A FULLY AUTOMATED BSIM PARAMETER EXTRACTION SYSTEM USING THE HP 4062 TEST SYSTEM

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ABSTRACT

A fully automated parameter extraction system for the BSIM (Berkeley Short Channel IGFET) model has been developed. This system incorporates the HP 4062 semiconductor parametric test system, the Electroglas 2001X automatic prober, and the HP 9836 computer. This version, BSIM-4062, based on previous BSIM extraction systems, greatly facilitates multiple die measurements and permits arbitrary device pad layout patterns.

April 27, 1986

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1. INTRODUCTION

For the integrated circuit manufacturer, the bottom line is cost. Cost has direct correlation to yield. If the IC process is good, then the yield depends on how well the engineer designs and analyzes his circuit. The design and analysis must include, among other things, nominal process parameters, process variations, and process limits. Breadboarding a circuit is no longer a viable method. The prevalent solution today is computer simulation.

Computer programs for simulating integrated circuits, such as SPICE, can only be as good as the mathematical equations that model the characteristics of the transistors. Because of the tremendous advancements in MOS technology over the last decade, Simple MOS transistor models that are adequate for the technology 10 years ago are no longer adequate today.

The BSIM model is a process-oriented MOS transistor model. Hence all process variations are taken into account. Even behaviors that are not well known mathematically can be accounted for because the BSIM model treats the devices on a macroscopic level.

The BSIM model is used in conjunction with the BSIM extraction system to ensure accurate simulation of MOS transistors. Using the BSIM extraction system, the user can get a set of accurate process parameters of his own wafer. In turn, these parameters are used in SPICE, where the BSIM model is implemented.

Several graduate researchers from UC Berkeley contributed to the extraction system. Brian Messenger developed the original CSIM (Compact Short Channel IGFET Model) program. Later CSIM became BSIM as Joe Pierret made enhancements to the program. Tony Fung implemented the subthreshold model. Peter Lee is currently developing the substrate current model. Hong June Park is currently developing the AC model. Min-Chie Jeng contributes on-going improvements. All of this research has been done using the HP 4145 parametric tester.

A more flexible and powerful BSIM extraction system is implemented using the HP 4062 semiconductor parametric test system. BSIM-4062 allows the user to extract BSIM parameters easily and painlessly. If the user wants more accuracy in modeling his devices or needs to know how the devices vary across the wafer, he has to measure many devices across many dies. Using BSIM-4145 with a manual prober, he will probably spend many, many hours at the probe station to get this data. The beauty of BSIM-4062 is that it is fully automatic: the user can set it up and leave. Measuring 100 devices across 20 dies becomes as easy as measuring 2 devices on 1 die.

Although the BSIM-4145 extraction system has an automatic mode, it is not very flexible because at most 4 probes can be used. Therefore, the devices must be lay out so that the 4 pads of any device are spaced identically as any other device. In other words, the 4 pads of any device must fit in an area that has the same dimensions as the 4 pads of any other device. Unfortunately, most of the popular layout patterns use shared pads; for example, a row of 10 devices may have 1 pad for gate, 1 pad for source, 1 pad for body, and 10 individual pads for 10 separate drains. This usually means the 4 pads of one device fit in an area that has different dimensions than another device. Thus the user must resort to the manual or semi-automatic mode using a manual prober. Of course, this conflict can be alleviated by laying out devices to suit the BSIM-4145 extraction system. Better still, BSIM-4062 extraction system adapts to arbitrary pad patterns.

This report describes everything needed to operate the BSIM-4062 extraction system. First, the individual pieces of equipment and their initial setup are described. Next, the reader is guided through the operation of the BSIM-4062 extraction program. Finally the differences between the BSIM-4062 and BSIM-4145 programs are given.

2. EQUIPMENT

The following equipment are required for the BSIM-4062 extraction system:

1. HP 4062 semiconductor parametric test system.
2. HP 9836 computer.†
   a. At least 1 Mbyte of memory (e.g., HP 9888A bus expander).
   b. HP Pascal system (2.0 or newer).
3. Electroglas 2001X automatic probe station (basic unit).
   a. Mounting hardware for the switching matrix. (The matrix, HP 4085, is part of the 4062 system.)
   b. Probe ring assembly

†The BSIM-4062 program uses the internal HP-IB interface card (interface select code 7) to talk to the 4062 system and the 2001X prober. The HP software uses different interface cards (interface select code 27).

3. Putting The System Together

3.1. Introduction - HP 4062

The 4062 system consists of 4 pieces of equipment - DC source / monitor (4141), switching matrix controller (4084), C-Meter / C-V plotter (4280), and switching matrix (4085). The 4062 system is shown in figure 3-1. Because the AC model for BSIM is not yet available, the C-Meter / C-V plotter is not currently used.

The switching matrix is to be mounted on top of the Electroglas 2001X prober. This matrix can have up to 48 sets of measurement pins. Each set consists of 3 pins that are joined together just before making contact to a device pad. Each set is one electronic board that plugs into the matrix.

The HP 9836 computer is used as the controller for the 4062. The BSIM-4062 program uses the internal HP-IB interface card (interface select code 7) to talk to the 4062 and 2001X. System software is included with every 4062 system.† The software consists of some very handy programs and subroutines that control the 4062 hardware. This software can be executed from a HP Basic system. The BSIM extraction program is, of course, written in Pascal so that the accompanied software is useless. This is unfortunate because there are some very useful high level routines that could not be incorporated into the BSIM extraction program. Therefore, all routines controlling the hardware are written in low level command strings. However, the 4062 manuals do not explain how the system can be controlled using HP-IB command strings. Thus the author deeply appreciates the 4062 software group at Hewlett Packard for providing the "HP-IB Operations" documents.

3.2. Introduction - Electroglas 2001X

The Electroglas 2001X (figure 3-2) is a very fancy automatic prober. Many options are available for the 2001X (e.g., automatic wafer alignment, multiple wafer handler,

†The HP software uses an external interface card (interface select code 27) to talk to the 4062.

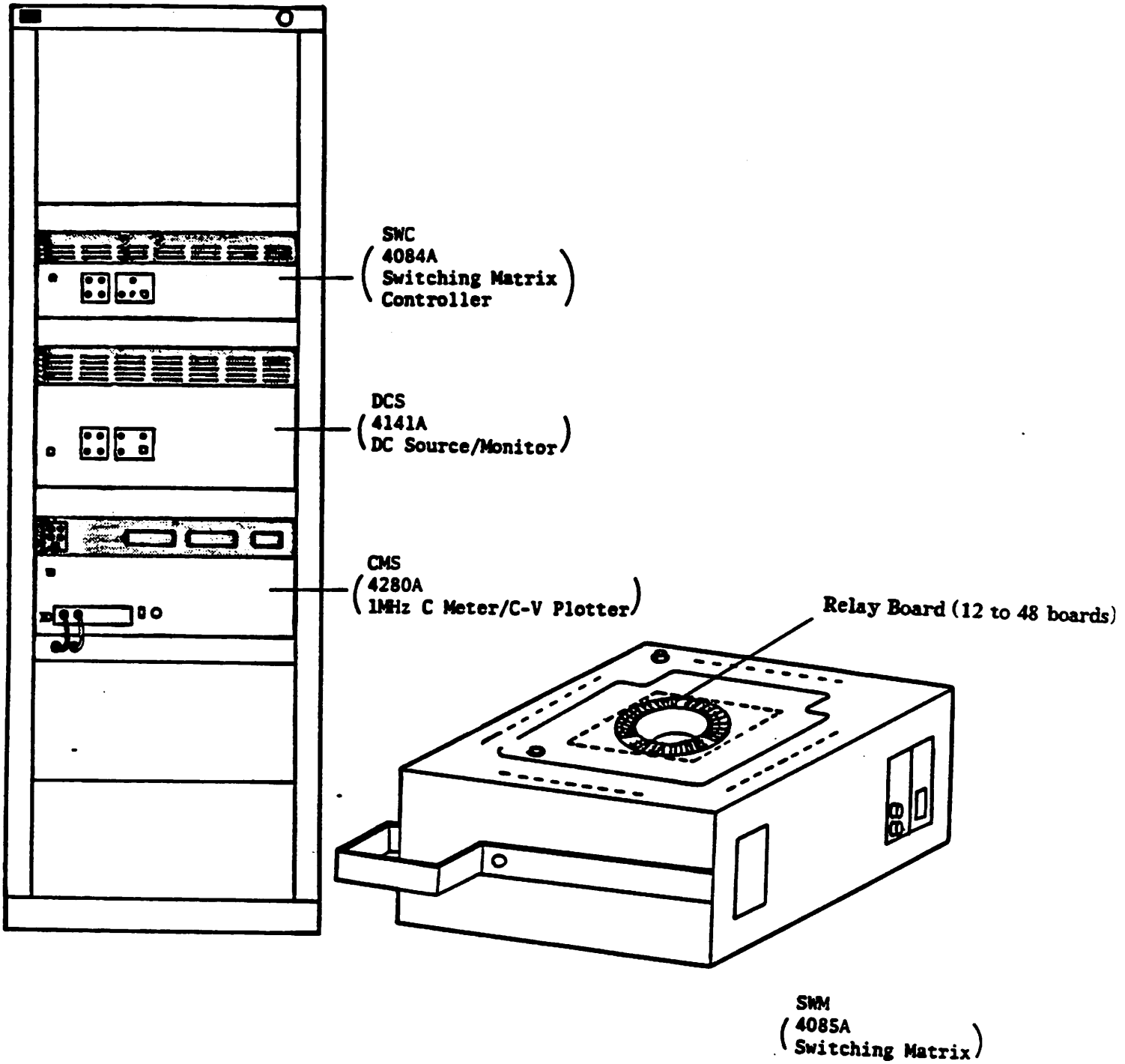
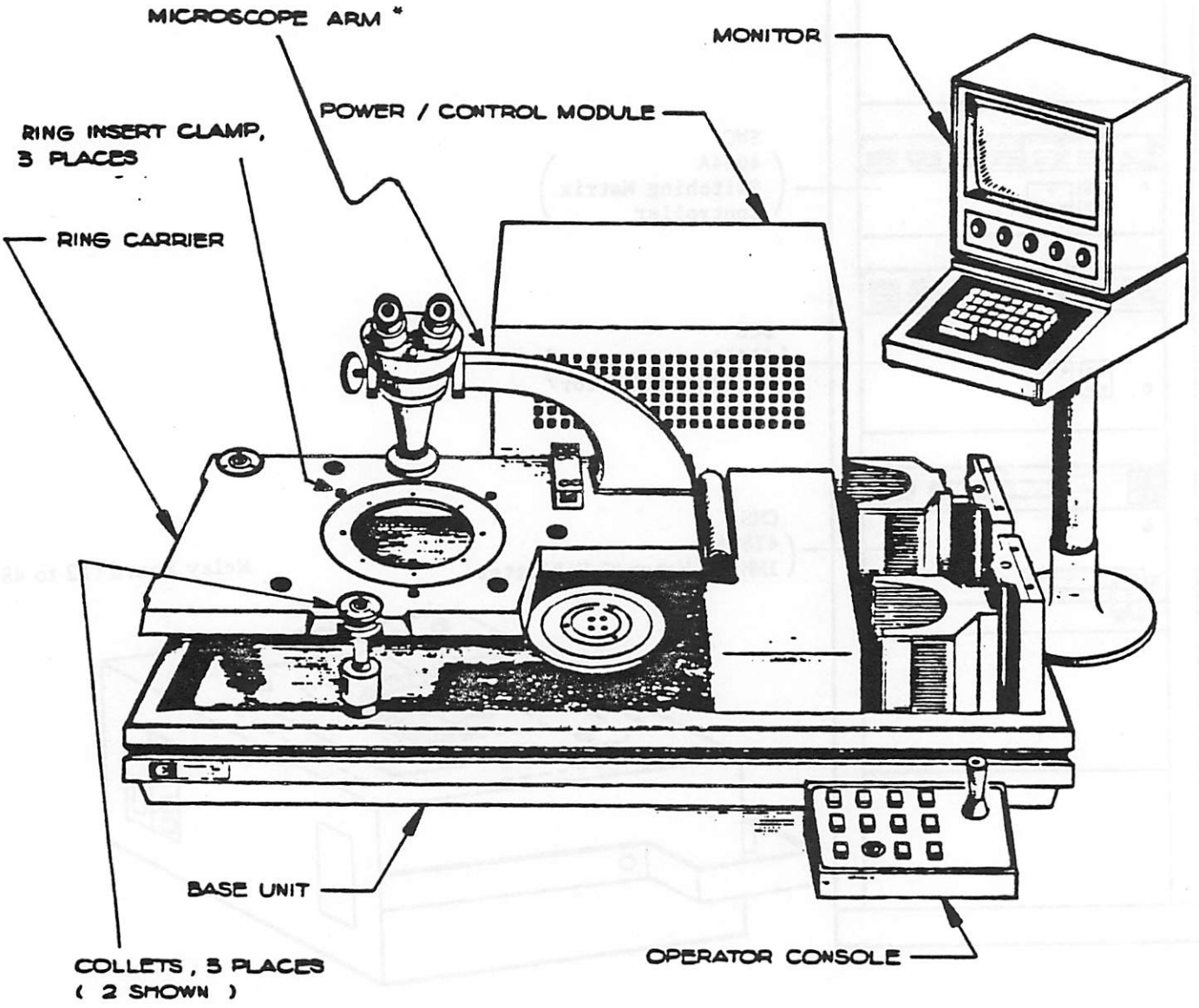


Figure 3-1. HP 4062 system (not to scale)



*The microscope arm shown will not work with the 4062 system. The arm must have a rectangular shape so that the microscope can reach over and into the matrix.

Figure 3-2. Electroglas 2001X Automatic Prober

camera, etc.), but none of them is incorporated into BSIM-4062. In fact, the basic unit has many functions, but only a few of them are used. A less expensive probe station would suffice, but the system here at Berkeley is donated by Electroglas.

3.3. Mounting The Matrix

The tricky part about setting up the BSIM-4062 extraction system is mounting the matrix onto the prober. Since many probers and test systems are available today, neither the 4062 manual nor the 2001X manual explains how to join the two together. This section describes how to put the two together to get one smoothly operating machine.

3.3.1. Mounting Hardware

Initially, the "high frequency mounting hardware" (figure 3-3) must be purchased from a vendor (e.g., Electroglas). The high frequency mounting hardware is just 2 aluminum rails and 2 swivel brackets which are bolted onto the ring carrier table. The matrix is mounted onto the 2 swivel brackets, thus allowing the matrix to be vertically rotated away from the table when not in use. When the switching matrix is in place, it rests upon the 2 rails. There are also 2 clips that come with the 4062 system which are bolted onto the end of the rails. The clips hold the matrix in place when it is being used.

3.3.2. Probe Ring Assembly

The probe ring assembly (figure 3-4) consists of a socket carriage, a probe ring socket, and a probe ring (interface ring). This set can be purchased from Electroglas or Probe technology. The assembly holds together the interface between the matrix and the device under test. The entire assembly fits into the middle of the ring carriage table.

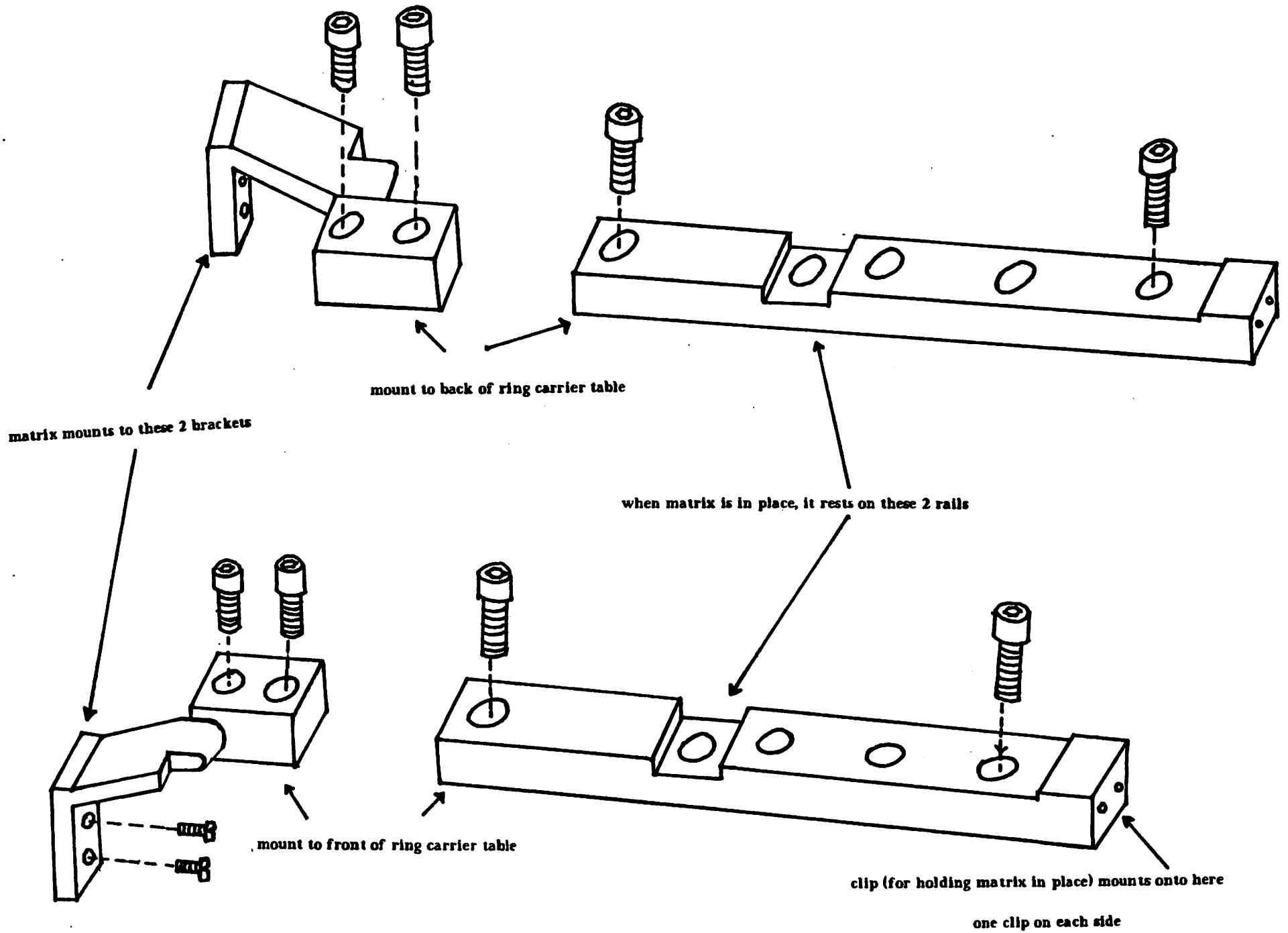


Figure 3-3. High Frequency Mounting Hardware

Probe Ring Assembly

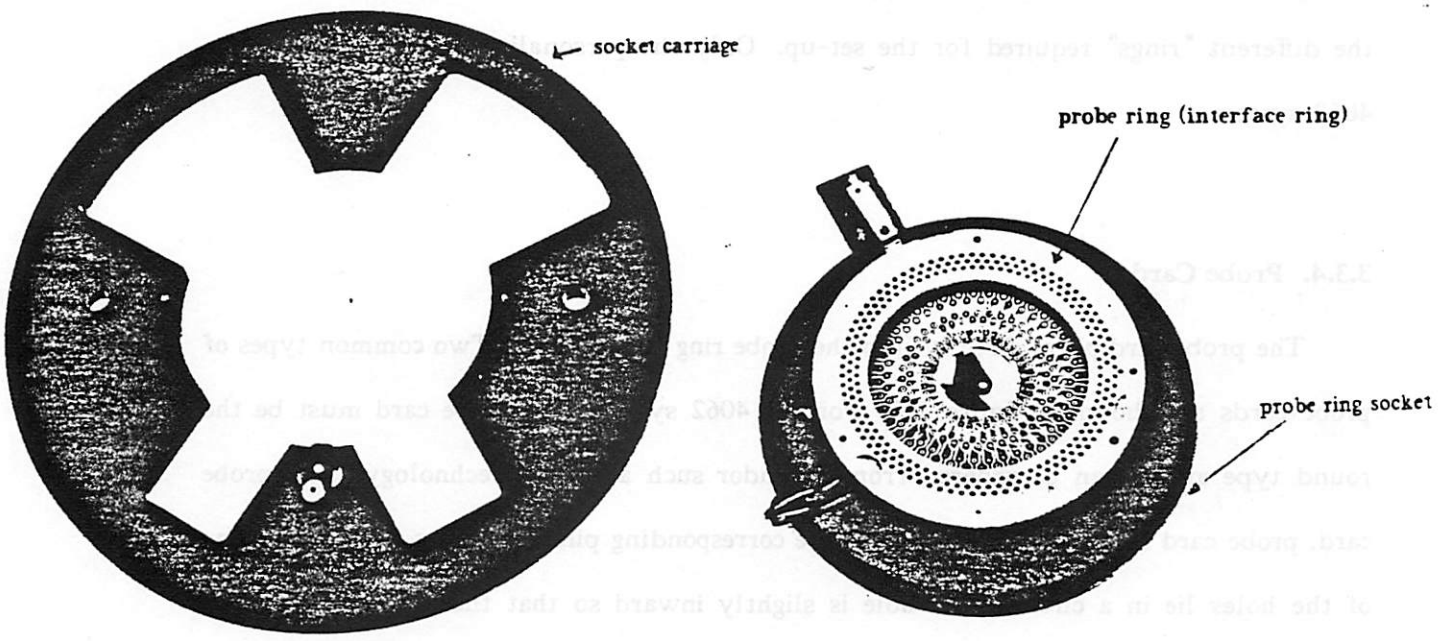


Figure 3-4. Probe Ring Assembly

3.3.3. Personality Ring

The "personality ring" (figure 3-5) is the main interface between the switching matrix and the probes. One personality ring comes with each 4062 system. The ring has 48 fingers, one for each set of pins in the matrix. Each set of pins consists of 3 pins - force, sense, and guard. By having separate force and sense lines for each connection, the ohmic drop along the cables between the device under test and the DC source/monitor (4141) is greatly reduced. When the matrix is in place, the pins lie directly on top of the personality ring. Each finger of the personality ring has an exposed trace where the corresponding set of pins lie; hence the force and sense lines are connected at the ring. A wire has to be soldered from the personality ring to the probe ring. Figure 3-6 shows all the different "rings" required for the set-up. Only the personality ring comes with the 4062 system.

3.3.4. Probe Card

The probe card plugs directly into the probe ring (figure 3-6). Two common types of probe cards are shown in figure 3-7. For the 4062 system, the probe card must be the round type and it can be ordered from a vendor such as Probe Technology. The probe card, probe card socket, and probe ring have corresponding pins and holes. All except one of the holes lie in a circle. This hole is slightly inward so that the probe card can be inserted, without force, only one way.

At this hole , there is a small arrow that normally indicates the front or back of a prober. When probes are ordered from a vendor and if the location (hole numbers) of the probes are not specified exactly, then the probe-maker will typically use the small arrow as an indication for lining up a row of probes. Since the arrow points to the front of the prober, this row of probes will be made parallel to the front edge.† The row of probes

†BE CAREFUL, this assumes you are using a 48 pin probe ring and probe card. If you have a 60 pin probe ring and probe card, as we do at Berkeley, then you will have to specify the location of the probes. Otherwise, the probes you ordered will be skewed by about 30 degrees, which is too much.

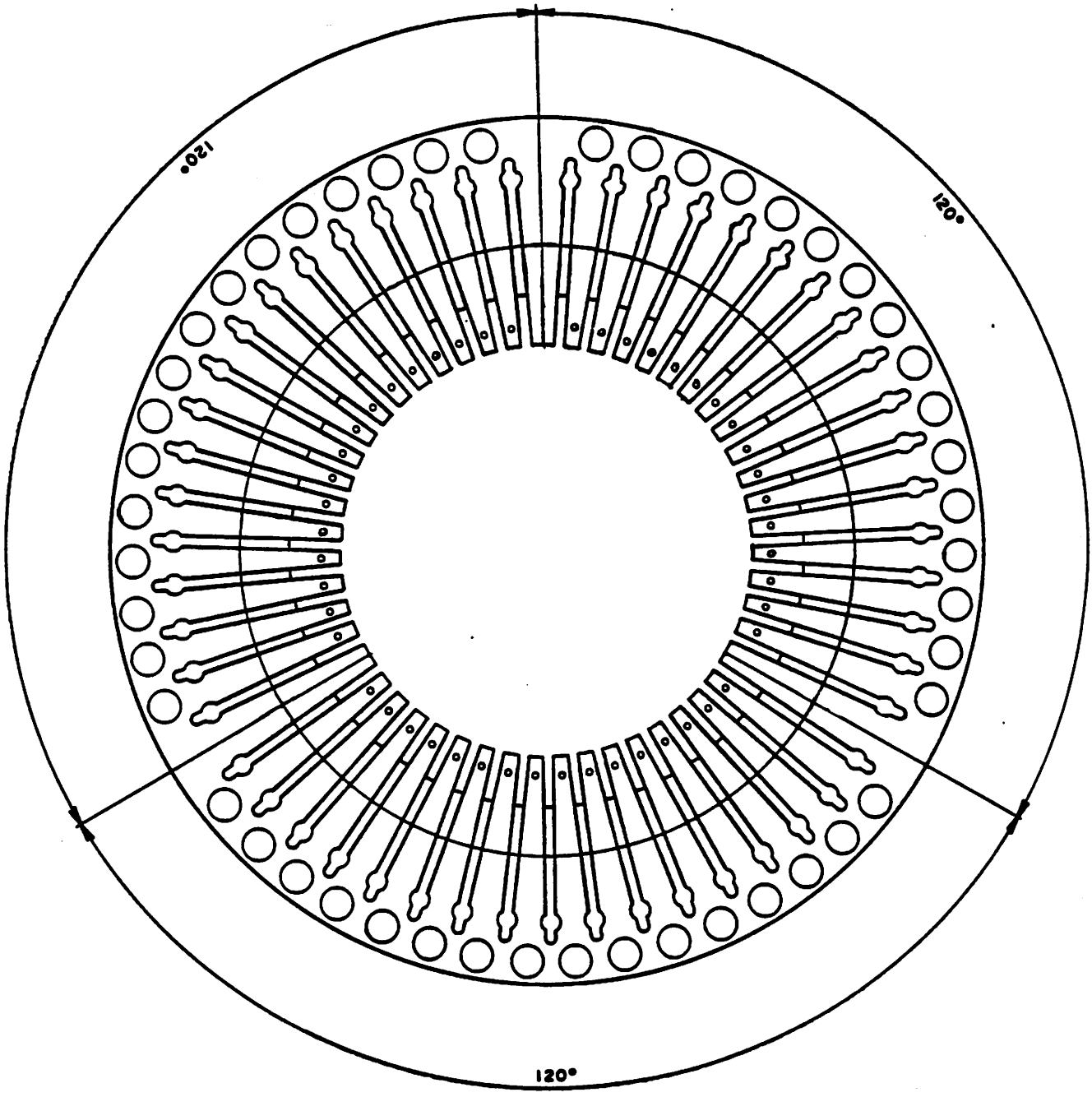


Figure 3-5. Personality Ring

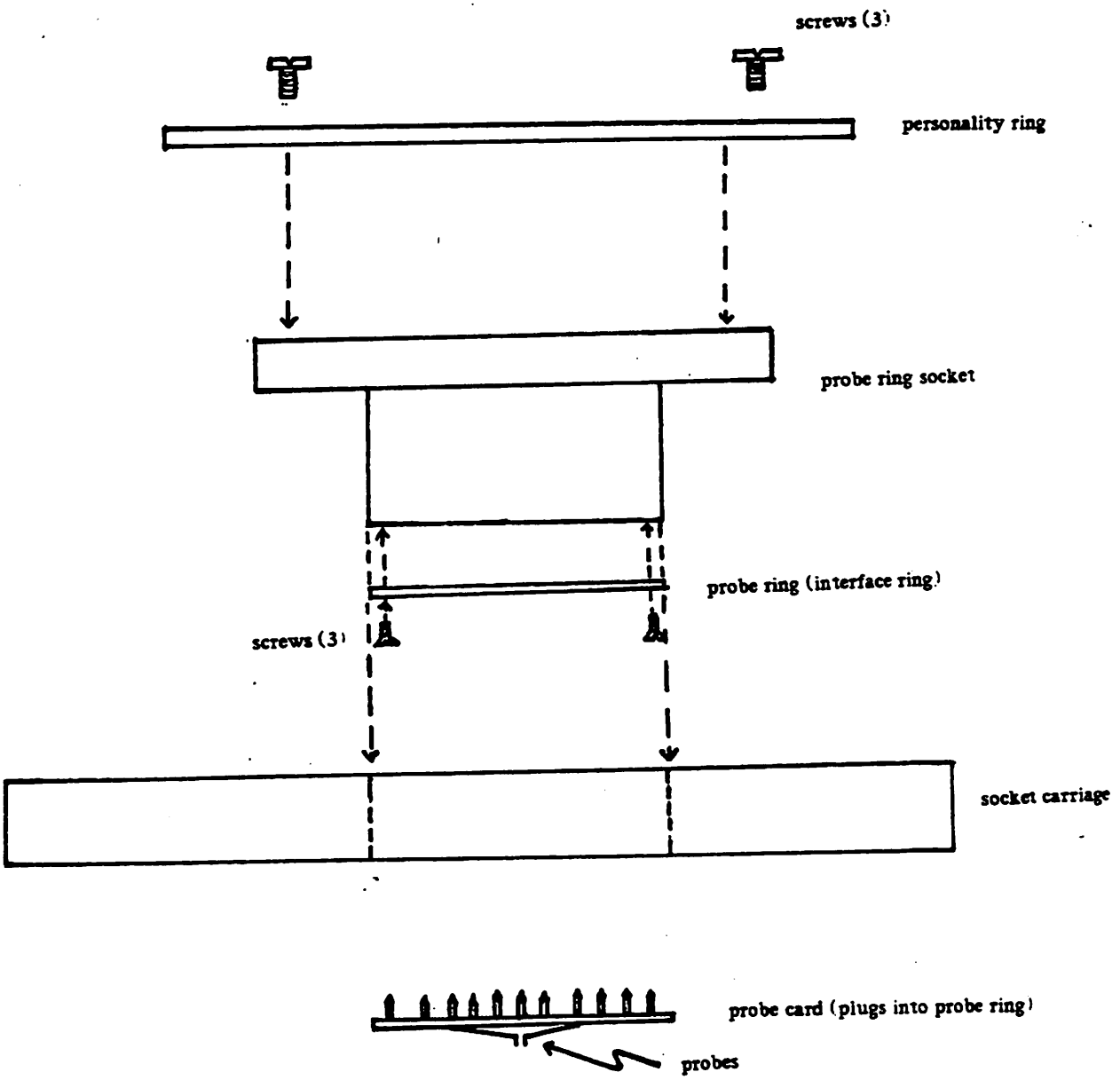
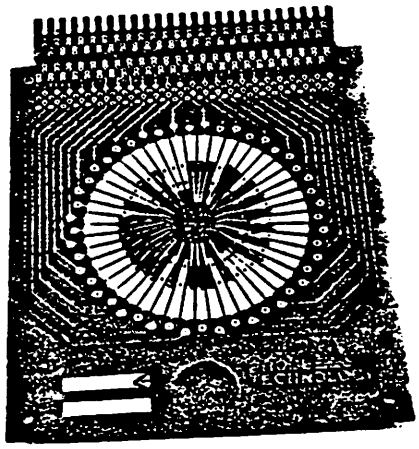


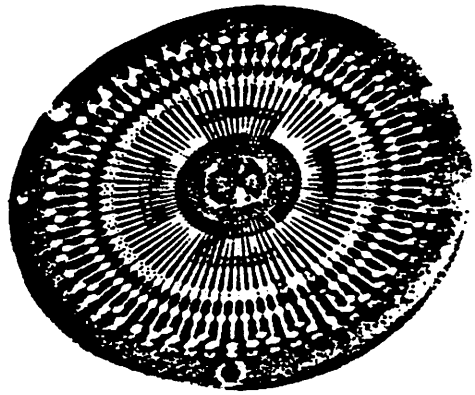
Figure 3-6. Set-up of the Required Rings (side view)

Blade Card



NOT FOR 4062 System

Epoxy Card



FOR 4062 System

Figure 3-7. Common Probe Cards.

must be parallel to the front edge because that is a requirement for automatic probing. Of course, there is some room for error. The prober has about 6 degrees of fine adjustment and the socket carriage can be rotated slightly. However, if the row of probes is skewed too much, then wafer alignment for automatic probing is not possible.

Edge sensors are not used and should not be part of the probe card. The edge sensor lets the prober know when the probes have reached the edge of a wafer. IC manufacturers typically use automatic probers to test an entire circuit (i.e. one die) and an edge sensor will rest on a scribe line when the probes are not at the edge of the wafer. However, the BSIM extraction system is typically used to measure individual devices and so probing is done within a die. Therefore, if the probe card has an edge sensor, it will rest somewhere inside the die and not on the scribe line. This will damage the die. Moreover, the BSIM-4062 program requires a prober file to describe the wafer and hence edge sensing is not needed.

3.3.5. Ring Carrier Table

The 2001X prober can be equipped for rectangular or round probe cards. These are called "blade card" and "epoxy card" by Probe Technology. The setups for the two are different. A rectangular probe card slides into a pair of card guides that mounts beneath the ring carrier table. This setup requires the table to be higher than that for a round probe card.

The 4062 system requires a setup for a round probe card. To convert from a rectangular card configuration to a round card configuration, the table has to be lowered by 0.7 inches. Otherwise, the wafer, which rests on the chuck, will not ascend high enough to make contact to the probes.

The ring carrier table can be adjusted by rotating the 3 collets (figures 3-2, 3-8). There are 10 marks on each collet; each mark is 0.005 inches. The 3 fat knobs lock the

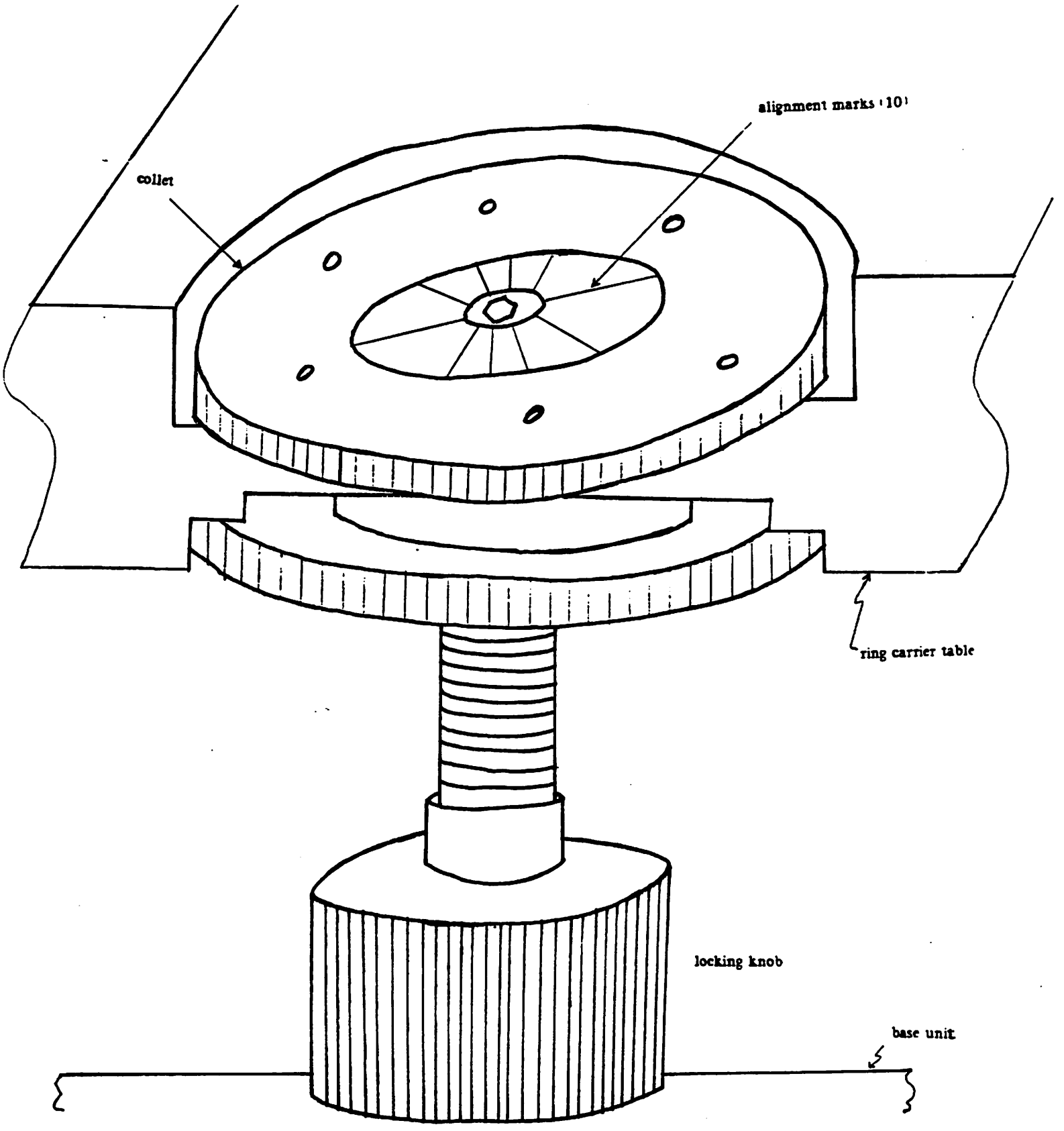


Figure 3-8. Expanded View of Collet

table in place; so they first have to be loosen. Then an Allen wrench is needed to loosen the screw on top of the collet. The collets can now be turned by hand. Fourteen clockwise revolutions will bring the table down by 0.7 inches (i.e., the height difference between the rectangular and round probe card configurations).

3.3.6. Microscope Arm

Because of the size of the switching matrix, the normal microscope arm, which has a gradual curvature (see figure 3-2), will not be tall enough to reach over and into the matrix. Therefore, a rectangular shaped arm must be used. It can be purchased from Electroglas.

4. Operating The BSIM-4062 Extraction System

4.1. Introduction

The BSIM-4062 extraction system can be operated in one of two measurement / extraction modes - automatic and single device. The single device mode seems incongruous with an automatic system and hence it is not the main purpose of BSIM-4062. However, the single device mode allows the user to check the system quickly and permits easy demonstrations. Moreover, this mode will generate 20 size-dependent BSIM parameters that can be used in the BSIM model for highly accurate simulations.

Nevertheless, the beauty of BSIM-4062 is evident in the automatic mode. In this mode, all the difficulties of automatic extraction inherent in the BSIM-4145 extraction system have been removed. The following sections describe how to run a BSIM-4062 extraction session.

4.2. Loading The Program

1) Boot up the 9836 with the HP Pascal system (2.0 or newer).
2) Set up a memory volume of 2500 blocks (fewer if less memory is available).
3) If not already done, load into the Pascal library the following modules:

   - hpib_0
   - hpib_1
   - hpib_2
   - hpib_3
   - general_0
   - general_1
   - general_2
   - iodeclarations
   - iocomasm
   - dgl_lib

4) Load bsim.CODE into memory volume.
5) Execute bsim.CODE. It will wait for input.

Other than loading the library, the above steps can be put into the AUTOSTART file

so that all these steps will be done automatically upon power-on. An example of an AUTOSTART file is shown in figure 4-1.

4.3. Setting Up The Electroglas 2001X

1) Plug in the appropriate probe card.

2) Turn ON the prober.

3) If the monitor is not already ON, turn it ON.

4) Answer the questions on the monitor or else wait for default response from prober. It takes about 30 seconds for a default response.

Type Message Plus Enter=> **Enter key**
Wait for Pattern Rec I/O Test... **Wait about 30 seconds**
Rom Test? **Y**
Repeat Test? **Enter key**

5) Now you will see ****XY MOTOR BLANK**** at the bottom of the screen. The stage is now floating on the platform. Pull it to the front right corner against the 2 edges.

6) Press the button inside the left side of the joystick control panel (figure 4-2). **THE PROBER WILL NOT RESPOND UNTIL YOU PRESS THIS BUTTON.**

7) Pull out the vacuum level at the front panel. A hissing noise indicates compressed air coming into the probe station.

8) Using the monitor console keyboard (figure 4-3), set up the prober as shown in figures 4-4b to 4-4e. Of course, the parameters *DIE*, *WAFER DIAMETER*, *ZUP LIMIT*, and *Z DOWN LIMIT* will depend on your particular wafer. To get any of the screens, press the appropriate key on the monitor console keyboard.

9) Place the wafer on the chuck and press [VAC] and [LAMP]. The device pads must be roughly parallel to the probes.

10) Align the wafer (i.e., rotate the chuck until the device pads are perfectly parallel to the probes). The following section describes more fully how to align the wafer.

11) After the wafer is aligned, use the joystick to move the wafer so that the probes are directly over the pads of the devices to be tested. The die should be the origin die and the devices should be the origin row of devices within that die, as specified in the prober file.

```
7-APR-86
12:00
M#45
2500
30
FP#45:
Q
p#11:EDITOR.
p#11:FILER.
FF#11:LIBRARY
RAM:LIBRARY
F#11:bsim.CODE
RAM:bsim.CODE
F#11:probe.TEXT
RAM:probe.TEXT
Q
WBRAM:LIBRARY.
SRAM:
DRAM:
Q
P#11:COMPILER.
```

Figure 4-1. AUTOSTART FILE

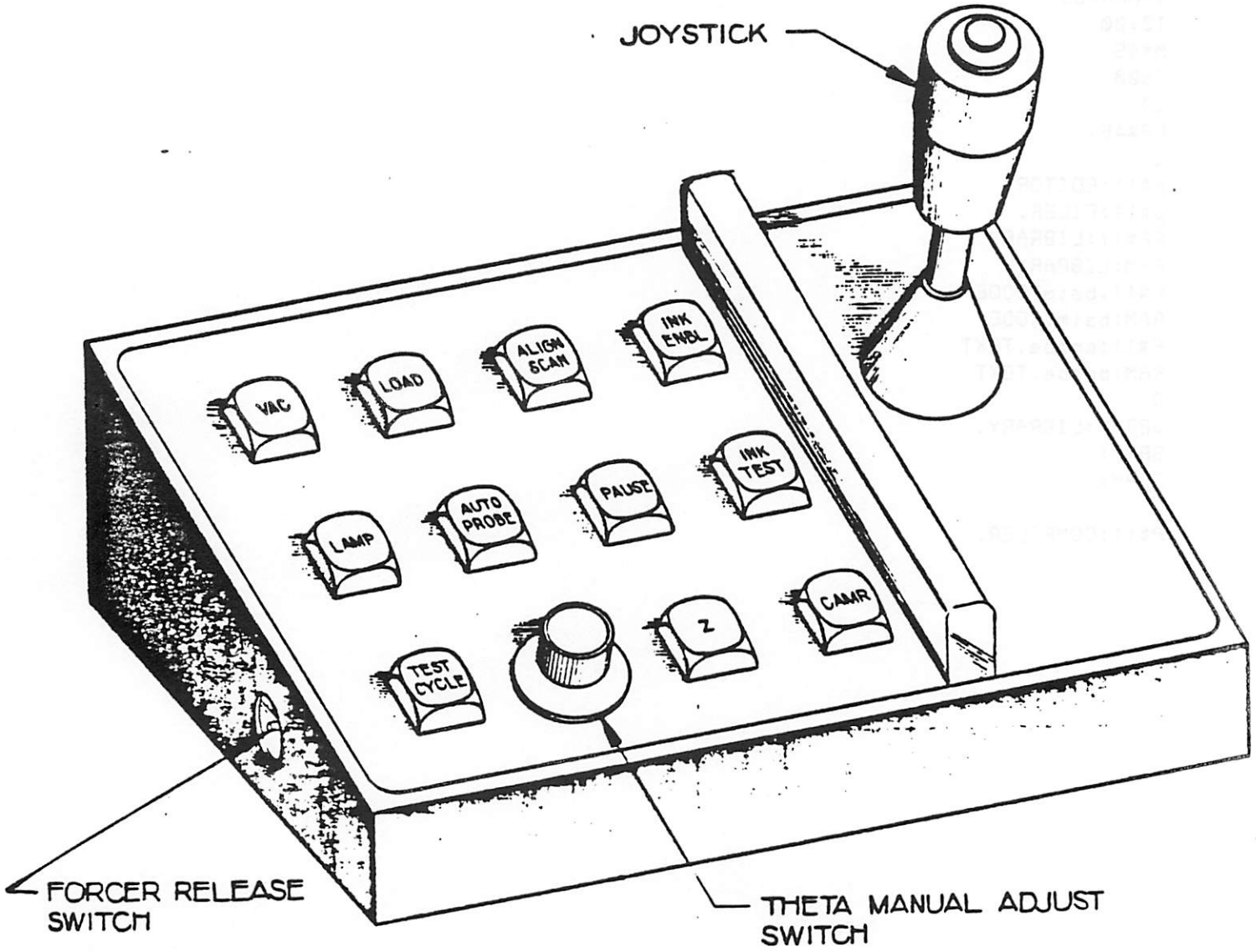


Figure 4-2. Operator Control Console

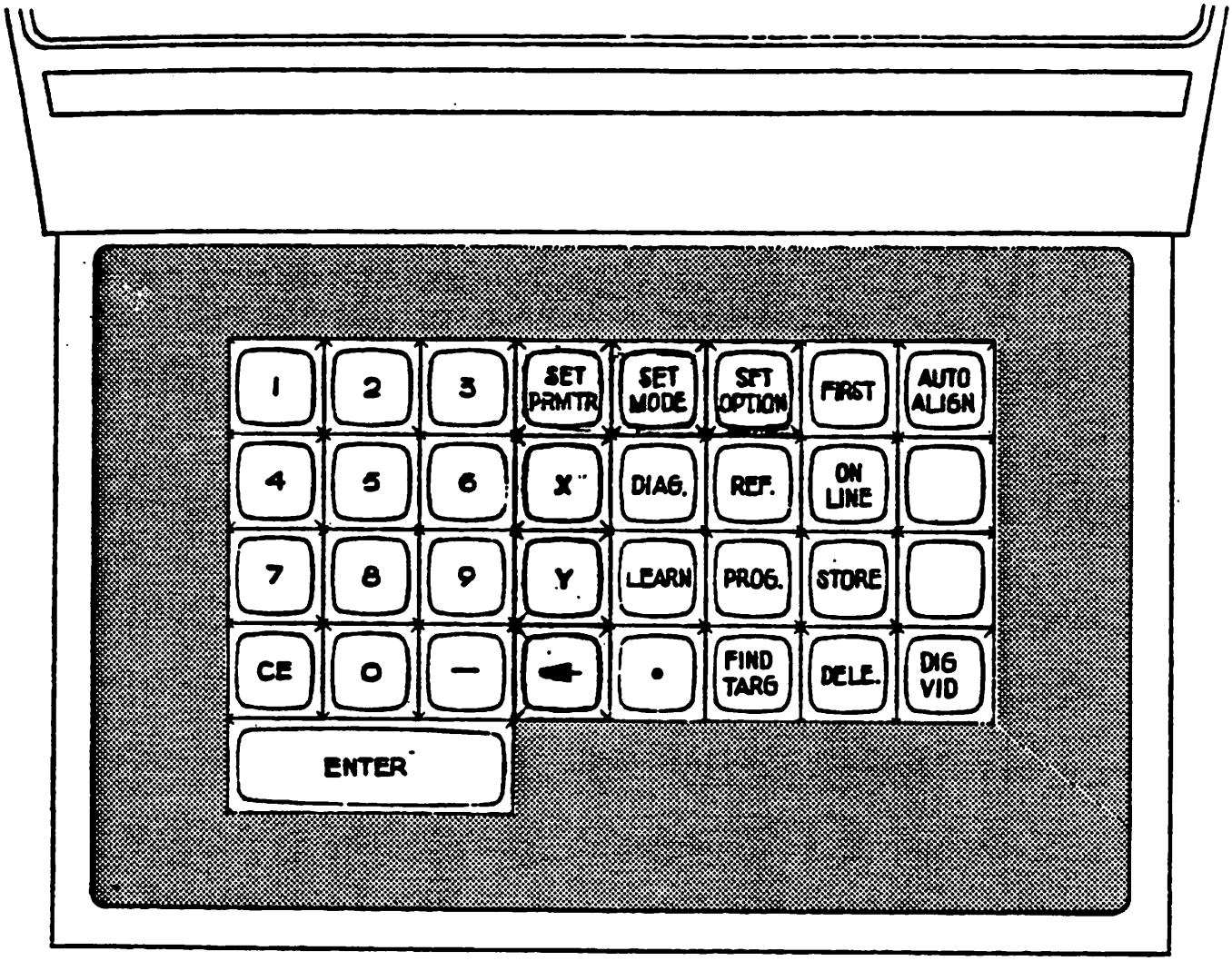


Figure 4-3. Monitor Console Keyboard

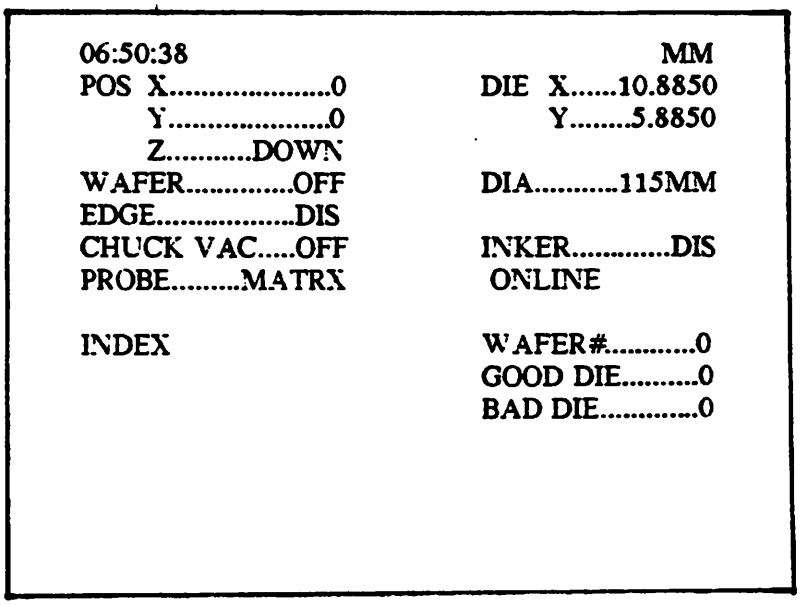


figure 4-4a. Default Display

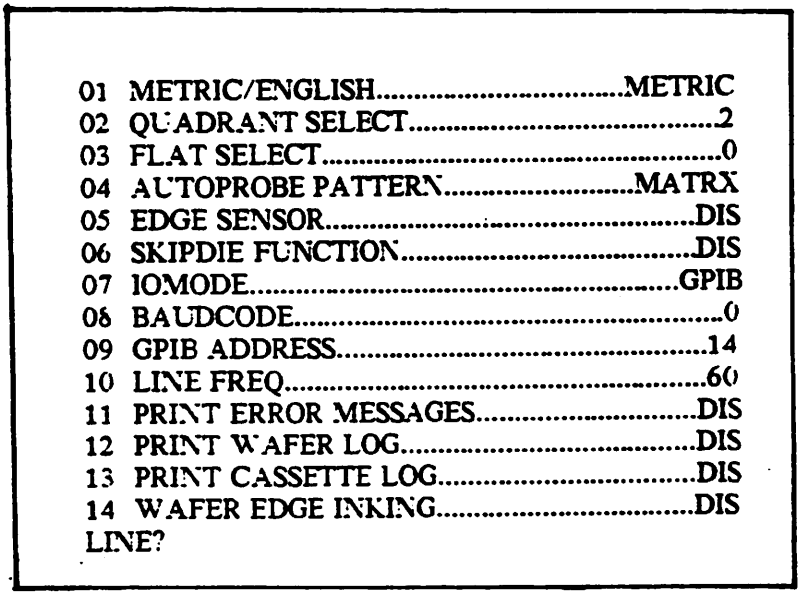


figure 4-4b. SET MODE Display

```
01  DIE                    X.....10.8850   MM
                           Y.....5.8850    MM
02  PRESET                 X.....0 Y.....0 DIE
03  MATRIX                 X.....0 Y.....0 DIE
04  INKER OFFSET.....0 DIE
05  TURNAROUND.....0 DIE
06  WAFER DIAMETER.....115 MM
07  Z OVERTRAVEL.....0.00 MILS
08  Z CLEARANCE.....0.00 MILS
09  Z UP LIMIT.....294 MILS
10  Z DOWN LIMIT.....284 MILS
11  Z ALIGN.....200 MILS
12  NEXT PAGE

LINE?
```

figure 4-4c. SET PRMTR Display

```
                        SETPARM  PAGE #2
01  ALIGN SCAN VEL.....300 MPS
02  REPROBE LIMIT.....0 DIE
03  SET RUNTIME DISPLAY CLOCK









LINE?
```

figure 4-4d. SET PRMTR Page 2 Display

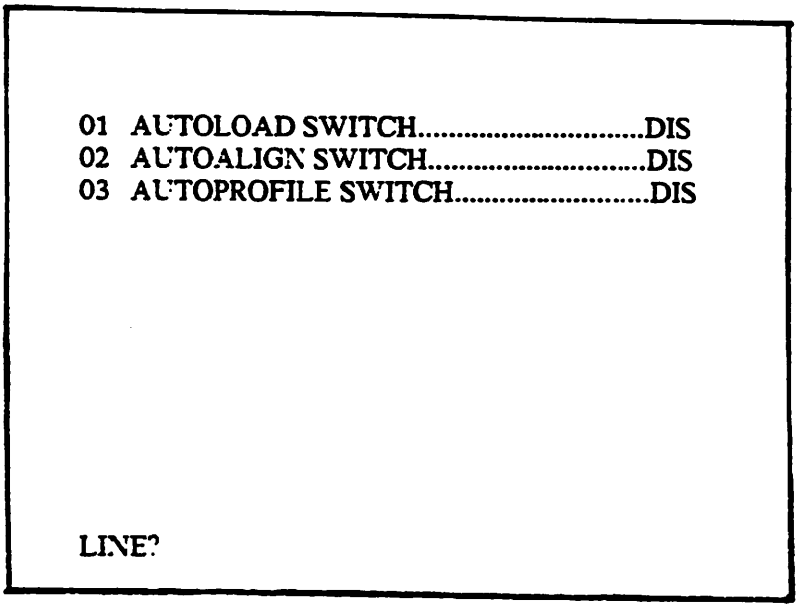


figure 4-4e. SET OPTION Display

12) Press [Z] to raise the wafer to the probes. You may have to reset the *Z UP LIMIT* parameter (see figure 4-4c) in the [SET PRMTR] mode. If the probes are not touching the pads, slightly increase *Z UP LIMIT* and then press [Z] twice (once to lower wafer, once to raise it). When you see that all the probes are barely touching all the pads, increase *Z UP LIMIT* by 0.5 to 1.0 MILS to provide some overdrive. Too much overdrive will wear out the probes and the pads very quickly.

4.3.1. Aligning the Wafer

Aligning the wafer will take some practice. Alignment is done when the wafer (actually the stage holding the wafer) is moving from side to side under the probes.

The idea is to rotate the wafer until the device pads are parallel to the probes. When they are not parallel, then even if the probes are directly over the pads at one end of the wafer, the probes will not be directly over the corresponding pads at the other end of the wafer (figure 4-5).

Initially, the prober should be setup similar to the one shown in figures 4-4b to 4-4e. Some prober parameters will depend on the particular wafer being used. The *WAFER DIAMETER* parameter tells the prober how far the stage should move before reversing the direction of movement. The *ALIGN SCAN VEL* parameter ([SET PRMTR] , page 2) sets how fast the stage will move. Three hundred MPS is a reasonable speed for wafer alignment.

4.3.1.1. Alignment Instructions

Refer to the operator control console (figure 4-2) while reading the following instructions. The rectangularly enclosed words below represent keys on the joystick panel.

1) Follow steps 1 to 9 of section 4.3.

2) Press [ALIGN SCAN] .
This causes the stage to move from the right front corner to the right of the probes.

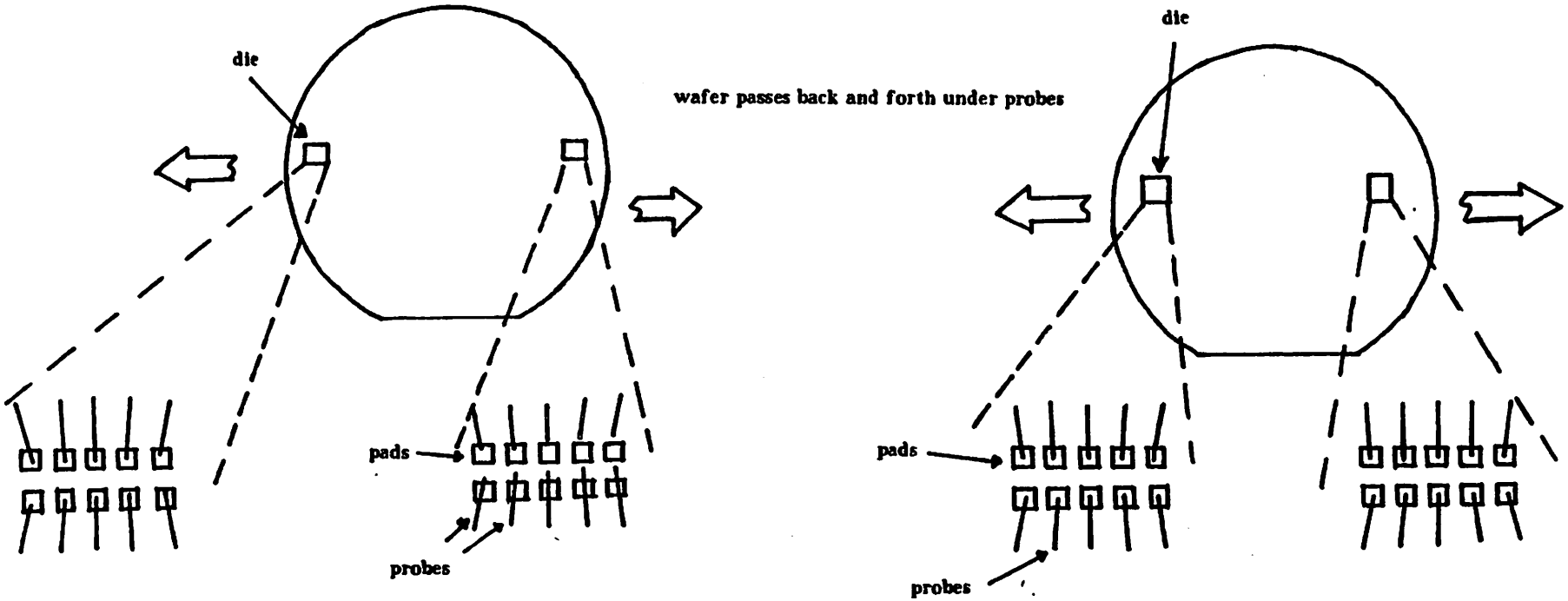


Figure 4-5. Wafer Alignment

3) Press [PAUSE].
The stage moves to the left of the probes.

4) Turn the joystick until you see "scan" at the lower left column of the monitor. Use the joystick to move the wafer until you see some linear pattern below the probes. You will use this pattern in step 6) to judge whether the probes are parallel to the pads or not. The pattern can be the pads of a row of devices or the edge of the dies.

5) Press [PAUSE].
The stage now moves back and forth. Successively pressing [PAUSE] causes the stage alternately to stop and start moving.

6) As the wafer is moving, look under the microscope and compare the probes to the pattern. If they are not parallel from one end of the wafer to the other, then turn the theta knob, causing the wafer to rotate. Play with the knob until the probes are parallel to the pattern.

7) When you are confident that they are parallel, use the joystick to move the pads to directly underneath the probes. You can use the joystick to move it fast (scan), slow (jog), or fixed (index). How far the stage moves in index mode depends on what the X and Y die sizes are set to (see figure 4-4c).

4.4. Running the BSIM-4062 Program

The best way to explain how something works is by example. So in this section, the "how to run BSIM-4062" is demonstrated by an example. The wafer used is from an CMOS process, but for simplicity only the NMOS transistors are used. The devices have the NBS (National Bureau of Standards) standard pad layout pattern (figure 4-6). The 9836 monitor displays from the program are shown in figures 4-9a to 4-91. Figure 4-9a shows the main menu. The valid operating modes are fully automatic measurement and extraction, single device measurement and extraction, and other options. The modes of operation are described below.

4.4.1. Fully Automatic Mode

4.4.1.1. Prober File

For the fully automatic mode, a prober file must have been created prior to running the program. The format for the BSIM-4062 prober file is different from the format for the BSIM-4145 prober file. The prober file is diveded into 2 parts. The first part is identical for the 2 programs. The second part is very different.

The first part of the prober file (figure 4-7) contains information about the wafer. Lines 1 and 2 are the width and length of a die, respectively. Next there is a 20X20 array representing the dies on the wafer. The upper left corner of the array is location (1, 1). The dies on an actual wafer can be (and probably will be) a subset of the 20X20 array. The "X" indicates the origin die (i.e., the first die to be probed). When the program begins execution, the probes must be on this die. All locations marked with a "1" will be probed. All locations marked with a "0" will not be probed. In the example (figure 4-7), the locations of the dies to be probed are (4, 5), the origin die location, and (5, 5).

The second part of the prober file contains information about the die. This information is used for every die to be probed. Figure 4-8 shows 5 rows of devices within a die.

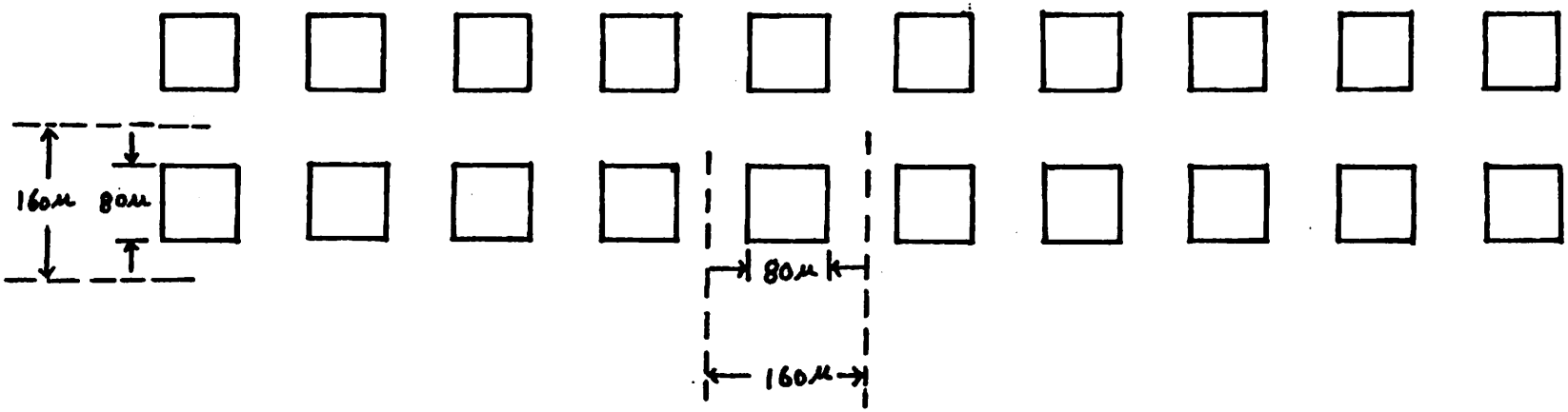


Figure 4-6. NBS Device Pad Layout

```
10885                    {Die size (microns) in the x direction}
10885                    {Die size (microns) in the y direction}
00000000000000000000
00000000000000000000  {This is the 20X20 array to designate which}
00000000000000000000  {    dies are to be tested.}
00000000000000000000
000X1000000000000000
00000000000000000000
00000000000000000000  {The location marked "X" is the origin die.}
00000000000000000000  {    which means the probes have to be on}
00000000000000000000  {    this die when the program begins.}
00000000000000000000  {The locations marked "1" are to be tested.}
00000000000000000000  {The locations marked "0" are not touched.}
00000000000000000000
00000000000000000000  {The upper left corner of the array is location}
00000000000000000000  {    (1,1). X increases to the right.}
00000000000000000000  {    Y increases to the left.}
00000000000000000000
00000000000000000000  {The origin die in this example is (4,5).}
00000000000000000000
00000000000000000000
00000000000000000000

{The following portion describes the devices within a die.}
{Any line not beginning with an m, d, w, l, d, e, or p will be ignored.}
{A row of devices must begin with mx and my.}
{A row of devices is defined as all devices that concurrently have probes}
{    on their pads. In other words, if the prober has to move to get to}
{    get to a device, then the information for this device must begin with}
{    a new mx and my.}

mx=0          {This is the origin of every die. mx and my are in microns}
my=0          {mx and my are specified once for each row of devices}
dv1           {device #1 of the row of devices at mx=0, my=0}
w=5           {width=5 microns}
l=10          {length=10 microns}
dt=1          {device type. -1 for PMOS, 1 for NMOS}
ed=1          {enhancement (ed=1), depletion (ed=-1), or zero-threshold (ed=0)}
pg=10         {matrix pin number 10 is connected to the gate}
pd=44         {matrix pin number 44 is connected to the drain}
ps=6          {matrix pin number 6 is connected to the source}
pb=48         {matrix pin number 48 is connected to the body}
dv2           {device #2 of the row of devices at mx=0, my=0}
w=5
w=7
dt=1          {NMOS device}
ed=1          {enhancement device}
pg=14
pd=40
ps=6
pb=48
dv3           {device #3 of the row of devices at mx=0, my=0}
w=5
l=4
```

Figure 4-7. Prober File

```
dt=1
ed=1
pg=24
pd=30
ps=6
pb=48
dv4             {device #4}
w=5
l=5
dt=1
ed=1
pg=20
pd=34
ps=6
pb=48
                {a blank line for readability. though not necessary}
mx=0            {starting a new row of devices}
my=320          {this row is 320 microns below the origin row}
dv1             {device #1 of the row of devices at mx=0, my=320}
w=10
l=5
dt=1
ed=1
pg=20
pd=34
ps=6
pb=48

mx=0            {starting a new row of devices}
my=640
dv1             {this line is needed even though it's the only device in the row}
w=20
l=5
dt=1
ed=1
pg=20
pd=34
ps=6
pb=48

mx=0            {starting the 4th row of devices}
my=960          {this row is 960 microns down from the origin row}
dv1
w=50
l=5
dt=1
ed=1
pg=20
pd=34
ps=6
pb=48
                {THE LAST LINE MUST BE A BLANK LINE!}
```

Figure 4-7. Prober File (continued)

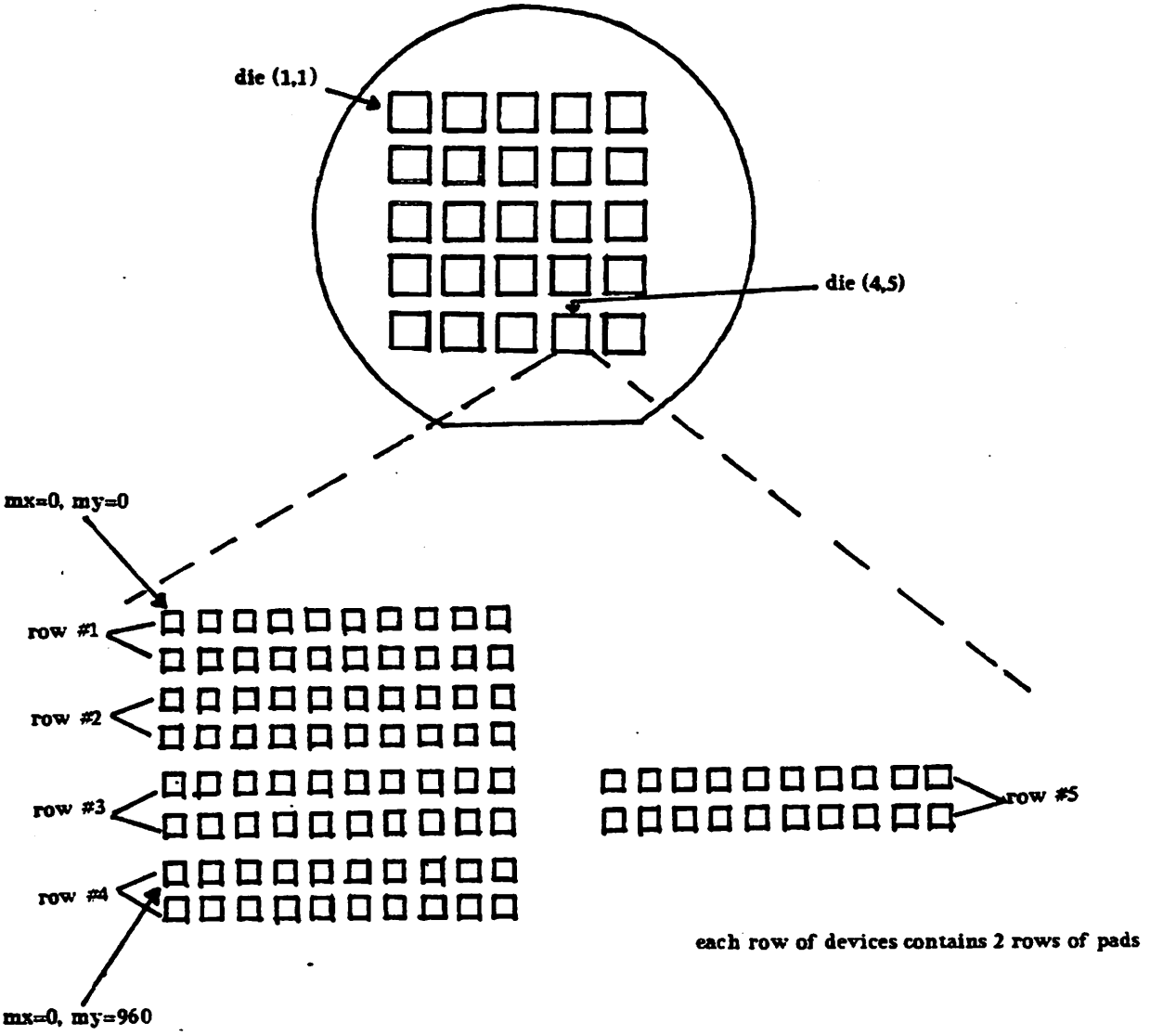


Figure 4-8. Rows of Devices Within One Die

Each row of devices contains 2 rows of pads. According to the prober file (figure 4-7), 4 of these rows will be probed. The mnemonics in the prober file will now be explained.

Mx and my are the x and y coordinates (in microns) of a row of devices. In the prober file, information for each row is separated by a blank line, although this is just for readability and is not necessary. New mx and my coordinates indicate a new row so that all transistors in one row have the same mx and my. When starting the program, the probes must be at the first row (i.e., at mx=my=0). Subsequent coordinates are relative to the first row. In figure 4-7, row 3 has the same mx but my is 960 microns away.

The device number, dv#, is a separator for the devices in a single row; dt is the device type (1=NMOS, -1=PMOS); ed is for an enhancement (ed=1), depletion (ed=-1), or zero-threshold (ed=0) device; w is the width in microns and l is the length in microns.

The number of the matrix pin† connected to a device terminal depends on how the user sets up his personality ring (i.e., which finger of the personality ring is connected to which probe); pg is the number of the pin connected to the gate; pd is the number of the pin connected to the drain; ps is the number of the pin connected to the source; pb is the number of the pin connected to the body. The program will use the pin numbers to connect SMU1 (source / measurement unit #1) to gate, SMU2 to drain, SMU3 to source, and SMU4 to body. (The 4141 has 4 SMUs just like the 4145.) If the back side of the wafer is used for the body terminal, then a cable connecting the chuck to a dedicated matrix pin must be installed. The number of this pin still has to be entered for every device into the prober file.

In the example (figure 4-7), device number 2 of the first row of devices is an NMOS enhancement transistor with dimensions W/L = 5/7. Its gate is connected to matrix pin #14, drain to matrix pin #40, source connected to matrix pin #6, and body to matrix pin #48.

† One pin number refers to all 3 pins (force, sense, and guard) of a connection.

THE LAST LINE IN THE PROBER FILE MUST BE A BLANK LINE! Otherwise, an ambiguous system error will be reported.

4.4.1.2. Automatic Mode Inputs

The displays for automatic mode inputs are shown in figure 4-9b and 4-9c. Most of the prompts are self-explanatory. The input to "Prober File=?" must be the full name (i.e., including any extensions like ".TEXT") of the file.

The second page gives the user the option to see I-V curves or BSIM parameter curves at the end of each die. If "Y" is entered, then the program stops at the end of each die to ask the user if he wants to enter the graphics mode. If "N" is entered, then the program executes until measurement and extraction on all dies are completed. At that point, the user can still view the I-V curves of any die that has been measured.

4.4.1.3. BSIM Extraction Status

Figure 4-9d shows the "BSIM EXTRACTION STATUS" display. The program is executing only above threshold measurement and extraction, so that the subthreshold parameters N0, X2NB, and X3ND do not have any values. These 20 parameters are only for the device being measured and they will be used later to calculate a set of 63 size-independent parameters. The 63 parameters will then be put into the process file. Each die measured will have its own set of parameters in the process file.

4.4.1.4. BSIM Parameter Graphs

Figures 4-9e, 4-9f, and 4-9g show the BSIM parameter graphics displays. The user can choose to plot any of the BSIM parameters versus W or L. The 6 possible device types are NMOS enhancement, NMOS depletion, NMOS zero-threshold, PMOS enhancement,

PMOS depletion, and PMOS zero-threshold. Figure 4-9e shows only the NMOS enhancement since it is the only device type measured for this example. Figure 4-9h is a plot of 1/BETA0 versus W.

4.4.1.5. Preparation for I-V Graphics

When the program enters the I-V graphics mode, the user must provide some information about the device he wants to view. The X and Y die positions (figure 4-9i) must be that of a die which has been measured. Because the program can enter into the I-V graphics mode after the extraction of every die, a die specified in the prober file but not yet measured can not be checked in the I-V graphics mode. In other words, the die must have its set of parameters in the process file. The default die is the one just measured. The user simply hits [ENTER] to get the default die.

There are 6 possible device types (NMOS enhancement, NMOS depletion, PMOS enhancement, etc.), but the program will accept only the types that have been measured.

4.4.1.6. BSIM I-V Graphics Menu

The user has to enter the type of graph wanted (figure 4-9j). If a measured data mode is entered, the device selected will be measured. If that device is listed in the prober file, then the prober stage is automatically moved so that the probes are on that device and all pin connections are made automatically. If the device is not listed in the prober file (i.e., no measurement or extraction done on that device), then the prober stage is moved so that the probes are on top (not touching) of the correct die; the user now enters the number of the pins connected to gate, drain, source, and body, and then manually places the probes on the desired device.

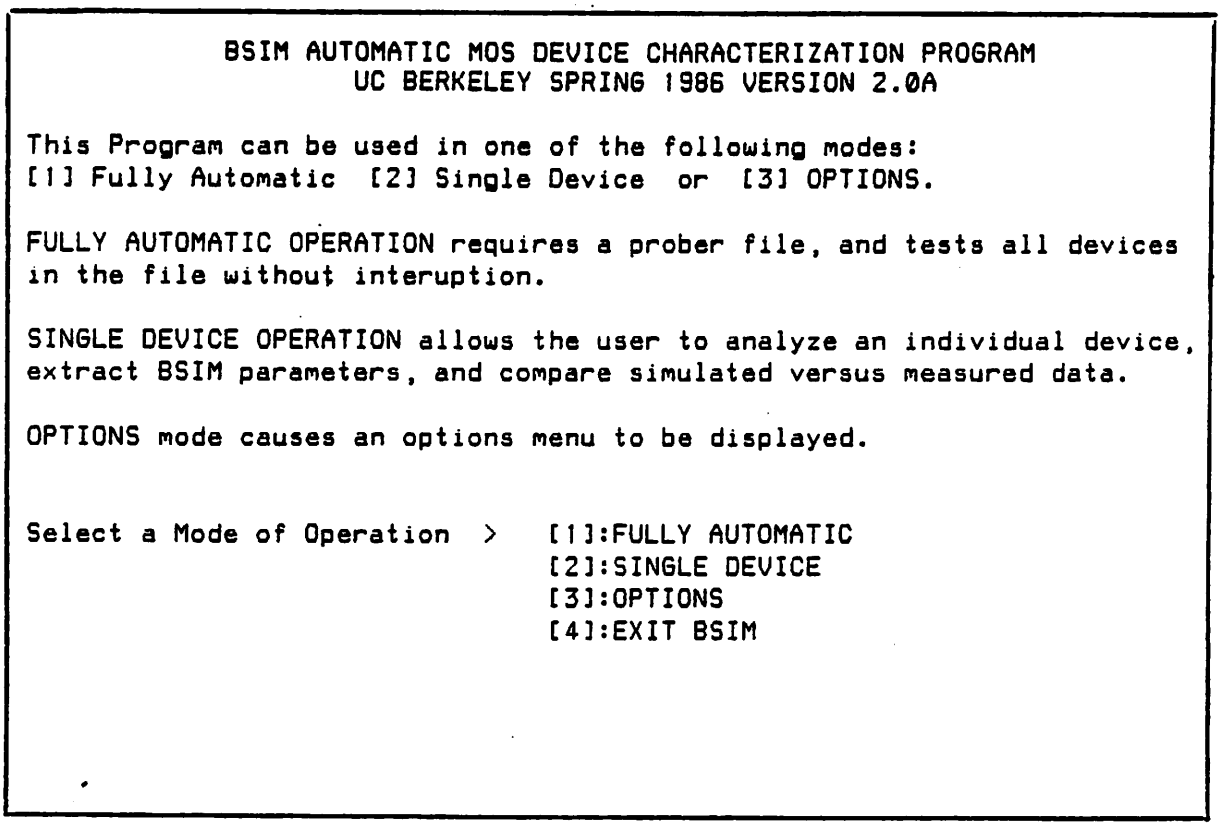


Figure 4-9a. BSIM Main Menu

```
            ***AUTOMATIC OPERATION***

Process Name=CMOS
Lot=500
Wafer=XXX
Date=4-20-86
Operator=BSIM SLAVE
Output File=bsimauto.TEXT
VDD(volts)=5.00
TEMPERATURE(deg. C)=27.00
TOX(angstroms)=298.00
SUBTHRESHOLD measurement and extraction?  (Y/N)  >NO
Prober File=?  >probeny.TEXT
```

Figure 4-9b. Automatic Mode Inputs (part 1)

```
          *** CONTINUE AUTOMATIC MODE INPUTS ***


At the end of each die, you have the OPTION of viewing the I-V graphics.
If YES, then you will be prompt at the end of each DIE for whether you
want to see I-V graphics or not.
If NO, then you will be prompt only at the end of the WAFER.
You also have the option of viewing the BSIM PARAMETERS vs W or L at
the end of each die.


At the end of EACH DIE, would you like to view

          BSIM PARAMETER vs W or L PLOTS?  (Y/N)  >YES
          I - V CURVES?  (Y/N)  >YES


Probing Instructions
     The prober should be on, and the probes should be down
on the starting die, starting position.  (see prober instructions)
HIT a "C" for changes, or any other key to start.  >
```

Figure 4-9c. Automatic Mode Inputs (part 2)

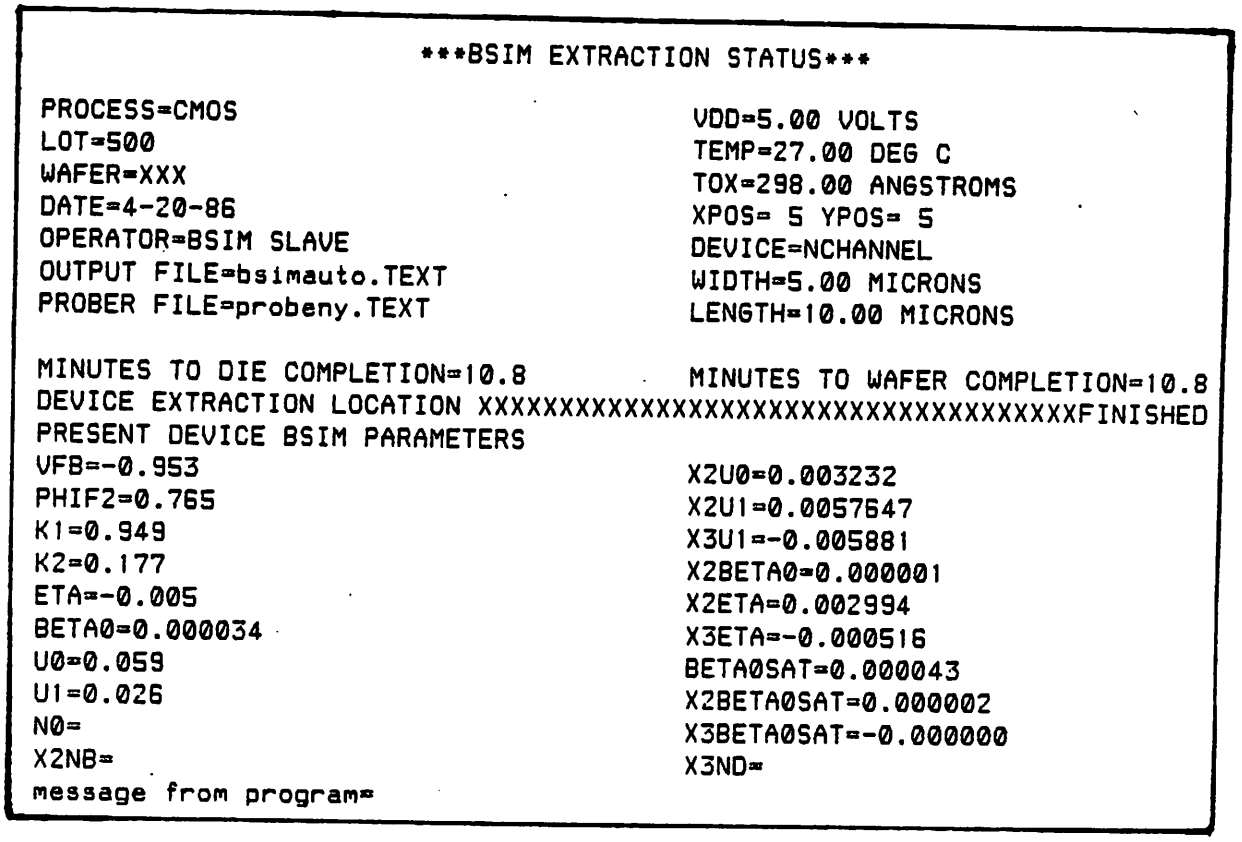


Figure 4-9d. BSIM Extraction Status (Automatic Mode)

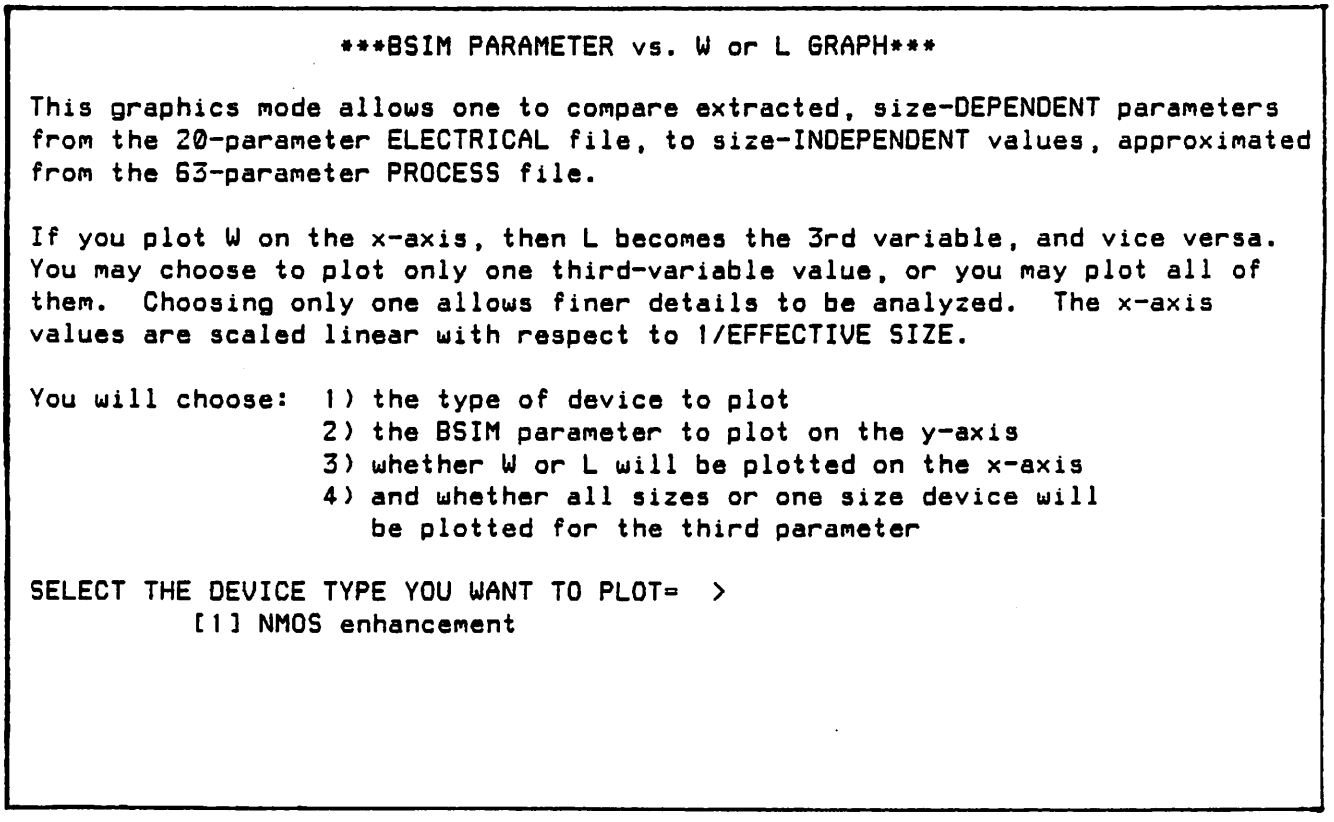


Figure 4-9e. BSIM Parameter Graphics Menu (part 1)

```
W/L ratios of devices successfully tested are listed here:
W          5.0    5.0    5.0    5.0   10.0   20.0   50.0
L         10.0    7.0    4.0    5.0    5.0    5.0    5.0









SELECT DESIRED GRAPH=? >
          [1] BSIM PARAMETER vs. W --- for all values of L
          [2] BSIM PARAMETER vs. L --- for all values of W
          [3] BSIM PARAMETER vs. W --- for single value of L.  L=? >
          [4] BSIM PARAMETER vs. L --- for single value of W.  W=? >
```

Figure 4-9f. BSIM Parameter Graphics Menu (part 2)

```
SELECT THE PARAMETER TO BE GRAPHED=  >
           [1] VFB
           [2] 2PHIF
           [3] K1
           [4] K2
           [5] ETA
           [6] BETA0
           [7] U0
           [8] U1
           [9] X2MU0
          [10] X2ETA
          [11] X3ETA
          [12] X2U0
          [13] X2U1
          [14] MU0SAT
          [15] X2MU0SAT
          [16] X3MU0SAT
          [17] X3U1
          [18] N0
          [19] X2NB
          [20] X3ND
```

Figure 4-9g. BSIM Parameter Graphics Menu (part 3)

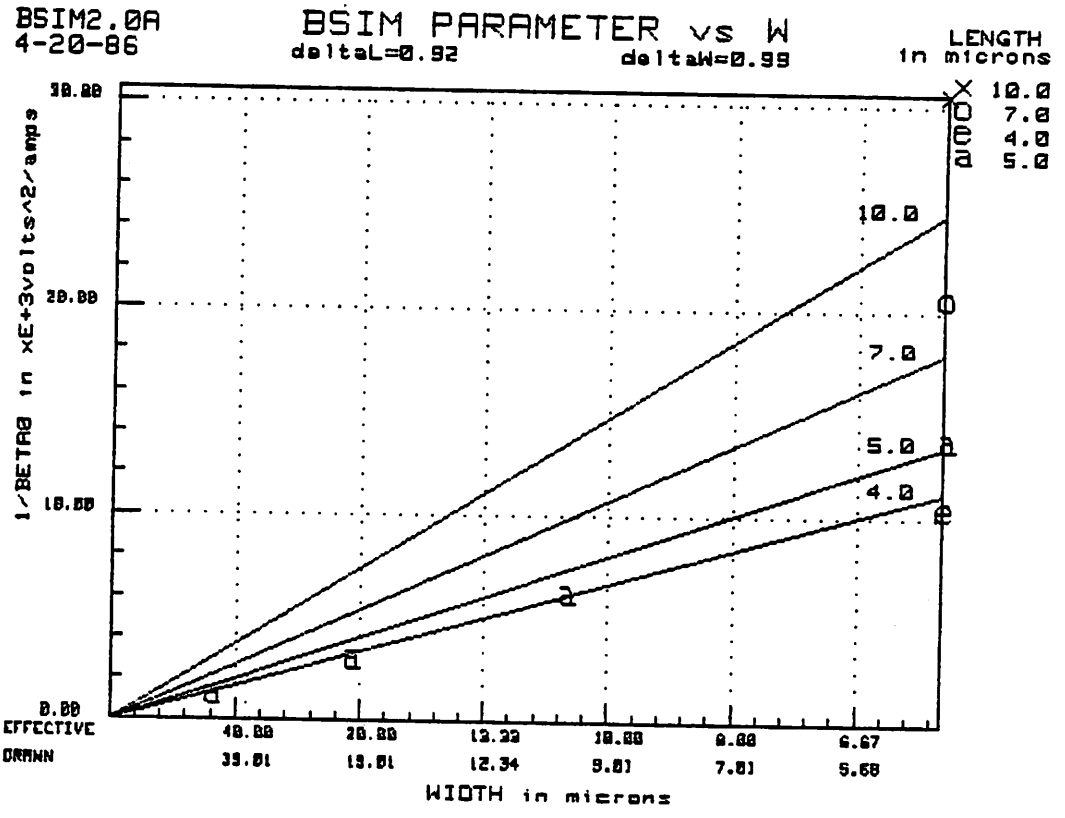


Figure 4-9h. Graph of BSIM Parameter 1/BETA0 versus W

```
                    ***PREPARATION FOR I-V GRAPHICS***

X DIE POSITION OF DEVICE TO BE GRAPHED (DEFAULT IS CURRENT)=  >

Y DIE POSITION OF DEVICE TO BE GRAPHED (DEFAULT IS CURRENT)=  >

                                          [1] NMOS enhancement
SELECT THE NUMBER CORRESPONDING           [2] NMOS depletion
TO THE DEVICE TYPE WHICH                  [3] NMOS zero-threshold
YOU WOULD LIKE TO GRAPH=   >              [4] PMOS enhancement
                                          [5] PMOS depletion
                                          [6] PMOS zero-threshold

DEVICE WIDTH (microns) =  >

DEVICE LENGTH (microns) =  >
```

Figure 4-9i. Preparation For I-V Graphics Menu

```
                    ***BSIM I-V GRAPHICS MENU***

The BSIM I-V graphics routines will draw measured and/or simulated I-V data.
If the program is operating in the "SINGLE" mode, the 20 ELECTRICAL parameters
just extracted will be used. In the "AUTOMATIC" mode, the 20 ELECTRICAL
parameters will be generated from the 63 parameter process file.

              SELECT A NUMBER FOR A GIVEN DISPLAY MODE=  >
                   1)Measured Data Only
                   2)Simulated Data Only
                   3)Measured and Simulated Data

               SELECT A NUMBER FOR A GIVEN GRAPH TYPE=  >
                   1)IDS versus VDS            VBS=?  >
                   2)IDS versus VGS            VDS=?  >
                   3)log(IDS) versus VGS        VDS=?  >
```

Figure 4-9j. I-V Graphics Menu

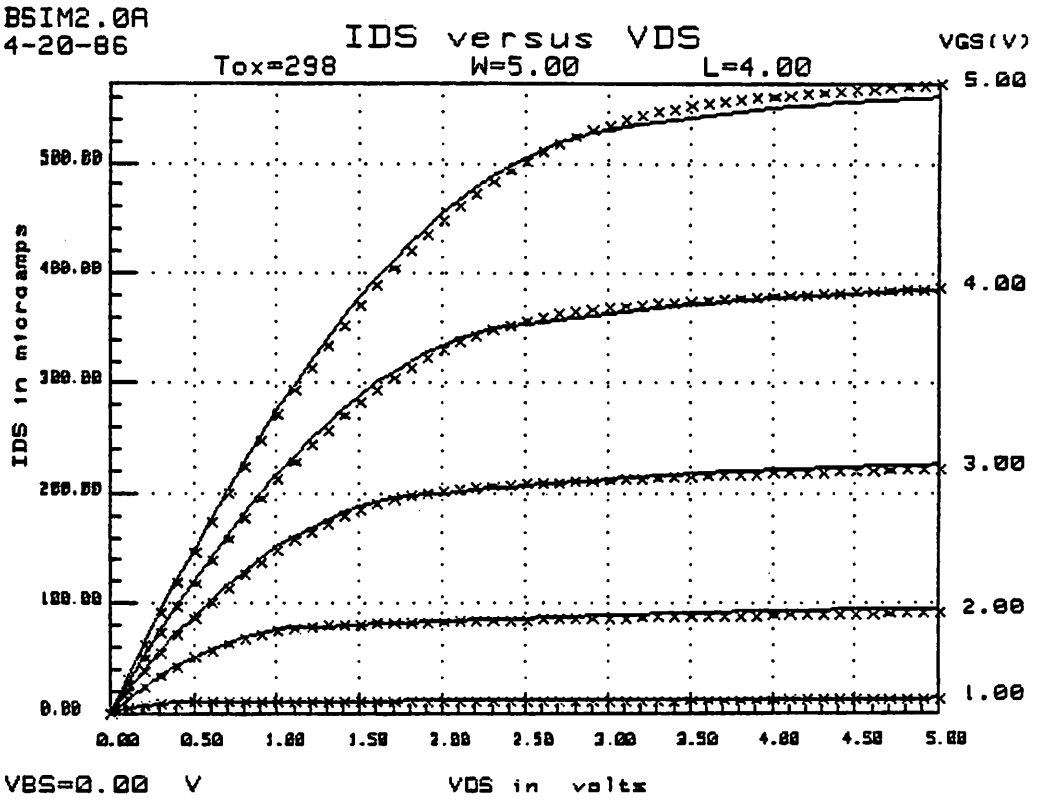


Figure 4-9k. IDS versus VDS Curve

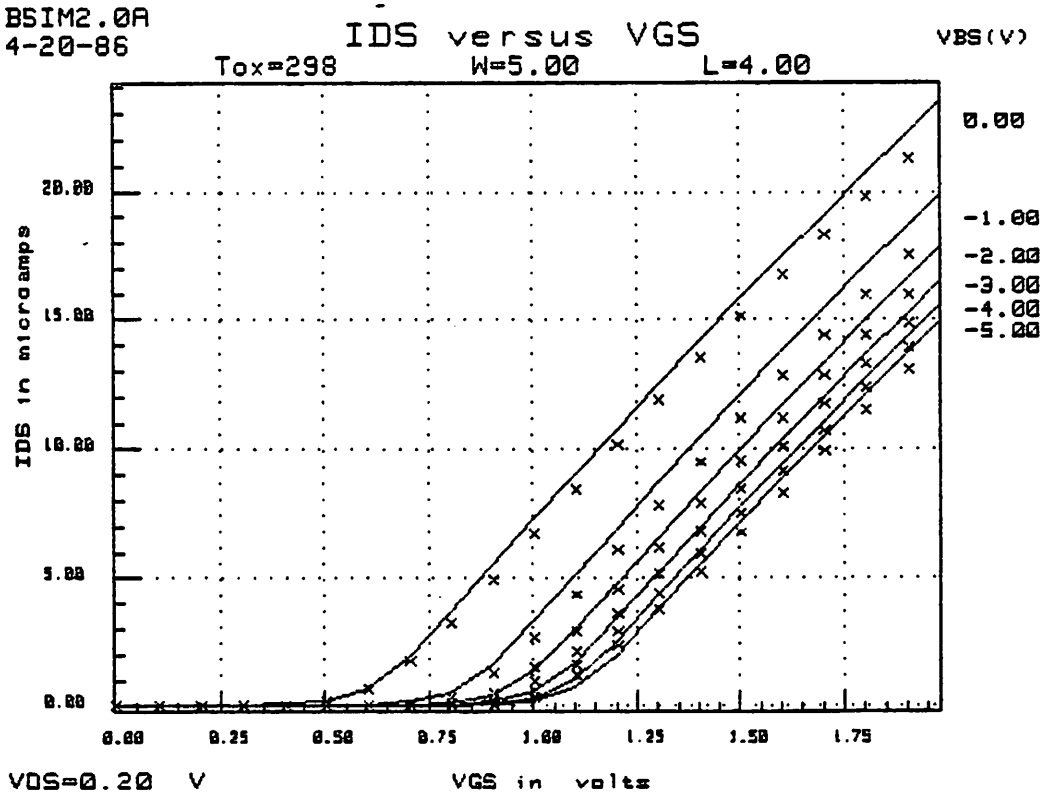


Figure 4-9l. IDS versus VGS Curve

4.4.1.7. I-V Graphics

Figures 4-9k and 4-91 are examples of two I-V curves. The solid lines are simulated curves and the X's are measured points.

4.4.1.8. Process File

The final product of the BSIM extraction system is the process file (figure 4-10). This file contains the information needed by SPICE to use the BSIM transistor model. Presently, SPICE requires the user to enter some more process information into the file before the BSIM model can be used. In the current example, the process file contains information for 2 dies, which is the number of dies specified in the prober file.

Line 1 is the device type; NM1 stands for NMOS enhancement. The next 7 lines are extraneous information needed by the extraction program but not needed by SPICE. Rest of the process file for die 1 contains size-independent parameters and statistical data.

The data in the first 3 columns are the 63 size-independent parameters (60 device parameters, oxide thickness, temperature, and supply voltage). For the 60 device parameters, each number in column 1 is P0, in column 2 is PL, and in column 3 is PW. These size-independent parameters are used to calculate the size-dependent parameter P in equation equation 4.1.

$$P = P0 + \frac{PL}{L + \Delta L} + \frac{PW}{W + \Delta W} \tag{4.1}$$

P is just a generic symbol for one of the 20 size-dependent BSIM parameters (e.g., VFB, ETA, BETA0, etc.). Because the subthreshold measurement and extraction are not done in this example, the last 3 full rows (of each die) have 0's for P0, PL, and PW. The last row consists of the oxide thickness, temperature, and supply voltage.

When a parameter is simulated using equation 4.1, the simulated parameter is compared to the actual extracted value of each device. The largest RMS deviation and the size

```
NM1
*PROCESS=CMOS
*RUN=500
*WAFER=XXX
*XPOS=4
*YPOS=5
*OPERATOR=BSIM SLAVE
*DATE=4-20-86
-9.1390E-001,2.66001E-001,-5.2620E-002,4.05033E-001,5.00000E+000,5.00000E+000
7.54969E-001,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,1.00000E+001
9.36379E-001,-4.4967E-001,-6.2769E-003,5.09112E-001,5.00000E+000,5.00000E+000
2.01194E-001,-5.3919E-002,-1.5991E-001,8.31179E-001,5.00000E+000,5.00000E+000
-8.2590E-003,1.45610E-002,-7.7279E-004,3.80808E+000,5.00000E+000,5.00000E+000
6.66170E+002,6.87959E-001,1.00098E+000,0.00000E+000,0.00000E+000,0.00000E+000
9.40073E-002,8.11173E-002,-1.7841E-001,8.60325E-001,5.00000E+000,5.00000E+000
1.98182E-001,8.44503E-001,4.86424E-002,5.71302E-001,5.00000E+000,5.00000E+000
5.74080E+000,-1.3565E+001,2.27035E+001,1.98666E-001,5.00000E+000,5.00000E+000
7.50890E-004,8.67863E-003,3.82305E-003,4.60805E+000,5.00000E+000,5.00000E+000
1.17043E-003,-1.7277E-003,-4.3886E-003,4.76668E+001,5.00000E+000,5.00000E+000
1.63256E-003,-3.6745E-003,7.92135E-004,8.98168E+000,5.00000E+000,4.00000E+000
5.63787E-002,-1.6012E-001,9.49113E-002,2.18627E+001,5.00000E+000,5.00000E+000
8.24664E+002,7.51789E+002,-2.8963E+002,1.12946E+000,5.00000E+000,5.00000E+000
8.89817E+000,3.76749E+001,4.20749E+001,6.22065E+000,5.00000E+000,5.00000E+000
-2.3020E+001,1.56629E+002,1.01176E+001,1.00135E+001,5.00000E+000,1.00000E+001
-1.0066E-001,4.33998E-001,-2.7650E-003,1.09633E+002,5.00000E+000,5.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,1.00000E+001
0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,1.00000E+001
0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,1.00000E+001
2.98000E-002,2.70000E+001,5.00000E+000
NM1
*PROCESS=CMOS
*RUN=500
*WAFER=XXX
*XPOS=5
*YPOS=5
*OPERATOR=BSIM SLAVE
*DATE=4-20-86
-9.3288E-001,2.43494E-001,-7.7464E-002,1.49831E+000,5.00000E+000,7.00000E+000
7.60717E-001,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,1.00000E+001
9.28493E-001,-3.4919E-001,7.22211E-002,1.58431E+000,5.00000E+000,7.00000E+000
1.96953E-001,-2.5732E-002,-1.2864E-001,1.88755E+000,5.00000E+000,7.00000E+000
-7.9483E-003,1.54511E-002,-1.4168E-003,2.14666E+001,5.00000E+001,5.00000E+000
6.50155E+002,8.66525E-001,9.90487E-001,0.00000E+000,0.00000E+000,0.00000E+000
1.09177E-001,7.96936E-002,-2.4541E-001,2.05199E+001,2.00000E+001,5.00000E+000
1.17575E-001,9.83758E-001,1.97044E-001,2.79561E+001,5.00000E+001,5.00000E+000
4.55304E+000,-9.3409E+000,2.77935E+001,1.24833E+001,5.00000E+001,5.00000E+000
9.41739E-004,7.69074E-003,4.57885E-003,6.08732E+000,1.00000E+001,5.00000E+000
1.09777E-003,-1.0225E-003,-5.8832E-003,3.33455E+002,1.00000E+001,5.00000E+000
1.08456E-003,-1.9640E-003,3.44349E-003,1.89438E+001,2.00000E+001,5.00000E+000
3.60121E-002,-1.0058E-001,1.23318E-001,5.32178E+001,5.00000E+001,5.00000E+000
7.58834E+002,8.10342E+002,-1.6541E+002,1.41528E+000,5.00000E+001,5.00000E+000
-1.1839E-001,4.93238E+001,7.71574E+001,2.07252E+001,5.00000E+001,5.00000E+000
-2.6522E+001,1.54347E+002,2.62456E+001,9.07502E+001,5.00000E+001,5.00000E+000
-9.7190E-002,3.76092E-001,4.98754E-002,2.04102E+002,2.00000E+001,5.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,1.00000E+001
0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,1.00000E+001
0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,1.00000E+001
2.98000E-002,2.70000E+001,5.00000E+000
```

Figure 4-10. Process File (Automatic Mode)

of the device that yields this deviation are stored in the process file. Each number in column 4 is the error; each number in column 5 is the width; each number in column 6 is the length.

4.4.2. Single Device Mode

In single device mode, the user interacts more frequently with the program. No prober file is used so that the user must enter the information (figure 4-11a) for each device he measures. Most of the prompts are self explanatory. The display shows a prompt for "PHIF2 or NSUB=? >". Either PHIF2 or NSUB can be entered. PHIF2 is more conventionally known as $2\phi_F$ (i.e., 2 times the equilibrium electrostatic potential) and is typically 0.6V. NSUB is the substrate doping. The program can distinguish which one is entered because of the difference in magnitude of the 2 numbers. If the user does not know either values exactly, then entering 0.6 will probably be a good estimate. In the automatic mode, this value is extracted from the devices and hence it does not have to be entered by the user.

When above threshold measurement and extraction are done, then the user is asked if he wants subthreshold measurement and extraction (figure 4-11b). When parameter extraction is done, then the I-V graphics mode can be entered. In the single device mode, the user can view the characteristics of only the current device.

A process file (figure 4-12) is also created in single device mode. The format is identical to the automatic mode. However, the numbers in the second, third, and fourth columns are all 0. This means PL and PW are 0 so that equation 4.1 becomes equation 4.2.

$$P = P0 + \frac{0}{L + \Delta L} + \frac{0}{W + \Delta W} = P0 \qquad (4.2)$$

Therefore, the parameters in the single device mode process file are just the 20 size-dependent BSIM parameters (e.g., VFB, ETA, BETA0, etc.). Subthreshold measurement and extraction are done on this device, so that P0's for the last 3 full rows are not 0.

```
                    ***SINGLE DEVICE OPERATION***

Process Name=CMOS
Lot=500
Wafer=XXX          XPOSITION=0          YPOSITON=0
Date=4-20-86
Operator=BSIM SLAVE
Output File=bsimout.TEXT
VDD(volts)=5.00
TEMPERATURE(deg. C)=27.00
TOX(angstroms)=298.00
PHIF2 or NSUB=6.00000E-001
drawn width (microns)=5.00
drawn length (microns)=4.00
Device type=enhancement

PIN connected to GATE=24
PIN connected to DRAIN=30
PIN connected to SOURCE=6
PIN connected to BODY=48

Hit a "C" for changes or any other key to start.  >
```

Figure 4-11a. Single Device Mode Inputs

```
                    ***BSIM EXTRACTION STATUS***

PROCESS=CMOS                              VDD=5.00 VOLTS
LOT=500                                   TEMP=27.00 DEG C
WAFER=XXX                                 TOX=298.00 ANGSTROMS
DATE=4-20-86                              XPOS= 0 YPOS= 0
OPERATOR=BSIM SLAVE                       DEVICE=NCHANNEL
OUTPUT FILE=bsimout.TEXT                  WIDTH=5.00 MICRONS
PROBER FILE=SINGLE DEVICE OPERATION       LENGTH=4.00 MICRONS

MINUTES TO DIE COMPLETION=0.0             MINUTES TO WAFER COMPLETION=0.0
DEVICE EXTRACTION LOCATION XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXFINISHED
PRESENT DEVICE BSIM PARAMETERS
VFB=-0.583                                X2U0=0.000734
PHIF2=0.600                               X2U1=0.011039
K1=0.714                                  X3U1=0.006075
K2=0.127                                  X2BETA0=0.000001
ETA=-0.003                                X2ETA=0.004460
BETA0=0.000095                            X3ETA=-0.000428
U0=0.080                                  BETA0SAT=0.000136
U1=0.134                                  X2BETA0SAT=0.000005
N0=                                       X3BETA0SAT=0.000003
X2NB=                                     X3ND=
Are you interested in subthreshold region measurements and extraction?(Y/N)  >
```

Figure 4-11b. BSIM Extraction Status (Single Device Mode)

```
NM1
*PROCESS=CMOS
*RUN=500
*WAFER=XXX
*XPOS=0
*YPOS=0
*OPERATOR=BSIM SLAVE
*DATE=4-20-86
-5.8265E-001,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
6.00000E-001,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
7.13838E-001,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
1.27382E-001,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
-2.9461E-003,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
9.46484E-005,0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000
8.03394E-002,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
5.34652E-001,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
7.07904E+000,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
4.45960E-003,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
-4.2750E-004,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
7.34269E-004,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
4.41560E-002,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
9.38588E+002,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
3.12739E+001,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
2.32734E+001,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
2.42991E-002,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
2.45631E+000,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
-8.6294E-002,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
2.01947E-001,0.00000E+000,0.00000E+000,0.00000E+000,5.00000E+000,4.00000E+000
2.98000E-002,2.70000E+001,5.00000E+000
```

Figure 4-12. Process File (Single Device Mode)

4.4.3. Options Mode

The options Menu is show in figure 4-13a. In this mode, the user can enter I-V graphics directly from the initial execution of the program or run simple diagnostics on the 4062 hardware.

4.4.3.1. I-V Graphics

If a process file has been created from an earlier BSIM extraction session, then the user can examine his data by plotting the simulated I-V characteristics. This option gives the user the flexibility to check his data without having to run first the time-consuming measurement and extraction routines. The user can also check any actual device characteristics against the simulated curves as in the normal I-V graphics mode. Of course, the user would then have to set up the BSIM-4062 measurement system. There are differences between this mode and the normal I-V graphics mode:

- all prober movements are manual.
- all matrix pin connections must be entered.

4.4.3.2. 4062 Self Tests

The DC source/monitor (4141) and the switching matrix (4085) can be checked for hardware problems (e.g., stuck matrix relay, inoperative SMU, etc.). The self-test menu is shown in figure 4-13b.

The relay test adapter (HP 16075) is needed to check out the switching matrix. This adapter comes with the 4062 system and is shown in figure 4-14. The matrix must be placed so that the matrix pins are facing upward. The adapter is screwed on top of the pins.

If something is wrong with the 4141, then the program will inform the user and the equipment should then be shipped to Hewlett-Packard for repairs.

```
                    *** OPTIONS MENU ***

In options mode, you can view I-V graphics or run the 4062 diagnostics.

In the I-V graphics option, you also must enter a valid process file.
The X and Y die position (which you'll be prompted for later) must be
that of a die in the process file.  All prober movements in this mode
will be MANUAL.




                                [1]: IV GRAPHICS
Select an option    >           [2]: 4062 SELF TESTS
                                [3]: EXIT TO MAIN MENU
```

Figure 4-13a. Options Menu

```
                    *** 4062 SELF TEST ***

The available diagnostics are for the DC source/monitor (HP4141) and
the switching matrix (HP4085).

In order to test the switching matrix, place the matrix so that the
matrix pins are facing up.  Then screw the relay test adapter (HP16075)
onto the matrix facing the pins and then you are ready.




Select an option  >     [1]:DC SOURCE / MONITOR
                        [2]:SWITCHING MATRIX
                        [3]:EXIT TO MAIN MENU
```

Figure 4-13b. Self Test Menu

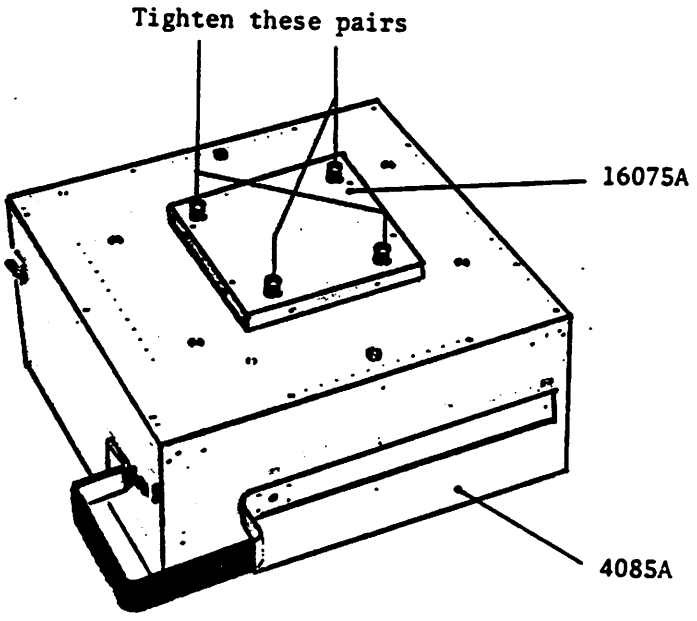


Figure 4-14. Relay Test Adapter

The switching matrix, however, can often be repaired by the user. Typically a relay will go bad (stuck open or close). The diagnostics does a good job in locating which relay of which board is bad, but the test stops when the first bad relay is found, so that the relays have to be repaired one by one The error messages are in encoded form and the user should refer to next section for explanation of message.

4.4.3.3. Switching Matrix Failure Codes

During the matrix self test, if something is not working properly, then the program will display a cryptic message on the 9836 monitor. The self test will stop after the first error condition is detected. The message is in the form

FL *failure_code* **PC** *pin_board_id* **K** *relay_id*

where **FL** means a failure has occurred. *Failure_code* is one of the conditions in the table 4-1. *Pin_board_id* is one of the circuit boards in the matrix and the number is between 1 and 48. *Relay_id* is the number of the faulty relay on that board. Figure 4-15 shows the relay numbers on a board. Table 4-1 shows only failure codes 06 to 63 because failure codes 01 to 05 can not be returned to the computer via HP-IB. Hence these codes will not displayed and the user will not know what is wrong. Fortunately, a flashing LED on the matrix controller indicates that "something" is wrong. Here are the failure codes that are not displayed:

Codes 01, 02, or 03: ROM failure.

Code 04: RAM malfunction.

Code 05: HP-IB chip malfunction or illegal HP-IB address.

As an example, if the error message is

FL36PC42K11.

Failures 06 through 09 indicate a 4084A malfunction.

06: power failure detected.
07: receive parity check circuit malfunctioning.
08: send/receive timing circuit malfunctioning.
09: MPU malfunctioning.

Failures 11 through 19 indicate a 4085A malfunction.

11: 4084A and the 4085A are not interconnected.
12: Switching Matrix Open interrupt circuit is faulty.
13: no pin boards installed.
14: send error detected.
15: receive parity error detected.
16: REPLY line is stuck.
17: relay power supply overload.
18: send-parity generator is malfunctioning.
19: a pin board was removed or it malfunctioned during system START.

Failures 20 through 29 indicate a Relay Test failure.

20: Relay Test Adapter not installed on the 4085A.
21: SENSE ADC malfunctioning.
22: FORCE ADC malfunctioning.
23: GUARD ADC malfunctioning.
24: Test Relay Board missing.
25: Test ADC Board missing.
26: Fewer than 5 pin boards installed in the 4085A.

Failures 31 through 37 indicate an open relay (contacts will not MAKE).

31 (32, 33): SENSE (FORCE, GUARD) contacts of a MAKE relay are open.
34: Normally open (NO) contacts of a SENSE TRANSFER relay will not make.
35: Normally closed (NC) contacts of a SENSE TRANSFER relay are open.
36: NO contacts of a FORCE TRANSFER relay will not make.
37: NC contacts of a FORCE TRANSFER relay are open.

Failures 41 through 47 indicate a stuck relay (contacts will not BREAK).

41 (42, 43): SENSE (FORCE, GUARD) contacts of a MAKE relay are stuck.
44: NO contacts of a SENSE TRANSFER relay are stuck.
45: NC contacts of a SENSE TRANSFER relay are stuck.
46: NO contacts of a FORCE TRANSFER relay are stuck.
47: NC contacts of a FORCE TRANSFER relay are stuck.
56: Indicates a relay tri-point short, but the defective pin board cannot be determined.

Failures 61 through 63 indicate that the specified pin board has one or more faulty relays, but the faulty relay(s) cannot be isolated.

Table 4-1. Failure Codes

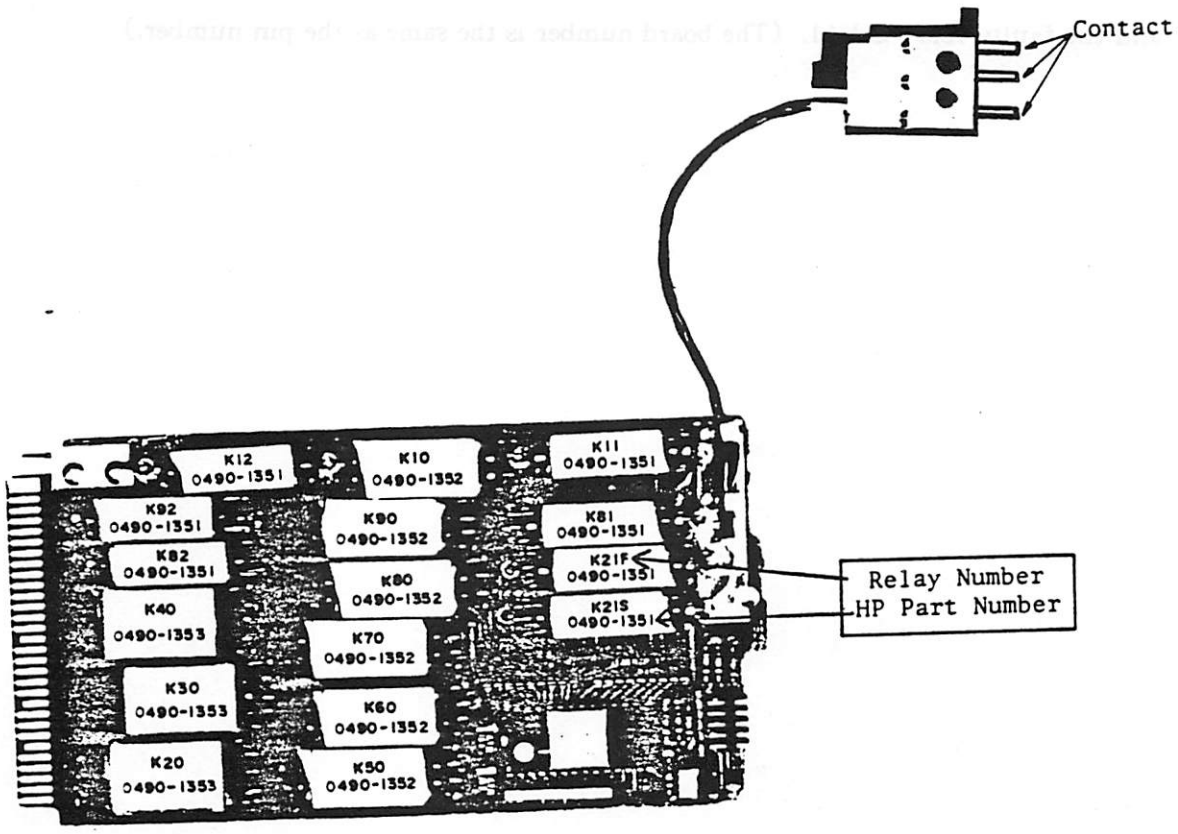


Figure 4-15. Relay Locations

then the failure code is 36, which, according to table 4-1, means that the "normally open" contacts of a relay will not make (i.e., will not close). The defective board is board #42 and the faulty relay is K11. (The board number is the same as the pin number.)

5. Modifications to the BSIM-4145 program

Several graduate researchers have contributed to the BSIM extraction program using the HP 4145 analyzer. Section 5.1 contains a list of newly added procedures for the BSIM-4062 program. Section 5.2 contains a list of modified procedures. Each procedure is listed by the order it appears in the BSIM source code.

5.1. Procedures Added

Procedure init_global_variables

Global variables are initialized.

Procedure pause

This is a 'for loop' that does nothing for about 5 seconds.

Procedure clear_and_connect_matrix_pins

The switching matrix is initially cleared and then matrix connections (SMU1 to gate, SMU2 to drain, SMU3 to source, and SMU4 to body) are made. The pin numbers (i.e., the number of the pin connected to gate, etc.) are specified by user in either the prober file or single device input menu.

Procedure matrix_self_test

The switching matrix diagnostics are executed. A "passed" or "failed" message is displayed. If failed, then the error code is displayed.

Procedure DCS_self_test

The DC source/monitor (4141) diagnostics are executed. A "passed" or "failed"

message is displayed. If failed, then the SMU, VS, or VM number is displayed.

Procedure self_test_4062

The self test menu is displayed and the routine to test DC source/monitor or switching matrix is called.

Procedure set_vdrain_to_measure_IDSvsVGS

This procedure is used to reset the drain voltage each time an IDSvsVGS curve is measured. The BSIM-4145 version resets all the voltage sources, which is not necessary for the 4062.

Procedure measure_IDSvsVGS_using_next_vg

The 4062 has a secondary sweep, but it does not operate like the one in the 4145. This procedure is used in a loop to simulate the 4145 secondary sweep.

Procedure search_for_device

The arrays w[] and l[] are searched to find the device that the user wants to plot for I-V graphics.

Procedure iv_auto_prober_move

This procedure moves the prober-stage to the die that the user specified for I-V graphics. If the device specified is one that has been measured, then the probes are placed on that device.

Procedure measure_IDSvsVGS_data_using_next_vb

This procedure sets the body voltage.

Procedure measure_IDSvsVDS_data_using_next_vg

This procedure sets the gate voltage.

Procedure options_menu

This procedure displays the "OPTIONS" menu and gets the input from user.

Procedure options

This procedure executes the option specified by user.

5.2. Procedures Modified

Procedure bsim_timer

The constant minutes_per_device is changed to a variable so that the time for subthreshold measurement and extraction may be included.

Procedure initial_bsim_page

The main menu display is changed. Mode '1' is now automatic; mode '2' is single; mode '3' is options.

Procedure automatic_mode_inputs

Prompts for P0 graphics, iv graphics, and subthreshold measurement are added.

Procedure single_device_mode_inputs

Prompts for SMU connections are now PIN connections.

Procedure initial_status_inputs

Values for the global variable 'mode' are changed.

Procedure source_setup_to_test_device_type

HP-IB strings are changed for the 4141 (DC source/monitor).

Procedure measure_device_type

HP-IB strings are changed for the 4141.

Procedure source_setup_nchannel_device_functionality

HP-IB strings are changed for the 4141.

Procedure source_setup_pchannel_device_functionality

HP-IB strings are changed for the 4141.

Procedure measure_device_functionality

HP-IB strings are changed for the 4141.

Procedure source_setup_measure_IDSvsVGS

HP-IB strings are changed for the 4141.

Procedure measure_and_reduce_IDSvsVGS_data

The flashing message "MEASUREMENT IN PROGRESS" is added to let the user know that the program is executing. Since the 4141 does not have a secondary sweep mode, this procedure calls measure_IDSvsVGS_using_next_vb in a loop to simulate a secondary sweep.

Procedure measure_device_data

All calls but the initial call to procedure source_setup_IDSvsVGS are replaced by the calls to set_vdrain_to_measure_IDSvsVGS since vdrain is the only voltage that needs to be changed.

Procedure measure_device

HP-IB strings are changed for the 4141.

Procedure measure_and_reduce_subthIDSvsVGS

The flashing message "MEASURING SUBTHRESHOLD DATA" is added to notify user that the program is executing.

Procedure linear_region_extraction

If Newton-Raphson routine does not converge, then linear_extract_error is set to 2. The message "LINEAR REGION EXTRACTION IN PROGRESS" is added.

Procedure large_device_20f_extraction

If Newton-Raphson routine does not converge, then large_device_error is set to 2. The message "PHIF2 EXTRACTION IN PROGRESS" is added.

Procedure linear_region_threshold_analysis

Mode = '2' is now the single device mode.

Procedure saturation_region_data_extraction

If the Newton-Raphson routine does not converge, then saturation_extract_error is set to 2. The message "SATURATION REGION EXTRACTION IN PROGRESS" is added.

Procedure zero_u1_saturation_extraction

If Newton-Raphson routine does not converge, then zero_u1_error is set to 2.

Procedure saturation_parameter_refinement

The message "REFINING SATURATION REGION PARAMETERS" is added.

Procedure subthreshold_parameter_extraction

The message "SUBTHRESHOLD PARAMETER EXTRACTION IN PROGRESS" is added.

Procedure prober_move

The argument "zpos" is added to the parameter list. "zpos" tells this procedure

whether or not to raise the wafer to the probes (i.e., make contact). This procedure has been moved since it is now also called from within procedure iv_graphics.

Procedure set_die_size

This procedure has been moved since it is now called from within procedure iv_graphics.

Procedure prepare_for_iv_graphics

In the "PREPARATION FOR I-V GRAPHICS" menu, default values for the X and Y die positions and the width and length are added. If the user does not enter the X and Y positions, the default positions will be the current die position. Similarly, the default width and length are set to 10 microns. If the user enters I-V graphics from the "OPTIONS" mode, then the variable "cox" will be set in this procedure.

Procedure source_setup_measure_IDSvsVGS

The HP-IB strings are changed for the 4141. SMU 4, the power supply connected to the body, is now set in the newly added procedure measure_IDSvsVGS_data_using_next_vb.

Procedure measure_IDSvsVGS_data

The HP-IB strings are changed for the 4141. The messages "measuring IDS vs VGS data" and "FINISHED MEASURING" are added. The procedure measure_IDSvsVGS_data_using_next_vb is called in a loop to simulate the secondary sweep of the 4145.

Procedure source_setup_measure_IDSvsVDS

The HP-IB strings are changed for the 4141. SMU 1, the power supply connected to

the gate, is now set in the newly added procedure measure_IDSvsVDS_data_using_next_vb.

Procedure measure_IDSvsVDS_data

The HP-IB strings are changed for the 4141. The messages "measuring IDS vs VDS data" and "FINISHED MEASURING" are added. The procedure measure_IDSvsVDS_data_using_next_vg is called in a loop to simulate the secondary sweep of the 4145.

Procedure measure_data

The arguments passed to this procedure are pin numbers instead of SMU numbers.

Procedure IDvsVD

The message "CALCULATING SIMULATED GRAPH" is added.

Procedure logIDvsVG

The message "CALCULATING SIMULATED GRAPH" is added.

Procedure IDvsVG

The message "CALCULATING SIMULATED GRAPH" is added.

Procedure draw_menu

"SEMI-AUTOMATIC" mode has been deleted.

Procedure page3

In the P0 graphics menu, the 3 subthreshold parameters will be displayed only if subthreshold measurement has been performed.

Procedure process_file_development

The 2 statements to rewrite and close process file after checking for a new wafer are deleted. These statements are redundant because creating the process file (i.e., rewrite and close) is done in another procedure. Moreover, these statements form a bug because the variable "new_wafer" is never set to false. Therefore, when another set of parameters is suppose to be appended to the process file, the new set actually destroys the old set, leaving at most 1 set of parameters in the process file. This bug is not a problem if the user measures only one die.

Procedure read_prober_file

Because the format of the prober file is changed, this procedure is changed to accommodate the new file. This procedure performs the following steps.

a) counts number of dies to be probed.
b) counts number of devices per die.
c) fills in the arrays mx, my, dt, ed, pd, ps, pg, pb, mxmap, and step_array using the information in the prober file.

Procedure find_and_switch_best_device

The matrix pin arrays (pd, ps, pg, pb) are used instead of SMU arrays (sd, ss, sg, sb).

Procedure load_automatic_parameters

Matrix pins are used instead of SMUs.

6. CONCLUSION

The BSIM parameter extraction system has been implemented using the HP 4062 test system and the Electroglas 2001X automatic prober, thus making fully automatic parameter extraction a practical reality. New features have been added to the extraction program to make the system more user-friendly, to make it more resilient, and to make it more useful.

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