BSIM – SUBSTRATE CURRENT MODELING

by

Peter M. Lee

Memorandum No. UCB/ERL M86/49

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ABSTRACT

As MOS device dimensions become smaller in VLSI circuits, device degradation becomes an increasingly worrisome issue, especially as the power supply voltage remains unscaled at 5 V. As a result, hot-electron substrate current is enhanced in small-geometry devices, and has been found to cause threshold-voltage shifts because of the generation of surface states at the silicon- silicon dioxide interface and electron trapping in the silicon dioxide.

The purpose of this research is to develop an accurate substrate-current model for circuit simulation. This model will be implemented in SPICE as a supplementary model in the BSIM family. With this tool, a circuit designer will be able to simulate the substrate current of individual devices in his circuit in operation, and therefore evaluate the reliability of his circuit in the early stage of design. It is also anticipated that more degradation-resistant circuit-design techniques will be developed once this model is available in SPICE.

This work was supported by the Semiconductor Research Corporation

ACKNOWLEDGEMENTS

I am deeply indebted to the support and technical assistance of my research advisor, Professor Ping K. Ko, who gave me the guidance to successfully complete my research. His patience and understanding were greatly appreciated. I would also like to extend my gratitude to Min-Chie Jeng, Dr. Bing J. Sheu, Norman Yuen, and Tung-Yi Chan for their help throughout the project. Our many technical discussions helped greatly.

I wish to thank my parents, Maurice and Kuniko, for their encouragements and support over the past several years. Their patience and guidance are deeply appreciated.

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I. INTRODUCTION

With technological advancements in creating smaller and smaller features in VLSI circuits, MOS device dimensions have continued to shrink at a rapid pace. Circuit designers increasingly utilize smaller devices to decrease chip area, power consumption, and propagation delays. However, the power supply has remained at 5 volts, and as a consequence, greater electric fields exist within small-geometry devices, and hot-electron effects become important.

As maximum electric field in the drain end increases with shorter channel lengths, more and more hot electrons acquire sufficient kinetic energy not only to damage the silicon-silicon dioxide interface but also to overcome or tunnel through the silicon dioxide barrier and become trapped in the oxide. Both result in threshold voltage shifts that could potentially be fatal in circuit design.

Greater lateral electric field also causes an increase in the number of electrons which possess the required energy to create electron-hole pairs by impact ionization. The excess holes that are produced are swept into the substrate by the vertical field as substrate current. Because both hot-electron-induced degradation and substrate current generation are induced by the same force (namely the channel electric field), it can be shown that a direct correlation exists between the amount of degradation occurring and the substrate current measured [1].

Because of this fact, knowledge of the substrate current of the devices used in a circuit can provide valuable information on how reliable the circuit will be. It is therefore important to develop an accurate model of the substrate current and to incorporate it into circuit simulation.

In this project, a parametric substrate current model is implemented into the Berkeley Short-Channel IGFET Model (BSIM). 11 bias-independent parameters are added to the existing 20 to accurately simulate substrate current behavior for a variety of processes. In

parallel with the other models of the BSIM family, each bias-independent parameter is then decomposed into three size-independent parameters which are used to create a single process file for each die. Presently, the model has been carefully evaluated for conventional and lightly-doped drain (LDD) NMOS enhancement-mode devices. A more detailed description of the general extraction process and a user's guide to the BSIM program (not including the substrate current implementation) are given in [2].

The following section of this report contains the theoretical motivation in the development of the substrate current model used in BSIM. Next, a detailed description of the actual measurement and extraction process is given. Experimental results from several technologies are then summarized. In the Appendices, a brief user's guide to the operation of the substrate current measurement portion of the BSIM program and a summary of the procedures added or modified to the source code are given.

II. SUBSTRATE CURRENT MODEL

2.1 Introduction

The substrate current model used in BSIM is based on work done by El-Mansy [3,4] and Ko [5]. El Mansy derived an exponential relationship of the channel electric field in the saturated region of the channel using quasi-two-dimensional concepts, and using this electric field model he derived a simplified model for the substrate current. This model was subsequently improved by Ko to include the effect of junction depth and channel doping.

The following is an outline of the derivations done to obtain the substrate current expression. For a more detailed derivation, one is referred to the above references.

2.2 The Model

Because the main contribution to the substrate current is from electron impact ionization, the derivation is begun by integrating the electron impact ionization coefficient $\alpha_n = A_i e^{-\frac{B_i}{E}}$ in the velocity-saturated region of the channel.

$$I_{bs} = I_{ds} A_i \int_{y=0}^{\Delta L} e^{-\frac{B_i}{E_s(y)}} dy \tag{2.1}$$

$y = 0$ is at the edge of the saturated region in the channel, $y = \Delta L$ is at the drain, and $E_s(y)$ is the electric field in the channel direction. To find $E_s(y)$, a pseudo-two-dimensional analysis is performed of a Gaussian box enclosing the saturated region. This results in an exponential relationship of $E_s(y)$ versus distance.

$$E_s(y) = E_{crit} \cosh(\frac{y}{l_c}) \tag{2.2}$$

E_{crit} is the critical field for velocity saturation, and l_c can be termed as an "effective conduction depth" of mobile carriers. $E_s(y)$ can also be expressed in terms of voltage within the saturated region.

$$E_s(y) = \left[\frac{(V_s(y) - V_{dsat})^2}{l_c^2} + E_{crit}^2\right]^{\frac{1}{2}} \tag{2.3}$$

After an appropriate change in variables, equation (2.1) can then be rewritten as

$$I_{bs} = I_d l_c A_i \int_{E_s=E_{crit}}^{E_d} \frac{e^{-\frac{B_i}{E_s}}}{(E_s^2 - E_{crit}^2)^{\frac{1}{2}}} dE_s \tag{2.4a}$$

$$\approx \frac{I_d A_i l_c E_d}{B_i} e^{-\frac{B_i}{E_d}} \tag{2.4b}$$

where E_d is the electric field at the drain end.

$$E_d = \left[\frac{(V_{ds} - V_{dsat})^2}{l_c^2} + E_{crit}^2\right]^{\frac{1}{2}} \tag{2.5}$$

In saturation, $E_d \gg E_{crit}$, so that equation (2.5) can be approximated by

$$E_d \approx \frac{V_{ds} - V_{dsat}}{l_c} \tag{2.6}$$

Inserting equation (2.6) into equation (2.4b), we obtain the final expression for I_{bs}.

$$I_{bs} = \frac{A_i}{B_i} I_{ds} (V_{ds} - V_{dsat}) e^{-\frac{B_i l_c}{V_{ds} - V_{dsat}}} \tag{2.7}$$

Leaving A_i and B_i fixed at commonly used values of $2\times10^6\ cm^{-1}$ and $1.7\times10^6\ \frac{V}{cm}$ respectively, two parameters remain to be determined, V_{dsat} and l_c.

For short-channel devices, V_{dsat} departs from the well-known relationship $V_{dsat} = V_{gs} - V_{th}$ for long-channel devices because electrons in the channel region become velocity-saturated before V_{ds} reaches $V_{gs} - V_{th}$. The model used in BSIM to account for this behavior was derived by Sodini and Ko [6].

$$V_{dsat} = \frac{E_{crit} L (V_{gs} - V_{th})}{E_{crit} L + (V_{gs} - V_{th})} \tag{2.8}$$

where L is the channel length. E_{crit} is then extracted as a parameter from measured V_{dsat} values.

- Several approximate analytical forms for l_c have been published, including those of El-Mansy et al [3,4] and Ko [5] with a $t_{ox}^{\frac{1}{2}}$ dependency, but none can comprehensively account for dependencies on bias and size. In this work, a semi-empirical approach is established in which these dependencies are extracted directly from measured data.

2.3 Summary

It has been shown that by making liberal approximations, a relatively compact expression for the substrate current can be derived. In the next section, we will see how to implement this expression into a parameter extraction process that can accurately predict actual device behavior.

III. PARAMETER EXTRACTION

3.1 Introduction

Although the parameter extraction of the substrate current used in BSIM is firmly based on theoretical analysis, the desire to achieve more accurate modeling created the need to find empirically-based expressions, especially to predict bias voltage and size dependencies. There is no exact expression for the substrate current, and because of the many approximations that had to be made in deriving the exponential model, it was inevitable that accuracy would be sacrificed. Thus, the BSIM model uses the simple exponential model as a base to extract parameters that are generally bias- and size-dependent, and from this data BSIM produces bias- and size-independent parameters using empirically-determined analytical expressions.

The parameter extraction process is divided into two stages - one to extract E_{crit} and the other to extract l_c, from equations (2.7) and (2.8). Bias voltages to extract the substrate parameters have been carefully chosen so that leakage currents do not affect extraction. Extraction is performed for 5 V_{gs} values (starting at V_{th} + 0.3 to a maximum value of $0.8V_{dd}$ in equal increments, with V_{th} taken at maximum substrate bias) and four user-selectable V_{bs} values, in addition to measuring at a low gate bias ($V_{gs} - V_{th} = 0.3$) for each V_{bs} value. A total of 48 measurements of both I_{bs} and I_{ds} are done in a time span of approximately 5 minutes. After the measurements are completed, all bias-independent parameters are extracted using a least-squares fit routine. These bias-independent parameters are then separated into length and width dependencies in a manner similar to those used in existing BSIM models after all desired devices of a single die are measured. The resulting 33 size-independent parameters are then simply appended to the standard process file.

3.2 Extraction of E_{crit}

Recently, an empirical method to determine V_{dsat} was proposed by T.Y. Chan et al [7]. In that work, it was found that parallel contours could be plotted by plotting constant $\frac{I_{bs}}{I_{ds}}$ curves in I_{ds} - V_{ds} space (Fig. 1). V_{dsat} could then be found simply by noting the $\frac{I_{bs}}{I_{ds}}$ contour that intersected the origin at $I_{ds} = 0$ and $V_{ds} = 0$, and extracting the V_{ds} value at which this contour intersected the normal I_{ds} - V_{ds} graph.

The approach taken in the actual extraction process is as follows. A specific $\frac{I_{bs}}{I_{ds}}$ current contour is chosen internally by the program. Presently, this current ratio is set at 0.2 decades below the $\frac{I_{bs}}{I_{ds}}$ value at $V_{ds} = V_{dd}$ and maximum gate bias, or at 10^{-5}, whichever is smaller. This procedure ensures that a current ratio is chosen such that leakage current is not substantial, yet is less than the maximum current ratio measured at $V_{ds} = V_{dd}$ for all gate biases. Next, $\frac{I_{bs}}{I_{ds}}$ is measured at $V_{gs} - V_{th} = 0.3$ (Fig. 2). At this low gate bias, V_{dsat} is approximately $V_{gs} - V_{th}$. The program then notes the V_{ds} value at which the measured $\frac{I_{bs}}{I_{ds}}$ value is equal to the previously set current ratio. An offset voltage $V_{doffset}$ is then found by taking the difference between this drain voltage and $V_{dsat} \approx V_{gs} - V_{th}$ (Fig. 2). Now, because the $\frac{I_{bs}}{I_{ds}}$ current ratio contours are parallel for all gate bias. V_{dsat} for other gate voltages can be found simply by noting the V_{ds} value at which $\frac{I_{bs}}{I_{ds}}$ is equal to the preset current ratio, and then subtracting $V_{doffset}$ from it. This difference will equal V_{dsat} for that specific gate voltage. Generally, $V_{doffset}$ changes for different body biases so that the low gate bias measurement must be done for each body bias value.

Once the V_{dsat} values are extracted, they are fitted to the analytical model mentioned previously and repeated here for reference:

$$V_{dsat} = \frac{E_{crit} L (V_{gs} - V_{th})}{E_{crit} L + (V_{gs} - V_{th})} \tag{3.1}$$

After measurements on various wafers, it was found that the V_{dsat} values obtained could accurately be predicted by making the critical electric field parameter E_{crit} dependent on both gate and body bias while using the first-order threshold voltage model.

$$V_{th} = VFB + PHIF2 + K1\sqrt{(PHIF2 - V_{bs})} - K2(PHIF2 - V_{bs}) \tag{3.2}$$

VFB, PHIF2, K1, and K2 are parameters extracted in the normal I_{ds} extraction process [3]. The best fit was obtained by using a linear fit in terms of the bias voltages.

$$E_{crit}(V_{bs}, V_{gs}) = E_{crit0} + E_{critg} V_{gs} + E_{critb} V_{bs} \tag{3.3}$$

Figs. 3 and 4 clearly show the linear E_{crit} dependency to V_{gs} and V_{bs}. The increase in E_{crit} with increasing gate or substrate bias correlates with previously established results [6]. In that work, this increase is attributed to electron mobility degradation caused by vertical fields, which in turn causes an increase of the lateral field necessary to velocity-saturate the channel electrons.

An additional modification was found to be needed to accurately extract the E_{crit} parameters. Because equation (3.1) becomes inaccurate for low gate bias, it was found that E_{crit} actually decreased before increasing when plotted with increasing gate bias. Thus the program ignores all data that occur before this minima and uses data points only after it senses a positive slope in E_{crit}.

Fig. 5 compares the simulated and measured value of V_{dsat} using this method. As can be seen, the predicted values correlate well with measured behavior.

3.3 Extraction of l_c

Once all measured V_{dsat} values are known, l_c can be extracted from measured $\frac{I_{bs}}{I_{ds}}$ values from equation (2.7).

$$\frac{I_{bs}}{I_{ds}} = \frac{A_i}{B_i}(V_{ds} - V_{dsat})\, e^{-\frac{B_i l_c}{(V_{ds} - V_{dsat})}} \tag{3.4}$$

A_i and B_i, constants from the electron impact ionization coefficient α_n, are set at well-adopted values of $2\times10^6\ cm^{-1}$ and $1.7\times10^6\ \frac{V}{cm}$ as mentioned previously.

Extensive measurements were done on NMOS enhancement devices for various processes, with device sizes ranging from 4 μm to 100 μm in width, and 1.5 μm to 20 μm in length. All data could not be accurately predicted without making l_c bias dependent. After separating the various bias effects, the best form for l_c was found to be

$$l_c(V_{bs}, V_{gs}, V_{ds}) = \sqrt{t_{ox}}\,[l_1 + l_2(\frac{1}{V_{gs}+2})] \tag{3.5}$$

where

$$l_1 = l_{c0} + l_{c1}(\frac{1}{V_{bs}-4}) + [l_{c2} + l_{c3}(\frac{1}{V_{bs}-4})]V_{ds} \tag{3.6a}$$

$$l_2 = l_{c4} + l_{c5}(\frac{1}{V_{bs}-4}) + [l_{c6} + l_{c7}(\frac{1}{V_{bs}-4})]V_{ds} \tag{3.6b}$$

The "2" in the expression $\frac{1}{V_{gs}+2}$ and the "4" in $\frac{1}{V_{bs}-4}$ were determined so that the expressions would be valid for V_{gs} and $V_{bs} = 0$ while giving a good fit to data measured from a wide variety of wafers. All data taken below a preset drain bias, $V_{dthresh}$, is ignored so that leakage current effects will not alter the extraction. $V_{dthresh}$ is set at 0.2 volts greater than the drain voltage where $\frac{I_{bs}}{I_{ds}}$ falls to 10^{-8} on the maximum gate bias contour.

The motivation behind using the forms in equations (3.5) and (3.6) can be seen from

Figs. 6 - 8. These plots show the effect of gate, drain, and substrate bias on extracted values of l_c. The importance of the cross-term parameters l_{c3} and l_{c7} can be realized by looking at Figs. 7 and 8. Note that the slope of the measured curve is dependent on the third variable, V_{bs}. Thus, a simple linear relationship is not possible.

- The inverse V_{gs} dependence of l_c is used to take into account an observable substantial decrease of I_{bs} (and therefore a non-linear increase of l_c) for low $V_{gs} - V_{th}$ (Fig. 6). This effect as well as the inverse V_{bs} dependence may be qualitatively explained as being caused by the modulation of the inversion layer thickness of the channel electrons as a secondary effect in addition to the normal decrease in channel charge. As either gate or substrate bias decreases, more electrons flow in a lower field region further away from the silicon-silicon dioxide interface. This results in less electrons experiencing the critical field necessary for impact ionization, and therefore a greater decrease in substrate current than that predicted by theory is observed. This effect is more pronounced for shorter channel lengths and larger drain voltages. At present, no theoretical derivation for this behavior has been published.

3.4 Creating Size-Independent Parameters

In parallel with the existing BSIM models, each of the 11 parameters are decomposed into three size-independent parameters using the following relation:

$$P_i = P_0 + \frac{P_L}{L_{MK} - \Delta L} + \frac{P_W}{W_{MK} - \Delta W} \tag{3.7}$$

L_{MK} and W_{MK} are mask length and width, and ΔL and ΔW account for any process bias that may be present. The 33 size-independent parameters, with other statistical information, are then stored in lines 29 to 39 of the process file. These parameters are then used to simulate the I-V characteristics in the graphics playback mode.

3.5 Summary

After much analysis, it can be seen that theoretical derivations alone are not sufficient to explain completely and accurately the device behavior observed. It is therefore necessary to empirically determine an expression that is strongly based upon theory but can also simulate accurately actual device characteristics. In this way, device behavior can be predicted before the theory of that behavior has been firmly established. The accuracy of this parameter extraction process is presented in the following section.

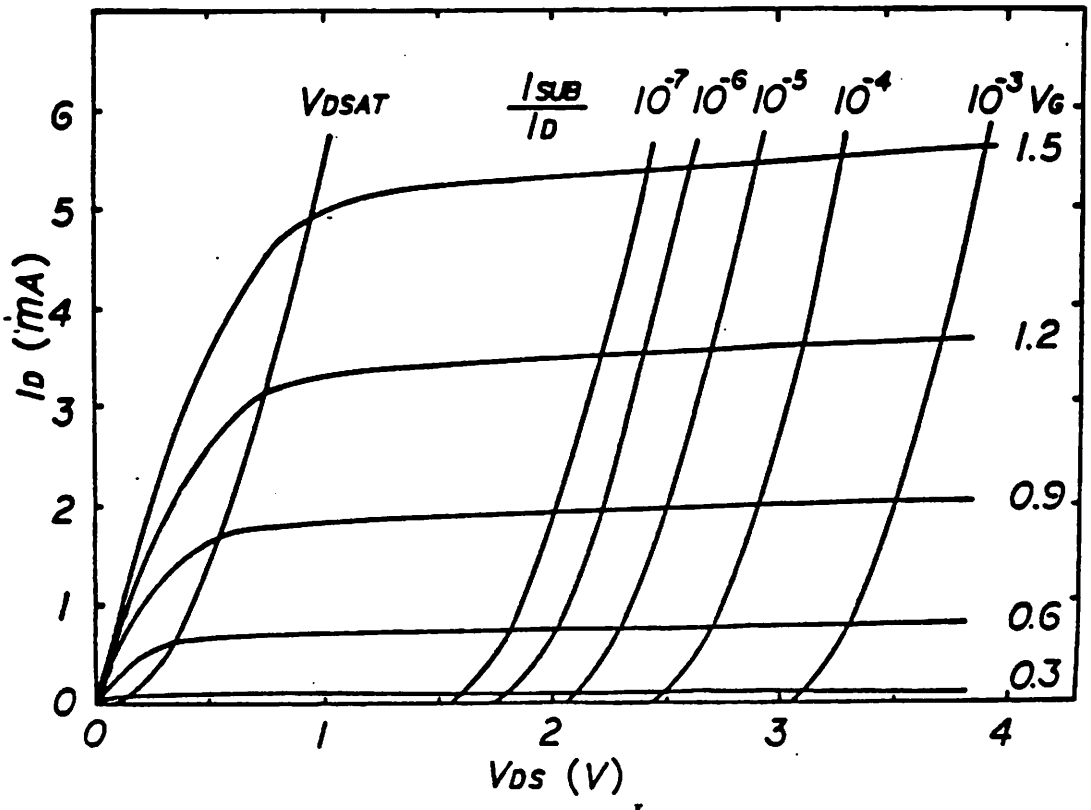


Fig. 1 Parallel contours of constant $\frac{I_{bs}}{I_{ds}}$ (from T.Y. Chan et al. [7]).

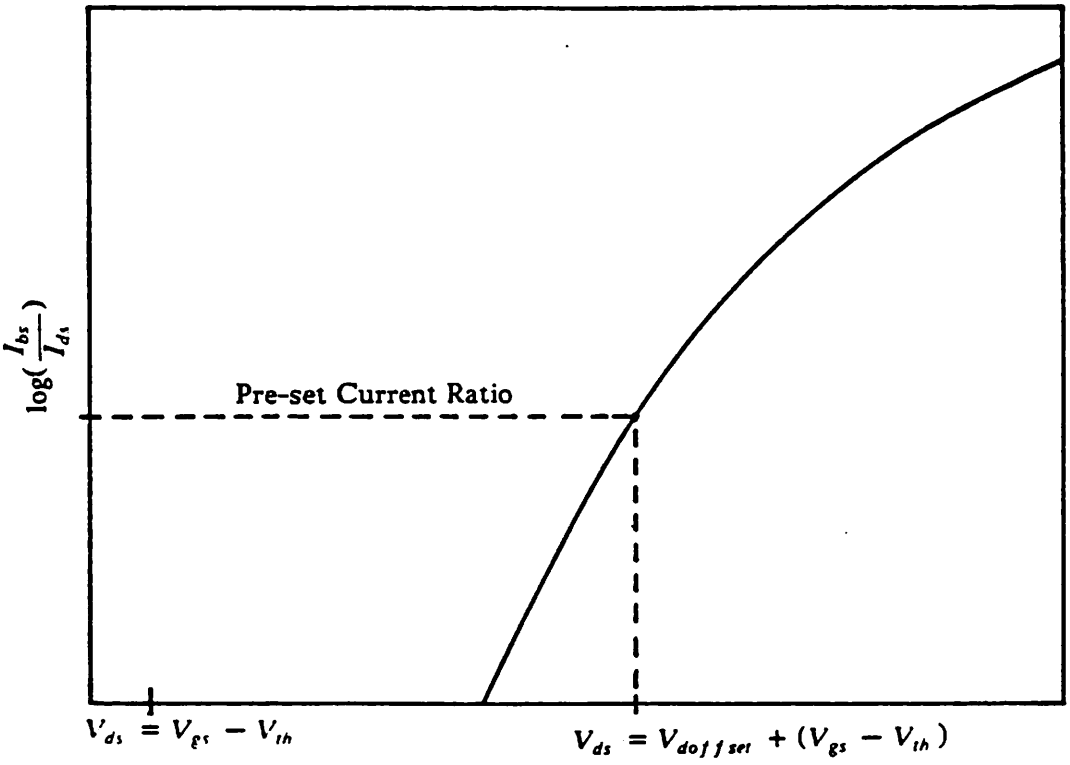


Fig. 2 Calculation of $V_{doffset}$.

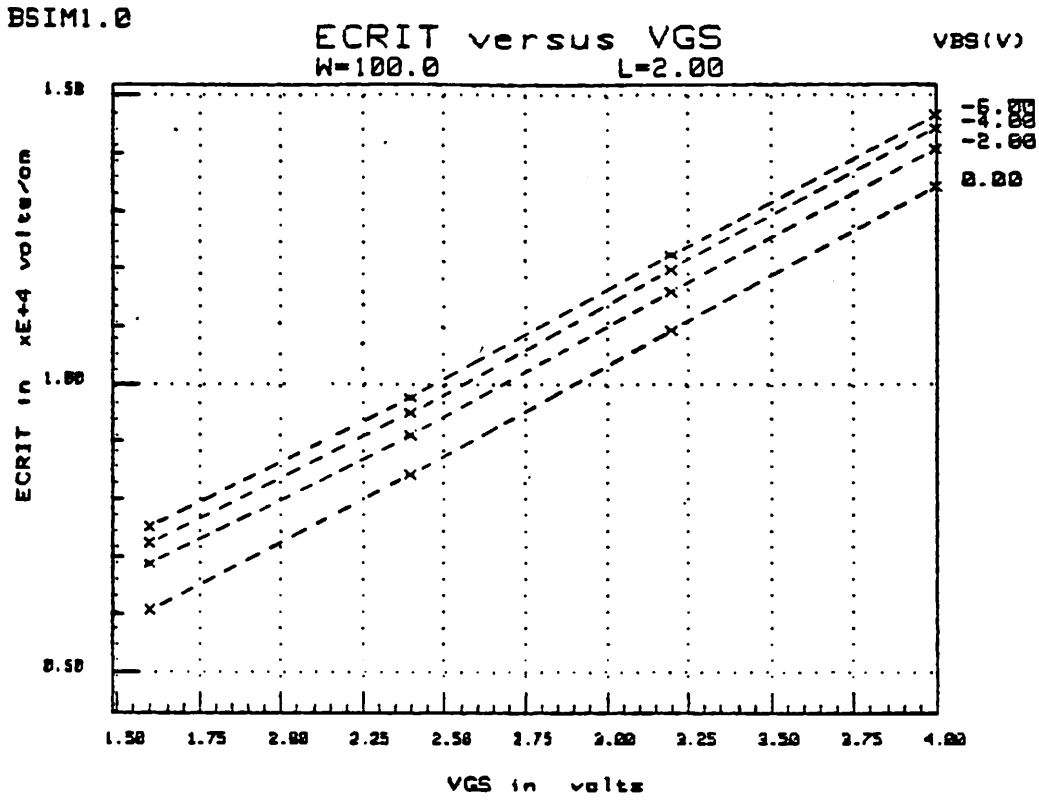


Fig. 3 E_{crit} versus V_{gs} (Reticon device, W = 100 μm , L = 2 μm).

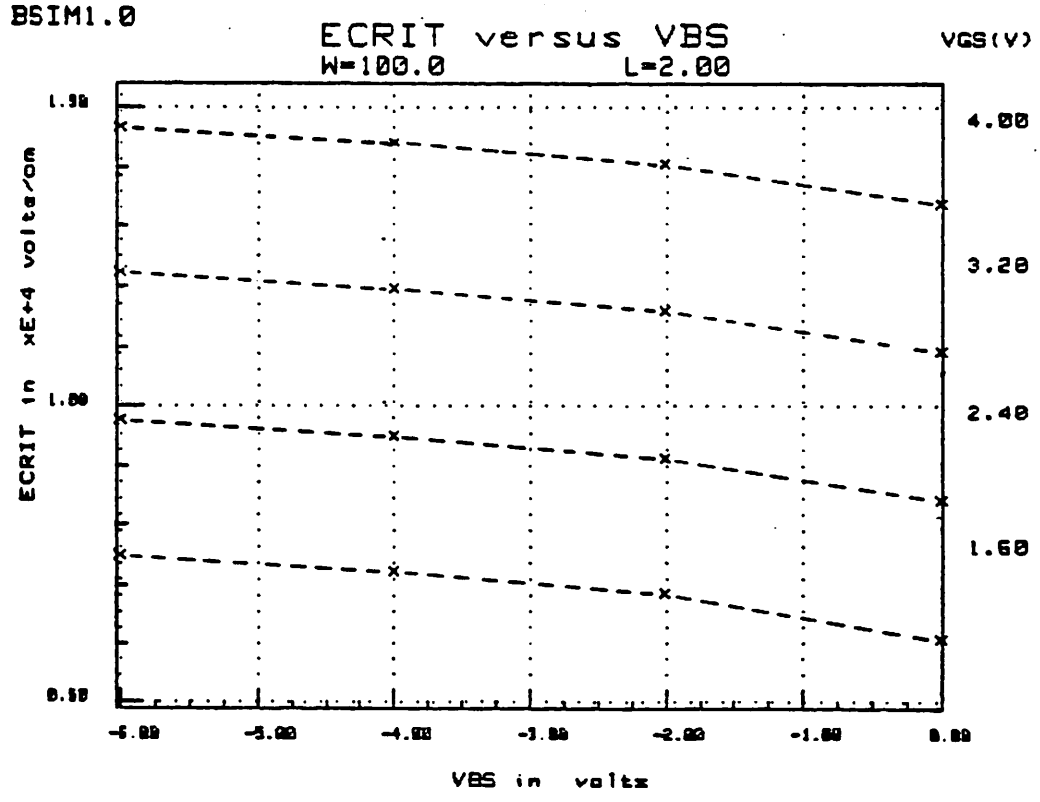


Fig. 4 E_{crit} versus V_{bs} (Reticon device, W = 100 μm , L = 2 μm).

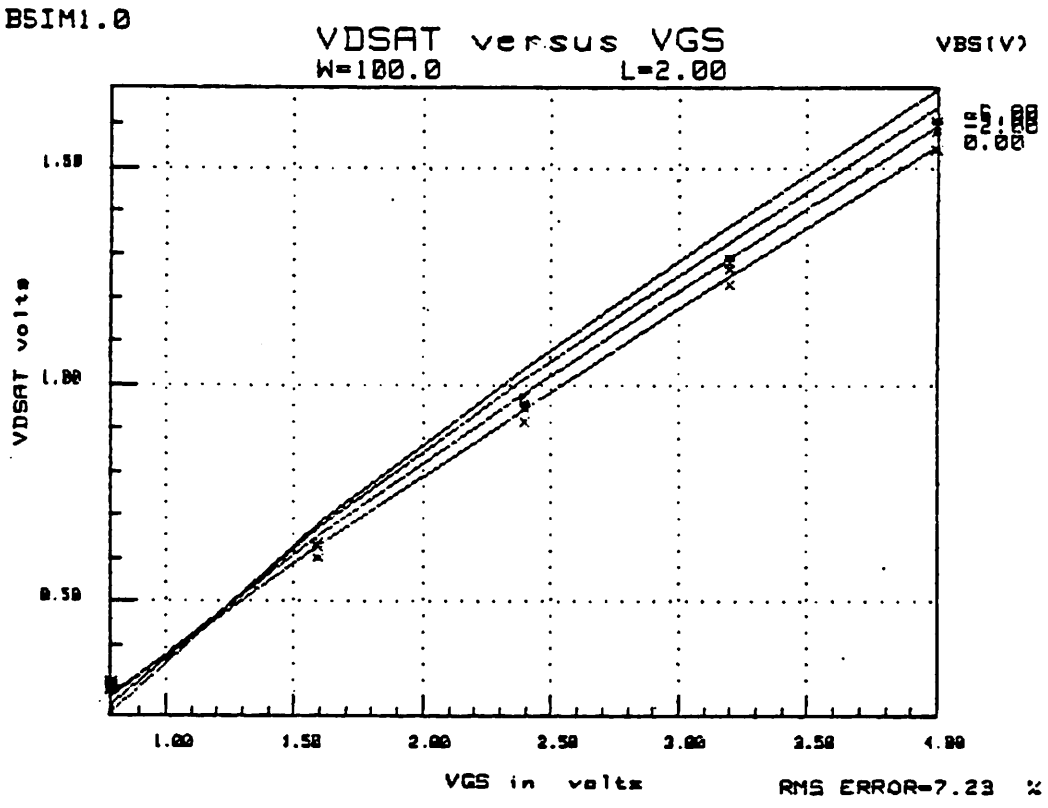


Fig. 5 V_{dsat} versus V_{gs}. with V_{bs} as the third parameter (Reticon device, W = 100 μm, L = 2 μm).

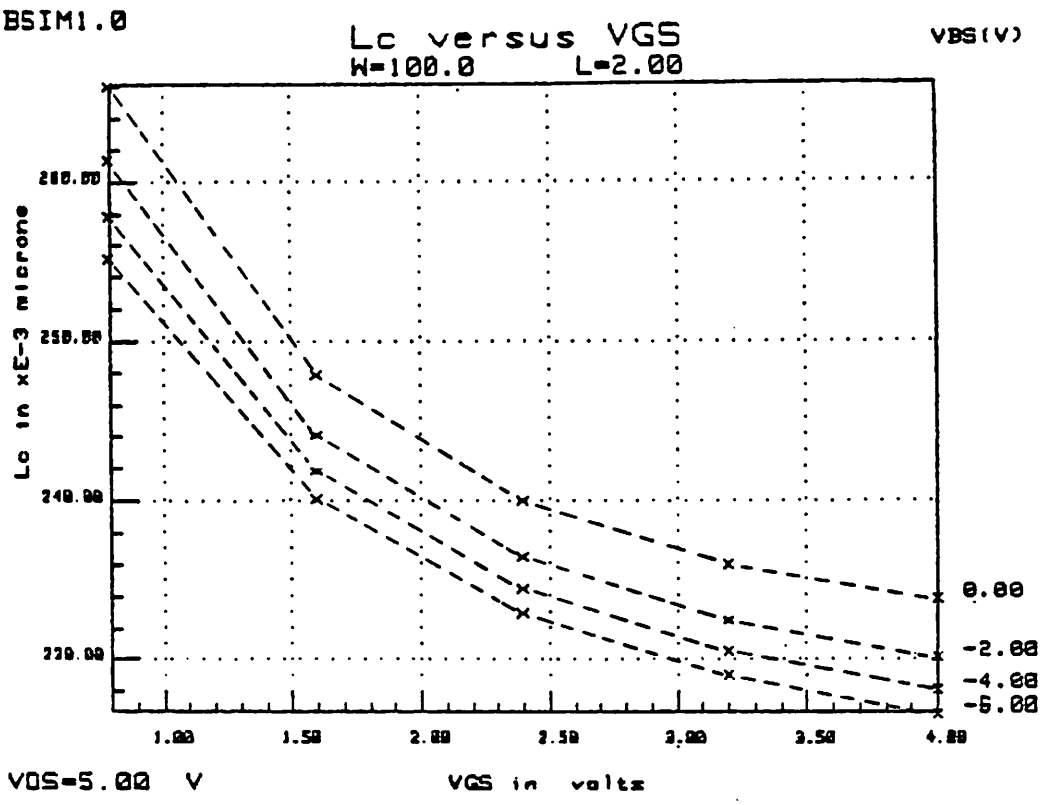


Fig. 6 l_c versus V_{gs}, with V_{bs} as the third parameter (Reticon device. W = 100 μm. L = 2 μm).

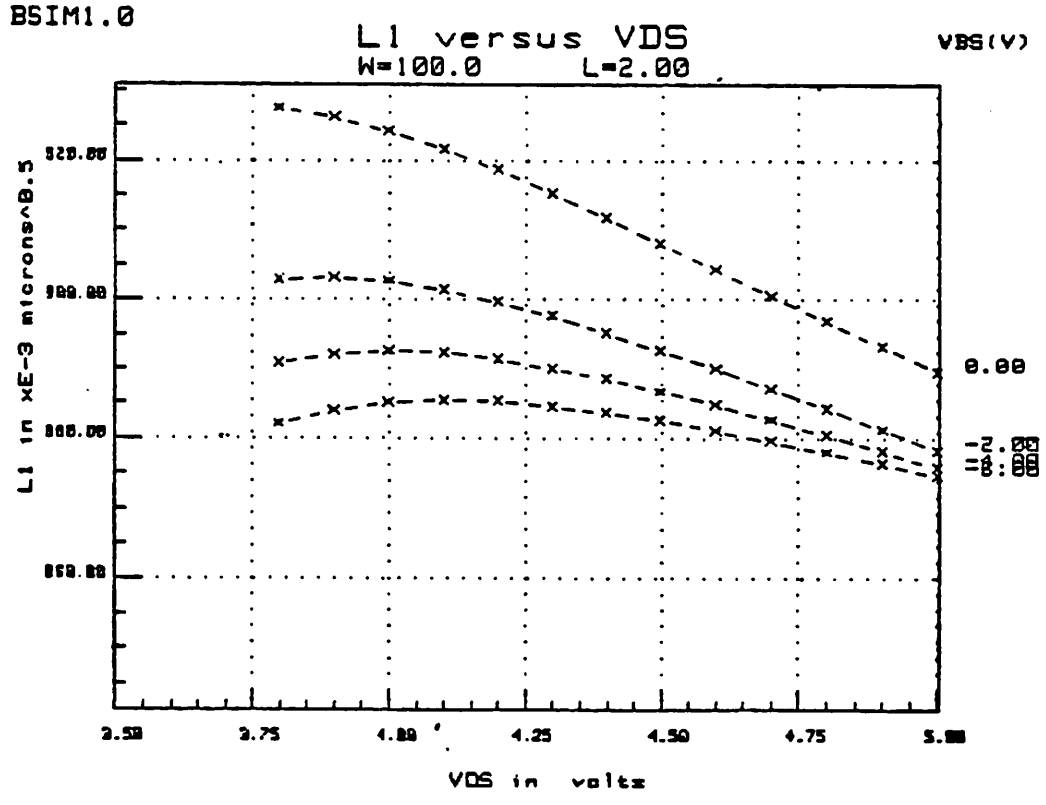


Fig. 7 l_1 versus V_{ds}, with V_{bs} as the third parameter (Reticon device. W = 100 μm. L = 2 μm).

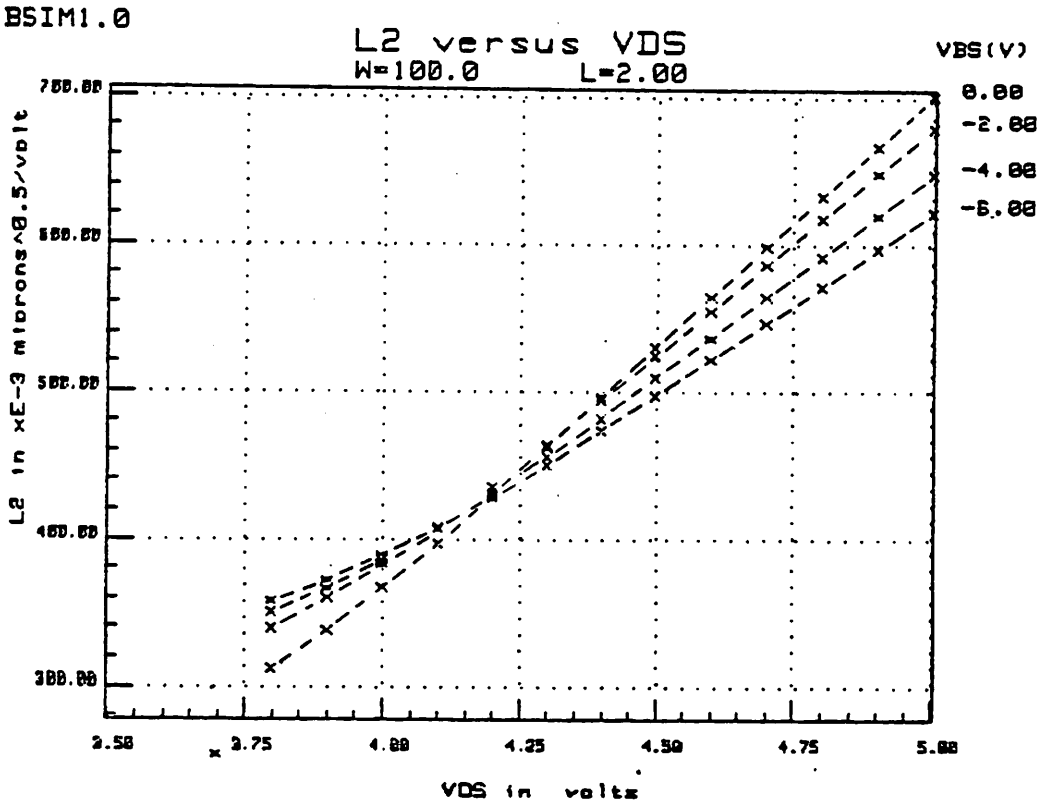


Fig. 8 l_2 versus V_{ds}, with V_{bs} as the third parameter (Reticon device, W = 100 μm, L = 2 μm).

IV. EXPERIMENTAL RESULTS

Experimental measurements to test the accuracy of the extraction process were performed on NMOS enhancement devices fabricated by various processes. The results presented here are taken from conventional devices fabricated by Advanced Micro Devices (AMD), with an oxide thickness of 285 angstroms, an average substrate doping of $5\times10^{14}\ cm^{-3}$, and source and drain diffusion junction depths of $0.3\mu m$, and from conventional devices made by Reticon, with an oxide thickness of 530 angstroms and extracted average doping of $2.8\times10^{15}\ cm^{-3}$. In addition, the results of simulating substrate current in lightly-doped drain (LDD) structures are also presented from devices fabricated by AMD with the same specifications as that of their conventional devices, with lightly-doped n- region junction depths half as deep as the source and drain diffusion junction depths. The devices measured have dimensions (in microns) of 8/5, 6/5, 4/5, 4/4, 4/3, 4/2, and 4/1.5 for the AMD conventional devices, 100/5, 100/4, 100/3, 100/2, and 4/4 for the Reticon devices, and 20/2.25, 6/2.25, 4/2.25, 4/3, 4/2, and 4/1.5 for the AMD LDD devices. One process file per die is used to simulate current characteristics of all devices on the same die.

All measurements are accomplished using a Hewlett Packard 9836 Computer acting as a controller through the HPIB to a 4145A Parametric Analyzer, which in turn is connected to a probe station with metal shielding. A detailed description of the measurement setup is given in [2].

Two types of plots are available for the substrate current in graphics playback, $\log(\frac{I_{bs}}{I_{ds}})$ versus V_{ds} and I_{bs} versus V_{gs}. Both types are presented in the following figures.

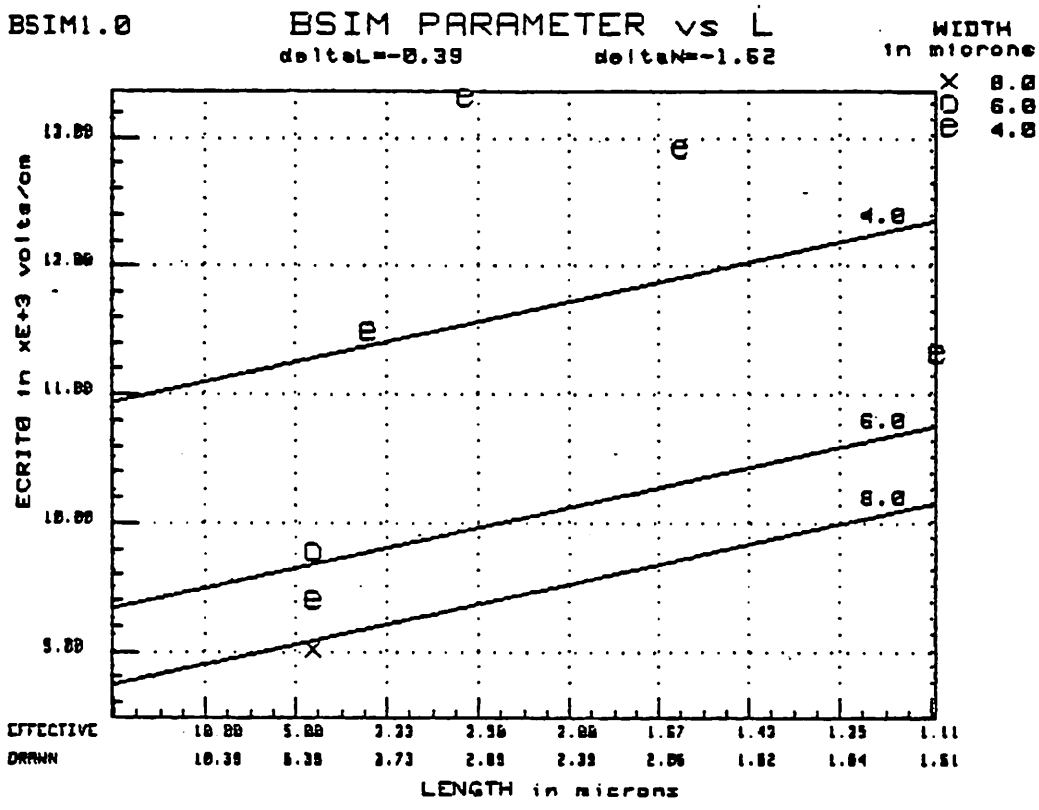
The first several figures present selected data from AMD conventional devices. Figs. 9 - 19 display each of the 11 substrate parameters for all seven device tested. Figs. 20 - 23 show the actual $\log(\frac{I_{bs}}{I_{ds}})$ plots, while Figs. 24 and 25 show I_{bs} versus V_{gs} plots for the

4/1.5 device.

Figs. 26 through 38 display substrate current data and simulated playback of selected Reticon and AMD LDD devices in similar fashion.

Fig. 39 shows the process file that was generated for the AMD conventional devices. The substrate parameters appear after the three consecutive row of zeroes in the first four columns (subthreshold extraction was not done).

From the figures, it can be seen that the simulated curves predict quite closely the measured current characteristics. The fact that the simulations are accurate for various device sizes using a single process file adds confidence to the correctness of the model.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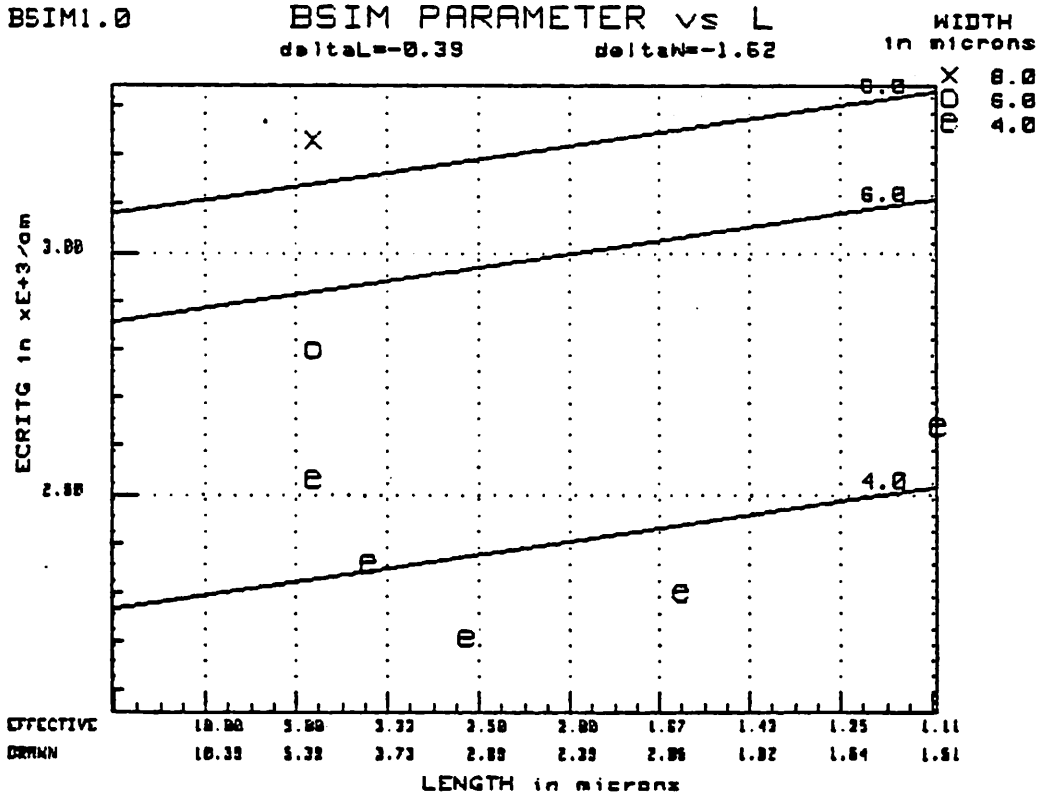
BSIM PARAMETER vs L
deltaL=-0.39
deltaW=-1.62
WIDTH
in microns
X 8.0
O 6.0
e 4.0
ECRITO in xE+3 volts/cm
13.00
12.00
11.00
10.00
9.00
4.0
6.0
8.0
EFFECTIVE 10.00 5.00 3.33 2.50 2.00 1.67 1.43 1.25 1.11
DRAWN 10.39 5.39 3.73 2.89 2.39 2.06 1.82 1.64 1.51
LENGTH in microns

Fig. 9


BSIM1.0
BSIM PARAMETER vs L
deltaL=-0.39
deltaW=-1.62
WIDTH
in microns
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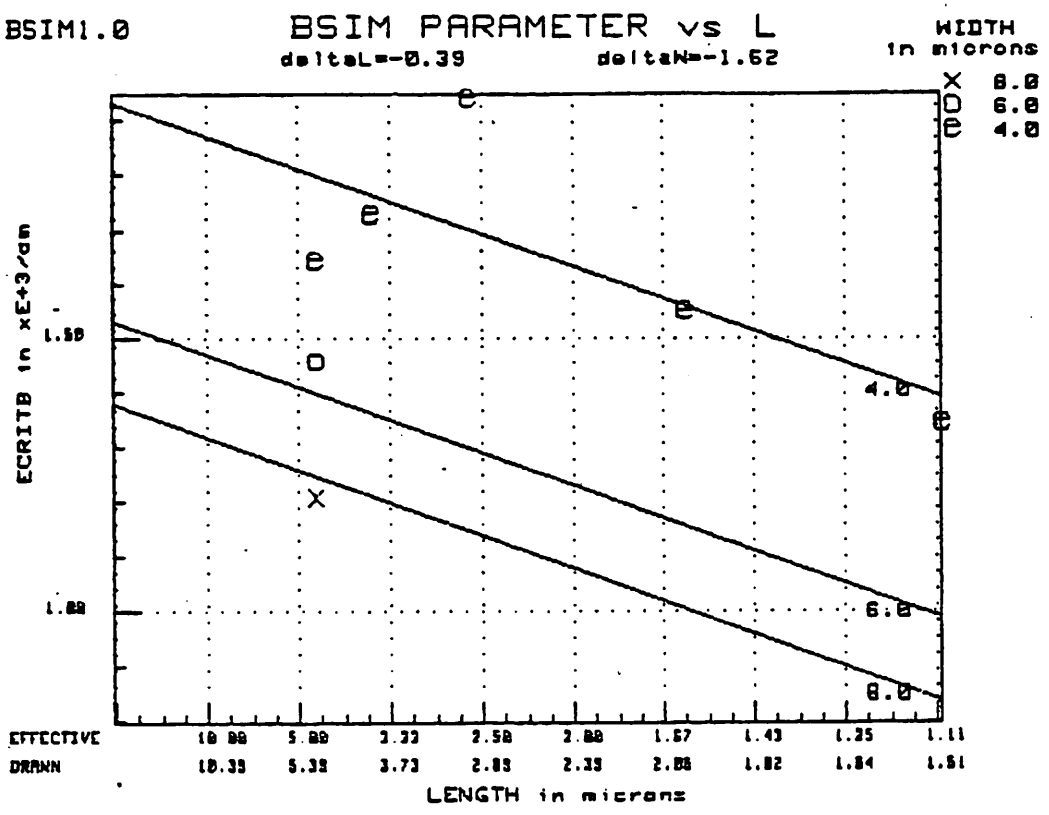
O 6.0
e 4.0
ECRITG in xE+3/cm
3.00
2.00
8.0
6.0
4.0
EFFECTIVE 10.00 5.00 3.33 2.50 2.00 1.67 1.43 1.25 1.11
DRAWN 10.39 5.39 3.73 2.89 2.39 2.06 1.82 1.64 1.51
LENGTH in microns

Fig. 10


BSIM1.0
BSIM PARAMETER vs L
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deltaW=-1.62
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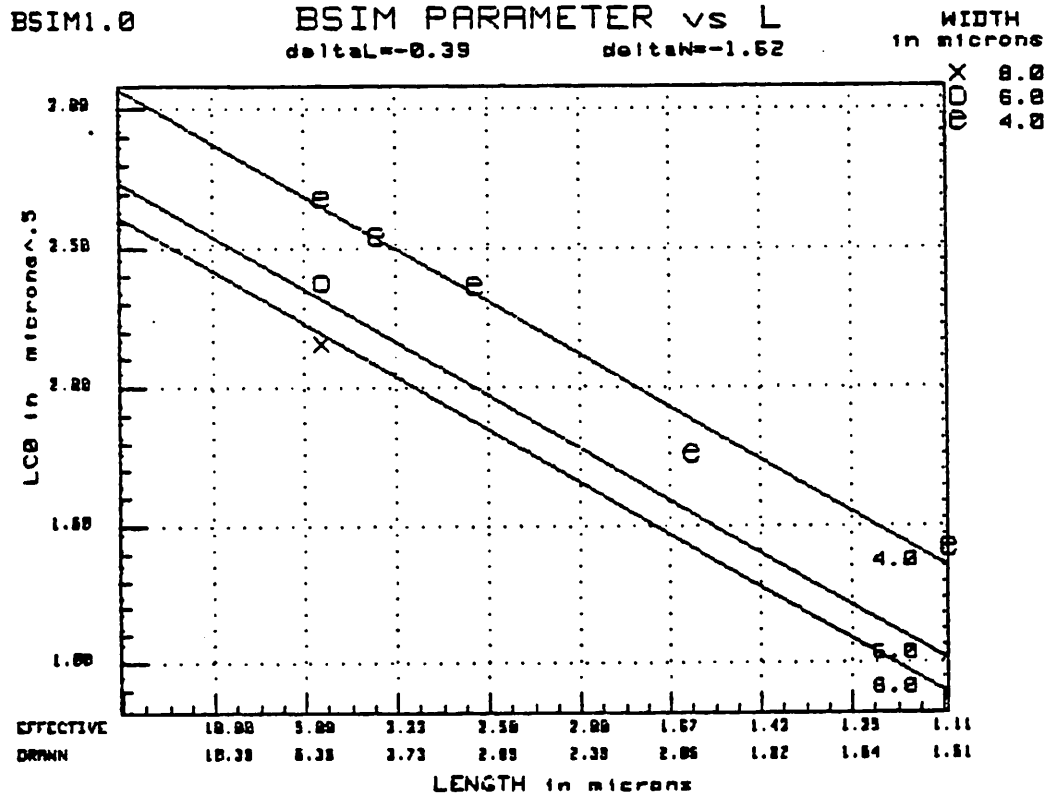
in microns
X 8.0
D 6.0
e 4.0
ECRITB in xE+3/cm
1.50
1.00
4.0
6.0
8.0
EFFECTIVE
DRAWN
10.00 5.00 3.33 2.50 2.00 1.67 1.43 1.25 1.11
10.33 5.33 3.73 2.83 2.33 2.06 1.82 1.64 1.51
LENGTH in microns

Fig. 11


BSIM1.0
BSIM PARAMETER vs L
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deltaW=-1.62
WIDTH
in microns
X 8.0
D 6.0
e 4.0
LC0 in microns^.5
3.00
2.50
2.00
1.50
1.00
4.0
6.0
8.0
EFFECTIVE
DRAWN
10.00 5.00 3.33 2.50 2.00 1.67 1.43 1.25 1.11
10.33 5.33 3.73 2.83 2.33 2.06 1.82 1.64 1.51
LENGTH in microns

Fig. 12

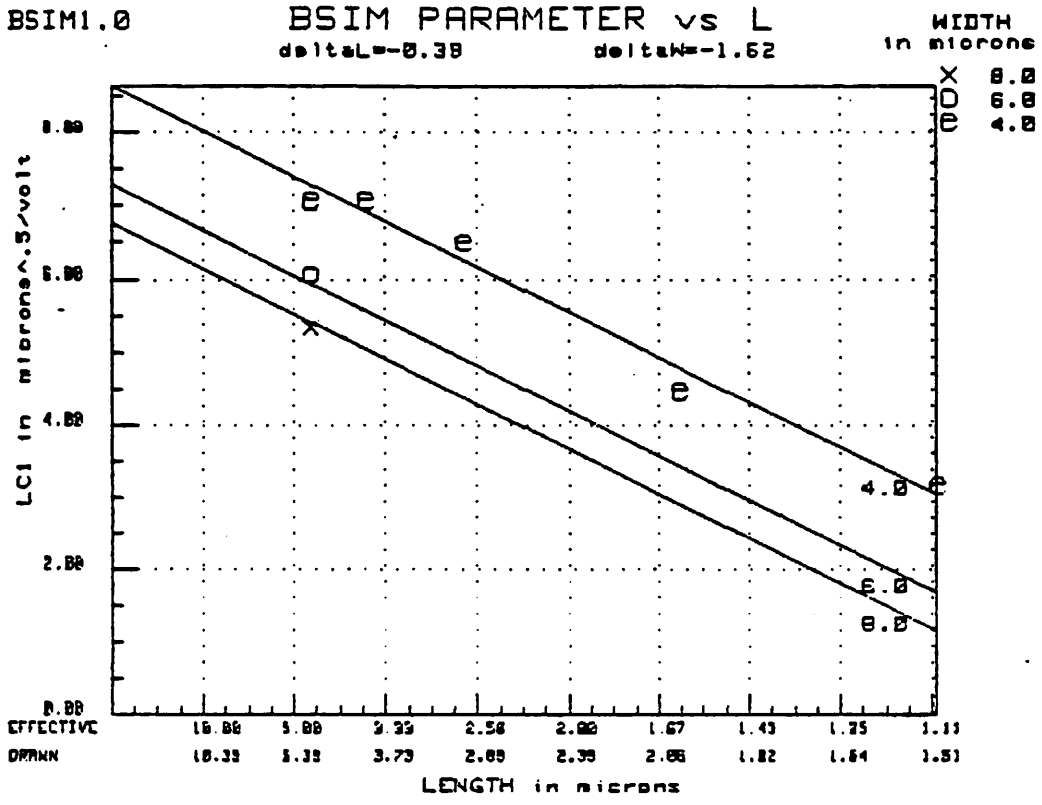
BSIM1.0
BSIM PARAMETER vs L
deltaL=-0.38
deltaW=-1.62
WIDTH
in microns
X 8.0
D 6.0
E 4.0
LC1 in microns^.5/volt
8.00
6.00
4.00
2.00
0.00
4.0
6.0
8.0
EFFECTIVE
DRAWN
LENGTH in microns

Fig. 13

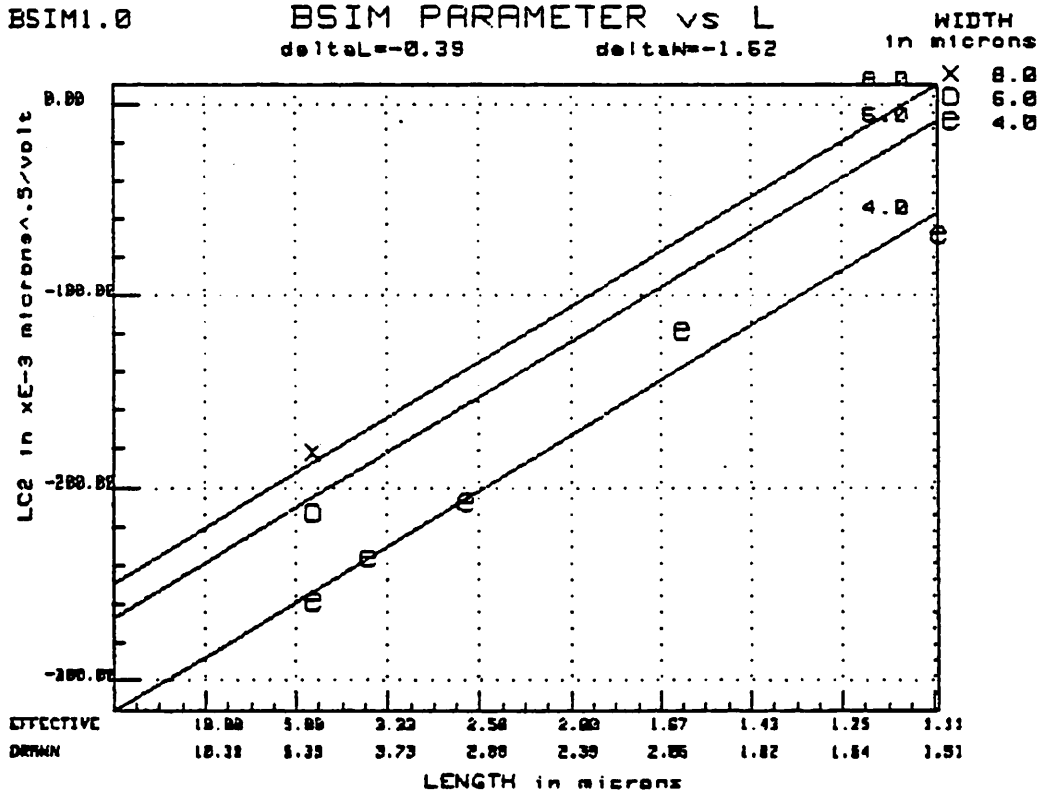
BSIM1.0
BSIM PARAMETER vs L
deltaL=-0.38
deltaW=-1.62
WIDTH
in microns
X 8.0
D 6.0
E 4.0
LC2 in xE-3 microns^.5/volt
0.00
-100.00
-200.00
-300.00
4.0
EFFECTIVE
DRAWN
LENGTH in microns

Fig. 14

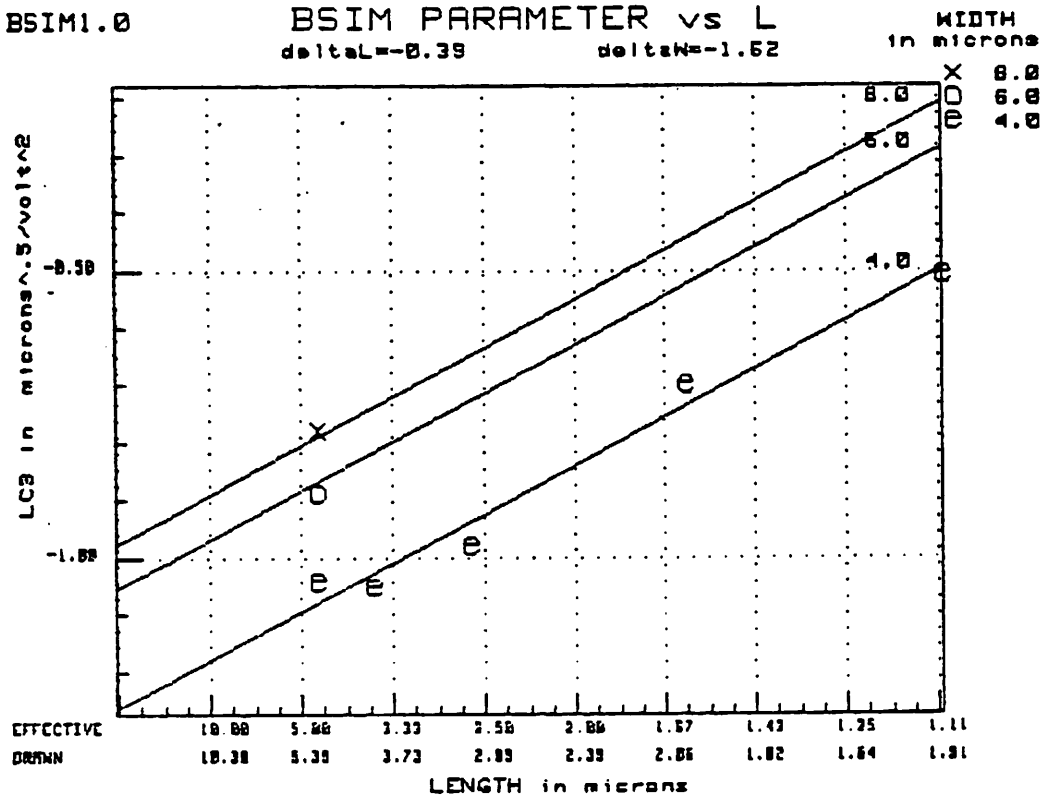
BSIM1.0
BSIM PARAMETER vs L
deltaL=-0.39
deltaW=-1.62
WIDTH
in microns
X 8.0
O 6.0
e 4.0
8.0
6.0
4.0
LC3 in microns^.5/volt^2
-0.50
-1.00
EFFECTIVE
DRAWN
LENGTH in microns

Fig. 15

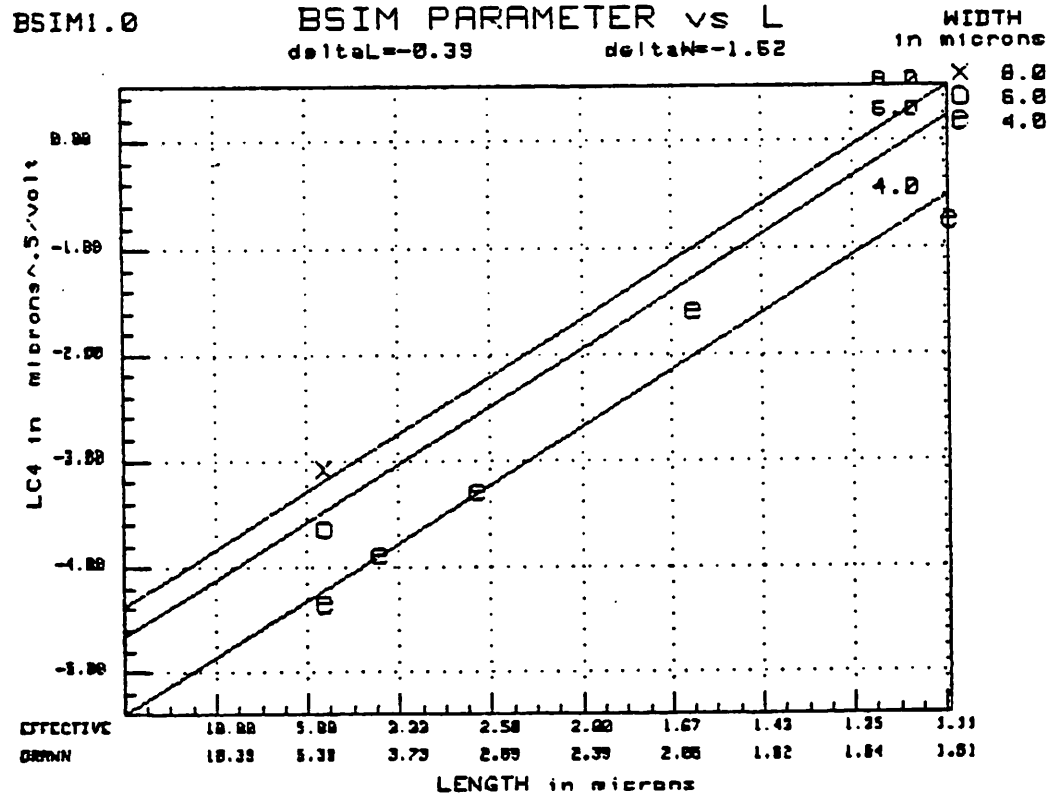
BSIM1.0
BSIM PARAMETER vs L
deltaL=-0.39
deltaW=-1.62
WIDTH
in microns
X 8.0
O 6.0
e 4.0
6.0
4.0
LC4 in microns^.5/volt
-1.00
-2.00
-3.00
-4.00
EFFECTIVE
DRAWN
LENGTH in microns

Fig. 16

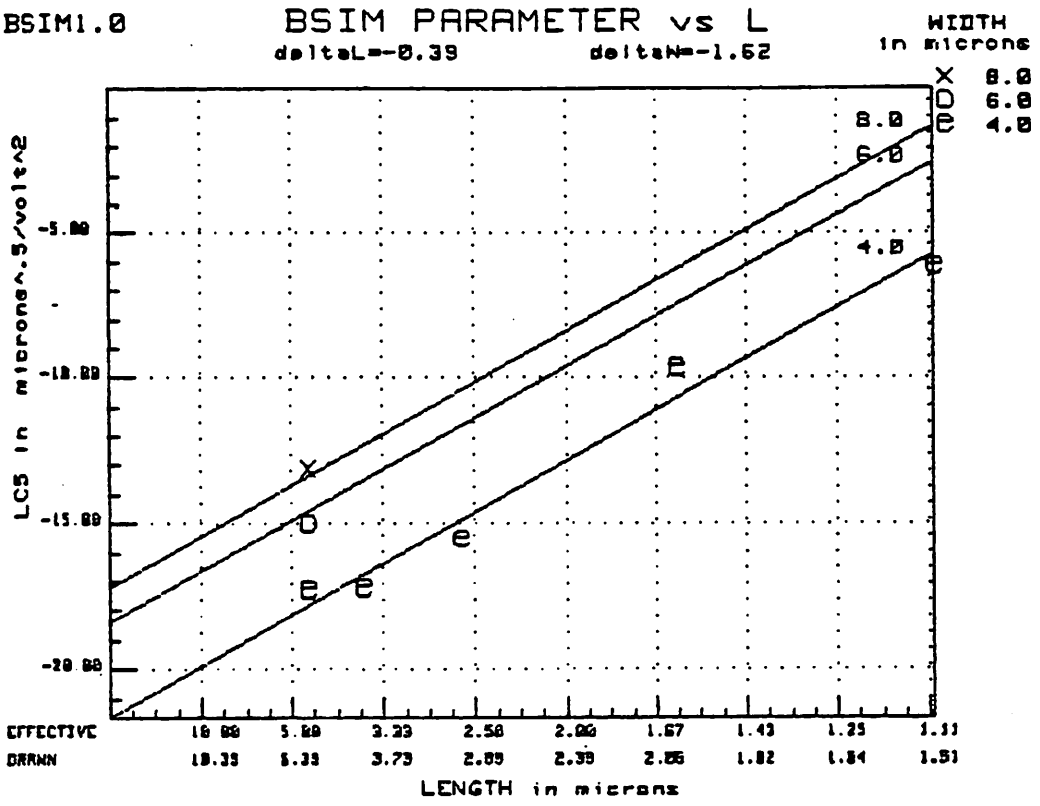
BSIM1.0
BSIM PARAMETER vs L
deltaL=-0.39
deltaW=-1.62
WIDTH
in microns
X 8.0
D 6.0
e 4.0
8.0
6.0
4.0
LC5 in microns^.5/volt^2
-5.00
-10.00
-15.00
-20.00
EFFECTIVE
DRAWN
10.00 5.00 3.33 2.50 2.00 1.67 1.43 1.25 1.11
10.33 5.33 3.79 2.89 2.39 2.05 1.82 1.64 1.51
LENGTH in microns

Fig. 17

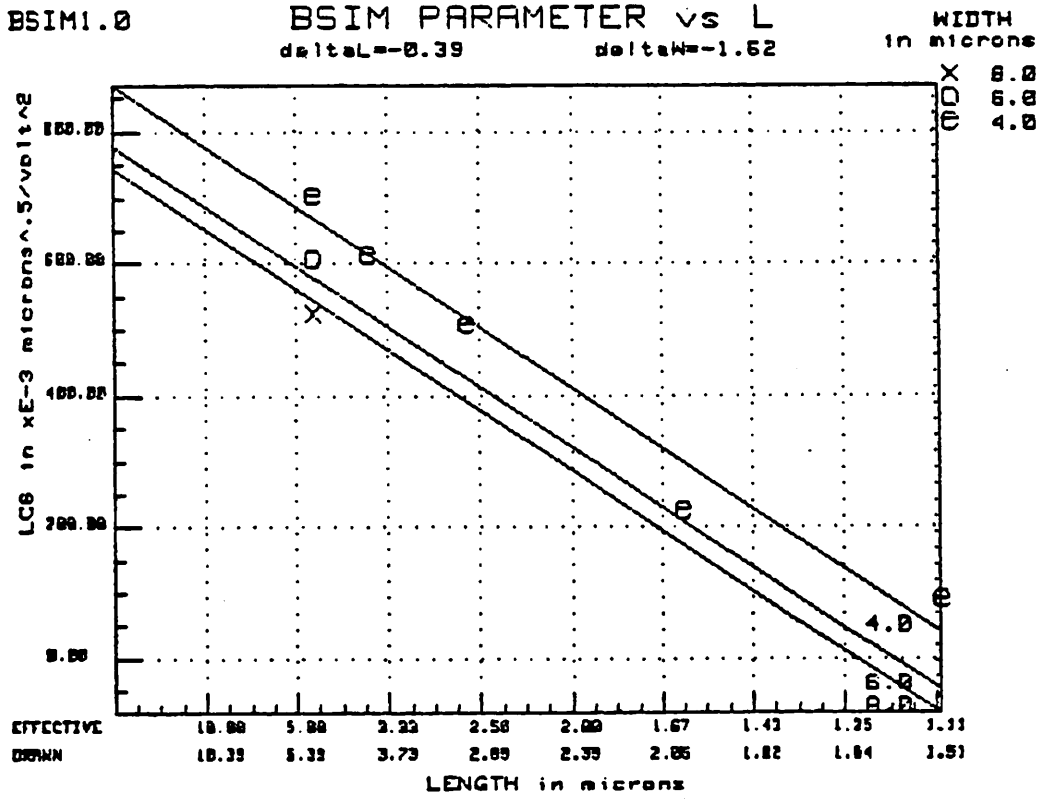
BSIM1.0
BSIM PARAMETER vs L
deltaL=-0.39
deltaW=-1.62
WIDTH
in microns
X 8.0
D 6.0
e 4.0
LC6 in xE-3 microns^.5/volt^2
800.00
600.00
400.00
200.00
0.00
4.0
6.0
8.0
EFFECTIVE
DRAWN
10.00 5.00 3.33 2.50 2.00 1.67 1.43 1.25 1.11
10.33 5.33 3.79 2.89 2.39 2.05 1.82 1.64 1.51
LENGTH in microns

Fig. 18

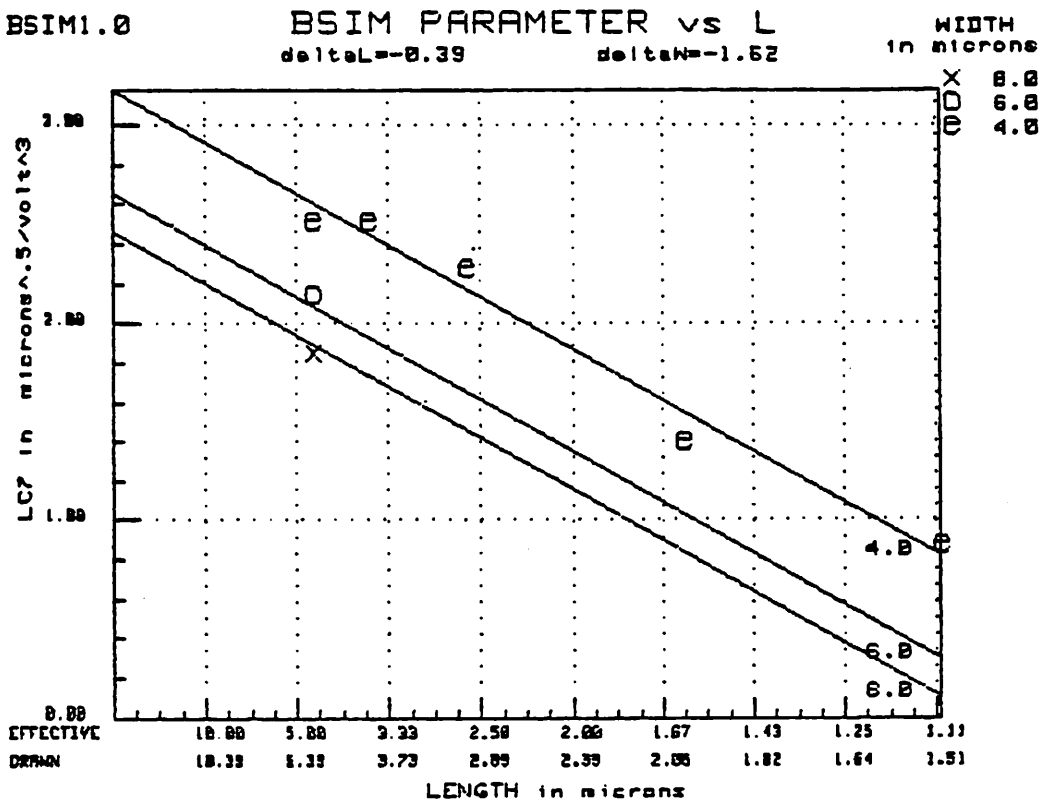
BSIM1.0
BSIM PARAMETER vs L
deltaL=-0.39
deltaW=-1.62
WIDTH
in microns
8.0
6.0
4.0
LC? in microns^.5/volt^3
3.00
2.00
1.00
0.00
4.0
6.0
6.0
EFFECTIVE
DRAWN
10.00
5.00
3.33
2.50
2.00
1.67
1.43
1.25
1.11
10.33
5.33
3.73
2.89
2.39
2.06
1.82
1.64
1.51
LENGTH in microns

Fig. 19

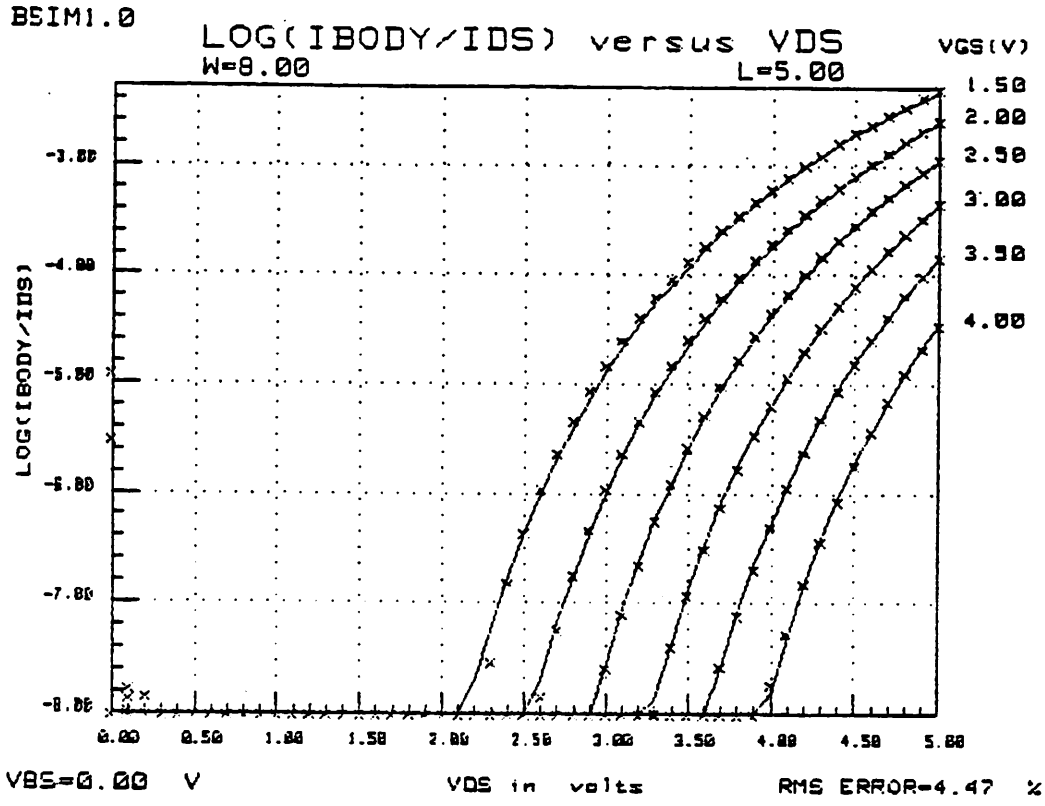

Fig. 20 AMD conventional device. $V_{bs} = 0$ ($W = 8\ \mu m$, $L = 5\ \mu m$).

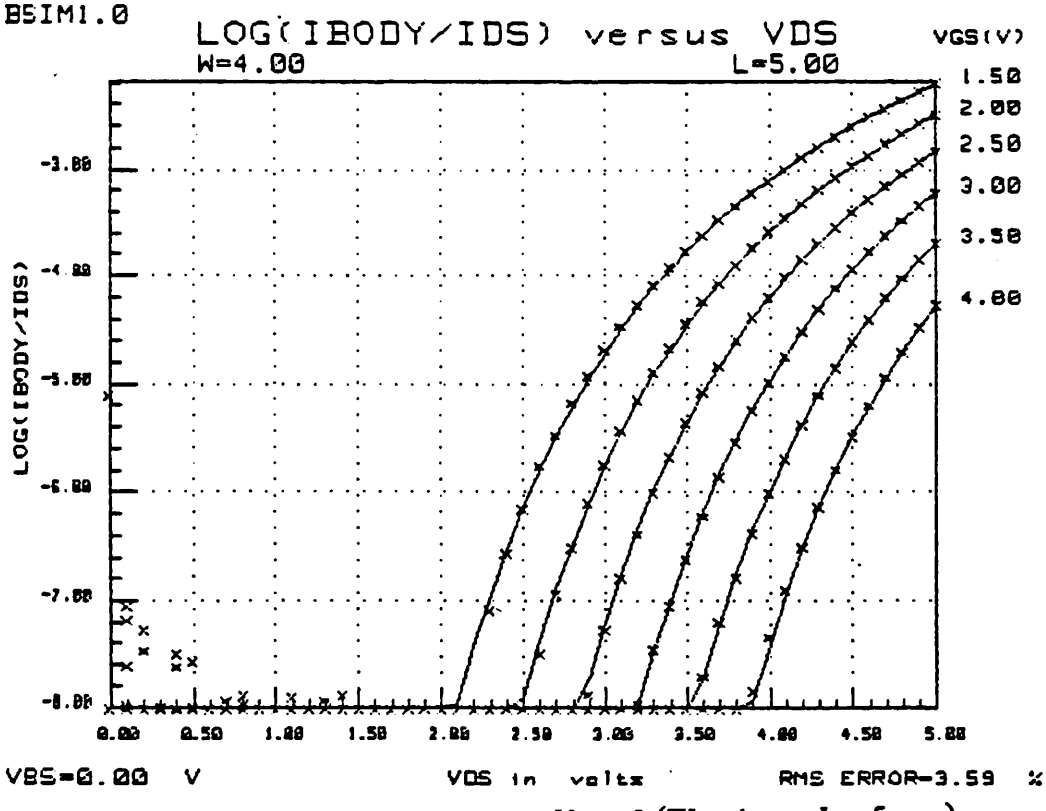

Fig. 21 AMD conventional device. $V_{bs} = 0$ ($W = 4\ \mu m$, $L = 5\ \mu m$).

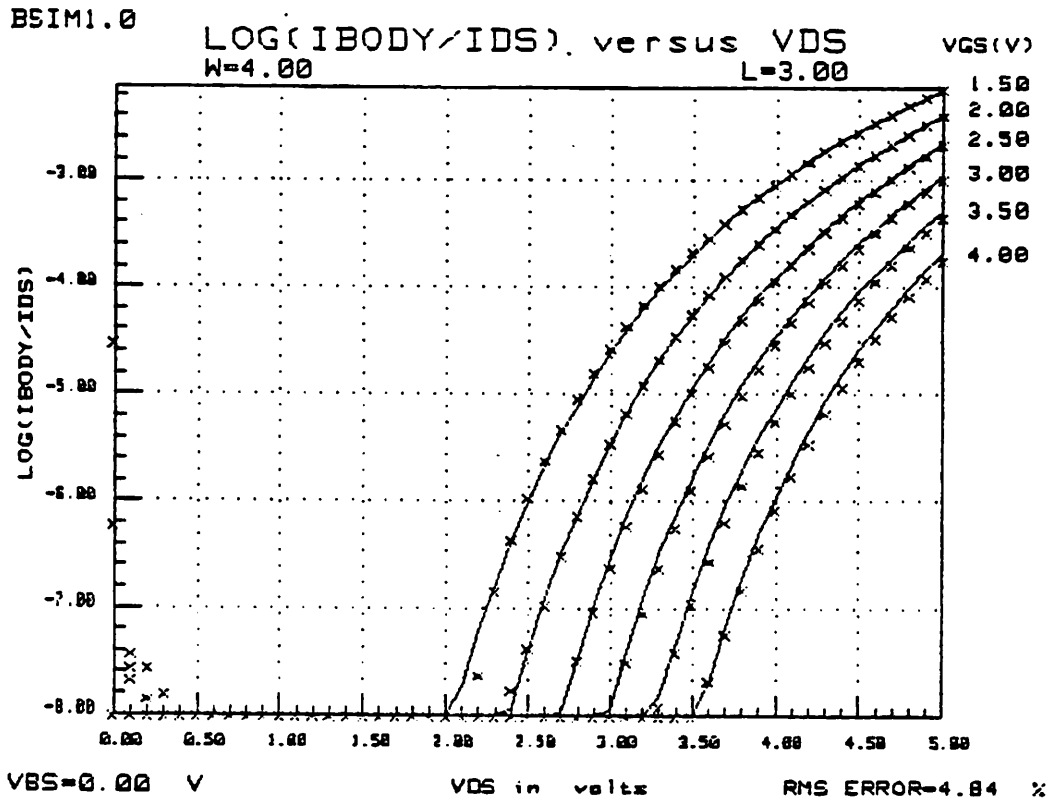

Fig. 22 AMD conventional device. $V_{bs} = 0$ (W = 4 μm , L = 3 μm).

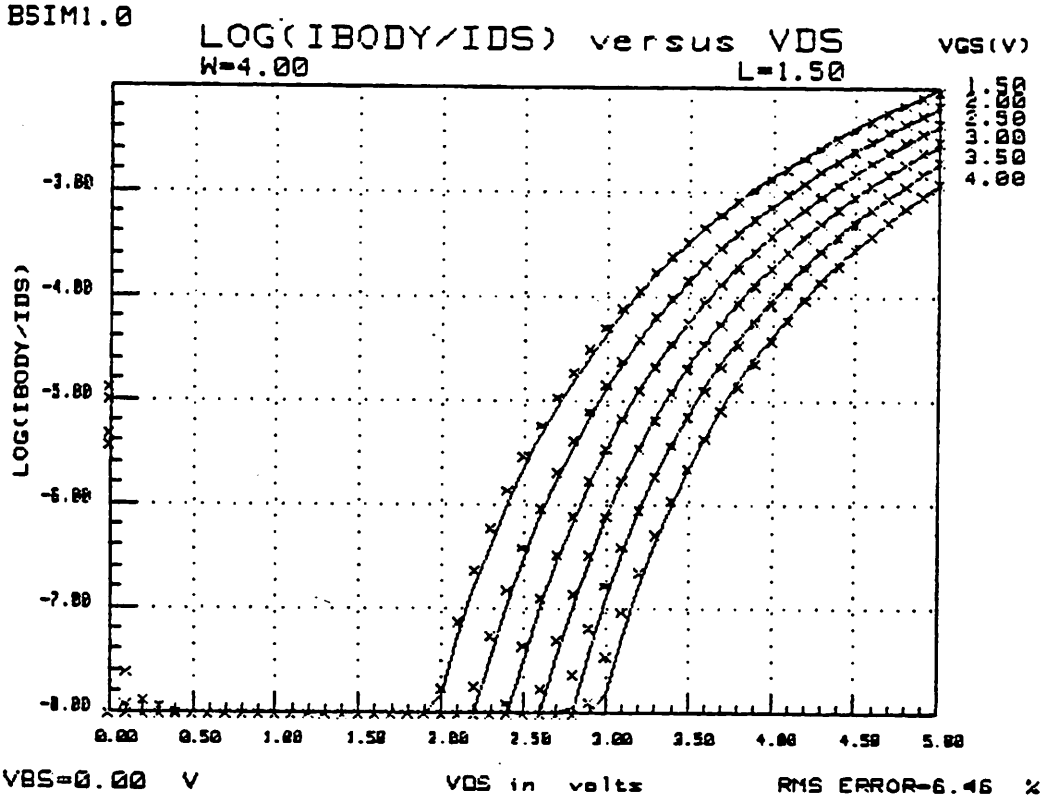

Fig. 23 AMD conventional device. $V_{bs} = 0$ (W = 4 μm , L = 1.5 μm).

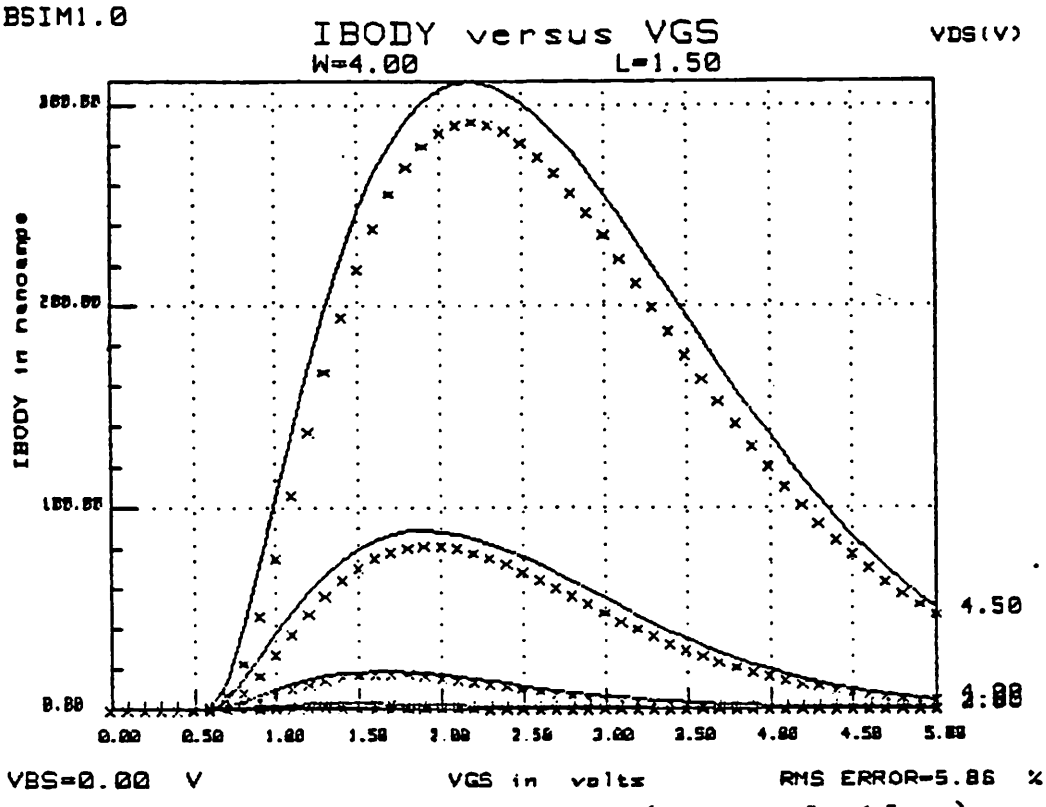

Fig. 24 AMD conventional device, $V_{bs} = 0$ (W = 4 μm, L = 1.5 μm).

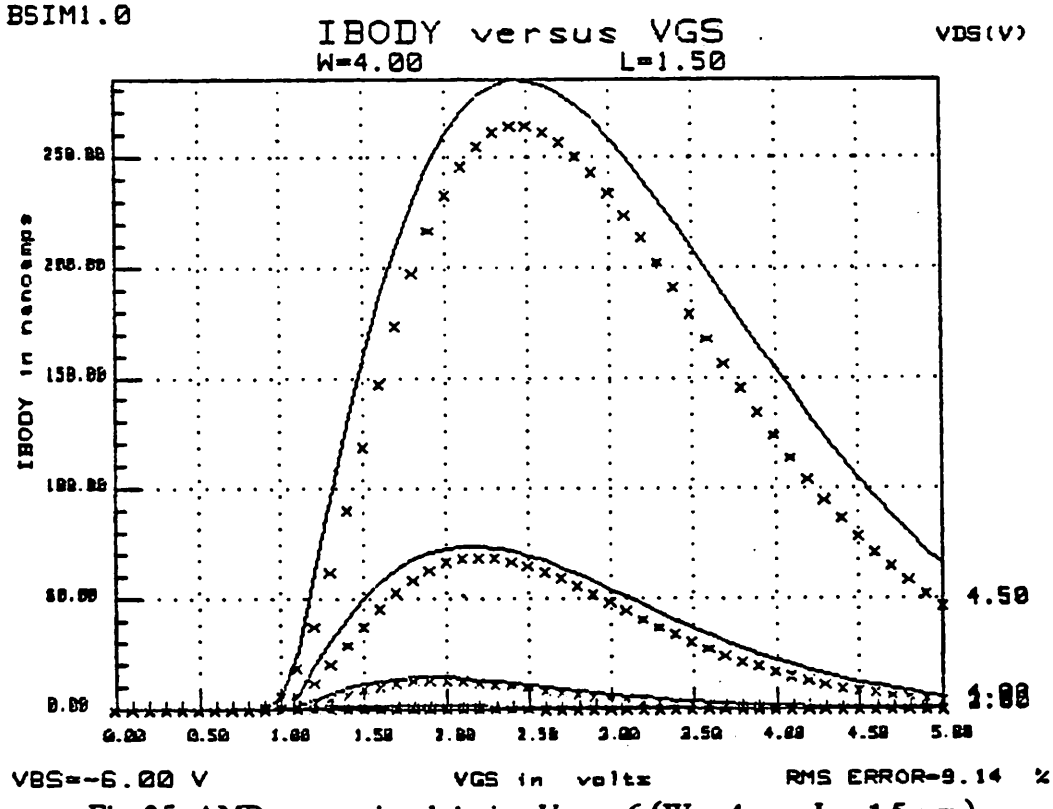

Fig. 25 AMD conventional device, $V_{bs} = -6$ (W = 4 μm, L = 1.5 μm).

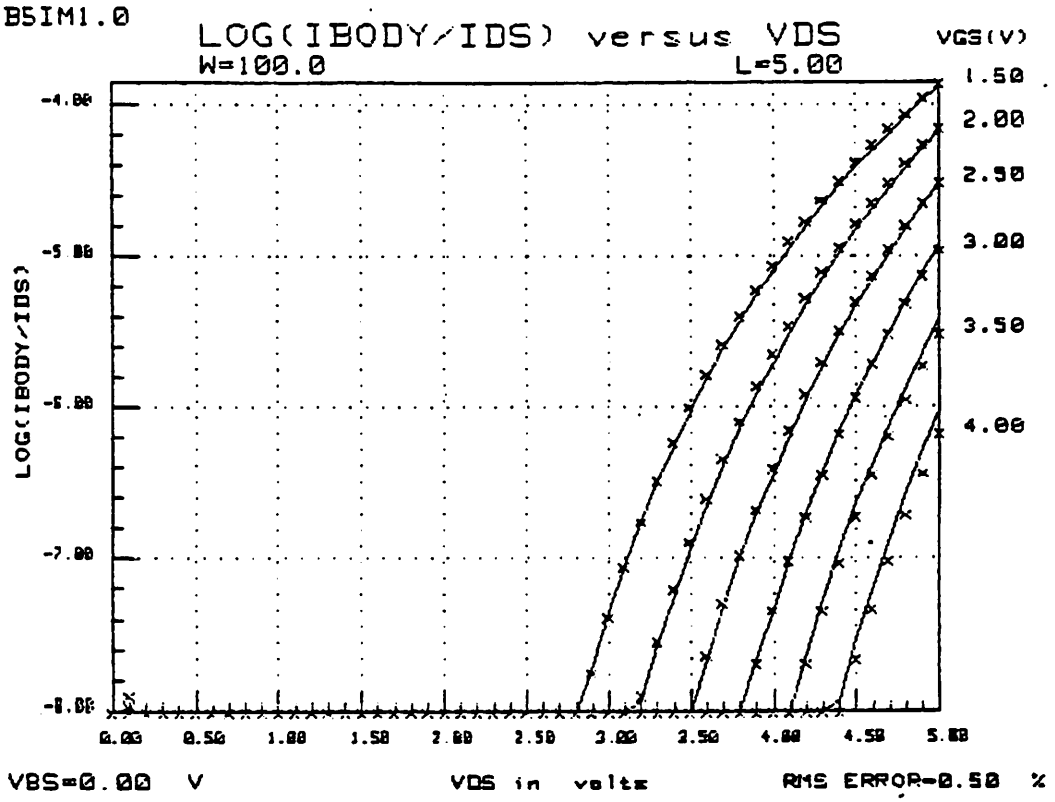

Fig. 26 Reticon conventional device, V_{bs} = 0 (W = 100 μm, L = 5 μm).

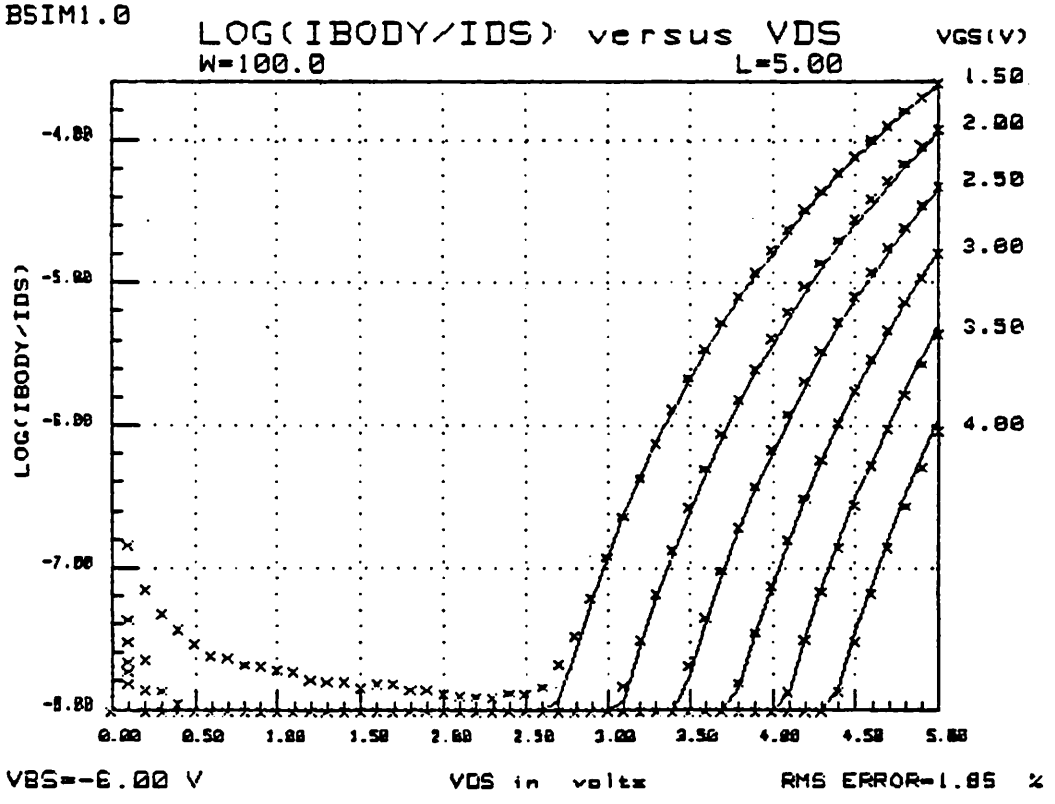

Fig. 27 Reticon conventional device, V_{bs} = -6 (W = 100 μm, L = 5 μm).

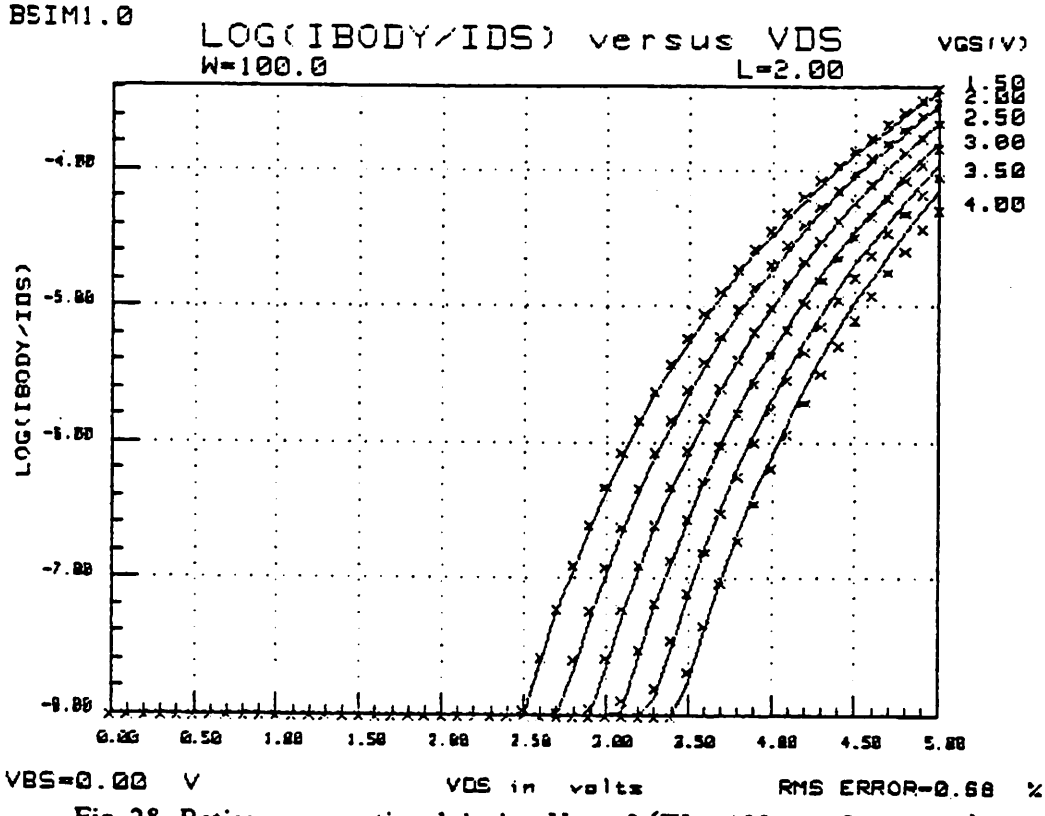

Fig. 28 Reticon conventional device, V_{bs} = 0 (W = 100 μm, L = 2 μm).

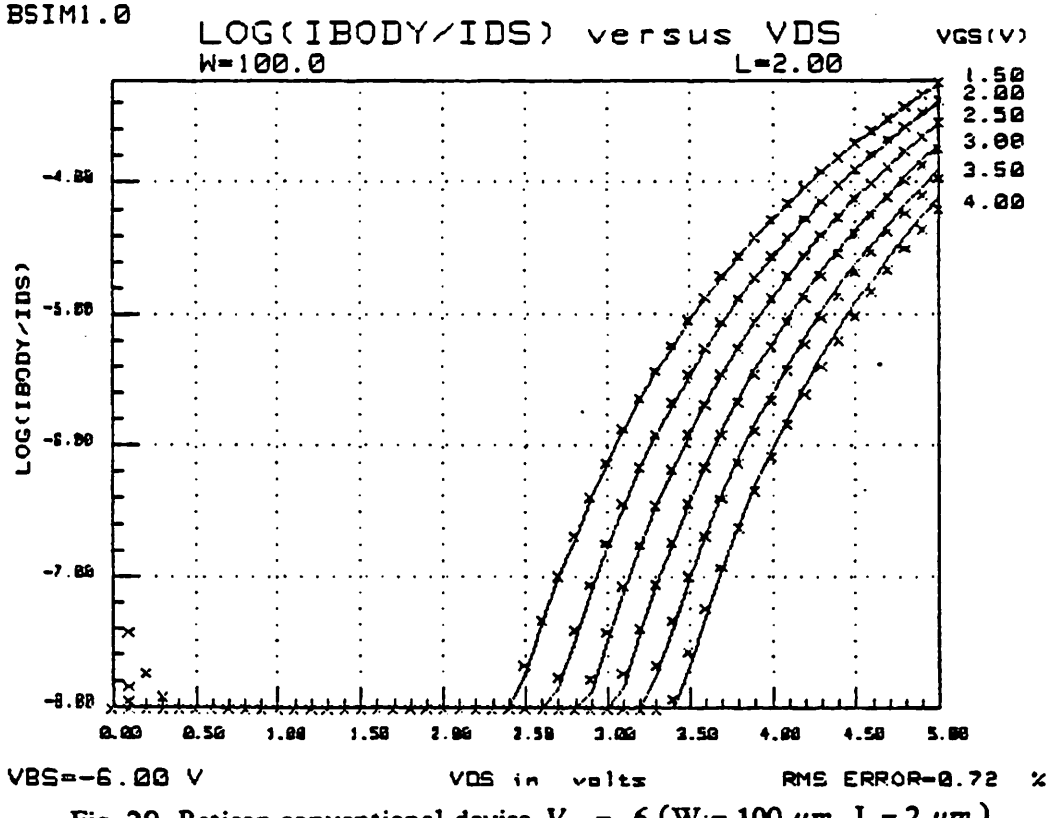

Fig. 29 Reticon conventional device, V_{bs} = -6 (W = 100 μm, L = 2 μm).

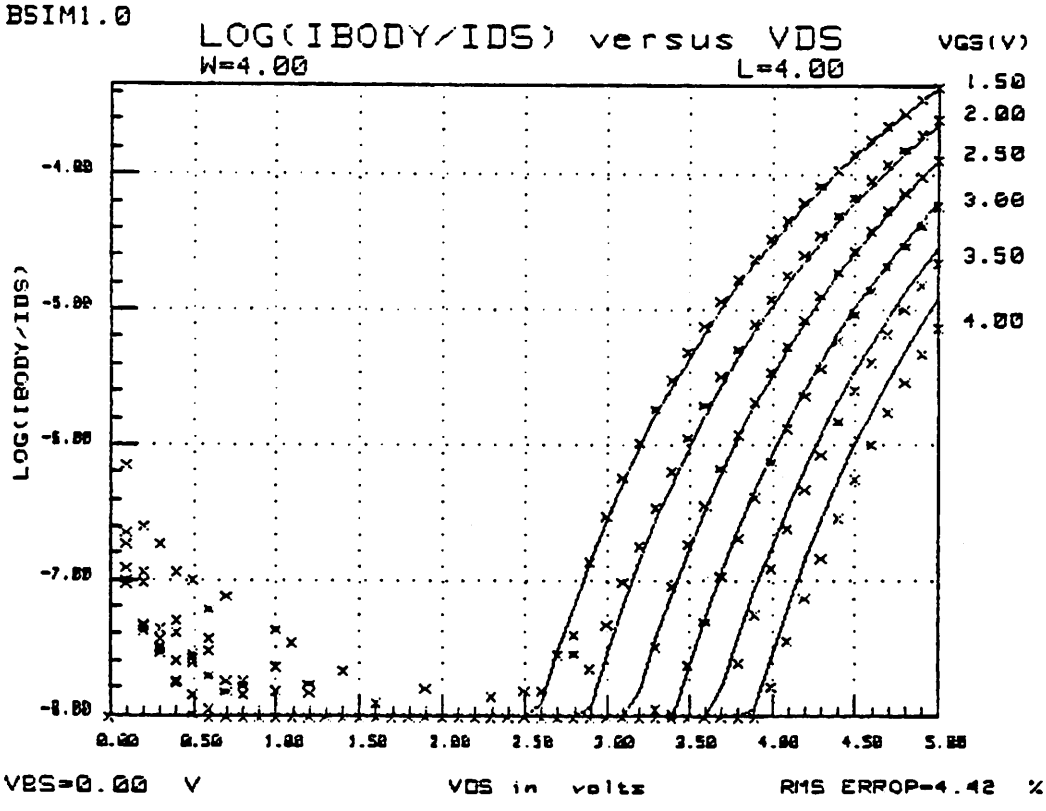

Fig. 30 Reticon conventional device. $V_{bs} = 0$ (W = 4 μm, L = 4 μm).

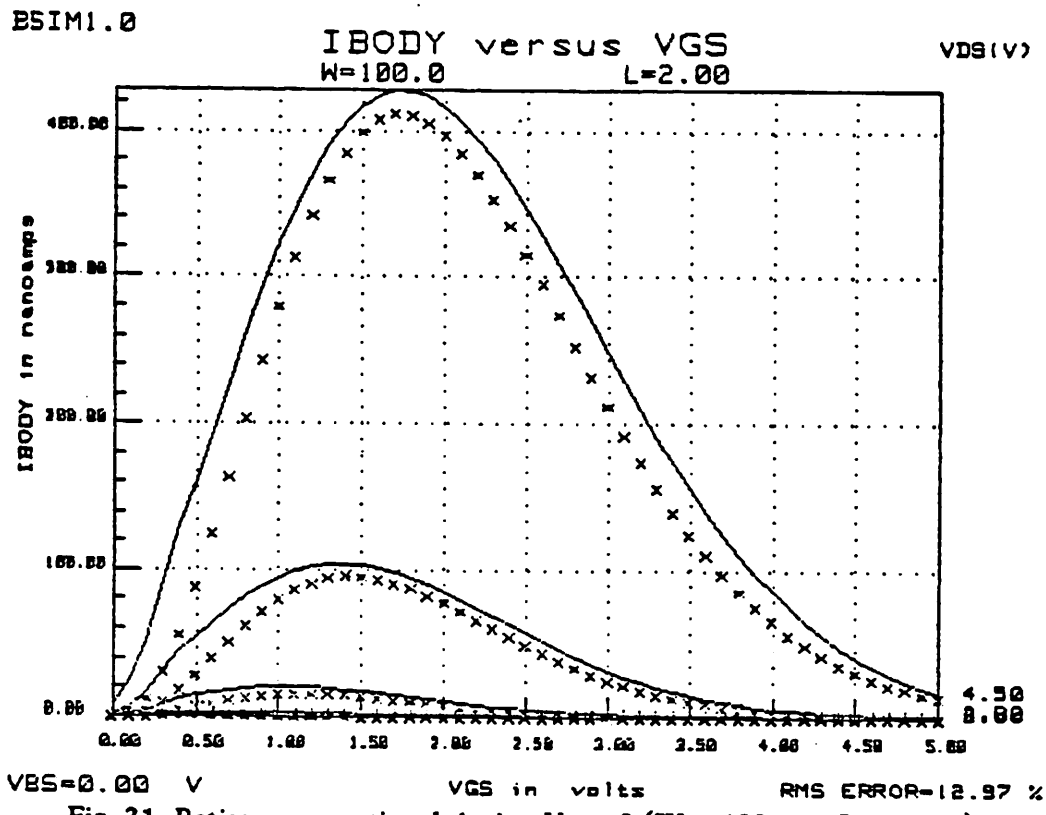

Fig. 31 Reticon conventional device, V_{bs} = 0 (W = 100 μm, L = 2 μm).

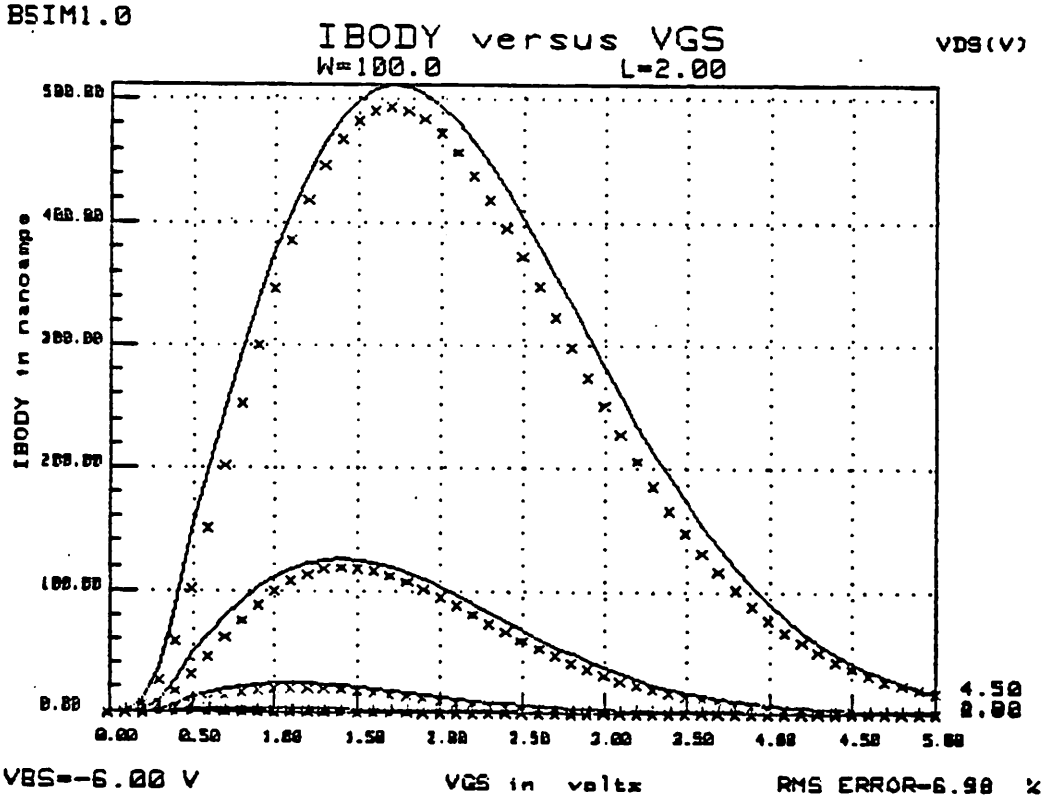

Fig. 32 Reticon conventional device, V_{bs} = -6 (W = 100 μm, L = 2 μm).

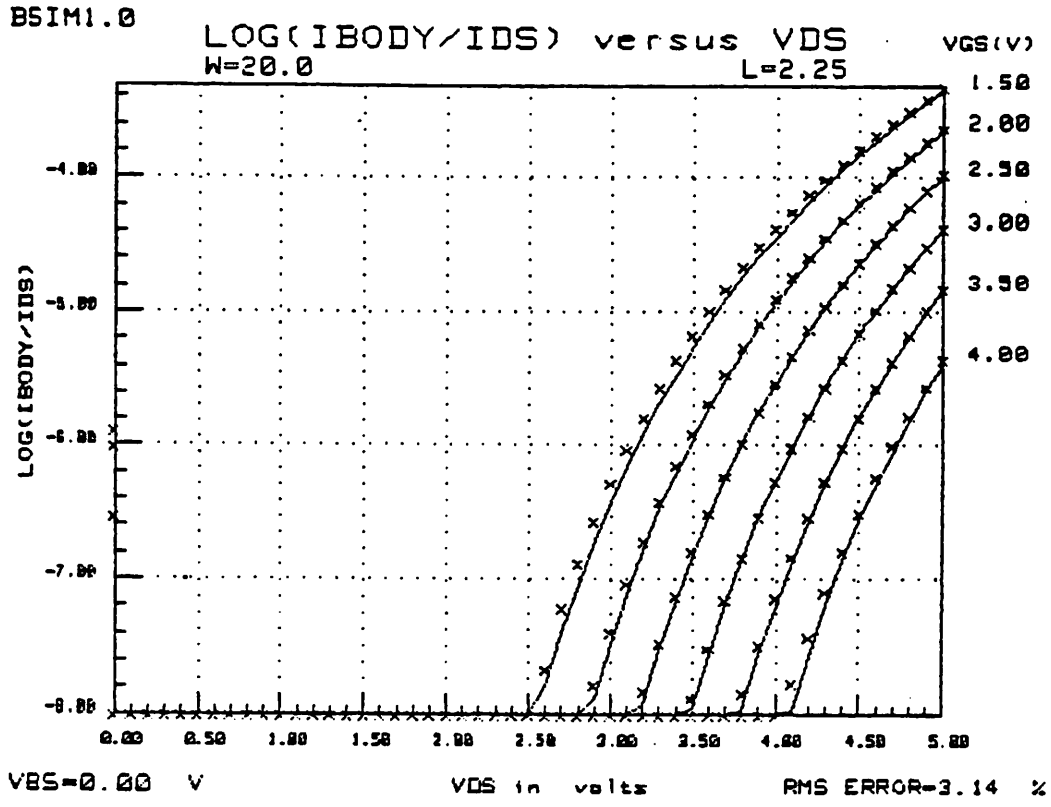

Fig. 33 AMD LDD device, $V_{bs} = 0$ (W = 20 μm, L = 2.25 μm).

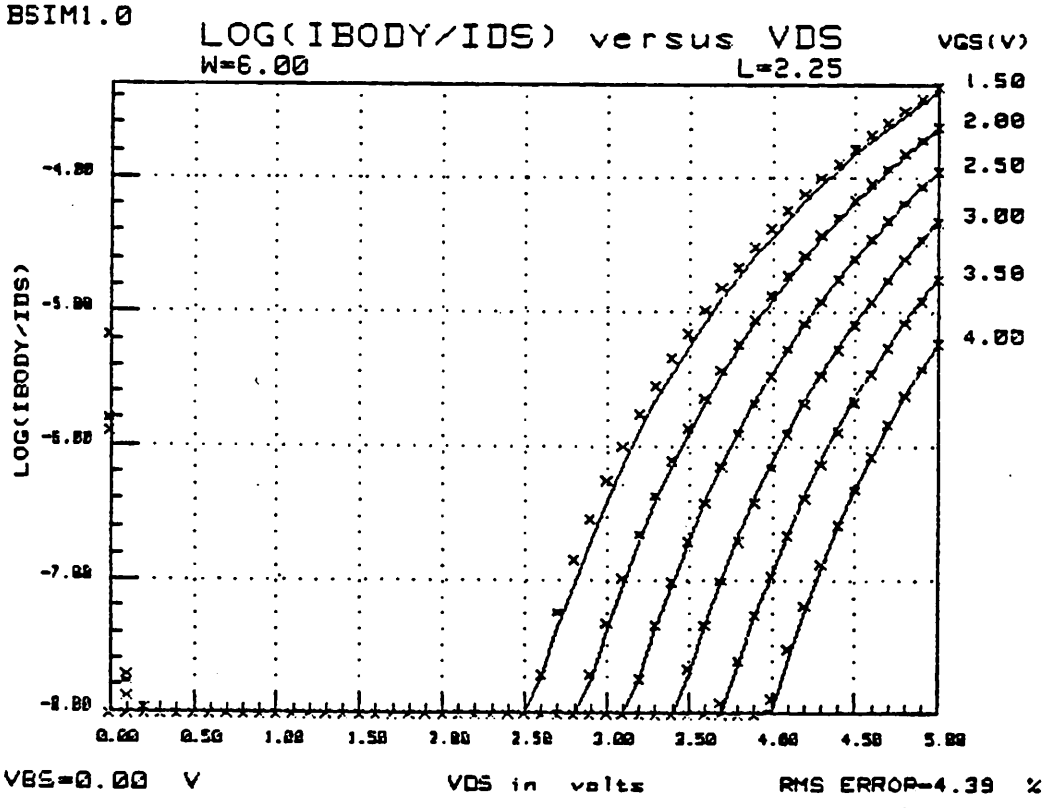

Fig. 34 AMD LDD device, $V_{bs} = 0$ (W = 6 μm, L = 2.25 μm).

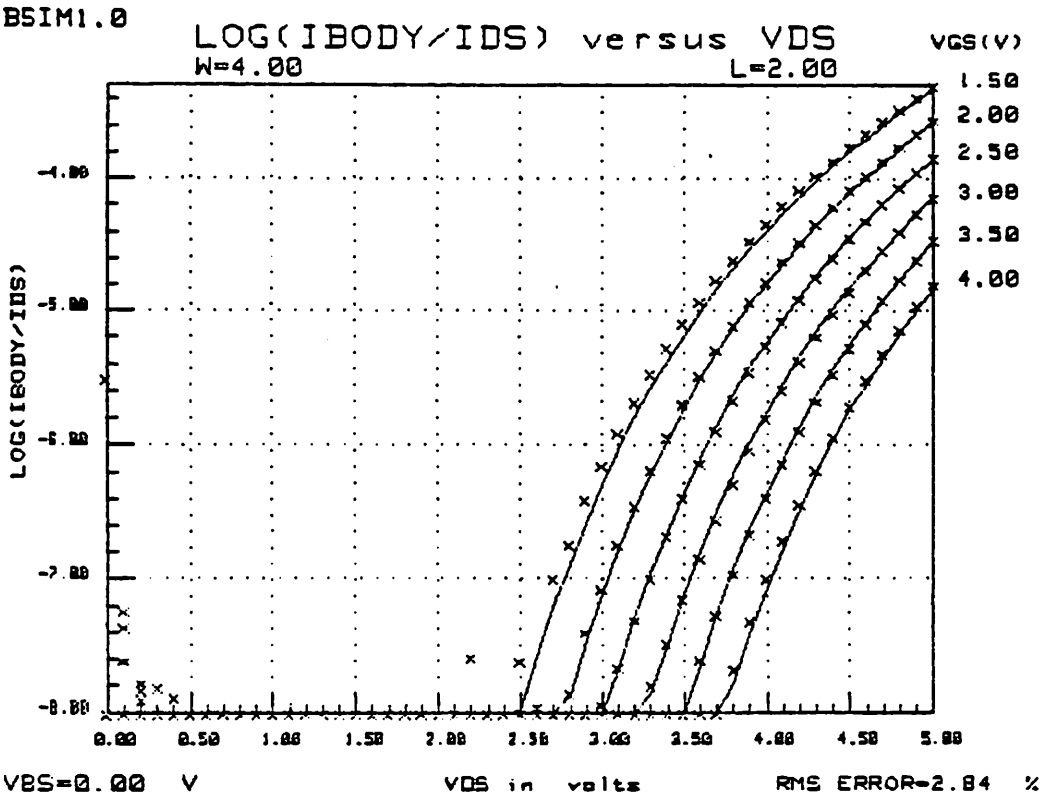

Fig. 35 AMD LDD device. V_{bs} = 0 (W = 4 μm , L = 2 μm).

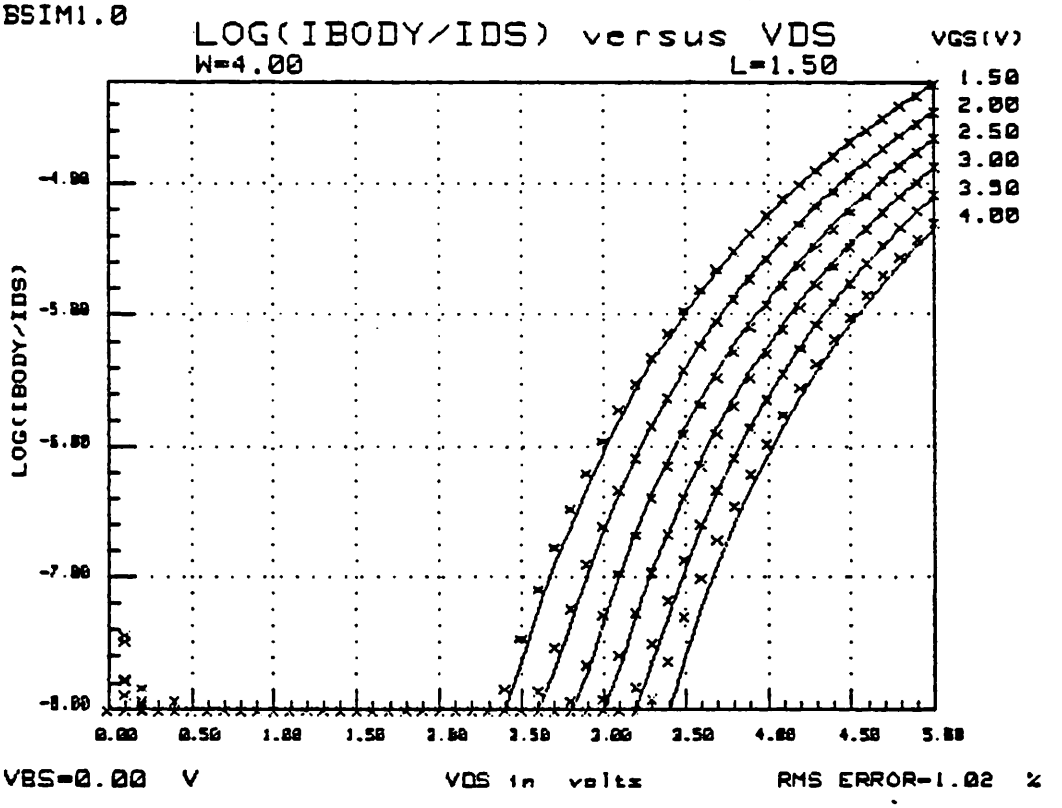

Fig. 36 AMD LDD device. V_{bs} = 0 (W = 4 μm , L = 1.5 μm).

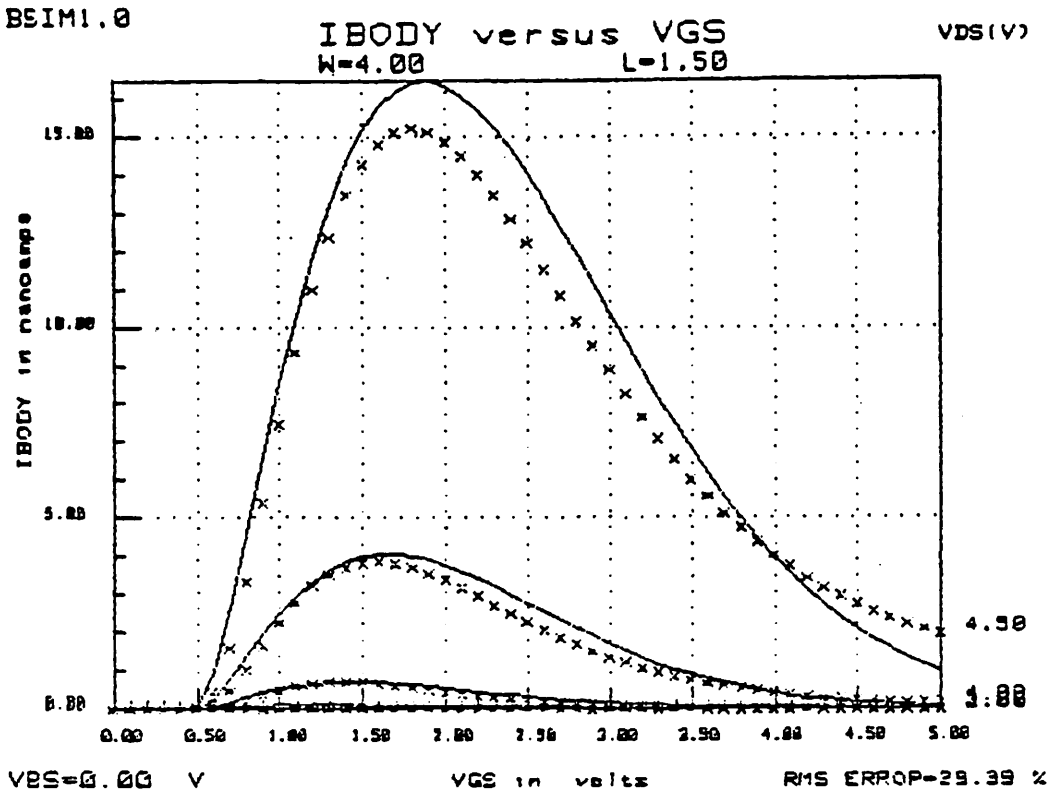

Fig. 37 AMD LDD device, V_{bs} = 0 (W = 4 μm, L = 1.5 μm).

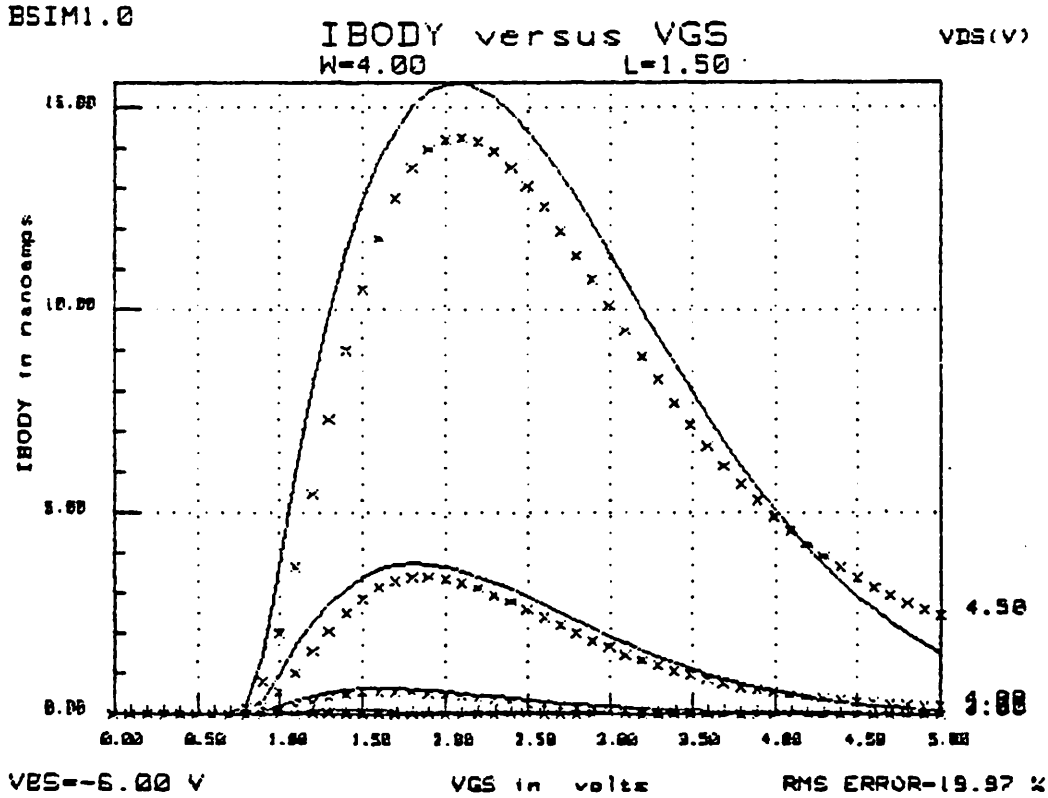

Fig. 38 AMD LDD device, V_{bs} = -6 (W = 4 μm, L = 1.5 μm).

```
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*RUN=
*WAFER=AMD
*XPOS=1
*YPOS=1
*OPERATOR=PETER LEE
*DATE=2-2-86
-4.1874E-001,3.33521E-002,-5.1117E-002,1.81149E+000,4.00000E+000,3.00000E+000
7.13753E-001,0.00000E+000,0.00000E+000,0.00000E+000,8.00000E+000,5.00000E+000
5.58365E-001,-1.6834E-001,2.74712E-001,3.16997E+000,4.00000E+000,2.00000E+000
1.05796E-001,-4.1177E-003,-8.2256E-002,8.07083E+000,4.00000E+000,2.00000E+000
-7.2300E-003,3.07340E-002,-1.4362E-003,2.31228E+002,4.00000E+000,3.00000E+000
5.32795E+002,-3.9402E-001,-1.6235E+000,0.00000E+000,0.00000E+000,0.00000E+000
5.46885E-002,4.12085E-002,-6.2018E-002,3.38129E+000,6.00000E+000,5.00000E+000
2.36098E-001,4.42758E-001,-1.8607E-002,2.01095E+001,4.00000E+000,5.00000E+000
7.35931E+000,-4.8293E+000,1.21072E+001,4.57048E+000,6.00000E+000,5.00000E+000
2.11581E-003,4.58996E-003,-3.8212E-004,1.01782E+001,4.00000E+000,4.00000E+000
-1.6744E-004,-2.0221E-003,-1.1733E-003,2.54243E+001,8.00000E+000,5.00000E+000
2.65956E-003,-2.5147E-003,1.70682E-003,8.71070E+000,6.00000E+000,5.00000E+000
-1.3051E-002,2.75034E-002,1.52139E-002,4.72137E+002,4.00000E+000,4.00000E+000
6.29382E+002,3.90953E+002,-1.6179E+002,5.33771E+000,4.00000E+000,2.00000E+000
6.12994E+000,2.11353E+001,8.09024E+000,9.15519E+000,4.00000E+000,2.00000E+000
-8.6353E-001,8.55419E+001,-2.3212E+001,1.72410E+001,4.00000E+000,3.00000E+000
-2.0974E-003,8.37179E-002,-2.2668E-002,1.35588E+001,4.00000E+000,3.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000,8.00000E+000,5.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000,8.00000E+000,5.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000,0.00000E+000,8.00000E+000,5.00000E+000
1.01647E+004,3.94291E+003,-5.6175E+003,1.16049E+001,4.00000E+000,5.00000E+000
2.99713E+003,-5.0905E+002,3.70774E+002,6.05593E+000,4.00000E+000,2.00000E+000
1.65674E+002,5.63348E+002,-4.1546E+002,4.37837E+002,4.00000E+000,5.00000E+000
1.94944E+000,-1.5686E+000,1.40142E+000,7.91657E+000,4.00000E+000,2.00000E+000
4.22982E+000,-4.9338E+000,5.85560E+000,7.82674E+000,4.00000E+000,2.00000E+000
-1.5710E-001,2.45792E-001,-1.9944E-001,3.87216E+001,4.00000E+000,1.50000E+000
-6.0306E-001,6.84631E-001,-9.0453E-001,6.22404E+000,4.00000E+000,2.00000E+000
-2.8755E+000,4.84726E+000,-3.6936E+000,8.53727E+001,4.00000E+000,1.50000E+000
-1.1199E+001,1.53871E+001,-1.7046E+001,1.21459E+001,4.00000E+000,2.00000E+000
5.55000E-001,-8.4885E-001,4.46489E-001,1.90791E+002,4.00000E+000,1.50000E+000
1.57731E+000,-2.2878E+000,2.69803E+000,1.18346E+001,4.00000E+000,2.00000E+000
2.85000E-002,2.70000E+001,5.00000E+000
```

Fig. 39 Process file for the AMD conventional devices measured.

V. CONCLUSION

A parametric model of the substrate current has been incorporated into the BSIM model. 11 additional parameters are introduced to model the various bias dependencies that exist. three to model V_{dsat} , and eight to model l_c . Each of the 11 parameters are then decomposed into three size-independent parameters in an identical manner with the previously existing BSIM model. The now 33 additional parameters are then simply appended to the process file using the same format as before [2].

Two additional types of plots have been added to display the substrate current. A $\log(\frac{I_{bs}}{I_{ds}})$ versus V_{ds} is available for low current characteristics as well as a more conventional I_{bs} versus V_{gs} graph showing the current peaking effect.

It has been shown experimentally that this substrate current model using one process file agrees well with actual data taken from devices of various dimensions and different technologies. Future work will be devoted to port the additional parameters into SPICE to be used for circuit simulation. Knowledge of the substrate current will enable circuit designers to analyze the resistance of their circuits to MOSFET degradation.

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[2] M.-C. Jeng, B.J. Sheu, P.K. Ko, "BSIM Parameter Extraction - Algorithms and User's Guide," University of California, Berkeley, ERL Memo, UCB/ERL M85/79, October 7, 1985.

[3] Y.A. El-Mansy and D.M. Caughey, "Modeling Weak Avalanche Multiplication Currents in IGFETS and SOS Transistors for CAD," IEDM Technical Digest, pp.31-34, 1975.

[4] Y.A. El-Mansy and A.R. Boothroyed, "A Simple Two-Dimensional Model for IGFET Operation in the Saturation Region," IEEE Trans. Electron. Devices, Vol. ED-24, pp.254-262, March 1977.

[5] P.K. Ko, "Hot-Electron Effects in MOSFETS," University of California, Berkeley, Ph.D. Thesis,1981.

[6] C. Sodini and P.K. Ko, "The Effect of High Fields on MOS Device and Circuit Performance," IEEE Trans. Electron. Devices, Vol. ED-31, pp.1386-1393, October 1984.

[7] T.Y. Chan, P.K. Ko, and C. Hu, "A Simple Method to Characterize Substrate Current in MOSFETs," IEEE Trans. Electron. Device Letters, Vol. EDL-5, p.505, December 1984.

APPENDIX A: BSIM SUBSTRATE CURRENT USERS GUIDE

This brief outline describing the operation of the substrate current extraction portion of BSIM assumes that the reader is already familiar with the general operation of the program. All inputs required from the user are directly analogous to the normal extraction process. For more information, refer to [2].

After the normal and (if chosen) subthreshold extraction is completed, the program will prompt whether substrate current extraction is desired (Fig. A1). Entering "n" or "N" will terminate the extraction process and the program will continue normally as before through the graphics routines. If "y" or "Y" is entered, then the substrate current extraction routine is entered.

The display that is now written onto the screen is similar to the previous status display except that the substrate current parameters appear on the screen (Fig. A2). Extraction will proceed after the user has entered minimum and maximum substrate bias values. The program, as before, will indicate any errors that occur and the time remaining until completion. After all measurements are completed and if the user had not chosen the single device mode, the program will prompt whether the measurements are satisfactory to continue the extraction. Once "y" or "Y" is entered, the substrate current parameters are calculated and displayed on the screen. The program then continues by measuring the next device, or by developing the process file and entering either the parameter graphics routines or the current playback routines according to the user's choice.

Substrate current parameter graphics and current playback are viewed in analogous fashion with the other parameters and currents. Thus the operation of the rest of the program is identical to that described in [2].

```
                    ***BSIM EXTRACTION STATUS***

PROCESS=                                    VDD=5.00 VOLTS
LOT=                                        TEMP=27.00 DEG C
WAFER=                                      TOX=285.00 ANGSTROMS
DATE=                                       XPOS= 1 YPOS= 1
OPERATOR=                                   DEVICE=NCHANNEL
OUTPUT FILE=bsimout.TEXT                    WIDTH=8.00 MICRONS
PROBER FILE=amdprfile.TEXT                  LENGTH=5.00 MICRONS

MINUTES TO DIE COMPLETION=15.1              MINUTES TO WAFER COMPLETION=15.1
DEVICE EXTRACTION LOCATION XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX FINISHED
PRESENT DEVICE BSIM PARAMETERS
VFB=-0.421                                  X2U0=0.002207
PHIF2=0.714                                 X2U1=-0.000961
K1=0.567                                    X3U1=0.002651
K2=0.092                                    X2BETA0=0.000001
ETA=-0.001                                  X2ETA=0.002958
BETA0=0.000089                              X3ETA=-0.000630
U0=0.053                                    BETA0SAT=0.000116
U1=0.074                                    X2BETA0SAT=0.000002
N0=                                         X3BETA0SAT=0.000002
ND=                                         NB=
Are you interested in substrate current measurements and extractions?(Y/N) >
```

Fig. A1 Prompt to enter substrate current portion of BSIM.

```
                    ***BSIM EXTRACTION STATUS***

PROCESS=                                    VDD=5.00 VOLTS
LOT=                                        TEMP=27.00 DEG C
WAFER=                                      TOX=285.00 ANGSTROMS
DATE=                                       XPOS= 1 YPOS= 1
OPERATOR=                                   DEVICE=NCHANNEL
OUTPUT FILE=bsimout.TEXT                    WIDTH=8.00 MICRONS
PROBER FILE=amdprfile.TEXT                  LENGTH=5.00 MICRONS

MINUTES TO DEVICE COMPLETION=4.8
DEVICE EXTRACTION LOCATION XXXXXXXXX                              FINISHED
PRESENT DEVICE BSIM SUBSTRATE PARAMETERS
LC0=                                        LC7=
LC1=                                        ECRIT0=
LC2=                                        ECRIT6=
LC3=                                        ECRITB=
LC4=
LC5=
LC6=

message from program=

***SUBSTRATE CURRENT MEASUREMENTS IN PROGRESS***
```

Fig. A2 Substrate current measurement status display.

APPENDIX B: MODIFICATIONS TO THE BSIM SOURCE CODE

I. PROCEDURES ADDED

1. Procedure substrate_status_display

This procedure displays the status of the substrate current measurements on the screen.

2. Procedure string_setup_measure_IBODYvsVDS

Similar to procedure string_setup_measure_IDSvsVGS, this procedure sets up the strings necessary to measure substrate current.

3. Procedure source_setup_measure_IBODYvsVDS

Similar to procedure source_setup_measure_IDSvsVGS, this procedure sends the strings necessary to properly set up the 4145A.

4. Procedure measure_device_functionality_IBODYvsVDS

Similar to procedures source_setup_nchannel_device_functionality and measure_device_functionality combined, this procedure determines whether the substrate is open- or short- circuited to the source and drain.

5. Procedure chan_definition_device_functionality_IBODYvsVDS

Similar to procedure chan_definition_device_functionality, this procedure sets up the channel definition page of the 4145A for the functionality test.

6. Procedure measure_and_reduce_IBODYvsVDS

This procedure contains two procedures within itself to measure substrate and drain current for the extraction of l_c and E_{crit}.

7. Procedure measure_IBODYvsVDS

The actual measurement of the substrate and drain curves are done.

8. Procedure reduce_IBODYvsVDS

This procedure contains two others to reduce data to determine E_{crit} and l_c. The parameter extraction for l_c is also done.

9. Procedure measure_and_reduce_vdsat

Data to determine V_{dsat} parameters is reduced to values of E_c.

10. Procedure reduce_and_extract_parameter_l

Data to determine l_c is reduced, and the bias-dependent parameters for l_c are extracted.

11. Procedure substrate_parameter_extraction

Extraction of the remaining 3 E_{crit} parameters is done, and the 11 parameters are printed on the screen.

12. Function bsimsim_body

Similar to function bsimsim, this function plots the $\frac{I_{bs}}{I_{ds}}$ graphs.

13. Procedure IBODYvsVDS_data

Measurement for I-V graphics playback for $\frac{I_{bs}}{I_{ds}}$ versus V_{ds} is performed.

14. Procedure channel_definition_for_IBODYvsVDS_data

Preliminary setup of the 4145A is done for data playback.

15. Procedure string_setup_measure_IBODYvsVDS

Bias voltage setups are written into strings.

16. Procedure source_setup_measure_IBODYvsVDS

Bias voltage setup strings are sent to the 4145A.

17. Procedure measure_IBODYvsVDS_data

The actual data measurement is done.

18. Procedure IBODYvsVGS_data

This procedure and its related subprocedures are analogous to procedure IBODYvsVDS_data and its related subprocedures (numbered 13 - 17 above) except that data measurement for I_{bs} versus V_{gs} graphics playback is done.

19. Procedure IBODYvsVD

This procedure generates the measured and simulated values for plotting $\frac{I_{bs}}{I_{ds}}$ versus V_{ds} in logarithmic scale.

20. Procedure IBODYvsVG

This procedure generates the measured and simulated values for plotting I_{bs} versus V_{gs} in linear scale.

21. Procedure bsim_timer_body

Similar to procedure bsim_timer, this procedure keeps track of extraction time during substrate current measurement.

22. Procedure clear_yb

This procedure clears the second y-axis plot from the graphics page so that data buffer overflow does not occur on the HP4145A for measurements that are done after the $\frac{I_{bs}}{I_{ds}}$ measurements.

23. Procedure select_substrate_bias

Bias voltages for substrate current IV playback are selected by the user in this procedure.

24. Procedure error_calculations_body

This procedure is identical to procedure error_calculations except valid current levels for error calculations are set according to minimum and maximum currents graphed in substrate current analysis.

II. PROCEDURES MODIFIED

1. Procedure measure_device_data

Substrate current measurement routine is added.

2. Procedure measure_device

Substrate current error checking is added.

3. Procedure channel_definition_for_IDSvsVGS_data

This procedure now also sets up the 4145A for substrate current measurements.

4. Procedure draw_menu

The options to plot I_{bs} versus V_{gs} and $\log(\frac{I_{bs}}{I_{ds}})$ versus V_{ds} are added.

5. Procedure graphics

The substrate current plots are added.

6. Procedure make_xyz_axis_labels

Labels for the 11 substrate parameters added.

7. Procedure page3

Choices for the 11 substrate parameters are added.

8. Procedure store_parameters_in_die_files

The substrate parameters are added to the process file.

9. Procedure load_up_process_parameters

Array sizes increased to accommodate 11 more substrate parameters.

10. Procedure bsim1.0 (MAIN BSIM PROGRAM)

Substrate current measurement enhancements added.