Copyright © 1986, by the author(s).
All rights reserved.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission.

APPLICATIONS OF SIMPL

by

Lynn Gibson

Memorandum No. UCB/ERL M86/56

27 June 1986

APPLICATIONS OF SIMPL

by

Lynn Gibson

Memorandum No. UCB/ERL M86/56

27 June 1986

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

ABSTRACT

This report describes several applications of versions 1 and 2 of SIMulated Profiles from the Layout (SIMPL)). These programs, developed by Grimm (1) and Lee (2) were used to simulate MOS, bipolar, and advanced processes. Of particular interest were the test structures in the Advanced Berkeley CMOS (ABCMOS) project. Several cases of these applications are documented here as examples. From the applications, the current capabilities of the programs are evident, along with areas in need of expansion.

I. Introduction

SIMPL is a CAD tool which automatically generates a cross-sectional view of an integrated circuit along any arbitrary cut-line drawn on the layout. The user must only provide the layout information in CIF (3) format and the process steps required. SIMPL output is viewed on a color graphics terminal. This report gives examples for a variety of technologies including NMOS, CMOS, GaAs, bipolar and trench DRAM. It provides documented examples as well as an overview of the current status of the programs.

For this report, both versions of SIMPL were run on a VAX-11/780. SIMPL-1 output was viewed on several MFB- and KIC-compatible terminals. Photographs for the SIMPL-1 output are taken from a Matrix Instruments 3000 color graphics recorder with the AED 512. A Tektronix 4113 color graphics terminal was used for the SIMPL-2 output, and photographs were taken directly from the screen.

SIMPL-1 applications are given first followed by demonstrations of SIMPL-2. We begin with a good learning example of SIMPL-1, the Mead and Conway NMOS process. As an example of the versatility of SIMPL, a GaAs FET process is demonstrated. SIMPL is particularly useful for seeing test structures, as is presented here for an n-well CMOS process. The programs were also applied to a p-well CMOS and a magnetometer fabrication process. A very complicated trench transistor DRAM was also attempted and revealed many needs for extensions in SIMPL-2.

II. SIMPL-1

This first version was used to simulate an NMOS inverter, a field effect transistor in GaAs, some unusual test structures in CMOS, and an integrated circuit sensor in bipolar technology.

A. NMOS inverter

The most basic example of SIMPL-1 applications is the well-known NMOS process

described by Mead and Conway [3]. The layout and process are from their text, "*Introduction to VLSI Systems*".

Process inputs, layout structure, and the cross section derived by SIMPL-1 are presented in Figs. 1-4. Figure 3 shows the cross section at a horizontal cut-line running from the left most contact in Fig. 2, across the polysilicon gate, and through the rightmost contact. This view shows the cross section of the "butting contact". Figure 4 is from a vertical cut-line down the center of the middle metal line. In all of the SIMPL cross sections, colors signify the following:

yellow: p-type silicon. Deeper shades indicate heavier doping.

green: n-type silicon. Deeper shades indicate heavier doping.

pink: oxide

red: polysilicon

blue: metal

This was a straightforward application for SIMPL-1, which performed the simulation well.

B. GaAs DFET

SIMPL is generic in that it can run any mask set and process sequence. Here is a simulation of a GaAs process published by Greiling and Krumm [4].

The MESFET structure in gallium arsenide is detailed in Figs. 5-7. Notice that the GaAs substrate is treated like silicon. There is no oxidation in this case, and doping profiles depend only on the given process standard deviations and peak doping locations. For these processes, the substrate character does not matter to the simulator. One common GaAs metallization process, lift-off, cannot be simulated by SIMPL at this time, but it was simulated through a deposition and etch with a reversed mask polarity. For the ohmic contacts in blue and the gate and first-level metal in black [Fig.7], the two user-defined layers available in in SIMPL-1 were used. The second-level metal is in silvery blue. Here, the cut-line was horizontal and passed through the center of the contact and gate and continued through the top metal.

In Fig. 7, an asymmetry in the doping profile can be observed. This was an error in the original code which has been located and fixed by Joe Wu.

C. ABCMOS test structures (Advanced Berkeley CMOS)

ABCMOS is an n-well CMOS process developed at Berkeley. Several layouts from the test chip were input to SIMPL-1 to examine various test structures used with this process. Another motivation for this applications was the desire for cross sections of the test structures for presentation at a conference. These are described in Figs. 8-14.

Three structures from the ABCMOS [4, 5, 6] test chip were modeled by SIMPL-1. Bipolar transistors appear first. The layout (Fig. 9) shows two lateral transistors, nwell-p-nwell on the left and n^{+}-p-nwell on the right. Cutlines were vertical and down the center of each. Fig. 10 and 11 show SIMPL-1 cross sections of each transistor. Fig. 12 and 13 give the layout and cross section of the matching capacitors, part of the analog test structure. The cut-line was horizontal and passed through the center of the two top capacitors in Fig.12. Finally, the latchup test structure was simulated (Figs. 14, 15). The horizontal cut-line for the cross section of Fig. 15 was drawn through the center of the left hand n-channel and p-channel MOSFET pair (Fig.14). The gate contacts are external to this cut-line.

The ABCMOS layouts presented a special challenge for SIMPL-1 since some layers were a combination of others. For example, the n-type source-drain mask NNII sometimes had to be derived from the active area mask and the PPII mask. However, since SIMPL-1 has neither mask manipulation capabilities nor multiple-exposure models for resist, different processes had to be written for each test structure. One such process is given in Fig.8.

These unusual test structures were difficult for SIMPL only because of the layout problems described above. Mask manipulation capabilities are clearly needed, along with the ability to perform multiple exposures of resist. However, SIMPL-1 demonstrated good capability to simulate large cross sections in expansive mask sets here.

D. Magnetic Field Sensor

This bipolar-based integrated circuit sensor was designed at Berkeley by J. Goicolea [8]. Figs. 16-18 show the process listing, layout and cross section of this device. The horizontal cut-line runs down the center of the lower, large pink rectangle in Fig. 17. The dense blue lines visible here are part of the magnet coil.

Notice in the cross sectional view the split buried layers. With current in the magnet coils on the top, the transistor current will be deflected more to one n-type buried region than the other. Thus, one side will have more emitter current than the other, and this imbalance of current will be detected by additional circuitry on the chip.

Note that in Fig. 18 there is no upward diffusion into the epi from the buried layer. This could be overcome by a nonphysical process of implanting after epi deposition. Also, in a process special to this magnetic field sensor, a thick oxide was deposited before the metal magnet coil was deposited and patterned.

III. SIMPL-2

Some of these same processes were simulated using arbitrary polygonal shapes with SIMPL-2. This worked well for the Berkeley p-well CMOS and n-well ABCMOS processes. However, attempts to simulate a more advanced process, a trench transistor cross-point DRAM, indicated many areas in which expanded process capabilities are required.

A. Berkeley p-well inverter

A good learning example of the use of SIMPL-2 is this Berkeley p-well CMOS process (Fig. 19). The cut-line of interest is along the center of an inverter, as indicated by the black line on the top of Fig. 20.

Notice in the cross sectional view that SIMPL-2 simulates a bird's beak for the LOCOS oxide growth. The lateral diffusion of the p-well and thinning of metal at steps are also clearly

shown.

Several inconveniences in running the SIMPL-2 simulation were noted. First, SIMPL-2 always refused the user's first cut-line point with seven or eight beeps and the comment "outside layout view-port." Since this only occurs for the first SIMPL-2 request after logging on, it may not seem like much of a problem. But since SIMPL-2 has no control character to stop it externally (if it seems to be in trouble), one has to power down and log in again many times during process development. Second, SIMPL-2 takes a long time to draw a cross section (up to 15 minutes) after several doping steps.

The SIMPL-2 etch routine was found to be very limited. Etching less than the total thickness of any layer requires special treatment of the layers above. That is, the layer above the desired "partial etch" layer must have just undergone a masking step. To see the difficulty consider the following example. During a SIMPL-2 simulation of a CMOS process, the active area has been defined through a LOCOS oxidation. A thin "sacrificial" oxide, $0.02\mu m$, is grown on all surfaces for a boron threshold-adjust implant. In the laboratory, the next step would be to etch all of the sacrificial oxide and grow the gate oxide. SIMPL-2 steps to simulate this sacrificial oxide etch process are:

1) Instruct SIMPL-2 to etch 0.02 μm oxide. SIMPL-2 will, instead, etch all of the oxide.

2) Deposit resist, expose the resist, develop the resist, and then etch the 0.02 μm oxide. Remove all of the undeveloped resist. This will exactly simulate the partial oxide etch, but unfortunately it takes six SIMPL-2 steps instead of one.

3) Leave the sacrificial oxide in place and neglect the thin oxide etch step.

For the p-well CMOS process, method 3) was chosen. The gate oxide was then grown on top of the sacrificial oxide.

B. ABCMOS

Two of the ABCMOS test structures were simulated by SIMPL-2. The matching capacitors

and latchup test structure are shown in Figs. 22 and 23, respectively. Again, more realistic two-dimensional topography effects are seen.

Mask definition problems as indicated in Section II)C again required different processes for these two structures; one process flow is given in Fig. 21. Also, SIMPL-2 could not handle the full length of the chosen cut-lines; thus the masks were scaled down by a factor of up to twenty. This then required changes of doping profiles so as not to short together source/drain regions from the two-dimensional ion implant routines of SIMPL-2.

Notice in Fig. 23 that no contact cuts are visible in the cross section. While the contact mask is clearly observed in the layout (top of figure), it is impossible to manually position the cut-line coincident with the contact mask. A "zoom" capability for small layout structures is therefore desirable in SIMPL-2.

C. Advanced Processes

Simulation of a trench transistor cross-point DRAM process proved to be impossible with the current version of SIMPL-2. The attempted device was modeled after the Texas Instruments DRAM cell [7].

1. The first few steps of the TI process required a) a lightly-doped epitaxial layer grown on a heavily-doped p-type substrate, followed by b) a recessed oxide patterned to mask the implanted $n+$ bit lines, c) an etch of $8\mu m$ trenches, and finally d) a thin oxide growth on the entire surface. Problems with SIMPL-2 as seen in attempts to model this part of the process were

   i) Deposited, doped Si layers (epi) could not have oxide grown on them.

   ii) There is no model for recessed oxide growth.

   iii) SAMPLE cannot simulate trench etch as deep as $8\mu m$.

   iv) While SAMPLE successfully modeled the isotropic oxide deposition, SIMPL-2 took the results and went off into an infinite loop.

SIMPL-2 was successful in etching shallow trenches in silicon, however. The process written to approximate steps a) - c) is given in Fig. 24, with cross sectional view in Fig. 25; it has no epi layer and a regular LOCOS oxidation is used for bit-line implant definition and isolation.

2. Further steps in this DRAM process require doped polysilicon deposition followed by a matched rate resist etchback to ensure that the trench is filled with poly but that all other surface polysilicon is removed. SIMPL-2 was successful in deposition of polysilicon and resist [Figs. 26,27], but problems encountered in simulating the actual process steps were

   i) Doped polysilicon is not available.

   ii) Etch rates of polysilicon and resist cannot be specified; this capability is required for simulation of matched rate resist etchback.

IV. Conclusion

This report gives examples of the use of SIMPL-2 and SIMPL-2 for a variety of technologies including NMOS, CMOS, GaAs, bipolar, and trench DRAM. It provides documented examples as well as an overview of the current status of the programs. For SIMPL-1, the NMOS example developed here is suggested as a learning case for new users. A GaAs DFET and bipolar magnetometer were developed to show the versatility of SIMPL-1. For newcomers, either of the CMOS processes developed here would be good as examples of SIMPL-2. The most revealing example of SIMPL-2 was its application to a trench transistor cross-point DRAM. Here, many needs for generalization of the SIMPL-2 process capabilities were apparent.

Several changes and expansions of the SIMPL programs are recommended. They fall into one of three categories: errors, convenience issues and specific process enhancements and are as follows:

1) Errors. Only one error was seen, the doping asymmetry problem in SIMPL-1. It has already been fixed.

2) Conveniences. These are SIMPL-2 problems. Refusal of first cut-line point, lack of control character to stop program if it gets in trouble, long time to draw cross sections.

3) Processes. Both SIMPL-1 and -2 need lift-off, mask manipulation capabilities and multiple exposure capabilities. SIMPL-2 needs to accommodate longer cut-lines and provide more flexibility in oxidation for recesses, trenches, and deposited layers as well as access to more of the SAMPLE capabilities in etching.

REFERENCES

1. Grimm, M. A., "SIMPL (SIMulated Profiles from the Layout)," M.S. Thesis, University of California, Berkeley, December, 1983.

2. Lee, K., "SIMPL-2 (SIMulated Profiles from the Layout - Version 2)", Ph.D. Thesis, University of California, Berkeley, July 1985.

3. C. A. Mead and L. A. Conway, "*Introduction to VLSI Systems,* Addison-Wesley, 1980.

4. Greiling, P.T. and C.F. Krumm, " The Future Impact of GaAs Digital Integrated Circuits," in *VLSI Electronics: Microstructure Science, Vol. 11,* Academic Press, 1985.

5. Oldham, W.G., A. R. Neureuther, Y. Shacham, and F. Dupois, "Berkeley CMOS Process: A User Guide," University of California, Berkeley, Electronics Research Laboratory Memorandum No. UCB/ERL M84/84, October, 1984.

6. Oldham, W.G. and A. R. Neureuther, "Berkeley CMOS Process Test Patterns," University of California, Berkeley, Electronics Research Laboratory Memorandum No. UCB/ERL M84/26, June 1984, Vol. I.

7. ibid., Vol. II

8. Goicolea, J. and R. S. Muller, "A Silicon Magneto-Coupler Using A Carrier-Domain Magnetometer," *IEDM Technical Digest,* 1985.

9. Richardson, W.F., et al., "A Trench Transistor Cross-Point DRAM Cell," *IEDM Technical Digest, 1985.*

Acknowledgements

I would like to thank Professor A.R. Neureuther for his guidance, support and friendship throughout this work. Thanks also goes to Professor Ping Ko for reading this paper.

I thank Gino Addiego for his help with SAMPLE, Rick Spickelmier for assistance with KIC, and Ken Lee for advice on the use of SIMPL-2.

I am grateful to Dr. Yosi Shacham-Diamand for sharing his technical expertise and his priceless good humor during the project.

I thank my husband, George, for his support and patience.

Finally, I would like to express thanks to Professor W.G. Oldham for enabling me to finish my degree at Berkeley.

The financial support from SRC grant SRC 82-11-008 is gratefully acknowledged.

Fig. 1. NMOS SIMPL-1 process listing

```
C This is the Mead and Conway NMOS inverter process.
C Each section of the process below corresponds to a
C cross section in Plate 1.
C
C Plate 1a)
SUBS P 1E15
OXID 0.3
DEPO RST 1.0
MASK NEG ACTV 0 0
ETCH ERST 1.1
ETCH OX 0.9
ETCH RST 1.1
C
C PLATE 1b)
DEPO RST 1.0
MASK NEG DEPL 0 0
ETCH ERST 1.1
DOPE N 1.0E17 0.095 0.0 0.1
C
C Plate 1c)
ETCH RST 1.1
OXID 0.10
DEPO POLY 0.5
DEPO RST 1.0
MASK POS POLY 0 0
ETCH ERST 1.1
ETCH POLY 0.6
ETCH RST 1.1
C
C Plate 1d)
DOPE N 1.0E20 0.3 0.0 0.2
C
C PLATE Plate 1e)
DEPO OX 0.6
DEPO RST 1.0
MASK NEG CONT 0 0
ETCH ERST 1.1
ETCH OX 0.9
ETCH RST 1.1
C
C Plate 1f)
DEPO METL 0.7
DEPO RST 1.0
MASK POS MTL 0 0
ETCH ERST 1.1
ETCH METL 0.8
ETCH RST 1.1
```

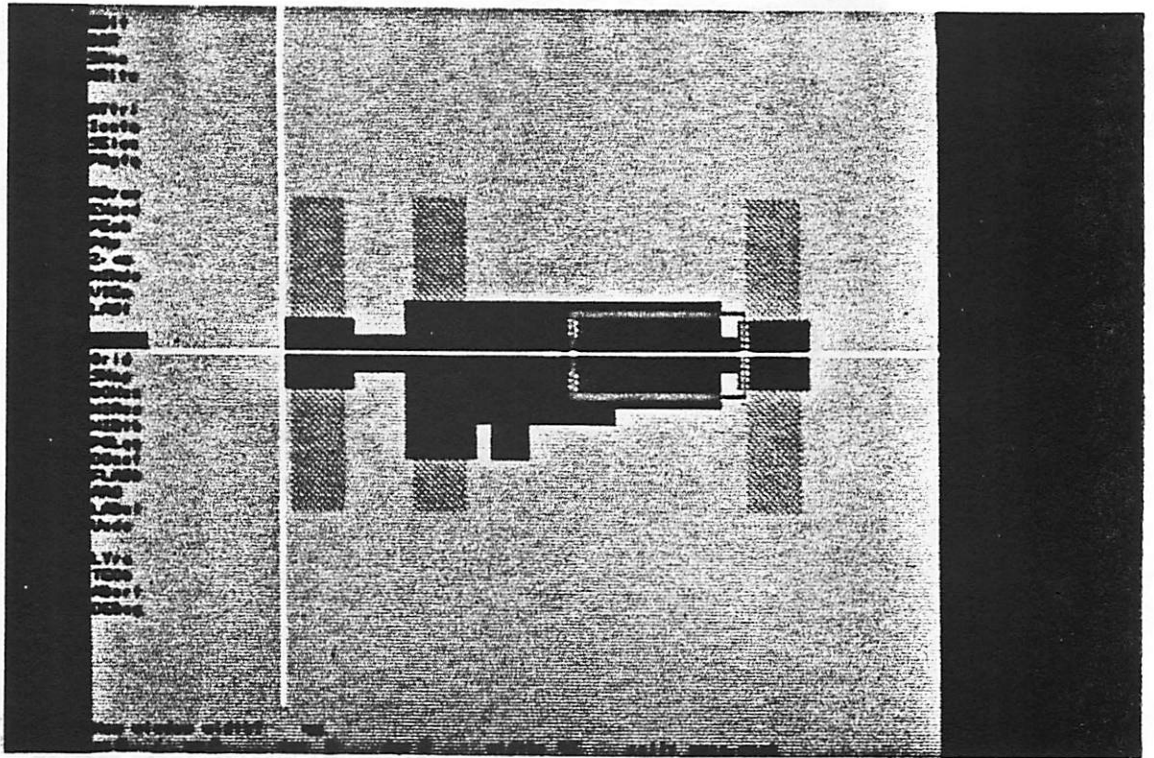

Figure 2. NMOS Inverter Layout

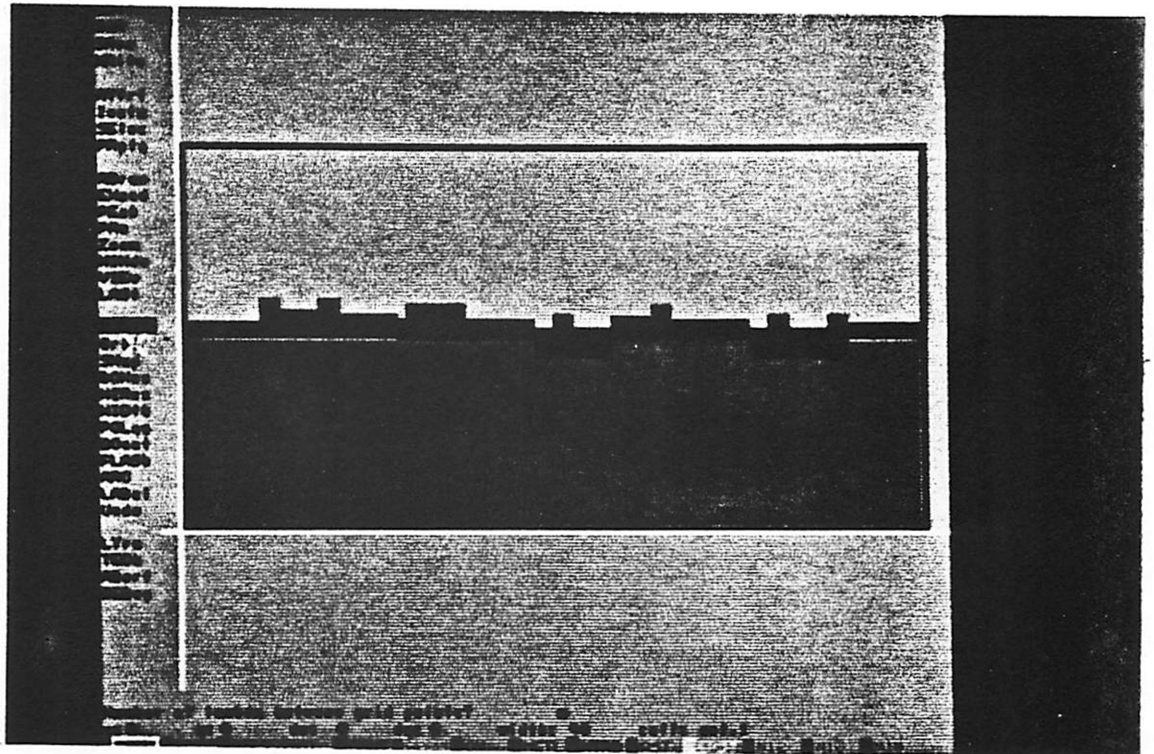

Figure 3. Horizontal cutline NMOS cross section.

Figure 4. Vertical cutline NMOS cross section.

Fig. 5. GaAs SIMPL-1 process listing.

```
SUBS P 1E15
DEPO N 1E17 0.2
DEPO OX 0.8
DEPO RST 1.0
MASK NEG NNII 0 0
ETCH ERST 1.1
ETCH OX 0.9
DOPE N 1E18 0.09 0.085 0.5
ETCH RST 1.1
ETCH OX 0.9
DEPO OX 0.8
DEPO RST 1.0
MASK POS PPII 0 0
ETCH ERST 1.1
ETCH OX 0.9
DOPE P 2E18 0.09 0.143 0.5
ETCH RST 1.1
ETCH OX 0.9
DEPO METL 0.1
DEPO RST 1.0
MASK POS NNII 0 0
ETCH ERST 1.1
ETCH METL 0.3
ETCH RST 1.1
DEPO L1 0.2
DEPO OX 0.8
DEPO RST 1.00
MASK POS MTL1 0 0
ETCH ERST 1.1
ETCH OX 0.9
ETCH L1 0.3
ETCH RST 1.1
ETCH OX 0.9
DEPO OX 0.2
DEPO RST 1.1
MASK NEG CONT 0 0
ETCH ERST 1.1
ETCH OX 0.7
ETCH RST 1.1
DEPO L2 0.4
DEPO OX 0.3
DEPO RST 1.0
MASK POS MTL2 0 0
ETCH ERST 1.1
ETCH OX 0.4
ETCH L2 0.5
ETCH RST 1.1
DEPO RST 1.0
MASK NEG MTL2 0 0
ETCH ERST 1.1
ETCH OX 0.4
ETCH RST 1.1
```

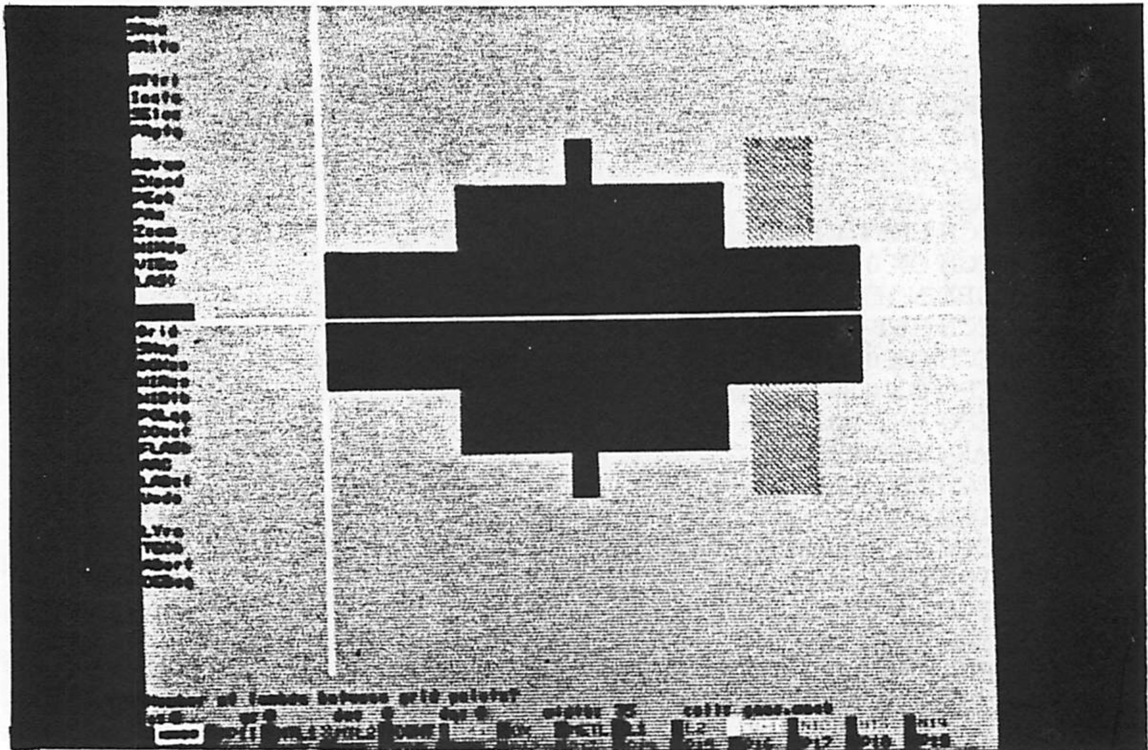

Figure 6. GaAs FET layout.

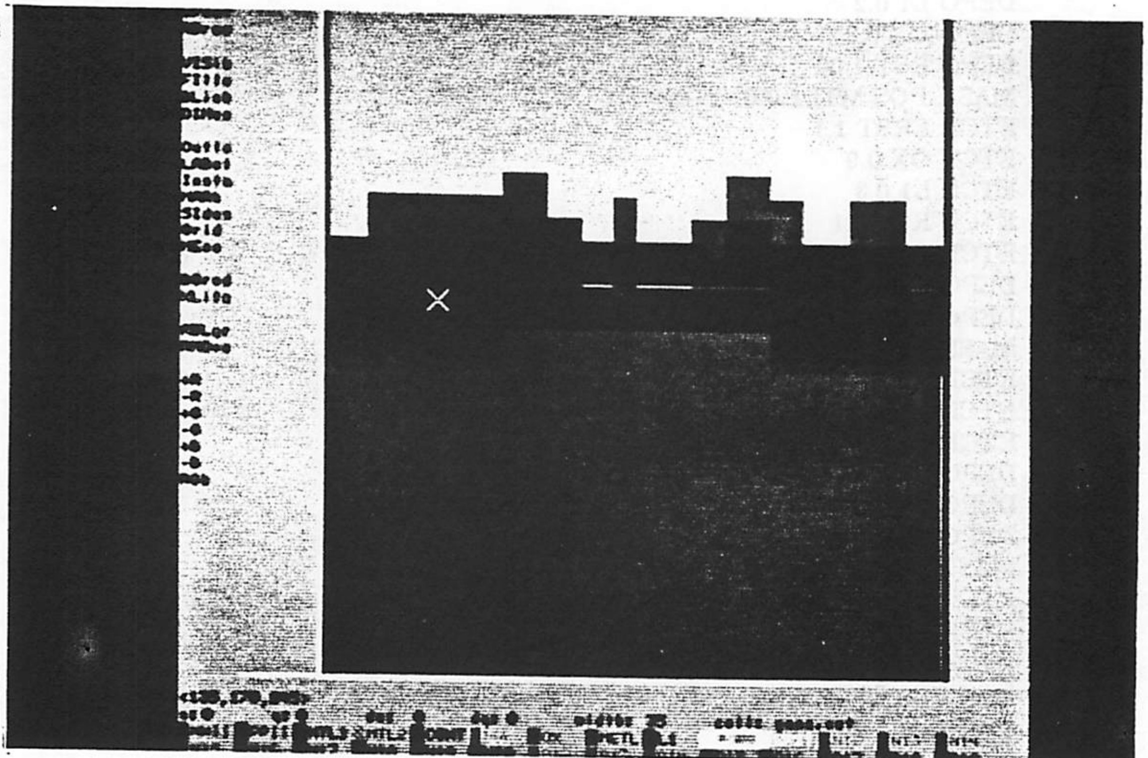

Figure 7. GaAs FET cross section

Fig. 8. ABCMOS SIMPL-1 process listing.

```
SUBS P 1e14
OXID 0.1
DEPO NTRD 0.1
DEPO RST 0.5
MASK POS WELL 0 0
ETCH ERST 0.6
ETCH NTRD 0.2
ETCH RST 0.6
OXID 0.5
ETCH NTRD 0.2
DOPE N 1.1e15 1.5 0 0.2
ETCH OX 0.7
OXID 0.1
DEPO NTRD 0.1
DEPO RST 0.5
MASK POS ACTV 0 0
ETCH ERST 0.6
ETCH NTRD 0.2
ETCH RST 0.6
DEPO RST 1.0
MASK POS WELL 0 0
ETCH ERST 1.1
DOPE P 1e19 0.15 0.05 0.2
ETCH RST 1.1
OXID 0.7
ETCH NTRD 0.2
DOPE P 1e20 0.5 0 0.2
DEPO POLY 0.25
DEPO RST 0.5
MASK POS POLY 0 0
ETCH ERST 0.6
ETCH POLY 0.6
ETCH RST 0.6
DEPO RST 1.0
MASK NEG NNII 0 0
ETCH ERST 1.1
DOPE N 1e21 0.22 0.1 1.0
ETCH RST 1.1
DEPO RST 1.0
MASK NEG PPII 0 0
ETCH ERST 1.1
DOPE P 0e21 0.2 0.1 0.2
ETCH RST 1.1
DEPO OX 0.3
DEPO RST 1.0
MASK NEG CONT 0 0
ETCH ERST 1.1
ETCH OX 1.3
ETCH RST 1.1
DEPO METL 1.2
DEPO RST 1.0
```

```
MASK POS METL 0 0
ETCH ERST 1.1
ETCH METL 1.3
ETCH RST 1.1
```

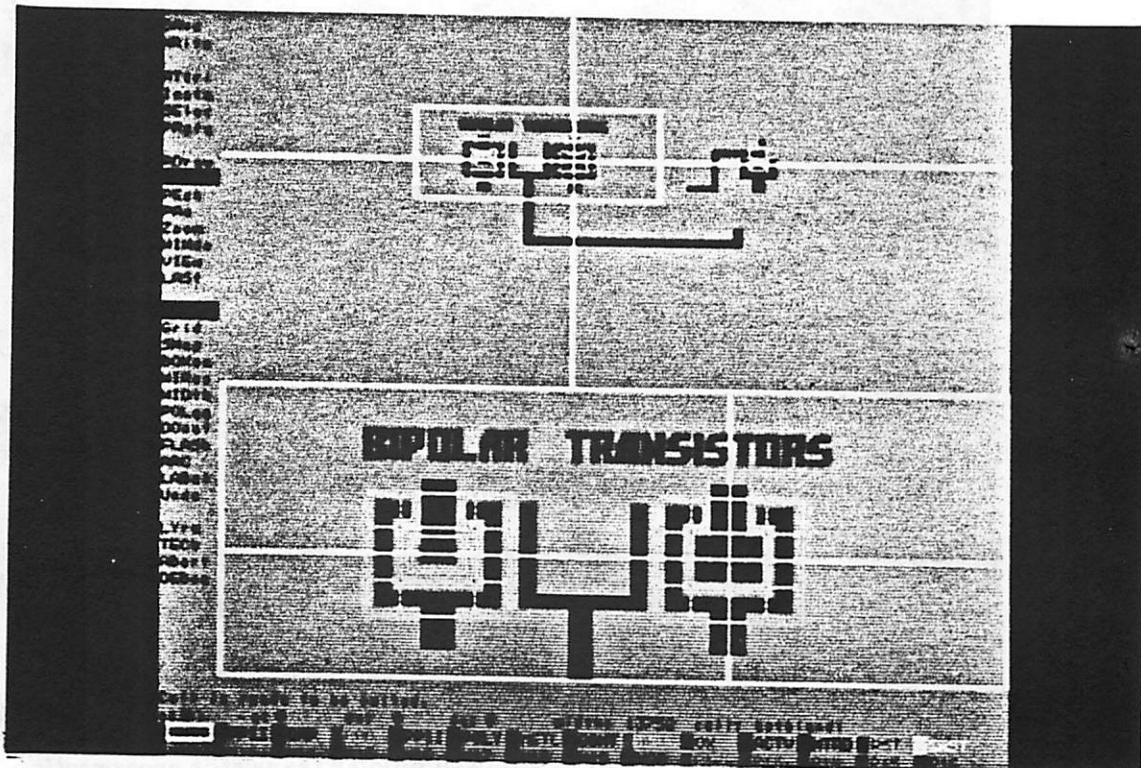

Figure 9. ABCMOS bipolar transistor layout.

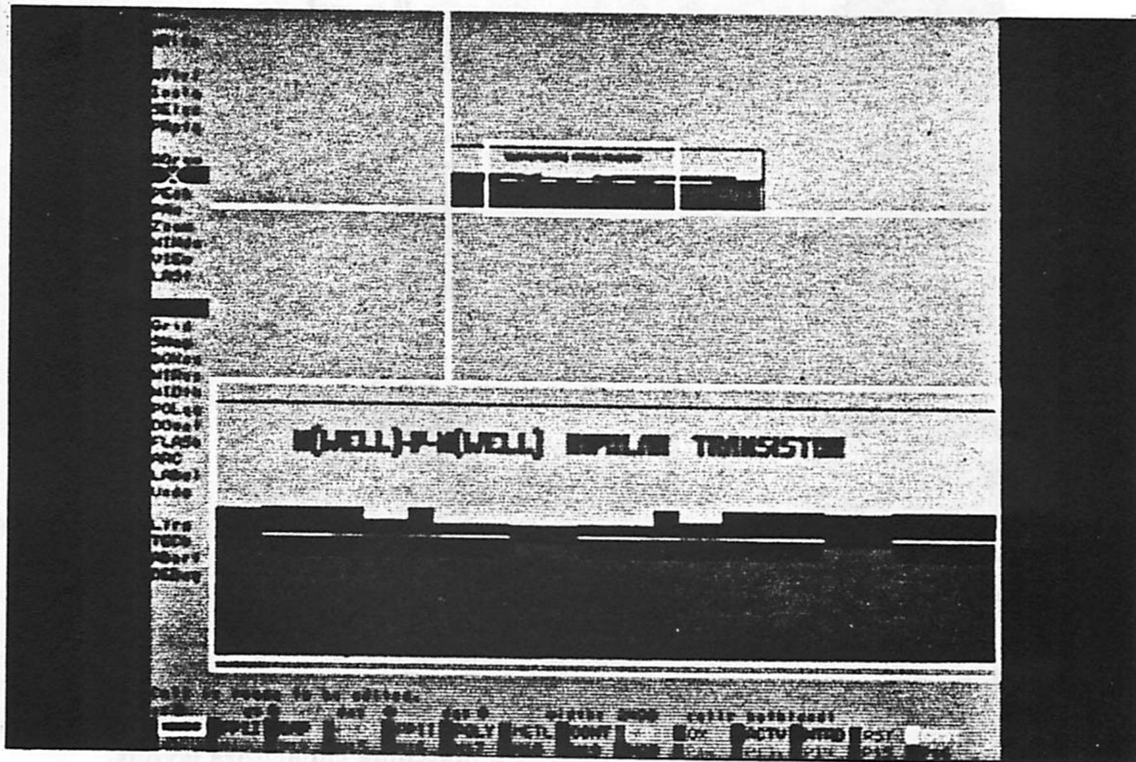

Figure 10. ABCMOS nwell-p-nwell bipolar transistor cross section.

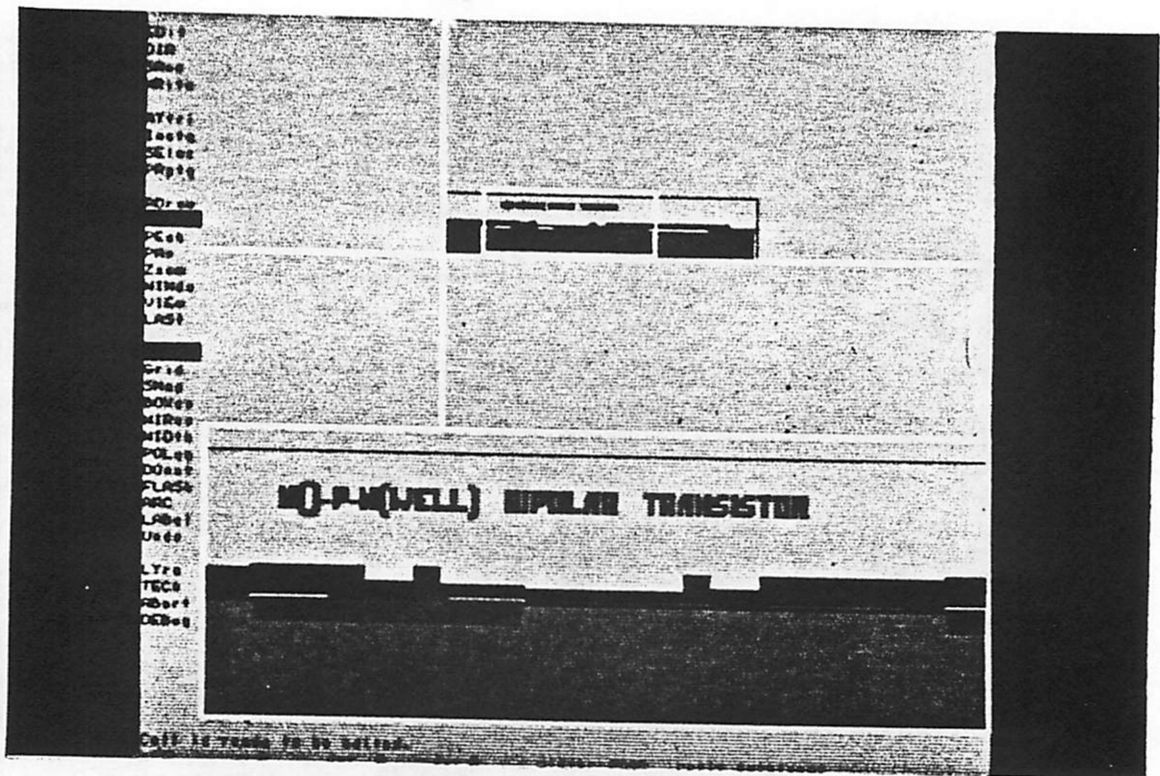

Figure 11. ABCMOS n^+-p-nwell bipolar transistor cross section

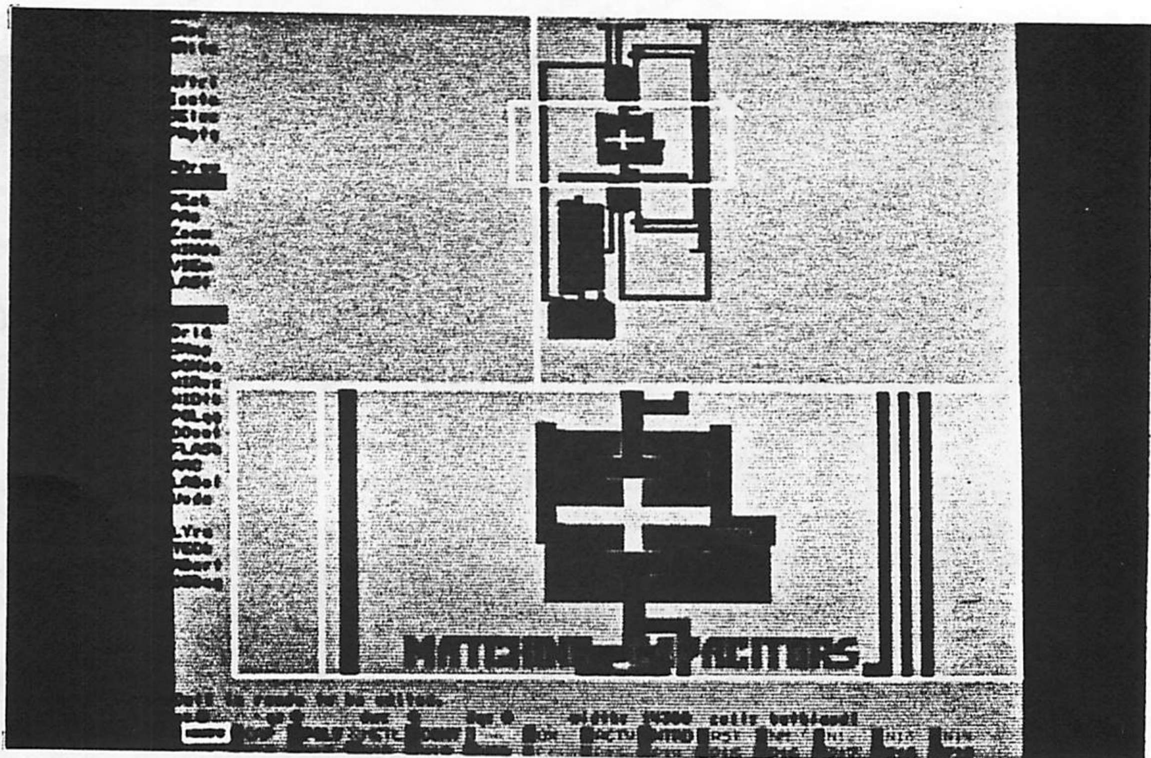

Figure 12. ABCMOS matching capacitors layout.

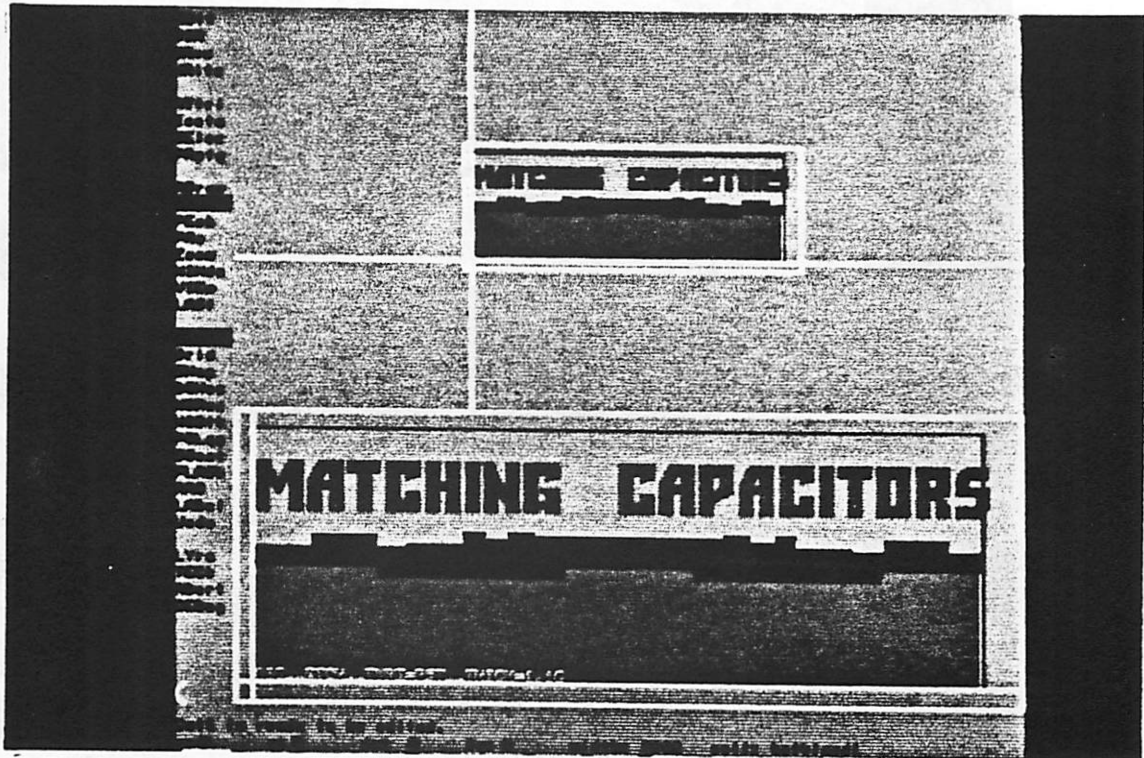

Figure 13. ABCMOS matching capacitors cross section.

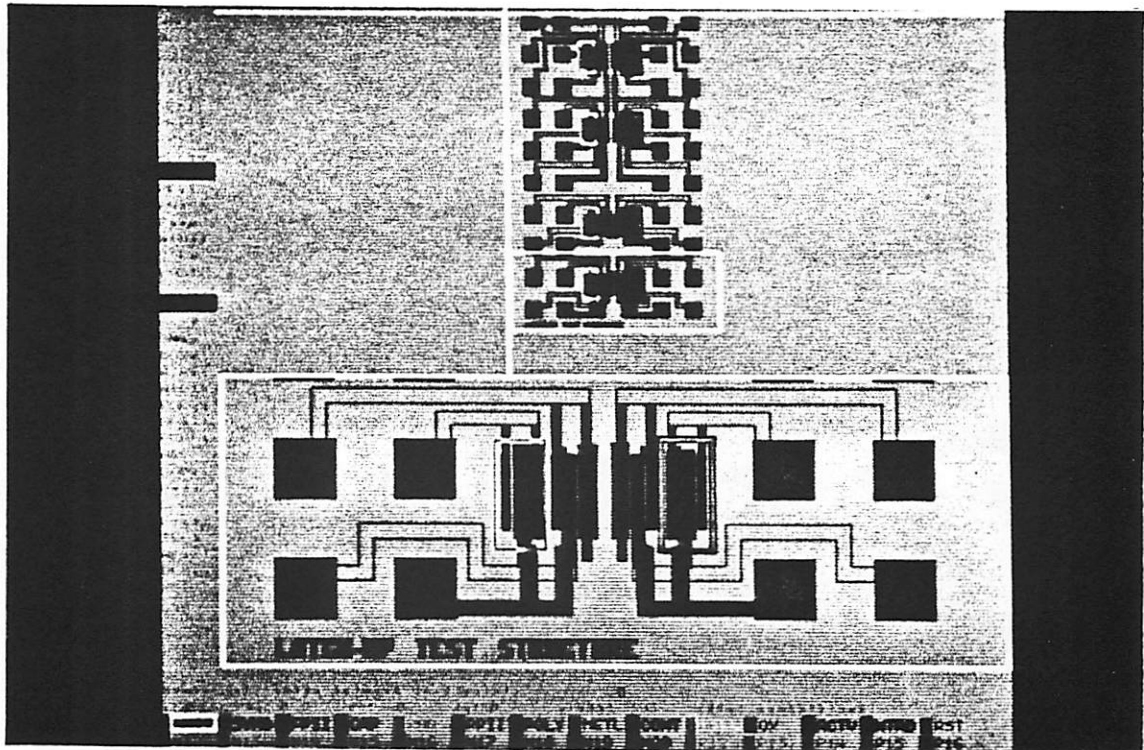

Figure 14. ABCMOS latchup test structure layout.

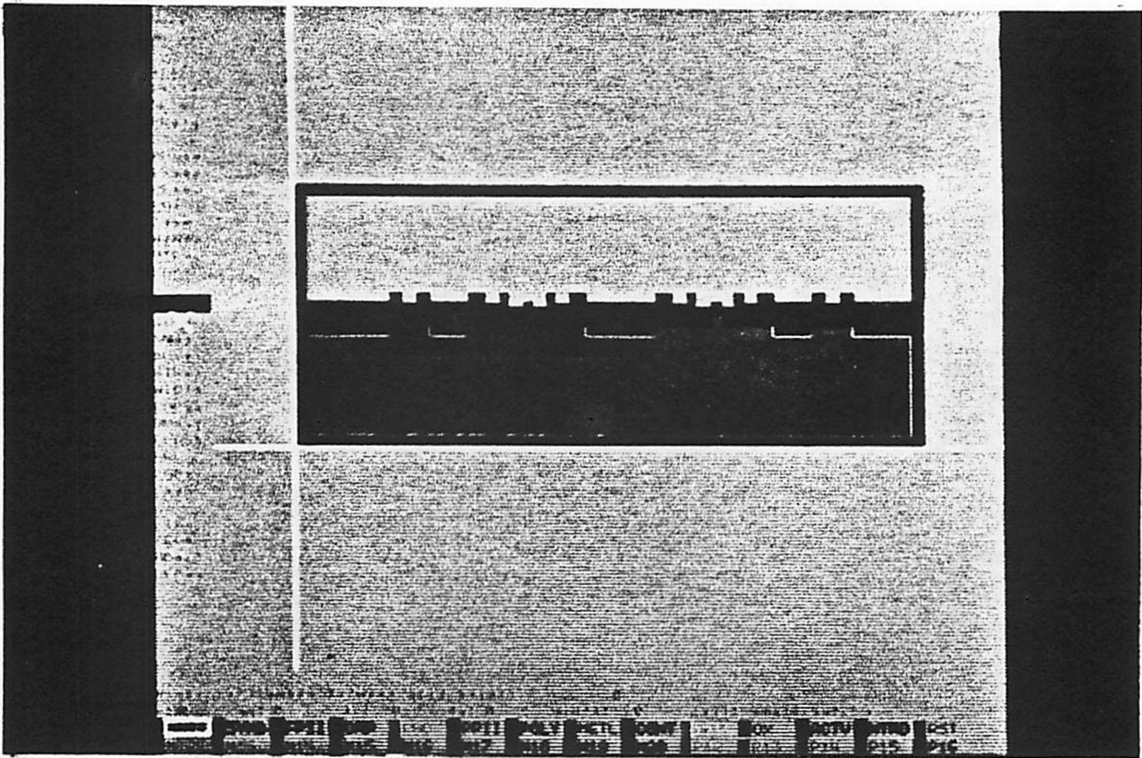

Figure 15. ABCMOS latchup test structure cross section.

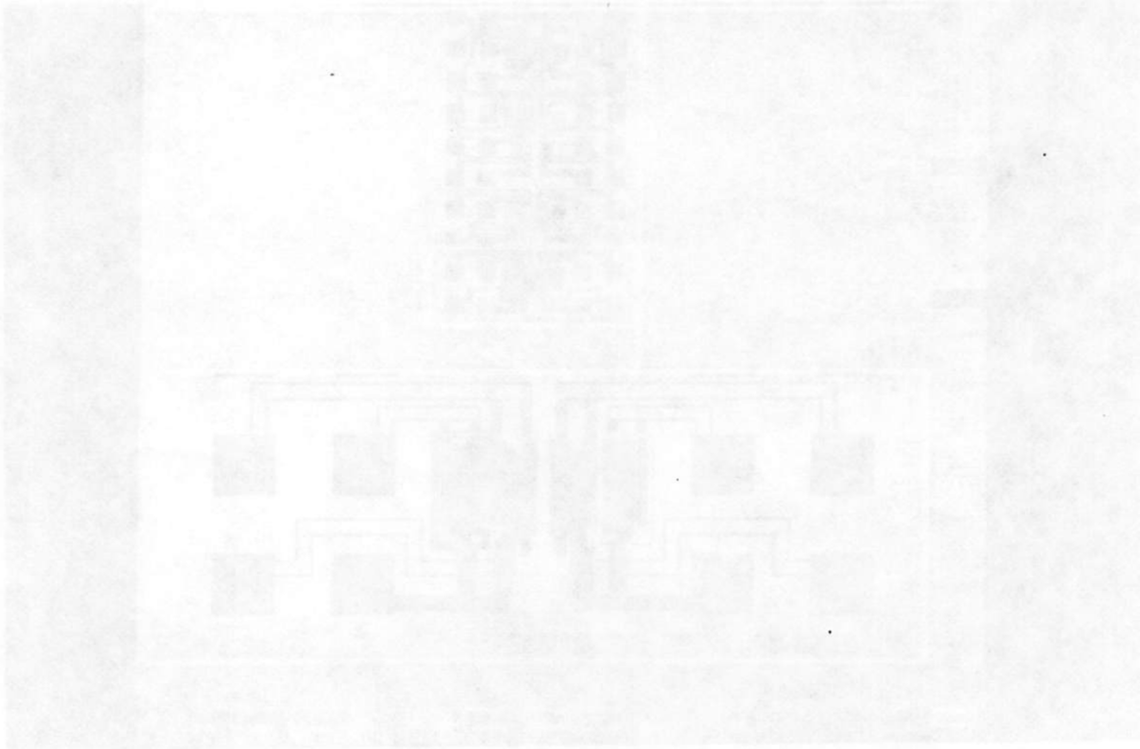

Fig. 16 Magnetocoupler SIMPL-1 process listing.

```
SUBS P 1E14
DEPO OX 0.8
DEPO RST 1.0
MASK NEG NI 0 0
ETCH ERST 1.1
ETCH OX 0.9
DOPE N 1E18 0.76 0.0 0.5
ETCH RST 1.1
ETCH OX 0.9
DEPO N 5E15 7.6
C Isolation implant
DEPO OX 0.8
DEPO RST 1.0
MASK POS PP 0 0
ETCH ERST 1.1
ETCH OX 0.9
DOPE P 2E17 4.5 0.0 0.5
ETCH RST 1.1
ETCH OX 0.9
C Base implant
DEPO OX 0.8
DEPO RST 1.0
MASK NEG PA 0 0
ETCH ERST 1.1
ETCH OX 0.9
DOPE P 2E18 0.796 0.0 0.5
ETCH RST 1.1
ETCH OX 0.9
C Emitter implant
DEPO OX 0.8
DEPO RST 1.0
MASK NEG NP 0 0
ETCH ERST 1.1
ETCH OX 0.9
DOPE N 5E19 0.376 0.0 0.5
ETCH RST 1.1
ETCH OX 0.9
C Contacts; oxide (CVD) = 0.5 micron
DEPO OX 0.5
DEPO RST 1.0
MASK NEG CH 0 0
ETCH ERST 1.1
ETCH OX 0.6
ETCH RST 1.1
C Metal
DEPO METL 1.2
DEPO RST 0.1
MASK POS ME 0 0
ETCH ERST 1.1
ETCH METL 1.3
ETCH RST 1.1
```

Figure 17. Magnetocoupler layout.

Figure 18. Magnetocoupler cross section.

Fig. 19. Berkeley p-well SIMPL-2 process listing.

```
WHICH PROCESS ? OXID
OXIDE THICKNESS (micro-meter) ? 0.100000
Xt (micro-meter) ? 0.100000
Xe (micro-meter) ? 0.050000
u1 ? 0.100000
u2 ? 0.500000
u3 ? 0.900000
d1 ? 0.100000
d2 ? 0.500000
d3 ? 0.900000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? n
DOSE (cm**(-2)) ? 1.000000e+12
STANDARD DEVIATION (micro-meter) ? 0.825000
PEAK DEPTH (micro-meter) ? 0.155000
BLOCK THICKNESS (micro-meter) ? 0.200000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? RST
THICKNESS OF THE MATERIAL (micro-meter) ? 1.000000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? PWEL
INVERT THE MASK (yes or no) ? yes
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? p
DOSE (cm**(-2)) ? 3.000000e+12
STANDARD DEVIATION (micro-meter) ? 1.000000
PEAK DEPTH (micro-meter) ? 1.000000
BLOCK THICKNESS (micro-meter) ? 1.000000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? OXID
ETCH ALL (yes or no) ? no
AMOUNT OF VERTICAL ETCH (micro_meter) ? 0.100000
RATIO X/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.000000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? RST
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? OXID
OXIDE THICKNESS (micro-meter) ? 0.300000
Xt (micro-meter) ? 0.300000
```

```
Xe (micro-meter) ? 0.150000
u1 ? 0.100000
u2 ? 0.500000
u3 ? 0.900000
d1 ? 0.100000
d2 ? 0.500000
d3 ? 0.900000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? OXID
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? END
WHICH PROCESS ? OXID
OXIDE THICKNESS (micro-meter) ? 0.020000
Xt (micro-meter) ? 0.020000
Xe (micro-meter) ? 0.010000
u1 ? 0.100000
u2 ? 0.500000
u3 ? 0.900000
d1 ? 0.100000
d2 ? 0.500000
d3 ? 0.900000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? NTRD
THICKNESS OF THE MATERIAL (micro-meter) ? 0.100000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? ACTV
INVERT THE MASK (yes or no) ? no
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? RST
THICKNESS OF THE MATERIAL (micro-meter) ? 1.000000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? PWEL
INVERT THE MASK (yes or no) ? yes
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? p
DOSE (cm**(-2)) ? 5.000000e+12
STANDARD DEVIATION (micro-meter) ? 0.070000
```

```
PEAK DEPTH (micro-meter) ? 0.300000
BLOCK THICKNESS (micro-meter) ? 0.100000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? RST
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? OXID
ETCH ALL (yes or no) ? no
AMOUNT OF VERTICAL ETCH (micro_meter) ? 0.020000
RATIO X/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.000000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? OXID
OXIDE THICKNESS (micro-meter) ? 0.550000
Xt (micro-meter) ? 0.550000
Xe (micro-meter) ? 0.275000
u1 ? 0.100000
u2 ? 0.500000
u3 ? 0.900000
d1 ? 0.100000
d2 ? 0.500000
d3 ? 0.900000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? NTRD
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? END
WHICH PROCESS ? OXID
OXIDE THICKNESS (micro-meter) ? 0.020000
Xt (micro-meter) ? 0.020000
Xe (micro-meter) ? 0.010000
u1 ? 0.100000
u2 ? 0.500000
u3 ? 0.900000
d1 ? 0.100000
d2 ? 0.500000
d3 ? 0.900000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? p
DOSE (cm**(-2)) ? 2.000000e+11
STANDARD DEVIATION (micro-meter) ? 0.037000
PEAK DEPTH (micro-meter) ? 0.100000
BLOCK THICKNESS (micro-meter) ? 0.030000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? OXID
OXIDE THICKNESS (micro-meter) ? 0.050000
Xt (micro-meter) ? 0.050000
Xe (micro-meter) ? 0.025000
u1 ? 0.100000
u2 ? 0.500000
u3 ? 0.900000
```

```
d1 ? 0.100000
d2 ? 0.500000
d3 ? 0.900000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? POLY
THICKNESS OF THE MATERIAL (micro-meter) ? 0.450000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? RST
THICKNESS OF THE MATERIAL (micro-meter) ? 1.000000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? POLY
INVERT THE MASK (yes or no) ? no
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? POLY
ETCH ALL (yes or no) ? no
AMOUNT OF VERTICAL ETCH (micro_meter) ? 0.450000
RATIO X/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.000000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? RST
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? RST
THICKNESS OF THE MATERIAL (micro-meter) ? 1.000000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? N+ II
INVERT THE MASK (yes or no) ? yes
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? n
DOSE (cm**(-2)) ? 1.000000e+ 15
STANDARD DEVIATION (micro-meter) ?0.0800000
PEAK DEPTH (micro-meter) ? 0.010000
BLOCK THICKNESS (micro-meter) ? 0.500000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? RST
```

```
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? RST
THICKNESS OF THE MATERIAL (micro-meter) ? 1.000000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? N+ II
INVERT THE MASK (yes or no) ? no
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? p
DOSE (cm**(-2)) ? 2.000000e+ 15
STANDARD DEVIATION (micro-meter) ? 0.130000
PEAK DEPTH (micro-meter) ? 0.000000
BLOCK THICKNESS (micro-meter) ? 0.500000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? RST
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? END
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? PSG
THICKNESS OF THE MATERIAL (micro-meter) ? 0.700000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? CONT
INVERT THE MASK (yes or no) ? yes
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? OXID
ETCH ALL (yes or no) ? no
AMOUNT OF VERTICAL ETCH (micro_meter) ? 0.100000
RATIO X/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.000000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? METL
THICKNESS OF THE MATERIAL (micro-meter) ? 0.800000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? A
SPUTTERING SOURCE ANGLE (degrees) ? 45.000000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? MTL
```

```
INVERT THE MASK (yes or no) ? no
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? END
```

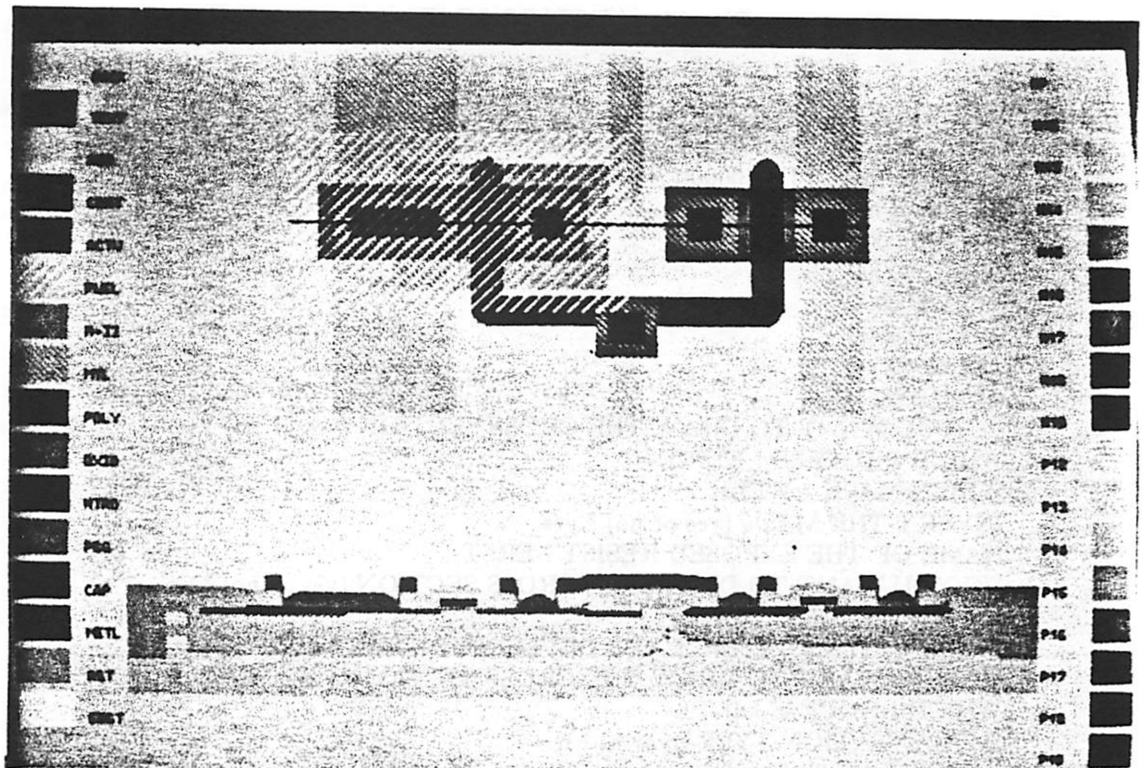

Figure 20. Berkeley p-well inverter.

Fig. 21. ABCMOS SIMPL-2 process listing.

```
WHICH PROCESS ? OXID
OXIDE THICKNESS (micro-meter) ? 0.100000
Xt (micro-meter) ? 0.100000
Xe (micro-meter) ? 0.050000
u1 ? 0.100000
u2 ? 0.500000
u3 ? 0.900000
d1 ? 0.100000
d2 ? 0.500000
d3 ? 0.900000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? WELL
INVERT THE MASK (yes or no) ? yes
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? n
DOSE (cm**(-2)) ? 1.750000e+ 12
STANDARD DEVIATION (micro-meter) ? 1.500000
PEAK DEPTH (micro-meter) ? 0.500000
BLOCK THICKNESS (micro-meter) ? 0.050000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? END
WHICH PROCESS? ETCH
? OXID
? yes
? no
WHICH PROCESS ? OXID
OXIDE THICKNESS (micro-meter) ? 0.020000
Xt (micro-meter) ? 0.020000
Xe (micro-meter) ? 0.010000
u1 ? 0.100000
u2 ? 0.500000
u3 ? 0.900000
d1 ? 0.100000
d2 ? 0.500000
d3 ? 0.900000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? NTRD
THICKNESS OF THE MATERIAL (micro-meter) ? 0.100000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
? WAIT
WHICH PROCESS ? EXPO
WHICH MASK ? ACTV
INVERT THE MASK (yes or no) ? no
```

```
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
? WAIT
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
? WAIT
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? RST
THICKNESS OF THE MATERIAL (micro-meter) ? 1.200000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
? WAIT
WHICH PROCESS ? EXPO
WHICH MASK ? WELL
INVERT THE MASK (yes or no) ? no
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
? WAIT
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? p
DOSE (cm**(-2)) ? 1.000000e+ 13
STANDARD DEVIATION (micro-meter) ? 0.150000
PEAK DEPTH (micro-meter) ? 0.050000
BLOCK THICKNESS (micro-meter) ? 0.050000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
? ETCH
? RST
? yes
? no
? WAIT
WHICH PROCESS ? OXID
OXIDE THICKNESS (micro-meter) ? 0.650000
Xt (micro-meter) ? 0.650000
Xe (micro-meter) ? 0.325000
u1 ? 0.100000
u2 ? 0.500000
u3 ? 0.900000
d1 ? 0.100000
d2 ? 0.500000
d3 ? 0.900000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? NTRD
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? END
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? p
DOSE (cm**(-2)) ? 2.300000e+ 12
STANDARD DEVIATION (micro-meter) ? 0.050000
```

```
PEAK DEPTH (micro-meter) ? 0.000000
BLOCK THICKNESS (micro-meter) ? 0.100000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? POLY
THICKNESS OF THE MATERIAL (micro-meter) ? 0.400000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? POLY
INVERT THE MASK (yes or no) ? no
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? RST
THICKNESS OF THE MATERIAL (micro-meter) ? 1.200000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? PPII
INVERT THE MASK (yes or no) ? no
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? n
DOSE (cm**(-2)) ? 1.200000e+ 15
STANDARD DEVIATION (micro-meter) ? 0.100000
PEAK DEPTH (micro-meter) ? 0.050000
BLOCK THICKNESS (micro-meter) ? 0.200000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? RST
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? RST
THICKNESS OF THE MATERIAL (micro-meter) ? 1.200000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? PPII
INVERT THE MASK (yes or no) ? yes
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
? DEVL
? ERST
? no
WHICH PROCESS ? IMPL
```

```
IMPLANTATION TYPE (p or n) ? p
DOSE (cm**(-2)) ? 1.200000e+ 15
STANDARD DEVIATION (micro-meter) ? 0.100000
PEAK DEPTH (micro-meter) ? 0.050000
BLOCK THICKNESS (micro-meter) ? 0.200000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? RST
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? END
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? PSG
THICKNESS OF THE MATERIAL (micro-meter) ? 0.600000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? CONT
INVERT THE MASK (yes or no) ? yes
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? OXID
ETCH ALL (yes or no) ? no
AMOUNT OF VERTICAL ETCH (micro_meter) ? 0.020000
RATIO X/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.000000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? MTL
THICKNESS OF THE MATERIAL (micro-meter) ? 0.500000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? A
? 45
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? METL
INVERT THE MASK (yes or no) ? no
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? ERST
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? END
```

Figure 22. ABCMOS matching capacitors.

Figure 23. ABCMOS latchup test structure.

Fig. 24. DRAM SIMPL-2 process listing.

```
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? NTRD
THICKNESS OF THE MATERIAL (micro-meter) ? 0.500000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? BTLN
INVERT THE MASK (yes or no) ? no
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? OXID
OXIDE THICKNESS (micro-meter) ? 0.300000
Xt (micro-meter) ? 0.300000
Xe (micro-meter) ? 0.150000
u1 ? 0.100000
u2 ? 0.500000
u3 ? 0.900000
d1 ? 0.100000
d2 ? 0.500000
d3 ? 0.900000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? NTRD
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? IMPL
IMPLANTATION TYPE (p or n) ? n
DOSE (cm**(-2)) ? 1.000000e+ 13
STANDARD DEVIATION (micro-meter) ? 0.150000
PEAK DEPTH (micro-meter) ? 0.000000
BLOCK THICKNESS (micro-meter) ? 0.200000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? END
WHICH PROCESS? DEPO
?  RST
? 1.0
? I
? no
WHICH PROCESS? EXPO
WHICH MASK ? TRCH
INVERT THE MASK (yes or no) ? yes
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? SI
```

```
ETCH ALL (yes or no) ? no
AMOUNT OF VERTICAL ETCH (micro_meter) ? 1.0
RATIO X/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.035000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? RST
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? END
```

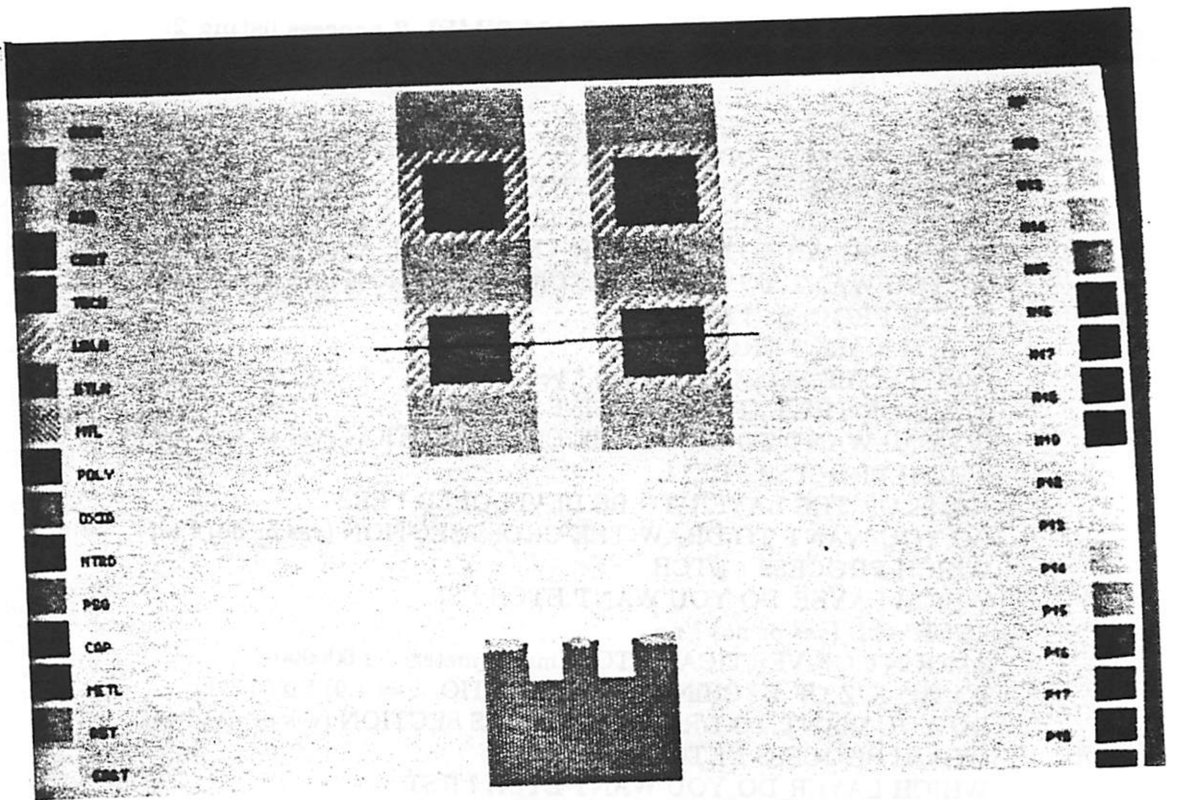

Figure 25. DRAM cross section 1.

Fig. 26. DRAM SIMPL-2 process listing 2.

```
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? RST
THICKNESS OF THE MATERIAL (micro-meter) ? 1.000000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? EXPO
WHICH MASK ? TRCH
INVERT THE MASK (yes or no) ? yes
NAME OF THE EXPOSED RESIST ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEVL
NAME OF THE LAYER TO BE DEVELOPED ? ERST
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? SI
ETCH ALL (yes or no) ? no
AMOUNT OF VERTICAL ETCH (micro_meter) ? 2.000000
RATIO X/Z OF ETCHING (0.0 <= RATIO <= 1.0) ? 0.035000
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? ETCH
WHICH LAYER DO YOU WANT ETCH ? RST
ETCH ALL (yes or no) ? yes
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? no
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? OXID
THICKNESS OF THE MATERIAL (micro-meter) ? 0.100000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? END
WHICH PROCESS ? DEPO
NAME OF THE MATERIAL ? POLY
THICKNESS OF THE MATERIAL (micro-meter) ? 0.750000
ISOTROPIC, ANISOTROPIC, OR VERTICAL (I, A, or V) ? I
DO YOU WANT TO DRAW THE CROSS SECTION (yes or no) ? yes
WHICH PROCESS ? END
```

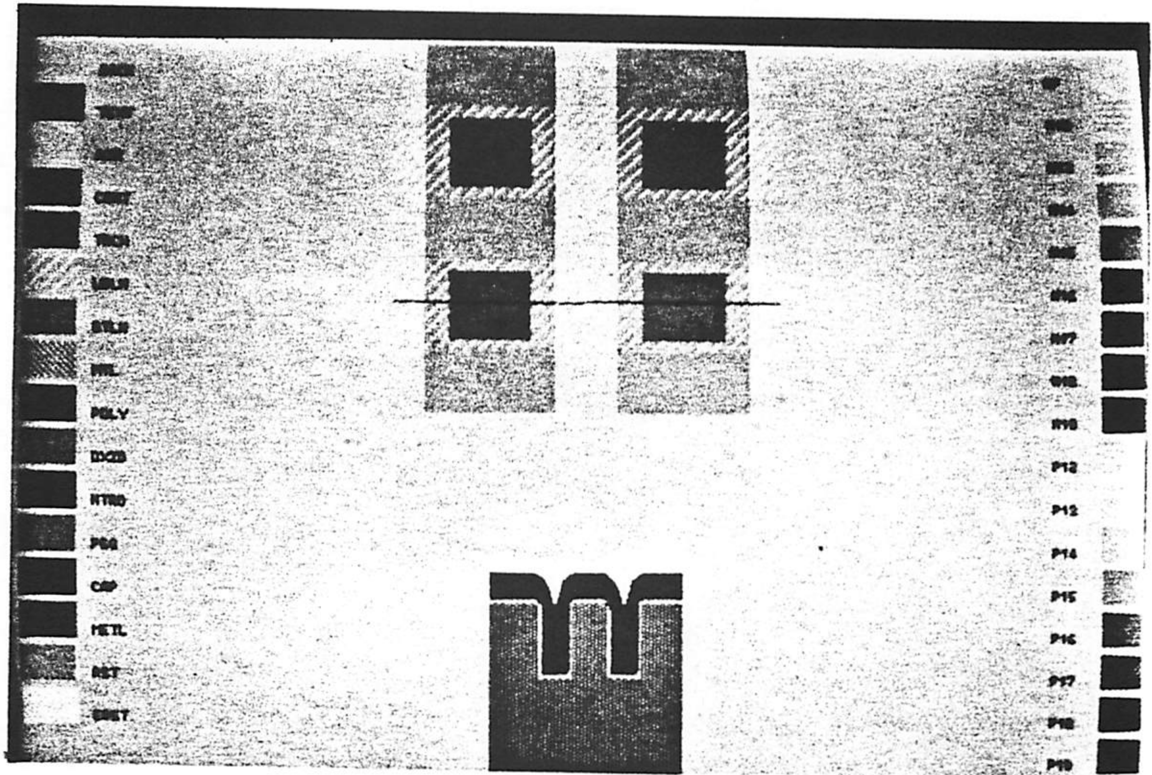

Figure 27. DRAM cross section 2.