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Characterization of the BORON+® Planar Dopant Source Moisture Enhanced Process

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Abstract

BORON+ ® solid planar dopant sources have long been used in semiconductor device fabrication, mainly for diffusion of boron in bipolar devices. This paper examines the possibility of expanding the use of planar source wafers to lower temperatures enabling cmos applications. By adding a small amount of moisture (15-120 ppm) to the ambient, relatively high surface concentrations can be obtained. This process was characterized and deposition conditions determined for p-channel source and drain diffusion. Devices were successfully fabricated with minor process modifications.

Introduction

Solid planar dopant sources have long been used in solid state device fabrication, typically in applications where their simplicity and low cost make them the obvious choice over alternative methods such as ion implantation or spin-on dopant. They have been less frequently used in the processing of high-density integrated circuits, though the potential advantages over ion implantation of no channeling or topography-related shadowing effects would seem to make them worth consideration for this as well.

This paper concentrates on the characterization of the solid planar dopant sources by Owens-Illinois, BORON+ ® GS-126, in which the dopant is part of a glass-ceramic material. The results for this type of source are compared with those for ion implantation and for Boron Nitride, a planar dopant source manufactured by Carborundum Corporation.

The first section is concerned with developing and characterizing a moisture enhanced process. Because of low processing temperatures and high achievable surface concentrations using the Boron+ solid dopant sources in a moisture-enhanced ambient, the deposition process is potentially a viable technique for fabricating shallow sources and drains for p-channel devices in cmos technology. This is of particular interest because shallow p+ junctions cannot be realized by conventional ion implantation due to channeling effects [1].

The second section includes fabrication of cmos test devices and circuits using the Boron+ process for p-channel source and drain diffusion.

Boron Planar Dopant Sources

A generic planar dopant source process is shown in Figure 1. The silicon wafer surfaces to be doped are placed facing and in proximity to the planar dopant sources in a horizontal atmospheric furnace. The ambient gas, which is usually nitrogen but can be helium or argon, may contain additives to influence the nature of the dopant transport between source and silicon wafers [2]. This transport is accomplished by some doping specie, usually an oxide of the elemental dopant (for example, B_2O_3 for boron) evolving off the planar dopant sources and re-depositing on all

nearby surfaces including the silicon wafers. Once at the silicon surface, a heavily doped borosilicate glass results, from which some of the elemental dopant is then transferred and diffused into the underlying silicon. The B_2O_3 can also diffuse into silicon oxide if this happens to be underneath. Here the B_2O_3 remains in the oxidized state. This later transfer or diffusion occurs either in the the same step as the dopant deposition or in a subsequent higher temperature step if greater doping of the silicon is required.

Two types of boron planar dopant sources are in common use. The first consists of wafers of boron nitride specifically manufactured for use as diffusion sources. For this project BN-975 boron nitride sources from the Carborandum Corporation were used. Prior to the actual dopant deposition on silicon wafers, BN sources must undergo a "recovery" furnace cycle in an oxygen-rich ambient to create a thin layer of B_2O_3 on the source wafers' surface. This is necessary because the vapor pressure of BN is too low to achieve significant transfer of dopant to the silicon wafers [3]. This oxidation cycle must be repeated periodically as the B_2O_3 layer is consumed in the deposition process.

After this step, transfer of the dopant to the silicon wafers can be accomplished by the evolution of B_2O_3 vapor in one of the carrier gases mentioned above. However, the favored approach for reduced silicon defects and low junction leakage involves the controlled introduction of a small quantity of moisture into the system in a process typically called "H_2 injection" [4]. The dominant transport specie then becomes HBO_2, which has a vapor pressure several orders of magnitude higher than that of B_2O_3. This leads to a much faster dopant transfer to the silicon wafers and in turn to the fixing or "pinning" of surface silicon defects in the resulting super-saturated boron-silicon phase. These defects are then removed when this phase is later oxidized at a low temperature and etched away.

The second type of boron planar source consists of a glass-ceramic, a crystallized glass of B_2O_3, BaO, MgO, Al_2O_3 and SiO_2 [5]. Owens-Illinois Boron+ ® GS-126 sources were used in this project. The primary purpose of the multiple constituent glass is to provide rigidity to the sources since pure B_2O_3 melts at 460°C. A secondary purpose is to keep impurities, especially mobile ions,

from taking part in the deposition by tying them up in the glass and by reducing the vapor pressure of these impurities which are in solution in the glass. Much lower levels of deposited impurities are claimed for this type of source. Since B_2O_3 already exists in the source, no recovery cycle is necessary. However, because the fractional B_2O_3 content is less than unity, the content at the surface, where B_2O_3 is vaporized, must be constantly replenished by diffusion from the interior of the source. These sources have primarily been used in "dry processes"; those with the ambient or carrier gas being pure nitrogen, and not with H_2-injection processes because the diffusion from the interior of the source must not be exceeded by the vapor evolution rate at the surface if a uniform, repeatable process is to be achieved. If, however, reduced moisture levels (usually less than 0.1% of the carrier gas rather than the approximately one per cent used with BN sources) are used then some sort of "moisture enhanced" process can be made to work. Evaluation of this type of process is the main thrust of this paper.

The two types of sources have several characteristics in common. B_2O_3 readily absorbs moisture and this makes for significant and non-uniform changes in the deposition rate. Both types of sources must experience only brief exposures to room air, although, of the two the BN source has the more severe problem because on its oxidized surface the B_2O_3 content is unity and absorbs ~ 1% moisture, while the Boron+ source surface content is a fraction of this and can absorb only 0.01% moisture [6]. Typical practice is to store the sources in the same furnace in which the dopant deposition is done at a reduced temperature, and to limit the load and unload times when the sources are in room air. The dopant glass deposition thickness on the silicon wafers is dependent on their separation from the sources, so a special quartz boat is used to insure that sources and silicon wafers are parallel and equidistant. Both types of sources are prone to warpage due to thermal gradients across them so boats containing sources are slowly withdrawn from and inserted into the furnace and silicon wafers are always kept on either side of every source to increase heat transfer from the center of the source and to reduce the gradient that occurs because the source edge cools more readily.

CMOS Process

It was mentioned in the introduction that the ultimate aim was selection of a doping process to be used in the fabrication of cmos p+ sources and drains. The cmos process was the 2.0 um gate, n-well, single-level metal process developed at the University of California at Berkeley [7]. The objective was to implement the new doping technique with minimal change to the rest of the cmos fabrication sequence. The p+ source/drain activation anneal was not changed.

The two primary concerns regarding the deviation from the standard all-implant process were first that the blocking oxide over the previously fabricated n+ sources and drains would be insufficient to block boron from the deposited doped glass, causing, at least, high contact and series source/drain resistances, and second, that the field and blocking oxide lost during removal of the deposited borosilicate glass would be excessive. Both of these concerns are addressed.

Evaluation Criteria

The following were to be criteria used in selecting the proper doping technique for use in the cmos process:

1) Deposited glass thickness

2) Field oxide loss

3) Sheet resistivity

4) The pattern effect:

   It has long been known that some boron doping techniques, in particular some of those using planar dopant sources, exhibit variable doping which is strongly dependent on the size of the silicon feature to be doped and its nearness to other such features. This has been shown to be due to the preference of the boron dopant adsorbed on the silicon to migrate to nearby oxide [8]. This occurs because of boron's high solubility in silicon dioxide, resulting in a relative deficiency of the dopant specie at the oxide surface. This diffusion of boron dopant away from the silicon results in a surface concentration gradient. Bare silicon wafers do not exhi-

bit this and large exposed silicon features do so to a lesser extent because there is no SiO_2 "sponge" present to absorb the available dopant. This phenomenon is usually called the "pattern effect".

5) Doping profiles and junction depth

6) Silicon surface defect density

7) Diodes

8) Cmos process and devices

Test Vehicle

For this project a test chip was designed and then laid out in KIC, Berkeley's own graphics editor. Masks for the GCA-Mann aligner-stepper were created with a GCA- Mann optical pattern generator. There were three mask levels: diffusion (openings in field oxide), contact via, and metal. This test chip is shown in Figure 2. There were two types of devices in the test vehicle: diffusion-to-substrate diodes and four-terminal diffused resistors.

The generic four-terminal diffused resistor used in this test chip is shown in Figure 3. Two dimensions were significant: L, the linewidth of the diffused resistor itself, and W, the width of the field oxide frame surrounding the resistor and separating it from the large diffusion that in turn surrounds the oxide frame. L was varied discreetly as 1.25, 2.5, 5.0, 10 and 40 um on the chip; W as 1.25, 5.0, 20 and >500 um. These variations were fully convolved: there was one resistor on the chip for every combination of L and W. The purpose of all these devices, which follow those of Abbasi [8], is to measure the variation in sheet resistance due to the pattern effect mentioned earlier.

The diodes on the test chip were all 80 um by 160 um and had varying perimeters.

Fabrication

The process flow for fabricating the test vehicle was as follows:

1) Grow field oxide, 5000A

2) Pattern and etch diffusion areas

3) Grow source/drain blocking oxide, ~ 350A (Removed for planar sources)

4) Doping process (ion implantation, Boron+, or BN)

5) Source/drain activation anneal

6) Pattern and etch contact vias

7) Sputter aluminum metallization

8) Pattern and etch metallization

9) 400° Sinter

1) The starting material used for both the patterned test vehicle and the unpatterned monitors were 10 cm <100> n-type 10-20 ohm-cm wafers. Care was taken that these should all be from the same manufacturer's lot to eliminate lot-to-lot variability as a concern. Field oxide growth was accomplished by a 1000°C wet oxidation for 100 minutes. Because of the relatively large number of wafers involved, several batches were required. This is in general true for all the processing steps. Thicknesses measured using a Nanospec thin film measurement system varied between 4503A and 5141A. Because of the rather large inter-wafer field oxide thickness variability, plans to randomize the wafers afterward were dropped. Instead every effort was made to see that wafers with similar thicknesses were processed together.

2) A positive resist process was used with exposure by the GCA-Mann 10X reduction stepper. The oxide was then etched using 5:1 buffered HF with endpoint determined from the dewetting of the backs of the wafers followed by a 20 second overetch. The resist for this and subsequent patterned etch steps was stripped with acetone followed by an O_2 ash in either a Technics or LAM etcher.

The test vehicle resistor patterns with their varied diffusion linewidths and oxide frames represented a worst- case situation for photolithography: there were both isolated 1.25 um

lines and isolated 1.25 um spaces. Wet etching of 0.5 um field oxide to define diffusion is not a high resolution process. For both these reasons, the 1.25 um W (oxide window frame) resistors were shorted and 1.25 um L (diffusion linewidth) resistors were really substantially larger with corresponding increases in other resistor L's.

3) The blocking oxide was grown in an 800°C wet oxidation for 60 minutes. The temperature was the same used in the Berkeley CMOS blocking oxide regrowth; the time was chosen to achieve the proper thickness. In normal cmos processing, this blocking oxide would be due to what remained of the gate oxide plus the additional oxide grown on the source/drain during gate poly-Si reoxidation. In the case of the planar doping source processes, it additionally provides protection for the n+ sources and drains from being counterdoped by the deposited boron-doped glass.

4) The planar dopant source doping processes, all done at 900°C, are described in the next section of this paper; they can be rather elaborate in themselves. The ion implantation was done on wafers after blocking oxide growth with no intermediate processing. The implant mask was the patterned field oxide. The implant conditions were a BF_2^+ dose of 2.0E15 ions/cm^2 at 50 KeV with the wafers tilted seven degrees.

5) The source/drain activation anneal was 950°C in an N_2 ambient for 30 minutes.

6) Vias in the blocking oxide were patterned and etched for two minutes in 10:1 buffered HF. At this point, the unpatterned monitors were blanket etched and tested for dewetting. Absence of dewetting of what were supposed to be silicon surfaces would have indicated that some of the super-saturated boron-silicon phase or "boron silicide" was still present on those wafers.

7) 8) 4000A aluminum was sputtered on the wafers, patterned and wet etched.

9) The metal sinter was done in a forming gas ambient at 400°C for 30 minutes.

Planar Dopant Source Processes

A. Boron+[®]

Because the planar dopant source processes were different from and more complicated than ion implantation, this section, which corresponds to step 4 of the process flow in the previous section, has been devoted to them. The Boron+ doping process was as follows:

1) Blocking Oxide Removal

Before the blocking oxide etch, the oxide thickness was measured to insure that it was similar on all wafers and to select the wafer with the thickest oxide for use as an etch monitor. Prior to the actual oxide etch, an H_2SO_4:H_2O_2 clean was done. The blocking oxide etch itself was in 25:1 HF with endpoint determined by the dewetting of the back of the etch monitor followed by a 30 second overetch. The wafers were dried in a Fluoroware spin dryer after achieving 14 Mohm-cm in a DI resistivity tank. This etch and the subsequent deposition furnace step were timed so that wafers went from the dryer directly into the furnace. The intent of all this was to insure that wafers with clean, dry, unoxidized silicon surfaces went into the furnaces. Note that this was a blanket etch; to simplify the overall process flow, no resist pattern was used. In the fabrication of actual cmos, the p+ source/drain implant mask would be used to protect field and n+ source/drain blocking oxides while the p+ source/drain blocking oxide was removed. The substitution of planar dopant sources for implantation would then require no change in photolithography and insignificant oxide loss prior to the removal of the borosilicate glass.

2) Borosilicate Glass Deposition

The Boron+ deposition program is detailed in Appendix 1.

The Boron+ sources were placed in the deposition furnace as received from the manufacturer with no intermediate clean. With virgin sources or after a furnace shutdown, a sixteen hour deposition was done to stabilize or "age" the sources. In evaluating the moisture-enhanced Boron+ process, several values of ambient moisture were examined. The moisture level was monotonically increased and a six hour deposition always preceded any test or run

depositions to ensure that the sources had achieved an equilibrium HBO_2 evolution rate at the new moisture level. This stabilization involved allowing the bulk to surface B_2O_3 gradient to reach a steady state.

Deposition times and temperatures were selected to give monitor sheet resistivities comparable to ion implantation. The deposition time was decreased as the moisture content was increased for the different depositions because the dopant transferred to the silicon is dependent on the moisture content. (See second page of Appendix 1.)

3) Borosilicate Glass Removal

After measurement of its thickness, the deposited borosilicate glass was carefully removed using 20:1 buffered HF. The removal was monitored with ellipsometric measurement of remaining film thickness. The intent was to etch no longer than was necessary to remove the glass so as to keep field oxide loss to a minimum.

4) Reoxidation

The Boron+ deposition process was complete after 20 minutes 800°C wet oxidation to regrow the blocking oxide in the diffusion areas and to consume any boron silicide left over from the previous steps.

B. Boron Nitride

The process for the BN sources was quite similar to that for Boron+ and was as follows:

1) Blocking oxide removal (Same as in Section A above)

2) Borosilicate glass deposition

The BN source glass deposition is described in Appendix 2. The deposition conditions were chosen to achieve deposited glass thicknesses comparable to those of the Boron+ processes.

The BN sources were also placed in the furnace as received from the manufacturer. These too underwent several dummy depositions prior to any test or run depositions

for the same reasons cited above. The same Tylan TYTAN II furnace was used for both deposition processes. This furnace possessed only profile and not spike thermocouples so that care had to be exercised in the thermal ramping and equilibration steps to insure good temperature control.

3) "Soak" anneal

The function of the additional "soak" anneal was to drive boron from the deposited glass into the silicon. This is necessary because the BN process deposition temperature necessary for reasonable glass thicknesses, 800°C is too low for significant boron diffusion into the silicon. Immediately following the glass deposition, the silicon wafers were taken to another furnace for a 40 minute 920°C N_2 ambient anneal. The temperature was chosen to give sheet resistivities comparable to Boron+ sources after removal of the doped glass.

4) Borosilicate glass removal (Same as in Section A above)

5) Reoxidation (Same as in Section A above)

After this processing the wafers were ready for the source/drain anneal, step 5 of the process flow in the previous section.

Measurements and Results

Test Wafer Positions

In the following reported results, frequent reference is made to the position of silicon wafers in the deposition boat. Figure 4 shows some of the loading positions in a deposition boat containing twenty-seven Boron+ sources. The position of a silicon wafer in the boat is specified by the number of the source it faces and also by whether the surface to be doped faces up- or down- stream of the gas flow. For the various run groups reported here, patterned silicon wafers were placed at positions 1u (upstream), 3d (downstream), 5u, 14d, 25u and 27d.

Positions 1u and 27d are not usually used in production processes because they are known to have higher sheet resistivities than the other positions and because their omission negligibly affects load size: they are two positions out of fifty. They are included here so that the worst-case boat uniformity may be examined.

Unpatterned monitors were placed in positions 10d and 20u with an additional wafer for film analysis at 14u. In the subsequent discussion and appendices the alphabetical suffix is dropped for simplicity.

Similarly for Boron Nitride process with only twenty sources, patterned wafers were placed at 1u, 3d, 5u, 10d, 18u and 20d with unpatterned monitors at 7d and 14u.

Measurement Techniques

Numbered sections below correspond to the Evaluation Criteria (page 4.).

1) 2) All film thickness measurements were done with an ellipsometer. Thickness and doped silicon measurements on patterned wafers were taken at a diffusion feature approximately 350 um by 2000 um.

3) Monitor sheet resistance was measured using a standard four point probe.

Patterned wafer four-terminal resistors were measured using an HP 4062B automatic parameter test system in combination with an Electroglass 2001X wafer prober.

Care was taken to adjust the measurement current for each device to maintain sensitivity and still keep the voltages involved small to avoid extraneous effects. Test software took advantage of this system's TIS software while data storage, retrieval and manipulation routines were custom software. Figure 5 shows the chips tested on each wafer.

While first trying to make the electrical measurements, it was discovered that many of the wafers irrespective of the doping process used, had open contacts due to a thin oxide left in the contact area prior to metallization. The problem was alleviated by prestressing of the contacts to blast through this oxide layer prior to any electrical testing.

One milliamp current was forced to flow through each contact to the substrate. This did not harm any of the devices.

4) Measurement of the linewidths of the resistors for sheet resistance calculation was done on a Vickers image shearing optical linewidth measurement system. It was impossible to process all the wafers at once, particularly for the photolithography, so four different starting material "runs" were made. Records were kept designating those runs from which wafers were taken for the various depositions or implants. Linewidth measurements were made on wafers from each of these runs. Due to the lithography and etch effects mentioned earlier, the openings in the field oxide were larger than corresponding mask features: 1.25 um mask dimensions typically yielded a 2.2 um diffusion linewidth (opening in the field oxide).

   For simplicity, in the appendices, graphs and discussions that follow, these devices are referred to by their mask dimensions. The measured dimensions of the actual devices are provided in Appendix 7 for every process batch.

5) Dopant concentration profiles by the spreading resistance technique were done by Solecon, Incorporated. Standard lapping and staining was applied to measure diffusion depths [9].

6) Defect density was examined by standard etching techniques. Both Sirtl etch and Wright etch were applied, the latter with ultrasonoration.

7) 8) Reverse bias diode leakage and device characterization measurements were made with an HP 4145 Semiconductor Parameter Analyzer and manual probe station with TECAP software. With a light-tight box and shielded cables and probes, very low current levels could be accurately measured.

Deposited Glass Thickness

The deposited borosilicate glass thickness data is presented in Appendix 3 and shown in Figures 6 and 7. Glass thickness and subsequent sheet resistivity are functions of the deposi-

tion time, the moisture content and deposition temperature.

As mentioned earlier, deposition times were decreased with increasing moisture content (at a constant 900°C temperature) in order to obtain constant resistivities. Accordingly, glass thickness remained fairly constant over the studied range. It is not clear why the patterned wafers (top line) had thicker glass than that of the unpatterned monitors. It may be due to the boron being the growth rate limiting factor in the formation of BSG on the blank wafers where silicon is abundantly available, while on the patterned wafers, with small open silicon areas, the opposite is true.

There is no difference at higher moisture concentrations. However, the total glass thickness is less on the patterned wafers. This is proably due to the shorter deposition times of these runs (under 30 minutes glass formation decreases rapidly).

Boron nitride depositions (Figure 7) simply indicate an increase in glass thickness due to increased moisture. Deposition/sourcing times were the same for both runs.

After the removal of the borosilicate glass, ellipsometric measurements of the doped silicon surfaces were done. These are summarized in Appendix 4 and Figures 8 through 13. It has been shown that the deviation of the two ellipsometry parameters psi and delta of doped silicon from those of undoped silicon is an indication of the presence and thickness of a boron silicide layer [10].

The thickness of the boron silicide can be calculated if the index of refraction is taken to be 1.60. The results of these calculations are given in Appendix 4 and shown in Figures 12 and 13. It can be seen from Figure 12 that as the moisture content is increased, the thickness gradually increases but remains below 25 A.

Comparison of Figures 12 and 13 show that the Boron Nitride process yields a thicker boron silicide layer (60-70 A) even though the sheet resistance is much higher on the monitors. This thick layer is a concern because it retards the doping of the underlying silicon necessitating higher temperature drive-in anneals. It has to be removed at some point during the processing so that good contact may be made to the silicon and because it may lead to

higher silicon surface defect densities [11].

Field Oxide Loss

Data for the field oxide loss during removal of the the borosilicate glass is summarized in Appendix 5. It was quickly discovered that for the Boron+ processed wafers, the deposited glass on the patterned wafers etched more rapidly than that on the unpatterned monitors. After this was understood, the oxide loss was kept under 400 A and frequently under 250 A. The later number should be acceptable for the cmos process.

It should be kept in mind also that the 20:1 buffered HF used for this etch is far from the optimum etchant for doped glass-to- thermal oxide selectivity. p-etch is better etch if reduced field and n+ blocking oxide loss is required [6].

The Boron Nitride deposited borosilicate glass etched much slower and significant field loss was recorded. The difference in deposited glass etch rate between this process and the Boron+ processes is probably due to the use of BHF to etch the glass and to differences in the boron contents of the glasses. Such an interaction has been previously reported [12]. Some etchants, in particular BHF, exhibit a non-monotonic rate dependence on the boron doping content of the glass; the etch rate actually decreases significantly down to some minimum value as the boron content increases. Something similar appears to have happened with the 250 ppm Boron+ deposited glass.

Resistivity and Pattern Effect

Sheet resistivity data is summarized in Appendices 6, 7 and 8 and Figures 14 and 15. The ion implanted wafers (see page 18 of Appendices) show no pattern effect. Data from the BN is rather scattered but show no pattern effect (page 17 and Figure 15). No comparison was made with the dry BN process.

For the Boron+ processes, Figure 14 would have one believe that the introduction of moisture leads to only a modest reduction in the pattern effect (higher R_s on smaller features) unless the moisture content is increased to 120 or 250 ppm.

This figure, however, is based on summaries over entire six wafer batches, and may be misleading. It is not necessary to use the relatively higher moisture contents to obtain most of the pattern effect reductions. Figure 16 shows the Boron+ dry process boat profile. This particular one was chosen because it was done with the same Boron+ sources as the latter moisture-enhanced depositions. Figure 17 shows that the 30 ppm wet process considerably improved uniformity and reduced the pattern effect. Figures 18 and 19 show the same thing happening for the boat position in Figure 16 which had the greatest resistivity variation (14D).

Why does the addition of moisture make such a difference? There is a marked reduction in the pattern effect with the introduction of moisture for the same reason that the boron nitride H_2-injection process has minimal pattern effect: the flux of boron dopant specie is so great that local depletion of the boron adsorbed on the silicon is much reduced or eliminated. It is true that for reasonable quantities of moisture the Boron+ monitor and patterned wafer sheet resistivities still differ but this is not a serious problem. Elimination of the large variation on patterned wafers and the constant difference between patterned wafers and unpatterned monitors which can be characterized makes moisture-enhanced Boron+ a viable process for small geometry technologies.

Diodes

The diode data is presented in Appendix 9. For the most part the leakage currents are somewhat high considering the small diode areas. No trends seem apparent. Sampling of some of the wafers indicates that the single die measurements are indeed representative of the whole wafers; it is real data and not noise.

Other Measurements

Spreading resistance doping concentration profiles are shown in Figures 20-23. These are from unpatterned monitor wafers after they had undergone complete processing.

The profiles look quite normal. The amount of boron going into the silicon is determined by the solid solubility of boron in silicon at that temperature and by the amount of available source at the surface. The dry process surface concentration indicated some depletion (~ 4.5 x $10^{18}/cm^3$) at the surface; the 15 ppm shows a higher number (~ 0.5 x $10^{19}/cm^3$) while the 60 ppm process resulted in the highest surface concentration (~ 1.5 x $10^{19}/cm^3$). The junction depth, however, is determined by the diffusion time and diffusion coefficient at the given temperature. Thus, it is deepest for the dry process, which was a 70 minute run and most shallow for the 60 ppm run which took only 25 minutes.

Junction depths were also determined by the usual lapping and staining method; results are tabulated in Appendix 10. The goal was to obtain 0.45 - 0.5 um deep junctions, which we did, within measurement error. This technique can be accurate to about +/- 0.02 um but it is very operator dependent. No trend can be observed here.

Defect density counts are tabulated in Appendix 11. The Wright etch is a more sensitive etch for all crystal orientations. Most runs indicate defects due to doping which is a normal occurrence. No trend is apparent.

Recommendations for the Cmos Process

The addition of small quantities of moisture to the Boron+ process markedly reduces the pattern effect. The internal source diffusion rate imposes a ceiling on the amount of moisture that can be added. The internal diffusion rate and hence this ceiling are of course temperature dependent: at higher temperatures the ceiling will be greater. Lacking data on whether the higher moisture concentrations are operable over the long-term, it would seem appropriate to operate in the center of the known margin space. At 900°, it is known that the process saturates at 120 ppm. The recommended operating range is therefore 15 to 60 ppm. To achieve the proper sheet resistance on patterned wafers it will be necessary to increase the deposition time. If this is not sufficient then a small increase in the deposition temperature can be made. P-etch should be used to reduce the field and n+ blocking oxide loss and eliminate the anomolous doped glass etch rate behavior exhibited by BHF.

Some effort should be made to determine whether the higher moisture contents where saturation of the doped glass deposition occurred are usable operating points over the long term. If so, the additional reduction in the pattern effect that was observed at these operating points makes them highly desirable.

CMOS Process

Several wafers were processed through the standard cmos process, both p-well and n-well, with the modification of introducing Boron+ diffusion of p+ sources and drains, instead of ion implantations. Currently this process is designed to produce 0.45 - 0.50 micrometer deep source/drain junctions but we are looking for shallower/smaller devices for future work. Thus, the Boron+ planar dopant process was investigated as a possible substitute for ion implantation to avoid channeling. The most important concern was to introduce minimal changes in the overall process. This has been successfully accomplished, though not without some problems.

The main problem turned out to be the protection of nmos devices during Boron+ source/drain diffusion. The normal process' blocking oxide, ~ 400 A, was not sufficient coverage. No n-channel devices survived the 30 minute dry Boron+ process at 950°. Increasing the blocking oxide to ~ 700 A helped somewhat (same Boron+ dry process) but contact resistance was still present on all nmos devices, not on pmos. (Figures 24 and 25 a, b, c.) This lot had an n-well cmos process.

At this point it looked like oxide protection was not going to be enough for the moisture enhanced Boron+ process where even more boron glass is grown. Thus, a thin nitride layer (~ 100 A) was deposited on the wafers just before p+ source/drain definition. The nitride was plasma etched before buffered HF etch of SiO_2 to open p+ source/drain areas for diffusion.

Boron+ deposition was done with 60 ppm moisture in N_2 at 900°C for 30 minutes. (R_s was 90 ohms/square on an n-type control). The boron glass was removed in p-etch (3 parts

concentrated HF, 2 parts concentrated HNO_3, 60 parts deionized H_2O); then, the protective oxide was regrown over the p+ source/drain areas and the nitride layer removed with standard wet etch (hot phosphoric acid). The wafers were completed as per the Berkeley CMOS Process.

Both n- and p-channel 2 micrometer devices were successfully fabricated a p-well cmos process (p-wells were ion implanted). Device characteristics are shown in Figures 26 and 27. They are quite acceptable and similar to those of all implanted wafers. To determine limits of the Boron+ diffusion process, i.e., just how shallow devices can be built with it, the whole cmos process has to be scaled down. As it is, it works well for the 2 micrometer process.

Summary

The moisture enhanced Boron+ process was characterized with the intent of obtaining a usable process for cmos applications. In the first part of the project it was determined that BSG formation is thinner on blank control wafers than on patterned wafers for the same deposition conditions. However, the deposited glass etches faster on the patterned wafers than on blank monitors. This is an important factor to consider if the process is to be used in cmos device/circuit fabrication. For the targeted 900°C deposition cycle the total oxide loss was ~ 400 A, which, as it turned out, was not acceptable for use in the standard Berkeley CMOS Process. This problem was alleviated as discussed below.

The boron silicide layer, which commonly forms on the surface, was determined to be around 25 A. This layer has to be removed at some point in the process to allow good contact to the silicon. Thus, thinner layers are more desirable. 25 A is a thin enough layer to be dissolved during reoxidation of the source/drain areas.

The addition of moisture to the N_2 ambient resulted in an increase of boron flux, greatly reducing the pattern effect. The optimal amount is between 15-120 ppm. Suggested deposition conditions for cmos p+ source/drain diffusion are: 900°C, 30 minutes in N_2 + 30 ppm H_2O.

Limited comparison of the two types of sources. Boron+ and BN in a moisture-enhanced process. did not show much difference. The only point to be mentioned here is that the amount of silicide formation was greater on the wafers processed with the BN sources. Defect decoration was inconclusive. Spreading resistance measurements indicated similar profiles for both types of sources.

Boron+ diffusion was successfully incorporated into the Berkeley CMOS Process. Two micron gate length devices were fabricated and tested. To protect the n-channel devices. a thin nitride layer was deposited before p+ source/drain diffusion. No additional masking step was required. Boron+ diffused devices were indistinguishable from those processed with ion implantation.

Acknowledgments

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The authors would like to thank the staff of the Microfabrication Laboratory of the University of California. Berkeley. for their generous and enthusiastic help during the course of this project.

References

[1] T. M. Liu and W. G. Oldham "Channeling Effect of Low Energy Boron Implant in <100> Silicon." IEEE Electron Device Lett., vol. EDL-4. pp. 59-62. 1983.

[2] D. Rupprecht and J. Stach. "Oxidized Boron Nitride as an In-Situ Boron Dopant for Silicon Diffusions". Journal of the Electrochemical Society. vol. 120. no. 9. Sept. 1973.

[3] N. Goldsmith. J. Olmstead and J. Scott. Jr. "Boron Nitride as a Diffusion Source for Silicon". RCA Review. vol. 28. no. 6. June 1967.

[4] D. Rupprecht and J. Stach. "'Sourcing' Rate Control of Oxidized Boron Nitride". 147th Meeting of the Electrochemical Society at Toronto. May 11-16. 1975.

[5] J. J. Steslow. J. E. Rapp. and P. L. White. "Advances in Solid Planar Dopant Sources for Silicon". Solid State Technology. vol. 18. no. 1. January 1975.

[6] J. E. Rapp. Private communication.

[7] W. G. Oldham. et. al. "Berkeley CMOS Process: A User Guide". Memorandum No. UCB/ERL M84/84.

[8] S. A. Abbasi. "The Effects of Masking Oxide on the Diffusion of Boron into Silicon". Doctoral thesis, University of Southhampton, March 1980.

[9] C. P. Wu, et. al. "Techniques for Lapping and Staining Ion-Implanted Layers". Journal of the Electrochemical Society, vol. 126, no. 11, November 1979.

[10] K. M. Busen, W. A. Fitzgibbons, and W. K. Tsang. "Ellipsometer Investigations of Boron-Rich Layers on Silicon". Journal of the Electrochemical Society, vol. 115, no. 3, March 1968.

[11] S. F. Bevacqua and M. F. Chang. "The Induced Surface Defects Versus Carrier Lifetime as a Function of Boron Planar Diffusion Sources". Presented at the Electrochemical Society Meeting held in Boston, Mass., May 6-11, 1979.

[12] L. R. Plauger. "Etching Studies of Diffusion Source Boron Glass". Journal of the Electrochemical Society, vol. 120, no. 10, October 1973.

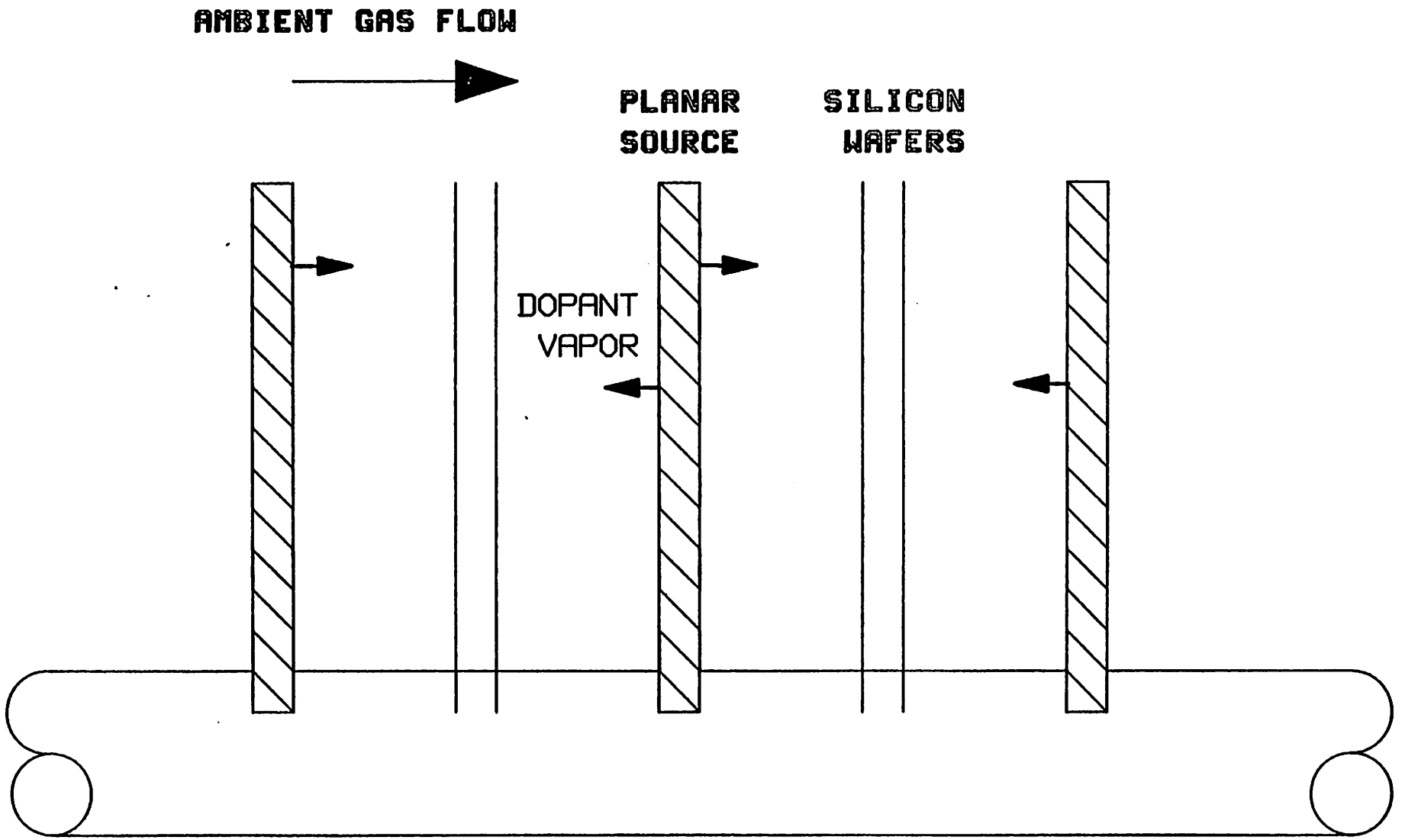


FIGURE 1: PLANAR DOPANT SOURCE PROCESS SCHEMATIC

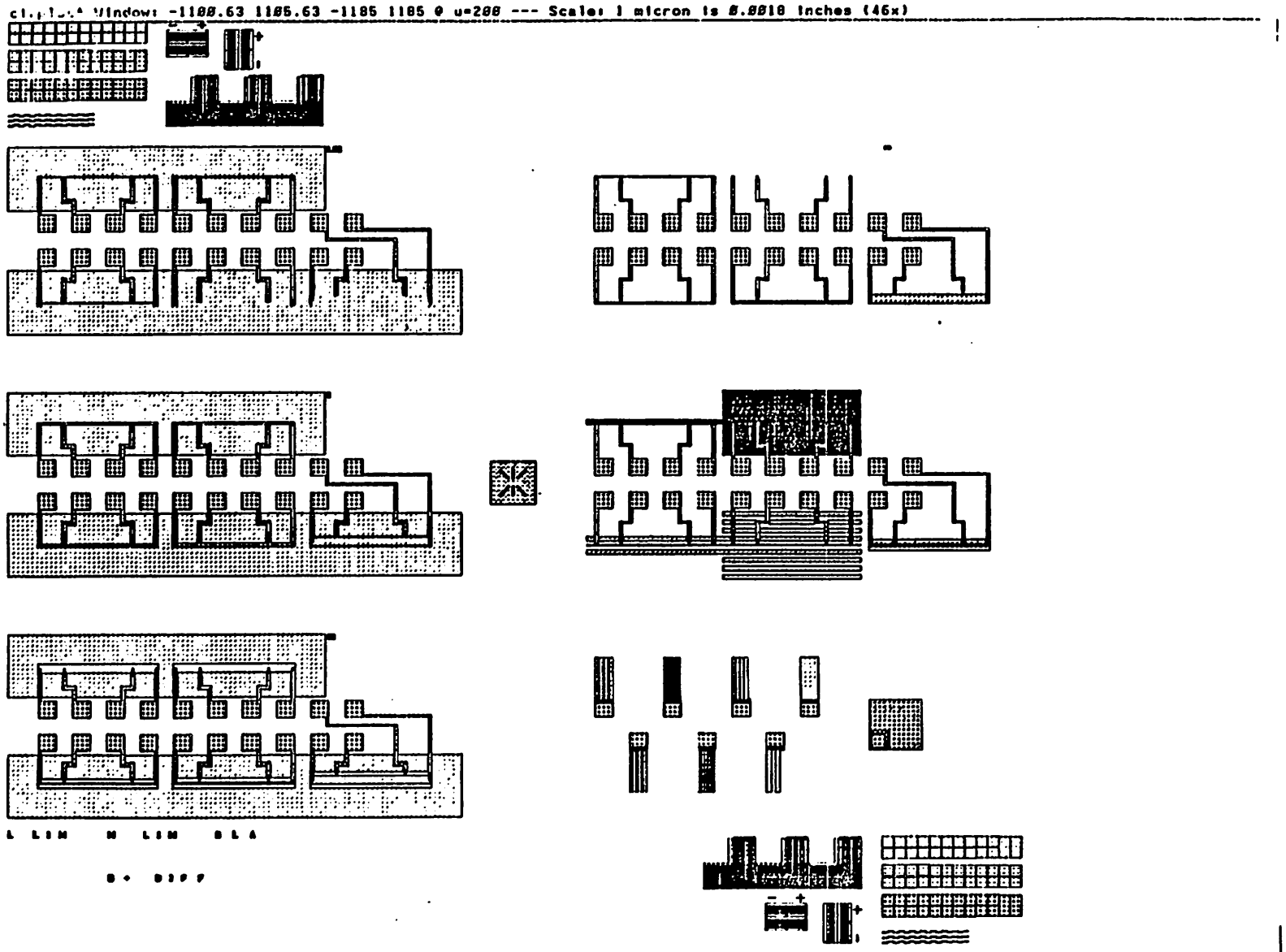
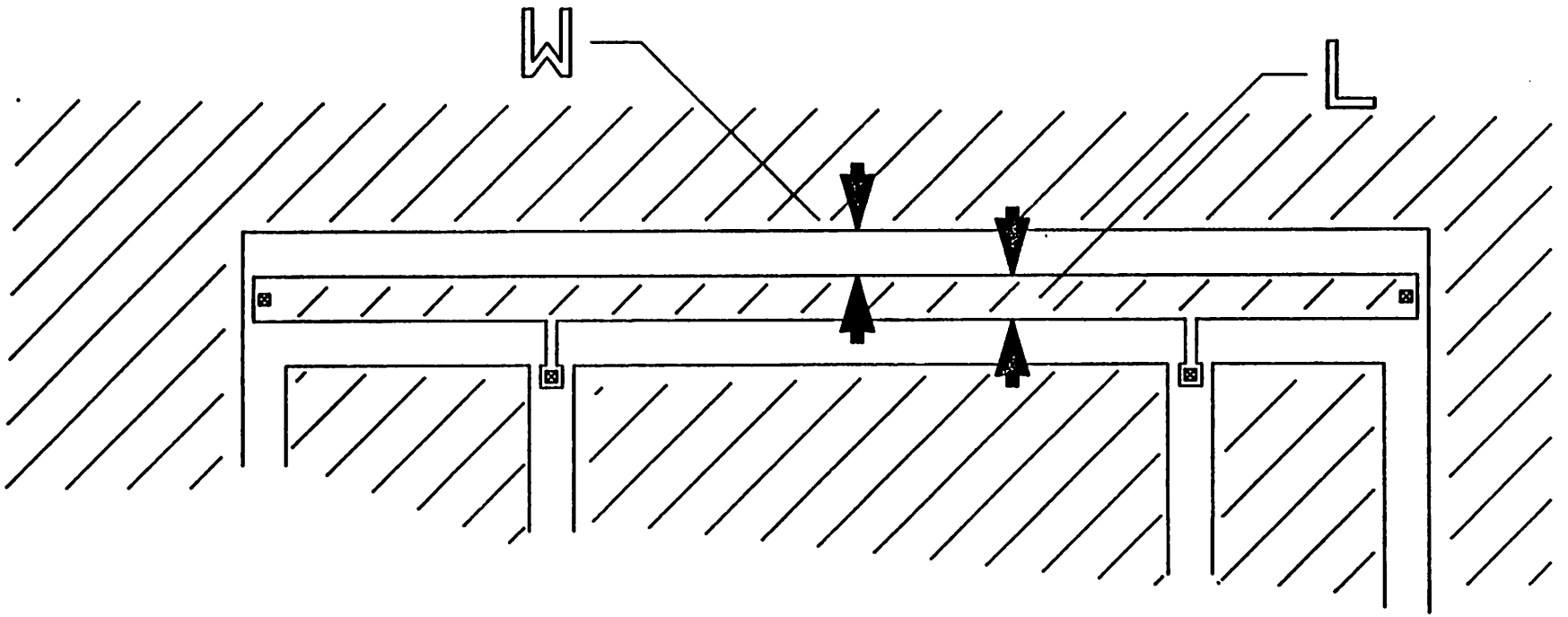


FIGURE 2: DOPING PROCESS TEST CHIP LAYOUT



CROSS HATCHED AREAS ARE P+ DIFFUSION

"W" IS THE WIDTH OF THE SURROUNDING

FIELD OXIDE FRAME WIDTH. "L" IS

THE DIFFUSION LINEWIDTH.

FIGURE 3: TEST VEHICLE FOUR TERMINAL RESISTOR

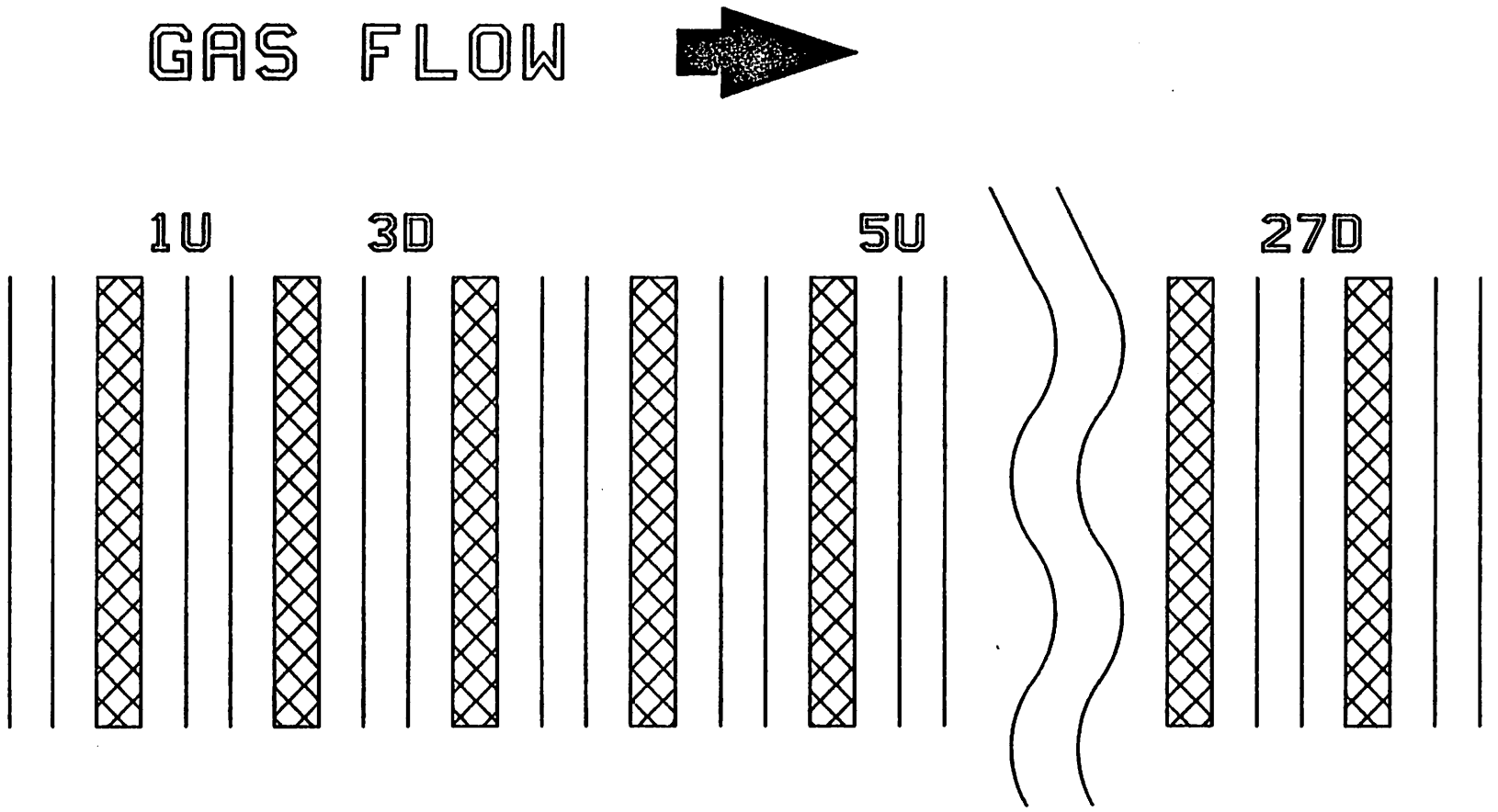
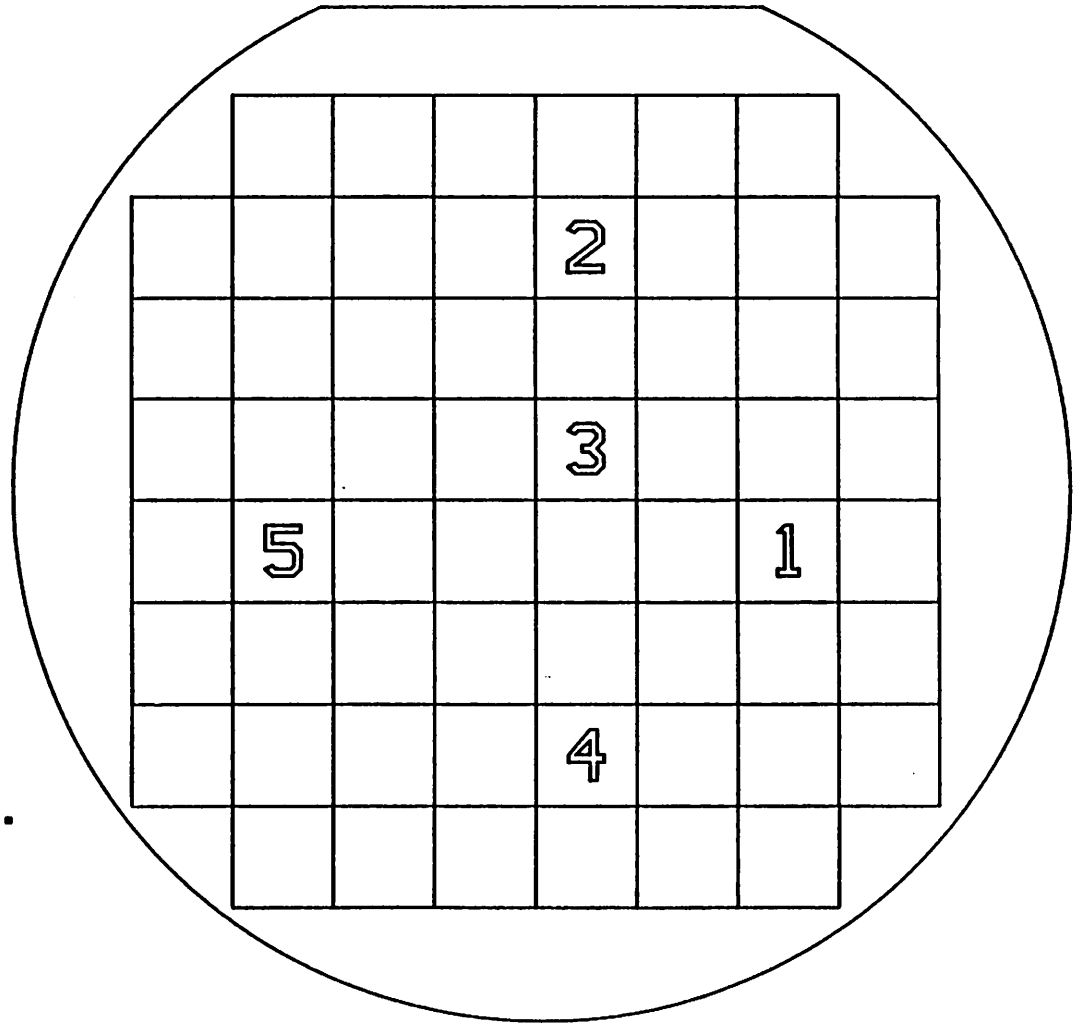


FIGURE 4: BORON+ LOADING DIAGRAM

FIGURE 5: WAFER TEST MAP



RESISTORS WERE
TESTED AT POINTS 1-5
WHILE DIODES WERE
TESTED AT POINT 3 ONLY.

FIGURE 6
BORON+ DEPOSITED GLASS THICKNESS VS. MOISTURE

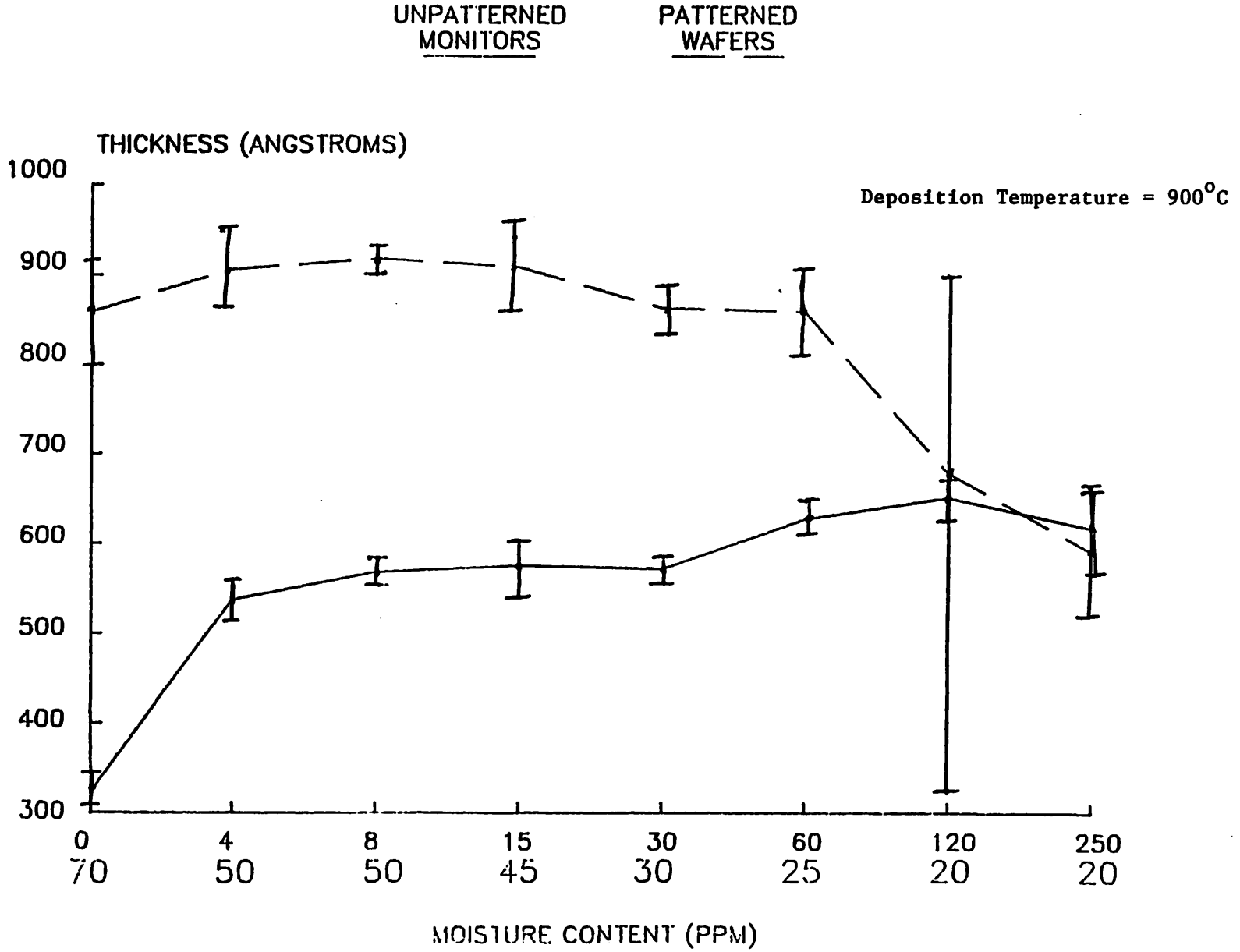


FIGURE 7
BORON NITRIDE GLASS THICKNESS VS. MOISTURE

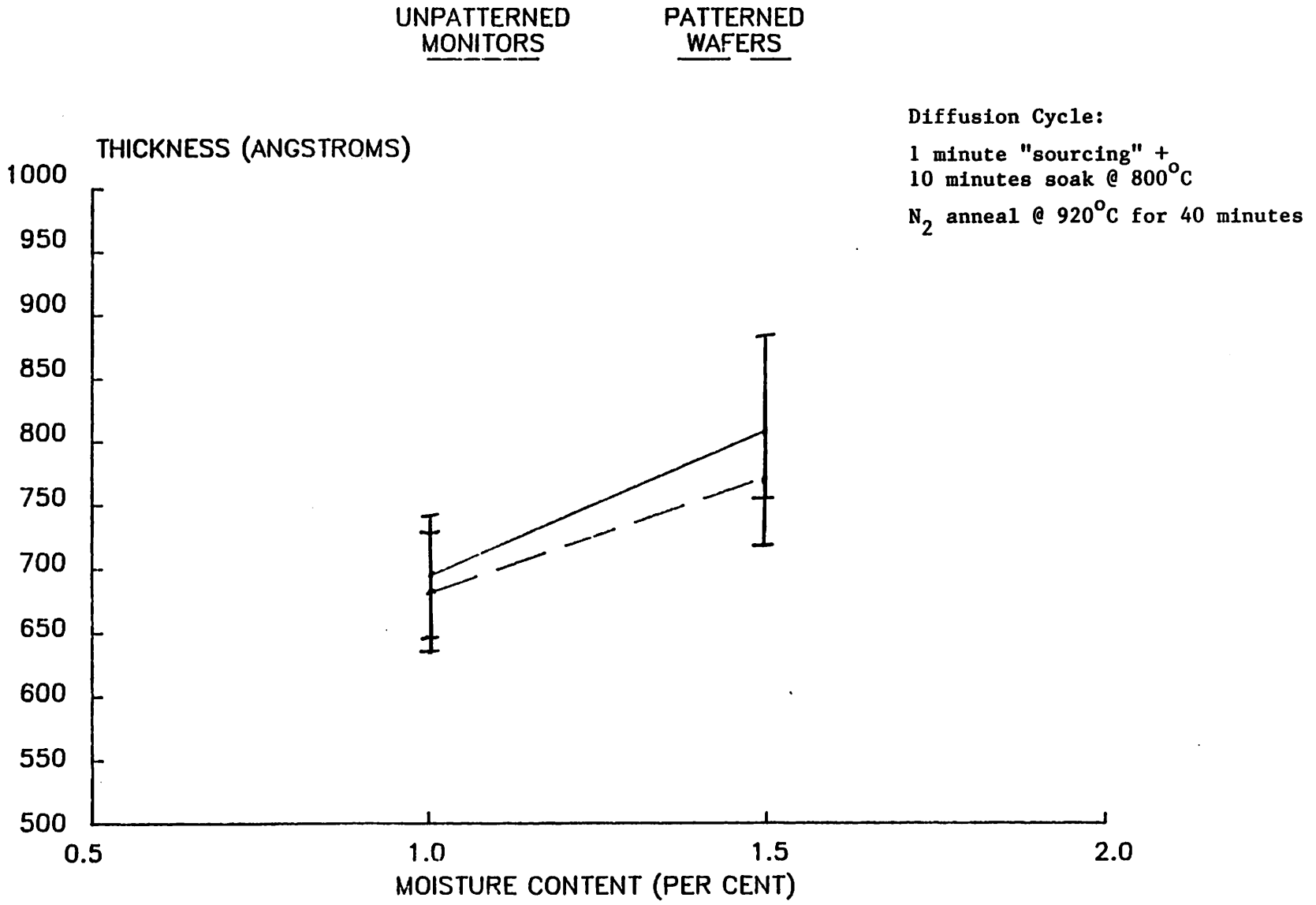


FIGURE 8
BORON+ ELLIPSOMETER PSI VERSUS MOISTURE

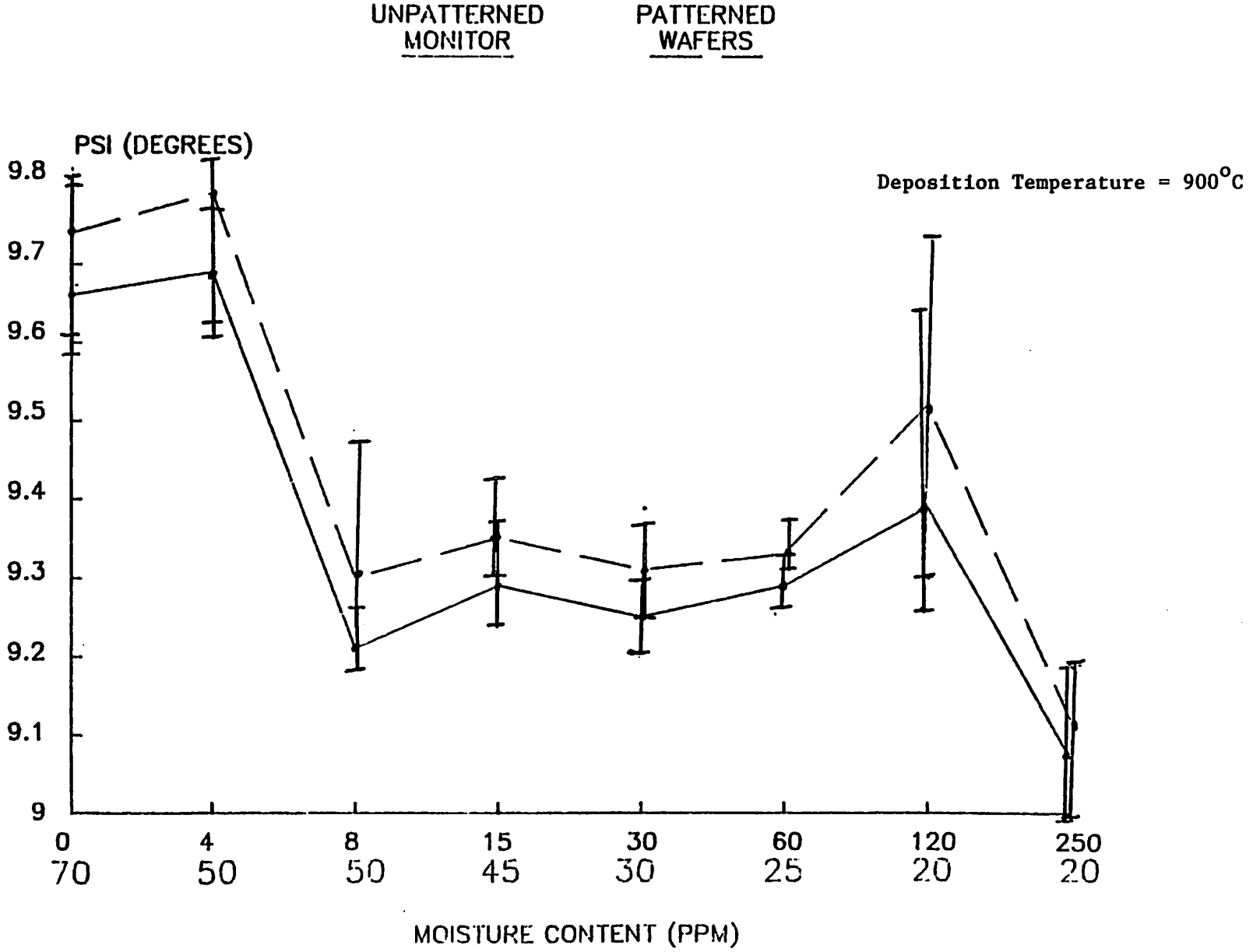


FIGURE 9
BORON+ ELLIPSOMETER DELTA VERSUS MOISTURE

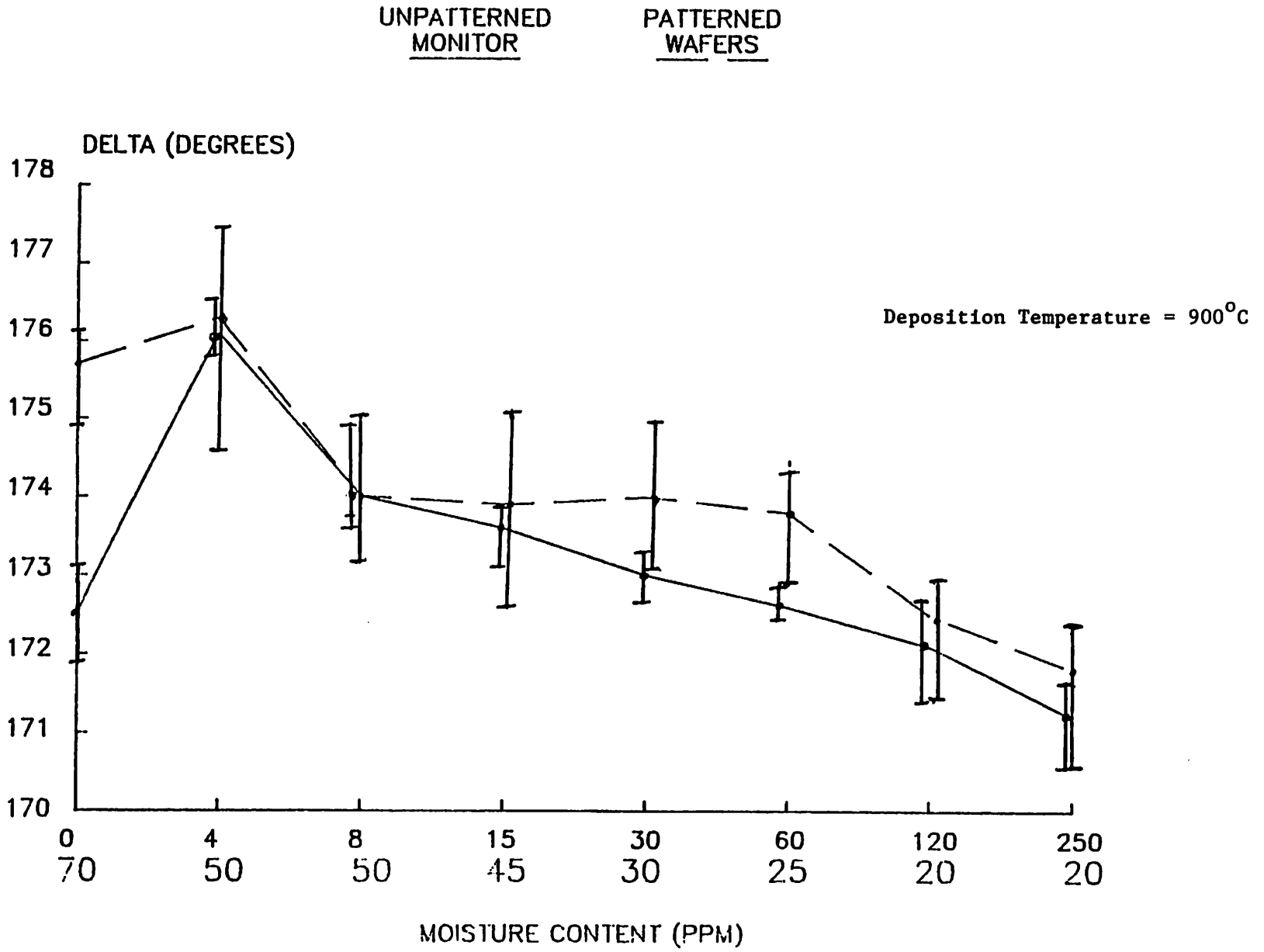


FIGURE 10
BORON NITRIDE ELLIPSOMETER PSI VS. MOISTURE

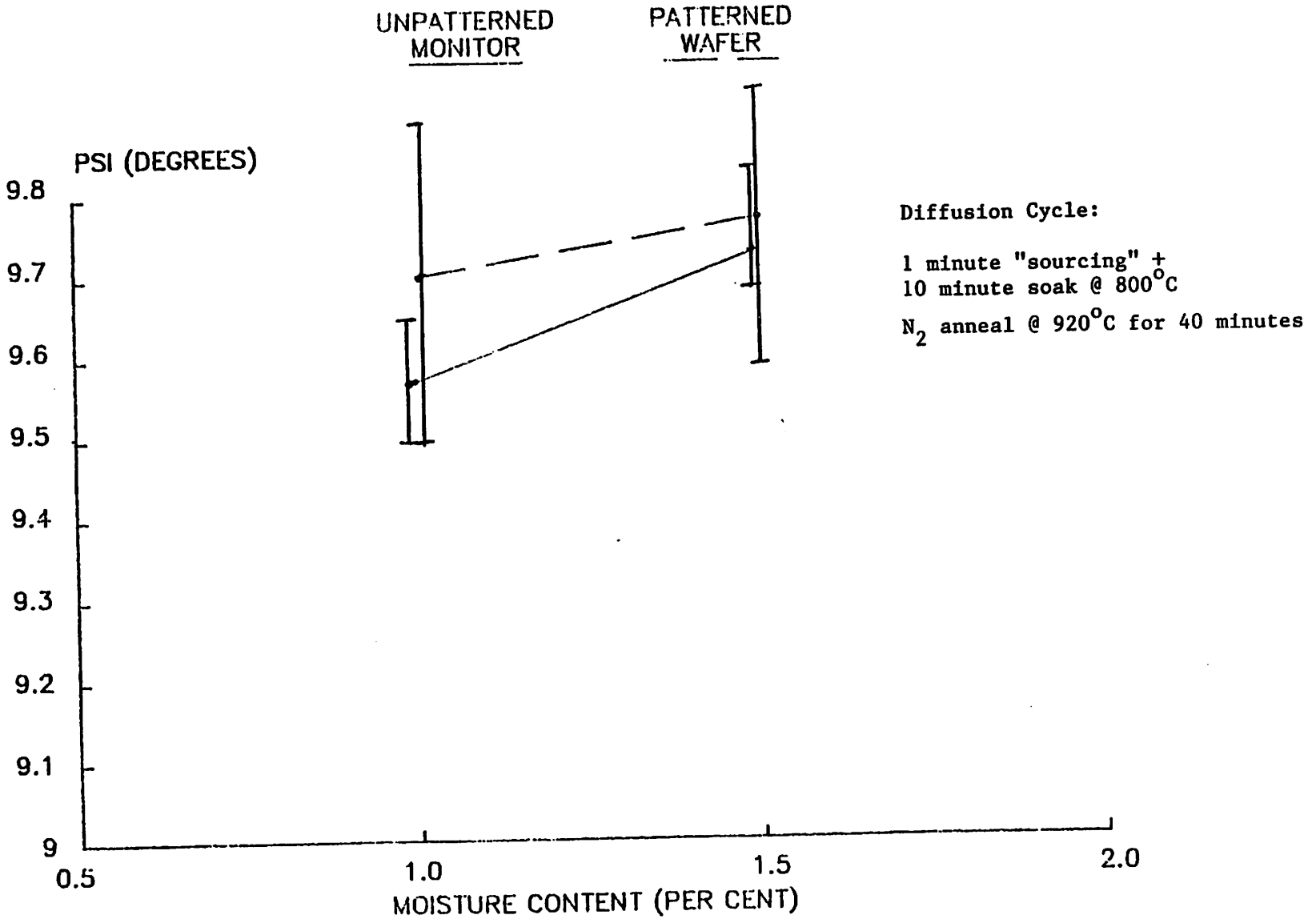


FIGURE 11
BORON NITRIDE ELLIPSOMETER DELTA VS. MOISTURE

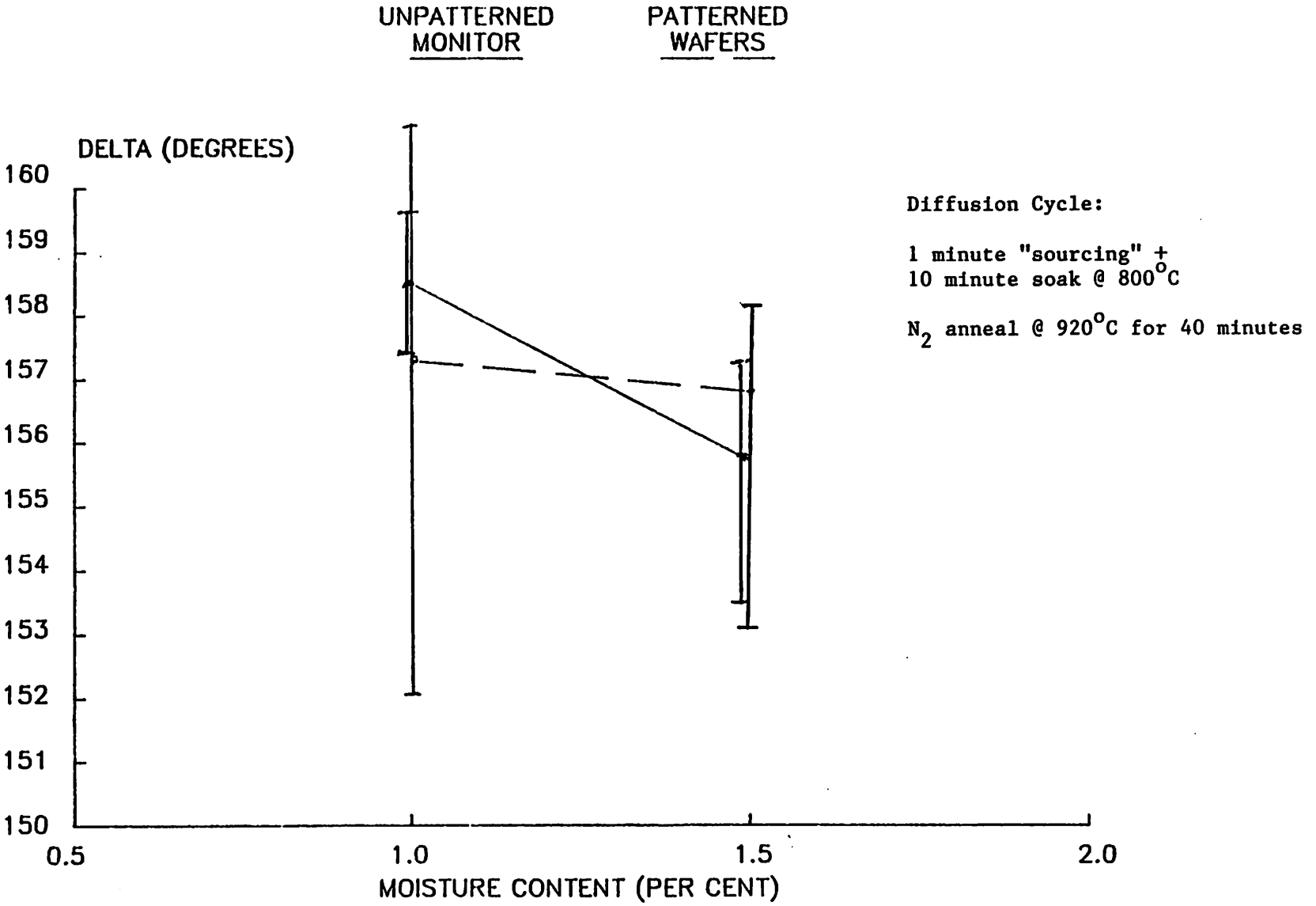


FIGURE 12

BORON+ BORON SILICIDE THICKNESS VS. MOISTURE

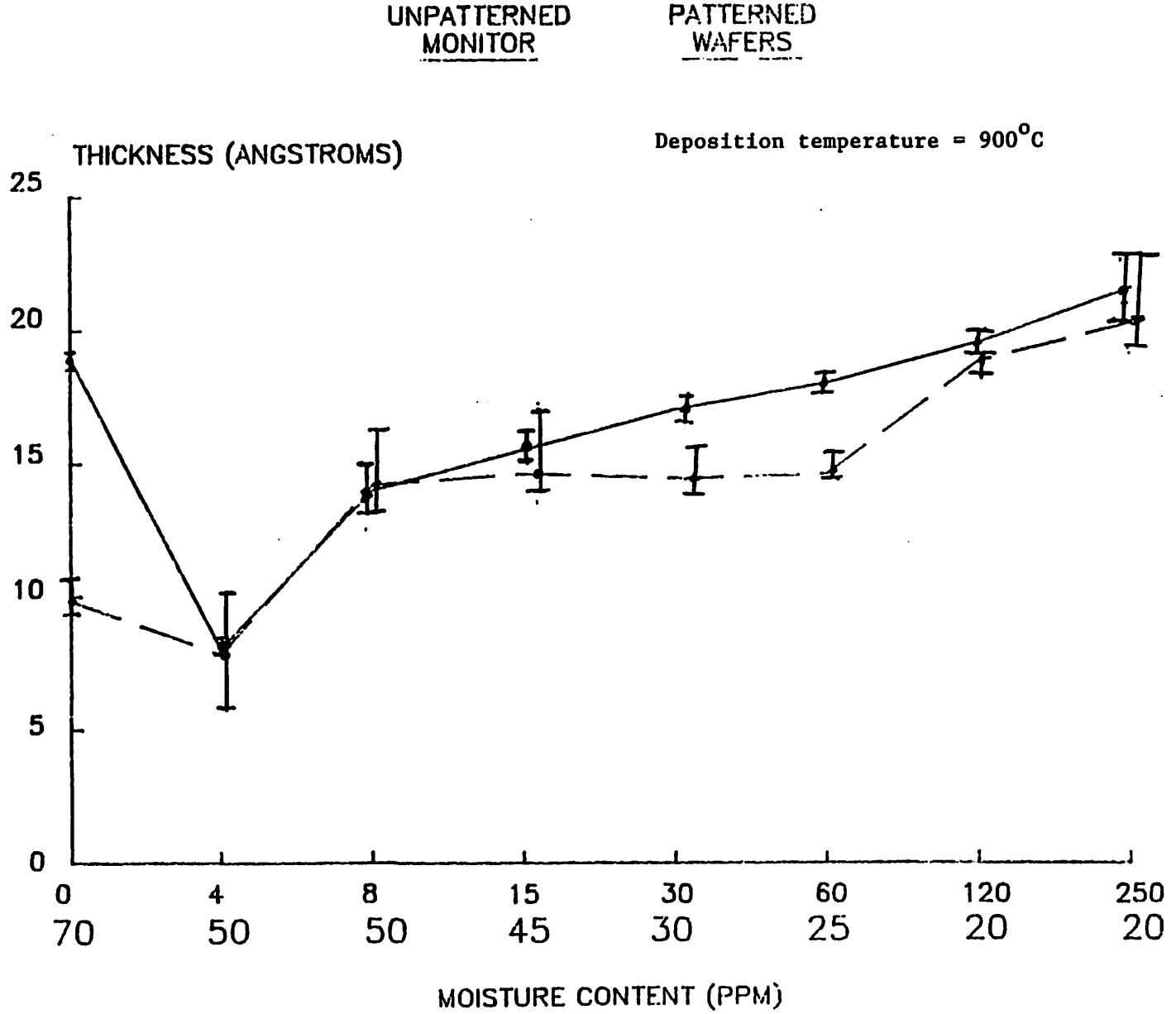


FIGURE 13

BN BORON SILICIDE THICKNESS VS. MOISTURE

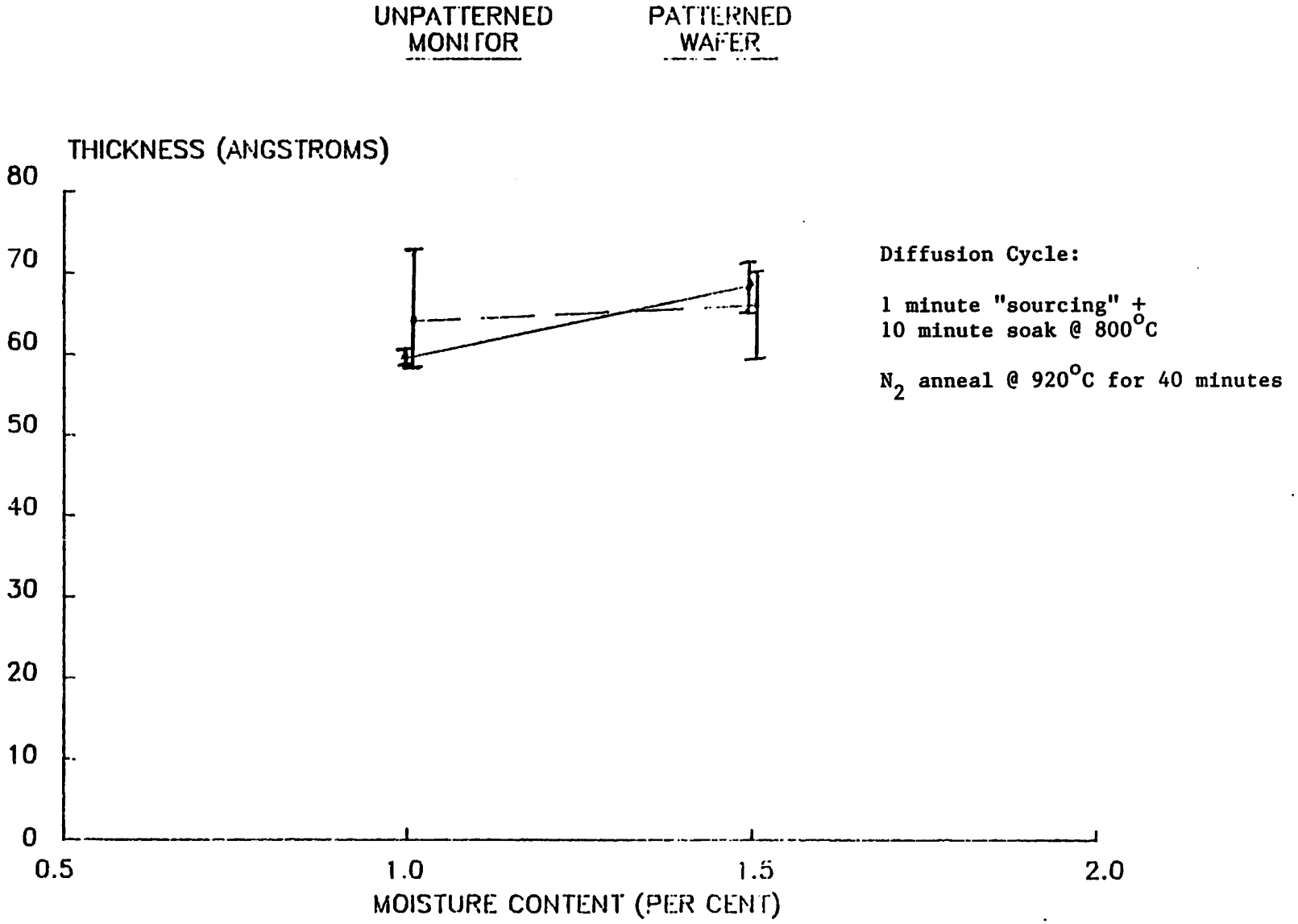


FIGURE 14
BORON+ RS VERSUS MOISTURE CONTENT

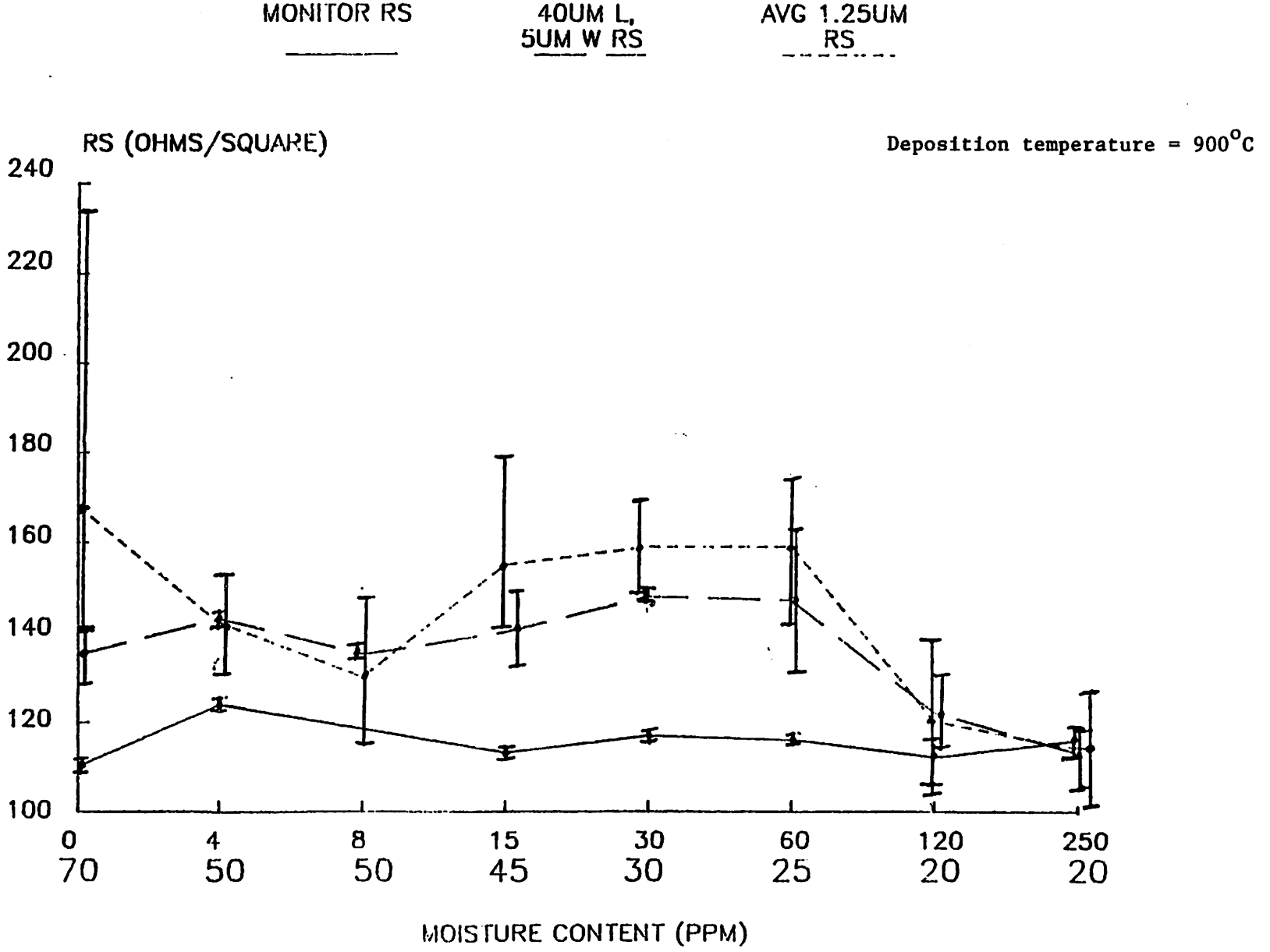


FIGURE 15
BORON NITRIDE RS VERSUS MOISTURE CONTENT

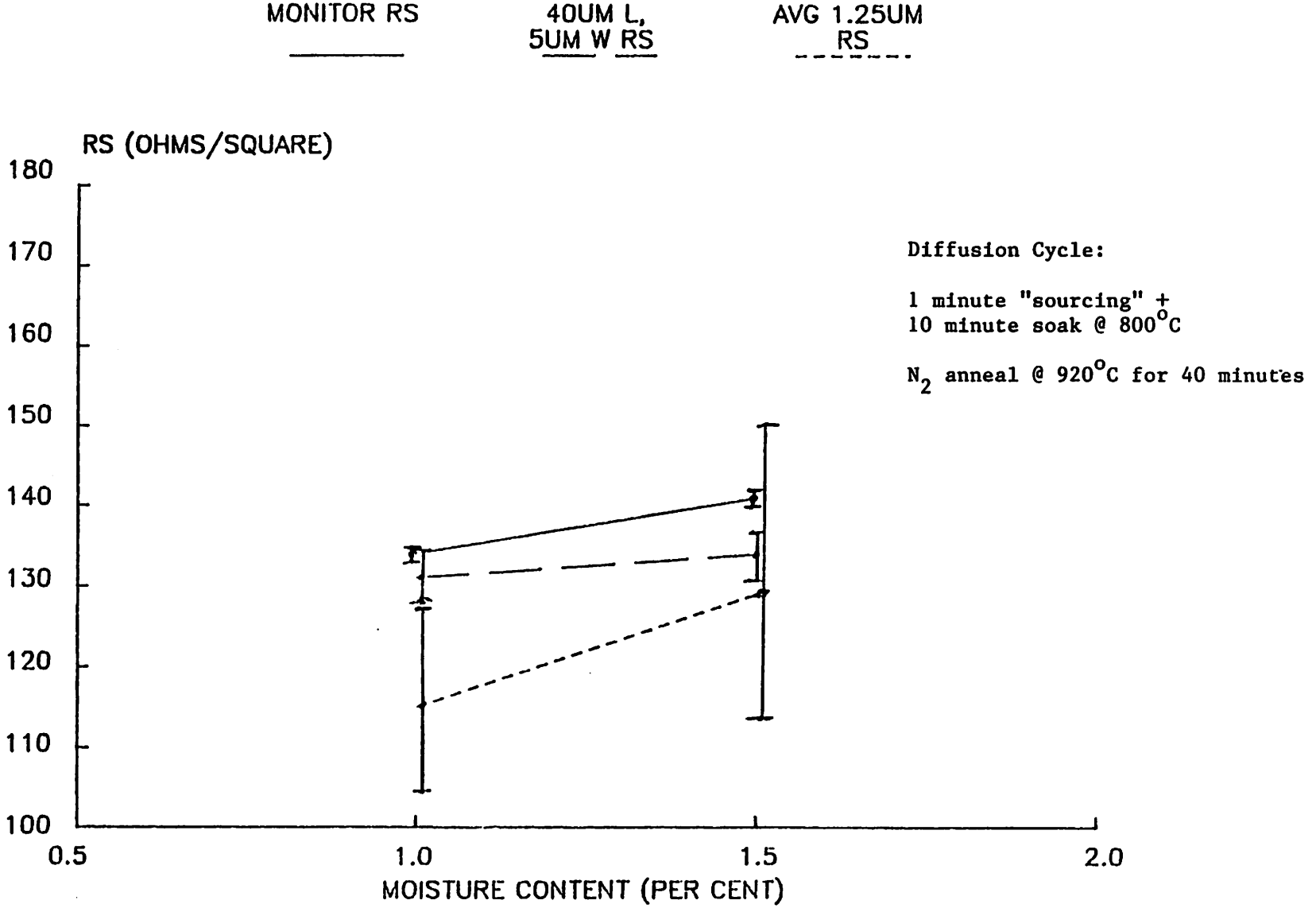
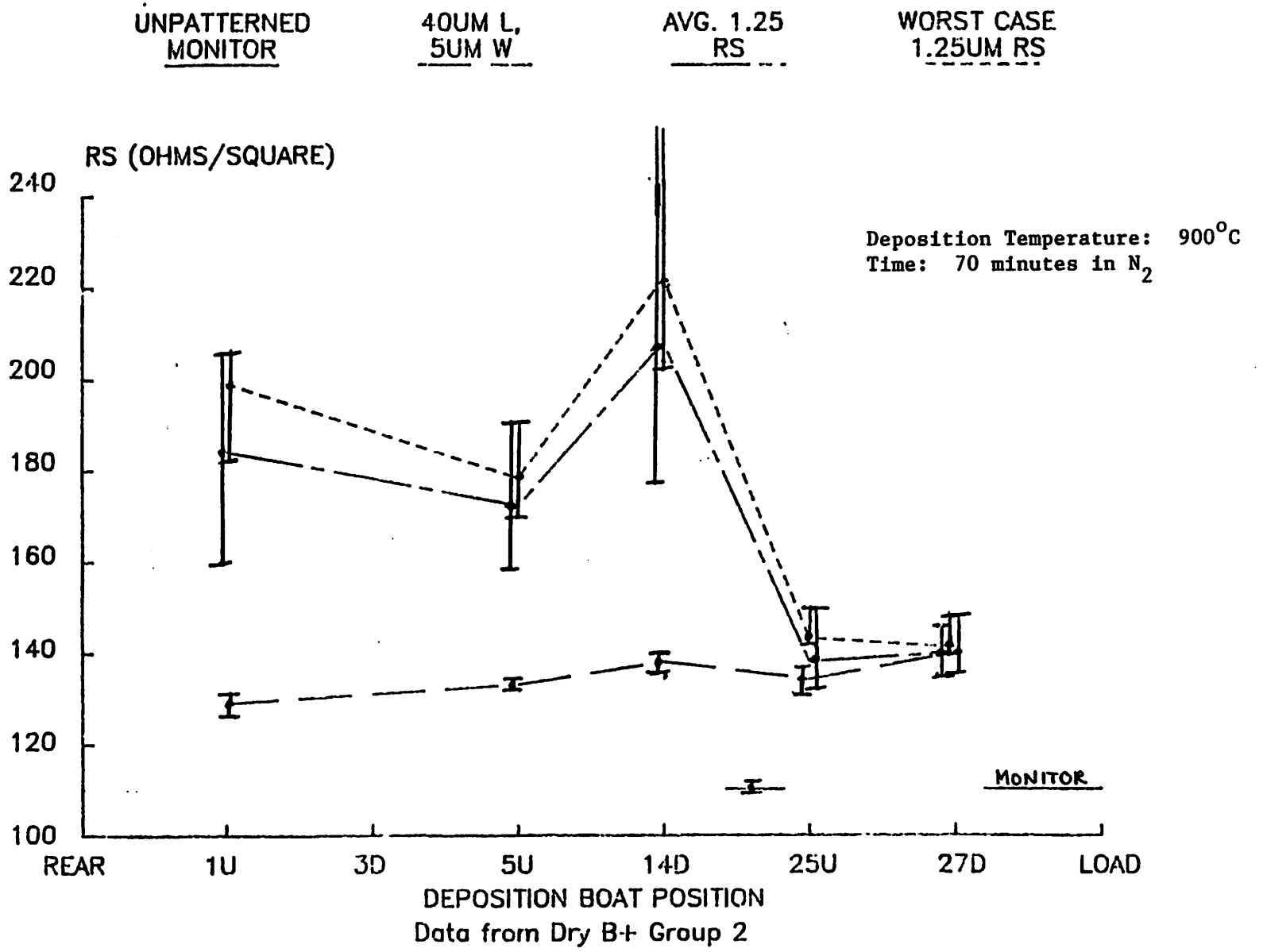


FIGURE 16
BORON+ DRY PROCESS RS VS. BOAT POSITION



Data from Dry B+ Group 2

FIGURE 17
BORON+ 30 PPM RS VS. BOAT POSITION

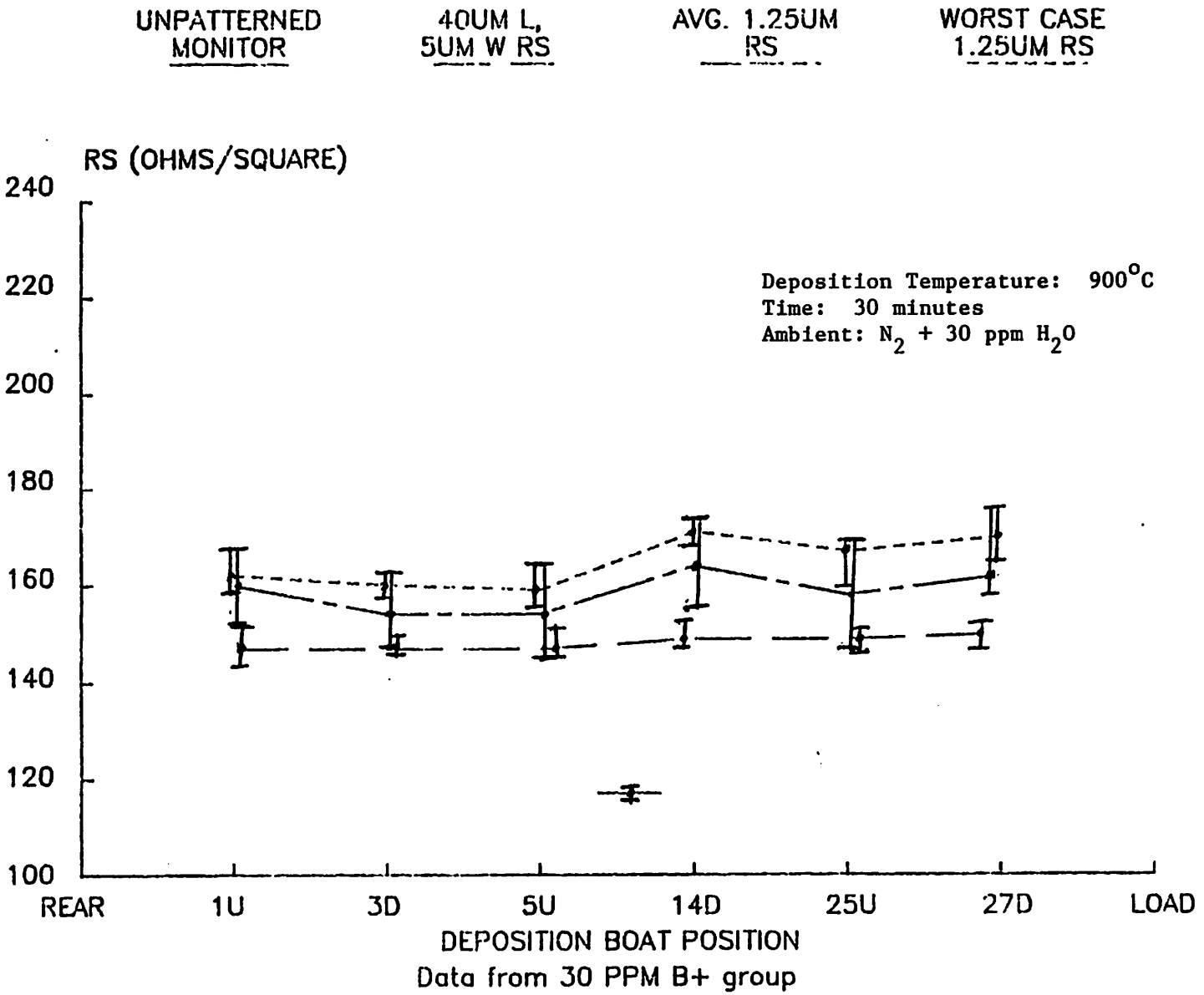
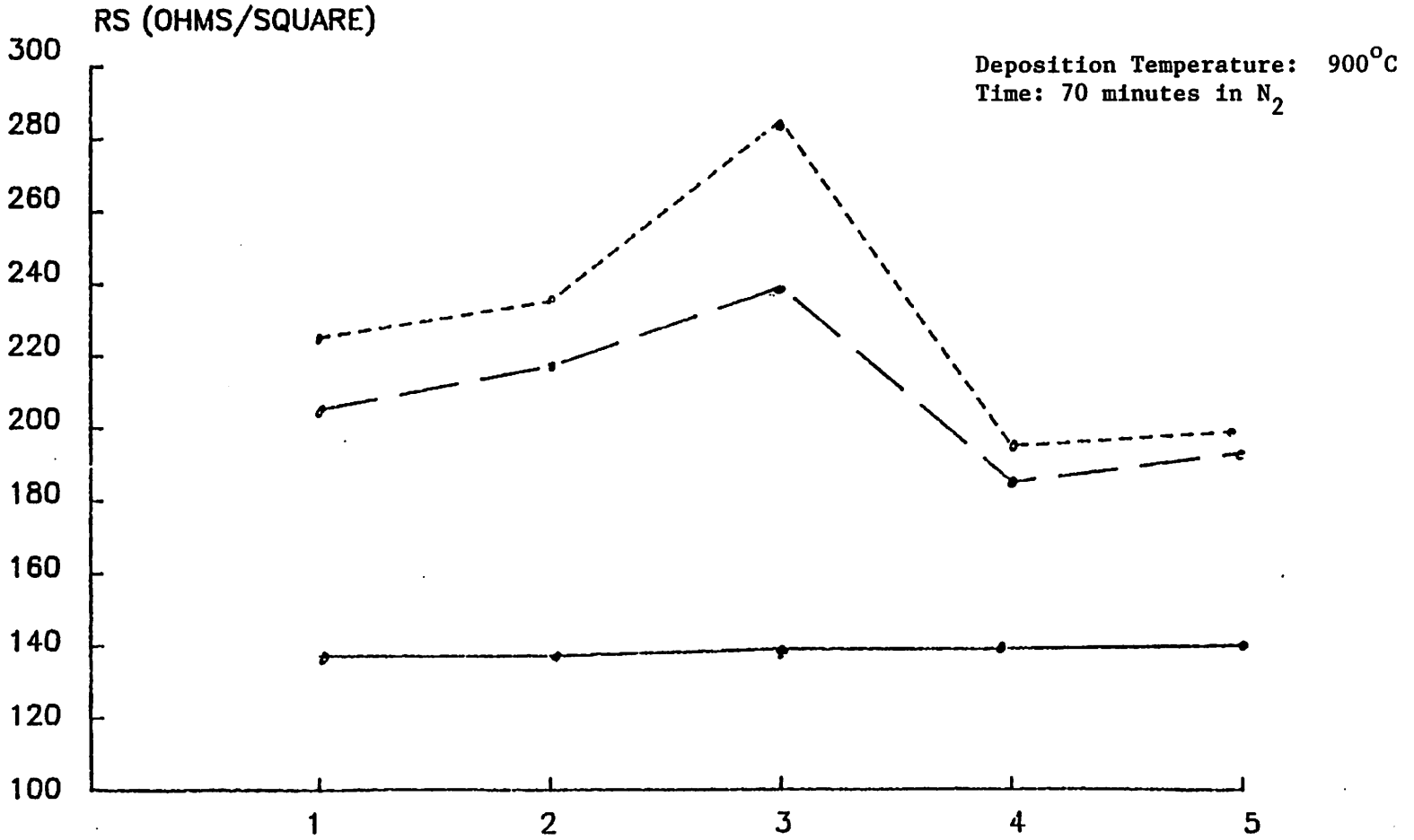


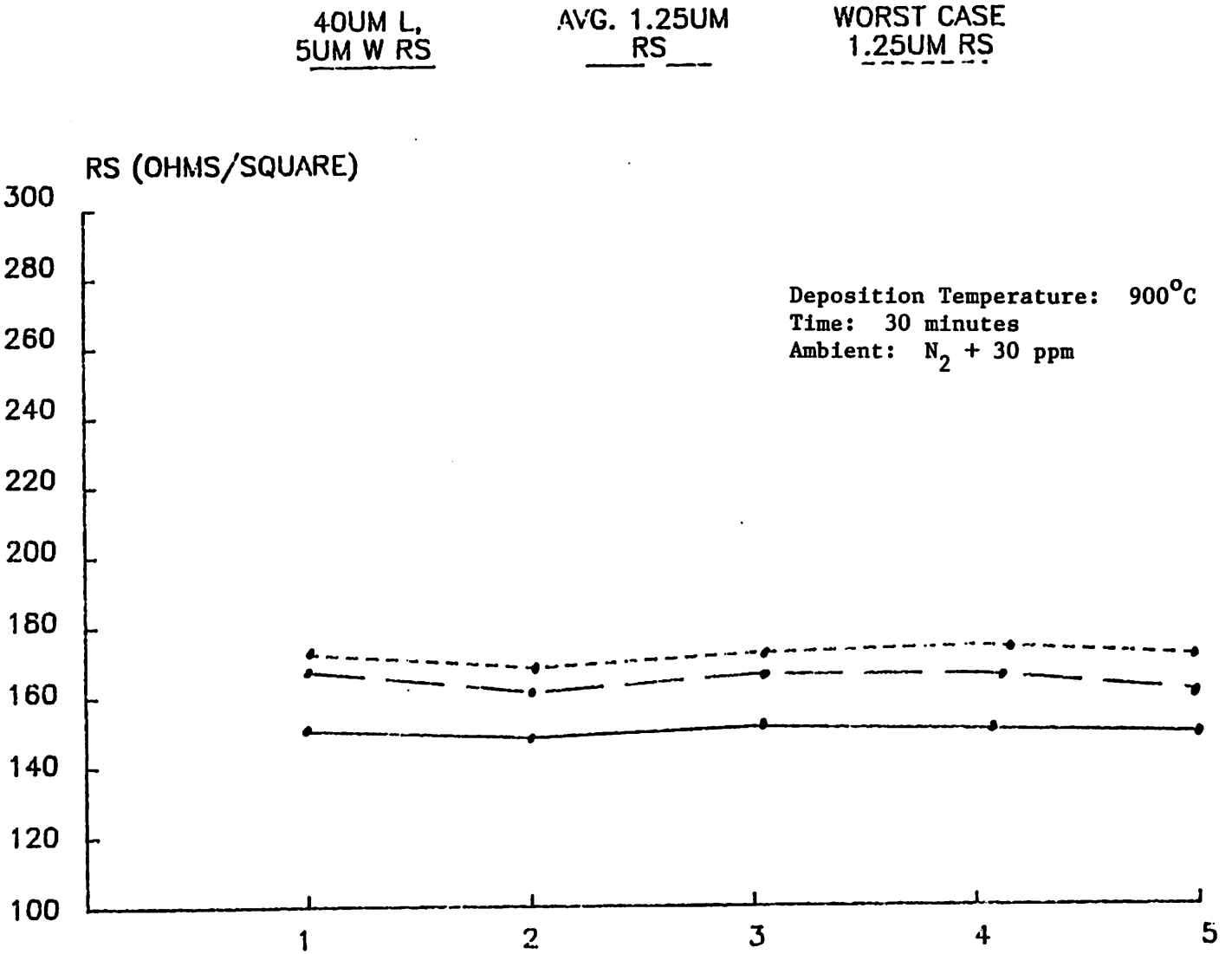
FIGURE 18
BORON+ DRY PROCESS RS VS. CHIP POSITION

40UM L, 5UM W RS — AVG. 1.25UM RS — WORST CASE 1.25UM RS



Data taken from Dry B+ Group 2, wafer 14

FIGURE 19
BORON+ 30PPM PROCESS RS VS. CHIP POSITION



Data taken from 30 PPM B+ group, wafer 14

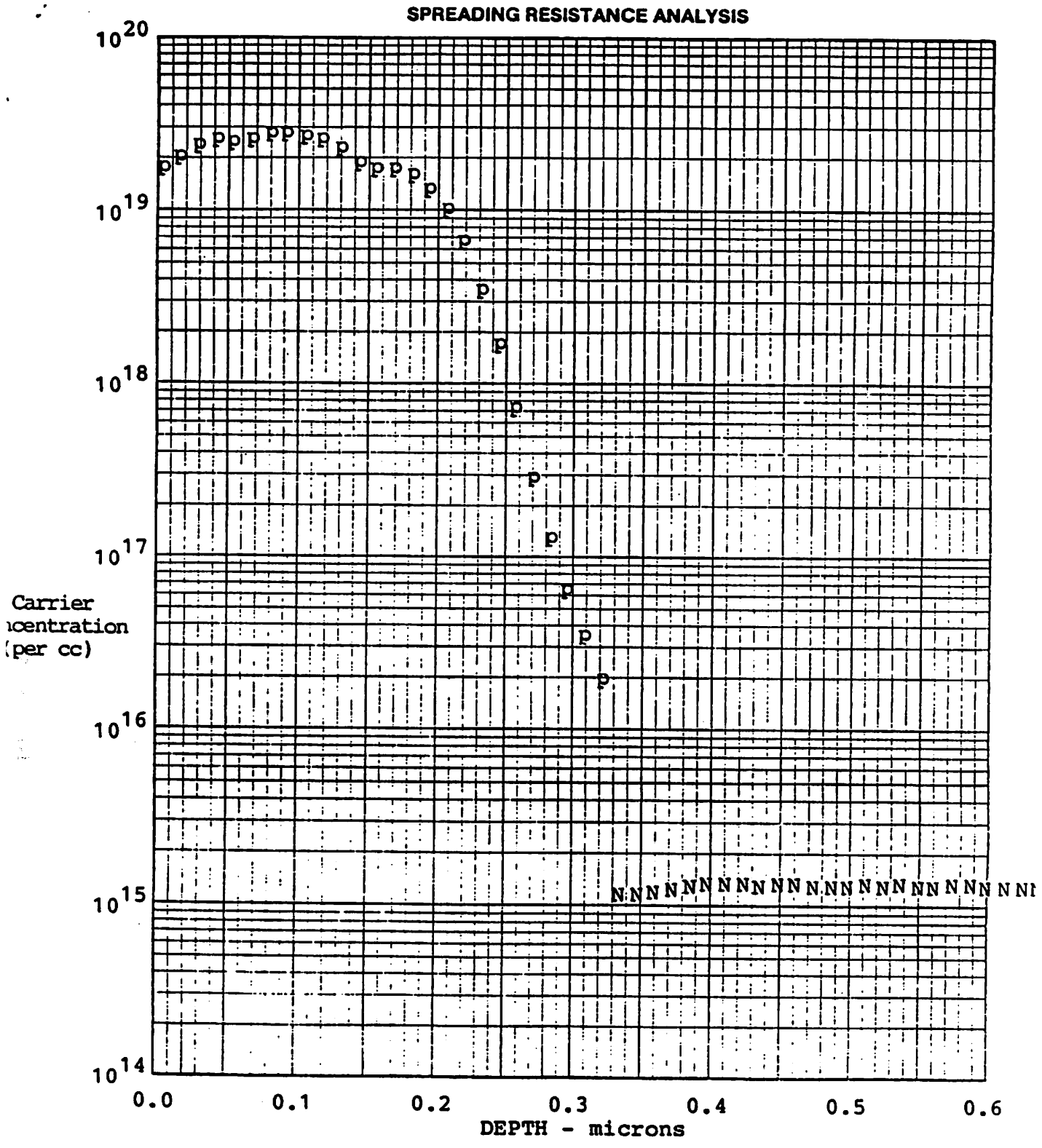


FIGURE 20: BORON NITRIDE 1% H2
INJECTION DOPING PROFILE

800°C 1 min. sourcing, 40 min. drive @ 920°C

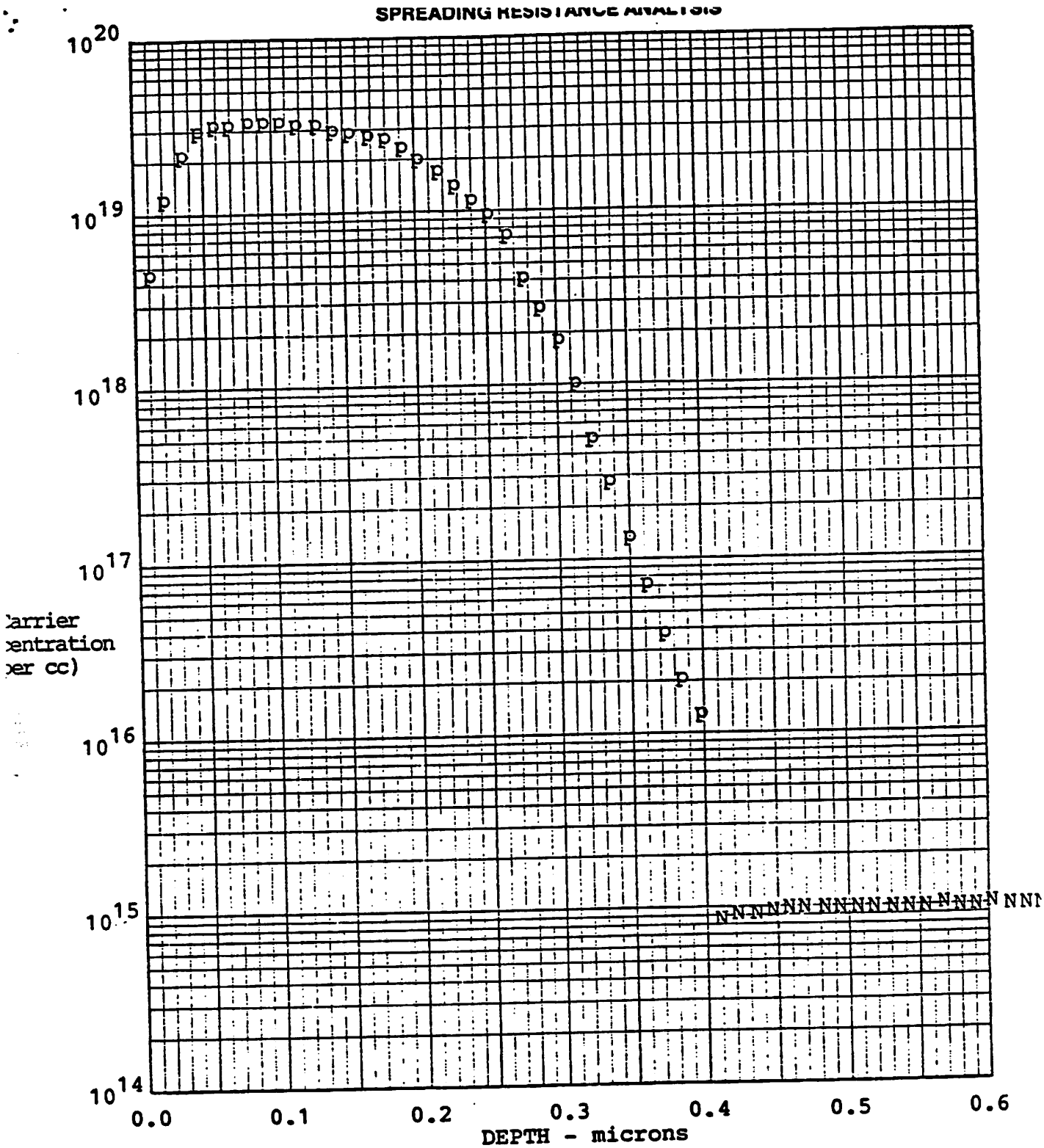


FIGURE 21: BORON+ DRY PROCESS
DOPING PROFILE

900°C for 70 min. dry N_2

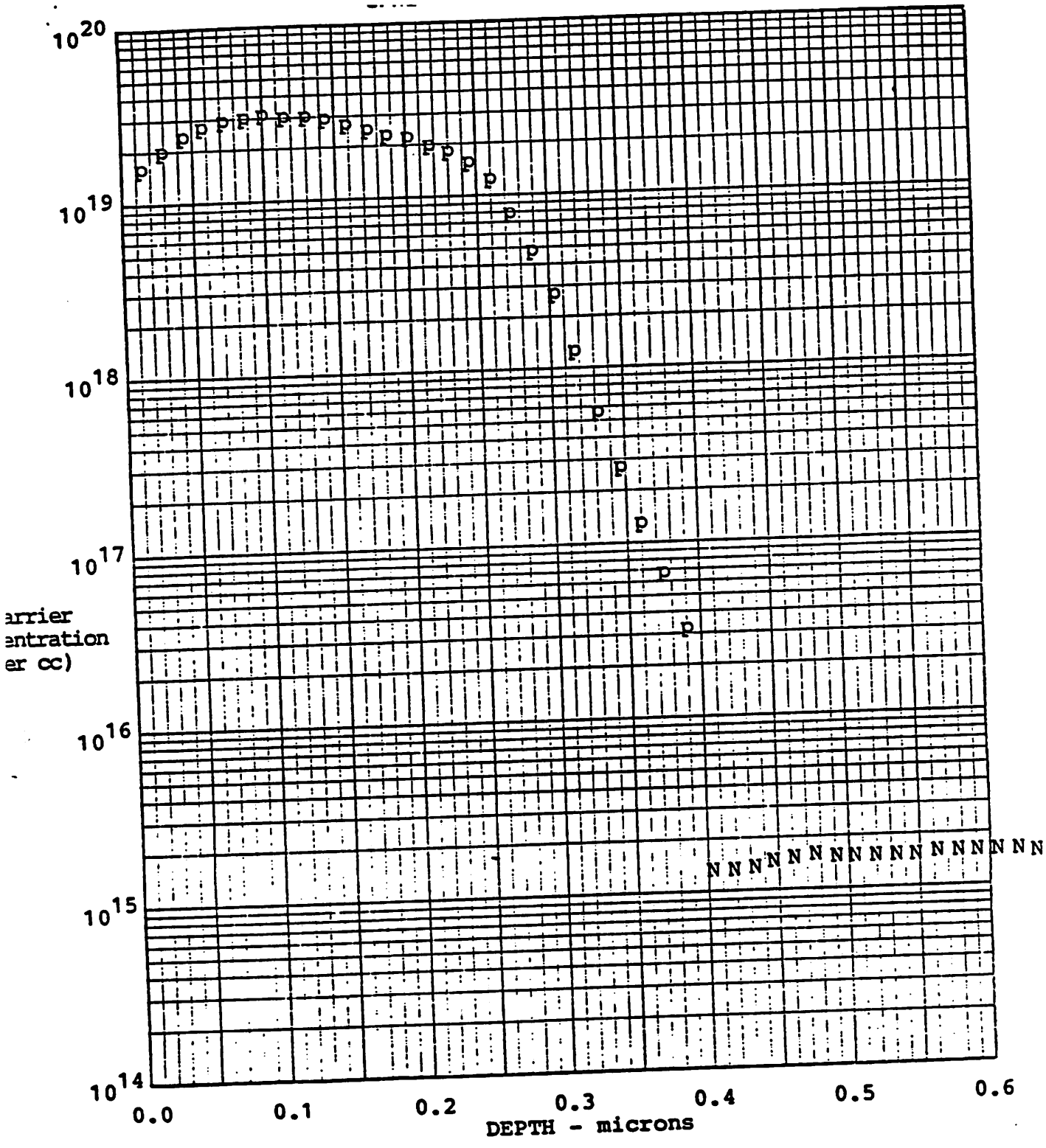


FIGURE 22: BORON+ 15 PPM DOPING PROFILE

900°C for 45 min. N_2 + 15 ppm H_2O

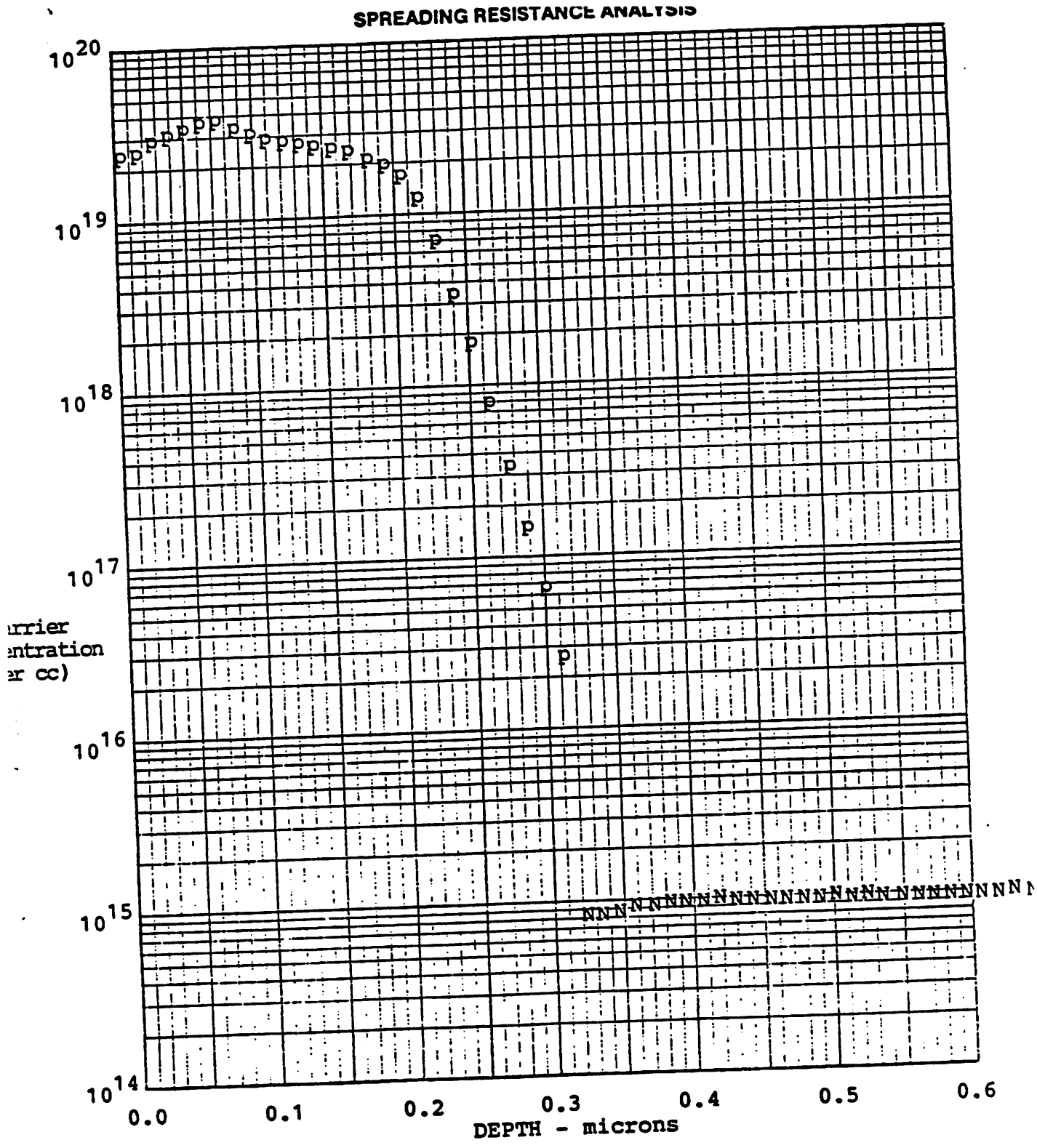


FIGURE 23: BORON+ 60 PPM DOPING PROFILE

900°C for 25 min. N_2 + 60 ppm H_2O

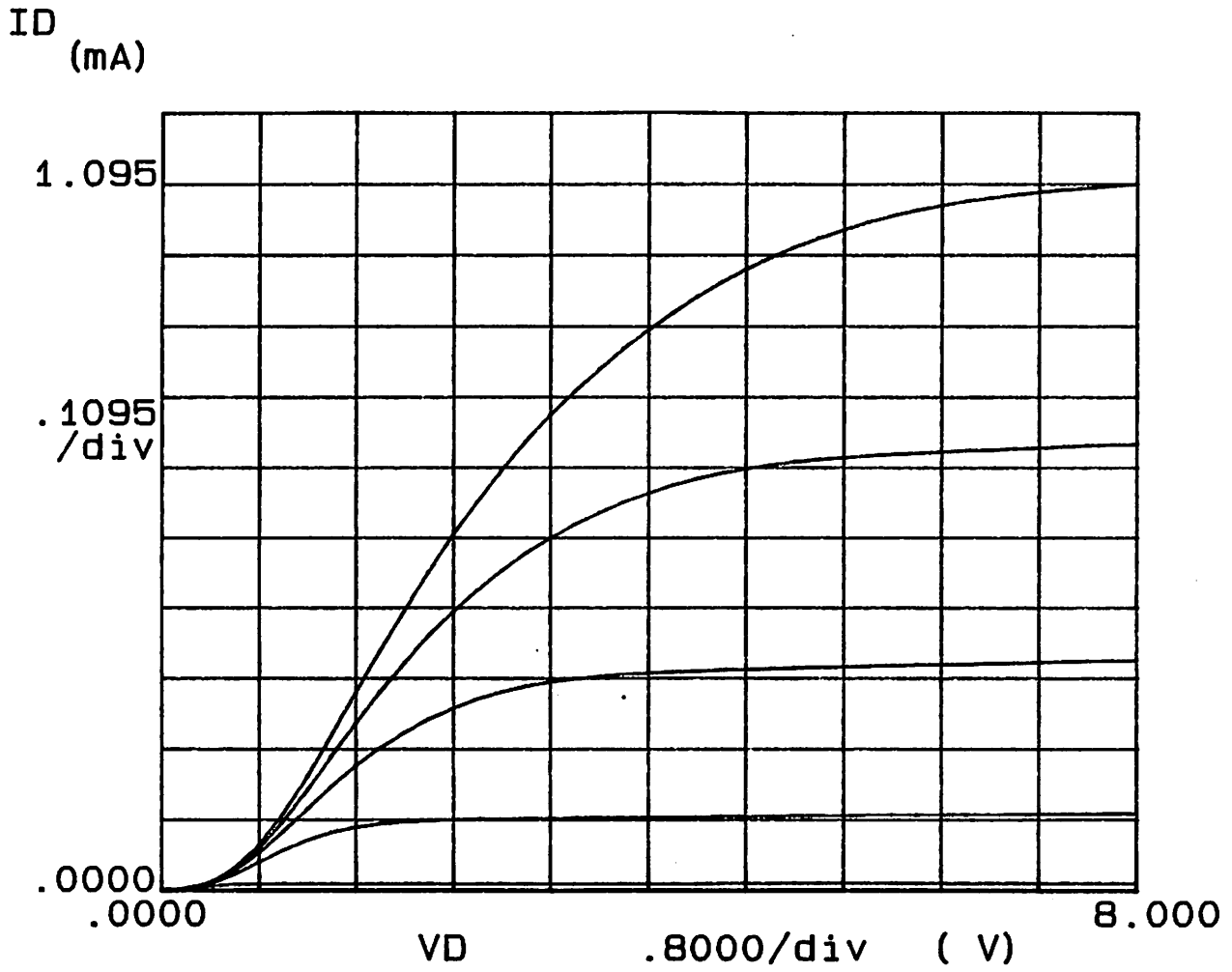


Figure 24

Dry BORON+ Process (30 minutes, 950°C in N_2)

700 A SiO_2 over NMOS

Devices show contact resistance

ROUT (Ω) = ΔVD/ΔID
GD (/Ω) = ΔID/ΔVD

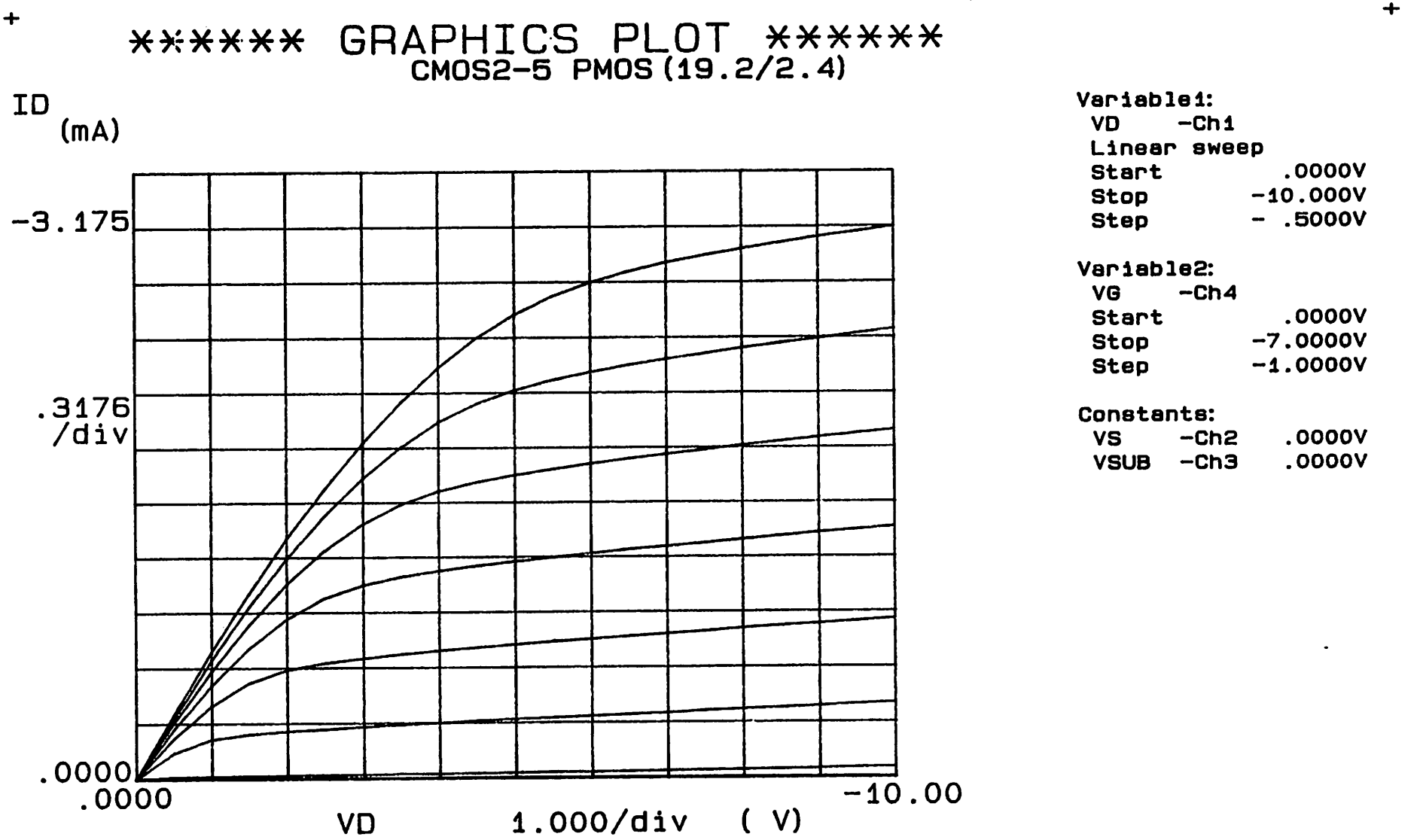


Figure 25a

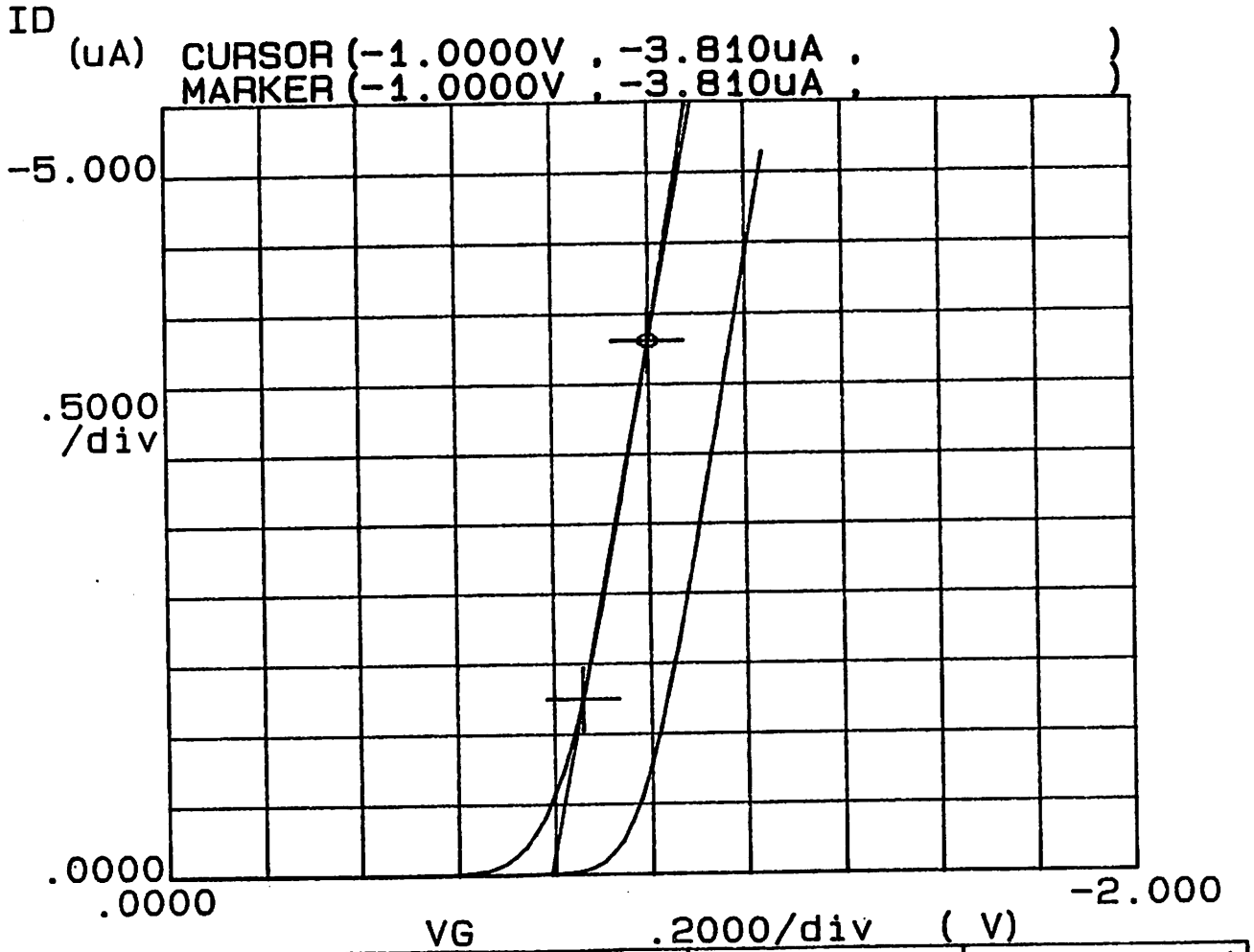
Dry BORON+ Process (30 minutes, 950°C in N_2)

L = 2.4 um p-channel devices

ROUT (Ω) = ΔVD/ΔID
GD (/Ω) = ΔID/ΔVD

****** GRAPHICS PLOT ******

CMOS2-5 PMOS (19.2/2.4)



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	18.3E-06	54.6E+03	-792E-03	14.5E-06
LINE2				

ISUB (A) = ABS (ISU)
I ( ) = 1

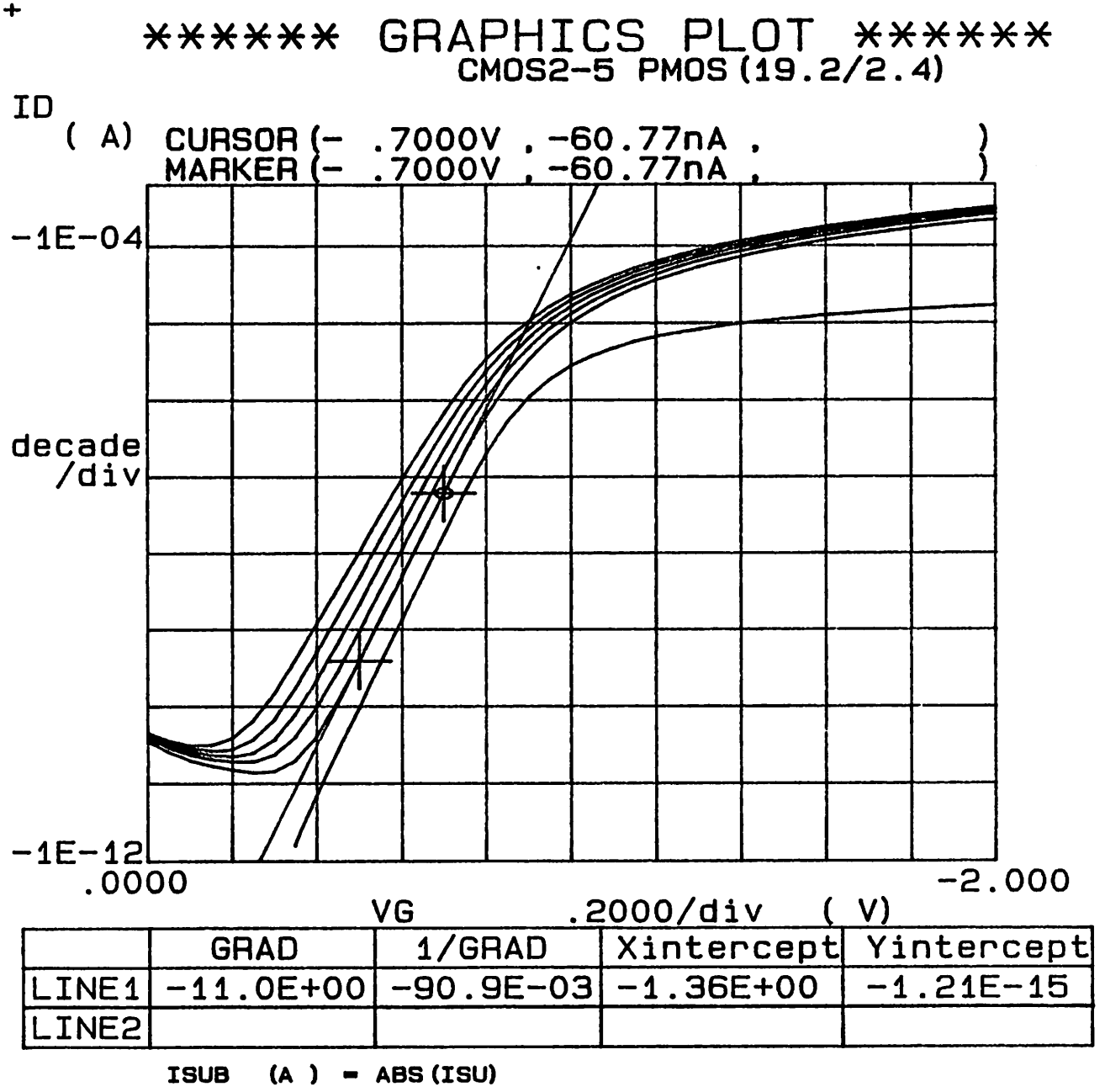
Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop -2.0000V
Step - .0200V

Variable2:
VSUB -Ch3
Start .0000V
Stop 1.0000V
Step 1.0000V

Constants:
VD -Ch1 - .0500V
VS -Ch2 .0000V

Figure 25b

pmos v_t = -0.79 V



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-11.0E+00	-90.9E-03	-1.36E+00	-1.21E-15
LINE2				

ISUB (A) = ABS (ISU)

Figure 25c

Subthreshold current characteristics for pmos device

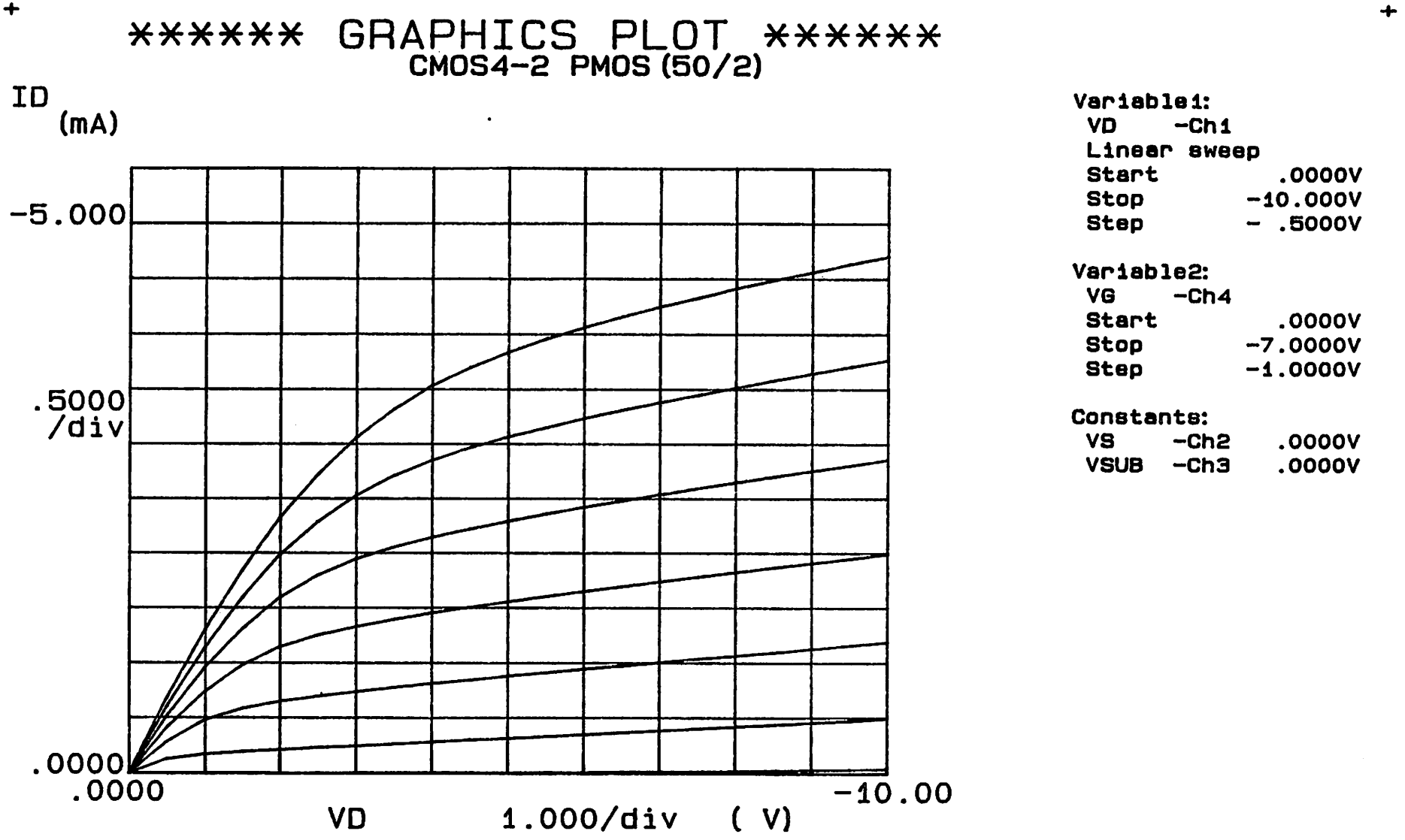
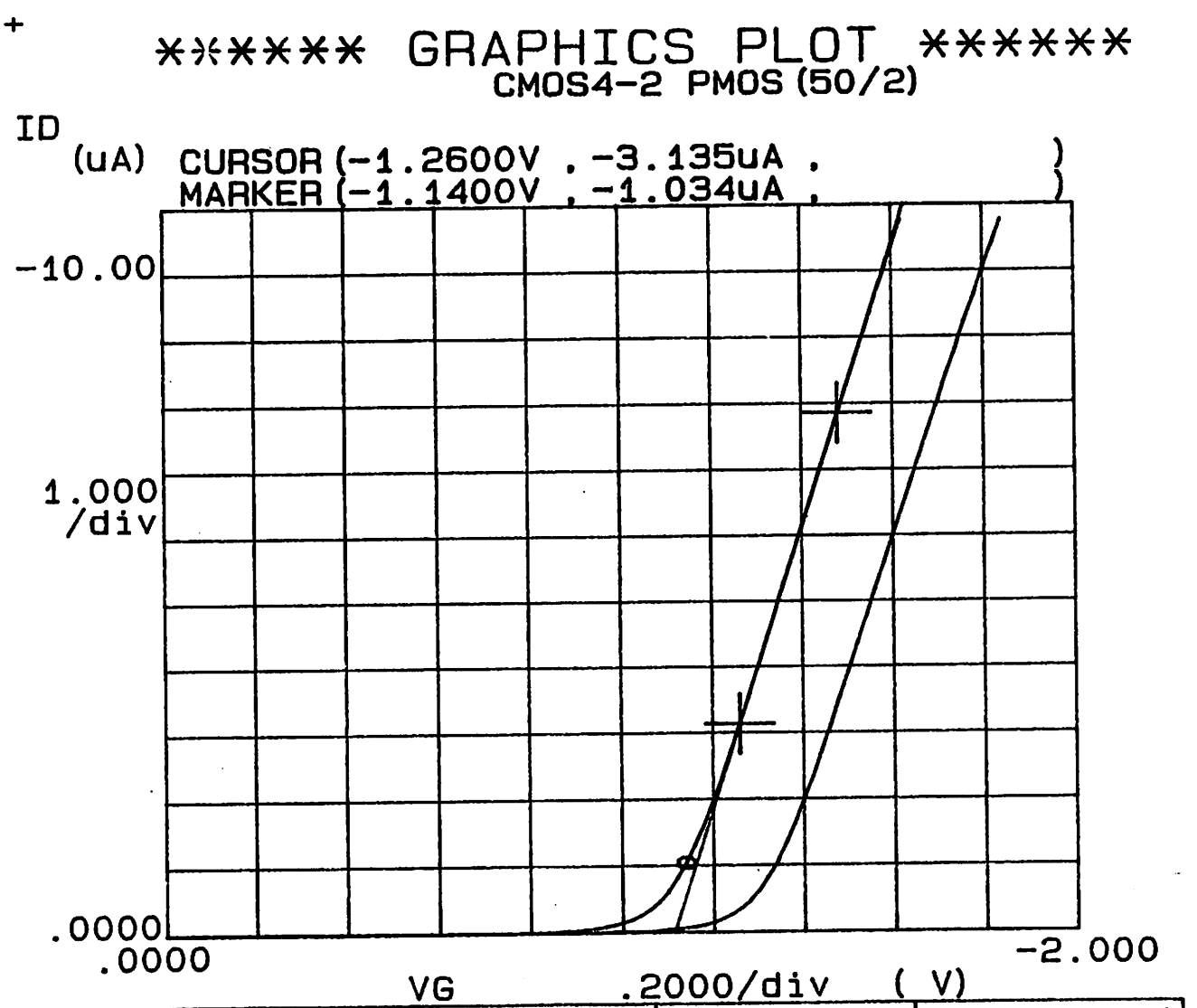


Figure 26a

BORON+ deposition @ 900°C for 30 minutes
Ambient: 60 ppm $H_2O + N_2$
L = 2 um pmos



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	21.5E-06	46.6E+03	-1.11E+00	23.9E-06
LINE2				

ISUB (A) = ABS (ISU)
I ( ) = 1

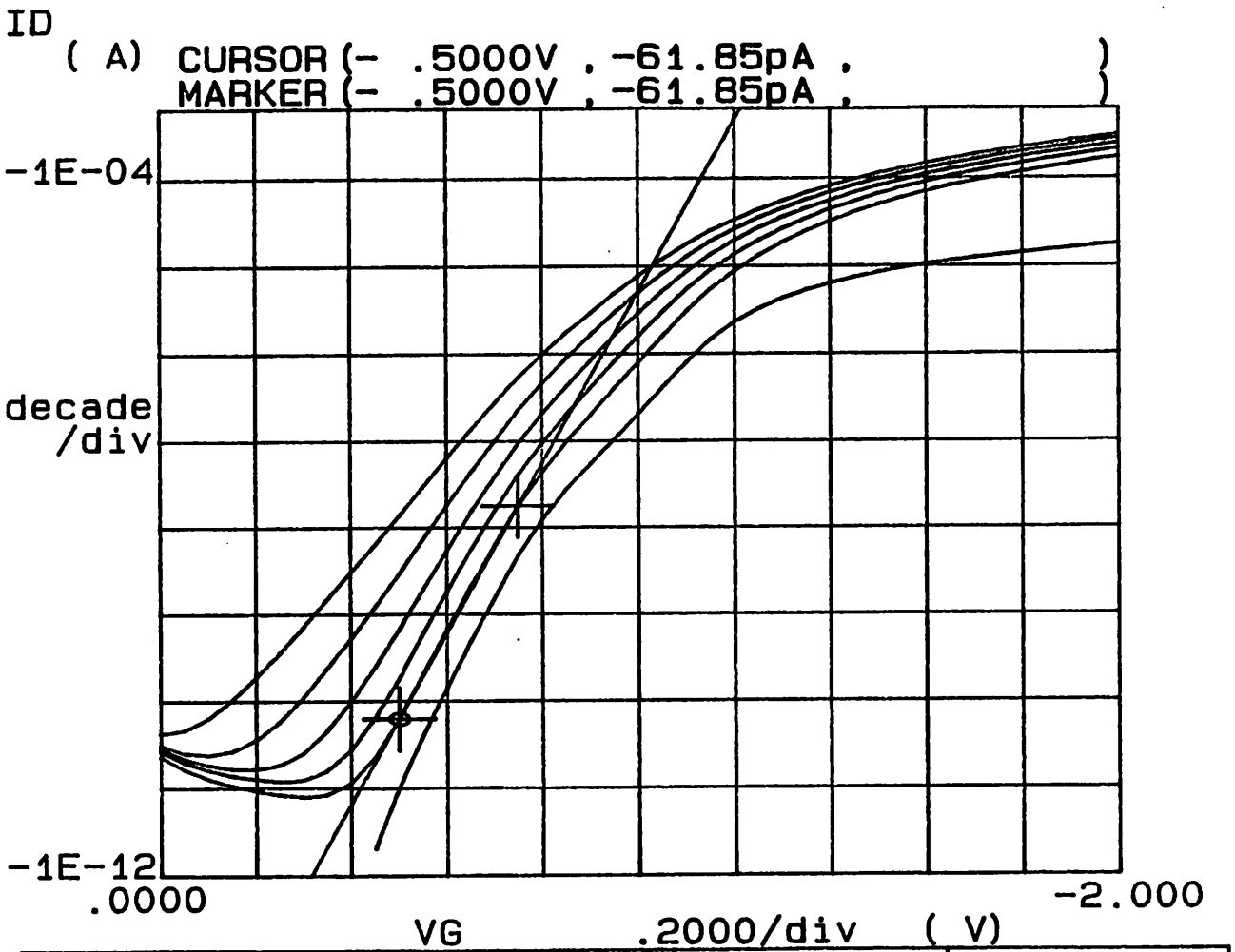
Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop -2.0000V
Step - .0200V

Variable2:
VSUB -Ch3
Start .0000V
Stop 1.0000V
Step 1.0000V

Constants:
VD -Ch1 - .0500V
VS -Ch2 .0000V

Figure 26b

pmos V_t = -1.1 V



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-9.82E+00	-102E-03	-1.54E+00	-758E-18
LINE2				

ISUB (A) = ABS (ISU)

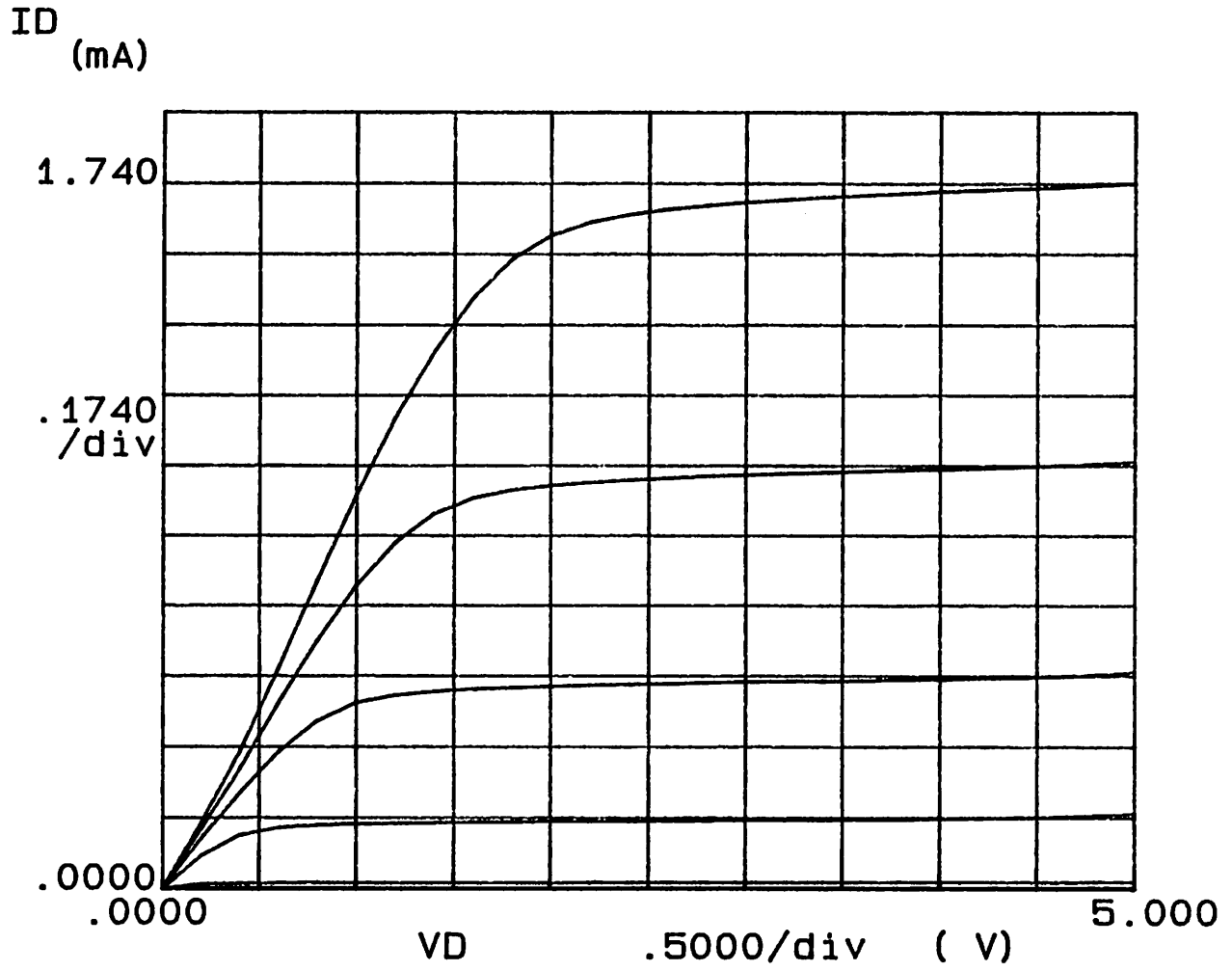
Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop -2.0000V
Step - .0500V

Variable2:
VD -Ch1
Start - .0500V
Stop -5.0500V
Step -1.0000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 26c

Subthreshold current characteristics for pmos device



Variable1:
VD -Ch1
Linear sweep
Start .0000V
Stop 5.0000V
Step .2000V

Variable2:
VG -Ch4
Start .0000V
Stop 7.0000V
Step 1.0000V

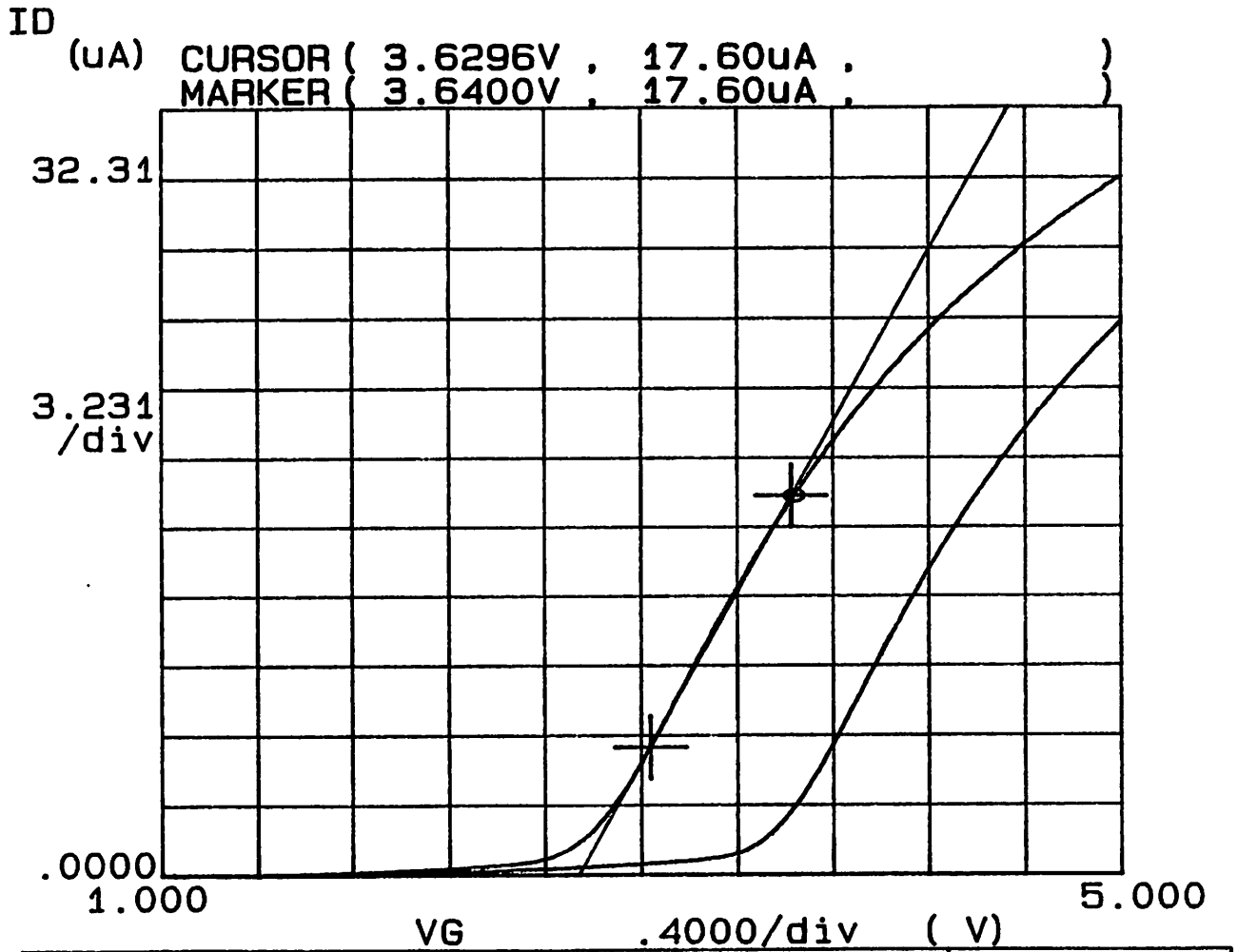
Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 27a

N-MOS devices covered
with thin nitride
during BORON+ diffusion

L = 2um nmos

ROUT (Ω) = ΔVD/ΔID
GD (/Ω) = ΔID/ΔVD



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	19.9E-06	50.3E+03	2.74E+00	-54.5E-06
LINE2				

ISUB (A) = ABS (ISU)
I ( ) = 1

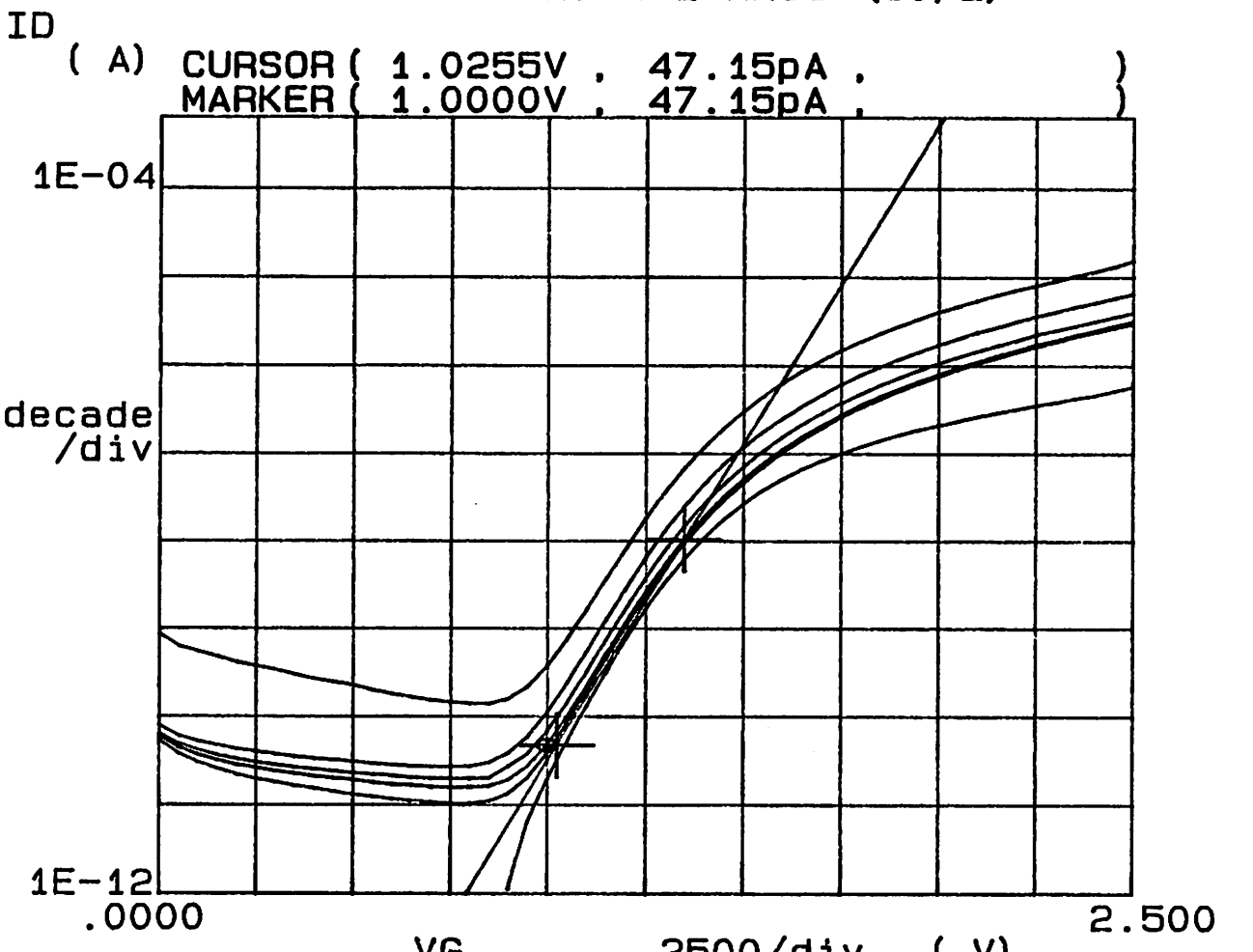
Variable1:
VG -Ch4
Linear sweep
Start 1.0000V
Stop 5.0000V
Step .0200V

Variable2:
VSUB -Ch3
Start .0000V
Stop - .5000V
Step - .5000V

Constants:
VD -Ch1 .0500V
VS -Ch2 .0000V
V1 -Vs1 .0000V

Figure 27b

nmos V_t = 2.7 V



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	7.21E+00	139E-03	2.46E+00	1.89E-18
LINE2				

ISUB (A) = ABS(ISU)

Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 2.5000V
Step .0500V

Variable2:
VD -Ch1
Start .0500V
Stop 10.049V
Step 2.0000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 27c

Subthreshold current characteristics for nmos device

Appendix 1

Boron+ Deposition Program		
Step	**Description**	**Duration (min.)**
Standby	State in which the furnace is kept at when not in use, with the source wafers in it 600°C, N_2 = 2000 sccm	Indeterminate
Thermal Ramp	Ramp furnace to 800°C	10
Temp. Check	Wait until T = 800+/-10°C	Indeterminate
Unload	Extract deposition boat at 3.5 inches/minute, N_2 = 10000 sccm, load silicon wafers	Indeterminate
Load	Insert boat at 3.5 inches/minute	15
Equilbration	Allow boat and furnace to achieve thermal equilibrium at T = 800°C, N_2 = 5000 sccm	15
Thermal Ramp	Ramp to deposition temperature: 900°	10
Set-Up	Delay after thermal ramp is completed and before deposition cycle is begun to allow temperatures to stabilize	3
Deposition	The actual doping glass deposition occurs during this step. All conditions are detailed in the BORON+ DEPOSITION CYCLE table also in this appendix.	Variable
Thermal Ramp	Turn off all process gases except N_2, N_2 = 5000 sccm, ramp furnace down to 800°C	5
Temp. Check	Wait until T = 800+/-10°C	Indeterminate
Unload	Extract deposition boat at 3.5 inches/minute, N_2 = 10000 sccm, unload silicon wafers	Indeterminate
Load	Insert boat at 3.5 inches/minute, N_2 = 10000 sccm	15
Standby	T = 600°C, N_2 = 2000 sccm	Indeterminate

Appendix 1
(Continued)

Boron+ Deposition Cycle Conditions				
Run	**N_2 Flow (sccm)**	**O_2 Flow (sccm)**	**3% H_2 Forming Gas Flow (sccm)**	**Deposition Time (min.)**
Dry B+, Group 1	5000	0	0	70
Dry B+, Group 2	5000	0	0	70
Dry B+ with O_2	5000	2.5	0	70
4 PPM H_2	5000	2.5	0.8	50
8 PPM H_2	5000	2.5	1.4	50
15 PPM H_2	5000	2.5	2.6	45
30 PPM H_2	5000	2.5	5.2	30
60 PPM H_2	5000	2.5	10.0	25
120 PPM H_2	5000	2.5	24	20
250 PPM H_2	5000	2.5	48	20

Appendix 2

BN Deposition Program		
Step	**Description**	**Duration (min.)**
Standby	State in which the furnace is kept when not in use, with the source wafers in it 600°C, N_2 = 2000sccm	Indeterminate
Thermal Ramp	Ramp furnace to 700°C	10
Temp. Check	Wait until T = 700+/-10°C	Indeterminate
Unload	Extract deposition boat at 3.5 inches/minute, N_2 = 10000 sccm, load silicon wafers	Indeterminate
Load	Insert boat at 3.5 inches/min.	15
Equilibration	Allow boat and furnace to achieve thermal equilibrium at T = 700°C, N_2 = 5000 sccm	15
Thermal Ramp	Ramp to deposition temperature: 800°	10
Recovery	Create B_2O_3 surface layer on BN sources O_2 = 2500 sccm	15 N_2 = 2500 sccm,
Deposition	The actual doping glass deposition occurs during this step. For the 1% process, N_2 = 900 sccm, 3% forming gas = 1600 sccm. For the 1.5% process, N_2 = 0 sccm, 3% forming gas = 2400 sccm. In both cases O_2 = 2500 sccm.	1
Soak	Turn off all process gases except N_2, N_2 = 5000 sccm	10
Unload	Extract deposition boat at 3.5 inches/minute, N_2 = 10000 sccm, unload silicon wafers	Indeterminate
Load	Insert boat at 3.5 inches/min. N_2 = 10000 sccm	15
Standby	T = 600°C, N_2 = 2000 sccm	Indeterminate

Appendix 3

Deposited Doped Oxide Thickness			
Run	**Boat Position**	**Thickness (Angstroms)**	**% Standard Deviation**
Dry B+ Group 1	1	686	8
	3	687	7
	5	681	5
	M 10	222	10
	14	717	5
	M 20	230	10
	25	719	3
	27	811	6
Dry B+ Group 2	1	825	7
	3	878	5
	5	864	4
	M 10	324	4
	14	850	4
	M 20	322	3
	25	867	3
	27	872	8
Dry B+ with O_2	1	792	4
	3	766	6
	5	787	5
	M 10	345	4
	14	828	4
	M 20	398	4
	25	851	3
	27	934	3
4 PPM H_2O B+	1	904	5
	3	899	3
	5	903	4
	M 10	521	4
	14	917	2
	M 20	553	3
	25	910	1.6
	27	905	3
8 PPM H_2O B+	1	912	1.6
	3	923	1.2
	5	918	1.9
	M 10	558	3
	14	922	1.3
	M 20	579	2
	25	921	1.1
	27	914	2

"M" prefix indicates an unpatterned monitor

Appendix 3
(Continued)

Deposited Doped Oxide Thickness
(Continued)

Run	Boat Position	Thickness (Angstroms)	% Standard Deviation
15 PPM H_2O B+	1	912	2
	3	950	6
	5	916	4
	M 10	556	6
	14	902	2
	M 20	595	2
	25	876	3
	27	892	2
30 PPM H_2O B+	1	872	3
	3	875	2
	5	872	3
	M 10	566	3
	14	864	1.6
	M 20	577	2
	25	846	1.6
	27	850	0.9
60 PPM H_2O B+	1	890	4
	3	880	3
	5	867	3
	M 10	623	3
	14	837	6
	M 20	631	2
	25	832	5
	27	846	4
120 PPM H_2O B+	1	858	6
	3	586	20
	5	817	3
	M 10	not available	
	14	848	1.1
	M 20	651	4
	25	421	22
	27	539	23
250 PPM H_2O B+	1	520	10
	3	601	6
	5	680	11
	M 10	620	8
	14	639	6
	M 20	613	2
	25	624	7
	27	477	12

"M" prefix indicates an unpatterned monitor

Appendix 3
(Continued)

Deposited Doped Oxide Thickness
(Continued)

Run	Boat Position	Thickness (Angstroms)	% Standard Deviation
1.0%H_2 Injection BN	1	704	7
	3	703	7
	5	680	14
	M 7	699	4
	10	668	5
	M 14	690	2
	18	627	9
	20	702	6
1.5%H_2 Injection BN	1	762	8
	3	779	5
	5	771	7
	M 7	774	3
	10	763	5
	M 14	845	5
	18	725	5
	20	832	7

Appendix 4

Ellipsometer Measurements on Doped Silicon				
Run	**Boat Position**	**Psi and Std. Dev. (Degrees)**	**Delta and Std. Dev. (Degrees)**	**B-Si Thickness (Angstroms)**
Dry B+ Group 1	1	9.80+/-0.02	175.3+/-0.6	11
	3	9.84+/-0.04	175.7+/-0.6	10
	5	9.82+/-0.04	175.6+/-0.8	10
	M 10	9.74+/-0.03	169.9+/-0.5	27
	14	9.77+/-0.06	175.0+/-1.0	12
	M 20	9.72+/-0.08	170.1+/-0.4	26
	25	9.86+/-0.03	175.2+/-0.8	11
	27	9.94+/-0.04	172.5+/-2.0	19
Dry B+ Group 2	1	9.65+/-0.04	175.9+/-0.2	9
	3	9.72+/-0.05	176.0+/-0.2	9
	5	9.77+/-0.07	175.5+/-0.3	10
	M 10	9.62+/-0.05	172.5+/-0.7	19
	14	9.77+/-0.04	175.6+/-0.4	10
	M 20	9.71+/-0.03	172.5+/-0.6	19
	25	9.77+/-0.11	175.4+/-0.6	11
	27	10.34+/-0.72	164.7+/-4.9	44
Dry B+ with O_2	1	9.30+/-0.05	174.2+/-0.3	14
	3	9.33+/-0.09	174.3+/-0.4	13
	5	9.25+/-0.04	174.1+/-0.6	14
	M 10	9.19+/-0.04	171.3+/-0.4	22
	14	9.27+/-0.03	172.8+/-1.5	18
	M 20	9.18+/-0.04	172.4+/-0.4	19
	25	9.41+/-0.05	173.2+/-0.9	17
	27	9.78+/-0.28	169.2+/-4.2	29
4 PPM H_2O B+	1	9.83+/-0.01	176.8+/-0.6	6
	3	9.79+/-0.08	176.4+/-0.6	8
	5	9.84+/-0.04	176.6+/-0.6	7
	M 10	9.73+/-0.02	176.1+/-0.2	8
	14	9.69+/-0.07	176.3+/-0.7	8
	M 20	9.65+/-0.07	176.1+/-0.3	8
	25	9.81+/-0.02	175.6+/-1.2	10
	27	10.42+/-0.38	167.0+/-8.8	37

Measurements were all carried out at theta = 70 degrees. Film thickness calculations assume boron silicide phase refractive index = 1.60.

"M" prefix indicates an unpatterned monitor.

Appendix 4
(Continued)

Ellipsometer Measurements on Doped Silicon
(Continued)

Run	Boat Position	Psi and Std. Dev. (Degrees)	Delta and Std. Dev. (Degrees)	B-Si Thickness (Angstroms)
8 PPM H_2O	1	9.33+/-0.04	173.9+/-1.0	14
B+	3	9.37+/-0.13	174.1+/-0.8	14
	5	9.24+/-0.03	174.2+/-0.9	13
	M 10	9.21+/-0.05	174.2+/-0.8	13
	14	9.27+/-0.05	174.2+/-0.9	14
	M 20	9.21+/-0.03	173.8+/-0.2	15
	25	9.29+/-0.04	173.4+/-0.5	16
	27	9.44+/-0.22	170.8+/-4.7	24
15 PPM H_2O	1	9.34+/-0.04	174.2+/-0.8	14
B+	3	9.36+/-0.05	173.9+/-1.2	14
	5	9.35+/-0.04	174.0+/-1.1	14
	M 10	9.28+/-0.06	173.7+/-0.2	15
	14	9.35+/-0.03	174.2+/-0.8	14
	M 20	9.30+/-0.01	173.5+/-0.3	16
	25	9.37+/-0.07	173.0+/-1.9	17
	27	9.33+/-0.02	173.3+/-0.3	16
30 PPM H_2O	1	9.29+/-0.04	174.1+/-0.7	14
B+	3	9.31+/-0.02	174.2+/-0.8	14
	5	9.33+/-0.05	174.0+/-0.7	14
	M 10	9.25+/-0.05	173.1+/-0.1	17
	14	9.33+/-0.05	173.8+/-0.7	16
	M 20	9.25+/-0.03	173.0+/-0.3	17
	25	9.30+/-0.03	174.0+/-0.6	14
	27	9.38+/-0.08	171.2+/-2.2	22
60 PPM H_2O	1	9.30+/-0.02	174.0+/-0.6	14
B+	3	9.34+/-0.03	174.0+/-0.6	14
	5	9.33+/-0.03	173.7+/-0.7	15
	M 10	9.31+/-0.02	172.7+/-0.2	18
	14	9.33+/-0.03	173.8+/-0.3	15
	M 20	9.27+/-0.03	172.6+/-0.1	18
	25	9.33+/-0.05	173.7+/-0.5	15
	27	9.32+/-0.02	173.1+/-0.5	17

"M" prefix indicates an unpatterned monitor.

Appendix 4
(Continued)

Ellipsometer Measurements on Doped Silicon
(Continued)

Run	Boat Position	Psi and Std. Dev. (Degrees)	Delta and Std. Dev. (Degrees)	B-Si Thickness (Angstroms)
120 PPM H_2O	1	9.57+/-0.06	172.4+/-0.3	19
B+	3	9.70+/-0.05	172.5+/-0.4	19
	5	9.65+/-0.07	172.5+/-0.4	19
	M 10	9.57+/-0.05	172.3+/-0.5	19
	14	9.37+/-0.08	172.2+/-0.8	19
	M 20	9.22+/-0.05	172.0+/-0.7	20
	25	9.29+/-0.03	172.8+/-0.4	18
	27	9.37+/-0.09	172.0+/-1.2	20
250 PPM H_2O	1	9.15+/-0.06	172.1+/-0.6	19
B+	3	9.11+/-0.04	172.0+/-0.6	20
	5	9.22+/-0.08	171.9+/-0.6	20
	M 10	9.15+/-0.05	171.8+/-0.2	20
	14	9.07+/-0.05	172.2+/-0.6	19
	M 20	9.00+/-0.02	170.6+/-1.0	23
	25	9.05+/-0.06	170.7+/-0.3	23
	27	9.07+/-0.04	171.9+/-0.7	20
1.0%H_2	1	9.89+/-0.12	154.5+/-2.8	73
Injection	3	9.73+/-0.07	156.6+/-1.2	66
BN	5	9.71+/-0.07	156.8+/-1.1	65
	M 7	9.54+/-0.04	158.4+/-1.1	60
	10	9.53+/-0.02	158.8+/-2.1	59
	M 14	9.60+/-0.04	158.7+/-0.8	59
	18	9.62+/-0.03	158.8+/-1.0	59
	20	9.65+/-0.06	158.4+/-1.0	60
1.5%H_2	1	9.83+/-0.11	155.4+/-1.4	70
Injection	3	9.82+/-0.06	157.1+/-1.1	65
BN	5	9.83+/-0.09	155.5+/-2.1	70
	M 7	9.73+/-0.03	156.6+/-0.7	66
	10	9.63+/-0.06	158.8+/-0.9	59
	M 14	9.73+/-0.07	154.8+/-0.9	71
	18	broken	----+/----	—
	20	9.76+/-0.01	157.3+/-1.1	64

"M" prefix indicates an unpatterned monitor.

Appendix 5

Field Oxide Lost During Doped Oxide Removal				
Run	**Boat Position**	**Oxide Lost (Angstroms)**	**%Standard Deviation**	**20:1 BHF Etch Time (sec)**
Dry B+ Group 1	1 3 5 14 25 27	Data Not Available	Data Not Available	Data Not Available
Dry B+ Group 2	1	349	4	30
	3	409	14	
	5	388	5	
	14	398	10	
	25	329	11	
	27	242	16	
Dry B+ with O_2	1	300	13	35
	3	388	11	
	5	377	7	
	14	369	8	
	25	318	12	
	27	261	15	
4 PPM H_2O B+	1	269	13	45
	3	343	12	
	5	349	18	
	14	388	9	
	25	340	6	
	27	310	4	
8 PPM H_2O B+	1	249	20	60
	3	300	7	
	5	304	7	
	14	276	8	
	25	282	14	
	27	210	18	
15 PPM H_2O B+	1	216	4	40
	3	215	14	
	5	210	11	
	14	213	8	
	25	219	10	
	27	157	6	

Appendix 5
(Continued)

Field Oxide Lost During Doped Oxide Removal
(Continued)

Run	Boat Position	OxideLost (Angstroms)	%Standard Deviation	20:1 BHF Etch Time (sec)
30 PPM H_2O B+	1	231	22	40
	3	259	2	
	5	259	5	
	14	240	5	
	25	244	1	
	27	222	14	
60 PPM H_2O B+	1	229	14	40
	3	274	7	
	5	226	11	
	14	246	11	
	25	243	5	
	27	222	6	
120 PPM H_2O B+	1	235	9	40
	3	300	8	
	5	267	4	
	14	233	9	
	25	290	6	
	27	265	13	
250 PPM H_2O B+	1	1045	5	220: Rate on wafer 14 only 280A/min. and additional etch required to remove all glass.
	3	1038	6	
	5	1008	5	
	14	851	9	
	25	1016	10	
	27	910	8	
1.0% H_2 Injection BN	1	562	7	560: Rate on wafer 10 only 117A/min. for the doped glass.
	3	570	12	
	5	643	5	
	10	544	4	
	18	579	7	
	20	656	8	
1.5% H_2 Injection BN	1	604	7	530: Rate on wafer 10 only 122A/min. for the doped glass.
	3	551	5	
	5	628	6	
	10	490	6	
	18	561	2	
	20	536	7	

Appendix 6

In the tables that follow, the mean and standard deviation of the calculated sheet resistance is presented for all combinations of L, the diffusion resistor linewidth, and W, the width of the field oxide frame surrounding the resistor and separating it from another very large p+ diffusion which in turn surrounds the frame. The dimensions quoted below are all mask dimensions; the actual dimensions on the wafer after processing were measured and used in the calculation of the sheet resistances but are not shown here for clarity's sake: they can instead be found in Appendix 7. All the statistics are for batches of five or six wafers (i.e., each point represents 25-30 measurements).

Sheet Resistance from Four Terminal Resistors

Dry B+ Group 1					
Mean Sheet Resistance (ohms/square)					
W (um)	**L (um)**				
	1.25	**2.5**	**5.0**	**10**	**40**
5.0	185.7	135.9	126.3	127.9	130.9
20	186.2	134.1	128.7	132.3	134.4
>500	164.9	143.7	135.8	141.1	141.8
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	**L (um)**				
	1.25	**2.5**	**5.0**	**10**	**40**
5.0	36.1	5.8	4.0	3.0	4.7
20	35.3	6.1	4.5	3.7	3.5
>500	14.7	6.4	4.3	3.4	3.6

Dry B+ Group 2					
Mean Sheet Resistance (ohms/square)					
W (um)	**L (um)**				
	1.25	**2.5**	**5.0**	**10**	**40**
5.0	169.4	133.3	129.2	129.3	134.9
20	173.5	136.2	131.5	136.1	138.9
>500	160.9	143.6	136.9	143.4	145.4
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	**L (um)**				
	1.25	**2.5**	**5.0**	**10**	**40**
5.0	38.5	25.0	4.5	6.4	4.2
20	34.1	7.1	4.8	4.4	4.9
>500	18.2	8.2	4.9	3.7	4.4

Appendix 6
(Continued)

Sheet Resistance from Four Terminal Resistors
(Continued)

Dry B+ with O_2					
Mean Sheet Resistance (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	111.9	112.5	110.5	116.0	122.9
20	113.9	116.1	115.6	120.3	125.9
>500	125.9	126.2	123.3	129.3	133.7
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	5.1	4.2	3.3	3.2	3.7
20	4.5	4.0	3.5	3.5	3.9
>500	6.3	4.1	3.4	3.6	4.4

4 PPM B+					
Mean Sheet Resistance (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	137.3	132.0	129.2	134.7	142.6
20	142.3	130.5	131.7	140.2	146.4
>500	145.5	139.8	139.0	149.5	154.7
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	10.0	3.5	2.8	2.4	2.5
20	9.0	3.5	3.0	2.6	2.5
>500	8.0	4.3	3.5	2.9	2.6

Appendix 6
(Continued)

Sheet Resistance from Four Terminal Resistors
(Continued)

8 PPM B+					
Mean Sheet Resistance (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	120.3	123.2	119.4	127.5	134.9
20	125.4	129.0	128.3	132.7	138.5
>500	144.9	143.0	137.7	143.6	147.3
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	10.0	11.8	15.4	4.2	4.3
20	6.5	5.5	4.8	4.3	4.4
>500	9.1	5.1	4.5	4.7	5.2

15 PPM B+					
Mean Sheet Resistance (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	153.1	142.5	133.1	136.0	139.7
20	160.6	142.0	135.6	139.0	142.4
>500	150.9	143.7	139.5	146.2	150.0
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	15.6	17.6	13.3	11.6	9.1
20	16.8	16.7	11.9	10.1	7.8
>500	8.5	7.8	7.5	7.3	7.2

Appendix 6
(Continued)

Sheet Resistance from Four Terminal Resistors
(Continued)

30 PPM B+					
Mean Sheet Resistance (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	151.9	144.1	139.0	142.6	148.2
20	159.4	145.2	143.0	147.1	151.8
>500	164.7	154.4	149.1	156.4	161.0
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	5.0	2.5	2.0	1.9	1.9
20	4.9	2.4	2.1	1.9	2.1
>500	5.4	4.2	3.5	3.8	3.8

60 PPM B+					
Mean Sheet Resistance (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	155.6	143.5	137.0	140.8	146.8
20	162.1	143.7	137.8	141.5	147.0
>500	160.6	149.9	144.1	151.3	156.6
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	13.1	12.6	13.0	14.8	17.3
20	11.4	10.9	12.5	14.8	16.6
>500	14.9	14.8	14.5	15.9	17.6

Appendix 6
(Continued)

Sheet Resistance from Four Terminal Resistors
(Continued)

120 PPM B+					
Mean Sheet Resistance (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	111.8	112.6	111.3	116.8	121.9
20	121.8	115.1	113.7	118.1	122.8
>500	126.8	123.5	119.4	123.5	128.4
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	10.5	10.0	9.0	9.1	9.7
20	11.9	10.6	10.0	10.0	10.5
>500	15.8	15.8	13.8	14.2	15.3

250 PPM B+					
Mean Sheet Resistance (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	106.1	106.7	104.0	108.4	112.6
20	113.7	107.9	105.6	109.0	112.7
>500	122.0	116.1	108.6	110.8	113.5
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	L(um)				
	1.25	2.5	5.0	10	40
5.0	7.4	6.6	5.7	5.2	5.9
20	8.5	7.3	6.9	6.4	6.8
>500	11.7	9.6	7.1	5.9	6.8

Appendix 6
(Continued)

Sheet Resistance from Four Terminal Resistors
(Continued)

1.0% H_2 Injection BN					
Mean Sheet Resistance (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	112.1	116.3	116.6	125.0	131.1
20	114.1	112.6	114.9	124.4	130.4
>500	117.7	117.8	114.8	121.6	126.2
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	8.9	5.3	4.9	4.5	4.2
20	8.9	5.2	4.5	4.2	4.0
>500	13.7	11.0	6.8	4.8	3.6

1.5% H_2 Injection BN					
Mean Sheet Resistance (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	132.3	124.7	122.2	129.4	134.5
20	131.5	119.7	119.8	128.9	133.5
>500	124.5	119.4	116.7	124.3	129.5
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	17.9	5.6	4.7	5.1	4.2
20	16.1	5.8	4.6	4.2	4.1
>500	10.1	7.3	5.3	4.8	4.5

Appendix 6
(Continued)

Sheet Resistance from Four Terminal Resistors
(Continued)

BF_2 Implant (Wafers 5 and 6 only)					
Mean Sheet Resistance (ohms/square)					
W (um)	**L (um)**				
	1.25	**2.5**	**5.0**	**10**	**40**
5.0	124.7	122.7	116.4	121.2	122.7
20	125.0	125.8	119.3	122.4	123.3
>500	134.5	129.1	121.1	124.1	124.6
Sheet Resistance Standard Deviation (ohms/square)					
W (um)	**L (um)**				
	1.25	**2.5**	**5.0**	**10**	**40**
5.0	2.4	1.9	1.1	0.8	1.0
20	2.7	2.0	1.5	1.3	1.0
>500	4.3	1.8	1.3	0.9	1.2

Appendix 7

Measured Linewidths ("L" in Figure 3) of Four Terminal Resistors

In what follows, the measured diffusion linewidths for the various groups are listed in the same format as in the preceeding Appendix 6.

Dry B+ Group 1; Dry B+ Group 2; 4 PPM B+; 1.0% H_2 Injection BN; 1.5% H_2 Injection BN					
W (um)	L (um)				
	1.25	2.5	5.0	10	40
5.0	2.064um	3.383	5.492	10.3	40
20	2.11	3.26	5.42	10.3	40
>500	2.11	3.26	5.42	10.3	40

Dry B+ with $O_2$2, 8 PPM B+, BF2 Implant					
W (um)	L (um)				
1.25	2.5	5.0	10	40	
5.0	2.245um	3.29	5.39	10.2	40
20	2.21	3.28	5.44	10.2	40
>500	2.21	3.28	5.44	10.2	40

15 PPM B+, 30 PPM B+, 60 PPM B+					
W (um)	L (um)				
1.25	2.5	5.0	10	40	
5.0	2.391um	3.61	5.73	10.4	40
20	2.48	3.57	5.73	10.4	40
>500	2.48	3.57	5.73	10.4	40

120 PPM B+, 250 PPM B+					
W (um)	L (um)				
1.25	2.5	5.0	10	40	
5.0	2.53um	3.74	5.84	10.5	40
20	2.72	3.78	5.91	10.5	40
>500	2.72	3.78	5.91	10.5	40

Appendix 8

Unpatterned Monitor Sheet Resistance			
Run	**Boat Position**	**Rs (ohms/square)**	**Std. Dev.**
Dry B+ Group 1	10 20	100 broken	2.3%
Dry B+ Group 2	10 20	broken 110	1.0%
Dry B+ With O_2	10 20	103 broken	1.5%
4 PPM B+	10 20	124 broken	0.9%
8 PPM B+	10 20	broken broken	
15 PPM B+	10 20	broken 113	0.5%
30 PPM B+	10 20	117 broken	0.4%
60 PPM B+	10 20	broken 116	0.6%
120 PPM B+	10 20	108 116	2.0% 3.1%
250 PPM B+	10 20	116 broken	2.5%
1% H_2 Injection BN	7 14	broken 134	0.7%
1.5% H_2 Injection BN	7 14	141 broken	0.6%
BF2 Implant	9	118	2.2%

Appendix 9

Diode Reverse Breakdown Data					
Run	**Boat Position**	**Area Diode Leakage at -10V (pA)**	**Area BDV (V)**	**Edge Diode Leakage at -10V (pA)**	**Edge BDV (V)**
Dry B+ Group 1	1	23	37	27	37
	3	7.8	39	7.9	39
	5	15	46	9.5	47
	14	7.8	57	6.7	53
	25	8.0	80	5.5	77
	27	11	59	9.3	66
Dry B+ Group 2	1	9.2	41	13	41
	3	broken			
	5	13	40	15	42
	14	18	56	20	55
	25	13	78	8.1	74
	27	12	48	15	49
Dry B+ with O_2	1	15	48	12	50
	3	9.3	50	11	51
	5	broken			
	14	2.5	44	2.0	56
	25	2.6	53	3.1	51
	27	14	52	18	51
4 PPM B+	1	1.0	70	1.2	69
	3	12	48	12	43
	5	9.1	76	8.1	71
	14	10	89	8.8	83
	25	3.8	62	2.0	62
	27	9.2	80	12	76
8 PPM B+	1	11	47	17	48
	3	11	69	8.5	66
	5	16	68	12	64
	14	3.3	42	2.8	37
	25	0.7	68	0.8	62
	27	1.2	60	2.0	59
15 PPM B+	1	2.7	80	3.0	77
	3	8.9	>100	6.4	>100
	5	broken			
	14	20	67	17	57
	25	1.6	54	1.5	52
	27	7.6	87	8.7	82

Appendix 9
(Continued)

Diode Reverse Breakdown Data (Continued)					
Run	**Boat Position**	**Area Diode Leakage at -10V (pA)**	**Area BDV (V)**	**Edge Diode Leakage at -10V (pA)**	**Edge BDV (V)**
30 PPM B+	1	9.8	>100	13	>100
	3	8.8	94	13	89
	5	7.6	99	7.0	95
	14	9.4	73	4.9	71
	25	18	73	19	71
	27	2.7	50	7.8	50
60 PPM B+	1	8.9	40	10	42
	3	1.1	65	1.3	64
	5	1.5	70	1.4	68
	14	1.0	66	0.8	65
	25	1.1	72	2.5	61
	27	3.8	66	7.5	65
120 B+	PPM 1	2.6	97	2.2	
	3	1.7	86	1.3	84
	5	2.4	69	3.8	68
	14	broken			
	25	4.7	67	5.4	65
	27	3.0	>100	3.7	>100
250 B+	PPM 1	8.6	>100	11	
	3	3.6	69	1.9	67
	5	9.7	>100	7.5	>100
	14	10	>100	10	>100
	25	19	75	25	71
	27	1.3	61	1.3	45
1.0% Injection BN	H	s8	d2	u	s0
	3	9.0	42	14	42
	5	12	56	11	47
	10	6.4	65	5.3	61
	18	6.1	49	5.6	42
	20	10	68	2.1	64
1.5% H_2 Injection BN	1	6.2	49	49	51
	3	9.2	47	8.9	46
	5	7.3	62	11	62
	10	10	68	9.7	69
	18	8.9	49	9.4	52
	20	9.3	61	13	60
BF2 Implant Wafers	1	0.6	50	0.8	49
	2	0.6	44	0.8	44
	3	39	42	46	41
	4	1.3	56	1.5	52
	5	0.9	37	1.0	36
	6	1.0	56	1.0	52

Appendix 10

Junction Depth Measurements (All measurements in micrometers)				
		X_j		X_j
Sample # (Patterned/Unpatterned)	Process	Lapping and Staining* Patterned	Unpatterned	Spreading Resistance Unpatterned
RM25/RM12	N_2/O_2 B+	0.31	0.64	-
RA14/RM11	Dry B+	0.44, 0.47	0.61, 0.63	0.42
RB14/RM1	Dry B+	0.47	0.55	0.40
RC14/RM5	4 ppm	0.43	0.53, 0.55	0.40
RG14	8 ppm	0.45	-	-
RH14/RH20	15 ppm	0.41	0.55	0.39
RI14/RI10	30 ppm	0.41	0.41, 0.44	-
RJ14/RJ20	60 ppm	0.48, 0.50	0.48	0.31
RL5/RL20	120 ppm	0.49, 0.51	0.44	-
RM14/RM10	250 ppm	0.54	0.51	-
RD10/RM6	BN	0.43	0.54	-
RE10/RM4	BN	0.45, 0.46	0.55	0.32
RK5	II	0.32, 0.33	-	-
RK1	II	0.35	-	-

*Two measurements indicate two separate lappings.

Appendix 11

Defect Densities on Patterned Wafers			
Sample	Process	Dislocation Pits/cm²	
		Sirtl Etch 2 min.	Wright-Jenkins Etch 1 min.
RM25	N_2O_2 B+	< 10	4
RA14	Dry B+	6.25×10^5	3.23×10^5
RB14	Dry B+	2.86×10^6	2.04×10^6
RC14	4 ppm	< 10	< 10
RG14	8 ppm	1.38×10^6	1.09×10^6
RH14	15 ppm	1.05×10^6	7.83×10^5
RI14	30 ppm	2.55×10^5	3.27×10^5
RJ14	60 ppm	< 10	2.69×10^5
RL5	120 ppm	< 10	< 10
RM14	250 ppm	< 10	1.45×10^6
RD10	BN	< 10	< 10
RE10	BN	< 10	8.26×10^4
RK5	II	< 10	< 10

Sirtl Etch:
1 part concentrated HF
1 part CrO_3 5M solution (50 g CrO_3/100 ml H_2O)

Wright Etch:
2 parts concentrated HF
2 parts concentrated acetic acid
1 part concentrated nitric acid
1 part CrO_3 5 M solution
2 g $Cu(NO_3)_2$ $3H_2O$ (reagent grade)