WIDE-BAND, LOW-NOISE, MATCHED IMPEDANCE AMPLIFIERS IN SUBMICRON MOS TECHNOLOGY

by

Kai-Yap Toh

Memorandum No. UCB/ERL M86/78

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Kai-Yap Toh

Ph.D.

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and Computer Sciences

Signature: Robert G Meyer
(Prof. Robert G. Meyer)
Chairman of Committee

ABSTRACT

This thesis describes research into circuit design techniques for realizing wide-band, low-noise, matched impedance amplifiers in submicron MOS technology, and to identify process and device parameters that determine the optimized submicron MOS technology suitable for both high-speed digital and analog applications.

A new circuit configuration with multiple feedback loops has been synthesized and fabricated in a 1μm NMOS technology. The fabricated amplifier has an insertion gain of 16.35 db, a -3 db bandwidth of 758 MHz, a maximum input VSWR of 2.45, a maximum output VSWR of 1.60 and an average noise figure of 6.7 db (with reference to 50Ω source resistance) from 10 MHz to 758 MHz. The measured results were found to agree closely with computer simulations within the -3 db frequency band. With improved process control, computer simulations indicate that a bandwidth in excess of 1 GHz is possible with this 1μm NMOS technology.

The design techniques used could also be applied directly to any submicron MOS or GaAs MESFET/HEMT technologies.

ACKNOWLEDGEMENTS

I wish to express my sincere gratitude to my research advisor, Professor Robert G. Meyer, for his technical guidance and financial support throughout the course of this Ph.D. thesis work. I am also indebted to the High Speed Electronics Research Dept.(11365) of AT&T Bell Laboratories in Holmdel, NJ for allowing me to use their research facilities for portion of this work. A special thank to all members of Dept. 11365, particularly, Dr. P.K. Tien, Dr. David C. Soo, Mr. G.M. Chin, Dr. Alex M. Voshchenkov for their professional advice and encouragement. I also wish to thank Professor P.K. Ko for his advice in the area of device physics, advanced MOS technology and short channel MOS device characterizations, and the Microwave Semiconductor Div. of Hewlett Packard Co. in San Jose, Ca. for the use of their microwave measurement equipment.

I would like to acknowledge the assistance of Mr. Gino Addiego for proof reading my thesis and the many discussions and friendships afforded by my fellow graduate students who have helped make my graduate school life an enjoyable and rewarding experience.

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CHAPTER 1

INTRODUCTION

MOS technology is the dominant IC technology for high density, low cost VLSI circuits. Device dimensions have been constantly shrunk to achieve ever higher density and higher speed. Device channel lengths have been reduced from 10μm in the early 70's down to 1.5μm in the early 80's. We are now in the era of submicron MOS technology as 1μm and 0.75μm channel length devices are being used for 1 and 4 Mbits DRAM productions [1.2], with 0.5μm MOS production technology [3] on the horizon and 0.25μm MOS technology being actively studied at various R&D establishments [4].

The main driving force of submicron MOS technology is digital VLSI. However, as speed and circuit complexity increase, it becomes desirable to incorporate high-frequency analog front-end amplifiers and output drivers on chip, such as in high-speed fiber optic communication circuits. In the SSI/MSI domain, submicron MOS devices (which have high f_T) are a potential contender for microwave IC applications, such as wide-band amplifiers in the GHz range. A brief survey of the current state-of-the-art in wide-band amplifiers in the literature and commercial market is illustrated in Fig. 1.1. As can be seen, the dominant technologies are BJT and GaAs MESFET/HEMT. None is in MOS technology. Obviously, there are problems associated with applying submicron MOS technology in such applications, despite the high f_T of the devices. In general, submicron MOS devices have low device gain, high device output conductance, high device noise characteristics, high gate and parasitic capacitance, which make such design difficult.

The purpose of this thesis is to investigate circuit design techniques that achieve wide-band, low-noise, matched impedance amplifiers in submicron MOS technologies and to identify process and device parameters that must be improved to achieve an optimized submicron MOS technology suitable for both high speed digital and analog applications. As a test vehicle, a 50Ω matched impedance wide-band amplifier was fabricated in a 1μm

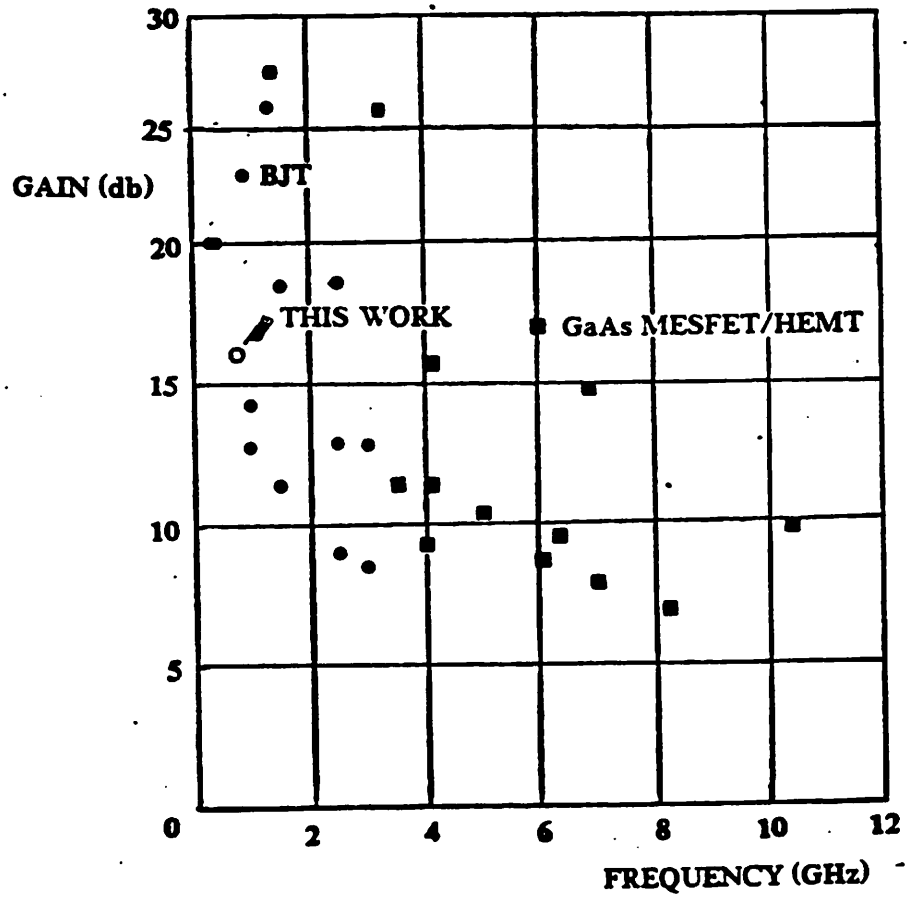


Fig.1.1 State-of-the-art in wide-band amplifiers

NMOS technology (SIGMOS*) to demonstrate the feasibility of the new design approach. Extension of these design techniques for an on-chip front end amplifier with 50Ω input impedance will be discussed. The design techniques used can also be extended to any submicron MOS or GaAs MESFET/HEMT technologies.

In chapter 2, submicron MOS device characteristics are discussed. Detailed information of the SIGMOS technology and process enhancements developed for this project are described. Measured device characteristics, including 1/f noise characteristics, are included. SPICE MOS level 3 device model parameters used in numerical examples throughout this

*SIGMOS stands for Silicon Gigabit MOS and is a 1μm NMOS research process of AT&T Bell Laboratories.

thesis are tabulated for reference. In chapter 3, the basic design issues related to MOS device in wide-band amplifier design are discussed, particularly the circuit noise and high-frequency impedance matching. In chapter 4, new design techniques for achieving wide-band, low-noise, matched impedance MOS amplifier in short-channel MOS technology are described. The proposed test circuit is analyzed and simulated. In chapter 5, measured amplifier performances are reported and discussed. In chapter 6, amplifier performance and the important process and device parameters that must be optimized for high-frequency analog and high-speed digital applications are summarized.

Important information and experimental data not directly related to circuit design issues are included in Appendix A to E. Appendix A outlines the process flow of the SIG-MOS technology and the design rules used in this project. Appendix B outlines the 2nd level metal process developed for the SIGMOS process. Appendix C described the electrical characteristics of the nitride capacitor. Appendix D is a brief introduction to short channel MOS device characteristics based on a set of simplified assumptions. Appendix E describes the 1/f noise measurement set-up and 1/f noise model parameter extraction procedures for SPICE circuit simulations.

CHAPTER 2

SIGMOS TECHNOLOGY AND DEVICE CHARACTERISTICS

2.1. Introduction

SIGMOS technology is a NMOS research process of AT&T Bell Laboratories at Holmdel, New Jersey. The test circuit described in this thesis was fabricated using this process. Information regarding SIGMOS technology can be found in [5]. A new set of relaxed design rules is used for this project as compared with that used in [6]. However, the nominal device effective channel length remains at 1μm. For easy reference, the process flow and design rules used are outlined in Appendix A. This chapter highlights the features which make the SIGMOS process suitable for high-frequency applications (besides short channel length), its limitations, and process enhancements developed specifically for this work. Measured device characteristics, including device noise characteristics, are examined. Device model parameters for circuit design considerations and for SPICE simulations are extracted and tabulated.

2.2. SIGMOS Technology and Process Enhancement

A cross-section of a SIGMOS device structure is shown in Fig. 2.2.1. Nominal device effective channel length is 1μm. Nominal gate oxide thickness is 200Å and the gate material is n^+ polysilicon. Nominal threshold voltages of the enhancement and depletion NMOS devices are 1.0 and -1.5V respectively, with -5V substrate bias. There are two features that make this particular technology suitable for high-frequency applications:

(1) sidewall oxide of the polysilicon gate which reduces overlap capacitance between gate and n^+ source/drain;

(2) the n^+ source/drain region consists of two parts: a shallow n^+ arsenic source/drain near the channel required for short channel structure and a deep n^+ phosphorus source/drain away from the channel for contact purpose. The latter has lower bottom-plate capacitance per unit area and is usually larger in area.

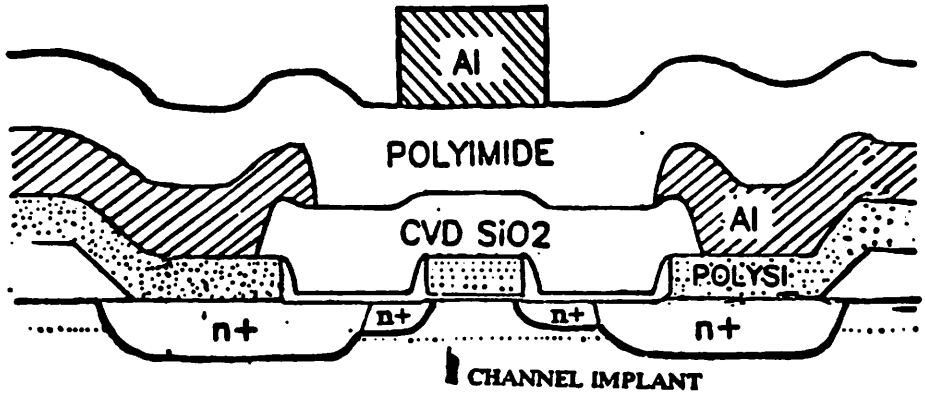


Fig. 2.2.1 SIGMOS device structure cross-section

Therefore the total n^+ source/drain to substrate capacitance at this node is reduced substantially.

The original SIGMOS process has only one layer of metal. Studies based on noise considerations and signal attenuation along a resistive gate showed that a second layer of metal was needed for low noise and high frequency applications (This will be discussed in section 2.5). A second layer metal process has thus been developed as part of this thesis work. Details of the process is outlined in Appendix B. The dielectric material used is XU284, a low curing temperature (<325°C) polyimide material. This is a spun on material and provides good planarization over steps. Both metal layers are aluminum with 1% copper. The first layer is deposited by E-gun evaporation and a resist lift-off technique is used to achieve 1.5μm line and 1.5μm space design rules. The second layer is deposited by conventional thermal evaporation and then wet etched. A relaxed 4μm line and 2μm space design rules are used. The minimum via size is 3μmx3μm. Via opening is etched in O_2 plasma with photoresist acting as an erodable mask. A tapered sidewall profile in the via is

obtained as shown in Appendix B. The second layer of metal is primarily used for power line routing in this work.

An on-chip capacitor is also added to the process for frequency compensation and for power-line decoupling. A nitride layer on top of the polysilicon layer is used as the capacitor dielectric. Field polysilicon forms the bottom plate and metal 1 forms the top plate of the capacitor. The advantage of this arrangement is that there are no additional processing complexities and thermal cycles added to the original process (except for the one extra masking step and etching required to define the top plate which are required in any process). The total nominal thickness of the nitride layer is about 700Å. The relative dielectric constant of the nitride layer is 7.5. The nitride capacitor has been characterized for leakage current and voltage coefficient and results are included in Appendix C. Leakage current is found to be less than 300 pA/cm^{-2} and voltage coefficient is less than 40 ppm/V within $\pm$ 5V operation. There is no pin hole problem with this nitride layer and the breakdown voltage is well beyond 20V.

The total number of masks used in this process, including second level metal and capacitor, is 10. It could be reduced to 9 by using a blanket threshold implant for the enhancement devices and adjusting the threshold implant dosage for the depletion devices accordingly.

2.3. Device Characteristics

There are substantial differences in the electrical characteristics between long channel and short-channel MOS devices. For easy reference, a brief introductory discussion of submicron MOS device characteristics based on a set of simplified assumptions is included in Appendix D. Although more detailed submicron device models are available on circuit simulators, such as SPICE2 (MOS Level 3 model or BSIM) [7, 8], they tend to need a large number of model parameters and do not lend themselves directly to the physical understanding of device behavior and their relationships to ac parameters for circuit design. The "first order" model described in Appendix D shows clearly the various short-channel

device effects in relation to various physical variables. The model can predict device behavior within ±25% of measured characteristics in most cases.

In this section, only the measured SIGMOS device characteristics are discussed. Data shown was taken from the actual process run in which the test circuit was made. It should be pointed out that this particular process run had problems with the ion implanter, contact oxide etch and no sputtering etch (equipment not available) for cleaning the via before metal 2 deposition. The consequences are:

(1) the threshold voltages of both the enhancement and depletion devices are out of the normal spread of values and both device types have lower r_{ds};

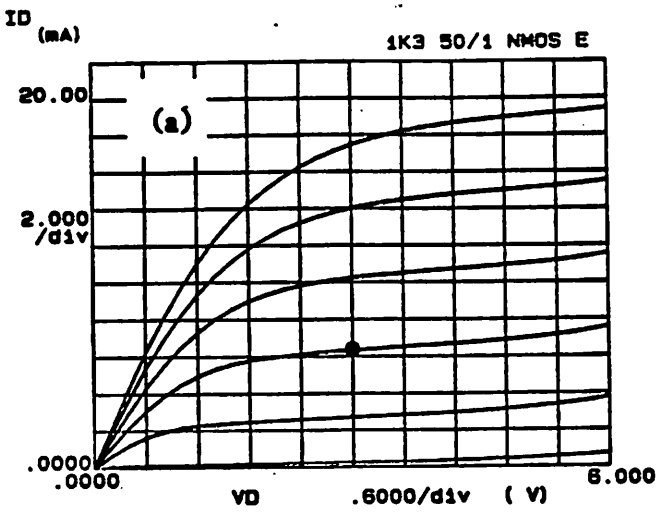
(2) the depletion device has an unintended buried channel and has much lower r_{ds}, resulting in low device gain;

(3) the capacitor dielectric has been thinned down giving a larger compensation capacitance value which reduces the bandwidth of the amplifier;

(4) contact resistance between the two layers of metal is high and not consistent, causing high source resistance which resulted in a lower effective device g_m and poor matching between devices.

Device characteristics are thus degraded significantly and the circuit did not perform as well as expected with an optimum process.

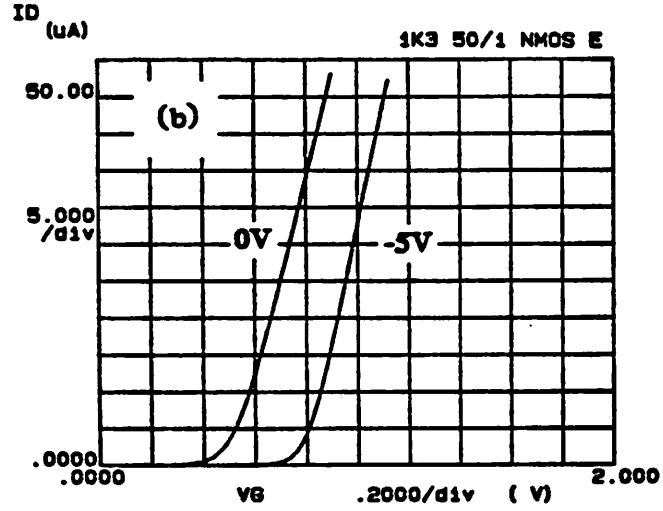
The device characteristics of the enhancement mode SIGMOS device are shown in Fig. 2.3.1(a) to (c). The device has $W = 50\,\mu m$ and $L_{eff} = 1\mu m$. Measurements are taken with the HP4145A Semiconductor Parameter Analyzer. Fig. 2.3.1(a) shows the I-V characteristics and Fig. 2.3.1(b) shows the I_D vs. V_{GS} at low V_{DS} (50mV) for $V_{SUB} = 0V$ and $-5V$. The threshold voltage of the device can be determined by the intercept of the slope at the V_{GS} axis since the I_D equation in the ohmic region is linear. The slope of the line is related to μ_{eff} as discussed in Appendix D and repeated here for convenience:



Variable1:
VD -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .2000V

Variable2:
VG -Ch4
Start 1.0000V
Stop 6.0000V
Step 1.0000V

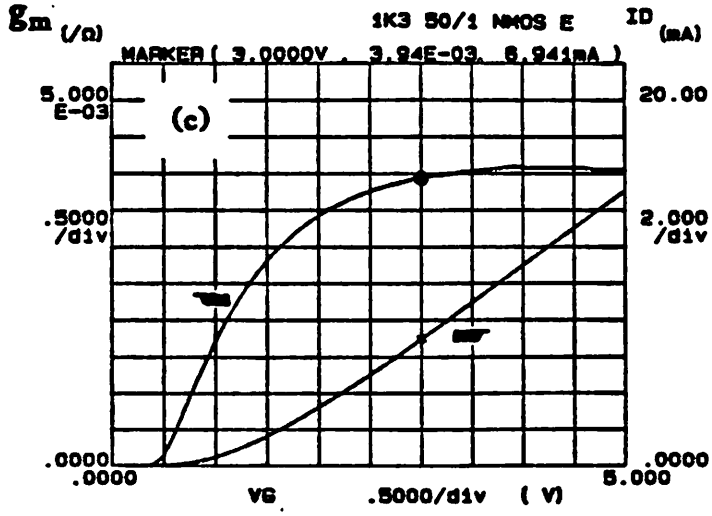
Constants:
VS -Ch2 .0000V
VSUB -Ch3 -5.0000V



Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 1.2000V
Step .0200V

Variable2:
VSUB -Ch3
Start .0000V
Stop -5.0000V
Step -5.0000V

Constants:
VD -Ch1 .0500V
VS -Ch2 .0000V
Vi -Vsi .0000V



Variable1:
VG -Ch4
Linear sweep
Start -2.0000V
Stop 3.0000V
Step .1000V

Variable2:
VD -Ch1
Start 5.0000V
Stop 5.0000V
Step .5000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 -5.0000V

Fig.2.3.1 Enhancement mode SIGMOS device characteristics, W=50μ, L_{eff} = 1μ
(a) I-V characterisaics
(b) I_D vs. V_{GS} at V_{DS} = 50 mV, for V_{SUB} = 0V and −5V
(c) g_m and I_D vs. V_{GS} at V_{DS} = 5V

$$I_D \approx \frac{\mu_{eff} C_{ox} W}{L}(V_{GS} - V_T)V_{DS} \quad \text{at very low } V_{DS} \tag{2.3.1}$$

$$\mu_{eff} \approx \frac{slope * L}{C_{ox} W V_{DS}} \tag{2.3.2}$$

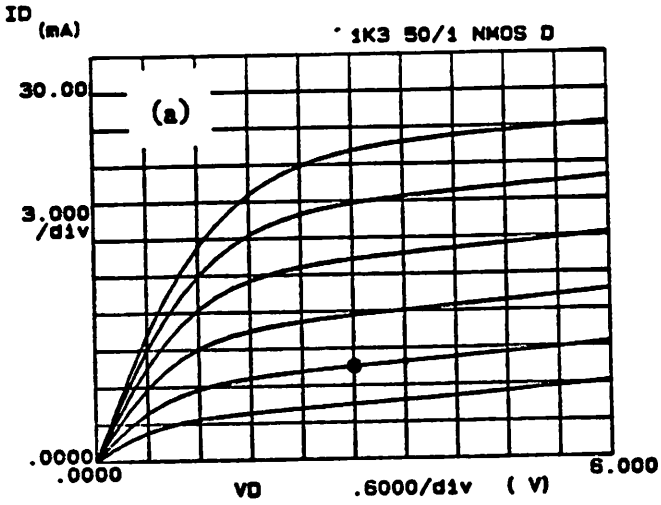
From the data shown, $V_T = 0.8V$ with -5V substrate bias and $\mu_{eff} = 371\ cm^2/V\text{-}s$. Fig.2.3.1(c) shows the g_m and I_D vs. V_{GS} characteristics at $V_{DS} = 5V$. Note that g_m becomes constant and I_D becomes linearly dependent on V_{GS} at high V_{GS} when carrier velocity saturates as discussed in Appendix D. As shown, $g_{m,max}/W$ is 84 mS/mm. At the bias point shown (dot), g_m/W is $79mS/mm$ and r_o x W is 135 $K\Omega$-μm.

The corresponding set of curves for a depletion device are shown in Fig.2.3.2(a) to (c). Note that in Fig.2.3.2(b), the device cannot be turned off at $V_{SUB} = 0V$ and that there are two slopes at $V_{SUB} = -5V$, indicating an unintended buried channel exists at low gate voltage. The effective threshold voltage at $V_{GS} = 0$ is -2.3V. g_m/W at the bias point is $75mS/mm$. The I-V characteristics of a depletion mode device connected as a depletion load is shown in Fig. 2.3.3. The equivalent resistance at the bias point shown is about 67 $K\Omega$-μm. The stage gain of an inverter shown in Fig. 2.3.4 with W_e:W_d = 1:1 is therefore only 3.5 instead of 4.6 expected from a normal run.

For circuit simulations, SPICE version 2G.6 MOS level 3 device model is used. The model parameters and comparison of simulated and measured I-V characteristics are discussed in section 2.6.

2.4. Noise Characteristics

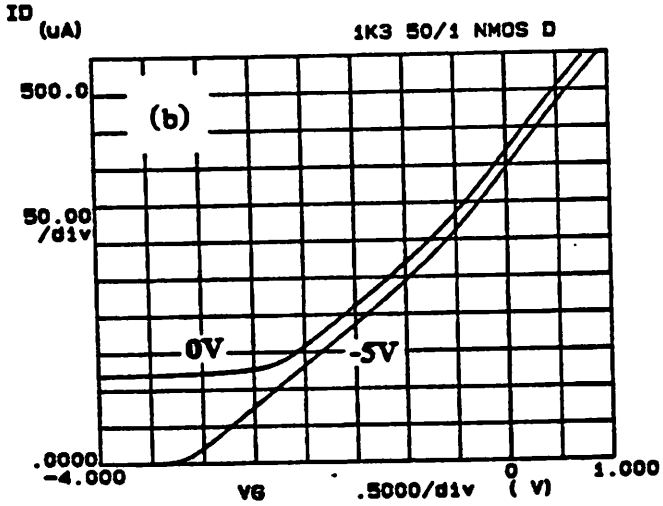
The noise performance of a wide-band amplifier is an important design consideration. Both $1/f$ device noise and high-frequency device noise have to be considered in most wide-band amplifier designs. Unfortunately, there is limited information available on short-channel MOS device noise characteristics in the literature [9, 10]. However, accurate circuit noise simulations can be obtained if device noise are characterized at the same bias point where the device will operate in the circuit. using this technique, a straight forward method of extracting the $1/f$ noise model parameters for SPICE 2G.6 is developed and



Variable1:
VD -Ch1
Linear sweep
Start .0000V
Stop 6.0000V
Step .2000V

Variable2:
VG -Ch4
Start -1.0000V
Stop 4.0000V
Step 1.0000V

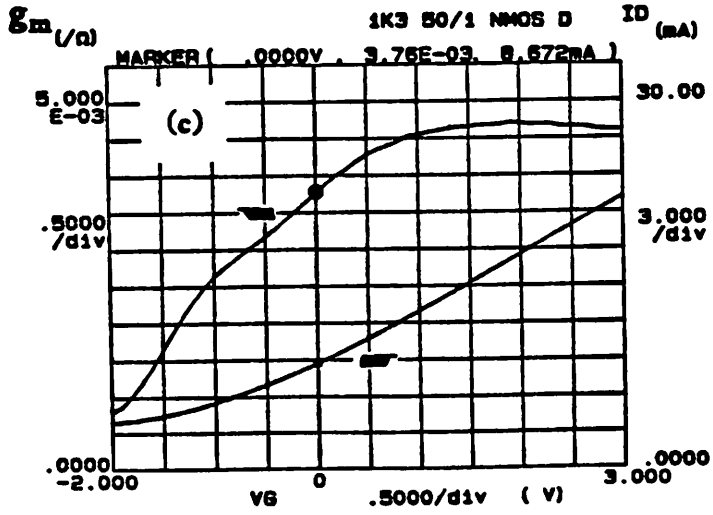
Constants:
VS -Ch2 .0000V
VSUB -Ch3 -5.0000V



Variable1:
VG -Ch4
Linear sweep
Start -4.0000V
Stop 1.0000V
Step .0500V

Variable2:
VSUB -Ch3
Start .0000V
Stop -5.0000V
Step -5.0000V

Constants:
VD -Ch1 .0500V
VS -Ch2 .0000V
Vi -Vs1 .0000V



Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 5.0000V
Step .1000V

Variable2:
VD -Ch1
Start 6.0000V
Stop 6.0000V
Step 1.0000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 -5.0000V

Fig.2.3.2 Depletion mode SIGMOS device characteristics, W=50μ, $L_{eff} = 1\mu$
(a) I-V characterisaics
(b) I_D vs. V_{GS} at V_{DS} = 50 mV for V_{SUB} = 0V and −5V
(c) g_m and I_D vs. V_{GS} at V_{DS} = 5V

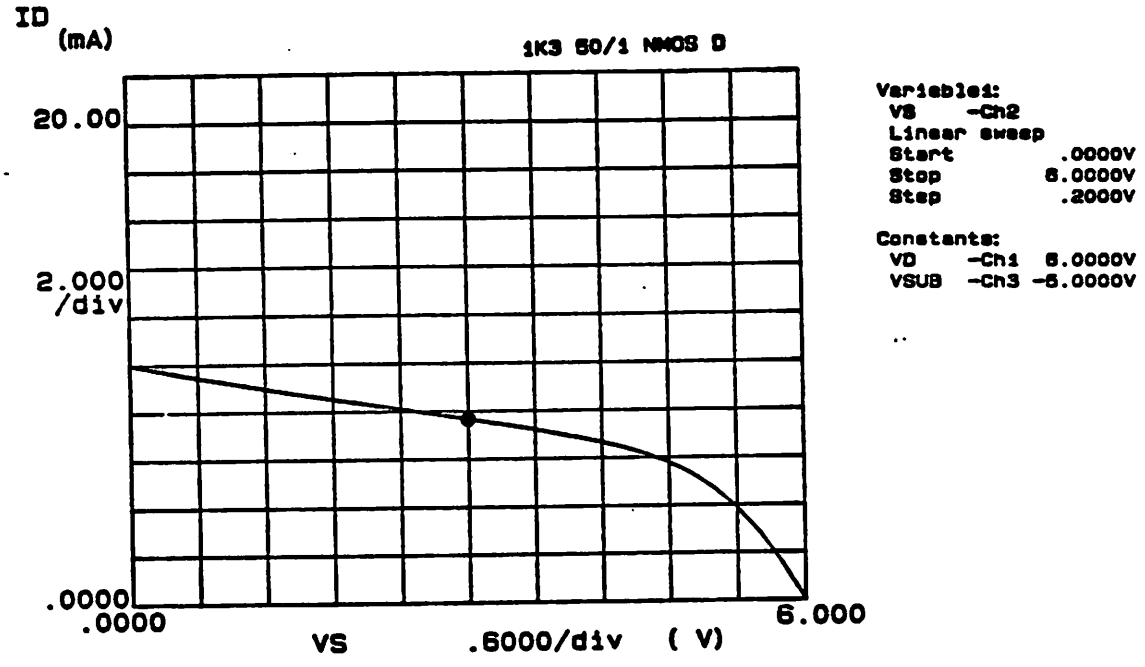


Fig.2.3.3 I-V characteristic of a depletion load in SIGMOS technology, W=50μ, L_{eff} = 1μ

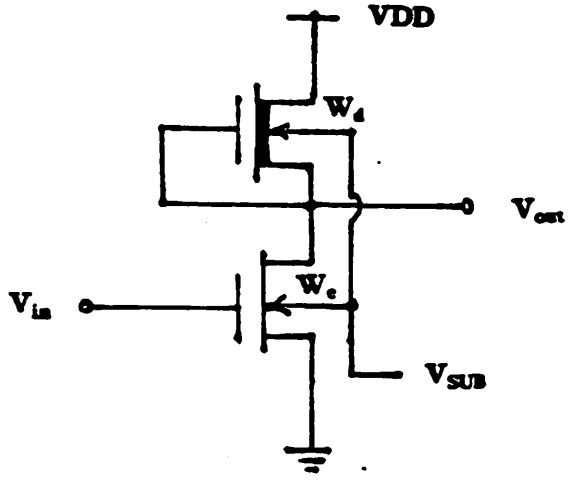


Fig. 2.3.4 Depletion load inverter

described in Appendix E. There is good correlation between the measured and simulated amplifier noise performance using this method (Chapter 6).

The basic MOS device noise sources are shown in Fig.2.4.1(a) and (b) [11]. Fig.2.4.1(a) shows the gate current noise source, $\overline{i_{gn}^2}$, and the drain current noise source, $\overline{i_{dn}^2}$. Where,

$$\frac{\overline{i_{gn}^2}}{\Delta f} = 2qI_g \tag{2.4.1}$$

$$\frac{\overline{i_{dn}^2}}{\Delta f} = 4kT\Gamma g_m + \frac{K_n}{f} \quad \text{where} \quad K_n = \frac{K_F I_D^{A_F}}{C_{ox} L^2} \tag{2.4.2}$$

This is the basic model used in SPICE for MOS circuit noise simulations. In practice, the gate current I_g of MOS device is small so that $\overline{i_{gn}^2}$ can be ignored. Γ is 2/3 for long channel MOS devices and had been reported to be 1.03 for a short channel MOS device [12]. The origin for the high Γ is not clear and is generally ascribed to high-field effects in the channel [13]. It may also be partly due to contributions from gate resistance and/or process dependency. In circuit simulations, gate resistances, parasitic source/drain resistances and contact resistances are all included explicitly for circuit simulations. The factor 2/3 is used in SPICE and the fact that there is good correlation between the measured and simulated amplifier noise characteristics (Chapter 6) indicates that Γ is close to 2/3 for the 1μm SIGMOS devices. For design considerations, the drain-current noise source is most often referred to the input and represented by an equivalent input noise voltage, $\overline{v_{i,eq}^2}$ and current sources, $\overline{i_{i,eq}^2}$ as shown in Fig.2.4.1(b), where.

$$\frac{\overline{v_{i,eq}^2}}{\Delta f} = \frac{1}{g_m^2}\frac{\overline{i_{dn}^2}}{\Delta f} = \frac{4kT\Gamma}{g_m} + \frac{K_n}{g_m^2}\frac{1}{f} \tag{2.4.3}$$

$$\frac{\overline{i_{i,eq}^2}}{\Delta f} = \overline{i_{dn}^2}\left(\frac{sC_g + sC_{gdov}}{g_m}\right)^2 \approx 4kT\Gamma g_m \left(\frac{f}{f_T}\right)^2 \tag{2.4.4}$$

From Eqn 2.4.4, it is seen that at very high-frequency, the noise level will increase as f^2. However, it may be ignored when $f \ll f_T$, especially when the impedance level in the input circuit loop is low. This is the case for the types of circuit under study and is

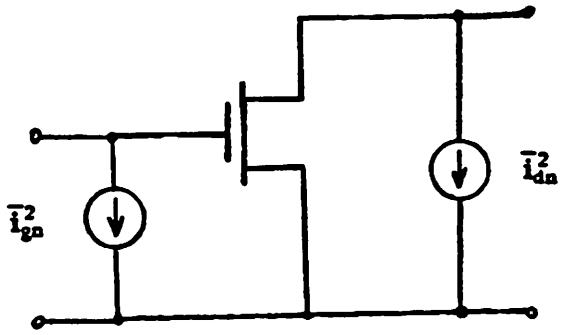


Fig.2.4.1(a) MOS device current noise sources: gate current noise source, $\overline{i}^2_{gn}$ and drain current noise source, $\overline{i}^2_{dn}$

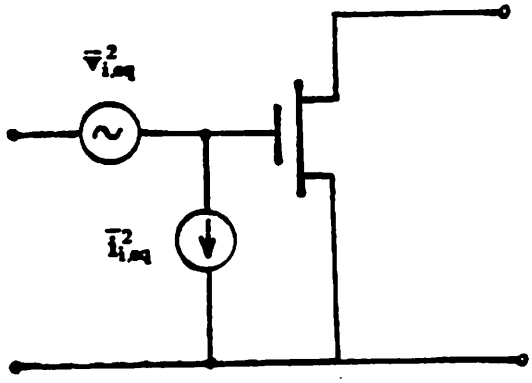


Fig.2.4.1(b) Equivalent input noise sources: input equivalent noise sources, $\overline{v}^2_{i,eq}$ and $\overline{i}^2_{i,eq}$

therefore ignored. Only $\bar{v}_{i,eq}^2$ is considered for subsequent discussions. From Eqn. 2.4.3, $\bar{v}_{i,eq}^2$ can be reduced by increasing device size (W), as g_m is directly proportional to W.

For MOS device using polysilicon gate process, where gate resistance R_G can be significant, noise contribution from R_G should be added to Eqn.2.4.3. So that in general,

$$\frac{\bar{v}_{i,eq}^2}{\Delta f} = 4kTR_G + \frac{4kT\Gamma}{g_m} + \frac{K_n}{g_m^2}\frac{1}{f} \tag{2.4.5}$$

In the test circuit, all devices are biased at $\frac{1}{2}VDD$ and all should have the same K_n. The value of K_n can be obtained from the slope of the low-frequency device noise measurements at the same bias condition as described in Appendix E. Then for SPICE simulation purpose, one may assume $A_F = 1$ and K_F can be derived by equating the $1/f$ noise coefficients shown in Eqn. 2.4.2.

Device $1/f$ noise was measured with an HP8566A Spectrum Analyzer in the range from 1 KHz to 10 MHz. A typical low-frequency device noise measurement result is shown in Fig.2.4.2. The estimated $1/f$ noise corner frequency for the test device used is about 30 MHz. Following the procedures outlined in Appendix E and setting $A_F = 1$.

$$K_F = 8*10^{-28}\,(F-A) \tag{2.4.6}$$

For design purposes, high-frequency noise will consist of mainly the gate resistance noise and channel thermal noise as given in the first two terms of Eqn. 2.4.5. Note that for a MOS device,

$$R_G \approx \frac{W}{L} R_{\square poly} \tag{2.4.7}$$

where $R_{\square poly}$ is the sheet resistance of the gate poly. Clearly, to minimize amplifier noise, R_G must be minimized and W should be large. This apparent conflict can be resolved by connecting small segments of devices together in parallel to form the required device size, W. The optimum segment width to be used will be analyzed in the next section.

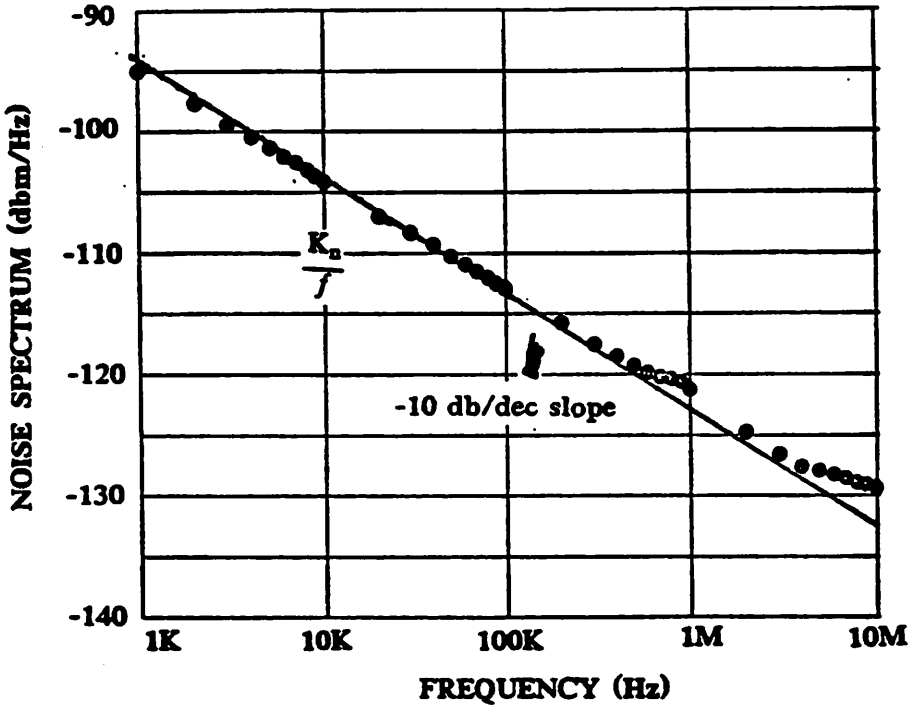


Fig. 2.4.2 1/f noise characteristics of a 1μ SIGMOS enhancement device

2.5. Optimum Gate Width

From the previous section, it is evident that for low amplifier noise, a large W is at least required for the input device. (Input high frequency matching limits the input device size to $\leqslant 1000\mu m$, as will be discussed in section 3.4.) In a n+ polysilicon gate process, a single long gate width will have large resistance which contributes significant input noise (this is in analogy to the base resistance of a BJT). In addition, the distributed nature of the gate resistance and capacitance will affect the frequency response of the circuit. It is therefore desirable to connect small segment of devices together via low resistive paths (metal lines) in parallel to form the required large W device. On the other hand, too small a segment will increase the total source/drain junction sidewall capacitance due to increase perimeter which will degrade high-frequency performance. Note that one layer of metal is used for gate jumpers and output jumpers. A second layer of metal is therefore required for connecting the power lines to the sources and drains.

The distributed RC effect of a MOS device gate is illustrated in Fig.2.5.1. The segment width is w in μm. R_c is the contact resistance between the gate poly and metal 1. The specific contact resistance is about $10^{-6}\ \Omega\text{-}cm^2$. R_p is the poly resistance over the field region. The sheet resistance of polysilicon layer, $R_{\Box poly}$, is about 25 $\Omega/\Box$ (worse case). R_G is the gate resistance, and C_s is the parasitic gate capacitance over the field oxide which is negligible except in a non-practical case when $w \rightarrow 0$. R_c is estimated to be about 45 Ω and R_p is about 41 Ω for the minimum design rules in SIGMOS process tabulated in Appendix A. R_G is calculated as follow.

$$R_G \approx \frac{w}{1.3} * 25\ \Omega$$

A lumped equivalent of the distributed RC line can be approximated by a series resistance R/2.43 and a shunting C [14]. The frequency at which the amplitude of the gate signal from the far end is at -3db from that of the contact end is given by

$$f_{-3db} \approx \frac{1}{2\pi(R_G / 2.43 + 86) * 1.73 * 10^{-15} w} \qquad (2.5.2)$$

The variations of f_{-3db} with segment width w is shown in Fig. 2.5.2. As a rule of thumb, for an amplifier bandwidth of 1 GHz, one would like to have $f_{-3db} \geq 10\ GHz$, and that corresponds to a device segment width $w < 29\mu m$. For different segment widths used to achieve a 1000μm device width, the effective gate resistance is different. The variation is also shown in Fig.2.5.2, but normalized to $2/3g_m$, denoted by r_n. For a segment width of 25μm, the effective gate resistance is about 14 Ω but $2/3g_m$ is only 8.3 Ω and r_n is about 1.7. This ratio is high for low-noise application. A segment width of 12.5μm is therefore preferred. r_n in this case is about 0.5. The optimum segment width is therefore determined by noise considerations.

It is interesting to apply the same analysis to a silicide gate process (including polycide gate process). The sheet resistance and contact resistance to metal in these process are typically an order of magnitude lower than that of the polysilicon gate process [15]. The variations of f_{-3db} and r_n for both the poly gate and silicide gate processes are shown in

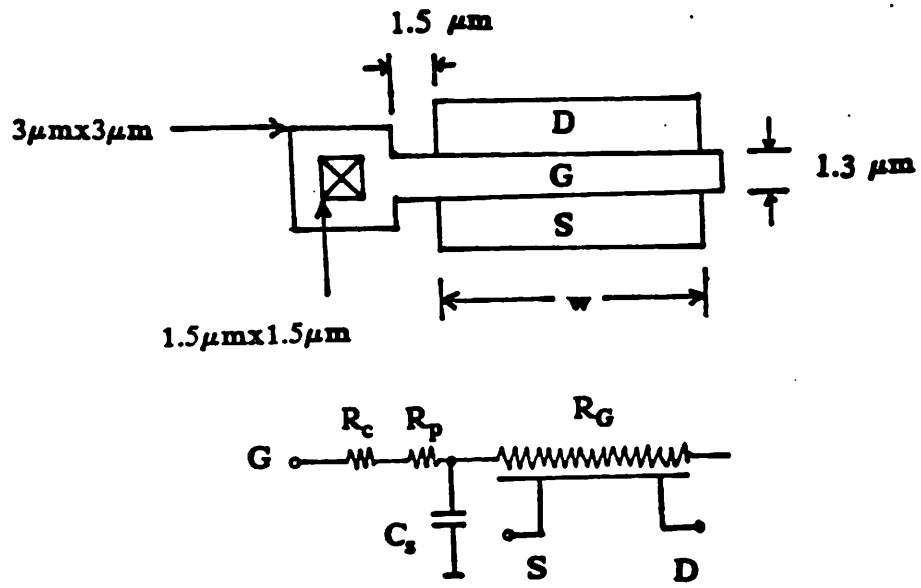


Fig.2.5.1 Top view of polysilicon gate MOS device and equivalent circuit

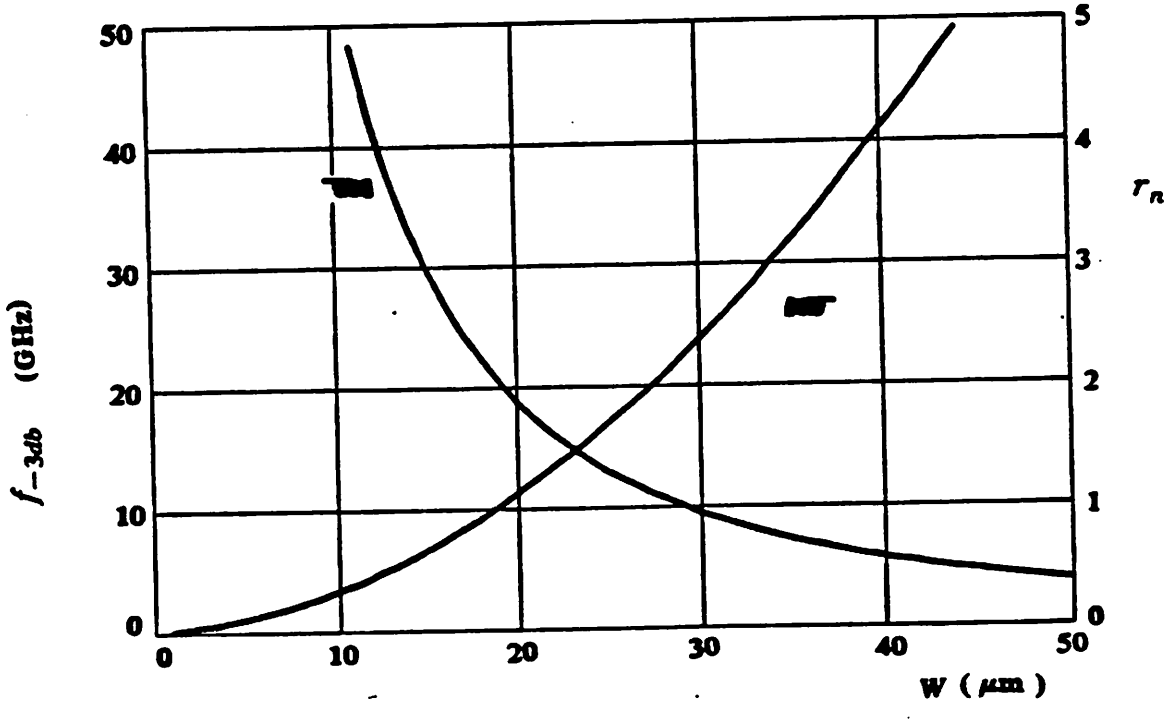


Fig.2.5.2 f_{-3db} and r_n vs. gate width

Fig. 2.5.3. For a silicide gate process, r_n for the same segment width (roughly same frequency performance) is 10 times lower. Thus at $w = 25\mu m$, $r_n = 0.17$. R_G no longer dominates the input noise. The segment width may be extended to 45μm for $r_n = 0.5$. The trade off is between noise performance and bandwidth. The use of refractory metal as the gate material will further reduce the gate resistance but at the expense of cost and process complexity.

2.6. SPICE 2G.6 MOS Model Level 3 Parameters

Two sets of SPICE model parameters, as shown in Table 2.6.1, are used in this thesis. Set A are the parameters for the normal device characteristics expected and are used in the early stage of this work for design considerations. The bias point is at $V_{GS} = 2.5V$ and $V_{DS} = 2.5V$. Set B are the parameters for the actual fabricated devices discussed in section 2.3 and are used to compared the simulated and measured amplifier performance. The bias

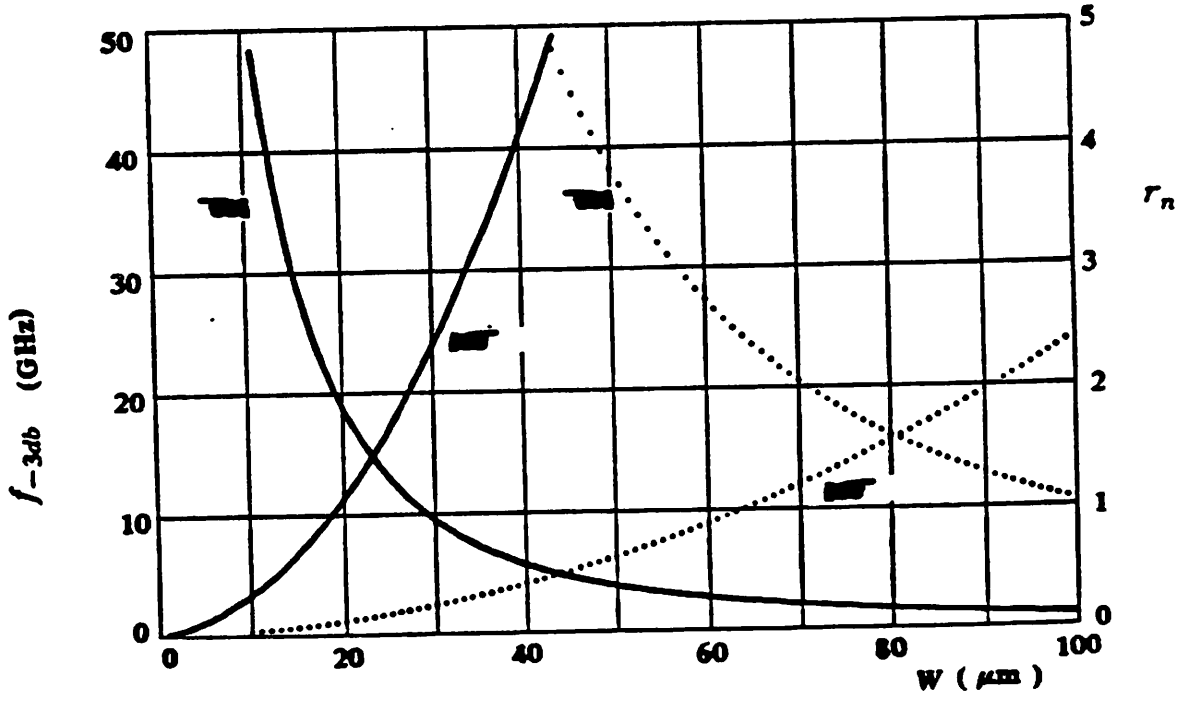


Fig.2.5.3 f_{-3db} and r_n vs. gate width for both polysilicon gate (solid) and silicide gate (dotted) processes.

Parameters	Set A Nominal		Set B Lot 1K3	
Type	Enhancement	Depletion	Enhancement	Depletion
Level	3	3	3	3
VTO	0.75	-1.75	0.56	-2.5
GAMMA	0.3	0.3	0.235	0.235
CGSO	2.50e-10	2.50e-10	2.50e-10	2.50e-10
CGDO	4.20e-10	4.20e-10	4.20e-10	4.20e-10
CGBO	1.38e-10	1.38e-10	1.38e-10	1.28e-10
RSH	0.0	0.0	0.0	0.0
CJ	2.73e-4	2.73e-4	2.73e-4	2.73e-4
CJSW	9.00e-10	9.00e-10	9.00e-10	9.00e-10
TOX	2.00e-8	2.00e-8	2.00e-8	2.00e-8
NSUB	2.00e16	2.00e16	2.00e16	2.00e16
NFS	1.00e10	1.00e10	1.00e10	1.00e10
TPG	1.0	1.0	1.0	1.0
XJ	3.00e-7	3.00e-7	3.00e-7	3.00e-7
LD	1.50e-7	1.50e-7	1.50e-7	1.50e-7
UO	6.00e2	6.50e2	6.50e2	6.250e2
VMAX	2.00e5	2.50e5	1.750e5	1.80e5
KF	8.00e-28	8.00e-28	8.00e-28	8.00e-28
AF	1.0	1.0	1.0	1.0
THETA	0.27	0.27	0.26	0.26
ETA	0.0	0.0	0.15	0.25
KAPPA	2.0	1.8	0.75	0.8
DEFL	1.25	1.25	1.3	1.3

Table 2.6.1 SPICE 2G.6 MOS level 3 model parameters

point is at $V_{GS} = 3V$. and $V_{DS} = 3V$. Due to limitations in the model. it is impossible to select a set of parameters that will agree with the measured data over the entire range. The model parameters are chosen so that there is a best fit at the bias point in terms of dc and ac parameter values. Simulated (Set B) and actual measured device I-V characteristics are shown in Fig.2.6.1(a) and (b).

The typical device parameters used for design considerations are tabulated in Table 2.6.2. The estimated nominal parameter variations with process and the measured parameter variations over temperature from 0° to 100° C are also measured and tabulated in Table 2.6.3.

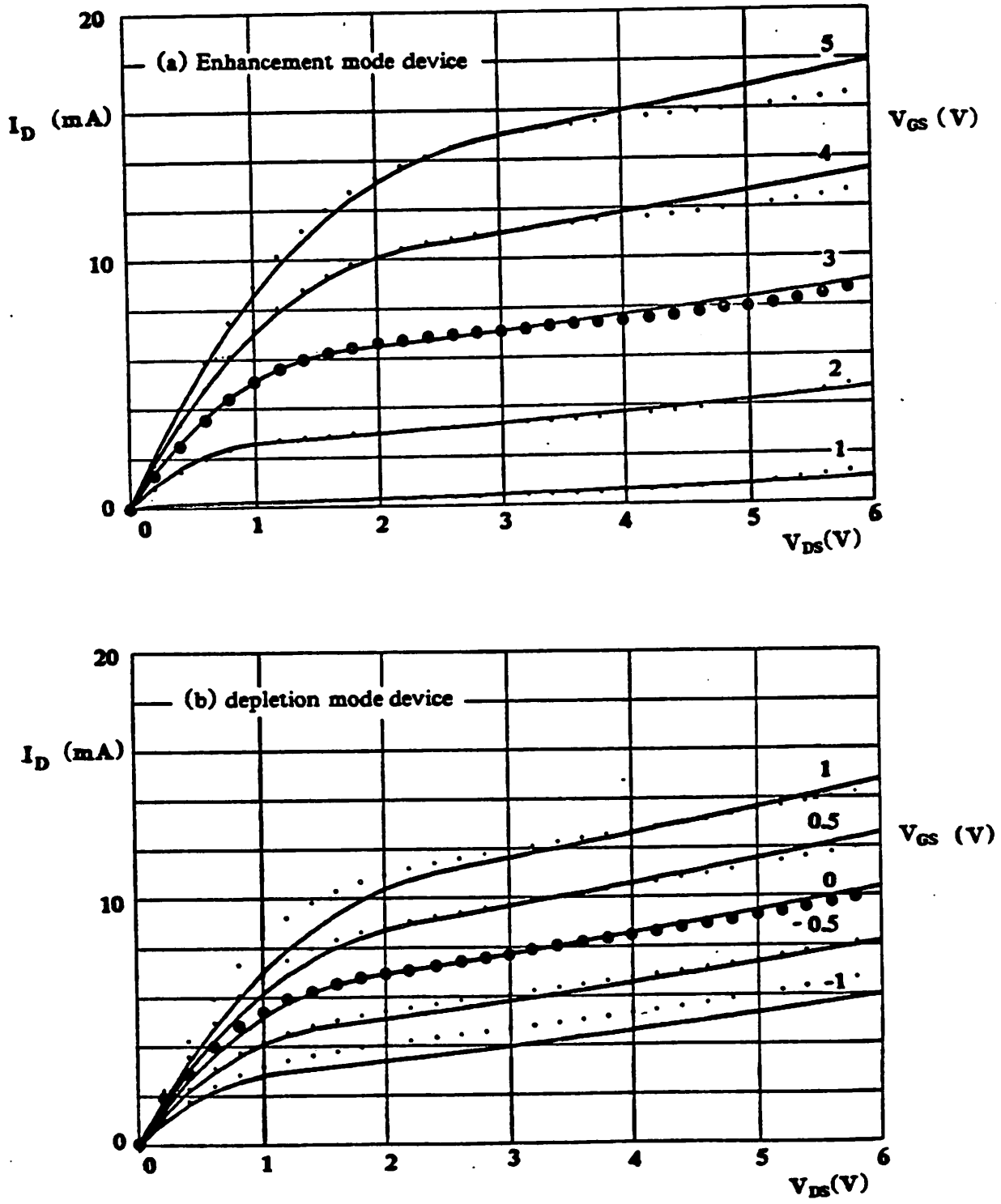


Fig. 2.6.1 Measured (dotted) and simulated (solid) device I-V characteristics. Set B parameters: (a) Enhancement, (b) Depletion.

Parameters	Typical	Conditions
V_{TE}	1.0V	at $V_{SUB} = -5V$
V_{TD}	-1.5V	at $V_{SUB} = -5V$
$g_{m,max}/W$	$88\mu S/\mu m$	at $V_{GS} - V_T = 1.5V$
g_m/W	$80\mu S/\mu m$	at $V_{GS} - V_T = 1.5V$
C_{ox}	$173nF/cm^2$	
$g_{mb}(enh.)$	$0.02g_m$	
$g_{mb}(dep.)$	$0.02g_m$	
$r_{ds}(enh.)$	160 $K\Omega/\mu m$	
$r_{ds}(dep.)$	110 $K\Omega/\mu m$	
$g_m r_{ds}(enh.)$	12.8	
$g_m r_{ds}(dep.)$	8.8	

Table 2.6.2 Device parameters

As an example, using the nominal device parameters, the f_T of the SIGMOS device can be calculated with reference to Fig. 2.6.2:

$$A_I = \frac{i_o}{i_{in}} = \frac{sC_{gd} - g_m}{s(C_{gsT} + C_{gd})} \tag{2.6.1}$$

where $C_{gsT} = C_{gs} + C_{gsov} = 0.82\, C_{ox} W$ and $C_{gd} \approx C_{gdov} = 0.15\, C_{ox} W$

thus for $|A_I| = 1$, $f_T = 7.6$ GHz

This is an impressive figure. As f_T is rougly inversely proportional to L for short channel devices, the f_T of a 0.5μm device will be about 15 GHz. It should be noted that althought the f_T of the device is high, the useful frequency of a MOS device can be reduced significantly with increased output capacitive load due to its own parasitic capacitance

Parameter	Process	temperature
g_m	±10%	±20% decreases as temperature increases
r_{ds}	±10%	±10% increases as temperature increases
$g_m r_{ds}$	±10%	±10%

Table 2.6.3 Parameter variations with process and temperature

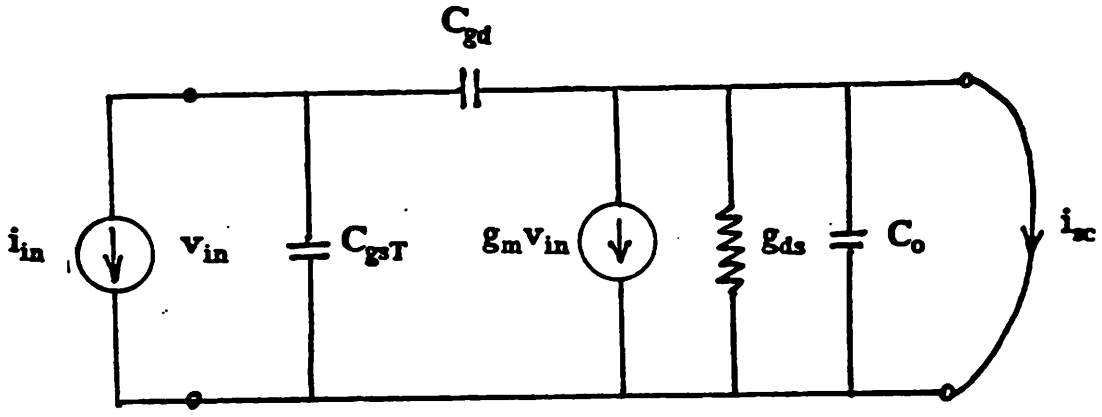


Fig. 2.6.2 AC model for short circuit current gain

which will be discussed in section 3.2.

CHAPTER 3

BASIC DESIGN CONSIDERATIONS

3.1. Introduction

In this chapter, the basic design issues of wide-band, low-noise, 50Ω matched input/output impedance amplifier in MOS technology is discussed. Specifically, bandwidth shrinkage of cascading amplifying stages, evaluation of amplifier noise figure for different types of input matching configuration, and the effect of high frequency input impedance matching due to reactive components are discussed in detail. The feasibility of using short channel MOS devices in conventional feedback circuits for such application is examined. Numerical examples used throughout this chapter are based on the SIGMOS technology discussed in Chapter 2. However, similar considerations can be directly extended to any submicron NMOS/CMOS technologies or submicron GaAs MESFET/HEMT technologies, as these devices have very similar device characteristics and similar problems in regard to wide-band amplifier design.

To achieve wide bandwidth, a general rule of thumb is to keep the circuit configuration as simple as possible. In SIGMOS technology, a simple depletion load inverter shown in Fig. 2.3.4 is used as a gain stage. Input and output are biased at $\frac{1}{2}VDD$ for direct cascading and for optimum g_m/I_D ratio. This can be achieved with $W_e:W_d = 1:1$ in SIGMOS technology. The nominal gain is about 4.6 and r_o is about 60 $K\,\Omega$–μm. These values represent the low end of most state-of-the-art submicron technologies. It is therefore appropriate to use these values for discussions and extend it to cover submicron technologies without lost of generality. This is because in wide-band circuit, feedback is always used to widen the bandwidth and for impedance matching. Circuit midband performance will, in general, improve as the stage gain and loop gain are increased.

One of the main issues of using submicron MOS devices in wide-band amplifier applications is that with low amplifier open-loop gain, the achievable loop gain with feedback is

low. Conventional high gain approximations used in feedback circuit analysis are no longer accurate in determining loop gain (T) and the overall transfer function. The analysis must be carefully re-examined in order to obtain meaningful insight to the problem. A few cases of simple conventional feedback circuits will be analyzed in this chapter. Only midband frequency analyses are presented and discussed. High frequency performance is best analyzed by computer simulations due to the complexity involved. Closed form expressions for transfer functions, loop gains, input and output impedances are given. From these expressions and from the practical parameters given in section 2.6, it can be shown that the usual terms that are ignored in the high loop gain situations can contribute as much as -30 to -50%, or more in some cases, to the closed looped functional values. In such cases, one must use the exact closed loop expressions. The feedback improvement is still given by (1+T). It should be noted that although low loop gain is not desirable, it is acceptable. In fact, low loop gain is common in microwave amplifier design. Also the loop gain near the edge of the band is always low, even when the low frequency loop gain is high. It is often the performance at the edge of the band that determines the specifications of the amplifier.

3.2. Gain Bandwidth Product of Cascaded Stages

In the previous chapter, f_T of the SIGMOS device is shown to be 7.6 GHz. But, f_T is not a good indicator for the frequency limitation of a MOS circuit. Fig.3.2.1 shows a cascading of identical amplifier stages. The total capacitance at the output node, B is about $2C_{ox}WL$ for minimum design rules ($0.8C_{ox}WL$ is from the amplifier on the left and $1.2C_{ox}WL$ is from the amplifier on the right, assuming a gain of -1). The gain bandwidth product, GBW, is given by:

$$GBW = \frac{f_T}{2} = 3.6\ GHz$$

This would mean that for a stage gain of 14db, the -3db bandwidth is 760 MHz (with no impedance matching as yet and not driving any resistive load). When several of these stages are cascaded together to achieve larger gain, the bandwidth will shrink. This can be

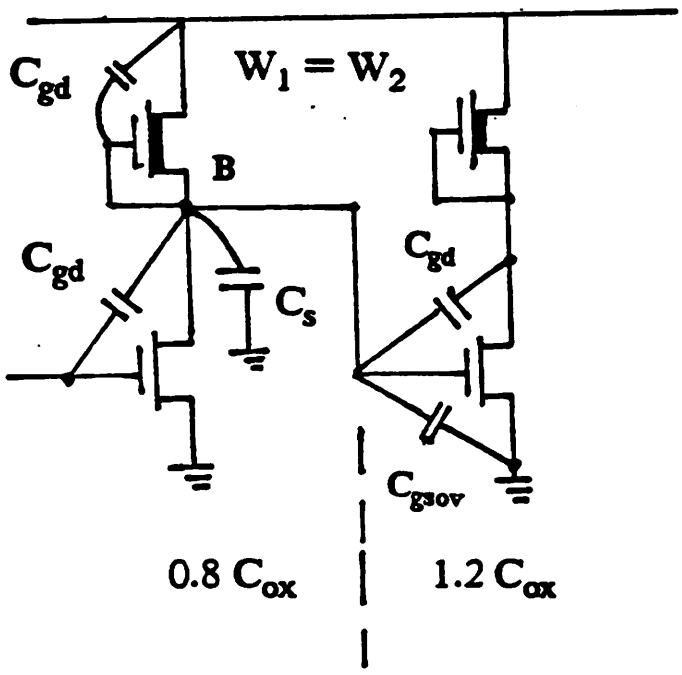


Fig. 3.2.1 Cascading of identical MOS amplifier stages

calculated by considering cascading n identical stages, each with a single dominate pole p as shown in Fig.3.2.2(a). The overall transfer function TF is given by:

$$TF = \frac{G^n}{(1 + s/p)^n} \quad \text{and the } -3\text{db bandwidth is}$$

$$BW_{-3db} = p\,[2^{1/n} - 1]^{1/2} \tag{3.2.1}$$

The shrinkage factors are tabulated in Fig.3.2.2(b). Thus, for 3 cascaded stages, the bandwidth is reduced to 387 MHz. Of course, when the cascading stages are not identical, the bandwidth can be different from that predicted above. In particular, when the following stage has smaller gate width, the -3db bandwidth can be widened. This can be used to its advantage in MOS amplifier design, particularly when the first stage normally has the largest gate width for low noise design. Other approaches are to reduce the impedance at each output node via local shunt feedback or reduce the capacitive loading effect by local series feedback. Limitation of these latter approaches will be examined in sections 3.5 and

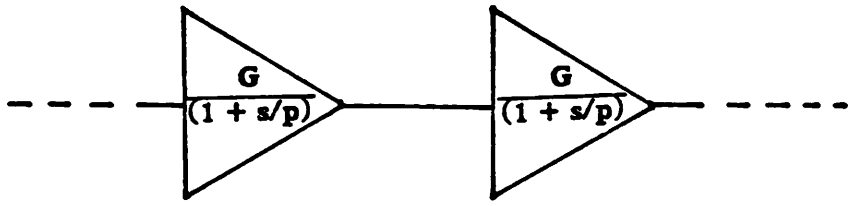


Fig. 3.2.2(a) Cascading of n identical stages

n	BW_{-3db}/p
1	1.00
2	0.64
3	0.51

Fig. 3.2.2(b) Bandwidth shrinkage for identical cascading amplifiers

3.6. Another common approach is to buffer the critical stage with a source follower as shown in Fig.3.2.3(b) (Fig. 3.2.3(a) shows two cascading stages without source follower stage for direct comparison). The idea is to reduce the capacitive loading at point B by isolating device M2 from device M1 with a source follower consisting of M3 and M4. The practical usefulness of such an approach at high frequency has been studied by computer simulations. With the gate width of each device as shown in Fig. 3.2.3. the simulated amplitude and phase responses of the amplifiers are as shown in Fig. 3.2.4(a) and (b) respectively. The amplifier with a source follower stage does have a wider -3 db bandwidth (at 1 GHz) as compared to that without a source follower stage (at 600 MHz). Although the buffered stages have lower midband gain (due to the fact that the source follower stage has a dc gain of 0.8). the high frequency gain between 600 MHz to 3 GHz is

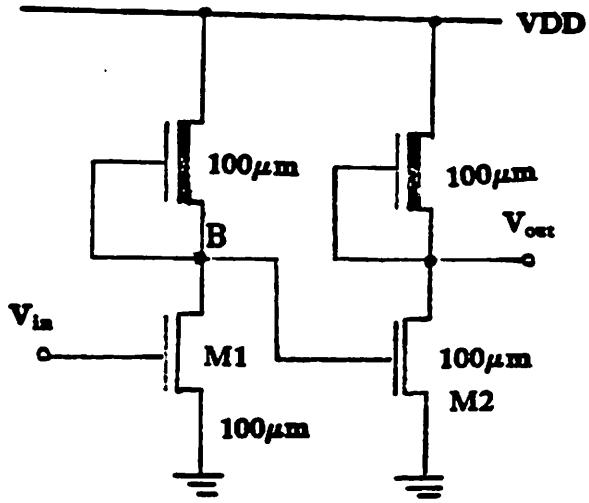


Fig. 3.2.3(a) Cascading amplilfiers without buffered stage

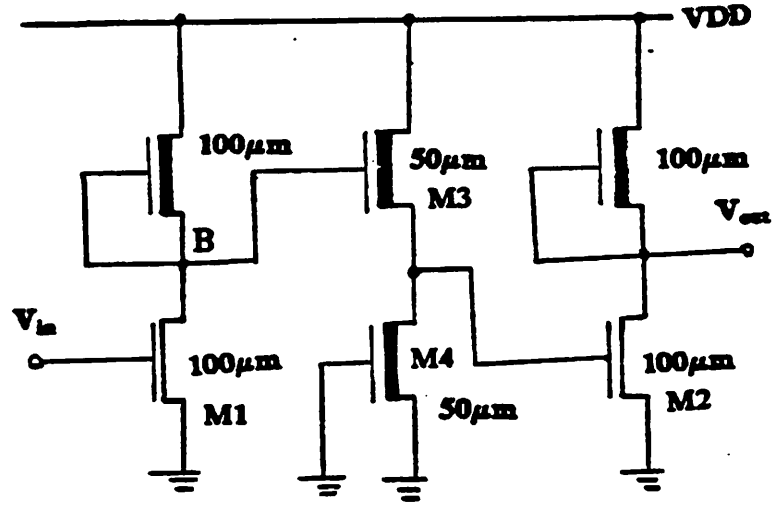


Fig. 3.2.3(b) Cascading amplifier with buffered stage

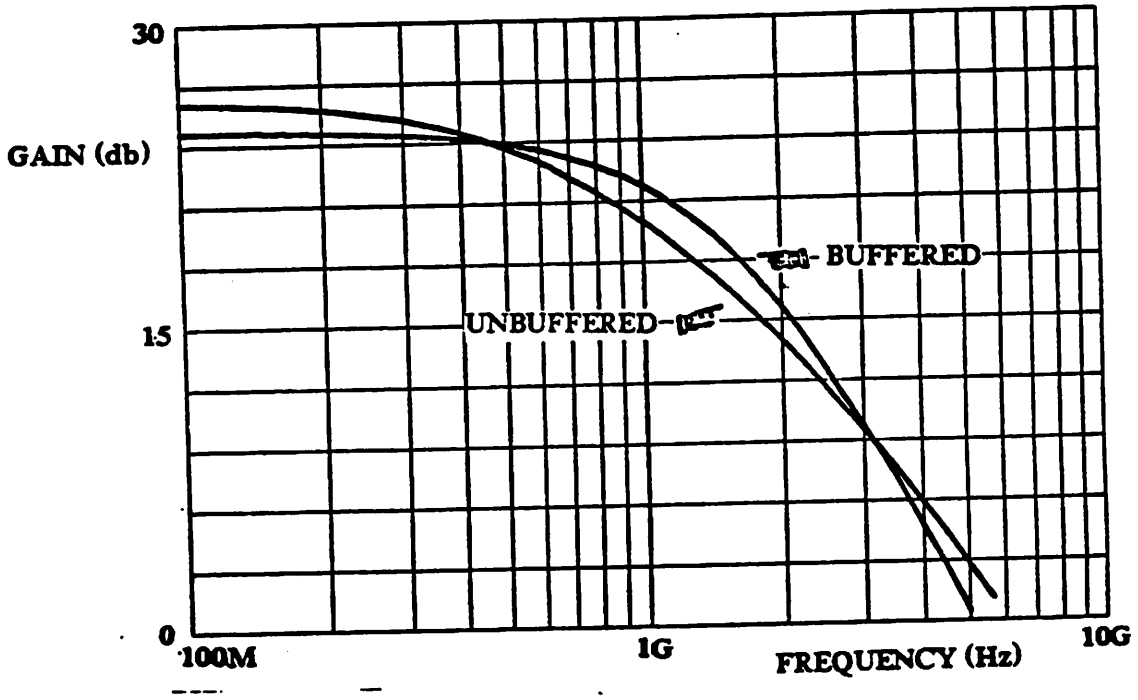


Fig. 3.2.4(a) Amplitude response of cascading amplilfiers with and without buffered stage

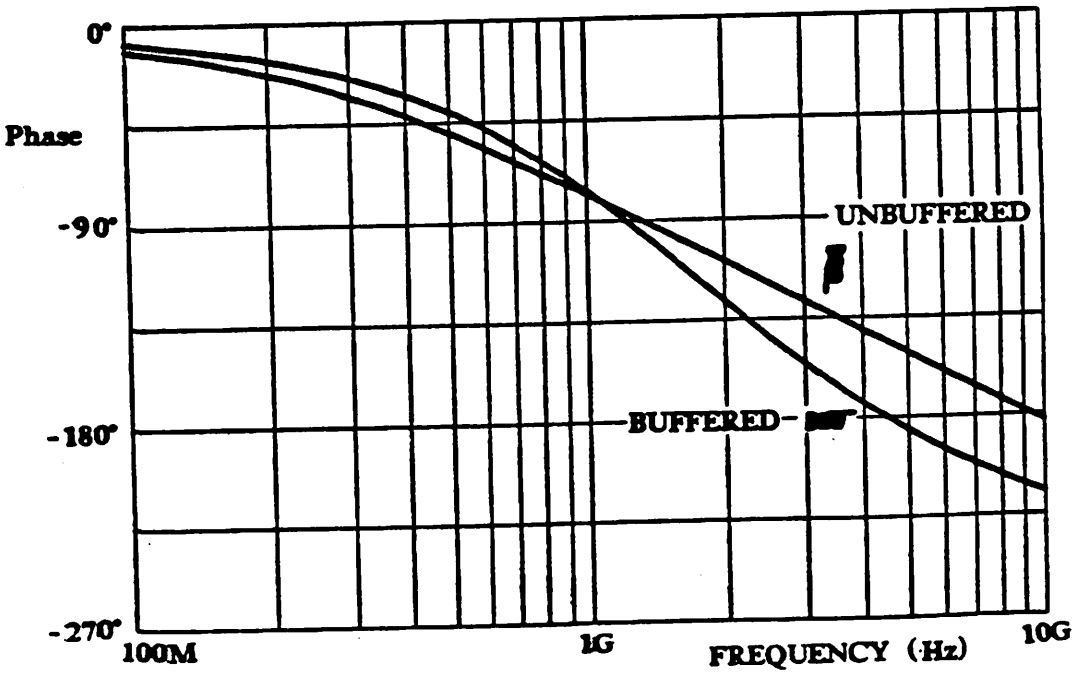


Fig. 3.2.4(b) Phase response of cascading amplifier with and without buffered stage

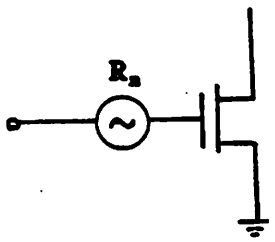
larger. However, the high frequency phase shift in the buffered amplifier increases substantially beyond 1GHz. In fact, the phase shift at 0 db gain is more than 180° making it not suitable for feedback application because of stabilility problem. In comparison, the phase shift of the unbuffered amplifer is less than 180° at 0 db gain and it is therefore possible to use this with an additional wide-band inverter stage to form the basic open-loop amplifier for negative feedback application. Although the phase shift could be reduced by increasing the device sizes of the follower stage, the power consumption of the circuit will be increased. In addition, because of the added stage and phase shift, it might be necessary to over-compensate the frequency response for stable operation, resulting in a smaller bandwidth. Excessive phase shift introduced by complex circuitry is precisely why it is advisable to keep a wide-band circuit as simple as possible. Buffered stages are therefore not used in this thesis work.

3.3. CIRCUIT NOISE CONSIDERATIONS

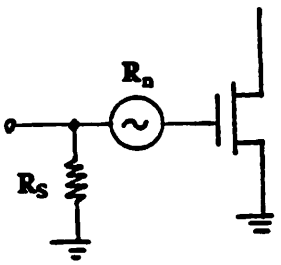
The noise characteristics of a SIGMOS device has been discussed in section 2.4. In this section, the effect of input impedance matching requirements on amplifier noise performance is examined. The input noise of the amplifier may be represented by a equivalent input thermal noise resistance R_n in the analysis. Three possible input impedance matching circuit configurations shown in Fig. 3.3.1(b) to (d) are considered. Since amplifier noise is dominated by the input stage, the lowest noise is obtained with a simple depletion load inverter gain stage. It is therefore reasonable to assume that R_n is more or less the same for all four configurations shown. Figure 3.3.1(a) is used as a reference. The input impedance is infinite at low frequency. The noise figure (NF), with respect to the source impedance, R_S, is given by

$$NF_a = 1 + \frac{R_n}{R_S} \tag{3.3.1}$$

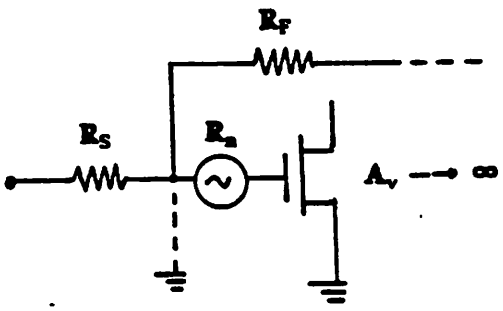
Note that the NF specification is dependent on the value of R_S. NF decreases for a higher value of R_S. Typical value of NF for microwave amplifiers with 50Ω source resistance in BJT and GaAs technologies reported in the literature is in the range of 3 to 8 db. Lower NF



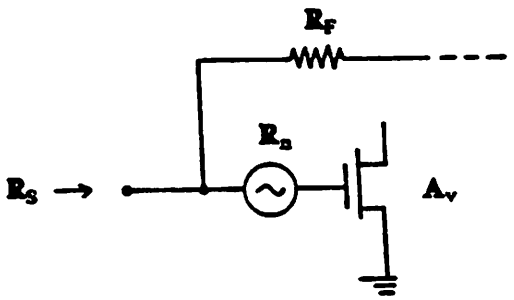
(a) Reference circuit



(b) Direct shunt terminmation



(c) Series termination



(d) Active termination

Fig. 3.3.1 Circuit configuration for input impedance matching to R_S

is typically achieved in a narrow band amplifier in which lossless components are used for impedance matching or when it is referred to its optimum noise resistance which is typically larger than 50Ω

Figure 3.3.1(b) is a direct shunt termination. and

$$NF_b = 2 + \frac{4R_n}{R_s} = 4(NF_a - 0.5) \tag{3.3.2}$$

Figure 3.3.1(c) has a matched resistance in series with a virtual ground and

$$NF_c \approx NF_a + 1 + \frac{4R_S}{R_F}(1 + \frac{R_n}{R_F} + \frac{R_n}{R_S}) \tag{3.3.3}$$

Figure 3.3.1(d) uses a resistive shunt-shunt feedback to match the input resistance. The input resistance is determined by the amplifier gain (A_v) and R_F. For a constant A_v

$$NF_d \approx NF_a + \frac{R_S}{R_F} + \frac{R_n R_S}{R_F^2} + \frac{2R_n}{R_F} \tag{3.3.4}$$

Variations of NF vs. normalized amplifier noise resistance. R_n / R_S. are plotted in Fig.3.3.2. for the case of $R_S / R_F = 0.05$. The formulae were compared with SPICE simulations using a resistor for R_n and controlled voltage source for the amplifier. NF_a and NF_b are exact. Due to the approximations involved in the derivations. the formulae given for NF_c and NF_d are within $\pm 0.2db$ from the simulated noise figure in the range of interest. i.e. from 2db to 10db. and are considered accurate enough for practical purposes.

For low noise design. it is seen that configuration (d) is most preferred. However. this requires a stable open-loop voltage gain. A_v >10. to be practical. This is not always possible with conventional feedback configurations in submicron MOS technology. Attempting to provide a stable A_v with local series feedback will necessitate a $R_E \gg 50$ ohm at the source of the input device. Also. thermal noise in R_E translates to the input directly and therefore negates the advantage of configuration (d) and the final NF achieved will not be better than that of configuration (c). Configuration (b) has a consistently higher NF within the NF range of interest with a maximum increase of about 6db at the

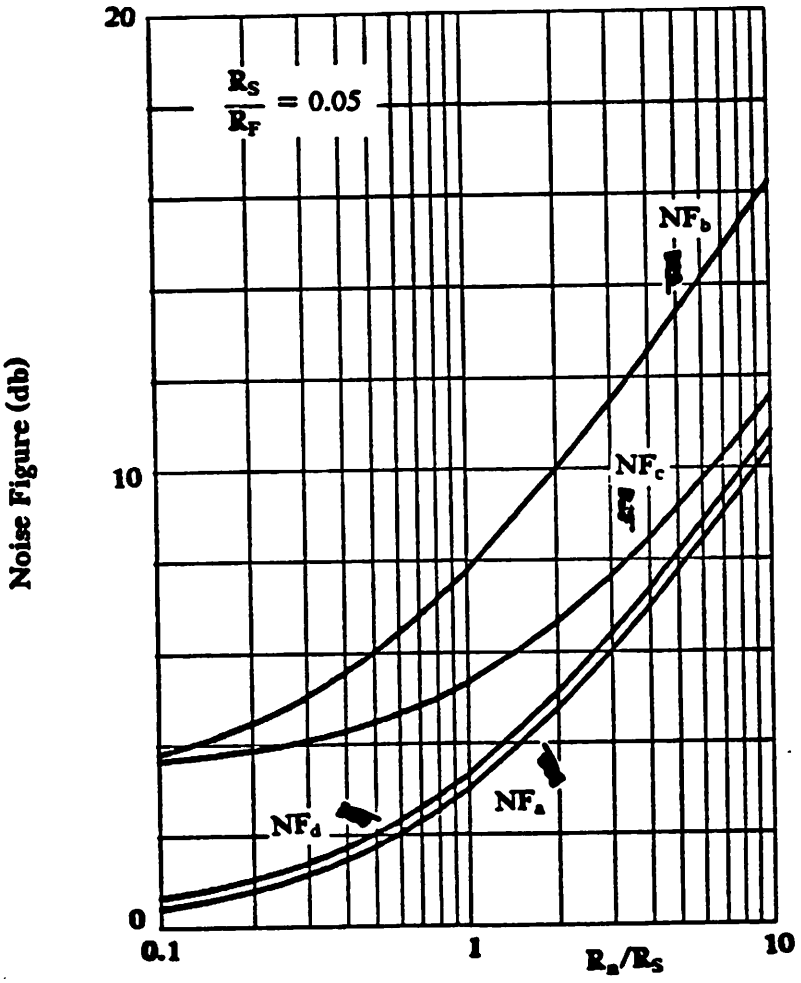


Fig.3.3.2 Variations of noise figures with R_n/R_S.

high NF regime with respect to NF_d. This high noise figure will show up at the low *1/f* noise frequency range and at the very high frequency range. This configuration is therefore not suitable. Configuration (c) also has higher noise in the range of interest. It also has a lower open-loop input pole than that of configuration (b) and (d) for the same gate width, W. This can create a dominant pole for large W and limit the frequency response of the amplifier. In addition, a virtual ground at the input of the amplifier cannot be realized in practice due to the low open-loop gain limitation in submicron MOS technology. This configuration is therefore not practical.

Lower noise figure can be achieved by increasing W, but the practical constraint on power dissipation in the package, about 1 Watt, limits the total width of enhancement

device in the circuit to about 2500μm. In addition, if the first stage gain is low, the noise contribution from subsequent stages must be included according to Eqn. 3.3.5 [16].

$$NF = NF_1(1st\ stage) + \frac{NF_2(2nd\ stage) - 1}{|A_{v1}|^2} + \ldots\ldots \qquad (3.3.5)$$

As an example, assuming the same NF for all subsequent stages and $W = 1000\mu m$, $A_{v1} = 2$, $\Gamma = 2/3$ and $R_S = 50$, R_n per stage is

$$R_{n1} \approx 2 * \frac{2/3}{g_m} \approx 17\ \Omega \quad \text{and} \quad \frac{R_{n1}}{R_S} = 0.34$$

The factor of 2 in the above equation is due to the contribution from the depletion device in a depletion load inverter gain stage. The effective R_n is

$$R_n = 0.34 + \frac{0.34}{2^2} = 0.43 \quad \text{From Fig. 3.3.2} \quad NF_d = 1.8\ \text{db}$$

Note that noise contributions from the 3rd stage and beyond are usually small and can be neglected. Many other factors can degrade the NF estimated above. For example, noise contributions from poly gate resistance, contact resistance and parasitic source/drain resistance can increase the noise level significantly. For example, if the gate resistance is 4 ohms, NF_d would increase to 2.1 db. Also due to high power dissipation, chip temperature will rise, causing g_m and device gain to decrease (as discussed in Chapter 2), thermal nosie to increase, all of which will lead to an increase in the circuit noise figure. Finally, A_v is actually frequency dependent and rolls down at both ends of the frequency band. Thus the noise figure will increase at these ends. $1/f$ noise and high frequency noise (f^2 component) will also add to the average NF of the amplifier. The final average NF_d will be about 3 db. the corresponding values for NF_b and NF_c are about 7.3 db and 5.1 db respectively.

It should be pointed out that the estimates shown above were based on idealized circuit configurations shown in Fig.3.6(a) to (d). A practical circuit with a smaller second stage and a combination of the above circuit configurations would certainly yield a higher NF. As is clear from Eqn. 3.3.5 , any reduction of the first stage gain will increase the

amplifier NF.

3.4. HIGH FREQUENCY I/O IMPEDANCE MATCHING

The input and output impedances of a wide-band amplifier typically consist of both resistive and reactive components. In order that the low frequency impedance may be matched to 50 ohms, the high frequency characteristics may be quite different. This is particularly true at the input of a MOS amplifier which is donminantly capacitive. From the discussion in the previous section, it is desirable to have a large width device at the input stage to achieve low noise specification, but this will increase the input capacitance and therefore increase the high-frequency mismatch. This section discusses the effect of reactive components to high frequency matching.

I/O impedance matching in wide-band amplifiers is usually quantified by voltage standing wave ratio (VSWR). With reference to Fig. 3.4.1. VSWR is related to the reflection coefficient (ρ) as follows.

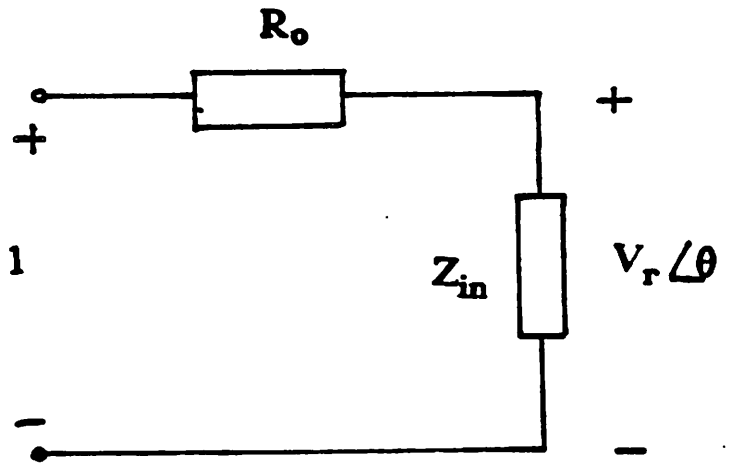


Fig. 3.4.1 A simple one port with a source resistance R_o

$$\rho = \frac{Z_{in} - R_o}{Z_{in} + R_o} \qquad \text{where} \quad Z_{in} = R_{in} + jQ_{in} \tag{3.4.1}$$

$$VSWR = \frac{1 + |\rho|}{1 - |\rho|} \tag{3.4.2}$$

$$= \frac{2}{1 - \sqrt{4V_r^2 - 4V_r \cos\theta + 1}} - 1 \tag{3.4.3}$$

where V_r is the relative voltage amplitude and θ is the relative phase at the input port. Eqn.3.4.3 provides a mean of calculating the VSWR from a SPICE output file. Note that ideally, for perfect matching, $\rho = 0$, and VSWR = 1. A typical specification for wide-band amplifier is VSWR < 2 over the entire frequency band for both the input and output ports. Fig. 3.4.2 shows the VSWR variation with respect to frequency for a simple case of 50Ω in parallel with a capacitor of various capacitance values. The capacitor represents the input of a SIGMOS device. The input capacitance can be estimated from Eqn. 3.4.4.

$$C_{in} \approx \frac{2}{3}C_{ox}WL + 0.15C_{ox}WL + 0.3C_{ox}WL, \text{ where } L = 1\,\mu m \tag{3.4.4}$$

The first term is C_{gs}, the second term is C_{gsov} and the last term is the Miller capacitance, assuming a gain of -1. From Fig.3.4.2, it can be seen that for VSWR < 2 at 1 GHz, the maximum input capacitance is about $2pF$ which corresponding to a device width, W, of about 1000 μm.

In addition to the capacitive component, the bonding wire contributes to a series reactive component to the input node. Bonding inductance can be estimated from Eqn. 3.4.5 [17].

$$L_w = 2l[\ln(\frac{4l}{d}) - 1] \tag{3.4.5}$$

where the wire inductance L_w is in nH, wire length l and wire diameter d are in cm. Hence for a 1 mil aluminum wire,

$$\frac{L_w}{l} \approx 0.8\ nH/mm$$

Fig.3.4.3 shows the variations of VSWR with frequency for different L_w for the input port shown in the insert. Note that a small amount of bonding wire at the input node helps to lower VSWR at high frequency. However, the gain of the amplifier will be reduced. A

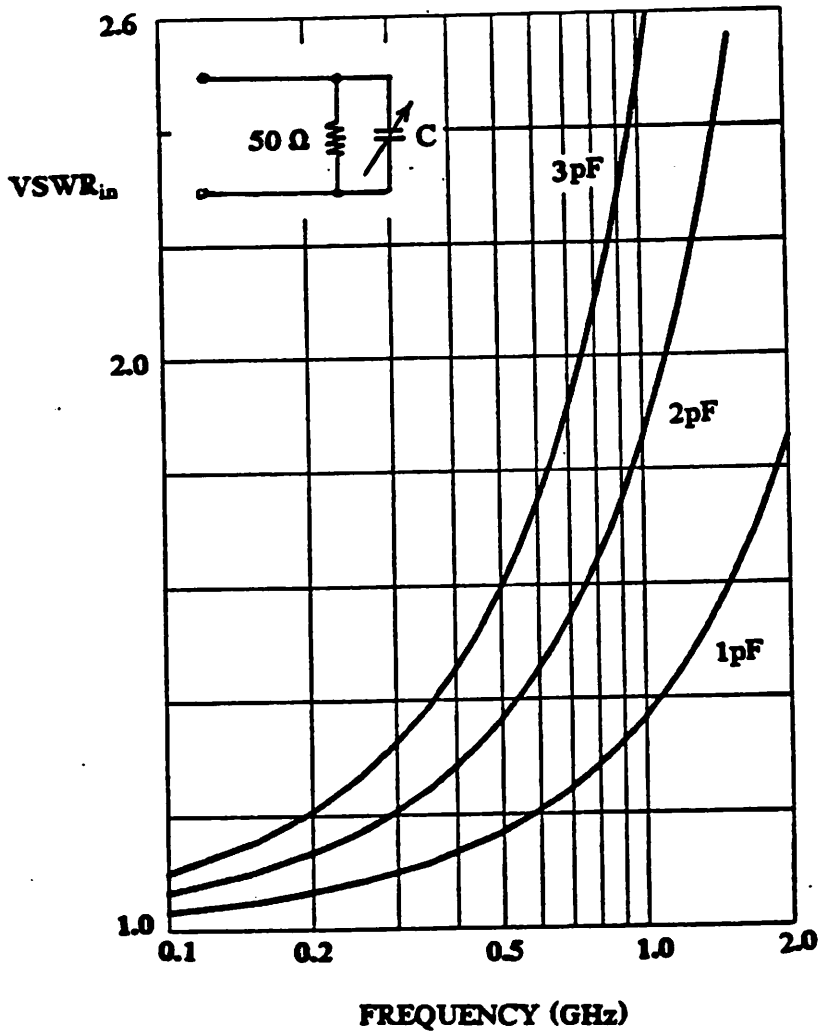


Fig.3.4.2 High frequency VSWR variations with R_o parallel C

mismatch in R_{in} will also affect input VSWR. Fig.3.4.4 shows the variation of VSWR with different effective R_{in}. Note that VSWR will increase when $R_{in} > R_o$. For the circuit configuration shown in Fig. 3.3.1(d). R_{in} is expected to increase at high frequency due to reduced loop gain which will cause the input VSWR to increase further in addition to the increase due to capacitive component. The input VSWR may be improved with a series RC branch shunting across the input which will help to lower R_{in} at high frequency.

At the output node of the amplifier. the capacitive component is much smaller than that of the input and therefore will have a better output VSWR characteristic in general.

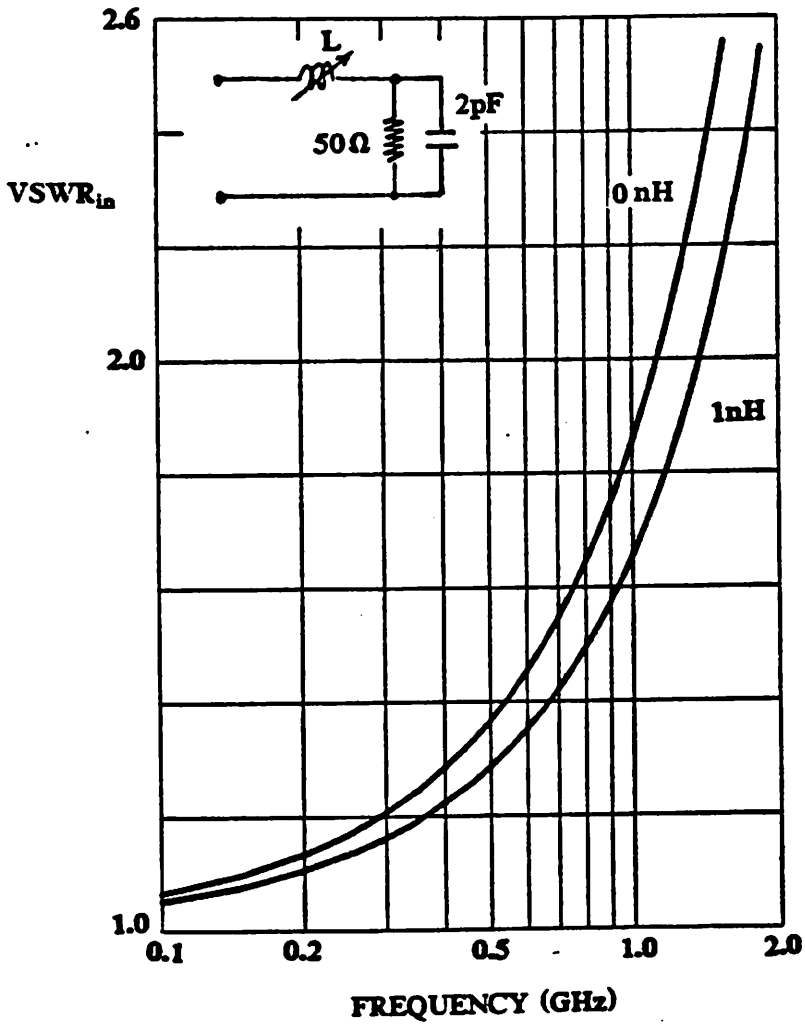


Fig.3.4.3 High frequency VSWR variations with series inductance

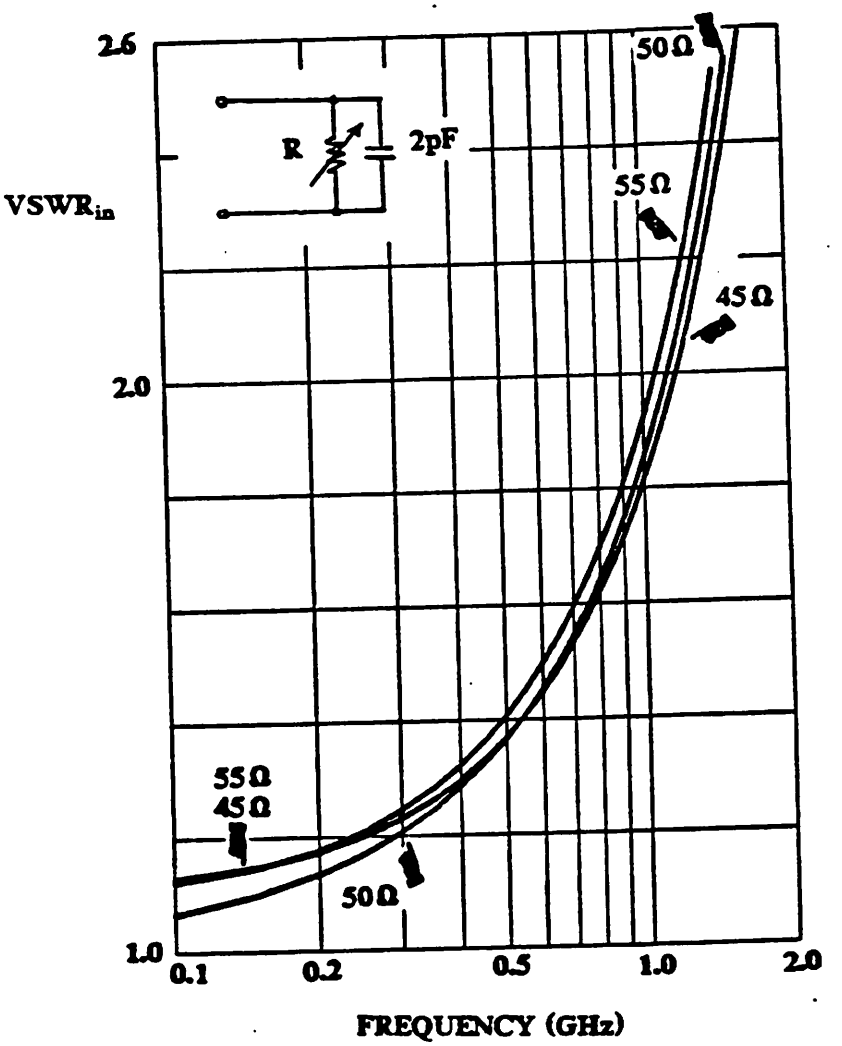


Fig.3.4.4 High frequency VSWR variations with R_{in}

3.5. Single Stage Series Feedback [17]

A simplified single stage MOS amplifier with local series feedback is shown in Fig.3.5.1(a) and the corresponding midband ac equivalent circuit is shown in Fig. 3.5.1(b). It can be shown that at midband.

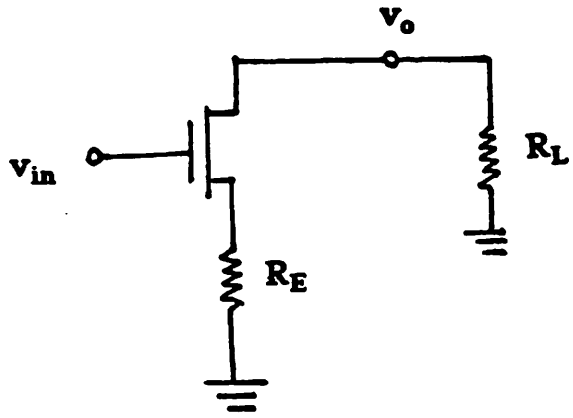


Fig. 3.5.1(a) Single stage MOS amplifier with local series feedback

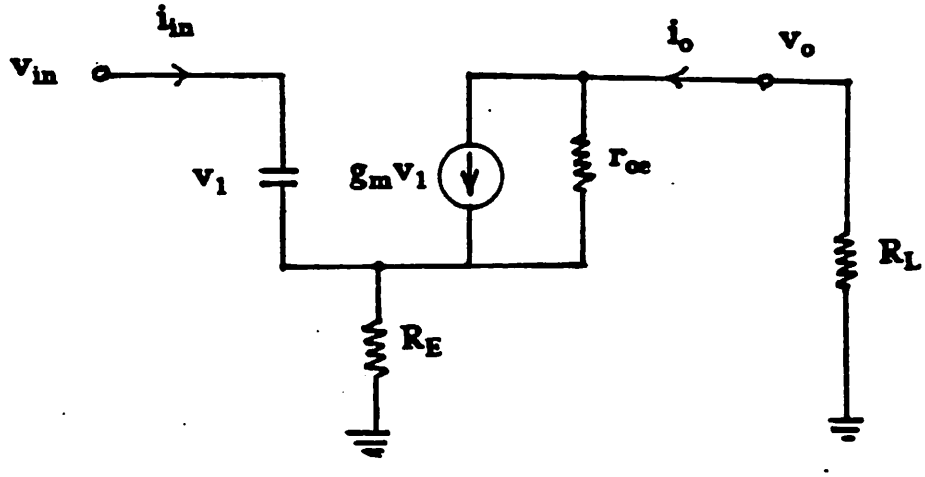


Fig. 3.5.1 (b) Midband ac equivalent circuit

$$G_T \equiv \frac{i_o}{v_{in}} = \frac{g_m}{1+g_m R_E} \frac{1}{1+\frac{R_E+R_L}{r_{oe}(1+g_m R_E)}} \tag{3.5.1}$$

$$A_l = -g_m R_E \left| \frac{r_{oe}}{r_{oe}+R_E+R_L} \right| \tag{3.5.2}$$

$$R_{in} \equiv \frac{v_{in}}{i_{in}} = \frac{1}{s\left|\frac{C}{1+|A_l|}\right|} + R_E /\!/ (R_L + r_{oe}) \tag{3.5.3}$$

$$R_{out} \equiv \frac{v_o}{i_o} = (1+g_m R_E) r_{oe} + R_E \tag{3.5.4}$$

For $R_E = 50\ \Omega$. $W_e = 1000\mu m$. $W_d = 800\mu m$ (depletion load). $g_m \approx 72mS$. $r_{oe} \approx 200\ \Omega$. $R_L = r_{od} \approx 150\Omega$. hence. $g_m R_E = 3.6$ and $A_l = -1.8$. $G_T = 0.18 g_m = 13mS$. so that $G_T R_L = 1.9$. If an external load of 50Ω is added. the overall gain is 0.48. which is less than one!

The following should be noted:

(a) R_E contributes to the amplifier noise figure directly if it is in the first stage. Hence $R_E \leqslant 50$ ohm is desirable. But from Eqn.3.5.2. reducing R_E will reduce the loop gain.

(b) For 5V VDD supply voltage. due to the voltage drop across R_E. V_{gs} for the driving device is reduced. Thus g_m and f_T are reduced. Lower g_m also means higher channel noise.

(c) In a multistage circuit. local series feedback requires level shifting for direct coupling. this further reduces the forward gain and the bandwidth as discussed in section 3.2.

The conclusion is that the series stage should not be used for the first stage for submicron MOS amplifier. The same arguments also applied to the alternate series/shunt stages. series-shunt feedback pair. the series-series- shunt triple feedback circuits.

3.6. Single Stage Shunt Feedback [17]

A simplified single stage MOS amplifier with local shunt feedback is shown in Fig.3.6.1(a) and the corresponding midband ac equivalent circuit is shown in Fig.3.6.1(b). Note that a source resistance R_S is included explicitly in the following analysis. It can be shown that at midband.

$$R_T \equiv \frac{v_o}{i_{in}} = -(R_F - \frac{1}{g_m})\left|\frac{|A_l|}{1+|A_l|}\right| \tag{3.6.1}$$

$$A_l = -g_m r_{oe}^{'}\left|\frac{R_S}{R_S+R_F+r_{oe}^{'}}\right| \quad \text{where} \quad r_{oe}^{'} = r_{oe} /\!/ R_L \tag{3.6.2}$$

$$R_{in} \equiv \frac{v_{in}}{i_{in}} = \frac{R_F}{1+g_m r_{oe}^{'}} \tag{3.6.3}$$

$$R_{out} \equiv \frac{v_o}{i_o} = \left|\frac{R_F+R_S}{1+g_m R_S}\right| /\!/ r_{oe} \tag{3.6.4}$$

Ideally, the shunt stage is to stablize $R_T \rightarrow -R_F$. As R_F increases, loop gain A_l decreases thus reducing the feedback effect. With a SIGMOS process using a depletion load inverter as gain stage with $W_e = W_d = 1000\mu m$, $R_S = 50\Omega$, $R_L = 50\Omega$ and $R_F = 240\Omega$, the gain is about 1.2 and the loop gain is about 0.35! A single stage with shunt feedback is therefore not useful because of the low forward gain. A shunt-shunt feedback over 3 cascading stages is a better alternative.

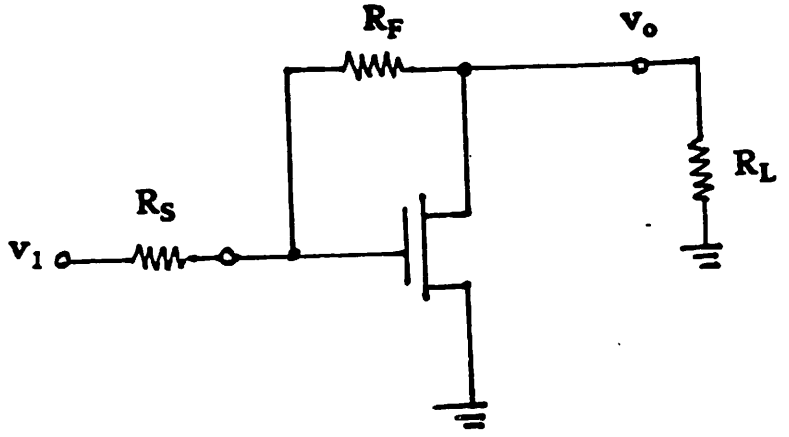


Fig. 3.6.1(a) Single stage MOS amplifier with local shunt feedback

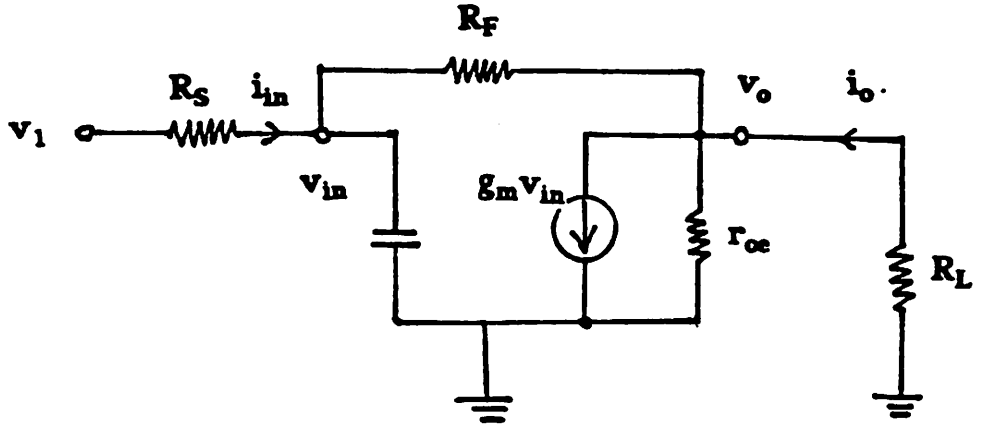


Fig. 3.6.1(b) Midband ac equivalent circuit

CHAPTER 4

MATCHED IMPEDANCE MOS AMPLIFIER DESIGN

4.1. Introduction

The problems associated with the design of matched impedance, low-noise, wide-band amplifiers with submicron MOS technology are high device noise characteristics, low g_m, low r_{ds}, and high input capacitance. New design techniques must be developed to achieve reasonable amplifier performance. Design procedures for a new amplifier configuration that has 3 gain stages and two feedback loops are described in this chapter. A test circuit and the high frequency package used for testing are also described. Numerical quantities used for discussions are based on the 1μm SIGMOS technology. But the principle involved can be applied directly to any submicron MOS technology or GaAs MESFET/HEMT technologies.

4.2. Ideal Matched Impedance MOS Amplifier

Fig. 4.2.1 shows an idealized midband ac model for a MOS gain stage. The value of r_o is assumed to be large and r_o is not included. Shunt-shunt feedback is used to achieve input/output impedance matching. The following can be derived [18],

$$R_{in} = R_{out} = \frac{R_F + R_o}{1 + g_m R_o} \tag{4.2.1}$$

If $R_F = g_m R_o^2$, then $R_{in} = R_{out} = R_o$ and, $A_v = 1 - g_m R_o$. For a gain of -5, $g_m > 6/R_o$. For a single stage MOS amplifier in SIGMOS technology, this requires $W > 1500\mu m$ in a 50Ω system. The previous discussion in section 3.4 has already indicated that the high frequency input VSWR would exceed 2 for an input stage with W> 1000μm. In addition, for short channel devices, r_o is low for large W. For example, in the case of SIGMOS technology, the effective r_o, including the effect of the depletion load, is about 40Ω! Clearly, this has violated the assumption that r_o is large and above all, it is impossible to match the output to a 50Ω load. Series feedback will increase amplifier noise and reduce gain as dis-

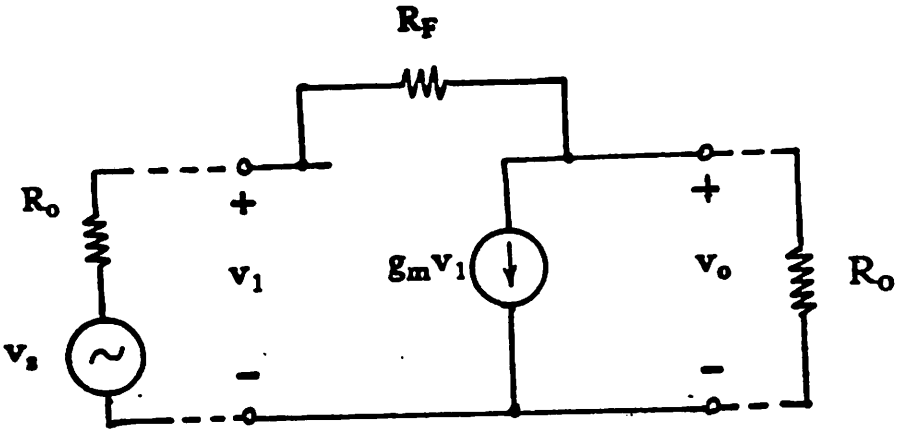


Fig. 4.2.1 Idealized AC equivalent circuit of a MOS amplifier

cussed in section 3.5. It is clear that a multistage design is necessary and the low r_o of the output stage must be included into the design formula.

4.3. Resistive Shunt-Shunt Feedback

In this section, a generalized analysis of an MOS amplifier using resistive shunt-shunt feedback to achieve input/output impedance matching is presented. The midband ac equivalent circuit of a basic MOS amplifier is shown in Fig. 4.3.1. Note that r_{ds} is included at the output. R_1 is an external resistor whose significance will be explained later. In a multistage amplifier, the g_m shown would represent the effective g_{mT} and the r_{ds} would be the r_{ds} of the last stage. For noise considerations, as explained in section 3.3, a shunt-shunt resistive feedback is most desirable as shown in Fig. 4.3.2 with the terminating resistor R_o included. The short circuit Y matrix of the circuit enclosed within the dotted lines can be written by inspect:

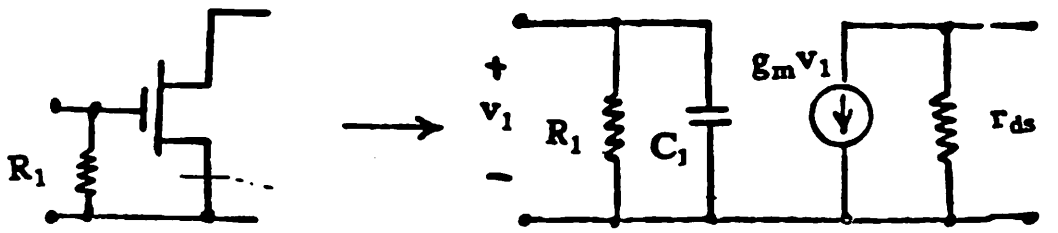


Fig. 4.3.1 AC equivalent circuit of a MOS amplifier

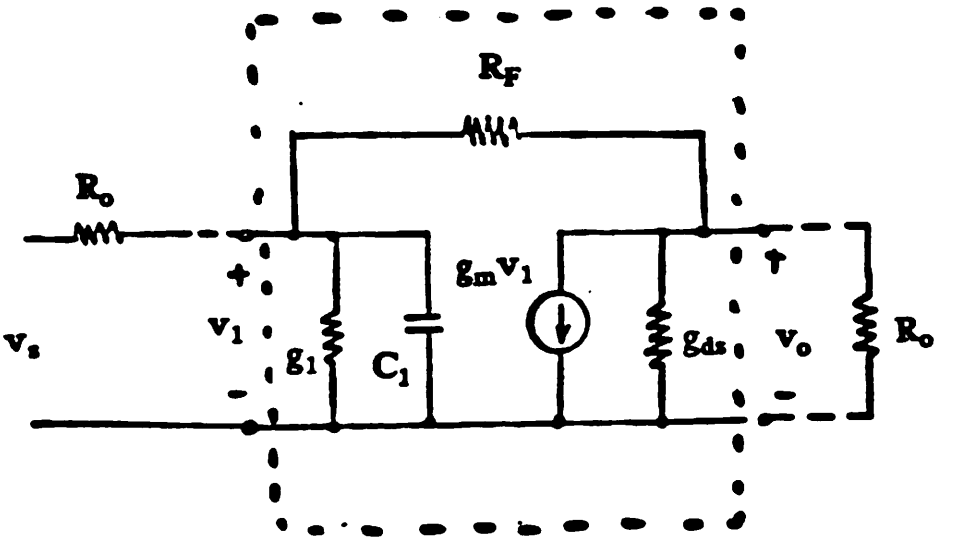


Fig. 4.3.2 Resistive shunt-shunt feedback MOS amplifier

$$\mathbf{Y} = \begin{vmatrix} g_F + g_1 & -g_F \\ g_m - g_F & g_F + g_{ds} \end{vmatrix} \tag{4.3.1}$$

This can be transformed into the scattering matrix S. where

$$\mathbf{S} \equiv \begin{vmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{vmatrix}$$

with $\hat{y}_{ij} \equiv y_{ij} R_o$. the scattering matrix parameters s_{ij} are given by [19]:

$$s_{11} = \frac{(1-\hat{y}_{11})(1+\hat{y}_{22}) + \hat{y}_{12}\hat{y}_{21}}{(1+\hat{y}_{11})(1+\hat{y}_{22}) - \hat{y}_{12}\hat{y}_{21}}$$

$$s_{12} = \frac{-2\hat{y}_{12}}{(1+\hat{y}_{11})(1+\hat{y}_{22}) - \hat{y}_{12}\hat{y}_{21}}$$

$$s_{21} = \frac{-2\hat{y}_{21}}{(1+\hat{y}_{11})(1+\hat{y}_{22}) - \hat{y}_{12}\hat{y}_{21}}$$

$$s_{22} = \frac{(1+\hat{y}_{11})(1-\hat{y}_{22}) + \hat{y}_{12}\hat{y}_{21}}{(1+\hat{y}_{11})(1+\hat{y}_{22}) - \hat{y}_{12}\hat{y}_{21}}$$

VSWR are related to s_{ii} by $VSWR_{in} = \frac{1+|s_{11}|}{1-|s_{11}|}$ and $VSWR_{out} = \frac{1+|s_{22}|}{1-|s_{22}|}$

For perfect impedance matching. $s_{11} = s_{22} = 0 \longrightarrow VSWR_{in} = VSWR_{out} = 1$.

The results of the transformation are:

$$s_{11} = \frac{1}{A_1}\left[\frac{R_F}{R_o}(1 + R_o g_{ds}) - R_o(g_m + g_{ds}) - \frac{R_F}{R_1} - \frac{R_o}{R_1}(1 + g_{ds} R_F)\right] \tag{4.3.2a}$$

$$s_{12} = \frac{2}{A_1} \tag{4.3.2b}$$

$$s_{21} = -\frac{2}{A_1}(g_m R_F - 1) \tag{4.3.2c}$$

$$s_{22} = \frac{1}{A_1}\left[\frac{R_F}{R_o}(1 - R_o g_{ds}) - R_o(g_m + g_{ds}) + \frac{R_F}{R_1} - \frac{R_o}{R_1}(1 + g_{ds} R_F)\right] \tag{4.3.2d}$$

with $$A_1 \equiv 2 + R_o(g_m + g_{ds}) + \frac{R_F}{R_o}(1 + g_{ds} R_o) + \frac{R_F}{R_1} + \frac{R_o}{R_1}(1 + R_F g_{ds}) \tag{4.3.2e}$$

Note that A_1 is normally a large value (typically > 50). as it is inversely proportional to the reversed transmission gain. s_{21}. which should be small. From Eqn. 4.3.2d. for $s_{22} = 0$. i.e. $VSWR_{out} = 1$.

$$R_F = \frac{R_o^2(g_m + g_{ds} + g_1)}{(1 + R_o g_1)(1 - R_o g_{ds})}$$

Thus $R_F > 0$ implies $r_{ds} > R_o$. that is to say that for the output impedance to match R_o. r_{ds} must be larger than R_o. as expected. It is interesting to note that from Eqn.4.3.2(a) and Eqn.4.3.2(d).

$$s_{11} - s_{22} = \frac{2R_F}{A_1}(g_{ds} - \frac{1}{R_1}) \tag{4.3.3}$$

$$s_{11} + s_{22} = \frac{2}{A_1}\left|\frac{R_F}{R_o} - R_o(g_m + g_{ds}) - \frac{R_o}{R_1}(1 + g_{ds}R_F)\right| \tag{4.3.4}$$

Perfect low frequency matching at both the input and output is achieved when

$$s_{11} - s_{22} = 0 \quad \text{and} . \tag{4.3.5}$$

$$s_{11} + s_{22} = 0 \tag{4.3.6}$$

The significance of R_1 is now apparent. Without R_1. Eqn. 4.3.3 implies that at least one of the amplifier ports cannot be matched. When r_{ds} is large. i.e. g_{ds} is small. the mismatch may be tolerable. But for short channel devices. r_{ds} is small (i.e. g_{ds} is large) and the mismatch could be large even at low frequency. From Eqn.4.3.3. Eqn.4.3.5. is satisfied as long as $R_1 = r_{ds}$. independent of all other device parameters. Note that even with process variations that affect r_{ds} and R_1. the mismatch at the input/output port is greatly reduced by R_1. It should be noted that R_1 is directly shunting across the input and will increase the input noise level of the amplifier. However. as long as r_{ds} of the output stage is a few times larger than R_o. the increase will be tolerable. For low r_{ds}. the trade off is between the degree of midband impedance matching and the noise level of the amplifier.

From Eqn.4.3.4. Eqn.4.3.6 is satisfied when

$$R_F = g_m R_o^2 \left|\frac{1 + \frac{g_{ds} + g_1}{g_m}}{(1 - R_o^2 g_{ds} g_1)}\right| \tag{4.3.7}$$

Under these ideal conditions (denoted by a superscript o).

$$R_1^\circ = r_{ds} \tag{4.3.8a}$$

$$R_F^\circ = g_m R_o^2 \left| \frac{1 + \frac{2g_{ds}}{g_m}}{1 - (R_o g_{ds})^2} \right| \tag{4.3.8}$$

$$s_{11}^\circ = 0 \tag{4.3.8c}$$

$$s_{12}^\circ = \frac{2}{A_1^\circ} \tag{4.3.8d}$$

$$s_{21}^\circ = -\frac{R_o(g_m + g_{ds})-1}{(1 + R_o g_{ds})} \tag{4.3.8e}$$

$$s_{22}^\circ = 0 \tag{4.3.8f}$$

with $$A_1^\circ \equiv \frac{2[1 + R_o(g_m + g_{ds})]}{(1 - R_o g_{ds})} \tag{4.3.8g}$$

The above set of equations gives the design formulas for resistive shunt-shunt feedback to achieve simultaneous input/output impedance matching in the present of finite r_{ds}. Evidently, a large g_m is desirable to achieve reasonable gain. A large g_m can be obtained by cascading 3 stages, so that $g_{mT} = g_m(g_m r_{ds})^2$. But g_{mT} will have large variations. In the next sections, an alternative circuit will be examined.

As an example, consider 3 cascaded stages, with $W_3 = 500\mu m$. Using nominal SIG-MOS device parameters, $g_{mT} = (4.6)^2 * 40 * 10^{-3} = 846.4\ mS$, $r_{rd3} = 120\Omega$. Four matching conditions will be evaluated:

(1) $R_1 \to \infty, s_{22} = 0$ i.e. output port matched:

(2) $R_1 \to \infty, s_{11} = 0$ i.e. input port matched:

(3) $R_1 \to \infty, s_{11} + s_{22} = 0$ i.e. $VSWR_{in} = VSWR_{out}$:

(4) $R_1 = r_{ds3}, s_{11} = s_{22} = 0$ i.e both ports matched.

The results are tabulated in Table 4.3.1. Note that the midband VSWRs that can be achieved without R_1 are larger than 1.8 even at midband. The high frequency VSWR undoubtedly will grow even larger with increasing frequency as discussed in section 3.4. The addition of R_1 is therefore necessary for a technology that has a low device r_{ds}.

Variable	Case(1) $R_1 \rightarrow \infty$ $s_{22} = 0$	Case(2) $R_1 \rightarrow \infty$ $s_{11} = 0$	Case(3) $R_1 \rightarrow \infty$ $s_{11} = s_{22}$	Case(4) $R_1 = r_{ds3}$ $s_{11} = s_{22} = 0$
R_F (Ω)	3663	1508	2137	2611
A_1	148.5	87.5	105.3	150.0
$VSWR_{in}$	2.4	1.0	2.0	1.0
$VSWR_{out}$	1.0	1.8	2.0	1.0
$s_{21}(db)$	32.4	29.3	30.7	29.4
$s_{12}(db)$	-37.4	-32.8	-34.4	-37.5

Table 4.3.1 Amplifier midband performance under various matching conditions

These results can be explained intuitively as follows. Since R_F is usually large. the input impedance of the loaded open-loop circuit is large. whereas the output impedance is low for short channel device so that there is a large mismatch between these two values to begin with. As R_F is decreased. both the closed-loop input and output impedances will decrease due to shunt feedback. When the output is matched. the input impedance is still large. thus giving a large $VSWR_{in}$ (case 1). As R_F is reduced further such that the closed loop input impedance equals R_o. the output impedance would be reduced to a value that is much below R_o. resulting in a large $VSWR_{out}$ (case 2). There is an R_F value in between these two extreme cases such that the input impedance is larger than R_o and the output impedance is lower than R_o by the same ratio. This will be the case when $s_{11} = -s_{22}$. resulting in $VSWR_{in} = VSWR_{out}$ (case 3). However. if both open-loop input and output impedances are equal and greater than R_o to start with. s_{11} equals s_{22} for all values of R_F and there is one particular value of R_F that makes both the closed loop impedances equal to R_o at the same time (case 4).

As shown in Table 4.3.1. although case(4) has good midband performance for typical parameter values. the g_{mT} is subjected to large process variations and affects all other s_{ij} parameters. In the next two sections. alternative circuits will be examined that will reduce the g_{mT} variation.

4.4. An MOS Voltage Amplifier

Fig.4.4.1 shows a MOS voltage amplifier with an active shunt-shunt feedback. Simple depletion load inverters are used as gain stages. W_x refers to the width of the enhancement devices. Midband analysis gives

$$A_v = -\frac{W_1}{W_4}\frac{1}{1+\frac{1}{T}} \tag{4.4.1}$$

where T is the loop gain and is given by:

$$T = \frac{(g_{m1}r_{ds1})(g_{m2}r_{ds2})(g_{m3}r_{ds3})}{1+\frac{W_1}{W_4}} = \frac{(g_m r_{ds})^3}{1+\frac{W_1}{W_4}} \tag{4.4.2}$$

Variations of T and A_v with W_1/W_4 ratio are shown in Fig.4.4.2 For reasonable gain. $W_1/W_4 = 20$ is chosen. giving $T = 4.65$ and $A_v = -16.5$ *or* 24.4 *db* (no impedance matching as yet). An additional resistive shunt-shunt feedback is needed to achieve I/O impedance matching. However, because of the shunt node at the last stage. the effective r_o

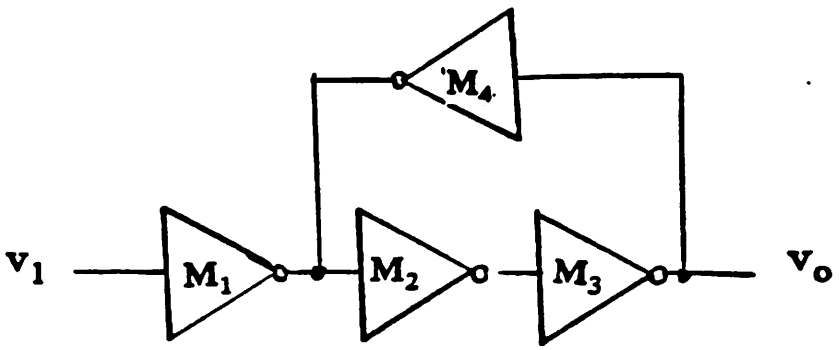


Fig.4.4.1 MOS voltage amplifier with active shunt-shunt feedback

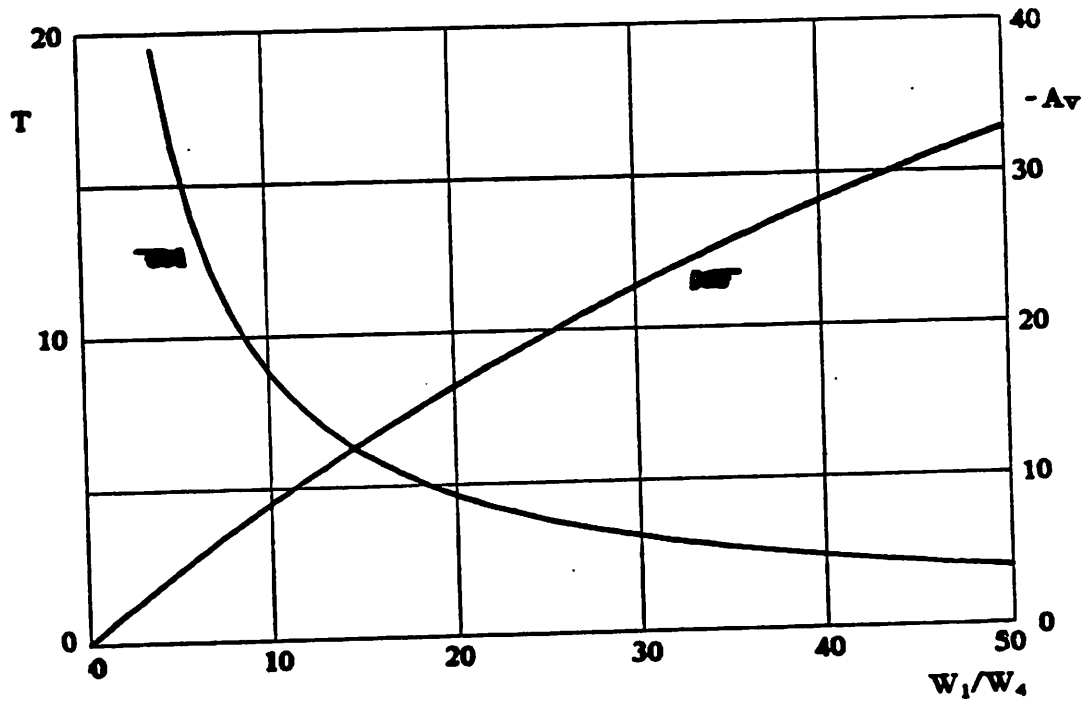


Fig. 4.4.2 Loop gain and voltage gain vs. W_1/W_4

is lower than r_{ds3} by a factor of (1+T) which is typically lower than R_o. As an example. in SIGMOS technology. to drive a 50Ω load. $W_3 \approx 500\mu m$. $r_{ds3} \approx 120\Omega$ and $r_o \approx 20\Omega$! It is therefore not possible to design R_F to match the output impedance to R_o. An alternative will be discussed in the next section. The circuit configuration discussed can be used as an on-chip wide-band amplifier where only the input impedance needs to be matched. The low output impedance is good for driving on chip capacitive loads.

4.5. An Alternative

Fortunately, a MOS device is voltage controlled. With reference to Fig.4.5.1. consider voltage v_3. which is required to provide an output v_o' analyzed in the previous section. With matching devices between stage M3 and M5. the same v_3 should produce an identical v_o. Thus v_o/v_1 has the same relationship as v_o'/v_1. But now. the output impedance looking into v_o is r_{ds5}. which is larger than R_o. It is then possible to applied an additional resistive shunt feedback from v_o to v_1 to achieve impedance matching at both the input and output

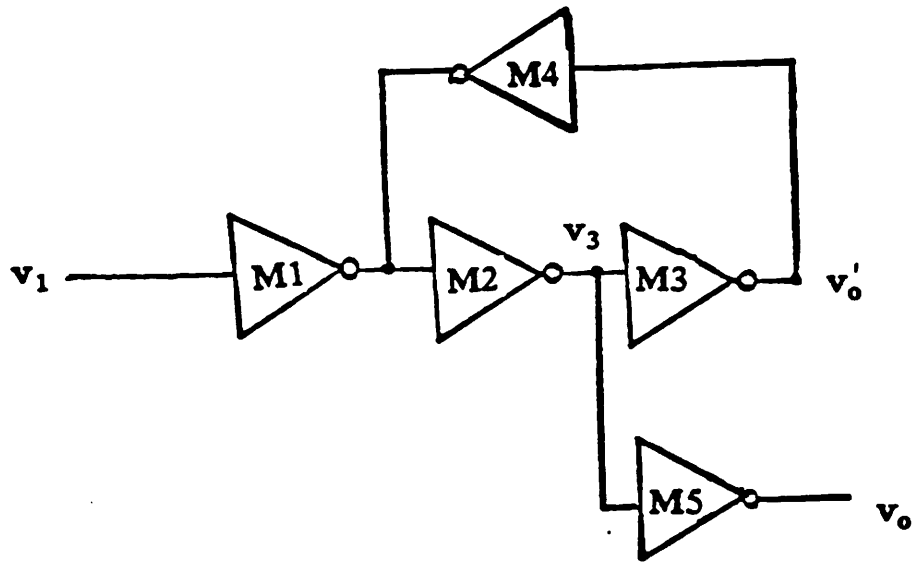


Fig.4.5.1 An alternative circuit

nodes according to the design procedures outlined in section 4.3.

Fig.4.5.2(a) shows the ac circuit of a test circuit based on this principle. Fig. 4.5.2(b) shows the full schematic of the test circuit. Note that stage M3 is not driving the 50Ω load and is made smaller and equal to W_4. $W_5 = 500\mu$ is chosen to provide sufficient drive to the 50Ω load with at least ±0.5V swing with less than 3% distortion in the worst case. $r_{ds\,5}$ is about 120Ω in SIGMOS technology but is typically at least a factor of two higher in other technologies. W_2 is made equal to the sum of W_3 and W_5. R_L' is added to M3 to provide similar loading effect to M3 as seen by M5 but scaled by a factor of W_5/W_3 for matching purposes. i.e.

$$R_L' = \frac{W_5}{W_3}\frac{R_o R_F}{R_o + R_F}$$

g_m in equation 4.3.8 is then given by

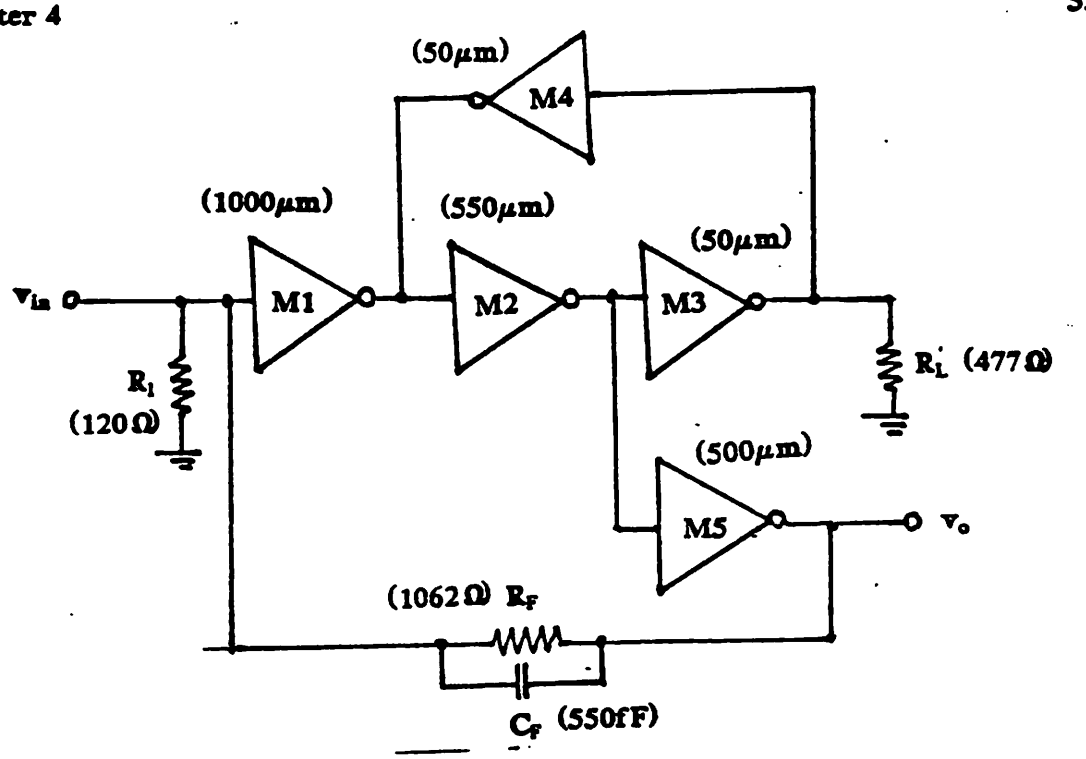


Fig. 4.5.2(a) AC equivalent circuit of the test circuit

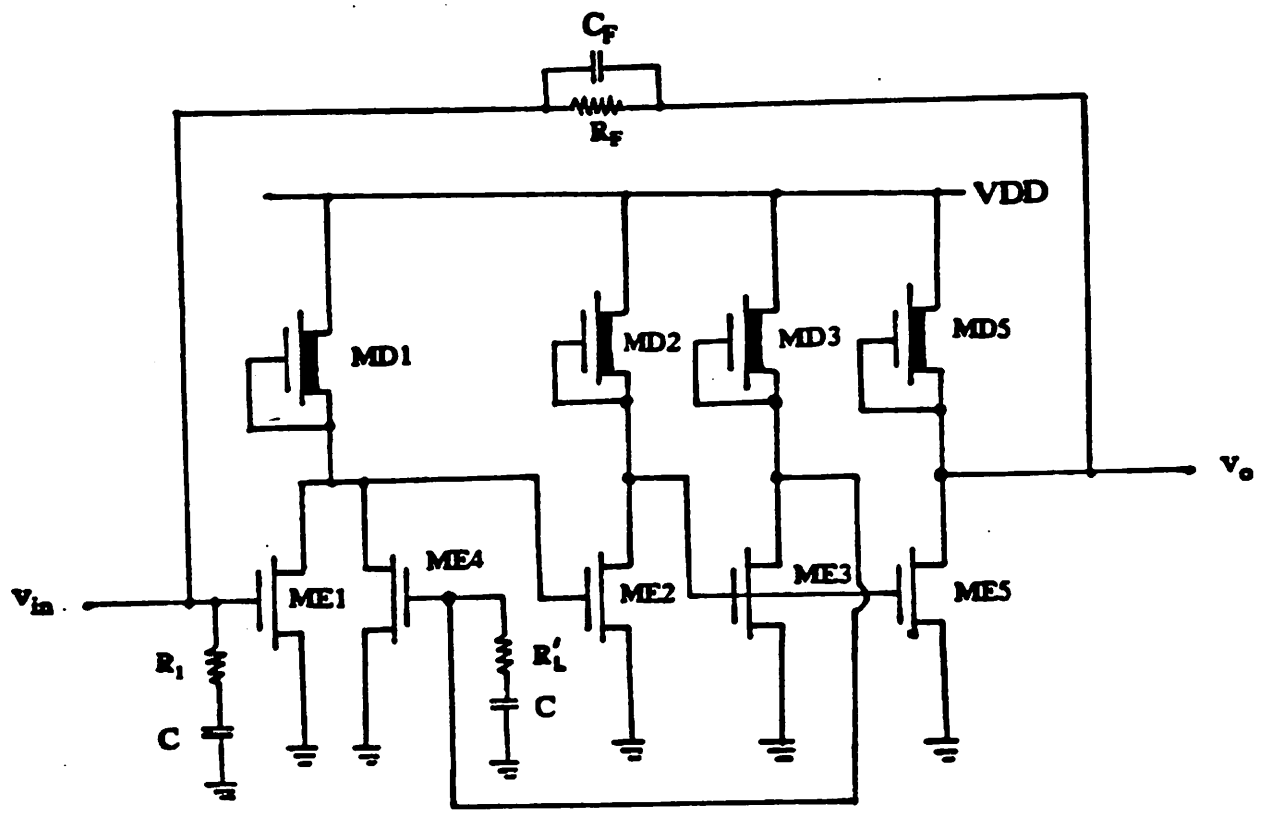


Fig.4.5.2(b) Full schematic of the test circuit

$$g_m = \frac{W_1}{W_4}\frac{W_5}{W_3}\frac{1}{R_L}\frac{1}{1+\frac{1}{T}} \qquad (4.5.1)$$

where $R_L = r_{o3} // R_L'$, and T is the loop gain of the circuit given in Eqn. 4.4.2 with R_L replacing r_{ds3}. R_F is determined to be 1062 Ω according to Eqn. 4.3.8. C_F is added to provide a feedback zero to widen the bandwidth. It is determined to be *550 fF* from simulation. The simulated amplitude response of the test circuit based on nominal SIGMOS device parameters (set A) is shown in Fig. 4.5.3. A bandwidth of slightly above 1 GHz and an insertion gain of 19 db are expected. More simulated results will be presented in Chapter 5. Field polysilicon is chosen to realize R_F instead of N^+ diffusion because of the lower parasitic capacitance. The effect of additional phase shift in R_F is simulated by representing it as a distributed RC network. The phase shift does degrade the frequency response: the bandwidth is reduced and the gain is peaking slightly. $VSWR_{in}$ has increased slightly also. These results are illustrated in Fig. 4.5.3 and Fig. 4.5.4.

4.6. Amplifier Package

Due to high power consumption (about 1 watt) and high frequency nature of the amplifier, the amplifier is carefully mounted on a microwave package as shown in Fig.4.6.1. Chip size is 1.3 mm x 1.3 mm, including bonding pads and scribe lines. The package material is aluminum. As the substrate of the chip is to be biased at -5V, it must be isolated from the case. This is achieved by placing it on a MOS capacitor and the capacitor oxide provides the necessary isolation. Also the thin oxide and the silicon bulk of the MOS capacitor provide a low thermal resistance path from the chip to the case. The capacitor is in turn secured directly onto the aluminum block with silver epoxy, chosen for its good electrical conductivity and thermal conductivity. Fig.4.6.2 shows the printed circuit board used for the testing. The board is made of teflon loaded fiber and the printed lines are gold plated for wire bonding purpose. The bottom of the circuit board serves as a ground plane and is secured onto the case for good grounding. The ground from the top is connected to the bottom via plated through holes. The center ring is one of these holes.

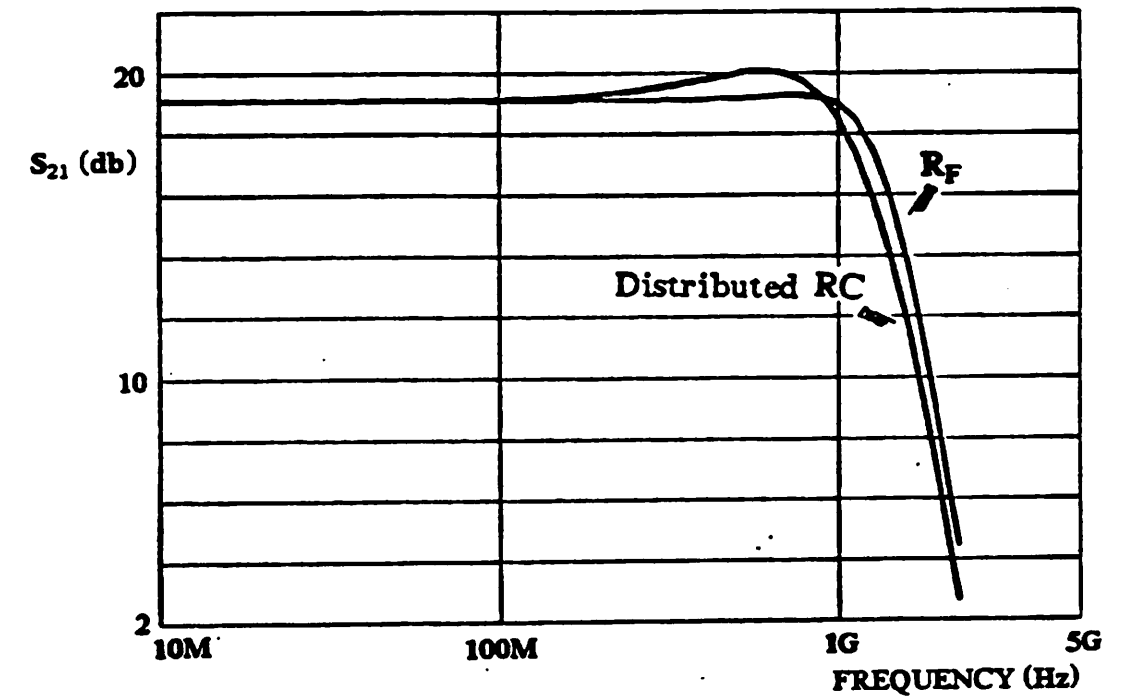


Fig. 4.5.3 Insertion gain of test circuit with and without distributed R_F

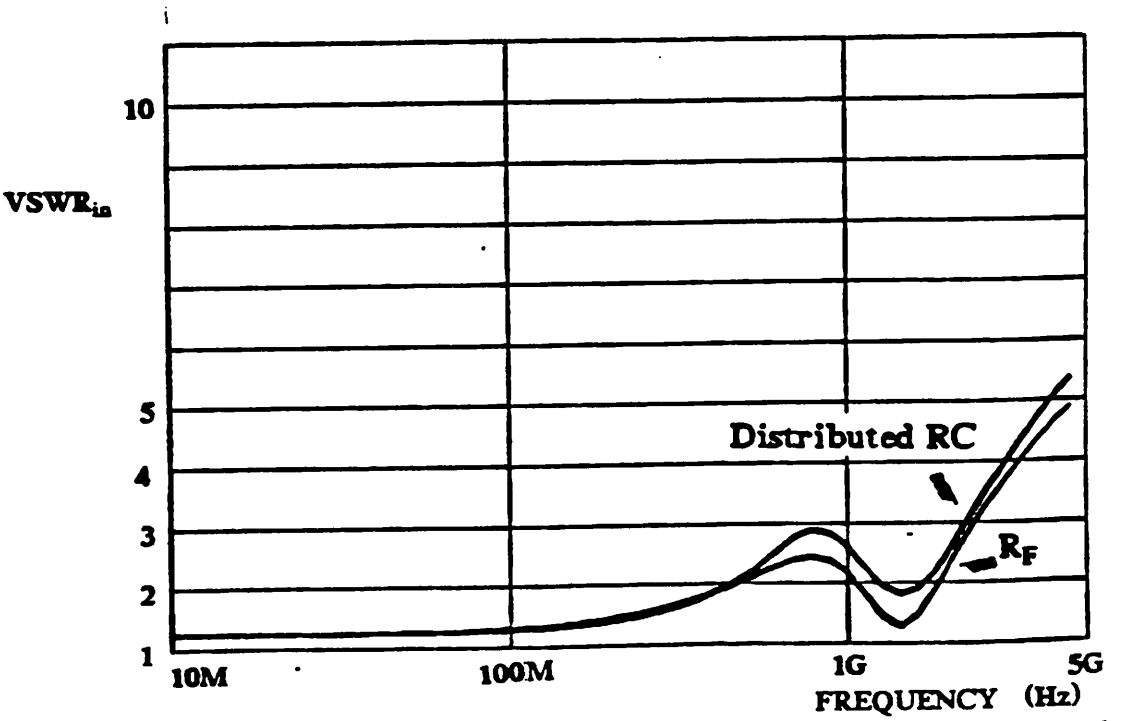


Fig.4.5.4 $VSWR_{in}$ of test circuit with and without distributed R_F

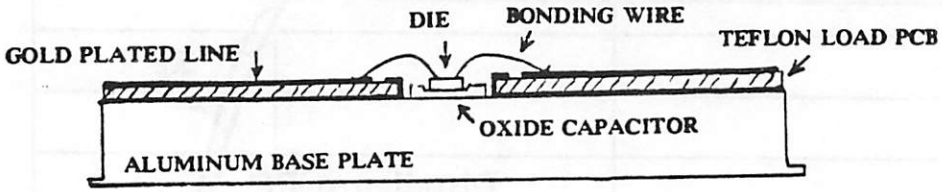


Fig.4.6.1 Microwave package for the amplifier

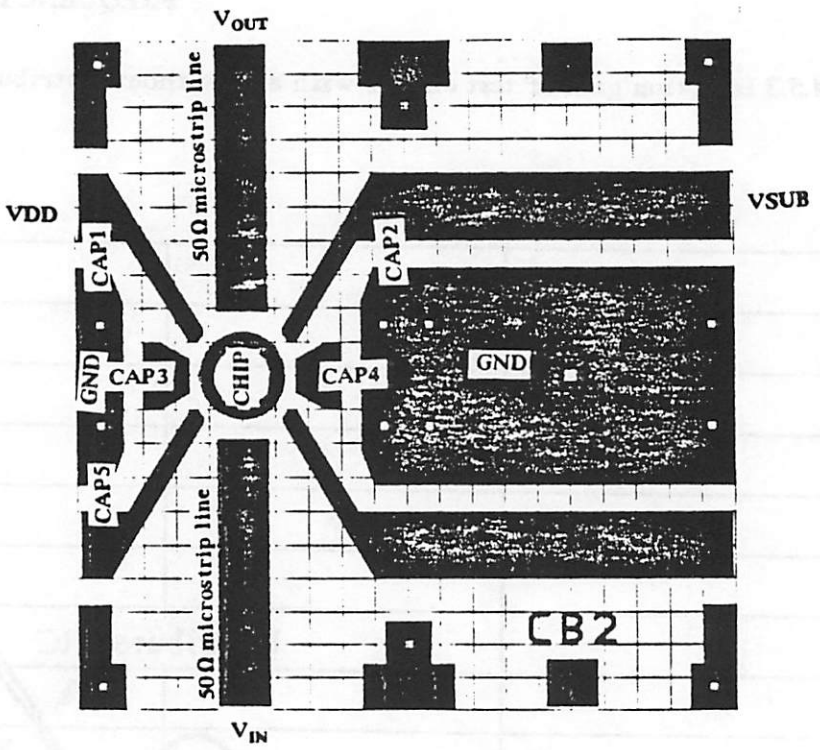


Fig. 4.6.2 Art work for the teflon loaded PCB

The input and output lines are 50Ω microstrip lines. The ϵ_r of the PCB used is 2.5. board thickness t is 1/32" and the line width for 50 microstrip is calculated to be 0.08" [20].

A die photo of the test circuit is shown in Fig. 4.6.3. The circuit is laid out with two fold symmetry. Ground pads are located on all four sides of the chip and bonded to the center ground ring on the PCB to minimized ground lead inductance and for shielding between signal wires. The total ground lead inductance is estimated to be 0.3nH. Chip capacitors for power-line decoupling and AC coupling to ground are placed at locations shown in Fig. 4.6.2. The package for the amplifier is actually a four terminal package: VDD, VSUB, V_{IN} and V_{OUT}. The other leads were included for other purposes, such as bias voltage monitoring.

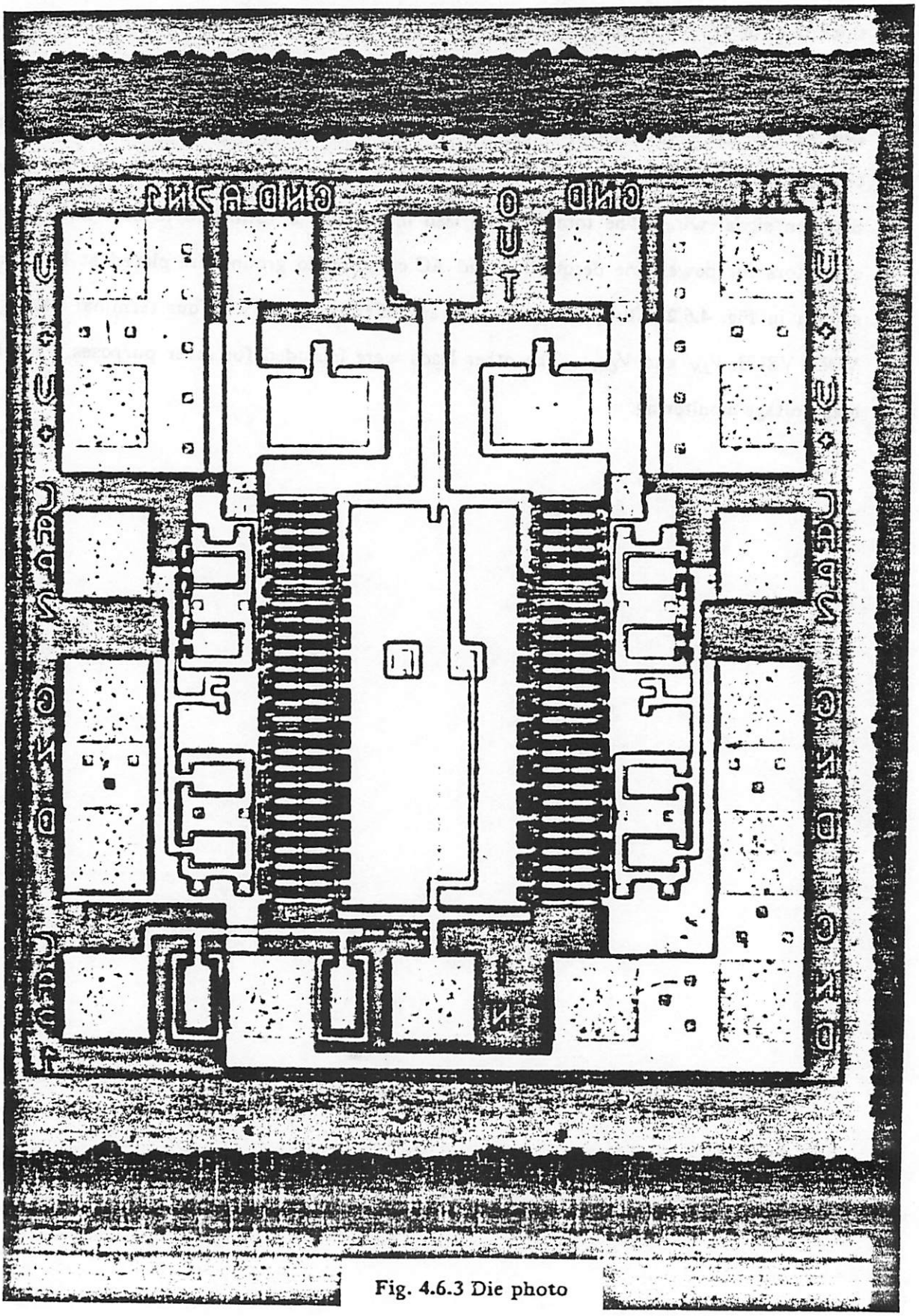


Fig. 4.6.3 Die photo

CHAPTER 5

MEASUREMENT RESULTS AND DISCUSSIONS

5.1. Introduction

The test circuit shown in section 4.5 was fabricated in 1μm SIGMOS technology at AT&T Bell Laboratories, Holmdel, NJ. Device characteristics taken from this particular run have been discussed and SPICE level 3 model parameters (set B) have been tabulated in Chapter 2.6. There are several process related problems with this particular run. The threshold voltages of the enhancement and depletion devices are 0.7V and -2.3V instead of 1.0V and -1.5V respectively. The problem was due to incorrect ion implant voltages. Device characteristics and circuit performance are degraded as a result and the supply voltage must be increased to 6V for proper operation. The dielectric layer of the capacitor is thinner than expected and the capacitance per unit area is increased by about 55%. The bandwidth of the amplifier thus shrinks significantly due to excessive frequency compensation.

In this chapter, measured and simulated amplifier characteristics are presented. Predictions of circuit performance in other submicron MOS technologies will be discussed. The frequency response of the packaged amplifier was measured with a HP 8510A Vector Network Analyzer*, and a HP 8756A Scalar Network Analyzer. The amplifier noise figure was measured with a HP 8970A Noise Figure Meter*.

5.2. Measurement Results

The S parameters of the amplifier were measured with a HP8510 Vector Network Analyzer. The measurement procedures are as follow:

1. Calibrate short circuit terminations:
2. Calibrate opened circuit terminations:

* Courtesy of Microwave Semiconductor Division of Hewlett Packard Co. at San Jose, Ca.

3. Calibrate 50Ω terminations:

4. Calibrate 50Ω through line:

5. Measure S parameters with amplifier in place.

The frequency range used is from 45 MHz to 1.5 GHz. The lower limit is set by the equipment and the upper limit is chosen to be consistent with the upper limit of the Noise Figure Meter. The frequency response below 45 MHz is essentially flat as confirmed by measurements taken with a HP 8756A Scalar Netwrok Analyzer down to 10 MHz. Open, short, and 50Ω terminations are all laid out on an identical circuit frame with the same number of bonding pads and supplies lines and packaged identically as the amplifier chip itself. Fig. 5.2.1 shows the measured (solid line) and simulated (dotted) insertion gain of the amplifier. The midband insertion gain is 16.35 db and the -3db frequency is at 758 MHz. Fig.5.2.2. shows the input VSWR. It is 1.38 at low frequency and less than 2.45 at 758 MHz. Fig. 5.2.3 shows the reverse transmission gain. It is less than -30db at midband and less than -25db at 758 MHz. Fig. 5.2.4 shows the output VSWR. It is 1.30 at low frequency and less than 1.60 at 758 MHz. Fig.5.2.5 shows the noise-figure measurement. An expanded view of the noise measurements on linear-linear scale is shown in Fig. 5.2.6. The average noise figure from 10 MHz to 758 MHz is 6.7 db. Insertion gain can also be measured by the noise figure meter. This is the raw or actual insertion gain as the package effects are included. The measurement result is shown in Fig. 5.2.7. The -3db frequency is at about 600 MHz. It appears that there is an uncertainty in the gain measurement of about 1 db between the noise figure meter measurement and the vector network analyzer measurement which could be due to instrumentation and/or calibration errors.

As can be seen, the simulated and measured data agreed very well within the -3 db frequency band. The higher than expected $VSWR_{in}$ and $VSWR_{out}$ at midband are due to lower amplifier gain caused by degraded device characteristics, and hence an increase in the impedance at midband. Note that both $VSWR_{in}$ and $VSWR_{out}$ are roughly equal at midband even under such adverse conditions, confirming the advantage of including R_1 as dis-

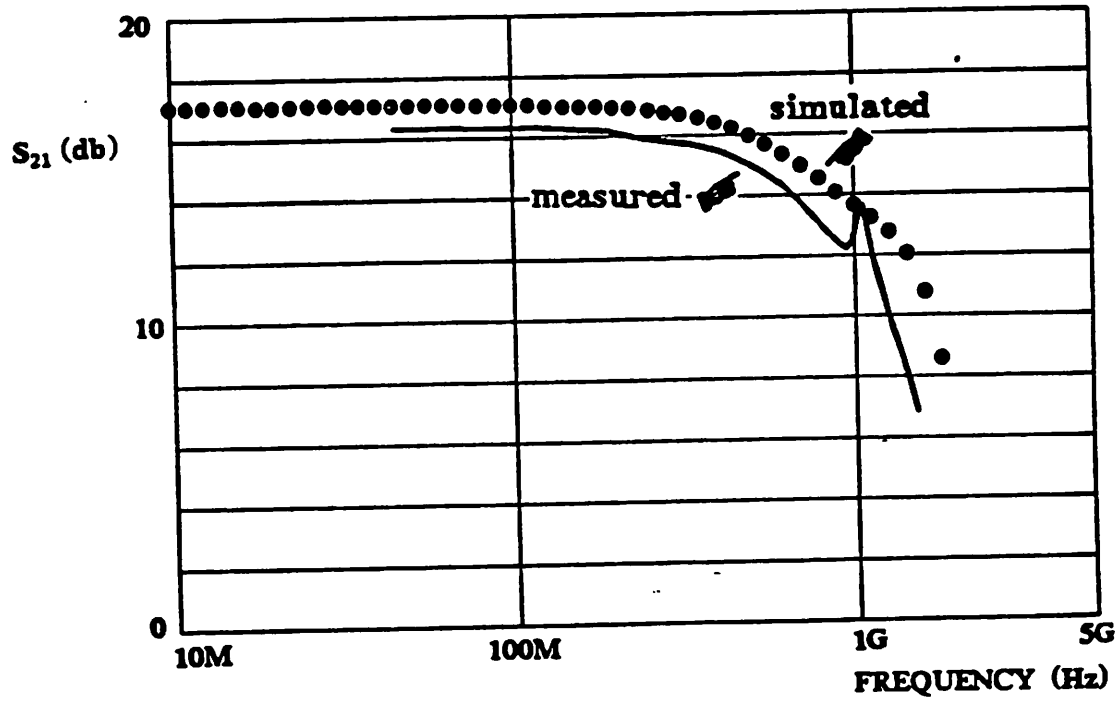


Fig.5.2.1 Insertion gain

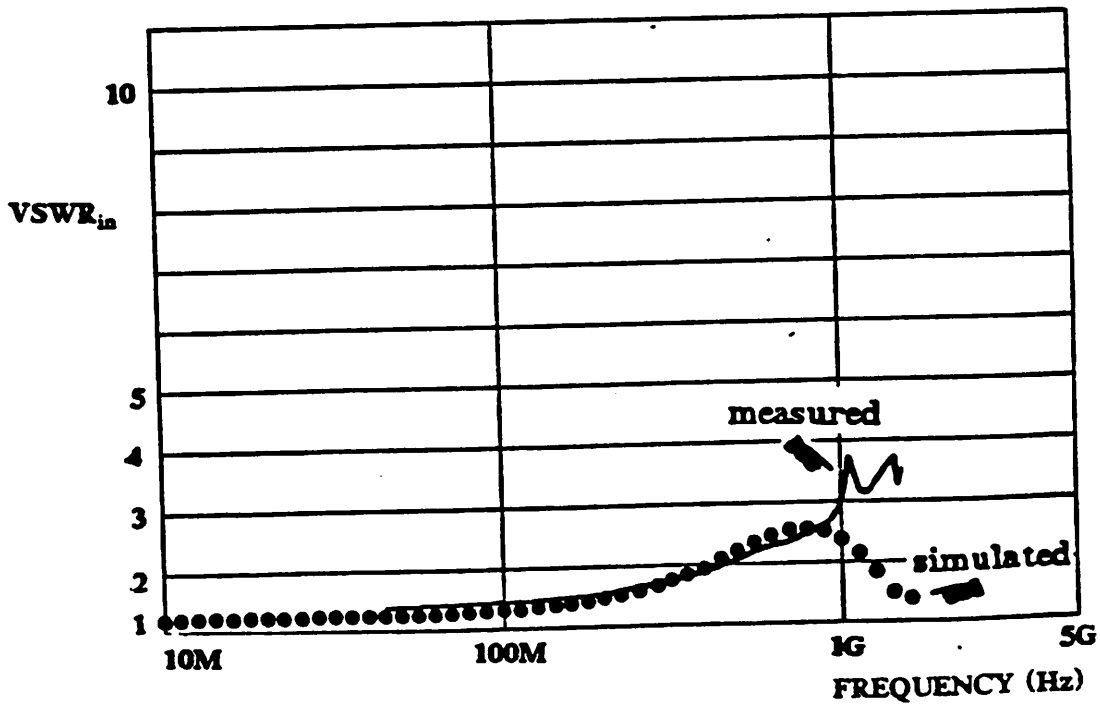


Fig.5.2.2 Input VSWR

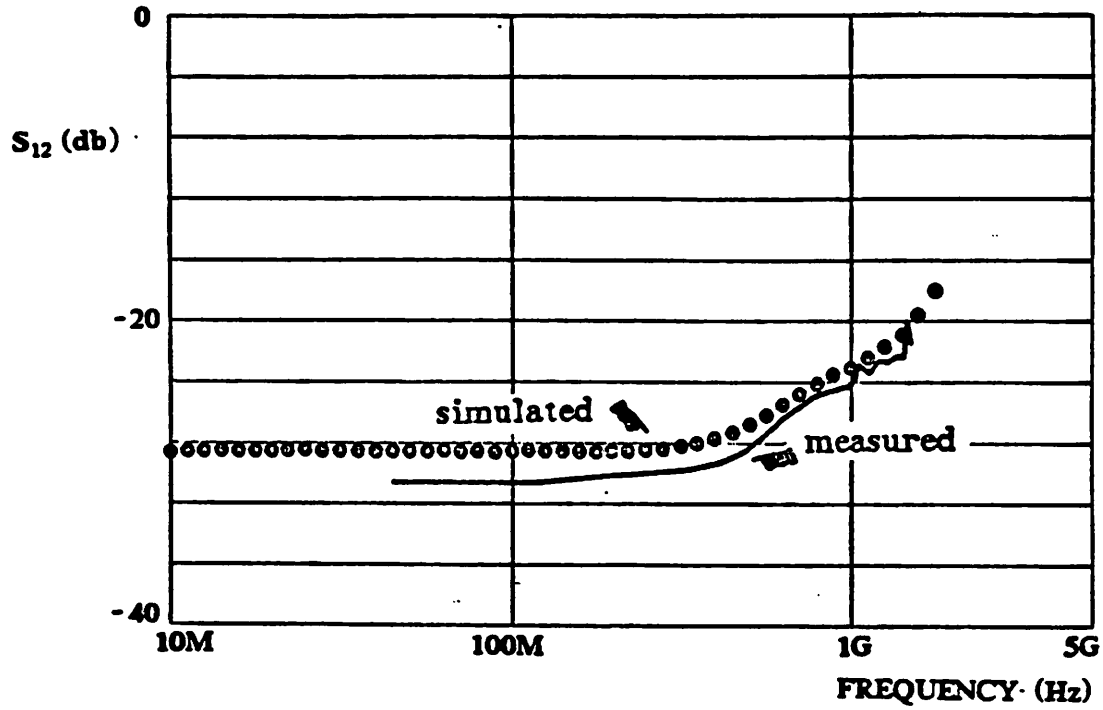


Fig.5.2.3 Reversed transmission gain

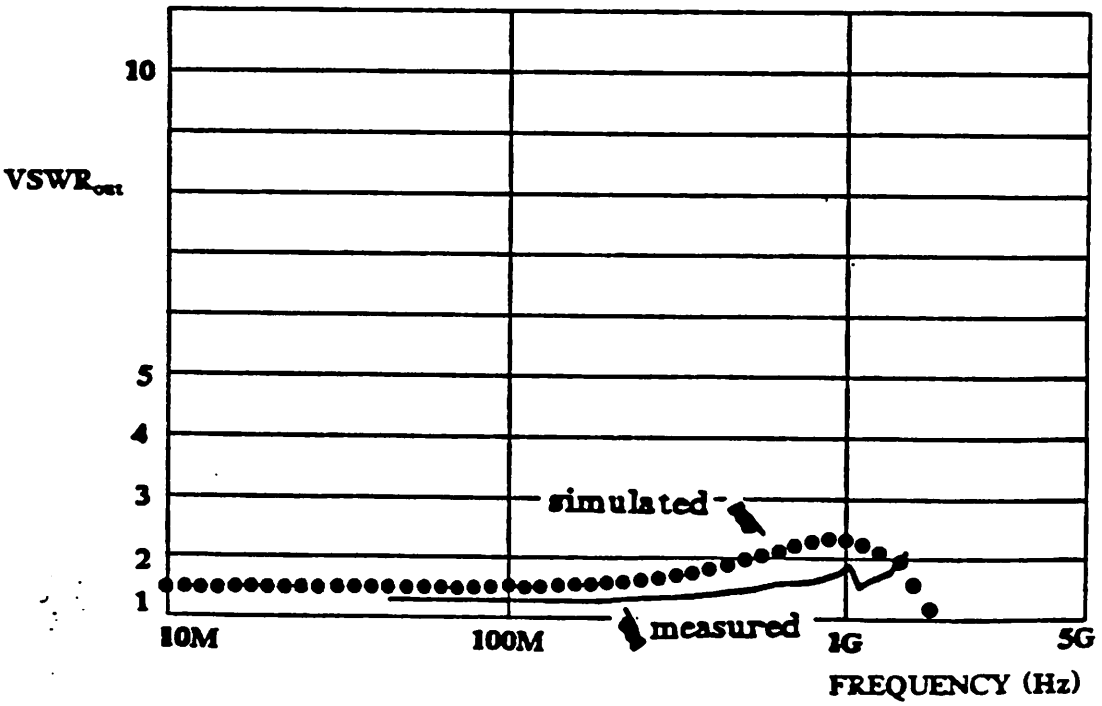


Fig.5.2.4 Output VSWR

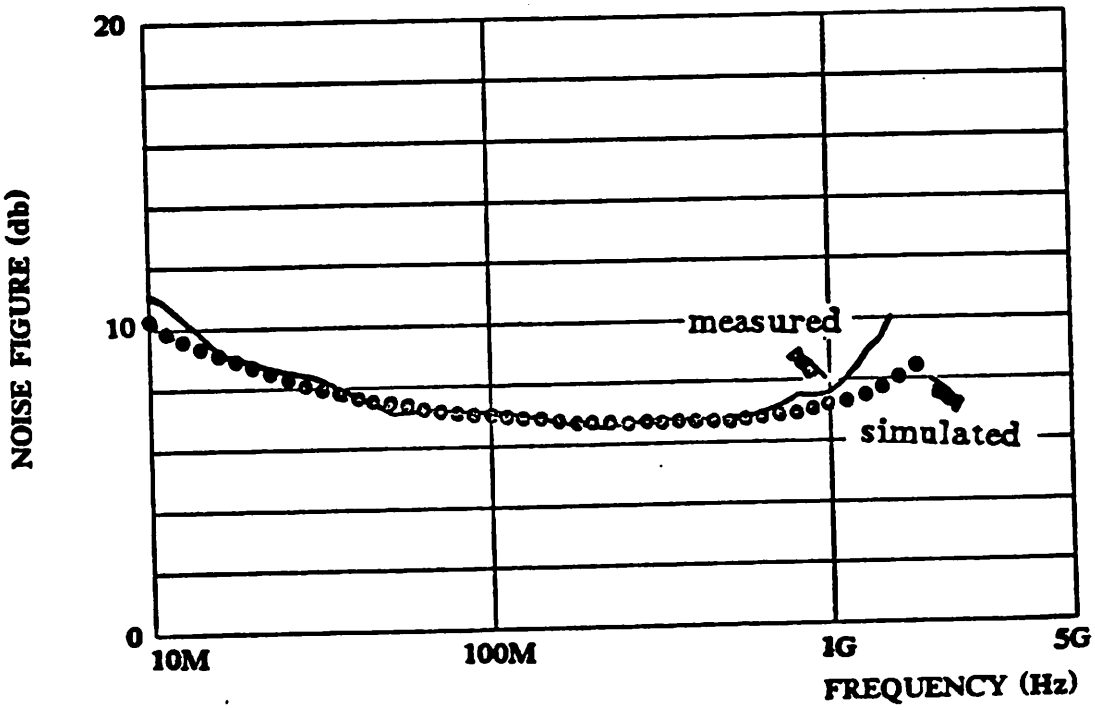


Fig.5.2.5 Noise figure (db-log scale)

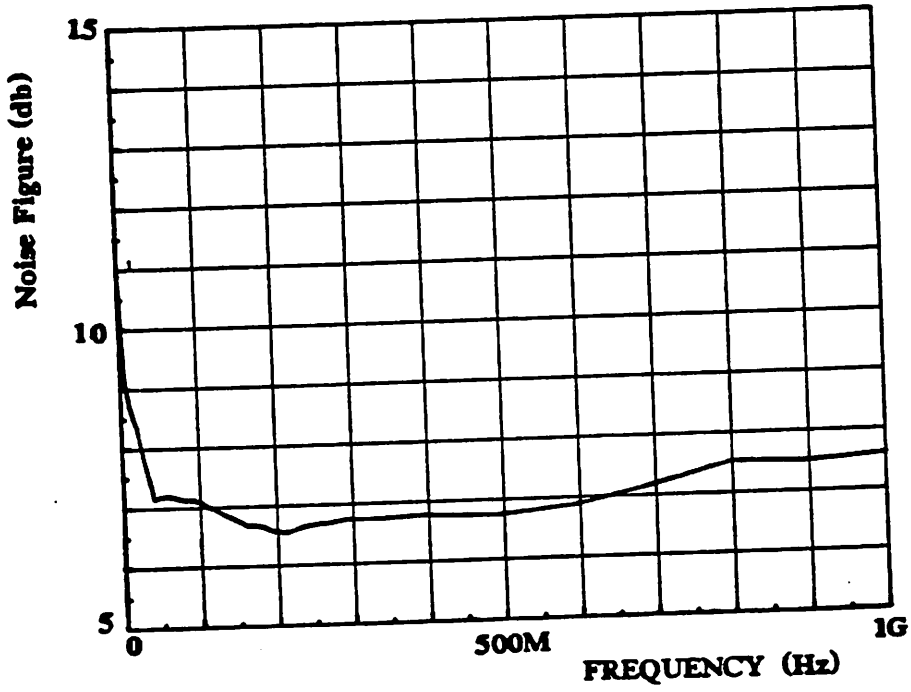


Fig.5.2.6 Noise figure (linear-linear scale)

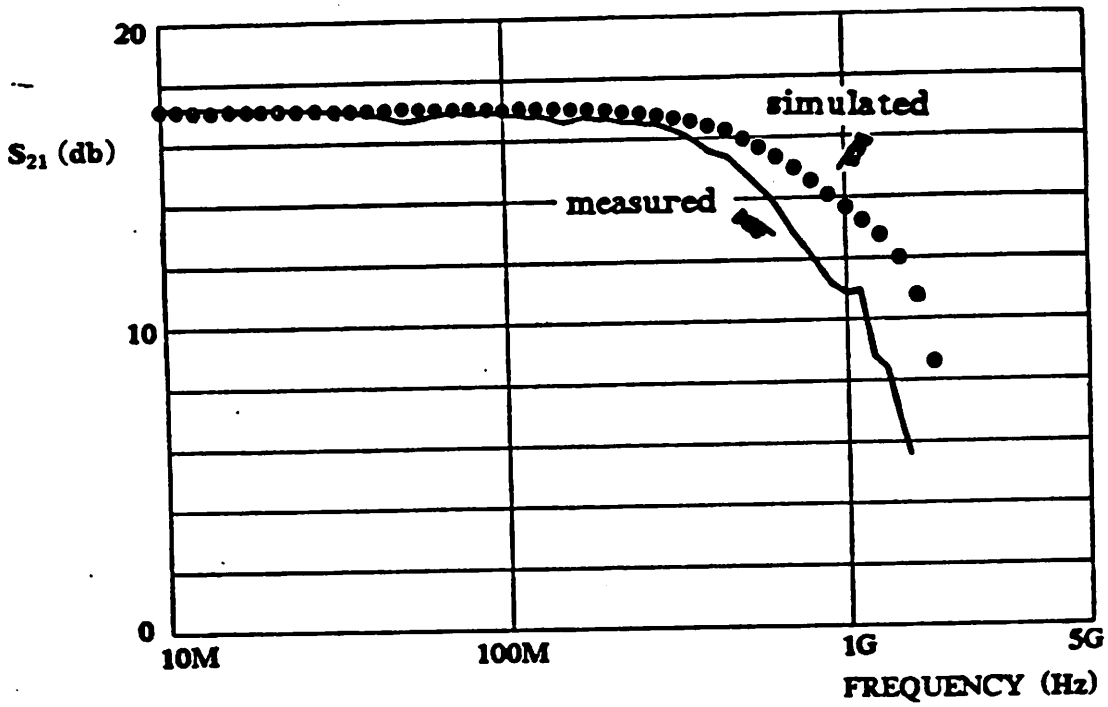


Fig. 5.2.7 Insertion gain measured by Noise Figure Meter

cussed in section 4.3. If the amplifier gain had been correct, or R_F could be trimmed lower, the midband VWSR for both input and output would have been much lower.

For completeness, a full set of amplitude and phase measurement of the S parameters are shown in Fig. 5.2.8 to Fig. 5.2.12 in various forms obtained directly from the vector network analyzer measurements. Amplitude and phase measurements of s_{21} are shown in Fig. 5.2.8. $VSWR_{in}$ is shown in Fig. 5.2.9(a) and the complex input admittance is shown in Fig. 5.2.9(b). $VSWR_{out}$ is shown in Fig. 5.2.10(a) and the complex output admittance is shown in Fig. 5.2.10(b). A polar plot of s_{21} is shown in Fig. 5.2.12. At midband, the input impedance is equivalent to 69Ω in parallel with 3.9pF, the output impedance is equivalent to 64.4Ω in parallel with 1.1pF. The reason for the higher resistive components has been discussed earlier in this section. The input capacitance (C_{in}) of the amplifier is unexpectedly high causing $VSWR_{in}$ at the edge of the band to be greater than 2. This is due to the unexpected high C_{gd}, a new short channel effect described in [22].

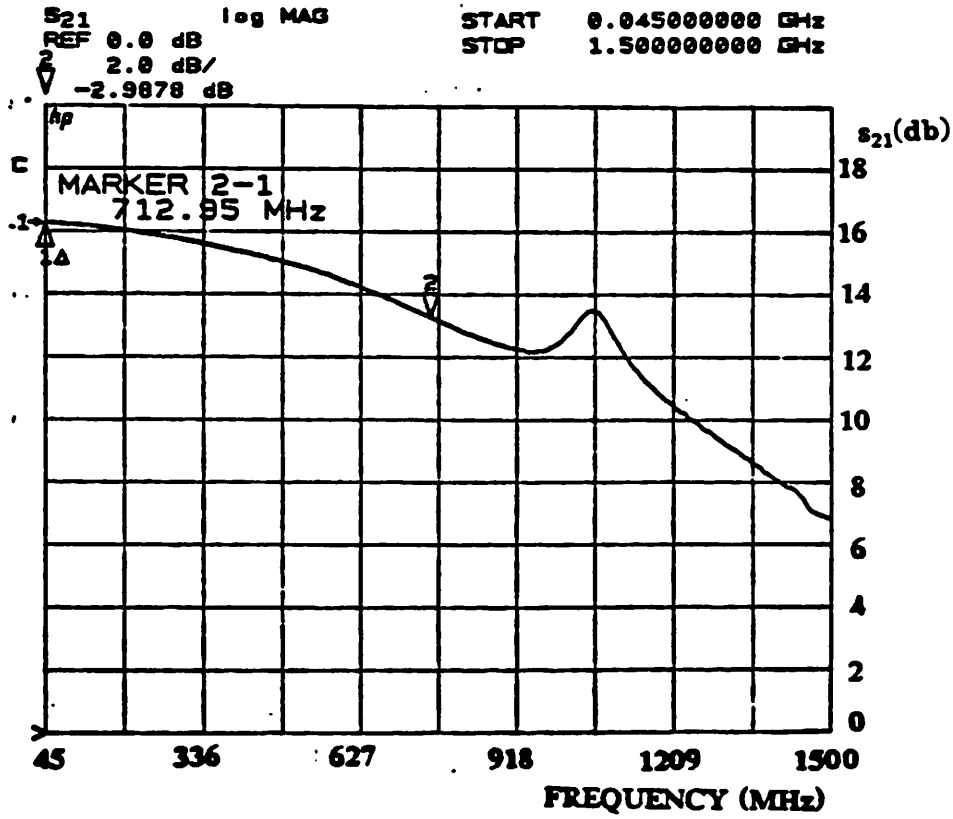


Fig. 5.2.8(a) s parameter measurements: amplitude of s_{21}

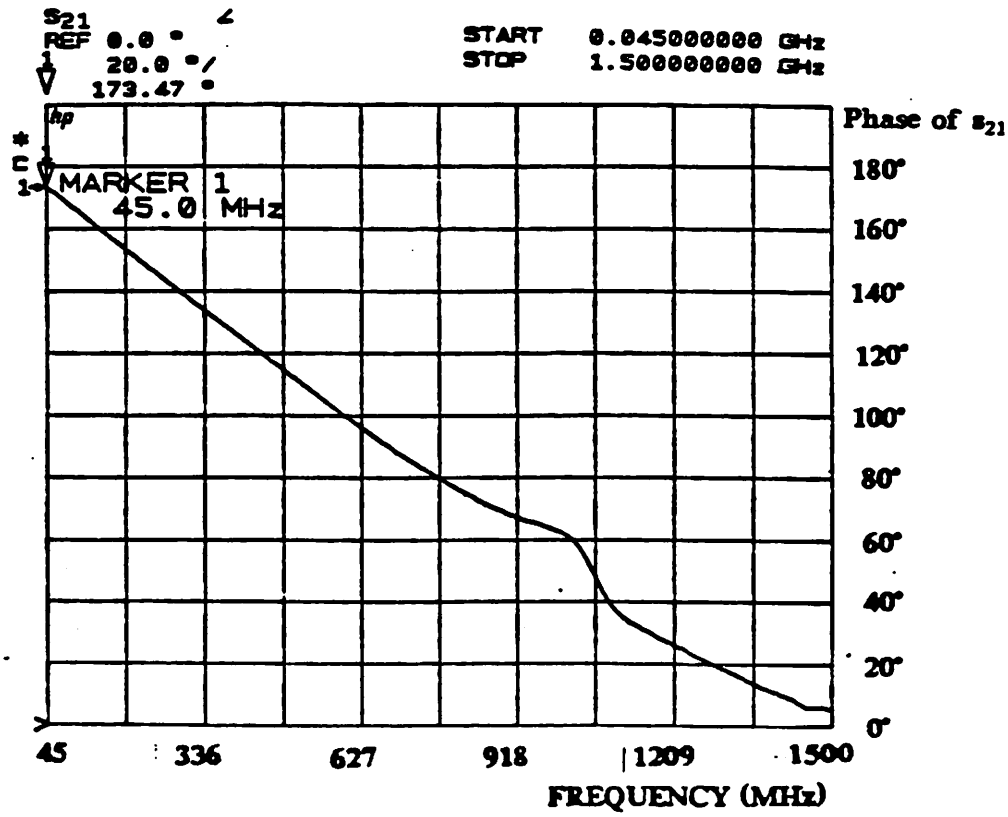


Fig. 5.2.8(b) s parameter measurements: phase of s_{21}.

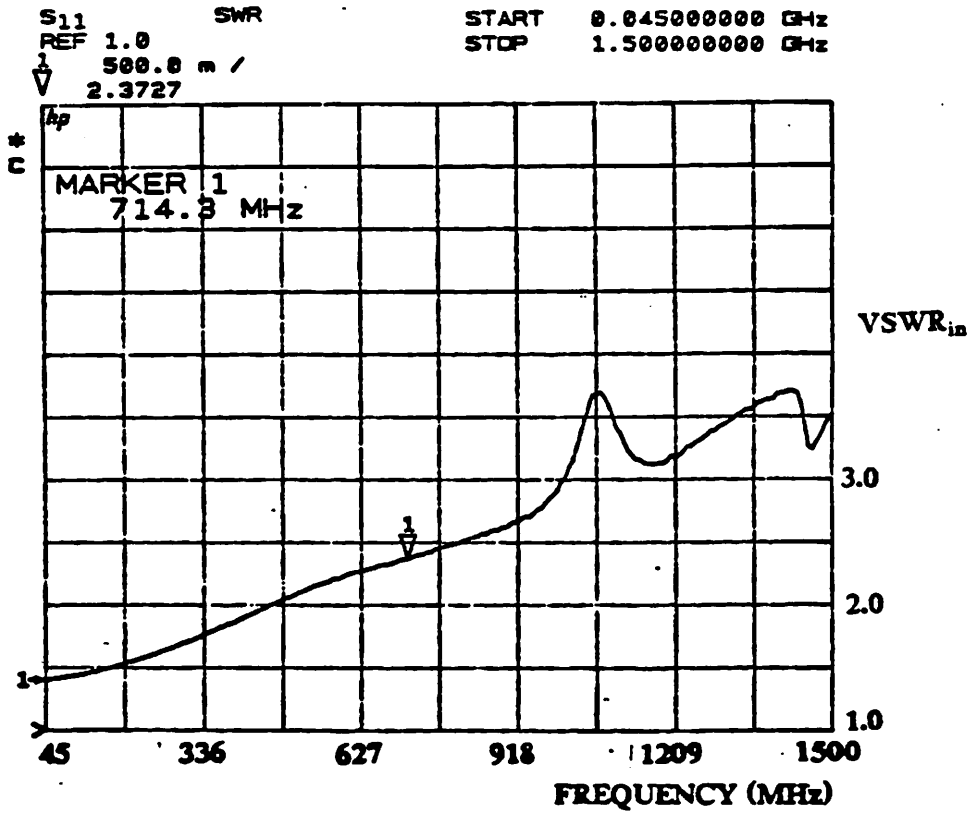


Fig. 5.2.9(a) VSWR$_{in}$

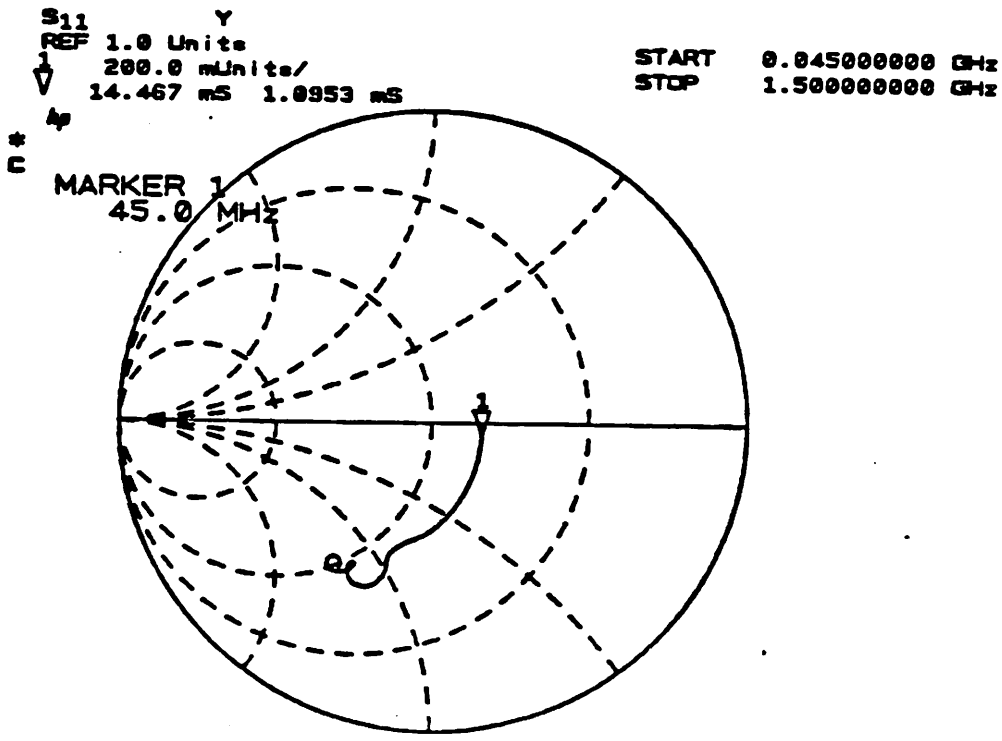


Fig. 5.2.9(b) Complex input admittance

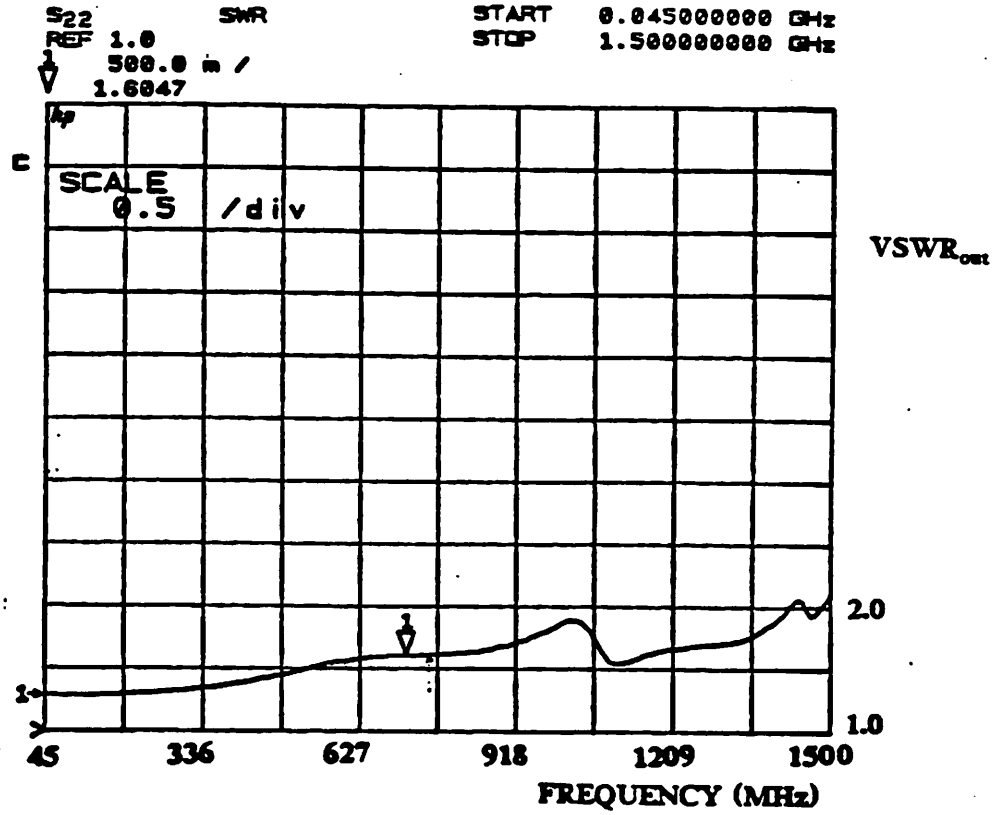


Fig. 5.2.10(a) VSWR$_{out}$

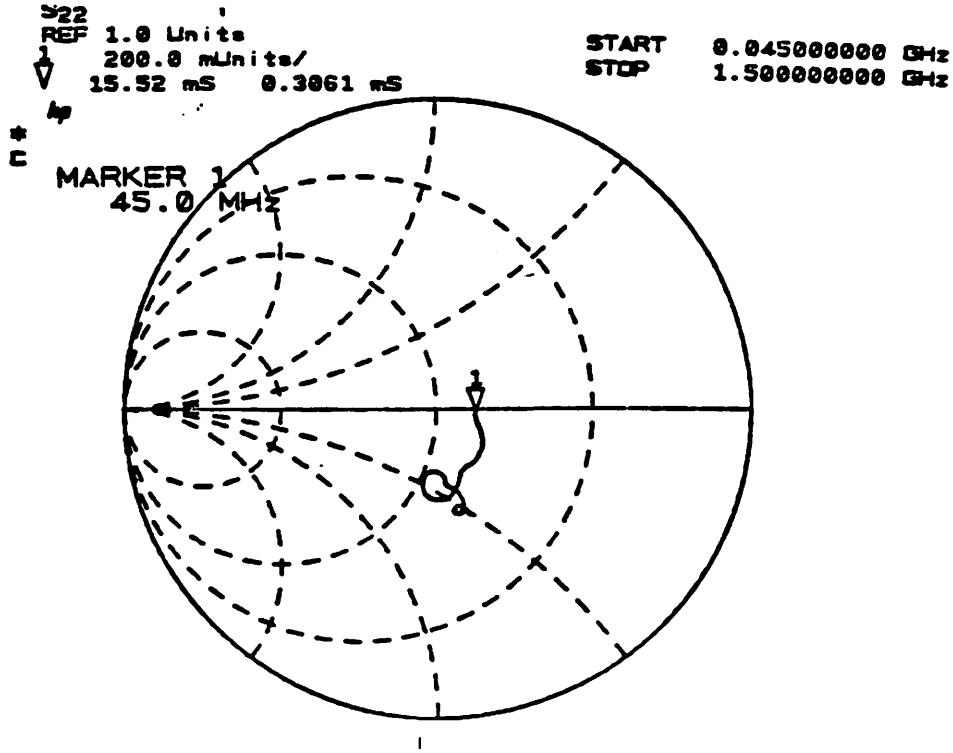


Fig. 5.2.10(b) Complex output admittance

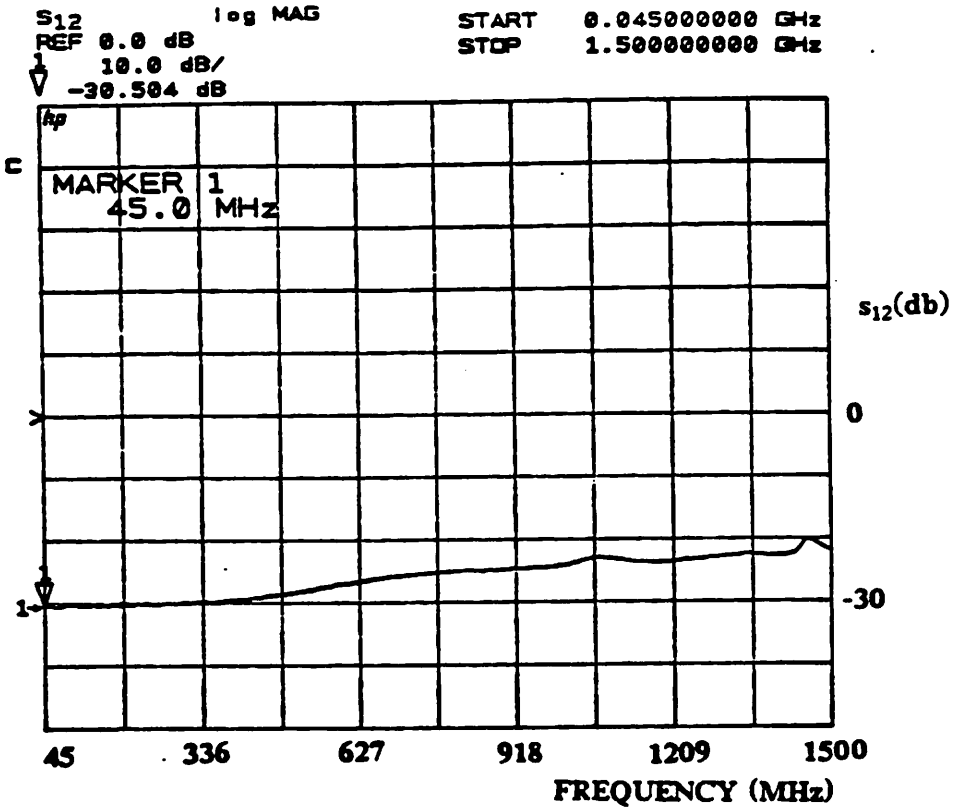


Fig. 5.2.11(a) s parameter measurements: amplitude of s_{12}

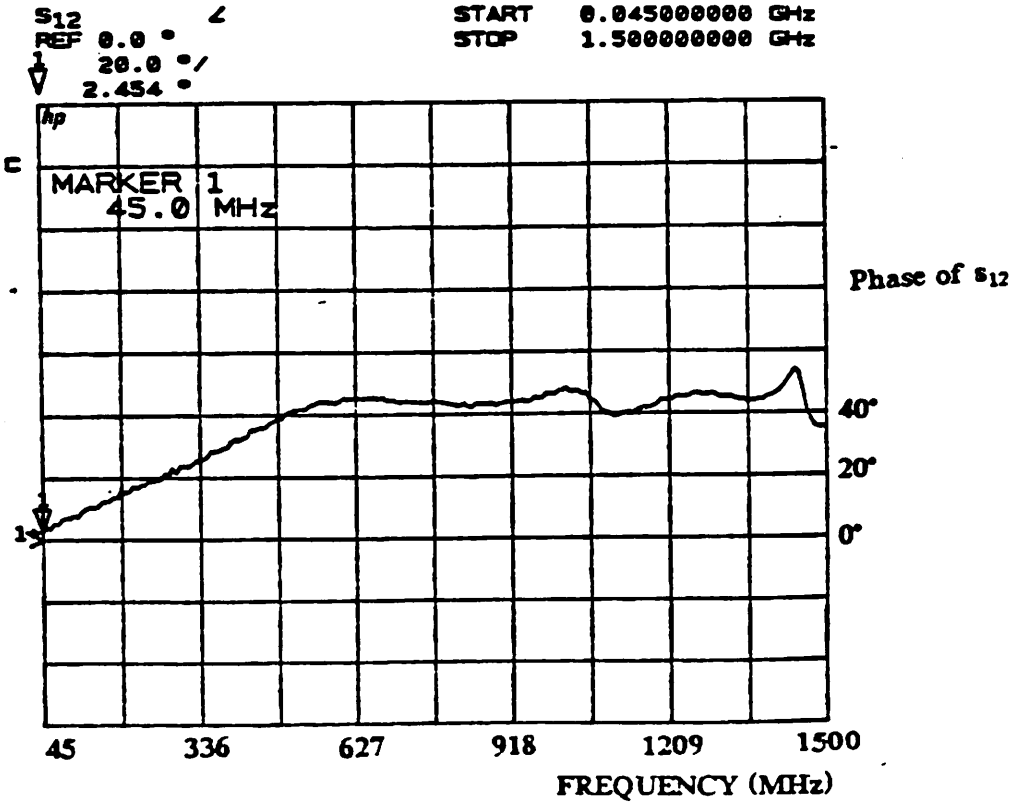
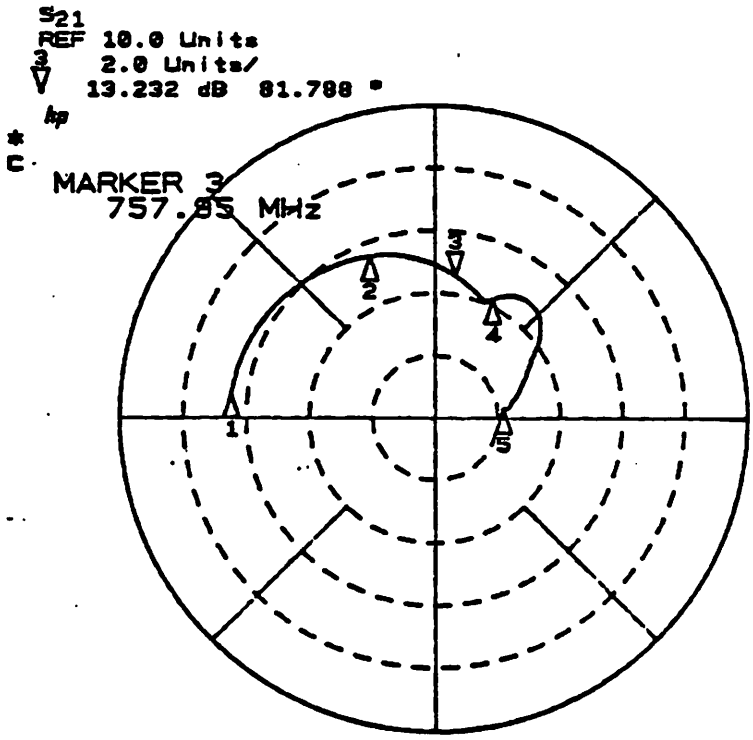


Fig. 5.2.11(b) s parameter measurements: phase of s_{12}.



MARKER	FREQ.(GHz)
1	0.045
2	0.500
3	0.758
4	1.000
5	1.500

Fig.5.2.12 Polar plot of insertion gain

$$C_{in} = C_{gs(sat.)} + (1 + |A_{v1}|)C_{gd} + C_s$$

C_s is due to other stray capacitances not accounted for, including capacitances that are not compensated completely with the calibration measurements due to unavoidable differences in the layout used in the calibration chips.

$$C_{gs(sat.)} \approx C_{gsov} + 0.7C_{ox} W L_{eff} + C_{gsf}$$

where the last term is due to the fringing field.

$$C_{gd} \approx C_{gdov} + \zeta C_{ox} W L_{eff} + C_{gdf}$$

where the second term is due to short channel effect and the last term is due to fringing field. From recent work [23], ζ is found to be about 10% for a 1μm device. As a result, the Miller capacitance reflected to the input has been increased. All of the above, not including C_s, amounted to 3.2pF instead of 2.2pF estimated from the classical capacitance model. This is a significant increase and should be taken into account in future design.

5.3. Performance Comparisons

The performance of the amplifier tested is summarized in Table 5.3.1. The performance of other commercially available wide-band amplifiers fabricated in other IC technologies are tabulated in Table 5.3.2 for comparisons. It can be seen that despite the various disadvantages in the SIGMOS technology as compared to other technologies such as microwave BJT and GaAs MESFET/HEMT, the performance of the test circuit is fairly comparable with the commercial products in the specifications shown.

With improved process control, simulations indicate that a gain of 19 db. and a bandwidth of about 1.2 GHz is possible with the SIGMOS technology.

5.4. Discussions

It is interesting to estimate quantitatively the performance of the circuit in other MOS technologies. For process with silicide gate, the noise figure could be expected to be

Specifications	Measured
Insertion gain (db)	16.3
BW_{-3db} (MHz)	758
$VSWR_{in}$	<2.45
$VSWR_{out}$	<1.6
NF (db)	6.7

Table 5.3.1 Performance summary of test circuit

Company	Part No.	Freq.(MHz)	Gain(db)	NF(db)	Dated
Avantek	GPM-552	5-500	37	4.5	July 1986
Avantek	GPM-1052	5-1000	23.0	7.0	July 1986
Avantek	PPA-1005	5-1000	12.6	6.0	July 1986
Aydin Vector	MHT-1075	5- 500	20.0	3.0	July 1986
Aydin Vector	MHT-1013	5-1000	14.5	3.3	July 1986
HP	HP8447A	0.1- 400	20.0	5.0	before 1984
HP	HP8447D	0.1-1300	26.0	8.5	before 1984

Table 5.3.2 Partial specifications of commercial wide-band amplifiers

about 5 to 5.5 db due to the reduction of gate resistance. Most modern MOS short channel technologies have higher r_{ds} per unit width than the SIGMOS technology. This will allow a larger R_1 at the input and reduce the noise level of the amplifier further. r_{ds} could be increased by reducing source/drain junction depth and/or with retrograded substrate doping profile. A factor of two increase in R_1 would reduce the noise figure by about 1db. A combination of the two would bring the noise figure down to the 4.5 db range. Modern submicron MOS technology often has self-aligned silicide source/drain, which will increase the effective g_m and reduce source/drain resistance, both will reduce device noise. The frequency response is expected to improved as well, since the minimum gate width per segment can be increased, thereby reducing the parasitic capacitance at the output node of the gain stages. For shorter channel length without scaling the gate oxide thickness, g_m per device width is increased and a smaller W may be used for the same g_m. This will reduce the input capacitance because of smaller W and L and therefore improve the high frequency input VSWR performance. Bandwidth is expected to increase inversely proportionally to L_{eff} In a fully scaled technology however, the gate capacitance will increase as well and the high frequency input VSWR wll not be improved as much. But because of reliability issues of thin gate oxide ($t_{ox} \ll 200$ Å), the trend toward scaling is such that the channel length is scaled more than the gate oxide thickness. It is therefore reasonable to expect that the amplifier performance in such a submicron technology will have gain in the 20db range, -3db frequency bandwidth in excess of 1 GHz, input/output VSWR of less than 2 and a noise figure of about 4 db.

Amplifier frequency response can also be improved by reducing the parasitic capacitance of the MOS device. An example of this device structure is reported in [21] and is shown in Fig. 5.4.1. The technology is known as COO MOS, contact over oxide MOS technology. Note that the source/drain area is on top of field oxide 1 and surrounded on 3 sides by field oxide 2. The source/drain capacitance is therefore mostly eliminated. With reference to Fig. 3.2.1, it is estimated that the total capacitance at node B is now reduced to about $1.5C_{ox}WL$ for the similar 1μm device, which is a 33% reduction. However g_m is

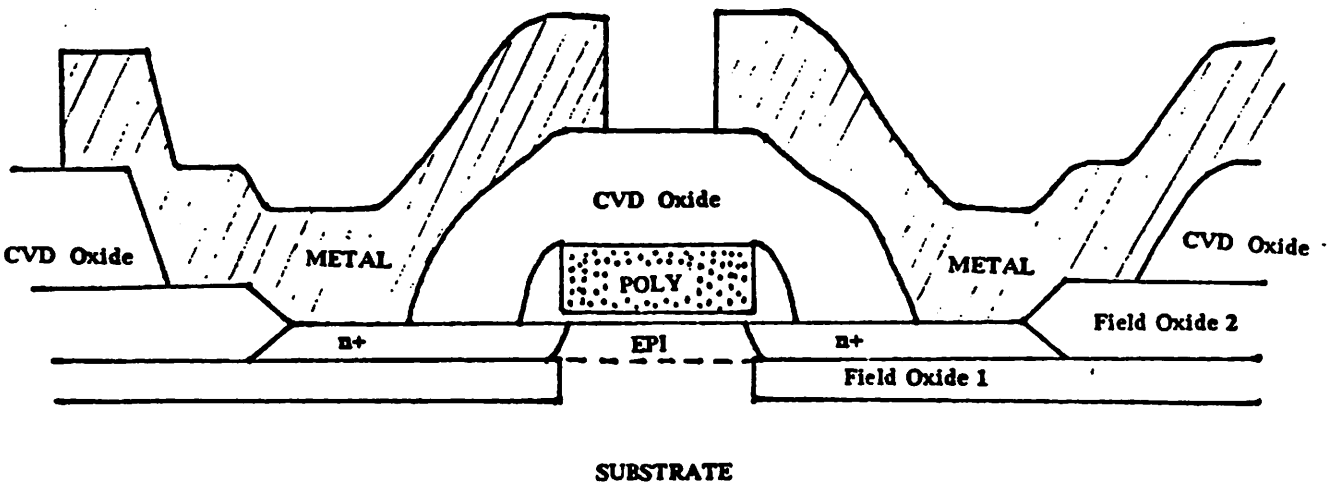


Fig. 5.4.1 Cross-section of a COO MOS device

degraded by 10% in this technology and therefore the gain bandwidth product. GBW is estimated to be about 23% higher. The bandwidth of the amplifier built in this technology is therefore expected to increase by about the same percentage (23%).

CHAPTER 6

CONCLUSIONS

Circuit design techniques for realizing wide-band, low-noise, matched impedance amplifiers in submicron MOS technology have been investigated and discussed. It is concluded that a resistive shunt-shunt feedback with a shunt terminating resistor at the input gives low-noise performance and good impedance matching in the present of low device output resistance. A new circuit configuration has been developed and fabricated in a 1μm NMOS technology. The measured amplifier performance is found to agreed closely with computer simulations. The amplifier has 16.35 db insertion gain, 758 MHz bandwidth, 6.7 db average noise figure (50 Ω source resistance). The input VSWR is less than 2.45 and the output VSWR is less than 1.60 from 10 MHz to 758 MHz. Improved circuit performance can be achieved through improvements in device structure and process technology such as reducing source/drain parasitic capacitance, increasing device output resistance, using polycide or silicide gate and self-aligned silicide source/drain. Two levels of metal and on chip capacitor are essential for high frequency, low-noise amplifier design in submicron MOS technology.

APPENDIX A

SIGMOS* PROCESS OUTLINE AND DESIGN RULES

A.1 Process Outline

1 Field Oxidation

1.1 Clean wafer, p type.
1.2 Oxidation, wet oxide, plus N_2 anneal. (Use dry-wet-dry sequence)

2 Field Implant

2.1 Blanket implant, B^{2+} implantation.
2.2 N_2 anneal.

3 Active Area (N2)

3.1 Resist coating, prebake.
3.2 Active mask (N2), expose, develop, postbake, descum.
3.3 Etch field oxide.
3.4 Remove resist.

4 Gate Oxide

4.1 Clean wafer.
4.2 Oxidation, 200Å, N_2 anneal.
4.3 Thin Poly CVD deposition, undoped.

Threshold Implant

5.1 Blanket implant, As^+.

6 Threshold Implant (N4)

6.1 Resist coating,
6.2 Enhancement IL mask (N4), expose, develop, postbake, descum.
6.3 B^+ implant.

* SIGMOS is a 1μm NMOS process of AT&T Bell Laboratories.

6.4. Remove resist.

7 Threshold Implant (N5)

7.1 Resist coating.
7.2 Depletion II mask (N5). expose. develop. postbake. descum.
7.3 As^+ implant.
7.4 Remove resist.

8 Backside Implant

8.1 Resist coating on front side.
8.2 B^+ implant on back of wafer.
8.3 Remove resist.

9 Buried Contact (N3)

9.1 Clean wafer.
9.2 Resist coating.
9.3 Buried contact mask (N3). expose. develop. postbake. descum.
9.4 Wet etch poly.
9.5 Wet etch 200Å gate oxide.
9.6 Remove resist.

10 Gate Poly (N6)

10.1 Clean wafer.
10.2 Poly CVD deposition.
10.3 Blanket implant. P^+.
10.3 Piranha clean.
10.4 100:1 HF dip.
10.5 Nitride CVD deposition.
10.6 Resist coating.
10.7 Gate mask (N6). expose. develop. postbake. descum.
10.8 Dry etch Nitride and dry etch Poly.
10.9 Remove resist.

11 Sidewall Oxide

11.1 Clean wafer.
11.2 Regrow sidewall oxide.

12 Source/Drain Implant

12.1 Blanket implant. As^+.
12.2 Nitride CVD depositon.

13 CVD Oxide

13.1 Phos. doped CVD oxide.
13.2 Densify and reflow.

14 Contact (N7)

14.1 Resist coating.
14.2 Contact mask (N7). expose. develop. postbake. descum.
14.3 Etch oxide. wet-dry sequence.
14.4 Remove resist.
14.6 Clean wafer.
14.7 Reflow.
14.8 Dry etch nitride.

15 Capacitor (N1)

15.1 Clean wafers.
15.2 Resist Coating.
15.3 Capacitor mask (N1). expose. develop. postbake. descum.
15.4 Wet etch oxide.

16 CVD Poly (*optional*)

16.1 Clean wafer.
16.2 Poly CVD. undoped.
16.3 PBr_3 predeposition. N_2 drive in.
16.5 Resist coating.
16.6 Remove junk on back of wafer: poly. CVD oxide. nitride. poly. gate oxide.
16.7 Remove resist.
16.8 Clean wafer.
16.9 Resist coating.
16.10 Metal 1 mask (positive). expose. develop. postbake. desum.
16.11 Dry etch poly.
16.12 Remove resist.

17 Metal 1 (N8)

17.1 Clean wafer.
17.2 Resist coating.
17.3 Metal 1 mask (Negative).
17.4 Develop and post-bake.
17.5 Metal deposition. E-Gun. Al with 1% Cu.

17.6 Resist lift off, in Acetone.
17.7 Dip wafer in cold Al etch for 30 sec.
17.8 Rinse and dry.
17.9 Forming gas sintering.

18 Polyimide (N9)

18.1 Spin on adhesion promoter and XU284 polyimide, Ciba Geigy.
18.2 Bake in oven, 85°C, 30 min., 150°C, 15 min., 240°C, 15 min.
bake on hot plate, 280°C, 10 min.
18.3 Resist coating.
18.4 Via mask (N9)
18.5 Dry etch in O_2 plasma.
18.6 Post bake, 300°C, 5 min.

19 Metal 2 (N10)

19.1 Etch wafer in cold Al etchant for 30 sec.
19.2 Rinse and spin dry.
19.3 Metal deposition, thermal evaporation in vacuum.
19.4 Back sputter about 100Å Al (not available).
19.5 Resist coating.
19.6 Metal 2 mask (N10).
19.7 Wet etch Al in Al etchant, 45°C.
19.8 Rinse and dry.

A.2 Design Rules

Design Rules	
Features	min.(μm)
Wa	1.5
Wb	1.5
Wc	1.5
Wp	1.5
Wm1	1.5
Wm2	4.0
Wv	3.0
Saa	5.0
Sam	1.5
Scc	1.5
Spa	1.5
Spp	1.5
Smm1	1.5
Smm2	2.0
Svv	6.0
Eba	1.5
Ebp	0.5
Eca	1.5
Epa	1.5
Epc	0.75
Eia	1.5
Eip	1.5
Em1c	0.75
Em1v	1.5
Em2v	2.5

Wx : Width of layer x
Sxy : Separation between layer x and y
Exy : Extension of layer x over layer y
a:Active area
b: Buried contact
c: Metal1 to poly contact
p: poly
i: ion implant
m1: metal 1
m2: metal 2
v: via between metal 1 and metal 2

APPENDIX B

SECOND LEVEL METAL PROCESS OUTLINE

B.1 Process Flow Outline

1 Pre-treatment

1.1 If first level metal was done by a resist lift-off technique, the edges may be rough, dip wafer in cold Al etchant for 30 sec at room temperature, etch rate is about 13 Å/sec.

2 Polyimide Coating

2.1 Rinse and spin dry wafer.
2.2 Apply promoter: 1 cc XU289 conc : 9 cc XU 290 dilutant, 5000 RPM, 20 sec.
2.3 Spin on XU284 polyimide from Ciba Geigy, 3000 RPM, 30 sec.
2.4 Dry polyimide as follows:
(a) 85°C, oven, 30 min..
(b) 150°C, oven, 15 min..
(c) 240°C, oven, 15 min..
(d) 280°C, hot plate, 10 min.

3 Via Mask (N9)

3.1 Resist coating, 2μm thick, prebake, 90°C, 30 min.
3.2 Via mask (N9), 365nm, 110 mJ., develop, postbake 110C, 15 min., descum
3.3 Etch polyimide in O_2 plasma (resist will be completely etched)
3.4 Bake wafer on hot plate, 300°C, 5 min.

4 Metal 2 (N10)

4.1 Dip wafer in Al etchant for 30 sec. at room temperature.
4.2 Rinse and spin dry wafer
4.3 Back sputtering of Al (Not available)
4.4 Evaporate metal 2, Al with 1% Cu, 1μm thick
4.5 Resist coating
4.6 Metal 2 mask (N10, positive for wet etch, negative for lift-off)
4.7 Wet etch of resist lift-off metal

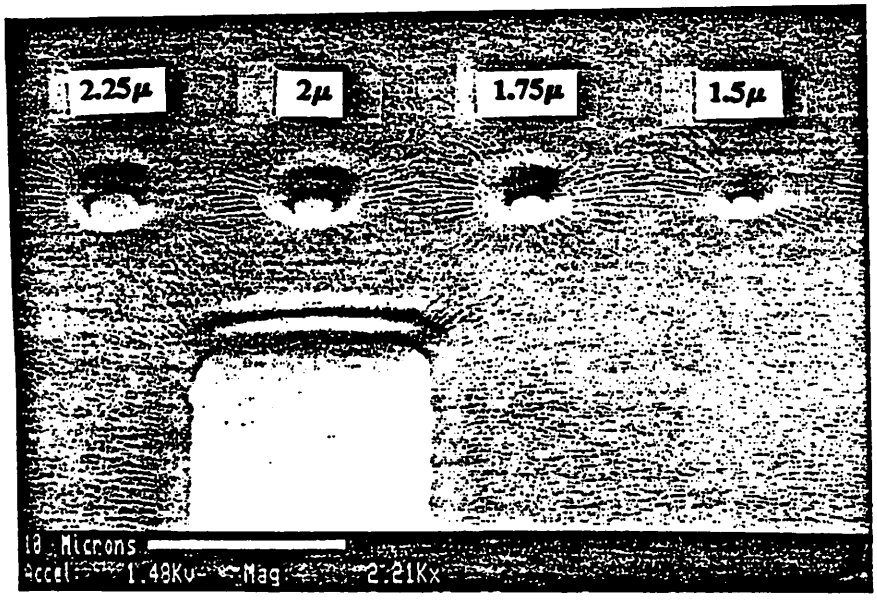


Fig. B1 SEM photo of etched via hole of various sizes (mask dimensions) after process step 3.4.
Note gentle tapered sidewall achieved with this process.

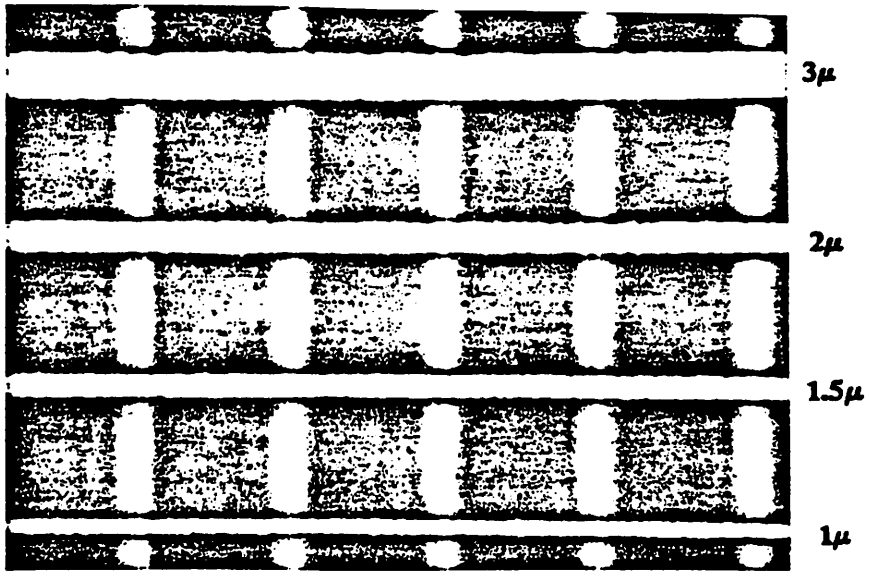


Fig. B2 Metal 2 (horizontal) over metal 1 (vertical) steps,
showing good planarization achieved by spinned on polyimide.
Metal 1 and metal 2 are both 1μm thick and defined by resist lift-off technique.

APPENDIX C

ELECTRICAL CHARACTERISTICS OF NITRIDE CAPACITOR

C.1 Nitride Capacitor Structure

The capacitor in this process uses a nitride layer as dielectric in between field poly and metal 1 as shown in Fig. C1. The dielectric consists of 200Å CVD nitride that has gone through 950°C 20 min. oxidation cycle plus another 500Å CVD nitride which also went through a 950°C 30 min. CVD oxide densification and reflow cycles. These thermal cycles ensure good quality nitride layers with low leakage current. No pin hole problem has been observed. The top plate opening is done by wet etching CVD oxide in 10:1 BHF at 32°C.

The capacitor is meant for on chip frequency compensation and power line decoupling. Dimension control and linearity are thus not very critical. The capacitance value is

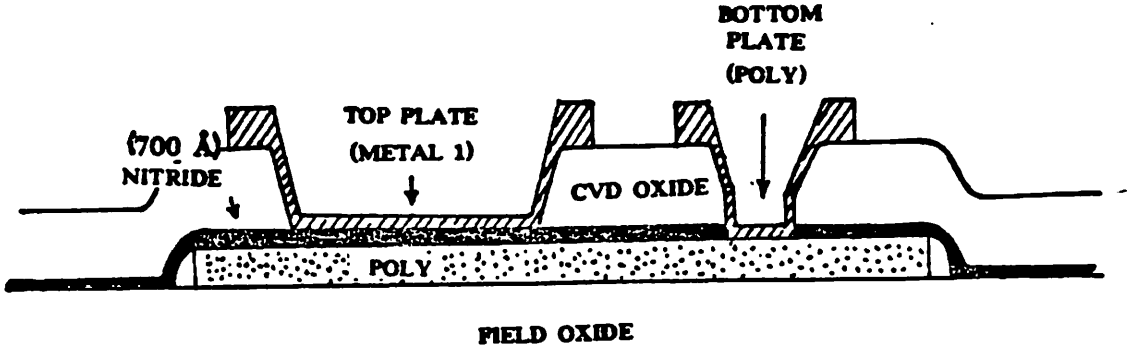


Fig. C1 Nitride capacitor structure

about $0.95fF/\mu m^2$. The relative dielectric constant is about 7.5.

C.2 Capacitor Leakage Current

Capacitor dc leakage current was measured with Pico-Ameter from 0 to 20V. The test area is 200μmX200μm in size. The result is shown in Fig. C2. The leakage current at 5V is about 300 pA/cm^2.

C.3 Voltage Coefficient

Variations of capacitance with applied voltage is measure with a LCR meter biased from -20V to 20V. The result is shown in Fig. C3. The voltage coefficient within the ± 5V range is about 40 *ppm/volt*. The breakdown voltage is beyond ± 20V and is not a concern for this project.

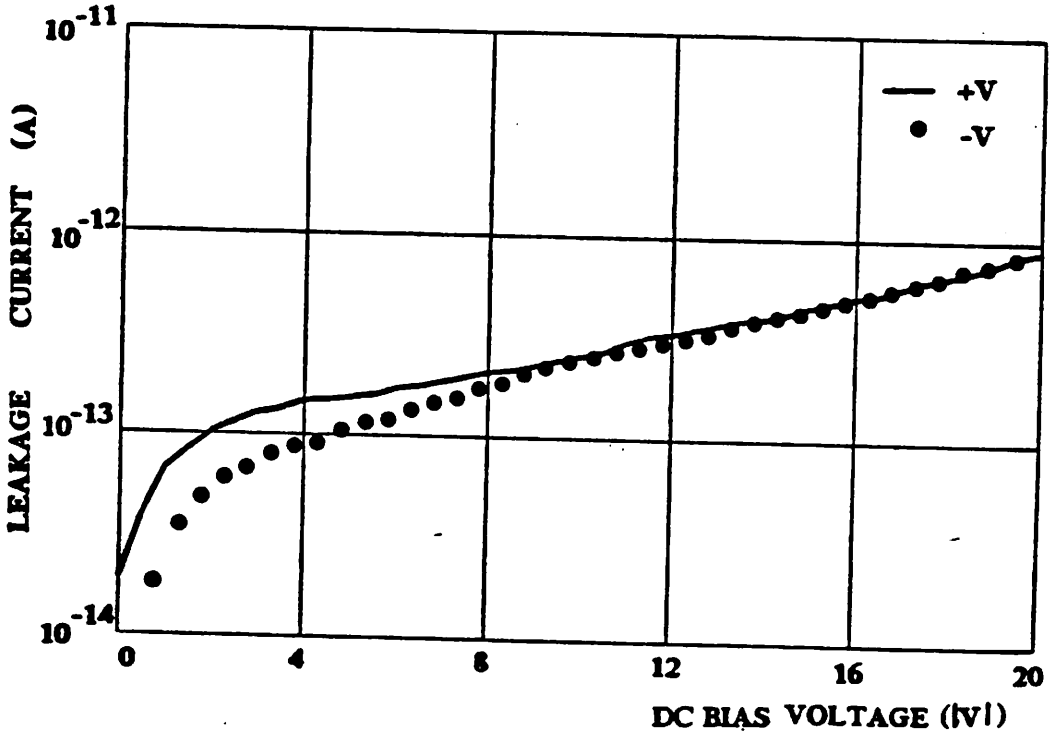


Fig. C2 Capacitor leakage current, area is 200μm X 200μm.

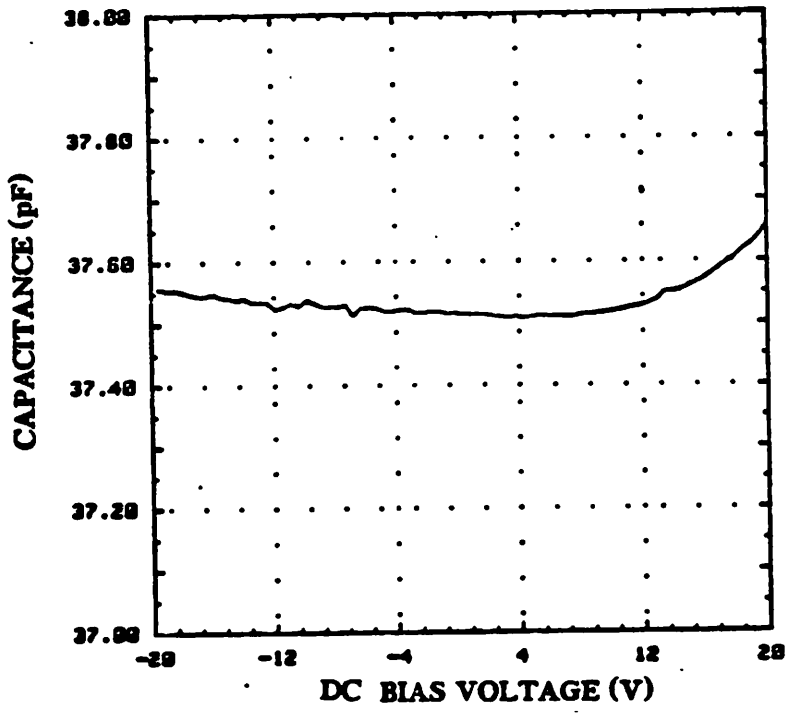


Fig. C3 Capacitance vs. applied voltage

APPENDIX D

SUBMICRON CHANNEL MOS DEVICE CHARACTERISTICS

D1 Introduction

There are substantial differences in the electrical characteristics between long channel and short channel MOS devices. The purpose of this chapter is to review the differences and to describe a simple model for evaluating the electrical parameters of short channel MOS devices, particularly in regard to I_D, g_m and g_{ds}, which are the most important design parameters for analog circuit applications.

Accurate modeling of short channel MOS device electrical characteristics is extremely complicated and is a special field by itself. Elaborate models are available in several circuit simulation programs such as SPICE MOS level 3 model or BSIM (details of which may be found in their respective documentations [7,8]). These programs require large numbers of model parameters and do not provide intuitive insight of various short channel effects for the circuit designer. The simplified model* described here is useful in providing the physical insight and estimating first order effects, ac small signal parameters in the early stage of the design cycle, and to predict trends in the short channel MOS device characteristics as the device is scaled down further.

Throughout this appendix, measured device characteristics are illustrated and realistic numerical examples are given to substantiate the discussion. It is shown that despite the substantial deviations from the long channel behavior, several simple equations are sufficient to predict the I_D and g_m of most state-of-the-art submicon MOS devices to within ±25%, and g_{ds}, which is sensitive to device structure and substrate doping profile, to within a factor of 2.

---

* The model described here is extracted from the EECS 231 class materials provided by Prof. P.K. Ko of UC Berkeley in Spring, 1986.

Although only short channel NMOS devices are discussed (because NMOS technology was the technology available for this project), similar behavior in PMOS devices are expected except that the numerical values of various coefficients are different and that the "hot hole" effects should be less significant than the "hot electron" effects.

D2 Model for Long Channel Devices

For long channel MOS device, assuming gradual channel approximation (GCA) and charge sheet model (i.e. taking an average voltage between the gate and the channel to be $V_{GS} - V_T - \frac{1}{2}V_{DS}$), the I-V characteristics are described, as in most standard texts, by:

$$I_D = \nu C_{ox} W (V_{GS} - V_T - \tfrac{1}{2}V_{DS}) \tag{D2.1a}$$

For low field operation, $\nu = \mu_o E$, $E = V_{DS}/L$, giving

$$I_D = \begin{cases} \dfrac{\mu_o C_{ox} W}{L}(V_{GS} - V_T - \tfrac{1}{2}V_{DS})V_{DS} & \text{for } V_{DS} < V_{Dsat} \\ \dfrac{\mu_o C_{ox} W}{2L}(V_{GS} - V_T)^2 \equiv I^o_{Dsat} & \text{at } V_{DS} = V_{Dsat} \\ I^o_{Dsat}\left(\dfrac{L}{L - X_d}\right) = I^o_{Dsat}[\,1 + \lambda(V_{DS} - V_{Dsat})\,] & \text{for } V_{DS} > V_{Dsat} \end{cases} \tag{D2.1b}$$

where μ_o is the low field mobility and

$$V_{Dsat} = V_{GS} - V_T \tag{D2.1c}$$

$$\lambda = \frac{1}{I_D}\frac{\partial I_D}{\partial V_{DS}} \qquad \text{for } V_{DS} > V_{Dsat} \tag{D2.1d}$$

(Note that V_{Dsat} is included in the last line of Eqn. D2.1b as it may not be negligible in comparison to V_{DS} in the range of < 5V.)

In saturation, from Eqns. D2.1b to D2.1d,

$$g_m = \frac{\mu C_{ox} W}{L}(V_{GS} - V_T) \tag{D2.1e}$$

$$g_{ds} = \lambda I^o_{Dsat} \tag{D2.1f}$$

Note that for long channel devices in saturation,

$$I_{Dsat}^{\circ} \propto (V_{GS} - V_T)^2$$

$$g_m \propto (V_{GS} - V_T)$$

and g_{ds} is essentially a constant with respect to V_{DS}. These features are in agreement with measured data of a long channel NMOS device as shown in Fig. D2.1(a)-(d). Data are taken from a p-well CMOS device processed in the MICROFAB VLSI facilities at UC Berkeley. The device has channel length $L = 100\mu m$, width $W = 100\mu m$ and gate oxide thickness $t_{ox} = 800\text{Å}$

D3 Model for Short Channel Devices

For short channel NMOS devices, still using GCA and charge sheet model,

$$I_D = vC_{ox}W(V_{GS} - V_T - \tfrac{1}{2}V_{DS})$$

For device operates at high field, v is no longer proportional to E. A simple piece-wise carrier drift velocity model may be used:

$$v = \begin{cases} \dfrac{\mu_{eff}E}{1+\dfrac{E}{E_c}} & \text{for } E \leq E_c \\ v_{sat} & \text{for } E \geq E_c \end{cases} \qquad \text{(D3.1)}$$

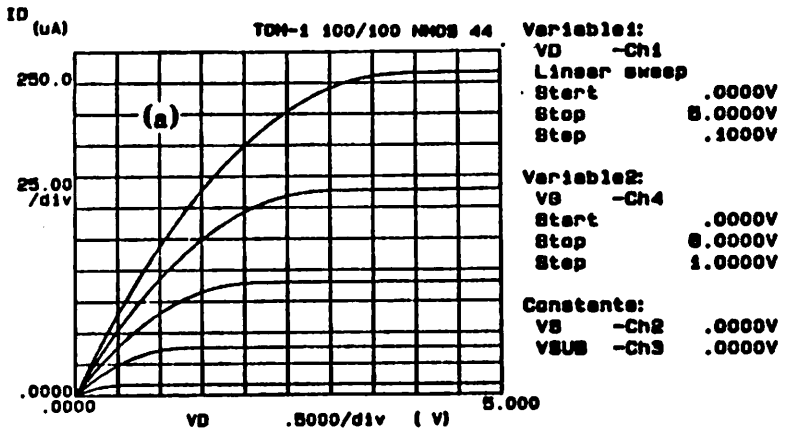
where $\mu_{eff} = \dfrac{\mu_o}{1 + \Theta(V_{GS} - V_T)}$ μ_o is again the low f ield mobility (D3.2)

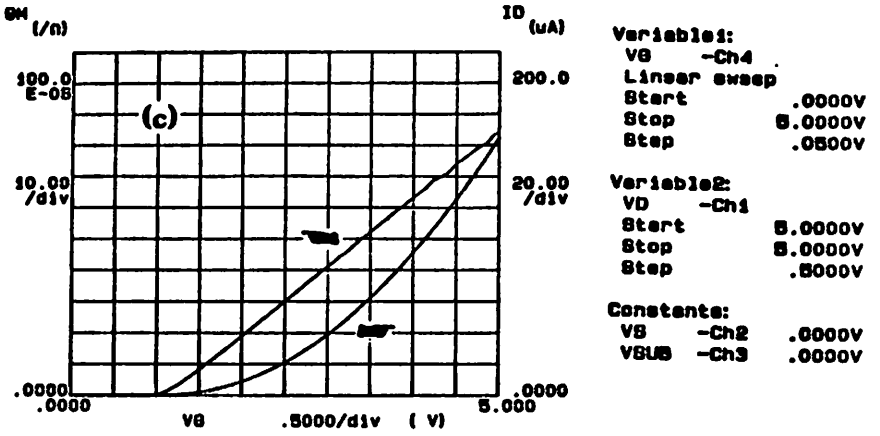
and $\Theta \approx \dfrac{2*10^{-7}}{t_{ox}}$ where t_{ox} is in cm (D3.3)

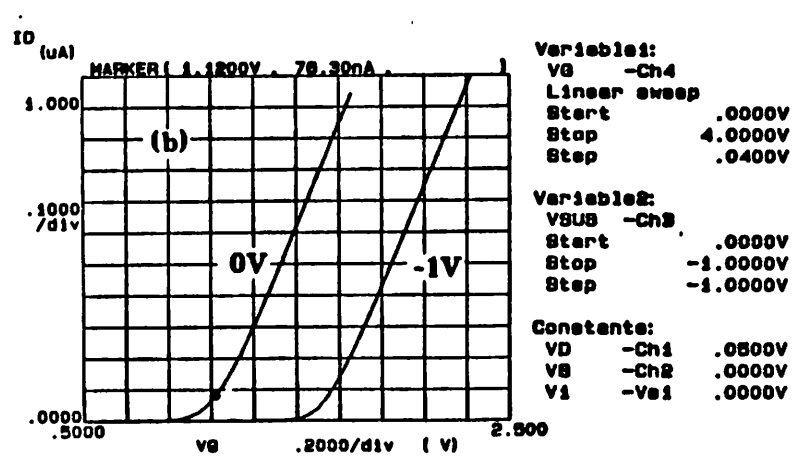
Θ represents the effect of mobility degradation due to high traversed field at the surface due to thin gate oxide. In addition, there is also high longitudinal field due to short channel length which also reduces carrier mobility. This effect may be represent by:

$$v = \frac{\mu_{eff}E}{1 + \dfrac{V_{DS}}{E_c L}} \text{ and } E = \frac{V_{DS}}{L}$$

As E approaches E_c, carrier drift velocity tends to saturate, and μ_{eff} can no longer be used. v_{sat} for Silicon material is about $10^7\, cm/s$. Eqn. D3.1 is shown in Fig. D3.1 at a







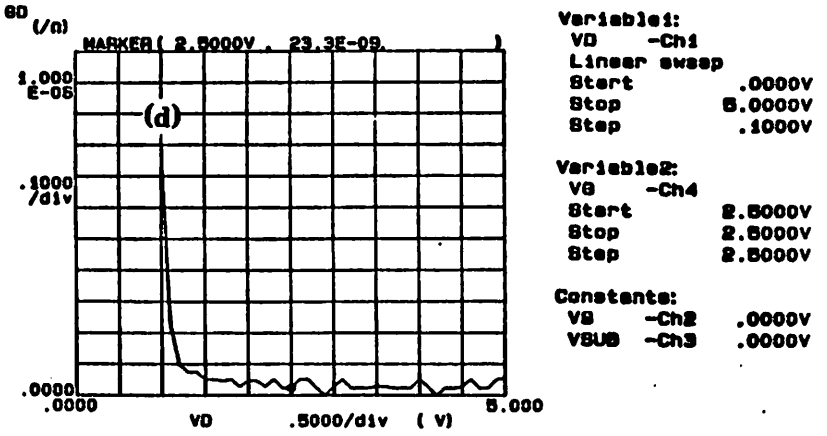


Fig. D.2.1 Characteristics of a 100μm/100μm NMOS device in a p-well CMOS process

(a) I-V characteristics, (b) I_D vs. V_{GS} at low V_{DS}, (c) g_m, I_D vs. V_{GS} at high V_{DS}, (d) g_{ds} vs. V_{DS}.

moderate traversed fields where $\mu_{eff} = 600\ cm^2/V\text{-}s$. Another commonly used model for drift velocity is

$$v_1 = \frac{\mu_{eff} E}{\left[1+(\frac{E}{E_o})^2\right]^{1/2}} \qquad E_o \approx 7\ KV/cm \text{ for bulk silicon} \tag{D3.4}$$

v_1 is also shown in Fig. D3.1. The model in Eqn. D3.1 is not perfect around the knee point but is used in the following discussions for its simplicity and for providing analytical solutions for the following:

$$I_D = \begin{cases} \mu_{eff} C_{ox} \dfrac{W}{L} \dfrac{1}{1+\dfrac{V_{DS}}{E_c L}} (V_{GS} - V_T - \tfrac{1}{2}V_{DS}) V_{DS} & \text{for } V_{DS} < V_{Dsat} \\ v_{sat} C_{ox} W (V_{GS} - V_T - V_{Dsat}) & \\ \quad \equiv K v_{sat} C_{ox} W (V_{GS} - V_T) \equiv I_{Dsat}^{o} & \text{at } V_{DS} = V_{Dsat} \\ I_{Dsat} \dfrac{L}{L - X_d} + I_{SUB} & \text{for } V_{DS} > V_{Dsat} \end{cases} \tag{D3.5}$$

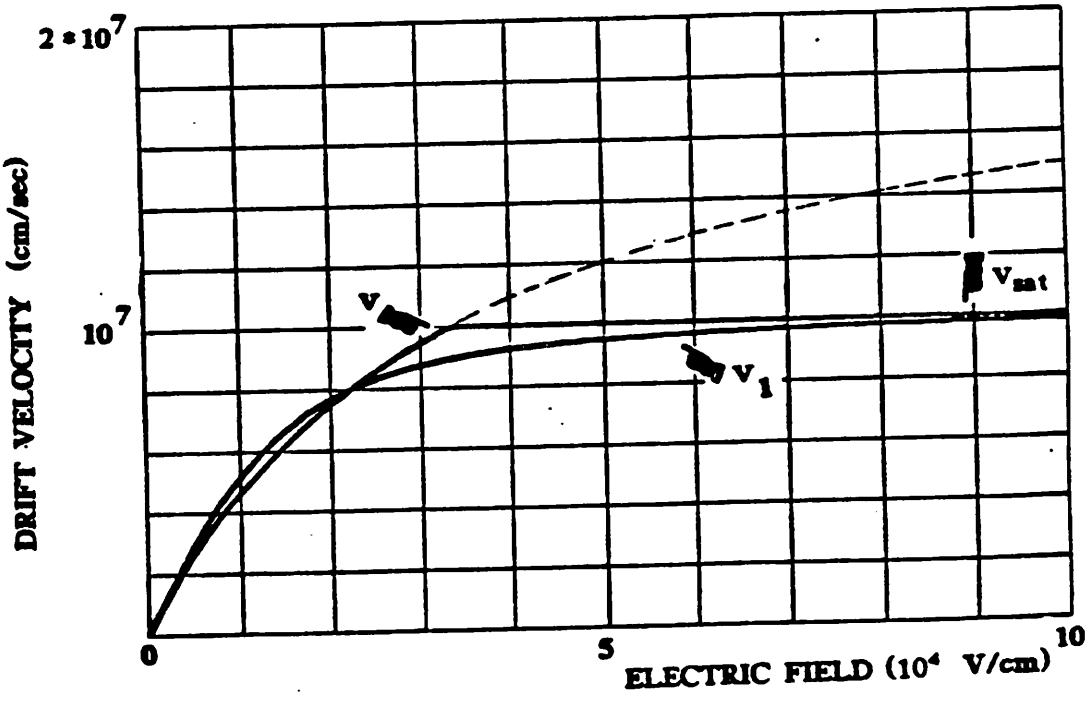


Fig. D3.1 Carrier velocity model

$$E_c = \frac{2v_{sat}}{\mu_{eff}} = \frac{2v_{sat}}{\mu_o}[1+\theta(V_{GS} - V_T)] \tag{D3.6}$$

$$V_{Dsat} = (1 - K)(V_{GS} - V_T) \tag{D3.7}$$

$$K = \frac{1}{1 + \frac{E_c L}{V_{GS} - V_T}} \tag{D3.8}$$

Not included in Eqns. D3.5 are hot electron gate current and drain/substrate junction leakage current which are negligible under normal circuit operation, which is true, particularly in analog circuit applications. I_{SUB} is the hot electron substrate current which is normally much smaller than I_{Dsat} (typically, $I_{SUB}/I_D < 10^{-2}$ at low $V_{GS} - V_T$ and high V_{DS}). However, a more significant effect of I_{SUB} on I_D is the fact that I_{SUB} reduces substrate bias, which reduces V_T, and in turn increases I_D. (This is why I_{Dsat} is used in Eqn. D3.5 instead of I^o_{Dsat} as in Eqn. D2.1b.) There is no analytical form which relates this effect of I_{SUB} to I_D as yet. This is the reason why it is difficult to estimate g_{ds} of a short channel device accurately at large V_{DS}. As I_{SUB} increases with V_{DS}, the incremental changes in I_D in high field with respect to changes in V_{DS} can be large. g_{ds} can therefore increase siginificantly even at moderately low I_{SUB}.

In saturation, i.e. $V_{DS} > V_{Dsat}$, based on the above equations, it can be shown that [25]

$$X_d = \frac{1}{A}\ln\left[\frac{A(V_{DS} - V_{Dsat}) + E_d}{E_c}\right] \tag{D3.9}$$

$$E_d = \sqrt{E_c^2 + A^2(V_{DS} - V_{Dsat})^2} \tag{D3.10}$$

where $A^2 \approx \frac{\epsilon_{ox}}{\epsilon_{si}}\frac{1.5}{x_j t_{ox}}$ and x_j, t_{ox} are in cm (D3.11)

$$I_{SUB} \approx \frac{A_I}{B_I}(V_{DS} - V_{Dsat})I_{Dsat}\, e^{-\left[\frac{B_I}{A(V_{DS} - V_{Dsat})}\right]}. \tag{D3.12}$$

The values of A_I and B_I are estimated from [24] and shown in table D3.1. These coefficients are related to the impact ionization coefficient of the carrier, α as follows.

$$\alpha = A_I e^{-\left(\frac{B_I}{E}\right)} \tag{D3.13}$$

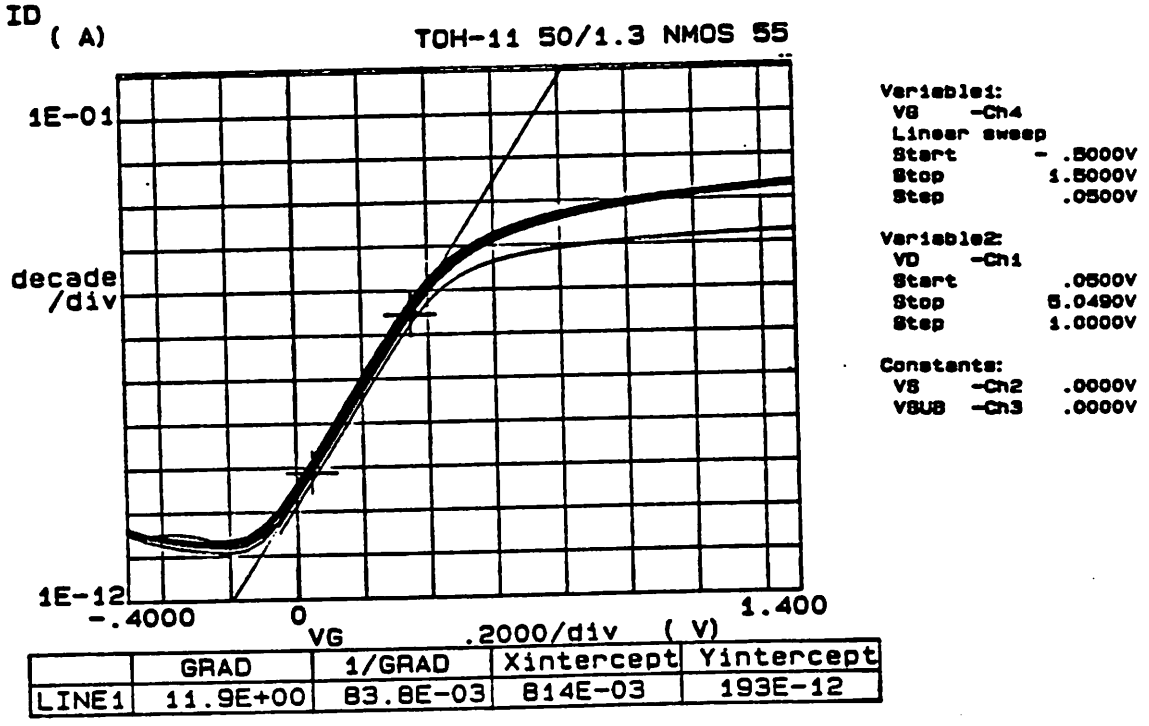
	electron	hole
A_1	$7.85*10^5$	$2.23*10^6$
B_1	$1.21*10^6$	$2.00*10^6$

Table D3.1 coefficients for α expression in Eqn. D3.13

For long channel device, V_T is a function of substrate bias. In short channel MOS devices, V_T is also a function of V_{DS}, especially at high value of V_{DS}, due to drain induced barrier lowering (DIBL) effect. This is reflected as a horizontal shift in the subthreshold conduction characteristic when V_{DS} is increased as shown in Fig. D3.2. It is common practice to relate this by:

$$V_T = V_{To} - \eta V_{DS} \qquad \text{(D3.14)}$$

V_{To} is the V_T at $V_{DS} = 0$ and η is typically less than 0.03 for 1μm channel length MOS



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	11.9E+00	83.8E-03	814E-03	193E-12

Fig. D.3.2 V_T shift due to DIBL effect

device. Note that η can be a major contributor to g_{ds} as indicated in Eqn. D3.16.

Note that for a given t_{ox}, x_j, L and measured values μ_o and η, most of the electrical parameters of a short channel MOS device can be estimated from the above formulas. There are also ways where μ_{eff} can be estimated without measurement [26] and if one ignores η or assumes a typical value of η, the electrical parameters can be estimated without the need of probing any device. This is useful when one must study a particular circuit configuration before any device is available, which may be encountered in a research environment.

From the above equations, one can derive

$$g_m = K_1 v_{sat} C_{ox} W \tag{D3.15a}$$

$$where\ K_1 = [2 - K(1 + \frac{2v_{sat}\Theta L}{\mu_o})] \tag{D3.15b}$$

$$g_{ds} > v_{sat} C_{ox} W \eta + \frac{I_D}{E_d (L - X_d)} \tag{D3.16}$$

The reason for using a $>$ sign in Eqn. D3.16 is because of the lack of any explicit relationship for the I_{SUB} effect on V_T that affects g_{ds}, as explained in section D3. Note that as $L \rightarrow 0$ and/or very high $(V_{GS} - V_T)$, $K \rightarrow 1$, $K_1 \rightarrow 1$ and from Eqn. D3.5 and D3.14:

$$I_{Dsat} \propto (V_{GS} - V_T)$$

$$g_{m\,max} \rightarrow v_{sat} C_{ox} W$$

which are the ultimate relationships for very short channel MOS devices. A typical set of measured short channel NMOS device characteristics are shown in Fig. D3.3. Data are taken from a p-Well CMOS device processed at the MICROFAB VLSI facilities at UC Berekeley. The device has channel length $L = 1.3\mu m$, width $W = 50\mu m$ and gate oxide thickness $t_{ox} = 200\text{Å}$

D4 Calculated Short-Channel NMOS Device Characteristics

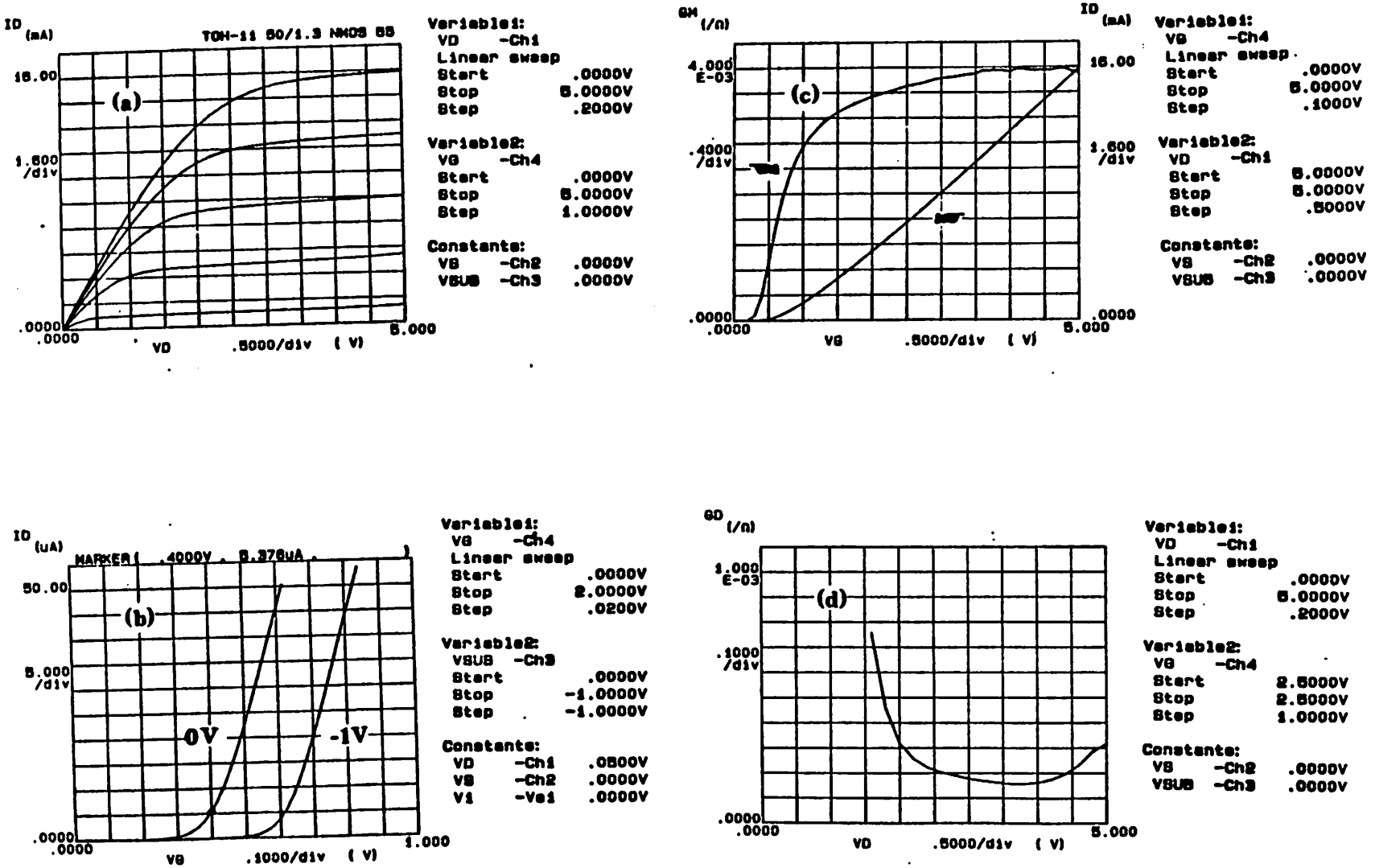


Fig. D.3.3 Characteristics of 50μm/1.3μm NMOS device in a p-well CMOS process (a) I-V characteristics, (b) I_D vs. V_{GS} at low V_{DS}, (c) g_m, I_D vs. V_{GS} at high V_{DS}, (d) g_{ds} vs. V_{DS}.

Submicron device electrical characteristics can be studied with this simple model. For example, a NMOS devices with $L = 1\mu m$, $t_{ox} = 200$ Å operating at a high V_{DS} so that the carrier velocity is saturated at the drain region, the variations of g_m, K and K_1 vs. $V_{GS} - V_T$, are calculated and shown in Fig.D4.1(a) and (b). As shown, g_m, K and K_1 tend towards saturation at high $V_{GS} - V_T$, in agreement with the trend shown in Fig. D3.3(c). The g_m , I_D at saturation for a particular $(V_{GS} - V_T)$ can be estimated from Eqns. D3.5 and D3.15a with the corresponding K and K_1 values given in Fig. D4.1. For example, at $V_{GS} - V_T = 1.5$ $K_1 = 0.5$ and $g_m = K_1 v_{sat} C_{ox} W = 86\ mS/mm$. The measured g_m of the typical 1μm NMOS SIGMOS device is about 80 mS/mm which is in good agreement with the calculated g_m considering the simplifications used in estimating the value of K_1. As another example, the meausred g_m of an 1.3μm NMOS device in an experimental p-well CMOS process is 71 mS/mm as estimated from Fig. D3.3(c). The gate oxide of this device is 200Å. The lower g_m in this device is due to the longer effective channel length. From Fig. D.4.4(b), the K_1 value of a 1.3μm device with 200Å gate oxide is 0.43, and therefore the calculated g_m should be about 74 mS/mm, which again is in good agreement with the measured g_m value.

Fig. D4.3(a) shows the computed X_d at $V_{GS} - V_T = 1.5V$ for the 1μm device and Fig. D4.3(b) shows the g_{ds} vs. V_{DS} at $V_{GS} - V_T = 2.1V$ for the 1.3μm device for direct comparison with that shown in Fig. D3.3(d). Note that the computed g_{ds} did not account for the I_{SUB} effect and therefore does not increase at high V_{DS}. X_d is about 0.2 to 0.3 μm with V_{DS} in the range of 2.5 to 5.0V. Hence, the effective electrical length of the device under normal bias condition is about 0.7 to 0.8 μm. The computed r_{ds} at $V_{DS} = 3V$ is about 230 KΩ-μm. The corresponding r_{ds} from Fig. D3.3(d) is about 280 KΩ-μm.

Fig. D4.4(a) and (b) shows the trend in g_m and K, K_1 factors vs. device length below 2μm for $t_{ox} = 100$ Å (solid lines) and 200 Å (dotted lines). As expected, g_m increases with decreasing L_{eff}, and K_1 approaches 1 as L_{eff} approaches 0. It should be noted that g_m will not double in value as L_{eff} reduces from 1μm to 0.5μm while keeping t_{ox} constant.

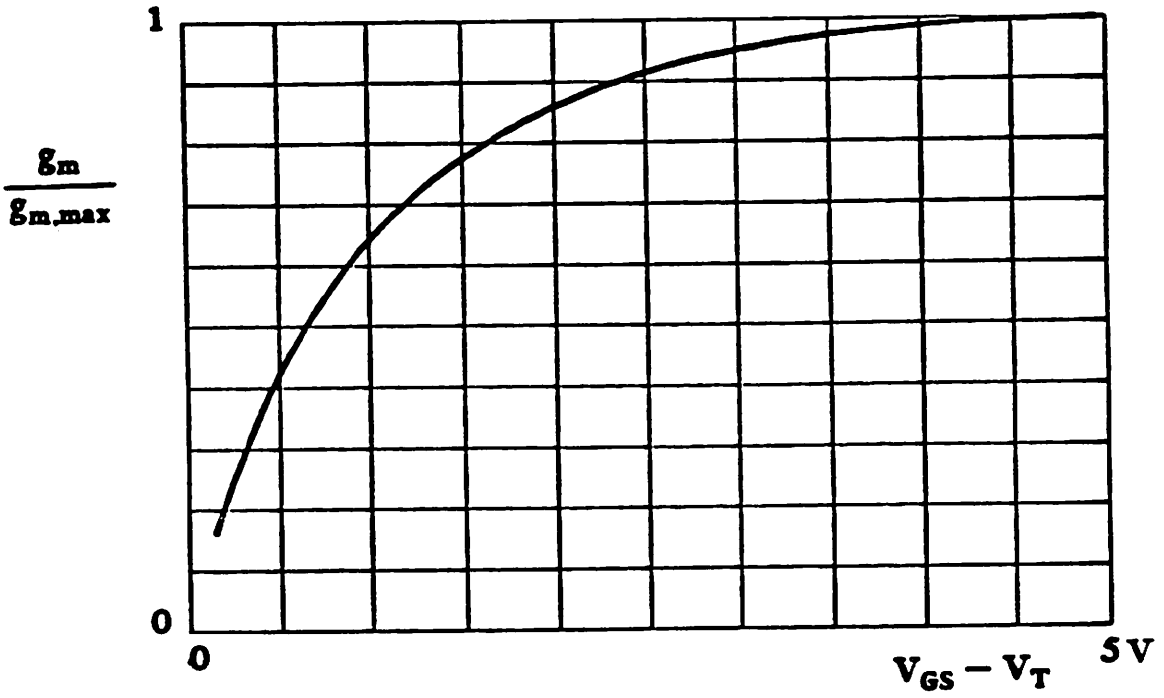


Fig. D.4.1(a) Calculated $g_m/g_{m,max}$ vs. $V_{GS} - V_T$

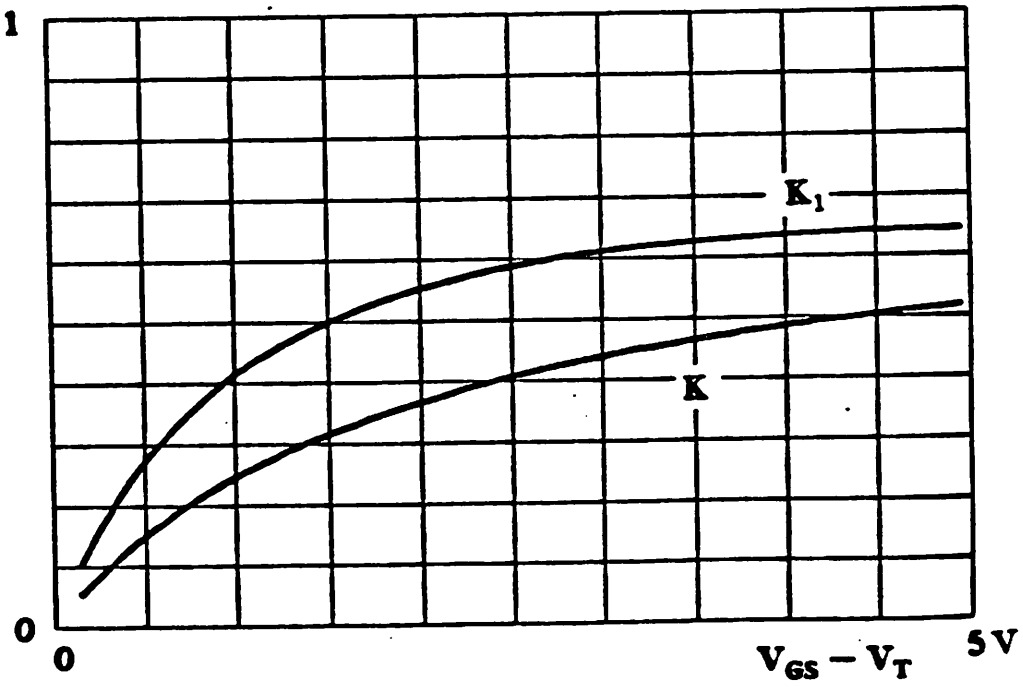


Fig. D.4.1(b) Calculated K and K_1 factors vs. $V_{GS} - V_T$

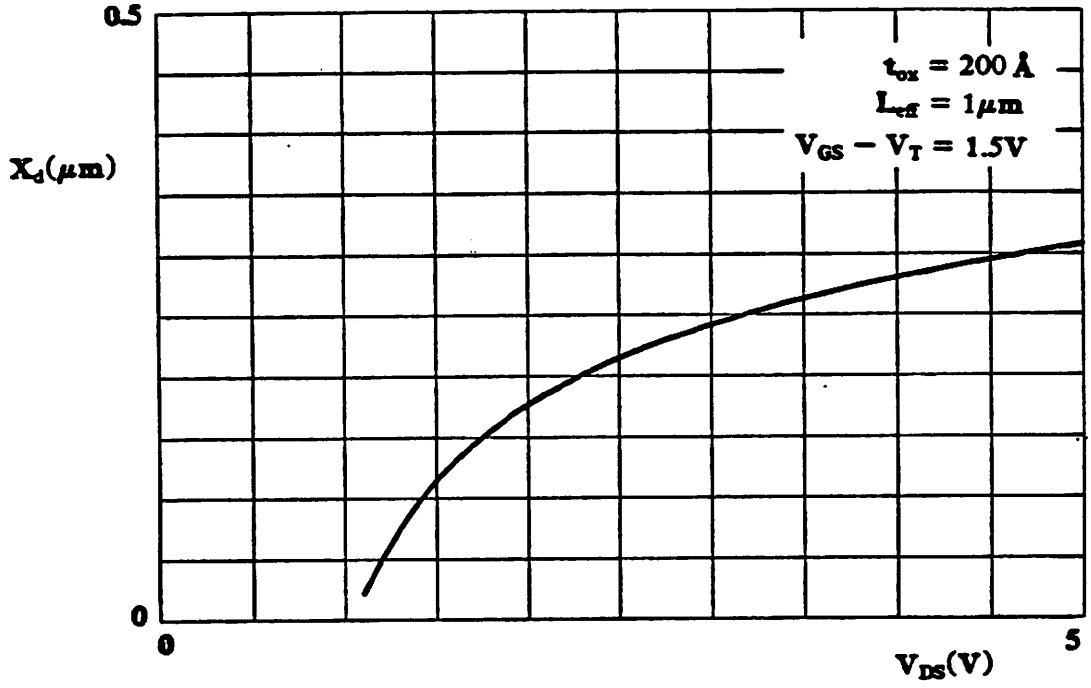


Fig. D.4.3(a) Computed X_d vs. V_{DS}

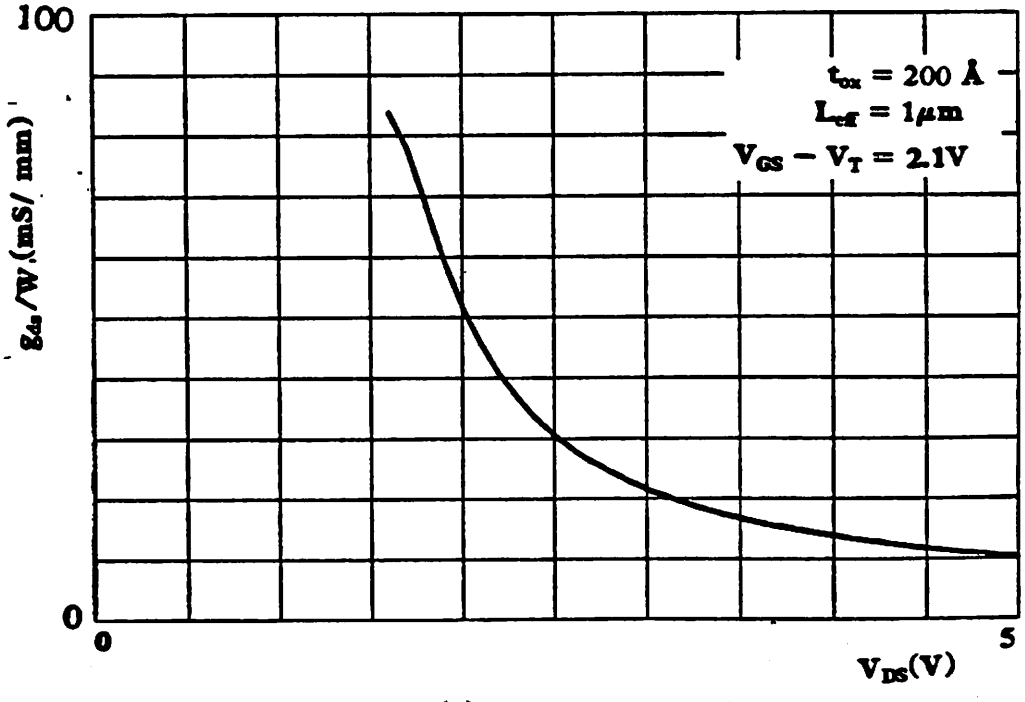


Fig. D.4.3(b) Computed g_{ds} vs. V_{DS}

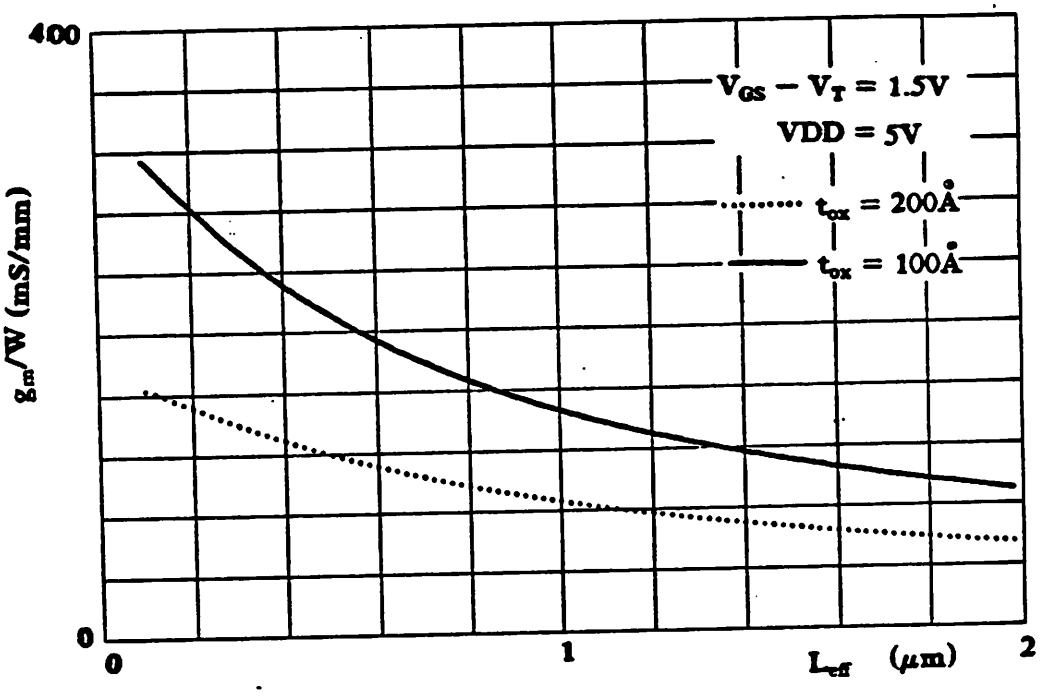


Fig. D.4.4(a) Calculated g_m vs. L_{eff}

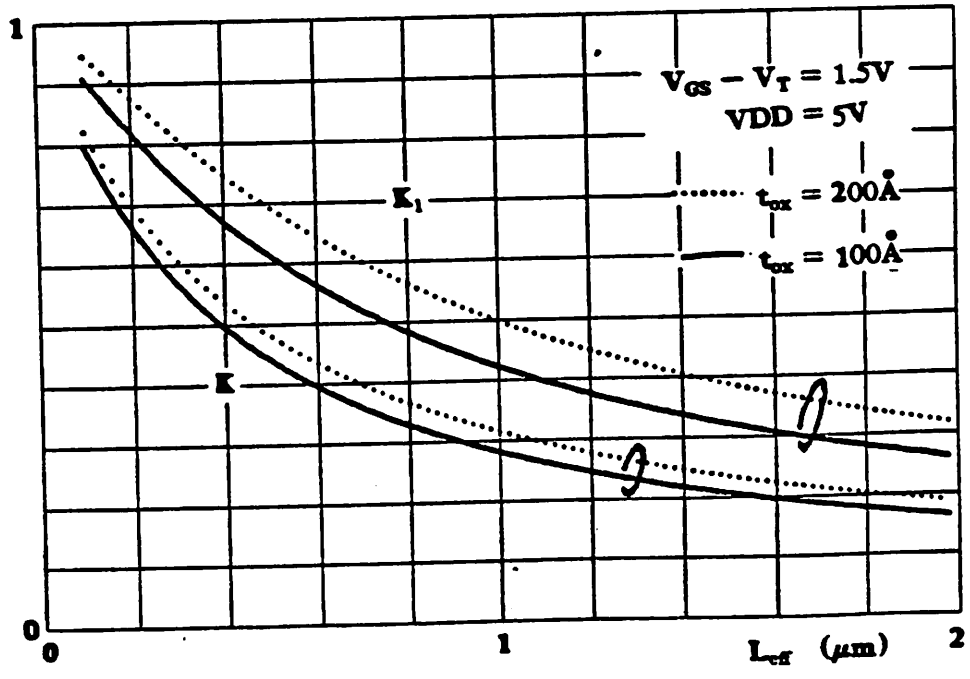


Fig. D.4.4(b) Calculated K and K_1 factors vs. L_{eff}

FBAPPENDIX E

NOISE MEASUREMENTS

In SPICE 2G.6. MOS device noise is modeled based on the input and output current noise sources as shown in Fig. 2.4.1(a). The $1/f$ noise component in the drain current is calculated as follows:

$$\frac{\overline{i_{dn}^2}}{\Delta f} = \frac{K_F\, I_D^{A_F}}{C_{ox} L^2} \frac{1}{f} \tag{E1}$$

Although the exact process parameter dependency in the above formula for short channel devices operated at velocity saturation is in doubt. the $1/f$ noise characteristics do exist in real short channel devices as shown in Fig. E3. This component can be represented by:

$$\frac{\overline{i_{dn}^2}}{\Delta f} = \frac{K_n}{f} \tag{E2}$$

the K_n factor can be estimated from device low frequency noise measurements. The setup is shown in Fig.E.1. A low noise BJT pre-amplifier is used to isolate the device from the HP8566A spectrum analyzer. The pre-amplifier was built from SL560. which is a low noise wideband BJT amplifier IC. The frequency-response of the pre-amplifier is shown in Fig. E2. Midband gain is 29 db. or a gain of 28 and is flat below 10 MHz. The $1/f$ noise spectrum of an enhancement SIGMOS device is shown in Fig. E3. The test device has $W = 200\mu m$ and $L_{eff} = 1\mu m$. The bias point is at $V_{GS} = 2.5V$ and $V_{DS} = 2.5V$. The drain current $I_D = 23.6mA$. The noise spectrum as shown has been corrected for pre-amplifier noise. Since the gate current is negligible. the device drain current noise $\overline{i_{dn}}$ is given by

$$\frac{\overline{i_{dn}^2}}{\Delta f} = \frac{P_o * 50}{|A_v|^2} \frac{1}{R_L^2} \tag{E3}$$

where $P_o = 10^{\frac{P_m}{10}} * 10^{-3}$ and $R_L = r_{ds} // R_{bias}$

where P_m is the measured noise spectrum density in dbm/Hz, A_v is the pre-amplifier voltage gain. R_L is the AC load at the drain of the MOS device under test. The input

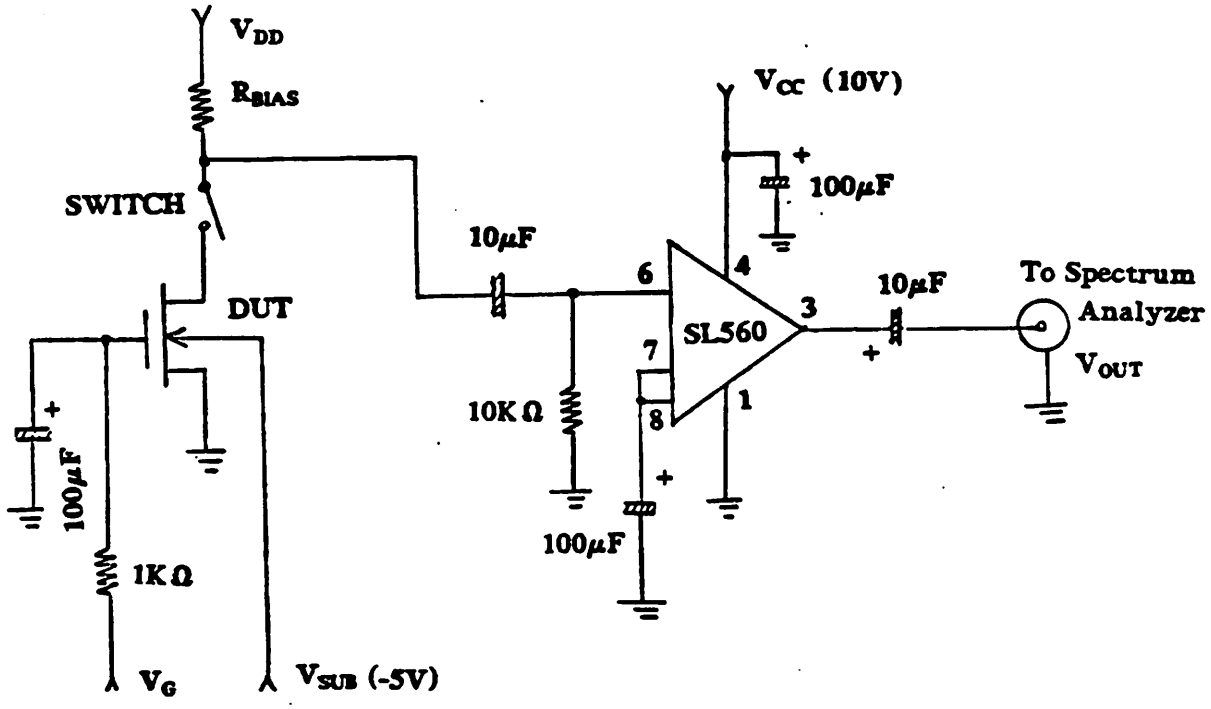


Fig. E1 MOS device 1/*f* noise measurement set up

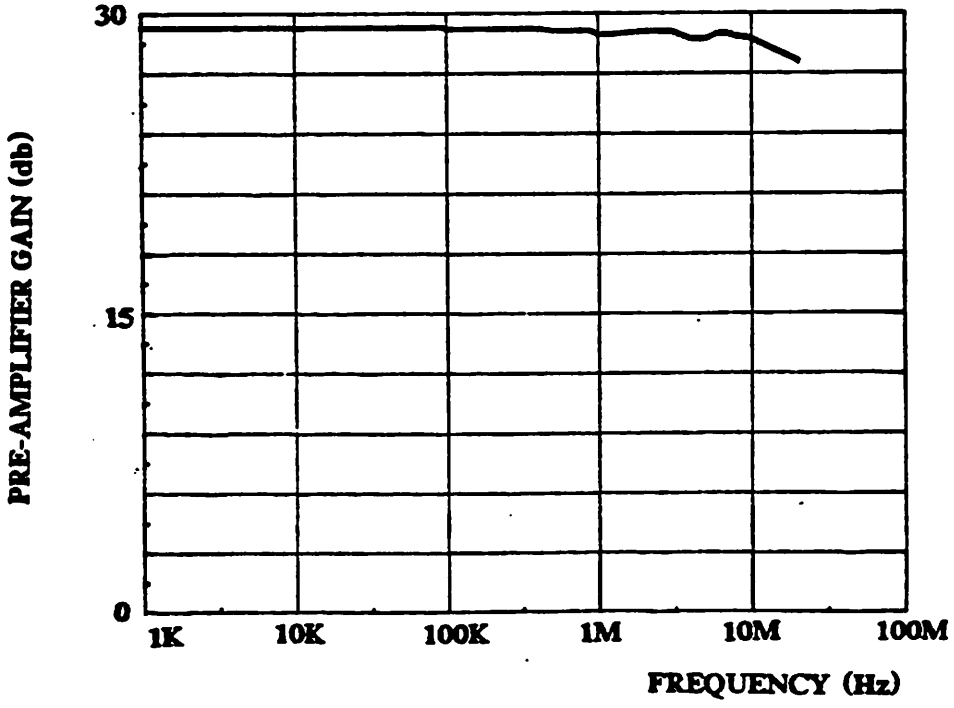


Fig. E3 Frequency response of pre-amplifier.

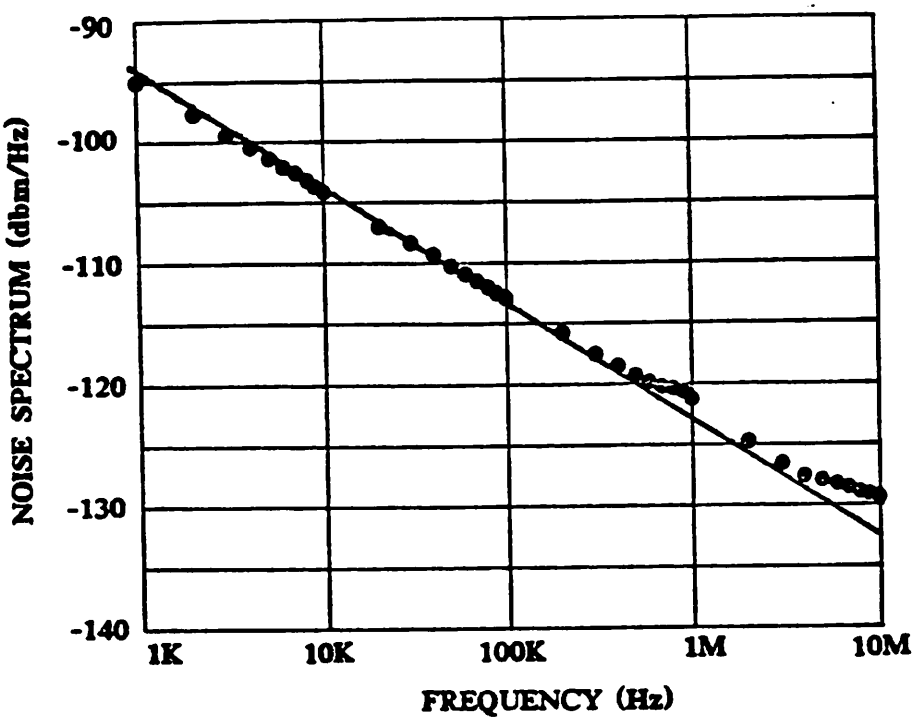


Fig. E4 1μ SIGMOS (enhancement) device 1f nosie spectrum, W=200μm, $V_{GS} - V_T = 1.5V$, $V_{DS} = 2.5V$, $I_D = 23.6$ mA

impedance of the pre-amplifier is high and therefore is not included in R_L. K_n can be determined from the device $1/f$ noise measurement shown in Fig. E3 at the bias and channel length of interest. The K_F factor used in SPICE can then be calculated by equating the $1/f$ coefficient in Eqn. E1 and E2, assuming $A_F = 1$, the default value.

For the 1μm SIGMOS device under test, $R_{bias} = 50\Omega$, R_L is about 48Ω taking into account the loading of r_{ds} of the device itself. At 1 KHz, from Fig. E3, noise level is at -94 db, hence $K_n = 1.1*10^{-14}$. Since I_D is 23.6 mA, $C_{ox} = 172.6nF/cm^2$, equating the $1/f$ coefficient gives $K_F = 8*10^{-28}(F-A)$. This value were used in SPICE to simulate circuit noise performance in Chapter 6. Good correlation between measured and simulated amplifier noise is obtained.

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