MOS PROCESSES IN THE MICROFABRICATION LABORATORY

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Katalin Voros and Ping K. Ko

Memorandum No. UCB/ERL M87/12

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Katalin Voros
Ping K. Ko

Abstract

This report describes the "standard" MOS processes in the Microfabrication Laboratory of the University of California, Berkeley. These processes are available as options for students doing research in silicon circuit design or fabrication technology. Test devices are described and test results are shown in the appendices.

MOS Processes in the Microfabrication Laboratory

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MOS Processes in the Microfabrication Laboratory

Introduction

During the past two years a strong effort has been made to stabilize and characterize operations in the Microfabrication Laboratory and to develop silicon MOS processes which can be applied to the fabrication of integrated circuits. Maintaining "standard" or "staff" processes has several advantages, the most important being that it provides stability and continuity in an educational laboratory where students come and go, where each project is different and new students need to identify a starting point from which they can carry on their projects. Another important factor is the capability to provide circuit designers with a choice of processes which can be used to design new circuits and to fabricate chips for those who cannot spend the time or are not interested in doing it themselves. Yet, the designer is close to processing, can follow it in detail, and can help make processing decisions; thus, the lab is still providing valuable experience for the student.

The Microlab staff currently maintains a 2μm NMOS process, a 2μm N-Well CMOS process, a 3μm P-Well CMOS process with double poly-silicon and a 2μm P-Well CMOS process with double metal (5μm first metal pitch). Complete process descriptions are included in the appendices.

NMOS Process

The 6-mask NMOS process includes LOCOS isolation, 200Å of gate oxide, buried contacts to provide an extra layer of interconnections and an optional thin poly-silicon layer under the aluminum to prevent spiking.

The test chip, designed by Dr. P. Li, includes the usual process and device test structures and a 512 x 8 bit RAM, which was a FIFO test chip for image processing circuitry designed by P. Ruetz.[1] Listings of devices and transistor test results are shown in Appendix I.

N-Well CMOS Process

The first CMOS process in the new Microfabrication Laboratory was developed during a two-semester graduate course given by Professors Oldham and Neureuther with Dr. Yosi Shacham-Diamand.[2,3] This was an N-Well process which was modified and established as the staff process during 1985.

The test chip was designed by the students in the course EECS 290N and the mask set, made during the course EECS 290O, was used for the staff CMOS 1 and 2 runs. Some features of the current N-Well CMOS process are: LOCOS isolation; 250A of gate oxide; self-aligned field implant with double resist photolithography; blanket threshold-adjust implant; single polysilicon; PSG reflow; single metal. Process flow sheets and device results are shown in Appendix II. Device descriptions can be found in References 2 and 3.

P-Well CMOS Processes

A. A p-well CMOS process was developed during 1986 using a test chip designed by K. Y. Toh[4] and a switched capacitor filter circuit by C. K. Wang.[5] 3 micron MOSIS[6] design rules were applied to ensure compatibility with MOSIS processes. The Wang chip, which tested successfully after MOSIS fabrication, served as a control for our first p-well run (CMOS3). The next two lots (CMOS4 and 5) were of a composite chip consisting of four different circuits designed by students and the Toh test chip as a drop-in in four locations.

The p-well CMOS process has 500A of gate oxide: two polysilicon layers, the second layer containing only the capacitor top plates, no interconnects. The punchthrough implant is a blanket phosphorus implant which is done before the well implant. A self-aligned p- field implant adjusts doping concentrations in the well (outside of active areas): the reversal of the well mask and the nitride layer are used to protect well and p- active areas during field implant outside of the well.

Process flow sheets, device descriptions and transistor test results are shown in Appendix III.

B. Another variation of the p-well CMOS process was applied to the CMOS6 run. For this lot Pei-in Pai, with the help of Kim Chan, developed a double-metal process which has a composite of spin-on glass/plasma deposited silicon dioxide as the intermetallic dielectric.[7] The rest of the process is basically the same as described in Section A, except that it has only one polysilicon layer. Pertinent information is listed in Appendix IV.

Equipment

The Microlab is a complete facility for fabricating integrated circuits, beginning with design, mask making, processing all the way through assembly and testing. Test chip design and layout is done using UCB's KIC graphics editor for integrated circuits.[8] CIF files are transferred into MANN files and loaded on magnetic tape for the GCA MANN 3600 optical pattern generator. The mask shop includes a GCA 3600 pattern generator, two APT automatic mask developers, (one for emulsion and one for chrome), capable of handling 2.5", 3" and 5" plates; an Ultratech mask copier and a 10:1 mask reduction camera.[9] Students normally make their own mask; staff will also accept tapes and will make masks for a charge for those who are not frequent users of the lab or need only a limited number of masks.

The VLSI area of the lab is equipped to process 4" silicon wafers. Photolithography is done on an Eaton cassette-to-cassette wafer track, a GCA 6400 10X wafer stepper, and an MTI Omnichuck developer. Hard baking is done in a VWR convection oven. Resist removal is accomplished by acetone rinsing on the MTI Omnichuck or by plasma ashing in a Technics parallel plate etcher. The process is capable of printing 1 μm lines and spaces routinely and 0.75 μm lines with some extra effort.

For furnace operations the lab has Tylan's Tytan II furnace system with a Tycom 9900 automatic controller. Of the sixteen furnace tubes, four are used for low pressure chemical vapor deposition of silicon nitride, polycrystalline silicon and phosphosilicate glass, or low temperature oxide. Polysilicon is in-situ doped with phosphine to obtain a resistivity of $\sim 7\times10^{-4}\,\Omega$-cm after anneal. Wet oxidation is done with the addition of steam from a dropper-type steam generator. No chlorine is added during dry oxidations. Standard tubes are TCA cleaned for at least 4 hours prior to processing. A set of standard programs, with time/temperature/dopant options, written and tested by students in conjunction with staff, is available for all users. If anything out of the ordinary is needed, students may write their own programs after discussing it with the process engineer.

Standard wafer cleaning before furnace operations consists of "piranha" cleaning (mixture of sulfuric acid and hydrogen peroxide) at 120°C for 10 minutes, twice; the second time it is done in the restricted "clean" sink. Cassettes and spin-dryers are also dedicated to "dirty" and "clean" sinks. Wet etching is done in the "dirty" sinks.

For dry etching the Microlab has a LAM plasma etcher dedicated to polysilicon etching ($CCl_4/He/O_2$) and a Technics plasma etcher for silicon nitride etching (SF_6/He) and silicon dioxide etching (CHF_3/O_2). Dry etching of silicon dioxide is the weak point in the process currently and upgrading the equipment as well as the process is being investigated.

Metallization is done by sputtering Al/2% Si in a DC magnetron sputterer. A Technics plasma enhanced chemical vapor deposition (PECVD) system is used to deposit passivation glass. Wafers can be diced with a Tempress diamond saw and chips packaged with the aid of a West-bond Ultrasonic wire bonder.

Analytical equipment includes a Nanospec, an ellipsometer and a Tencor profilometer for thin film measurements; a manual and an automatic (Prometrix) four-point probe station and a Tencor Sonogage for resistivity measurements; a C-V test set-up with heated chuck and a manual probe station with curve-tracer for in-process electrical testing. A Vickers image shearing micro-scope, a Nanoline and a Cwikscan electron microscope by Nanometrics are used for linewidth measurements and visual inspection.

Electrical testing in wafer form is done in the Device Characterization Laboratory which is equipped with several probe stations with HP4145 Semiconductor Parameter Analyzers, HP4280 Capacitance Meter/C-V Plotters and associated instruments and computers to allow for detailed testing and data analysis. An electroglass automatic wafer tester with an HP computer is currently being programmed to provide another option for data collection.

Documentation

Operations in the Microlab are controlled by the Berkeley Laboratory Information System (BLIS) which was developed by C. Williams as part of Professor Hodges' Computer-Integrated Manufacturing (CIM) project.[10] The user interface and command interpreter software, called the Wand, has provisions for keeping records such as processing data, equipment operating manuals, etc., along with a host of other capabilities. Thus, all pertinent information is kept on the Wand, which is accessible to all users.

The manual on the Wand contains operating instructions for all equipment in the lab; chemical safety data; process modules for 4" silicon wafer processing (see Appendix V) and standard MOS process outlines as shown in Appendices I-IV. Students use their lab computer accounts to maintain their own records. There is a joint account called "cmos" for the processing staff (in addition to their own) to record all information pertaining to staff projects. To facilitate uniform data entry, a shell script called the "hotpotato", similar to that used in the 290NO classes has been written by L. Lim. Each lot will have a new file and after a step has been completed, processing information is entered along with observations, measurements, etc. The "hotpotato" format and the shellscript listing is included in Appendix V.

Staff

The Microlab, which also provides a facility for III-V compounds and cryoelectronic device research along with silicon work, is supported by 12 full-time employees consisting of 5 maintenance technicians, a junior engineer responsible for facilities, with a development engineer as supervisor, a senior process engineer, who is also the lab manager with 3 processing assistants/associates, and an administrative assistant with part-time student help for office support. The Microlab is a separate cost center within ERL; with its own accounting, purchasing and billing. The processing assistants/associates carry out the work involved with the staff projects, provide operational maintenance and act as advisors/helpers to students who require it. A part-time student operates the ion implanter and another one provides software support.

The Faculty-in-charge, who is a professor chosen by the Director of ERL, acts as liaison between faculty and staff. He also plays an active role in overseeing the budget and in purchasing new equipment. His most important function, however, is to be the technical advisor for the staff's development work and to help to establish short and long term goals for the lab.

Summary and Proposals for Further Projects

This report is a simplified overview of the staff activities during the past two years in the Microfabrication Laboratory. It should answer several often heard questions: What processes is the staff working on? What standard processes are available for designers? How is such a facility operated?

Now that the standard processes are in place and the lab is operating in a steady state, more or less, further development work can be started. Due to limited resources, the staff cannot take on independent research contracts; projects are determined by need, requests from faculty or students suggesting joint projects, volunteering to do part of the work.

There are several possibilities for investigation. The most obvious approach would be to apply independently developed process steps, such as metal lift-off,[11] and contrast enhancement lithography,[12] boron diffusion from planar sources,[13] or those that are being developed, such as silicide application to the existing processes. With the recent acquisition of a 3-target sputtering system further exploration of multi-level metallization is within our reach. Bringing all the improvements together the design rules for the current processes could be scaled down. Developing a bipolar and/or bi-cmos process in the lab could also be a challenging goal and would expand our design capabilities considerably.

Acknowledgements

This development effort could not have been done without the dedicated work of the Microlab staff. They are: Don Rogers, now retired, former manager; Robert Hamilton and his maintenance group, Brad Bingham, Dick Chan, Phil Guillory, Steve Hoagland, Robert Norman, James Parrish; the processing group, Kim Chan, Marilyn Kushner, Robin Wallach; Rosemary Spivey in the office, and the student helpers who worked part-time for the Microlab, Tom Booth, Thomas Coleman, Ron Johnson, Lyndon Lim, Martin Lim, Dave Mudie, Tom Muller, Gyula Nagy, and Joe Salazar.

Several graduate students were also instrumental in the successful implementation of the standard processes. They are: Chuck Dennison, Pei-Lin Pai, K. Y. Toh, Christopher Williams, Albert Wu and Konrad Young.

Finally, many thanks are due to the professors who built and supported the Microlab from the beginning and are continuously encouraging and appreciating the work being done there.

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Appendix I

NMOS Process

Microlab NMOS Process

Version 1.1 (July, 1985)

0.0 **Starting Wafers**: 18-22 ohm-cm, P-type, <100>

1.0 **Buffer Oxide Growth**: Target t_{ox} = 400Å

1.1 TCA clean oxidation tube.

1.2 Standard clean wafers:piranha for 10 minutes
1:25 HF dip until hydrophobic

1.3 Dry Oxidation: 95 minutes dry O_2
10 minutes N_2 anneal (ramp down)

2.0 **Nitride Deposition**: Target t_{nit} = 1500Å

2.1 Standard clean wafers.

2.2 Deposit 1500Å of Si_3N_4: 25 minutes at 800°C.

3.0 **Active Area Definition**: Mask NACT

3.1 Standard clean wafers.

3.2 HMDS: 1 minute
Spin photoresist on Eaton: Kodak 820, 4600 RPM, 25 seconds
soft bake at 120°C, 45 seconds

3.3 Expose: GCA 6200 10x Wafer Stepper

3.4 Develop: on MTI Omnichuck, Kodak 932:H_2O=1:1, 60 seconds
Inspect for alignment and exposure.

3.6 Descum: Technics-c, O_2 plasma, 300 mtorr, 50 Watts, 1 minutes

3.7 Hard Bake: 20 minutes at 120°C in air

4.0 **Nitride Etch**: Technics C, SF_6:He, 35 Watts.

5.0 **Field Ion Implantation**

5.1 Boron (B^{11}), 100 KeV, 6 x $10^{12}/cm^2$, angle of incidence: 7°

5.2 Resist strip: plasma ash resist in Technics-c:
O_2, 300 Watts, 7 minutes. Piranha clean in sink 8.

6.0 **Locos Oxidation**: Target t_{ox} = 7500Å

6.1 TCA clean wet oxidation tube.

6.2 Standard clean wafers. 1:25 HF dip, 30 seconds.

6.3 Wet Oxidation at 950°C: 5 min dry O_2
5 hrs 30 min wet O_2
20 min N_2 anneal
t_{ox}=

7.0 Nitride Removal

7.1 Oxide dip: 1:25 HF, 2 minutes.

7.2 Hot phosphoric acid etch (155°C) for approx. 30 minutes
(Do not dip off pad oxide.)

8.0 Depletion Photo: Mask DEPI
Normal exp. time and focus. Inspect, descum, hard bake.

9.0 Depletion Implant

9.1 As, 200 KeV. Split lot into 3 for doses as follows:
a) $2.0 \times 10^{12}/cm^2$
b) $2.5 \times 10^{12}/cm^2$
c) $3.0 \times 10^{12}/cm^2$

9.2 Remove resist and piranha clean wafers.

9.3 Strip off pad oxide in 1/10 HF until back side is clear.
Do a 10 second overetch.

10.0 Gate Oxidation: Target t_{ox} = 200Å

10.1 Standard clean wafers, 1:25 HF dip for 30 seconds

10.2 TCA clean gate oxidation tube.

10.3 Dry oxidation at 950°C: 40 min dry O_2
20 min N_2 anneal (no ramp down)
t_{ox}=

11.0 Thin Polysilicon: t_{poly} = 500Å

11.1 Immediately after gate oxide deposit 500Å of poly-Si

12.0 Threshold Adjust Implant
Blanket implant, B^{11}, 50KeV
(Each group from depl. impl. will receive 3 different doses)
a) $4.0 \times 10^{11}/cm^2$
b) $6.0 \times 10^{11}/cm^2$
c) $8.0 \times 10^{11}/cm^2$

13.0 Buried Contact Photo: Mask BCON
Increase exposure by 10%.

13.1 Standard clean.

13.2 Dehydrate wafers at 750°C for 5 minutes.

13.3 HMDS, spin, expose, develop, inspect, descum, hard bake.

14.0 **Thin Poly-Si Etch**
Etch rate ~ 100Å/second. Etch 10 seconds+ 2 seconds overetch.

15.0 **Oxide Etch**

15.1 Etch in 5:1 BHF for 45 seconds Wet wafers before etching.

15.2 Remove resist, piranha clean in sink 8.

16.0 **Gate Poly-Si Deposition:** target t_{poly} = 4500Å

16.1 Standard clean, 1:25 HF dip, 30 seconds (or until dewets).
*It is crucial that there be no oxide left in the contacts.

16.2 Deposit gate poly-Si: 4500Å

17.0 **Gate Definition Photo**: Mask NPLY

17.1 HMDS, spin, expose, develop,inspect, descum, hardbake.

18.0 **Polysilicon Etch**

18.1 Plasma etch poly-Si in LAM.

18.2 Remove photoresist. Piranha clean for 5 minutes

19.0 **Source/Drain Implant**: As, 180 KeV, 5 x $10^{15}/cm^2$

20.0 **Reoxidation and Activation**

20.1 TCA clean oxidation tube.

20.2 Standard clean, 1:25 HF dip, 30 seconds.

20.3 Reoxidize gate and S/D areas 950°C: 30 minutes dry O_2
20 minutes N_2 anneal

21.0 **PSG Deposition**: Target t_{PSG} = 8000Å
Deposit 8000Å PSG.

22.0 **Densification**
950°C, 30 minutes wet O_2

23.0 **Contact Photo**: Mask CONT
Increase exposure time by 25%. Immersion develop.

23.2 Do an etch-bake-etch sequence.

23.2 Plasma strip photoresist. Piranha clean, 1:25 HF dip, 30 seconds

OPTIONAL:
24.0 **Polysilicon Deposition**

24.1 Deposit thin poly-Si: 500Å

24.1 **Anneal**: Anneal at 900°C, 30 min N_2.

25.0 **Metallization**: Target t_{Al} = 0.7 micron.
Sputter on Al/2% Si.

26.0 **Metal Photo**: Mask METL

26.1 HMDS, spin, expose, develop, inspect, descum, hard bake.
Reduce exposure time by 20%

26.2 Wet etch aluminum.

OPTIONAL:
27.0 **Polysilicon Etch**: Wet etch for 15 seconds.

28.0 **Backside Etch**

28.1 Spin protective photoresist on front side twice, with hard bake after each coat of photoresist.

28.3 Etch oxide in 5:1 buffered HF until down to poly-Si.

28.4 Wet etch poly-Si on back (gate poly-Si thickness).

28.5 Etch in 5:1 BHF until back clears.

28.6 Strip front side photoresist in acetone or plasma O_2.
No piranha!

30.0 **Sintering**: Sinter in forming gas for 20 minutes, 400°C.

End of Process

Original Process: Ping K. Ko
Modified by Ping Li (2/7/85) and K. Voros (7/19/85)

Microlab NMOS Process

Mask Descriptions:

1. Active Area:	NACT (cf-emulsion)
2. Depletion Implant:	DEPI (df-chrome)
3. Buried Contact:	BCON (df-chrome)
4. Gate Definition:	NPLY (cf-emulsion)
5. Contact:	CONT (df-chrome)
6. Metal:	METL (cf-emulsion)

Ion Implantations:

1. Field Implant:	Boron (B^{11}), 100 KeV, 6.0 x $10^{12}/cm^2$
2. Depletion Implant:	Arsenic (As^+), 200 KeV, 2.5 x $10^{12}/cm^2$
3. Threshold Implant:	(Blanket) Boron (B^{11}), 50 KeV, 6.0 x $10^{11}/cm^2$
4. Source/Drain Implant:	Arsenic (As^+), 180 KeV, 5.0 x $10^{15}/cm^2$

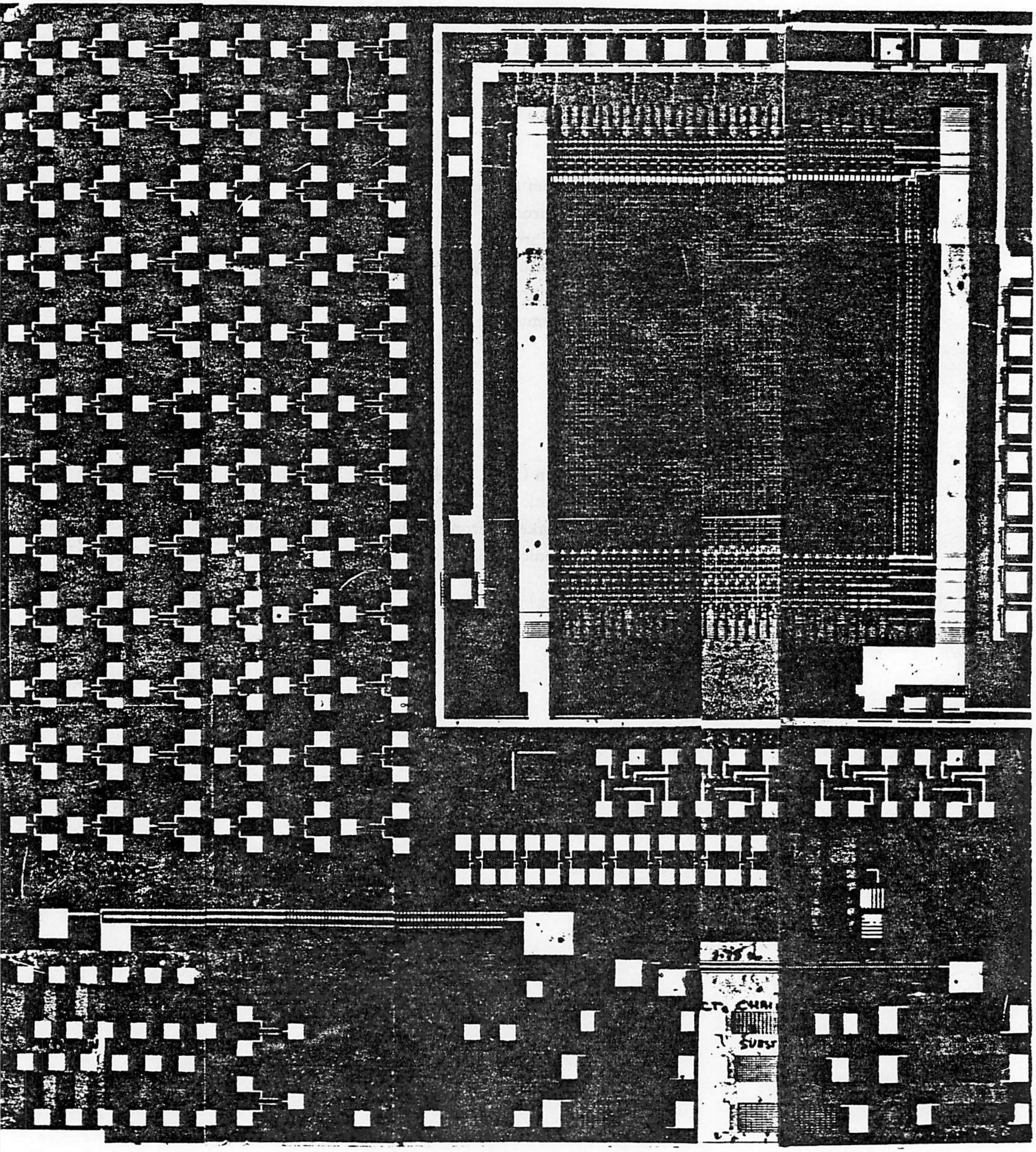


Figure 1. Berkeley NMOS Test Chip

NMOS Test Chip Device Listing

Test Transistors: (starting from upper left-hand corner)

3 columns of depletion mode NMOS transistors: W = 10, 50, 100 μm
3 columns of enhancement mode NMOS transistors: W = 10, 50, 100 μm

Each column has varying gate lengths starting from the top:

L = 0.75, 1.0, 1.25, 1.5, 1.75, 2.0, 2.5, 3.0, 4.0, 5.0, 6.0, 10.0 μm

FIFO Test Circuit:

512 x 8 bit RAM (see Reference 1),
L = 3 μm, contacts: 2 μm x 2 μm, metal pitch: 9.0 μm

Alignment Verniers:
0.1 μm steps, ± 1 μm total

Amplifiers:

4 differential pairs: L_1 = 8 μm on all
L_2 = 8 μm on all

7 Inverters:
L = 1.0, 1.25, 1.50, 1.75, 2.0, 2.25, 2.5 μm

Photolithography Test Patterns:

contact holes to substrate and to poly-silicon: 2 x 2, 2.5 x 2.5, 3 x 3, 4 x 4, 5 x 5 μm;
elbows and line space test patterns

Ring Oscillators:

(left) 200 stage, L = 2 μm
(right) 200 stage, L = 1.75 μm

Resistors: (from left)

2 columns poly-silicon, 2 columns depletion implant, 2 columns substrate;
5 μm lines; 323 □ total.

2 Field Transistors:
W = 100 μm, L = 10 and 7 μm

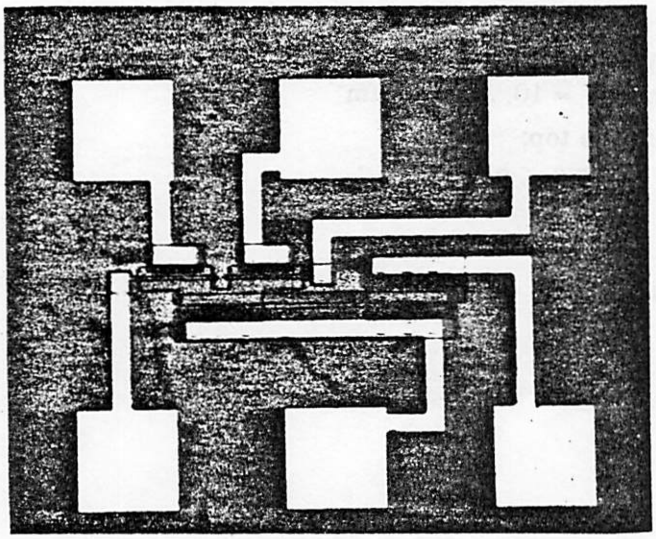
Diode: substrate/n+

2 Capacitors:
depletion implant gate oxide/poly, field oxide/poly, 430 μm x 250 μm

Large Transistor:
L = 200 μm, W = 350 μm

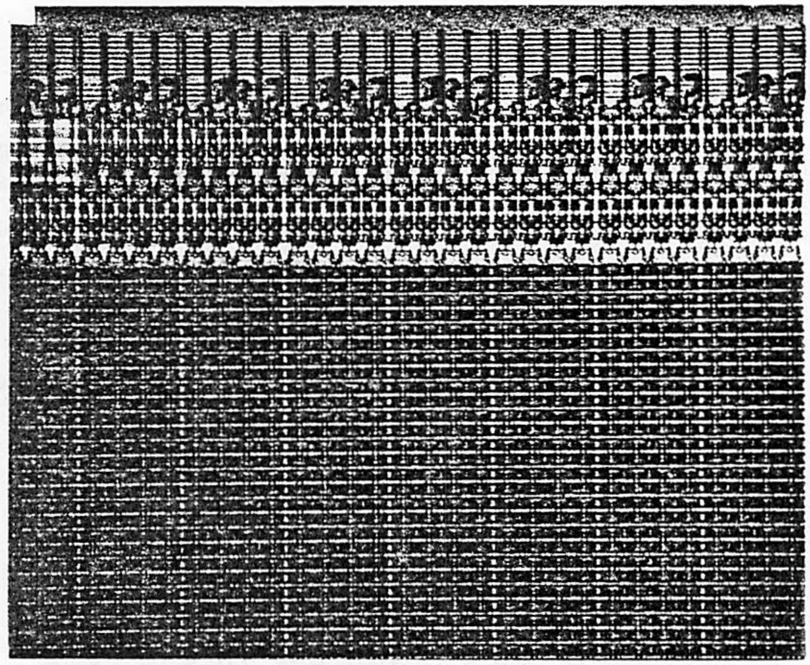
Contact Chains:
2 x 2 μm contacts: 3 to poly-silicon, 3 to substrate, 3 buried contacts

Designed by P. Li
(January 1985)



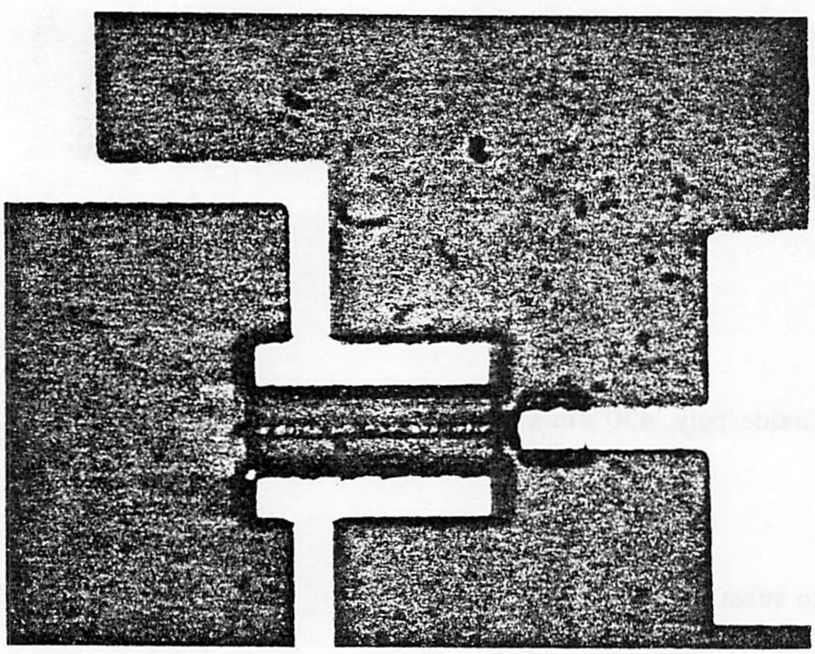
100X

Differential Amplifier



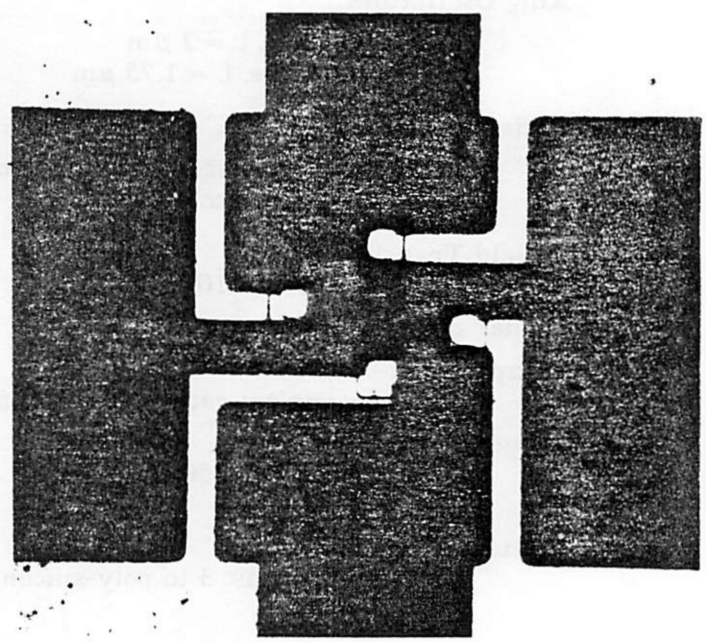
40X

Section of FIFO Test Circuit



400X

NMOST

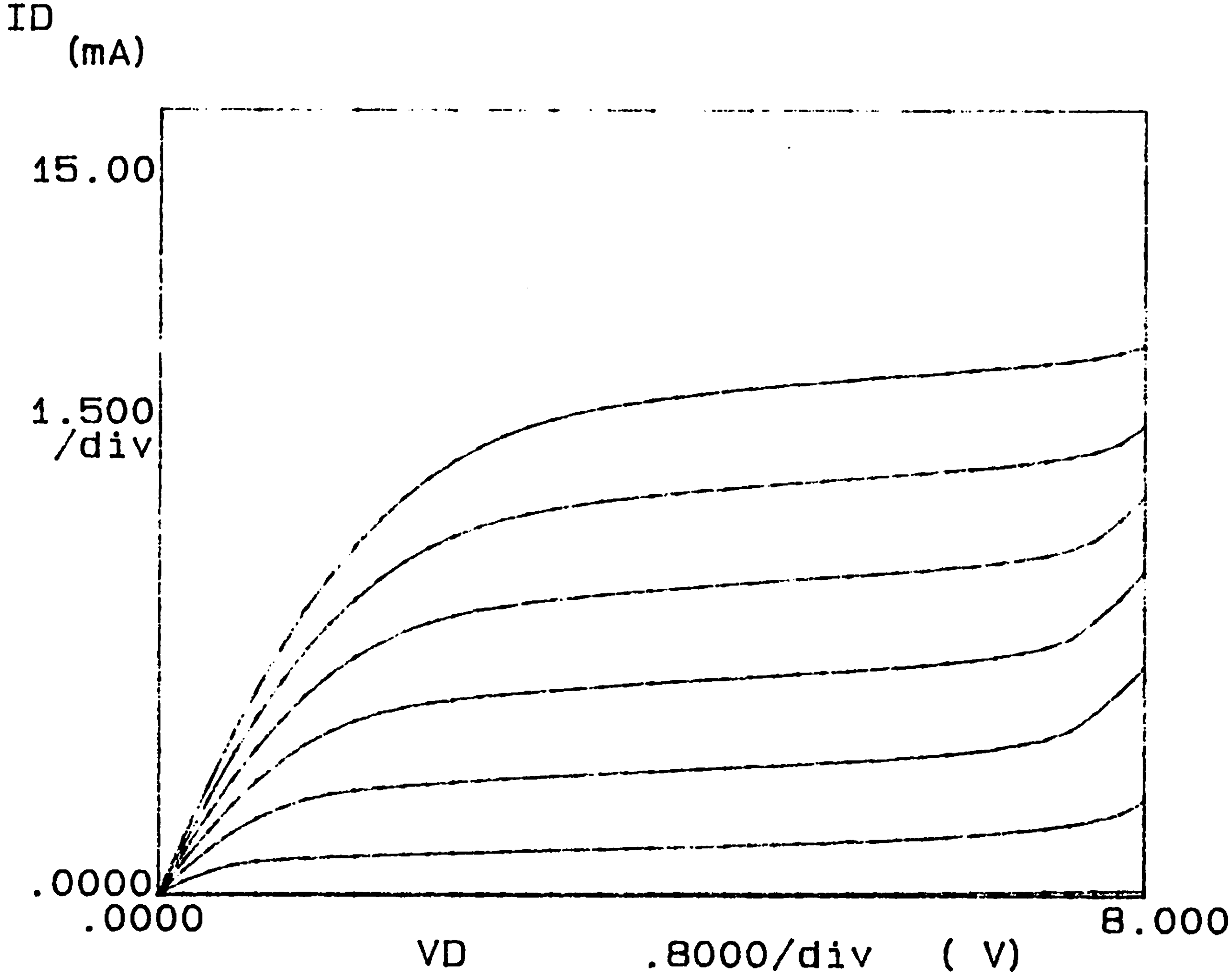


400X

Inverter

Figure 2. Photomicrographs of completed wafer NMOS 2 - 3A

****** GRAPHICS PLOT ******
NMOS2-1A 50/2 ENH 10/7/86



Variable1:
VD -Ch1
Linear sweep

Start	.0000V
Stop	8.0000V
Step	.2000V

Variable2:
VG -Ch4

Start	.0000V
Stop	7.0000V
Step	1.0000V

Constants:

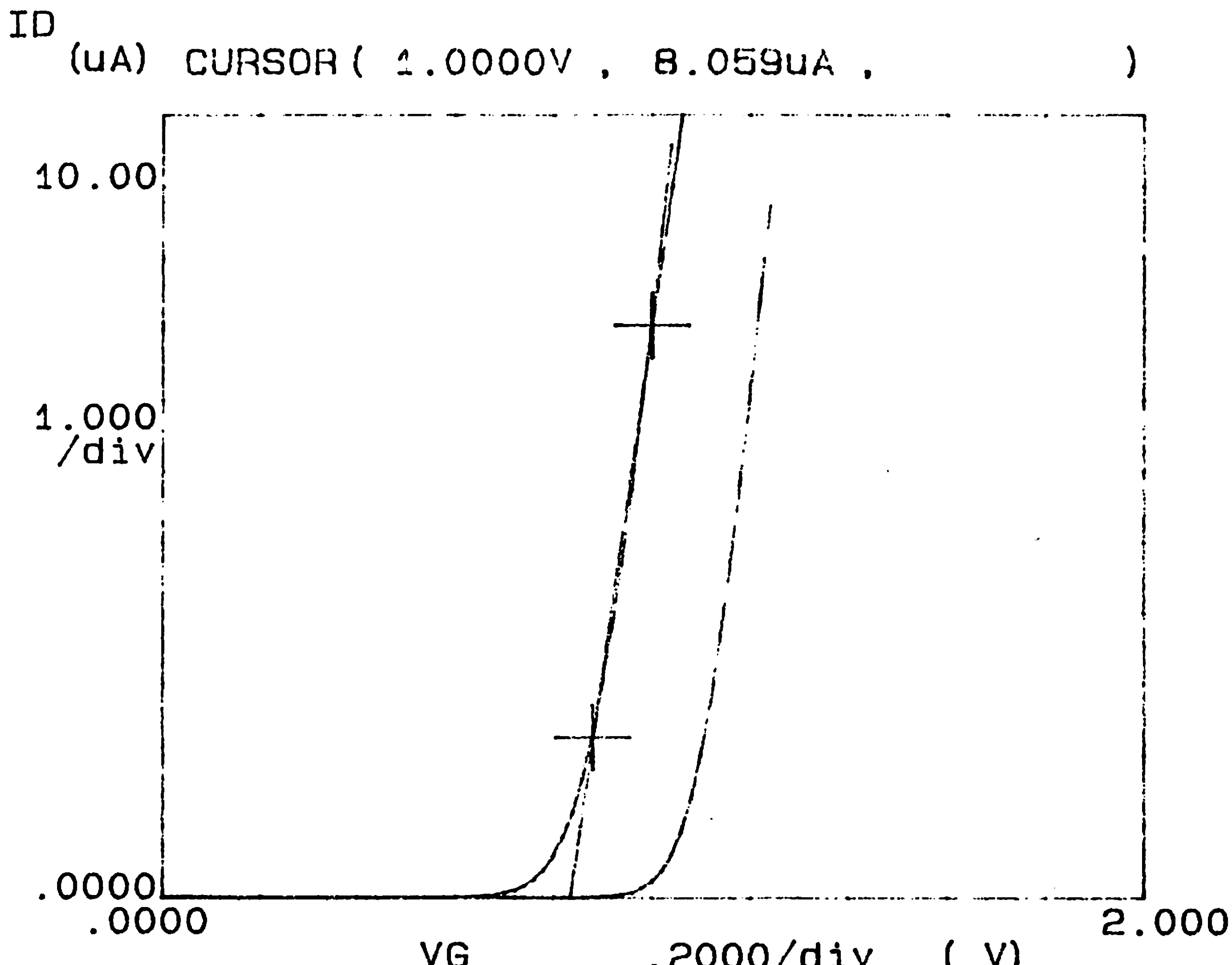
VS	-Ch2	.0000V
VSUB	-Ch3	.0000V

ROUT (Ω) = ΔVD/ΔID
GD (/Ω) = ΔID/ΔVD

Figure 3a. NMOS2-1A W=50um; L=2um

****** GRAPHICS PLOT ******

NMOS2-1A 50/2 ENH 10/7/86



Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 2.0000V
Step .0200V

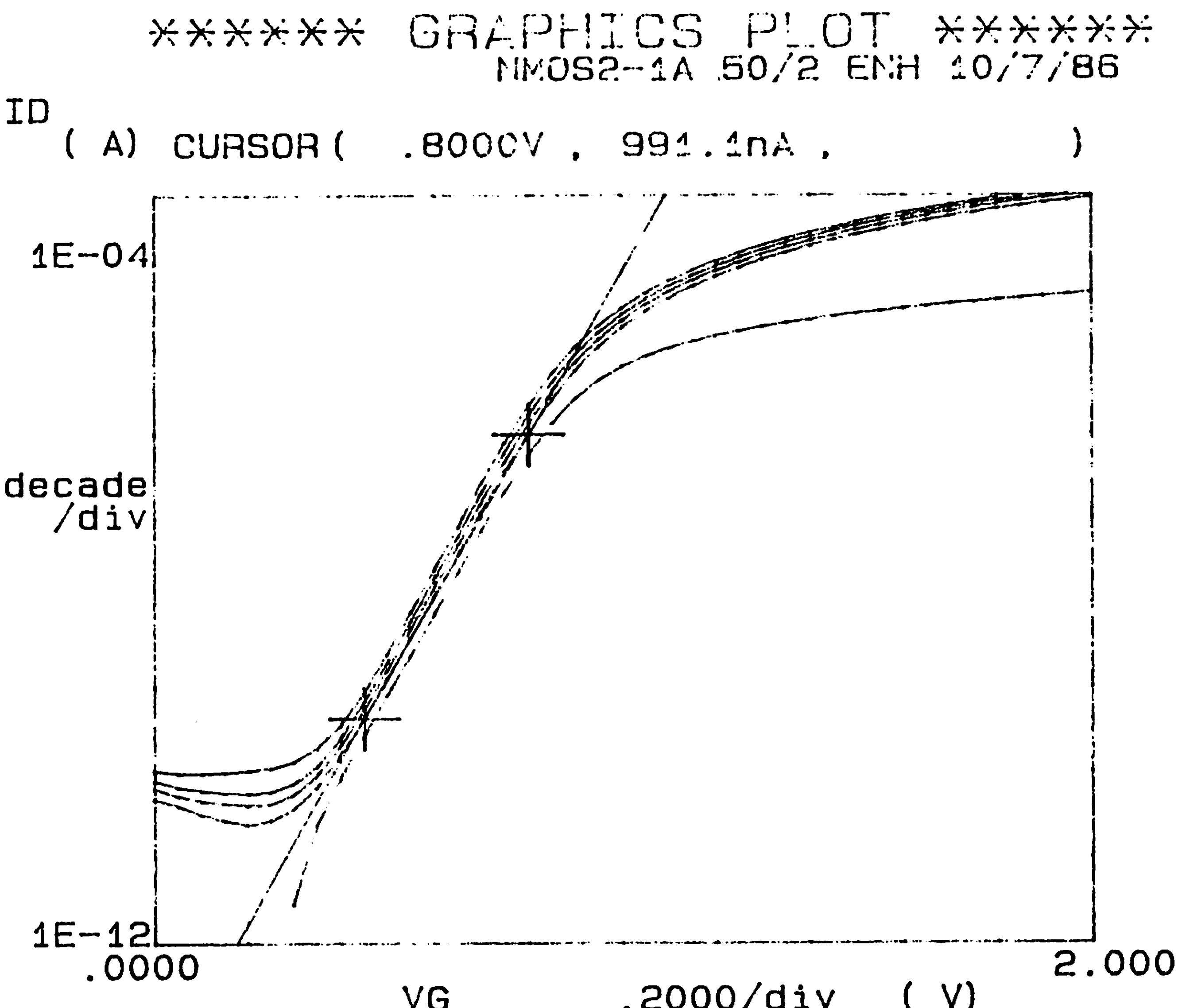
Variable2:
VSUB -Ch3
Start .0000V
Stop -1.0000V
Step -1.0000V

Constants:
VD -Ch1 .0500V
VS -Ch2 .0000V
V1 -Vs1 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	48.4E-06	20.6E+03	834E-03	-40.4E-06
LINE2				

ISUB (A) = ABS(ISU)
I ( ) = 1

Figure 3b. L=2um Enhancement Mode Device V_t= 0.83 V



Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 2.0000V
Step .0500V

Variable2:
VD -Ch1
Start .0500V
Stop 5.0490V
Step 1.0000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

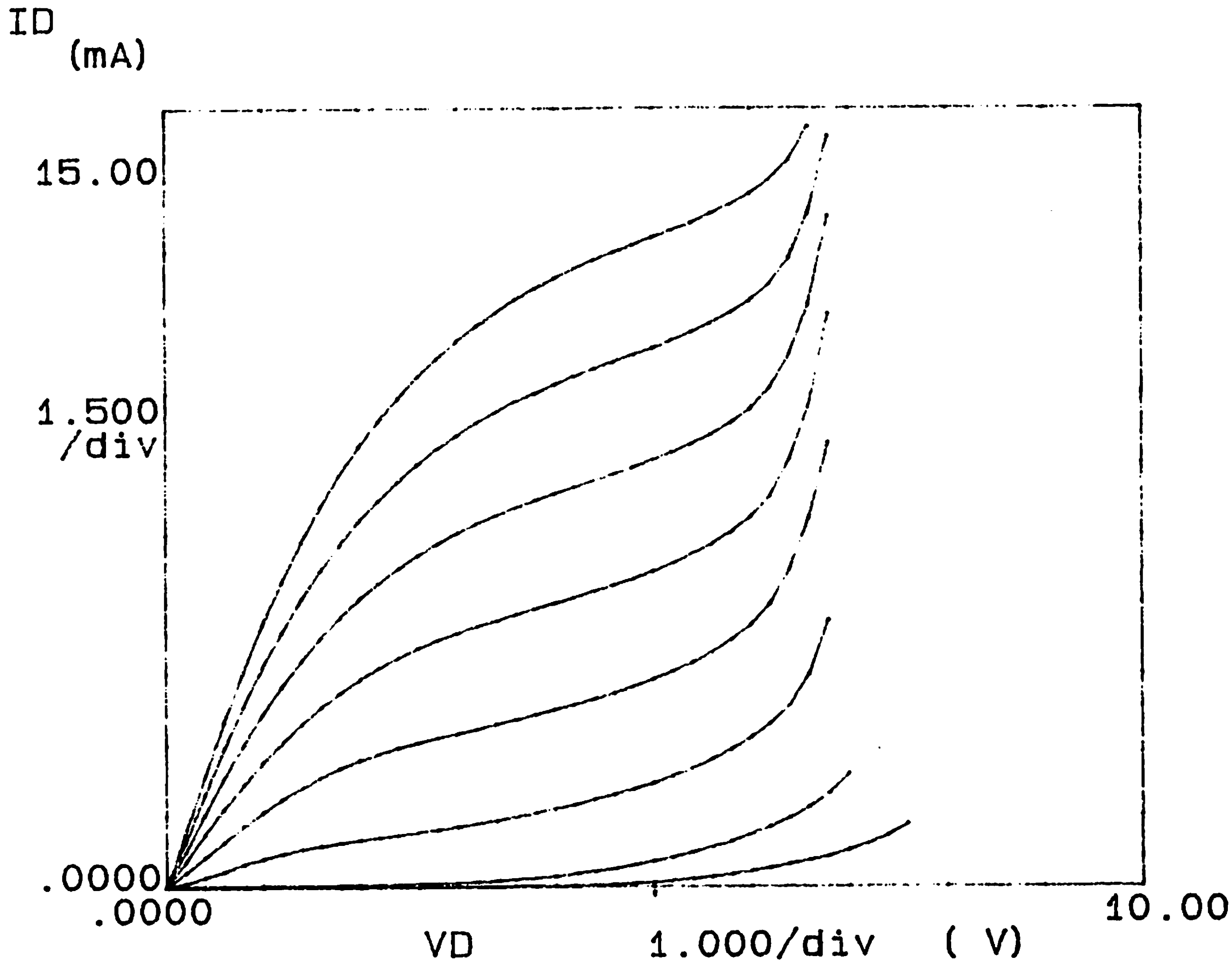
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	9.62E+00	104E-03	1.42E+00	19.9E-15
LINE2				

ISUB (A) = ABS(ISU)

Figure 3c. Subthreshold Current Characteristics of 2um Enhancement Mode Device

****** GRAPHICS PLOT ******

NMOS2-1A 50/1.25 ENH 10/7/86



Variable1:
VD -Ch1
Linear sweep

Start	.0000V
Stop	10.000V
Step	.2000V

Variable2:
VG -Ch4

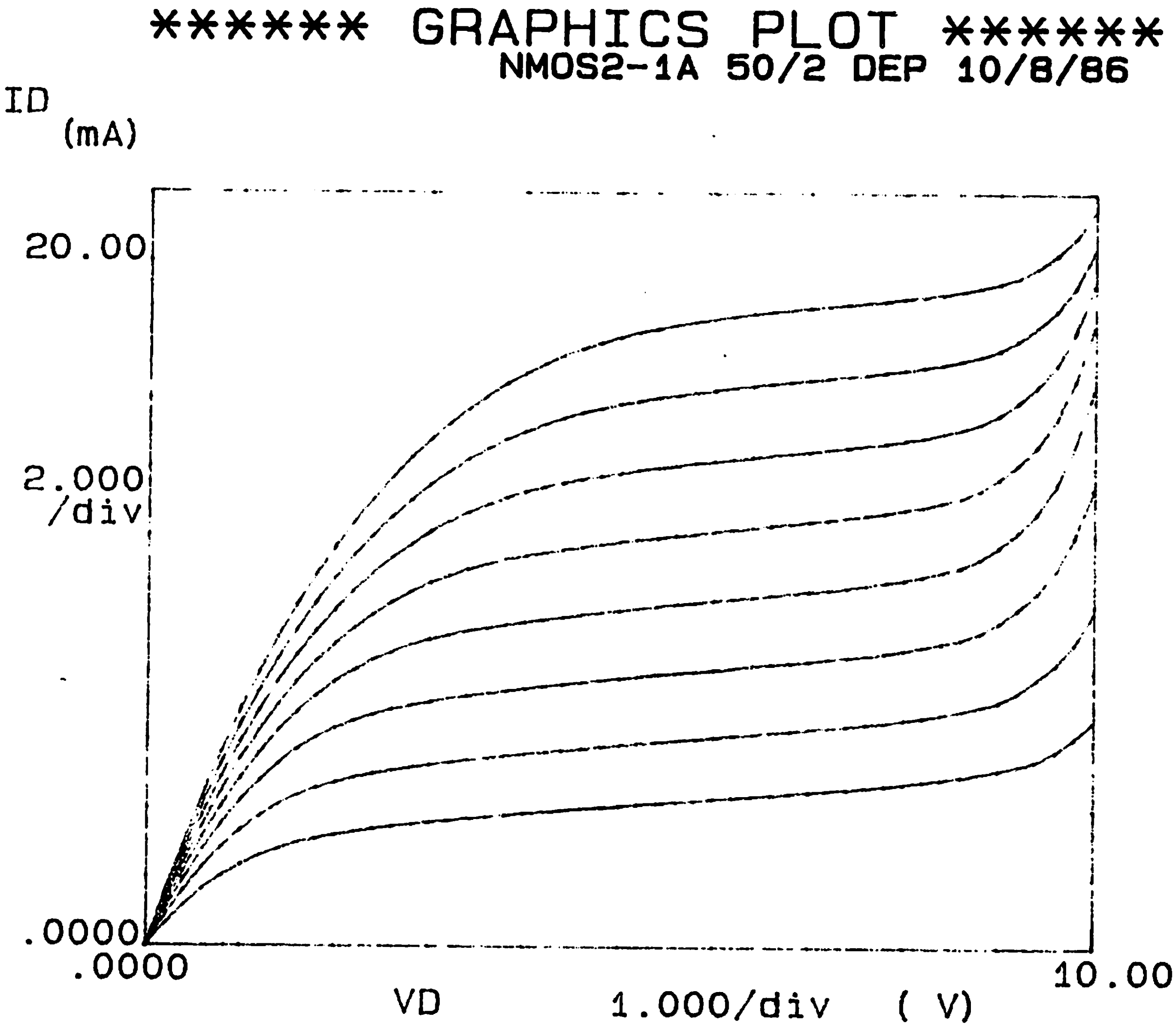
Start	.0000V
Stop	7.0000V
Step	1.0000V

Constants:

VS	-Ch2	.0000V
VSUB	-Ch3	.0000V

Figure 3d. L=1.25um Enhancement Mode Device

ROUT (Ω) = ΔVD/ΔID
GD (/Ω) = ΔID/ΔVD



Variable1:
VD -Ch1
Linear sweep
Start .0000V
Stop 10.000V
Step .2000V

Variable2:
VG -Ch4
Start .0000V
Stop 7.0000V
Step 1.0000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

ROUT (Ω) = ΔVD/ΔID
GD (/Ω) = ΔID/ΔVD

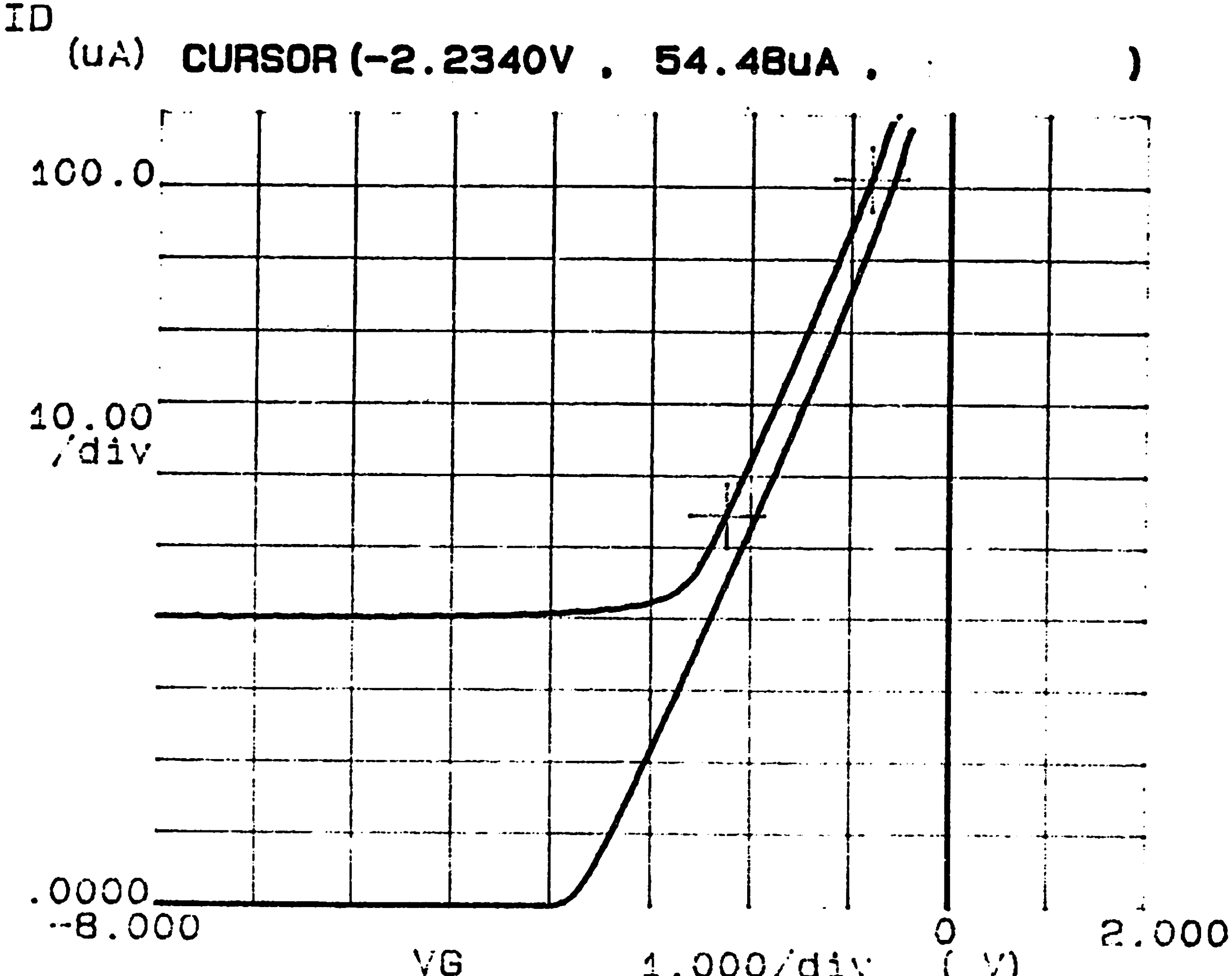
Figure 4a. NMOS2-1A L=2um Depletion Mode Device

Depletion Implant: $2 \times 10^{12}/cm^2$

Threshold Implant: $4 \times 10^{11}/cm^2$

******** GRAPHICS PLOT ********

NMOS2-1A 50/2 DEP 10/8/86



Variable1:
VG -Ch4
Linear sweep

Start	**-8.0000V**
Stop	**2.0000V**
Step	**.0500V**

Variable2:
VSUB -Ch3

Start	**.0000V**
Stop	**-1.0000V**
Step	**-1.0000V**

Constants:

VD	**-Ch1**	**.0500V**
VS	**-Ch2**	**.0000V**
V1	**-Vs1**	**.0000V**

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	32.6E-06	30.7E+03	-3.91E+00	127E-06
LINE2				

ISUB (A) = ABS(ISU)
I ( ) = 1

Figure 4b. Depletion Mode Device
L=2um; V_t=-3.9V

Appendix II

N-Well CMOS Process

Microlab CMOS Process

Modified 290NO process: Version 1.2 (Feb. 5, 1986)
3 um, N-well, single poly-Si, single metal

1.0 Starting Wafers: 18-22 ohm-cm, p-type, <100>

2:0 Initial Oxidation: target = 1000Å

2.1 TCA clean furnace tube.

2.2 Standard clean wafers: piranha clean for 10 minutes,
10/1 HF dip, spin-dry.
Include one p-type control: WELL.

2.3 Wet oxidation at 1000°C:
5 minutes dry O_2
11 minutes wet O_2
5 minutes dry O_2
20 minutes dry N_2
Measured t_{ox}= on WELL cont.

3.0 Well Photo: Mask-WELL
Control wafers are not included in the photoresist steps.

3.1 Spin resist on Eaton: Kodak 820, 4600 RPM, 25 seconds,
soft bake at 120°C, 45 seconds

3.2 Expose: GCA 6200-10X wafer stepper

3.3 Develop in MTI-Omnichuck: Kodak 932/H2O=1:1, 60 seconds

3.4 Descum in TechnicsC: O_2 plasma, 50 W, 1 minute

3.5 Hard bake in oven: 120°C, 20 minutes in air.

4.0 Well Implant: phosphorus, $4 \times 10^{12}/cm^2$, 150 KeV
(Resist is left on wafers.) Include WELL control (no resist).

5.0 Well Drive-In: target x_j = 3 um, t_{ox} = 3000Å

5.1 TCA clean furnace tube.

5.2 Etch pattern into oxide in 5/1 BHF. Include WELL control.

5.3 Remove resist and piranha clean wafers.

5.4 Standard clean wafers, include WELL control.

5.5 Dry oxidation and drive at 1150°C:
4 hrs dry O_2
4 hrs dry N_2
a) Measured t_{ox}= on WELL control
b) Scribe chip off of WELL control: measured x_j=

6.0 Locos Pad Oxidation/Nitride Deposition:
target = 200Å SiO_2 + 1000Å Si_3N_4

6.1 TCA clean furnace tube.

6.2 Remove all oxide in 5/1 BHF until wafers dewet.
Include WELL control.

6.3 Standard clean wafers.

6.4 Dry oxidation at 950°C:
28 minutes dry O_2
20 minutes dry N_2 anneal.
a) Measured t_{ox}= on WELL control
b) Strip oxide off of WELL control in BHF.

6.5 Deposit 1000Å of Si-nitride immediately:
Dep.time = 22 minutes temp.= 800°C.
a) Include WELL control. Measured t_{nit}=
b) Save WELL control for Step 12.

7.0 Active Area Photo: Mask-ACTV
Spin, expose, develop, descum, hard bake.

8.0 Nitride Etch: TechnicsC plasma etcher
Do not etch oxide, do not remove resist.

9.0 Field Implant Photo: Mask-FDII (double photo)
Spin, expose, develop, descum, hard bake.

10.0 Field Ion Implantation

10.1 Boron (B^{11}), 100 KeV, $1x10^{13}/cm^2$

10.2 Remove resist and piranha clean wafers.

11.0 Locos Oxidation: target = 5500Å

11.1 TCA clean furnace tube.

11.2 Standard clean wafers; dip until field area dewets.

11.3 Wet oxidation at 950°C:
5 minutes dry O_2
3 hrs 20 minutes wet O_2
5 minutes dry O_2
20 minutes N_2 anneal
Measured t_{ox}= on a device wafer in the field area

12.0 Nitride Removal
Include WELL control.

12.1 Oxide dip in 10/1 HF for 1 minute

12.2 Etch nitride off in hot phosphoric acid: 155°C, 30 minutes

---

13.0 **Sacrificial Oxide:** target = 200Å

13.1 TCA clean furnace tube.

13.2 Standard clean wafers. Include WELL control.

13.3 Dry oxidation at 950°C:
28 minutes dry O_2
20 minutes N_2 anneal
a) Measured t_{ox}= on WELL control
b) Do not include WELL control in Step 14.

14.0 **Threshold Implant:**
Blanket implant of boron (B^{11}) at 30 KeV
Split lot: $0.9x10^{12}/cm^2$
$1.0x10^{12}/cm^2$
$1.1x10^{12}/cm^2$

15.0 **Gate Oxidation/Poly-Si Deposition:**
target = 250Å SiO_2 + 4500Å poly-Si

15.1 TCA clean furnace tube; reserve poly-Si deposition tube.

15.2 Standard clean wafers.include WELL cont.+ 1 p-type cont.:NCH

15.3 Dip off sacrificial oxide (dewet) in 10/1 HF (approx. 1 minute).

15.4 Dry oxidation at 950°C:
40 minutes dry O_2
20 minutes N_2 anneal.
t_{ox}(WELL)= t_{ox}(NCH)=

15.5 Immediately after oxidation deposit 4500Å
of phos.doped poly-Si.
time = 2 hrs. temp.= 650°C
Do not include WELL. NCH controls; include a new
control with 1000Å thermal SiO_2 on it. t_{poly}=

16.0 **Gate Definition:** Mask-POLY

16.1 Spin. expose. develop. descum. hard bake.

16.2 Plasma etch poly-Si in LAM etcher. Inspect under microscope.

16.3 Remove resist. piranha clean wafers.

17.0 **Reoxidation:** target=1000Å on poly-Si. 500Å on S/D

17.1 TCA clean furnace tube.

17.2 Standard clean wafers, include both controls, WELL, NCH.

17.3 Wet oxidation at 850°C:
5 minutes dry O_2 / 30 minutes wet O_2 / 5 minutes dry O_2 /
20 minutes N_2 anneal.
t_{ox}(WELL) = t_{ox}(NCH) =

18.0 N-Channel Source/Drain Photo: Mask-NNII.
Spin, expose, develop, descum, hard bake.

19.0 N+ Source/Drain Implant

19.1 Implant arsenic at 100 KeV, $3x10^{15}/cms^2$, include NCH control.

19.2 Remove resist and piranha clean wafers.

20.0 N+ S/D Drive-In

20.1 TCA clean furnace tube.

20.2 Standard clean wafers, include NCH control.

20.3 Anneal wafers in N_2 at 925°C for 1hr 15 minutes

21.0 P-Channel Source/Drain Photo: Mask-PPII
Spin, expose, develop, descum, hard bake.

22.0 P+ S/D Implant

22.1 Implant B^{11} at 50 KeV, $2x10^{15}/cms^2$, include WELL control.

22.2 Remove resist and piranha clean wafers.

23.0 P+ Anneal and Reoxidation

23.1 Standard clean wafers, include WELL, NCH controls.

23.2 Anneal and oxidize at 900°C: 10 minutes N_2, 8 minutes wet O_2
Include WELL, NCH controls.

24.0 Reflow Glass: target = 7000Å

24.1 Oxide deposition: incl. a new cont.=PSG,WELL,NCH cont.
Thickness: 2000Å undoped LTO
4000Å 8% phos.PSG (PH3 flow at 10.3)
1000Å undoped LTO
time = (approx.) 30 minutes temp.= 450°C
t_{PSG}= on PSG cont.

24.2 Densify glass at 950°C: include PSG, WELL, NCH controls,
5 minutes dry O_2 / 30 minutes wet O_2 / 5 minutes dry O_2

24.3 Do wet oxidation dummy run afterwards to clean tube:

1 hr wet oxidation at 950°C.

24.4 Measurements on WELL and NCH controls:
Cut piece off for x_j measurement,strip oxide from rest of wfr.
R_sWELL (p-ch S/D)= x_jWELL(well)=
R_sNCH (n-ch S/D)= x_jNCH(S/D)= x_jWELL(S/D)=

25.0 **Contact Photo:** Mask-CONT
Spin, expose, hand develop, descum, hard bake.

26.0 **Contact Etch**

26.1 Plasma etch in TechnicsC:
Wet etch - bake - plasma etch - wet etch
Measure t_{ox} between steps to estimate etch time.

26.2 Remove resist and piranha clean wafers.

26.3 Do a 25/1 HF dip just before metallization.

27.0 **Metallization:** target = 6000Å
Sputter Al/1% Si on all wafers.

28.0 **Metal Photo:** Mask-METL

28.1 Spin, expose, develop, descum, hard bake.

28.2 Wet etch Al. (Wet wafers first in DI water.)

28.3 Do not remove resist.

29.0 **Back Side Etch**

29.1 Spin photoresist (front side),
hard bake for 20 minutes at 120°C

29.2 Spin photoresist again,
hard bake for 20 minutes at 120°C.

29.3 Etch back side of wafers as follows:
a) Dip off oxide in BHF.
b) Wet etch poly-Si (gate thickness).
c) Final dip in BHF until back dewets.

29.4 Remove resist: plasma or acetone (no pirahna!) t_{Al}=

29.5 Rinse wafers in DI water for 20 minutes, dry.

30.0 **Sintering:** 400°C for 20 minutes in forming gas.

End of Process

Microlab N-WELL CMOS Process

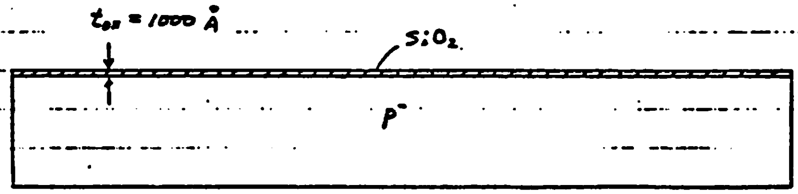
Mask Descriptions:

1. N-Well Implant:	WELL (df-emulsion)
2. Active Area:	ACTV (cf-emulsion)
3. Field Implant:	FPII (cf-emulsion)
4. Gate Definition:	POLY (cf-emulsion)
5. N-Channel S/D:	NNII (df-emulsion)
6. P-Channel S/D:	PPII (df-emulsion)
7. Contact Opening:	CONT (df-emulsion)
8. Metal:	METL (cf-emulsion)
9. Passivation:	PAD (df-emulsion)

Ion Implantations:

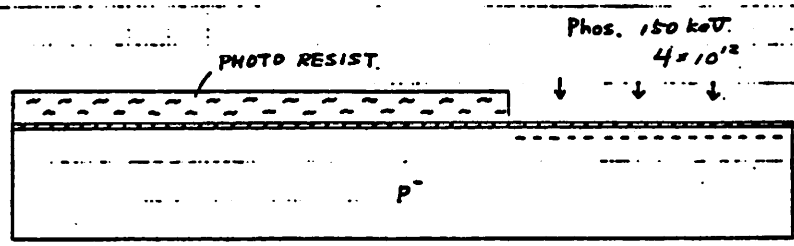
1. Well Implant:	Phosphorus (P^+), 150 KeV, $4.0 \times 10^{12}/cm^2$
2. Field Implant:	Boron (B^{11}), 100 KeV, $1.0 \times 10^{13}/cm^2$
3. Threshold Adjust:	Boron (B^{11}), 30 KeV, $1.0 \times 10^{12}/cm^2$
4. N+ Source/Drain Implant:	Arsenic (As^+), 100 KeV, $3.0 \times 10^{15}/cm^2$
5. P+ Source/Drain Implant:	Boron (B^{11}), 50 KeV, $2.0 \times 10^{15}/cm^2$

BERKELEY N-CMOS PROCESS



INITIAL OXIDATION

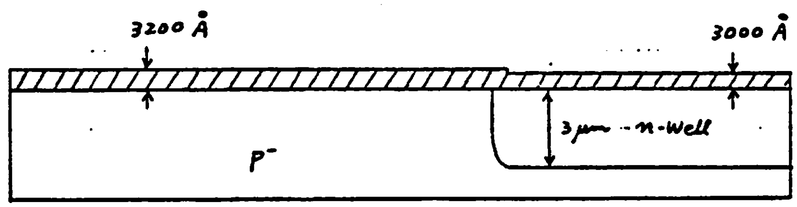
750 → 1000°C N_2 2°C/min
1000°C O_2 { 5 min dry, 11 min wet, 5 min dry }
1000°C N_2 20 min
1000 → 750°C N_2



WELL PHOTO

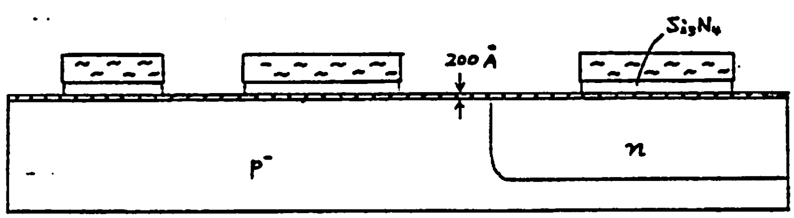
WELL IMPLANTATION

Phos.
150 keV
4×10^{12} cm^{-2}



WELL DRIVE-IN

1150°C O_2 240 min
1150°C N_2 240 min



PAD OXIDATION

950°C O_2 28 min
950°C N_2 20 min

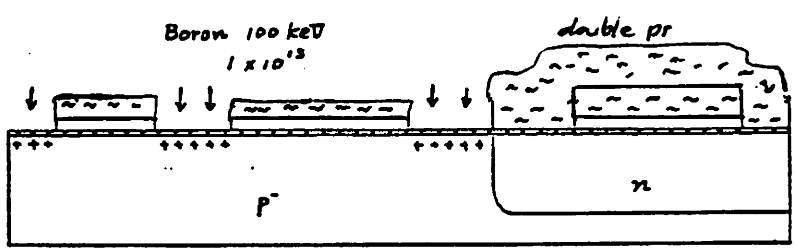
Si_3N_4 DEPOSITION

1000 Å

ACTV PHOTO

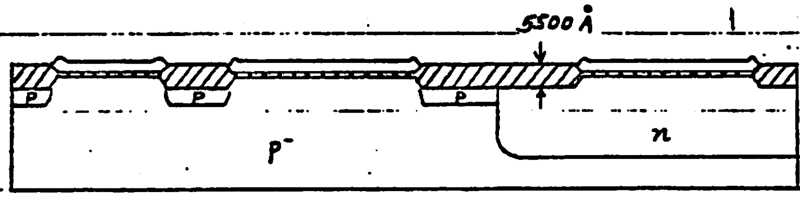
Plasma etch Si_3N_4
Hard bake, 30 min, 150°C

FPII PHOTO



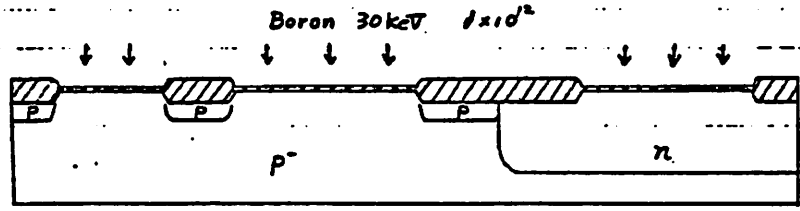
FIELD IMPLANTATION

Boron
100 keV
1×10^{13} cm^{-2}



LOCOS OXIDATION

950°C wet 200 min
950°C N_2 20 min



Si_3N_4 REMOVAL

Wet etch

SACRIF. OXIDE GROWTH

950°C O_2 28 min
950°C N_2 20 min

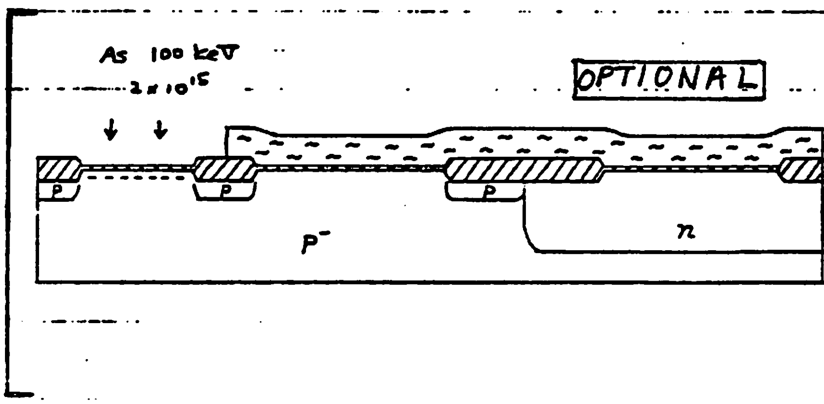
THRESHOLD ADJUSTMENT IMPLANTATION

Boron

30 keV

1×10^{12} cm^{-2}

($V_{TN} = 0.8$, $V_{TP} = -0.8$)



OPTIONAL

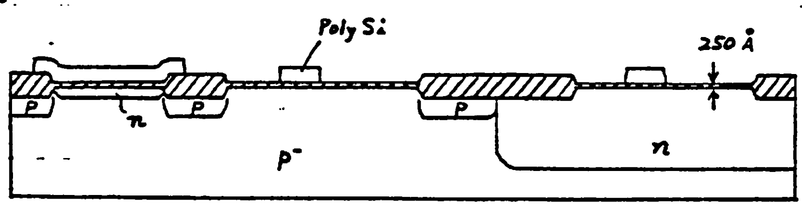
CAP PHOTO

CAPACITOR IMPLANTATION

As.

100 keV.

2×10^{15} cm^{-2}



GATE OXIDATION

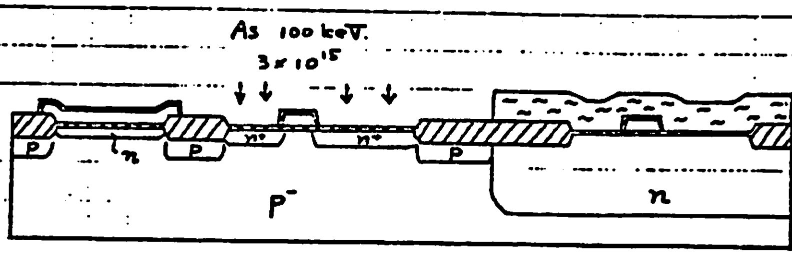
950°C O_2 40 min
950°C N_2 20

POLY DEPOSITION

0.45μm

GATE PHOTO

Plasma etch poly-Si



POLY+ S/D REOXIDATION

850°C wet O_2 30 min

$t_{ox} = \begin{cases} 1000\ \text{Å} & \text{on Poly} \\ 500\ \text{Å} & \text{on S/D} \end{cases}$

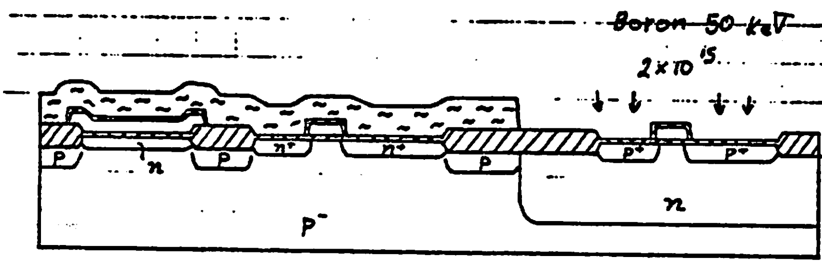
NNII PHOTO

N+ S/D IMPLANTATION

As
100 keV.
$3 \times 10^{15}\ cm^{-2}$

N+ S/D DRIVE-IN

925°C N_2 75 min



PPII PHOTO

P+ S/D IMPLANTATION

Boron.
50 keV
$2 \times 10^{15}\ cm^{-2}$

PSG DEPOSITION

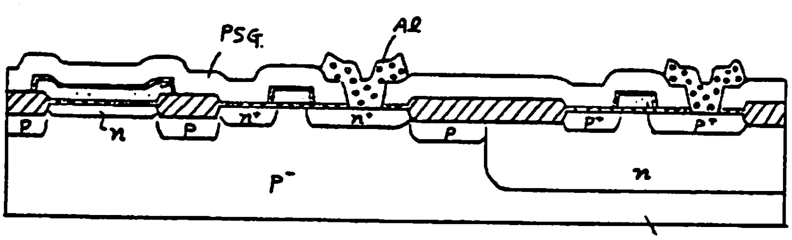
0.2 μm nondoped LTO
0.4 μm PSG
0.1 μm LTO

PSG DENSIFICATION

950°C wet O_2 30 min

CONT PHOTO

Plasma etch cont.



Al DEPOSITION

Al-2%Si 0.6 μm

METAL PHOTO

Wet etch Al
Backside eth

SINTERING

400°C N_2/H_2

Appendix II

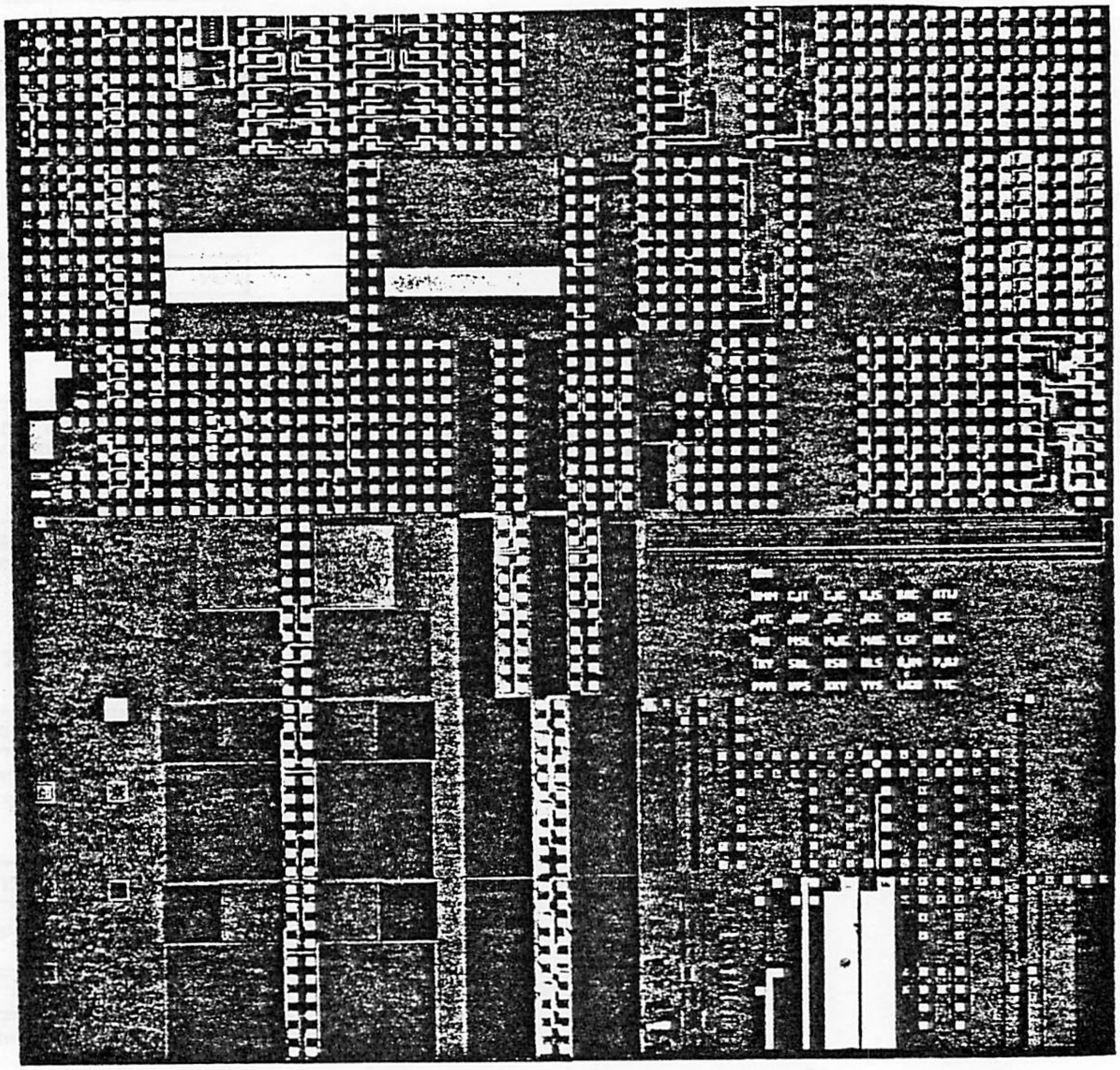
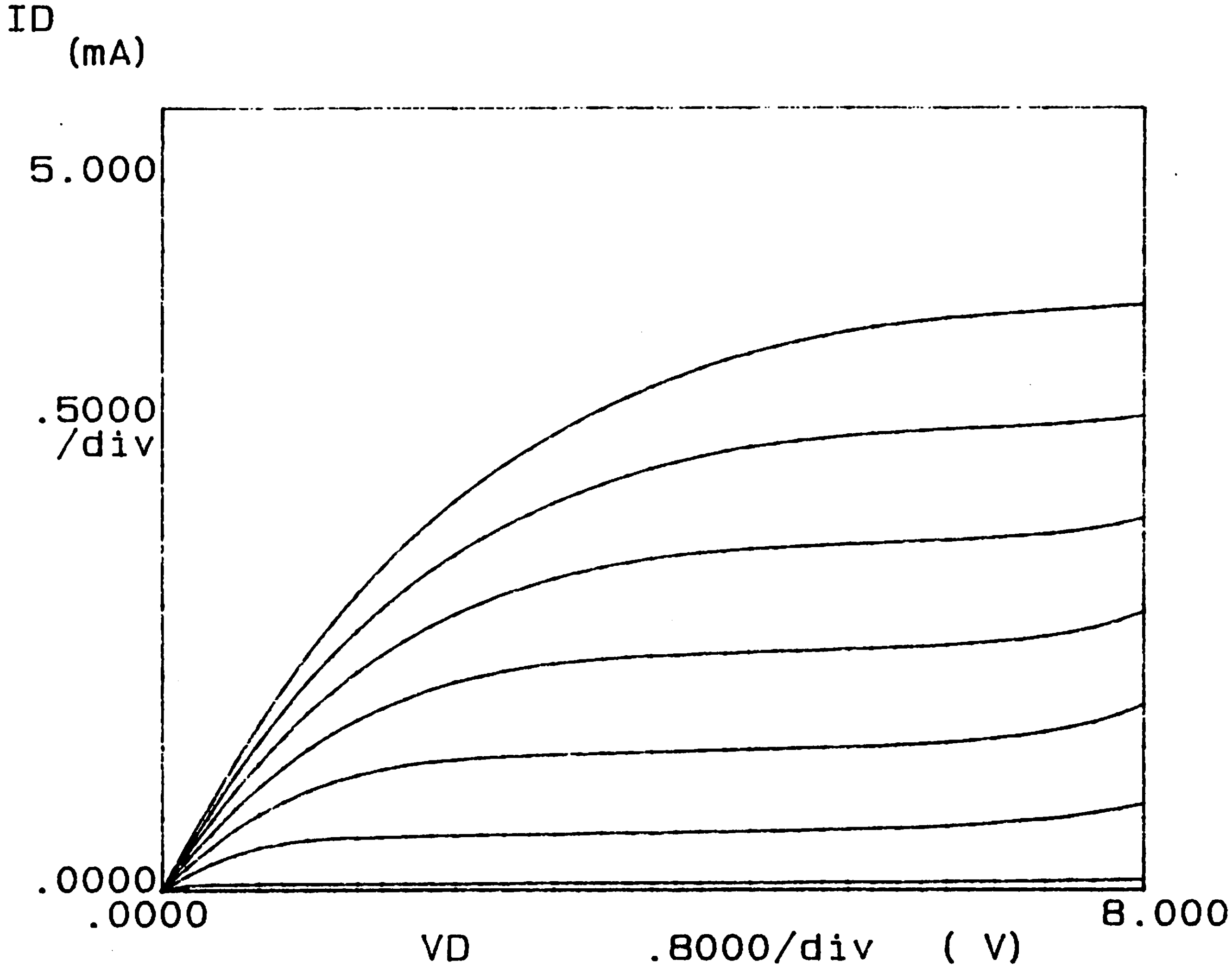


Figure 1. Photomicrograph of Test Chip from Wafer CMOS2-9
(Device Description in References 2 and 3)

****** GRAPHICS PLOT ******

CMOS2-7 19.2/2.4 NMOS 9/26/86



Variable1:
VD -Ch1
Linear sweep
Start .0000V
Stop 8.0000V
Step .2000V

Variable2:
VG -Ch4
Start .0000V
Stop 7.0000V
Step 1.0000V

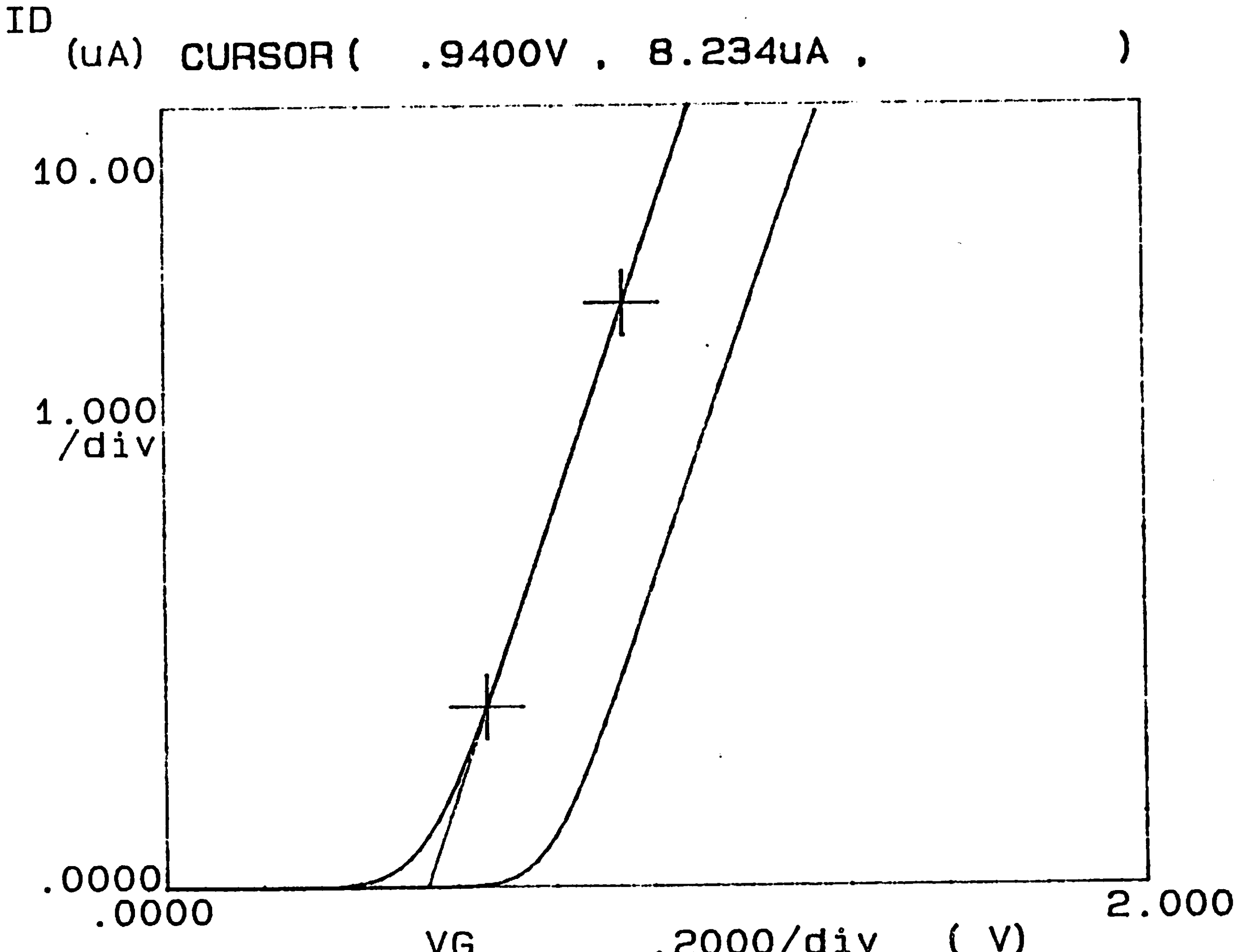
Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 2a. L=2.4um NMOS Device

ROUT (Ω) = ΔVD/ΔID
GD (/Ω) = ΔID/ΔVD

****** GRAPHICS PLOT ******

CMOS2-7 19.2/2.4 NMOS 9/26/86



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	20.4E-06	49.1E+03	536E-03	-10.9E-06
LINE2				

ISUB (A) = ABS(ISU)
I ( ) = 1

Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 2.0000V
Step .0200V

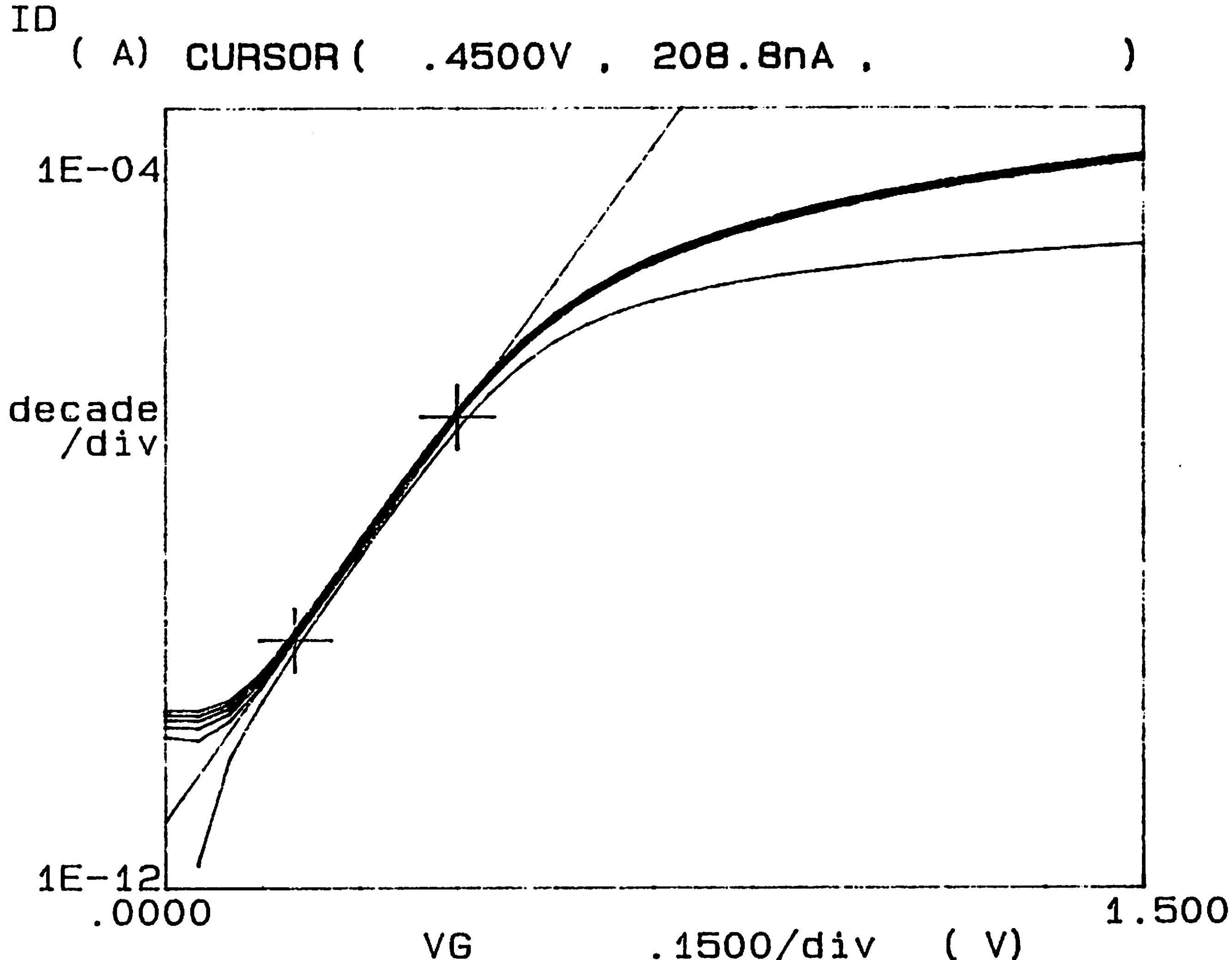
Variable2:
VSUB -Ch3
Start .0000V
Stop -1.0000V
Step -1.0000V

Constants:
VD -Ch1 .0500V
VS -Ch2 .0000V
V1 -Vs1 .0000V

Figure 2 b. L=2.4um
V_t=0.54V

******* GRAPHICS PLOT *******

CMOS2-7 19.2/2.4 NMOS 9/26/86



Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 1.5000V
Step .0500V

Variable2:
VD -Ch1
Start .0500V
Stop 5.0490V
Step 1.0000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

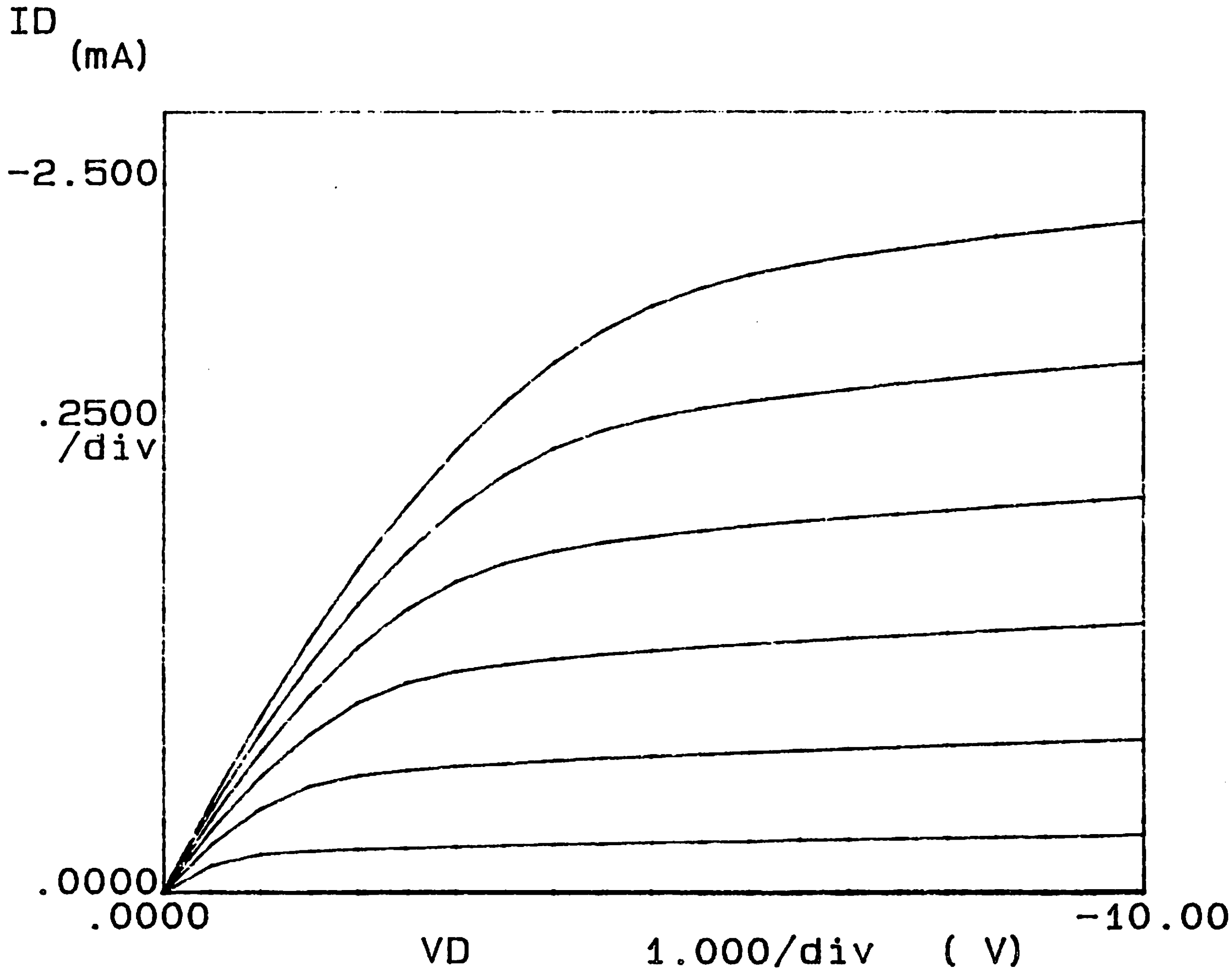
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	10.1E+00	98.5E-03	1.11E+00	5.66E-12
LINE2				

ISUB (A) = ABS(ISU)

Figure 2c. Subthreshold Current Characteristics of L=2.4um NMOS

****** GRAPHICS PLOT ******

CMOS2-7 19.2/2.4 B+ PMOS 9/26



Variable1:
VD -Ch1
Linear sweep
Start .0000V
Stop -10.000V
Step - .5000V

Variable2:
VG -Ch4
Start .0000V
Stop -7.0000V
Step -1.0000V

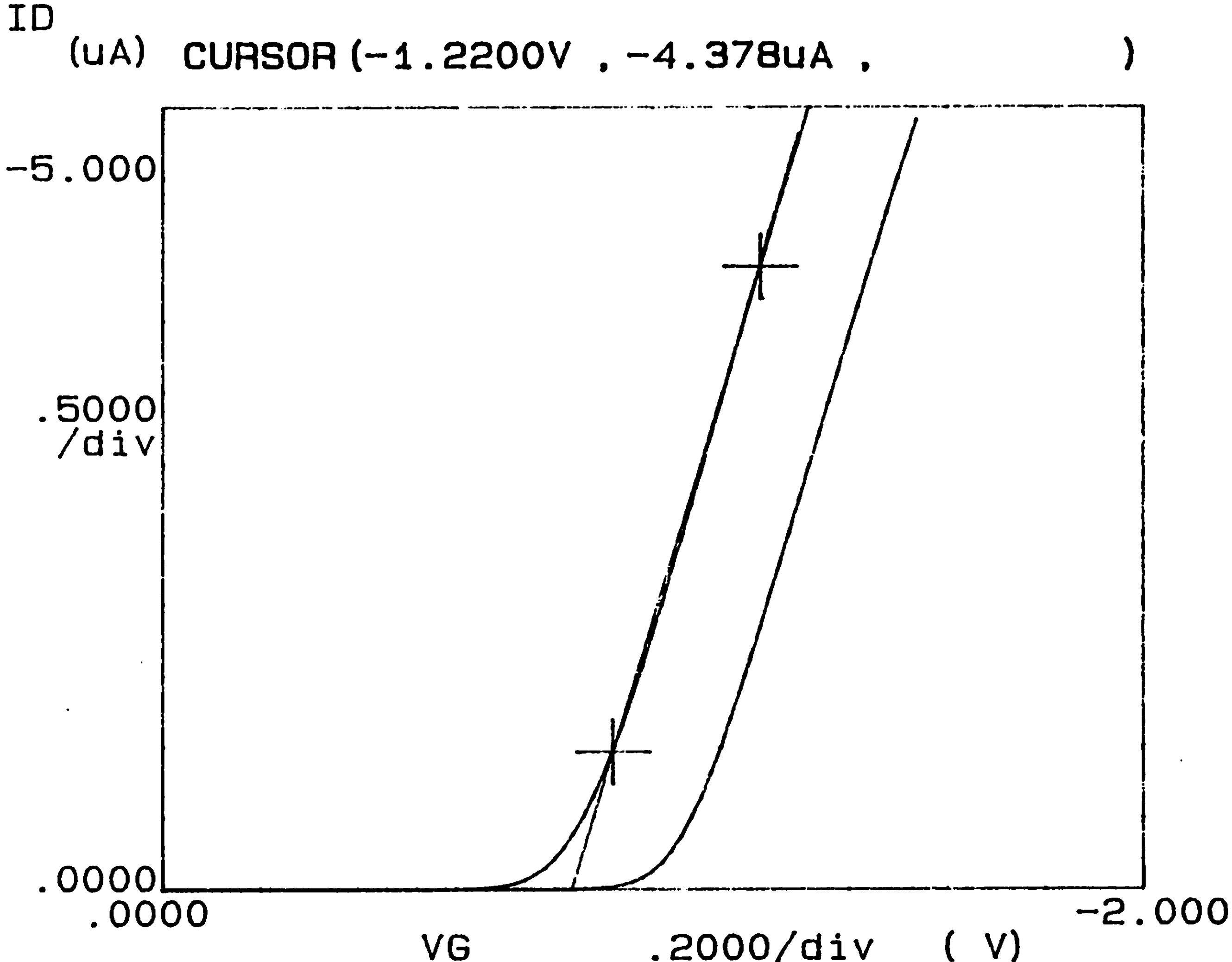
Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

Figure 3a. L=2.4um PMOS Device

ROUT (Ω) = ΔVD/ΔID
GD (/Ω) = ΔID/ΔVD

****** GRAPHICS PLOT ******

CMOS2-7 19.2/2.4 B+ PMOS 9/26



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	11.4E-06	87.8E+03	-836E-03	9.52E-06
LINE2				

ISUB (A) = ABS (ISU)
I ( ) = 1

Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop -2.0000V
Step - .0200V

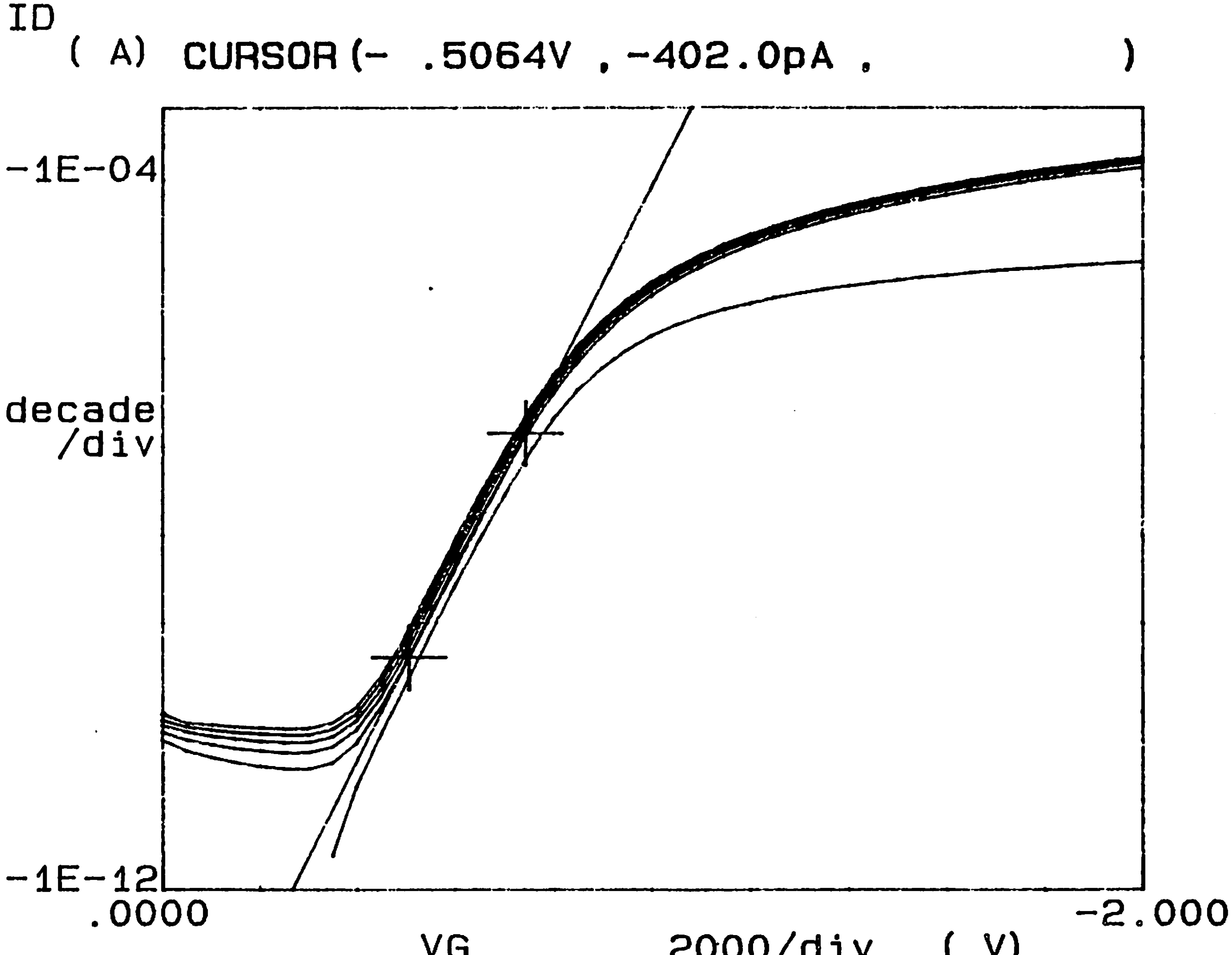
Variable2:
VSUB -Ch3
Start .0000V
Stop 1.0000V
Step 1.0000V

Constants:
VD -Ch1 - .0500V
VS -Ch2 .0000V

Figure 3b. L=2.4um
V_t=-0.84V

****** GRAPHICS PLOT ******

CMOS2-7 19.2/2.4 B+ PMOS 9/26



Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop -2.0000V
Step - .0500V

Variable2:
VD -Ch1
Start - .0500V
Stop -5.0500V
Step -1.0000V

Constants:
VS -Ch2 .0000V
VSUB -Ch3 .0000V

	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-10.8E+00	-92.8E-03	-1.38E+00	-1.41E-15
LINE2				

ISUB (A) = ABS(ISU)

Figure 3c. Subthreshold Current Characteristics of 2.4um PMOS Device

Appendix III

P-Well CMOS Process

Microlab CMOS Process

Version 2.4 (Jan. 13,1987)
3 μm, P-well, double poly-Si, single metal
(Capacitors formed last)
(Double field implant)

0.0 Starting Wafers: 8-12 ohm-cm, n-type, <100>
Control Wafers: PWELL (n-type), PCH (n-type)
Measure R_s on PWELL control.

1.0 Initial Oxidation: target = 1000Å

1.1 TCA clean furnace tube.

1.2 Standard clean wafers: piranha clean for 10 min,
10/1 HF dip, spin-dry.
Include one n-type control: PWELL.
Measured R_s= on PWELL control

1.3 Wet oxidation at 1000°C:
5 min dry O_2
11 min wet O_2
5 min dry O_2
20 min dry N_2
Measured t_{ox}= on PWELL cont.

2.0 N- (Punch-Through) Implant:
Blanket implant of phosphorous at 145 keV, $1.2\text{x}10^{12}/cm^2$
Include PWELL control.

3.0 Well Photo Mask: PWELL-CW (chrome-df)
Control wafers are not included in the photoresist steps.

3.1 Standard clean wafers.
Dehydrate in furnace for 5 minutes at 750°C.

3.2 Spin resist on Eaton: Kodak 820, 4600 RPM, 25 seconds,
soft bake at 120°C, 45 seconds

3.3 Expose: GCA 6200-10X wafer stepper

3.4 Develop in MTI-Omnichuck: Kodak 932/H2O=1:1, 60 seconds

3.5 Descum in TechnicsC: O_2 plasma, 50 W, 1 minute

3.6 Hard bake in oven: 120°C, 20 minutes in air.

4.0 Well Implant: Boron (B11), $3\text{x}10^{12}/cm^2$, 80 KeV
(Resist is left on wafers.) Include PWELL control (no resist).

5.0 Well Drive-In: target x_j = 4 μm, t_{ox} = 3000Å

5.1 TCA clean furnace tube.

5.2 Etch pattern into oxide in 5/1 BHF. Include PWELL control.

Measured R_s= on PWELL control

5.3 Remove resist and piranha clean wafers.

5.4 Standard clean wafers, include PWELL control.

5.5 Dry oxidation and well drive at 1150°C:
4 hrs dry O_2
5 hrs dry N_2
Measure oxide thickness on work wafer: in well and outside

6.0 Locos Pad Oxidation/Nitride Deposition:
target = 200Å SiO_2 + 1000Å Si_3N_4

6.1 TCA clean furnace tube.

6.2 Remove all oxide in 5/1 BHF until wafers dewet.
Include PWELL control.

6.3 Standard clean wafers.

6.4 Dry oxidation at 950°C:
28 min dry O_2
20 min dry N_2 anneal.
a) Measured t_{ox}= on PWELL control
b) Strip oxide off of PWELL control in BHF.

6.5 Deposit 1000Å of Si-nitride immediately:
Dep.time = 22 minutes, temp.= 800°C.
a) Include PWELL control. Measured t_{nit}=
b) Strip nitride and measure R_s on PWELL cont.
c) Save PWELL control for Step 13.2

7.0 Active Area Photo Mask: ACTIVE-CD (emulsion-cf)
Spin, expose, develop, descum, hard bake.

8.0 Nitride Etch: TechnicsC plasma etcher
Do not etch oxide, do not remove resist.

9.0 Field (P-) Implant Photo Mask: PWELL-CW (chrome-df)

9.1 Spin, expose, develop, descum, hard bake.(Double photo)
Field inside well is open, active areas are covered
with Si_3N_4 and pr.

9.2 Measure resist thickness on active area with profilometer.
Wafers cannot be passed unless pr is 0.8 μm thick .

10.0 Field Ion Implantation

10.1 Boron (B11), 100 KeV, $1x10^{13}/cm^2$

10.2 Remove resist and piranha clean wafers.

10.3 Standard clean and bake wafers for 5 min at 750°C in N_2.

10.4 Field (N-) implant photo: PWELL mask (emulsion-cf)
Well area is covered with pr, active areas with Si_3N_4.

10.5 Phosphorous implant, 40 KeV, 3-5x10^{12}/cm^2.

10.6 Remove resist and piranha clean wafers.

11.0 **Locos Oxidation:** target = 6500Å

11.1 TCA clean furnace tube.

11.2 Standard clean wafers: dip until field area dewets.

11.3 Wet oxidation at 950°C:
5 min dry O_2
4 hrs 40 min wet O_2
5 min dry O_2
20 min N_2 anneal
Measured t_{ox}= on a device wafer in the field area

12.0 **Nitride Removal**

12.1 Oxide dip in 10/1 HF for 1 minute

12.2 Etch nitride off in hot phosphoric acid: 145°C, 30 minutes

13.0 **Sacrificial Oxide:** target = 200Å

13.1 TCA clean furnace tube.

13.2 Standard clean wafers. Include PWELL control.

13.3 Dry oxidation at 950°C:
28 min dry O_2
20 min N_2 anneal
a) Measured t_{ox}= on PWELL control
b) Do not include PWELL control in Step 14.

14.0 **Threshold Implant:**
Blanket implant boron (B^{11}) at 30 KeV.
3x10^{11}/cm^2 & 5x10^{11}/cm^2.

15.0 **Gate Oxidation/Poly-Si Deposition:**
target = 500Å SiO_2 + 4500Å poly-Si

15.1 TCA clean furnace tube; reserve poly-Si deposition tube.

15.2 Standard clean wafers.include PWELL control and
one n-type control: PCH.

15.3 Dip off sacrificial oxide (dewet) in 10/1 HF (approx. 1 min).

15.4 Dry oxidation at 950°C:
2 hr. 10 minutes dry O_2

20 min N_2 anneal.
t_{ox}(PWELL)= t_{ox}(PCH)=

15.5 Immediately after oxidation deposit 4500Å of phos.doped poly-Si.
time = 2 hr. 15 minutes, temp.= 650°C
Do not include PWELL, PCH controls; include a new control with 1000Å thermal SiO_2 on it. t_{poly}=

16.0 Gate Definition Mask: POLY-CP (emulsion-cf)

16.1 Spin, expose, develop, descum, hard bake.

16.2 Plasma etch poly-Si in LAM etcher (CCl4). Inspect.

16.3 Remove resist, piranha clean wafers.

17.0 Reoxidation: target=800Å on poly-Si, 500Å on S/D

17.1 TCA clean furnace tube.

17.2 Standard clean wafers, include both controls, PWELL, PCH.
From here on: only 10 seconds dip in 25/1=H2O/HF after piranha.
NOT MORE!

17.3 Dry oxidation at 950°C:
30 min dry O_2
10 min N_2 anneal.
t_{ox}(PWELL) = t_{ox}(PCH) =

18.0 N-Channel Source/Drain Photo Mask: PII-CS (emulsion-cf)
Spin, expose, develop, descum, hard bake.

19.0 N+ Source/Drain Implant

19.1 Implant arsenic at 100 KeV, $3x10^{15}/cm^2$, incl. PWELL cont.

19.2 Remove resist and piranha clean wafers (no dip here).

20.0 N+ S/D Drive-In

20.1 TCA clean furnace tube.

20.2 Standard clean wafers, include PWELL control (10 seconds dip).

20.3 Anneal wafers in N_2 at 925°C for 1hr 15minutes

21.0 P-Channel Source/Drain Photo Mask: NII (chrome-df)
Spin, expose, develop, descum, hard bake.

22.0 P+ S/D Implant

22.1 Implant B11 at 50 KeV, $2x10^{15}/cm^2$, include PCH control.

22.2 Remove resist and standard clean wafers (no dip).

23.0 Capacitor Formation: SiO_2 target = 800Å

23.1 TCA clean furnace tube; reserve poly-Si deposition tube.

23.2 Standard clean wafers (10 seconds dip). Include PCH control.

23.3 *Capacitor oxidation at 950°C:
30 min dry O_2, 10 min N_2 anneal
t_{ox}(PCH)= t_{ox}(POLY)=

23.4 Second Poly-Si deposition: target = 2000Å
Immediately after anneal deposit 4500Å of phos.doped poly-Si: time = 1 hr., temp.= 650°C
Include only a new control with 1000Å SiO_2. t_{poly}=

24.0 Capacitor Photo Mask: CAP-CE (emulsion-cf)

24.1 Spin, expose, develop, descum, hardbake.

24.2 Plasma etch poly-Si in LAM etcher. Inspect.
Do not remove resist.

25.0 Back Side Etch

25.1 Spin photoresist (front side), do not expose; hard bake.

25.2 Spin photoresist again, and hard bake.

25.3 Etch back side of wafers as follows:
a) Dip off oxide in BHF.
b) Wet etch poly-Si (cap. poly thickness).
c) Etch capacitor oxide off in BHF.
d) Wet etch poly-Si (gate poly thickness).
e) Final dip in BHF until back dewets.

25.4 Remove resist and piranha clean wafers (no dip).
Measure oxide thickness in S/D area.

26.0 Reflow Glass: target = 7000Å

26.1 Standard clean wafers (10 second dip).
Include only one new, PSG control.

26.2 Deposit PSG : incl.PSG control
Layers: 1000Å undoped LTO (~ 5 minutes)
6000Å PSG (PH3 flow at 10.3) (~ 30 minutes)
time = (approx) 35 minutes total (check current dep rates)
temp. = 450°C
t_{PSG}= on PSG cont.

26.3 Densify glass in tube 2 at 950°C:
include PSG, PWELL, PCH cont.
5 min dry O_2, 30 min wet O_2, 5 min dry O_2

26.4 Do wet oxidation dummy run afterwards to clean tube:
1 hr wet oxidation at 950°C.

26.5 Measurements on WELL and NCH controls:
Cut piece off for x_j measurement,
strip oxide from rest of wfr.
R_sPWELL(n-ch S/D)=
R_sPCH(p-ch S/D)=
x_jPCH(P+S/D)=
x_jPWELL(N+S/D)=
x_jPWELL(well)=

27.0 **Contact Photo Mask:** CONTACT-CC (chrome-df)
Spin, expose, hand develop, descum, hard bake.

28.0 **Contact Etch**

28.1 Plasma etch in TechnicsC in CHF3/O_2
Do etch - bake - etch sequence as follows:
a) Wet etch in 10:1 BHF until 5K-6K oxide is left.
b) Bake wafer for 5 minutes at 120°C in air.
c) Plasma etch at 100 watts, pressure ~ 150 mTorr,
CHF3=7.0 sccm, O_2=2.0 sccm,
until approximately 300-400Å of SiO_2 remains.
d) Wet etch in 10:1 BHF until clear.
e) Spin dry at 1000 rpm. Inspect.

28.2 Back side etch:
a) Spin resist on front side again.
b) Etch in 5:1 BHF until back clears.

28.3 Remove resist in O_2 plasma: 3 minutes at 300 watts.
and piranha clean wafers (no dip after first piranha).

28.4 Do a 20 seconds 25/1 HF dip just before metallization.

29.0 **Metallization:** target = 6000Å
Sputter Al/2% Si on all wafers. (1 minute 30 seconds at 1200 watts)

30.0 **Metal Photo Mask:** METAL1-CM (emulsion-cf)

30.1 Spin, expose, develop, descum, hard bake.

30.2 Wet etch Al. (Wet wafers first in DI water.)

30.3 Remove resist with acetone (no piranha!) tAl=

30.4 Rinse wafers in DI water for 20 minutes, dry.

31.0 **Sintering:** 400°C for 20min in forming gas.

End of Process

Appendix III

List #1 is the masks as they will be used during the process.

MOSIS	UCB	mask type	description
CW	PWELL-CW	chrome	dark field
CD	ACTIVE-CD	emulsion	clear field
CP	POLY-CP	emulsion	clear field
CS	N+II	chrome	dark field
CS	P+II-CS	emulsion	clear field
CE	CAP-CE	emulsion	clear field
CC	CONTACT-CC	chrome	dark field
CM	METAL1-CM	emulsion	clear field
CM2	METAL2-CM2	emulsion	clear field
CV	VIA-CV	chrome	dark field

List #2 is the masks as they should be generated. Note especially, that masks #4, 5, 6, should be generated as closely together as possible, preferably within 24 hours.

MOSIS	UCB	mask type	description
(1) CW	PWELL-CW	chrome	dark field
(2) CV	VIA-CV	chrome	dark field
(3) CS	N+II	chrome	dark field
(4) CC	CONTACT-CC	chrome	dark field
(5) CD	ACTIVE-CD	emulsion	clear field
(6) CP	POLY-CP	emulsion	clear field
(7) CS	P+II-CS	emulsion	clear field
(8) CE	CAP-CE	emulsion	clear field
(9) CM	METAL1-CM	emulsion	clear field
(10) CM2	METAL2-CM2	emulsion	clear field

download date: Jan 30, 1986
file: CHIP.mann.s
sorted: yes
center: not specified
for: Microlab
by: Lyndon C. Lim

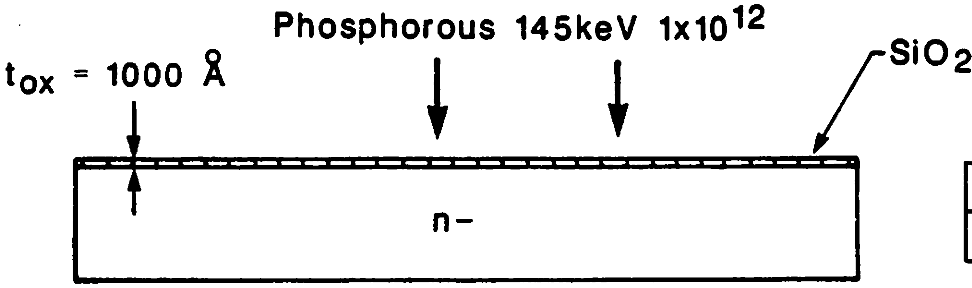
layer	scale(ktc)	scale(ctm)	invert	mask type	flashes
CW	0.1	10	no	chrome(5")	2626
CV	0.1	10	no	chrome(5")	12385
CS	0.1	10	no	chrome(5")	1703
CC	0.1	10	no	chrome(5")	49372
CD	0.1	10	no	emulsion(5")	7425
CP	0.1	10	no	emulsion(5")	11779
CS	0.1	10	no	emulsion(5")	1703
CE	0.1	10	no	emulsion(5")	976
CM	0.1	10	no	emulsion(5")	19259
CM2	0.1	10	no	emulsion(5")	4242

P-Well CMOS

Ion Implantations:

1. N^- (Punchthrough) Implant:	Phosphorus, 145 KeV, 1.2 x $10^{12}/cm^2$
2. P-Well Implant:	Boron (B^{11}), 80 KeV, 3.0 x $10^{12}/cm^2$
3. Field (P^-) Implant:	Boron (B^{11}), 100 KeV, 1.0 x $10^{13}/cm^2$
4. Field (N^-) Implant:	Phosphorus, 40 KeV, 4.0 x $10^{12}/cm^2$
5. Threshold Implant:	Boron (B^{11}), 30 KeV, 3.0 x $10^{11}/cm^2$
6. N^+ Source/Drain Implant:	Arsenic (As^+), 100 KeV, 3.0 x $10^{15}/cm^2$
7. P^+ Source/Drain Implant:	Boron (B^{11}), 50 KeV, 2.0 x $10^{15}/cm^2$

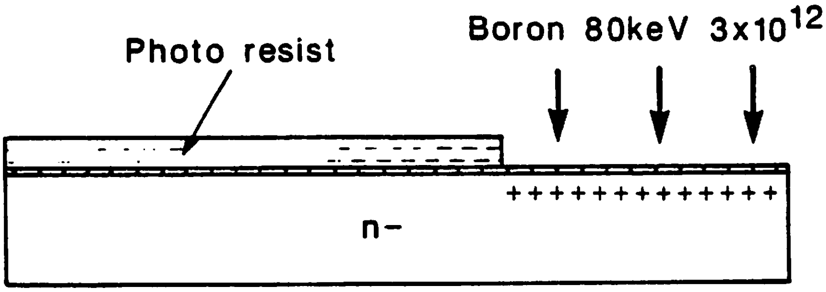
BERKELEY P-CMOS PROCESS



INITIAL OXIDATION

N- IMPLANT

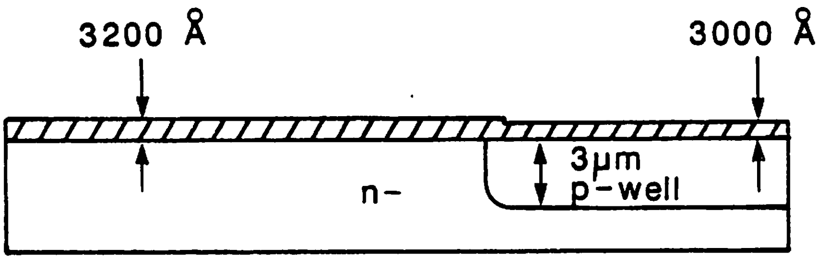
1000°C wet O_2 11 min
1000°C N_2 20 min
Phosphorous implant
145keV
$1x10^{12}$ cm^{-2}



WELL PHOTO

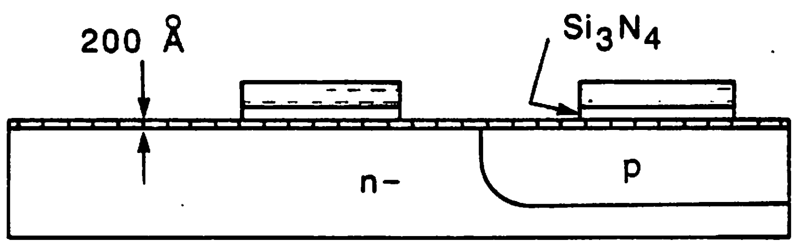
WELL IMPLANTATION

Boron
80keV
$3x10^{12} cm^{-2}$



WELL DRIVE-IN

1150°C O_2 240 min
1150°C N_2 300 min

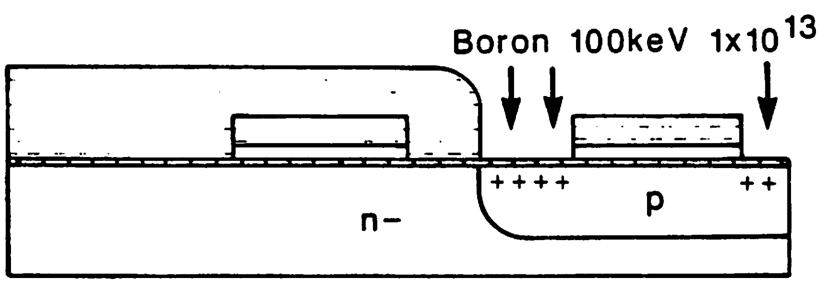


PAD OXIDATION

950°C O_2 28 min
950°C N_2 20 min

Si_3N_4 DEPOSITION

1000 Å



ACTV PHOTO

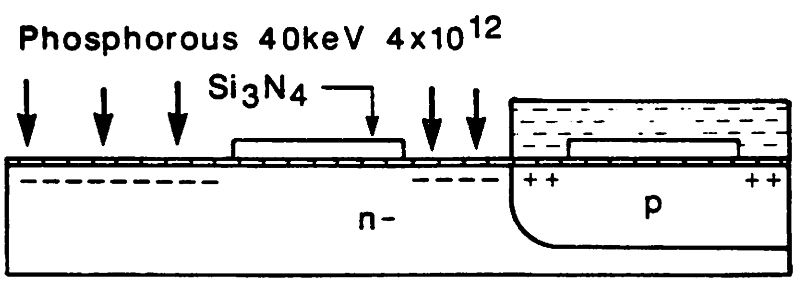
Plasma etch Si_3N_4
Hard bake, 30 min, 150°C

P-WELL MASK

Double photo

FIELD IMPLANTATION

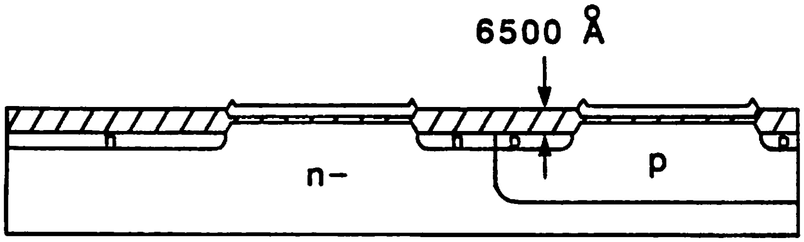
Boron
100keV
$1x10^{13} cm^{-2}$



REVERSED P-WELL MASK

FIELD (N-) ION IMPLANTATION

Phosphorous
40keV $4x10^{12} cm^{-2}$

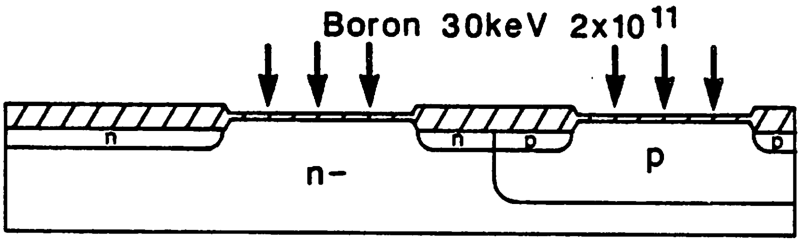


LOCOS OXIDATON

$950^{o}C$ wet O_2 280 min
$950^{o}C$ N_2 20 min

Si_3N_4 REMOVAL

Wet etch



SACRIF. OXIDE GROWTH

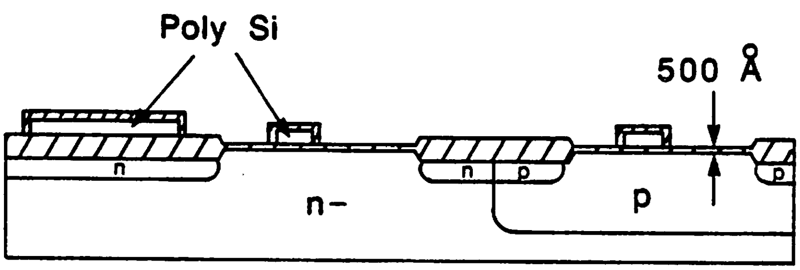
$950^{o}C$ O_2 28 min
$950^{o}C$ N_2 20 min

THRESHOLD ADJUSTMENT IMPLANTATION

Boron
30keV
$2x10^{11}cm^{-2}$
(VTN = 0.8, VTP = -0.8)

GATE OXIDATION

$950^{o}C$ O_2 130 min
$950^{o}C$ N_2 20 min



POLY DEPOSITION

Doped: 0.45μm

GATE PHOTO

Plasma etch poly-Si

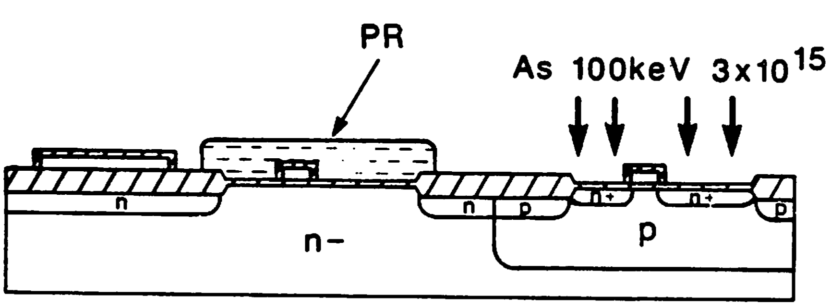
POLY+ S/D REOXIDATION

$950^{o}C$ O_2 30 min
N_2 10 min

$t_{ox} = \{$ 800 Å on Poly
500 Å on S/D

N+ S/D PHOTO

(p select mask)

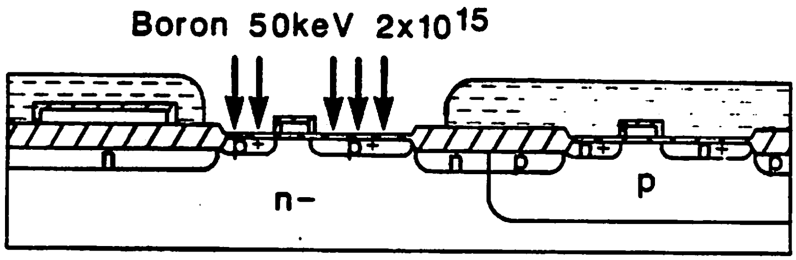


N+ S/D IMPLANTATION

As
100keV
$3x10^{15}cm^{-2}$

N+ S/D DRIVE-IN

$925^{o}C$ N_2 75 min

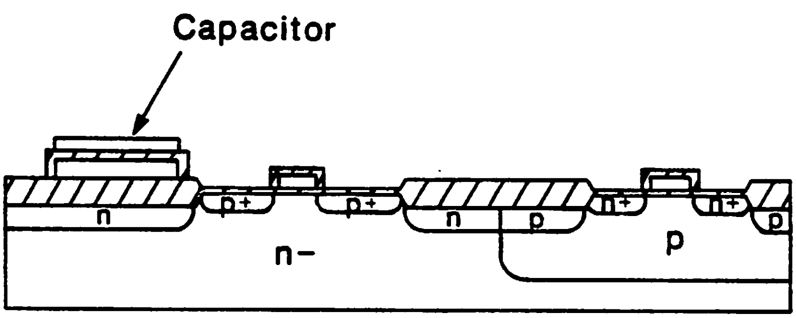


P+ S/D PHOTO

(Reversed p-select mask)

P+ S/D IMPLANTATION

Boron
50keV
$2\times10^{15}cm^{-2}$



CAPACITOR OXIDATION

$950^{o}C$ 30 min O_2
10 min N_2

SECOND POLY-Si

Doped: 0.2μm

CAPACITOR MASK

Plasma etch poly-Si
Backside etch

PSG DEPOSITION

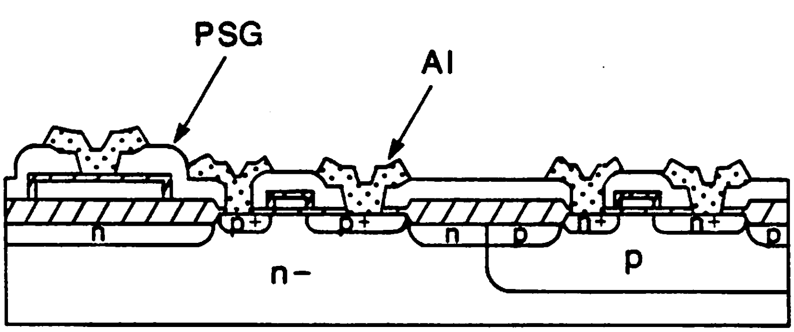
0.2μm undoped LTO
0.4μm PSG
0.1μm undoped LTO

PSG DENSIFICATION

$950^{o}C$ wet O_2 30 min

CONTACT PHOTO

Plasma etch cont.



Al DEPOSITION

Al-2%Si 0.6μm

METAL PHOTO

Wet etch Al
Backside etch

SINTERING

$400^{o}C$ N_2/H_2 20 min

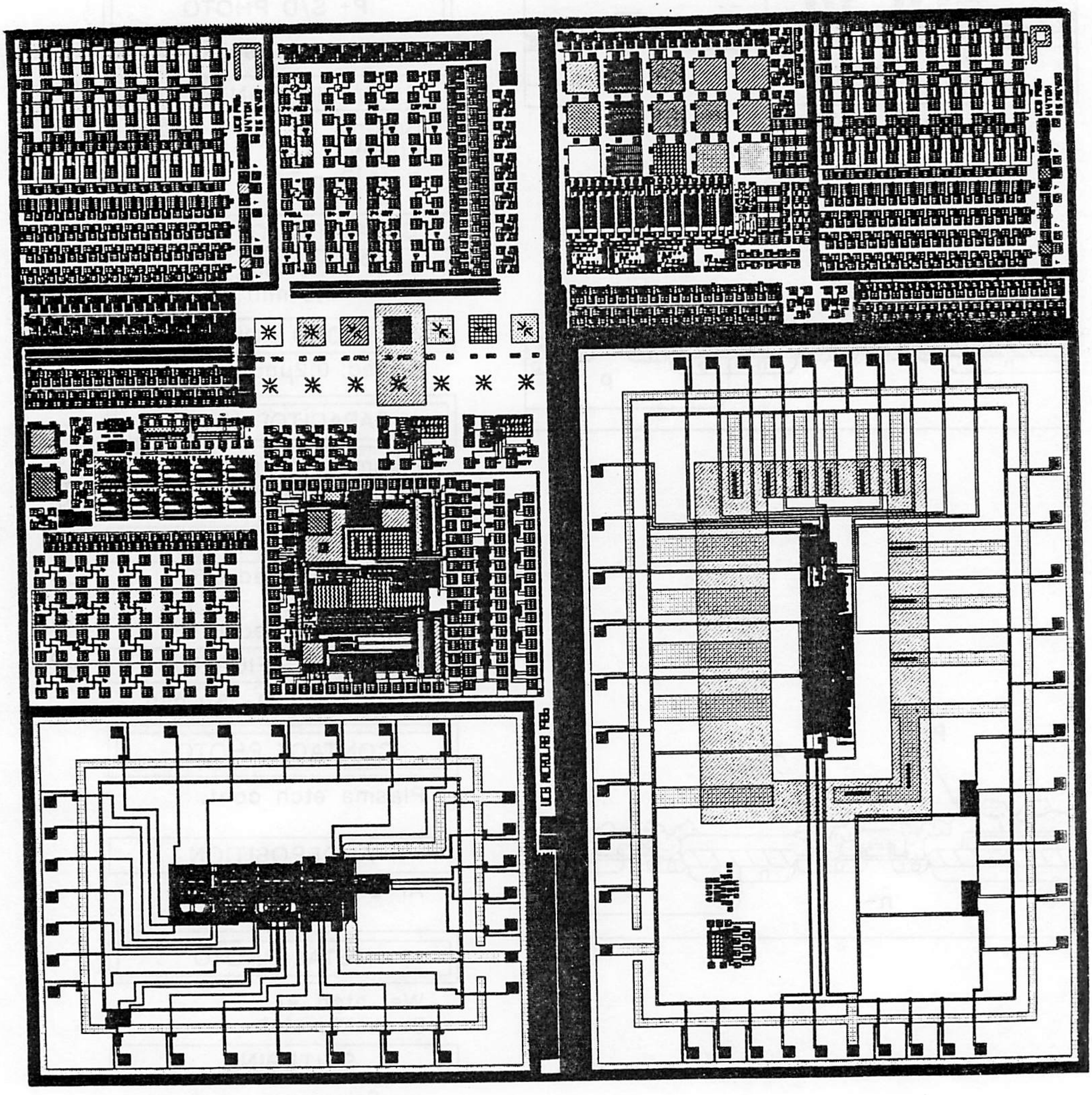


Figure 1. UCB Microlab Test Chip
P-Well CMOS
Test Structures by K. Y. Toh
January 1986

CCH

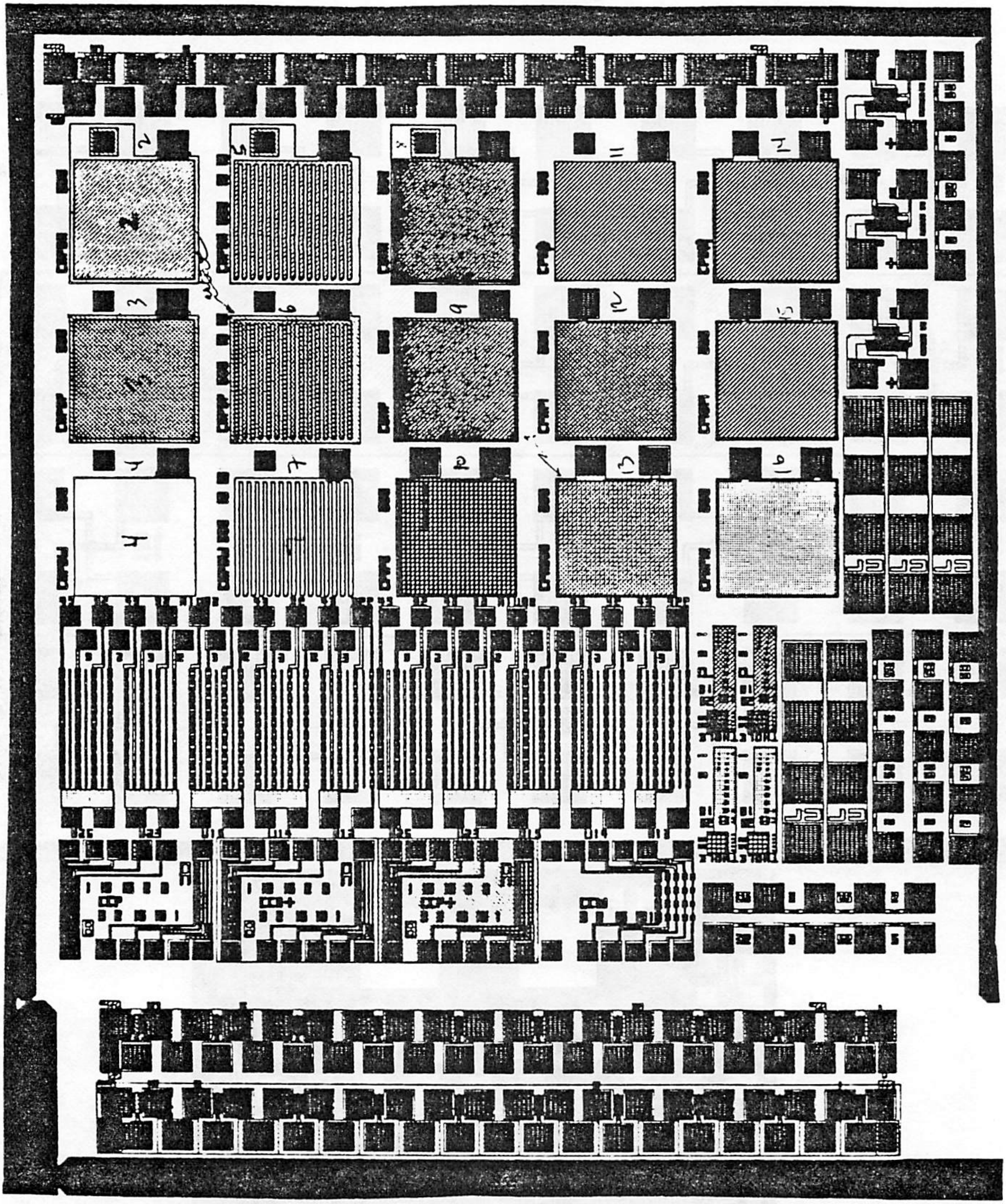


Figure 2. CCH Section
Capacitors and Contact Chains

CCR

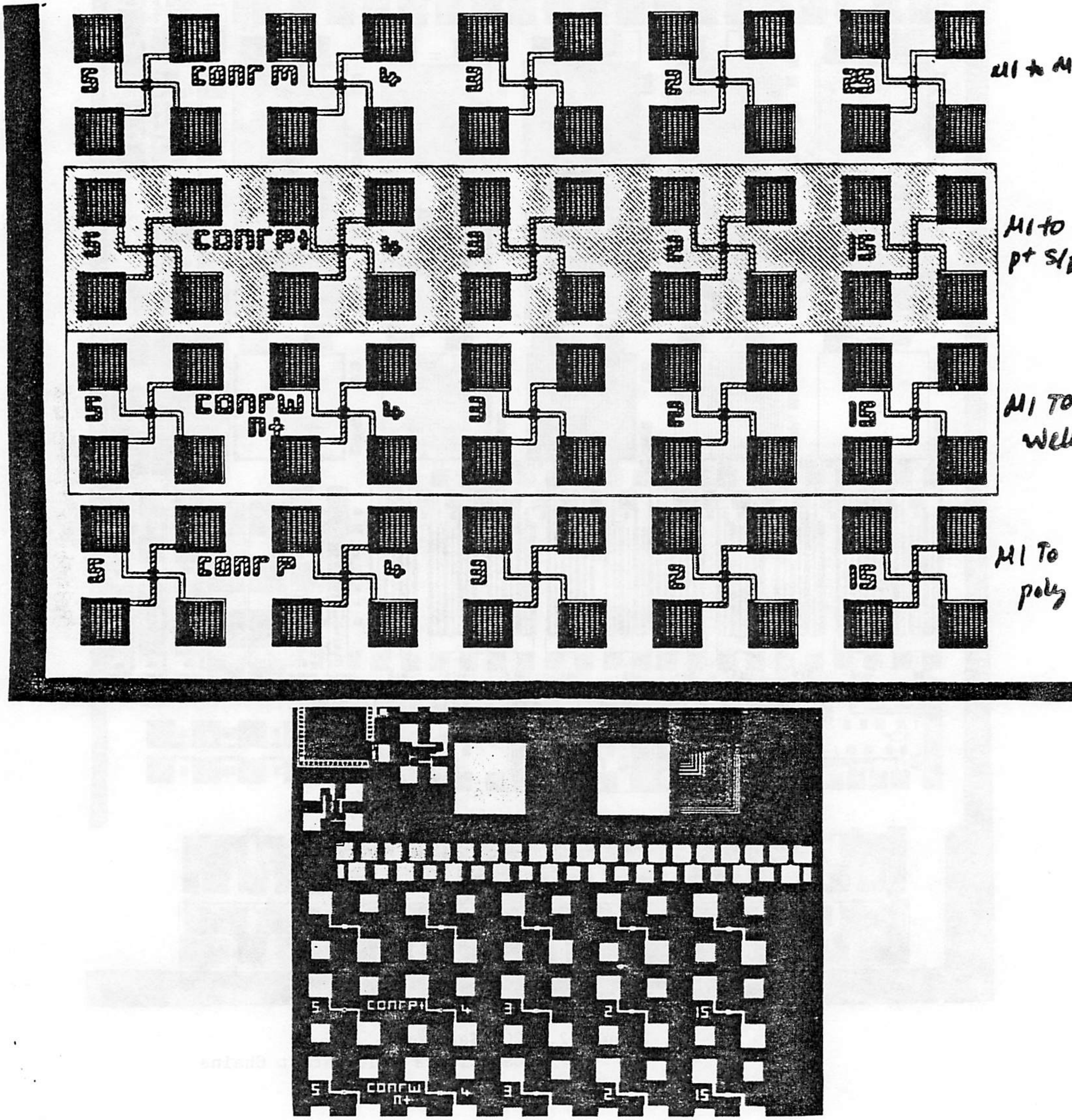


Figure 3. CCR Section
Contact Resistance

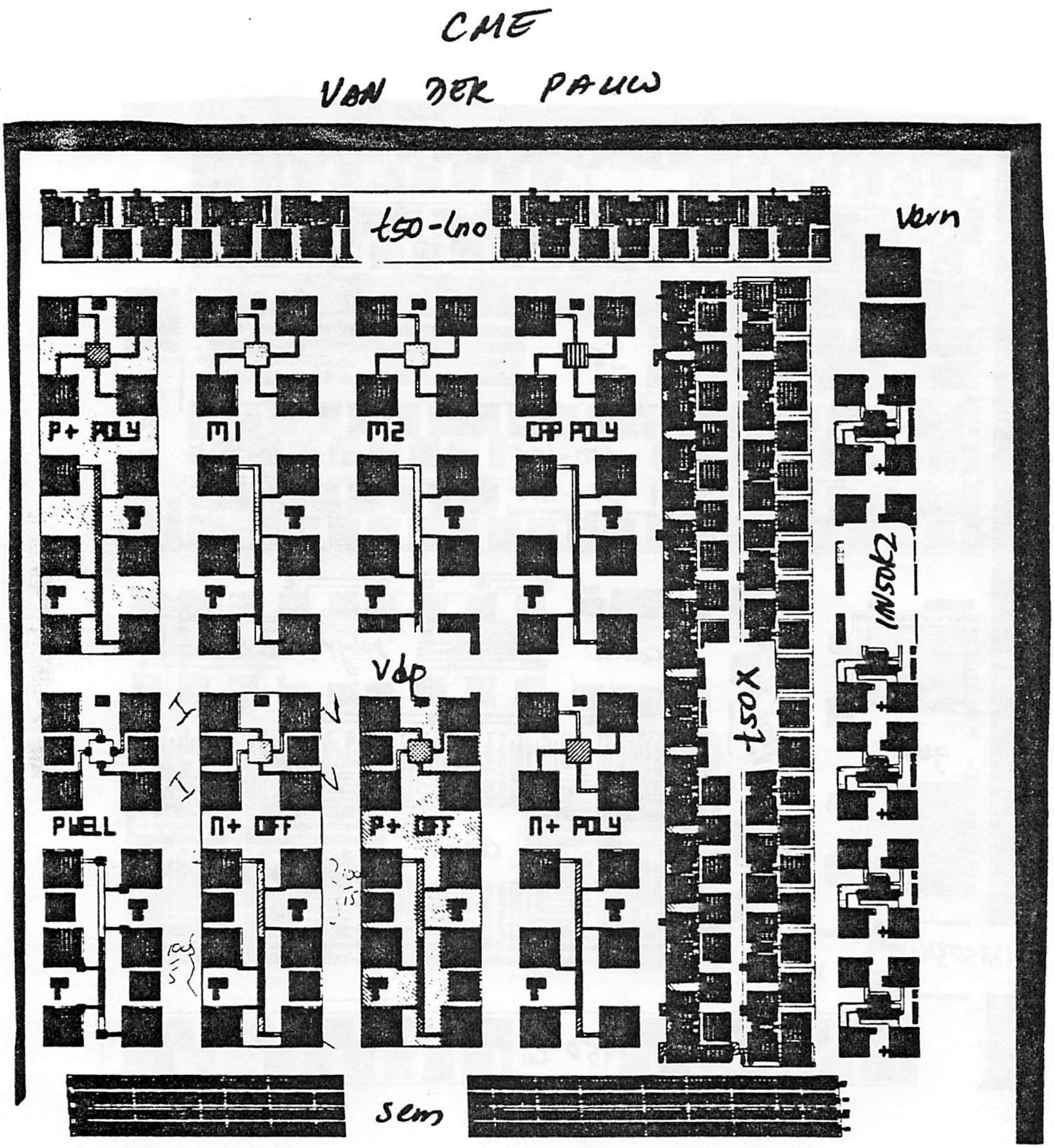


Figure 4. CME Section
Resistivity Test Structures, inverters

CVI

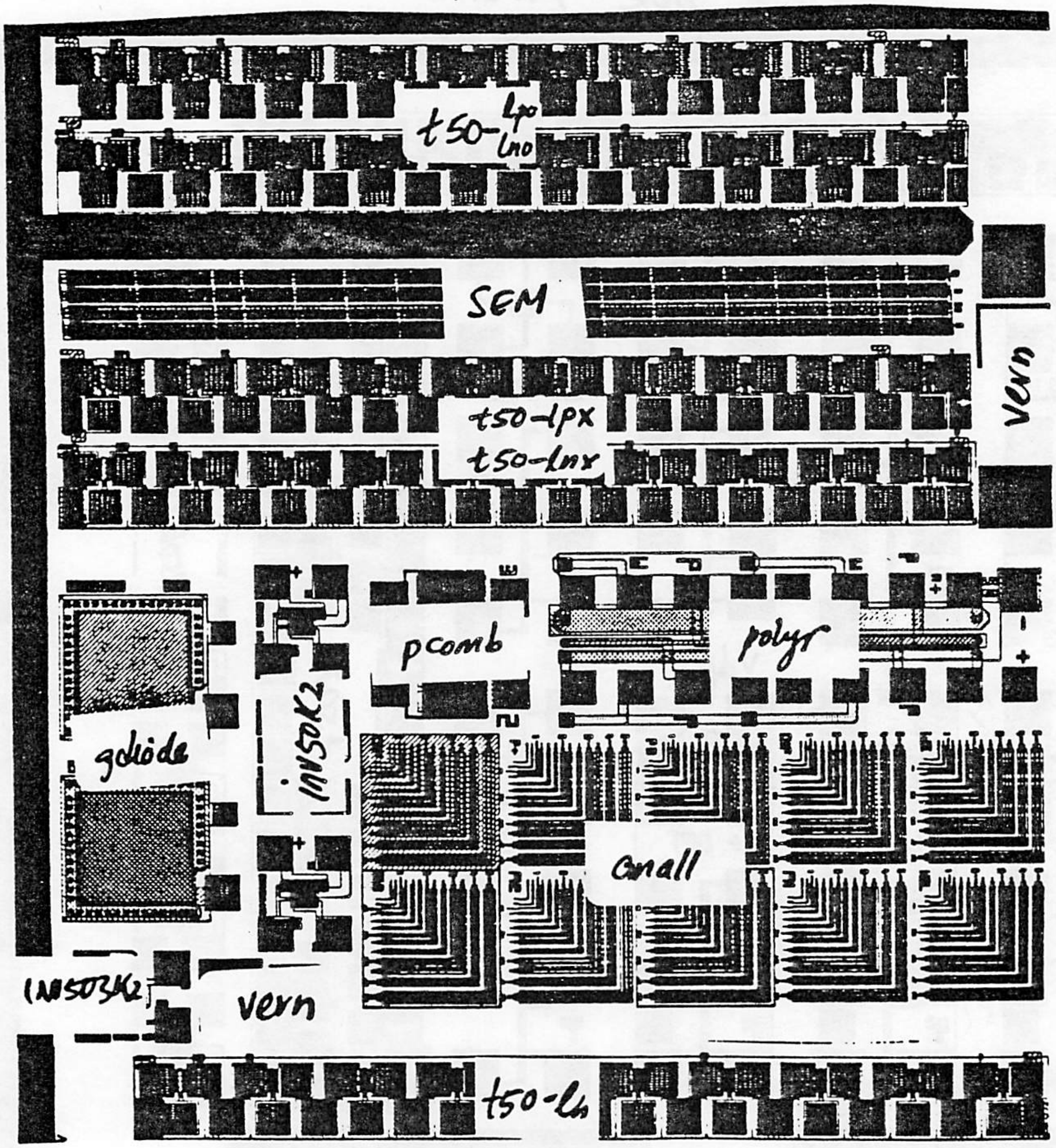
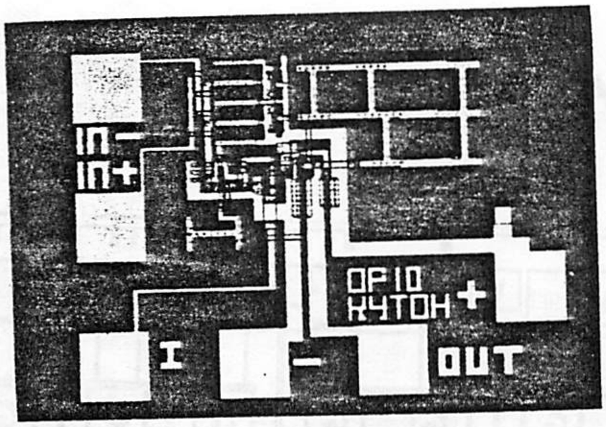


Figure 5. CVI Section
PMOS, NMOS Test Transistors, Gated Diodes, Inverters, Verniers, Angle Patterns, SEM Structures



Opamp
(3um Design Rules)

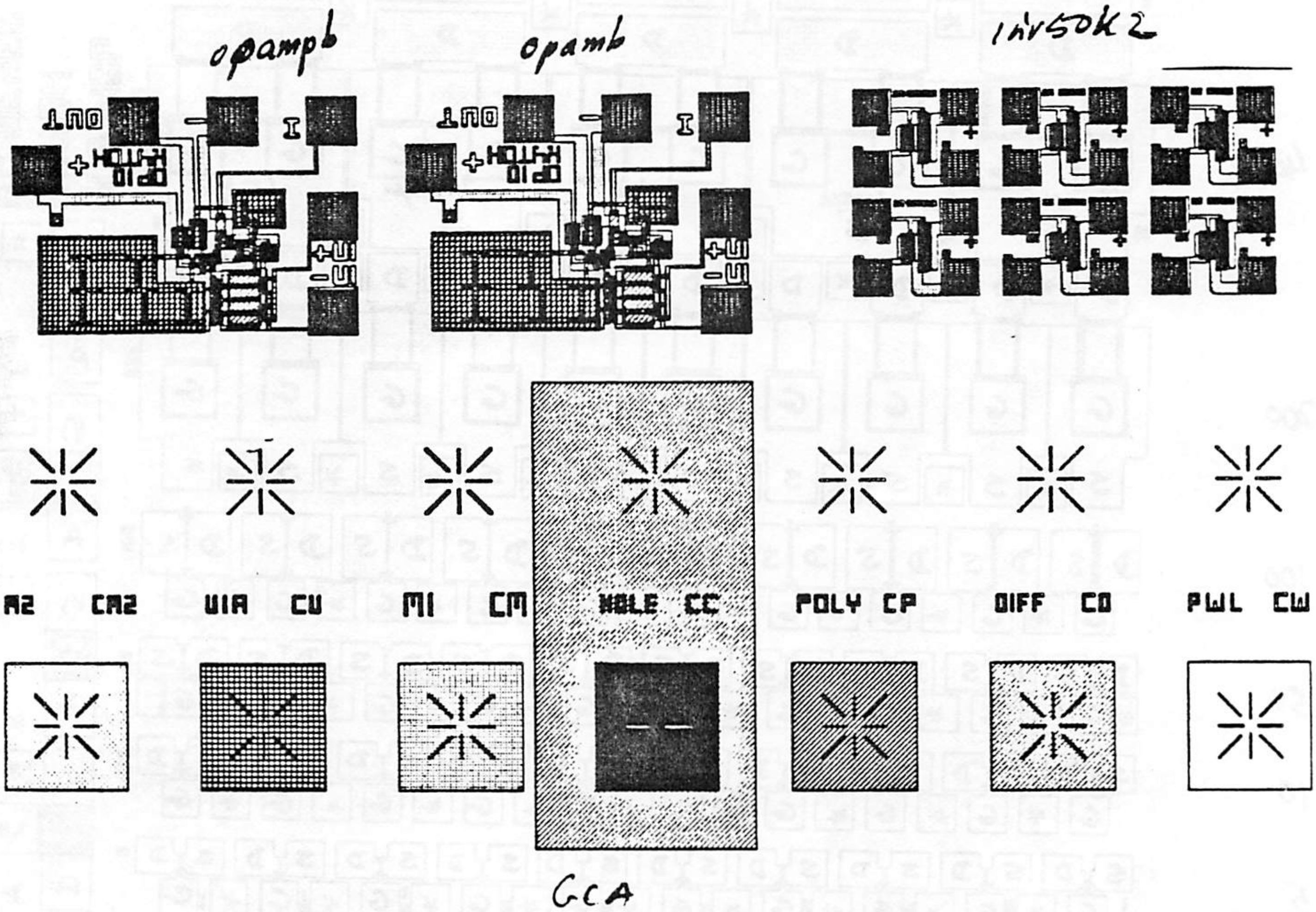


Figure 6. GCA Section
Opamps and Inverters
GCA Alignment Marks

CTN

NMOS DEVICES

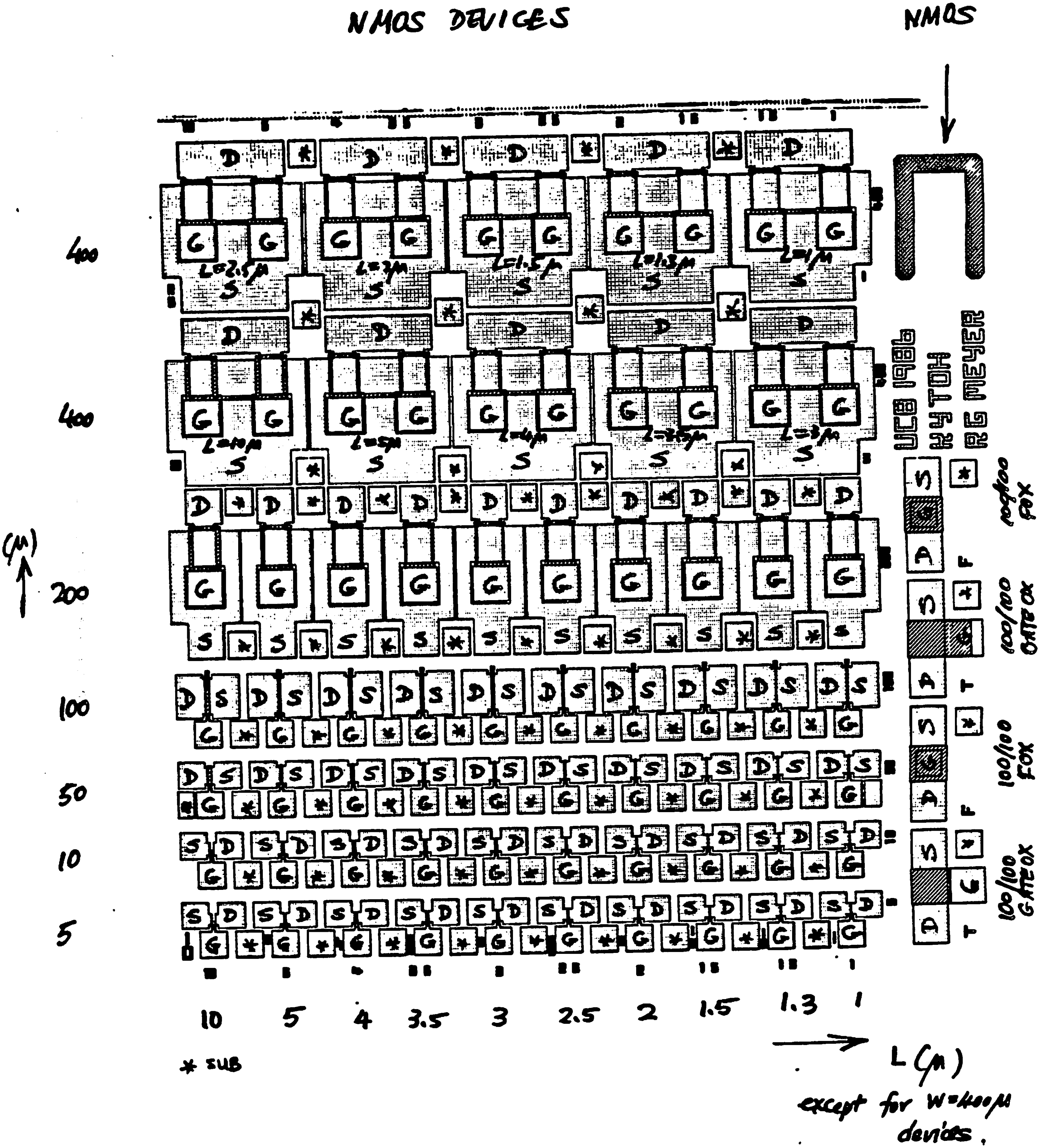
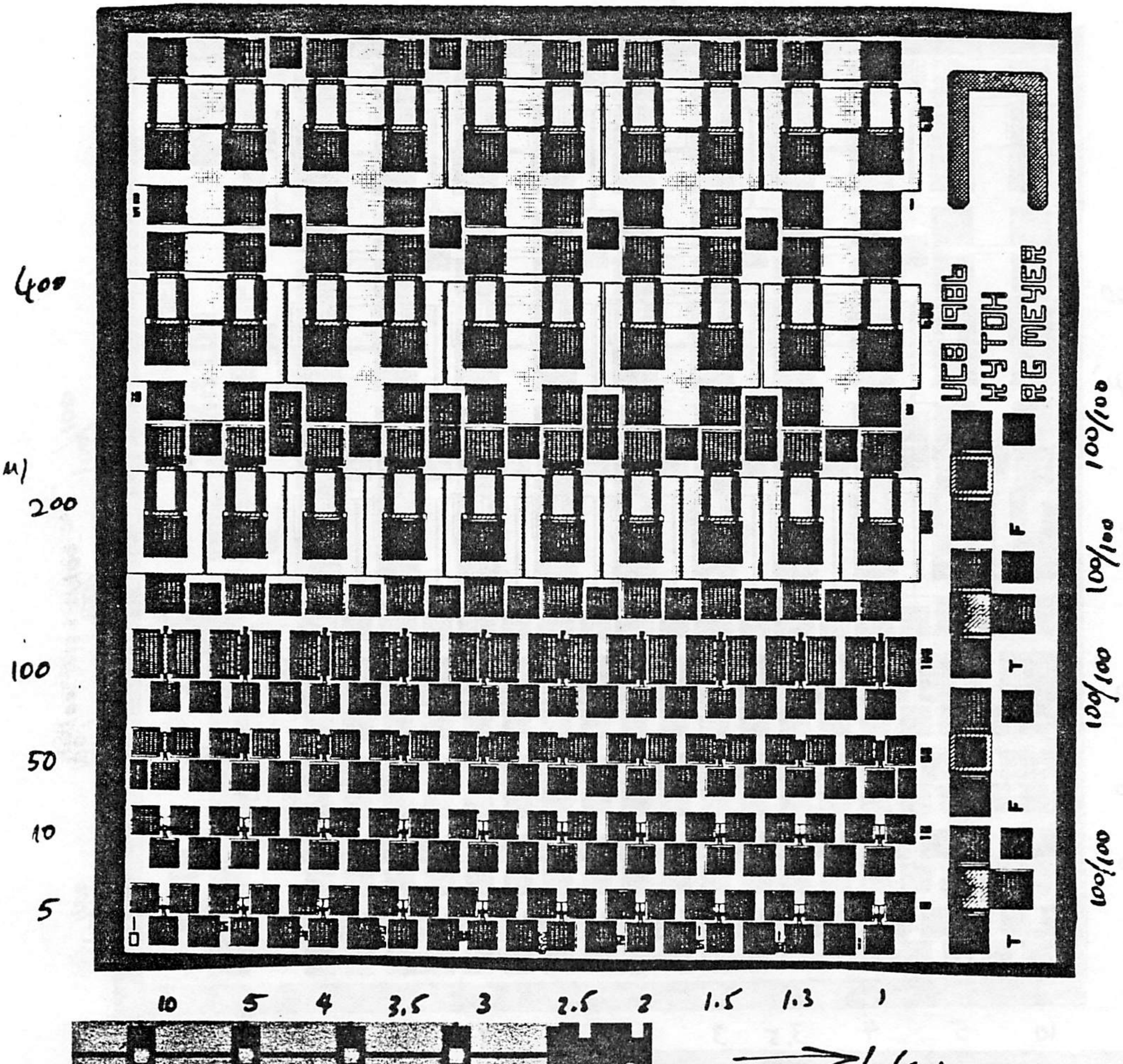


Figure 7. CTN Section
NMOS Devices

CTN

tnmos



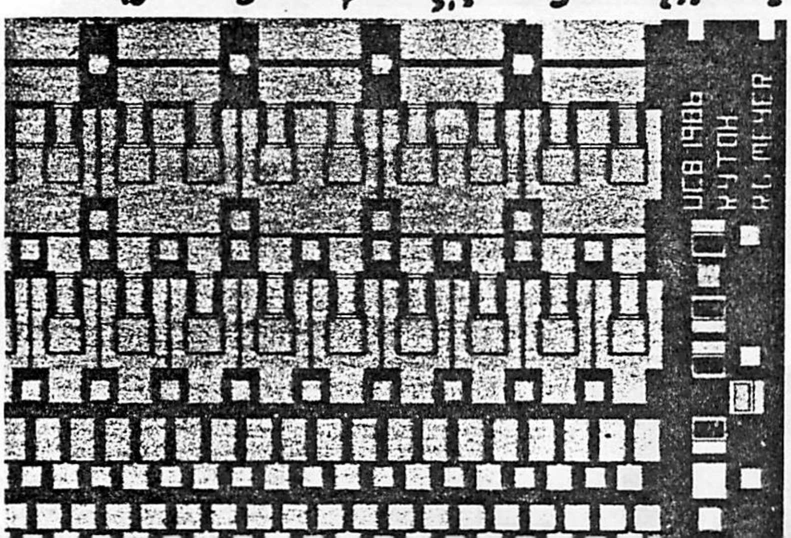
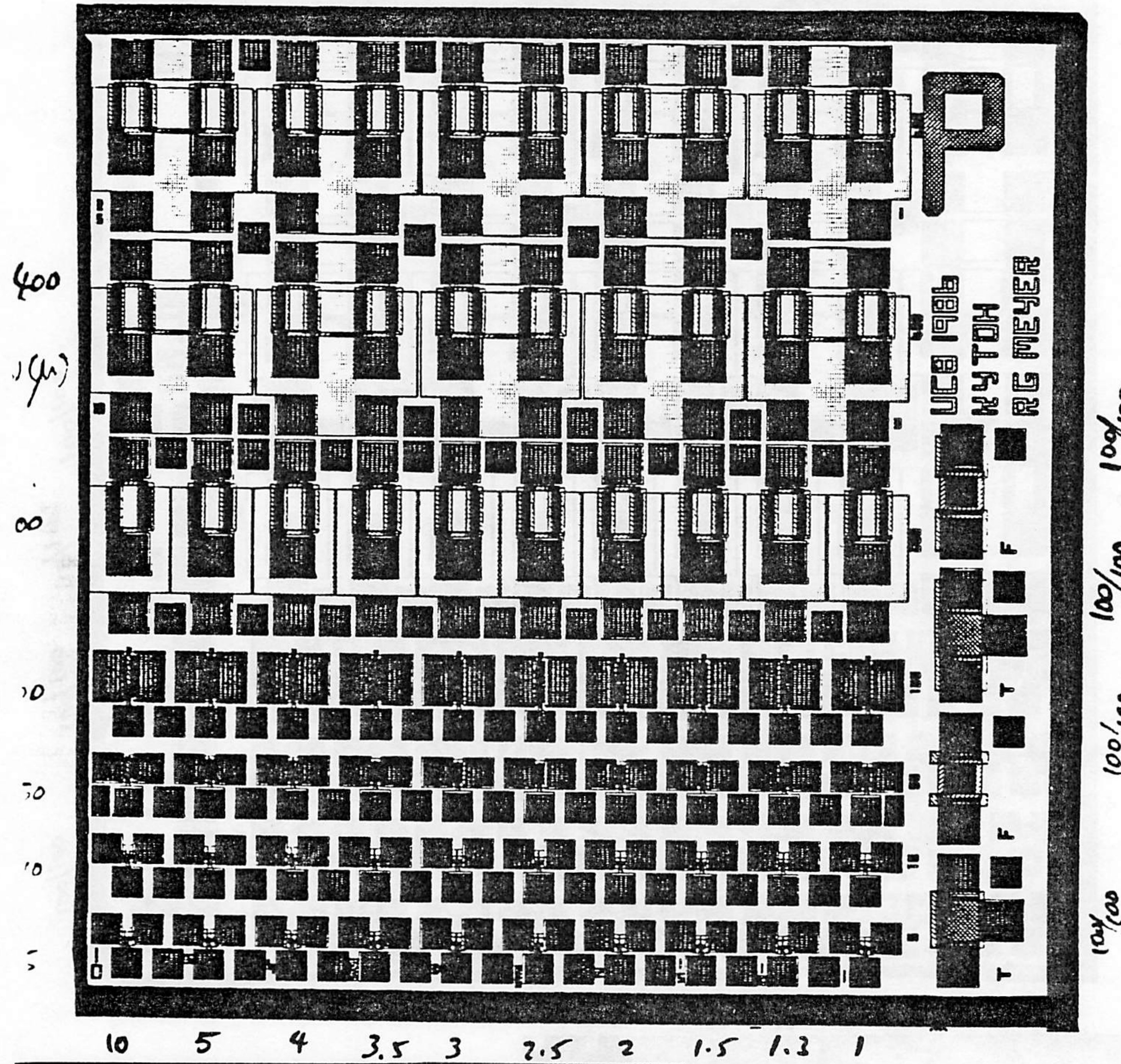


Figure 8. CTN Section
NMOS Devices

CTP — PMOS DEVICES

tpmos



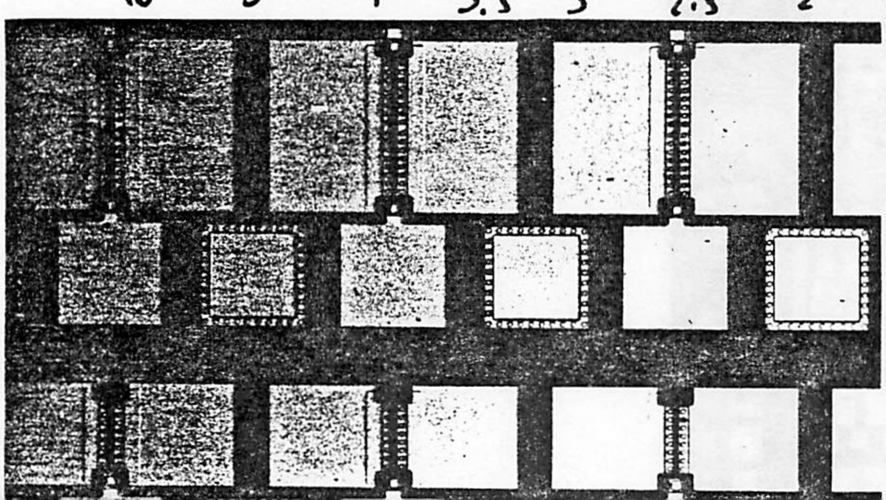


Figure 9. CTP Section
PMOS Devices

--- Test Transistors and Substrate Contacts; W = 100 um and 50 um

Appendix III

P-Well Test Pattern Device Description

KIC FILE:	anali		
CONSISTS OF:	angle patterns for visual inspection, 1u to 5u		
DESCRIPTIONS:	kic name	label	layer
	ancw	WE	wel
	ancd	DIFF	active
	ancp	PO	poly1
	ancs	P+	p+ select
	ance	CAP	poly2
	ancc	HOL	contact hole
	ancm	M1	metal1
	ancv	VIA	via
	ancm2	M2	metal2
	ancg	GLA	glass
LAYOUT:	see cifplot, CVI		

KIC FILE: CCH
CONSISTS OF: Contact chains for M1/Poly, and M1/M2; Capacitors; Via holes Invertes and test transistors
DESCRIPTIONS:
1. tmos-lpo: see description for itself
2. capbn: n+/pwell capacitor, 300ux300u
3. capbp: p+/substrate capacitor, 300ux300u
4. capbw: pwell/substrate capacitor, 300ux300u
5. capsn: n+/pwell capacitor, 15 strips of 300ux10u
6. capwp: p+/substrate capacitor, 15 strips of 300ux10u
7. capsw: pwell/substrate capacitor, 15 strips of 300ux10u
8. coxn: nmos gate capacitor, 300ux300u
9. coxp: pmos gate capacitor, 300ux300u
10.cp1p2: poly capacitor, 290ux290u
11.cfop: poly1/fox/substrate capacitor, 300ux300u
12.cm1p1: metal1 to ploy1 capacitor,, 290ux290u
13.cm1sub:metal1 to substrate capacitor, 290ux290u
14.cfon: poly1/fox/pwell capacitor, 300ux300u
15.cm2p1: metal2 to poly1 capacitor, 290ux290u
16.cm1m2: metal1 to metal2 capacitor, 290ux290u
17. inv50k2: see description of itself
18.tvial: minimum metal1 to metal2 test chain, 100ux100u
19.m1vm2: metal1 to metal2 test chain, based on different design rules and via sizes
20.pm1vm2:same as m1vm2 except that there is a poly pad underneath the metal1
21:thole: via hole pattern, from 1u to 50u
22.tholep:same as thole, except that there is a poly pad underneath thef metal1
23.tvia: metal1 to metal2 conatct chain, with different hole sizes:3.5u 3u 2.5u 2u
24.ccp: poly1 to metal1 contact chain
25.ccn+: soucre/drain to metal1 contact chain
26.ccp+: source/drain to metal1 contact chain
27.ccw: pwell to metal1 contact chain
28.t50-lp:see description of itself
29.t50-ln:see description oc itself

LAYOUT: Refer to cifplot, CCH

KIC FILE: CCR
CONSISTS OF: Contact Resistance test paaterns
DESCRIPTIONS:
1. conrm: metal1 to metal2
2. conrp+: metal1 to p+ source/drain
3. conrwn+: metal1 to n+ source/drain
4. conrp: metal1 to poly1

LAYOUT: see cifplot, CCR

KIC FILE: CME
CONSISTS OF: Van Der Pauw structures, test transistors and SEM structures
DESCRIPTIONS:
1. t50-lno: see description of itself
2. t50x: combination of t50-ln and t50-lp plus source connected to substrate via metal1.
3. vern: See description of itself
4. inv50k2: See descriptionso of itself
5. vdp: consists of one van der pauw square structure and a split resistive line for delta width measurements, one for each of the following layers:
   i. p+ poly: poly1 with p+ implant
   ii. M1: metal1
   iii.cap poly:poly2

iv. pwell: pwel·
v. n+diff: n+ source/drain
vi. p+diff: p+ source/drain
vii.n+ poly: poly1 with n+ implant
6. sem: see description of itself

LAYOUT: see cifplot, CME

KIC FILE: CVI
CONSISTS OF: inn503k2, inv50k2, gdiode, t50-in, polyr, vern, anall,sem
DESCRIPTIONS: see desription of individual subcells
LAYOUT: see cifplot, CVI

KIC FILE: gdiode
CONSISTS OF: gated diodes in pwell and n substrate
DESCRIPTIONS: gated diode, 250ux250u
LAYOUT: see cifplot, CVI

KIC FILE: GCA
COSISTS OF: GCA wafer stepper alignment keys
DESCRIPTIONS:

key	GCA alignment locations positive	negative
CW	-2.6 -1.6	-2.6 -2.1
CD	-2.2 -1.6	-2.2 -2.1
CP	-1.8 -1.6	-1.8 -2.1
CC	-1.4 -1.6	-1.4 -2.1
CM	-1.0 -1.6	-1.0 -2.1
CV	-0.6 -1.6	-0.6 -2.1
CM2	-0.2 -1.6	-0.2 -2.1

LAYOUT See cifplot, GCA

KIC FILE: inv50k2
CONSISTS OF: 3 inverters
DESCRIPTIONS: inv503k2: channel length= 3u, K=2
inv502k2: channel length= 2u, K=2
inv5015k2:channel length= 1.5u, K=2
LAYOUT: See cifplot GCA, CVI, CME, CCH;
+ for VDD, - for GND, O for OUTPUT, IN for INPUT

KIC FILE: latch
CONSISTS OF: simple latch-up test patterns
DESCRIPTIONS: Consult Hans Zapple
latcha is based on 3u design rules
latchb is based on 2u design rules
LAYOUT: See cifplot, latch

KIC FILE: MT4A
CONSISTS OF: Microlinear Test Patterns
DESCRIPTIONS: Refer to MicroLinear Test Patterns Documentation
LAYOUT: Refer to cifplot, MT4A

KIC FILE: opampb
CONSISTS OF: a simple op amp
DESCRIPTION: a simple op amp based on 3u design rules
LAYOUT: see cifplot, GCA

KIC FILE: pcomb
COSISTS OF: Test pattern for poly etch
DESCRIPTION: interlaced fingers with 3u and 2u design rules
LAYOUT: see cifplot, CVI

KIC FILE: polyr
CONSISTS OF: resistor of large width
DESCRIPTIONS: well,poly1,n+ source/drain,p+ source/drain
LAYOUT: see cifplot, CVI

KIC FILE: sem
CONSISTS OF: very long devices for sem cross section view
DESCRIPTIONS: channel length: 3u 2.5u 2u 1.5u,
contact holes: all 3u squares, staggered
LAYOUT: See cifplot,CVI

KIC FILE: tnmos or CTN
CONSISTS OF: nmos test transistors
Descriptions: channel length: 10u 5u 4u 3.5u 3u 2.5u 2u 1.5u 1.3u 1u
device width: 5u 10u 50u 100u 200u 400u
device T thin gate device: 100u/100u
device F field ox device : 100u/100u
Two each of T and F, one set has large contact hole openings for checking contact hole etch.
LAYOUT: See attached cifplot CTN.
note lower case letter n on upper right corner.

KIC FILE: tpmos or CTP
CONSISTS OF: pmos test transistors
Descriptions: channel length: 10u 5u 4u 3.5u 3u 2.5u 2u 1.5u 1.3u 1u
device width: 5u 10u 50u 100u 200u 400u
device T thin gate device: 100u/100u
device F field ox device : 100u/100u
Two each of T and F, one set has large contact hole openings for checking contact hole etch.
LAYOUT: Identical to tnmos. Note upper case letter P on upper right corner. See cifplot CTF.

KIC FILE: t50-lno
CONSISTS OF: nmos test transistors
DESCRIPTIONS: channel length: 10u 5u 4u 3.5u 3u 2.5u 2u 1.5u 1.3u 1u
device width: 50u
Devices has large contact hole opeings.
LAYOUT: See cifplot CVI, CME, CCH , note label "n".

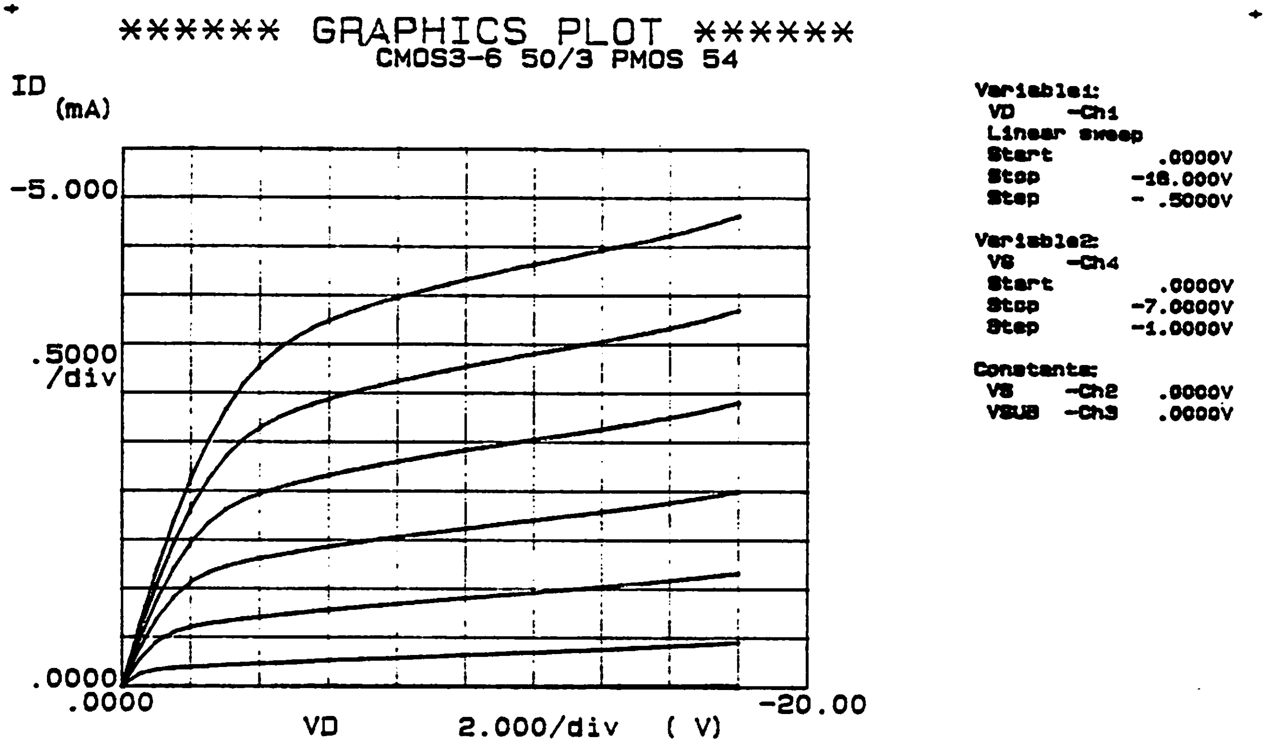
KIC FILE: t50-lnx
CONSISTS OF: nmos test transistors
DESCRIPTIONS: channel length: 10u 5u 4u 3.5u 3u 2.5u 2u 1.5u 1.3u 1u
device width: 50u
Source tied to substrate via metal 1
LAYOUT: See cifplot CVI, note label "n".

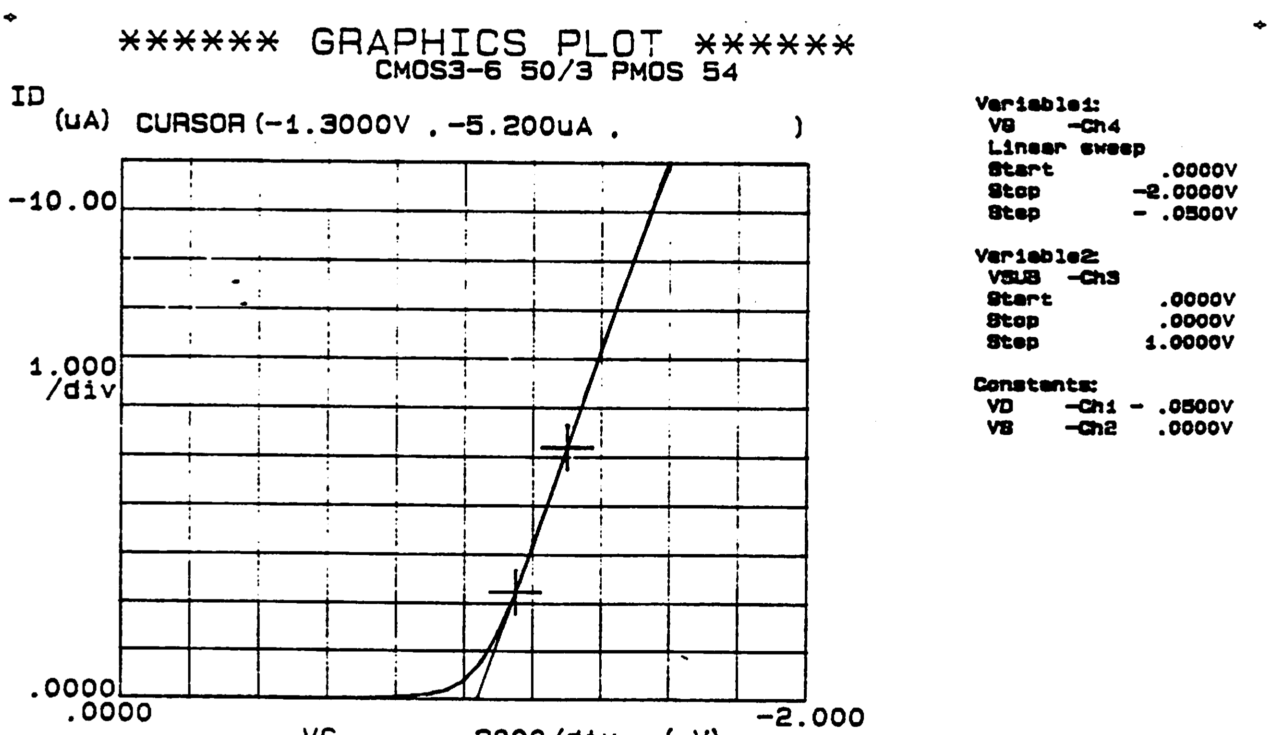
KIC FILE: t50-lpo
CONSISTS OF: pmos test transistors
DESCRIPTIONS: channel length: 10u 5u 4u 3.5u 3u 2.5u 2u 1.5u 1.3u 1u
device width: 50u
Devices has large contact hole opeings.
LAYOUT: See cifplot, note label "P".

KIC FILE: t50-lpx
CONSISTS OF: pmos test transistors
DESCRIPTIONS: channel length: 10u 5u 4u 3.5u 3u 2.5u 2u 1.5u 1.3u 1u
device width: 50u
Source tied to substrate via metal 1.
LAYOUT: See cifplot CVI, note label "P".

KIC FILE: t50x
CONSISTS OF: test transistor with source tied to substrate
DESCRIPTIONS: combination of t50-ln and t50-lp, except that source is tied to substrate via metal1
LAYOUT: see cifplot CVI

KIC FILE: vern
CONSISTS OF: alignment verners, horizontal and vertical
DESCRIPTIONS: alignment error is 0.2u X number of bars from the aligned bar away from center bar
i.e. center of bar should be aligned ideally
LAYOUT: See cifplot



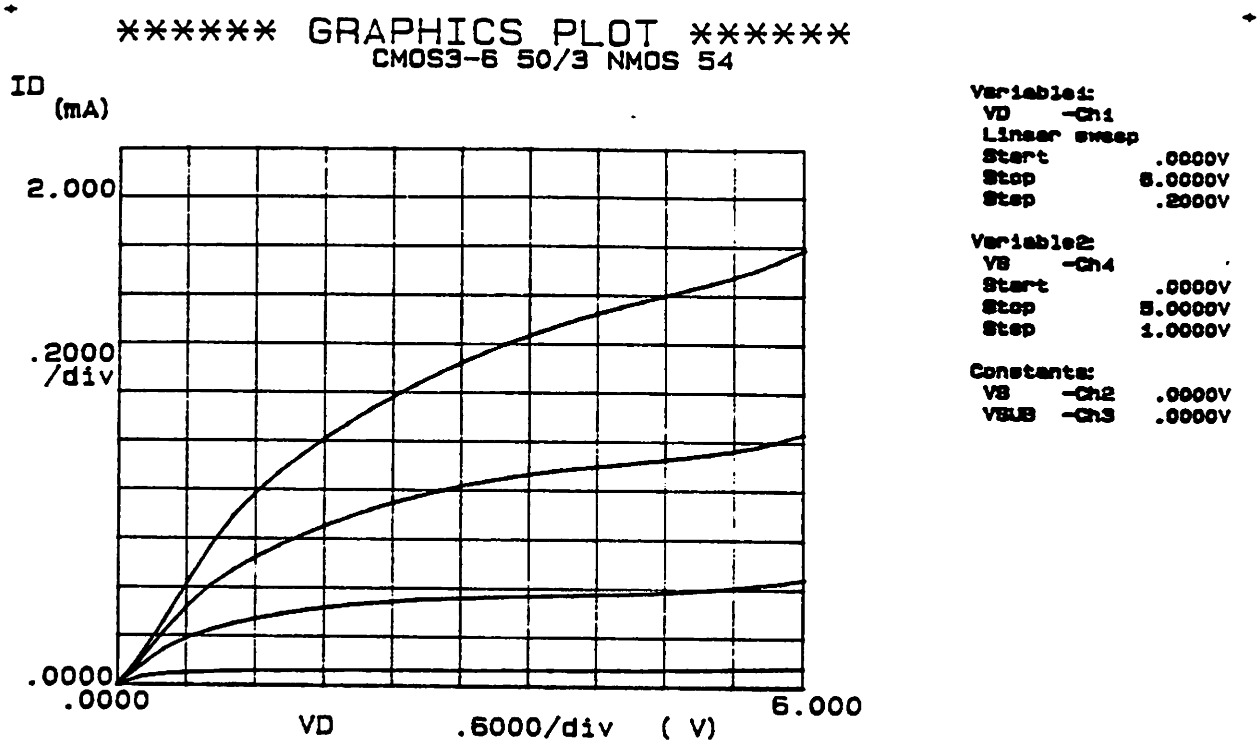


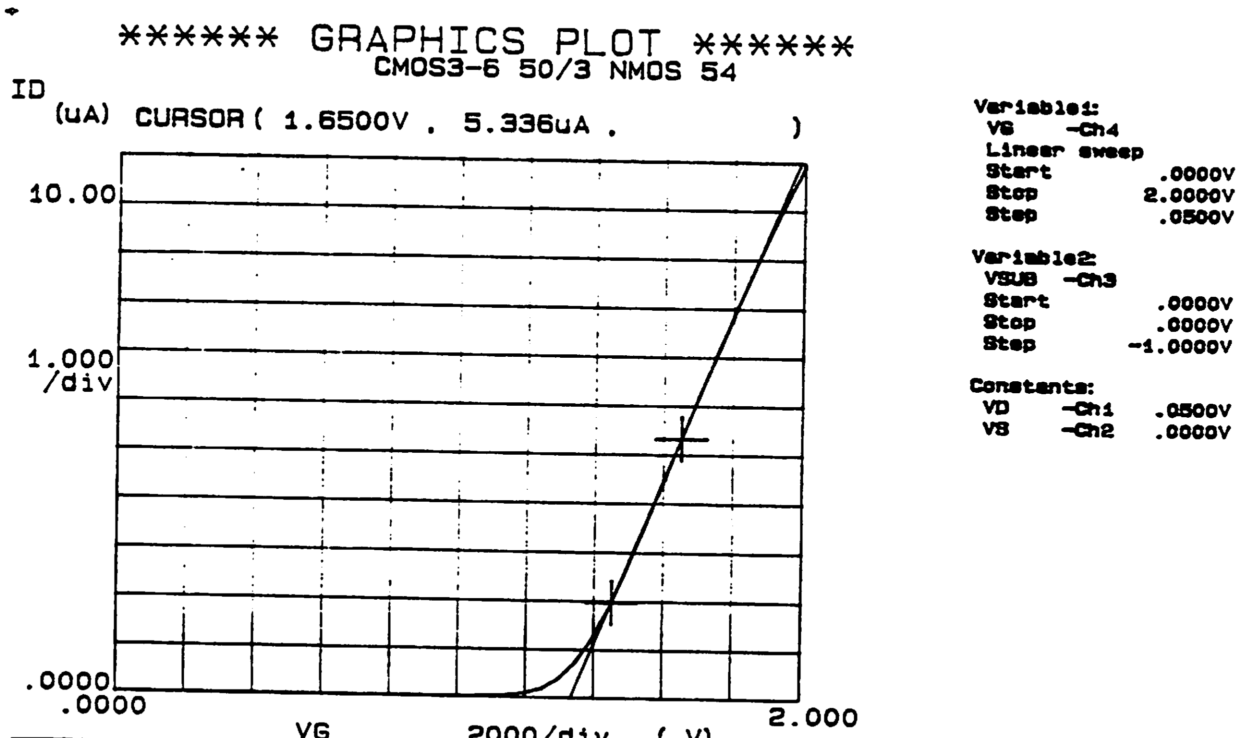
	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	19.8E-06	50.6E+03	-1.04E+00	20.5E-06
LINE2				

ISUB (A) = ABS (ISU)

Figure 10. PMOS Device, L=3 um

V_t= -1.04 V

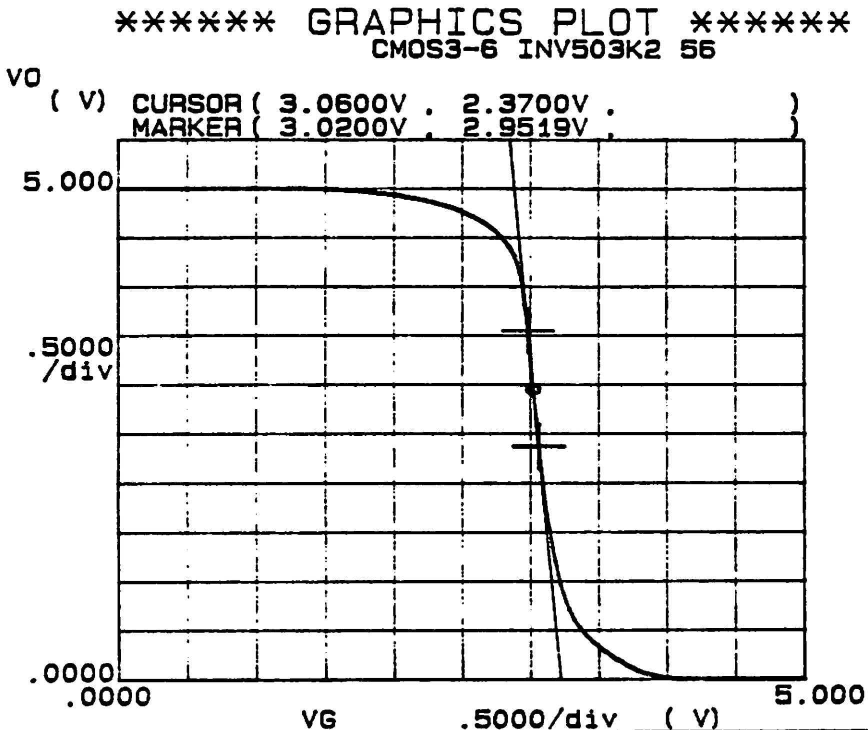




	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	16.8E-06	59.7E+03	1.33E+00	-22.3E-06
LINE2				

ISUB (A) = ABS(ISU)

Figure 11. NMOS Device, L = 3 um
V_t = 1.33 V



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-14.7E+00	-67.8E-03	3.22E+00	47.5E+00
LINE2				

Variable1:
VG -Ch4
Linear sweep
Start .0000V
Stop 5.0000V
Step .0200V

Constants:
VD -Ch1 5.0000V
IO -Ch2 .000 A
VSUB -Ch3 .0000V

Figure 12. Voltage Transfer Characteristics of Inverter 503K2 (CME Section)

Appendix IV

P-Well CMOS Process
Double Metal

Microlab CMOS Process

Version 3.2 (Jan. 14, 1987)
2 μm, P-well, single poly-Si, double metal

0.0 Starting Wafers: 8-12 ohm-cm, n-type, <100>
Control Wafers: PWELL (n-type), PCH (n-type)
Measure bulk resistivity (ohm-cm) of PWELL on Sonogage.

1.0 Initial Oxidation: target = 1000Å

1.1 TCA clean furnace tube.

1.2 Standard clean wafers, include PWELL control:
piranha clean for 10 min, 10/1 HF dip, spin-dry.

1.3 Wet oxidation at 1000°C:
5 min dry O_2
11 min wet O_2
5 min dry O_2
20 min dry N_2
Measured t_{ox}= on PWELL cont.

2.0 N- (Punch-Through) Implant:
Blanket implant of phosphorous at 145 keV, $1.2x10^{12}/cm^2$
Include PWELL control.

3.0 Well Photo Mask: SHIN-PWELL-CW (chrome-df)
Control wafers are not included in the photoresist steps.

3.1 Standard clean wafers.
Dehydrate in furnace for 5 minutesat 750°C.

3.2 Spin resist on Eaton: Kodak 820, 4600 RPM, 25 seconds,
soft bake at 120°C, 45 seconds

3.3 Expose: GCA 6200-10X wafer stepper

3.4 Develop in MTI-Omnichuck: Kodak 932/H2O=1:1, 60 seconds

3.5 Descum in Technics-c: O_2 plasma, 50 W, 1 minute

3.6 Hard bake in oven: 120°C, 20 minutes in air.

4.0 Well Implant: Boron (B11), $3x10^{12}/cm^2$, 80 KeV
(Resist is left on wafers.) Include PWELL control (no resist).

5.0 Well Drive-In: target x_j = 4 μm, t_{ox} = 3000Å

5.1 TCA clean furnace tube.

5.2 Etch pattern into oxide in 5/1 BHF.

5.3 Remove resist and piranha clean wafers.

5.4 Standard clean wafers, include PWELL control.

5.5 Dry oxidation and well drive at 1150°C:
4 hrs dry O_2
5 hrs dry N_2
Measure oxide thickness on work wafer: in well and outside

6.0 Locos Pad Oxidation/Nitride Deposition:
target = 200Å SiO_2 + 1000Å Si_3N_4

6.1 TCA clean furnace tube.

6.2 Remove all oxide in 5/1 BHF until wafers dewet (inc. PWELL).
Measure Rs (ohm/sq) of PWELL control on Prometrix.

6.3 Standard clean wafers.

6.4 Dry oxidation at 950°C:
28 min dry O_2
20 min dry N_2 anneal.
a) Measured t_{ox}= on PWELL control
b) Strip oxide off of PWELL control in BHF.

6.5 Deposit 1000Å of Si-nitride immediately:
Dep.time = 22 minutes, temp.= 800°C.
a) Include PWELL control. Measured t_{nit}=
b) Save PWELL control for Step 12.0

7.0 Active Area Photo Mask: SHIN-ACTIVE-CD (emulsion-cf)
Spin, expose, develop, descum, hard bake.

8.0 Nitride Etch: Technics-c plasma etcher
Do not etch oxide, do not remove resist.

9.0 Field (P-) Implant

9.1 Photo Mask: SHIN-PWELL-CW (chrome-df)
Spin, expose, develop, descum, hard bake.(Double photo)
Field inside well is open, active areas are covered
with Si_3N_4 and pr.

9.2 Measure resist thickness on active area with profilometer.
Wafers cannot be passed unless pr is 0.8 μm thick .

9.3 Field (P-) Ion Implantation: boron (B11), 100 KeV, $1x10^{13}/cm^2$

9.4 Remove resist and piranha clean wafers.

10.0 Field (N-) Implant

10.1 Standard clean and bake wfrs for 5 min at 750°C in N_2.

10.2 Photo mask: SHIN-PWELL mask (emulsion-cf)
Spin, expose, develop, descum, hard bake.
Well area is covered with pr, active areas with Si_3N_4.

10.3 Phosphorus implant, 40 KeV, $5x10^{12}/cm^2$.

10.4 Remove resist and piranha clean wafers.

11.0 Locos Oxidation: target = 6500Å

11.1 TCA clean furnace tube.

11.2 Standard clean wafers; dip until field area dewets.

11.3 Wet oxidation at 950°C:
5 min dry O_2
4 hrs 40 min wet O_2
5 min dry O_2
20 min N_2 anneal
Measured t_{ox}= on a device wafer in the field area

12.0 Nitride Removal (include PWELL cont.)

12.1 Oxide dip in 10/1 HF for 1 minute

12.2 Etch nitride off in hot phosphoric acid: 145°C, 30 minutes

13.0 Sacrificial Oxide: target = 200Å

13.1 TCA clean furnace tube.

13.2 Standard clean wafers. Include PWELL control.

13.3 Dry oxidation at 950°C:
28 min dry O_2
20 min N_2 anneal
a) Measured t_{ox}= on PWELL control
b) Do not include PWELL control in Step 14.

14.0 Threshold Implant:
Blanket implant boron (B11) at 30 KeV, $3x10^{11}/cm^2$ & $5x10^{11}/cm^2$.

15.0 Gate Oxidation/Poly-Si Deposition:
target = 500Å SiO_2 + 4500Å poly-Si

15.1 TCA clean furnace tube; reserve poly-Si deposition tube.

15.2 Standard clean wafers,include PWELL and PCH controls.

15.3 Dip off sacrificial oxide (dewet) in 10/1 HF (approx. 1 min).

15.4 Dry oxidation at 950°C:
2 hr. 10 minutes dry O_2
20 min N_2 anneal.
t_{ox}(PWELL)= t_{ox}(PCH)=

15.5 Immediately after oxidation deposit 4500Å
of phos.doped poly-Si.
time = 2 hr. 15 minutes, temp.= 650°C

Do not include PWELL, PCH controls; include a new control with 1000Å thermal SiO_2 on it. t_{poly}=

16.0 Gate Definition Mask: SHIN-POLY-CP (emulsion-cf)

16.1 Spin, expose, develop, descum, hard bake.

16.2 Plasma etch poly-Si in LAM etcher (CCl4). Inspect.

16.3 Remove resist, piranha clean wafers.

17.0 Reoxidation: target=800Å on poly-Si, 500Å on S/D

17.1 TCA clean furnace tube.

17.2 Standard clean wafers, include both controls, PWELL, PCH.
From here on: only 10 sec dip in 25/1=H2O/HF after piranha.
NOT MORE!

17.3 Dry oxidation at 950°C:
30 min dry O_2
10 min N_2 anneal.
t_{ox}(PWELL) = t_{ox}(PCH) =

18.0 N-Channel Source/Drain Photo Mask: SHIN-NII-CS (emulsion-cf)
Spin, expose, develop, descum, hard bake.

19.0 N+ Source/Drain Implant

19.1 Implant arsenic at 100 KeV, $5x10^{15}/cm^2$, incl. PWELL cont.

19.2 Remove resist and piranha clean wafers (no dip here).

20.0 N+ S/D Anneal

20.1 TCA clean furnace tube.

20.2 Standard clean wafers, include PWELL control (10 sec dip).

20.3 Anneal wafers in N_2 at 925°C for 1hr 15minutes

20.4 Strip PWELL control and measure Rs (ohm/sq) on Prometrix.
Save PWELL control in "completed controls" box.

21.0 P-Channel Source/Drain Photo Mask: SHIN-PII (chrome-df)
Spin, expose, develop, descum, hard bake.

22.0 P+ S/D Implant

22.1 Implant B11 at 50 KeV, $2x10^{15}/cm^2$, include PCH control.

22.2 Remove resist and standard clean wafers (no dip).

23.0 P+ S/D Anneal

23.1 TCA clean furnace tube.

23.2 Standard clean wafers, include PCH control.

23.3 Anneal at 900°C in N_2 for 15 min, incl. PCH control.

23.4 Measure Rs (ohm/sq) of PCH control on Prometrix.
Save PCH control in "completed controls" box.

23.5 Measure oxide thickness in S/D area.

24.0 **Reflow Glass:** target = 7000Å

24.1 Standard clean wafers (10 sec dip).
Include only one new, PSG control.

24.2 Deposit PSG : incl.PSG control
Layers: 1000Å undoped LTO (~ 5 minutes)
6000Å PSG (PH3 flow at 10.3) (~ 30 minutes)
time = (approx) 35 minutes total (check current dep rates)
temp. = 450°C
t_{PSG}= on PSG cont.

24.3 Densify glass in tube 2 at 950°C:
include one PSG control.
5 min dry O_2, 30 min wet O_2, 5 min dry O_2

24.4 Do wet oxidation dummy run afterwards to clean tube:
1 hr wet oxidation at 950°C.

25.0 **Contact Photo Mask:** SHIN-CONTACT-CC (chrome-df)
Spin, expose, hand develop, descum, hard bake.

26.0 **Contact Etch**

26.1 Plasma etch in Technics-c in CHF3/O_2
Do etch - bake - etch sequence as follows:
a) Wet etch in 10:1 BHF until 5K-6K oxide is left.
b) Bake wafer for 2 minutes at 120°C on hot plate.
c) Plasma etch at 100 watts, pressure ~ 150 mTorr,
CHF3=7.0 sccm, O_2=2.0 sccm,
until approximately 600-800Å of SiO_2 remains.
d) Wet etch in 10:1 BHF until clear.
e) Spin dry and inspect thoroughly.

27.0 **Back Side Etch**

27.1 Spin photoresist (front side), do not expose; hard bake.

27.2 Spin photoresist again, and hard bake.

27.3 Etch back side of wafers as follows:
a) Etch off PSG in BHF.
b) Wet etch poly-Si (gate poly-Si thickness).
e) Final dip in BHF until back dewets.

27.4 Remove resist in O_2 plasma: 5-7 minutes at 300 watts. and piranha clean wafers (no dip after first piranha).

27.4 Do a 20 second 25/1 HF dip just before metallization.

28.0 **First Metallization:** target = 6000Å
Sputter Al/2% Si on all wafers.

29.0 **First Metal Photo Mask:** SHIN-METAL1-CM1 (emulsion-cf)

29.1 Spin Hunt WX-235 resist, expose, develop, descum; no hard bake.

29.2 Wet etch Al. (Wet wafers first in DI water.)

29.3 Remove resist with acetone (no piranha!) t_{Al}=

29.4 Rinse wafers in DI water for 20 minutes, dry.

29.5 Probe test devices.

30.0 **Inter-Metal Dielectric**

30.1 Spin on SiO_2 glass: Futurex IC1-200, 3000 RPM, 20 seconds

---

30.2 Bake SOG: 120°C for 30 min + 200°C for 30 min in air.

30.3Ånneal SOG: 400°C for 30 min in N_2 (Tylan 14).

30.4 Deposit 8000Å of undoped SiO_2 by PECVD (Technics-b).

31.0 **Via Photo Mask:** SHIN-VIA-CV (chrome-df)

31.1 Spin resist, expose, develop, descum, hard bake.

31.2 Etch glass: wet etch ~ 6000Å in BHF, plasma etch rest.

31.3 Remove resist with acetone (no piranha!)

31.4 Rinse wafers in DI water for 20 minutes, dry.

31.5 Probe test devices.

32.0 **Second Metallization:** target = 8000Å

32.1 Dip in Al etch for 10 sec just before sputtering; rinse well.

32.2 Sputter 8000Å ofÅl/2% Si on all wafers.

33.0 **Second Metal Photomask:** SHIN-METAL2-CM2 (emulsion-cf)

33.1 Spin Hunt WX-235 resist, expose, develop, descum, no hard bake.

33.2 Wet etch Al. (Wet wafers first in DI water.)

33.3 Remove resist in acetone (no piranha!) t_{Al}=

33.4 Rinse wafers in DI water for 20 minutes, spin dry.

33.5 Probe test devices.

34.0 **Sintering:** 400°C for 20 minutes in forming gas.

End of Process

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cifplot* Window: -2502.06 2502.06 -2504.12 2504.12 @ u=200 --- Scale: 1 micron is 0.00079 inches (20x

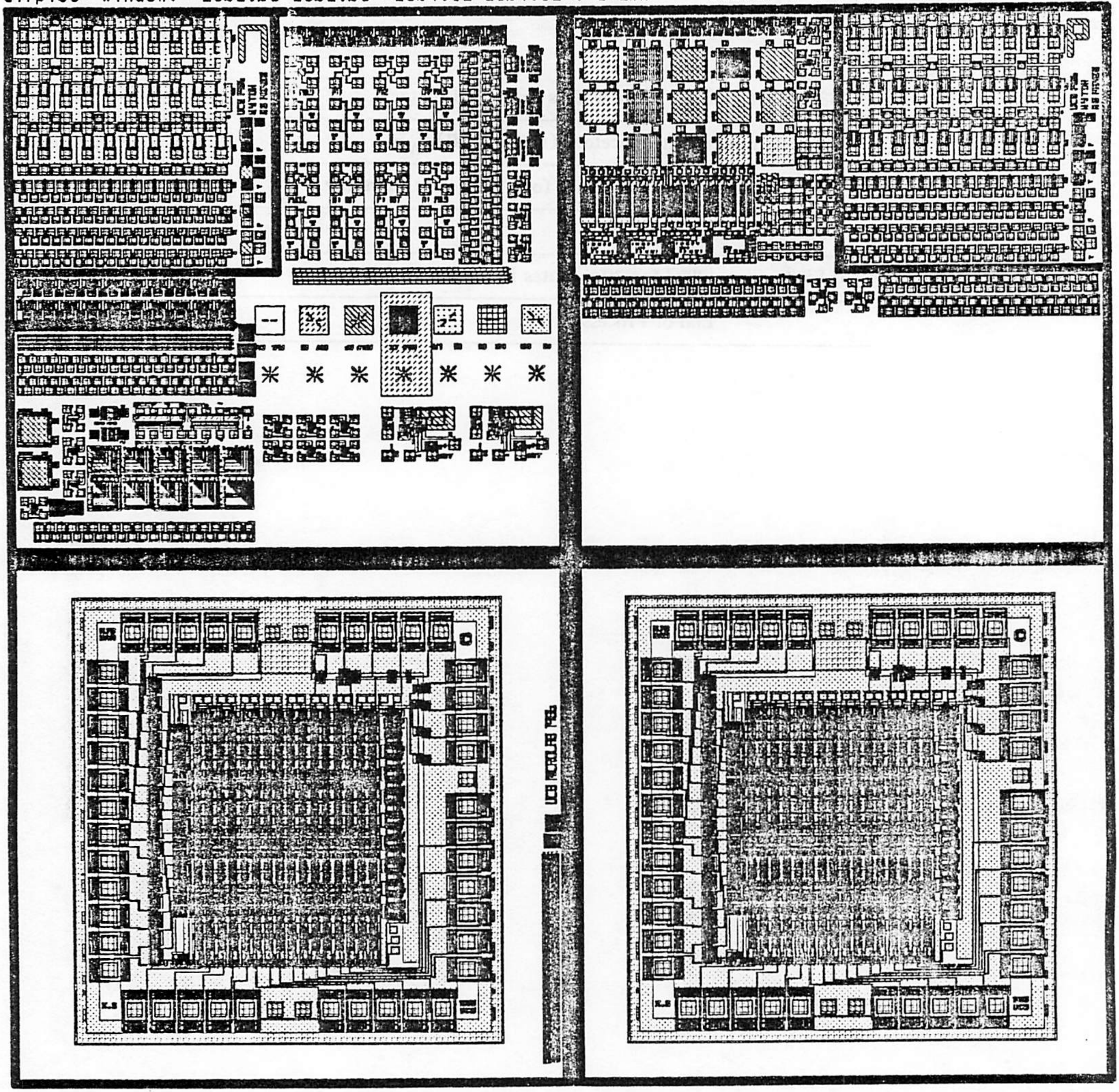

Figure 1. CMOS6 Composite Chip
Top row: Toh's test devices
Bottom row: students' circuit

Appendix V

Process Modules
Process Information Storage

Standard 100mm Berkeley VLSI Process Modules

Version 1.2
(November 18, 1986)

Table of Contents

[[MOD 1]] STANDARD WAFER CLEANING PROCEDURE (Piranha Clean) (K.Y. Toh)

[Purpose]: to remove organic residue and complex heavy metal ions.

[Equipment]: Sink 6, two temperature controlled baths in rear, rinse tanks

Note: This is the pre-furnace clean sink. If wafers have just had photoresist removed, they must be cleaned in Sink 8 first.

[Summary]:

(1) Add 100 ml of hydrogen peroxide to the 120°C sulfuric acid bath just before cleaning wafers. This mixture is called piranha and is sufficient to clean 2 carriers filled with wafers.

(2) Wet wafers by immersing the carrier in filled rinse tank #1 or 4.

(3) Immerse wafers in hot piranha for 10 minutes

(4) Standard rinse/spin.

[Detailed Procedure]:

(1) Check that the temperature controllers to the piranha baths in the rear of Sink 6 are turned on and that the temperature setting is 120°C. If not, turn on the heater by pressing the green TEMP CONT button. Temperature will be stabilized in about 30 minutes The bath contains concentrated sulfuric acid.

(2) Put the wafers in the white teflon wafer cassette marked #6.

(3) When the bath temperature has been stabilized at 120°C, and just prior to immersing the wafers into the bath, slowly add 100 ml of hydrogen peroxide to the bath. The piranha mixture should start bubbling immediately and should continue bubbling through the cleaning period.

(4) Wet wafers with DI by immersing them in the rinse tank. This prevents bubbles from sticking to the wafer surface.

(5) Immerse cassette with wafers in the hot piranha bath for 10 minutes

(6) Standard rinse/spin ([[MOD 2,3]]).

[[MOD 2]] STANDARD RINSE-SPIN PROCEDURE (J. Lee)

[Purpose]: to rinse to resistivity of 10 MΩ/square and spin dry

[Equipment]: Sink 6 and Fluorocarbon rinser/spinner

[Summary]:

(1) Rinse in the first (#1 or 4) DI-H_2O tank for at least 1 minute.

(2) Rinse in the second (#2 or 5) DI-H_2O tank for at least 1 minute.

(3) Rinse in the final (#3 or 6) DI-H_2O tank to at least 10 MΩ/square. Be sure the button for the appropriate resistivity monitor is lit.

(4) Spin dry for 2.5 min. 2400 RPM.

[Detailed Procedure]:

(1) Press RINSE START button, light will come on.

(2) Press TANK FILL button for each tank (lights on). Make sure that TANK DRAIN button lights are off.

(3) Wait until DI-H_2O rinse tanks are filled. Once filled, push the TANK FILL buttons to turn them off. Turn them on only when the carrier is in the tank so as to conserve DI water.

(4) Remove wafers from the cleaning or dipping solution.

(5) Place carriers into the first DI-H_2O rinse tank (tank #1 or 4) for 1 minute. Make sure that DI-H_2O overflows during rinsing.

(6) Place wafers into the second DI-H_2O rinse tank (tank #2 or 5) for 1 minute.

(7) Dip wafers into the final DI-H_2O rinse tank (tank #3 or 6) until the resistivity meter reads at least 10 MΩ/square.

(8) Wearing new plastic gloves, load the carrier into the Fluorocarbon rinser/spinner, H-bar facing out. Make sure the bar on the spinner while serves to hold the wafers in the carrier is at the top.

(9) Make sure that the following settings are used:

DRY TIME = 2.5 min
SPIN SPEED = 2400 RPM
DRY ONLY light is on

(10) Push START button to start the spin cycle. Check spin speed during cycle. When the STOP button light is lit, remove carrier from the spinner. Make sure that the shoulders of the spinner are in the down position before removing carrier to avoid spilling wafers.

(11) To drain DI-H_2O rinse tanks:

(a) Press TANK FILL button (lights off).
(b) Press TANK DRAIN button (lights on).

(12) Wait until DI-H_2O rinse tanks are drained.

(13) Press RINSE START (light off) to stop cycle.

[[**MOD 3**]] STANDARD OXIDE DIP PROCEDURE (S. Lester)

[**Purpose**]: to remove 20 to 300Å of oxide on wafer with no photoresist

[**Equipment**]: Sink 6

[**Summary**]:

(1) DI water, 15 seconds

(2) Dip (H_2O/HF=25/1 or H_2/HF=10/1, 25°C, 1 minute)

Note: Etch rate = 200 Å/minute (25/1); 500 Å/minute (10/1) or adjust dip time according to thickness of oxide to be stripped.

(3) Standard rinse-spin procedure.

[**Detailed Procedure**]:

(1) Clean HF bath.

(2) Rinse with DI water, aspirate. Repeat ten times.

(3) For $H_2O/HF=25/1$, fill dip tank with 3500 ml DI H_2, add 140 ml HF. For $H_2O/HF=10/1$, fill dip tank with 3500 ml DI H_2, add 350 ml HF.

Note: Solution should be mixed ten minutes before use. These dips are usually prepared in advance by the process technicians and changed out when depleted.

(4) Fill rinse tanks. Be sure tank fill lights are on and tank drain lights are off.

(5) Load wafers into a white teflon carrier and dip into DI water tank 1 or 4 to wet.

(6) Dip wafers into HF bath. Etch rate=200 Å/minute or 3.33 Å/second (25/1); 500 Å/minute or 8.33 Å/second (10/1).

(7) Standard rinse-spin procedure [[**MOD 3**]]

[[**MOD 4**]] WAFER CLEANING PROCEDURE AFTER RESIST REMOVAL (R. Wallach)

[Purpose]: to clean wafers of resist residue after resist has been removed using acetone or plasma ashing ([MOD 13,14])

[Equipment]: Sink 8 and Fluorocarbon rinser/spinner

(1) See Summary and Detailed Procedure for Standard Wafer Cleaning [[MOD 1]]. However, **clean in Sink 8** rather than sink 6 as directed. Sink 8 piranha bath is reserved specifically for cleaning wafers of resist residue.

(2) All wafers going into the furnace must be cleaned again in Sink 6 after Sink 8 per [MOD 1].

(3) Be sure to use the carriers numbered for the appropriate sink. Do not mix carriers between sinks 6, 7 and 8.

[[**MOD 5**]] STANDARD DEHYDRATION BAKE PROCEDURE (P.L. Pai)

[Purpose]: to dehydrate wafers before resist coating

[Equipment]: Tylan tube 7 or 8

[Summary]:

(1) Temp= 750°C

(2) Time= 10 minutes

[Detailed Procedure]:

(1) Standard clean wafers [[**MOD 1, 2, 3**]].

(2) Check tube temperature using ROP or on Tycom.

(3) Press OUT in the Remote Operating Panel (ROP) to bring boats out of tube.

(4) Wait 5 minutes once the boat is fully out to cool.

(5) Put wafers in the boat using the vacuum pick.

(6) Press IN on the ROP to return boat to the tube.

(7) Wait approximately 10 minutes once the tube has closed.
(8) Press OUT on ROP and wait 5 minutes for the wafers to cool.
(9) Transfer wafers back to the cassette.
(10) Press IN on the ROP to move boat back into the tube.

[[MOD 6]] STANDARD PHOTORESIST COATING PROCEDURE (K.Y. Toh)

A. HMDS TREATMENT OF WAFER SURFACE

[Purpose]: to improve photoresist adhesion to the wafer surface

[Equipment]: Sink 5

[Summary]:
(1) Immerse wafers in HMDS vapor for 3 minutes.

[Detailed Procedure]:
(1) Check that there is HMDS in the container in sink 5. You only need about a 1 cm depth of HMDS. Add HMDS if necessary.
(2) Transfer your wafers, in a carrier, to the HMDS container in sink 5 and close the cover.
(3) Wait for 3 minutes
(4) Remove the wafer carrier and replace the cover.
(5) Do **[MOD 6b]** Kodak 820 photoresist coating **immediately.**

B. KODAK 820 PHOTORESIST COATING

[Purpose]: to spin a 1.3 μm thick Kodak 820 positive photoresist layer onto 4" wafers

[Equipment]: EATON Wafer Track, program #10

[Summary]:

Note: Wafer must have been dehydrated and/or have had HMDS treatment.
(1) Execute program #10:
(a) Dispense photoresist for 3 seconds statically.
(b) Spin at 4600 RPM for 25 seconds.
(c) Soft bake at 120°C for 60 seconds.
(d) Cool on cold chuck at 20°C for 60 seconds.

[Detailed Procedure]:
(1) Enable the Eaton on the wand.
(2) Turn on the purge supply gas valve to the machine. The gas valve is under the front panel. The machine will beep and the TRACK 2 light will flash. Depress TRACK 2 to stop beeping.

(3) Depress STOP or HOLD button. Select program #10.

Note: You may transfer your wafers to the left blue wafer carrier. For best coating result, it is advisable to run three dummy wafers prior to your first run. The photoresist at the dispenser tip is likely to be contaminated and/or dried.

(4) Press START button to begin executing the program. Both loading and the receiving wafer carriers must be moved down when the program execution starts. If either of them does not move, lift it up, replace it onto the platform, and depress the white reset button behind the platform.

Note: If the machine beeps at any point during the coating process, stop beeping by depressing TRACK 2 button and depress ERROR 2 DISPLAY in sequence. The LED display window will display the error code. Refer to the quick reference guide in the drawer for error message.

(5) When all wafers have been coated and loaded into the receiving wafer carrier, depress the white button on the box right behind the receiving platform to raise the carrier to the top position.

(6) Remove your wafers and replace the carrier back to the receiving platform.

(7) Turn off the purge supply gas valve under the front panel.

[[MOD 7]]: STANDARD PHOTORESIST DEVELOPMENT (K.Y. Toh)

A. Photoresist Development with Kodak 932 Developer

[Purpose]: to develop 4 wafer with Kodak 932 developer (concentration: 50%)

[Equipment]: MTI Omnichuck.

[Summary]:

(1) Execute Program #1:

(a) Dispense developer for 60 seconds, at 5 psi tank pressure, 25°C controlled temperature, using number 22 needle, which will dispense about 30 cc per minute.
(b) Rinse at 2% speed for 20 seconds.
(c) Spin dry at 50% speed for 20 seconds.

[Detailed Procedure]:

(2) Turn on the power to the machine by pressing the red POWER button. The terminal will response with READY?

(3) Transfer your wafers to the blue wafer carrier and place on the loading platform.

(4) Type RUN,1 exactly as shown at the terminal, followed by <CR>.

(5) The blue RUN button on the machine will flash. Depress this button to begin executing the program.

(6) When all wafers have been developed, wait until the carrier returns to the up position before removing it from the platform.

(7) Remove your wafers and return the carrier back to the loading platform.

(8) Turn off the power to the machine.

B. INSPECTION

[Purpose]: inspect for clear development and correct line width

[Equipment]: Microscope, Nanoline, or Vickers

[Detailed Procedures]:

(1) Inspect wafer under microscope for clear development and correct line width.

(2) If development is satisfactory, go to the next step in your process flow path.

(3) If development is not satisfactory, carry out the following:

(a) [[MOD 13]] Acetone Resist Stripping
(b) [[MOD 4]] Wafer Cleaning After Resist Removal
(c) [[MOD 5]] Standard Dehydration Bake
(d) [[MOD 6,7]] Kodak 820 Photoresist Coating and Development

[[MOD 8]] STANDARD HARD BAKE PROCEDURE (M. Kushner)

[Purpose]: to bake out solvent in photoresist before etching or ion implantation

[Equipment]: Convection Oven

[Detailed Procedure]:

(1) Next to the convection oven are teflon cassettes specifically for use in hard bake. Load the wafers into one of the cassettes.

(2) Put cassette with wafers in convection oven for time and temperature specified below for the photoresist you intend to use.

General Resist Parameters

Product	Shipley Microposit S1450J (S1400-31)	Shipley Microposit S1450B	Kodak Micro Positive Resist 820	Hunt XWX-235 Waycoat Xanthochrome Positive Resist
Temp (C):	120.00	120.00	150.00	100.00
Time (min.):	25 ± 5	25 ± 5	30.00	30 (Optional)

[[MOD 9]] STANDARD DE-SCUM PROCEDURE (R. Wallach)

[Purpose]: to remove resist residue in normally cleared areas

[Equipment]: Technics-C

[Summary]:

(1) Vent the system and place wafers in chamber.

(2) Pump system down to base pressure (~ 35 mTorr).

(3) Introduce oxygen into chamber.

(4) Strike plasma by turning on power to 50 watts. Time for 1 minute.

(5) Turn off power, then gas.

(6) Pump down chamber to remove reacted gases.

(7) Vent chamber and remove samples.

[Detailed Procedure]

(1) The status of the machine should be as follows:

Mode:	Manual
Sol'n (Solenoid):	Closed
Vent:	Off
Power:	Toggle Off, Knob Pegged Counterclockwise
Gas #1:	Off
Gas #2:	Off

Occasionally the solenoid which controls the vacuum pump is left open. If this is the case, close it before enabling the system.

(2) Once you are ready to introduce your sample, vent the chamber by toggling the VENT switch. Be sure that the sol'n is closed when you do this. It will take about 15 seconds for the chamber to fill. Once it is at atmospheric pressure, open it carefully — the top is very heavy — and place your wafers on the plate. Close the top carefully, being sure not to allow it to fall.

(3) Oxygen for photoresist descum is connected through Gas #2.

(4) You are now ready to start the vacuum pump. **Leaving the vent *ON*, toggle the solenoid (vacuum pump) switch open. After 2 or 3 seconds, close the vent switch to allow the pump to lower the pressure of the chamber.**

(5) You can watch the pressure drop as the system comes under vacuum. When the system reaches 35 mTorr, you can introduce oxygen into the chamber by toggling the GAS #2 switch. The pressure in the chamber will rise as gas flows in, and then should stabilize.

(6) Once gas flow into the chamber is stable and at the desired pressure, (~ 300 mTorr - this is preset) you can strike a plasma by switching the POWER toggle on and turning the dial clockwise until 50 Watts is reached. You can see the plasma through the window on the front of the chamber. Begin timing your run for 1 minute.

(7) Once the run is complete, turn off the power, then the gas. *Always* turn off the power **before** turning off the gas.

(8) Allow the chamber to pump down to 35 mtorr so you can be sure all potentially harmful gases have been swept out of the chamber.

(9) Turn off the vacuum pump by switching the sol'n toggle to closed position. Now you may vent the chamber. Again, remember not to vent the chamber until the sol'n has been closed.

(10) The chamber will now come up to atmosphere and you may remove your sample.

(11) Once your sample has been removed, close the chamber and start the vacuum with the vent open. After a couple of seconds, close the vent and allow the chamber to pump down to ~ 35 mtorr. Close the sol'n. Be sure that gas switches and power are off.

[[MOD 10]] STANDARD WET OXIDE ETCHING PROCEDURE (R. Wallach)

[Purpose]: to etch oxide films in buffered oxide etch

[Equipment]: Wet Process Stations or Fume Hood

[Summary]:

(1) Being sure any photoresist on wafers has been hard baked, wet wafers in DI H_2O to prevent wafers sticking to film surface.

(2) Dip wafers in buffered HF (BHF) for required amount of time.

(3) Rinse/dry wafers per [[MOD 3]].

[Detailed Procedure]:

(1) Wet wafers in DI H_2O in tank 1 or 4.

(2) Immerse wafers in buffered HF for required amount of time based on etch rate (see below).

Etch rates (approximate):

BHF 10/1 ~ 500 Å/minute
BHF 5/1 ~ 1000 Å/minute

(3) Follow with rinse/spin ([[MOD 2,3]]).

[[MOD 11]] PLASMA ETCHING IN TECHNICS-C (R. Wallach)

[Purpose]: plasma etching of nitride and oxide films

[Equipment]: Technics-C

[Summary]:

(1) Carry out an O_2 scourge to clean chamber.

(2) Vent the system and place wafers in chamber.

(3) Pump system down to base pressure (~ 35 mTorr).

(4) Introduce desired gases into chamber.

(5) Strike plasma by turning on power to desired wattage. Time.

(6) Turn off power and gas.

(7) Pump down chamber to remove reacted gases.

(8) Vent chamber and remove samples.

[Detailed Procedure]

(1) The status of the machine should be as follows:

Mode:	Manual
Sol'n (Solenoid):	Closed
Vent:	Off
Power:	Toggle Off, Knob Pegged Counterclockwise

Gas #1: Off
Gas #2: Off

Occasionally the solenoid which controls the vacuum pump is left open. If this is the case, close it before enabling the system.

(2) Carry out an O_2 to clean the system with O_2 at 300 Watts for 20 minutes, following the outline given below for system operation (from Step (4)).

(3) Once you are ready to introduce your samples, vent the chamber by toggling the VENT switch. Be sure that the SOL'N is closed when you do this. It will take about 15 seconds for the chamber to fill. Once it is at atmospheric pressure, open it carefully — the top is very heavy — and place your wafers on the plate. Close the top carefully, being sure not to allow it to fall.

(4) Oxygen for photoresist descum/ashing and cleaning the system (scourge) is connected through Gas #2. The Gas #1 switch will flow (1) SF_6; (2) He; (3) CHF_3, and (4) O_2. Check correction factors on the PD module and setpoints for the particular gas you are going to use.

(5) You are now ready to start the vacuum pump. **Leaving the vent *ON*, toggle the solenoid (vacuum pump) switch open. After 2 or 3 seconds, close the vent switch to allow the pump to lower the pressure of the chamber.**

(6) You can watch the pressure drop as the system comes under vacuum.. When the system reaches 35 mTorr, you can introduce the gases you need into the chamber by toggling the appropriate gas switches on the PD and PE modules. The pressure in the chamber will rise as gas flows in, and then should stabilize. (See below for specific recipes for nitride and oxide etching.)

(7) Once gas flow into the chamber is stable and at the desired pressure you can strike a plasma by switching the POWER toggle on and turning the dial clockwise until desired wattage is reached. You can see the plasma through the window on the front of the chamber. Begin timing your run for required amount of time based on etch rate.

(8) Once the run is complete, turn off the power, then the gas. *Always* turn off the power before turning off the gas.

(9) Allow the chamber to pump down to 35 mtorr so you can be sure all potentially harmful gases have been swept out of the chamber.

(10) Turn off the vacuum pump by switching the sol'n toggle to closed position. Now you may vent the chamber. Again, remember not to vent the chamber until the sol'n has been closed.

(11) The chamber will now come up to atmosphere and you may remove your sample.

(12) Once your sample has been removed, close the chamber and start the vacuum with the vent open. After a couple of seconds, close the vent and allow the chamber to pump down to ~ 35 mtorr. Close the sol'n. Be sure that gas switches and power are off.

A. Nitride Etch

Set Points: SF6 - 13.0
He - 21.0

Power: 50 Watts

Etch Rate: ~ 500 Å/minute

It is suggested that you approximate the time you will need to etch through your nitride film, run your sample for half the total time, open the chamber and rotate your wafers around their central axes by 180°C, and then etch again. This provides more uniformity in etching.

B. **Oxide Etch**

Set Points:	O2 - 2.0 CHF3 - 7.0 (Gas #1, using PD module to regulate flow)
Pressure:	Between 100-150 mTorr
Power:	100 W

It is difficult to estimate the etch rate, since doped oxides will etch a good deal more rapidly than undoped oxides. It is suggested you do a test run for your particular film before actually etching your sample.

[[MOD 12]] LAM PLASMA ETCHER OPERATING PROCEDURE (P.L. Pai)

[**Purpose**]: to etch polysilicon with CCl_4/He plasma

[**Equipment**]: Lam etcher

[**Summary**]:

(1) Load the recipe.

(2) Load the carrier with wafers into system.

(3) Run the recipe.

(4) Unload the wafers.

[**Detailed Procedure**]:

(1) Insert the poly-Si etching recipe module into the slot.

(2) Load the recipe by pushing SAVE button.

(3) Check recipe by pushing RECIPE button. End of etching is determined by the end point detector. You do not need to enter anything.

(4) If you want to change process variables and enter new etching time:

(a) move the cursor to the proper position
(b) enter via keyboard if numerical
(c) enter via FIELD SELECT button if not numerical.

(5) Load the wafers into cassette at the sending end.

(6) Push START button.

(7) When the process is finished, unload the wafers from the receiving end.

(8) Do not leave machine while it is processing your wafers.

[[MOD 13]] ACETONE RESIST STRIPPING PROCEDURE (K.Y. Toh)

[**Purpose**]: to remove soft photoresist from wafer

[**Equipment**]: MTI Omnichuck

Note: Program steps are in step 10 to step 16.

[Summary]:

(1) Execute Program #10:

(a) Spin wafer at about 300 RPM.
(b) Dispense acetone for 10 seconds.
(c) Rinse with DI water for 20 seconds.
(d) Spin dry for 20 seconds.

(2) Do [[**MOD 4**]] wafer cleaning procedure after resist removal.

[Detailed Procedure]:

(1) Transfer your wafers to the blue wafer carrier in the machine and return it to the loading platform.
(2) Turn on power to the machine.
(3) Terminal will response with READY?.
(4) Type: RUN,10 on the terminal followed by <CR>. Blue RUN button on the machine will flash.
(5) Press the RUN button to start the program. Wafers will return to the wafer carrier after the process is completed.
(6) Wait till the carrier returns to the original position before removing it from the platform.
(7) Remove your wafers with vacuum wand or flip-transfer and replace the wafer carrier to the loading platform.
(8) Turn off power to the machine.
(9) Do [[**MOD 4**]] wafer cleaning procedure after resist removal.

[[MOD 14]] PLASMA ASHING OF PHOTORESIST (K.Y. Toh)

[Purpose]: to remove photoresist using oxygen plasma

[Equipment]: Technics-C

[Summary]: **Note**: Etch rate is linear with time and power:

Etch Rate [**A/minute**] = 12.5 * power [**watts**]

(1) Vent the system and place wafers in chamber.
(2) Pump system down to base pressure (~ 35 mTorr).
(3) Introduce oxygen into chamber.
(4) Strike plasma by turning on power to 300 watts. Time.
(5) Turn off power, then gas.
(6) Pump down chamber to remove reacted gases.
(7) Vent chamber and remove samples.

[Detailed Procedure]

(1) The status of the machine should be as follows:

Mode:	Manual
Sol'n (Solenoid):	Closed
Vent:	Off
Power:	Toggle Off, Knob Pegged Counterclockwise
Gas #1:	Off
Gas #2:	Off

Occasionally the solenoid which controls the vacuum pump is left open. If this is the case, close it before enabling the system.

(2) Once you are ready to introduce your sample, vent the chamber by toggling the VENT switch. Be sure that the sol'n is closed when you do this. It will take about 15 seconds for the chamber to fill. Once it is at atmospheric pressure, open it carefully — the top is very heavy — and place your wafers on the plate. Close the top carefully, being sure not to allow it to fall.

(3) Oxygen for photoresist ashing is connected through Gas #2.

(4) You are now ready to start the vacuum pump. **Leaving the vent *ON*, toggle the solenoid (vacuum pump) switch open. After 2 or 3 seconds, close the vent switch to allow the pump to lower the pressure of the chamber.**

(5) You can watch the pressure drop as the system comes under vacuum. When the system reaches 35 mTorr, you can introduce oxygen into the chamber by toggling the GAS #2 switch. The pressure in the chamber will rise as gas flows in, and then should stabilize.

(6) Once gas flow into the chamber is stable and at the desired pressure, (~ 300 mTorr - this is preset) you can strike a plasma by switching the POWER toggle on and turning the dial clockwise until 300 Watts is reached. You can see the plasma through the window on the front of the chamber. Begin timing your run.

(7) Once the run is complete, turn off the power, then the gas. *Always* turn off the power before turning off the gas.

(8) Allow the chamber to pump down to 35 mtorr so you can be sure all potentially harmful gases have been swept out of the chamber.

(9) Turn off the vacuum pump by switching the sol'n toggle to closed position. Now you may vent the chamber. Again, remember not to vent the chamber until the sol'n has been closed.

(10) The chamber will now come up to atmosphere and you may remove your sample.

(11) Once your sample has been removed, close the chamber and start the vacuum with the vent open. After a couple of seconds, close the vent and allow the chamber to pump down to ~ 35 mtorr. Close the sol'n. Be sure that gas switches and power are off.

[[**MOD 15**]] PHOTORESIST STRIPPING WITH NOPHENOL 922 (K.Y. Toh)

[**Purpose**]: to remove hardened photoresist on wafer after high energy implant

Note: Photoresist can normally be removed using plasma ashing ([MOD 14]). Only in cases of abnormally high implant doses does the resist become hard enough to warrant this treatment.)

[**Equipment**]: Sink 5, temperature controlled bath on the left.

[**Summary**]:

(1) Heat up Nophenol 922 to 110°C.
(2) Immerse wafer in solution for 10 minutes
(3) Rinse thoroughly in DI water.
(4) Do [[**MOD 4**]] wafer cleaning procedure after resist removal.

[Detailed Procedure]:

(1) Turn on the temperature controller to the Nophenol 922 bath, which is on the left of wet bench 5.
(2) Check that the temperature setting is 110°C. It will take about 30 minutes to stabilize at this temperature.
(3) Transfer your wafers to the white teflon cassette specially marked as 922.

Important: Use only the cassette and cassette holder that are marked with

(4) Immerse cassette and wafers in the bath for 10 minutes when the temperature is stablized. (It is advisable to rotate your wafers by 90° with respect to the cassette after about 7 minutes to avoid incomplete dissolution of the photoresist hidden within the slots).
(5) Remove the cassette from the bath. Inspect your wafers visually for resist residue. Repeat step 4 if necessary.
(6) Rinse wafers 3 times with DI water in the overflow tanks number 1, 2 and 3, until the resistivity of the water is above 12 MΩ-cm.

Note: Water may become milky in the first rinse.

(7) Turn off temperature controller if you do not expect anyone to use it within the next hour.
(8) Do [[**MOD 4**]] wafer cleaning procedure after resist removal.

[[**MOD 16**]] STANDARD FURNACE CLEANING PROCEDURE (I.C. Chen, K. Voros)

[Purpose]: to remove heavy metal ions from the furnace tube

[Equipment]: Tylan furnaces

[Summary]:

A. Run STCA recipe: Standard TCA clean

(a) Ramp up to 1100°C.
(b) Oxygen flow: 2 minutes (02=4, N2=0)
(c) TCA clean: 5 minutes (TCA=on, 02=2.0) 60 cycles of (b) and (c).
Note: the TCA flow rate can not be specified in the recipe.
(d) Post-ox: 5 minutes (02=4, TCA=off)
(e) Ramp down to 750°C. This process takes about 7 hours.

B. Run MAIN recipe: Temperature calibration in 50° steps from 750°C to 1100°C.

(a) Oxygen flow: 2 minutes (02=4, N2=0)
(b) TCA clean: 5 minutes (02=4.0, TCA=ON)
(c) 60 cycles of (a) and (b).
(d) Ramp down to 750°C. This process takes about 10 hours.

[Detailed Procedure]:

(1) Put the Tyln Main floppy disc in the disc drive.
(2) Load STCA or MAINtenance program into required tube.
(3) When the computer asks for delay time, type in requested time such that the process ends after 8am.
(4) If the loading is completed, a GOOD LOAD response will appear on the screen.
(5) Go to the tube and press RUN on the ROP (remote operation panel), or type RUN tube#.
(6) Open the scavenger door fully (tubes 5-8, 13-16).
(7) After the cleaning is done, the alarm will sound. Press the ALARM ACK button on the ROP.
(8) For best results, use tube soon after cleaning.

NOTE: These programs can only be aborted in an oxygen flow step.

[[MOD 17]] STANDARD TYLAN OPERATION PROCEDURE (I.C. Chen)

[Purpose]: to load the recipe into the furnace controller and run the process

[Equipment]: Tylan furnaces

[Summary]:

(1) Load the recipe into the controller.
(2) Run the recipe.
(3) Load the wafers onto the boat. Push the wafers in.
(4) When program has concluded, remove wafers.

[Detailed procedure]:

(1) Put the floppy disc in the disc driver. There is a standard disk available to all users.
(2) Load the recipe to the tube by typing 'LO recipename tube#'.
(3) If the loading is completed, a GOOD LOAD response will appear on the screen.
(4) Go to the tube and press RUN on the ROP (remote operation panel), or type in
(5) After the boat puller stops, load the wafers onto the boat using the vacuum pen.
(6) Press the ALARM ACK button on the ROP, and the wafers will be pushed in.
(7) After the run is complete, the alarm will sound. Press ALARM ACK on ROP or type 'ACK tube#' to stop the alarm.
(8) Press the OUT button on the ROP and the boat will be pulled out, or start recipe again (step 4).
(9) Wait a few minutes (to let the wafers cool down), then unload the wafers using the vacuum pen.
(10) Press the IN button on the ROP to let the puller in, or repeat Step 6, then ABORT.

Note: It is a good idea to check your run at the critical steps such as turning on wet oxidation, to avoid surprises at the end.

[[MOD 18]] SPIN-ON SIO_2 GLASS (SOG) PROCEDURE (P.L. Pai, K. Chan)

[Purpose]: to provide inter-metal dielectric for double metallization

[Equipment]: Headway spinner, convection bake oven, and Tylan tube 14.

[Summary of Double Metallization Procedure]:

(1) First define Al pattern (0.6μm thick).
(2) Coat wafer with SOG as described in detailed procedure below.
(3) Deposit 0.8 μm undoped SiO_2 by PECVD on Technics-B.
(4) Print via photo mask.
(5) Etch: wet etch ~ 0.6μm of oxide, plasma etch remaining oxide and SOG.
(6) Remove resist.
(7) Dip in Al etch for 10 seconds just before sputtering second Al.
(8) Rinse well, do not bake.
(9) Sputter 0.8-1.0μm of Al.
(10) Define second Al.
(11) Sinter at 400°C for 20 min in forming gas.

[Detailed Procedure]:

(1) Dry the wafer in convenction oven at 120°C for 30 minutes.
(2)
  a. Place wafer on the Headway spinner.
  b. Adjust speed to 3000 rpm.
  c. Set spinning time to 20 seconds.
  d. Use a dropper to dispense 3 cc of Futurex IC1-200 SiO2 SOG on the wafer.
  e. Start spinning.
(3)
  a. Place wafer in 120°C oven for 30 minutes.
  b. Increase temperature of oven to 200°C and bake wafer for 30 minutes.
(4) Anneal wafer in Tylan tube 14 using either SOGN2 or SOGO2 program (400°C for 30 minutes.)

```
#!/bin/csh -f
#
# define shell for which this script is written
#    -f option specifies fast shell start-up
#         i.e. csh neither searches for, nor executes
#              commands found in .cshrc in current directory
#
#
# -----------------------------------------------------------------
# |                                                               |
# |   script "hotpotato"                                          |
# |                                                               |
# |   revised 12/18/86 by Lyndon C. Lim                           |
# |                                                               |
# |  Microfabrication Laboratory                                  |
# |                                                               |
# -----------------------------------------------------------------
#
# files:
# ------
#    entry.template          - contains the template for the entries
#                              to the process log file "process.log"
#
#    hotpotato.help          - help file for "hotpotato" script
#
#    process.log             - running account of the process status.
#                              Contains process parameters and
#                              measured values as recorded during the
#                              run, e.g. oxide thickness, implant energy
#                               (1) date and time of entry
#                               (2) who was the last person working
#                                   on the wafer lot
#                               (3) location of wafer lot
#                               (4) the last process step performed
#                               (5) the next process step to be performed
#                               (6) relevant observations and measurements
#
#    process.modules         - contains detailed descriptions for
#                              individual process steps, e.g. wafer
#                              cleaning, photoresist application,
#                              oxide etching.
#
#    $process_name.outline - contains outline of the process being
#                              run.  More explicit details of process
#                              steps are in the "process.modules" file.
#
#
# variables:
# ----------
#    $archives           := directory where process directories
#                           (of type $process_name) are kept.
#                           (script-defined)
#
#    $library            := directory where following files are kept
#                           (script-defined)
#                            - entry.template
#                            - hotpotato.help
#                            - process.modules
#                            - $process_name.outline
#
#    $path               := string of characters where each word of
#                           the path variable is a directory in which
#                           commands are sought for execution.
#                           Otherwise, if no path variable is specified,
#                           only commands specified with their full path
#                           names will execute.  Used by the shell.
#
#    $pathroot           := directory where the following directories
#                           are located.  (script-defined)
#                            - $archives
#                            - $library
#
#    $process_archives := full path name of the process directory.
#                           Consists of $archives + $process_name.
#
#    $process_name       := process directory where following files for
#                           a particular process are kept: (user-defined)
#                            - process.log
#                            - old process logs (dated)
```

```
#
#
# hierarchy:
# ----------
#
#                             pathroot
#                              /    \
#                             /      \
#                            /        \
#                     library        archives
#                                   /   |   \
#                                  /    |    \
#                                 /     |     \
#               process_name1   process_name2   process_name3
#
#
#
#
#
# aliases:
# --------
#    show      := program executed to display files,
#                   e.g. "lookat" or "more"  (script-defined).
#
#
# define variables and aliases
# -------------------------
set path      = ( /usr/ucb    \
                  /usr/bin    \
                  /usr/local  \
                  /bin        )
set pathroot = /lab/users/cmos
set archives = $pathroot/Process_Archives
set library  = $pathroot/Process_Library
set TRUE     = 1
set FALSE    = 0
alias show     /usr/local/lookat -hs
#
#    options invoked with lookat:
#         -h  prints out a short help prompt at top of window
#         -s  squeezes out multiple consecutive blank lines
#                in order that the maximum amount of useful
#                information can be displayed on the screen.
#
#
#---------------------------------------------------------------
#
# If this script is invoked without an argument, where $argv[1]
#    is the name of the process, then display a menu of existing
#    processes and prompt for a process name.  If the process
#    name given at the prompt is a null string, then abort script
#    execution.
#
# Otherwise, the argument given is taken to be the process name.
#---------------------------------------------------------------

if $user != "cmos" then
    echo "$user is not a valid user for $0"
    exit
    endif

if ( $#argv == 0 ) then

    set process_undefined = $TRUE

    else

    set process_undefined = $FALSE

    endif

process_menu:

if  ( $process_undefined ) then

    clear
    echo    "Existing Processes:"
```

```
    echo    "==================".
    echo    ""

    ls -1 $archives

    echo    ""
    echo -n "Select an existing process or enter a new process.  "
    echo    "End with [RETURN]"
    echo    ""
    echo -n "Process name: "

    set process_name = $<


    if ($process_name == "" ) then
        echo ""
        echo "No action taken.  Exiting $0...."
        echo ""
        exit
    endif

else

    set process_name = $argv[1]

endif

set process_archives = $archives/$process_name
#
#
#-----------------------------------------------------------------------
#
# if the process requested exists and is a directory, then display
#   the menu of operations.  Otherwise, verify that user wishes to
#   to create a new process, prompt for the location of the process
#   outline, and create the corresponding directory, "process.log",
#   and $process_name.outline files.
#-----------------------------------------------------------------------
if ( ! ( -e $process_archives && -d $process_archives )) then

    echo    ""
    echo -n "Create new process [" $process_name "] ? (y/n) "

    set response = $<

    if ( $response == "y" ) then

        echo -n "Process outline: (specify complete path) "
        set response = $<


        if ( -e $response && -f $response ) then

            cp $response $library/$process_name.outline

        else

            echo    ""
            echo    "Process outline $response not found."
            echo    "No action taken.  Exiting $0...."
            echo    ""
            exit

        endif


        mkdir $process_archives

        echo    "Microlab " $process_name " Process Log" \
                                    >! $process_archives/process.log
        echo    "Begun on `date` by $user@`hostname`"    \
                                    >> $process_archives/process.log

        chmod 666  $process_archives/process.log

    else

        echo ""
```

```
        echo "No action taken.  Exiting $0....."
        echo ""
        exit

    endif

endif
#
#----------------------------------------------------------------
#
# Display second menu page, which lists options to change and
# to view the various files relating to the process requested.
#----------------------------------------------------------------
#
onintr option_menu

option_menu:
#
# display menu
# ------------
    clear
    echo    ""
    echo $0 " - Select an option:    [ Process: $process_name ]"
    echo    "======================================================="
    echo    ""
    echo    "[ 1] ( dl) Display the process log"
    echo    "[ 2] ( el) Edit    the process log"
    echo    ""
    echo    "[ 3] ( dm) Display the process modules"
    echo    "[ 4] ( do) Display the $process_name process outline"
    echo    "[ 5] ( ro) Replace the $process_name process outline"
    echo    ""
    echo    "[ 6] ( lo) Display process log and $process_name"
    echo    "           process outline          (split screen)"
    echo    ""
    echo    "[ 7] (  h) Help"
    echo    "[ 8] (  r) Return to menu of available processes"
    echo    "[ 9] (e q) Exit / End script"
    echo    ""

await_response:

    echo -n "Enter option followed by [RETURN]: "

    set response = $<
    echo    ""

    switch ($response)

#
#
# display the "process.log" file
# ------------------------------
#        i.e. recorded process run parameters
#
    case  "1":
    case  "dl":
        clear
        echo 'Type "e" to go to end of process log.'
        show $process_archives/process.log
        breaksw
#
#
# edit "process.log" file
# -----------------------
    case  "2":
    case  "el":
#
        if (-e $process_archives/$process_name.lock) then
            echo   "Simultaneous write access to $process_name process"
            echo   "log is not allowed.  Please try again later."
            breaksw

        else

            date > $process_archives/$process_name.lock

        endif
```

```
        set unique = `date | awk '{print $2 $3 $4}'`

        rm -f $process_archives/log.*
        cp $process_archives/process.log $process_archives/log.$unique
#
#       set up template at end of process log file
#       -----------------------------------------
        echo ""                        >> $process_archives/process.log
        echo "Microlab $process_name Process Step File"       \
                                       >> $process_archives/process.log
        echo "Last Modified on `date` by $user"              \
                                       >> $process_archives/process.log

        cat $library/entry.template >> $process_archives/process.log
#
        clear
        echo 'Type "G" to go to end of process log.'
#
        onintr remove_lock
        vi $process_archives/process.log
#
remove_lock:
        rm -f $process_archives/$process_name.lock
        onintr option_menu
        breaksw
#
#
# display the "process.modules" file
# --------------------------------
    case  "3":
    case  "dm":
        show $library/process.modules
        breaksw
#
#
# display the "$process_name.outline" file
# ---------------------------------------
    case  "4":
    case  "do":
        show $library/$process_name.outline
        breaksw
#
#
# replace the "$process_name.outline" file
# ---------------------------------------
    case  "5":
    case  "ro":
        echo    "Replace old $process_name outline with new outline. "
        echo -n "Process outline: (specify complete path) "
        set response = $<

        if ( -e $response && -f $response ) then

            cp $response $library/$process_name.outline

        else

            echo   ""
            echo   "Process outline $response not found."
            echo   "No action taken."
            goto await_response

        endif

        breaksw
#
#
# display the "process.log" file and
#   "$process_name.outline" file
#    in a split screen format
# --------------------------------
    case  "6":
    case  "lo":
        show $process_archives/process.log
             $library/$process_name.outline
        breaksw
#
```

```
#
# display the "hotpotato.help" file
# --------------------------------
    case   "7":
    case   "h":
        echo "Brief explanation of each of the commands"
        show $library/hotpotato.help
        breaksw
#
#
# return to the menu of available processes
# ------------------------------------------
    case   "8":
    case   "r":
        set process_undefined = $TRUE
        goto process_menu
        breaksw
#
#
# exit the program
# ----------------
    case   "9":
    case   "q":
    case   "e":
        echo "Exiting $0...."
        echo ""
        exit
#
#
# response to unrecognized commands
# ---------------------------------
    default:
        echo "Unrecognized response - $response"
        goto await_response
        breaksw
#
#
    endsw

goto option_menu
#
# THE END
```