AN EXPERT SYSTEM FOR POLYSILICON RECIPE GENERATION

by

Kuang-Kuo Lin

Memorandum No. UCB/ERL M87/50

21 July 1987

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Table of Contents

An Expert System for Polysilicon Recipe Generation

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ABSTRACT

An expert system that generates process steps for low pressure chemical vapor deposition (LPCVD) in-situ doped polysilicon is a component of the Berkeley Intelligent Processing System (BIPS). Inputs are the desired physical and electrical properties of polysilicon, and priorities or limits on process temperature, time, etc. Tabular, functional, and heuristic knowledge is employed. Outputs include machine-independent LPCVD process parameters as well as machine-specific commands for direct control of fabrication equipment. Experimental polysilicon films based on recipes generated are close to the input specifications.

July 14, 1987

PART I: The System Preview

Chapter 1: Introduction

An integrated-circuit (IC) expert system, the Berkeley Intelligent Processing System (BIPS), has been implemented. It is a system comprised of many smaller expert systems for the IC manufacturing environment [1-2]. The system is aimed at automating the IC manufacturing process starting from the more abstract and front-end machine-independent design to the more specific and back-end machine-dependent monitoring and diagnosis. In other words, BIPS provides a complete solution for an IC manufacturing process by first generating an IC process recipe based on general semiconductor knowledge, later translating the machine-independent recipe to machine-specific recipe for achieving the required processing environment, and then finally monitoring and diagnosing the process. The knowledge base of BIPS integrates the heuristic reasoning ability of expert systems as well as conventional quantitative aids for analysis, design, simulation, data acquisition, and data reduction. BIPS works with quantitative data relevant to design, fabrication, and test stored in a common INGRES database. The architecture of BIPS is modular and hierarchical. The architecture is also designed to be easily adaptable to other IC processes. A specific focus is now on the design and control of the low pressure chemical vapor deposition (LPCVD) furnace process. The first process examined in depth is in-situ doped polysilicon deposition.

In-situ doped polysilicon produced by low pressure chemical vapor deposition (LPCVD) simplifies polysilicon processing by eliminating a separate doping step. It is a relatively new and complicated process involving 11 processing parameters that control the resulting polysilicon film properties. Due to its level of complexity and practical significance, this polysilicon process was chosen as the first application domain of BIPS.

This report will start with a brief overview of BIPS architecture, then the report will concentrate on describing the front-end expert system recipe generator of BIPS for the LPCVD in-situ doped polysilicon. The inputs to the recipe generator are the desired physical and electrical properties of the polysilicon, and priorities or limits on process temperatures, process time, etc. The outputs include machine-independent LPCVD process parameters as well as machine-specific commands for direct control of the fabrication equipment.

The recipe generator partitions the knowledge base into general semiconductor knowledge and local equipment knowledge for an easier adaptation to individual integrated circuit (IC) manufacturing environment and a better IC process design environment. In addition, the generator supports the process design by employing diverse knowledge such as quantitative, qualitative and empirical knowledge. It also incorporates intelligent functions such as modular determination of the processing parameters and hypothetical generation of different possible operating scenarios. Interactive bit-mapped graphic displays present the engineer with all vital processing information. The recipe generator is linked to other modules of BIPS to provide direct monitoring and diagnosis of the on-going process [12-13]. The entire BIPS system is one aspect of our current effort to incorporate expert system technology in Computer Integrated Manufacturing (CIM) to improve both quality and productivity in IC processing.

BIPS has been developed using the Automated Reasoning Tools (ART) from Inference Corp. and Texas Instruments (TI) Explorer workstations. The present version has approximately 12,000 lines of code (with around 5000 lines for the recipe generator) consisting about 300 rules and 200 schema* (frames).

* A structure within a knowledge base that relates objects or classes of objects that share certain properties [10].

Chapter 2: An overview of the architecture

2.1 The architecture of BIPS

Within the BIPS architecture, the polysilicon design capability is partitioned into 3 modules: *the recipe generator, the recipe interpretor and the recipe supervisor.*

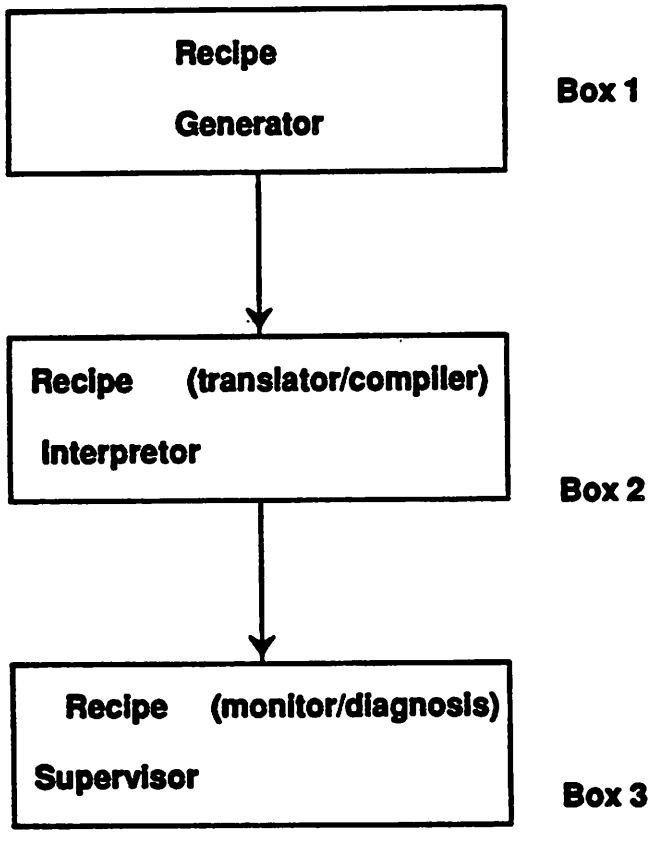


Fig. 2.1 BIPS architecture

The *recipe generator* (box 1 of Fig. 2.1), which is the front end module of BIPS, accepts higher-level goals such as the desired physical (e.g. thickness) and electrical (e.g. resistivity) properties of the polysilicon, and priorities on processing parameters, as inputs. Then the generator will synthesize equipment-independent recipes containing the processing conditions (such as the deposition temperatures/time, annealing temperature/time, pressure, gas flows, etc.) from its internal semiconductor knowledge base. The recipe generator is in one sense the reverse of many IC process simulators (such as SUPREM), which usually derive the goals from an input deck of trial processing parameters. Recipes from the recipe generator are equipment independent and therefore are portable between different manufacturing environments.

In order to provide a complete solution down to the machine executable level to process the wafers, the *translator/compiler module (i.e. the interpretor)* (box 2 of Fig. 2.1), where most of the local equipment knowledge base resides, maps the equipment independent recipe to equipment dependent and executable recipe. The equipment dependent and executable recipe consists of the specific equipment knob settings such as the temperature ramping rates and gas valves controls to achieve the required processing conditions specified by the recipe generator.

Finally, the ability to generate an equipment executable recipe does not assure that we meet the final objective. We therefore need to monitor the process to guarantee the achievement of the goals. Hence, after the recipe is down-loaded to the furnace by the translator/compiler module, the *monitor/diagnosis module (i.e. the supervisor)* (box 3 of Fig. 2.1) will display vital run-time processing information. It produces equipment maintenance warnings and failure diagnosis through graphical displays. All processing information (goals, recipes and run-time data) will be compressed before storing in the INGRES* database.

* INGRES is a relational database system currently used in the Berkeley microfabrication laboratory.

2.2 The architecture of the recipe generator

The complete architecture (Fig. 2.2) of the recipe generator should consist of all of the 6 proposed modules: resistivity, thickness, uniformity, grain size, stress and supporting. It should also consist of a mixed knowledge base, a numerical interpolator and a hypothetical generator.

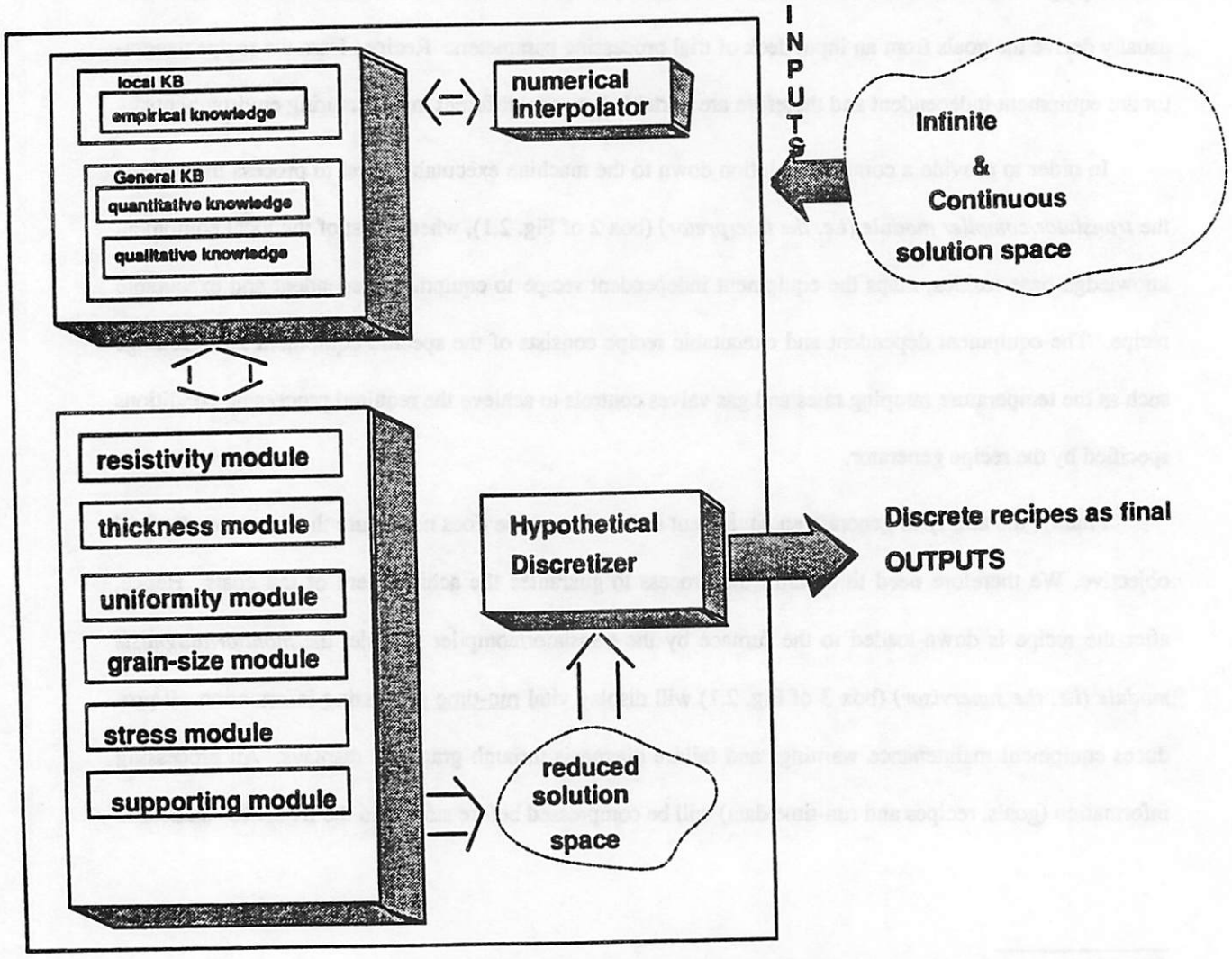


Fig. 2.2 The architecture of the recipe generator

(1) There are 11 processing variables for the in-situ doped polysilicon LPCVD process. Thus simultaneous determination of all the parameters is almost an impossible task (ref. Chapter 4). The strategy of "divide and conquer" was employed by dividing the recipe generator into 6 submodules (resistivity, thickness, uniformity, grain size, stress and supporting) to simplify the determination of the 11 processing parameters. Each module is responsible for a subset of the parameters and provides sufficient interactions with the others via parameter passing. For example, the resistivity and thickness submodules control the center-zone deposition temperature, while the uniformity submodule will determine the temperature relationship between the furnace center zone and end zones*. A detailed discussion of the modules will be given in Chapter 5.

(2) The recipe generator has a mixed knowledge base. The knowledge base has 3 components: the empirical knowledge base, the qualitative knowledge base and the quantitative knowledge base. Since the in-situ doped polysilicon LPCVD process is not a well-understood one, a complete quantitative solution derived entirely from first principle is infeasible. Hence for practical reasons, the recipe generator has to rely on different types of knowledge, i.e. the empirical, the qualitative and the quantitative, to solve the problem. In Chapter 6 the report will discuss the roles and interactions of the knowledge bases.

(3) A simple linear numerical interpolator was also implemented to aid the analysis of the empirical knowledge base. A more accurate algorithm, such as the spline interpolation algorithm, will be incorporated into the numerical interpolator to provide more precise information. The interpolator will be mentioned briefly in Chapter 6.

(4) Due to the inherit properties of the problem domain, there are many non-random combinations of the process variables that can satisfy a given set of input specifications. Therefore we have incorporated

* Conventional IC furnace is designed with several temperature zones for temperature controls Usually temperatures are setup differently in each zone to control the growth rate of the deposition material.

a hypothetical-generating capability into the recipe generator. The recipe generator will provide users with different possible scenarios and let the user explore alternate results. Alternatives are presented to the user in an interactive manner intended to stimulate creative thinking. Chapter 7 will give the implementation details of the hypothetical generator.

Chapter 3: Comparisons with conventional approaches

3.1 Synthesis vs Simulation

BIPS is in one sense the reverse of many current IC process simulators (e.g. SUPREM). Traditional IC process CAD tools are simulation-oriented. Users must supply the processing steps for simulation and hopefully, by trial and error, obtain the desired results. BIPS, on the other hand, is goal-oriented. It synthesizes the processing steps from the given processing goals, such as the polysilicon thickness and resistivity for a polysilicon deposition.

3.2 Direct link to equipment

BIPS can down-load the generated equipment executable recipes to run the process. Ad hoc fine tunings of the equipment for different processing goals will be minimized. This implies a shorter turn-around time, which is especially essential to Application Specific Integrated Circuit (ASIC) production. Also, direct links to equipment enables monitoring and diagnosis so as to ensure on-target results.

3.3 Partition and Classification of Knowledge

The modular and hierarchical separation of the general semiconductor knowledge (which resides mostly in the recipe generator module) and the local equipment specific knowledge (which resides mostly in the translator/compiler module and monitor/diagnosis module) result in the following advantages:

(1) A simpler design environment: Conventionally, IC process engineers/technicians needed to be familiar with general semiconductor knowledge and local equipment knowledge. Both types of

knowledge are difficult to acquire and accumulate, and both are required for writing complicated CAD simulation instructions to achieve the design goals [4] (sample run shown on Appendix 1, pg. 52) and for translating the confirmed simulated results to equipment executable codes for processing the wafers (sample equipment codes shown on Appendix 2, pg. 53). BIPS generates recipes down to the equipment settings based on the specifications of the process goals. Users can now concentrate on the design goals rather than the intermediate processing steps to attain the final goals. BIPS has simplified the design of a polysilicon recipe by relieving the users of the details of complicated processing steps and the equipment-specific commands to execute the steps.

(2) An easier diagnostic environment: Diagnosis is made easier by classifying problems into process-related problems and equipment-related problems. Process-related problems can be referenced back to the recipe generator module for possible correction or updating of the existing rules. Equipment-related problems can be referenced back to the monitoring/diagnosis module for possible warnings or maintenance actions.

(3) An easier accommodation to frequent changes in fabrication equipment and process [3]: Only a portion of the entire knowledge base needs to be modified, without affecting the others, in case of changes in general semiconductor knowledge base (module 1) or in local equipment knowledge base (module 2-3).

(4) An easier adaptation to local manufacturing environment: With only modifications needed for the *translator/compiler and monitor/diagnosis* modules for different vender machines, the BIPS system can be easily tailored to local manufacturing environments.

(5) Preservation and integration of valuable knowledge: The valuable semiconductor knowledge and equipment specific knowledge, that are difficult to acquire at the same time, are being integrated and preserved in one system.

PART II: The Implementation Details

Chapter 4: Classification of the operating parameters and determination of the operating ranges

The 11 processing parameters (3 deposition zone temperatures, deposition time, annealing temperature, annealing time, gas flows for SiH_4, PH_3, N_2, system pressure and system geometry) for the LPCVD in-situ doped polysilicon deposition are classified into *primary* parameters (such as deposition temperature, deposition time, annealing temperature, annealing time, etc.) and *secondary* parameters (such as N_2 gas flow, system geometry, etc.). Primary parameters are first estimated and then fine tuned with reference to secondary parameters. Processing parameters are confined to practical and well-behaved regions in order to reduce the search space. For example, the specified polysilicon thickness should be greater than 2000 Å to reduce the dependence of resistivity on thickness. The PH_3/SiH_4 ratio is kept above 0.01 so that both deposition rate and resistivity are less sensitive to the gas flows [5-8].

4.1 The solution space

The system *inputs* are (listed in order of significance):

(1) Polysilicon film thickness

(2) Polysilicon sheet-resistance (or resistivity)

(3) Polysilicon grain size

(4) Polysilicon stress

The system *outputs* are (listed in order of significance):

(1) Deposition temperatures at the 3 furnace zones: load, center and source.

(2) Deposition time

(3) Annealing temperature

(4) Annealing time

(5) Gas flow rate for PH_3, SiH_4, N_2

(6) Furnace pressure

(7) System geometry of furnace, wafer boats, wafer spacing and loading factor.

4.2 Screening and classification of parameters

Simultaneous determination of the values for the 11 output parameters is impossible. Hence prior *screening* and *classification* of the parameters are needed [9]. The output parameters are classified into 2 classes:

(1) primary -- deposition temperatures at 3 zones, deposition time, annealing temperature, annealing time and PH_3, SiH_4 flow rates.

(2) secondary -- N_2 flow rate, furnace pressure and system geometry.

The current preliminary system can determine a subset of the primary parameters (center zone deposition temperature, deposition time, annealing temperature, annealing time and PH_3, SiH_4 flow rates) while leaving all secondary parameters at their "optimum" values most commonly used in our lab. An algorithm for determining the relationship between the end zones temperature and the center zone temperature is still under investigation and not yet implemented in the expert system.

Also, input parameters are classified into primary (polysilicon thickness and resistivity) and secondary (polysilicon grain size and stress) inputs. The current preliminary version only accepts polysilicon thickness and resistivity (or sheet resistance) as inputs. We are not able to measure grain size and stress of the deposited polysilicon in our lab. Modules for these two input parameters are not implemented.

4.3 Preconfinement of the operating ranges

Parameters should be confined to practical and well-behaved operating regions in order to reduce the search space for a solution. Current operating ranges for the outputs assumed are:

(i) Deposition Temperatures: For short processing time and minimum resistivity, deposition temperatures are confined to the range from 600 to 700 °C. The maximum zones temperature difference in the furnace for achieving film thickness uniformity is 50 to 70 °C to avoid widely varying polysilicon grain size along the furnace tube.

(ii) Annealing Temperatures: Usually the annealing temperature is from 800 °C to 1100 °C to minimize the dopant movement from the previous processing step.

(iii) Gas Flows: To simplify the design process, the ratio of PH_3 flow rate to SiH_4 flow rate is restricted to be greater than 0.01 (PH_3 / SiH_4 >= 0.01). With this restriction, the deposition rate and resistivity of the deposited polysilicon are relatively insensitive to PH_3 and SiH_4 flow rates. As limited by the mass flow controller in the furnace, the PH_3 flow must be greater than 1 sccm*. Finally the SiH_4 flow should be greater than 100 sccm for better film coverage.

(iv) System Pressure--Since this is an LPCVD system, the operating pressure is around 300 mtorr.

* standard cubic centimeter per minute

For the inputs, to further simplify the process, we restrict the specified polysilicon thickness to be greater than 2000 Å in order to eliminate the resistivity dependence on thickness. Resistivity is restricted within the range of the empirical data which is currently from 4.6×10^{-4} to 1.3×10^{-2} Ω-cm.

Chapter 5: Functionalities of the modules and their interactions

The complete plan for the recipe generator has 6 modules: resistivity, thickness, uniformity, grain size, stress and supporting. Modules which determine the primary parameters (ref. Chapter 4) are implemented first. For example, the resistivity and thickness modules which estimate the deposition temperature/time and annealing temperature/time are implemented as the first two modules. Modules responsible for secondary parameters (ref. Chapter 4) will be implemented later as they require the values of primary parameters for fine tunings. For example, the uniformity module will determine the end zones' temperatures after the center zone temperature is determined by the resistivity and thickness modules.

The first version of the recipe generator only implemented the resistivity and thickness modules. The uniformity module will be implemented once the proposed algorithm, discussed very briefly in Ch. 10., is verified by further experiments. The supporting module will be done after the uniformity module. The grain size and stress modules will be implemented if we have appropriate equipment available to measure the grain size and stress in the polysilicon film.

The detailed functionalities of the modules are described below:

(1) Resistivity module: determines the deposition temperature, the annealing temperature and annealing time based on the specified input resistivity (or sheet resistance). The algorithm is a mixed approach employing qualitative, quantitative and empirical knowledge (see Ch. 6). The system basically estimates an initial operating range from empirical data, and then subsequently narrows the operating (search) ranges by qualitative and/or quantitative criteria.

(2) Thickness module: The deposition rate of the polysilicon process is exponentially dependent on the temperature shown below.

$$G = C \exp(\frac{-E}{RT}) \qquad (5.1)$$

where

G=film growth rate

E=activation energy

R=universal gas constant

T=temperature

C=complicated constant depending on gas flows, system geometry, etc.

Thus once the temperatures are determined from the resistivity module and the values are passed to the thickness module, the deposition rate and hence deposition time can be calculated based upon the input specified thickness. Because the pre-exponential constant C in the equation shown above depends on furnace geometry and gas flows at each location of the tube, it is hard to extract. Instead, we use the design graph "deposition rate vs deposition temperatures" (Fig. 6.4) for wafers clustering at the center zone of the tube to determine the deposition rate and hence the deposition time.

(3) Uniformity module: Because the reactants (e.g. PH_3, SiH_4, and etc.) are depleted along the tube, the thickness of the deposited polysilicon will decrease along the tube if a flat temperature profile is used for deposition. Referring to the deposition rate equation (5.1), this implies that the pre-exponential constant C decreases with distance. Hence to maintain a uniform thickness independent of wafer position, we need a temperature gradient to compensate for the depleted reactants, i.e. the temperature in the front-zone should be less than the temperature in the back-zone. The relationships of the end zone temperatures (TempL--load zone temperature, TempS--source zone temperature) and the center zone temperature (TempC) can be determined based on the prior information from the first two modules and a proposed algorithm described very briefly in Ch. 10.

(4) Grain size module: determines the recipe based on the grain size requirement. The polysilicon grain size is very sensitive to the deposition temperature. Thus the temperature gradient set up for a

uniform polysilicon thickness should be kept minimal for a lesser variation of the polysilicon grain size. Although we can use the Scanning Electron Microscopy (SEM) technique, available in our lab, to evaluate the polysilicon grain structure, we have not devised an appropriate criterion for measuring the grain size. Hence, this module is not implemented.

(5) Stress module: determines the operating parameters given the stress input specification. Since we have no appropriate equipment for evaluating the stress of a polysilicon film, the module is also not implemented.

(6) Supporting module: The recipe generated from modules (1)-(5) is far from a complete recipe, it corresponds to only the deposition step (the most critical one) of the complete equipment-independent recipe shown in Fig. 5.1.

Processing Steps	Processing Time	Temperatures / Gas Flow rates			
Unload	00:12:00	S=580C	C=640C	L=590C	N2=2000sccm
Load	00:00:00				
Pump	00:00:40			N2=100sccm	
Grosscheck	00:01:00				
TempRecover	00:05:00	S=610C	C=550C	L=560C	
TempRamp	00:10:00	S=636C	C=630C	L=624C	
TempRamp	00:08:00	S=656C	C=650C	L=644C	
TempStab	00:02:00				
TempCheck					
Pump	00:02:00				
LeakCheck	00:01:00				
Purge	00:01:00			N2=200sccm	
Pump	00:01:00				
Phosphine	00:01:00			PH3=1sccm	
SiH4	00:01:00			SiH4=120sccm	
Deposit	xx:xx:xx				
TempCal	00:00:10				
Pump	00:01:00				
Purge	00:07:00			N2=100sccm	
Backfill	00:07:00			N2=5000sccm	

Fig. 5.1 An intermediate equipment-independent recipe for LPCVD in-situ doped polysilicon

This is because before executing the deposition step, the furnace has to be set up, such as unload the tube, load the wafers, pump to the specific pressure, ramp temperature to the designated deposition temperature, purge (pump with N_2), turn on the amount of gases required, etc. Hence the recipe generated from modules (1)-(5) have to be properly linked with all the pre-run and post-run commands by the supporting module. Note that the supporting module will generate an equipment-independent recipe using the predefined process primitives for the LPCVD process (shown in Fig. 5.1). Thus the final complete equipment-independent recipe should be portable among similar manufacturing environments, at the cost of translation and compilation to match the characteristics of specific equipment. The recipe supporting module is designed with an open architecture in mind so that it can also link together other "partial" recipes with pre-run and post-run set ups for LPCVD processes such as the undoped polysilicon deposition, the LTO undoped deposition, the nitride and the PSG processes (40 wt% and 80 wt%), etc. With additional work, the supporting module can be generalized for other furnace operations as well such as oxidation, annealing, epitaxy, etc.

Chapter 6: A mixed knowledge base

The LPCVD in-situ doped polysilicon deposition process is not well-understood. It is difficult to derive a recipe for the polysilicon process solely from quantitative first principles. Hence various sources of knowledge are needed to design a polysilicon deposition process. The recipe generator employs empirical knowledge (e.g., information about local machine behavior), qualitative knowledge (e.g., the qualitative requirements on surface morphology, process throughput, dopant movement) and quantitative knowledge (e.g., the use of equations/simulations to compute numerical values needed for reasoning).

6.1 Empirical knowledge

Empirical experimental data, in terms of design graphs (e.g. Fig. 6.2-6.4), expresses the knowledge of local machine behavior for a specific manufacturing environment. Empirical knowledge is one of the principal basises for the design of IC processes, such as a LPCVD doped polysilicon process, where accurate physical models are not available.

We have performed experiments to generate the necessary design graphs required for the generation of polysilicon recipes. Twelve wafers were split into 4 sets of wafers and then polysilicon was deposited on them at 4 different deposition temperatures (TG). These wafers were then subsequently annealed at 3 different annealing temperatures (TA). The experiments are summarized in Fig. 6.1.

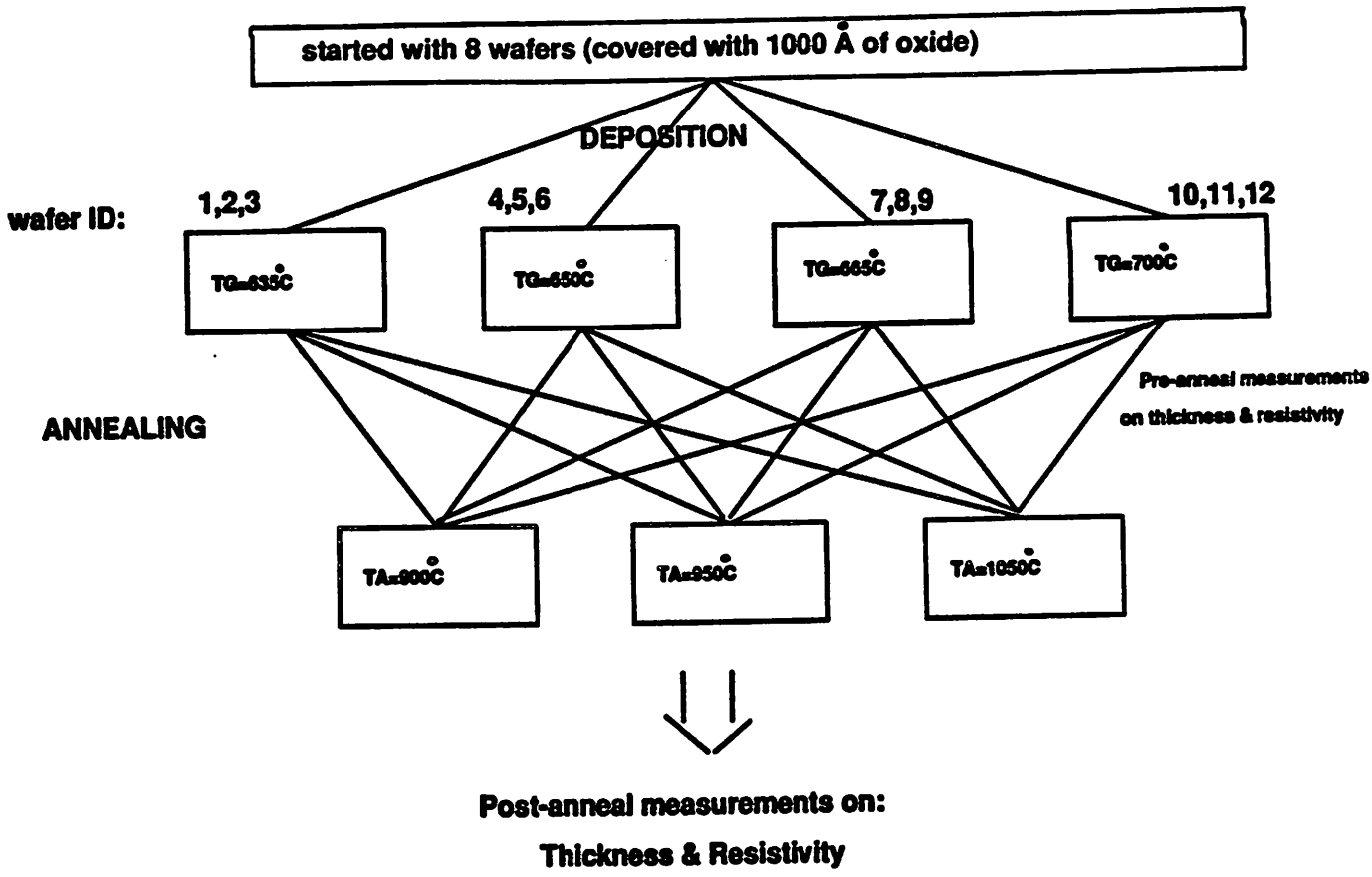


Fig. 6.1 Experiments performed to generate the empirical design graphs

Different design graphs are generated from the above experiments. The most important ones are shown below in Fig. 6.2 to Fig. 6.4. A representation of this same data in a LISP list format is shown in Fig. 6.5.

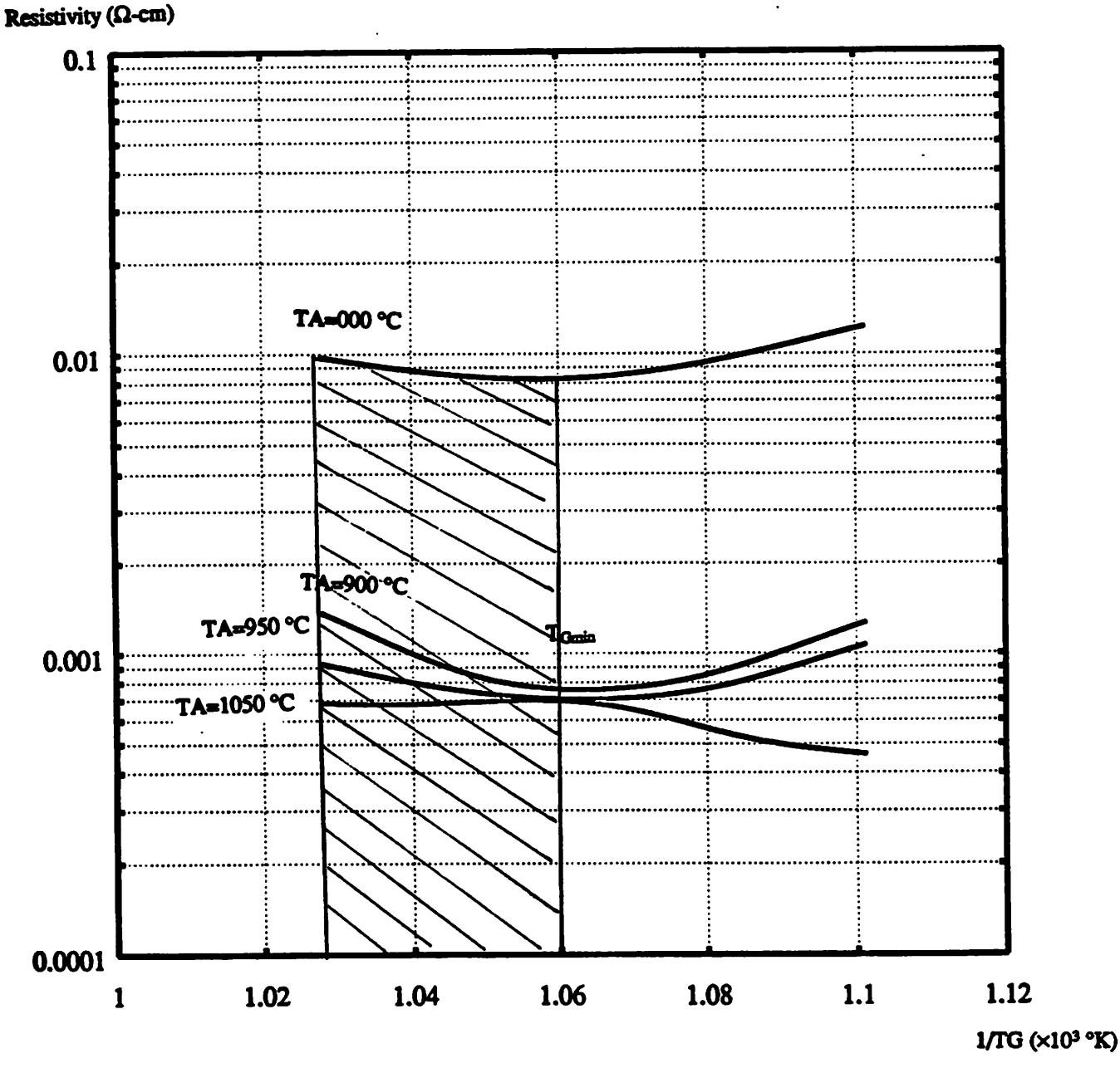


Fig. 6.2 Resistivity (Ω-cm log scale) vs $\frac{1}{TG}$ [10^3 °K^{-1}] at different TA [0 to 1050 °C] with operating range confined to the shaded region.

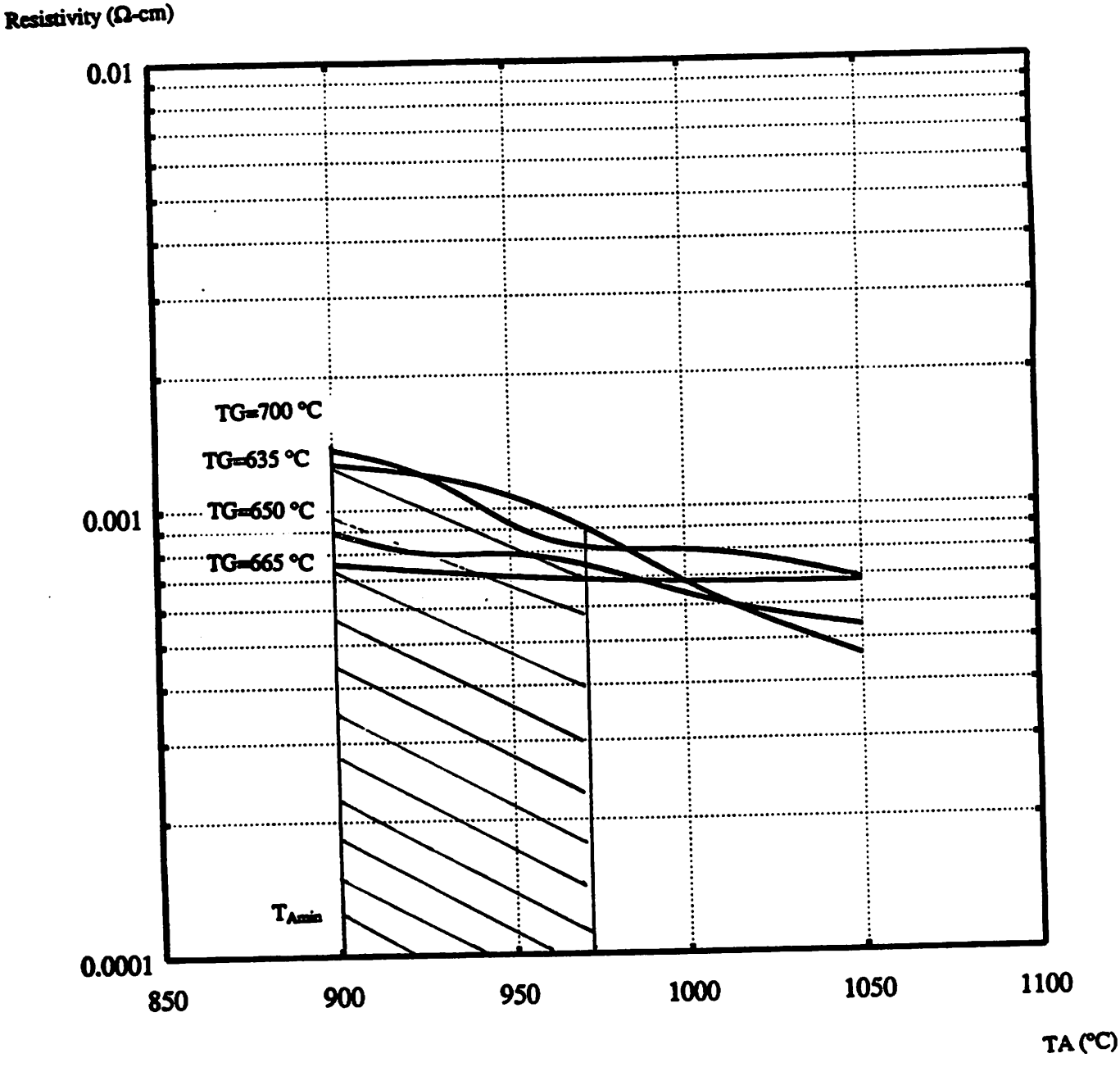


Fig. 6.3 Resistivity (Ω-cm log scale) vs TA [°C] at different TG [635 to 700 °C] with operating range confined to the shaded region.

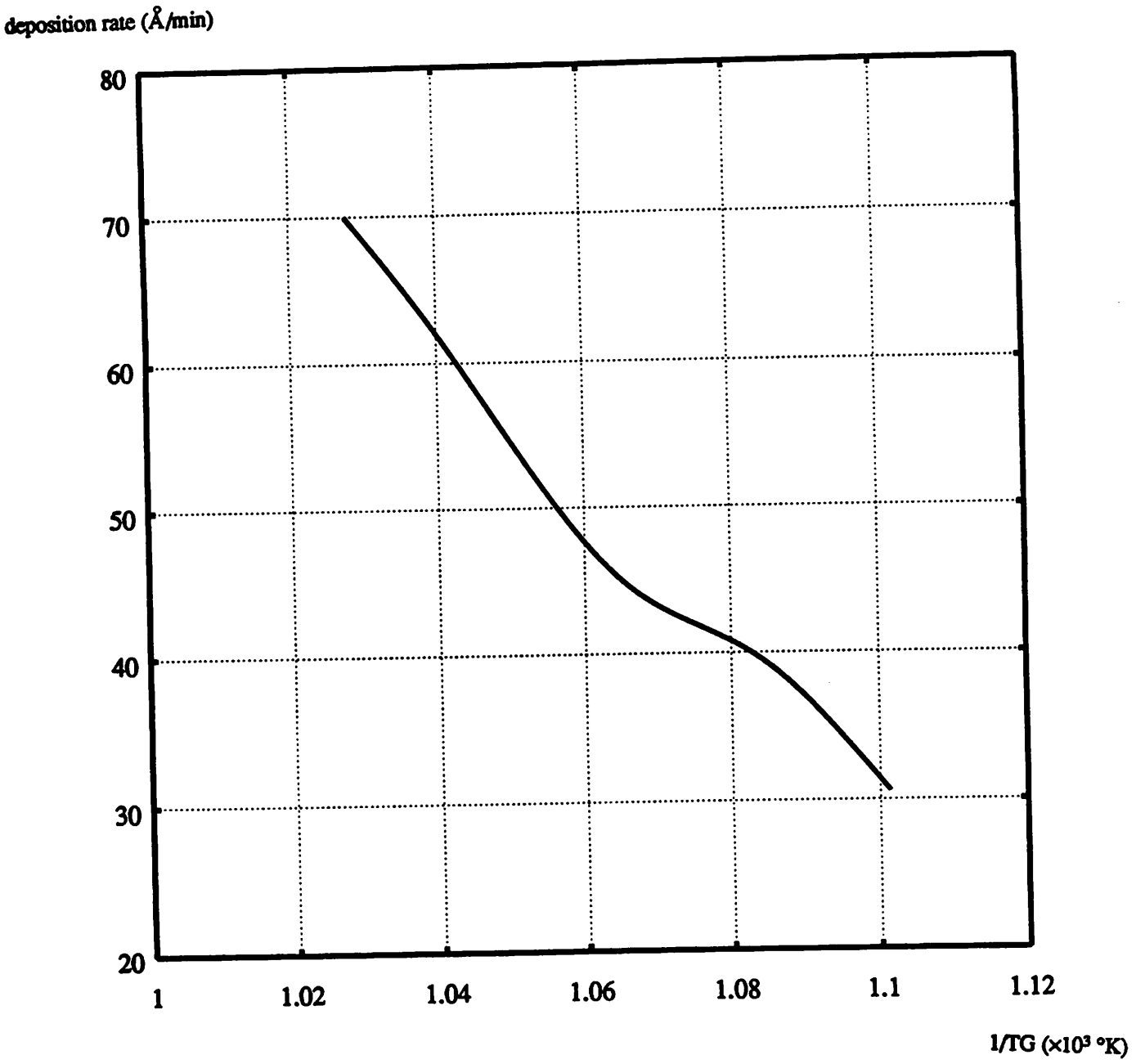


Fig. 6.4 Deposition rate [Å/min log scale] vs $\frac{1}{TG}$ [10^3 °K^{-1}]

```
(deffacts res-vs-TG-family
   (res-vs-TG 800.0 (1.10133e-3 -4.3982) (1.0834e-3 -4.6356) (1.066098e-3 -4.783
69)
                    (1.04e-3 -4.73300) (1.02774e-3 -4.63049))
   (res-vs-TG 900.0 (1.10133e-3 -6.6687) (1.0834e-3 -7.0209) (1.066097e-3 -7.182
19)
                    (1.04e-3 -6.90776) (1.02774e-3 -6.5929))
   (res-vs-TG 925.0 (1.10133e-3 -6.8124) (1.0834e-3 -7.0703) (1.066098e-3 -7.208
7)
                    (1.04e-3 -7.0243) (1.02774e-3 -6.8034))
   (res-vs-TG 950.0 (1.10133e-3 -6.8401) (1.0834e-3 -7.1397) (1.066099e-3 -7.255
9)
                    (1.04e-3 -7.1309) (1.02774e-3 -6.9836))
   (res-vs-TG 1050.0 (1.10133e-3 -7.68211) (1.0834e-3 -7.53138) (1.066098e-3 -7.
30228)
                     (1.04e-3 -7.29342) (1.02774e-3 -7.28755))
)

(deffacts res-vs-TA-family
   (res-vs-TA 635.0 (1050.0 -7.68211) (1000.0 -7.29342) (950.0 -6.84009)
                    (925.0 -6.72543) (900.0 -6.66874))
   (res-vs-TA 650.0 (1050.0 -7.531) (1000.0 -7.35404) (950.0 -7.13969)
                    (925.0 -7.13099) (900.0 -7.02092))
   (res-vs-TA 665.0 (1050.0 -7.30228) (1000.0 -7.293420) (950.0 -7.25589)
                    (925.0 -7.22247) (900.0 -7.18219))
   (res-vs-TA 682.5 (1050.0 -7.38579) (1000.0 -7.29342) (950.0 -7.19544)
                    (925.0 -7.05858) (900.0 -6.90776))
   (res-vs-TA 700.0 (1050.0 -7.28755) (1000.0 -7.13089) (950.0 -6.98356)
                    (925.0 -6.7254) (900.0 -6.59294))
)


(deffacts dep-rate-curve
   (dep-rate-vs-TG 0.0 (1.10133e-3 3.421) (1.0834e-3 3.684) (1.066098e-3 3.798)
                       (1.04e-3 4.127) (1.02774e-3 4.248))
```

Fig. 6.5 Experimental data in Lisp format

General functions to perform 2D and 3D interpolations, in addition to simple table-lookup routines, are implemented to manipulate any general empirical data. The following ART rules (Fig. 6.6) will interpolate x values for any general (single or multi-valued) curves given the y value. Currently a linear interpolation algorithm is used but will be upgraded to a spline interpolation algorithm in the near future.

```
(defrule interpolate-x-2
    (declare (salience 6))
    (viewpoint @?vp
       (find x ?graph-name ?y ?z)
       (not (?graph-name ?z $? (? ?y) $?))
       (?graph-name ?z  $? (?x2 ?y2) (?x1 ?y1) $?)
       (not (probed-x ?graph-name ?z ($? ?x2 ?x1 $?)))
       ?f-1 <- (probed-x ?graph-name ?z ($?probed-x))
       ?f-2 <- (x-list ?graph-name ?z ($?x-list))
    )
   (or (and (test (> ?y1 ?y))
            (test (> ?y ?y2)))
       (and (test (> ?y ?y1))
            (test (> ?y2 ?y)))
   )

=>
    (at ?vp
      (bind ?slope (quotient (- ?x1 ?x2) (- ?y1 ?y2)))
      (bind ?x (?x1 + (?slope * (?y - ?y1))))
      (retract ?f-1)
      (assert (probed-x ?graph-name ?z ($?probed-x ?x2 ?x1)))
      (retract ?f-2)
      (assert (x-list ?graph-name ?z ($?x-list ?x)))
    )
)
```

Fig. 6.6 An interpolation rule

6.2 Qualitative knowledge

Some of the important qualitative input parameters for polysilicon deposition are: process time, minimum substrate dopant movement, film morphology, polysilicon grain size and film stress. Only *process time, film morphology and minimum substrate movement* are used as the current subset of qualitative parameters. Currently the specification of the qualitative input parameters is mandatory for an output recipe. However the specification will be made optional in the future for those who want only a default recipe.

By specifying the priorities on the requirements of the above-mentioned parameters (Fig. 6.7), qualitative knowledge is used to guide the recipe generator to

(1) choose the appropriate design path/submodule

(2) use the correct design graph(s) within each chosen path/submodule

(3) reduce the search space for recipes.

For example (see Fig. 6.2), when "film morphology" (i.e. grain size) is selected as the first priority, recipes will have $T_G <= T_{Gmin}$*. When "minimum process time" is selected as first priority, the recipes will have $T_G >= T_{Gmin}$*. Ranges of T_A will also be further restricted by user-specified maximum tolerable substrate movement when the substrate dopant movement is the biggest concern* (see Fig. 6.3). [T_G =deposition temperature, T_A=annealing temperatures]

* T_{Gmin} (see Fig. 6.2) is the deposition temperature at which the resistivity is minimum. It is chosen as the separating boundary for two different deposition regions, $T_G > T_{Gmin}$ and $T_G < T_{Gmin}$.

* T_{Amin} (see Fig. 6.3) is the minimum annealing temperature for minimum dopant movement.

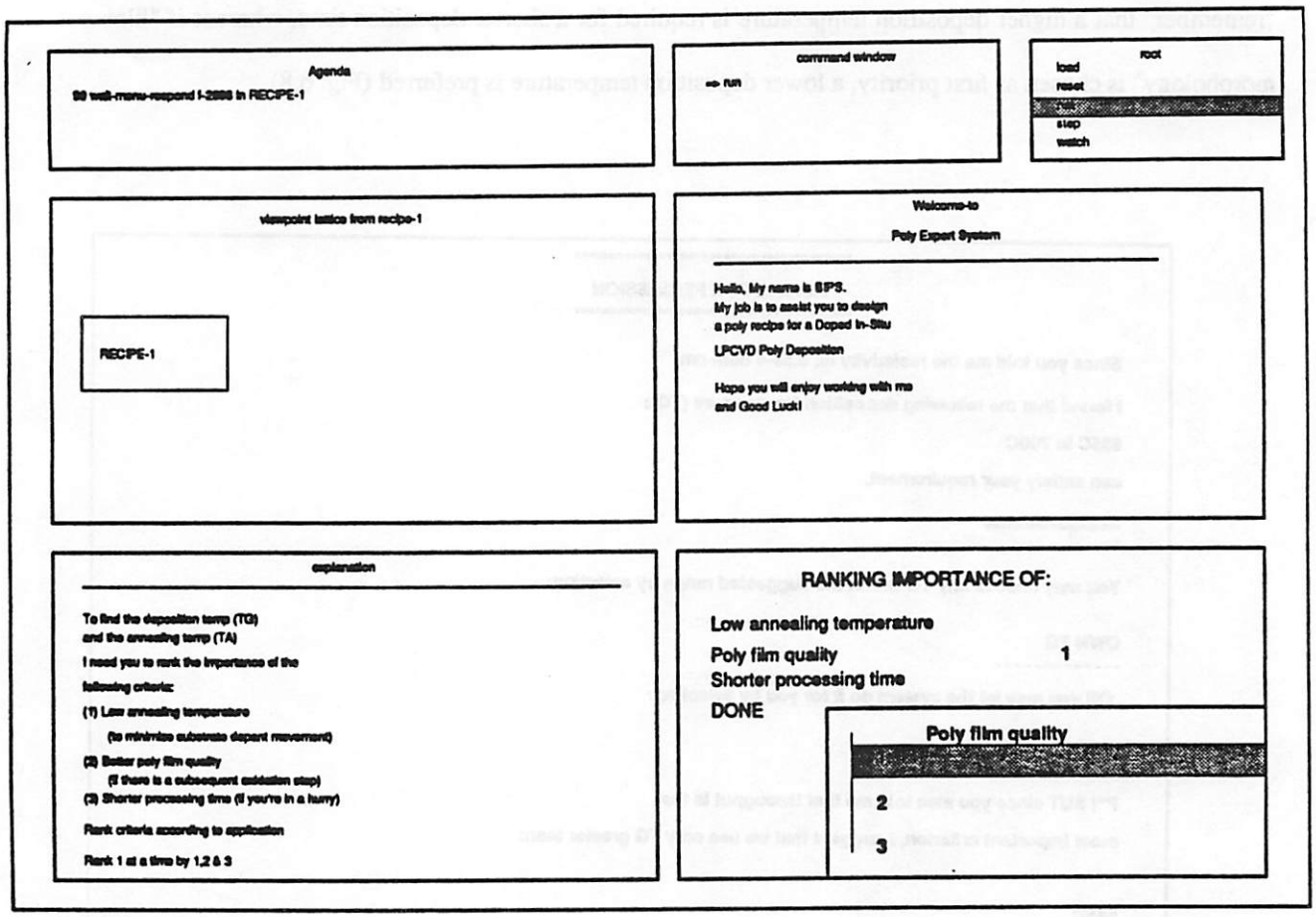


Fig. 6.7 Qualitative specifications

Also, subsequent submodules responsible for determining the process variables will always "remember" that a higher deposition temperature is required for a shorter deposition time, whereas if "film morphology" is chosen as first priority, a lower deposition temperature is preferred (Fig. 6.8).

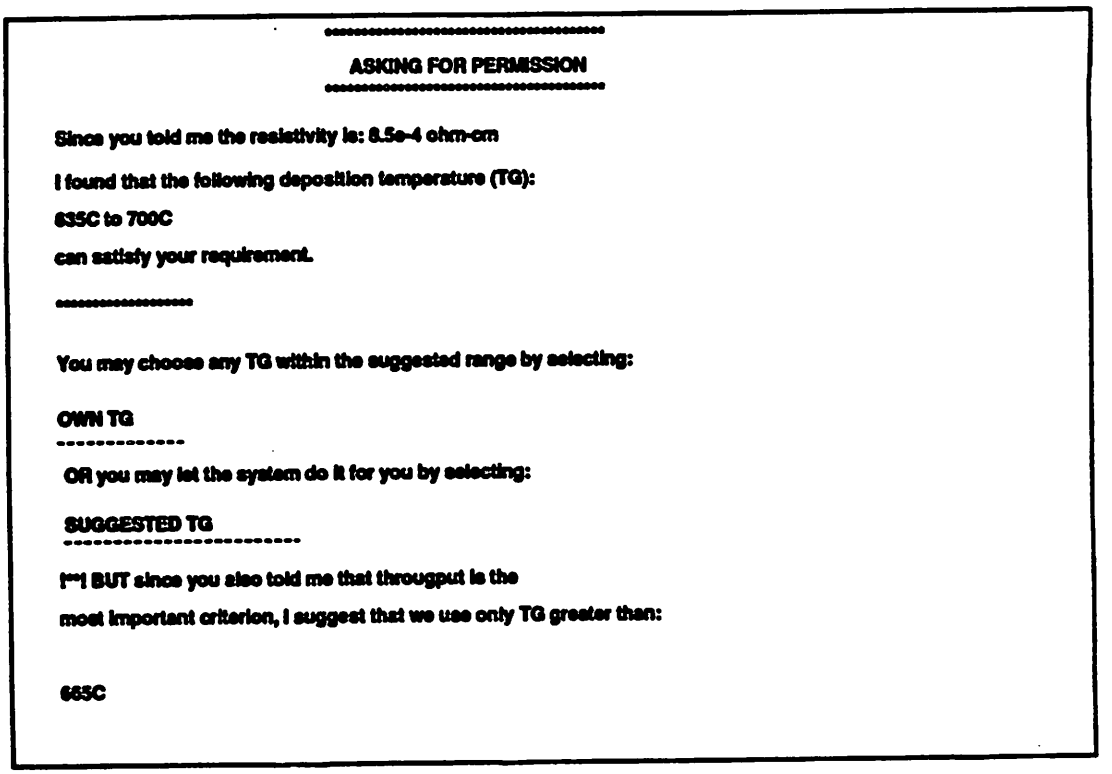


Fig. 6.8 Trimming of operating range

6.3 Quantitative knowledge

Numerical values derived from accurate physical models can provide useful information during the design. With this in mind, the recipe generator was designed with the capability to incorporate numerical equations and for a future interface to simulation tools like SUPREM.

An example of the use of quantitative knowledge is when "minimum substrate dopant movement" is specified as the first priority. In order to specify a reduced operating range for the annealing temperature, which has the biggest influence on dopant movement, the system has to know the dopant type and the maximum allowed dopant movement (measured in microns). To do this, the system uses the diffusion coefficient equation (which determines the diffusion constant at different temperatures using Do [frequency factor] and E [activation energy]),

$$D = D_o e^{\frac{-E}{kT}} \tag{6.1}$$

and the simple diffusion equation (which gives an estimate of the drift of dopant given the diffusion constant D and time t).

$$x_{diffused} = 2\sqrt{Dt} \tag{6.2}$$

These simple equations are used to demonstrate the usefulness of a mixed knowledge base. More sophisticated and accurate models (such as the Fick's diffusion equations), and/or simulation can be used to obtain more accurate results.

6.4 Partition of knowledge base in recipe generator

The recipe generator partitions the three different types of knowledge into different text files so that they can be modified and compiled separately without affecting others. An example is the experimental data shown in Fig. 6.5 (in Lisp format) can be easily replaced by individual local data at different manufacturing facilities.

Chapter 7: Hypothetical generation of recipes

Different *discrete* possible scenarios are hypothesized from the *infinite and continuous* solution space based on a logarithmic algorithm, resulting in a dynamic *discretization* of the solution space. More hypothetical solutions are generated in the rapidly varying regions and less in the slowly varying regions as a consequence of this dynamic discretization. Final recipes are optimized through user feedback [10]. Fig. 7.1 shows that 4 different possible recipes (recipe 2-5) are generated from the root recipe (recipe 1). Contents of any recipes can be viewed by an expanding command.

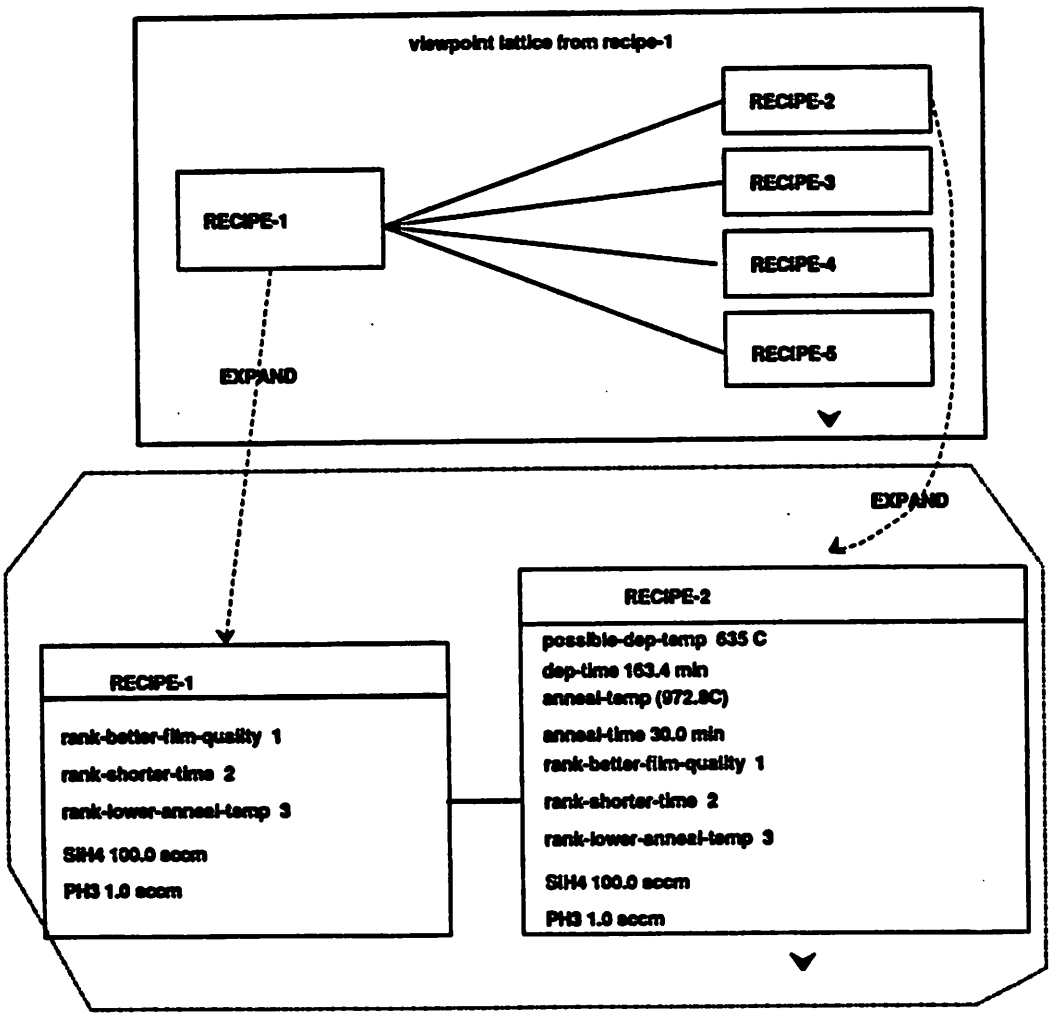


Fig. 7.1 Hypothetical generation of possible polysilicon recipes

7.1. An infinite and continuous solution space

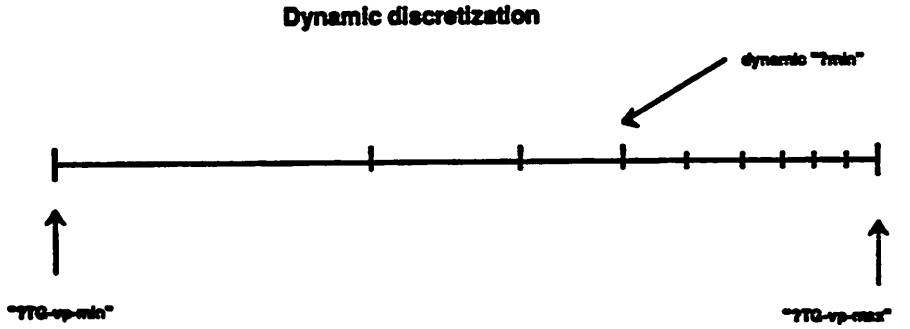
Due to the number of design parameters involved, there are an infinite number of non-random combinations of the design parameters that can satisfy a given set of input specifications. Our strategy is to seek a smaller solution space from the infinite search space by prior classification of the operating parameters and by limiting our consideration to more practical and well-behaved operating regions (Ch. 4), by modular design (Ch. 5), and by qualitative criteria specifications (Ch. 6). However, the final confined solution space (see Fig. 6.2-6.4), being intrinsically continuous and real-numbered in nature, still contains an infinite number of possible solutions. For example in Fig. 6.2, we know that if resistivity is specified at 8.5×10^{-4} Ω-cm, and if process time has the highest priority during the design, the deposition temperature (TG) will be confined to any value between 665 and 700 °C. Each deposition temperature will have a corresponding deposition time, annealing temperature (TA), etc., to form an infinite number of recipes within that operating range. Thus, we need to devise an algorithm to limit and discretize the solution space without sacrificing useful information.

7.2. The discretization algorithm

The discretization algorithm, by definition, will *extract* finite sets of solutions from the infinite solution space. The algorithm we devised has the following capabilities,

(i) Selection of key parameter to discretize--The choice of the key parameter (e.g. TG or TA) to be discretized, with other parameters (such as deposition time, annealing temperature, etc.) to be derived from the key parameter, depends on the qualitative priorities described. The choice of "film morphology"/"process time" as first priority will have TG discretized, while the choice of "minimum-dopant-movement" as first priority will have TA discretized (TG=deposition temperature, TA=annealing temperature).

(ii) Dynamic discretization--Because the initial infinite and continuous solution space is logarithm based, the algorithm will produce more solutions at the rapidly-varying regions and less in the slowly-varying regions. For example in the rule "TG-vp-seq-generator" (Fig. 7.2) that discretizes the deposition temperature (TG) when processing time is stated as first priority, a recipe is generated at an interval of 0.4*(?TG-vp-max - ?min) starting from ?TG-vp-min. The Lisp variable "?TG-vp-max(min)" is the maximum (minimum) temperature in the confined solution space. The variable "?min", which is dynamically changing it's value, is the maximum of the Lisp list "TG-vp-seq" which is also dynamically appended by the lastest value of "?min". A pictorial explanation is shown below,




```
(defrule TG-vp-seq-generator-1-proc-time
    (declare (salience 0))
    (rank shorter-proc-time 1)
    (find TG-vp-seq)
    ?f-1 <- (TG-vp-seq $?TG-seq ?min)
    (TG-vp-max ?TG-vp-max)
    (test (> (- ?TG-vp-max ?min) 5.0))
=>
    (bind ?next-min (+ ?min (* 0.4 (- ?TG-vp-max ?min))))
    (assert (TG-vp-seq $?TG-seq ?min ?next-min))
    (retract ?f-1)
)

(defrule TG-vp-seq-generator-2-proc-time
    (declare (salience 0))
    (rank shorter-proc-time 1)
    ?f-1 <- (find TG-vp-seq)
    ?f-2 <- (TG-vp-seq $?TG-seq ?min)
    (TG-vp-max ?TG-vp-max)
    (test (< (- ?TG-vp-max ?min) 5.0))
=>
    (bind ?next-min (+ ?min (* 0.6 (- ?TG-vp-max ?min))))
    (assert (TG-vp-seq $?TG-seq ?min ?next-min ?TG-vp-max))
    (retract ?f-1 ?f-2)
)
```

Fig. 7.2 Rules for dynamic discretization

The consequence is that more solutions are generated in the higher temperature region (a more rapidly varying zone in log-scale, refer to Fig. 6.2-6.4) than the lower temperature region (less varying zone). The dynamic discretization scaling factor 0.4 is currently static and somewhat arbitrary (to be explained in (iii) below).

(iii) Synthesis of practically distinct solutions-- discretized solutions should have sufficiently separated values to produce practically distinct end results. For example, recipes with deposition temperatures differing by 5 °C will essentially produce the same measurements, but not for a difference greater than 5 °C (a 10 °C difference is need for annealing). These rules of thumb are reflected in the rules shown in Fig. 7.2. The dynamic discretization scaling factor is also fine tuned to 0.4 to ensure sufficiently separated values for each discretized solution.

(iv) Retention of vital information-- the algorithm inherits all the vital information (design history) of the initial solution space via the ART internal programming capability to handle hypothetical reasoning (see section 7.3).

7.3. Generation of discrete recipes via ART programming capabilities

ART can reason about hypothetical situations, such as possible future moves in a game of chess. It can do this by constructing a branching tree of viewpoints, each node of which would represent an assumption about the next move to make. When reasoning within one of these viewpoints, ART would be able to "see" all the assumptions leading to that specific situation. Other assumptions, leading to other situations, would be invisible to it. ART would operate only on the facts and assumptions pertinent to that "hypothetical world."

A viewpoint in ART is defined as a way to store facts about different situations in such a way that ART will not accidentally mix facts from one situation with facts from another [10].

The simplest internal ART commands for generating "children" viewpoints from "parent" viewpoint are "sprout" or "hypothesize" through a "defrule" statement (i.e. a rule). The commands enable the "children" viewpoints to inherit all of the properties (e.g. the design history) of its "parent" viewpoint. The "children" viewpoint however can have its own properties different from the "root" viewpoint. The following rule "generate-TG-viewpoint" (Fig. 7.3) generates hypothetical worlds for each of the discrete TG (key/indexing parameter) stored in the Lisp list "TG-vp-seq", which is derived from the discretization algorithm. Other parameters needed to form a complete recipe, such as deposition time, annealing temperature, etc., will be derived in each of the hypothetical "children" viewpoint.

```
(defrule generate-TG-viewpoint
    (declare (salience 0))
    (or (rank better-film-quality 1)
        (rank shorter-proc-time 1))
    (not (find TG-vp-seq))
    (TG-vp-seq $?TG-vp-seq)
=>
    (for choice in$ ?TG-vp-seq do
        (hypothesize
            (assert (possible-TG =choice))
        )
    )
)
```

Fig. 7.3 Rule for generating viewpoints

We use "hypothesize" instead of "sprout" because "hypothesize" has more "knowledge maintenance" capabilities to avoid storing duplicate and/or contradictory facts in any individual viewpoint (refer to [10] for more details). Also the "hypothesize" command is more flexible for future reasoning with generated hypothetical viewpoints, such as optimization of the recommended recipes. Future implementation of an explanation facility for the actions taken by the system also depends upon the inheritance links between the "parent" and "children" viewpoints. The "hypothesize" command is believed to be more flexible and reliable than the simple "sprout" command.

7.4. Optimization of the generated recipes

The recipe generator will automatically compute and present the best system-proposed recipe to the user, based upon the qualitative criteria (Fig. 7.4). As usual, the recipe with the lowest TG will be chosen as the default optimal recipe if "film quality" is most crucial (vice versa if "process time" is critical). Default optimization of recipes with "minimal substrate dopant movement" is somewhat different--instead of chosing the recipe with the lowest TA (which gives least dopant movement), the optimization depends on the second most important qualitative criterion ("film quality" or "process time") because all the annealing temperatures (i.e. the TAs) in the hypothetical recipes satisfy the user specified minimum dopant movement (see section 6.3). Thus, with "film quality" as the second criterion, the recipe with the lowest TG is selected (vice versa if "process time" is the second criterion).

Users are free to reject a system-recommended recipe. They can single out the parameters for modifications (e.g. TG, TA, deposition time (tG), gas flows, etc.) and ask the system to provide recipes (if any) which satisfy altered constraints. An example (Fig. 7.5) is that a user may want recipes with deposition time less that the recommended 163 minutes despite the utmost criteria is "film quality" (perhaps he has a date!). The system will search through all the viewpoints with deposition time less than 150 minutes (user specified) and then let the user select a final recipe.

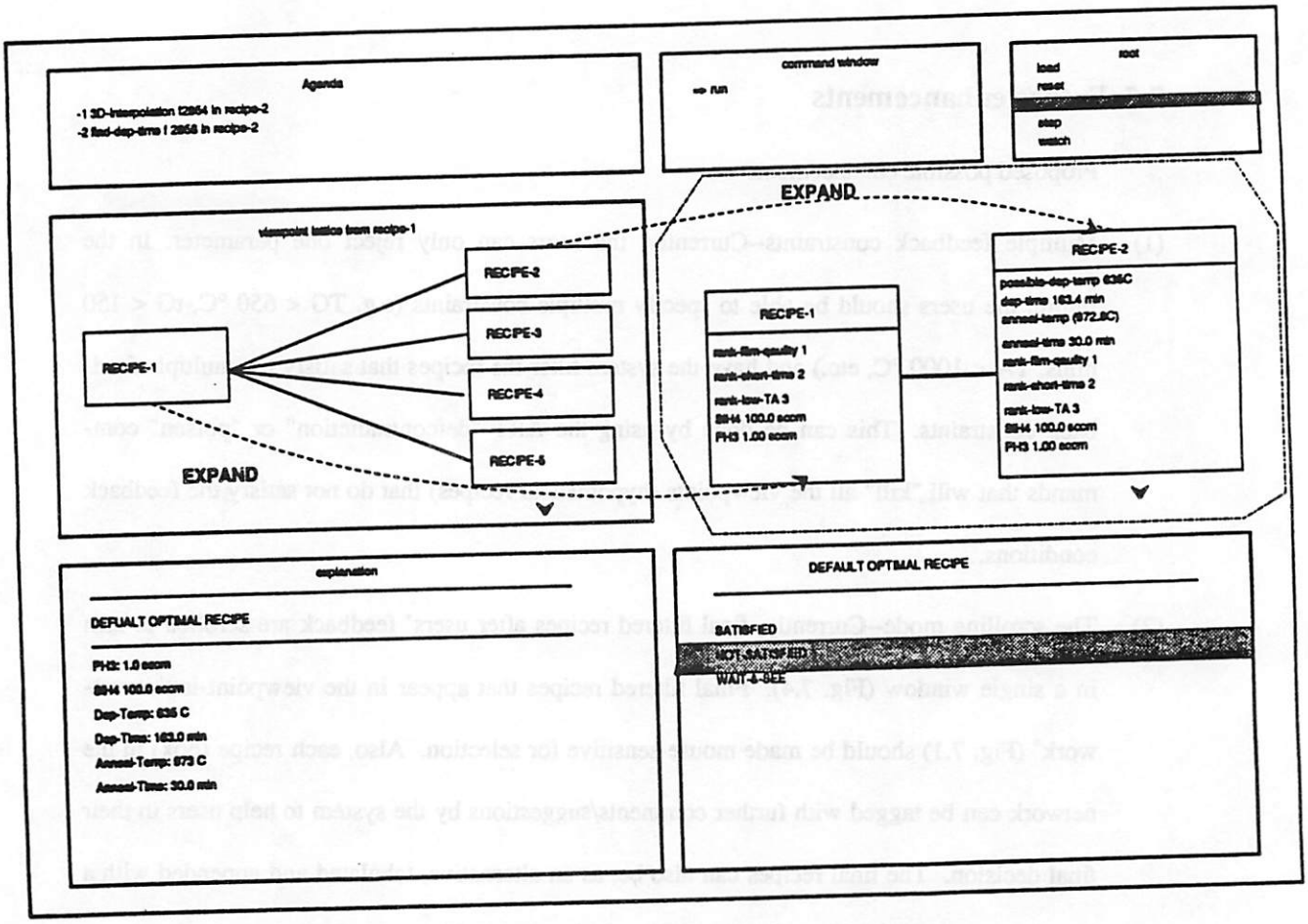


Fig. 7.4 System recommending default optimal recipe

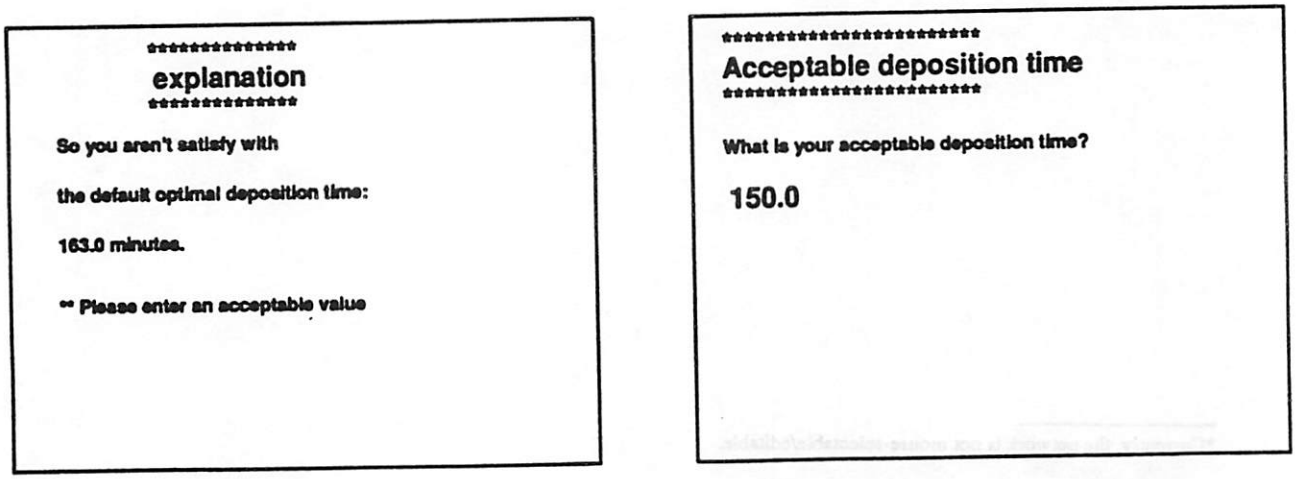


Fig. 7.5 User reaction to the default optimal parameters

7.5. Future enhancements

Proposed possible enhancements are:

(1) Multiple feedback constraints--Currently, the users can only reject one parameter. In the future, the users should be able to specify multiple constraints (e.g. TG < 650 °C, tG < 150 mins, TA < 1000 °C, etc.) and have the system filter the recipes that satisfy the multiple feedback constraints. This can be done by using the ART "defcontradiction" or "poison" commands that will "kill" all the viewpoints (hypothetical recipes) that do not satisfy the feedback conditions.

(2) The scrolling mode--Currently, final filtered recipes after users' feedback are scrolled in-turn in a single window (Fig. 7.4). Final filtered recipes that appear in the viewpoint-lattice network* (Fig. 7.1) should be made mouse-sensitive for selection. Also, each recipe (box) in the network can be tagged with further comments/suggestions by the system to help users in their final decision. The final recipes can also be, as an alternative, tabulated and appended with a "merit factor" for selection. The "merit factor" is generated by system to help users to select a final recipe.

*Currently, the network is not mouse-selectable/editable.

Chapter 8: The system interfaces: user-interface and equipment interface

8.1 The user interface

Traditional keyboard entries are very inconvenient and vulnerable to errors for IC processing personnel wearing protective hand gloves. Nevertheless, process personnel need frequent interaction with the computers for information processing. Thus a good user interface should present the user maximum information with minimum input effort. As a result, most of the user interactions in BIPS are via a pointing device (mouse), which is believed to be less vulnerable to errors than keyboard entries in an IC manufacturing environment. Voice input* will also be considered in future work [11].

BIPS summarizes and condenses useful information in bit-mapped graphical displays and menus. The window system of the user interface is designed with a hierarchical information display (e.g. pop-up menu) to prevent overloading users with excessive information. Also the system should not display only one set of predetermined information but should be flexible to accommodate wider sets of information under users' guidance.

* Note that the voice-input has not yet been implemented. Although the voice-input is technically more attractive, it might generate more contamination particles through the utterance of the processing personnel.

Figures 8.1-8.3 shows some examples of the current user interface.

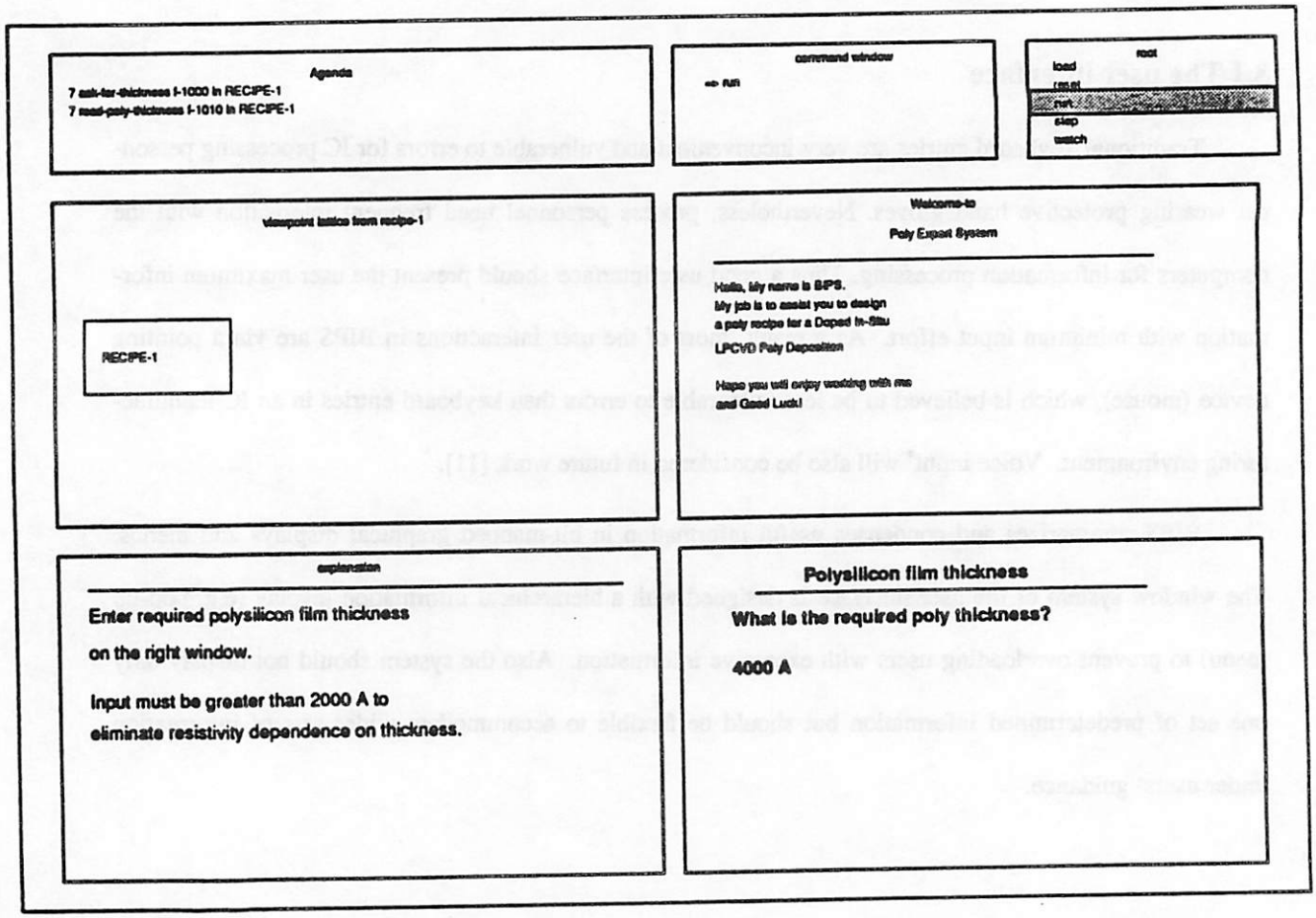


Fig. 8.1 Screen layout and keyboard input for polysilicon thickness

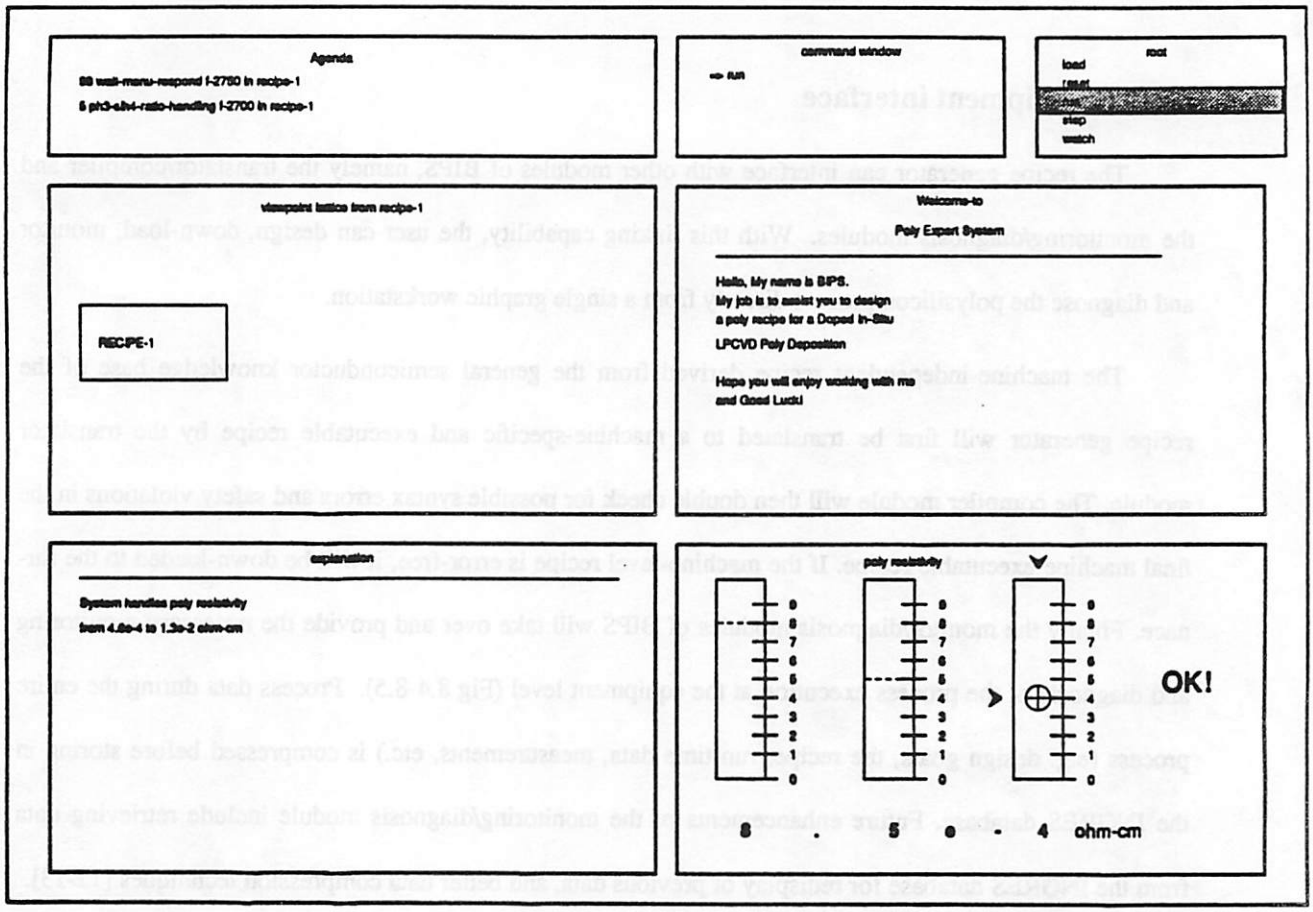


Fig. 8.2 Input interface for polysilicon resistivity

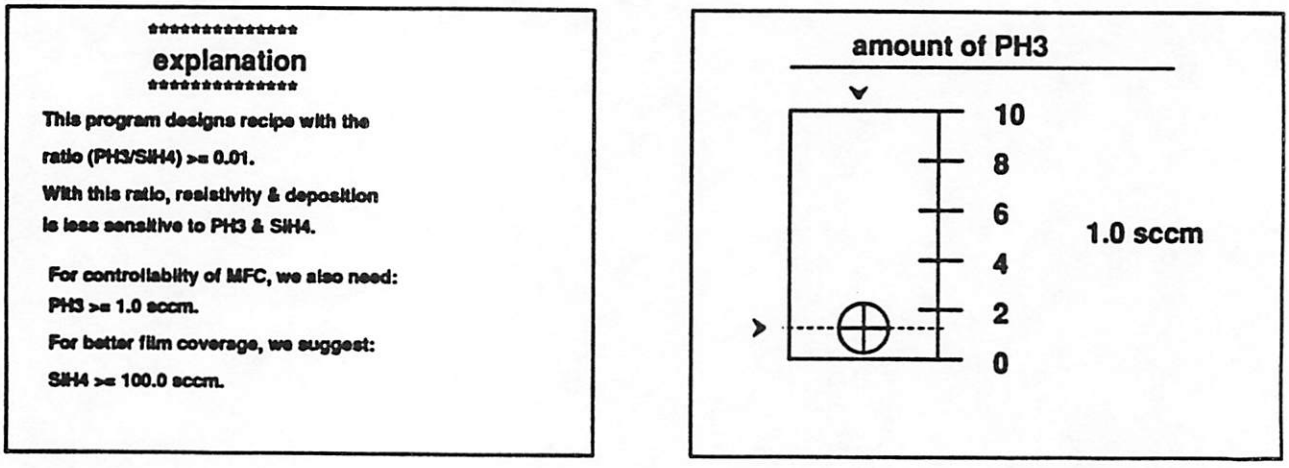


Fig. 8.3 Input interface for PH_3

8.2 The equipment interface

The recipe generator can interface with other modules of BIPS, namely the translator/compiler and the monitoring/diagnosis modules. With this linking capability, the user can design, down-load, monitor and diagnose the polysilicon process directly from a single graphic workstation.

The machine-independent recipe derived from the general semiconductor knowledge base of the recipe generator will first be translated to a machine-specific and executable recipe by the translator module. The compiler module will then double check for possible syntax errors and safety violations in the final machine executable recipe. If the machine-level recipe is error-free, it will be down-loaded to the furnace. Finally the monitor/diagnosis modules of BIPS will take over and provide the necessary monitoring and diagnosis of the process execution at the equipment level (Fig 8.4-8.5). Process data during the entire process (e.g. design goals, the recipe, run-time data, measurements, etc.) is compressed before storing in the INGRES database. Future enhancements of the monitoring/diagnosis module include retrieving data from the INGRES database for redisplay of previous data, and better data compression techniques [12-13].

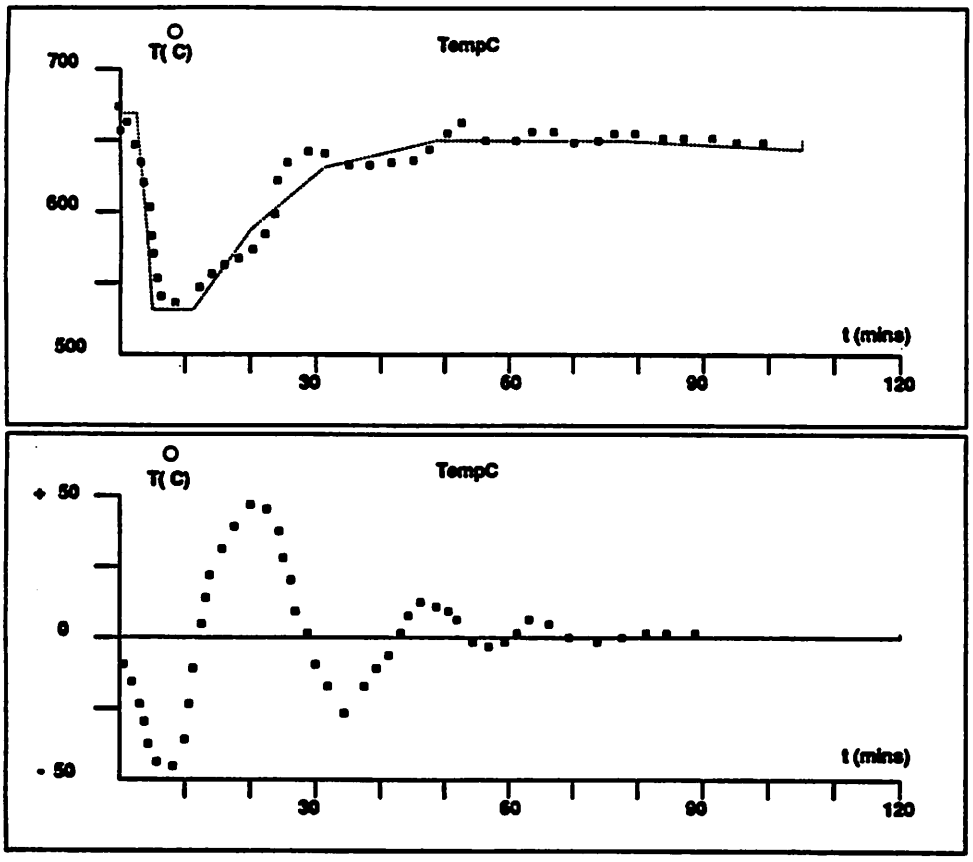


Fig. 8.4 An interface window for the monitoring module

Diagnostic Window

PROBLEM:

Step 45

Inconsistent temperature readings from the two independent circuits for the source zone

DIAGNOSIS:

Temperature calibration error.

RECOMMENDATION:

Re-calibrate temperature monitoring circuits for the source zone.

Fig. 8.5 An interface window for the diagnosis module

PART III: The System Status

Chapter 9: Preliminary evaluation of the recipe generator

9.1 Experimental results

Wafers have been processed in our laboratory according to several recipes developed by the preliminary version of BIPS, which contains *only* the resistivity and thickness submodules. Measured parameters, taken from wafers deposited at the center-zone of the furnace and averaged over 5 distinct locations on each of the wafers, are in reasonable agreement with the initial goals (Table 1). Recipes should improve after the uniformity module is implemented. Recipes derived from the same input thickness and resistivity may have deposition times differing by a factor of 2 (recipe 1 & 2), depending on the priorities chosen during the design. Annealing temperatures from different recipes, targeted for the same input specifications, can differ by as much as 70 °C (recipe 3 & 4). The results suggest that through the recipe generator one may design processes with higher throughput and/or lower processing temperatures, as may be desirable for VLSI production.

Target:		
Resistivity =	7.3×10^{-4} ohm-cm	
Thickness =	4000 Å	
Recipes Generated:	**1**	**2**
Deposition Temp =	635 °C	676 °C
Deposition Time =	130 mins	77 mins
Annealing Temp =	995 °C	950 °C
Annealing Time =	30 mins	30 mins
Measurements:		
Resistivity =	6.5×10^{-4} ohm-cm	7.23×10^{-4} ohm-cm
Thickness =	4850 Å	2570 Å

Target:		
Resistivity =	8.9×10 ohm-cm	
Thickness =	2000 Å	
Recipes Generated:	**3**	**4**
Deposition Temp =	635 °C	650 °C
Deposition Time =	65 mins	50 mins
Annealing Temp =	970 °C	900 °C
Annealing Time =	30 mins	30 mins
Measurements:		
Resistivity =	6.7×10^{-4} ohm-cm	8.36×10^{-4} ohm-cm
Thickness =	2020 Å	1480 Å

TABLE 1: Experimental Results– Wafers are processed at center zone of furnace.
Results are averages of 5 readings from different locations on each wafer.

9.2 Computer time

With complete graphical interface turned on (i.e. when the viewpoint-lattice network and the agenda* are on), the system can generate recipes within 3 to 5 minutes. With viewpoint network and "agenda" turned off, recipes can be designed within a minute. The time to generate a recipe is much faster than a typical lab user in our lab.

9.3 Other observations

The system is capable of handling a larger design matrix, which is usually very difficult to be acquire and handle by a single typical process personnel. Valuable experience has been gained from the implementation of BIPS system and this experience will be helpful for future enhancements of the current modules, for implementation of other modules, and for other systems.

* "Agenda" is a specific window showing the rule firings during the execution of the program.

Chapter 10: Future plans--a system level overview

10.1 Implementing uniformity and supporting modules.

The knowledge base of the preliminary version of the recipe generator was based partly on the empirical measurements on two 4" wafers. These wafers were clustered at the center zone of the 3 zone Tylan furnace used in our lab, with 48 wafers acting as dummy wafers.

The preliminary experimental results based on the recipes generated indicate that the resistivity is within an average of 10% of the targeted value. The thickness has a greater average deviation of around 20 to 30% from the targeted value. The disagreement between the designed recipes and experimental results, we speculate, is due to the depletion of gas reactants (e.g. SiH_4, PH_3, etc.) along the furnace tube, which we currently have not yet taken into account (see Ch. 9 for experimental results).

In a real manufacturing environment, the LPCVD process is done in batch mode with 50 to 100 wafers per run. Uniform results (e.g. thickness and resistivity) are desired for all wafers in the same tube. The standard industrial requirement is a maximum of 5% deviation for both the latitudinal uniformity (in-wafer uniformity) and the longitudinal uniformity (wafer-to-wafer uniformity).

We have done experiments to investigate the effects of reactant depletion on the uniformity of thickness and resistivity for wafers at different locations in the furnace tube. We found that the longitudinal uniformity of polysilicon thickness is the biggest problem.

We initially tried to apply a conventional fluid dynamic approach [14] to solve the uniformity problem. We found that the fluid dynamic approach is not suitable for a manufacturing environment because it is too complicated, too computationally intensive, and geometry dependent.

Our approach, which is still under investigation, has the following characteristics:

(a) The algorithm has mixed knowledge, and techniques consisting of empirical data, heuristics and a simple physical model.

(b) The algorithm is less computationally intensive. It has no differential equations and thus is more suitable for expert system application.

(c) The algorithm is more general. It should be "quasi-geometry and equipment-independent". The principle should be adaptable to other LPCVD processes such as the Nitride or P-glass process, etc.

We believe that our approach should be more portable between different fabrication lines. We plan to implement the algorithm once it is fully verified. The supporting module will be implemented immediately after the uniformity module.

10.2 Explanation facility

Explanation facility, such as answering the "why" type of questions, has not been incorporated into the current system. Simple documentations for help and answering "why" questions will be implemented in short future since it is very important for training purposes.

10.3 Interface to other process simulators

We would like to verify the generated recipe with a process simulator. The problem is not simple because we have to synthesize the input data for the simulator from the recipe. This problem is complicated and requires experience (see Appendix 1, pg. 52). Moreover, we are not aware of any existing process simulators that models the LPCVD in-situ doped polysilicon deposition because the problem is currently not well understood (which is therefore excellent for expert system application). Thus a compromise tentative proposal is to model the in-situ process by an undoped process followed by a dopant implantation or diffusion, which we will investigate in detail later [4].

PART IV: Conclusions and References

Chapter 11: Summary

An expert system that generates the processing steps for LPCVD in-situ doped polysilicon is described. Empirical, functional, and heuristic knowledge is employed. The system incorporates intelligent functions such as hypothetical generation and modular determination of parameters. Recipes generated can be translated and compiled to machine-specific commands for direct equipment control. Vital input/output information is presented using interactive bit-mapped graphics. The system has designed recipes which offer trade-offs between processing temperature and throughput. Recipes were verified by experiments and produced results in reasonable agreement with initial design goals.

12. References

[1] C. Y. Fu, Norman H. Chang, Kuang-Kuo Lin and D. A. Hodges. *Expert System for IC Computer-Aided Manufacturing*, SEMICON EAST technical sessions, September 1987.

[2] Kuang-Kuo Lin, C. Y. Fu, Norman H. Chang and D. A. Hodges. *Recipe Generator for LPCVD Polysilicon*, submitted to 172nd meeting of Electrochemical Society, Honolulu, Hawaii, October 1987.

[3] F. Hayes-Roth, D. A. Waterman, and D.B. Lenat, editors. *Building Expert Systems*. Addison-Wesley, 1983.

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Appendix 1: SUPREM sample run on NMOS Silicon Gate

```
4... Comment      Initialize silicon substrate.
5... Initialize   <100> Silicon, Boron Concentration=1e15
  ...   +          Thickness=1.5 dX=.005 XdX=.02  Spaces=150

6... Comment      Grow pad oxide, 400A.
7... Diffusion    Temperature=1000  Time=40  DryO2

8... Comment      Deposit 800A of CVD Nitride.
9... Deposit      Nitride  Thickness=.0800  Spaces=15

10... Comment     Grow field oxide.
11... Diffusion   Temperature=1000  Time=180  WetO2
12... Print       Layer

13... Comment     Etch to silicon surface.
14... Etch        Oxide all
15... Etch        Nitride all
16... Etch        Oxide all

17... Comment     Implant boron to shift the threshold voltage.
18... Implant     Boron  Dose=4e11  Energy=50

19... Comment     Grow gate oxide
20... Diffusion   Temperature=1050  Time=30  DryO2  HCL%=3

21... Comment     Deposit polysilicon
22... Deposit     Polysilicon  Thickness=0.5  Temperature=600

23... Comment     Heavily dope the polysilicon using POCl3
24... Diffusion   Temperature=1000  Time=25  dTmin=.3
  ...   +          Phosphorus  Solidsolubility

25... Print       Layer
26... Plot        Chemical Boron       Xmax=1.5  Clear YAxis Linetype=2
27... Plot        Chemical Phosphorus  Xmax=1.5  YClear YAxis Linetype=3
28... Plot        Chemical Net         Xmax=1.5  YClear  Axis

29... Comment     Save the structure at this point.  The simulation runs
30... $           are split for the gate and source/drain regions.
31... Save        Structure  File=s3ales

32... Stop        End of SUPREM-III Example 1.
```

Appendix 2: Tylan recipe for polysilicon deposition

```
0001.0015    TEMPL=644
0001.0020    TEMPC=650
0001.0025    TEMPS=656
0001.0030    KR=20
0001.0035    KC=10
0001.0040    KP=16
0001.0045    TEMPL TOLERANCE=2
0001.0050    TEMPC TOLERANCE=2
0001.0055    TEMPS TOLERANCE=2
0001.0060    VACUUM=OFF
0001.0065    ULDISA=OFF
0001.0070    LLDISA=OFF
0001.0075    SIH4=OFF
0001.0080    SIH4=0.0
0001.0085    PH3=OFF
0001.0090    PH3=0.0
0001.0095    KXLC=4
0001.0100    KXCC=3
0001.0105    KXSC=4
0001.0110    KXLH=50
0001.0115    KXSH=50

0005.0000  STEP  CHECK FOR AUTO MODE
0005.0005     TIME:00:00:01
0005.0010     ULDISA=ON
0005.0015     LLDISA=ON

0010.0000  STEP  CHECK FOR AUTO MODE (CONT.)
0010.0005     TIME:00:00:01
0010.0010     IF AUTOTMP=OFF GOTO 0005
0010.0015     IF GPAUTO=OFF GOTO 0005
0010.0020     IF VACALM=OFF GOTO 0005

0015.0000  STEP  PRESS ALARM ACK TO AVOID UNLOADING (FOR COATING DEP)
0015.0005     TIME:00:00:15
0015.0010     IF ALMACK=ON GOTO 0025
0015.0015     ULDISA=OFF
0015.0020     LLDISA=OFF
0015.0025     UNLOAD=ON
0015.0030     LOAD=OFF

0020.0000  STEP  UNLOAD (NO MORE REQUIRED WAIT)
0020.0005     TIME:00:12:00
0020.0010     UNLOAD=ON
0020.0015     N2=2000
0020.0020     LOAD=OFF
0020.0025     TEMPS=580
0020.0030     TEMPC=640
0020.0035     TEMPL=590
0020.0040     KP=4
0020.0045     IF ALMACK=ON GOTO 0025

0025.0000  STEP  LOAD
0025.0005     TIME:00:00:00
0025.0010     UNLOAD=OFF
0025.0015     LOAD=ON
0025.0020     IF SPIN=ON GOTO 0030
0025.0025     IF ALMACK=ON GOTO 0030
0025.0030     KRC=2

0030.0000  STEP  SHORT WAIT
0030.0005     TIME:00:00:05
0030.0010     LOAD=ON
```