HIGH-FREQUENCY MONOLITHIC PHASE-LOCKED LOOPS

by

Mehmet Soyuer

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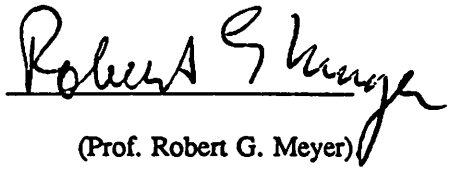
Ph.D. Mehmet Soyuer Department of EECS



(Prof. Robert G. Meyer)
Committee Chairman

ABSTRACT

This thesis describes research concerned with the design and realization of monolithic phase-locked loops (PLLs) at frequencies of 100 MHz and above using silicon bipolar technology. Several types of oscillators and phase detectors have been simulated and their performances compared with a special interest in narrowband filtering applications. Varactor-tuned LC-oscillators are preferred at frequencies above 100 MHz since they have low jitter and small temperature coefficient (TC). Analog phase detectors have been shown to perform better than digital phase detectors at these frequencies. Analysis and simulations showed that it was feasible to implement a monolithic PLL above 500 MHz using analog circuit design techniques and a 10-GHz bipolar process.

A 2-micron oxide-isolated bipolar process was used to fabricate a monolithic PLL test circuit. A varactor-tuned VCO and an analog phase detector have been utilized as building blocks. An on-chip varactor diode has been designed using the junctions available in the bipolar process with temperature and supply compensation provided by a band-gap reference. There is a good correlation between the measurements and the simulation results. The VCO has a voltage coefficient of 0.3 percent/volt and a TC of -100 ppm/°C over 20 to 100°C up to 250 MHz. When housed in a 40-pin DIL package, the maximum VCO center-frequency was 350 MHz, and the PLL pull-in range was larger than ±1 percent. The monolithic PLL circuit has the potential to be used as a narrowband filter ($Q > 100$) at 500 MHz with an optimum package.

CHAPTER 1

INTRODUCTION

Phase Locked Loop (PLL) circuits are widely used in various communications and control systems applications, including frequency synthesis, clock signal (timing) recovery, modulation and demodulation of signals. As the frequency of interest goes higher, (e.g., cable and fiber optic data links), there is a greater need for monolithic circuits that can operate at these frequencies. Several technologies are possible candidates for operating frequencies into the GHz range and beyond. Silicon bipolar, [1]-[6], and NMOS, [7], as well as GaAs MESFET, [8]-[9], and heterojunction bipolar, [10], technologies are among the contenders. As the ultra-high frequency VLSI technologies become available, there is a strong motivation to include several subsystems on the same chip. However, the maximum operating range of most currently available monolithic PLL circuits is limited to frequencies below 150 MHz, [11]-[16]. Therefore, this research is concerned with the realization of monolithic PLLs above 100 MHz using high-frequency silicon bipolar technology. Silicon bipolar, being the most mature high-frequency technology, offers higher speed and larger transconductance through its exponential nonlinearity and smaller offsets through its well-controlled thermal voltage, $\frac{kT}{q}$. A balanced analog circuit topology similar to Emitter Coupled Logic (ECL) in digital circuits is a good choice throughout the design for optimum speed and matching. Although, higher speed means more power dissipation in general, [17]-[21], the circuits should be able to operate with a single 5 V supply to keep the power consumption low.

At high-frequencies, good isolation is hard to achieve and parasitic losses cannot be ignored. Therefore, the package performance has to be considered together with the inherent device limitations, [22]-[23]. Especially, inductive parasitics and coupling can deteriorate the high-frequency performance. Another common isolation problem is the unwanted coupling between the capacitive paths (crosstalk) which becomes worse as the frequency of operation increases. The silicon substrate is also susceptible to resistive coupling since it is a poor insulator. At very high-frequencies, skin-effect becomes significant

and that increases the resistive losses. Therefore, the quality factors of energy storage elements are degraded. Careful circuit design, layout and packaging can be used to circumvent some of these problems. It may be helpful to model the critical components in the high-frequency path as distributed RC-sections or lossy transmission lines. Applying a high-frequency signal or delivering it out may become easier if the reflections are minimized by using proper terminations.

There are several outputs available from a PLL which can be useful depending on the application. In demodulation of the FM signals, the loop filter output provides the modulating signal. In timing recovery applications, the VCO-output waveform is used as the recovered clock signal and the ultimate goal is to minimize the phase error between the input signal and the VCO and at the same time to filter out the noise components. In general, PLL itself must contribute much less noise than is present at its input. To minimize the jitter (dynamic phase error) caused by the input noise, the loop bandwith must be made very small compared to the input frequency. This, in turn, reduces the pull-in range available from the loop. The VCO center-frequency drift is one of the main contributors to the static phase error together with the dc-offsets in the phase detector and loop amplifier. Therefore, it should be minimized against temperature and supply variations. When used as a narrowband filter as in timing-recovery applications, a PLL with a stable VCO requires a relatively narrower pull-in range and this makes the filter design easier. Also, a high-frequency crystal is not required if the VCO can be compensated for temperature and supply variations. Although this design approach involves a trade-off between different PLL parameters, most significantly between pull-in range and noise bandwith, it is relatively easy to implement such a PLL without any extra circuitry for frequency acquisition. Furthermore, it is possible to minimize the noise contribution of the PLL by employing a VCO with a small noise bandwith. Since relaxation oscillators have large noise bandwith and jitter, [24], small noise bandwith requirement dictates the use of harmonic oscillators in which one of the tank circuit reactances or the phase shift through the active element is variable.

The main purpose of this research is to investigate the frequency limitations of main PLL components with a special interest in timing recovery applications, and then to use integrated circuit design

techniques to overcome some of these limitations. Using the general approach outlined above, several types of PLL building blocks are designed. Their performances are compared by extensive computer simulations. Digital as well as analog phase detectors are considered. In the monolithic implementation of the test circuits, an on-chip varactor diode is used to control the VCO frequency. Its quality factor is optimized by minimizing the resistance-capacitance product per area. The VCO stability is achieved by canceling the temperature dependence of the varactor diode capacitance to a first order approximation. For this purpose, a conventional band gap reference is used to derive the loop amplifier bias currents so that the reverse bias across the diode has a positive temperature coefficient which opposes the temperature coefficient of the built-in potential and dielectric constant of silicon. In this way, it is also possible to take the contribution of the phase detector and amplifier offsets to the VCO control voltage into account. An analog phase detector and input/output amplifiers complete the test circuit.

Chapter 2 gives an overview of the PLL parameters involved in a high-gain second-order loop design. The central question of how to design a stable high-frequency PLL with small phase error and noise bandwith and with large pull-in range is tried to be answered in that chapter. The importance of high-gain second-order loops is emphasized. Alternative approaches are also included. The main building blocks of the PLL are discussed in Chapters 3 and 4. An initial comparison is made among different possible topologies and their frequency limitations are assessed. The optimization procedure for each block and crucial component is described in detail. The design techniques used to improve the circuit performance are given in these chapters. In Chapter 5, measurement results for open loop and closed loop operation are presented for a 2-micron oxide-isolated bipolar technology. Possible improvements are also suggested. It is shown that the frequencies above 300 MHz are easily achieved with an on-chip-varactor controlled oscillator and an analog phase detector even when the circuit is housed in a 40-pin DIL-package. The circuit contains less than a hundred active devices and occupies an area of 0.5 mm^2. It dissipates 270 mW with a single 5 V supply and can be integrated into a larger subsystem.

CHAPTER 2

PLL DESIGN PARAMETERS

2.1. Introduction

There are several books, [25]-[29], and many papers, [30]-[33], written on the theory of phase-locked loops. Their integrated circuit implementations are also covered in different books, [34, ch. 10]-[35, ch. 12]. In this chapter, an overview of the PLL theory will be given and its important design parameters will be discussed.

A PLL circuit is essentially a negative feedback control system, Figure 2.1.

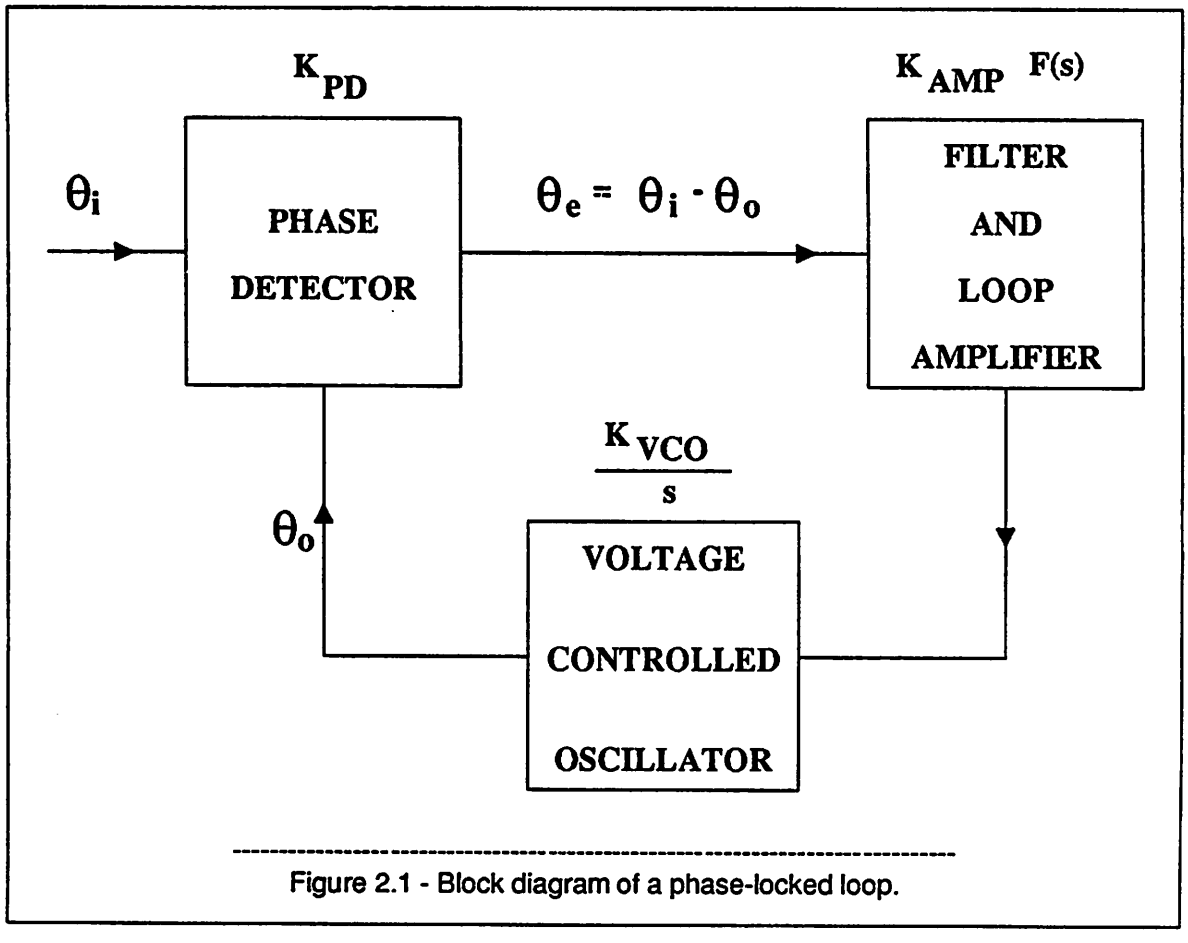


Figure 2.1 - Block diagram of a phase-locked loop.

The frequency of the voltage-controlled oscillator (VCO) is controlled by the phase detector output through the feedback loop and is made equal to the frequency of the input signal with a phase difference. There are two main regions of operation during the frequency and phase capturing process. Initially, the two frequencies are not equal and the circuit operates in a non-linear fashion. If the initial frequency difference is small enough, the negative feedback loop pulls the VCO frequency close to the input frequency until they become equal. This is the second region of operation or the quasi-linear mode. Assuming linear mode of operation, one can assign gain constants to each of the PLL building blocks. Hence, K_{PD} is the phase detector gain in volts per radian, K_{VCO} is the VCO gain in radians/second per volt, and K_{AMP} is the loop amplifier gain. If the loop filter has the transfer function F(s), the DC-loop gain is defined as:

$$K_{DC} = K_{PD}\, K_{VCO}\, K_{AMP}\, F(0) \tag{2.1.1}$$

K_{DC} has the dimensions of radians per second similar to an inverse RC-time constant, and it is an important parameter of the PLL. Together with the loop filter time constants, the DC-loop gain determines the dynamic properties of the PLL.

The range of frequencies that an initially unlocked PLL can lock onto is called the pull-in (also capture or frequency acquisition) range, $\Delta\omega_P$. The range of frequencies which a locked PLL can hold onto is called the hold-in (also hold or lock) range, $\Delta\omega_H$. In principle, the hold-in range is greater than or equal to the DC-loop gain and is always larger than the pull-in range. In practice, it is usually limited by the saturation of the loop amplifier for a high-gain loop.

Since VCO essentially performs an integration on frequency, the PLL transfer function has a pole at the origin even without any loop filter, and therefore it is called a first-order PLL. In order to obtain a second-order PLL, a loop filter with a single pole is necessary. An ideal integrator in the loop filter would provide an infinite DC-loop gain.

A typical application of a PLL as a narrowband filter would be as the timing-recovery filter in a regenerative repeater, as shown in Figure 2.2. If a discrete line at the clock frequency is not present in the input spectrum, non-linear processing must be performed before filtering. The recovered clock can

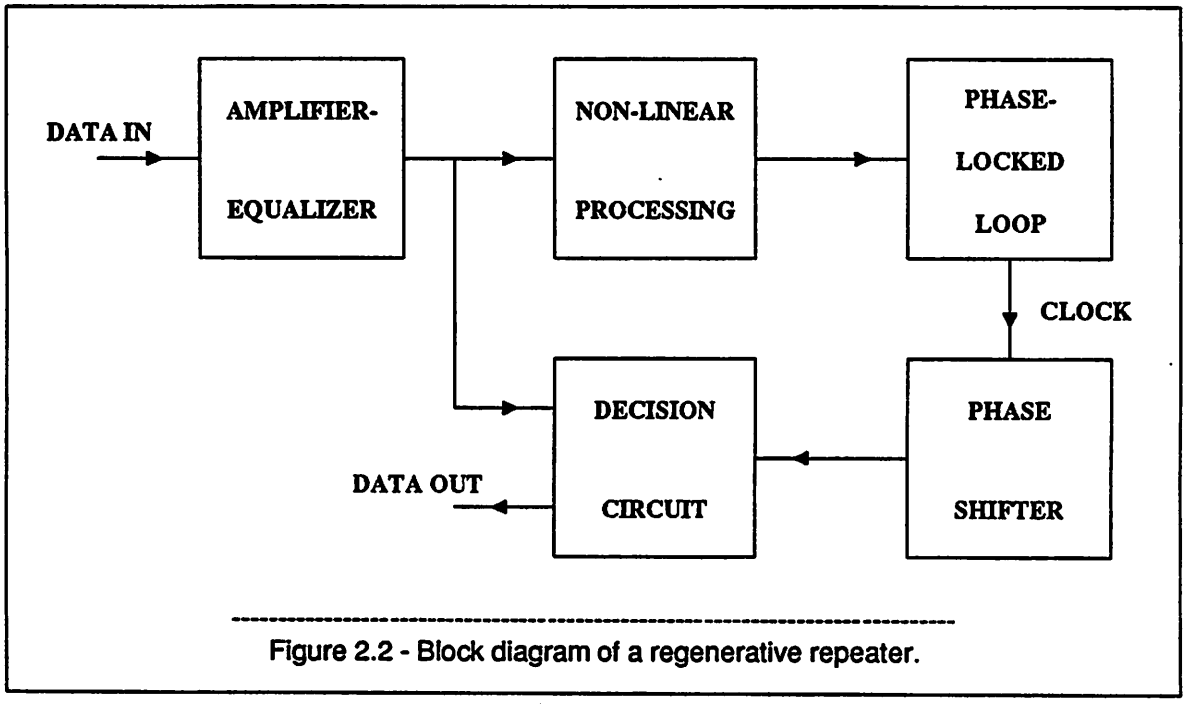


Figure 2.2 - Block diagram of a regenerative repeater.

be used in the decision circuit. The statistical properties of timing jitter in regenerative digital transmission is extensively analyzed in the literature, [36]-[43].

For most applications, it is necessary to build a high-gain second-order PLL. In the following sections, the reasons behind this necessity will be investigated.

2.2. Static Phase Error

Depending on the phase detector type used, there is a constant phase difference, usually 0, 90 or 180 degrees, between the input and the VCO under locked conditions. This phase difference is not a phase error and it may be called as the stable operating point of the PLL. However, unless ideal (hence unrealizable) building blocks are used, there will always be another component of phase difference between the input and the VCO. This component is termed as the phase error.

The phase error has two parts, a static part and a dynamic part (jitter), [36]. The static phase error is given by:

$$\Theta_e = \frac{V_{OS}}{K_{PD}} + \frac{\Delta\omega}{K_{DC}} \qquad (2.2.1)$$

where V_{OS} is the combined offset voltages of the phase detector and loop amplifier and $\Delta\omega$ is the initial frequency difference between the input and the VCO. This component actually can be termed as the quasi-static phase error since all the terms in the equation above are temperature and supply dependent. As it can be seen, a high-gain PLL with a stable VCO and small DC-offsets is necessary to minimize the static phase error.

2.3. Dynamic Phase Error

There are two main sources of jitter, the first one is external to the PLL (input noise) and the second one is internal (PLL noise). Input noise may contain a white noise component, and a pattern dependent noise component if a random data signal is present at the input. To filter out the noise components, a loop filter must follow the phase detector. Therefore, only a high-gain second-order PLL is useful as a narrowband filter. Higher order loops suffer from the stability problems. PLL noise is mainly due to the VCO phase noise, [25, ch. 6].

Assuming that the pattern dependent noise dominates the additive noise at the PLL input, and that the VCO phase noise is negligible, dynamic component of the phase error can be expressed as :

$$\overline{\Delta\Theta_e^2} = a\,\frac{\Theta_e^2}{Q_{PLL}} + b\,\frac{1}{Q_{PLL}} \tag{2.3.1}$$

where $\overline{\Delta\Theta_e^2}$ is the total mean-square value of the jitter at the PLL output with regard to the nominal input phase, "a" represents the amplitude effects of the random data, "b" represents the phase effects of the random data, and Q_{PLL} is the quality factor of the PLL, [36]. For a given random data pattern, numerical integration techniques are usually necessary to estimate the PLL jitter, [40]-[41], [44].

If a pilot tone is transmitted for clock recovery, then the variance of the VCO output phase due to the input noise can be expressed as:

$$\overline{\Delta\Theta_o^2} = \frac{W_i\,B_L}{P_s} \tag{2.3.2}$$

where P_s is the input signal power in watts and W_i is the noise power spectral density in watts/Hz, [25,

ch. 3]. Accordingly, for a given PLL output jitter, B_L must be minimized to account for the worst case, i.e. the lowest, level of the pilot tone.

Similar to an LC-filter, the quality factor of the PLL is given by:

$$Q_{PLL} = \frac{\pi}{4} \frac{f_C}{B_L} \tag{2.3.3}$$

where f_C is the input clock frequency and B_L is the noise bandwith of the PLL, [36]. For equal number of poles and zeroes in the loop filter, the noise bandwith can be approximated as:

$$B_L \approx \frac{1}{4} K_{DC} \frac{F(\infty)}{F(0)} \tag{2.3.4}$$

where $F(\infty)$ is the value of the loop filter transfer function at very high frequencies, [25, ch. 3].

A significant advantage of the PLL-filter over the passive filters is that static and dynamic phase errors can be minimized independently. Again, a second-order high-gain PLL is required for this purpose. The DC-loop gain must be increased to minimize the static phase error, and the loop filter attenuation must be increased to minimize the dynamic phase error. Implications of this on the pull-in range will be discussed in the next section.

2.4. Pull-In Range

Self-acquisition of frequency is called pull-in or capture. Due to the non-linear time-varying nature of the PLL-system during frequency acquisition, an analytical solution for pull-in is only possible for the first-order loop, [45]. Qualitatively, the VCO frequency is frequency modulated by the difference frequency, also called the beat note, during the capture process. Therefore, the phase detector output has a non-zero DC-average which enables pull-in to occur. If the DC-average is large enough compared to the undesired DC-offsets, negative feedback will pull the VCO frequency toward the input frequency.

Pull-in behavior is a strong function of the DC-loop gain, loop filter time constants and the type of the phase detector used. In the following discussion, a high-gain loop with a single-pole single-zero filter and a multiplier type phase detector is assumed. Second and higher order loops are best analyzed with

the help of a computer, [46]. An approximate analysis yields the following result for a second-order loop, [25, ch. 5]:

$$\Delta\omega_P \approx K_{DC} \sqrt{2 \frac{F(\infty)}{F(0)}} \tag{2.4.1}$$

A sinusoidal-multiplier is assumed for the phase detector. However, when combined with a high-gain amplifier, saturation effects may result in a trapezoidal or even a binary phase detector. The latter case is analyzed by J. F. Oberst, [47], and the end result for a passive lag-lead filter is:

$$\Delta\omega_P \approx 2 K_{DC} \sqrt{\frac{F(\infty)}{F(0)}} \tag{2.4.2}$$

Therefore, the binary type phase comparator improves the pull-in range by a factor of $\sqrt{2}$. In practice, the pull-in range may be assumed between these two limits.

The next question is how large a pull-in range is required. Obviously, it should be large enough to cover any initial VCO frequency offset. Therefore, one needs:

$$\Delta\omega_P \geq K_{DC}\, \Theta_e \tag{2.4.3}$$

In theory, an active filter would provide almost an infinitely large pull-in range, since it has a pole close to the origin. In practice, however, offset voltages in the phase detector and the loop amplifier will be integrated until the amplifier is saturated driving the VCO outside the capture range. Therefore, either external frequency acquisition or DC-feedback around the amplifier is necessary. Charge pump circuits can also be used for the same purpose, [48]. They do not require an amplifier to provide a pole at the origin. But usually they require complementary devices, and therefore they are limited in frequency, [13].

Comparing the equations for the pull-in range with the noise bandwith equation, it can be seen that they cannot be optimized independently. Therefore, either a compromise must be made in the loop filter design or the frequency acquisition capability of the PLL must be improved. Although the first approach is actually implemented in this study, it is worth mentioning some of the alternatives to realize the second approach.

The frequency acquisition can be aided by an additional frequency detector, [2], [13], [14], [21], [45], [49]-[52], by frequency sweeping, [25, ch. 5], by bandwith switching, [53]-[54], or by injection locking, [55]-[57]. Frequency detectors can have analog, [2], [14], [45], [49]-[50], or digital [13], [21], [51]-[52], implementations. A typical block diagram for a PLL with a frequency detector is shown in Figure 2.3.

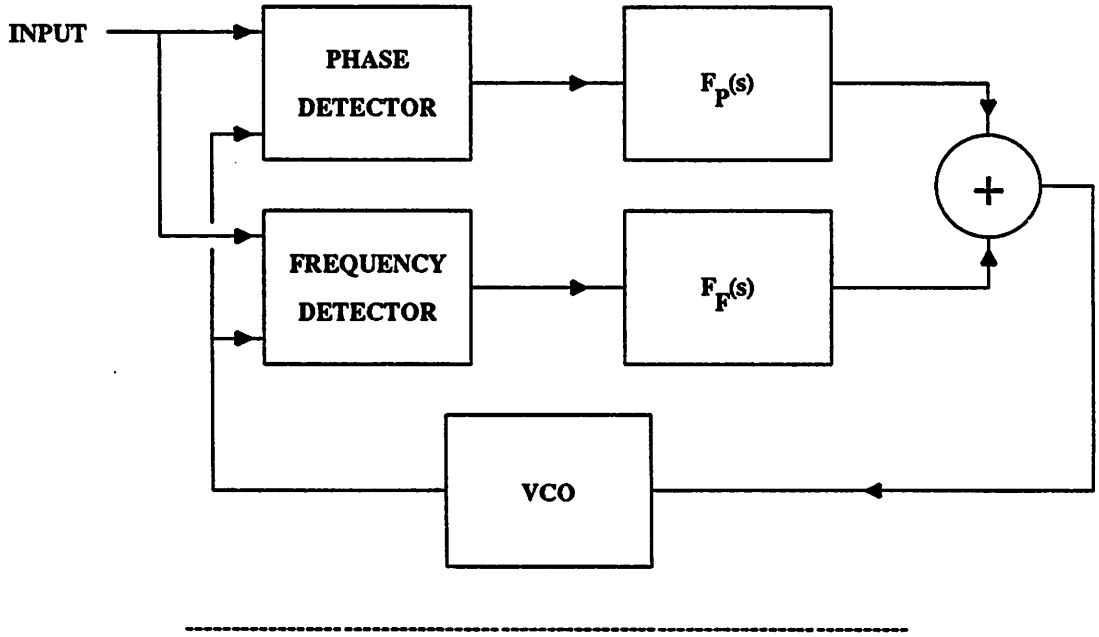


Figure 2.3 - PLL with a frequency detector.

In some cases, both the frequency and the phase detector may share the same filter. Actually, almost all the digital phase detectors with memory, i.e. sequential type phase detectors, can also provide frequency capability, [58]-[62]. This topic will further be discussed in Chapter 4 and Appendix A. A digital frequency detector design example using the rotational frequency detector concept, [51], is given in Appendix B. In analog implementations, the extra circuitry may include multipliers, filters and differentiators, [14], [49]-[50], and/or limiters, phase shifters and monostable multivibrators, [2]. Frequency sweeping can be achieved by introducing a constant current into the loop filter. Then, the control voltage is a ramp that sweeps the VCO frequency. Bandwith can be changed by gain switching either in the phase detector or the loop amplifier, or by switching the filter resistors. If the phase detector gain is proportional to the

signal level, automatic gain control circuits may replace the switches. Finally, signal injection into the VCO can improve pull-in behavior if carefully controlled. Injection is always present in any practical circuit especially at high frequencies due to poor isolation.

All these methods require extra circuitry and may degrade the PLL frequency performance. They also require more power consumption and larger chip area. In addition, switching noise from the digital circuits may create problems for the analog parts of the PLL. Therefore, the best strategy for the high frequencies seems to be that one should keep the circuits simple enough so that they can easily be implemented.

2.5. Noise Bandwith

It is already shown that reducing the noise bandwith is essential to minimize the jitter. However, the VCO phase noise puts a theoretical lower limit on the noise bandwith that can be achieved. To generalize, internal noise always puts an upper limit on the quality factor of any narrowband filter. For example, let us take the case of a PLL with a varactor-tuned LC-type VCO. In this case, the PLL noise bandwith has to be larger than the VCO noise bandwith.

In order to obtain some numerical values, the simplified model shown in Figure 2.4 will be used for the varactor-tuned VCO circuit. Assume that the only internal noise sources are the loop amplifier that generates the control voltage, and the amplifier stage employed within the VCO. First, let us try to estimate and compare the relative contribution of each amplifier to the tank circuit noise. To simplify the problem, one can break the positive feedback loop around the VCO, and also assume that the loop amplifier is band limited to B_{LA} by the bypass capacitor, C_{LARGE}. Let B_{TANK} be defined as the tank-circuit bandwith. Then, following a similar analysis as in Section 11.4 of Gray and Meyer, [34], one can show that:

$$\frac{v_{va}}{v_{la}} \approx \sqrt{\frac{W_{va}}{W_{la}} \frac{B_{TANK}}{B_{LA}}} \tag{2.5.1}$$

where v_{va} and v_{la} are the rms-voltages across the tank circuit resulting from the VCO and loop amplifier,

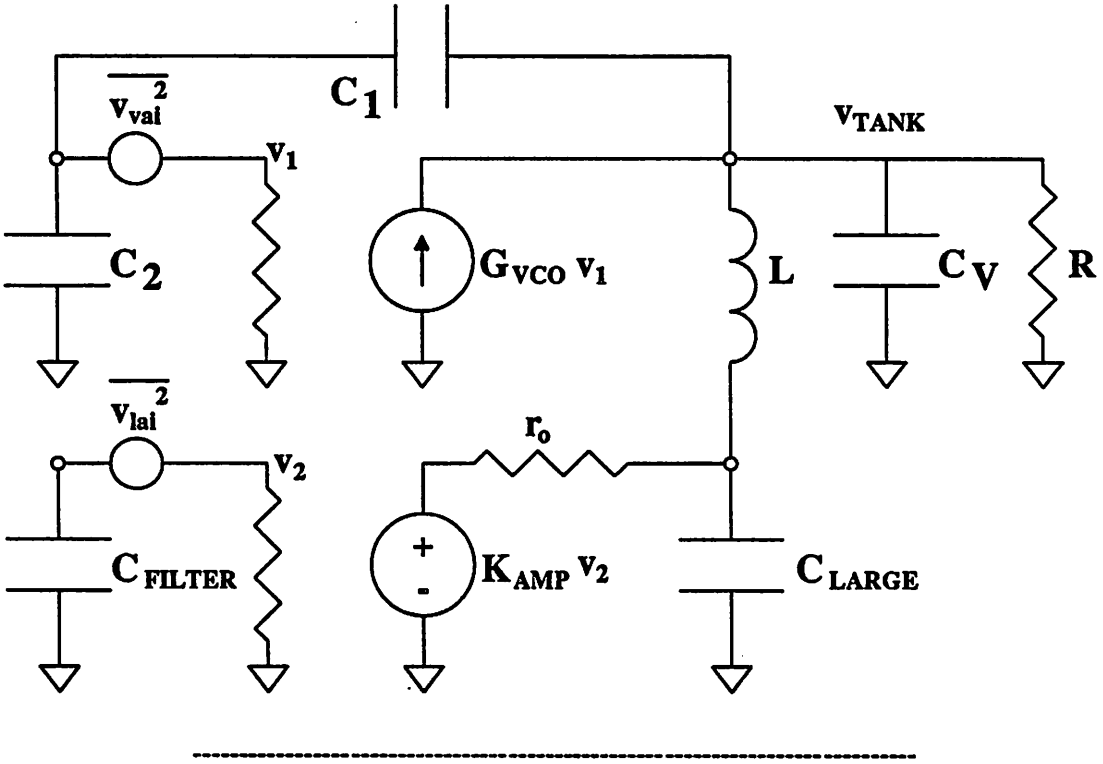


Figure 2.4 - Simplified VCO-noise model.

respectively. W_{va} is the noise power density of the VCO amplifier output at the high frequencies, and W_{la} is the noise power density of the loop amplifier output at the low frequencies. For $W_{la} = 20W_{va}$, and $B_{TANK} = 10B_{LA}$, v_{la} is three times larger than v_{vco}. It should be mentioned that this analysis is oversimplified since the non-linear effects and the flicker noise components are neglected.

Next, we close the positive feedback loop around the VCO-gain stage. According to Edson [63, ch. 15], the VCO noise bandwith due to the thermal noise in the load resistor is:

$$B_{VCO} = 2\pi kT \frac{K_o^2 f_o^2}{P\ Q^2} \tag{2.5.2}$$

where K_o is the amplification at the nominal operating frequency f_o, P is the power dissipated across the load, and Q is the tank circuit quality factor. For K_o = 10, f_o = 300 MHz, P = 0.04 mW, and Q = 10, B_{VCO} is 58.7 Hz. However, when the noise from the amplifiers included, B_{VCO} will increase considerably since the noise bandwith is proportional to the noise density, [64, ch. 1]. Assuming that the noise density

increases by a factor of 400, a very rough upper limit for Q_{PLL} will be about 10^4 with the values assumed above.

Obviously this value is very optimistic. As it was discussed in the preceding section, the pull-in range requirements would put stringer limits on Q_{PLL}. For example, if the pull-in range is one percent of f_o and the loop filter attenuation is ten percent, then from equations (2.3.3)-(2.4.1), Q_{PLL} turns out to be 225.

Typical Q values for different narrowband filters are less than 80 for LC-filters, [65, ch. 10], between 80 to 500 for PLLs, [5], [37], 500 to 1000 for SAW-filters, [66], and more than 1000 for dielectric resonator filters, [67], and for PLLs with crystal VCOs, [4], [68]. Reference [66] also provides a good comparison between the PLLs and SAW-filters. PLLs have less loss and better bandwith control, and they do not require a special substrate. But they are relatively difficult to implement at high-frequencies. In digital PCM transmission link repeaters, a Q of 200 to 250 is considered to be adequate to control the jitter down to 0.1 radian, [5], [37]. However, in general, jitter is a strong function of the coding of the random data as mentioned previously.

Another limitation that arises from employing a narrowband filter is the large pull-in time. For a high-gain PLL, the pull-in time is proportional to the square of the initial frequency difference, and inversely proportional to the cube of the noise bandwith, [25, ch. 5]. Therefore, for one percent pull-in range at 300 MHz and a pull-in time less than a millisecond, Q_{PLL} must be less than 1100. Consequently, PLLs with crystal-VCOs have longer pull-in times. Pull-in time can be reduced by several orders of magnitude by inserting an antiparallel diode pair between the phase detector and the loop filter, [69].

2.6. Stability

Stability of the PLL in locked condition can be analyzed using the Laplace Transform and the Bode plots. Referring to Figure 2.1, the open-loop gain of a PLL can be written as:

$$G(s) = K_{PD}\, K_{AMP}\, \frac{K_{VCO}}{s}\, F(s) \tag{2.6.1}$$

Then the closed-loop transfer function is:

$$H(s)=\frac{\Theta_o}{\Theta_i}=\frac{K_{PD}K_{AMP}K_{VCO}F(s)}{s+K_{PD}K_{AMP}K_{VCO}F(s)} \tag{2.6.2}$$

Therefore, a high-gain second-order loop performs a low pass filtering operation on phase inputs.

Any extra delay in the loop also creates poles that must be included in the stability analysis. Usually, the ripple filter used to minimize the phase detector output ripple and/or the limited bandwith of the loop-amplifier introduces a non-negligible pole which is smaller than the DC-loop gain.

A typical Bode plot of a second-order loop with a ripple filter is shown in Figure 2.5. C_r is the ripple filter capacitor. The loop filter transfer function including the ripple filter can be written as:

$$F(j\omega)=\frac{1+j\frac{\omega}{\omega_{zero}}}{1+j\frac{\omega}{\omega_{pole}}}\,\frac{1}{1+j\frac{\omega}{\omega_{ripple}}} \tag{2.6.3}$$

Strictly speaking, the loop is third order now, but choosing the ripple filter pole large compared to the loop filter zero enables us to analyze the loop as a second-order PLL. It can easily be shown that for a phase margin greater than 45°, the ripple filter pole is given by:

$$\omega_{ripple}\geq\frac{K_{DC}}{2}\,\frac{\omega_{pole}}{\omega_{zero}} \tag{2.6.4}$$

Therefore, a good rule of thumb is:

$$\frac{K_{DC}}{2}\,\frac{\omega_{pole}}{\omega_{zero}}\gg\omega_{zero}\gg\omega_{pole} \tag{2.6.5}$$

For example, if $K_{DC}=0.1\omega_o$, $\omega_{pole}=10^{-5}\omega_o$, and $\omega_{zero}=2x\,10^{-4}\omega_o$, then the ripple filter pole must be larger than $2.5x\,10^{-3}\omega_o$. Actually, the approximations involved in the derivation of equation (2.3.4) for the noise bandwith also put similar restrictions to those in equation (2.6.5). But they are easily satisfied if equation (2.6.5) is followed as a rule. Note that for the values above, Q_{PLL} is 100.

Before concluding this chapter, it might be interesting to check the scaling of the several PLL parameters with frequency. K_{DC} is proportional to the operating frequency ω_o, in radians per second,

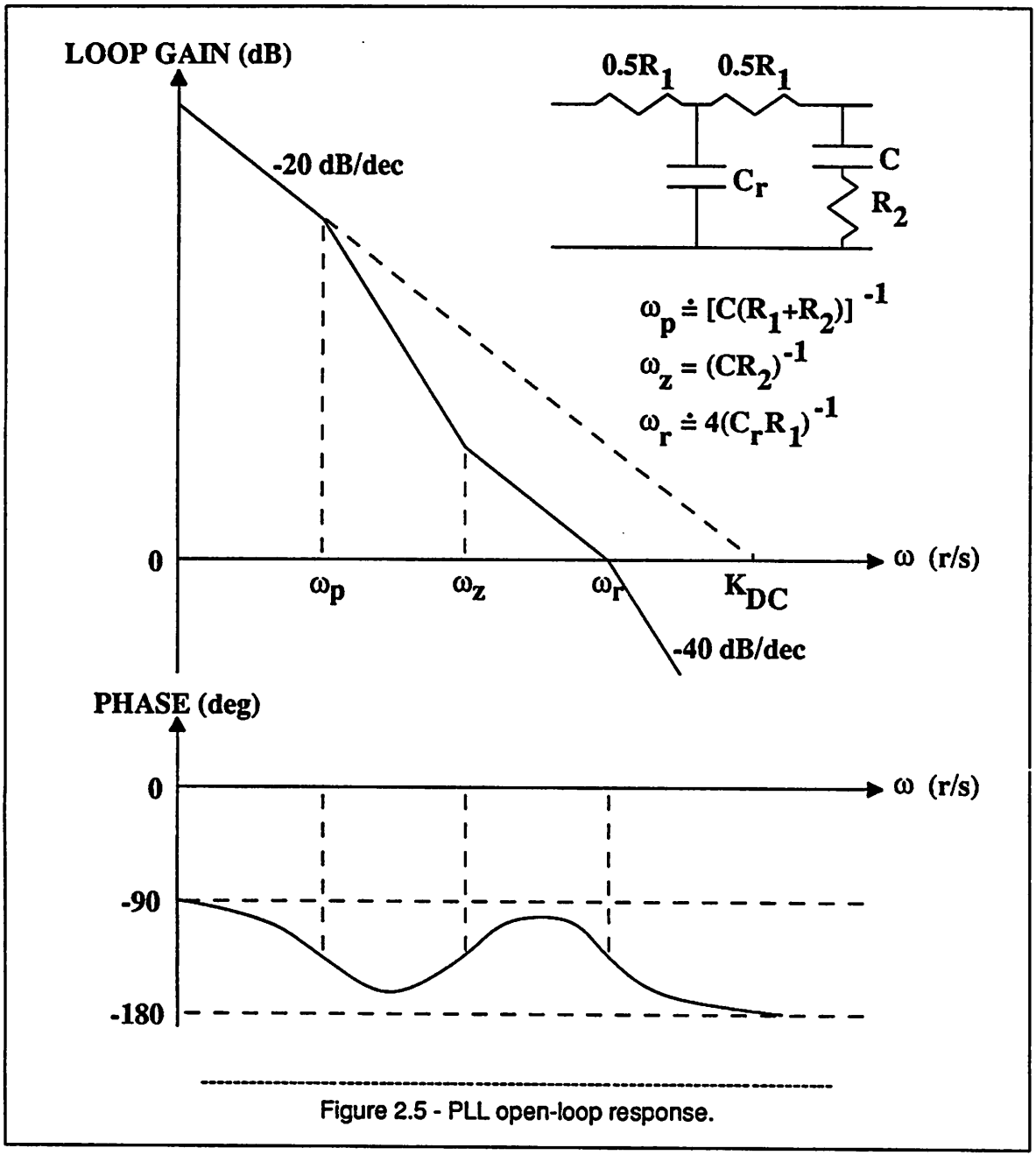


Figure 2.5 - PLL open-loop response.

assuming that K_{VCO} changes linearly with ω_o. Therefore, for a given K_{PD}, K_{AMP} and filter attenuation ratio, Q_{PLL} is independent of frequency from equations (2.3.3) and (2.3.4). On the other hand, pull-in range increases with frequency from equation (2.4.1) or (2.4.2). It seems that it is easier to obtain a given Q_{PLL} at higher frequencies if the VCO stability can be maintained constant throughout the frequency range of interest. However, as the frequency continues to increase, more extra poles will approach to

$$\frac{K_{DC}}{2}\frac{\omega_{pole}}{\omega_{zero}}$$

Hence, if nothing else, stability degradation will limit the maximum frequency that can be scaled in a simple way.

CHAPTER 3

VOLTAGE-CONTROLLED OSCILLATORS

3.1. Introduction

An oscillator is a circuit that produces a periodic signal at its output. An active circuit and a positive feedback network are the two essential parts of an oscillator. Oscillators can be analyzed either as two-port feedback networks or as one-port negative-resistance circuits. The design and analysis of oscillators are well covered in different books, [34]-[35], [70]-[72]. The amplitude of oscillation is usually determined by the nonlinearity in the active circuit. The frequency of oscillation is determined by the energy storage components, the voltage and current levels and by the phase shift or delay in the oscillator circuit. Therefore, varying any one of these quantities in a well-defined manner will result in an oscillator whose frequency can be controlled as desired. Voltage-controlled oscillator (VCO) is the general name used for such an oscillator.

There are several ways to implement a monolithic VCO. Depending on the controlling variable and the principle governing the dynamics of oscillations, they can be classified into four groups:

1. Varactor-controlled harmonic VCOs, [19]-[20], [50], [73],

2. Phase shift controlled harmonic VCOs, [13]-[14], [53]-[54],

3. Current-controlled relaxation VCOs, [11]-[12], [15]-[16], [74],

4. Delay-controlled ring VCOs, [7], [21], [75].

Harmonic oscillators employ an inductor, L, and a capacitor, C, for frequency selection. Therefore, varying the value of either one of these energy storage elements will result in a harmonic VCO. Since variable capacitors (varactors) are readily available in a monolithic process as junction capacitors, varactor-controlled VCOs are very attractive from the integrated circuit point of view. Unfortunately, inductors are not presently available in monolithic Si technology, and they have to be external to the

circuit. Using the two-port feedback approach, one of the required conditions for the oscillations to start is that the fed-back signal has to be in phase with the input signal. In other words, the total phase shift around the loop has to be zero. Therefore, any phase shift in the active circuit has to be compensated in the L-C tank circuit. This forces the operating frequency to shift depending on the tank circuit phase sensitivity with respect to frequency. Hence, it is possible to control the VCO frequency by introducing a deliberate phase shift into the active part of the oscillator and this may require some extra circuitry to introduce and control the phase shift. Moreover, at high frequencies, there already exists some phase shift associated with the parasitics of the active device used. All these can make the temperature compensation of the circuit quite difficult. In general, a frequency detector will be very useful when a phase shift controlled VCO is employed in the PLL, [13]-[14]. On the other hand, a varactor-controlled VCO essentially requires the compensation of its varactor capacitance. This task can be made easier if an on-chip junction capacitance with a known temperature dependence is used as the varactor. The phase shift can also be controlled by using R-C sections in the feedback network and without employing an inductor. However, the frequency selectivity becomes poor which, in turn, increases the noise bandwith of the oscillator.

As explained in the second chapter, the noise bandwith of a harmonic oscillator is inversely proportional to the square of the tank circuit quality factor, Q_T, and to the signal amplitude. Since the amplitude of oscillation is limited by other circuit constrains such as the requirement of forward active region of operation for active devices etc., it is best to keep the quality factor of tank circuit large, i.e. greater than ten, if possible. The same condition is also necessary to filter out the harmonics of the signal created by the nonlinearities in the circuit. Too much distortion will shift the oscillations to a lower frequency making the frequency control more difficult. The quality factor for a parallel tank circuit is given by:

$$\frac{1}{Q_T} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{3.1.1}$$

where Q_L and Q_C are the quality factors of L and C, respectively. Any other loading from the rest of the oscillator circuit will further lower the Q_T. Therefore, assuming a low-loss inductor, a high-quality varactor is essential for achieving a high-performance varactor-tuned harmonic VCO. This topic will be

discussed in detail in section 3.3. Even when a crystal can be used replacing the inductor, the losses in the varactor will reduce the Q_T.

Relaxation and ring oscillators have one significant property in common, that is, they are both broad band switching circuits. One of the storage elements which make the harmonic oscillators narrowband, L, is missing in relaxation and ring oscillators, and therefore, they are much more prone to noise, [64]. They also tend to have large temperature coefficients at high frequencies, [11], [15]-[16], [74]. Ideally, they are useful in obtaining square wave outputs. In a relaxation oscillator, a constant current source charging a timing capacitor reverses its polarity when a threshold voltage determined by the voltage drops in the circuit is reached. The switching behavior in each half cycle is described by a fast transition and a slow relaxation. If the current can be controlled through a voltage to current converter, a VCO is obtained. In general, the frequency is a linear function of the current and a very wide range of frequency control can easily be achieved compared to the varactor-tuned and ring-type VCOs. In a ring oscillator, odd number of inverter stages are cascaded in a ring formation. The delay through each stage multiplied by the number of stages gives the half period of oscillations. Frequency can be controlled by changing the delay which is a complicated function of several R-C time constants for a given inverter. In bipolar technology, the ECL gate and emitter follower bias currents are possible candidates to vary the gate delay, [17]-[18]. The process, temperature and supply variations strongly influence the frequency of oscillation since all the parasitics contribute to the gate delay. Multiple modes of oscillation encountered in ring oscillators is another common problem that must be addressed, [7], [75].

Consequently, varactor-controlled harmonic VCOs seem to be the best choice for high-frequency narrowband PLL implementations in monolithic technology if one desires low jitter and low TC. Therefore, the rest of this chapter is devoted to the discussion of varactor-controlled VCOs.

3.2. Negative Resistance and Frequency Limitations

As mentioned in the preceding section, every harmonic oscillator needs a gain stage and a feedback network. Since it is relatively straightforward to fabricate wideband transconductance amplifiers and

low-loss capacitive transformers using a silicon bipolar technology, a typical configuration that might include these components is shown in Figure 3.1.

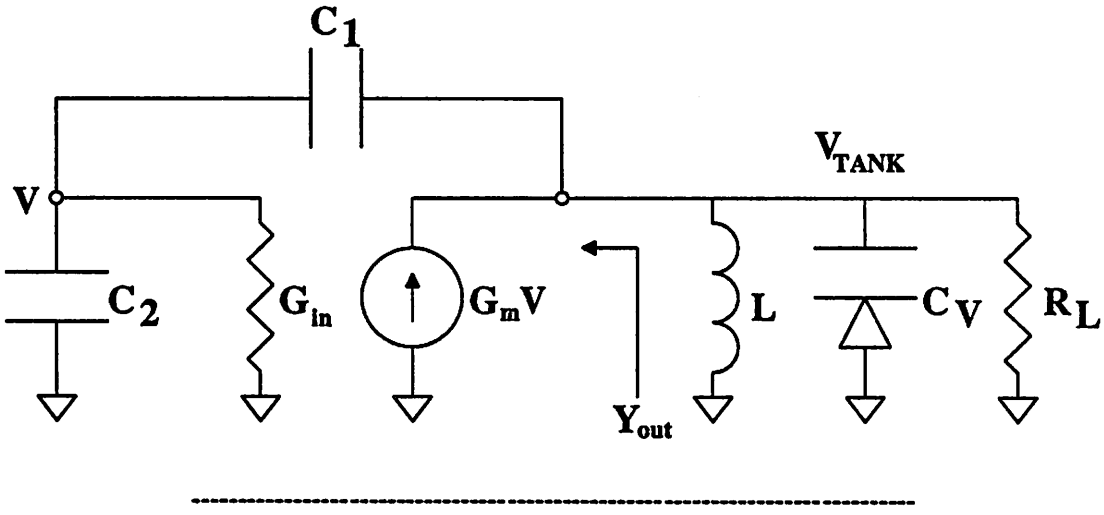


Figure 3.1 - Transconductance amplifier with feedback.

Assuming a negative conductance is available at the output, loading the amplifier with a a parallel tank circuit will result in a harmonic oscillator.

The next question that comes to mind is that for what frequency range one can assume an output impedance with a negative real part from this amplifier with capacitive feedback. It can easily be shown that for an ideal amplifier with infinite input impedance and with no other loading at its input, the output impedance of the circuit is always capacitive with a negative real part. Therefore, the only frequency limitation will come from the bandwith of the amplifier depending on how large a negative resistance required for a given loss in the tank circuit. A logical step would be to choose a common-base amplifier configuration since it has a very wide bandwith, [34, ch. 7]. This results in the well-known common-base Colpitts circuit as shown in Figure 3.2. Since the input conductance, G_{in}, of a common-base stage is close to its transconductance, G_m, one can show that the following equation has to be satisfied in order to obtain a negative output conductance which is larger than the shunt conductance, G_L, of the tank circuit:

$$\omega^2 > \frac{G_m^2}{C_1 C_2 G_m R_L - (C_1 + C_2)^2} \qquad (3.2.1)$$

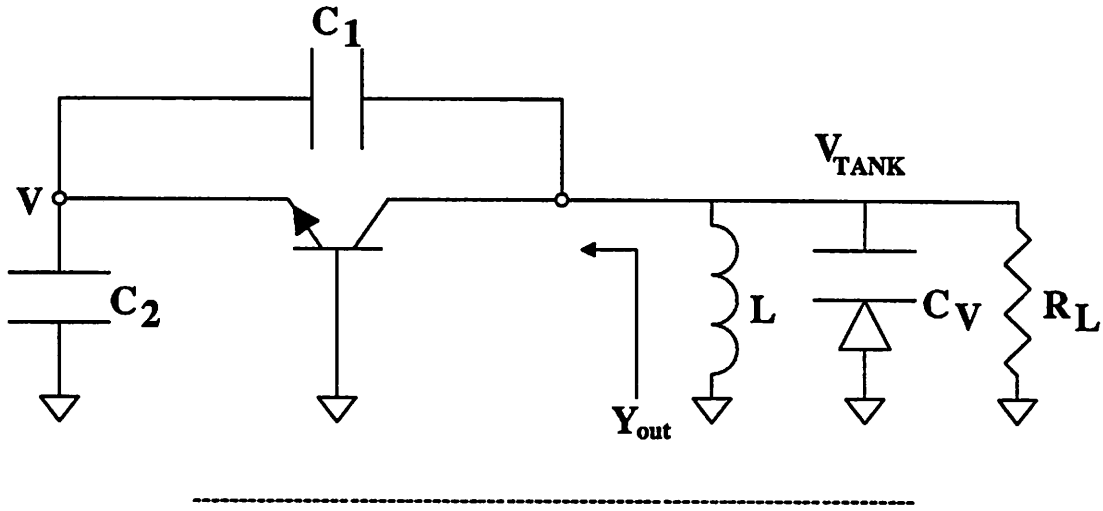


Figure 3.2 - Colpitts oscillator.

where R_L is the loading from the tank circuit. For I_C = 1 mA, C_1 = 1 pF, C_2 = 9 pF, R_L = 1 KΩ, the lower frequency limit turns out to be 390 MHz. Although only small-signal approximations are used so far, SPICE simulations agree very closely with the limits given by equation (3.2.1). Note that, for the values above, R_L has to be greater than 290 ohms so that the right-hand side of equation (3.2.1) is positive. Therefore, even though the bandwith of the common-base stage is very large, the loading from its input terminal restricts the useful bandwith of the circuit.

One way to decrease the loading on the capacitive transformer is to insert an emitter-follower stage as a buffer before the common-base stage. This results in an emitter-coupled pair (ECP) oscillator as shown in Figure 3.3. Now, the input conductance is decreased by a factor of transistor current gain, β, for the same amplifier transconductance, G_m. A similar expression can be derived for the ECP oscillator as it was done for the Colpitts. The final result is:

$$\omega^2 > \frac{{G_m}^2}{\beta^2 (C_1 + C_2) [G_m R_L C_1 - (C_1 + C_2)]} \qquad (3.2.2)$$

For I_C = 2 mA, C_1 = 1 pF, C_2 = 9 pF, R_L = 1 KΩ, and β = 100, the lower frequency limit is equal to 3.6 MHz.

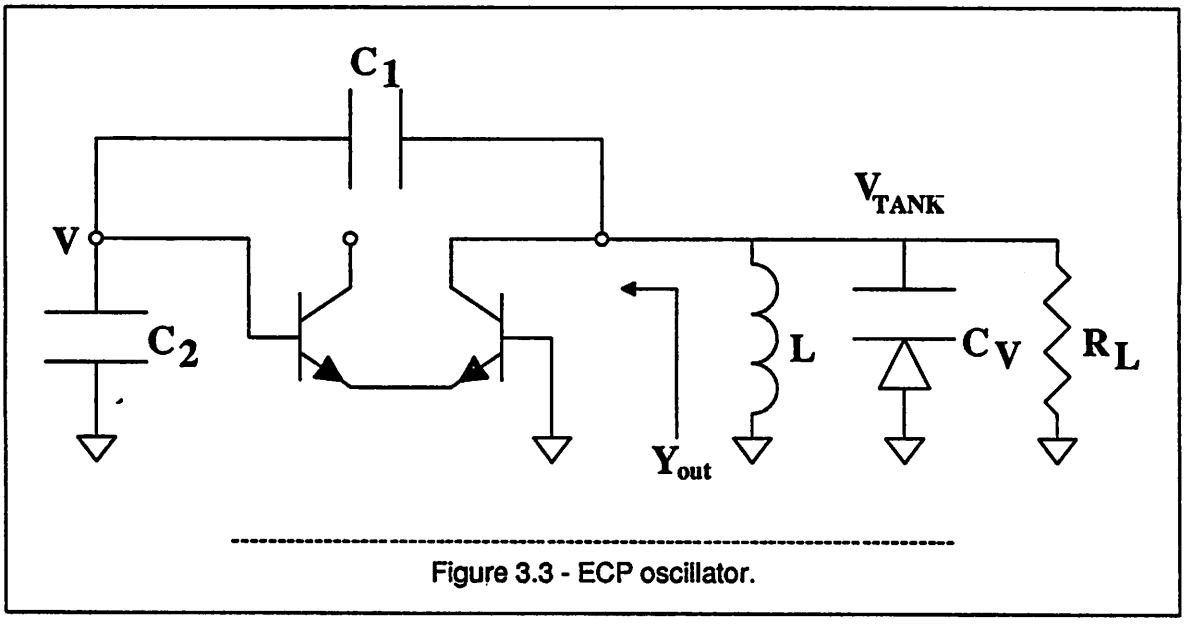


Figure 3.3 - ECP oscillator.

Next, we examine the imaginary part of the amplifier output impedance. For the Colpitts oscillator, it can easily be shown that the output impedance is always capacitive. However, for the ECP oscillator, there exists a frequency below which the output impedance is inductive. This frequency is given by:

$$\omega^2 = \frac{G_m^2}{\beta C_2 (C_1 + C_2)} \tag{3.2.3}$$

For the same values as above, the output impedance is capacitive if the frequency is greater than 64.5 MHz. This means that the circuit will self resonate at 64.5 MHz without a tank circuit at the output. Any capacitance in the tank circuit will reduce that frequency. However, even then, there will be a lower limit on the oscillation frequency for a given tank capacitance. This is so because of the fact that as the value of the inductor is made larger, the impedance of the tank inductor will be much larger than the inductive part of the amplifier output impedance at a low enough frequency. This puts an upper limit on the useful range of external inductance. In any case, ECP oscillator topology is a better choice than Colpitts for frequencies lower than a few hundred MHz.

Let us turn our attention to the higher end of the frequency range that can be achieved with the topologies considered. Since an ECP gain stage has a lower bandwith than a common-base stage, the ECP oscillator is expected to be more limited at the high-frequency end. The low-frequency models used

so far are not very useful any more and device parasitics have to be included in the models. Therefore, extensive computer simulations are required. Let us assume that the loading from the tank circuit is between 250 to 1000 ohms. This is a reasonable assumption since at very high frequencies the losses in the inductor and the varactor diode alone may impose the worst case limitations setting the maximum frequency of operation. To keep the value of C_1 minimum, a practical value of 1 pF is chosen. First, let us examine the Colpitts oscillator. The range of frequencies for which the common-base configuration can provide a negative shunt conductance larger than G_L is shown in Figure 3.4, for a bias current of 1 mA.

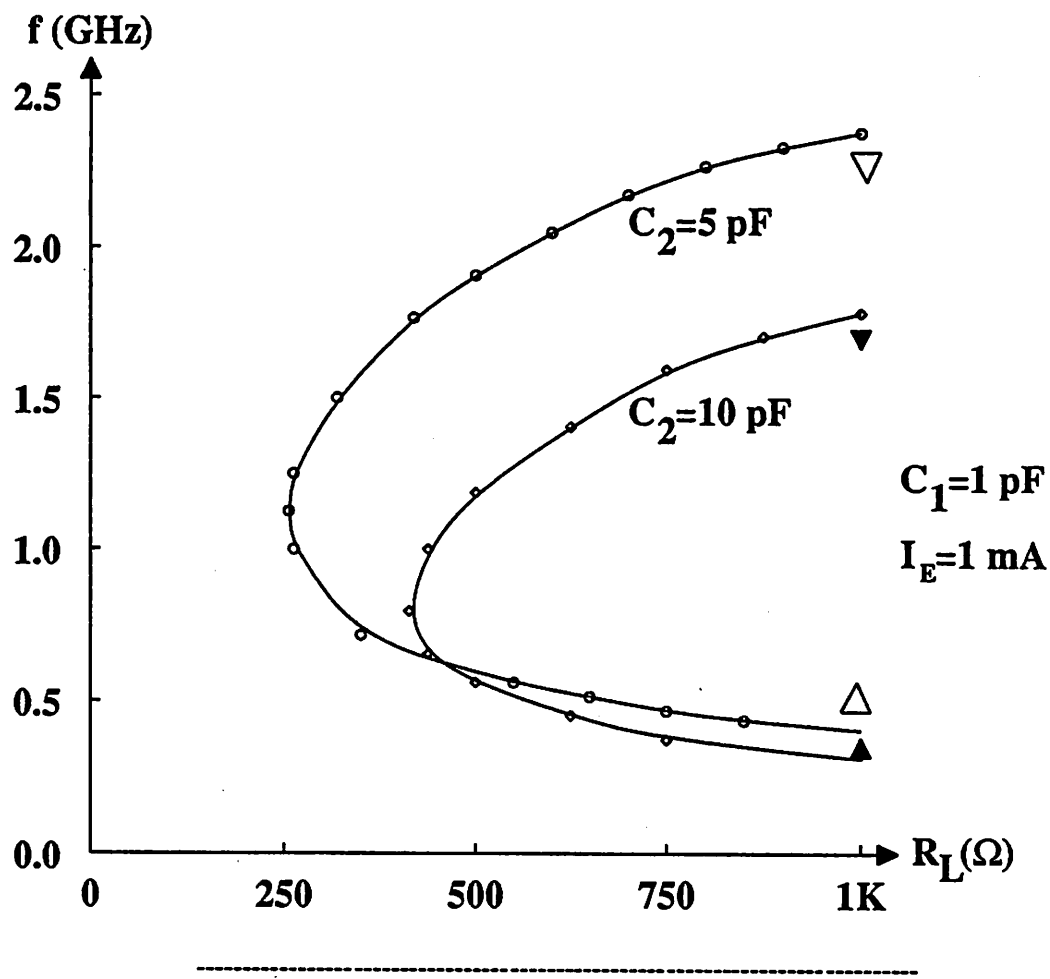


Figure 3.4 - Available range of oscillation frequencies for Colpitts oscillator.

Two curves for C_2 being equal to 5 and 10 pF are shown. The area enclosed by each curve gives the useful range of frequencies for the corresponding value of C_2. The cut-off frequency of the device is close

to its optimum value of 11 GHz. As predicted, the lower frequency range does not extend below 300 MHz even with a 1 KΩ load. The useful range becomes more limited as the loading increased. Similar curves are obtained for different bias conditions and C_2 values. Although the lower limit is always larger than 300 MHz, the upper limit can be more than 5 GHz for a load of 1 KΩ.

A similar set of curves are obtained from the SPICE analysis of the ECP oscillator. In order to obtain the same transconductance, $G_m = \frac{1\,mA}{26\,mV}$, from the ECP, the current in each transistor must be doubled. Two of these curves are plotted in Figure 3.5 for $C_2 = 2$ and 10 pF.

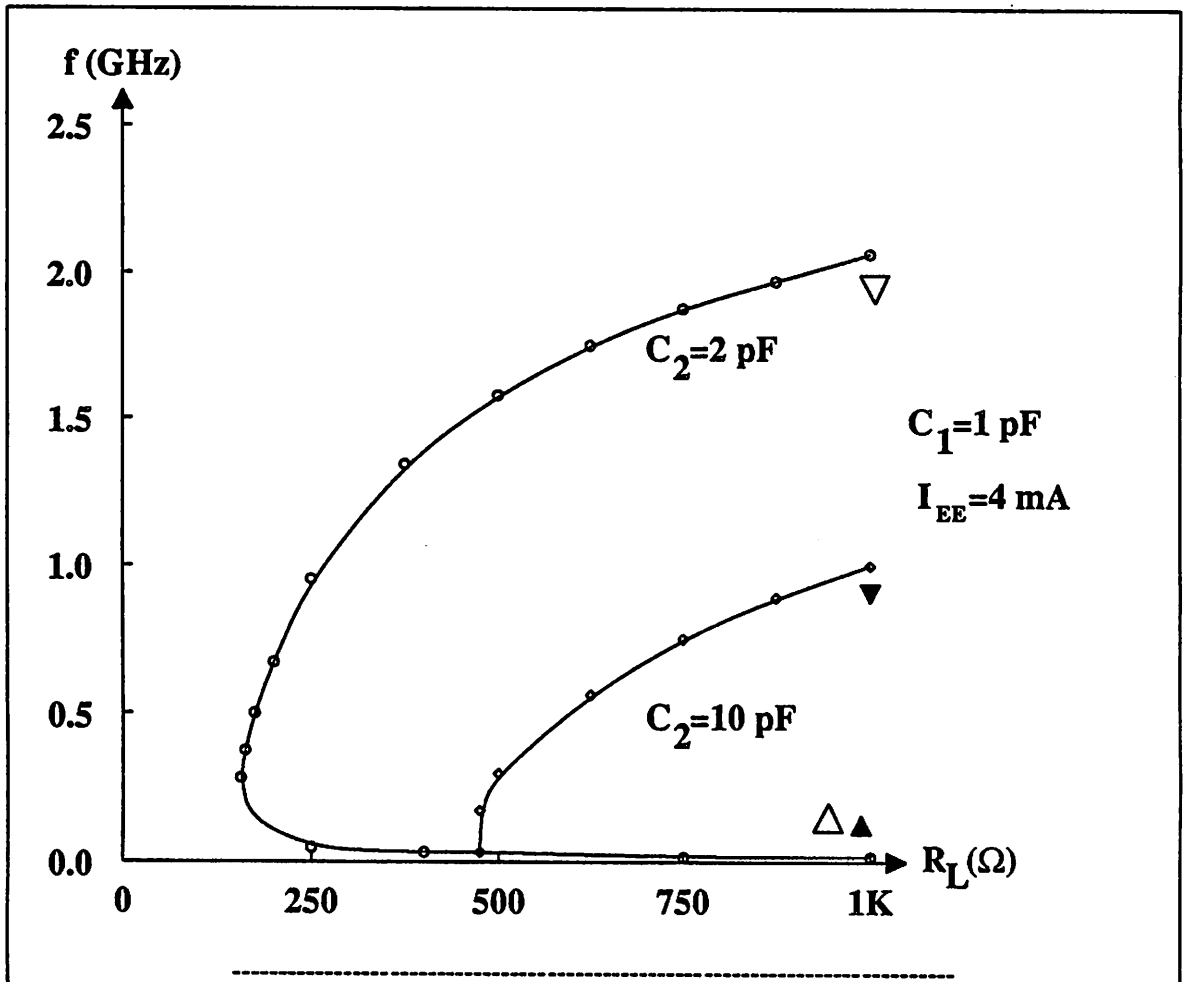


Figure 3.5 - Available range of oscillation frequencies for ECP oscillator.

Both the upper and lower frequency limits are shifted down compared to the Colpitts gain stage. However, assuming that we are interested in the frequency range from 100 MHz to 1 GHz, it is possible to

obtain a negative shunt conductance larger than G_L from the ECP stage by choosing a proper value of C_2 for a given bias current, I_{EE}, and a load, R_L. The maximum design value of C_2 that would result in a large enough negative conductance for the oscillations to start is plotted in Figure 3.6 for I_{EE} = 2 mA and 4 mA.

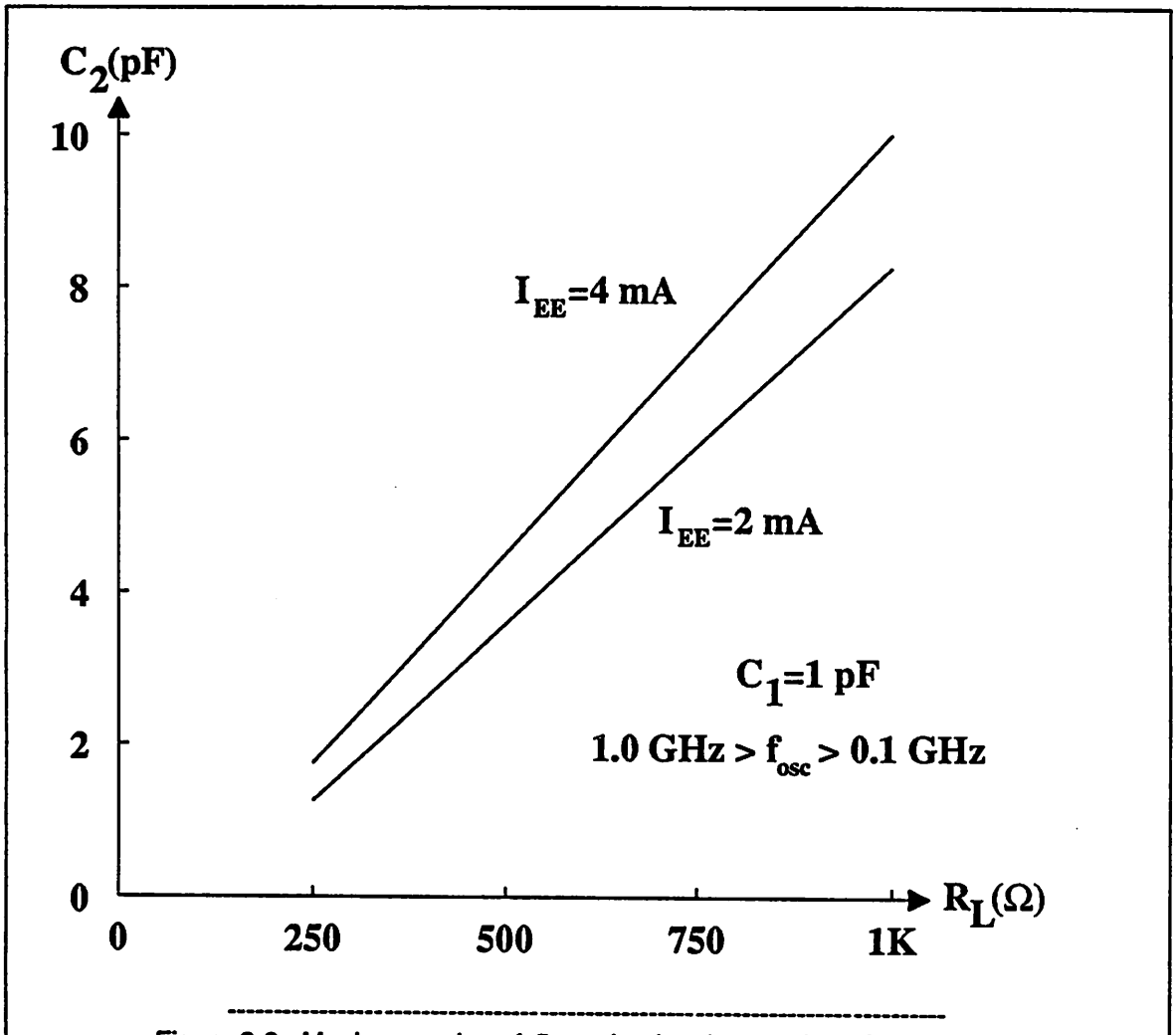


Figure 3.6 - Maximum value of C_2 vs. load resistance for ECP oscillator.

For the worst case loading of 250 ohms, the required design values are less than 2 pF. Higher values can be used if a narrower range of frequencies is required from the design. The conclusion is that the ECP will perform better than the Colpitts for the mentioned frequency range of interest and for a load resistance less than 1000 ohms.

3.3. Varactor Design

The depletion capacitance of a reverse-biased p-n junction is commonly used as a variable capacitance, [76, ch. 2]. The quality factor, Q_V, of a varactor is a function of bias and frequency. At low frequencies, the shunt conductance that represents the leakage current limits Q_V, whereas at high-frequencies, the series resistance is more significant. A typical curve for Q_V as a function of frequency would look like as shown in Figure 3.7.

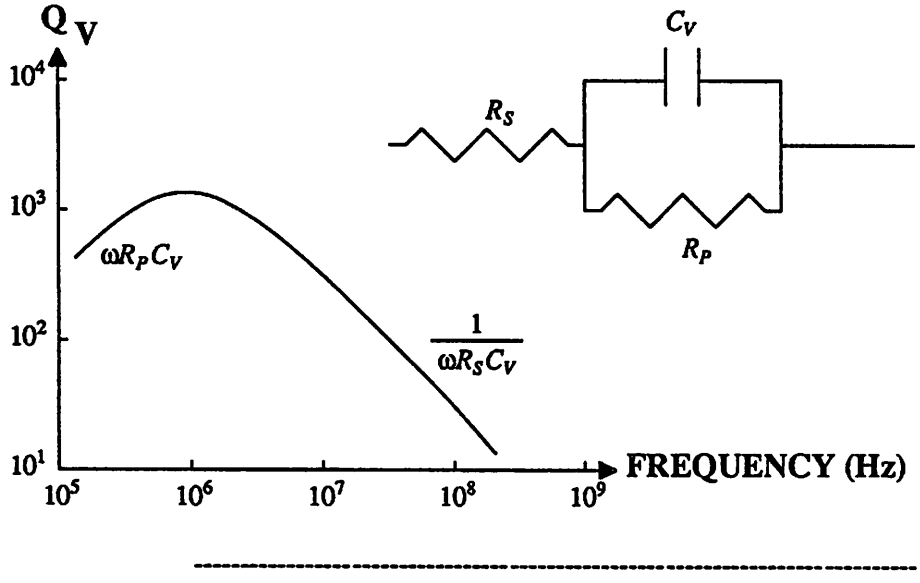


Figure 3.7 - Quality factor of a varactor vs. frequency.

The frequency at which the Q_V is maximum is usually less than a few MHz. Therefore, for frequencies greater than a few MHz, Q_V can be written as:

$$Q_V = \frac{1}{\omega R_S C_V} \tag{3.3.1}$$

Consequently, the R_S–C_V product must be minimized to achieve high Q_V at high frequencies. Although Q_V increases with reverse bias, this increase is limited by the breakdown voltage and the minimum design value of C_V.

Several p-n junctions can be considered for a varactor structure if a high-frequency bipolar process is available. Usually, such a process has a deep-p (DP) implant (or diffusion) for the extrinsic base and a

shallow-p (SP) implant for the intrinsic base. It is assumed that both implants have low enough resistivity to form a good contact with the metal which is usually aluminum. Therefore, in conjunction with the n-type epi layer, they can be used to form a varactor diode without any extra processing steps. Another possibility is the junction formed by the shallow-n (SN) emitter implant and the SP implant. All three structures are shown in Figure 3.8. Double collector and base contacts are used to reduce the collector and base resistances, respectively. A pair of deep-n, (DN), plugs connect the buried layer, (BL), to the collector contacts. Neglecting the metal losses, the dominant sources of series loss are the epi and the buried layer regions, for the base-collector junctions, and the intrinsic base region under the emitter for the base-emitter junction. The sheet resistance of the base implant under the emitter can be as high as 10 to 12 KΩ per square, and therefore it is difficult to obtain a high-quality junction capacitance. Furthermore, the breakdown voltage is lower than that of the base-collector junctions. Although the one-sided abrupt junction approximation is commonly used, in reality, the junction capacitance is determined by the dopant densities on both sides of the junction. Therefore, for the same area, the SP-EPI junction will have a slightly reduced capacitance, hence a higher Q_V, compared to the DP-EPI junction.

Let us consider the SP-EPI structure shown in Figure 3.9 as a unit cell. If the plane of cross-section is designated as the x-y plane, then, W and L are the width and length of the SP-implanted region in the x-(horizontal) and z-(perpendicular to the cross-section) directions, respectively. The maximum distance of interest in the y-(vertical) direction is the epi layer thickness, t_{EPI}. t_{EPI} is usually on the order of a few microns or less for a high-frequency process. If the R_S–C_V product of this unit structure can be minimized with respect to W and L, then any number of these cells can be connected in parallel without degrading the optimum Q_V. This problem is obviously three dimensional, but some simplifying assumptions can still be made. First of all, the contact resistance between the metal (Al) and silicon (Si) will be neglected. Secondly, the skin effect for Al-metal lines will be assumed negligible below 1 GHz. The bottom-wall and the side-wall capacitances will be considered separately, as shown in Figure 3.10. The following resistivities may contribute to the series resistance, R_{BW}, of the bottom-wall capacitance, C_{BW}:

Horizontal: ρ_{Al} for SP, ρ_{BL} for EPI,

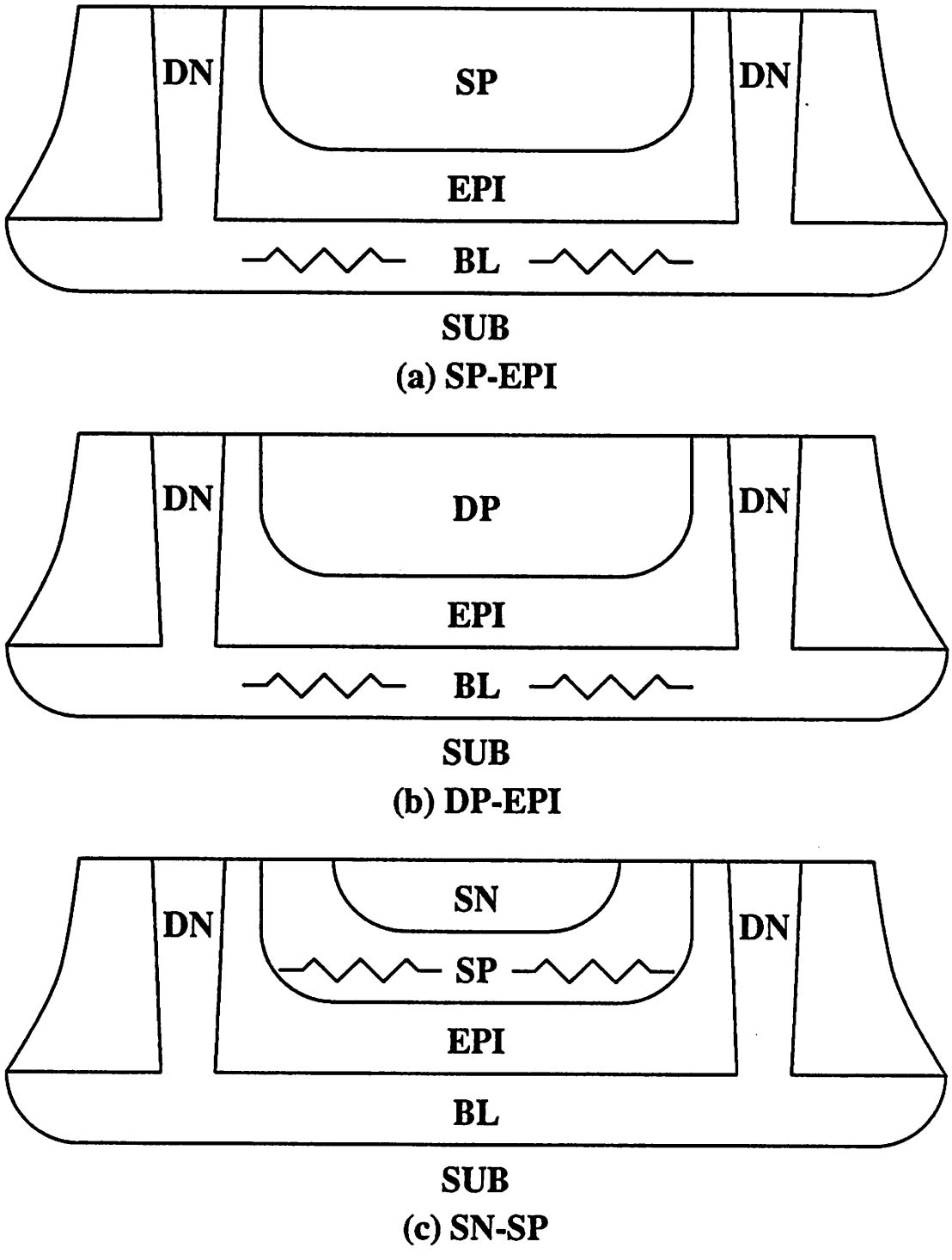


Figure 3.8 - Varactor diode structures in bipolar technology.

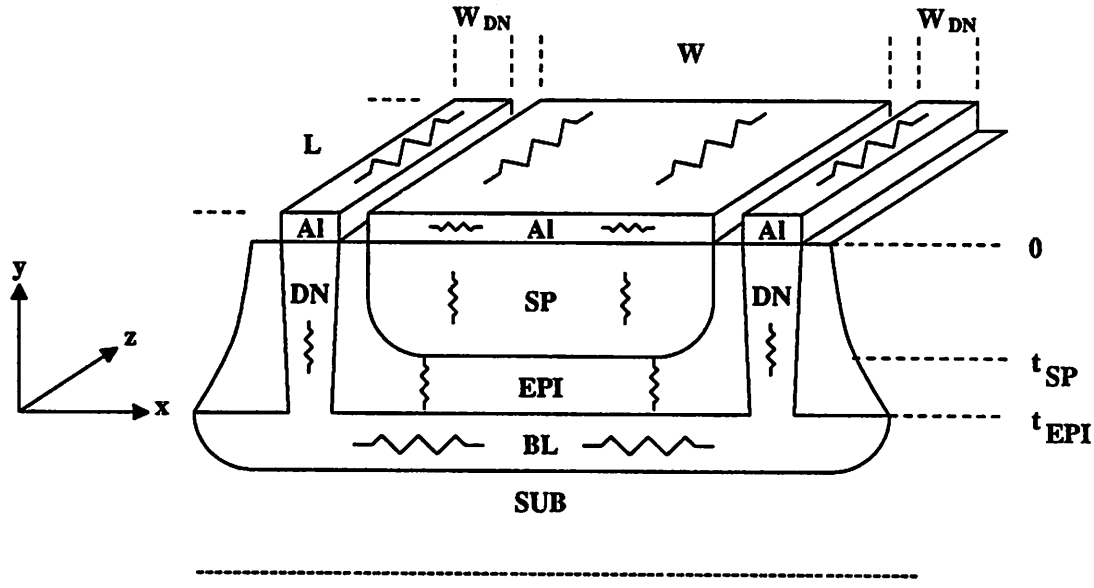


Figure 3.9 - Unit cell structure.

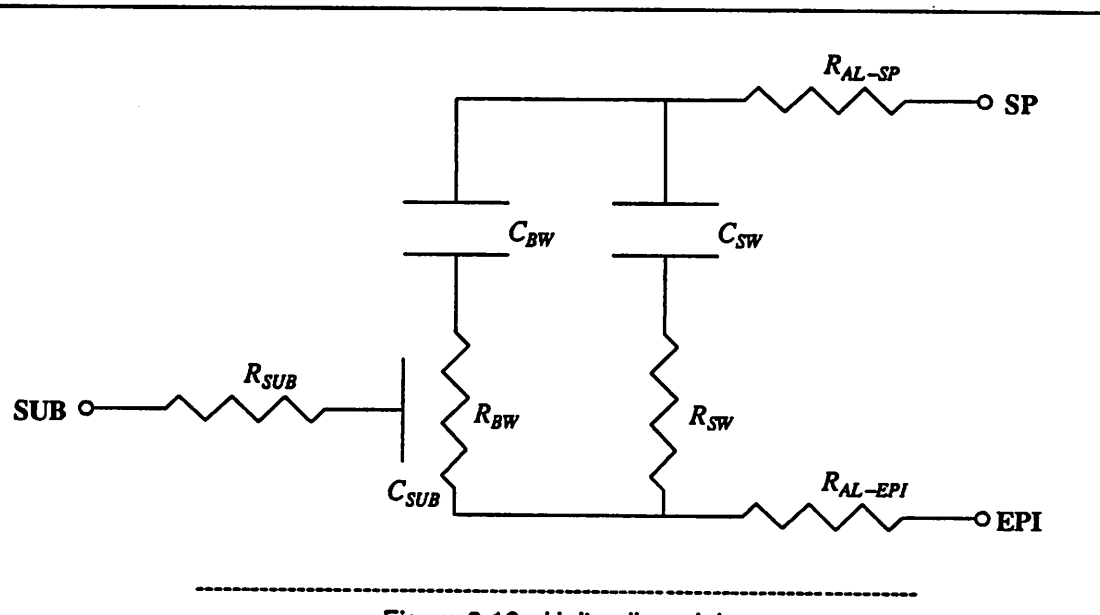


Figure 3.10 - Unit cell model.

Vertical: ρ_{SP} for SP, ρ_{EPI} for EPI,

Perpendicular: ρ_{Al} for SP, ρ_{AL} for EPI.

Similarly, the side-wall capacitance, C_{SW}, has the following resistive components contributing to its

series resistance, R_{SW}:

Horizontal: ρ_{Al} for SP, ρ_{EPI} for EPI,

Vertical: ρ_{SP} for SP, ρ_{DN} for EPI,

Perpendicular: ρ_{Al} for SP, ρ_{Al} for EPI.

The metal losses in the perpendicular direction are modeled by R_{Al-SP} and R_{Al-EPI}, as shown in Figure 3.10. Among the other components, only ρ_{BL} and ρ_{EPI} will be assumed to contribute to R_{BW}, whereas R_{SW} will mainly be determined by ρ_{EPI}. The buried-layer component of R_{BW} can be modeled as a RC-transmission line, [77], and the total bottom-wall loss can be written as:

$$R_{BW} = \frac{1}{12} R_{\square\text{-}BL} \frac{W}{L} + \rho_{EPI} \frac{d_{SP-BL}}{W\,L} \tag{3.3.2}$$

where d_{SP-BL} is the vertical distance between the SP and the BL regions. If the bottom-wall capacitance per area is $C_{\square}$, then one has:

$$C_{BW} = C_{\square} W\,L \tag{3.3.3}$$

One can also show that the side-wall resistance is given by:

$$R_{SW} = \frac{1}{2} \rho_{EPI} \frac{d_{DN-SP}}{L\,t_{SP}} \tag{3.3.4}$$

where d_{DN-SP} is the horizontal distance between the DN and the SP regions, and t_{SP} is the depth of the intrinsic base implant. Finally, C_{SW} can be written as:

$$C_{SW} = 2\,C_l\,L \tag{3.3.5}$$

where C_l is the capacitance per length. Assuming that both branches have a quality factor larger than 10, the quality factor of their parallel combination is given by the following equation:

$$Q_{BW//SW} = \frac{1}{\omega} \frac{C_{BW} + C_{SW}}{R_{BW}\,C_{BW}^2 + R_{SW}\,C_{SW}^2} \tag{3.3.6}$$

It can easily be shown that the equation above is a function of W but not L. Therefore, by taking the

derivative of equation (3.3.6) with respect to W, one can find W_{opt} which maximizes $Q_{BW//SW}$. Then, the effect of ρ_{Al} for a given number of unit cells, n, can be estimated using the following equations:

$$R_{Al-SP} = R_{\square-Al} \frac{L}{n\, W_{opt}} \tag{3.3.7}$$

and

$$R_{Al-EPI} = R_{\square-Al} \frac{L}{n\, W_{DN}} \tag{3.3.8}$$

where W_{DN} is the width of the DN region. Before giving a numerical design example, it is worth mentioning that the substrate capacitance, C_{SUB}, can have a very low quality factor. An AC-short circuit between the epi and the substrate terminals will minimize the effect of the substrate junction.

EXAMPLE

Let us assume that the following parameters are specified for an oxide-isolated bipolar process: ρ_{EPI} = 0.3 Ω/cm, $R_{\square-BL}$ = 32 Ω/□, d_{SP-BL} = 0.6 μ, $C_{\square}$ = 0.4 fF/μ^2, d_{DN-SP} = 3 μ, t_{SP} = 0.4 μ, C_l = 2 fF/μ, $R_{\square-Al}$ = 0.05 Ω/□.

From equations (3.3.2) and (3.3.3), Q_{BW} > 10 if W < 100 μ and f < 1.4 GHz. From equations (3.3.4) and (3.3.5), Q_{SW} > 10 if f < 900 MHz. Substituting these equations into (3.3.6), one can obtain:

$$Q_{BW//SW} = \frac{10^{15}}{\omega} \frac{0.4\, W + 4}{0.427\, W^3 + 288\, W + 72000}$$

where W is in microns. By taking the derivative of $Q_{BW//SW}$ with respect to W and equating it to zero, one can get:

$$W_{opt} = 40\,\mu$$

Substituting this value back into the equation for $Q_{BW//SW}$:

$$Q_{BW//SW} = \frac{28.7}{f}$$

where f is in GHz. Assuming that W_{DN} = 10 μ and using equations (3.3.7) and (3.3.8) :

$$R_{Al-SP} + R_{Al-EPI} = 0.00625 \frac{L}{n}$$

Now, for a zero-bias value of 10 pF, one can write:

$$10^4 fF = n\ (0.4\ W\ L + 4\ L)$$

where W and L are in microns. Therefore, if W = 40 μ, then nL = 500 μ. Choosing n = 5 results in L = 100 μ. Then, one has:

$$R_{Al-SP} + R_{Al-EPI} = 0.125\ \Omega$$

Since $Q_{BW//SW}$ is 28.7 at 1 GHz, $R_{BW//SW} = 0.555\ \Omega$ for C_V = 10 pF. In other words, the total series resistance, R_S, is 0.7 ohms. Therefore:

$$Q_V = \frac{1}{2\pi\ 10^9\ 10^{-11}\ 0.7} = 23$$

A layout sample with n = 5 is shown in Figure 3.11. Because of the various assumptions made in modeling this three-dimensional distributed structure, the above results are optimistic and should be used with caution. However, they are useful in estimating an upper limit for Q_V.

3.4. VCO Design

The complete VCO schematic is shown in Figure 3.12. For the reasons explained in section 3.2, an emitter-coupled pair is chosen as the gain stage for the VCO topology. This topology has the advantage of an isolated output from the tank circuit in addition to a gain stage with high input impedance. The total harmonic distortion is also smaller compared to a single-transistor oscillator since the tanh-nonlinearity of a differential pair has only odd harmonics. As mentioned before, a reverse biased shallow-base to collector-epi junction with buried-layer is used as the varactor diode in this design. The effect of the substrate junction is minimized by connecting the epi-side to the supply potential. Positive feedback is provided by the MOS capacitors C1 and C2. The worst case series resistance of the MOS capacitors can be estimated to be less than 5 ohms using a similar approach as it was done for the varactor. External inductance and capacitance can be used to adjust the center frequency and an external

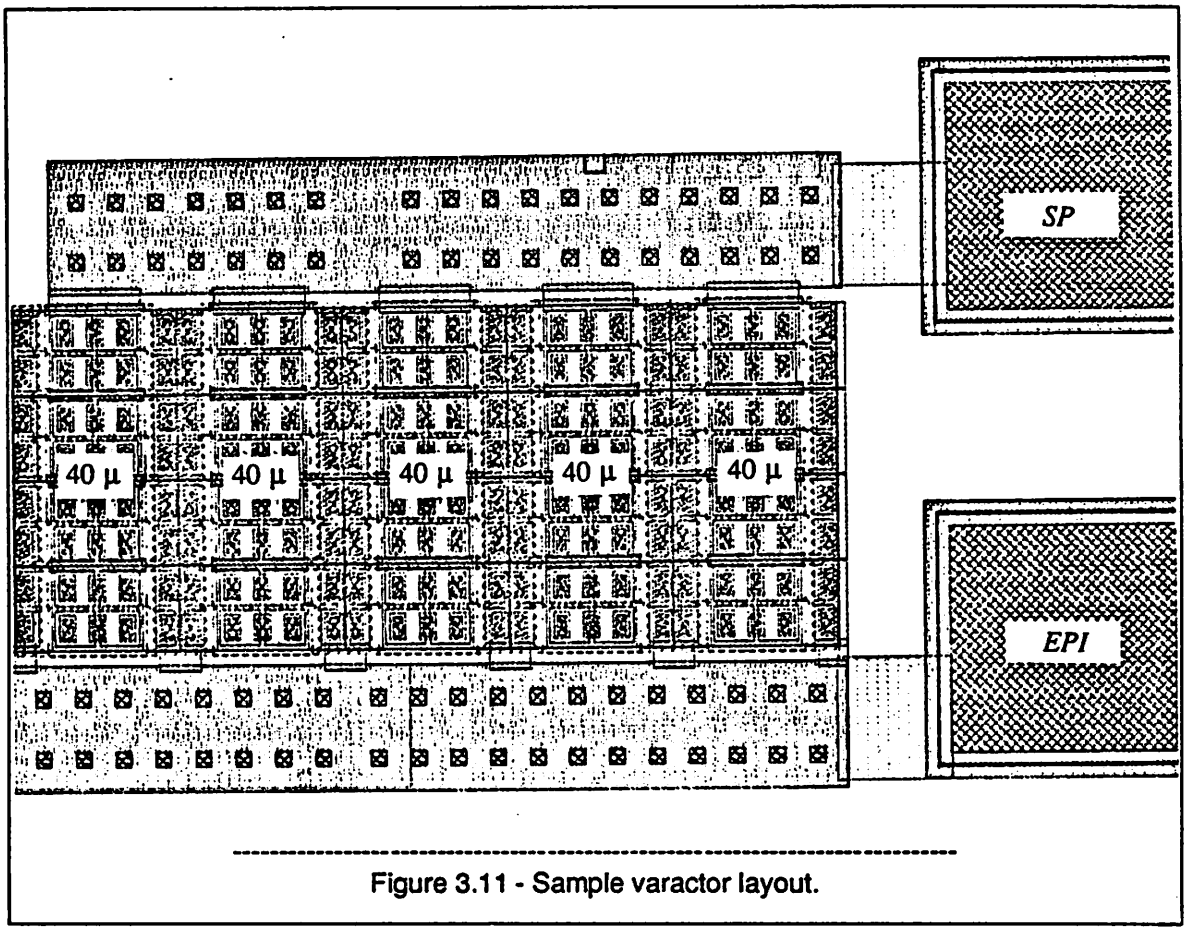


Figure 3.11 - Sample varactor layout.

resistor can be used to obtain the optimum amplitude of oscillation. A clock amplifier follows the VCO to provide a differential drive to the phase detector.

The amplitude of oscillation is a strong function of the losses in the varactor and the inductor at very high frequencies. For instance, if each of them has a Q of 30 with a series resistance of 1 ohm, the equivalent loading on the tank circuit will be 450 ohms. Then, the bias current, I_{EE}, and the transformer ratio, n = $\frac{C_1 + C_2}{C_1}$, have to be chosen accordingly for a given oscillation amplitude. Assuming a peak oscillation amplitude of 500 mV for a worst case loading of 400 ohms, the fundamental current component at the oscillation frequency has to be 1.25 mA. If the signal amplitude at the differential pair input is b times V_T, then, the product b times n must be equal to 20. Choosing b = 5 and n = 4 results in I_{EE} = 2.1 mA from Table 4.6-2 of the reference [70, page 117]. For C_1 = 1 pF, C_2 should be 3 pF. From the negative resistance curves of Figure 3.6, the oscillations are possible almost up to 1 GHz. In reality,

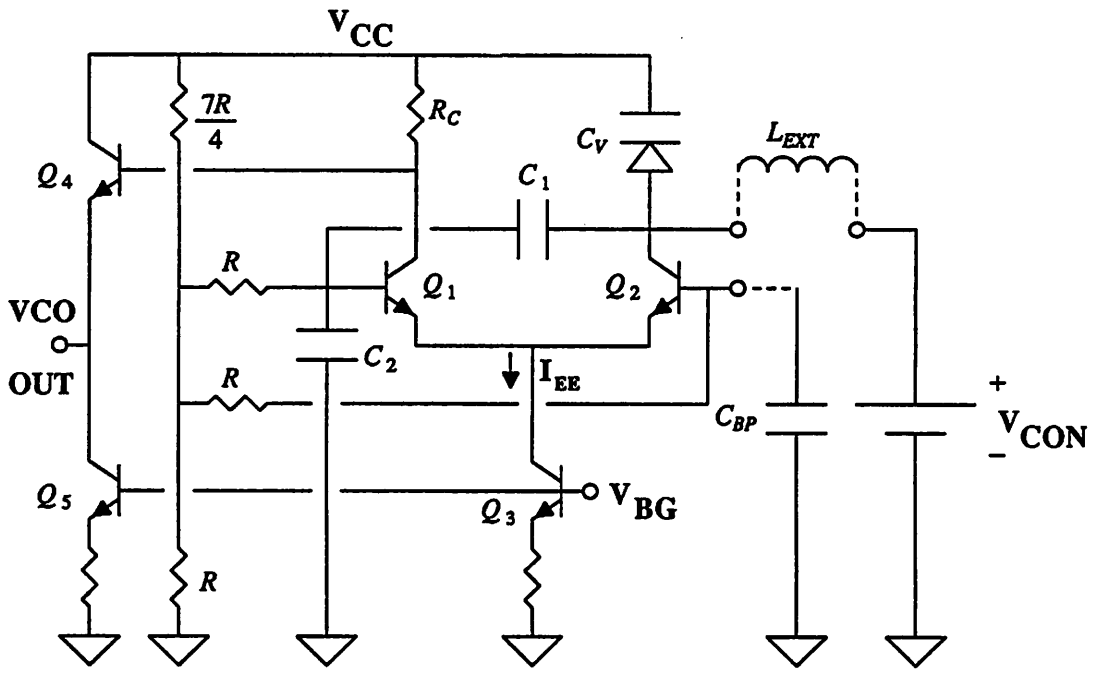


Figure 3.12 - Schematic of the varactor-tuned VCO.

the value of C_2 is designed to be closer to 2.5 pF by taking the parasitic capacitances into account. The varactor capacitance must be much larger than the equivalent MOS capacitance of 0.75 pF for a wide tuning range. Furthermore, if one wants to achieve a loaded tank quality factor greater than 10 at 500 MHz, then:

$$C_V > \frac{10}{2\pi\,(500x\,10^6)\,(400)} = 8\,pF$$

Naturally, at lower frequencies, there will be less loading from the tuning elements of the tank circuit, and therefore, the amplitude will increase. Then, in order to limit the peak amplitude around 1 V, an external resistance of 1 KΩ is required. This, in turn, results in a Q_T of 10 at 200 MHz. The reflected loading from the amplifier input impedance and the bias resistors can be shown to be negligible. The output resistance of the ECP is larger than 20 KΩ for I_{EE} = 2 mA. The extra phase shift introduced by the capacitive feedback circuit is less than 15 degrees down to 50 MHz. The base voltages of the ECP transistors are chosen to be $2V_{BE}$ to keep the current source in the forward active region. Assuming that

the largest control voltage, V_{CON}, available is $V_{CC} - V_{BE}$ and the peak oscillation amplitude is about one V_{BE}, the dynamic range of V_{CON} is limited to $V_{CC} - 4\,V_{BE}$ to keep the common-base transistor in the forward active region.

The AC-schematic of the VCO including the parasitics is shown in Figure 3.13.

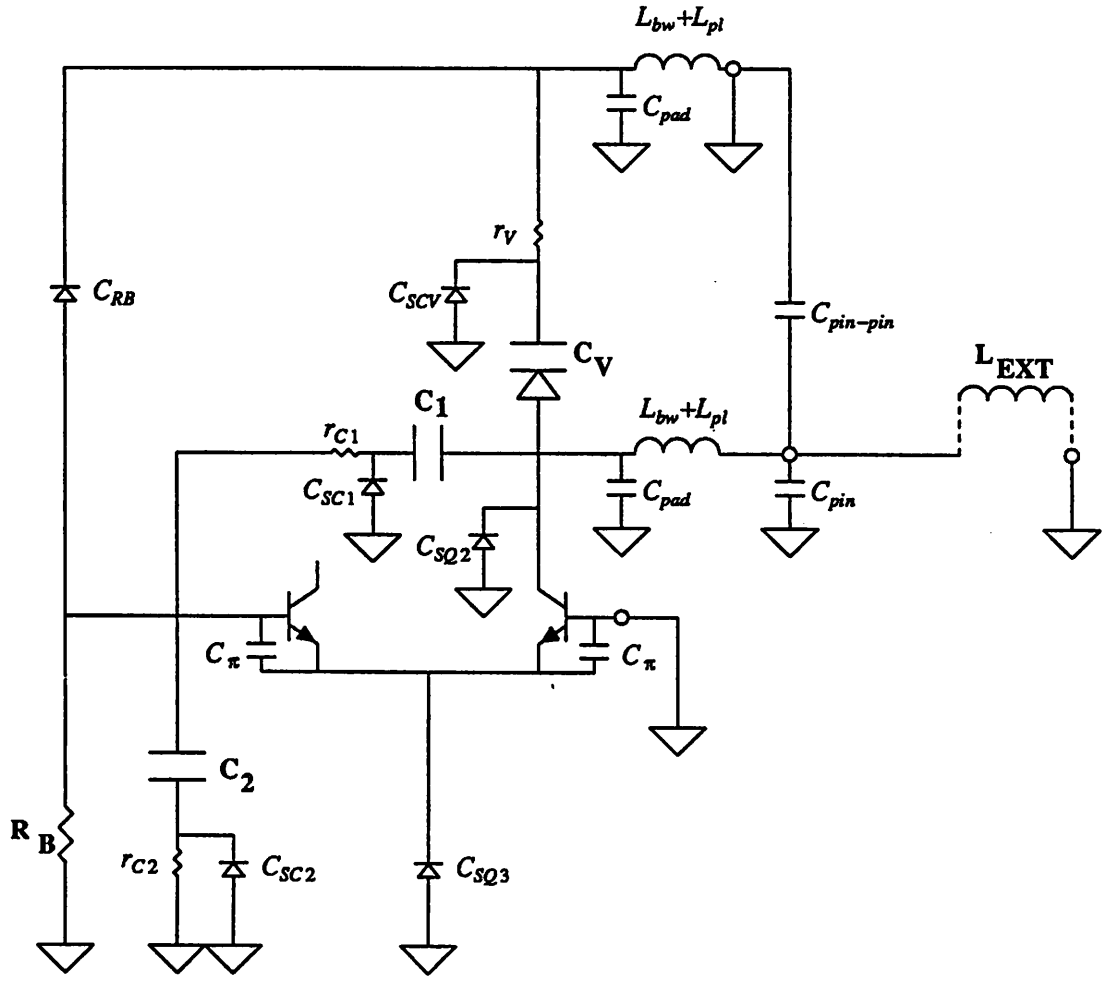


Figure 3.13 - AC-schematic of the VCO with parasitics.

Although a distributed L-C structure similar to a waveguide is a better model for frequencies approaching to 10 GHz, the lumped circuit model is assumed sufficient for frequencies less than 1 GHz. The center frequency of the VCO can be approximated as:

$$f_o = \frac{1}{2\pi\sqrt{(L_{EXT} + L_{bw} + L_{pl})\,(C_V + C_x)}} \qquad (3.4.1)$$

where

$$C_x = \frac{C_1 (C_2 + C_p)}{C_1 + C_2 + C_p} + C_{pad} + C_{pin} + C_{pin-to-pin} \tag{3.4.2}$$

and

$$C_V = \frac{C_0}{\left[1 + \frac{V_R}{V_{bi}}\right]^m} \tag{3.4.3}$$

In the equations above, C_p is the total parasitic capacitance across C_2 including the input capacitance of the gain stage and the substrate capacitance of C_1, and C_0 is the zero-bias value of the varactor capacitance, C_V. The epi-side of the capacitor C_1 is connected to C_2 in order not to load the tank circuit with its substrate capacitance. The epi-side of the capacitor C_2 is connected to the ground potential. At high-frequencies, bonding wire and package lead inductance together with pad and pin capacitance will affect the frequency of operation, and therefore they are also included in the first two equations.

A built-in potential, V_{bi}, of 0.4 V and a grading coefficient, m, of 0.2 are specified for the process used to fabricate the test circuit. The grading coefficient is disappointingly lower than the initially assumed design values of 0.33 to 0.4 due to the outdiffusion from the buried layer into the thin epi region, [78]. If V_R is between 0.8 and 2.8 volts, then C_V varies between $0.66C_0$ and $0.80C_0$. Since the minimum value for C_x is about 1.4 pF, $0.66C_0$ should be at least 7 pF. In other words, C_0 must be larger than 10.6 pF. The minimum tuning range that can be obtained with these values are -5 and +3 percent. Decreasing C_x or increasing C_0 will achieve an upper limit of -5.8 and +3.7 percent. However, the lower limit on C_x depends on the package used and the upper limit on C_0 depends on the practical values of external inductance, hence again on the package, if the chip area is not a crucial factor. For example, for a center-frequency of 500 MHz, a total inductance of 11.0 nH is required if C_0 is 10.6 pF and V_R is 1.8 volts. If the package contributes a pin inductance of 2 nH, then the external inductance should be 9 nH. The varactor also has a series inductance of 2 nH due to the supply pin, and therefore, its self-resonance frequency is 1.3 GHz. Consequently, it will be useful to use multiple pins for the supply to reduce the parasitic inductance for frequencies above 500 MHz. This will also help to reduce the effect of the sub-

strate junction on the varactor impedance. In the final design, a C_0 value of 13.5 pF is used. The estimated substrate capacitance is about 4.5 pF. Employing this varactor, the VCO will have a gain of $-0.051\omega_o$ and $+0.032\omega_o$ rad/(sec-volt). By shifting the V_R range to between 0.4 and 2.4 V, the the tuning range and the VCO gain can be increased to -6.9 and +3.9 percent, and $-0.069\omega_o$ and $+0.039\omega_o$ rad/(sec-volt), respectively. This would require limiting the oscillation amplitude to less than 400 mV.

The schematic of the clock amplifier is shown in Figure 3.14.

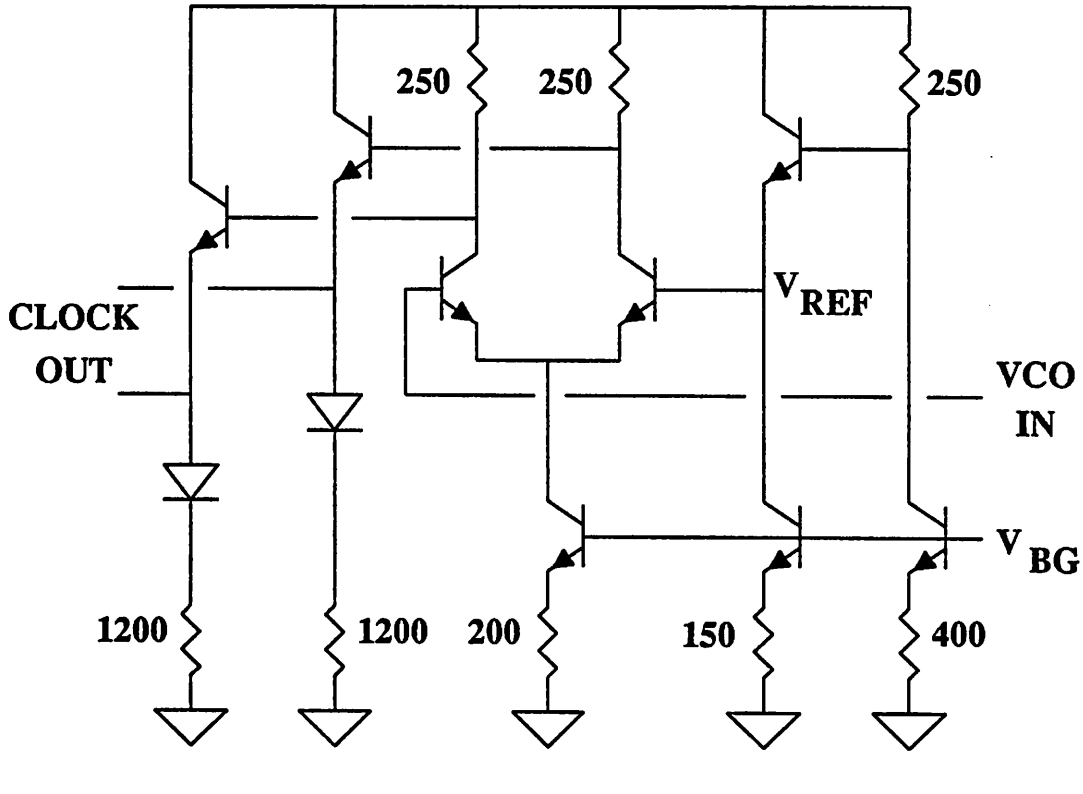


Figure 3.14 - Schematic of the clock amplifier.

It is a single-stage differential pair amplifier with a small-signal gain of 7.5 and a bandwith of 900 MHz. When considered together with the VCO, the clock amplifier behaves more like an ECL-NOR gate with complementary outputs to provide sufficient balanced drive to the phase detector. The input signal amplitude from the VCO can be made close to the oscillation amplitude by choosing an isolated-VCO-output gain of n, the turns ratio of the capacitive transformer. Then, for an oscillation amplitude of 100

mV or larger, the clock amplifier output is more than ± 400 mV. As the oscillation amplitude is increased beyond 200 mV, the differential clock output becomes equal to ± 500 mV by the limiting action of the clock amplifier.

Although the oscillations are nearly sinusoidal and the even-order nonlinearities are negligible, any asymmetry in the VCO gain stage and the clock amplifier will shift the duty cycle of the clock signal away from the ideal 50 percent. Apart from the random mismatches in the transistors of the differential pairs, the following sources contribute to the duty cycle shift:

1. Unequal switching times of the input transistor of the VCO gain stage which serves as a buffer for the common-base transistor. This mismatch between the turn-on and turn-off times becomes negligible as the frequency and the amplitude are decreased.

2. Different base-collector bias voltages and base terminations for the transistors of VCO differential pair.

3. The mismatch between the base voltages of the clock amplifier differential pair. The contribution from this mismatch becomes more significant as the oscillation amplitude is decreased. Therefore, the reference voltage of the clock amplifier must match the VCO output as close as possible.

Under the worst case conditions, the clock waveform duty cycle at 500 MHz is expected to be between 48 and 52 percent from the SPICE simulations. A fully-balanced configuration which will be affected only by the random component mismatches is shown in Figure 3.15. However, any device mismatch in the VCO gain stage will create an offset voltage at the clock amplifier input similar to the third mismatch source mentioned above. Furthermore, the chip area used for the varactors must be increased by a factor of four to achieve the same varactor capacitance as before.

Since the transconductances of all gain stages employed in the VCO design are inversely proportional to the absolute temperature, all the current sources are designed to be proportional to the ratio of a PTAT (Proportional To Absolute Temperature) voltage to a resistor. This helps to minimize the ampli-

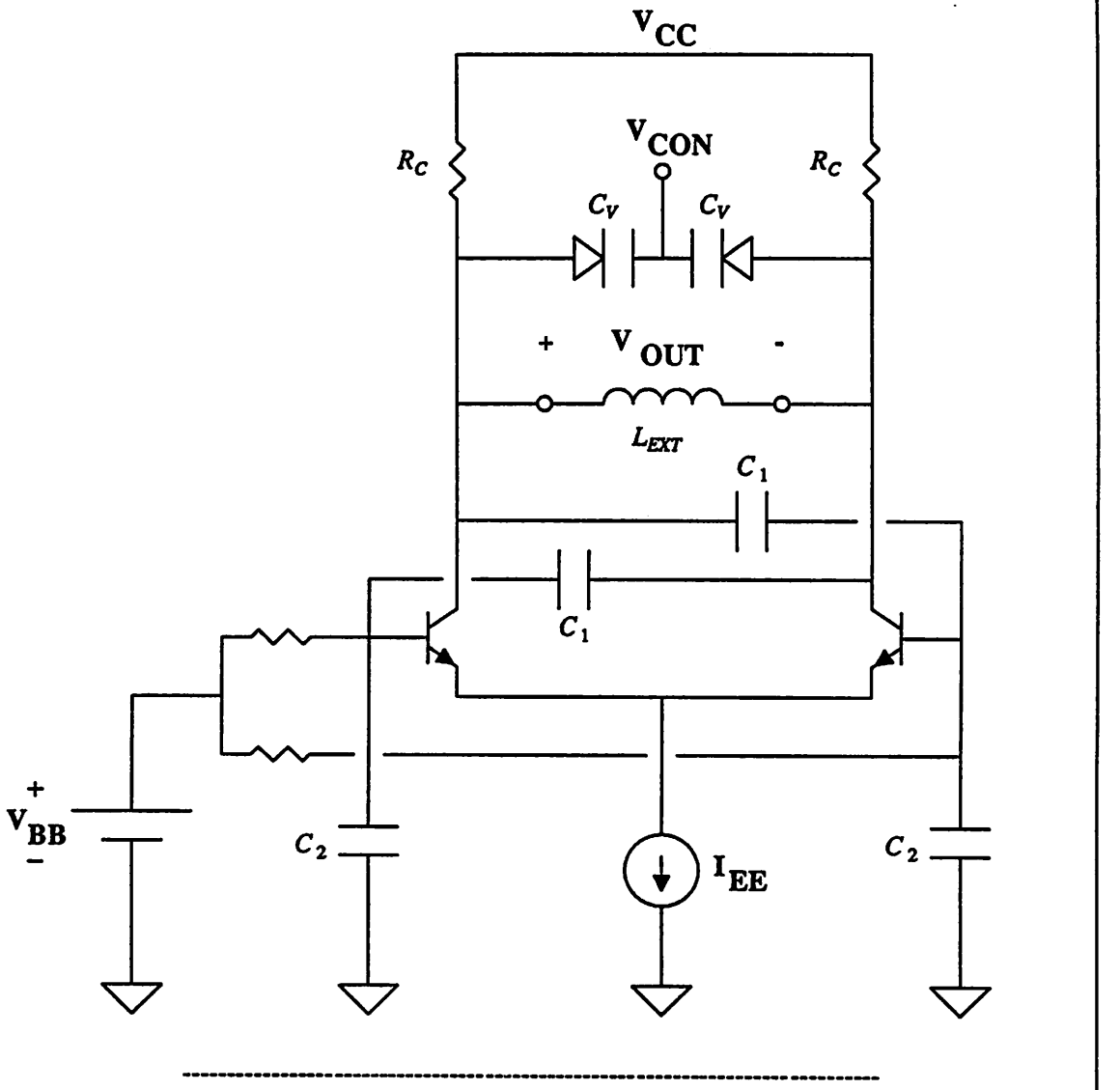


Figure 3.15 - A balanced-VCO schematic.

tude variations with supply and temperature. The reference voltage of the clock amplifier is derived from a bias circuit which mirrors the bias currents in the VCO. Therefore, it tracks the VCO output very closely with supply and temperature. The bandgap reference used to derive the PTAT voltages will be described in the next section.

3.5. Loop Amplifier and Bandgap Reference

A two-stage loop-amplifier with a gain of 50 is designed to achieve a high-gain second-order PLL. Figure 3.16 shows the schematic of the loop amplifier and the VCO.

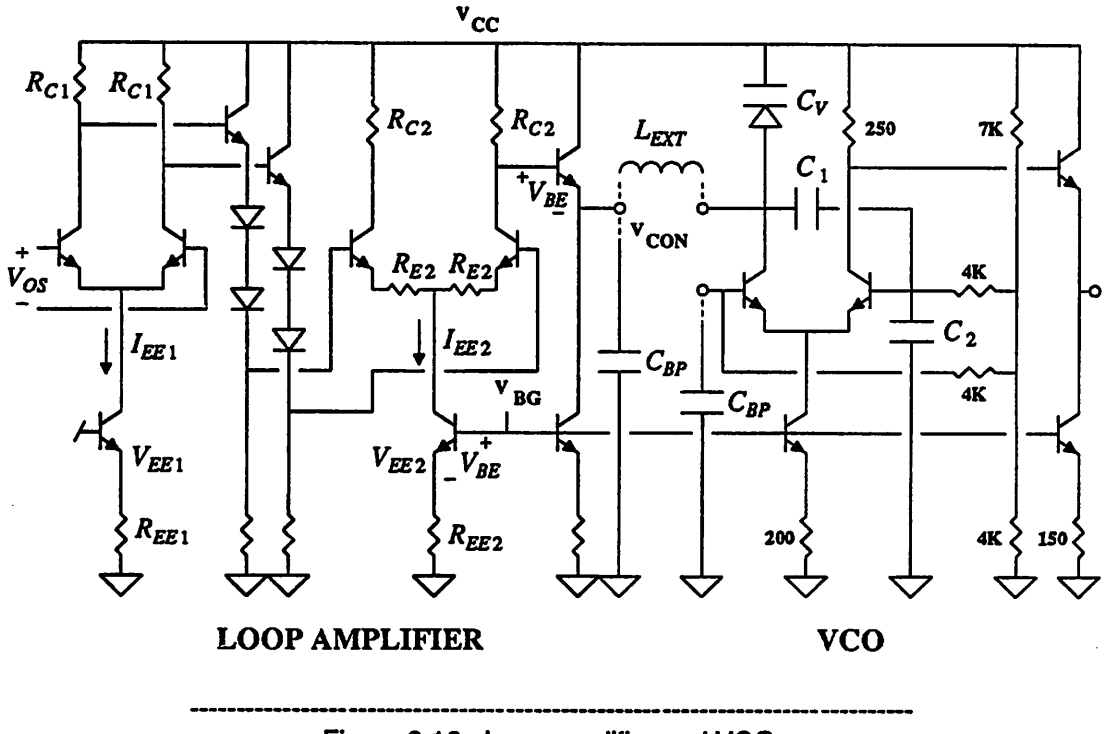


Figure 3.16 - Loop amplifier and VCO.

Assuming a worst case VCO gain of $0.03\omega_o$ rad/(volt-sec) and a worst case phase detector gain of 0.1 volt/rad, a PLL with this loop-amplifier introduces a phase error less than 4 degrees for a pull-in range of ± 1 percent. For an equal contribution from the offset voltages, the total offset voltage from the loop amplifier and the phase detector must be less than 7 mV. In order to minimize the contribution of the level shifting diodes and the second stage to the input offset, the first stage gain is designed to be 20. Large area (10 times the minimum) devices are used to improve the matching throughout the loop amplifier. The bias current of the first stage should be kept low (1 mA or less) to minimize the input offset current and to maximize the input impedance. The bias currents of the second-stage ECP and the emitter follower are high (5 to 6 mA) to achieve a low output impedance. The output impedance is less than 10 ohms at low frequencies and becomes inductive at high-frequencies. The bandwith of the loop

amplifier is not very critical as long as it passes the largest frequency difference between the input and the VCO without much attenuation during capture. This difference is usually less than a few percent of the input frequency. The inherent 3-dB bandwith of the loop amplifier is around 150 MHz. A 10 nF chip capacitor at the output limits the bandwith to 2 MHz. This bypass capacitor is necessary not to degrade the quality factor of the external inductor and to provide some positive phase margin against any parasitic feedback around the loop amplifier.

The low-frequency control voltage at the amplifier output can be written as:

$$V_{CON} = V_{CC} - V_{BE} - 0.5\,R_{C2}I_{EE2} - 0.5\,\frac{0.5\,I_{EE1}R_{C1}}{V_T}\,\frac{0.5\,I_{EE2}R_{C2}}{V_T + 0.5\,I_{EE2}R_{E2}}V_{OS} \qquad (3.5.1)$$

where V_{OS} is the sum of the offset voltages from phase detector output and amplifier input. The reverse bias across the varactor diode is:

$$V_R = V_{CC} - V_{CON} \qquad (3.5.2)$$

and this voltage appears in series with the built-in potential, V_{bi}, of the varactor diode. Therefore,

$$V_{bi} + V_R = V_{bi} + V_{BE} + 0.5\,R_{C2}I_{EE2} + 0.125\,\frac{I_{EE1}R_{C1}}{V_T}\,\frac{I_{EE2}R_{C2}}{V_T + 0.5\,I_{EE2}R_{E2}}V_{OS} \qquad (3.5.3)$$

Let us assume that

$$V_{OS} = \pm 0.2\,V_T \qquad (3.5.4)$$

$$I_{EE1} = \frac{V_{EE1}}{R_{EE1}} \qquad (3.5.5)$$

and

$$I_{EE2} = \frac{V_{EE2}}{R_{EE2}} \qquad (3.5.6)$$

where V_{EE1} and V_{EE2} are the required reference voltages. Then

$$V_{bi} + V_R \simeq V_{bi} + V_{BE} + 0.5\,V_{EE2}\frac{R_{C2}}{R_{EE2}} \pm 0.05\,V_{EE1}\frac{R_{C1}}{R_{EE1}}\frac{R_{C2}}{R_{E2}} \qquad (3.5.7)$$

One possible approach to minimize the temperature dependence of the expression above is to set

$$0.5\,\frac{R_{C2}}{R_{EE2}}\frac{\partial V_{EE2}}{\partial T} = -\frac{\partial}{\partial T}(V_{bi} + V_{BE}) \tag{3.5.8}$$

and

$$\frac{\partial V_{EE1}}{\partial T} = 0 \tag{3.5.9}$$

If

$$R_{C2} \approx 4\,R_{EE2} \tag{3.5.10}$$

and

$$V_{EE2} = V_{BG} - n\,V_{BE} \tag{3.5.11}$$

then from (3.5.8):

$$n \approx 1 \tag{3.5.12}$$

assuming that V_{bi} and V_{BE} have the same TC. Consequently, V_{EE1} can be set equal to the band-gap reference voltage, V_{BG}, and V_{EE2} can be set equal to the voltage difference between V_{BG} and V_{BE}. In this way, the varactor capacitance, hence the VCO center-frequency, can be made independent of supply and temperature to a first order approximation. In general, V_{bi} and V_{BE} have different TCs and the TC of the dielectric constant of silicon, ε_S, cannot be neglected for large reverse bias. If the varactor capacitance can be written as:

$$C_V = \left[\frac{K\,\varepsilon_S{}^{\alpha}}{V_{bi} + V_R}\right]^m \tag{3.5.13}$$

where K, α and m are constant with temperature, then, equation (3.5.10) can be modified as:

$$\frac{R_{C2}}{R_{EE2}} = 2\left[\frac{\dfrac{\partial V_{BE}}{\partial T} + \dfrac{\partial V_{bi}}{\partial T} - (V_{bi} + V_R)\,\alpha\dfrac{\partial \varepsilon_S}{\varepsilon_S\,\partial T}}{\dfrac{\partial V_{BE}}{\partial T}}\right] \tag{3.5.14}$$

$\frac{\partial V_{BE}}{\partial T}$ is found to be -1.5 mV/°C from SPICE simulations at a bias current of 5 mA and over 0 to 100 °C. $\frac{\partial V_{bi}}{\partial T}$ is found to be -2.9 mV/°C both from SPICE and using the equation (24) of [76, ch. 2] which assumes a linearly graded junction. α and $\frac{\partial \varepsilon_S}{\varepsilon_S \, \partial T}$ are assumed to be 2 and 200 ppm/°C, respectively, [79, ch. 2]. Then, from equation (3.5.14), the ratio $\frac{R_{C2}}{R_{EE2}}$ is around 7 for $V_{bi} = 0.4$ V and $V_R = 2.0$ V. This ratio provides a dynamic range of 2.6 volts for the control voltage. Finally, the following resistor values are used in the design: $R_{C1} = 1$ KΩ, $R_{EE1} = 1.2$ KΩ, $R_{C2} = 430$ Ω, $R_{EE2} = R_{E2} = 65$ Ω. With these design values and the assumptions made above, the TC of the VCO center frequency is ideally less than ± 6 ppm/°C for m = 0.2 and over 0 to 100 °C. A 10 percent design error in the resistor ratio increases these limits to ± 25 ppm/°C. Another 20 to 25 ppm/°C will be contributed by the phase shift in the VCO gain stage, the collector to emitter current gain of the devices, the resistor ratios, the MOS capacitors, the parasitic capacitors and the inductors. Considering all the assumptions made above, the TC of the VCO center frequency can be estimated to be between 50 to 100 ppm/°C.

Figure 3.17 shows the schematic of the bandgap reference used in this design. It is a simple two-cell reference circuit without any second order correction, [74], [80]. Q_1 has 8 times the area of Q_2, and therefore, the voltage across R_1 is V_T ln 8 neglecting the device resistances. Due to the PNP current mirror, the current through R_2 is $2\frac{V_T}{R_1}$ ln 8. Hence, the bandgap voltage is given by:

$$V_{BG1} = V_{BE2} + 2\frac{R_2}{R_1} V_T \ln 8 \qquad (3.5.15)$$

Choosing R_1 = 530 ohms results in $I_{C1} = I_{C2} = 0.1$ mA. Then, for the process used to fabricate the test circuit, equation (3.5.15) gives $R_2 = 4.3R_1 = 2280$ ohms. A second bandgap voltage, V_{BG2}, is derived through balancing the circuit with PNP current mirrors as shown in Figure 3.17. This voltage is used to derive all the bias currents in the PLL circuit except the first stage of the loop amplifier. The first stage current bias is set equal to 1 mA by the resistor R_3. The resistor R_4 at the second bandgap output is set equal to $\frac{R_3}{0.7}$ to allow for a load current of 0.3 mA. Several lateral PNP transistors are used in parallel to

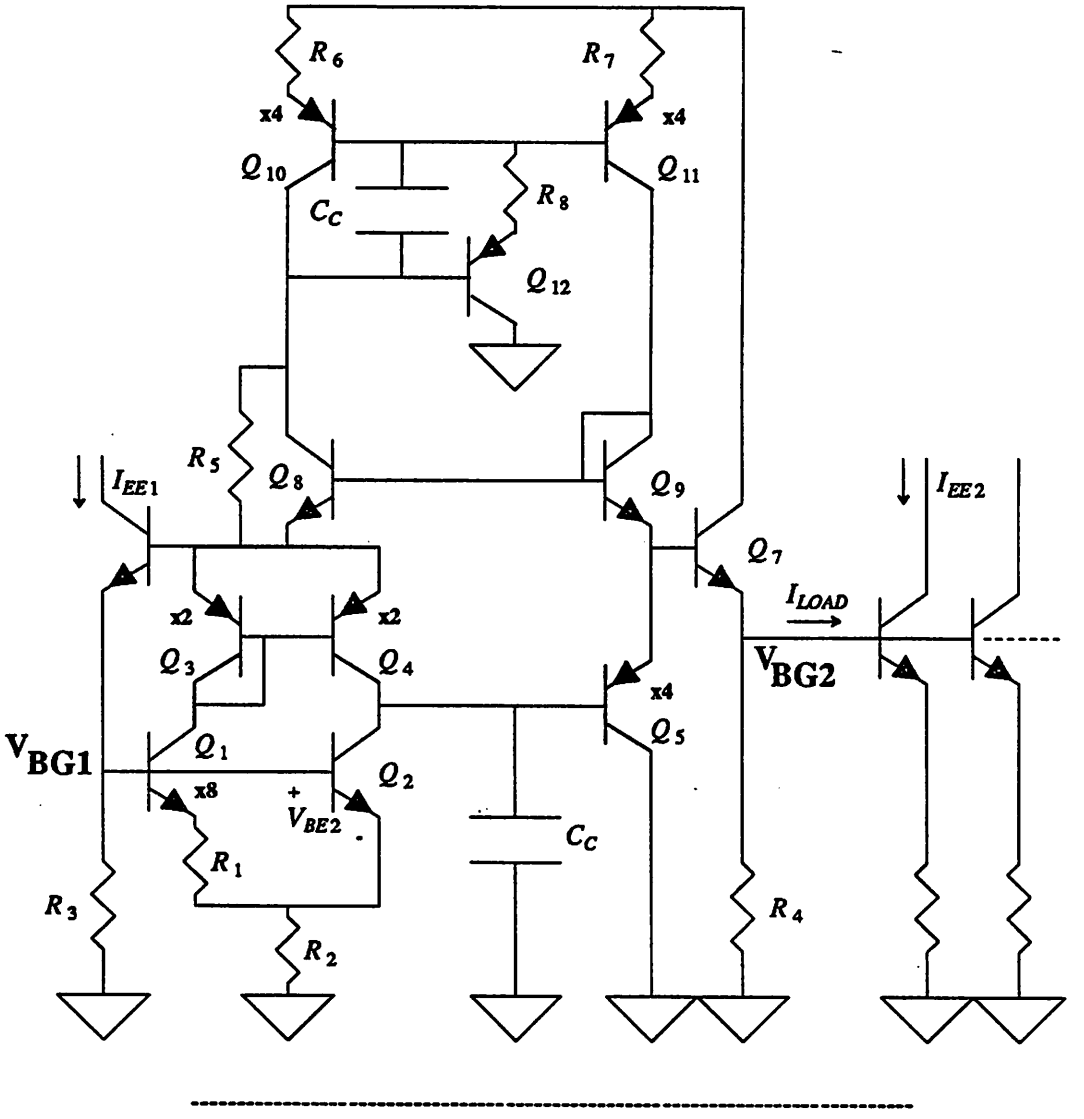


Figure 3.17 - Band-gap reference.

improve the current gain and the matching of the devices. A vertical PNP is used to cancel the base currents of Q_{10} and Q_{11}. R_5 is a 100 KΩ start-up resistor and C_C is a 1.3 pF compensation capacitor. SPICE simulations show a bandgap reference TC better than 65 ppm/°C from 0 to 100 °C. This will contribute less than 10 ppm/°C to the VCO frequency stability.

CHAPTER 4

PHASE DETECTORS

4.1. Introduction

A phase detector, or a phase comparator, is a circuit which compares the phases of two inputs at the same frequency and gives an output voltage proportional to the phase difference. Analog phase locked-loops may employ either analog or digital phase detectors. As long as the control voltage derived from the filter is an analog quantity, one still has an analog PLL. Most common analog phase detectors are the modulator type. They compare the input waveforms over the whole cycle, and hence, are affected by the input amplitudes and duty-cycles. Digital circuits can be either of two types: combinatorial or sequential. An exclusive-OR gate is a combinatorial circuit but it essentially behaves as an overdriven modulator-type phase detector, and therefore, it should be classified as an analog phase detector. On the other hand, a flip-flop is a sequential circuit and affected only by the transition times of the inputs. Besides being insensitive to duty cycles, sequential type circuits have memory, adding significant characteristics to their properties which are not possessed by simple modulator or combinatorial type circuits. Since sequential phase detectors can remember the previous phase difference and compare it with the current one, they have an inherent frequency detection capability in addition to their phase detection property. In this thesis, only this type of circuit will be classified as a digital phase detector. Consequently, the frequency acquisition capability of the PLL strongly depends on the phase detector type used. Analog (modulator and combinatorial type) phase detectors are memoryless and do not have the inherent frequency detection property of the digital (sequential type) phase detectors with memory. Analog frequency detectors which employ R-C filters as memory elements will not be included in this discussion.

As was shown in Chapter 2, a large gain and a small offset are required from a phase detector to minimize the phase error. In order to reduce the phase detector offset voltage, large area devices should

be used whenever possible without degrading the frequency performance. The frequency performance of analog phase detectors is superior to digital phase detectors as will be discussed in the next sections.

One can also classify phase detectors according to their transfer characteristics. Figure 4.1 shows four different phase detector characteristics: sinusoidal, triangular, sawtooth and adaptive.

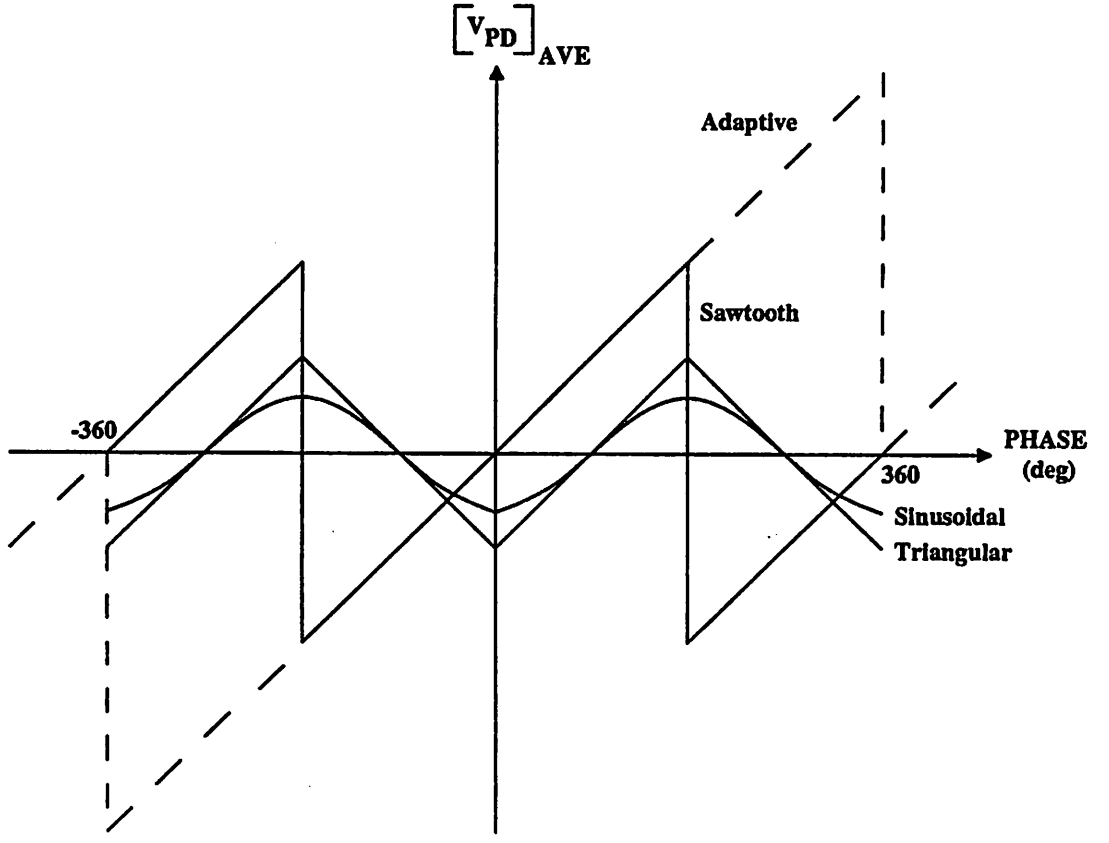


Figure 4.1 - Phase detector characteristics.

A sinusoidal characteristic is obtained from a modulator type phase detector when the PLL input has a small amplitude. A triangular characteristic is obtained when the input amplitude is large, [25, ch. 6], [34, ch. 10]. Ideally, the operating stable point is 90 degrees for analog phase detectors. A sawtooth-shaped transfer curve is obtained when an edge-triggered flip-flop is used as a phase detector, [60]. The stable operating point can be at 0 or 180 degrees. Finally, adaptive phase detectors employ up-down counters and have nonperiodic, but repetitive transfer functions, [59]. They have 0 degrees as their stable

operating point. All these curves are valid for low-frequency and noise-free operation. Furthermore, any loop amplifier with a finite input dynamic range will modify the phase detector characteristics into a near-trapezoidal shape. At high-frequencies and with noise, the triangular characteristics of analog phase detectors degenerate into sinusoidal characteristics. The digital phase detectors function reliably only under low-noise conditions.

4.2. Analog Phase Detectors

The most common analog phase detectors are modulators or mixers. A double-balanced modulator forms the basis of well-known four-quadrant multiplier, [34, ch. 10]. Similarly, the core of a two-quadrant multiplier is a single-balanced modulator. Although it is possible to implement these circuits using either transistors or diodes, transistors are active devices and hence they are preferred for higher phase detector gain. They also possess the same matching properties as diodes in integrated circuit implementations. It is interesting to note that a double-balanced modulator and an exclusive-OR gate have the same truth table for large input signals. Similarly, a single-balanced modulator can be "implemented" using combinatorial logic gates for high-level signals. All of these implementations have the common property that the complete waveforms within a cycle are compared by the phase detector. One consequence of this property is that the average output of an analog phase detector is sensitive to the duty cycles of the input waveforms. Another consequence is that one can obtain a sinusoidal or a triangular characteristics depending on the input signal level.

If a double-balanced modulator is used as the phase detector, the output is a replica of the VCO waveform when there is no input signal to the PLL as shown in Figure 4.2. Therefore, if the VCO does not have a 50 percent duty cycle, the phase detector output will have a DC-offset. A single-balanced modulator type circuit is proposed to eliminate this offset as shown in Figure 4.3. The differential output waveform can have three levels, hence this circuit is also called a tristate phase detector, [14]. Whenever there is no input signal, the phase detector output is ideally zero. Therefore, the VCO asymmetry has almost no effect on the tristate phase detector output for no input signal case. In the following para-

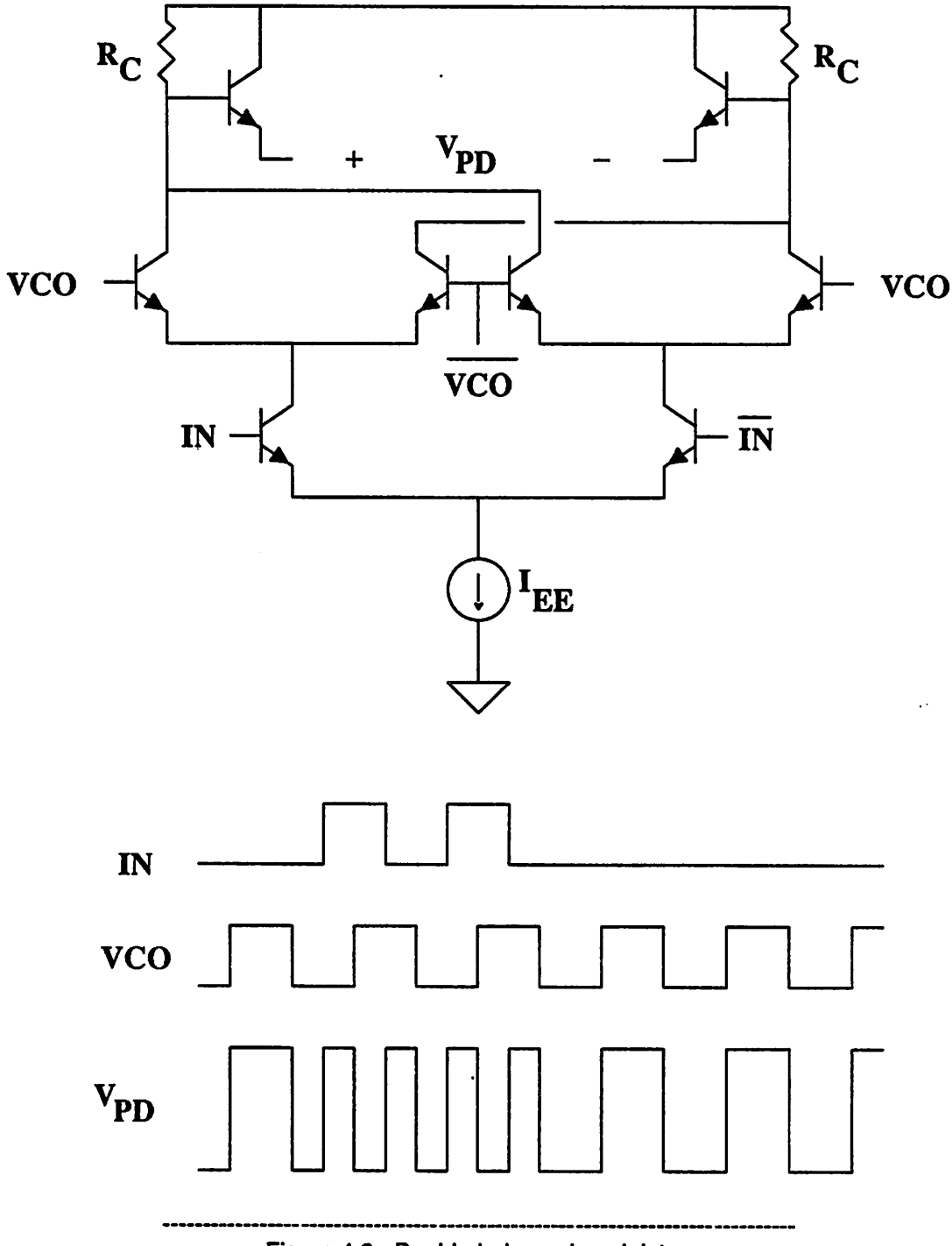


Figure 4.2 - Double-balanced modulator.

graphs, the static and dynamic performance of these two phase detector circuits will be compared in detail.

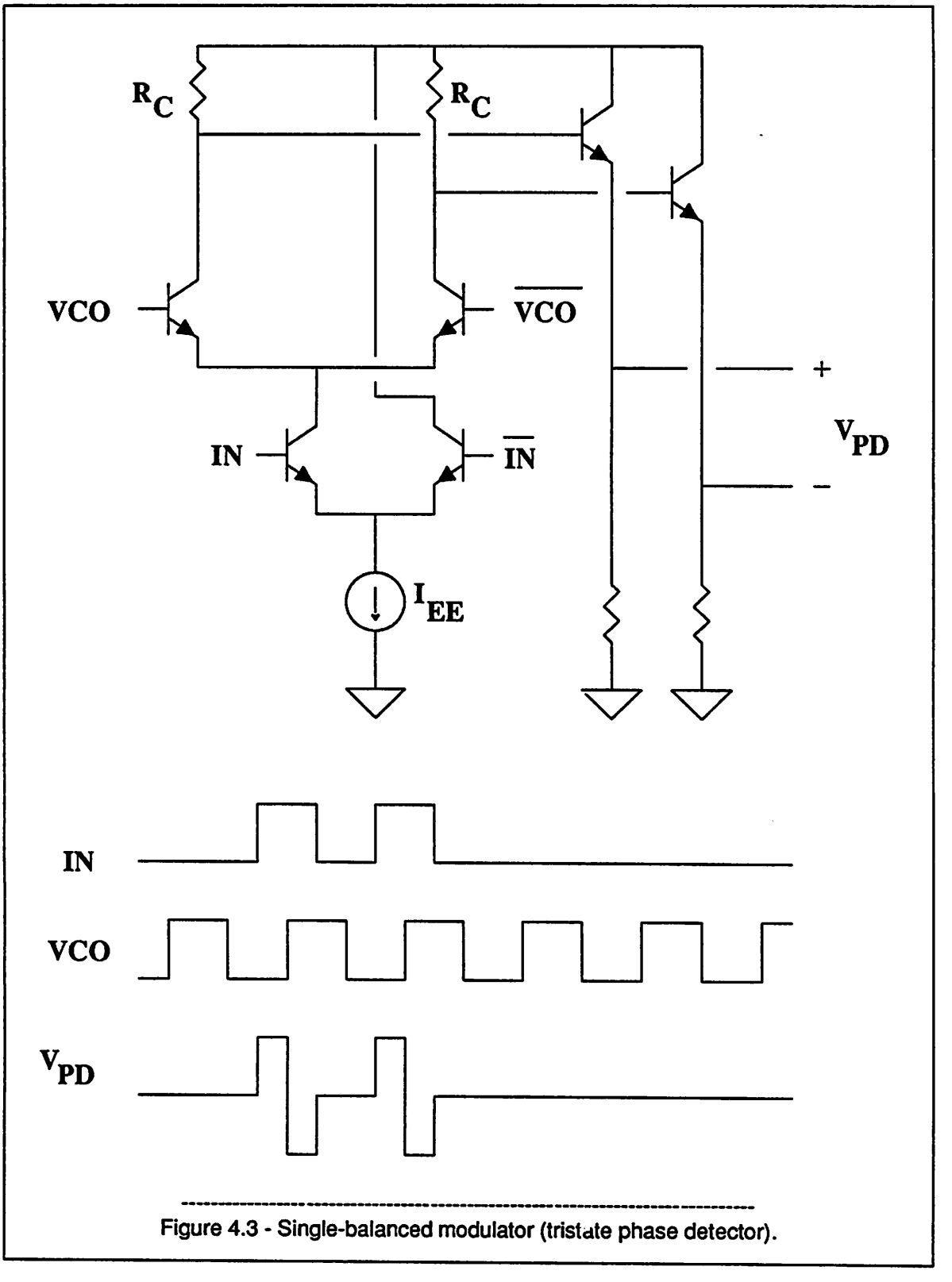


Figure 4.3 - Single-balanced modulator (tristate phase detector).

There are two parameters which define the static performance of a phase detector, its gain and DC-offset. First, let us assume that all the input transitions are present, i.e. the PLL input is a deterministic signal. It can be easily shown that the phase detector gain is:

$$K_{PD} = \frac{R_C I_{EE}}{\pi} \tag{4.2.1}$$

for a single-balanced modulator and

$$K_{PD} = 2\frac{R_C I_{EE}}{\pi} \tag{4.2.2}$$

for a double-balanced modulator.

In a practical circuit, V_{BE} mismatch between the output emitter followers and R_C mismatch between the load resistors contribute to the DC-offset. Therefore, large-area devices and wide resistors should be used to minimize these contributions. Bias currents must be kept low enough to minimize the effect of the emitter resistor mismatch in the devices. For large input signals, the DC-offset voltage is given by:

$$V_{OS} = \Delta V_{BE} + \frac{I_{EE}\,\Delta R_C}{4} \tag{4.2.3}$$

for a single-balanced modulator and

$$V_{OS} = \Delta V_{BE} + \frac{I_{EE}\,\Delta R_C}{2} \tag{4.2.4}$$

for a double-balanced modulator. The static phase error introduced by a phase detector can be written as:

$$\Theta_e = \frac{V_{OS}}{K_{PD}} \tag{4.2.5}$$

Now, let us consider the random data input case. If there are no input transitions, the second term in equation (4.2.3) becomes zero whereas equation (4.2.4) remains the same. Since the remaining terms are present all the time and can only be corrected when there are transitions in the data, the effective phase detector gain to be used in equation (4.2.5) is reduced by a factor of two (assuming equally likely

data) for all the terms in equations (4.2.3) and (4.2.4) except the second term in equation (4.2.3). Therefore, the static phase error for a single-balanced modulator is:

$$\Theta_e = \pi \left[\frac{2\,\Delta V_{BE}}{I_{EE}\,R_C} + \frac{\Delta R_C}{4\,R_C} \right] \tag{4.2.6}$$

Similarly, the static phase error for a double-balanced modulator is:

$$\Theta_e = \pi \left[\frac{\Delta V_{BE}}{I_{EE}\,R_C} + \frac{\Delta R_C}{2\,R_C} \right] \tag{4.2.7}$$

As it can be seen from the last two equations for equally likely data, the static performance of the tristate phase detector can be made better than that of the double-balanced modulator by increasing the phase detector gain.

The dynamic performance of a phase detector is of interest during capture. As it was discussed in Chapter 2, there is a minimum pull-in range requirement from a PLL which is given by:

$$\Delta\omega_P \geq K_{AMP}\,K_{VCO}\,\Delta V_{CON} \tag{4.2.8}$$

where ΔV_{CON} includes not only the average of V_{OS} for equally likely data, but also a component, V_{AOS}, which is a function of the duty cycles of the input and the VCO. As the frequency difference goes to zero, the phase detector output waveform approaches to the phase detector characteristics. It can easily be shown that when one of the inputs has a duty cycle different from 50 percent, an analog phase detector will have a trapezoidal characteristic instead of a triangular one. Whether the average of the phase detector characteristics over a period will still be zero depends on the circuit and the duty cycle of the other input. For a tristate phase detector, the average output as the frequency difference goes to zero can be shown to be

$$V_{AOS} = R_C\,I_{EE}\,D_{IN}\,(1 - 2\,D_{VCO}) \tag{4.2.9}$$

where D_{IN} and D_{VCO} are the duty cycles of the input and the VCO, respectively. Hence, it is possible to reduce this "acquisition offset" voltage by employing narrow input pulses. For a double-balanced modulator equation (4.2.9) becomes:

$$V_{AOS} = R_C\, I_{EE}\, (2\, D_{IN} - 1)(1 - 2\, D_{VCO}) \tag{4.2.10}$$

Therefore, deterministic input signals with duty cycles close to 50 percent result in a smaller acquisition offset with a double balanced modulator. On the other hand, an input signal with a duty cycle less than 1/3 yields a smaller acquisition offset voltage when a tristate phase detector is used instead of a double-balanced modulator.

However, D_{IN} is zero when there is no input transition at the PLL input, that is when a zero bit is received, and V_{AOS} becomes zero for a tristate phase detector from equation (4.2.9). Using equations (4.2.3) to (4.2.4) and (4.2.8) to (4.2.10) for equally likely random data, one can show that:

$$\Delta\omega_P \geq K_{AMP}\, K_{VCO} \left[\Delta V_{BE} + \frac{\Delta R_C\, I_{EE}}{8} + 0.5\, R_C\, I_{EE}\, D_{IN}\, (1 - 2\, D_{VCO}) \right] \tag{4.2.11}$$

for a single-balanced modulator and

$$\Delta\omega_P \geq K_{AMP}\, K_{VCO} \left[\Delta V_{BE} + \frac{\Delta R_C\, I_{EE}}{2} + R_C\, I_{EE}\, (1 - D_{IN})(1 - 2\, D_{VCO}) \right] \tag{4.2.12}$$

for a double-balanced modulator. The conclusion is that the tristate phase detector is a better choice if the duty cycle of the equally likely data waveform is less than 2/3. If the VCO duty cycle is 50 percent, the tristate phase detector always has a better dynamic performance for both deterministic and random input signals.

At low frequencies, it is usually assumed that there is a 90° phase difference between the two phase detector inputs when the PLL is in lock. However, this phase difference is also duty cycle dependent. In other words, the phase difference which produces a zero average output is a function of the input duty cycles. The zero output point can be found by plotting the phase detector characteristics for arbitrary duty cycles, D_{IN} and D_{VCO}. The final results are given by:

$$\Phi_o = \pi\, D_{IN} \tag{4.2.13}$$

for a tristate phase detector, and

$$\Phi_o = \pi\, (0.5 + D_{IN} - D_{VCO}) \tag{4.2.14}$$

for a double-balanced modulator. As it can be seen from the equations above, random variations in the VCO duty cycle do not create phase error (jitter) for the tristate phase detector.

At high frequencies, this phase difference may be different from 90°, even for inputs with 50 percent duty cycle, since there is a phase shift introduced by the phase detector circuit itself. (About 4° at 500 MHz for a tristate phase detector with a 10 GHz process). This phase shift is frequency, temperature and supply dependent and can degrade the circuit performance above a few hundred MHz. The phase detector bias current, I_{EE}, can be derived from a band-gap reference circuit to reduce that dependence.

The bandwith of the phase detector must be large enough to pass the beat frequency signals as high as ± 5 percent of the center frequency, f_o, and must lie well above the loop bandwith so that no undesirable phase shift is introduced. For small-signal PLL inputs, the tristate behaves like a sinusoidal phase detector. The circuit can be considered as a cascode connected amplifier for every half cycle of the VCO waveform. Therefore, the small-signal bandwith of the tristate phase detector can be estimated as:

$$f_{-3dB} = \frac{1}{2\pi[(R_S + r_b)(C_e + g_m\tau_F) + R_C(C_{co} + C_c + C_s)]} \qquad (4.2.15)$$

where C_{co} represents the loading from the emitter follower stage, [34, ch. 7]. This approximation yields a bandwith about 1.0 GHz for I_{EE} = 2 mA, R_S = 50 ohms, R_C = 200 ohms, and with double-base, 2 by 10 micron-square emitter-area transistors. Computer simulations show a small-signal bandwith of 1.3 GHz. These estimates become conservative when the tristate input swings are comparable to or larger than V_T. Then, one might use the large-signal time constants which are smaller than the ones used in equation (4.2.15) above, [17]. However, for large signals the phase detector characteristics are not exactly sinusoidal (triangular at low frequencies, more and more sinusoidal at higher frequencies) as shown in Figure 4.4. Hence, the phase detector gain (ideally the slope around 90° phase) and the peak value of the characteristics (ideally for 0° or 180° phase) may have different bandwith. Since we are interested in the bandwith of the phase detector gain, unless the sinusoidal approximation holds (i.e. the operating frequency is high enough), one has to depend on the computer simulations. For ± 200 mV VCO swing, SPICE gives a tristate bandwith of 2, 5, and 8 GHz for input amplitudes of ± 20, ± 100, and ± 200 mV,

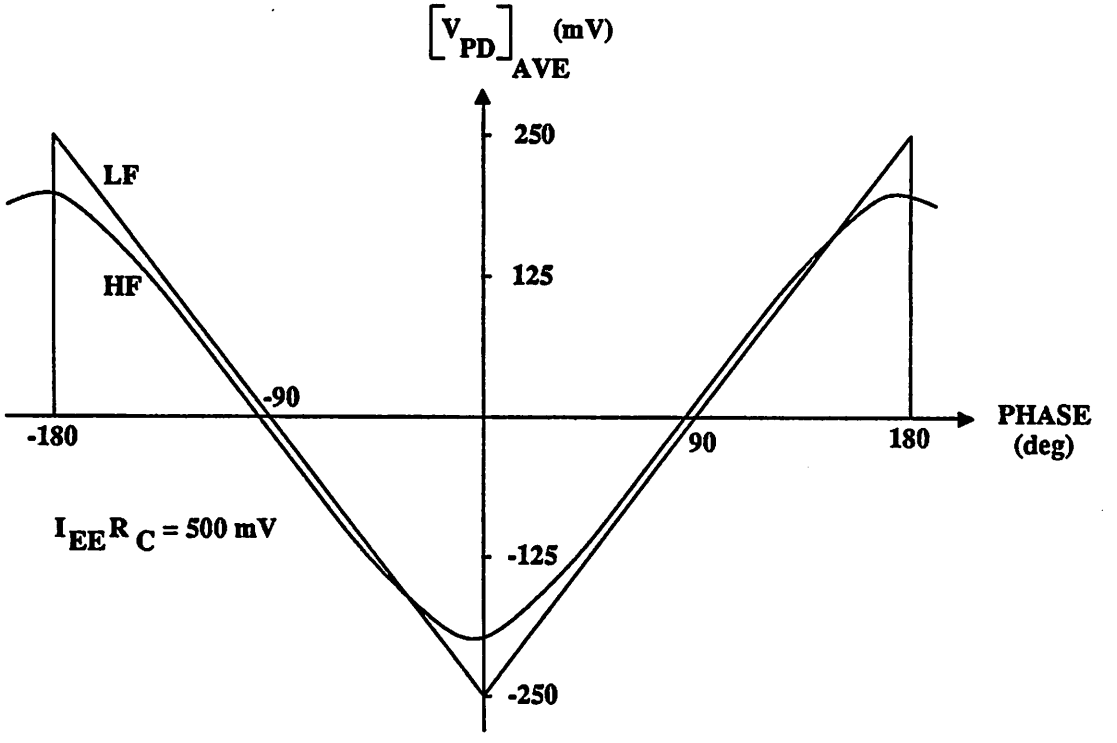


Figure 4.4 - Tristate phase detector characteristics at 500 MHz.

respectively, as shown in Figure 4.5. Therefore, the phase detector bandwith is very large and the VCO is the limiting factor in the operating frequency range. It can easily be shown that this conclusion is also valid for a double-balanced modulator.

In light of the comparisons made in this section, a single-balanced modulator is chosen over a double-balanced modulator as an analog phase detector in implementing the PLL. The complete circuit including the input amplifier is shown in Figure 4.6. Using I_{EE} = 2 mA and R_C = 250 ohms, the maximum phase detector gain is designed to be 160 mV/radian. The emitter follower transistors have an area 5 times larger than that of the switching devices to minimize the offset. The width of the resistors is 20 microns for good matching. For 1 mV V_{BE} mismatch and 1 percent resistor mismatch, V_{OS} is 2.25 mV from equation (4.2.3). When there are no input transitions, V_{OS} reduces to 1 mV. Then, the static phase error for equally likely data is 1.17 degrees from equation (4.2.6). The total offset that has to be overcome during capture is 4.125 mV from equation (4.2.11) assuming D_{IN} = 0.50 and D_{VCO} = 0.49.

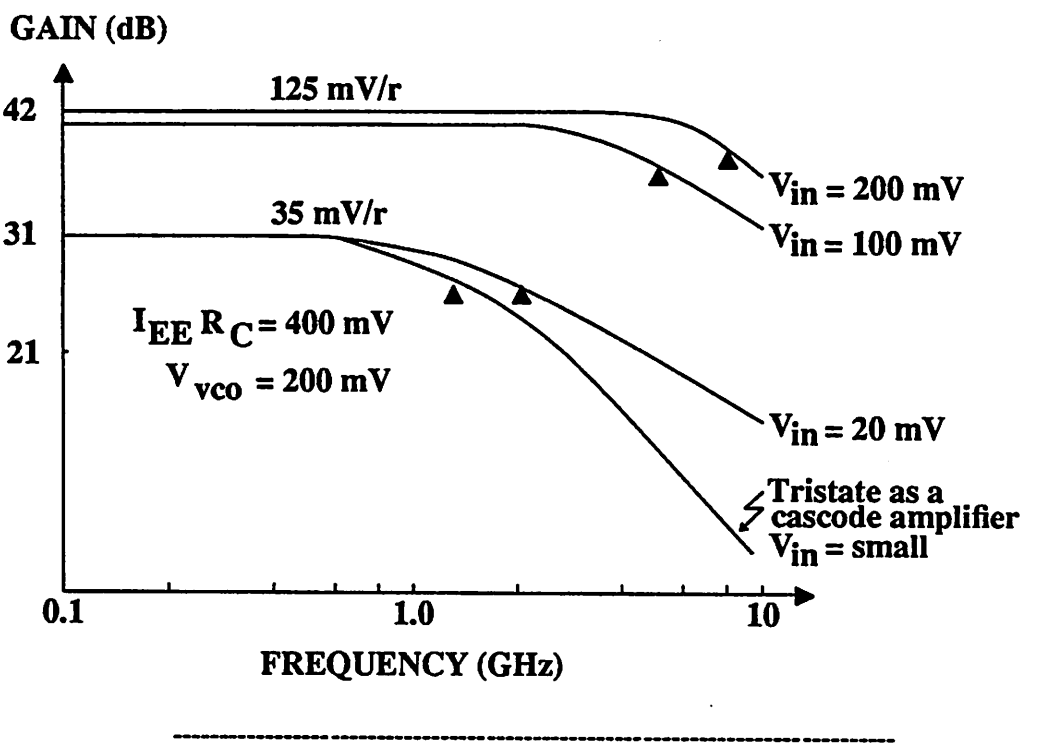


Figure 4.5 - Tristate phase detector gain vs. frequency.

The design of the input amplifier is very similar to the clock amplifier. The only difference is that the 250 ohm load resistors has been replaced by 400 ohm resistors to increase the gain. It has a small-signal gain of 12 and a bandwith of 650 MHz. When considered with large inputs, it behaves like an ECL-NOR gate with complementary outputs to provide sufficient balanced drive to the phase detector. The maximum logic swing is 800 mV. The reference voltage is derived from the bandgap reference and it is equal to V_{CC} - V_{BG}. The input amplifier helps to improve the phase detector gain for low level signals.

4.3. Digital Phase Detectors

There are two types of digital phase detectors which are commonly used; sawtooth [58], [62] and adaptive, [58]-[59], [61]. There exist several versions of each type, some of them being commercially available. Each version might have a different linear range. However, the underlying principle of operation does not differ in the sense that they are always sequential type circuits having memory. It is

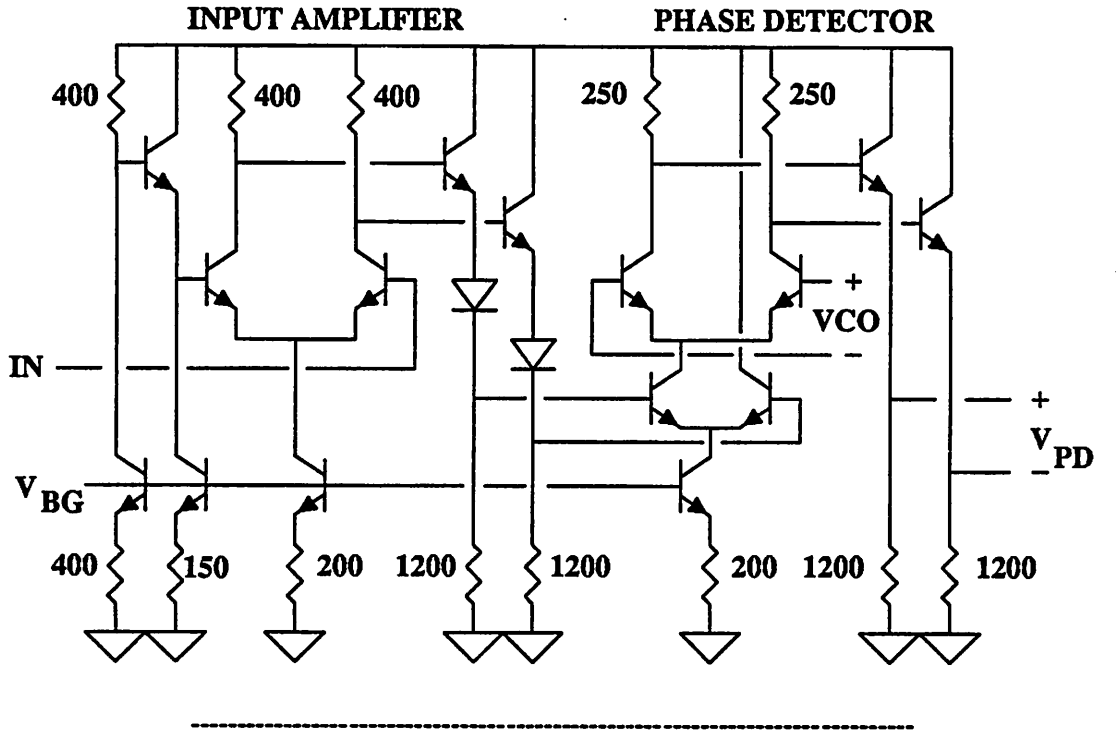


Figure 4.6 - Input amplifier and tristate phase detector.

intuitively simple to use this memory approach to understand the frequency detection property since any change in the phase difference has to be remembered for frequency detection. Therefore, they are capable of frequency detection in addition to phase detection regardless of their linear range. It may be worth to mention that the opposite is not necessarily true, that is, a sequential type frequency detector may not have the phase detection property. An example of this is given in Appendix B.

The sawtooth characteristics can be obtained with an R-S flip-flop or a D-type master-slave flip-flop. In the simplest case of R-S flip-flops, the output is set by the data transitions and reset by the VCO transitions. However, unless the data pulses are ideal impulses this phase detector has a large acquisition offset, [60]. Furthermore, when data transitions are missing, the output remains reset forcing the VCO away from the center frequency. To solve this problem, a set-toggle flip-flop can be used, [62]. In this case, the VCO transitions toggle the output when the data transitions are missing hence reducing the offset ideally to zero. A better alternative is to use an edge-triggered flip-flop eliminating the need for very narrow data pulses, [60]. The frequency detection property and the limitations of this phase detector

has been analyzed by R. C. Halgren et al. It is shown in [60] that the frequency discriminator gain of this circuit for random data is 1/9 of the gain for square-wave data. It is also shown that the frequency detector gain can be zero for some well-known coding schemes. Furthermore, to reduce the large acquisition offset coming from the set-up times and propagation delays, additional circuitry and variable R-C sections are required. Even with propagation delays around 1 nS, the frequency of operation is limited to frequencies below 100 MHz.

The second important class of digital phase detectors is the adaptive phase detectors. They also are implemented in different versions, [58]-[59], [61]. The digital phase-frequency detector (DPFD) is the most well-known adaptive phase detector. It is analyzed in detail in Appendix A. Two circuit implementations are shown in Figures A.1 and A.2. Although a DPFD cannot tolerate missing transitions, a PLL with a DPFD is sometimes useful to reduce the jitter following a passive narrowband filter or when a separate pilot tone is transmitted for clock recovery. The average differential output available from the DPFD is a measure of the phase difference between the positive-going edges of the two inputs. Therefore, input duty cycles do not have any effect on the output.

At high frequencies, the self-terminating reset pulse at the control gate output limits the frequency performance of the circuit. A detailed analysis has been made to understand the frequency detection property of the circuit and the effect of the reset pulse width. It is shown in Appendix A that the average differential output normalized by the logic swing is given by:

$$\overline{V_{AVE}} = \frac{\beta + 0.5}{\beta + 1.0} - \alpha \qquad (4.3.1)$$

where β is the normalized frequency difference with respect to the lower input frequency and α is the reset pulse width normalized by the inverse of that frequency. In order to have the correct polarity to help the frequency acquisition, V_{AVE} must be greater than zero as the frequency difference goes to zero. For example, a 4 nS reset pulse width limits the useful frequency range to less than 125 MHz.

SPICE simulations have extensively been used to verify equation (4.3.1). A junction-isolated 4 GHz process gives a maximum frequency of operation of 115 MHz for the D-type master-slave version

and 175 MHz for the R-S latch version. An oxide-isolated 12 GHz process yields a maximum frequency of 600 MHz for the D-type master-slave version and 770 MHz for the R-S latch version. The power dissipation is around 475 mW with a single 5 V supply. For the 4-GHz process, the reset pulse width is around 4 to 4.5 nS with the D-type master-slave flip-flops. This gives an estimated maximum frequency of 110 to 125 MHz agreeing with the simulation results.

Some high-frequency measurements have also been performed to verify the results of Appendix A. A commercially available R-S latch version of the circuit (MC12040) has been used in the measurements. The circuit is from the MECL family and fabricated with a 1 nS gate-delay bipolar process. It dissipates 520 mW. The reset pulse width measured from the phase characteristics was 5 nS. This puts the upper limit on the frequency of operation as 100 MHz which is close to the typical operating frequency given in the data sheet (70 MHz).

Due to the limitations of sawtooth and adaptive phase detectors as frequency discriminators, a digital rotational-frequency detector (DRFD) which can work with random data has been designed. The design philosophy is based on the rotational-frequency detector concept, [51]. The operation of the circuit is explained in detail in Appendix B. The DRFD employs six D-type flip-flops and two combinatorial gates as shown in Figure B.2. Since the circuit does not require any additional filtering (unlike the analog frequency detectors), it can easily be implemented with monolithic integration. The high-frequency performance of the circuit is limited by the set-up times and propagation delays of the flip-flops and by the logic swing. The logic swing cannot be made too small since the DRFD output is proportional to it. SPICE simulations show that the DRFD provides a correction voltage with the right polarity up to 2.5 GHz for frequency offsets greater than 25 percent with a 12 GHz process. This frequency limit reduces to 500 MHz for frequency differences larger than 5 percent and to 100 MHz for frequency offsets greater than 1 percent. The logic swing is 400 mV and the power dissipation is 400 mW.

As a conclusion, analog phase detectors are superior to digital phase detectors since they have better frequency performance with less power dissipation and smaller chip area. However, digital phase detectors provide larger pull-in range and shorter pull-in times.

4.4. Non-Phase Sensitive Effects

An ideal phase detector output is sensitive only to the input phase difference. In practice, however, several other sources my cause the phase detector output to change. Some of these sources will be reviewed in this section.

4.4.1. Temperature and Supply Dependence

The phase detector gain and the DC-offset are both functions of temperature and supply. However, the static phase error can be made independent of supply and temperature using a bandgap reference. Using equation (4.2.6), one can show that if the bias current, I_{EE}, is derived from a PTAT voltage, the effects of temperature and supply variations on Θ_e are eliminated to a first order approximation. As mentioned in Section 4.2, the stable operating point, Φ_o, is also temperature and supply dependent. Deriving I_{EE} from a bandgap reference will reduce that dependence to less than ± 2 degrees over 0 to 70 °C at 500 MHz.

4.4.2. Ripple and VCO Feedthrough

For a periodic input, the ripple at the output is at twice the input frequency for a double-balanced modulator and at the input frequency for a single-balanced modulator. The ripple is reduced by a factor of 10 or more by the loop filter. A ripple filter will further reduce the ripple if injection into the VCO is a problem. The average output resulting from the feedthrough of an asymmetric VCO waveform is quite negligible (a few microvolts) when a tristate phase detector is used.

4.4.3. Input Level Dependence

Examination of Figure 4.5 reveals that the input signal amplitude to a tristate phase detector must be more than 100 mV, or 4 V_T, for full switching of the lower differential pair. In this case, the phase detector characteristics can be assumed to be triangular and equation (4.2.1) can be used for the phase detector gain. An input amplifier with a gain of 10 or more reduces this requirement down to 10 mV or

less. The tristate phase detector gain for small signals can be found by following a similar analysis as in [34, ch. 10]. The final result is:

$$K_{PD} = \frac{R_C I_{EE}}{\pi} \frac{V_{in}}{2 V_T} \tag{4.4.1}$$

where V_{in} is the input signal amplitude to the lower differential pair of the tristate phase detector. This equation is valid for V_{in} less than 2 V_T. This region corresponds to an almost sinusoidal characteristics. For V_{in} between 2 V_T and 4 V_T, the phase detector gain saturates toward $\frac{R_C I_{EE}}{\pi}$, and the phase detector characteristics start changing from sinusoidal to triangular.

Similar results hold for the double balanced modulator after replacing equation (4.2.1) by (4.2.2). An advantage of the tristate phase detector over the double-balanced modulator for low input levels is that the mismatches in the lower differential pair appear as a common-mode signal without affecting the output offset of the phase detector.

4.4.4. Data Pattern Dependence and Noise

As was discussed in Section 4.2, the phase detector gain should be modified accordingly to account for the random nature of data when it is no longer used with maximum transition density inputs. These variations in the number of transitions result in both amplitude and phase modulation of the input to the phase detector. Actually, this dependence on the input data pattern is a major source of phase jitter at the VCO output. The nonlinear processing stage preceding the PLL also plays an important role in determining the amount of input jitter. Another advantage of the tristate phase detector is that it provides half-wave rectification on RZ signals with no DC-component thus creating a strong component at the clock frequency, [6].

As a result of the random nature of data, the ripple waveform at the output of the phase detector also resembles to a random signal as was shown in Figure 4.3. Although it is the cyclo-stationary property of such signals that provides the timing information, it will be assumed that the signal is wide-sense stationary to simplify the following analysis. Under this assumption and following a similar approach

used by W. R. Bennett in his classical paper, [43], the continuous power spectral density function, $S_r(\omega)$, of the ripple waveform of a tristate phase detector in perfect lock (no phase error) can be written as:

$$S_r(\omega) = \frac{1}{T_c}\, p\,(1-p)\,|F(\omega)|^2 \tag{4.4.2}$$

where T_c is the clock period, p is the probability of a transition, and $F(\omega)$ is the Fourier Transform of a single phase detector output pulse. $F(\omega)$ can be shown to be:

$$F(\omega) = 2\,j\,R_C\,I_{EE}\,\frac{T_c}{4}\,sinc\left[\frac{\omega\,T_c}{8}\right]\sin\left[\frac{\omega\,T_c}{8}\right] \tag{4.4.3}$$

Substituting (4.4.3) into (4.4.2):

$$S_r(\omega) = p\,(1-p)\,(R_C\,I_{EE})^2\,\frac{T_c}{4}\,sinc^2\left[\frac{\omega\,T_c}{8}\right]\sin^2\left[\frac{\omega\,T_c}{8}\right] \tag{4.4.4}$$

Since the bandwith of the PLL circuit is much smaller than the bit rate of the input data, equation (4.4.4) can be approximated as:

$$S_r(\omega) = p\,(1-p)\,(R_C\,I_{EE})^2\,\frac{T_c^3}{256}\,\omega^2 \tag{4.4.5}$$

This continuous spectrum behaves like thermal noise introducing jitter into the VCO. In order to find the jitter caused by the random phase detector output, S_r can be referred to the PLL input as:

$$S_i(\omega) = \frac{1}{{K_{PD}}^2}\,p\,(1-p)\,(R_C\,I_{EE})^2\,\frac{T_c^3}{256}\,\omega^2 \tag{4.4.6}$$

Then, the VCO jitter can be estimated by integrating equation (4.4.6) over the noise bandwith, B_L, of the PLL:

$$\overline{\Theta_o^2} = \frac{1}{{K_{PD}}^2}\,p\,(1-p)\,(R_C\,I_{EE})^2\,\frac{T_c^3}{256}\,\frac{{B_L}^3}{3} \tag{4.4.7}$$

From equation (2.3.5):

$$T_c\,B_L = \frac{\pi}{4}\,\frac{1}{Q_{PLL}} \tag{4.4.8}$$

Therefore, equation (4.4.7) becomes:

$$\overline{\Theta_o^2} = \frac{1}{K_{PD}{}^2}\, p\,(1-p)\,(R_C\, I_{EE})^2\, \frac{\pi^3}{49152}\, \frac{1}{Q_{PLL}{}^3} \tag{4.4.9}$$

Assuming that p = 0.5 and substituting the gain for a tristate phase detector:

$$\overline{\Theta_o^2} = \frac{\pi^5}{196608}\, \frac{1}{Q_{PLL}{}^3} \tag{4.4.10}$$

Therefore, if Q_{PLL} is 100 then the rms jitter is 0.0023 degrees or 6 ppm per cycle.

It may be interesting to compare the jitter caused by the continuous spectrum of the random ripple to that caused by the equivalent output noise spectrum of the phase detector circuit. The thermal noise in the resistors and the shot noise in the devices contribute to the output noise spectrum. The equivalent output noise resistance, R_n, of the tristate phase detector can be estimated to be 30 KΩ by modeling the circuit as a cascode amplifier and then applying the techniques of [34, ch. 11]. Hence, the VCO jitter can be approximated as:

$$\overline{\Theta_o^2} = \frac{1}{K_{PD}{}^2}\, 4kT\, R_n\, B_L \tag{4.4.11}$$

where 4kT = 1.66 x 10^{-20} V-C, $K_{PD} = \frac{0.5}{\pi}$ V/radian, R_n = 30 KΩ, and $B_L = \frac{\pi\ f_c}{4\ Q_{PLL}}$.

Assuming Q_{PLL} = 100, one has:

$$\overline{\Theta_o^2} = \pi^3\, 5x\, 10^{-18}\, f_c \tag{4.4.12}$$

At 100 MHz, the rms jitter is 0.0071 degrees or 20 ppm per cycle.

The conclusion is that the jitter caused by the tristate phase detector ripple waveform can be neglected when compared to the other components of PLL output jitter.

CHAPTER 5

MEASURED RESULTS AND DISCUSSION

5.1. Introduction

The block diagram of the test circuit is shown in Figure 5.1.

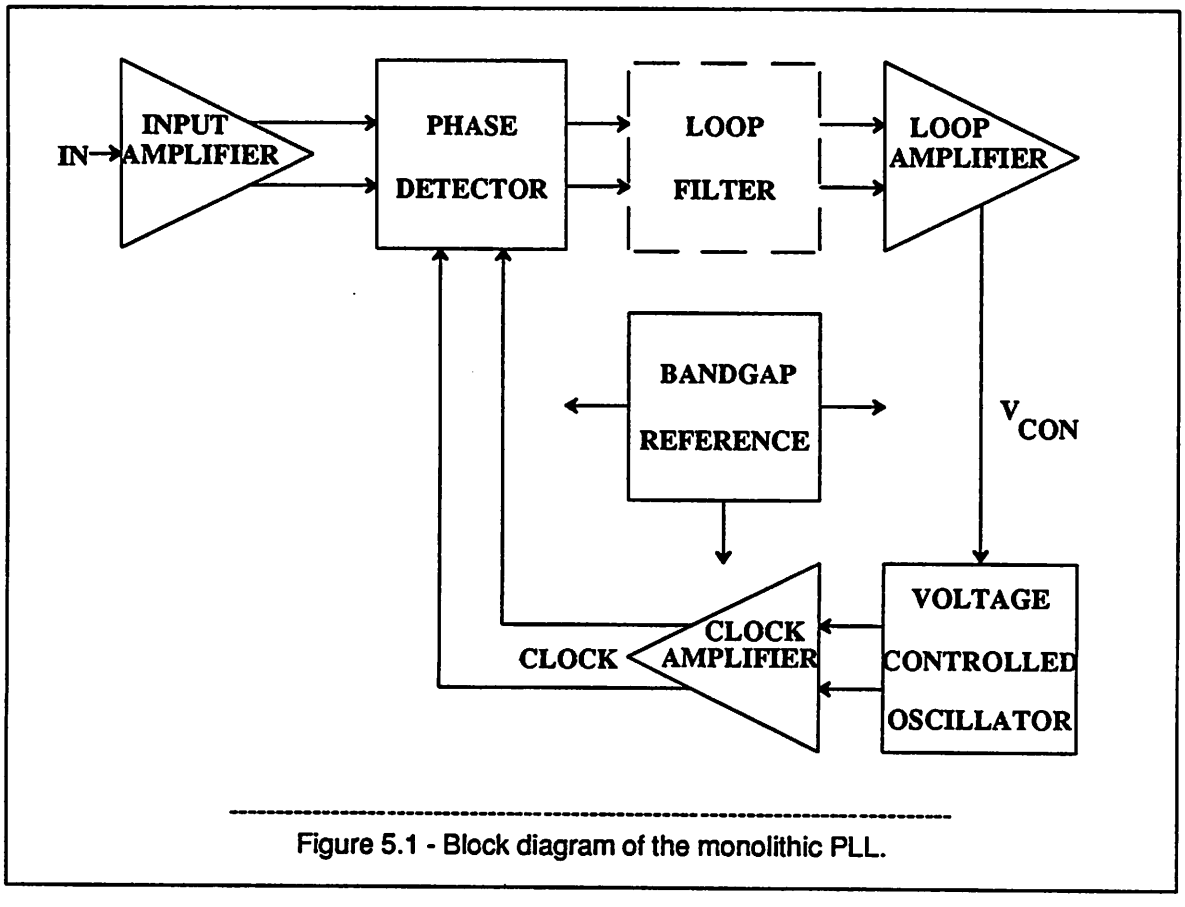


Figure 5.1 - Block diagram of the monolithic PLL.

Main building blocks of the PLL circuit are a single-balanced modulator employed as an analog phase detector, a varactor-tuned VCO with a two-stage loop amplifier and a bandgap reference. The test circuit was fabricated in a 2-micron oxide-isolated bipolar technology at Signetics Inc., Sunnyvale, CA. The cut-off frequency of the NPN transistors is between 9 to 12 GHz and collector to emitter breakdown voltage is 6 volts. The all-ion-implanted process uses a 1-micron epi layer, local oxidation for isolation, two

levels of metal, and washed-emitter technology. The minimum emitter size is 2 microns.

The complete schematic of the PLL circuit is shown in Figure 5.2.

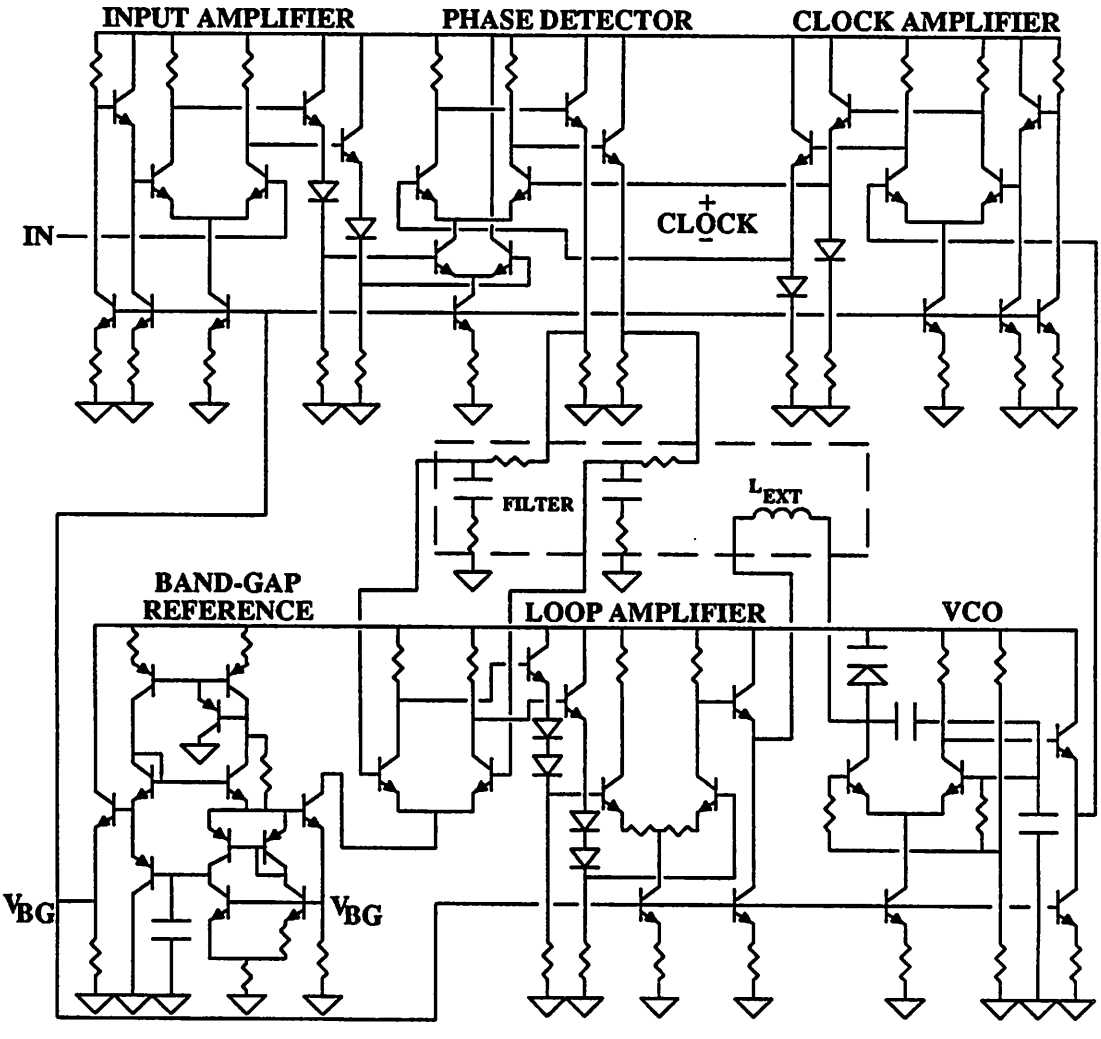


Figure 5.2 - Complete PLL schematic.

The loop filter, the inductor of the VCO tank circuit and the bypass capacitors (not shown) are external to the circuit. The test circuit has 32 pads to measure the performance of each block. The bandgap reference can be disconnected if an external bias is preferred for measurement purposes. Each major block has its own supply and ground pads for easy measurement. All the bypass capacitors at critical points are ceramic chip capacitors within a range of 1 to 100 nF. Although the complete circuit can be housed in a

14-pin small-outline (SO) package with low parasitic values, the test chip was housed in a 40-pin dual-in-line (DIL) package due to the large number of test pads. This degraded the high-frequency performance of the circuit considerably as it will be discussed in the next sections. The integrated circuit was mounted on an one-sided printed circuit board with a 40-pin socket for easy testing of different samples. Two sets of five samples were provided for measurements, each set having a different bonding scheme. A separate set of three samples packaged in TO-39 metal cans were used for the varactor diode measurements.

5.2. Varactor Measurements

The varactor capacitance as a function of the reverse bias was measured using the HP 4271A, 1 MHz Digital LCR Meter. The average capacitance of the three SP-EPI samples is plotted in Figure 5.3.

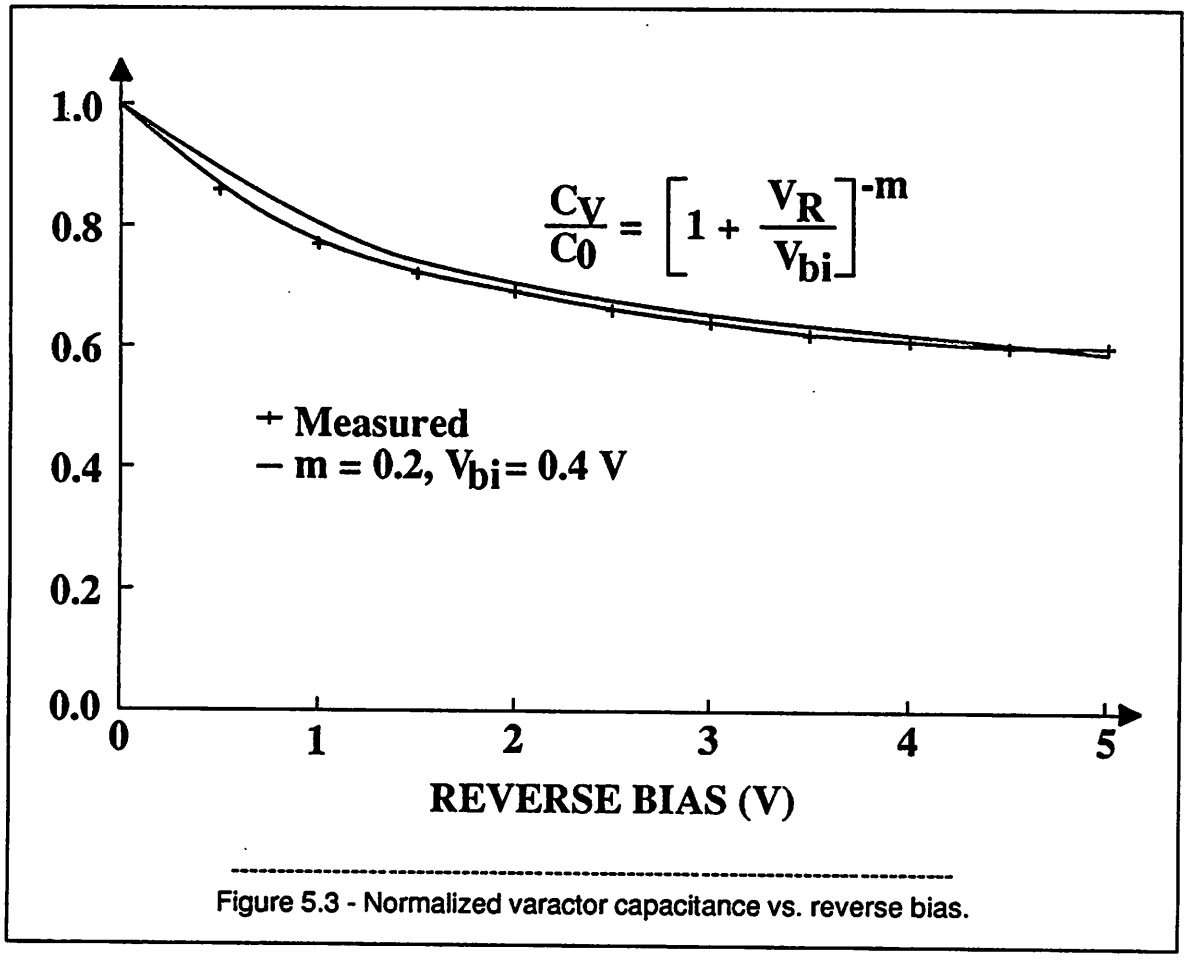


Figure 5.3 - Normalized varactor capacitance vs. reverse bias.

The absolute tolerance of the measured samples is better than 3 percent. As it can be seen from this figure, m = 0.2 and V_{bi} = 0.4 volts provide a good fit for the measured results. The reason that the grading coefficient is so small is due to the fact that the heavily doped buried layer extends into the thin epi layer making the variation in the depletion-layer width smaller than expected, [78]. Similar measurements with DP-EPI junctions show that the advantage of using SP-EPI junctions is marginal. For a reverse bias between 1 and 3 volts, the measured variation in capacitance is +12 and -6.5 percent with a zero-bias value of 8.2 pF. Larger zero-bias values were used in the PLL test circuit to reduce the effect of any fixed capacitance on the tuning range.

The temperature measurements were done using the Delta Design Temperature Test Chamber Model 6545-L. Figure 5.4 shows the varactor capacitance as a function of temperature.

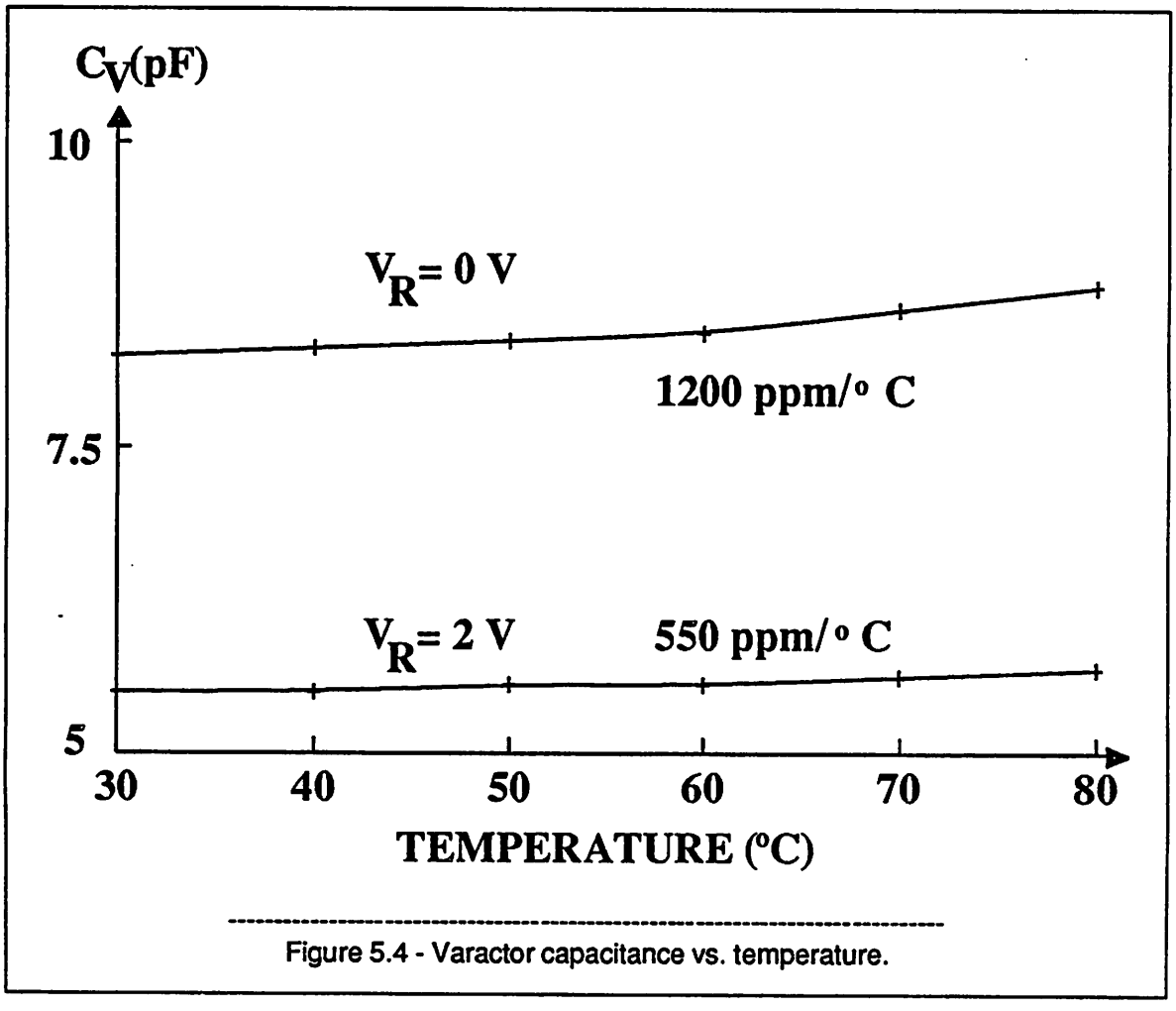


Figure 5.4 - Varactor capacitance vs. temperature.

The measured TC of the varactor is 1200 and 550 ppm/°C for a reverse bias of 0 and 2 volts, respectively. To compare these results with the assumptions made in Chapter 3, equation (3.5.13) for the capacitance will be repeated here:

$$C_V = \left[\frac{K\ \varepsilon_S{}^{\alpha}}{V_{bi} + V_R} \right]^m \tag{5.2.1}$$

If one assumes that m is constant with temperature, then the TC of the varactor can be written as:

$$\frac{\partial C_V}{C_V\ \partial T} = m \left[\frac{\partial Q_S}{Q_S\ \partial T} - \frac{\partial (V_{bi} + V_R)}{(V_{bi} + V_R)\ \partial T} \right] \tag{5.2.2}$$

where $Q_S = K\ \varepsilon_S{}^{\alpha}$. Substituting the measured values into (5.2.2) and solving for the temperature coefficients, the following results are obtained:

$$\frac{\partial V_{bi}}{\partial T} = -1.6\ \text{mV/°C}$$

$$\frac{\partial Q_S}{Q_S\ \partial T} = 2000\ \text{ppm/°C}$$

These values are quite different from the estimated values of -2.9 mV/°C and 400 ppm/°C obtained with SPICE in Chapter 3. To double check the results obtained from Figure 5.4, the variation in reverse bias that keeps the capacitance constant with respect to temperature was also measured. The results are shown in Figure 5.5 for a reverse bias of 2 volts at room temperature. The measurements show that the reverse bias should have a TC of + 5 mV/°C for the varactor capacitance to stay constant with temperature. Substituting this value into equation (5.2.2) and using the measured value of the varactor TC at zero bias, one can obtain:

$$\frac{\partial V_{bi}}{\partial T} = -1.9\ \text{mV/°C}$$

$$\frac{\partial Q_S}{Q_S\ \partial T} = 1300\ \text{ppm/°C}$$

These results are still not consistent with SPICE. It might be plausible to conclude that the parameters m, K, and α in equation (5.2.1) are also functions of bias and temperature, especially for complicated struc-

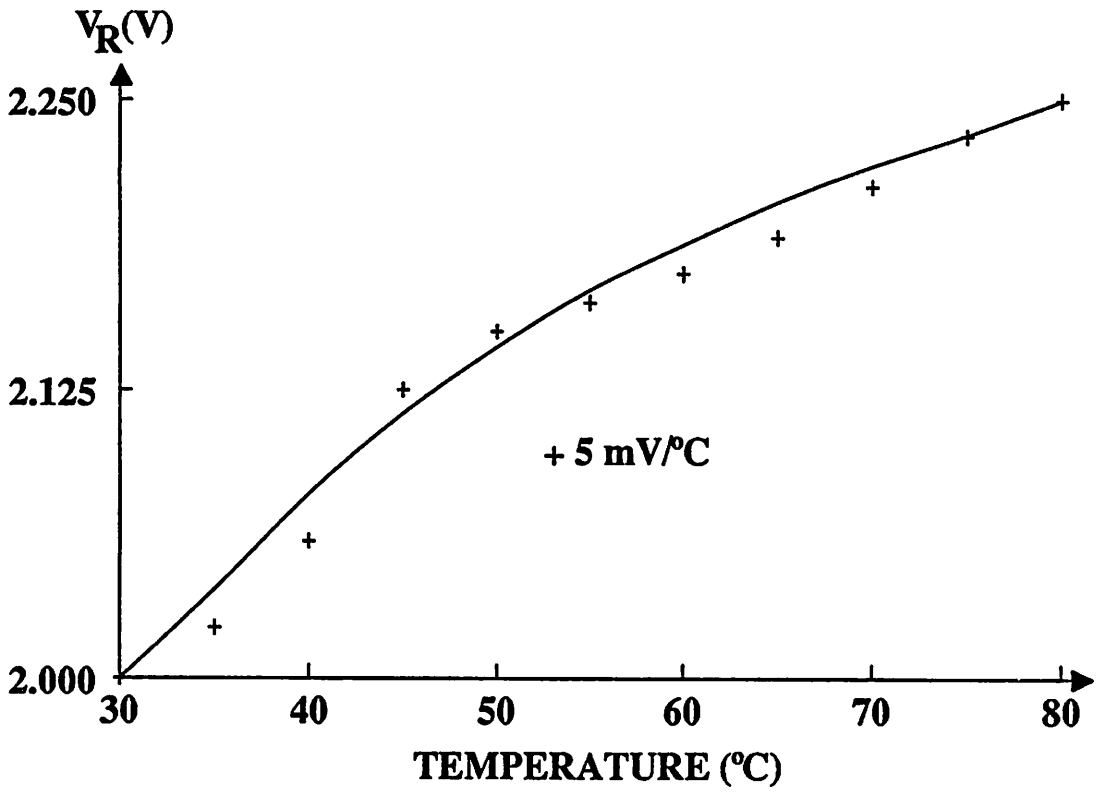


Figure 5.5 - Variation in reverse bias to keep varactor capacitance constant.

tures which cannot be modeled by an abrupt or a linearly-graded junction. Therefore, a design iteration may be necessary when an accurate varactor model is not available.

In principle, the high-frequency quality factor of passive components can be measured using the HP 8753A Network Analyzer and the HP 85046A S-Parameter Test Set with the HP 11602B Transistor Fixture. When measuring the quality factor of the varactor diodes, two major sources of error must be considered:

1. Calibration errors,

2. Package inductance.

The calibration errors increase with frequency due to the imperfect 50-ohm load termination above a few hundred MHz. The bonding wire and package lead inductances appear in series with the varactor diode and degrade the quality factor by increasing the series losses at high frequencies. All these make

an accurate measurement difficult especially for high-Q components. As a result, it was found that the measured varactor losses were very sensitive to the calibration errors.

The measurements were done on 8.2 pF and 13.2 pF varactors housed in TO-39 metal can and 40-pin DIL packages, respectively. From the self-resonance frequency of each device, the total inductance in series with the 8.2 pF varactor was measured as 6 nH. Similarly, the total series inductance was measured to be 20 nH for the 13.2 pF varactors. As an example, the quality factor of the package lead inductance for a TO-39 package is plotted in Figure 5.6.

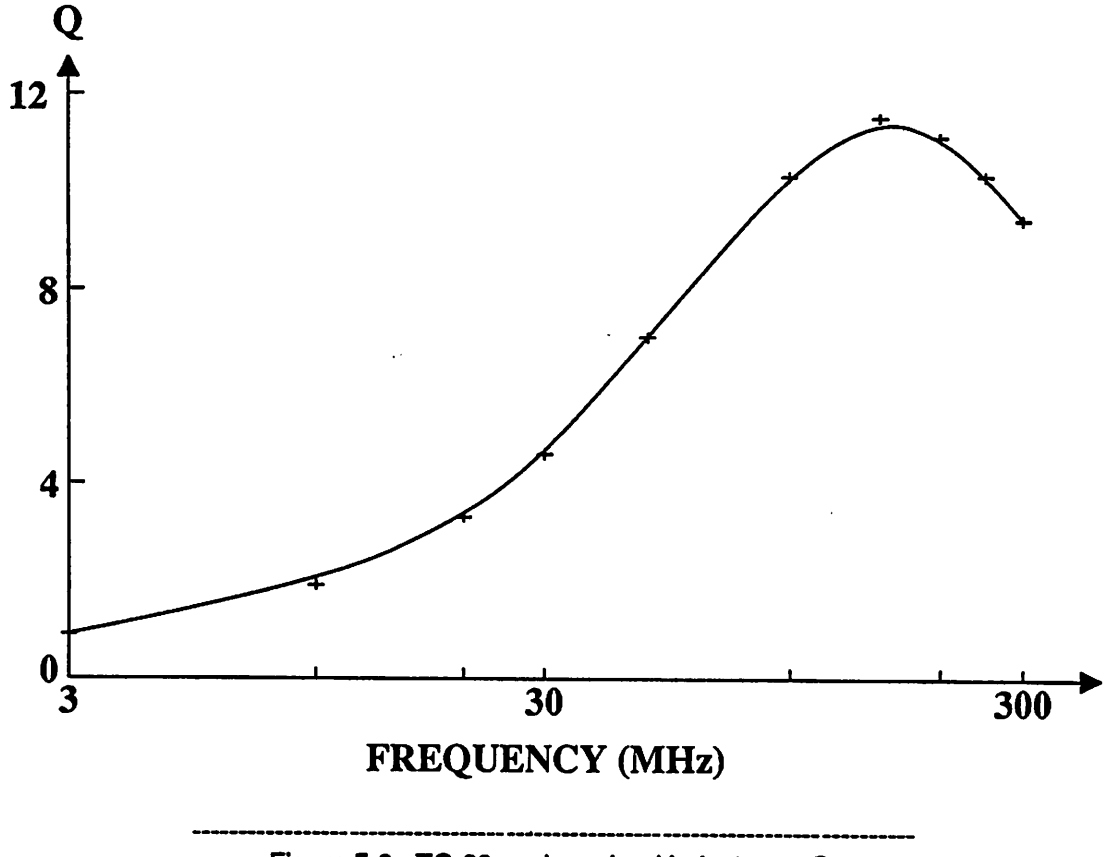


Figure 5.6 - TO-39 package lead inductance Q.

At 250 MHz, the series resistance is 1 ohm for an inductance of 6 nH. Therefore, the series resistance of the 20 nH DIL-package inductance can be estimated as 3.3 ohms assuming that the bonding wire and the package lead inductance have the same quality factor. (For comparison, a 30 nH air-core inductor with 2 turns has a series resistance of 3.4 ohms at 250 MHz). For a measured series-resonance loss of 4.3 ohms,

the 13.2 pF varactor has an estimated series resistance of 1 ohm. This corresponds to a Q_V of 48 at 250 MHz. The quality factor increases with reverse bias.

As a conclusion, the varactors have reasonably high quality factors but the 40-pin DIL package causes significant Q loss at high frequencies.

5.3. Open Loop PLL Measurements

Open loop measurements include the measurement of the gain constant of each PLL block, the offset voltage measurements, and the frequency measurements for different supply and temperature conditions.

The low-frequency phase detector gain was measured to be 140 mV/radian. This is close to the design value of 160 mV/radian. The measured output offset voltage was 1 mV when both outputs were high. The major contributor to this offset is believed to be the emitter resistance mismatch of the output devices used as emitter followers. A mismatch of 0.3 ohms at 3.3 mA bias current could produce this offset. The input amplifier preceding the phase detector has a measured gain of 13 at low frequencies.

The loop amplifier gain was measured as 50 with an input offset voltage of 0.25 mV. The first stage gain was measured to be 16.7. This value is large enough to reduce the input referred offset coming from the level shifting diodes to 0.2 mV. The nominal value of the output is 2.9 V with a dynamic range of 2.3 volts.

The band-gap reference measurements were done by connecting the loop amplifier current sources as load. The nominal value of the band-gap output was 1.27 V. This is 20 mV larger than 1.25 V obtained from the SPICE simulations. The measured TC of the bandgap reference is +200 ppm/°C from 20 to 100 °C. This value is also larger than expected. There may be several sources of error which explain these deviations. First of all, due to an error in the resistor design equations, the SP-resistor ratio in the bandgap core is about 10 percent larger than desired. Another contribution might come from the absolute tolerance (± 8 mV) and the matching of the base-emitter voltages of the NPN and PNP transistors. TC of the SP-resistor ratio and that of the current in the core transistors may also contribute to a

large TC at the bandgap output. However, since the control voltage mostly depends on the PTAT voltage derived from the bandgap reference, this TC is not very critical.

Figure 5.7 shows the base-emitter voltage of a minimum size NPN transistor and the loop amplifier control voltage as a function of temperature.

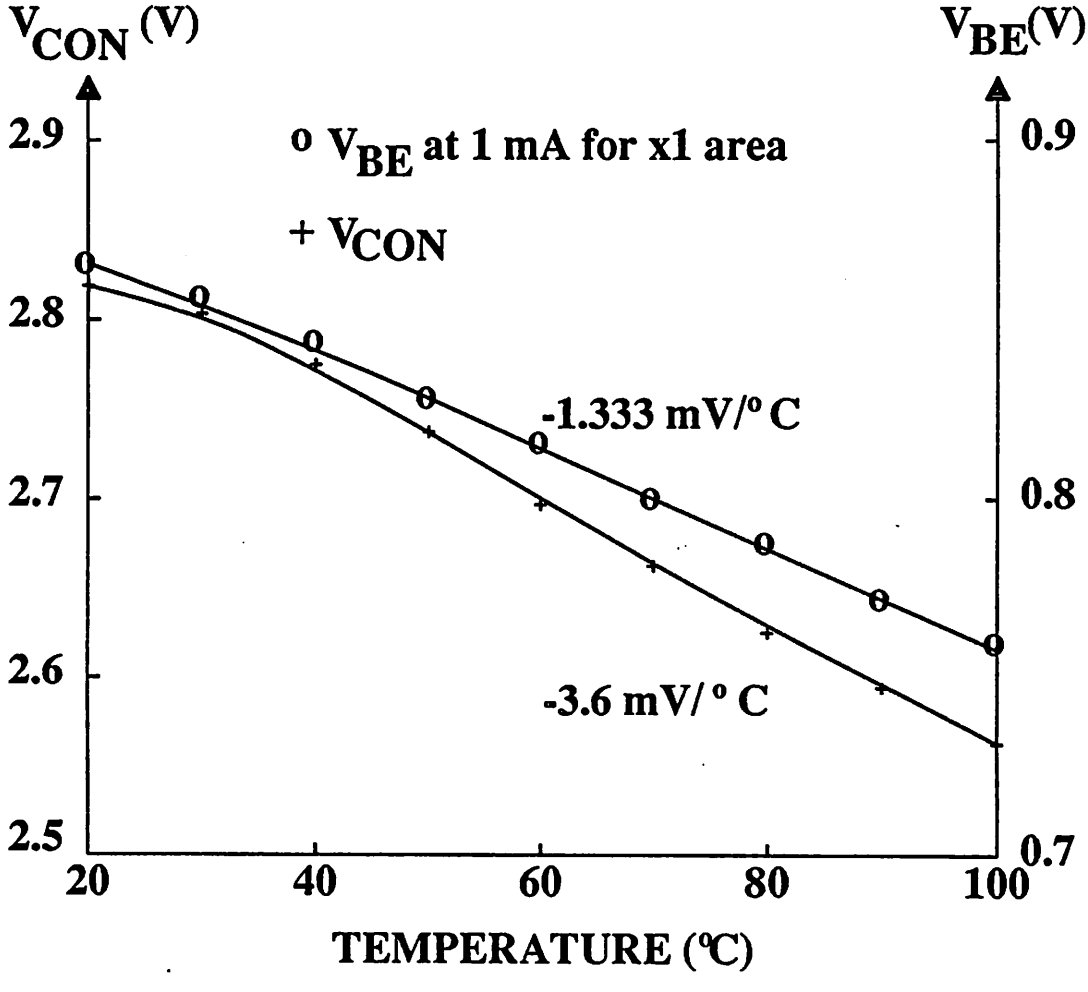


Figure 5.7 - Control voltage and base-emitter voltage vs. temperature.

The NPN transistor has a measured saturation current of $6x10^{-18}$ A and a base-emitter voltage TC of -1.333 mV/°C at 1.07 mA. However, the NPN transistors in the loop amplifier have an area ten times larger than that of a minimum size transistor. Also, the output emitter follower and the second stage current source run at a current level five times higher than 1.07 mA. Since $\frac{\partial V_{BE}}{\partial T}$ is proportional to

$\frac{V_{BE}}{T}$, the measured value above should be modified as:

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T \ln 0.5}{T} - 1.333 = -1.4\ mV/°C$$

This is close to -1.5 mV/°C obtained from the SPICE simulations. The control voltage has a measured TC of -3.6 mV/°C. In other words, the reverse bias across the varactor diode will have a TC of +3.6 mV/°C. This is 28 percent less than the desired value obtained from Figure 5.5. Therefore, the varactor still has a positive TC which is not compensated.

Figure 5.8 shows the temperature stability of the VCO center frequency with the compensation circuitry.

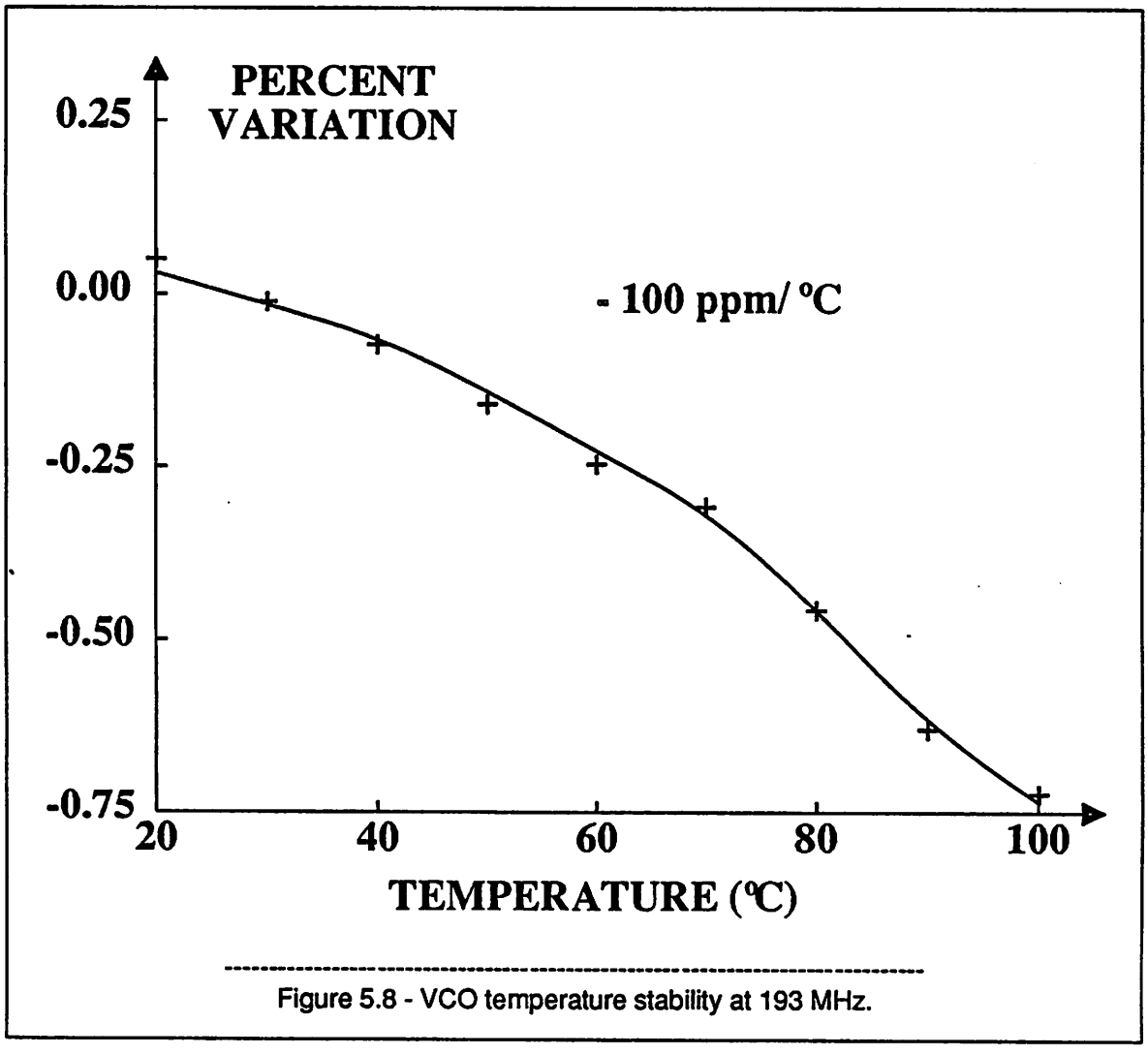


Figure 5.8 - VCO temperature stability at 193 MHz.

The Tektronix Oscilloscope 7904 (500 MHz) with the 7D15 Counter (225 MHz) was used for the frequency measurements. The TC of the VCO was measured to be around -100 ppm/°C at 193 MHz and over 20 to 100 °C. The reverse bias across the varactor was approximately 2 V. As the center frequency was increased to 250 MHz and beyond, the oscillations stopped at temperatures higher than 70 °C due to the increased losses in the VCO tank circuit. The actual TC without any fixed parasitic capacitance in the tank circuit would be around -150 ppm/°C. This is mainly coming from the uncompensated TC of the varactor and the TC of the inductances in the circuit.

Figure 5.9 shows the voltage coefficient (VC) of the VCO center frequency at 235 MHz.

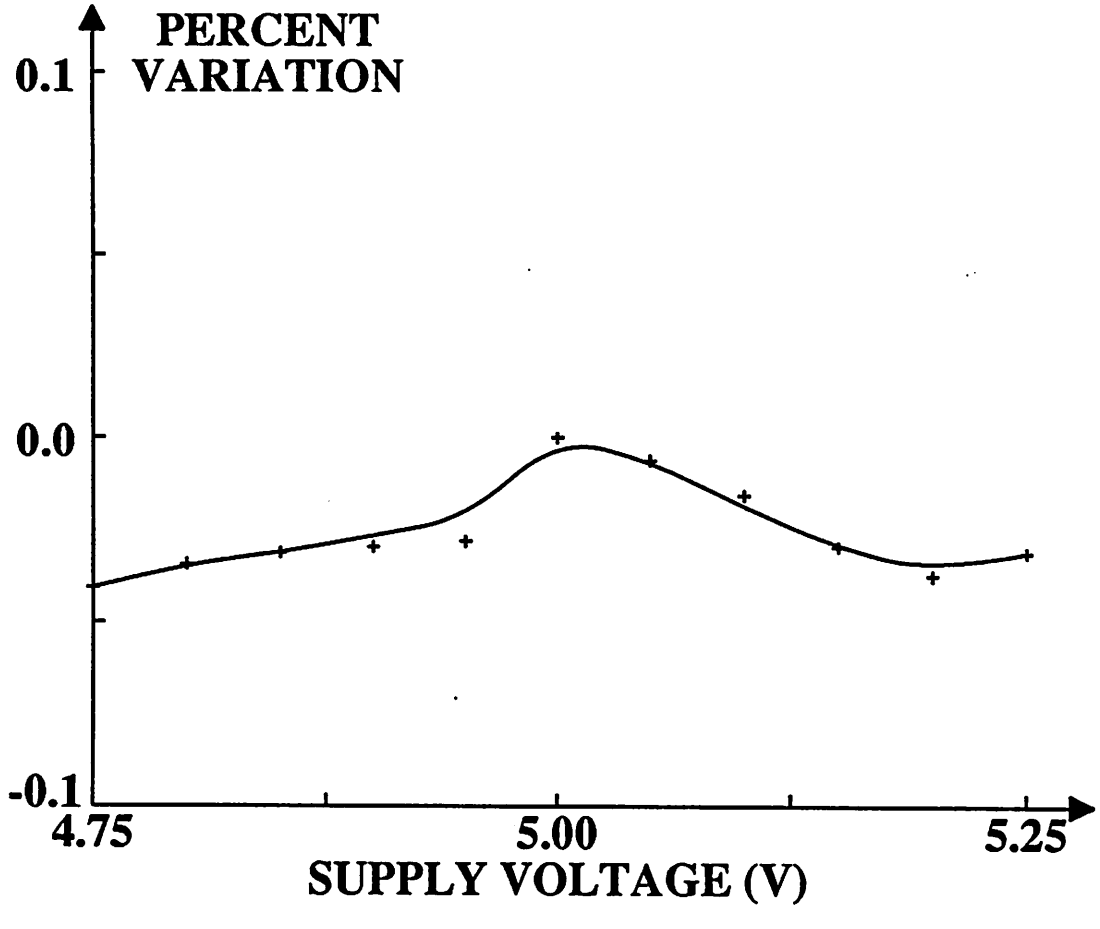


Figure 5.9 - VCO center frequency vs. supply at 235 MHz.

The supply variation was ± 5 percent at 5 V. The measured values for all samples were better than 0.3

percent/V up to 250 MHz. It was observed that the oscillations stopped for supply voltages below 3.9 V. This is because some of the transistors in the bandgap reference saturate for lower supply voltages.

The tuning range of the VCO is a function of the fixed capacitance introduced by the package and the printed circuit board including the socket. Figure 5.10 shows the tuning range at 188 MHz for a total fixed capacitance of 6 pF.

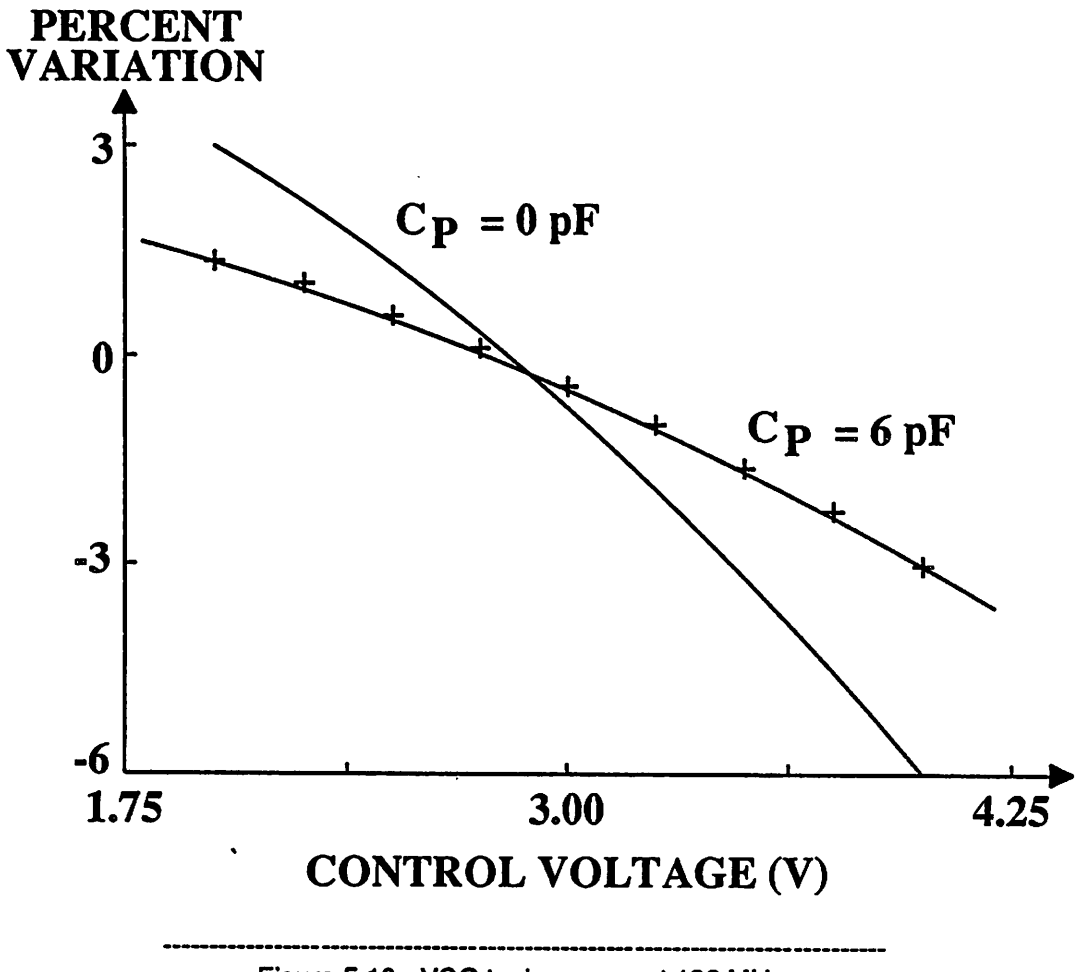
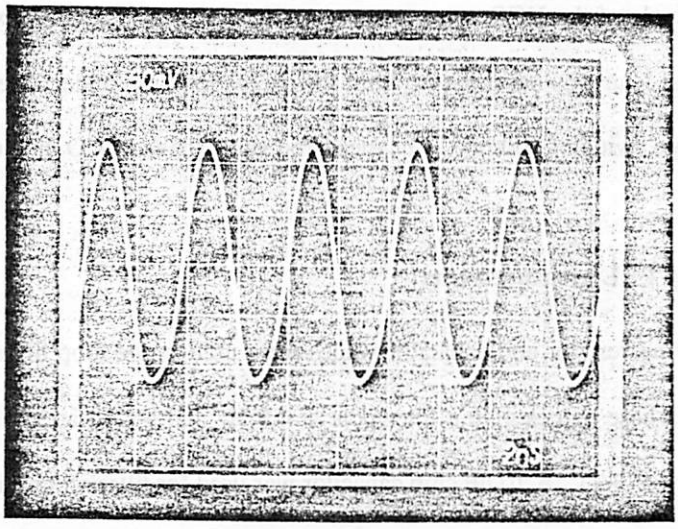


Figure 5.10 - VCO tuning range at 188 MHz.

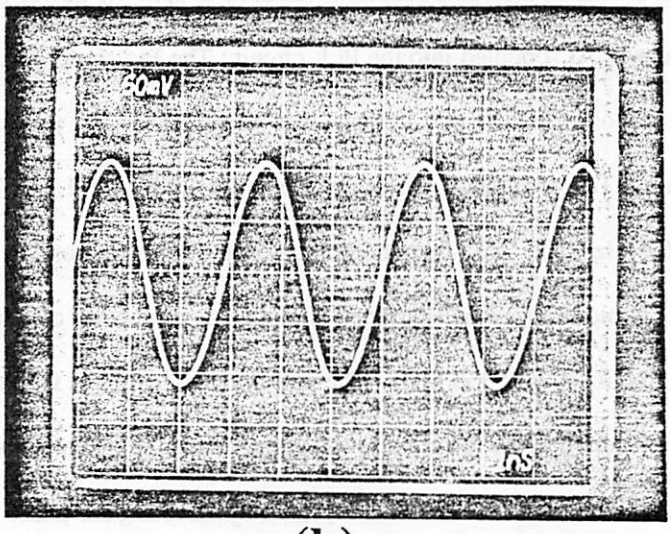
The ideal case with no parasitics is also plotted for comparison. The fixed capacitance reduces the tuning range to less than +2 and -4 percent. The average VCO gain estimated from these values is around $0.03\omega_o$ rad/(volt-sec). Similar results were obtained from the measurements at 216 and 235 MHz. Therefore, the DC loop gain of the PLL can be estimated as:

$$(0.14\,V/r)x(50)x(0.03\omega_o\ r/V\text{-}s) = 0.2\omega_o\ rad/sec.$$

Two different bonding schemes were used to check the effect of the package inductance on the VCO frequency. The varactor diode was bonded to the corner pins in one of them and to the center pins in the other. Figure 5.11 shows the VCO waveforms obtained in each case.



(a)



(b)

Figure 5.11 - VCO waveforms at (a) 250 MHz (b) 325 MHz.

When the center pins were used, the VCO center frequency increased from 250 MHz to 325 MHz for the same external inductance. The maximum oscillation frequency was measured to be 350 MHz when a silver wire of 5 nH with a Q of 10 was employed as the external inductor. The oscillation frequency is essentially determined by the package inductance at these frequencies. For a total capacitance of 15 pF, the inductance contributed by the package is about 9 nH.

The duty cycle of the VCO was measured at 73.5 MHz with a 1 KΩ external load on the tank circuit. The external load was necessary to limit the oscillation amplitude. The square-wave output of the VCO had a voltage swing of 400 mV. The measured value for the VCO duty cycle was 48 percent.

5.4. Closed Loop PLL Measurements

The following resistor and capacitor values were used in the loop filter: R_1 = 3 KΩ, R_2 = 300 Ω, and C = 10 μF. These values give a filter pole at 4.8 Hz and a zero at 53 Hz. Therefore the high frequency attenuation is 1/11. A 10 nF chip capacitor was used for filtering the ripple.

The Fluke 6071A Synthesized RF Signal Generator (200 KHz - 1040 MHz) was used as the input signal source. An Anzac H-8 Hybrid Junction was used to split the power into the PLL and the oscilloscope. The signal was AC-coupled into the PLL circuit. The PLL input and the output waveforms were observed on the oscilloscope. The pull-in range was measured varying the input signal frequency for different input levels. The frequency was read from the Fluke 6071A. Figure 5.12 shows the PLL waveforms at 350 MHz. The VCO output amplitude was 125 mV across 50 ohm. (> ± 125 mV into the phase detector). The normalized pull-in range is plotted as a function of the input signal level in Figure 5.13. The center frequency was 350 MHz. The pull-in range increases with the input power as expected. It is more than 2 percent (± 1%) for input levels greater than -23 dBm. In order to check the possibility of injection locking, the measurements were repeated by disabling the phase detector current source. No injection locking was observed up to an input level of -10 dBm.

The phase error was measured as ± 0.1 nS at 350 MHz. The total pull-in range was 13 MHz at an input level of -20 dBm. This corresponds to a phase error of ± 0.22 radian (± 12.6 °) for a pull-in range

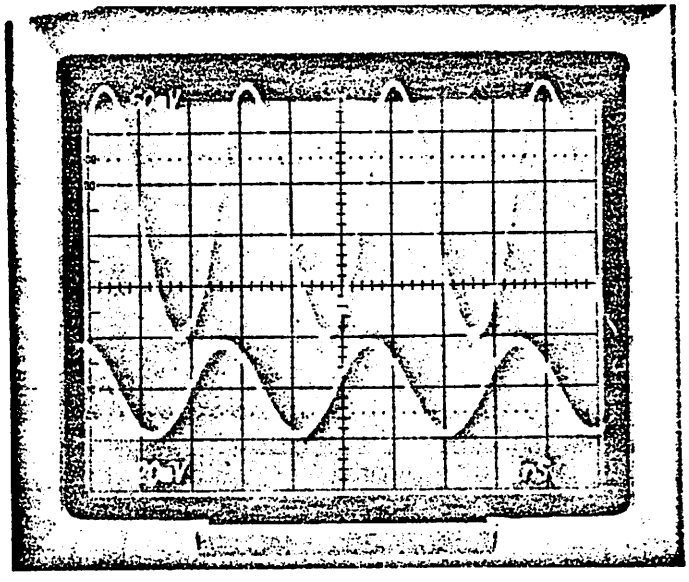


Figure 5.12 - PLL waveforms at 350 MHz (upper trace: VCO, lower trace: input).

of ±1.9 percent. Therefore, the DC loop gain can be estimated as:

$$\frac{0.019\omega_o}{0.22} = 0.09\omega_o \; rad/sec.$$

This is about half of what was estimated from the open loop measurements. The resolution of the oscilloscope screen is 0.1 nS introducing error into the measurements. Therefore, an average value of $0.15\omega_o$ can be assumed for the DC loop gain. The SPICE simulations with a first-order loop gave a phase error of ± 7 ° for a frequency variation of ± 1 percent. Therefore, there is a good correlation between the measurement and the simulation results. The simulation of the second-order loop was not attempted due to the enormous CPU time required. Only light ripple filtering was employed in the first-order loop simulations.

5.5. Discussion

Table 5.1 shows a summary of the performance characteristics of the monolithic PLL.

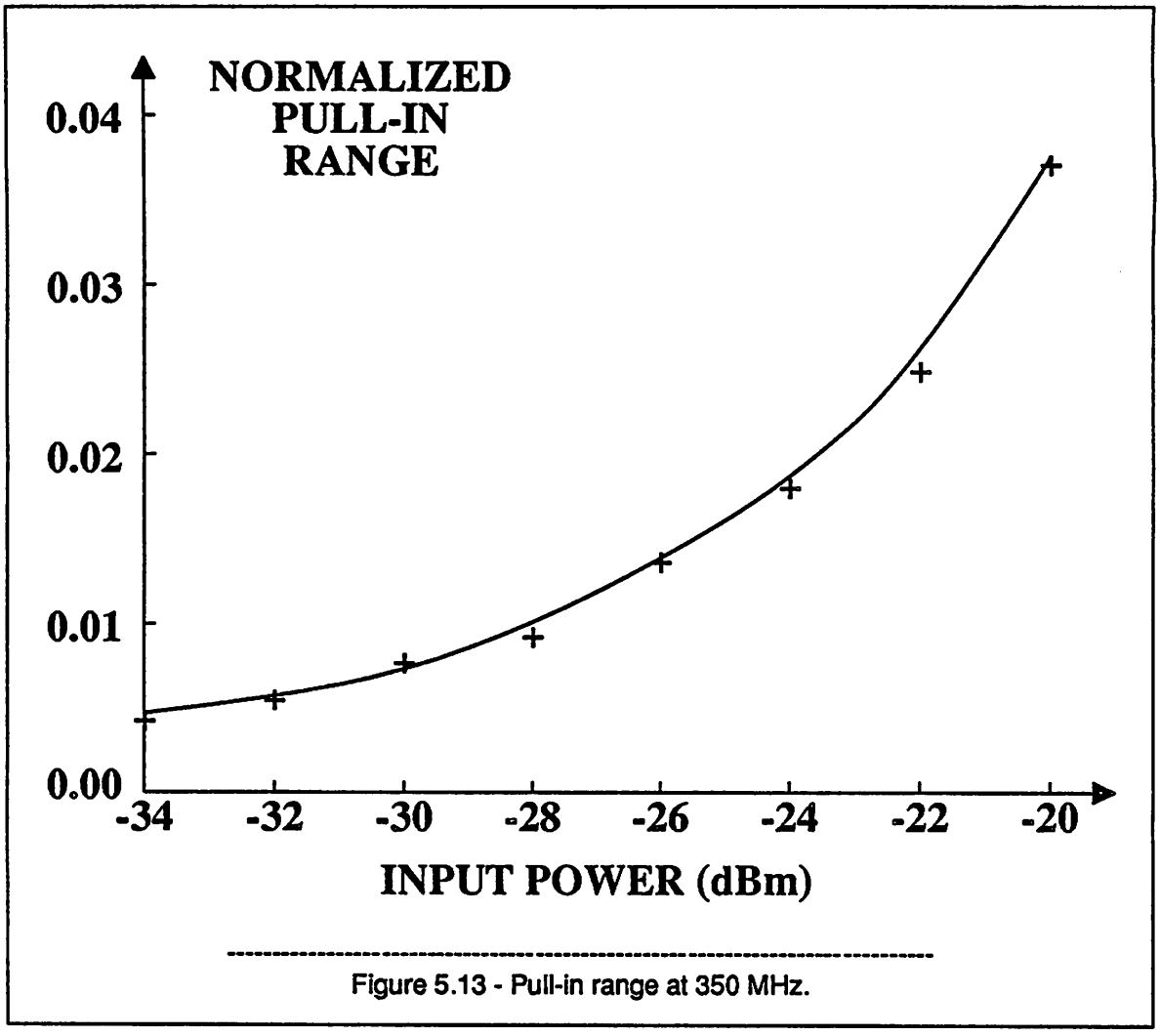


Figure 5.13 - Pull-in range at 350 MHz.

Supply Voltage	5 V
Power Consumption	270 mW
Maximum Frequency	350 MHz
Pull-in Range (at -23 dBm)	2 % at 350 MHz
DC Loop Gain	$> 0.09\omega_o$ rad/sec
TC of Center Frequency	-100 ppm/°C
VC of Center Frequency	0.25 %/V
Total Offset	1.25 mV

Table 5.1 - Measured PLL characteristics.

A single 5-volt supply was used and the total power dissipation was 270 mW. The power consumption can be reduced by lowering the bias current levels for the buffer stages. This will also improve the emitter follower matching for differential outputs.

The measured maximum frequency of operation was 350 MHz. The circuit is expected to achieve better high-frequency performance with fewer pads and an optimum package. A strip-line package and the use of a two-sided printed circuit board with a ground plane would further enhance the frequency performance above 300 MHz.

The worst case VCO center-frequency variation is on the order of ±1 percent over 20 to 100 °C, for ±1.25 mV total offset and ±5 percent supply voltage variation. Therefore, the measured pull-in range is adequate for input signal levels larger than -23 dBm. As was discussed in Chapter 2, the noise bandwith can be estimated as:

$$B_L \approx 0.25\, K_{DC}\, \frac{F(\infty)}{F(0)} = 0.25\,(0.09\omega_o)\,\frac{1}{11} = 0.002\omega_o\ Hz.$$

Therefore, Q_{PLL} can be found as:

$$Q_{PLL} = \frac{\pi}{4}\,\frac{f_o}{B_L} = 61$$

Increasing the filter attenuation by a factor of 3 results in $Q_{PLL} = 183$.

The die photo of the test chip is shown in Figure 5.14. The active area is 0.5 mm^2. The minimum pad size (110x110 μ^2) and the number of pads (32) determine the total chip area. The varactor diode is located on the upper right corner of the chip. It occupies an area of 250x340 μ^2 with the metal lines. The substrate contacts are placed close to the critical devices in the high-frequency path such as the varactor diode. A buried-P layer would help the shielding of the varactor diode by reducing the coupling through the substrate at higher frequencies. Connecting the n-side of the varactor to a separate supply would also help in several ways. First of all, the reverse bias across the varactor could easily be varied for different tuning range requirements. Secondly, the effect of the substrate junction would substantially be reduced. This can also be achieved by using multiple bonding wires for the varactor pins.

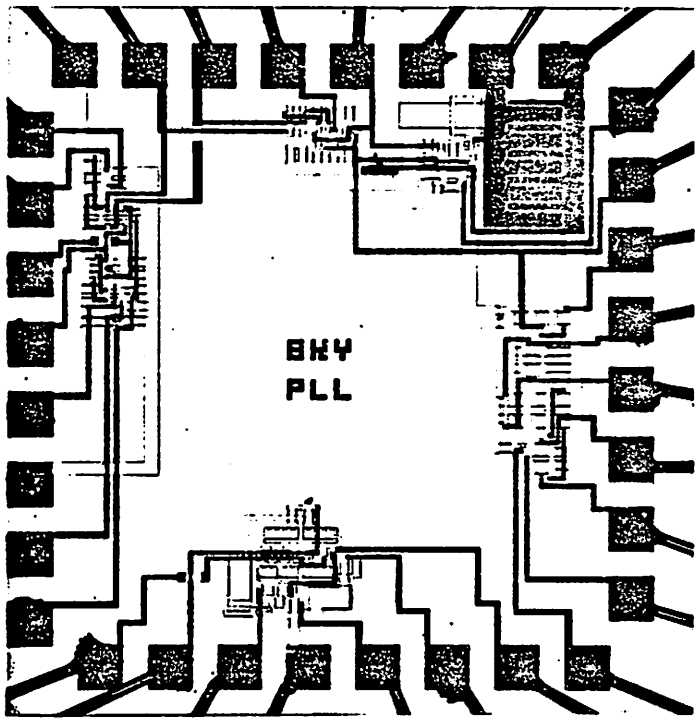


Figure 5.14 - Die photo of the test chip.

CHAPTER 6

CONCLUSIONS

In this thesis, the research carried out for realizing monolithic phase-locked loops (PLLs) above 100 MHz in silicon bipolar technology has been described. The frequency limitations of main PLL building blocks have been investigated with a special interest in timing recovery applications. An on-chip high-Q varactor diode design improves the VCO performance considerably. Although the Colpitts oscillator can operate up to several GHz with a 10-GHz bipolar process, the ECP oscillator functions better below 500 MHz providing larger negative conductance. Analog phase detectors have been shown to perform better at these frequencies; however, they lack the frequency detection capability of digital phase detectors. A digital frequency detector which provides a pull-in range larger than ± 25 percent has also been designed. It can be used with a monolithic PLL if the extra cost of increased power consumption and area is justified.

A 2-micron oxide-isolated bipolar process is used to fabricate the PLL test chip. A varactor-tuned ECP-VCO and a single-balanced modulator have been employed as building blocks. The temperature and supply variations of the varactor has been compensated by a band-gap reference. The agreement between the measurement and simulation results is good. The total DC-offset is less than 1.5 mV. The VCO has a voltage coefficient of 0.3 percent/volt and a TC of -100 ppm/°C over 20 to 100°C up to 250 MHz. The high-frequency PLL performance has strongly been affected by the package. The maximum frequency of the PLL is 350 MHz even when housed in a 40-pin DIL package. The pull-in range was larger than the worst case VCO center-frequency variation of ±1 percent, thus allowing a small noise bandwith (Q > 100). The operation frequency of the monolithic PLL can be extended up to 500 MHz with a high-frequency package. The circuit dissipates low power (270 mW from a 5 V supply) and occupies a small area (0.5 mm^2). Therefore, it can be integrated into a larger subsystem. It is concluded that the analog circuit techniques combined with a mature silicon bipolar technology will continue playing an

important role in high-frequency applications such as the narrowband PLLs.

The future research topics include the feasibility of on-chip inductors to reduce the number of external high-frequency pins and the use of other technologies like heterojunction bipolar, GaAs MES-FET and NMOS. The lack of a band-gap reference in GaAs might require a crystal-controlled low-frequency channel with dividers in the main VCO channel. A high-frequency charge pump circuit would be very beneficial making an on-chip loop filter feasible.

APPENDIX A

ANALYSIS OF A DIGITAL PHASE-FREQUENCY DETECTOR

A.1 Introduction

Digital Phase-Frequency Detectors (DPFDs) are commonly used to improve the pull-in (frequency acquisition) range and the pull-in time of PLL circuits. Although widely used, the frequency discriminator characteristics of the DPFDs are little known. In the following sections, the phase and frequency detector characteristics of a typical DPFD will be analyzed in detail. Also, the non-ideal behavior of the digital circuitry due to gate delays will be shown to alter the DPFD's frequency and phase discriminator characteristics significantly, thus limiting its maximum frequency of operation.

A.2 Low-Frequency Analysis

The DPFD circuit to be analyzed is a well-known circuit which can be implemented using either D-type master-slave flip-flops or R-S latches as shown in Figures A.1 and A.2, respectively. The outputs U and D will respond only to the positive-going edges of the inputs, R and V. Therefore, input duty cycles do not have any effect on the outputs. When the two input frequencies are equal, one of the outputs has a duty cycle which is a function of the difference between the input transition times while the other output remains inactivated or low. Which output is active depends on the initial conditions. Hence, the time average of the differential output $(U - D)_{AVE}$ is a function of the input phase difference. Figure A.3 shows the input and output waveforms and Figure A.4 shows the phase detector characteristics for low frequencies at which the gate delays are neglected.

Now, let us assume that the two input frequencies, f_R and f_V, are not equal. Then, one can define:

$$\alpha = \frac{f_V}{f_R} \tag{A.1}$$

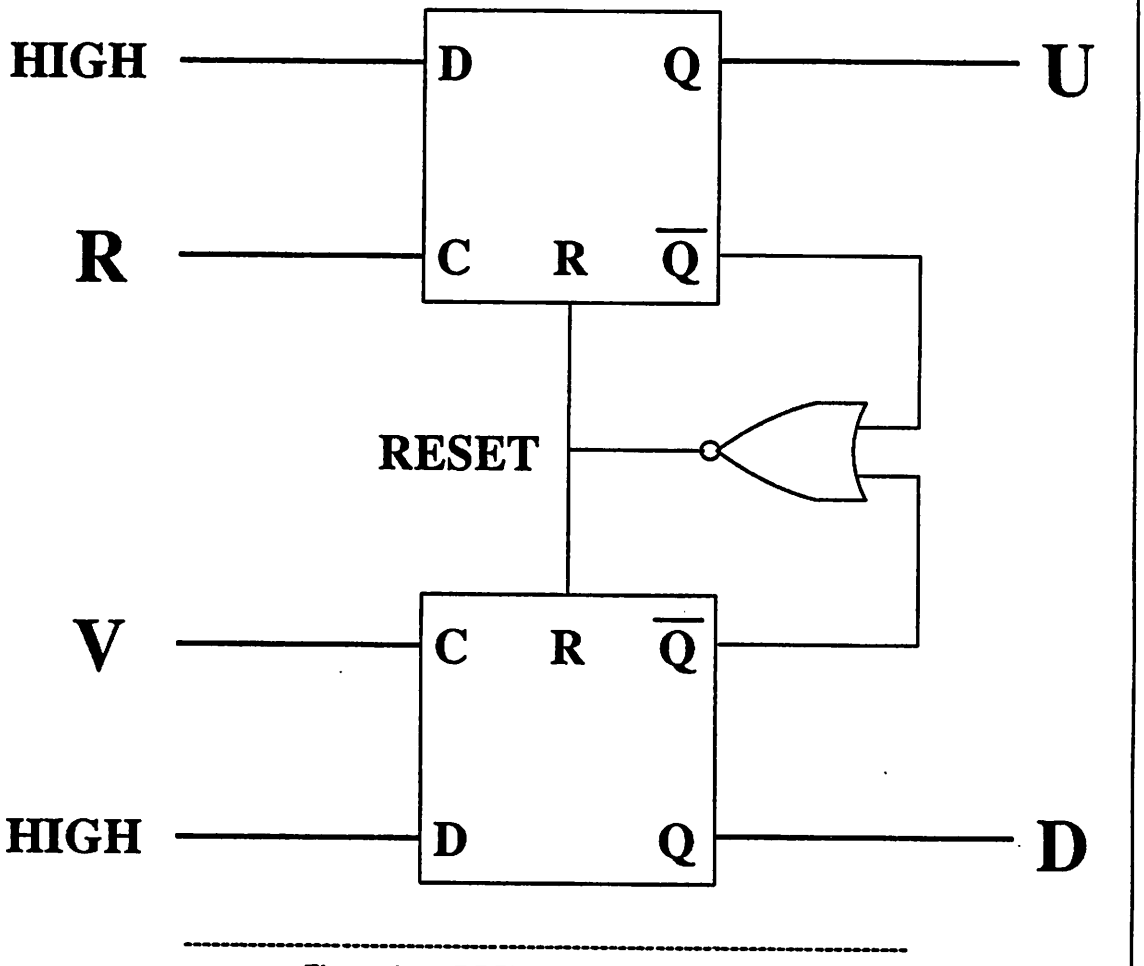


Figure A.1 - DPFD with D-type flip-flops.

and

$$\beta = \frac{f_R - f_V}{f_V} = \frac{1}{\alpha} - 1 \qquad \text{(A.2)}$$

If f_R is greater than f_V, then α is between 0 and 1 and β is always positive. In this case, the output U is set high by R and set low (or reset) by V. The output D ideally stays low. Furthermore, there is either a single or no V-transition between the two successive transitions of R. Figure A.5 shows the input and output waveforms for this case. Let us assume that R has two successive transitions at time t and $t + T_R$. Then, one can define the following probabilities:

$$P(0) = \textit{Probability of no V-transition in } [t, t + T_R] = 1 - \alpha \qquad \text{(A.3)}$$

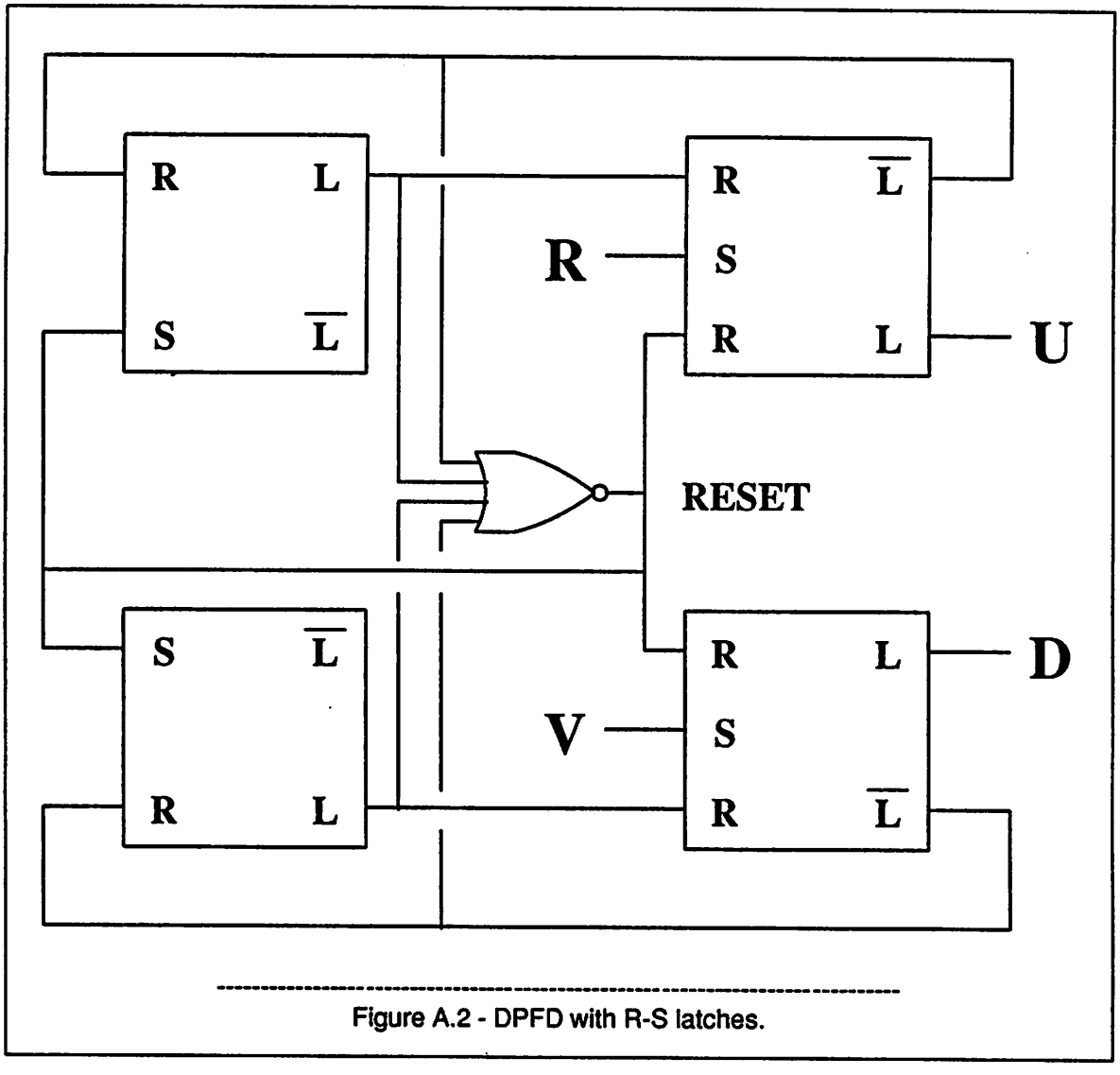


Figure A.2 - DPFD with R-S latches.

and

$$P(1) = \textit{Probability of a single V-transition in } [t, t + T_R] = \alpha \qquad \text{(A.4)}$$

Now, if there is no V-transition in [t, t + T_R], the output U is set to high at time t but never reset in that time interval. Therefore, $(U - D)_{AVE}$ normalized with respect to the logic swing is equal to 1. If there is a single V-transition in [t, t + T_R], the output U is set to high at time t and set to low when the V-transition appears. Assuming that the probability density function of a single V-transition within that interval is uniformly distributed, $(U - D)_{AVE}$ normalized with respect to the logic swing is equal to 0.5. Therefore, one has:

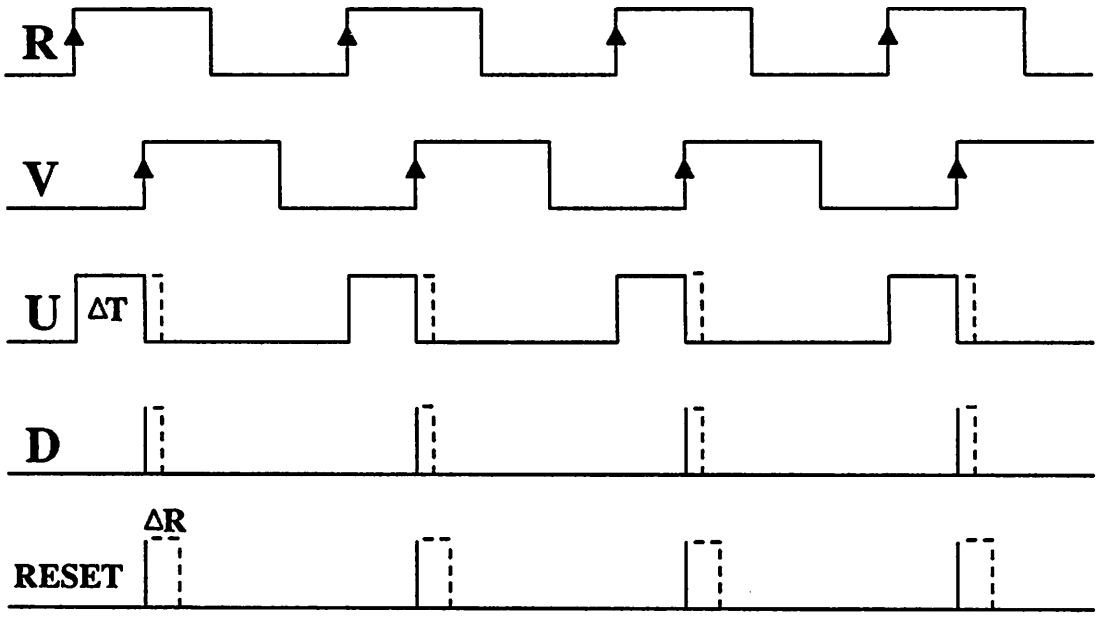


Figure A.3 - DPFD waveforms for equal input frequencies.

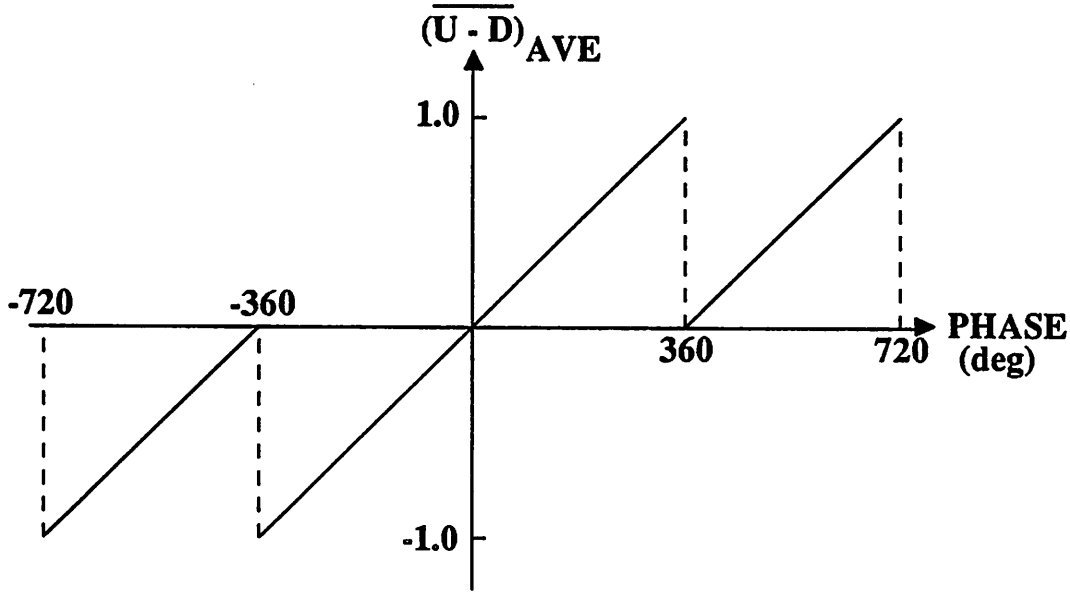


Figure A.4 - DPFD as a phase detector at low frequencies.

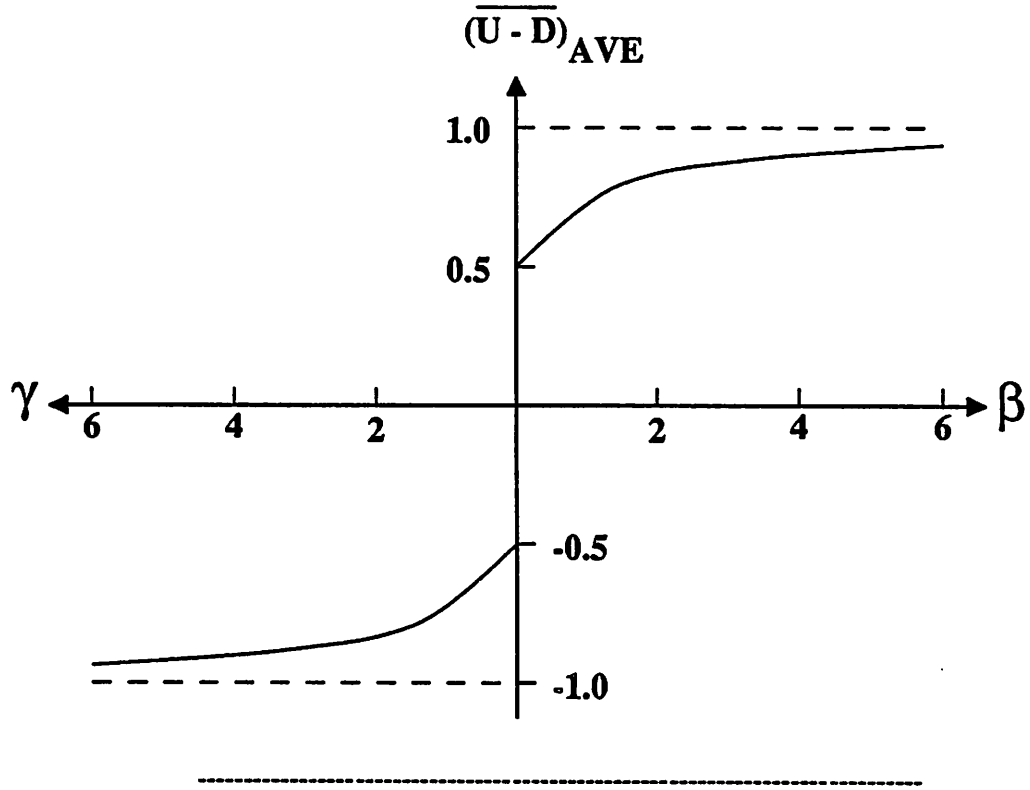


Figure A.6 - DPFD as a frequency detector at low frequencies.

A.3 High-Frequency Analysis

Let us refer to Figure A.1 and assume that both outputs are low initially. A transition at the R input sets the output U high. A following transition at the V input will set the output D high, creating a reset pulse at the output of the NOR-gate. This reset pulse will reset both of the outputs. When both outputs are returned to low, the reset pulse will be terminated by the NOR-gate so that the circuit is ready for the next input transition. The reset pulse has a finite width, ΔR as shown by the dashed lines in Figures A.3 and A.5, as a result of gate delays in the circuit. Therefore, a time interval ΔR is required for the circuit to return to its initial conditions before the next set of input transitions appear at R or V. This puts some limitations on the operation frequency of the circuit. Similarly, it is possible to show that the R-S latch version of the circuit also suffers from the same limitations at high frequencies.

First, the phase comparator characteristics will be examined where $T = T_R = T_V$. For phase differences between T - ΔR and T, the wrong output is activated reversing the polarity of $\overline{(U - D)_{AVE}}$. This

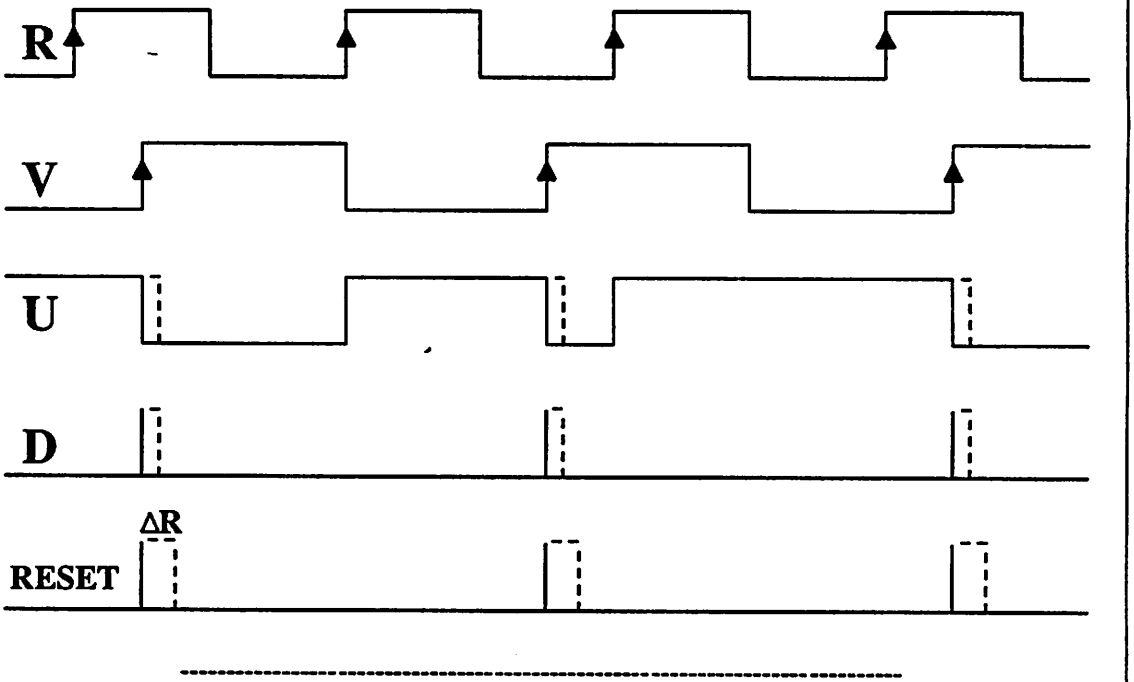


Figure A.5 - DPFD waveforms for unequal input frequencies.

$$\overline{(U-D)_{AVE}} = P(0)\,x\;1 + P(1)\,x\;0.5 = 1 - 0.5\,\alpha \tag{A.5}$$

from equations (A.3) and (A.4). Using equation (A.2) to replace α by β:

$$\overline{(U-D)_{AVE}} = \frac{\beta + 0.5}{\beta + 1.0} \tag{A.6}$$

Due to the symmetry of the circuits with respect to R and V, a similar analysis for $f_V > f_R$ yields:

$$\overline{(U-D)_{AVE}} = -\frac{\gamma + 0.5}{\gamma + 1.0} \tag{A.7}$$

where $\gamma = \frac{f_V - f_R}{f_R}$. Figure A.6 shows the low-frequency frequency discriminator characteristics of the DPFD. As it can be seen from Figure A.6, the DPFD circuits considered above have unlimited frequency acquisition capability at low frequencies. However, in a real PLL circuit, the VCO and the other loop components will put limits on the pull-in range.

Substituting equations (A.3) and (A.4) into (A.8):

$$\overline{(U-D)_{AVE}} = 1 - 0.5\,\alpha - \frac{\Delta R}{T_V} \tag{A.9}$$

Using equation (A.2) to replace α by β:

$$\overline{(U-D)_{AVE}} = \frac{\beta + 0.5}{\beta + 1.0} - \frac{\Delta R}{T_V} \tag{A.10}$$

Due to the symmetry of the circuits with respect to R and V, a similar analysis for $f_V > f_R$ yields:

$$\overline{(U-D)_{AVE}} = -\frac{\gamma + 0.5}{\gamma + 1.0} + \frac{\Delta R}{T_R} \tag{A.11}$$

where $\gamma = \frac{f_V - f_R}{f_R}$. Figure A.8 shows the high-frequency frequency discriminator characteristics of the DPFD.

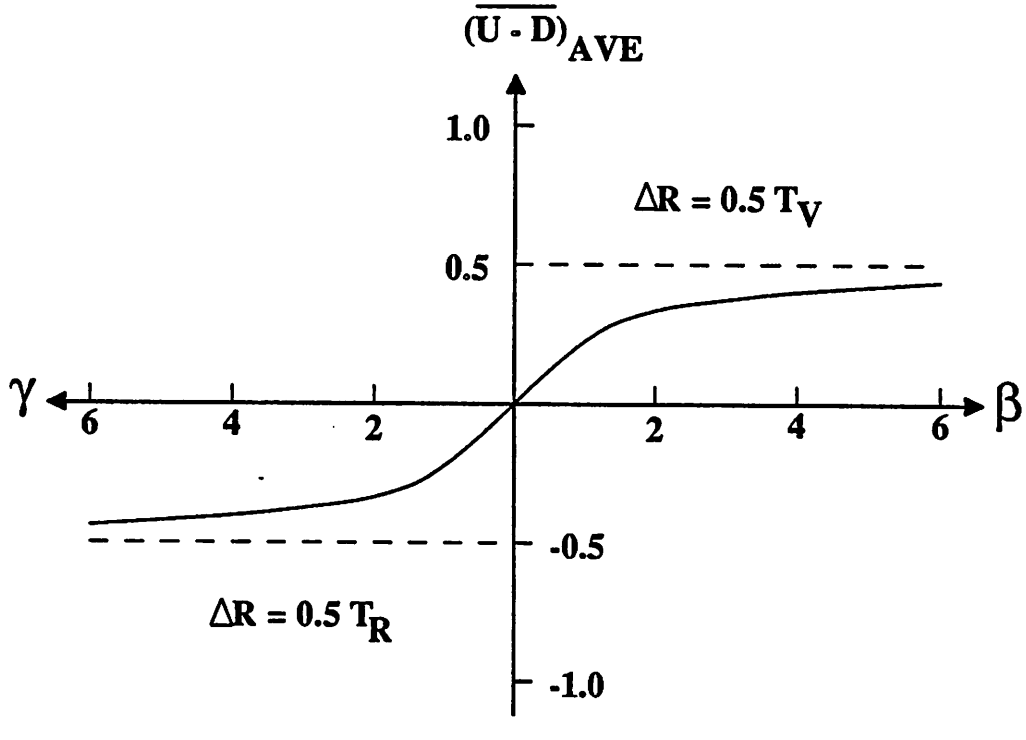


Figure A.8 - DPFD as a frequency detector at high frequencies.

narrows the linear range of the phase detector as shown in Figure A.7.

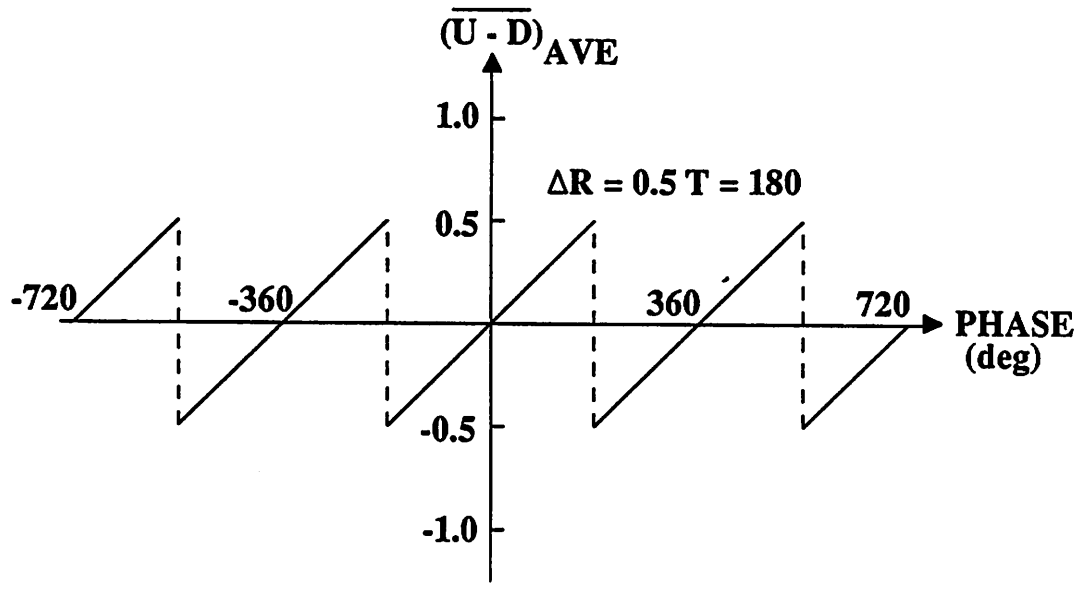


Figure A.7 - DPFD as a phase detector at high frequencies.

If ΔR is equal to 0.5 T, a sawtooth characteristics is obtained. Further reducing the period T will have detrimental effects on the frequency comparator characteristics of the circuits as it will be discussed next.

Let us again assume that f_R is greater than f_V and look at the time interval [t, t + T_R] between the two successive R-transitions. Now, the first R-transition at time t may or may not set the output U high depending on the ratio $\frac{\Delta R}{T_V}$. Actually, the probability that the R-transition at time t does not set the output U high is exactly equal to this ratio. This follows from the fact that the first R-transition does not set the output U high if it is within the time interval [t_V, t_V + ΔR] where t_V is the time at which the last V-transition appeared. Therefore, the probability that the first R-transition sets the output U high is 1 - $\frac{\Delta R}{T_V}$. Then, $(U - D)_{AVE}$ normalized with respect to the logic swing can be written as follows:

$$\overline{(U - D)_{AVE}} =$$

$$P(0)\,x\,1\,x\,\left[1-\frac{\Delta R}{T_V}\right]-P(0)\,x\,0\,x\,\frac{\Delta R}{T_V}+P(1)\,x\,0.5\,x\,\left[1-\frac{\Delta R}{T_V}\right]-P(1)\,x\,0.5\,x\,\frac{\Delta R}{T_V} \quad \text{(A.8)}$$

APPENDIX B

A DIGITAL ROTATIONAL-FREQUENCY DETECTOR DESIGN

B.1 Introduction

A digital rotational-frequency detector (DRFD) circuit is designed to improve the frequency acquisition capability of a PLL. In timing recovery applications, conventional phase-frequency detectors fail to function properly since some of the input transitions are missing. Although the new circuit does not have the phase detection property, it works reliably with random data inputs.

B.2 Circuit Design

The design philosophy is based on the rotational-frequency detector concept, [51]. The VCO-period is divided into four quadrants labeled A, B, C and D as in Figure B.1.

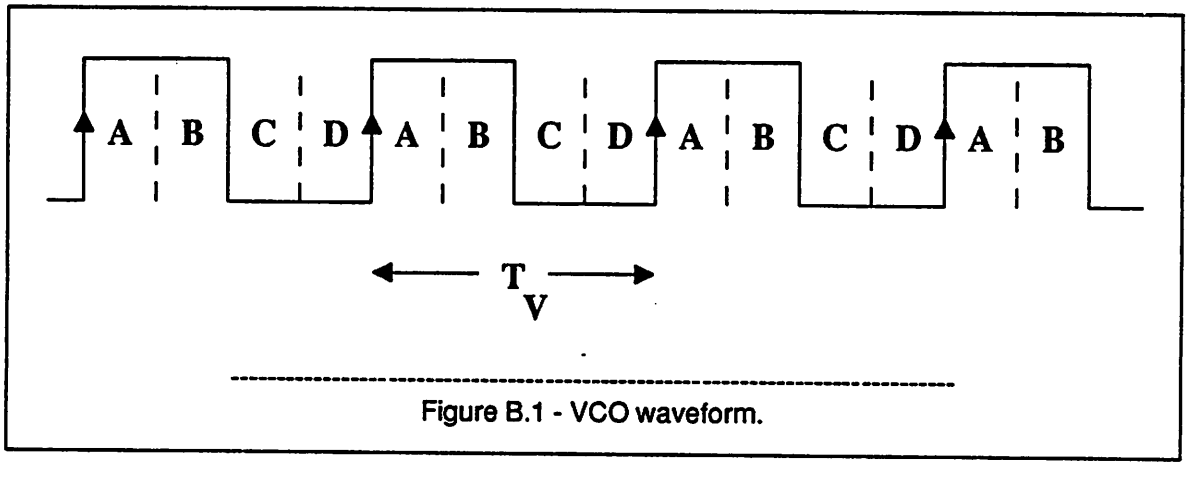


Figure B.1 - VCO waveform.

The circuit checks whether two successive data transitions are in two successive VCO-cycles or not, and also gives an output if one of the following conditions is met:

If a data transition in B is followed by a data transition in C ($1.5\, f_{DATA} > f_{VCO} > f_{DATA}$) then the output N which forces the VCO-frequency to decrease is active, if a data transition in C is followed by a

As it is seen from Figure A.8, $\overline{(U-D)_{AVE}}$ is reduced considerably as the frequency increases. If ΔR is equal to 0.5 T, $\overline{(U-D)_{AVE}}$ passes through the origin, thus providing very little output for small frequency differences. If ΔR is greater than 0.5 T, $\overline{(U-D)_{AVE}}$ will have the wrong polarity pushing the VCO frequency away from the input. As a result, this would lead to pull-out instead of pull-in.

These equations have been checked with SPICE simulations using a junction-isolated 4-GHz process and an oxide-isolated 12-GHz process and also with the measurements done on an off-the-shelf DPFD. The 4 GHz process gives a maximum frequency of operation of 115 MHz for the D-type master-slave version and 175 MHz for the R-S latch version. The 12 GHz process yields a maximum frequency of 600 MHz for the D-type master-slave version and 770 MHz for the R-S latch version. The power dissipation is around 475 mW with a single 5 V supply. For the 4-GHz process, ΔR is around 4 to 4.5 nS with the D-type master-slave flip-flops. This gives an estimated maximum frequency of 110 to 125 MHz agreeing with the simulation results. Similar estimations can be made for the other circuit and process variations. They all agree closely with the SPICE simulations. The measurements were done on a commercially available R-S latch version of the circuit (MC12040) which is fabricated with a 1 nS gate-delay bipolar process and consumes a power of 520 mW. ΔR measured from the phase characteristics was 5 nS. This puts the upper limit on the frequency of operation as 100 MHz which is close to the typical operating frequency given in the data sheet (70 MHz).

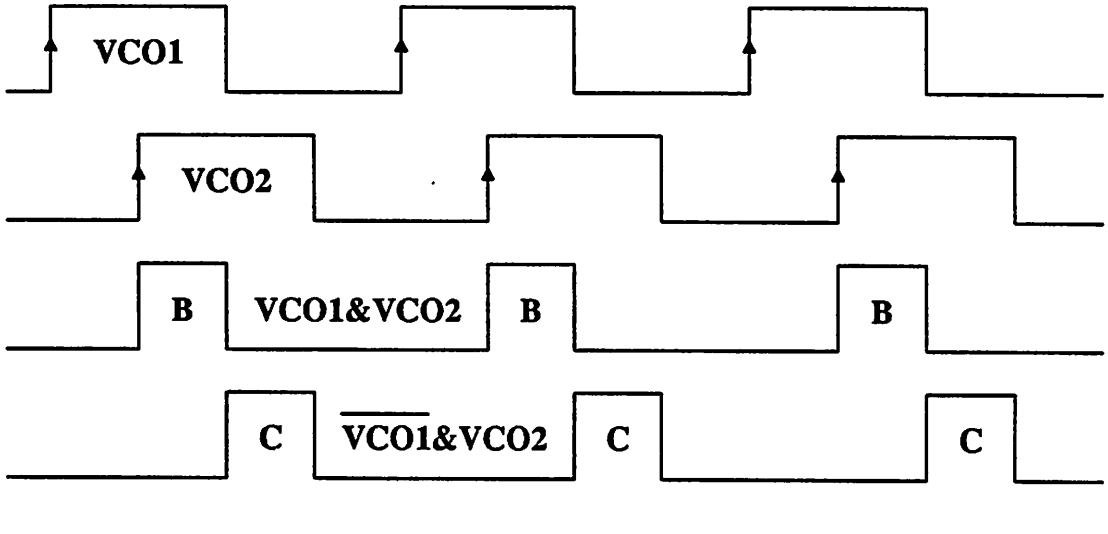


Figure B.3 - Obtaining waveforms B and C.

found as:

$$Pr[N] = Pr[B_k, C_{k+1}] = \frac{1.5\,T_V - T_D}{T_D} \tag{B.1}$$

for $1.5\,T_V > T_D > 1.25\,T_V$, and

$$Pr[N] = Pr[B_k, C_{k+1}] = \frac{T_D - T_V}{T_D} \tag{B.2}$$

for $1.25\,T_V > T_D > T_V$.

Note that there is also a probability that C_k follows B_k in the same VCO-cycle and causes the output N to be active for $T_D < 0.5\,T_V$. From Figure B.5(b) this probability can be found as:

$$Pr[N] = Pr[B_k, C_k] = \frac{0.5\,T_V - T_D}{T_D} \tag{B.3}$$

for $0.5\,T_V > T_D > 0.25\,T_V$, and

$$Pr[N] = Pr[B_k, C_k] = 1 \tag{B.4}$$

for $0.25\,T_V > T_D > 0$.

data transition in B ($f_{DATA} > f_{VCO} > 0.5\, f_{DATA}$) then the output P which forces the VCO-frequency to increase is active. The frequency detector outputs are zero for all other cases.

The complete circuit which works accordingly is shown in Figure B.2.

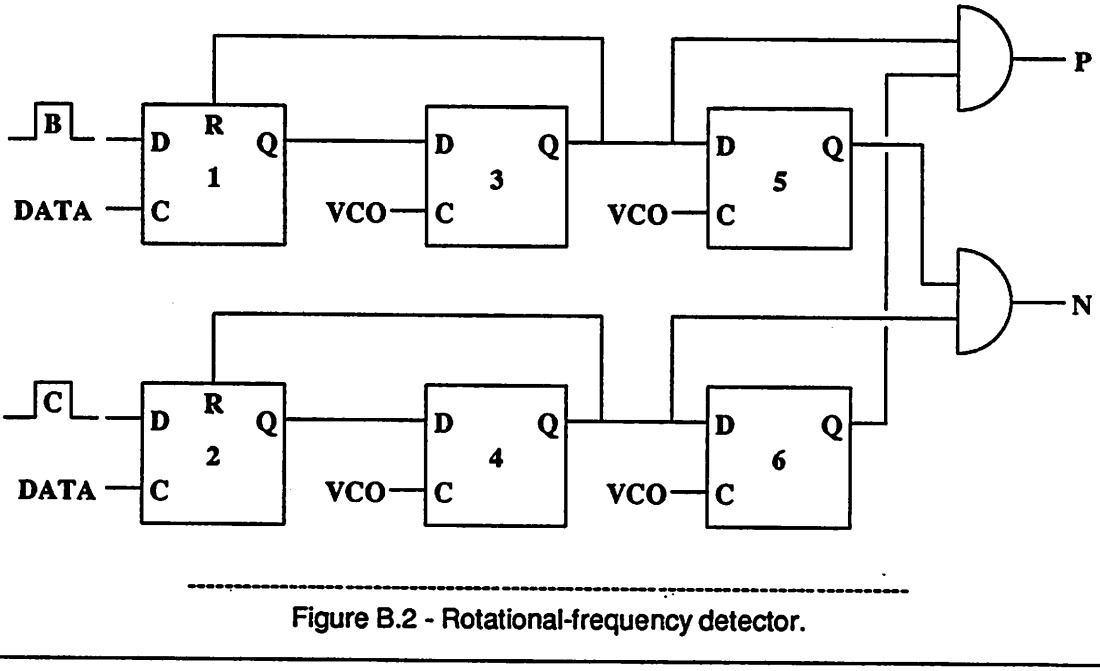


Figure B.2 - Rotational-frequency detector.

The inputs B and C can be obtained from VCO and its 90 degrees shifted version as in Figure B.3. This can be easily achieved with an L-C oscillator since current through the inductor lags the output voltage by 90 degrees.

Operation of the circuit with random data is shown by an example in Figure B.4, where $T_{VCO} = 0.8\, T_{DATA}$. The reset feedback from Q3-Q4 to Q1-Q2 maintains the proper operation of the circuit. If these reset inputs to Q1-Q2 are omitted, an erroneous pulse (at the output P in this case) also occurs at the DRFD output. This is shown by the dashed lines in Figure B.4.

B.3 DRFD Characteristics for Square Wave Inputs

Assume that $1.5\, T_V > T_D > T_V$. In this case, the output N is active, and from Figure B.5(a), the probability that a data transition in quadrant B_k is followed by a data transition in quadrant C_{k+1} can be

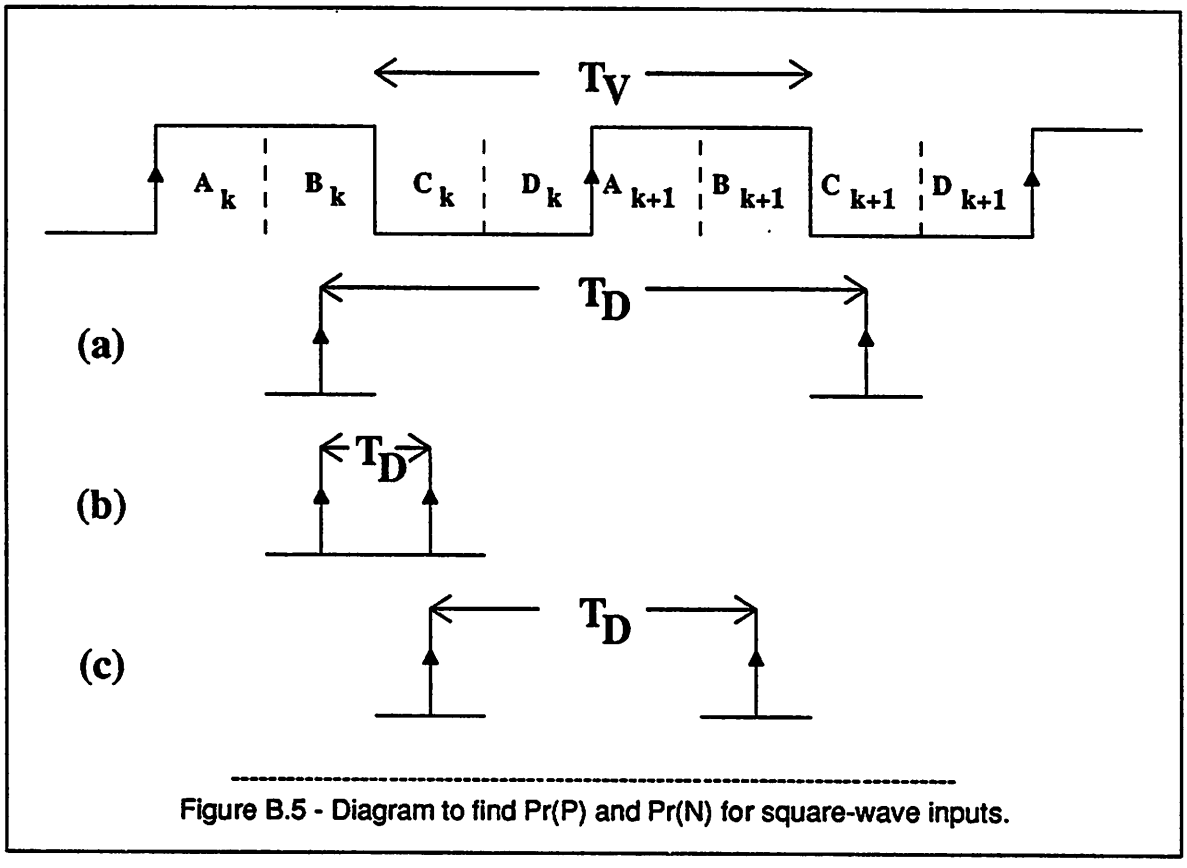


Figure B.5 - Diagram to find Pr(P) and Pr(N) for square-wave inputs.

available is given by:

$$\overline{(P-N)_{AVE}} = (Pr[P]-Pr[N])\frac{PULSE\ WIDTH}{T_V} \tag{B.7}$$

assuming equal output pulse widths on P and N.

In the circuit designed, output pulse widths are equal to T_V, therefore:

$$\overline{(P-N)_{AVE}} = Pr[P]-Pr[N]. \tag{B.8}$$

This equation is plotted in Figure B.6. Note that the DRFD output is useful only for $0.5 > \delta > -0.5$, where

$$\delta = \frac{f_D - f_V}{f_D}. \tag{B.9}$$

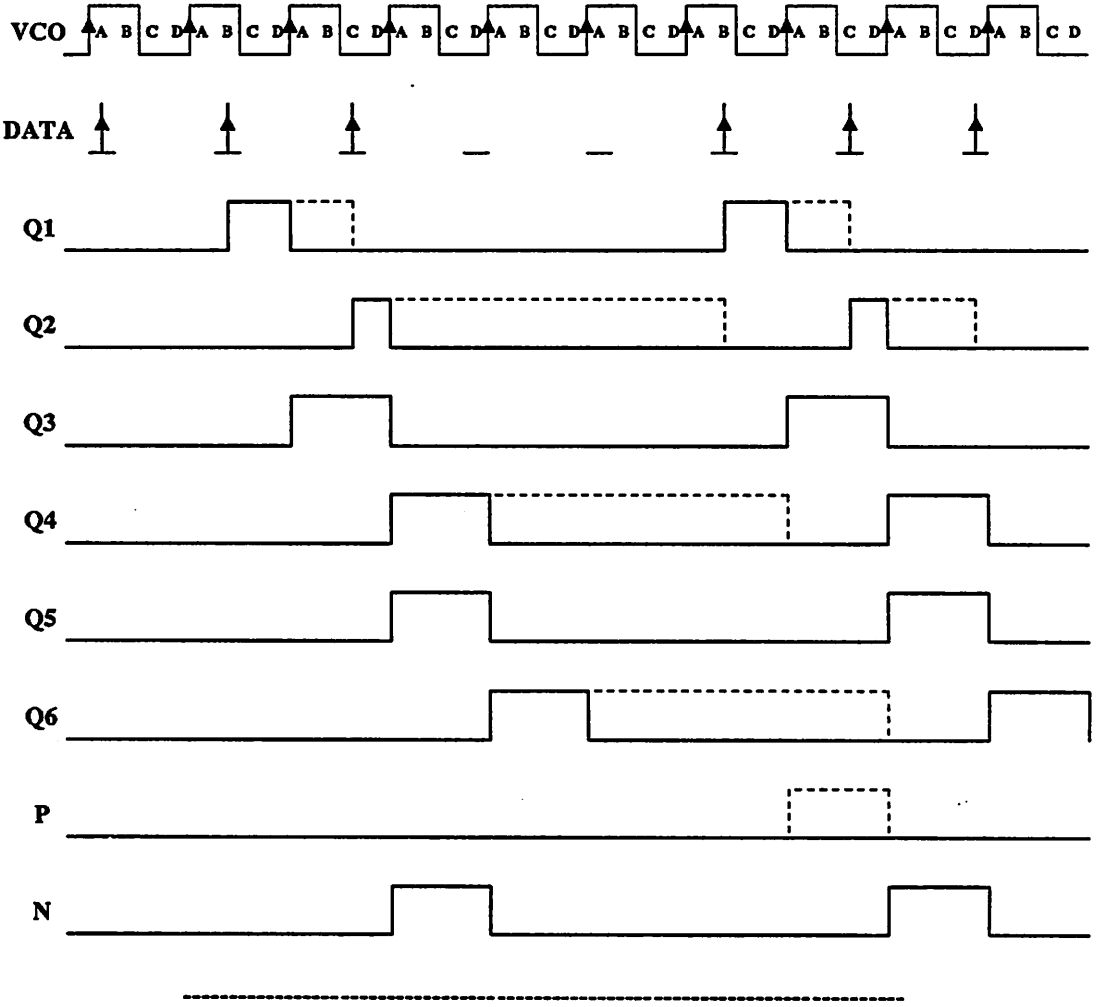


Figure B.4 - DRFD waveforms with random data.

Finally, the output P will be active for $T_V > T_D > 0.5\,T_V$, and from Figure B.5(c), we have:

$$Pr[P] = Pr[C_k, B_{k+1}] = \frac{T_V - T_D}{T_D} \tag{B.5}$$

for $T_V > T_D > 0.75\,T_V$, and

$$Pr[P] = Pr[C_k, B_{k+1}] = \frac{T_D - 0.5\,T_V}{T_D} \tag{B.6}$$

for $0.75\,T_V > T_D > 0.5\,T_V$.

Now, the average value of the frequency detector output normalized by the maximum pulse height

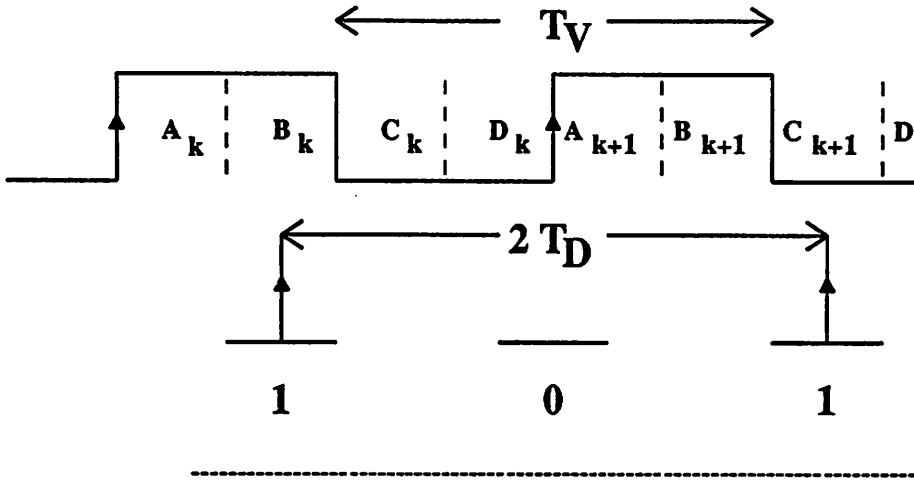


Figure B.7 - Diagram to find Pr(N) with random data.

$$Pr[N] = 0.125\,\frac{2\delta - 0.5}{1-\delta} \tag{B.10}$$

for $0.375 > \delta > 0.25$,

$$Pr[N] = 0.125\,\frac{1-2\delta}{1-\delta} \tag{B.11}$$

for $0.5 > \delta > 0.375$, and using Figure B.6:

$$Pr[P] = 0.25\,\frac{0.5-\delta}{1-\delta} \tag{B.12}$$

for $0.5 > \delta > 0.25$.

Figure B.6 is modified accordingly as shown in Figure B.8 for $0.5 > \delta > -0.5$. Note that the DRFD output is useful only for $0.375 > \delta > -0.5$.

B.5 Properties of the DRFD

The frequency detector characteristics are derived for square wave and random data inputs in sections B.3 and B.4, and plotted in Figures B.6 and B.8, respectively. It is clear from these characteristics that the designed circuit provides a correction voltage to the PLL for a ± 50 % offset in the VCO free-running frequency, for square wave inputs. For equally likely independent data, the VCO free-running

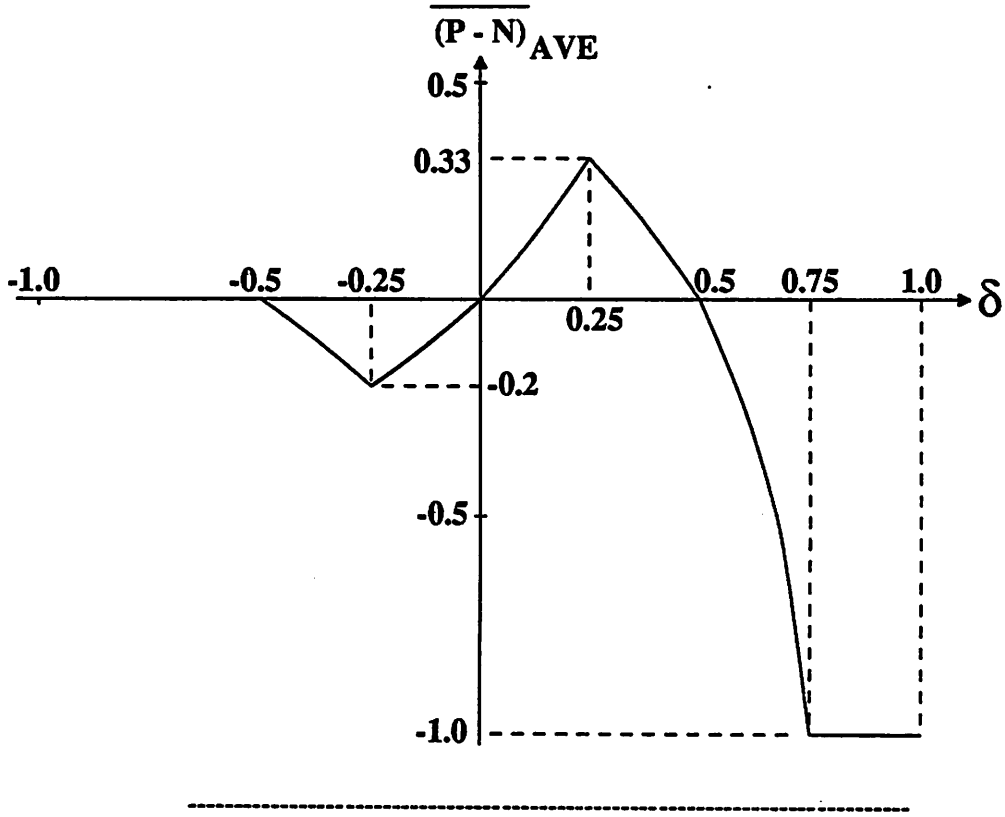


Figure B.6 - DRFD characteristics for square-wave inputs.

B.4 DRFD Characteristics for Random Data

For random data inputs, $\overline{(P-N)_{AVE}}$ of Figure B.6 must be multiplied by the probability of two data transitions in a row (0.25 for equally likely independent data).

However, this is true only for $T_D > 0.75\ T_V$ ($\delta < 0.25$), because if $T_D < 0.75\ T_V$, then either the P or N output can be active depending on the data sequence. Therefore, Figure B.6 must be further modified for $\delta > 0.25$.

Since the DRFD output is not useful for $\delta > 0.5$, we only need to examine the region where δ is between 0.25 and 0.5. In other words, we have to check the region in which $0.75\ T_V > T_D > 0.5\ T_V$. In that region, only the 101 data sequence will erroneously make the wrong output (N in this case) active as shown in Figure B.7. Therefore, the following probabilities can easily be calculated for equally likely data:

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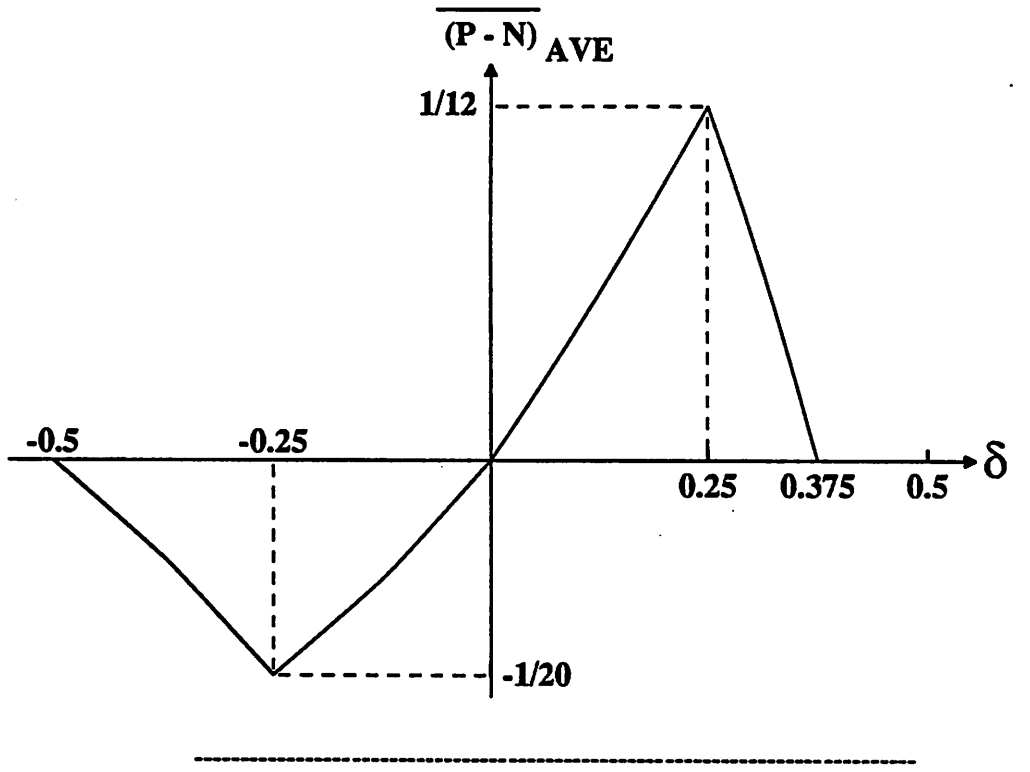

Figure B.8 - DRFD characteristics for random data.

frequency must be between 0.625 f_{DATA} and 1.5 f_{DATA} to get an useful DRFD output.

A PLL aided by this circuit can tolerate variations up to + 50 % and - 37.5 % in its free-running frequency, when it is used with equally likely random data inputs.

By a proper design of the phase detector, the data transitions can be kept in the vicinity of the D-to-A boundary in the VCO-cycle, when the PLL is in lock. Therefore, even an input phase jitter as large as ± 90 degrees will not produce any frequency comparator output. This is certainly a wide margin against input jitter.

The high-frequency performance of the circuit will be limited by the VCO transition times and flip-flop delays. The logic swing cannot be made too small since the DRFD output is proportional to it.

Since the circuit does not require any additional filtering (unlike the analog frequency comparators), it can easily be implemented in monolithic integrated form.

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