CMOS CHARGE DEMULTIPLEXING OPTICAL RECEIVER PROGRESS REPORT 1.0

by

Timothy Hu and Paul R. Gray

Memorandum No. UCB/ERL M88/28

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CMOS Charge Demultiplexing Optical Receiver
Progress Report 1.0

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ABSTRACT

The primary function of an optical receiver is to extract the optical signal from noise and other impairments, and reconstruct the signal information into the electrical domain correctly. Overall performance is determined by the preamplifier when a PIN diode is used as a photodetector[1]. Currently, two types of preamplifiers are commonly used; the transimpedance preamplifier and the high-impedance preamplifier[2]. When the operating frequency is in the medium range (~ 100 Mbit/s), the transimpedance preamplifier is most attractive and frequently used.

The objective of this research is to develop a new charge demultiplexing architecture using CMOS technology and to apply it to the design of a high speed receiver operating in the range of 100Mbit/sec, which is suitable for Local Area Network (LAN) applications. A receiver with this speed capability is difficult to implement in CMOS technology currently in production using the traditional architectures. Switched-capacitor circuit techniques together with parallel and pipelined signal paths are used to achieve the requirements. Problems under investigation are the system architecture and clock recovery scheme.

This progress report is a description of the work done on the receiver front end to date.

May 3, 1988

CMOS Charge Demultiplexing Optical Receiver
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1. Introduction

The primary function of an optical receiver is to extract the optical signal from noise and other impairments, and reconstruct the signal information into the electrical domain correctly. Overall performance is determined by the preamplifier when a PIN diode is used as a photodetector[1]. Currently, two types of preamplifiers are commonly used; the transimpedance preamplifier and the high-impedance preamplifier[2]. When the operating frequency is in the medium range (~ 100 Mbit/s), the transimpedance preamplifier is most attractive and frequently used.

Traditionally, implementations of direct detection fiber optic receivers have involved the use of several integrated circuit chips in the signal path between the photodiode and the parallel data interface to the host system. A broadband transimpedance amplifier, implemented in high speed bipolar technology for the lower speed ranges or GaAs for the higher speeds, is used to convert the photocurrent signal to a low-level voltage. A second bipolar chip is often included following this to do pulse shaping and other functions, and a third chip is used to perform timing recovery, decision, and serial-parallel converter functions.

The motivation for investigating new architectures for direct detection receivers is twofold. First, the current transimpedance amplifier configuration has the property that in an optimized design, its noise performance is dominated by the noise in the feedback resistor. The ability to make this resistor large, minimizing its noise current contribution, is limited by bandwidth considerations. As a result, the optical power required in such receivers for a given bit error ratio is usually far greater than that dictated by the quantum limit or other fundamental limits. It appears possible that other circuit approachs that capture and process the photogenerated charge packets directly may yield superior signal-to-noise performance.

The second motivation is cost reduction. A single-chip implementation of the complete receiver function from photodiode to digital parallel bus would have important economic benefits. However, there are important technological barriers to achieving this. The first is the handling of the low-level photocurrent signal on the same chip as large, high-energy amplified versions of it. Noise and parasitic feedback effects have precluded putting the entire function on fewer chips in the past. The second is that the serial-parallel converter requires complex digital processing, while the front end amplifier requires a technology capable of very wide analog bandwidth and low noise. While considerable work has been done on the implementation of broadband amplifier functions in MOS technology, most often the front end chips are GaAs or high speed bipolar while the processor is CMOS.

The objective of the proposed work is the investigation of new approachs to fiber receivers which would result in improved signal to noise ratio and higher levels of integration, at least for a range of data rates at the lower end of the spectrum of interest. A new architecture involving the direct processing of charge packets using switched capacitor circuitry will be used. Problems of low-noise charge parsing and clock recovery with baud rate sampling will be particularly emphasized. It is anticipated that the results of this work may be most applicable in the 100Mb/sec range of transmission rates as used for example in some local area network applications.

2. Optical Fiber System

A block diagram of a simple direct detection optical fiber digital communication system is given in Fig. 2.1.

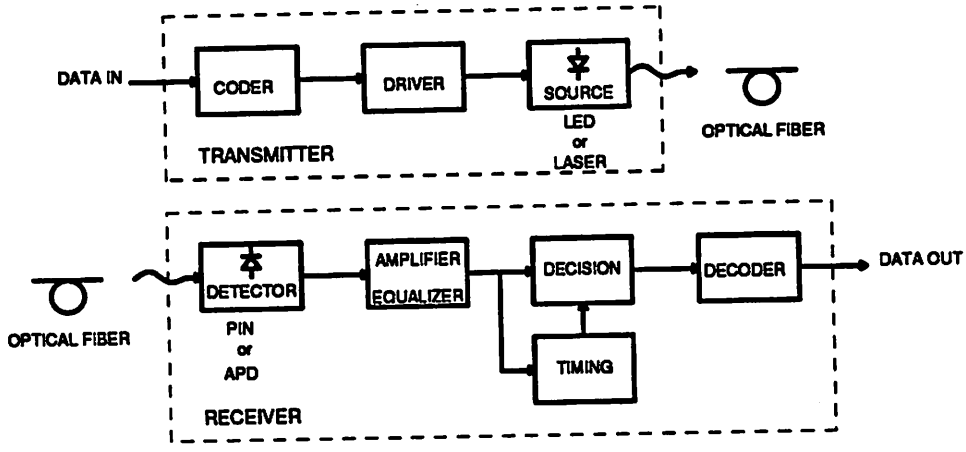

Fig. 2.1 Block diagram of an optical fiber digital transmission system

Like any other transmission system, it contains three main blocks: a transmitter, a transmission medium or channel, and a receiver.

The transmitter contains a line coder which converts the input sequence with an input rate into symbols with a symbol rate. The output of the coder is a binary stream of data with a certain bit rate. The relationships between the data rate, the symbol rate, and the bit rate depend on the coding scheme used. If the data is in a parallel form, the coder also has to perform parallel to serial conversion. This signal modulates, through a driver circuit, the intensity of the output power of the optical source which can be a light emitting diode (LED) or an injection laser diode.

The emitted power is injected into the optical fiber and propagates along it according to the principles of total internal reflection. During propagation the optical signal pulses suffer attenuation and dispersion. The dispersion is minimized in the region of 1.3 μm wavelength and the attenuation is about 0.3 dB/km for single mode fiber[3]. This wavelength is assumed to be used in our prototype as it is used in a lot of local area network standards[4].

At the receiver side, the optical pulses are converted, through the photodetector (PIN diode or avalanche photo diode APD), into electrical current pulses, which are amplified and equalized in order to maximize the signal-to-noise ratio at the decision point. The PIN diode is cheaper, has a higher bandwidth,

and operates at a lower biasing voltage than the APD. On the other hand, the APD can give higher sensitivity (5 to 15 dB higher) and a wider dynamic range. Therefore, depending on the application, the designer can have a choice. In our prototype, a PIN diode is assumed because of its low biasing voltage makes the use of single power supply possible.

The equalized signal is then regenerated by a time recovering circuit and decoded in order to deliver the original sequence. If parallel data is desired, a serial to parallel conversion has to be done by the decoder.

3. Characteristics of the Receiver

The characteristics of an optical receiver vary with the application. An example of some typical requirements for next generation local area networks[4,5] is shown in Table 3.1 below.

Typical requirements for LAN applications	
Bit Rate	125Mb/s
Bit Period	8ns
Bit Error Rate (BER) (MAX.)	10^{-9}
Signal to Noise Ratio (MIN.)	22dB
Minimum Optical Power Level	-27dBm
Maximum Optical Power Level	-10dBm
Minimum Signal Current	2μA
Minimum Signal Charge per Bit Period	16fC
Minimum number of Photons per Bit Period	100,000
Maximum Equivalent Input Noise Current	$160nA_{rms}$
Dynamic Range	40dB

Table 3.1 Typical Requirements for LAN applications

For future LAN applications, the Bit Rate must be higher than 100Mb/s. There are commercially available optical receivers that can achieve this high bit rate but all of them are either implemented in high speed bipolar technology or GaAs technology. In order to do complex data manipulation and coding on the received data, the link controller/processor chips are all implemented in CMOS technology. In order to reduce cost, a high level of integration is desired. Using traditional optical receiver architectures with CMOS to achieve such high bit rate is impossible at the moment because of the low f_T of the present CMOS technology. The fastest CMOS optical receiver reported so far is the AT&T ODL 50 Lightwave Data Link operating in the range of 50Mb/s which uses a transimpedance preamplifier[6].

The higher the sensitivity of the preamplifier, the lower the transmitting power required or, alternatively the longer the separation between repeaters for a fixed BER results in lower cost. Sensitivity down to -50dBm at 140Mb/s has been reported[7], corresponding to only 500 photons are needed per bit period. Even for this case, we are still more than an order of magnitude from the quantum limit of 20 photons per bit period. This is because the noise is dominated by the thermal noise of the preamplifier. Detailed explanations are given in the section reviewing traditional architectures.

The distance between optical repeaters varies from one site to another resulting in a wide range of incident optical power. The receiver must therefore has a large dynamic range.

The four main goals of this research is to first, find a new architecture that can achieve a higher bit rate than other architectures built with the same technology. Second, to achieve a higher sensitivity than existing architectures. Third, to have adequate dynamic range, and last but not least, to put the preamplifier, timing recovery and a serial-to-parallel converter all on the same chip.

4. Traditional Architectures for Optical Preamplifier

The photodetector converts the optical power into current. Since this current is small, a preamplifier is used to amplify and convert the current into voltage, while at the same time introducing as little noise as possible. If a PIN diode is used, the noise is dominated by the receiver and therefore for comparison purposes, a PIN diode is assumed.

4.1. High Impedance Amplifier

A simplified circuit diagram of a high impedance amplifier[8] is shown in Fig. 4.1.

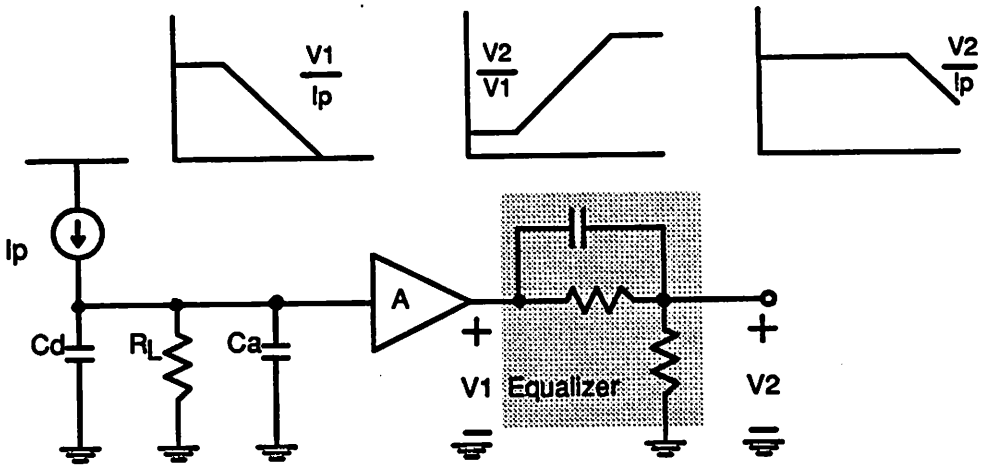

Fig. 4.1 Simplified circuit diagram of a high impedance amplifier

The photodiode can be modeled as a current source with a parasitic capacitance C_d. The amplifier is implemented with GaAs FETs to get a high impedance input and is biased with a high load resistor R_L. Only the input capacitance C_a of the amplifier is shown because the input resistance is large compared to R_L and is shunted away. This amplifier is widely used in applications where high bandwidth is required (above 100 MHz). As shown in the figure, an equalizer has to be put at the output to equalize the input for a flat band respond with high cutoff frequency.

The major advantage of this type of amplifier are high SNR because of the high input resistance, the equivalent input noise current is low results in high sensitivity. The high g_m of the GaAs FET allows the amplifier to have a low input capacitance C_a. Therefore maximum power transfer from photodetector is obtained.

The disadvantages are that the required large RC time constant reduces the front end bandwidth and an equalizer is required. This introduces a lot of design complexity in matching the pole and zero between the front end and the equalizer. Also, the low frequency components of the signal at the front end are enhanced causing early saturation of the amplifier which limits the dynamic range.

4.2. Transimpedance Amplifier

To increase the dynamic range of the high impedance receiver, a transimpedance amplifier[9] can be used. A simplified circuit diagram of a transimpedance amplifier is shown in Fig. 4.2 (a).

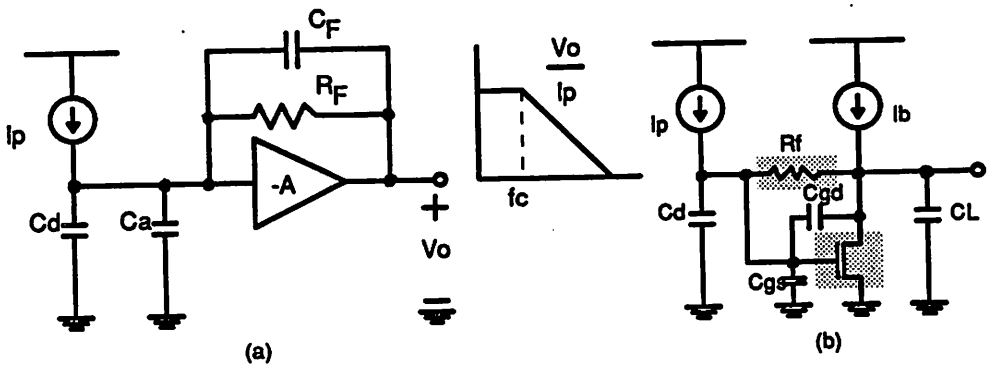

Fig. 4.1 (a) Simplified circuit diagram of a transimpedance amplifier

(b) Model used for noise calculation.

The amplifier here acts as an operational amplifier and therefore must have a high gain. The photo current passes through the feedback resister R_F with a parasitic capacitance C_F and is converted to voltage at the output. The advantages of the transimpedance amplifier are better dynamic range since no early saturation for low frequency components and no need for a matched equalizer for the front end. The disadvantages are lower bandwidth and lower sensitivity. Using the simplest model shown in Figure 4.2 (b), one can show that the equivalent input noise current is as follows:

$$\overline{i_n^2} = \frac{4kTB}{R_F}\left(1 + \frac{1}{3g_mR_F}\right) + \frac{8\pi^2}{9}(4kT)\left[\frac{B^3LC_d}{vsat}\right]$$

which is dominated by the thermal noise of the feedback resistor R_F. In order to have high sensitivity, R_F must be large. But on the other hand, the bandwidth of the preamplifier can be shown to be

$$\frac{V_o}{I_p} = \frac{-R_F}{1 + j\omega R_F\left[C_F + \frac{C}{A}\right]} \qquad C = C_d + C_a$$

where

$$\omega_c = \frac{A}{R_F(C + AC_F)}$$

When C, the total input capacitance is much larger than AC_F, the bandwidth is determined by the RC time constant of R_F and C. To have a high bandwidth, R_F must be small which contradicts with the low noise requirement. Besides these, the phase shift of the amplifier also limits the gain that can be employed within feedback loop without instability also requires a lower R_F. Also, if the shunt capacitance C_F of the feedback resistor is large, it can also limit the bandwidth. That is why this type of circuit is usually built with bipolar technology[10,11] operating in the low frequency range (around or below 100MHz) although GaAs technology is also used for higher frequency applications. The use of GaAs technology has the extra advantage that the high f_T allows a lower C_{in} for the amplifier and so a higher R_F can be used for a fixed bandwidth resulting in higher sensitivity[7].

4.3. Problems for implementation using CMOS in the 100Mbit/s range

In the sub 100Mb/s range, people trying to achieve high level of integration by implementing the receiver in CMOS, always use the transimpedance amplifier approach because no equalization is required. The additional design complexity of the high impedance amplifier just doesn't pay in this case and the low dynamic range makes it unattractive for LAN applications. For a particular type of application, the minimum required sensitivity is set by the required BER and minimum received power. This put a lower bound on R_F. The maximum bit rate achievable is then limited by the speed or f_T of the technology. The highest speed receiver commercially available thus far is the ODL 50 from AT&T which is implemented in 1.75μm CMOS, with a bit rate of 50Mbit/s and the sensitivity is -29dBm at a BER of 10^{-9}[12].

Fundamentally, a speed limit is set for this type of architecture and a new architecture is necessary for improvement in both speed and sensitivity.

5. Charge Demultiplexing Receiver

The major reason we cannot implement CMOS optical receiver in the 100Mb/s range is that the amplifier used must have the full bandwidth of the optical signal. One alternative approach that releases the bandwidth requirement is called the charge demultiplexing receiver. The system architecture is show in Fig. 5.1. It consists on four main blocks. A parallel channel front end receiver, a pipelined sampled and hold with decision feedback equalizer, a slicer, and a clock recovery block.

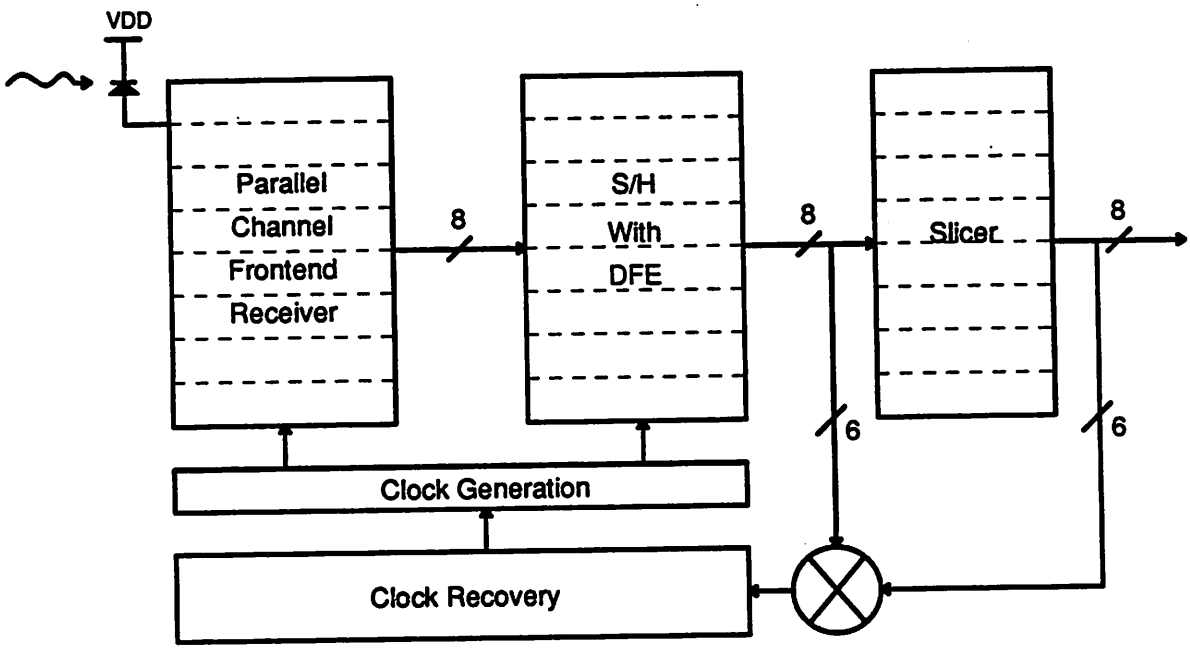

Figure 5.1 System block diagram of charge demultiplexing receiver

5.1. Parallel Front End Receiver

A conceptual picture of the front end receiver is show below in Fig. 5.2:

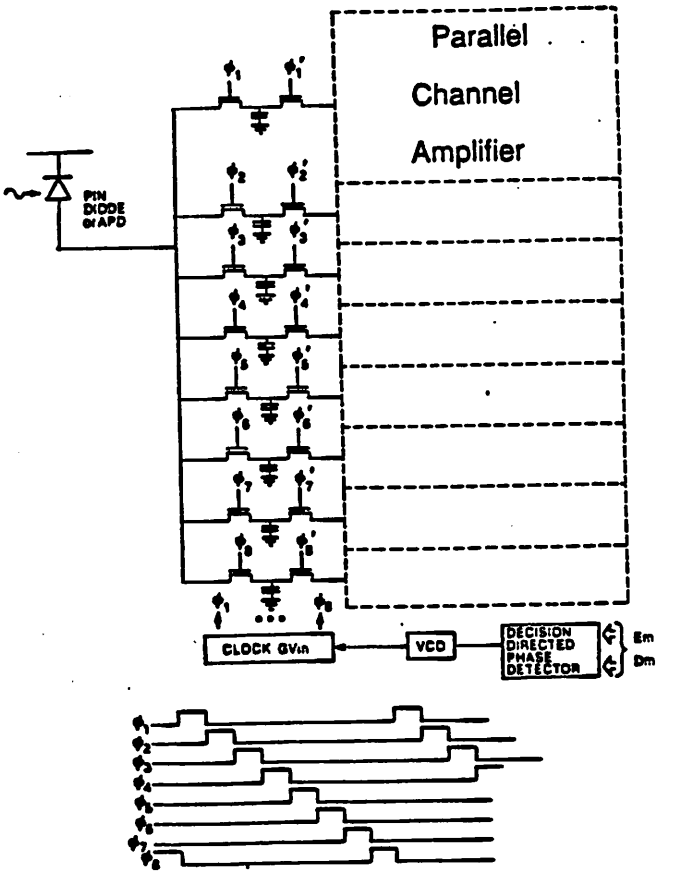

Figure 5.2 Conceptual picture of charge demultiplexing receiver

Instead of using one amplifier, a number of amplifiers are used (eight in this case). The photocurrent coming in as charge packets are demultiplexed into a number of lower-speed bit streams by carefully controlling the switches and sampling the charges on different sampling capacitors. The current to voltage conversion is done by integrating the charges on the sampling capacitors. This process is equivalent to doing eight integrate-and-dumps in parallel. The circuit is driven by an eight phase clock with each phase time equal to one bit period. When ϕ_1 is closed, the photocurrent is integrated onto the sampling capacitor and when it is done, ϕ_1 is opened and ϕ_1' is closed so that the parallel channel amplifier can process the data while at the same time, ϕ_2 is closed to sample another bit and so on. As a result, time for the parallel channel amplifier to process the data is much longer. Instead of one bit period, eight periods are available to the amplifier. † This scheme has several advantages. First, the parallel to serial conversion is done

† Actually only seven phases can be used cause one period is used to reset the sampling capacitor and the amplifier output which is not shown in here.

immediately at the front end. Secondly, the parallel channel amplifier now can have a much lower bandwidth than the incoming optical signal, which means that this approach can achieve a much higher data-rate with a technology with low frequency capability. The total noise bandwidth is also decreased and the noise due to the active components in each parallel channel amplifier is insignificant compared to the noise of the front end switches. The sensitivity is also larger because it is no longer limited by the thermal noise of the feedback resistor. Detailed calculation of the noise performance will be included in later section. The only circuit that runs at the bit rate is the internal clock circuitry that generates the controls to the switches.

This type of receiver also has its own problems. Since the photodetector itself has parasitic capacitance, not all the signal charges are sampled on the sampling capacitor. The residual charges on the diode capacitor are coupled into the next parallel stage resulting in intersymbol interference (ISI). One solution might be to increase the size of the sampling capacitor relative to the diode capacitor. However, this would result in a reduction of the signal voltage. As a result, the sampling capacitor cannot be made too large. Also, since the diode capacitance is unknown due to process variations, we cannot use any deterministic canceling scheme to offset the effect of the residual charges. An adaptive decision feedback equalization (DFE) scheme[13] is used to cancel the ISI, described in the next sub-section.

Another disadvantage is that the charge injection voltage of the switches is much larger than the signal voltage! The amplifiers itself also have their own input offset voltage and they are operating in the open loop mode without feedback. The voltage level of these two signals are in the 10 to 20 mV range while the minimum signal is only in the 1 or 2 mV range. A solution to this is to use a fully differential architecture for the front end. This cancels the offsets at the first order but they still exist because of process variations. Fortunately, these two offsets appear as a DC offset and can be eliminated using a DC-decoupling feedback to the amplifier to get rid of this DC offset. At the same time, if we choose the cutoff of the DC-decoupling feedback in the kHz range, we can also take care of the 1/f noise!

In order to achieve a wide dynamic range, another automatic gain control (AGC) feedback loop is included to prevent the amplifier from saturation when a large signal is input. A figure showing one parallel stage of the front end is shown in Fig. 5.3.

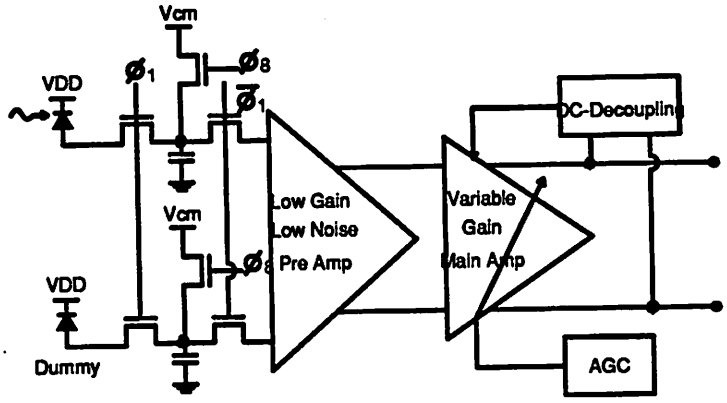

Figure 5.3 Simplified Channel Amplifier on the First Parallel Stage

5.2. Sampled and Hold with DFE and Slicer

After the front end has received and amplified the signals, they are sampled and held for the next block to do the DFE and slicing. By pipelining the received signal, another cycle which is equal to eight phases or eight bit periods is available to do the DFE and a broadband comparator is used for slicing. The output is delayed for 2 cycles which is 16 bit periods.

In order to implement a high-order DFE scheme, all pass symbol values are needed. This is impossible due to the time constrain on the circuits. Let the ratio between the diode capacitor C_d and the sampling capacitor C_s be r where $r = \frac{C_s}{C_d}$. If r is large, then for a signal at time k, the ISI due to signal at time k-2 is negligible. * Therefore only the signal at time k-1 is needed. Since the signals are sampled and held for eight consecutive bits, the desired feedback signal is already there. The feedback and slicing scheme is shown in Fig. 5.4.

* Calculations shown in the section of noise and ISI.

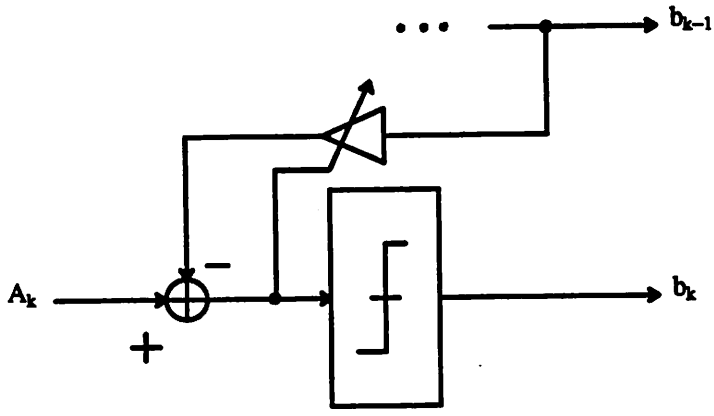

Figure 5.4 Adaptive Decision Feedback Equalization Scheme

5.3. Timing Recovering

This part is under research by another graduate student at Berkeley, Gregory Uehara. The input signal is an on-off signal with which the sampling capacitor is integrating the photocurrent. Because of the unique architecture of this receiver, the incoming analog waveform is integrated and demultiplexed into different channels. Traditional time recovering techniques at the baud rate cannot be used. We only have charges on the different capacitors from which to derive timing information. On the other hand, eight consecutive bits are available at once for detection. It is believed that a decision directed scheme based on FM modulation of the internal clock generator can be used to do bard rate timing recovering. Further details will be available in progress report written by Gregory at a later time.

6. Calculations for ISI and noise

For simplicity, a single-stage, single-ended architecture as shown in Fig. 6.1 is used for calculation. This can roughly tell whether the switching structure has sensitivity better or comparable to transimpedance preamplifier.

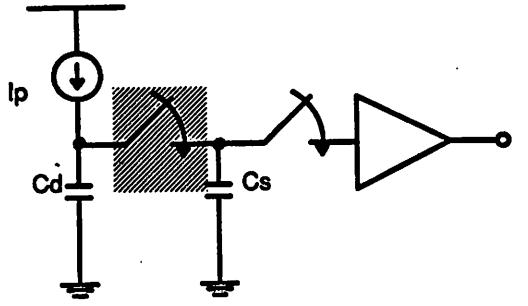

Figure 6.1 Major noise source from sampling switch

6.1. The symbols used are listed in Table 6.1.

C_d	Total capacitance on the Diode side
C_s	Total capacitance on the Sampling capacitor side
I_p	Equivalent photo current
Q_{sig}	Total charge of the signal in one bit period
R_{on}	On resister of the switch
V_d	Large signal voltage on C_d
V_{nd}	Noise coupled on C_d
V_{ns}	Noise coupled on C_s
V_s	Large signal voltage on C_s
$\Delta\tau$	One bit period

Table 6.1 Convention of symbols used

The basic assumptions for the calculations are that the noise due to the active component of the amplifier with its switch is negligible. This can be achieved in practise since the bandwidth is only 1/8 of the signal bandwidth and there are techniques to reduce the noise of an amplifier to a fairly low amount. Therefore the major noise source is the sampling switch.

$$Q_{sig} = I_p \times \Delta\tau \tag{6.1}$$

$$V_{sig} = \frac{Q_{sig}}{C_s} \tag{6.2}$$

$$C_s = r\, C_d \tag{6.3}$$

$$\sigma^2 = \frac{kT}{C_s} \tag{6.4}$$

6.2. Noise Voltages on C_s and C_d

The noise voltages coupled on C_d and C_s are different. This is because in the AC sense, the capacitors act as voltage dividers.

$$V_{ns} = \frac{V_{nr}\frac{1}{j\omega C_s}}{R_{on} + \frac{1}{j\omega C_s} + \frac{1}{j\omega C_d}}$$

$$= V_{nr}\frac{C_d}{C_d + C_s}\frac{1}{1 + j\omega R_{on}C}$$

where

$$C = \frac{C_s C_d}{C_d + C_s}$$

Therefore

$$\overline{V_{ns}^2} = \int_0^\infty \overline{V_{nr}^2}\left[\frac{C_d}{C_d + C_s}\right]^2 \left|\frac{1}{1 + j\omega R_{on}C}\right|^2 df$$

$$= 4kTR_{on}\left[\frac{C_d}{C_d + C_s}\right]^2 \frac{1}{4R_{on}C}$$

$$= \frac{kT}{C_s}\left[\frac{C_d}{C_d + C_s}\right] \tag{6.5}$$

Similarly

$$\overline{V_{nd}^2} = \frac{kT}{C_d}\left[\frac{C_s}{C_d + C_s}\right] \tag{6.6}$$

6.3. For time = 0

Initially, everything is uninitialized and is assumed to have zero voltage across every elements.

For large signal

$$V_s[0] = V_d[0] = \frac{Qsig[0]}{C_d + C_s} = V_{sig}[0]\left[\frac{C_s}{C_d + C_s}\right]$$

For the noise, it is as calculated in (6.5) and (6.6)

$$\overline{V_{ns}^2}[0] = \frac{kT}{C_s}\left[\frac{C_d}{C_d + C_s}\right] = \sigma^2\left[\frac{C_d}{C_d + C_s}\right]$$

$$\overline{V_{nd}^2}[0] = \frac{kT}{C_d}\left[\frac{C_s}{C_d + C_s}\right] = \sigma^2\frac{C_s^2}{(C_d + C_s)C_d}$$

6.4. For time = 1

Intersymbol Interference occurs and the noise of previous bit is also sampled and coupled into the next bit.

For large signal

$$V_s[1] = V_d[1] = V_{sig}[1]\left[\frac{C_s}{C_d + C_s}\right] + V_d[0]\left[\frac{C_d}{C_d + C_s}\right]$$

$$= \left[\frac{C_s}{C_d + C_s}\right]\left\{V_{sig}[1] + V_{sig}[0]\left[\frac{C_d}{C_d + C_s}\right]\right\}$$

For the noise, since the thermal noise of the switches at different time can be thought of as independent random Gaussian variables, the addition of the two are still Gaussian and the variance is the sum of the two individual variances.

$$\overline{V_{ns}^2}[1] = \sigma^2\left[\frac{C_d}{C_d + C_s}\right] + \overline{V_{nd}^2}[0]\left[\frac{C_d}{C_d + C_s}\right]^2$$

$$= \sigma^2\left[\frac{C_d}{C_d + C_s}\right] + \sigma^2\left[\frac{C_s}{C_d + C_s}\right]\left[\frac{C_s}{C_d}\right]\left[\frac{C_d}{C_d + C_s}\right]^2$$

$$\overline{V_{nd}^2}[1] = \sigma^2\left[\frac{C_s}{C_d}\right]\left[\frac{C_s}{C_d + C_s}\right] + \overline{V_{nd}^2}[0]\left[\frac{C_d}{C_d + C_s}\right]^2$$

$$= \sigma^2\left[\frac{C_s}{C_d}\right]\left[\frac{C_s}{C_d + C_s}\right]\left\{1 + \left[\frac{C_d}{C_d + C_s}\right]^2\right\}$$

6.5. For time = k

At any time k, k > 0 For large signal

$$V_s[k] = V_d[k] = \left[\frac{C_s}{C_d+C_s}\right]\left\{V_{sig}[k]+V_{sig}[k-1]\left[\frac{C_d}{C_d+C_s}\right]+V_{sig}[k-2]\left[\frac{C_d}{C_d+C_s}\right]^2\cdots+V_{sig}[0]\left[\frac{C_d}{C_d+C_s}\right]^n\right\} \qquad (6.8)$$

For the noise

$$\overline{V_{ns}^2}[k] = \sigma^2\left[\frac{C_d}{C_d+C_s}\right]+\sigma^2\left[\frac{C_s}{C_d+C_s}\right]\left[\frac{C_s}{C_d}\right]\left\{\left[\frac{C_d}{C_d+C_s}\right]^2+\left[\frac{C_d}{C_d+C_s}\right]^4+\cdots\left[\frac{C_d}{C_d+C_s}\right]^{2k}\right\}$$

for $k \to \infty$

$$\overline{V_{ns}^2}[k] = \sigma^2\left[\frac{C_d}{C_d+C_s}\right]+\sigma^2\left[\frac{C_s}{C_d+C_s}\right]\left[\frac{C_s}{C_d}\right]\left\{\left[\frac{C_d}{C_d+C_s}\right]^2\left[\frac{1}{1-\left[\frac{C_d}{C_d+C_s}\right]^2}\right]\right\}$$

$$= \sigma^2\left[\frac{C_d}{C_d+C_s}\right]\left\{1+\left[\frac{C_s}{C_d}\right]\left[\frac{C_d}{C_s+2C_d}\right]\right\}$$

$$= \frac{kT}{C_d}\left[\frac{2r+2}{r(1+r)(2+r)}\right]$$

From (6.8) the ISI is due to past symbols only and it is not a random function. Each coefficient is related to a ratio $\left[\frac{C_d}{C_d+C_s}\right]$ or $\frac{1}{1+r}$. If r is large, then the ISI due to signals at k-2, k-3, ..., is negligible.

Assuming the DFE is doing a perfect job without noise enhancement. The ISI consists of past symbols only, and therefore can be completely canceled by th DFE.

$$SNR = \frac{V_s^2}{\overline{V_{ns}^2}} = \frac{Q_{sig}^2}{kT}\left[\frac{1}{C_d}\right]\left[\frac{1}{2}\,\frac{r(r+2)}{(1+r)^2}\right]$$

For sufficiently large r.†

$$SNR \approx \frac{1}{2}\,\frac{Q_{sig}^2}{kT}\left[\frac{1}{C_d}\right] \qquad (6.7)$$

† Large means any integer larger than 3

6.6. Computer Simulations

For computer simulation, V_{sig} is normalized to 1, therefore the SNR can be expressed as .

$$SNR \approx \frac{1}{2}\frac{Q_{sig}^2}{kT}\left[\frac{1}{C_d}\right] = \frac{1}{2}\frac{r}{\sigma^2} \tag{6.9}$$

The relationship of SNR and probability of error P_e assuming the noise is Gaussian is as follows:

$$P_e = Q\left[\frac{V_s}{2\sigma}\right] = Q\left[\frac{\sqrt{SNR}}{2}\right]$$

Assuming 1 and 0 are equally likely and $Q(\cdot)$ is the area under the tail of a random Gaussian distribution.

With r = 10, 10^6 inputs are simulated for different SNR and the corresponding P_e is shown in table 6.2 below.

σ	SNR (dB)	P_e (Theory)	P_e (Simulation)	
			r = 10	r = 5
0.87	8.2	10^{-1}	0.88×10^{-1}	1.72×10^{-1}
0.48	13.3	10^{-2}	0.82×10^{-2}	4.74×10^{-2}
0.36	15.8	10^{-3}	1.03×10^{-3}	14.17×10^{-3}
0.30	17.4	10^{-4}	0.88×10^{-4}	46.30×10^{-4}
0.26	18.6	10^{-5}	0.70×10^{-5}	140.8×10^{-5}

Table 6.2 Simulation results compared with theory

The results agree with theoretical calculations when r = 10, which must be the case since model used to develop the theory is used in the simulation. The results are worse for r = 5 because of the error propagation of the DFE without canceling the ISI completely.

6.7. Summary

A receiver of this type is very promising in achieving a much higher sensitivity and speed than other architectures with the same technology. An interesting result is that instead of being limited by the thermal noise of the feedback resistor, the SNR is increased with decreasing C_d. Of course eventually this approach is limited by the noise of the amplifier. With a C_d of 1pF, a sensitivity of -43dBm is achievable. This is already 10 dB better than any other existing architectures.

7. Current Status and Future Work

7.1. Current Status

The survey of existing architectures, especially the noise and speed tradeoffs of the transimpedance preamplifier shows that there are fundermental limits for applying CMOS to build optical receiver in the 100Mb/s range. Therefore, a new architecture is required to apply CMOS to high speed, low cost, and highly integrated front end receivers suitable for LAN applications.

A new charge demultiplexing receiver is proposed to solved the speed limit. While solving the speed problem, there are many new problems which results from this new approach. The ISI due to residual charge is an issue as well as the sensitivity of the new architecture. Timing recovery is a another big problem.

Currently, a high level system block diagram has been set up. The adaptive DFE is proposed to solve the ISI problem. The noise performance has been analyzed, and it is expected to be better than any existing CMOS receivers and is comparable to the optical receivers built with GaAs components. This is a little optimistic because only single channel is used for the calculation. More refined model for multiple parallel stages is under investigation. High level simulations of the convergence of the DFE and the AGC loop together with noise of the switches has been performed. The results agrees with the calculated results. A new timing recovery scheme has also been developed utilizing the fact that eight bits are available at a time. A high level simulation also shows that this scheme does converge for phase detection with a minimal amount of jitter.

7.2. Future Work

There are still several system problems remained to be solved. What is the optimal ratio between C_s and C_d or r? If r is 10 then the ISI error is only 1% and the SNR is closer to the approximation. But on the other hand, the signal attenuation is large in terms of voltage because $V_{sig} = \frac{Q_{sig}}{(C_d+C_s)}$. and as a result noise of the amplifier may no longer be negligible. Using too small a r like 5 gives an error due to ISI of about 10% because only the previous signal is feeding back for the DFE. This degrades the sensitivity significantly, especially at high SNR and low BER because now the noise from ISI dominants. The effect is highly non-linear and hand analysis is difficult. Simulation will be used to find this value. Another

solution of the problem is to feed more than one bit back, which complicates the DFE scheme. A low noise front end preamplifier and a variable gain amplifier will be designed and a circuit level simulation will be done on the parallel channels.

The timing recovery scheme is being pursued by Gregory Uehara. He is currently looking into the structure of a ring oscillator to implement the FM modulated internal clock for the recovery scheme.

The circuit level design is expected to be completed in July and layout is expected to be done by August. After that the chip is going to be sent out for fabrication. The first prototype is designed using a well characterized 3μm process and is expected to run at 50Mb/s. Scaling will then be used to push the performance once the scheme has proven to be practical.

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