HIGH-FREQUENCY, TEMPERATURE-COMPENSATED MONOLITHIC VOLTAGE-CONTROLLED OSCILLATOR DESIGN TECHNIQUES

by

Ting-Ping Liu

Memorandum No. UCB/ERL M88/33

23 May 1988

HIGH-PRODUCTION, TEMPERATURE-COMPENSATED MONOLITHIC VOLTAGE-CONTROLLED OSCILLATOR DESIGN TECHNIQUES

by

Ting-Ping Liu

Memorandum No. UCB/ERL M89/7

23 May 1989

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

HIGH-FREQUENCY, TEMPERATURE-COMPENSATED MONOLITHIC VOLTAGE-CONTROLLED OSCILLATOR DESIGN TECHNIQUES

by

Ting-Ping Liu

Memorandum No. UCB/ERL M88/33

23 May 1988

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

HIGH-FREQUENCY, TEMPERATURE-COMPENSATED MONOLITHIC VOLTAGE-CONTROLLED OSCILLATOR DESIGN TECHNIQUES

by

Ting-Ping Liu

Memorandum No. UCB/ERL M88/33

23 May 1988

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

High-Frequency, Temperature-Compensated Monolithic Voltage-Controlled Oscillator Design Techniques

Ph.D. Ting-Ping Liu Department of EECS

Robert G Meyer

Chairman of Committee

Abstract

This research explores new voltage-controlled oscillator (VCO) architectures and circuit design techniques to optimize VCO performance at frequencies above 100 MHz. Through the use of negative feedback loops around a core VCO and matched linear frequency-to-voltage converters (FVC), the VCO oscillation frequency is stabilized against temperature, power supply and processing variations, while maintaining a linear voltage-to-frequency control characteristic.

To verify the feasibility of the proposed VCO architecture, an emitter-coupled VCO with dual-loop feedback has been designed and fabricated in a 2-μm oxide-isolated bipolar technology. The VCO, consuming 220 mW from a single 5-V supply and occupying 2,200 $mils^2$, achieves -65 ppm/°C TC of frequency over 20 to 80°C at center frequency 200 MHz. It has a 5:1 frequency control range and the maximum oscillation frequency is 250 MHz with better than 2% voltage-to-frequency linearity. The modulation bandwidth of the VCO is greater than 12 MHz and power supply rejection ratio is 0.4%/V.

Although the closed-loop architecture was applied to implement the high frequency emitter-coupled oscillator in bipolar technology to demonstrate the validity of theory, it is also of potential interest for other VCO configurations and technologies.

Acknowledgements

I wish to express my sincere gratitude to my research advisor, Professor Robert G.Meyer, for his constant guidance and support throughout the course of this Ph.D. dissertation work. I would also like to thank the linear division of Signetics Corporation and William Mack for fabricating the prototype VCOs and providing the die photography.

I am indebted to many of the fellow graduate students in the integrated circuits group, my colleague Mehmet Soyuer in particular, for their useful discussions and assistance.

The financial support provided by the Ministry of Education of the Republic of China for my first two year graduate study at Berkeley is acknowledged.

Last but not least, I would like to express my deep appreciation to my wife, Li-ping, and my parents for their love, understanding and patience through all these years.

This research was sponsored by U.S. ARO under Grant DAAL03-87-K-0079.

Table of Contents

CHAPTER 1

INTRODUCTION

1.1. Motivation

The function of a voltage-controlled oscillator (VCO) is to generate a stable and periodic waveform whose frequency can be varied by an applied control voltage. The relationship between the control voltage and the oscillation frequency depends upon the circuit architecture and topology, although a linear characteristic is generally preferred because of its wider applications and versatility. The basic concept of the VCO evolved from the cross-coupled trigger circuit as early as in the 1920's,[1] and since then tremendous efforts have been devoted to both the theory of oscillators and practical circuit realizations. With the advent of monolithic integration and resulting higher integration level, monolithic VCO's are widely used in communication systems, analog circuits, and complex digital systems. In order to function properly under adverse environments, the frequency stability with temperature is one of the most important performance requirements for a VCO. As the technology continues to progress to increase the circuit operating speed and thus the system performance, it becomes necessary to investigate new VCO architectures capable of operating at high speeds and still meeting the same temperature stability specification which conventional VCO's have accomplished at low frequency.

This research is aimed at identifying the sources of VCO frequency drift with temperature at high frequency, propose circuit solutions, and verify the feasibility through prototype circuits. As a test vehicle, a 250 MHz monolithic VCO was designed and fabricated in a 2-μm silicon bipolar technology to demonstrate the feasibility of the proposed circuit approaches. In addition to a small frequency drift with temperature, the frequency-to-voltage linearity of the VCO is better than 2% over a 50-250 MHz range as a result of the use of the matched linear frequency-to-voltage converters and the feedback loops for correcting the temperature drift. Although the prototype circuit is designed in bipolar technology to exploit the high frequency capability of the relaxation oscillator, the design techniques can be adopted for other technologies and VCO configurations as well.

1.2. Thesis Organization

Chapter 2 reviews the characterization, and applications of monolithic VCO's to provide the background needed in the design of electronic circuits for applications in frequency demodulation, signal generation, timing recovery, and so on. Two basic types of VCO, harmonic and relaxation, are also reviewed and compared from the point of view of monolithic IC design. Their advantages and limitations for high frequency applications are addressed as well. Chapter 3 describes the proposed new VCO architecture and theoretically analyzes its performance in terms of temperature stability, linearity, and frequency accuracy. The design and implementation of a prototype monolithic VCO based on the architecture in Chapter 3 are given in Chapter 4, followed by the experimental results which are examined and discussed in Chapter 5. Chapter 6 is concluded with the research summary and future topics.

CHAPTER 2

MONOLITHIC VOLTAGE-CONTROLLED OSCILLATORS

2.1. Introduction

Aside from amplifiers, oscillators are probably the most commonly used analog electronic circuits, by virtue of communication system applications. An extra dimension is added to oscillators when their oscillation frequencies can be varied, in an electronic manner, by a control voltage. The introduction of the frequency control, coupled with the invention of negative feedback, makes the voltage-controlled oscillator (VCO) a versatile and important building block in a variety of applications.

In this chapter an overview of monolithic VCO's is devoted to constitute a foundation for the discussions in the subsequent chapters. Applications and characterization for VCO's are presented in first two sections, followed by the description of various VCO configurations, and their performance. In the last section, the advantages and limitations in high frequency applications for VCO's are compared from the viewpoint of monolithic integrated circuit design.

2.2. Applications

Based on the functionality, VCO applications fall into two categories: (1) data transmission and signal generation, and (2) detection and frequency synthesis. In transmitters and signal generators, the VCO, along with other circuitry, generates periodic signals according to the input information, such as in FSK modulation, voltage-frequency conversion, and function generation. On the other hand, for applications in detection and frequency synthesis, more complicated systems, for example phase-locked loops (PLL), are involved to extract the desired information from the received signals, such as in FM demodulation, timing recovery, frequency synthesis, and coherent amplitude demodulation.

2.2.1. FSK Modulation

Frequency-shift keying (FSK) is a method commonly used in transmission of digital signals through voice-grade channels such as telephone lines. In this application, the digital information is

transmitted by switching the VCO frequency between two discrete frequencies f_1 and f_2, determined by the state of digital input, as shown in Figure 2.1.

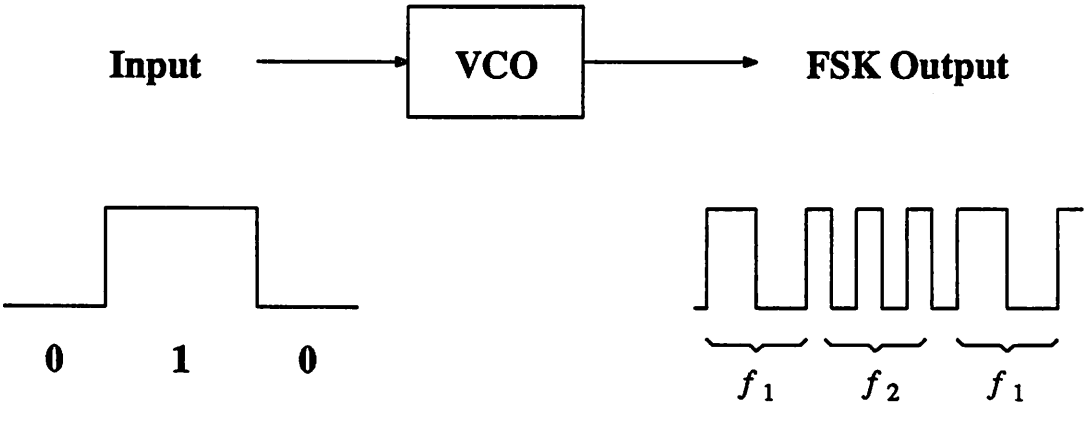


Figure 2.1 - VCO as FSK modulator

It is important to note that in FSK modulation the VCO output frequency should have fast response time to the input voltage change, while the linearity of its frequency-voltage control characteristic is not important due to the digital nature of the information.

2.2.2. Voltage-Frequency Conversion

There are many instances when it is necessary to convert an analog voltage to a frequency, which is then applied to a counter to obtain a digital output. The key performance requirement of such a function is the linearity of the VCO frequency with respect to the input voltage. An analog-to-digital converter using a VCO as voltage-frequency converter is illustrated in Figure 2.2. The analog signal V_{in} is first converted to a frequency, and is then counted by a binary counter to form a digital output. This particular technique is suited for transmitting analog data over fiber-optic links with a frequency counter located at the receiving end of the channel.

2.2.3. Function Generation

A function generator, consisting of a VCO, wave shaping circuitry, and an analog multiplier offers various output waveforms whose amplitude and frequency can be modulated by external signals. Figure

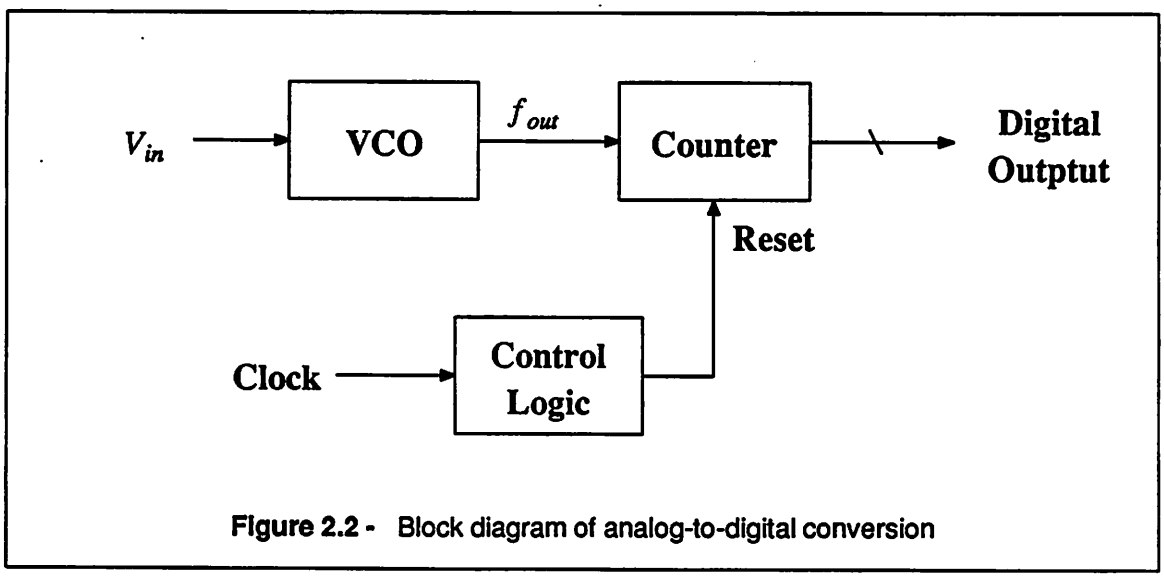


Figure 2.2 - Block diagram of analog-to-digital conversion

2.3 shows the block diagram of the function generator. In these applications, the relaxation oscillator is preferred because of its capability to generate both square waveforms, and triangular waveforms from which sine waveforms can be derived using shaping circuitry before they are modulated in amplitude by the modulating signals through the analog multiplier.

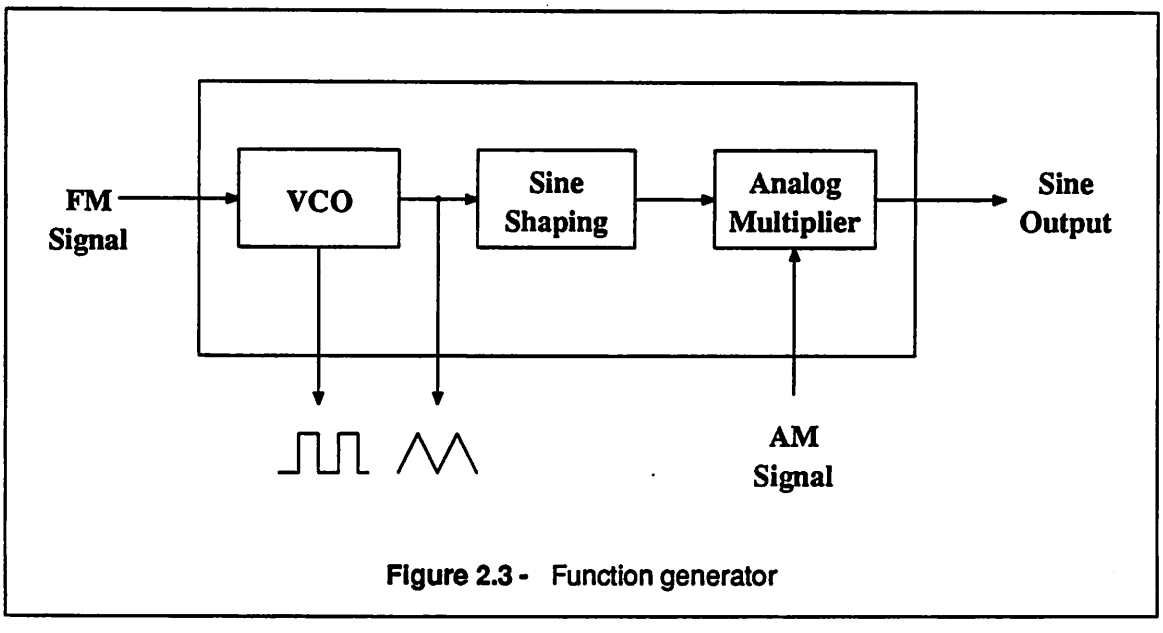


Figure 2.3 - Function generator

2.2.4. FM Demodulation

FM signals can be demodulated by using a PLL comprised of a phase detector, a low-pass filter, a gain stage, and a VCO, as shown in Figure 2.4. When the PLL is locked on the FM signal, the VCO

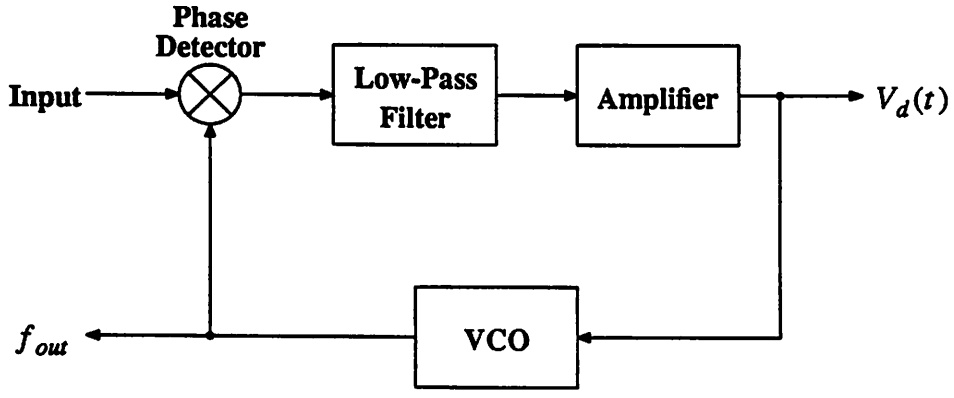


Figure 2.4 - Block diagram of PLL

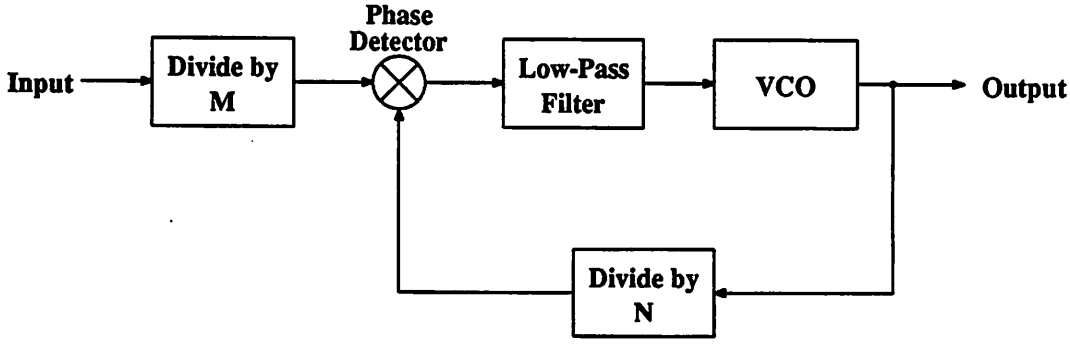
frequency follows the instantaneous frequency deviation of the input. Thus the voltage $V_d(t)$ at the input of the VCO corresponds to the demodulated output. In this case, the linearity of the VCO voltage-to-frequency characteristic is important since it determines the linearity of the PLL, and therefore the harmonic distortion of the demodulated output.

2.2.5. Timing Recovery

In digital transmission systems the key issue in the demodulation/detection process is to establish the bit synchronization - the optimum sampling clock for the matched-filtered demodulated baseband signal. A timing recovery circuitry to extract the clock embedded in the data and noise is basically a form of PLL as shown in Figure 2.4. The recovered clock f_{out}, however, is available at the output of the VCO. Therefore, in contrast to FM demodulation, a VCO with a linear frequency-voltage characteristic is not needed in timing recovery, as long as frequency acquisition is assured.

2.2.6. Frequency Synthesis

Frequency multiplication and/or division can be performed using a PLL in conjunction with divider elements as shown in Figure 2.5.



$$f_{out} = \frac{N}{M} f_{in}$$

Figure 2.5 - Simplified frequency synthesizer using PLL

By programming the divider modulus M and N, one can obtain a noninteger relationship between input and output frequencies. This operation, combined with frequency translation through mixers, can form programmable frequency synthesizers for spectrally pure signal generation and for signal tracking and processing, which are very widely used in transmitters, receivers, and transponders, as well as in laboratory instrumentation.

2.2.7. Coherent Amplitude Demodulation

Amplitude modulation can be detected coherently by using a coherent amplitude detector driven from the VCO output as illustrated in Figure 2.6. After the PLL locks on the carrier of the AM signal, the VCO has the same frequency as the AM carrier. The demodulated AM signal is obtained at the output filter by low-pass filtering the AM signal multiplied by the coherent reference signal at the quadrature

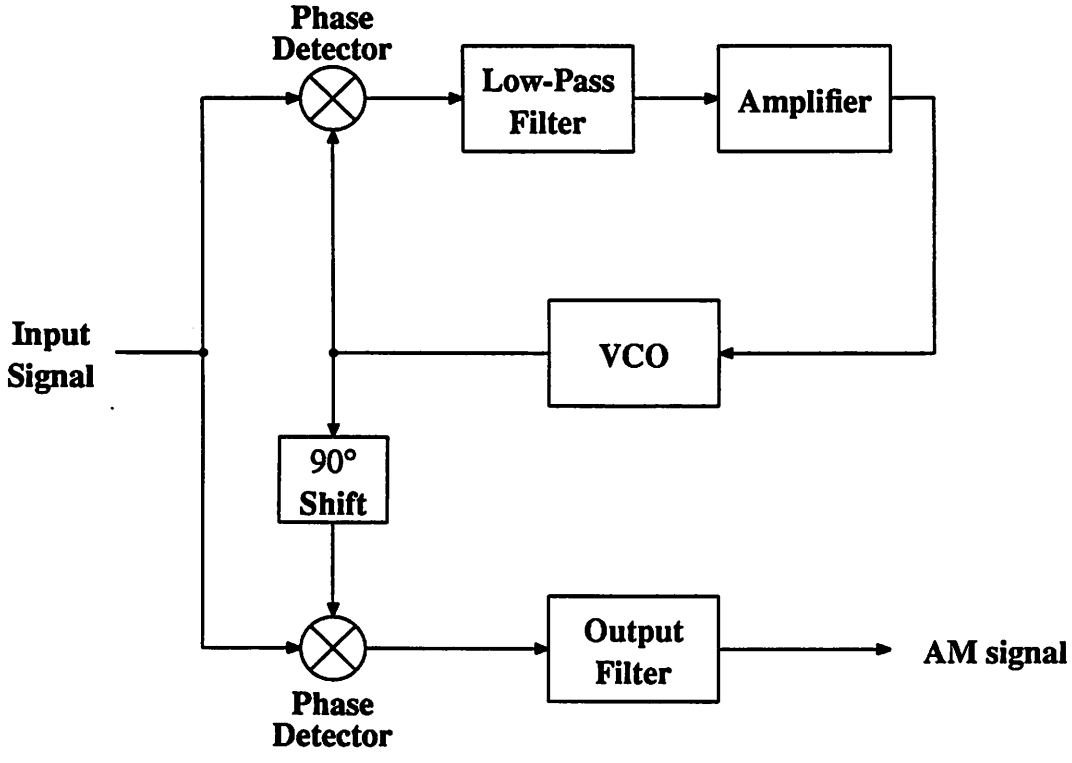


Figure 2.6 - Coherent AM detection

output of the VCO. The output can also be used in the generation of automatic gain control (AGC) or lock indication in applications such as IF receives with coherent AGC, and stereo decoder circuits.[2]

2.3. Characterization

In this section, the characterization of VCO's is presented. The VCO characteristics are strongly dependent on the VCO configurations, which will be described in the next section. Unfortunately, no particular VCO configuration prevails in every category since some requirements are in conflict with one another, and therefore, depending on the applications, a trade-off is necessary to favor some area while inevitably sacrificing others.

2.3.1. Frequency Stability

This is one of the most important requirements and, based on the frequency deviation rate, can be further divided into two parts: (1) long term stability, such as stability with temperature and power supply, and (2) short term stability, also characterized as phase noise.

2.3.1.1. Stability with Temperature

The oscillation frequency tends to drift as the environmental temperature changes, and this is most conveniently expressed in terms of the fractional change in oscillation frequency per degree centigrade of temperature variation, which is termed temperature coefficient of frequency, TC, with a unit of ppm/°C.

$$TC \equiv \frac{1}{f_{osc}} \frac{\partial f_{osc}}{\partial T} \tag{2.1}$$

Despite several published designs have been successful in stabilizing TC of frequency,[3,4] the usable frequency range is still limited to few tens of MHz, which is about a decade lower than the maximum operating frequency that typical monolithic VCO's can offer. As a result, to achieve a low TC at high frequencies is very important and will be detailed in the next chapter.

2.3.1.2. Stability with Power Supply

Usually this is measured as the frequency change in percentage per volt when power supply is varied. The variation of frequency is caused by the change in the parameters of active devices, such as gain, output impedance, reference level of detector, and parasitics. The requirement for the stability with power supply varies in different applications, but a useful rule of thumb for PLL applications is to keep it less than the ratio of the detection band to the center frequency of the VCO.

2.3.1.3. Phase Noise

Sometimes this is also called jitter. Due to the internal noise in the circuits modulating the zero-crossing or the thresholds of switching level, the period of oscillation tends to vary from cycle to cycle. The presence of the phase noise in the VCO imposes the ultimate limits on the resolution which a PLL can achieve. Narrowband detection PLL applications, such as timing recovery, require a low phase noise

VCO. The phase jitter, usually specified in parts per million (ppm), can be minimized by means of either reducing the noise bandwidth of the VCO, or by increasing the voltage swing across the timing capacitor used in the relaxation oscillator.[5]

2.3.2. Voltage-to-Frequency Characteristic

There are two important parameters in the voltage-to-frequency characteristic of the VCO; linearity and conversion gain. Strictly speaking, these parameters are functions of the frequency of applied control voltage. However, characterization is normally specified for slow changes since the oscillation frequency responds rapidly to control voltage in most cases.

2.3.2.1. Linearity

In order to achieve maximum versatility, a VCO with linear frequency-voltage characteristic is generally required. This directly determines the linearity of the demodulated output of PLL in the application of frequency demodulation. Any nonlinearity of the VCO characteristics will be reflected as distortion in the demodulated output. While nonlinearities caused by mismatch and finite output impedance can be minimized at low frequencies by proper circuit design, the nonlinearities at high frequencies are much more difficult to correct since switching delay is the main contributor of errors and it is very difficult to model the switching mechanism at high frequencies. One way to overcome this problem is to employ the feedback approach that will be described in the next chapter.

2.3.2.2. Conversion Gain

Conversion gain (K_v) is the slope of frequency-voltage characteristics if they are near-linear, or their derivative evaluated at the free-running frequency of the VCO if they are nonlinear. In PLL applications, K_v is made as large as possible to increase the dc loop gain, and thereby minimize the phase error between the input signal and VCO output. On the other hand, K_v is kept relatively low in order to reduce the VCO drift due to the offset drift of the phase detector output or the loop amplifier.[6] As a result, a compromise is needed for choosing K_v.

2.3.3. High Frequency Capability

High-speed data transmission and full utilization of bandwidth result in a demand for electronic circuits operating at high frequencies. The VCO is no exception. Higher operating frequencies allow wider applications, and in PLL applications the VCO is the typical limiting factor for high frequency operation because other components, both phase detector and gain stage, are high-speed ECL-type switching circuits. To minimize switching delays occurred in the circuits, the use of all-*npn* transistors with high unity gain frequency f_T allows VCO's capable of operating at up to several hundred MHz.[7,8] The inherent limitations on the high frequency capability of a VCO will be discussed later in this chapter.

2.3.4. Dynamic Range of Frequency Control

This is defined as, for given frequency-determining component(s), the ratio of the maximum frequency to the minimum frequency that can be obtained when varying the control voltage between two extremes. It ranges from few tenth of percent higher than unity, as in the case of crystal oscillators, to more than four decades, as in the case of relaxation oscillator. As in the case of high linearity and large conversion gain, the requirements for wide tuning range of frequency are in direct opposition to the requirements for frequency stability. In other words, the more stable the frequency, the more reluctant its change. Accuracy control of the frequency, to be described below, is related to frequency stability in the similar way.

2.3.5. Frequency Accuracy

In most cases, the VCO frequency is set by the external components. It is desirable that the frequency can be accurately governed by the external component setting with a minimum number of components. Frequency accuracy is practically limited by the on-chip component matching and process variations from lot to lot. At low frequencies, a typical accuracy of frequency that can be achieved without trimming is ±1%. However, this deteriorates rapidly at high frequencies as the parasitic capacitance or inductance are no longer negligible compared with external frequency-determining components. Frequency accuracy is particularly important in a PLL system with a narrow detection band. For example, if

a VCO is to be included in a narrow detection band PLL (for instance ±1% of center frequency) the frequency accuracy requirement for the VCO should be at least 1% to assure the loop can lock on the input signal during the capture process. In other words, a VCO may not be suitable at high frequencies simply because of the inaccuracy, even if it is capable of operating at high frequencies.

2.4. VCO Configurations

As a general classification, VCO's can be loosely categorized into two types, characterized by their output waveform: (i) Harmonic oscillators which generate nearly sinusoidal outputs, and (ii) relaxation oscillators which provide square or triangle outputs as circuits switch alternatively between two well-defined astable states.

2.4.1. Harmonic Oscillators

In general, a harmonic oscillator is composed of an amplifier, which provides adequate gain, and a frequency-selective network, which feeds the output within a certain frequency range back to the input. The oscillation frequency and amplitude can be determined by the two conditions required for a sustaining, stable oscillation. Two different approaches, negative resistance and feedback, are used to analyze the oscillators. Although the negative resistance approach can be used to analyse the oscillation condition for harmonic oscillators as well, the feedback approach is chosen here for the sake of simplicity. Fig 2.7 shows a generalized block diagram of a harmonic oscillator.

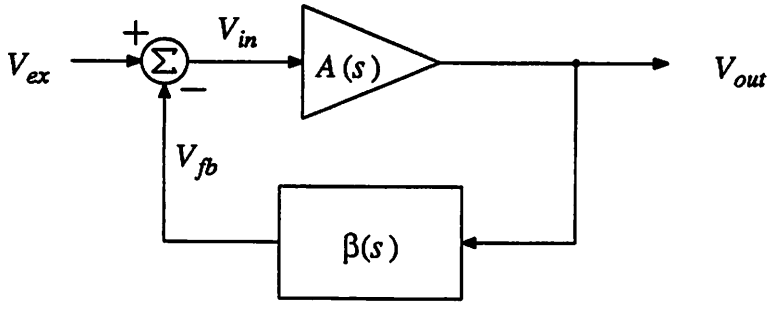


Figure 2.7 - Block diagram of harmonic oscillator

To ensure the oscillation, the amplifier A must supply enough energy to compensate the loss in the passive elements, while the feedback (frequency selective) network shifting the phase of the output signal an amount such that it is in phase with the input signal. Quantitatively, oscillations can take place and be sustained if the following conditions, the so-called the Barkhausen criteria,[9] are satisfied:

$$\left|\frac{V_{fb}}{V_{in}}\right| = \left|A(s)\right|\left|\beta(s)\right| \geq 1 \tag{2.2}$$

and

$$arg\left(\frac{V_{fb}}{V_{in}}\right) = \Phi_A + \Phi_\beta = 0 \tag{2.3}$$

where Φ_A and Φ_β are the phase shifts for the amplifier and feedback network, respectively. Note that the above equations are derived in the absence of external excitation, i.e., $V_{ex} = 0$. Interestingly, oscillators are the only circuits which can generate output signals without any input signal being applied. The presence of noise is accounted for in the start of the oscillation, which proceeds to build up if the initial loop gain is greater than unity. As the oscillation grows, the gain A of the amplifier, and thus the loop gain, eventually decreases because the circuit enters the nonlinear region of the amplifier. Eventually, a steady state is reached with such an amplitude and frequency that Equations (2.2) with equal sign and (2.3) are satisfied *simultaneously* . The actual time elapsed between the start-up of the oscillation and circuits reaching an equilibrium depends on many factors, such as initial loop gain, and the quality factor Q of the feedback network.

Fortunately, for most practical oscillators, it is possible to find the steady state amplitude and frequency by solving Equations (2.2) and (2.3) *independently* . In particular, if feedback network has a sharp roll-off phase-frequency characteristic, the frequency can be determined solely by equation (2.3) and then substituted into equation (2.2) to obtain the oscillation amplitude. In other words, the oscillation frequency can be approximated by knowing how much phase shift (0 or 180° depending on the polarity of the amplifier gain A) must be provided by the tank circuit with a high Q, while the amplitude of oscillation is determined by the limiting characteristics of the loop.

We now turn attention to the implementation of most commonly used practical harmonic oscillators in monolithic IC: LC oscillators and crystal oscillators.

2.4.1.1. LC Oscillators

An LC-tank circuit is used as feedback network and frequency determining component in an LC oscillator, which can easily operate at frequencies up to several hundred MHz. There are many variations of LC oscillators, which are discussed elsewhere,[10,11,12] therefore, without the loss of generality, a typical circuit implementation is shown in Figure 2.8 to illustrate the high frequency capability and the means of frequency tuning for this type oscillator.

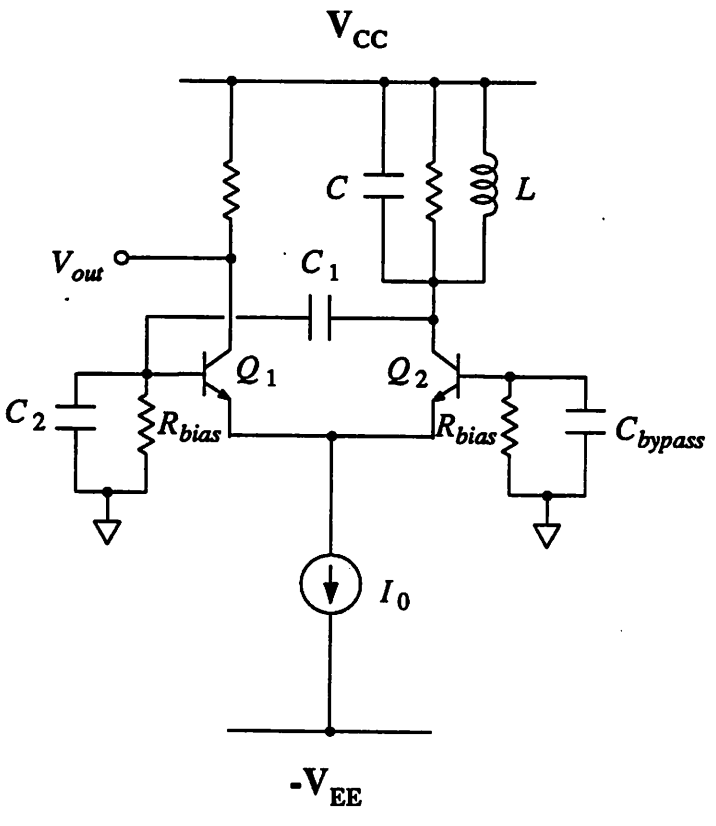


Figure 2.8 - Positive feedback Colpitts L-C oscillator

Since the only tuning component external to the chip is the inductor L, this circuit is particularly attractive to monolithic integration. The capacitor C and external L are the primary LC tank circuit

elements while other capacitors C_1 and C_2 constitute a capacitive transformer, which provides much more efficient feedback at high frequencies than a coiled transformer. Differential pair Q_1-Q_2 is used as the active element to give a positive gain with wide bandwidth from the base of Q_1 to the collector of Q_2. There are two advantages using differential pair as the gain stage. First, output V_{out} can be taken from the collector of Q_1 which is isolated from the tank circuit, and thus loading from output has no effect on the oscillation frequency. Second, the total harmonic distortion is less than with single transistor oscillators since all the even harmonics are absent due to the symmetric topology of the differential pair.[13]

Assuming that the loading effects and parasitics are negligible, the oscillator has a frequency of oscillation given by

$$f_{osc} = \frac{1}{2\pi\sqrt{L\left[C+\frac{C_1C_2}{C_1+C_2}\right]}} \tag{2.4}$$

It is clear that for a high Q tank circuit, the stability of the oscillation frequency is directly related to that of reactive elements L and C's, and is insensitive to the characteristics of active devices and the power supply drift. As a result, a stable oscillation frequency with temperature and power supply is obtained by the LC oscillator, provided that L and C's are stable. In addition, due to the narrow bandwidth of high Q tank circuit, the LC oscillator has a much lower phase jitter at the output than a relaxation oscillator.[14]

The range of oscillation frequency can be determined by examining (2.2). If the parasitics are neglected, the maximum operating frequency is limited by the bandwidth of the amplifier since oscillation would be stopped at some frequency where the amplifier can no longer supply enough gain to maintain the oscillations, as required in (2.2). In practice, the highest oscillation frequency is, however, limited by the inevitable parasitic capacitance and inductance from package, bonding wires, and active devices. For instance, if L_{effect}= 3 nH and C_{effect}= 5 pF, the corresponding upper frequency limit is 1.3 GHz. The minimum oscillation frequency is set by the feedback capacitive divider C_1-C_2 since at lower frequencies, the feedback quantity $\beta(s)$ is less than as required in (2.2) due to the loading from R_{bias} and Q_1, which are negligible at high frequencies. The lower frequency limit is typically in the order of few MHz.

The oscillation frequency can be varied by changing the value of either inductor or capacitor. Although inductors have been successfully fabricated in monolithic integrated circuits using GaAs technology,[15] yet they are not ready with current silicon technology to achieve similar performance, and that leaves only the possibility of the using the variable-reactance (varactor) diode to attain voltage control of the frequency of oscillation. In the varactor-tuned VCO, the capacitor C of the LC tank circuit is implemented by a reverse-biased junction capacitor whose value can be changed by varying the reverse bias voltage across it through the input control voltage V_{in}, as shown in Figure 2.9.

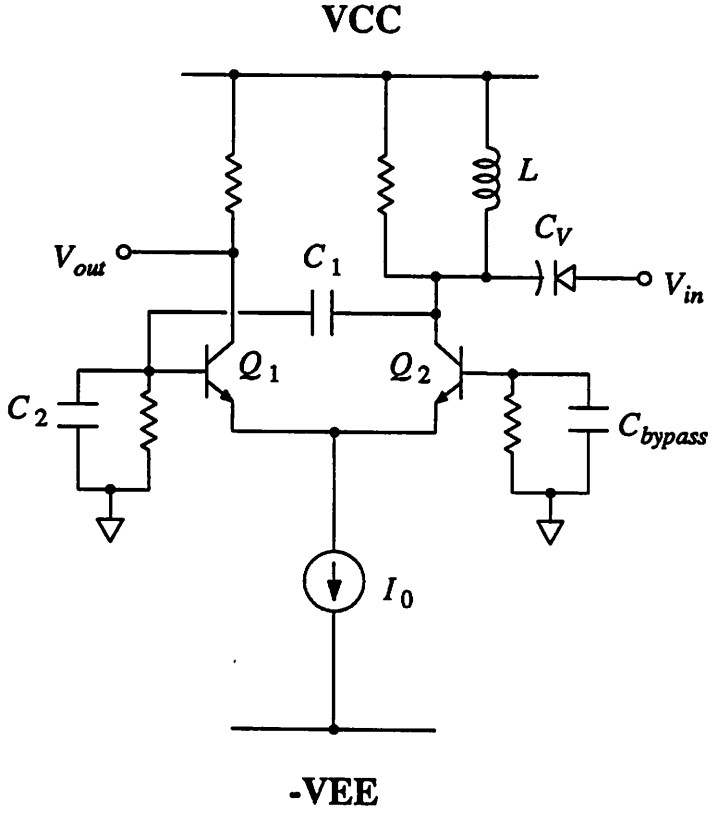


Figure 2.9 - Varactor-tuned VCO

From Eq (2.4) the oscillation frequency of the varactor-tuned VCO can be expressed as

$$f_{osc} = \frac{1}{2\pi\sqrt{L\left[C_0\left[\frac{V_{CC}-V_{in}}{\phi_i}\right]^{-m} + \frac{C_1C_2}{C_1+C_2}\right]}} \tag{2.5}$$

where C_0 is the zero-bias junction capacitance for the varactor, m is a constant between 0.3 and 0.5, depending on the doping profile of the junction, and ϕ_i is the built-in potential. By changing the input control voltage V_{in}, f_{osc} can be tuned accordingly in a *nonlinear* fashion by an amount of few percent of variations because it is a weak function of V_{in}, as seen in (2.5). These drawbacks, limited tuning range of the frequency and the nonlinear frequency-voltage control characteristics, exclude the varactor-tuned VCO from some applications, such as FM demodulation. Also careful design and accurate modeling of the varactor diode is required to realize good frequency stability with temperature.

In summary, the LC oscillator is capable of operating at high frequencies, and limited frequency tuning can be achieved by using a varactor diode at the expense of inferior temperature stability. The trade-off between stability and tuning range can be made by using voltage-controlled crystal oscillator. This will be described in the next section.

2.4.1.2. Crystal Oscillators

The stable electromechanical resonance characteristics of a quartz crystal is used to set the oscillation frequency for crystal oscillators. The reason why one employs a piezoelectric resonator in place of a conventional LC tank circuit described in the previous section is that the available Q in these mechanical vibration devices, when driven by sinusoidal voltages, may be up to thousand times greater than that available with conventional elements. As a result, crystal oscillators are the most stable of electronic oscillators and are always used for for such critical applications as frequency synthesizers or clock synchronizers.

Figure 2.10 illustrates the symbol for a crystal and equivalent circuit for a single mode if other modes are assumed operating far from resonance. Typically, the reactances associated with L and C are much higher than R_s, leading to an extremely high Q with values being several thousand to few million. One of the most commonly used crystal oscillators is the Pierce oscillator, shown in Figure 2.11. The

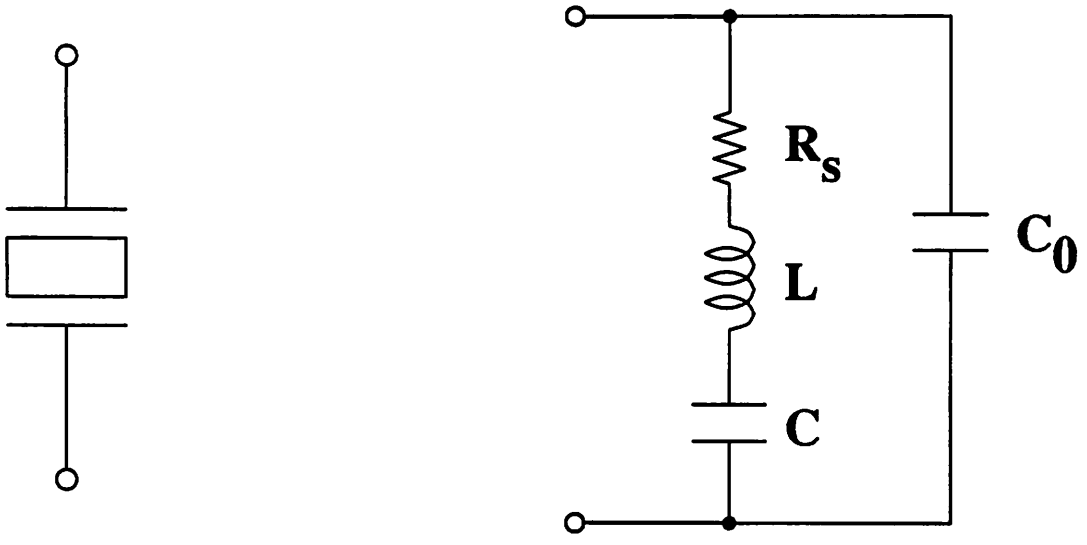


Figure 2.10 - Crystal and equivalent circuit

crystal is operated as an inductance, and capacitors C_1 and C_2 adjust the amount of feedback while the inverter, which is biased at the midpoint of the transfer curve through the large bias resistor R_{bias} to provide sufficient gain, does not significantly load the crystal to degrade the overall Q. A high Q in the crystal and the high input resistance of the gain stage result in near-sinusoidal waveforms developed across C_1, and the amplitude of sinusoidal waveform is a function of the ratio of C_1 and C_2 and the large signal transconductance G_m. The oscillation frequency of crystal oscillators is restrained between the series and parallel resonant frequencies in order that the crystal impedance is inductive. This results in the maximum possible frequency variations of crystal oscillators no more than C/C_o, which is typically a few tenths of a percent since C_0 is much higher than C for almost all crystals. A varactor diode connected in series with the crystal provides a variable capacitor C_V through a large isolation resistor R_{iso} and causes a pulling of the frequency. The oscillation frequency can be approximated by

$$f_{osc} = f_s \left[1 + \frac{1}{2} \frac{C}{C_V + C_0} \right] \tag{2.6}$$

where f_s = series resonant frequency = $\frac{1}{2\pi\sqrt{LC}}$. As can be seen in (2.6), compared with (2.5), the fre-

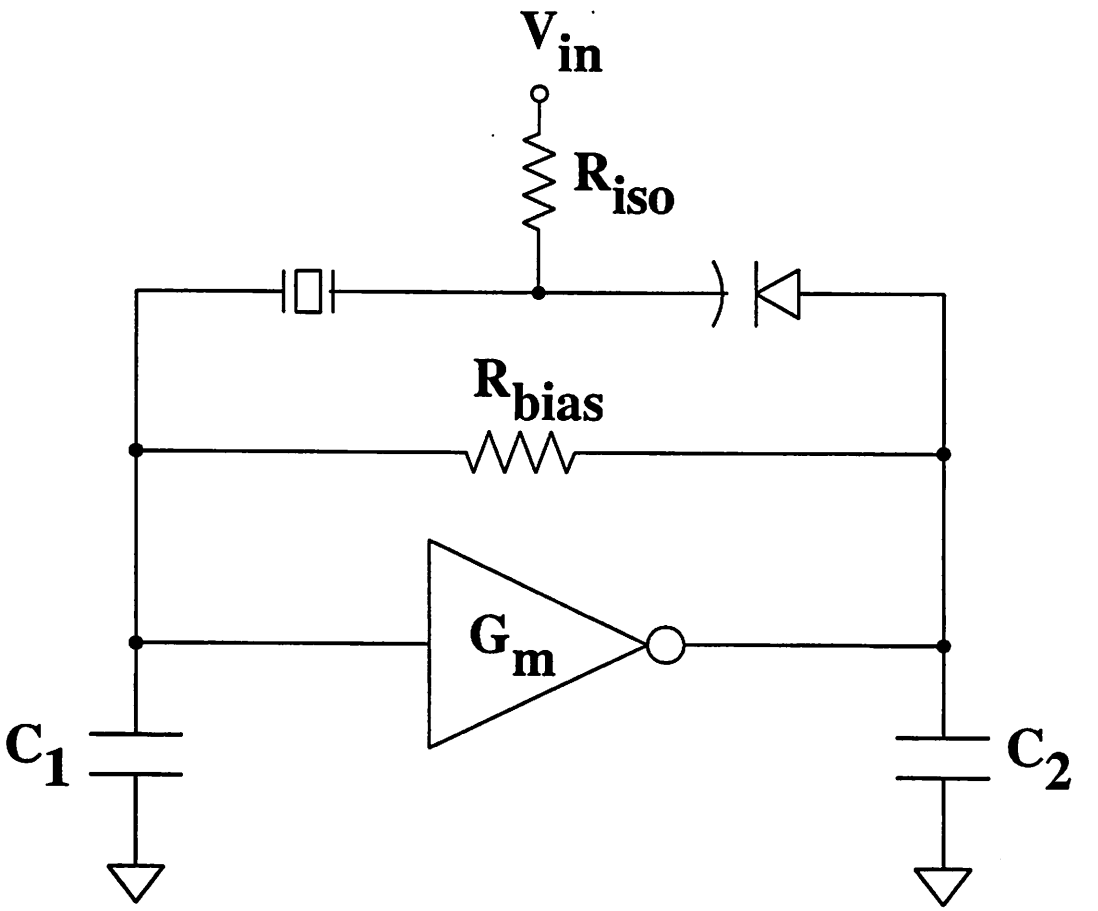


Figure 2.11 - Voltage-controlled crystal oscillator

quency pulling can be obtained is much smaller than with varactor-tuned LC oscillators, as a result of the high Q in crystal. However, the frequency stability with temperature and power supply, and phase noise are much improved at the same rate. For example, the temperature effects on active devices are absorbed by the sharp roll-off phase-frequency characteristics of crystal, and are negligible compared with the TC of crystal itself,[16] which is usually the dominant term. With careful design, monolithic crystal oscillators have demonstrated a TC of frequency less than one hundredth of ppm/°C for temperature -10 to +60 °C, and a power supply rejection of .05 ppm/V.[17]

Since the crystal dimension is inversely proportional to the mechanical frequency of fundamental vibration, practical considerations such as durability and power dissipation usually limit fundamental

operation to less than 20 MHz, although higher frequencies operation are possible by operating on an overtone frequency. Harmonic multiplication from lower frequencies must be employed for even higher frequencies.

The oscillation frequency of a crystal VCO (VCXO) with a varactor diode can change just as quickly as the capacitance of the varactor can be changed, and that is limited by the time constant of isolation resistor R_{iso} and varactor capacitance C_V.[18] Therefore, fast response of a VCXO is entirely feasible if circuits are properly designed.

2.4.2. Relaxation Oscillators

Relaxation oscillators are the most commonly used oscillator configuration in monolithic IC design because they can operate in a wide frequency range with a minimum number of external components. Unlike harmonic oscillators, there are no expensive frequency-selective tuning elements in relaxation oscillators but at most one timing capacitor for frequency determining, and thus relaxation oscillators are suitable for monolithic integration. Periodic square waveforms, often along with triangular waveforms, are generated while circuits switch back and forth between two astable states. During each period, circuits stay in one of the states for a certain period of time, then followed by a fast transition before relaxing into the other astable state for the same time interval as the previous state if symmetrical circuit schemes are used.

According to the mechanism of the oscillation and topology employed, relaxation oscillators can be further broken down into three types: (1) grounded capacitor VCO, (2) emitter-coupled VCO, and (3) delay-based ring VCO. The operation of the first two oscillators are similar in the senses that the time duration spent in each state is determined by the timing capacitors and charge/discharge currents while the third oscillator operates quite differently since the the timing relies wholly on the delay in each stage of the inverters which are connected in a ring configuration.

2.4.2.1. Grounded Capacitor VCO

The generalized circuit configuration of a typical grounded capacitor VCO is shown in figure 2.12.

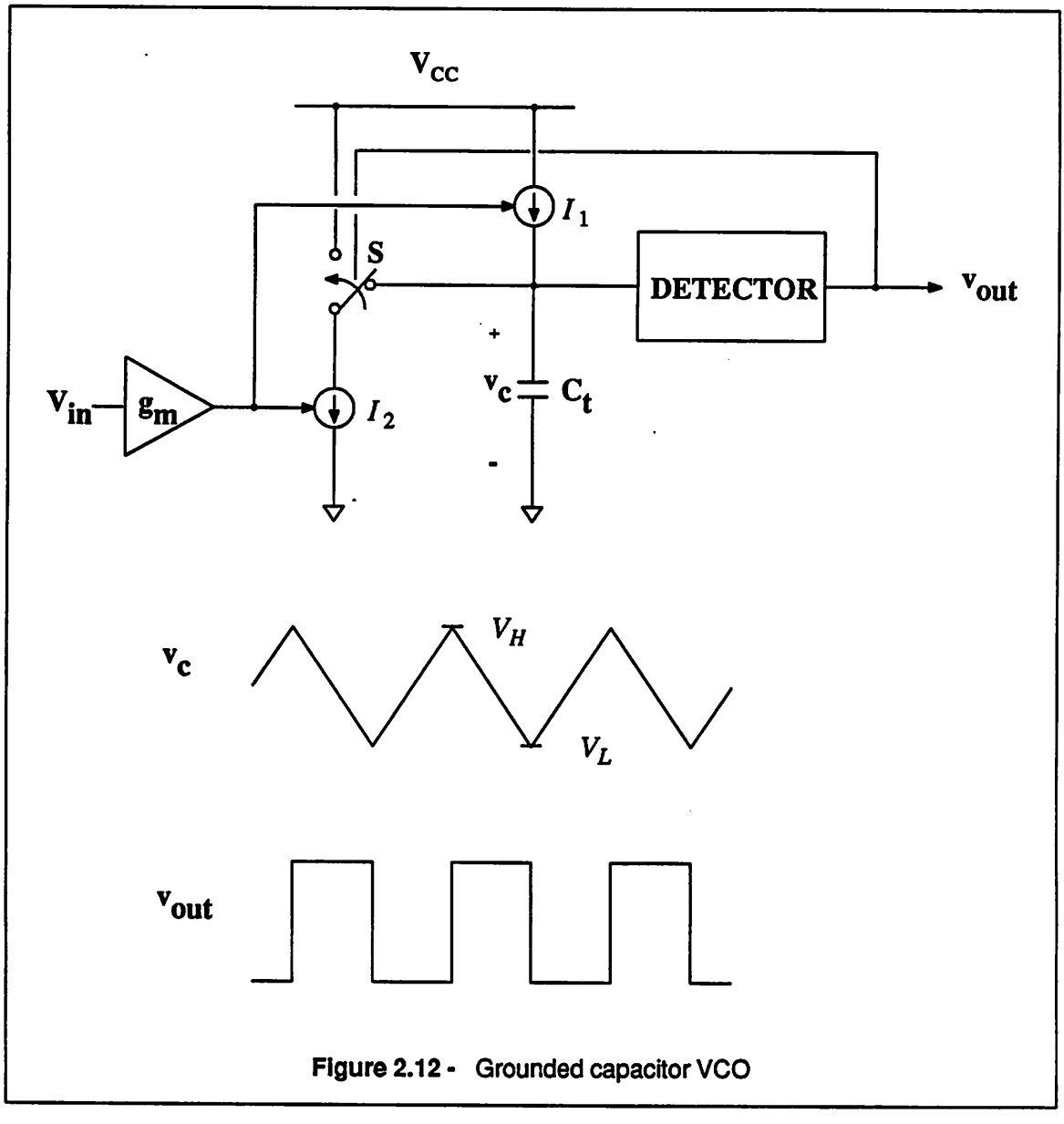


Figure 2.12 - Grounded capacitor VCO

The circuit consists of a detector which sense the voltage V_c across the timing capacitor C_t to determine the state of the switch S, a current sink I_1, a current source I_2, and a transconductance stage which converts input control voltage V_{in} linearly to current I_1 and I_2. The operation of the circuit can be briefly described as follows: Assuming initially S is thrown at the position as indicated in Figure 2.12, the capacitor C_t is therefore being discharged by a net current of $I_2 - I_1$, and the voltage is discharging at a rate of

$$\frac{dv_c}{dt} = -\frac{I_2 - I_1}{C_t} \tag{2.7}$$

This linear discharging continues until the lower threshold of the detector V_L is reached. At this point, the detector changes the state of switch and the capacitor C_t is charged with current sink at a rate of

$$\frac{dv_c}{dt} = \frac{I_1}{C_t} \tag{2.8}$$

until V_c reaches the upper threshold of the detector V_H and switch S is reset, thus completing one period of oscillation. For this type of oscillator, square and triangular waveforms are available at the output of the detector and the timing capacitor, respectively. If the current source I_2 is precisely twice the current sink I_1, the triangular waveform is symmetrical and the duty cycle of the square wave is 50%. Furthermore, the frequency of oscillation can be expressed as:

$$f_{osc} = \frac{I_1}{2C_t(V_H - V_L)} = \frac{V_{in}g_m}{2C_t(V_H - V_L)} \tag{2.9}$$

where g_m is the voltage-to-current conversion gain of the transconductance stage.

As indicated in the above equation (2.9), the oscillation frequency can be varied linearly with control voltage V_{in} over a wide range. However, this type of oscillator depends on the the tracking of the charge and discharge current in order to maintain a symmetrical triangle and square and thus the control range of frequency is limited to approximately 100:1. In practical applications, the timing capacitor is left external to the chip in order to have more flexibility in setting the operating frequency range, although the sweep range of frequency can be high for a given timing capacitor. The design of the detector section is important for the grounded capacitor VCO since the the precision of the oscillation frequency is dictated by the precision of the threshold voltages of the detector, together with g_m and C_t, which are usually set by external precision components.

There are two ways to implement the detector. One commonly used approach, which is suitable for applications up to several hundred MHz, is to employ one or two comparators to sense the voltage level of the input signal with threshold voltage levels of comparator defined through some external vol-

tage, for example power supply V_{CC}, and resistor ratio. The output of the comparator is then applied to a R-S flip-flop which in turn controls the switch to charge or discharge the timing capacitor accordingly. In this approach, threshold voltages are well-defined and therefore good frequency stability and accuracy can be achieved with careful design. However, there are many stages in the signal path and the resulting signal propagation delays become significant at high frequencies. Consequently, the accuracy and stability of the oscillation frequency deteriorate at frequencies higher than a few MHz due to excessive switching delays mainly stemmed from the finite response time of the comparator and flip-flop.

This disadvantage leads to the second approach which replaces the comparator and flip-flop by a single stage Schmitt trigger to reduce the associated switching delays. Normally the Schmitt trigger consists of only a non-saturating differential gain stage with positive feedback to achieve hysteresis in the voltage transfer curve. Since few active devices are used in the signal path, the switching delays in Schmitt trigger are minimized and this allows high speed operation. The threshold voltages, however, are determined by the internal circuit variables such as thermal voltage $V_T = \frac{kT}{q}$ due to the lack of stable, well-defined reference voltage in the positive feedback loop.

As a result, the use of single stage Schmitt trigger in the grounded capacitor VCO requires special circuit schemes to compensate the temperature dependent voltage levels and therefore stabilize the frequency drift with temperature, before one can take advantage of high-frequency capability of such a VCO. The compensation is accomplished by designing I_1 in eq. (2.9) having the same temperature dependence as the threshold difference $V_H - V_L$ of the Schmitt trigger and thereby their temperature effects are cancelled out to a first order to attain a stable frequency. [4] The reported TC of frequency for the VCO using this technique is 60 ppm/°C. Nevertheless, this compensation technique is restricted to the grounded capacitor VCO and effective for frequencies up to 20 MHz. For higher frequencies, the uncompensated switching delays are not negligible and inevitably become an important part of oscillation period. Moreover, switching delays are strongly temperature dependent and difficult to model accurately. In addition to temperature drift, voltage-to-frequency linearity and frequency accuracy control are degraded as well at high frequencies since switching delays must be included in Eq.(2.9). These design

considerations make it a difficult and challenging task to implement a linear, temperature-stable VCO at high frequencies. This will be the topic of Chapter 3.

Besides temperature instability, phase jitter is another limitation of relaxation oscillators. Since the relaxation VCO is essentially a wideband switching circuit, there exists no frequency limiting components except the timing capacitor and parasitics from the active devices. As a result, the phase noise in the grounded capacitor VCO, like other relaxation oscillators, is theoretically and practically higher than in LC or crystal oscillators, which have much lower noise bandwidth arising from the high Q tank circuits.[14] The triangular waveform across the timing capacitor, in contrast to the sinusoidal waveform in the tank circuit of harmonic oscillator, does not help the phase noise either because of its constant ramping property. One possible solution to reduce the phase jitter is to increase $V_H - V_L$ of the detector, i.e., the voltage swing of the timing capacitor, to relatively reduce the uncertainty of the switching instants which is caused by the noise modulating the thresholds of detector. Among various noise sources, the input-referred noise of the detector is usually the main contributor of phase jitter. Therefore, it is desirable to use low noise transistors in the detector input stage to minimize the jitter. For example, in bipolar technology the ideal candidate would be the transistors with high current gain and low base resistance while being biased at high current levels to the extent that the unity current gain frequency f_T is not significantly reduced.

2.4.2.2. Emitter-Coupled Oscillator

The high frequency capability of the grounded capacitor VCO can be further improved by combining the current switching components and Schmitt trigger into one high speed switching section. Since this reduces the number of stages involved in the switching process, the associated delays are minimized to attain high frequency operation. The simple, symmetrical circuit configuration and the use of all non-saturating *npn* transistors make them very popular in various monolithic designs.

The simplified emitter-coupled oscillator, as well as the associated waveforms, is illustrated in Figure 2.13. It eliminates the necessity to precisely match two current sources with opposite polarity, as required in the grounded capacitor VCO, by using a matched pair of *npn* current sources to alternately

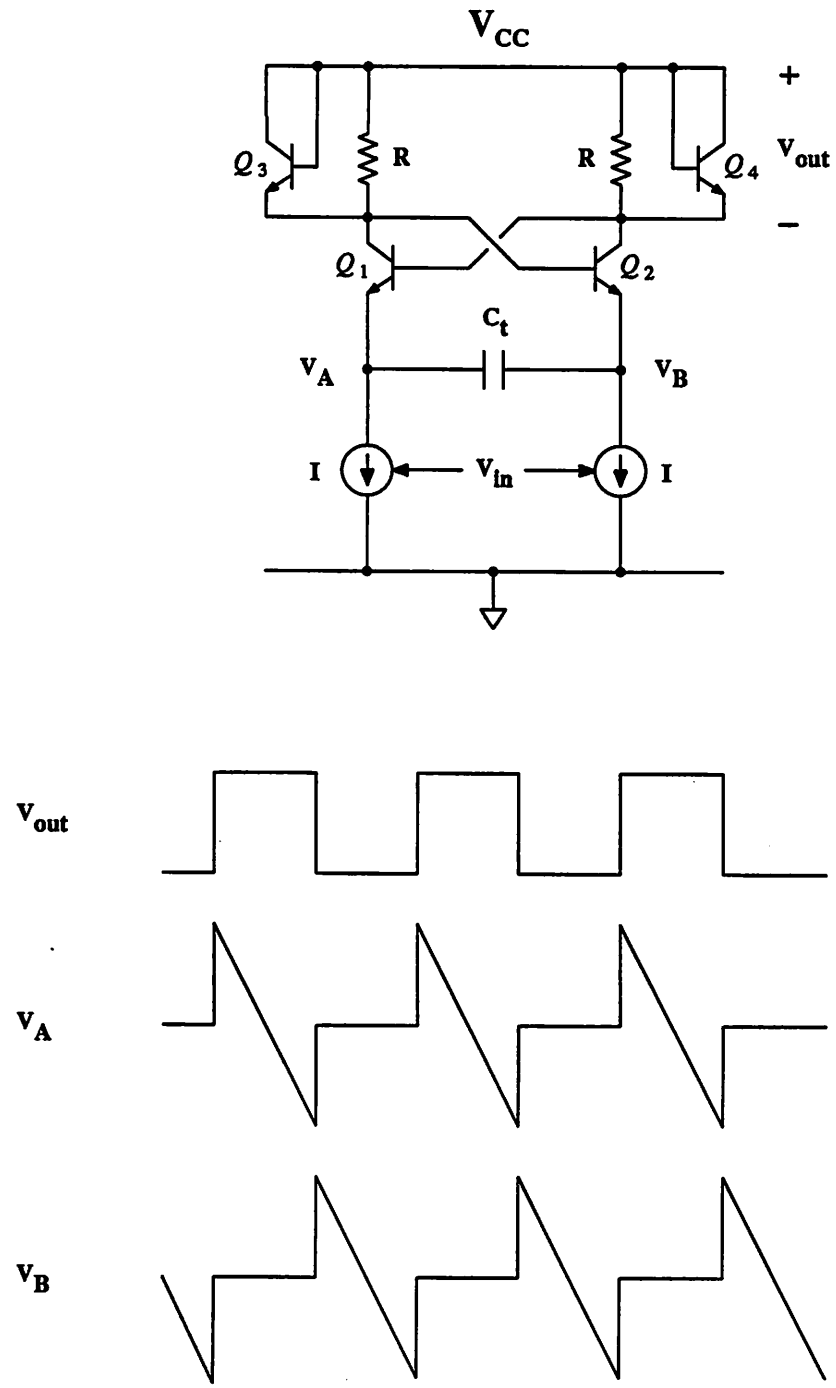


Figure 2.13 - Emitter-coupled oscillator

discharge each side of the timing capacitor C_t, through which the emitters of Q_1 and Q_2 are coupled. Since *npn* current sources can be matched better than *pnp* current sources, the circuit is capable of maintaining a symmetrical triangular and rectangular waveforms over a wide sweep range, typically 1000:1. The oscillator is composed of transistors Q_1 and Q_2 forming the positive feedback gain stage through the load resistor R and clamping diode-connection transistors Q_3 and Q_4 which clamp the voltage swing across R to 1 V_{BE}, and two well-matched *npn* current sources whose value can be varied by a control voltage V_{in}.

The operation of the circuit can briefly be described as follows. Assume initially that both Q_1 and Q_3 are conducting and Q_2 and Q_3 are off. If base currents are neglected, then the emitter of Q_1 is held at $V_{CC} - V_{BE}$ while the emitter of Q_2 is discharging at a rate of I/C_t. This discharging continues until the emitter of Q_2 reaches $V_{CC} - 2V_{BE}$, at which time Q_2 turns on. As a result, Q_4 starts conducting, which subsequently turns off both Q_1 and Q_3, causing the emitter of Q_2 to be pulled up to 1 V_{BE} below V_{CC}. Since the voltage across a capacitor cannot change instantaneously the $1V_{BE}$ voltage step is coupled to the other side of timing capacitor C_t, changing the voltage on the emitter side of Q_1 from $V_{CC} - V_{BE}$ to V_{CC}. At this time, the second half of the period begins, and proceeds in the same way as the first half with the roles of Q_1–Q_3 and Q_2–Q_4 interchanged since the circuit is symmetrical.

The frequency of the oscillation can be calculated, by taking the reciprocal of two times the each half period, as:

$$f_{osc} = \frac{I}{4V_{BE}C_t} \tag{2.10}$$

Note that in addition to several output waveforms available, being a square wave with peak-to-peak voltage swing of V_{BE} at collectors of Q_1 and Q_2, and two linear ramps at the emitters of Q_1 and Q_2, other waveforms can also be generated using linear or nonlinear processing. A linear triangular waveform is attainable by subtracting V_A from V_B, or vice versa, with a simple differential-to-single-ended amplifier. Similarly, the quadrature output can be readily derived by squaring the differential triangular voltage across the timing capacitor. This is desirable in some applications such as coherent AM detection

described in section 2.2.7. Other applications require sinusoidal waveforms and they can be obtained through the use of a differential gain stage with emitter degeneration.[19]

Since the emitter-coupled oscillator contains only *npn* transistors it is capable of very high frequency operation. The upper limit of the oscillation frequency is determined by the switching delays around the positive feedback loop and parasitic capacitors at the emitters of Q_1 and Q_2. These parasitics, which are nonlinear, are contributed from the base-emitter junction capacitances of Q_1 and Q_2, the collector-to-substrate capacitances of transistors making up of the current sources, and the parasitic capacitances from package where the circuit is housed if an external timing capacitor is employed. As discussed previously, those parasitics cause severe problems at high frequencies, including temperature instability, nonlinearity, and frequency inaccuracy. As to the lower limit of the oscillation frequency for the configuration in Figure 2.12, let us examine Equation (2.10) carefully. In Equation (2.10), it seems that the oscillation frequency f_{osc} can be decreased without limit as the current I is decreased. However, Equation (2.10) holds only when the voltage swing at collectors of Q_1 and Q_2 are clamped at V_{BE} by Q_3 and Q_4. Therefore, when I is decreased to such a value that $2IR = V_{BE}$, the oscillation frequency reaches a minimum:

$$f_{osc,min} = \frac{1}{8RC_t} \tag{2.11}$$

Further decreasing I would not change the oscillation frequency, until it reaches a critical value I_{crit} which is the minimum current needed to sustain the oscillation. This corresponds to the initial loop gain of the positive feedback around $Q_1 - Q_2$ in Figure 2.12 equal to unity. It can be shown that:

$$I_{crit} = \frac{kT}{qR} \tag{2.12}$$

where kT/q is the thermal voltage, and is equal to 26 mV at a room temperature of 27°C. If I is even further decreased, the oscillation will eventually die away before an intermediate state will be reached.

One major drawback exists with the oscillator of Figure 2.12. The sensitivity of the frequency with respect to temperature is poor due to the V_{BE} dependence of the period. The temperature coefficient can

be calculated by using Equations (2.1) and (2.10):

$$\frac{1}{f_{osc}}\frac{\partial f_{osc}}{\partial T} = -\frac{1}{V_{BE}}\frac{\partial V_{BE}}{\partial T} = \frac{2\ mV/°C}{800\ mV} = 2500\ ppm/°C \tag{2.13}$$

since V_{BE} varies at a rate of about -2 mV/°C with temperature. It should be noted that the frequency of the oscillator has a positive TC of 2500 ppm/°C even at low frequencies. This temperature effect may be compensated at low frequencies by making the discharge current source I with the same dependence of V_{BE} to a first order. This technique can yield a TC of ±300 ppm/°C for frequencies up to 5 MHz.

Further improvement of the temperature performance of this type oscillator can be achieved by clamping the voltage swings at the collectors of Q_1 and Q_2 in Figure 2.12 to a stable internal precision voltage reference V_R , rather than the V_{BE} drop of transistors.[20] This improved oscillator is illustrated in Figure 2.14. The operation of the circuit is similar to the operation described, therefore it will not repeated here. The voltage at the collector of Q_1 is alternatively clamped to $V_{CC} - V_R - V_D$ and $V_{CC} - V_D$ when Q_1 is on and off, respectively. Here V_D denotes the voltage drop of the diodes carrying current I. Therefore, the voltage swing at the collector of Q_1 is clamped at reference voltage V_R. Similar to Equation (2.10), the frequency of oscillation is expressed as:

$$f_{osc} = \frac{I}{4C_t V_R} \tag{2.14}$$

It is worth mentioning that the reference voltage V_R is normally derived from an on-chip bandgap reference and its value can be changed easily by resistor ratio, unlike the circuit in Figure 2.12, where voltage is fixed to $V_{BE} \approx 0.8$ V. This is important because for high frequency oscillation the voltage swings within the circuit must be small. For example, if f_{osc} = 100 MHz, $I = 2$ mA, and $C_t = 20$ pF, then the corresponding V_R is 250 mV, which is much smaller than V_{BE}.

With careful layout and design, including accurate prediction of temperature behavior at the proximities of the switching points, a temperature drift of less than ±100 ppm/°C over a 10,000:1 linear frequency sweep range can be attained. As with other circuits, however, the frequency stability deteriorates at high frequencies as a result of the absence of compensation for switching delays, and for the parasitics

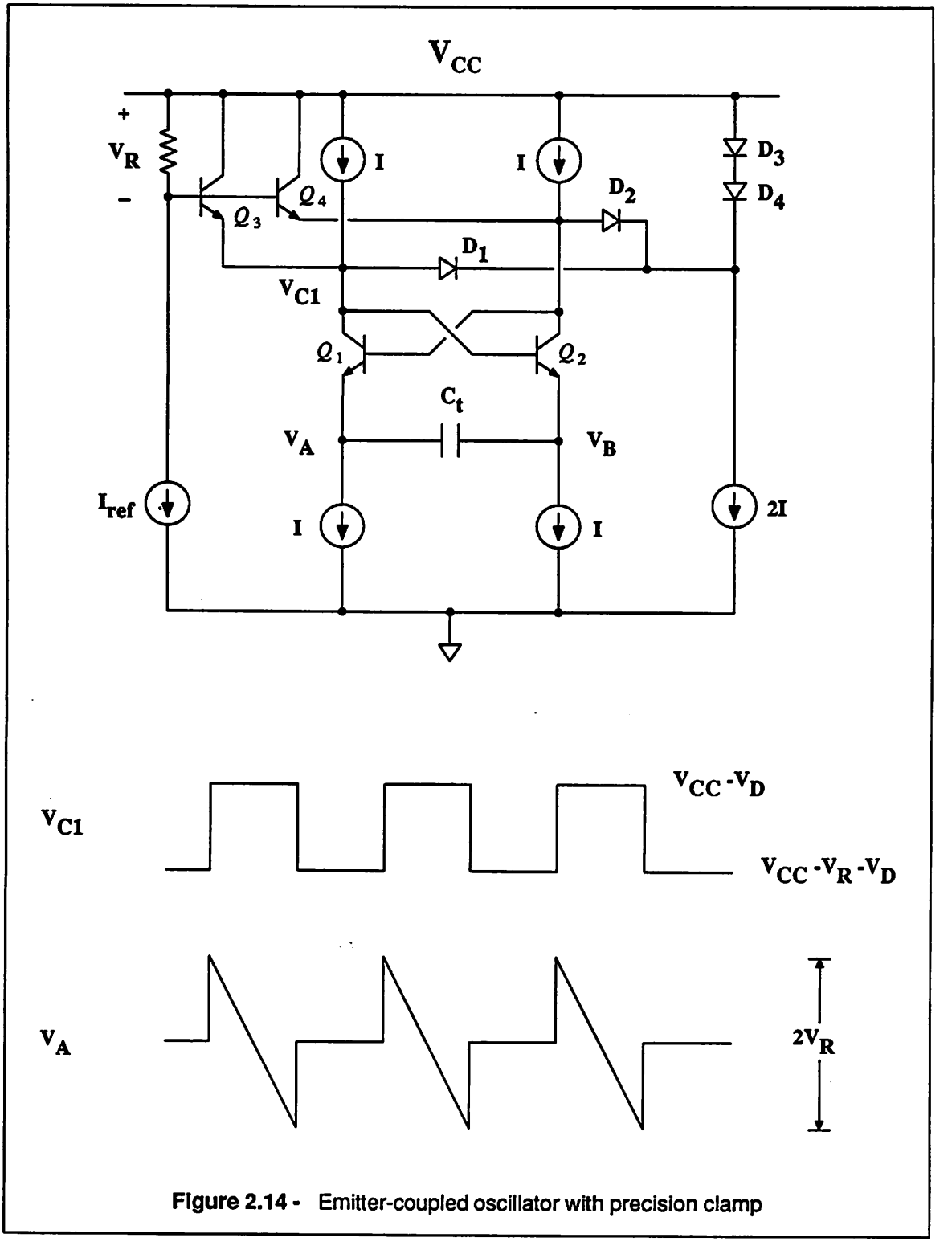


Figure 2.14 - Emitter-coupled oscillator with precision clamp

present at the both sides of the timing capacitor.

The emitter-coupled oscillator has performance similar to the grounded capacitor VCO in terms of phase jitter. Low jitter requires large voltage swing across the timing capacitor, and small input-referred noise at the base of switching transistors Q_1 and Q_2. Unless a small on-chip capacitor is used for timing, the requirements for low jitter and high- frequency capability are opposed to each other. The use of an on-chip capacitor, however, gives rise to potential problems since parasitics may now be of the same magnitude. Ring oscillators, the other type of relaxation oscillators, also use on-chip capacitors for high frequency operation and will be discussed in the following section.

2.4.2.3. Delay-based Ring Oscillator

Recently ring oscillators have received considerable attention in high frequency PLL applications for clock synchronization and timing recovery,[21,22,23,24] for they can provide very high frequency oscillation with rather simple digital-like circuits, which are compatible with digital technology and therefore suited for very large scale integration (VLSI), although the original applications were mainly in the measurement of the switching speeds of the inverter gates for monitoring process parameters. As shown in Figure 2.15, the ring oscillator, with multiphase outputs $\phi_1, \phi_2, \cdots, \phi_N$, is composed of an odd number of identical inverter stages which are connected in a ring configuration to form a feedback loop. The delay time of each inverter can be adjusted with an external voltage by varying either the currents or the RC time constants associated with the logic transitions. Figure 2.16 shows an inverter cell, implemented in CMOS technology, whose switching delay is controlled by the input voltage V_{in} through the two current sources used to charge/discharge the parasitic capacitors at node X.

Being different from the grounded capacitor and emitter-coupled VCO, which use the timing capacitor and controlled current sources to determine the oscillation frequency, the ring oscillator utilizes the delay time associated with each inverter cell, in conjunction with the gain provided by inverters, to oscillate between two logic states, "1" or "0", of the inverters. Actually, the ring oscillator is a degenerated harmonic oscillator and its operation can be explained by referring to the block diagram in Figure 2.7, where $A(s)$ corresponds to the effective gain stage, and $\beta(s)$ represents the lumped delay stage to

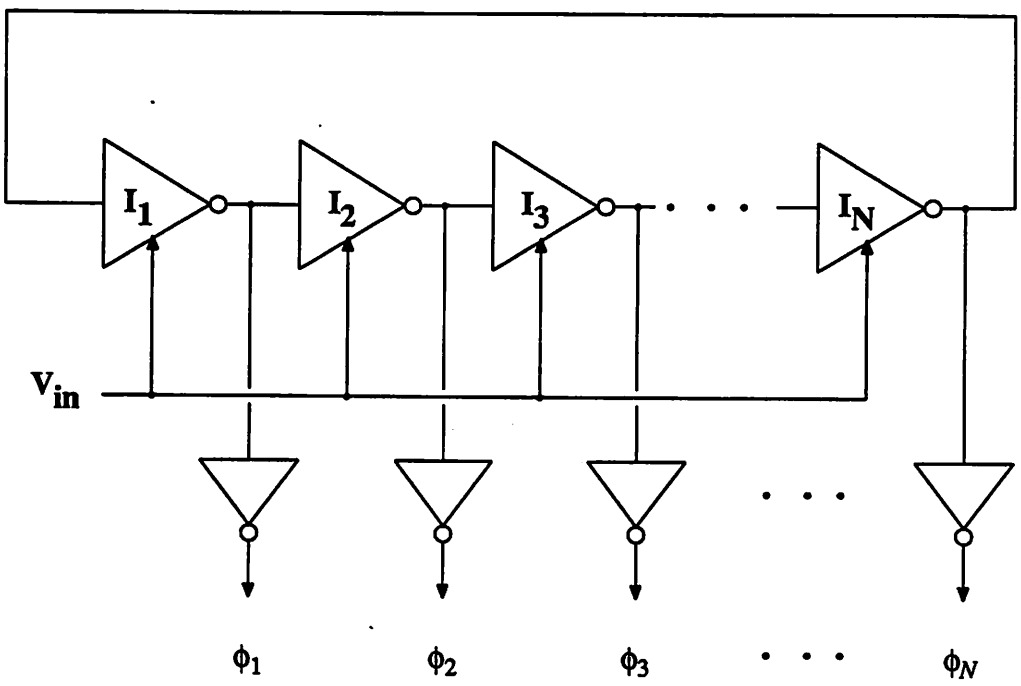


Figure 2.15 - Voltage-controlled ring oscillator

account for the resultant switching delay. More specifically,

$$A(s) = \prod_{i=1}^{N} a_i = a_1 a_2 \cdots a_N \tag{2.15}$$

and

$$\beta(s) = e^{-s\sum_{i=1}^{N}\tau_i} = e^{-s(\tau_1+\tau_2+\cdots+\tau_N)} \tag{2.16}$$

where N is the number of inverter stages in the ring, and a_i and τ_i are the gain and delay time associated with the i^{th} inverter stage I_i, respectively. Assuming each inverter stage is ideal and identical such that a_i = -a and $\tau_i = \tau$, Equations (2.15) and (2.16) becomes:

$$A(s) = (-1)^N a^N \tag{2.17}$$

and

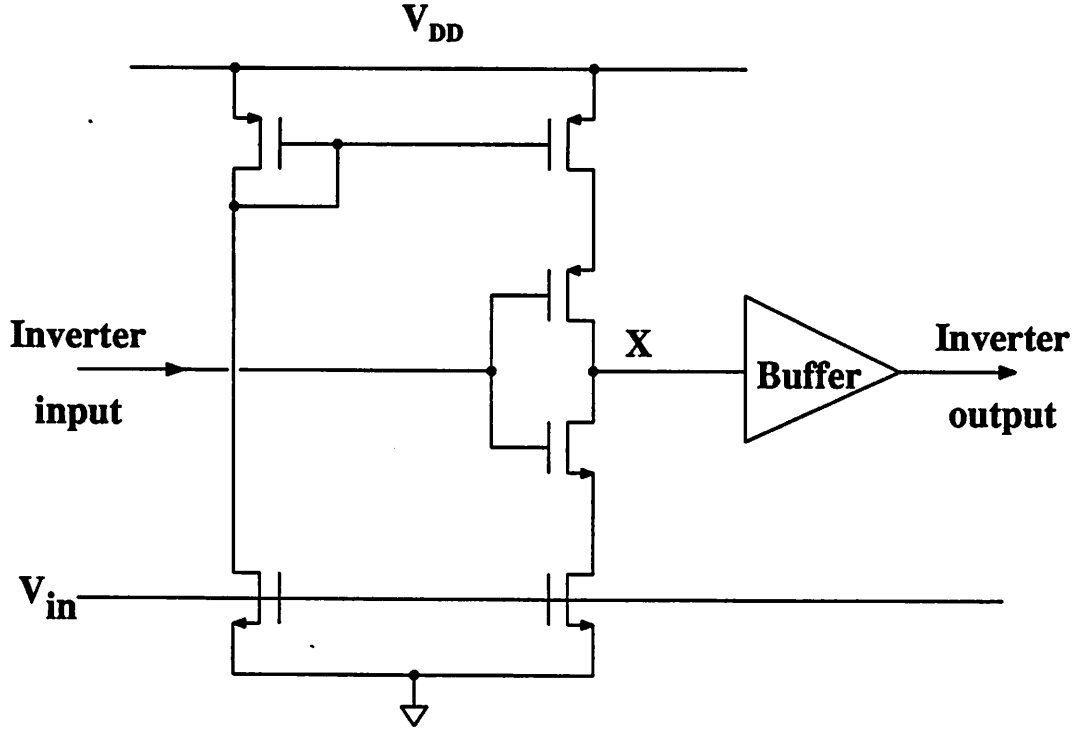


Figure 2.16 - Inverter cell of ring oscillator

$$\beta(s) = e^{-sN\tau} \tag{2.18}$$

From Equation (2.18) it becomes quite clear that since its equivalent feedback network $\beta(s)$ is nothing but a delay line, which is an all-pass filter with linear phase shift, the ring oscillator can be regarded as a harmonic oscillator with extremely low Q, and as a result, does not have sinusoidal waveforms but square waveforms instead. The frequency of oscillation can be found by substituting Equations (2.17) and (2.18) into (2.3) to yield:

$$\frac{\pi}{2}\left[1 + (-1)^{N+1}\right] + 2\pi f_{osc} N\tau = 2m\pi \tag{2.19}$$

$$where \quad m = 0,1,2,\cdots$$

Therefore, the oscillation frequency is:

$$f_{osc} = \frac{2m - \frac{1}{2}\left[1 + (-1)^{N+1}\right]}{2N\tau} \qquad (2.20)$$
$$where\ m = 0,1,2,\cdots$$

It can be seen from the above equation that in order to insure that oscillation occurs, the number of inverter stages constituting the ring must be an odd number, otherwise the circuit would be latched on to either state and no oscillation can take place since $f_{osc} = 0$ for $m = 0$ when N is even. If N is an odd number, the oscillation frequency can be expressed as:

$$f_{osc} = \frac{2m - 1}{2N\tau} \qquad (2.21)$$
$$where\ \ m = 1,2,3,\cdots, \text{and}\ N = 1,3,5,\cdots$$

Hence, the oscillation frequency is determined by the delay time of the inverter and number of inverter stages. Because the delay time τ of the inverter stage is small, usually few nanoseconds or less, the ring oscillator, which use no off-chip components, can easily operate in the sub-GHz range. This very high frequency capability, together with the simple circuit configuration, make the ring oscillator very competitive in GHz oscillator designs with current very high speed technology.

However, there are several drawbacks to the ring oscillator which must be taken into account before being used in practical applications. First, the oscillation frequency is very sensitive to temperature and power supply variations. This is due to the variations in parasitics caused by the change in temperature and power supply. Since the oscillation frequency is inversely proportional to the delay time, any variation in delay time resulted from parasitics will entirely be reflected as the frequency variations. Second, because of its dependence on the delay of each cell and thus the parasitics, the oscillation frequency is very sensitive to processing and cannot be controlled accurately. In practice, the difficulty in modeling parasitics and lot-to-lot process variations give rise to the frequency inaccuracy. Without being trimmed or locked into many reference frequency by using a PLL, the ring oscillator is not suitable for many applications where precise frequency control is needed. Third, even with accurate frequency control, the ring oscillator may not oscillate at the desired frequency. As indicated in Equation (2.21), for given N and τ, the oscillation frequency can be odd harmonics of fundamental frequency $1/(2N\tau)$, so

called multimode oscillation.[25] Therefore, precautions should be made in the design of the circuit to prevent those undesired modes of oscillation from taking place, especially when number of invert stages is large.

Finally, as in other broadband switching circuits, phase jitter is caused by the noise modulating the threshold levels in the circuits. For example, referring to Figure 2.16, noise at the inverter input and node X, which are mainly due to active devices and high speed switching, are the primary contributor of phase jitter. One way to improve the phase noise is to increase the voltage swings at critical nodes. The other approach is to use large number of inverter stages to "smooth out" the variations in the period of the oscillation. Both methods, however, are at the expense of larger power consumption and lower operating speed. In fact, it is a rule of thumb that by adding extra circuitry in each inverter stage, all the disadvantages just mentioned can be improved with an increase in circuit complexity and decrease in operating speed.

2.5. Summary

After reviewing the various types of VCO, it is worth comparing and summarizing their advantages and limitations in terms of high frequency monolithic IC design. The LC-tuned or crystal VCO have the following advantages:

- *Superior frequency stability.* This includes frequency stability with temperature, power supply, and noise. The high Q of the LC-tank circuit and crystal makes the oscillation frequency insensitive to those environmental effects on the active devices employed. However, if a varactor diode with adequate Q is used in place of the capacitor in the LC-tank, special compensation measures for the varactor must be taken to preserve the stability with temperature.
- *Good frequency accuracy control.* Since the oscillation frequency is primarily determined by the high Q tank circuit or crystal, it can be set very accurately. Although LC and varactor tuned oscillators are more suitable for higher frequency monolithic IC design than crystal oscillators, their frequency accuracy tends to deteriorate at high frequencies due to the fact that circuits with lower Q are more sensitive to parasitics.

- *High frequency capability.* This is normally limited not by the active devices but by the minimum physical size of inductor or crystal, and package parasitics since the role of active elements is limited to provide gain and the associated phase shifts can be neglected if a high Q tank circuit is used.

Nevertheless, there are two major drawbacks:

- *Not compatible with monolithic IC technology.* Their frequency-setting elements, namely inductors and crystals, are expensive and all external to the IC.
- *Limited frequency tuning range.* Besides limited attainable frequency tuning range by an external adjustment, usually less than few percent, a nonlinear relationship between control voltage and oscillation frequency excludes some important applications, such as FM demodulation.

On the contrary, relaxation oscillators prevail in the category of:

- *Compatible with monolithic IC technology.* Only one (or none) timing capacitor is needed. It can be external to be more flexible, or integrated on the chip if very high frequency oscillation is desired.
- *Linear voltage-to-frequency control characteristic.* Since frequency is normally proportional to a current or voltage and inversely proportional to timing capacitor, frequency can be varied linearly over a very wide range. The exception is the ring oscillator whose frequency is varied nonlinearly over a wide range.

The limitations of relaxation oscillators, stemming from their ease of frequency tuning that is on the other hand the major merit of such oscillators, are:

- *Poor frequency stability.* The frequency of oscillation is very sensitive to temperature, power supply, and noise because switching delays are strongly dependent upon those environment factors and become a large percentage of the oscillation period at high frequencies.
- *Frequency inaccuracy.* Accurate control of frequency is hampered by the switching delays, parasitics at the timing nodes, and the matching of on-chip components, which is the dominant term at low frequencies. It becomes worse if an on-chip timing capacitor is used to obtain higher frequency operation.

- *High frequency capability.* Again, switching delays are the primary limiting factors for high frequency capability. The ring oscillator seems to be the potential candidate for very high frequency operation. However, the high frequency capability is not an independent issue in general and must be resolved in conjunction with stability and accuracy of frequency when one attempts to extend the applications to higher frequencies.

The preceding discussion suggests that by the marriage of the merits of the crystal oscillators, being the excellent frequency accuracy and stability, and the merits of relaxation oscillators, being the very wide and linear frequency control characteristics and high frequency capability, it may be possible to design a VCO capable of operating at up to several hundred MHz while maintaining frequency stability with temperature and wide dynamic range, provided that high f_T transistors are used. This will be discussed in detail in the next chapter.

CHAPTER 3

CLOSED-LOOP VOLTAGE-CONTROLLED OSCILLATORS

3.1. Introduction

In Chapter 2 various VCO configurations were reviewed and compared for monolithic IC realization. It was found that a relaxation oscillator is preferred to a harmonic oscillator in many applications because it requires no inductor or crystal for frequency setting and has a wide frequency control range. Furthermore, among the monolithic relaxation oscillators, the emitter-coupled VCO is the most attractive one due to the fact that it is a versatile building block that can operate at very high frequencies if high speed devices and an on-chip timing capacitor are used to minimize internal switching delays and external parasitics. Nevertheless, its frequency stability with temperature, one of the most important requirements for the VCO, deteriorates at high frequencies. Although there has been a considerable amount of work directed to improve the temperature stability at high frequencies,[3,4,20,26] these temperature compensation techniques can achieve temperature coefficients of frequency less than ±100 ppm/°C at oscillation frequencies no more than 20 MHz. Such performance limits the use of VCO's in many applications such as high-frequency PLL's, FM demodulators, FSK demodulators used for data communications, optical data storage systems, and timing recovery in optical fiber digital transmission systems.

In order to overcome the difficulties of compensating temperature-dependent switching delays and parasitics at high frequencies, a novel VCO configuration with global feedback from the output oscillation frequency to input control voltage is presented in this chapter. As will be shown, the feedback approach not only stabilizes the frequency with temperature, but also improves the voltage-to-frequency linearity and frequency accuracy, which are also degraded at high frequencies due to switching delays and parasitics. Although this technique is intended for stabilizing emitter-coupled oscillators, it can also be applied to other oscillator configurations where precision, linearity, and temperature stability of frequency are required.

Before examining the proposed closed-loop VCO architecture, it is worth, at this point, clarifying

the necessity and importance of low TC of frequency for the VCO through the following questions: (1) why a low TC of frequency is important for the VCO, and (2) how low the TC of frequency should be.

3.2. Requirement of TC of Frequency for VCO

As described in Chapter 2, a VCO is mainly used in the transmitter or receiver circuits of communication systems. When employed in either case, the frequency stability of the VCO is essential since it determines whether the demodulation process in the receiver is successful. Among various factors affecting the frequency stability, temperature effects are the most prominent and troublesome. A VCO with a high TC of frequency can result in the failure of reception in communication, particularly in coherent communication.[27]

This can be best illustrated by using the example of the VCO in PLL applications. With reference to the block diagram as shown in Figure 2.4, the output from a PLL system can be obtained either as the voltage signal $V_d(t)$ at the loop filter output, or as a frequency signal f_{out} at the VCO output terminal. The voltage signal is used in FM demodulator applications, whereas the frequency signal is utilized in timing recovery applications. In either case, it is crucial that during the capture or acquisition process the PLL must be able to acquire lock with the input signal starting with the free-running condition, before any meaningful output is generated. For a successful acquisition in the capture process, the input frequency has to fall in the window as illustrated in Figure 3.1(a). The window, termed as the capture range which is one of the important PLL design parameters, is centered at the free-running or center frequency f_c of the VCO with a width approximately equal to two times the bandwidth of the loop filter in Figure 2.4.[28] The center frequency of the VCO (the VCO frequency when $V_d = 0$) and loop filter bandwidth should be carefully chosen to insure the loop will lock on the input frequency. However, the loop may fail to acquire lock with the input frequency in the capture process at other temperatures. This is illustrated in Figure 3.1(b), where the VCO center frequency drifts from f_c to f_c' when temperature changes from T_1 to T_2 while the bandwidth of loop filter is assumed constant for simplicity. The failure of acquisition during the capture process results in the PLL feedback loop being essentially broken since the frequency difference between the input and VCO frequency is beyond the the loop filter bandwidth and

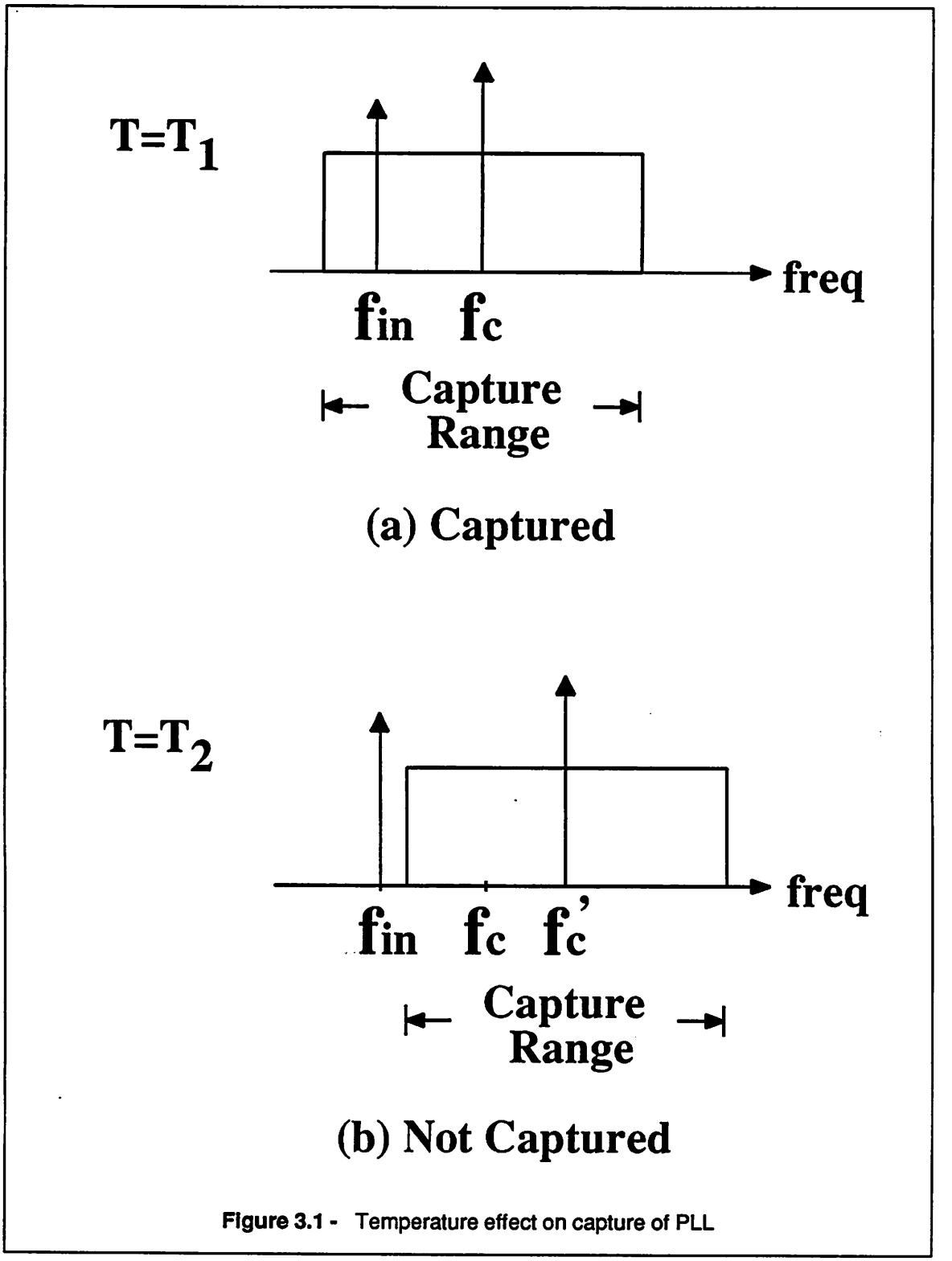


Figure 3.1 - Temperature effect on capture of PLL

no negative feedback action can take place to drive the VCO frequency towards the input signal frequency. As a result, both voltage and frequency outputs generated from the VCO for this case are unrelated to the input and are meaningless. A VCO with a low TC of frequency is therefore required to attain a constant capture range for the PLL, regardless of temperature variations. Although this example shows the necessity of a low TC for a VCO used in the PLL, the conclusion can be readily applied to the VCO in other applications. For instance, the frequency of the input signal in Figure 3.1 should have a low TC so that the acquisition is maintained even when environmental temperature changes. In other words, the VCO used as transmitter to generate the input signal frequency is required to have the same TC of frequency as required for the VCO in PLL applications.

The next question naturally raised is how low the TC of the VCO frequency should be. It is obvious that the TC should be kept as low as possible. However, the upper bound of TC depends upon the particular application. Stated more precisely, this is dictated by both the bandwidth of loop filter used and expected temperature variation range during the operation of system. For example, if a PLL is used as the timing recovery circuit, the loop filter bandwidth or equivalent capture range is typically about 1% of the VCO center frequency. Assume the PLL is operating in an environment where temperature is expected in the range of -20°C to 100°C. This means that the corresponding TC requirement for the VCO in this particular application can be approximately calculated as:

$$TC = \frac{\Delta f}{f}\frac{1}{\Delta T} = \frac{0.01}{[(100+20)/2]\ ^\circ C} = \pm 167\ ppm/^\circ C \tag{3.1}$$

It is clear that the estimated TC is quite optimistic since the worst case, i.e., the initial frequency offset between the input and VCO free-running frequency is not equal to zero, has not been taken into account. In practice, the VCO is designed to have a TC half the calculated value in Equation (3.1) in order to operate properly. For a PLL with a wide detection band such as used in FM demodulators, the TC requirement can be relaxed somewhat but in general is still kept no higher than ±100 ppm/°C for the worst case design. In fact, this is a quite useful rule of thumb for low TC VCO circuit design.

Although the preceding discussion about stability requirements is focused on temperature effects, it applies equally well to the stability requirements with respect to other environmental variables such as

power supply and process variations. Following the same argument in the temperature case, the requirements of stability with power supply and process variations for the VCO can be found in a similar way.

In the light of the motivation attaining a low TC for the VCO, the next legitimate point at issue is to investigate new VCO architectures to accomplish good frequency stability with temperature at high frequencies. This will be described in the next section.

3.3. Closed-loop VCO

All the relaxation VCO configurations that have been discussed so far can be topologically characterized as the open-loop VCO, see Figure 3.2(a).

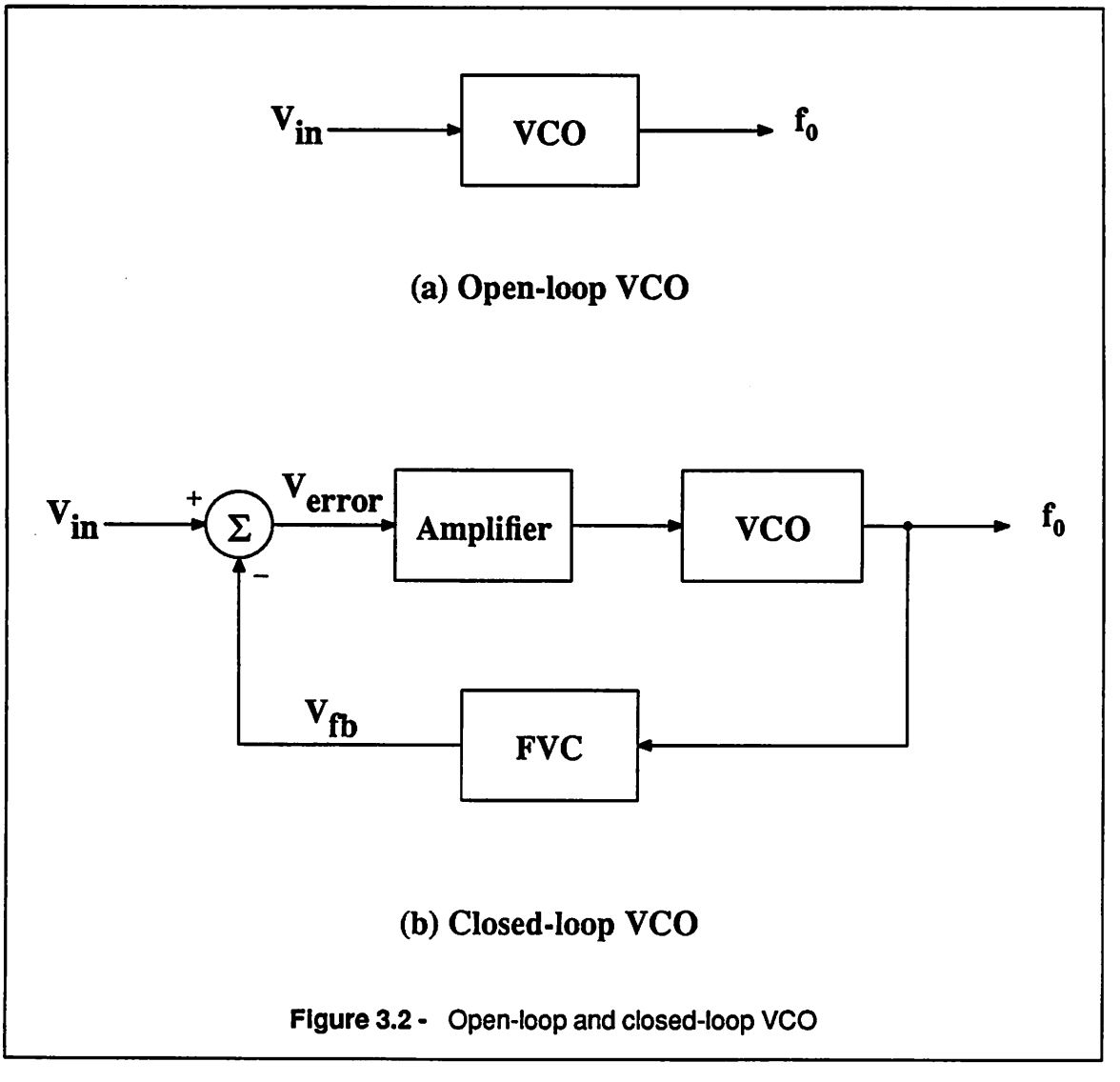


Figure 3.2 - Open-loop and closed-loop VCO

In this approach, the frequency stability, voltage-to-frequency characteristic, and frequency accuracy of the VCO are all determined by the *intrinsic* parameters, such as the reference voltages, charge/discharge currents, and timing capacitor. Despite the excellent performance attained at low frequencies, such techniques are not appropriate for high frequency VCO design for the reason that once the oscillation frequency deviates from the desired value, in terms of temperature drift, power supply variations, nonlinearity, or inaccuracy as a result of significant switching delays and parasitics, in no way can any compensations be made since there is no *global* feedback path between the input control voltage and output oscillation frequency. In addition to minimizing the switching delays and parasitics through the use of more advanced technology, one solution to remedy the errors occurring at high frequencies is to employ a global feedback loop around the input control voltage and output frequency, resulting in a **closed-loop** VCO.

The block diagram of the closed-loop VCO is shown in Figure 3.2(b). This is essentially a classical negative feedback control system with a unique feedback element frequency-to-voltage converter (FVC) which linearly converts the output frequency f_0, with a conversion gain k_f, back to the voltage signal V_{fb} to compare with the input control voltage V_{in} through an adder Σ. If the VCO frequency differs from the desired value due to any reason, the error voltage V_{error} is amplified by the amplifier with a gain of A and is then used to drive the VCO frequency in a direction to minimize the error voltage, as a consequence of the negative feedback action. In the steady state, V_{fb} is forced to be equal to V_{in} within a finite error voltage which is needed to drive the amplifier and VCO. In other words, f_0 will be linearly proportional to V_{in} if a linear FVC is used, even if the core VCO exhibits control nonlinearities.

Quantitatively, the analytic form governing f_0 and V_{in} is:

$$f_0 = \frac{Ak_V}{1 + Ak_V k_f} V_{in} \tag{3.2}$$

where k_V is the VCO gain. Normally loop gain $= Ak_V k_f >> 1$, Equation (3.2) becomes:

$$f_0 = \frac{1}{k_f} V_{in} \tag{3.3}$$

As indicated in Equation (3.3), if the loop gain is large enough, the feedback element FVC dictates the

input-output characteristic of the closed-loop VCO, independent of the parameters of the components in the forward path. Consequently, the performance of the closed-loop VCO relies on that of the FVC, rather than the core VCO itself. For this reason, let us examine the key element FVC before analyzing the performance of the closed-loop VCO.

Two different approaches are used to obtain a linear frequency-to-voltage conversion. First, a PLL such as shown in Figure 2.4 can accomplish the required conversion by locking on an input frequency and producing an error voltage proportional to the frequency deviations of the input signal. However, this method does not solve the existing problem because the linearity of conversion is dependent on the linearity of the VCO used in the PLL. In a word, such an approach is in vain since we literally shift the problem of VCO nonlinearity associated with high frequencies from one VCO to another without fundamentally eliminating it. Although the PLL still acts as an FVC in a nonlinear fashion and can be included in the closed-loop VCO to compensate temperature effects, it is our intention that the closed-loop VCO must be capable of meeting both linearity and thermal stability requirements. The second approach is to integrate a current pulse train with a period of T and fixed pulse width t_0, which is generated through an one-shot (monostable) circuit triggered by the input periodic signal f_{in}, as illustrated in Figure 3.3. The output of the one-shot circuit is used to control the on-off of the switch S, and therefore to set the average current supplied to the integrator circuit. The operation of the FVC is now briefly described as follows. For each cycle, the switch S is thrown at the position as shown for a time interval of t_0, determined by the internal parameters of the one-shot circuit, to integrate constant current I_0 through $R-C$ network. During the remaining of the cycle, S is set at the other position and the capacitor C discharges through R. Assume that its ripple is much smaller than dc term, the output voltage V_{out} can be found by equating the average currents entering and leaving the $R-C$ integrator.

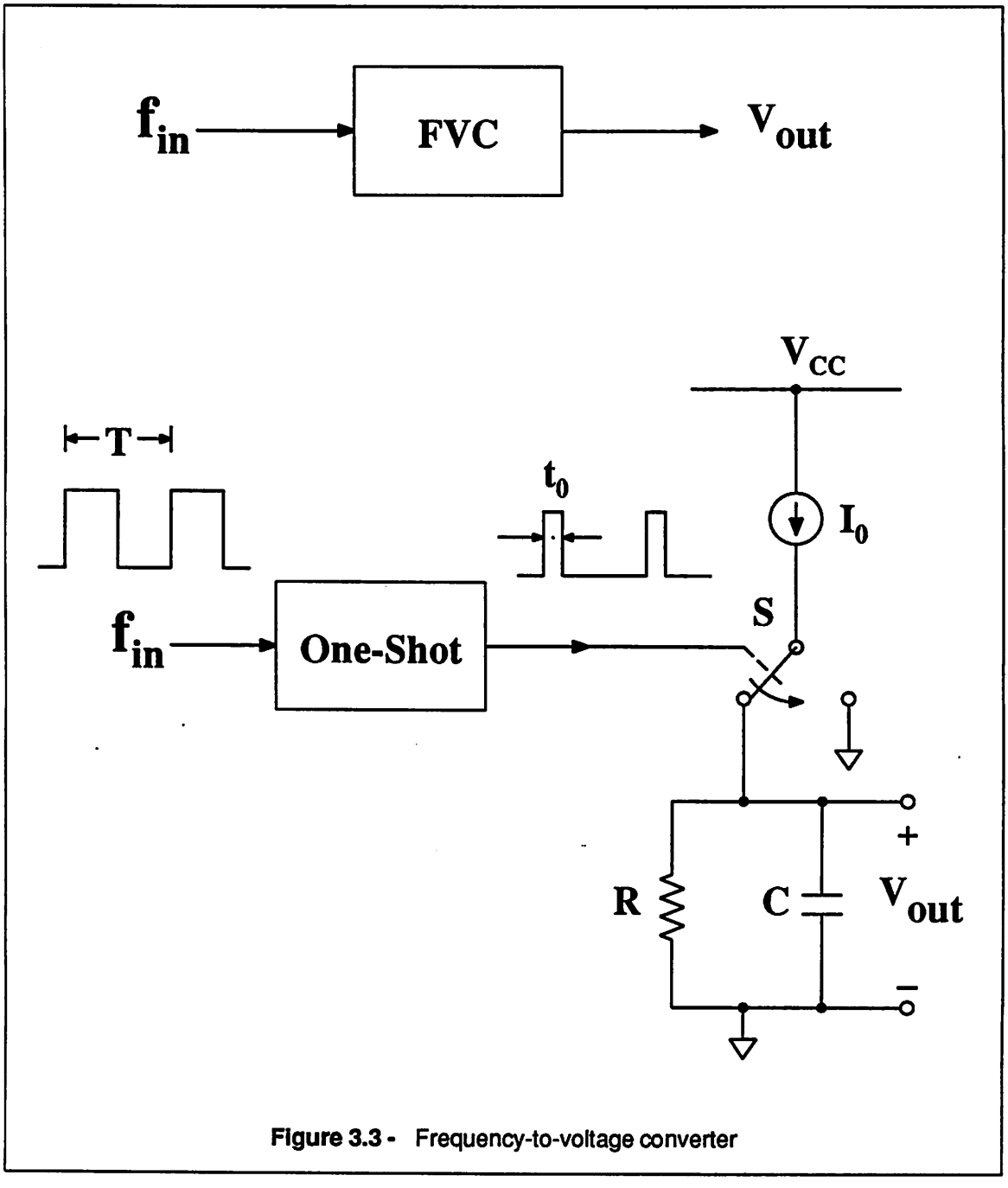


Figure 3.3 - Frequency-to-voltage converter

$$V_{out} = I_{avg} R = k_f f_{in} \qquad (3.4)$$
$$where \quad k_f = I_0 t_0 R$$

Therefore, the output voltage V_{out} of the FVC is linearly proportional to the input frequency f_{in} with a temperature-sensitive conversion gain since all the circuit parameters I_0, t_0, and R are generally tempera-

ture dependent. Note that the frequency response and output ripple of the FVC are directly related to the values of R and C. Unfortunately, both design considerations are in conflict with each other and a trade-off is inevitable. This will be discussed in detail in Chapter 4.

As a result, while the voltage-to-frequency characteristic of the closed-loop VCO can be made linear by using a linear FVC, the oscillation frequency still remains uncompensated with temperature since the conversion gain k_f of the FVC is generally temperature dependent. Therefore, the oscillation frequency of the closed-loop VCO would suffer from temperature instability as encountered in the open-loop approach, if no compensation scheme is employed in Figure 3.2(b).[29]

3.4. Temperature compensation

In this section, two different compensation techniques to yield a temperature-stable oscillation frequency for the closed-loop VCO are presented. As suggested in Equations (3.3), the oscillation frequency f_0 can be stabilized against temperature variations by means of either predistorting V_{in} in such a way that it has the same dependence of temperature as the conversion gain k_f of the FVC, or employing an additional feedback loop surrounding the FVC to stabilize k_f. Single-loop feedback is used in the first approach, whereas dual-loop feedback is used in the second approach.

3.4.1. Single-Loop Feedback

The block diagram of the temperature-compensated VCO using single-loop feedback is shown in Figure 3.4. The summer Σ and gain stage in Figure 3.2(b) are replaced by the operational amplifier (op amp) A. A multiplier Π is used to perform the required multiplication between V_{in} and the output of a duplicate frequency-to-voltage converter FVC_2 to predistort the input voltage applied to the noninverting input of op amp A. Ideally the two FVC's have the same temperature behavior and hence their effects on f_0 are neutralized since thermal drifts at the inputs of op amp are of the same form and then are rejected as common-mode signals.

Two references are needed in this approach: a frequency and voltage reference. To faithfully reflect the temperature dependence of k_f at the output of FVC_2, a precise and stable reference frequency

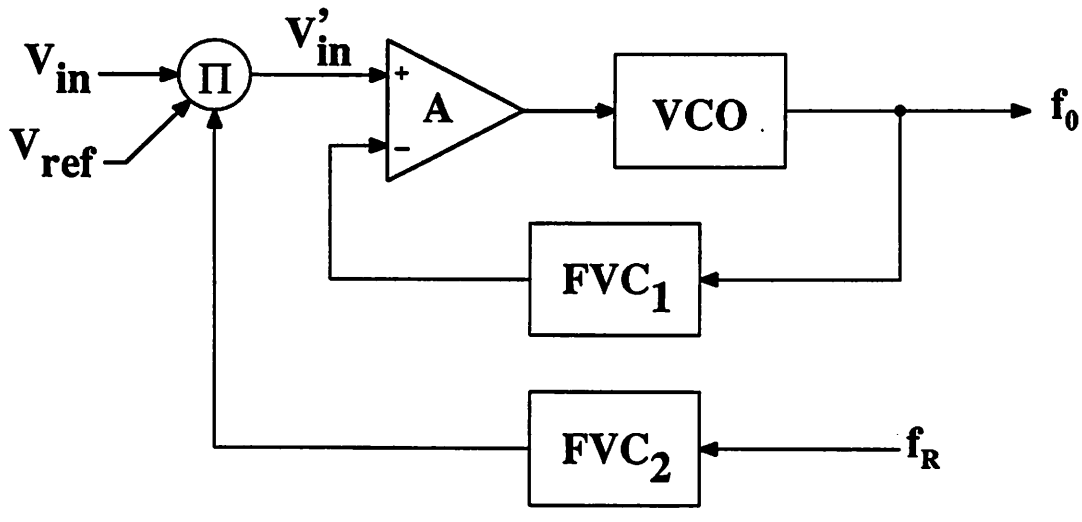


Figure 3.4 - VCO with single-loop feedback

f_R, which can be derived from the system clock if the VCO is integrated with a large system or from an on-chip self-contained crystal oscillator otherwise, is needed at the FVC_2 input. Derived from an on-chip bandgap reference, a constant reference voltage V_{ref} is essential because it provides the voltage scaling constant for the multiplier. The predistorted voltage at the noninverting input to the op amp is then:

$$V_{in}' = (\frac{f_R}{V_{ref}})V_{in}k_f \tag{3.5}$$

which is a linear function of k_f and V_{in} with a well-defined proportional constant f_R/V_{ref}. For large loop gain, the oscillation frequency f_0 can be found by substituting Equations (3.5) into (3.3):

$$f_0 = \frac{V_{in}}{V_{ref}} f_R \tag{3.6}$$

As desired, a linear dependence of frequency on input control voltage is attained to first order along with a proportional constant independent of temperature, power supply, and parasitics and nonlinearities associated with the core VCO.

Note that the linearity of the VCO voltage-to-frequency characteristic depends not only on the linearity of the FVC, but also on the linearity of the multiplier. However, as shown later, the offset

voltages of the multiplier must be kept low in order to minimize the temperature drift of the VCO oscillation frequency. It is difficult for a multiplier to attain two conflicting requirements simultaneously. Such a design difficulty leads to the other approach: the dual-loop feedback.

3.4.2. Dual-Loop Feedback

Figure 3.5 shows the block diagram of a closed-loop VCO with a dual-loop feedback.

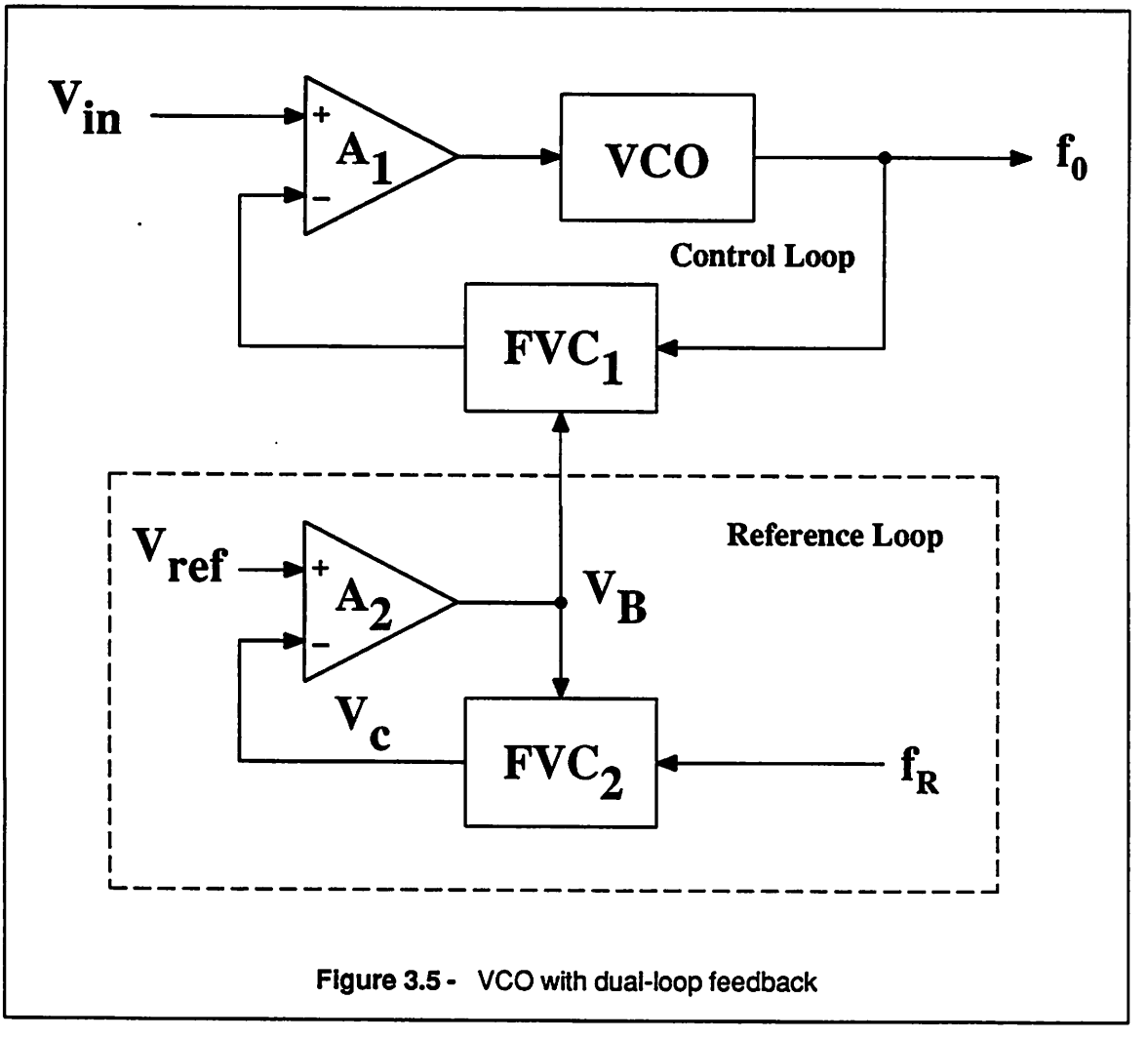


Figure 3.5 - VCO with dual-loop feedback

To eliminate the use of an analog multiplier to improve the linearity and minimize the offset voltages in the circuit, a reference loop, the replica of the first loop (control loop), is used to monitor and correct the variations in the conversion gain k_f of the FVC's due to temperature. It is interesting that both approaches, single-loop and dual-loop feedback, require the use of precision, stable, voltage and

frequency references. However, an FVC whose conversion gain can be adjusted through a second input voltage, different from the FVC used in the single-loop feedback, is required in the dual-loop feedback configuration. The implementation of this type of FVC will be presented in the next chapter.

The operation of the control loop is similar to the single-loop feedback configuration in that the oscillation frequency of the uncompensated VCO is forced to be linearly proportional to the control voltage V_{in} through negative feedback action of op amp A_1, and the linear frequency-to-voltage characteristic of FVC_1. The thermal drift of the FVC is stabilized through the reference loop consisting of FVC_2, op amp A_2, reference voltage V_{ref} and frequency f_R. Any temperature-induced drift in FVC_2 is amplified by A_2 and negatively fed back to adjust k_f in both FVCs in a direction to make V_c constant (equal to V_{ref}), while a stable reference frequency f_R is provided to the input of FVC_2. By applying the same adaptive bias voltage V_B to FVC_1 in the control loop, a temperature-stable FVC is achieved and therefore a linearly voltage-controlled, temperature-compensated frequency is available at the output of the core VCO.

It should be pointed out that temperature compensation for the FVCs is accomplished in the reference loop, outside the signal path, and hence the input signal is not affected by the presence of the temperature compensation circuits in the reference loop. Its importance will become clear when the frequency response for the closed-loop VCO is discussed in Chapter 4.

To provide an insight into the important factors of low TC and high linearity, the TC of the closed-loop VCO frequency is determined analytically in the next section. It will also be used as a guidance in the later circuit design phase to minimize the errors from various sources.

3.5. Effects of Nonideal Components

Several error sources affect the VCO performance in temperature stability. Practically, the oscillation frequency drifts with temperature due to temperature effects of the op amp finite gain, offset voltages in the circuit, imperfect tracking between FVC's, and temperature drift of reference voltage and frequency. As will be shown later, the drift of offset voltages and references are the dominant contributors to the VCO drift with temperature if the op amp is designed with a moderate gain. As far as the linearity

and precision of the oscillation frequency are concerned, offset voltages and the reference voltage turn out to be the limiting factors for the VCO performance. Since all the error terms are quite small compared to the signal level, the individual effect of different error sources can be considered *independently*. Therefore, for simplicity, one error source is taken into consideration at a time in the following analysis. The total VCO drift is then the summation of each component contributed from the corresponding error source. The following analysis is for the dual-loop feedback VCO but can be applied to the single-loop feedback VCO as well.

3.5.1. Op Amp Offset Voltages

Figure 3.6 shows the block diagram of a closed-loop VCO with offset errors in the op amps. Each op amp is assumed ideal except that an offset voltage V_{OS} is present and in series with its input. The TC can be analyzed by first obtaining the relationship between the oscillation frequency f_0 and input control voltage V_{in}. In the control loop, the output of FVC_1 is forced equal to the input voltage minus the voltage $V_{OS,1}$ of the op amp A_1:

$$V_{in} = k_{f1} f_0 + V_{OS,1} \qquad (3.7)$$
$$where \;\; k_{f1} = conversion\ gain\ of\ FVC_1$$

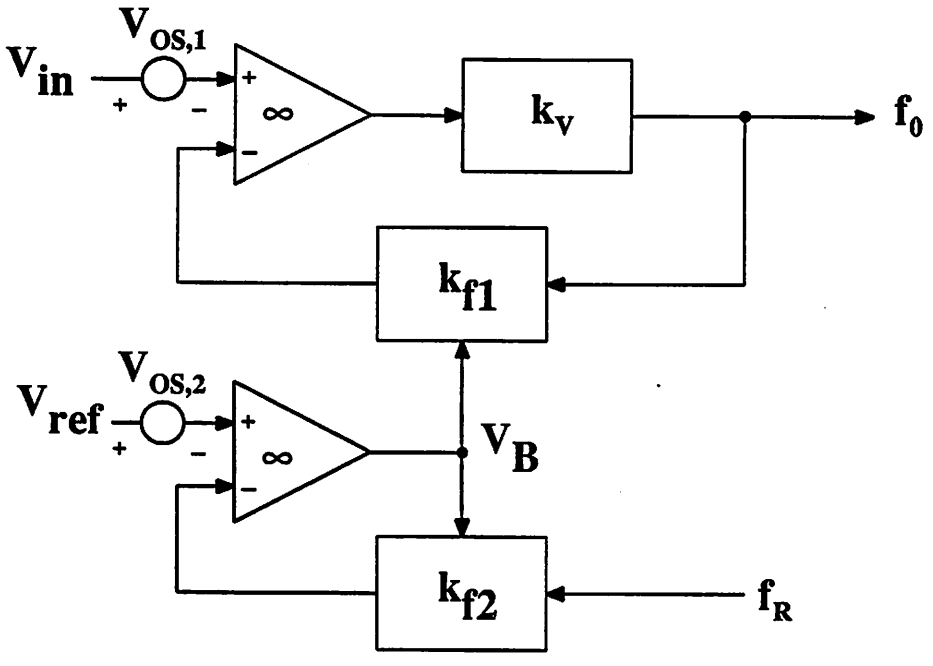
Similarly, for the reference loop:

$$V_{ref} = k_{f2} f_R + V_{OS,2} \qquad (3.8)$$
$$where \;\; k_{f2} = conversion\ gain\ of\ FVC_2$$

Assume that two FVC's are identical except that k_{f1} and k_{f2} are in proportion , i.e.

$$k_{f2} = k\ k_{f1} \qquad (3.9)$$

Here k is ideally a dimensionless constant independent of temperature and voltage, and is normally set by the geometrical ratio of resistors and transistors. The introduction of k is important because the control and reference loop can operate in different frequency ranges by properly setting such a scaling constant. Substituting Equations (3.9) and (3.8) into (3.7) yield:



$$\frac{k_{f1}}{k_{f2}} = k = constant$$

Figure 3.6 - Op amp offset voltage effects

$$f_0 = kf_R \left[\frac{V_{in} - V_{OS,1}}{V_{ref} - V_{OS,2}} \right] \tag{3.10}$$

Normally offset voltages $V_{OS,1}$ and $V_{OS,2}$ are much smaller than V_{in} and V_{ref}. Therefore Equation (3.10) can be simplified as:

$$f_0 = kf_R \left(\frac{V_{in}}{V_{ref}}\right) \left[1 - \frac{V_{OS,1}}{V_{in}} + \frac{V_{OS,2}}{V_{ref}} \right] \tag{3.11}$$

It can be seen from Equation (3.11) that f_0 is still *linearly* dependent on V_{in}, but deviates from the ideal value of $kf_R\left(\frac{V_{in}}{V_{ref}}\right)$ because of the presence of offset voltages in the op amps, as indicated by the second and third terms in the bracket. The effect of offset voltages on the frequency inaccuracy can be minimized by either reducing the inherent op amp offset voltages or increasing the input and reference voltage

levels.

The TC of frequency can now be derived by using Equations (2.1) and (3.11):

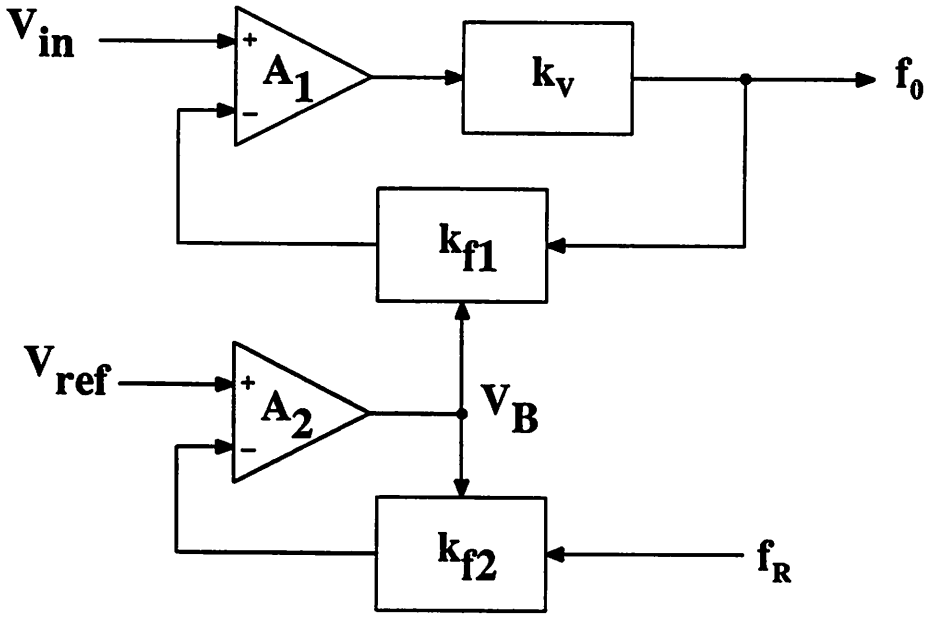
$$TC = \frac{1}{f_0}\frac{\partial f_0}{\partial T} = -\frac{V_{OS,1}}{V_{in}}\left[\frac{1}{V_{OS,1}}\frac{\partial V_{os,1}}{\partial T}\right] + \frac{V_{OS,2}}{V_{ref}}\left[\frac{1}{V_{OS,2}}\frac{\partial V_{OS,2}}{\partial T}\right] \qquad (3.12)$$

assuming other variables except $V_{OS,1}$ and $V_{OS,2}$ are held constant with respect to temperature. Equation (3.12) shows that the TC of each op amp offset voltage, the term in each bracket, weighted by the "offset-to-signal ratio" contributes directly to the TC of the closed-loop VCO. It is clear that, if the op amps are implemented in Si-bipolar technology, their effects on the VCO drift can be minimized by boosting the ratio of signal voltage at the op amp input to the op amp offset voltage, as in the case of frequency inaccuracy, since the TC of offset voltages due to the mismatch of components is equal to $\frac{1}{T}$ at the absolute temperature T°K. For example, for $T = 300\,°K$, $V_{OS} = 5mV$, and $V_{in} = 500mV$, the corresponding TC contribution from each op amp is 33 ppm/°C. Thus, in the worst case, the magnitude of TC for the VCO can be estimated to be about 70 ppm/°C from offset voltages alone, if each op amp contributes equally.

3.5.2. Op Amp Finite Gain

The block diagram of a closed-loop VCO with errors due to the finite gain of the op amp is shown in Figure 3.7. Each op amp is ideal but requires a finite voltage across its inputs to drive the VCO and FVCs. Since the op amp gain is finite and temperature dependent, the VCO oscillation frequency varies with temperature as a result of deviations in k_f's.

The analysis is similar to the one aforementioned. In fact, by replacing $V_{OS,1}$ and $V_{OS,2}$ in Equation (3.11) with $\frac{f_0}{A_1 k_V}$ and $\frac{V_B}{A_2}$, respectively, one can obtain the oscillation frequency f_0 as:



$$\frac{k_{f1}}{k_{f2}} = k = constant$$

Figure 3.7 - Finite op amp gain effects

$$f_0 = kf_R\left(\frac{V_{in}}{V_{ref}}\right)\left[1 + \frac{V_B}{A_2 V_{ref}} - \frac{1}{S_1}\right] \tag{3.13}$$

where $S_1 = open\ loop\ gain\ of\ control\ loop = A_1 k_{f1} k_V$

if each loop has a large but finite open loop gain. Although both Equations (3.11) and (3.13) are of the same form, the finite gain of op amps affects not only the frequency accuracy but also the linearity of f_0. As indicated in Equation (3.13), the finite gain A_2 in the reference loop causes the frequency to depart from the desired value by a fixed percentage of $\frac{100V_B}{A_2 V_{ref}}$, while the finite gain of the op amp in the control loop, thus finite S_1, gives rise to the nonlinearity error of f_0 through the conversion gain k_V, which is generally nonlinear and voltage dependent. Both absolute and nonlinearity errors can, however, be effectively reduced by increasing the gain of the op amps. For example, the inaccuracy due to the reference

loop can be kept lower than 0.1% if A_2 is 1000 or more, provided that $V_B \sim V_{ref}$. Similarly, since the effects of nonlinearities of the components in the forward path of the control loop on the oscillation frequency f_0 is reduced by the open loop gain,[28] a nonlinearity of 20% in the core VCO, for example, will cause approximately a nonlinearity of only .02% for f_0, if op amp A_1 has a gain of 1000 and $k_{f1}k_V = 1$.

It can be shown that, by differentiating Equation (3.13) with respect to temperature, the TC of frequency is:

$$TC = -\left(\frac{V_B}{A_2 V_{ref}}\right)\left[\frac{1}{A_2}\frac{\partial A_2}{\partial T}\right] + \frac{1}{S_1}\left[\frac{1}{A_1}\frac{\partial A_1}{\partial T}\right] + \frac{1}{S_1}\left[\frac{1}{k_V}\frac{\partial k_V}{\partial T}\right] \tag{3.14}$$

The first term on the right hand side of Equation (3.14) represents the contribution from the drift of finite op amp gain in the reference loop, whereas the second and third terms account for the drift of op amp gain A_1 and drift of conversion gain k_V of the core VCO, respectively. Again, their effects on the TC of frequency can be reduced by increasing the open loop gain for both loops. In practice, A_1, A_2, and k_V are functions of resistances or parasitic capacitances, which normally have TC's of several thousand ppm/°C. In other words, according to Equation (3.14) each term contributes only a few ppm/°C if both loops are designed with open loop gain of 1000 or more. Therefore, the effect of op amp finite gain is about an order of magnitude smaller than the effect of op amp offset voltages. Note that large open loop gain can only reduce the effects of errors in the forward path but not in the feedback path. As shown below, errors in the feedback path will be entirely reflected at the oscillation frequency of the closed-loop VCO.

3.5.3. Imperfect Tracking Between FVC's

So far the tracking between FVC's in the reference and control loop has been assumed perfect; the ratio, k, of the corresponding conversion gain k_f's is constant with temperature and other factors. Rather than constant, k may, however, be temperature dependent due to the thermal gradients across the chip, or the mismatch between devices caused by the limited resolution of the lithography and process-related gradients on the die. The effects of mismatch between FVC's on the linearity and TC of f_0 are now evaluated.

Figure 3.8 shows a block diagram of the closed-loop VCO with errors due to the imperfect tracking between FVC's. To model the effect, k_{f1} and k_{f2} are assumed to have different TC's, whereas everything else is ideal. The oscillation frequency is:

$$f_0 = \frac{k_{f1}}{k_{f2}} \left(\frac{V_{in}}{V_{ref}} f_R\right) \tag{3.15}$$

The accuracy of f_0 is related to the accuracy of the ratio of k_{f1} to k_{f2}, which in turn depends on the degree to which two passive components on the same die can be matched.

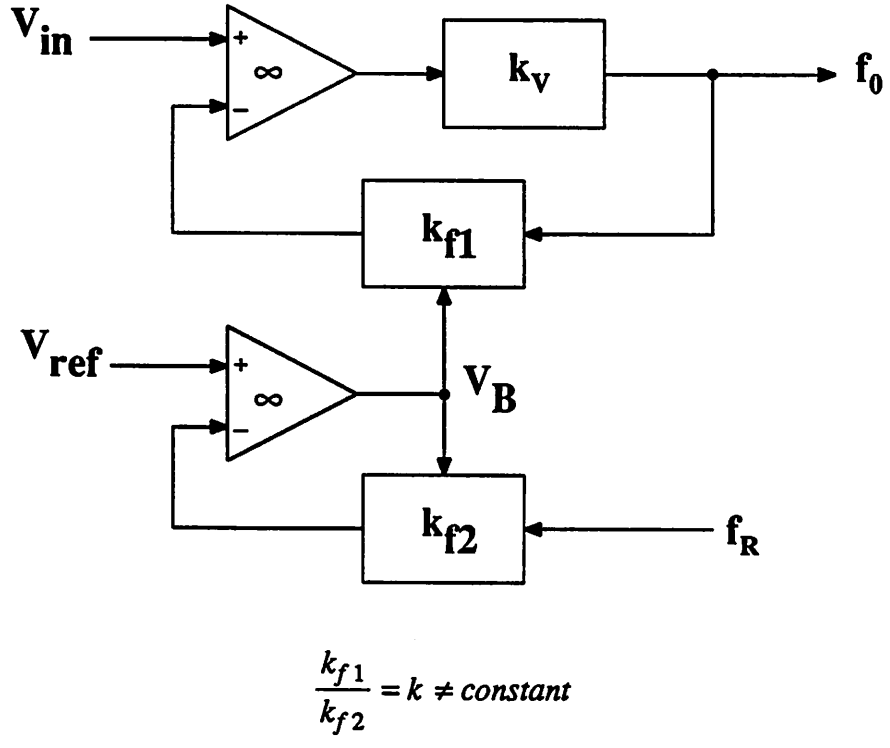


Figure 3.8 - Imperfect tracking effects

Therefore, the mismatch causes only inaccuracy in the oscillation frequency but not the nonlinearity error, if each FVC is ideally linear. Typically a mismatch of less than 0.5% at 3 σ over process variations can be achieved with current technology if components with large geometry are used. In other words, the mismatch between FVC's contributes about the same order of inaccuracy to f_0 as offest voltages.

The TC of f_0 can be obtained from Equation (3.15) as:

$$TC = \frac{1}{k_{f1}} \frac{\partial k_{f1}}{\partial T} - \frac{1}{k_{f2}} \frac{\partial k_{f2}}{\partial T} \tag{3.16}$$

Although it is simply the TC's difference in k_{f1} and k_{f2}, the TC of frequency cannot be estimated easily because the thermal gradient on the die is a complex function of layout, power consumptions, package, and so on, and is difficult to model accurately. To minimize the effects of imperfect tracking, two FVC's should be carefully laid out close to each other, particularly the crucial elements, and located on the isothermal lines, if possible. The often-used common centroid layout technique can be also applied to reduce the effects of both thermal and process-related nonuniform gradients to certain degree. With careful layout, the TC of f_0 due to the imperfect tracking between reference and control loop should be less than a few tens of ppm/°C.

3.5.4. Nonideal Voltage and Frequency References

The voltage and frequency references used in the reference loop provide the precision and temperature stability for f_0. In reality, both V_{ref} and f_0 are temperature dependent. Since a crystal oscillator can produce precisely the desired oscillation frequency with a very low TC, as discussed in Chapter 2, the voltage reference circuit usually limits the attainable precision and stability which the reference loop can furnish. This can be seen from the following equations for f_0 and its TC.

Interchanging the roles of k_{f1} and k_{f2} with the roles of f_R and V_{ref} in Equations (3.15) and (3.16), one has:

$$f_0 = (\frac{f_R}{V_{ref}})\, kV_{in} \tag{3.17}$$

and

$$TC = \frac{1}{f_R} \frac{\partial f_R}{\partial T} - \frac{1}{V_{ref}} \frac{\partial V_{ref}}{\partial T} \tag{3.18}$$

The accuracy of f_0 is limited by the accuracy of V_{ref} through Equation (3.17), while the TC of f_0 is directly connected to the TC of V_{ref} as indicated in Equation (3.18). The precision of V_{ref} relies on the

matching of transistors and resistors, and on the modeling of temperature dependence of device parameters such as V_{BE}. Normally V_{ref} can be accurate within 1% without trimming or external adjustment. As for the TC of V_{ref}, it depends on the voltage reference circuitry employed. If a first order bandgap reference is used to generate V_{ref}, a TC on the order of ±40 ppm/°C can be acquired. Compared with other sources of temperature drift, this is a significant component. Better TC performance is possible by means of laser trimming, or using a higher order bandgap reference.[30,31]

As a result, the typical TC of f_0 due to the temperature variations of nonideal references is several tens of ppm/°C, mainly from the voltage reference. Since a crystal oscillator can provide a very stable frequency reference, efforts should be concentrated on the design of the precision, temperature-stable voltage reference to minimize the effects of nonideal references.

3.6. Summary

Clearly, the purpose of using closed-loop VCO configurations is two fold. While the oscillation frequency is thermally stabilized through the use of the feedback loop, a linear voltage-to-frequency characteristic is also achieved regardless of the inherent nonlinearity of the core VCO, if an ideal FVC is used to perform linear frequency-to-voltage conversion. The reference loop used in the dual-loop feedback VCO monitors the variation of the FVC conversion gain k_f with temperature, process, and parasitics, and then corrects the resultant errors . As a consequence, a stable and well-defined k_f is obtained. This is particularly important for high frequency design because in practice, without the reference loop, k_f cannot be predicted accurately. Even if it can be found through computer simulations, k_f might deviate from the designed value due to process variations and parasitics. Since the use of the reference loop allows users to precisely define the desired k_f through reference voltage and frequency, the stability, linearity, and accuracy of oscillation frequency can be achieved simultaneously with closed-loop architectures.

This compensation technique can be applied to a oscillator which needs improvements in the stability, linearity, or accuracy of frequency. For example, the high frequency ring oscillator discussed in the previous chapter falls into this category. The ring oscillator allows very high frequency operation but requires stability with temperature and power supply in most practical applications, and good linearity if

used in FM demodulators. These problems can be eliminated by using the closed-loop architecture. Note that although the feedback element FVC determines the performance of the closed-loop VCO, the attainable frequency range of the closed-loop VCO is dependent upon the oscillation frequency range of the ring oscillator. Therefore, the ring oscillator must be designed to have a large frequency control range so that it would accommodate the oscillation frequency range imposed by Equation (3.17) over a certain specified range of V_{in}. Among other very high frequency oscillators which may require compensation is the emitter-coupled oscillator using parasitic capacitors as the timing capacitors. This has the potential of high speed operation above 1 GHz through the use of small parasitic capacitances to maximize the operating speed.[32] For such an oscillator, compensation is necessary because of the nonlinearity and strong temperature dependence of the parasitic capacitances which are used for timing.

The success of closed-loop VCO architectures is eventually hinged on the performance of pivotal elements, the FVC and op amp. The FVC has to be capable of operating at high frequencies with good linearity. The design of the FVC will be given in Chapter 4. On the other hand, the major limitation of the closed-loop VCO is that it requires a high speed op amp in the control loop to attain a wide bandwidth when the VCO is modulated by an input signal. Therefore, the useful modulation bandwidth of the closed-loop VCO is generally less than that of its counterpart open-loop VCO. For similar reasons, the jitter of the closed-loop VCO is not improved compared to the open-loop VCO. In fact, jitter originates primarily in the core VCO.

CHAPTER 4

INTEGRATED CIRCUIT REALIZATION

4.1. Introduction

As a test vehicle to demonstrate the feasibility of the closed-loop VCO architecture, a prototype based on the dual-loop feedback configuration described in Chapter 3 has been designed. The main targets in the design of a prototype were to achieve a TC of frequency less than ±100 ppm/°C and good linearity at oscillation frequencies higher than 100 MHz with the circuit operating from a single 5-V power supply. Also, the modulation bandwidth of the VCO should be at least 10 MHz when used in PLL receivers in applications such as demodulation of video signals from a 70MHz carrier in satellite communication. This chapter details the design of the prototype, including both the system and circuit design levels.

4.2. System Level Design

In the preceding chapter, we discussed the performance of the closed-loop VCO architecture, including the TC of frequency and the linearity of the voltage-to-frequency characteristic. The factors which limit the performance in each building block were also examined. However, those considerations were concentrated on the static situation. For the closed-loop VCO, which is a feedback system, we should further explore the dynamic behavior since it requires some unique design considerations, such as the loop stability, speed of response, and ripple effects, which are absent in the conventional VCO. In this section, we analyze the dynamic response of the control loop and then specify the related parameters in order to satisfy the requirements imposed by applications. These parameters, specified in the static or dynamic case, will be taken into account in the design of the closed-loop VCO prototype.

As discussed in Chapter 3, the VCO with dual-loop feedback is superior to the VCO with single-loop feedback due to the difficulty of designing a linear analog multiplier with a low offset voltage. Therefore, the VCO prototype adopts the dual-loop feedback configuration. Since the reference loop is primarily for temperature compensation, only the dynamics of control loop are analyzed. The result can

be, however, extended to the reference loop to find the stability condition, as well as others if necessary.

4.2.1. Loop Dynamic Response

Let us first consider the control loop as shown in Figure 4.1.

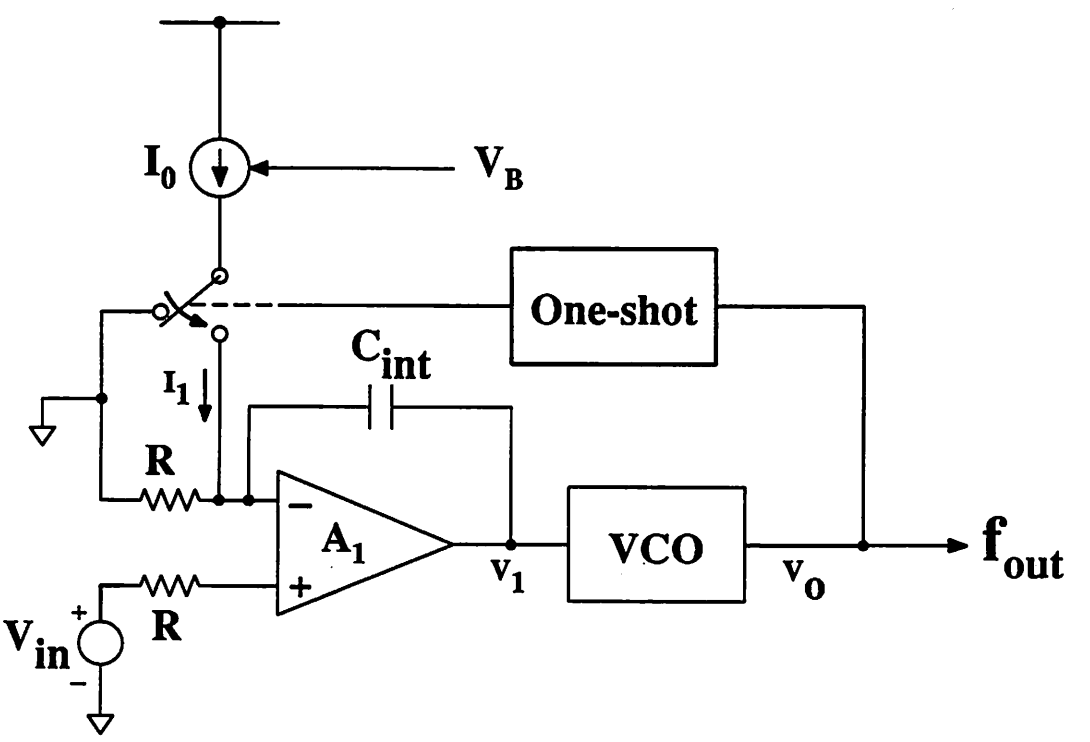


Figure 4.1 - Control loop schematic

This is basically identical to the control loop shown in Figure 3.5 except that the conceptual FVC is now replaced by its actual realization, which consists of a one-shot section, current switch section, and R-C filtering section, as illustrated in Figure 3.3. Note that the integrating capacitor C_{int}, instead of shunting the inverting node of the op amp as suggested by Figure 3.3, is connected between the output and inverting input of the op amp to act as an active low pass integrator by taking advantage of the op amp which is already present in the loop. The various waveforms in the control loop of the closed-loop VCO are shown in Figure 4.2. It turns out that the equation governing the dynamics of the loop, i.e., the output frequency f_{out} and input control voltage V_{in}, is a *nonlinear difference equation* and can only be solved

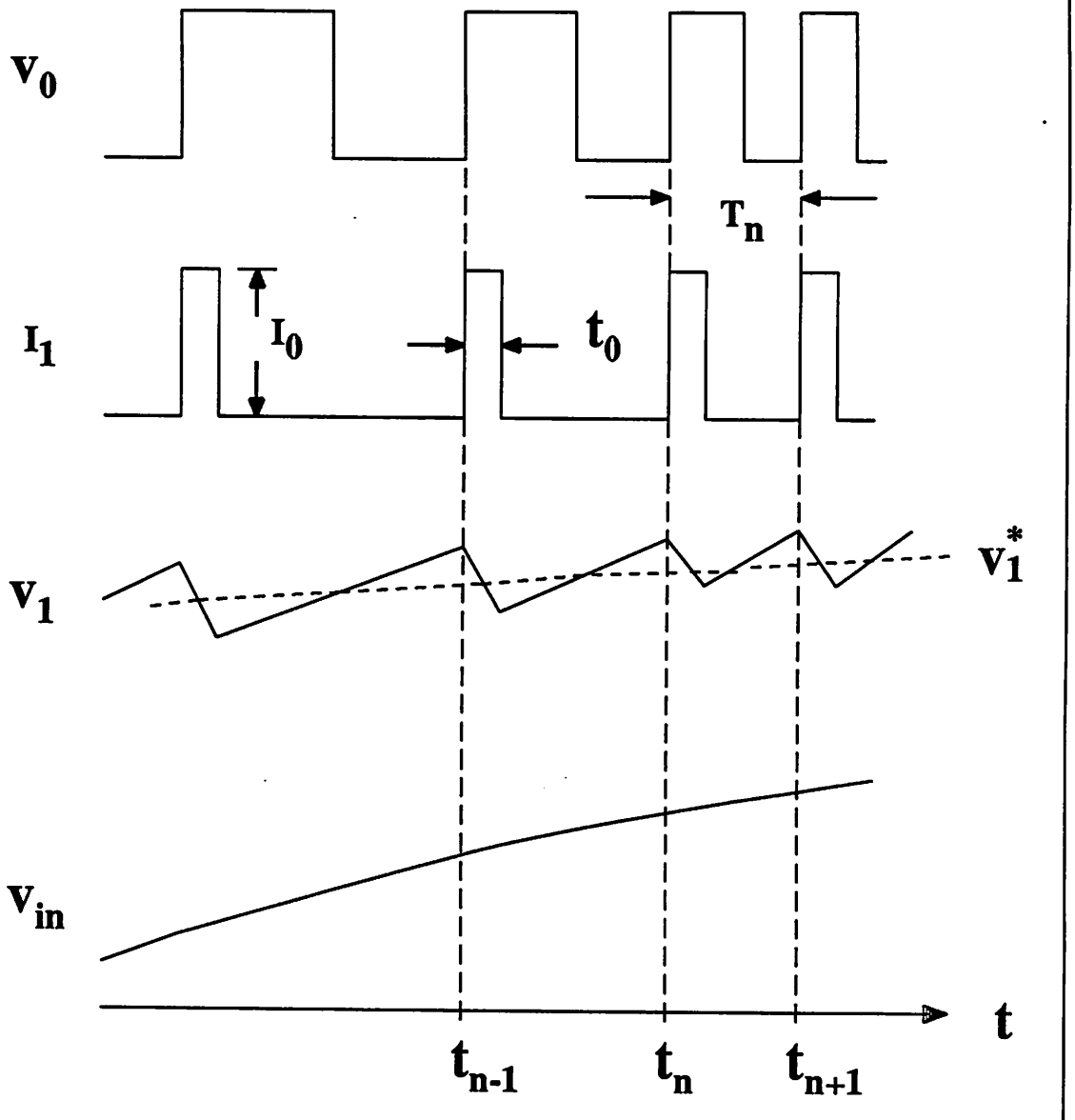


Figure 4.2 - Waveforms within the control loop

numerically. This is detailed in Appendix 1.

In order to obtain insight into the operation of the loop and overcome the mathematical difficulties, some approximations have to be made to obtain a simplified analytic form for f_{out} in terms of V_{in} and other parameters. This is important because the effect of each parameter can be understood and taken into consideration in the circuit design phase. If the op amp is initially assumed ideal, then the equations

describing the dynamics of the loop in Figure 4.1 are:

$$C_{int}\frac{d}{dt}(v_1 - V_{in}) + I_1 = \frac{V_{in}}{R} \tag{4.1}$$

and

$$f_{out} = k_V v_1^* = k_V \frac{\int_{-\infty}^{t} v_1\, dt}{\int_{-\infty}^{t} dt} \tag{4.2}$$

where v_1^* *is the average value of* v_1 and k_V *is the VCO gain.*

If the maximum input frequency is much less than the VCO oscillation frequency f_{out}, Equation (4.1) can be approximated as:

$$C_{int}\frac{d}{dt}(v_1^* - V_{in}) + I_0 t_0 f_{out} = \frac{V_{in}}{R} \tag{4.3}$$

Combining Equations (4.2) and (4.3) and now including the finite op amp gain $A_1(s)$, we obtain the loop dynamic equation in the frequency domain:

$$sC_{int}\left[\left[1 + \frac{1}{A_1(s)}\right]\frac{f_{out}}{k_V} - V_{in}\right] + I_0 t_0 f_{out} = \frac{V_{in} - \dfrac{f_{out}}{A_1(s)k_V}}{R} \tag{4.4}$$

The term $\dfrac{f_{out}}{A_1(s)k_V}$ in Equation (4.4) accounts for the finite voltage across the inputs of the op amp. The loop transfer function then is:

$$\frac{f_{out}}{V_{in}} = \frac{1}{k_f}\frac{1 + sC_{int}R}{1 + \dfrac{1}{A_1(s)k_V k_f} + s\left[\left[1 + \dfrac{1}{A_1(s)}\right]\dfrac{RC_{int}}{k_V k_f}\right]} \tag{4.5}$$

where $k_f = I_0 t_0 R$

Therefore the loop has a feedforward zero, $\dfrac{1}{RC_{int}}$, and a single pole,

$$P_a = \frac{k_V k_f}{RC_{int}} \tag{4.6}$$

for infinite op amp gain. If the zero is removed by intentionally introducing a pole at the input through another capacitor with the same capacitance as C_{int} shunting the noninverting node of the op amp, the -3-db bandwidth (also called the modulation bandwidth) of the closed-loop VCO can be made large by choosing a small time constant RC_{int} and large $k_f k_V$. Unfortunately, in practice the modulation bandwidth is limited by the stability requirement and finite gain-bandwidth product of the op amp, and ripple at the input of the core VCO. The limitation on the modulation bandwidth due to the stability requirement and ripple will be discussed in the following sections. We now examine the effect of limited op amp gain-bandwidth product.

Consider an op amp whose gain transfer function contains two dominant real poles

$$A_1(s) = \frac{A_0}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})} \tag{4.7}$$

Where A_0 is the low-frequency gain of the op amp

Substituting Equation (4.7) into (4.6) yields:

$$\frac{f_0}{V_{in}} = \frac{\frac{1}{R} + sC_{int}}{b_0 + b_1 s + b_2 s^2 + b_3 s^3} \tag{4.8}$$

where

$$b_0 = I_0 t_0 + \frac{1}{A_0 k_V R} \tag{4.8a}$$

$$b_1 = \left[1+\frac{1}{A_0}\right]\frac{C_{int}}{k_V} + \frac{p_1+p_2}{A_0 k_V R\, p_1 p_2} \tag{4.8b}$$

$$b_2 = \frac{C_{int}(p_1+p_2)}{A_0 k_V p_1 p_2} + \frac{1}{A_0 k_V R\, p_1 p_2} \tag{4.8c}$$

$$b_3 = \frac{C_{int}}{A_0 k_V p_1 p_2} \tag{4.8d}$$

If $A_0 \gg 1, p_1 \gg p_2$, and the loop is stable, then Equation (4.8) can be simplified and rewritten as:

$$\frac{f_0}{V_{in}} = \frac{1}{k_f}\left[1 - \frac{1}{A_0 k_V k_f}\right] \frac{(1+\frac{s}{z_a})}{(1+\frac{s}{p_a})(1+\frac{s}{p_b})(1+\frac{s}{p_c})} \tag{4.9}$$

where

$$z_a = \frac{1}{RC_{int}} \tag{4.9a}$$

$$p_a = \frac{k_V k_f}{RC_{int}} \frac{1}{1+\frac{1}{A_0 p_1 R\, C_{int}}} \tag{4.9b}$$

$$p_b = A_0 p_1 \frac{1+\frac{1}{A_0 p_1 R\, C_{int}}}{1+\frac{1}{p_2 R\, C_{int}}} \tag{4.9c}$$

$$p_c = p_2 + \frac{1}{R\, C_{int}} \tag{4.9d}$$

Again, assuming that zero z_a is taken away by inserting a pole at the input and p_a is the dominant pole, the modulation bandwidth of the closed-loop VCO with a nonideal op amp is reduced by a factor of $1 - \frac{1}{RC_{int}\omega_u}$ compared to the ideal case, where $\omega_u \equiv A_0 p_1 =$ op amp gain-bandwidth product. Therefore, ω_u, also the op amp unity-gain frequency, should be made much greater than $\frac{1}{RC_{int}}$ associated with the integrator section so that the modulation bandwidth approaches the ideal value as indicated in Equation (4.6). In addition, Equation (4.9) reveals that the low-frequency gain of the closed-loop VCO is also reduced by a factor of $1 - \frac{1}{A_0 k_V k_f}$ due to the limited low-frequency gain of the op amp A_0.

One may attempt to broadband the modulation bandwidth by decreasing the time constant RC_{int} according to Equation (4.9b). However, this also makes p_a no longer a dominant pole since $p_a \sim p_b \sim \omega_u$, and thus the effective bandwidth is less than predicted. To make matters worse, small RC_{int} could even result in instability in the control loop, in addition to a large ripple present at the op amp output which will affect the duty cycle of the VCO output waveform. We examine the stability requirement first.

4.2.2. Loop Stability

The stability of the control loop of the closed-loop VCO can be determined by the Routh-Hurwitz criterion used to find the necessary and sufficient condition that all roots of the characteristic equation lie in the left of the s–plane without actually solving for the roots.[33] Applying Routh's test to the denominator in Equation (4.8) produces the necessary and sufficient condition that the control loop is stable:

$$b_1 b_2 > b_3 b_0 \tag{4.10}$$

since all b_i's, $i = 0,1,2,3$ are positive. Again, assuming $A_0 \gg 1$ and $p_1 \ll p_2$, then Equation (4.10) becomes:

$$\frac{k_f k_V}{RC_{int}} < \left(1 + \frac{1}{A_0 p_1 R\, C_{int}}\right)\left(p_2 + \frac{1}{RC_{int}}\right) \tag{4.11}$$

To attain a stable control loop, the relationship among the parameters in the op amp, FVC, and core VCO as specified in Equation (4.11) must be satisfied. As a consequence, Equation (4.11) can be used as a guide in the circuit design to determine the range of certain parameters in the loop if others are known. For example, the value of RC_{int} has a lower bound imposed by the loop stability requirement. In comparison of Equations (4.11) with (4.9b), we see that the maximum attainable p_a, if it is still the dominant pole, is limited to $p_2 + \frac{1}{\tau_{min}}$, where τ_{min} is the corresponding minimum time constant RC_{int} for a stable loop. Loosely speaking, the modulation bandwidth is thereby limited by the gain-bandwidth product of the op amp if the op amp is designed with $p_2 = A_0 p_1$.

The stability requirement for the reference loop can be obtained in a similar way. Figure 4.3 shows the reference loop, which differs from the control loop in that the the adaptive bias voltage V_B generated by the op amp linearly controls the magnitude of the integration currents of FVC's in both loops. In addition, a constant reference frequency f_R is fed to the one-shot, whose output then controls the duration of integration in each cycle. The constant k provides a larger conversion gain for the reference loop which normally operates in the lower frequency range than the control loop, as described in the previous chapter.

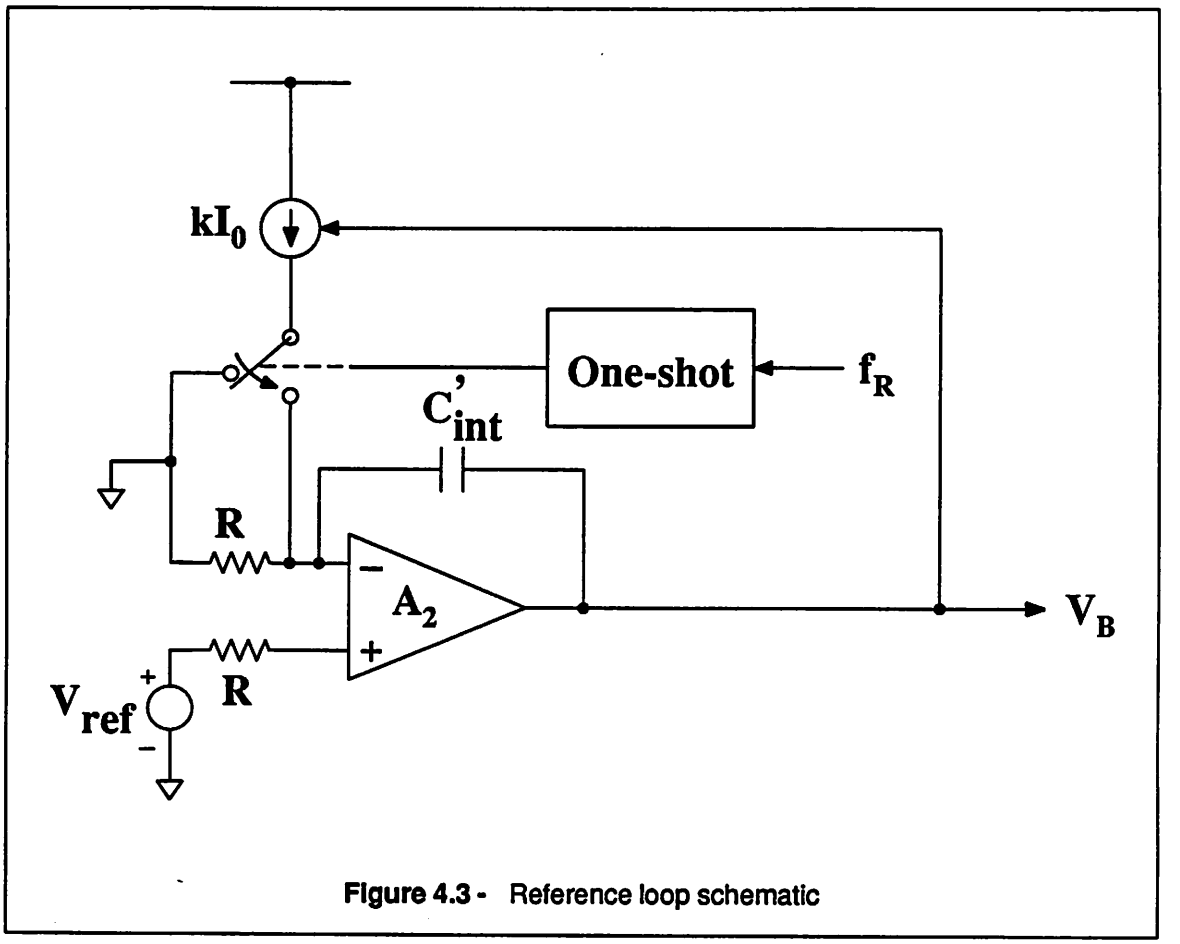


Figure 4.3 - Reference loop schematic

Obviously, if $k_V = 1$ and $I_0 t_0 = kg_R t_0 f_R$, then the control loop and reference loop are equivalent, where g_R represents the small signal gain of $\frac{I_0}{V_B}$. Therefore, the condition that the reference loop is stable can be found directly from Equation (4.11):

$$\frac{kg_R t_0 f_R}{C'_{int}} < \left(1 + \frac{1}{A_0 p_1 RC'_{int}}\right)\left(p_2 + \frac{1}{RC'_{int}}\right) \tag{4.12}$$

if op amp A_2 is identical to the op amp A_1 in the control loop. Unlike the control loop, the reference loop can use an integration capacitor C'_{int} as large as possible since there is no limitation on its bandwidth. As a consequence, stability usually is not a concern for the reference loop. In fact, a large value of C'_{int} should be used to minimize the ripple voltage at the output of the integrator, which may alternate the duty cycle of the VCO output waveform through the integration current in the control loop.

4.2.3. Effects of Ripple on VCO Waveform

Because the control loop is required to provide a wide modulation bandwidth in some applications, such as the demodulation of FM video signals from a 70 MHz IF carrier in a satellite PLL receiver, it is necessary to keep C_{int} small enough to allow the desired signal passing through without attenuation to modulate the VCO. In the mean time, there is a small ac ripple voltage superimposed on the ideally desired VCO input, due to the small value of C_{int} used. Although the oscillation frequency is not affected by the ripple and still exhibits the desired linear dependence on V_{in} since only the *average value* at the op amp output matters in determining frequency, the instantaneous charge/discharge currents in the core VCO vary from one half cycle to the other due to the presence of ripple, and therefore cause a fluctuation in the duty cycle of the oscillation. We now calculate the duty cycle of the oscillation under the influence of a small ripple at the core VCO input.

For simplicity, we assume a constant control input V_{in}, and therefore a fixed output oscillation frequency. Referring to Figure 4.2, we can calculate the peak-to-peak ripple voltage Δv_1 of the integrator output by estimating the integration current during the time interval $(t_n, t_n + t_0)$ since $v_1(t_n) = v_1(t_{n+1})$ in the steady state. Because the VCO oscillation frequency is normally less than the op amp unity gain frequency, it can be shown that the current sourced by the op amp through C_{int} in that time interval is

$$I_{int} = I_0 t_0 (1 - t_0 f_0) \tag{4.13}$$

Consequently, the peak-to-peak ripple voltage at the input of VCO is:

$$\Delta v_1 = \frac{I_0 (1 - t_0 f_0) t_0}{C_{int}} \tag{4.14}$$

Note that the ripple is also periodic with the same frequency as the VCO output. Therefore, its presence does not influence the average of v_1, and the consequent VCO oscillation frequency. However, the ripple does affect the average switching current in each half cycle of the oscillation and this results in unsymmetric VCO waveforms. For a relaxation oscillator such as described in chapter 2, the duty cycle of VCO output is thus half the ratio of the average current in the half cycle of oscillation to the average current in one period of oscillation. More precisely, the duty cycle D_v of the closed-loop VCO is

$$D_V = \frac{I_t \pm \frac{g_m \Delta v_1}{4}}{2I_t} \tag{4.15}$$

where I_t is the average current in the timing capacitor of VCO, g_m is the voltage-to-current conversion gain for the VCO, and Δi_t is the peak-to-peak variation of I_t, since the integrator output waveform is sawtooth-like. Substituting Equation (4.14) into (4.15) and using $I_t = 2C_t V_s f_0$ from Equation (2.9), we obtain:

$$D_V = \frac{1}{2} \pm \varepsilon_{error} \tag{4.16}$$

$$where \ \ \varepsilon_{error} = \frac{k_f k_V (1 - t_0 f_0)}{2RC_{int} f_0}$$

The second term in the right side of Equation (4.16) represents the percentage deviation of the VCO duty cycle from the ideal value 50%. For example, in the prototype closed-loop VCO, $k_f k_v = 2$, $t_0 = 2\,nS$, $f_0 = 200\,MHz$, $R = 2\,K\Omega$, and $C_{int} = 20$ pF, the corresponding ε_{error} is 3.7%. Computer simulations show an error of 2% in the duty cycle of the closed-loop VCO using the above parameters. The reason why the actual error in the duty cycle is less than predicted is that at oscillation frequencies near the op amp unity gain frequency, the ripple at the integrator output is less than predicted by Equation (4.14) due to the fall-off of the op amp gain. The duty cycle error can be reduced by choosing a larger value of C_{int} or decreasing $k_f k_V$. Unfortunately, examination of Equations (4.9b) and (4.16) reveals that the duty cycle error ε_{error} of the closed-loop VCO is proportional to the modulation bandwidth of the closed-loop VCO, namely,

$$\varepsilon_{error} = \frac{p_a}{2f_0}(1 - t_0 f_0) \tag{4.17}$$

Therefore, one has to trade the modulation bandwidth of the closed-loop VCO for the error in the duty cycle of the VCO output waveform in applications where a precise 50% duty cycle is important. One example is the PLL using the analog multiplier as a phase detector. Any VCO duty cycle error will be reflected as the phase error between the input signal and VCO output. To this end, the ripple should be

kept low to minimize the phase error.

Equation (4.17) also shows that for a fixed modulation bandwidth, ε_{error} is inversely proportional to the VCO oscillation frequency. This is due to the fact that as f_0 approaches the modulation bandwidth, it is more difficult for the integrator, acted as a first-order low-pass filter, to distinguish the "signal" from the ripple. To remedy this problem, a more sophisticated high-order low-pass filter may be used to attain a sharper transition band, and in addition, to give more latitude in optimizing the modulation bandwidth and ripple effects. However, this may cause loop stability problems because of the extra phase shifts introduced into the loop.

In addition to the duty cycle error, the presence of ripple also affects the performance of the op amp. Due to the limited op amp gain, the voltage at the inverting node of the op amp in Figure 4.1, v_-, is not constant but has a small ripple on it. If not designed carefully, the op amp may be overloaded by the ripple and thus operate in a nonlinear region. This will severely degrade the performance of the closed-loop VCO due to the decrease of the op amp gain and the increase of the offset voltage. Such effects are particularly prominent at higher frequencies. Computer simulations should be extensively used to help determine the ripple voltage at the high oscillation frequencies. The design of the op amp to overcome the input ripple will be described later in this chapter. After examing the system level design issues, we now examine circuit design, starting with the design of the frequency-to-voltage converter (FVC).

4.3. Frequency-to-Voltage Converter

This is an important part of the closed-loop VCO architecture since it dictates the linearity, high-frequency capability, and the modulation bandwidth of whole VCO. We examined the relationship between the modulation bandwidth and FVC parameters k_f and RC_{int} in the preceding section. The limitations on the linearity and high-frequency capability of the FVC are addressed herein.

As discussed in Section 3.3 of the preceding chapter, aside from an integrator, the FVC consists of an one-shot (monostable) circuit, and a switched current source whose current I_0 can be adjusted through a voltage. The one-shot circuit generates a pulse train with fixed pulse width t_0 when triggered by the rising edges of a periodic input signal f_{in}. The integration time of the current source is controlled by the

duration t_0 of the one-shot circuit output. Figure 4.4 shows the realization of the FVC, excluding the integrator.

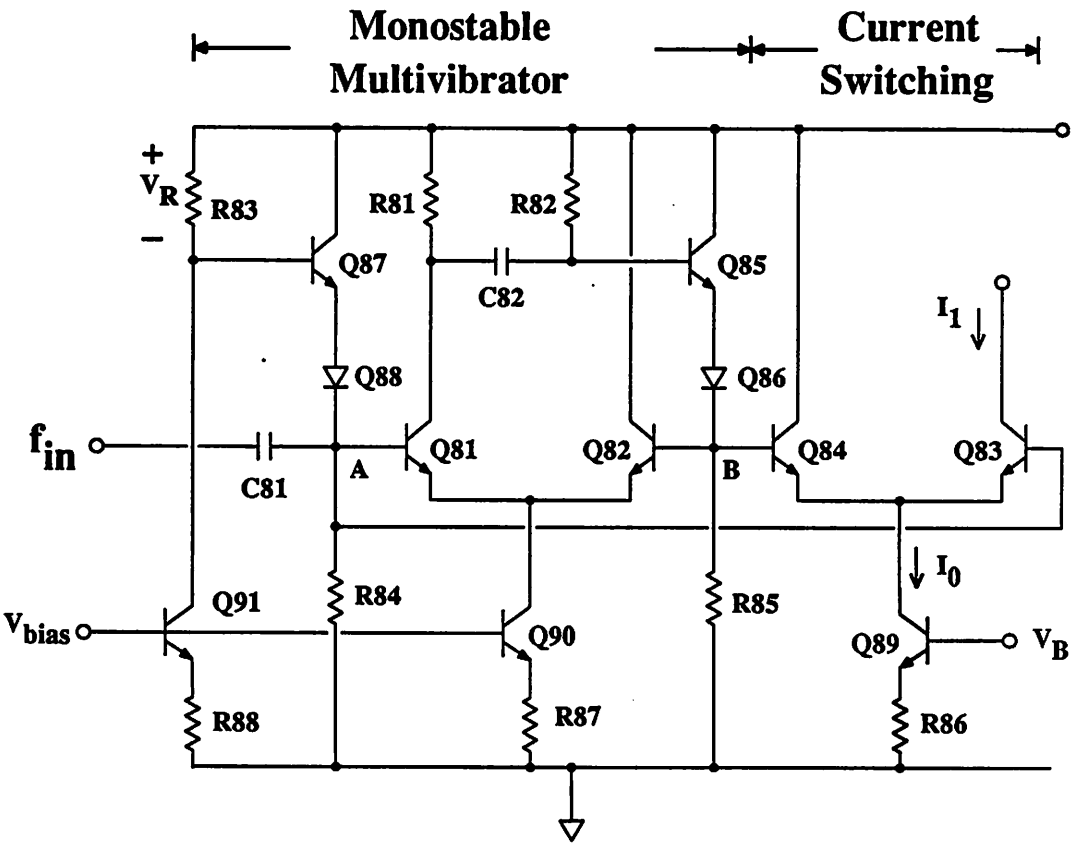


Figure 4.4 - Simplified circuit schematic of FVC

The current switching section is nothing but a high speed emitter-coupled differential pair consisting of transistors Q_{83} and Q_{84}, and a current source whose current I_0 is controlled by the adaptive bias voltage V_B generated in the reference loop. Note that Q_{83}–Q_{84} is a duplicate differential pair of transistors Q_{81}–Q_{82} in the one-shot section, and hence the output current for integration I_1, taken from the collector of Q_{83}, is simply the replica of the current in the collector of Q_{81}, I_{C81}. However, this is necessary since I_{C81} is not available for integration, arising from its being in the regeneration loop of the one-shot section. Ideally, I_1 is switched alternatively between 0 and I_0 with the same turn-on time t_0 as Q_{81}, which is determined solely by the one-shot section. In other words, two important parameters for the FVC, I_0 and

t_0, are determined by the current switching and one-shot sections, respectively. We now focus on the one shot section since it actually dictates the linearity and high-frequency capability of the FVC.

The one-shot section shown in Figure 4.4 is a well-known emitter-coupled monostable multivibrator.[34] This is essentially a positive feedback circuit which contains one stable state and one quasi-stable state. When triggered by the external signal f_{in}, the circuit is excited to the quasi-stable state through the regeneration. It remains in its quasi-stable state for a period of time t_Q before it returns to its original stable state to complete one cycle of the transition. Let us assume that it takes finite time t_{SQ} and t_{QS} for the circuit to make transitions from the stable state to the quasi-stable state and vice versa, respectively. The pulse width t_0 can then be approximated as the sum of t_Q and average value of t_{SQ} and t_{QS}. Before estimating the parameter t_0, let us first examine the operation of the circuit.

Transistors Q_{81} and Q_{82} convert the differential voltage $V_A - V_B$ across their bases to signal current in the collector of Q_{81} when the regeneration takes place, while the resistors R_{81} and R_{82} are used as the load to attain enough loop gain. Transistors Q_{85} and Q_{86} form the emitter follower to accomplish the level shift and feedback from the collector of Q_{81} to the base of Q_{82}. The base of Q_{81} is biased at a voltage of V_R lower than the base voltage of Q_{82}, through the biasing circuitry consisting of transistors Q_{87} and Q_{88}, resistors R_{83} and R_{84}, and current source Q_{91}. The voltage V_R, derived from an on-chip bandgap reference voltage through Q_{91} and R_{83}, should be chosen large enough so that the residual current in Q_{81} is negligible compared to the tail current of the differential pair Q_{81}–Q_{82} when the circuit is in its stable state. This is important because any residual current will be reflected to I_1 and results in errors in the frequency-to-voltage conversion. On the other hand, if V_R is too large, the circuit either never has the chance to be excited to its quasi-stable state when triggered by the external signal, or stays in the quasi-state for a very short of time with differential pair Q_{81}–Q_{82} never being fully turned on or turned off. In either case, the conversion gain k_f of the FVC is greatly reduced, and this literally makes the closed-loop VCO architecture futile because of lack of the loop gain. Note that a leakage current of less than 0.1% of the tail current can be attained if the differential voltage at an emitter-coupled pair exceeds $V_T \ln 1000 \sim 180\,mV$. In the prototype, V_R is set to about 200 mV.

Q_{81} and Q_{83} are normally off and essentially conduct zero currents for a large V_R. As the input f_{in} rises rapidly (the rising edge of the VCO output) to turn on Q_{81} through the on-chip MOS capacitor C_{81}, Q_{82} is turned off quickly as a result of regeneration action. Q_{83} and Q_{81} remain conducting currents for only a finite time t_Q because the base of Q_{85} is connected to V_+ through the resistor R_{82}. Therefore V_B will rise with a time constant $(R_{81}+R_{82})C_{82}$, and when it approaches V_A within a small voltage V_σ where the open loop gain is unity, a regeneration will take place, turning Q_{81} off and eventually returning the monostable multivibrator to its initial state. C_{82} is another on-chip coupling capacitor to insure high frequency operation.

Referring to the waveforms of the one-shot circuit as shown in Figure 4.5 and neglecting the transition times t_{SQ} and t_{QS},

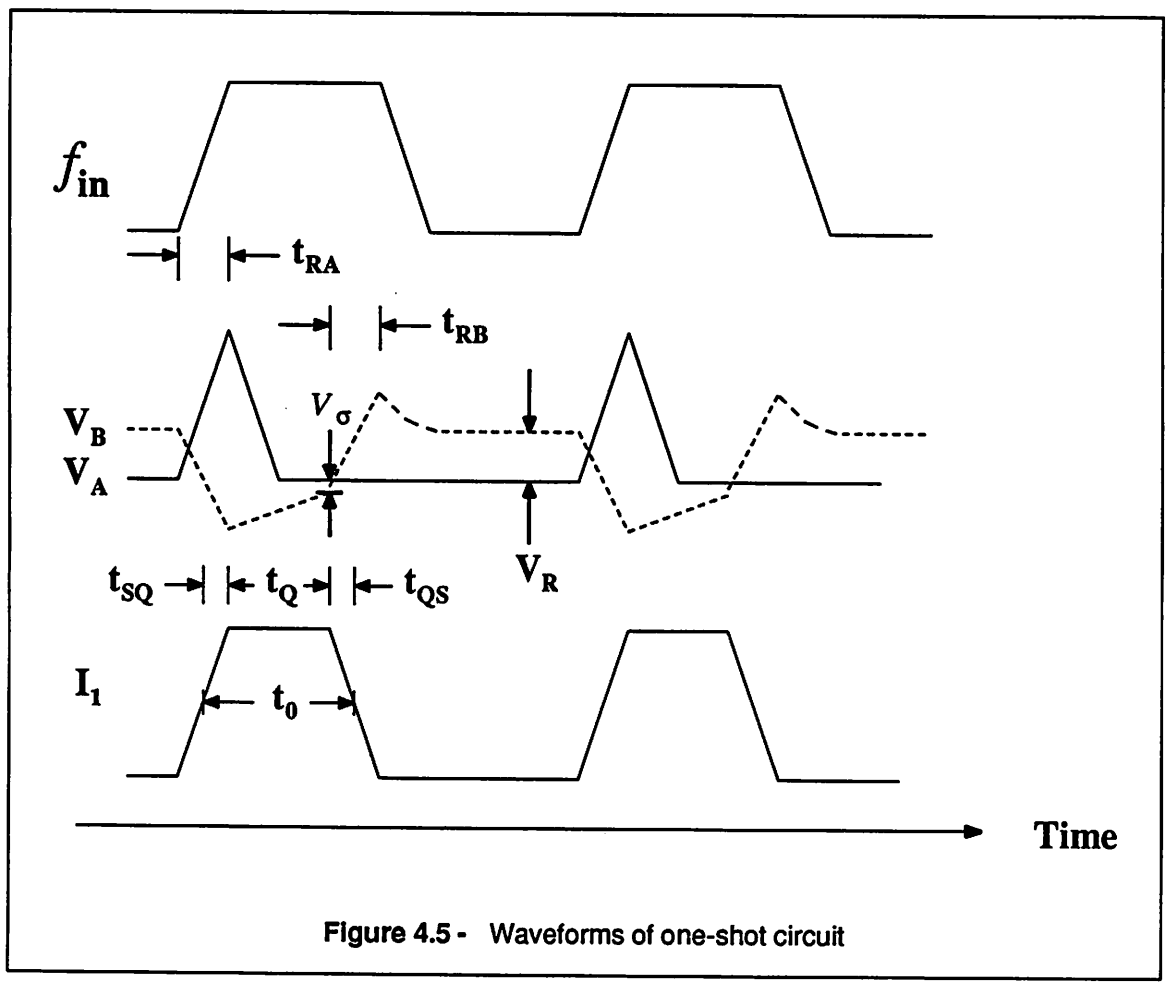


Figure 4.5 - Waveforms of one-shot circuit

t_Q can be approximated as

$$t_Q = (R_{81} + R_{82})C_{82} \ln\left[\frac{\Delta V}{V_R + V_\sigma}\right] \tag{4.18}$$

where $\Delta V = I_{C90}(R_{81} \,||\, R_{82})$ and I_{C90} *is the tail current in the current source* Q_{90}

Therefore, to the first order, t_0 is linearly proportional to the value of C_{82} and related to V_R through the log function. For the prototype, $R_{81} = R_{82} = 500\ \Omega$, C_{82}= 1.5 PF, V_R = 200 mV, I_{C90} = 1.5 mA, and V_σ = 60 mV, the calculated t_Q is 0.95 nS, being a good agreement with the result of circuit simulation program SPICE.[35] We now have to include t_{SQ} and t_{QS} to complete the estimation of t_0. It is very difficult to get an analytic form similar to Equation (4.18) for each transition time because of nonlinearities of the active devices involved in the transient. Therefore, approximations have to be used to simplify the analysis. Note that t_{SQ} is only related to the waveform of the input f_{in} since the time constant associated with the node A is small compared with the rise time t_{RA} of the input, as a result of the low impedance seen looking into the diode Q_{88} and emitter follower Q_{87}. In other words, V_A can follow the change of f_{in} instantly. Therefore, t_{SQ} is related to t_R and can be approximated as

$$t_{SQ} = \frac{t_{RA}}{2} \tag{4.19}$$

if we assume the regeneration occurs at the middle point of the transition. On the other hand, t_{QS} is involved with the waveform of V_B after the regeneration take places, and hence can be expressed as

$$t_{QS} = \frac{t_{RB}}{2} \tag{4.20}$$

where t_{RB} is the rise time for the waveform V_B. Combining Equations (4.18), (4.19), and (4.20), we obtain

$$t_0 = \tau \ln K + \frac{t_{RA}}{2} + \frac{t_{RB}}{2} \tag{4.21}$$

where $K = \dfrac{\Delta V}{V_R + V_\sigma}$ and $\tau = (R_{81} + R_{82})C_{82}$. Computer simulations shows that $t_{RA} \sim t_{RB} \sim 1\ nS$ and t_0 is approximately equal to 2 nS. In order to keep t_0 a constant at different input frequencies to achieve a

linear frequency-to-voltage conversion, a constant rise time t_{RA} is therefore essential for the FVC. This can be accomplished by inserting a high-speed differential gain stage between the core VCO and FVC to equalize the VCO output rise time before triggering the FVC.

The linearity of the FVC is limited by two different mechanisms. At low input frequencies, it is limited by the leakage current of I_1 which is a significant part of the signal current. At high frequencies, the linearity is degraded due to the fact that both waveforms V_A and V_B do not have enough time to settle to the same values attained at low frequencies, causing the variations in both t_0 and I_0, or equivalently the conversion gain k_f. To minimize the linearity error, t_0 should be kept low while maintaining a constant product of $I_0 t_0$ to the extent that the high frequency capability of transistors are not significantly degraded, in addition to reducing the residual current.

As for the high-frequency capability of the FVC, again, t_0 is the pivotal parameter. The maximum attainable input frequency for an FVC is

$$f_{in,max} = \frac{1}{2t_0} \tag{4.22}$$

because when the half cycle of the input signal is less than t_0, the negative going edges may prematurely trigger the regeneration, and therefore shorten the time elapsed in the quasi-stable state t_Q. As a result, at high frequencies the pulse width t_0 is not constant with the input frequency but instead tracks the period of input. In other words, the output of the FVC approaches a constant value of $\frac{I_0 R}{2}$ at high frequencies. The behavior of the FVC with f_{in} is illustrated in Figure 4.6. The decline in the output voltage at high frequencies is due to the same mechanism that causes the linearity error in the frequency-to-voltage conversion at high frequencies as described above.

4.4. Operational Amplifier

The op amp plays a very important role in the closed-loop architecture since the performance of the compensated VCO, including the TC of frequency, linearity of frequency control characteristic, and modulation bandwidth of the input control signal, are directly connected with the op amps used in the

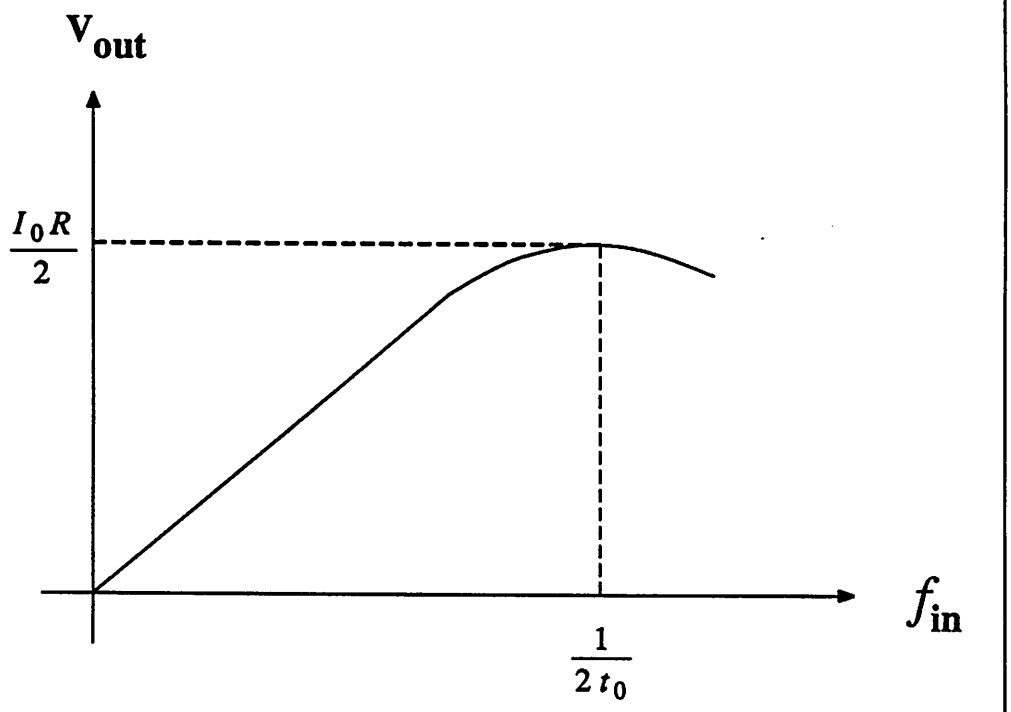


Figure 4.6 - FVC transfer function

feedback loops. As a result, a high performance op amp is needed to achieve a moderate low-frequency gain (>60 db),very high unity-gain frequency, adequate phase margin (>60°), and low input offset voltage. In addition, the op amp should be simple, not taking too much power and chip area. The preceding requirements for the op amp lead to the use of a double-cascode single-stage configuration with continuous time common-mode feedback. Figure 4.7 shows the simplified circuit of the op amp. The SPICE simulation shows that an open-loop gain of 61 dB, unity-gain frequency $f_u = 250$ MHz, and phase margin $\phi_M = 80°$ are attained for the op amp.

The operation of the op amp is described as follows. In order to achieve a gain more than 1000 in one stage, double-cascode *pnp* current sources Q_{27}, Q_{28}, Q_{29}, and Q_{30} are used as active loads. However, no differential to single-ended conversion is allowed because of the poor frequency response of *pnp* transistors. For this reason, the op amp outputs have to be taken differentially, and therefore a common-mode feedback circuit is needed to help define the common-mode voltages at the high impedance nodes at the collectors of $Q_{25} - Q_{28}$. A simple, all-*npn* transistor common-mode feedback circuit, composed of

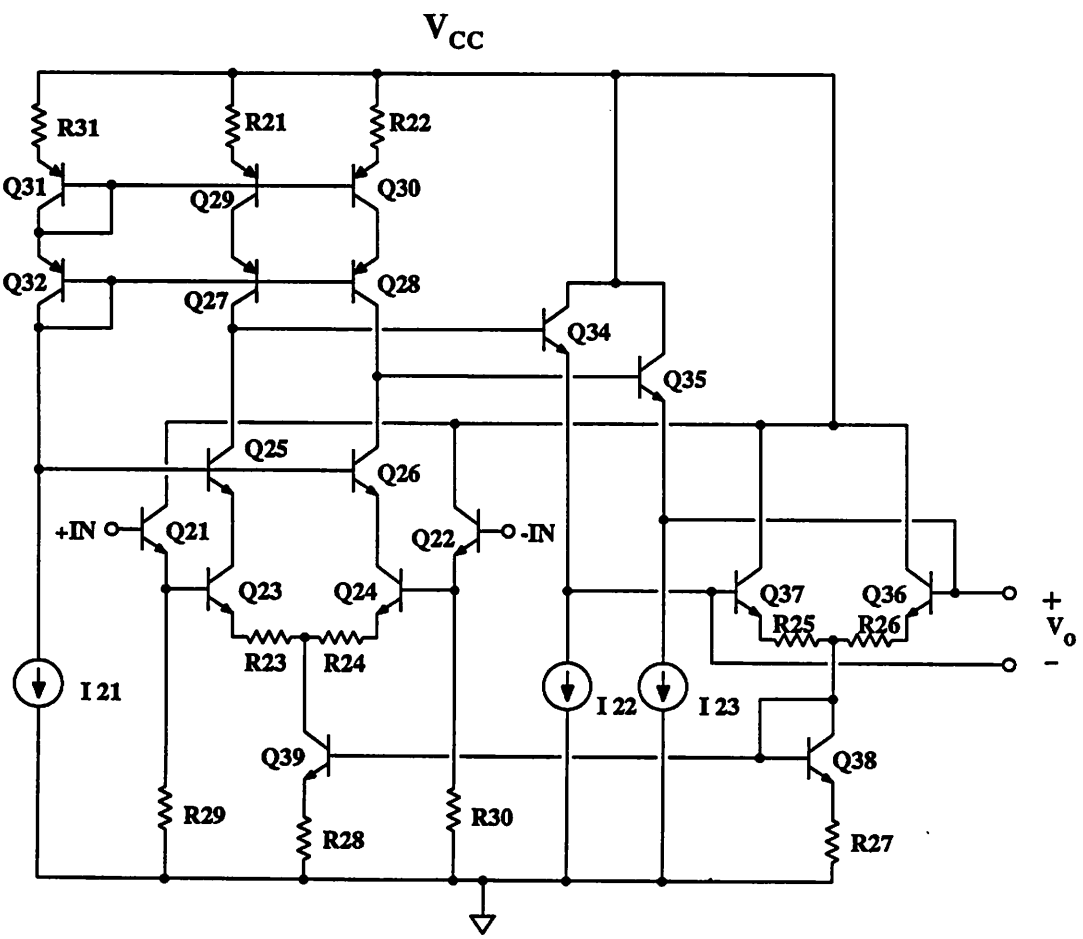


Figure 4.7 - Circuit diagram of op amp

transistors $Q_{36} - Q_{39}$ and resistors $R_{25} - R_{28}$, can provide fast settling time for the common-mode voltage, which is well defined at a voltage V_{com} such that the current I_{C39} in Q_{39} is twice the bias current I_{21} if all base currents are neglected and all *pnp* transistors are identical. R_{25} and R_{26} are used to extend the linear range of common-mode feedback circuit.

Similarly, emitter degeneration resistors R_{23} and R_{24} provide enough room to accommodate the ripple present at the op amp input, especially for the VCO with a wide modulation bandwidth. The low-frequency gain of the op amp can be written as[28]

$$A_0 = \frac{g_{m23}}{1 + g_{m23}R_{23}}\beta_{pnp}r_{o27} \tag{4.23}$$

$$where\ g_{m23} = \frac{I_{C23}}{V_T}\ and\ r_{o27} = \frac{V_{A,pnp}}{I_{C27}}$$

since the current gain β_{npn} and Early voltage $V_{A,npn}$ for *npn* transistors are normally much greater than their *pnp* counterparts, β_{pnp} and $V_{A,pnp}$. Note that the parasitic capacitances at the high impedance nodes serve as the compensation capacitances and, along with the high impedance, give rise to the first dominant pole at

$$p_1 = \frac{1}{\beta_{pnp}r_{o27}C_{\mu 27}} \tag{4.24}$$

$$where\ C_{\mu 27}\ is\ the\ base\text{-}collector\ capacitance\ of\ Q_{27}$$

since C_μ of pnp transistor is typically several times C_μ or the collector-substrate capacitance C_{sb} of the high-frequency *npn* transistor. Assuming the single-pole roll-off, the unity gain frequency of the op amp can be found

$$f_u = \frac{\omega_u}{2\pi} = \frac{1}{2\pi}\frac{g_{m23}}{(1 + g_{m23}R_{23})C_{\mu 27}} \tag{4.25}$$

The second dominant pole originates in the input stage $Q_{23} - Q_{24}$ with a form of

$$p_2 = \frac{1}{C_{\pi 23}R_1} \tag{4.26}$$

$$where\ R_1 = r_{\pi 23} \| \frac{r_{b23} + R_{23}}{(1 + g_{m23}R_{23})},\ r_{\pi 23} = \frac{\beta_{npn}}{g_{m23}},\ and\ r_{b23}\ is\ the\ base\ resistance\ of\ Q_{23}$$

For the transistor with an f_T of several GHz, the corresponding p_2 is typically above 1 GHz. Therefore, Equation (4.25) is a good approximation for the op amp f_u.

The offset voltage of the op amp can be reduced by replacing each input transistor with five identical transistors of minimum emitter size without significantly sacrificing the frequency response of the op amp. The differential outputs of the op amp are connected to the inputs of the core VCO through two stage emitter followers.

4.5. Emitter-Coupled Oscillator

As the powerhouse of the prototype VCO, a high frequency emitter-coupled oscillator (ECO) is employed to provide both wide frequency control range and high frequency oscillation up to several hundred MHz. Figure 4.8 shows its circuit schematic.

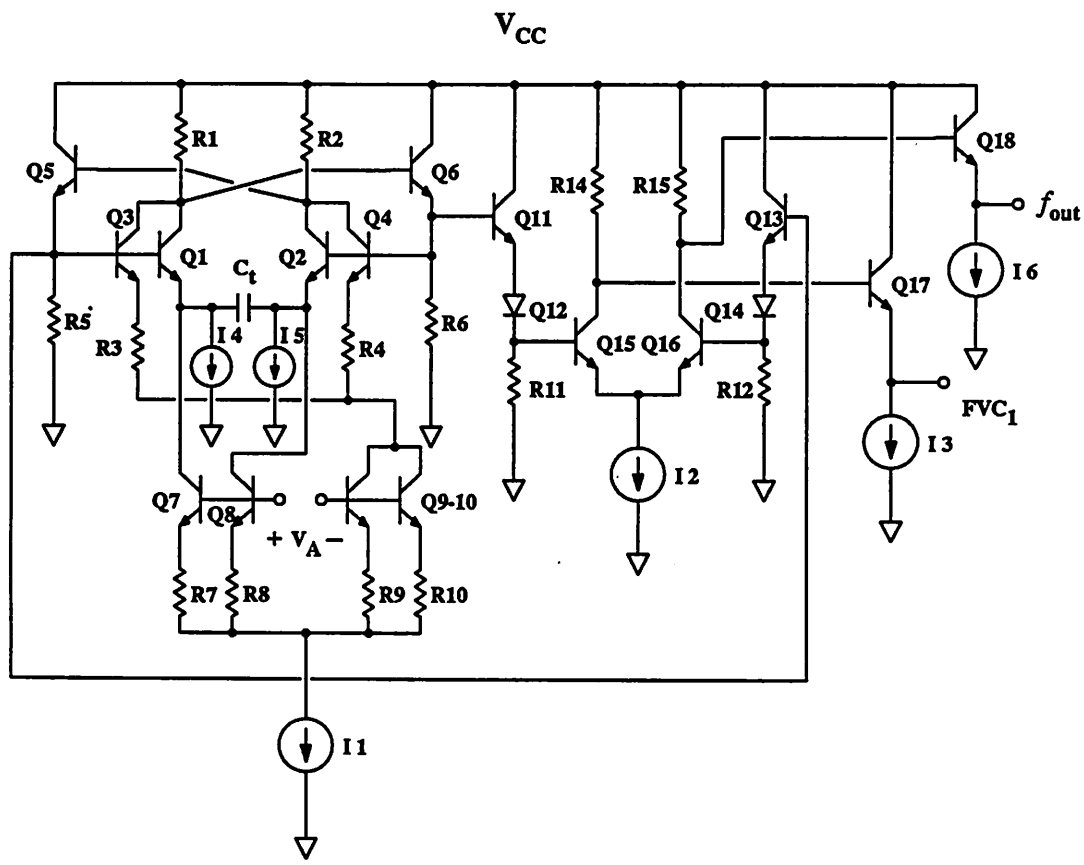


Figure 4.8 - Emitter-coupled oscillator schematic

This ECO operates in the same way as the conventional ECO shown in Figure 2.13 except that instead of using clamping diodes, the voltage swing across the timing capacitor C_t is held constant by adding an emitter-coupled pair Q_3–Q_4 to insure that the voltage drop across the load resistors R_1 and R_2 in either astable state does not vary with charge/discharge currents. With such an configuration, the voltage swing can be made small to attain high frequency operation at low power consumption. Although it can be implemented on chip, the timing capacitor C_t is external to the prototype for test purposes. Resistors R_3

and R_4, both small resistances of 100 Ω, are needed to guarantee oscillation, otherwise the output may be latched to one of the astable states. Neglecting the switching delay and parasitic capacitances, the oscillation frequency of the ECO is given by the expression

$$f_{osc} = \frac{(4I_4 + I_1) + g_V V_A}{8C_t (I_1 + 2I_4) R_1} \tag{4.27}$$

$$\textit{where } V_A \textit{ is the control voltage and } g_V = \frac{1}{R_7}$$

for $R_1 = R_2$, $I_4 = I_5$, and $R_7 = R_8 = R_9 = R_{10}$. The presence of resistors R_7 and R_8 provides a wide dynamic range for V_A and minimizes the ripple effect on the duty cycle of the ECO output waveform. However, this also reduces the conversion gain k_V of the ECO which is, from Equation (4.27)

$$k_V = \frac{g_V}{8C_t (I_1 + 2I_2) R_1} = \frac{1}{8C_t (I_1 + 2I_2) R_1 R_7} \tag{4.28}$$

Although we assume a linear ECO and then obtain its linearized gain k_V, the performance of the closed-loop VCO is not affected by the accuracy of Equations (4.27) and (4.28) as long as both open loop gains for the control and reference loops are high enough. In fact, as illustrated in the system level design, both Equations are quite useful in evaluating the closed-loop VCO performance.

Two identical auxiliary current sources I_4 and I_5 are used to eliminate the possibility that oscillation is interrupted when V_A goes below a certain voltage, due to noise or ripple from the FVC. Outputs with square waveform and ideally 50% duty cycle are taken from the emitter followers Q_5 and Q_6, followed by a differential amplifier Q_{15}–Q_{16} to square up the waveforms with sharp rising and falling edges (~ 1V/nS) before being fed to the one-shot section of the FVC through C_{81} to ensure the accurate triggering of the monostable multivibrator, as mentioned in the design of the FVC.

4.6. Bandgap Reference

In order to be self-contained, the prototype VCO requires an on-chip bandgap reference to provide the voltage reference for the reference loop. Figure 4.9 shows the schematic of the bandgap reference circuit. This is a simple first order circuit which only corrects the linear dependence of base-emitter vol-

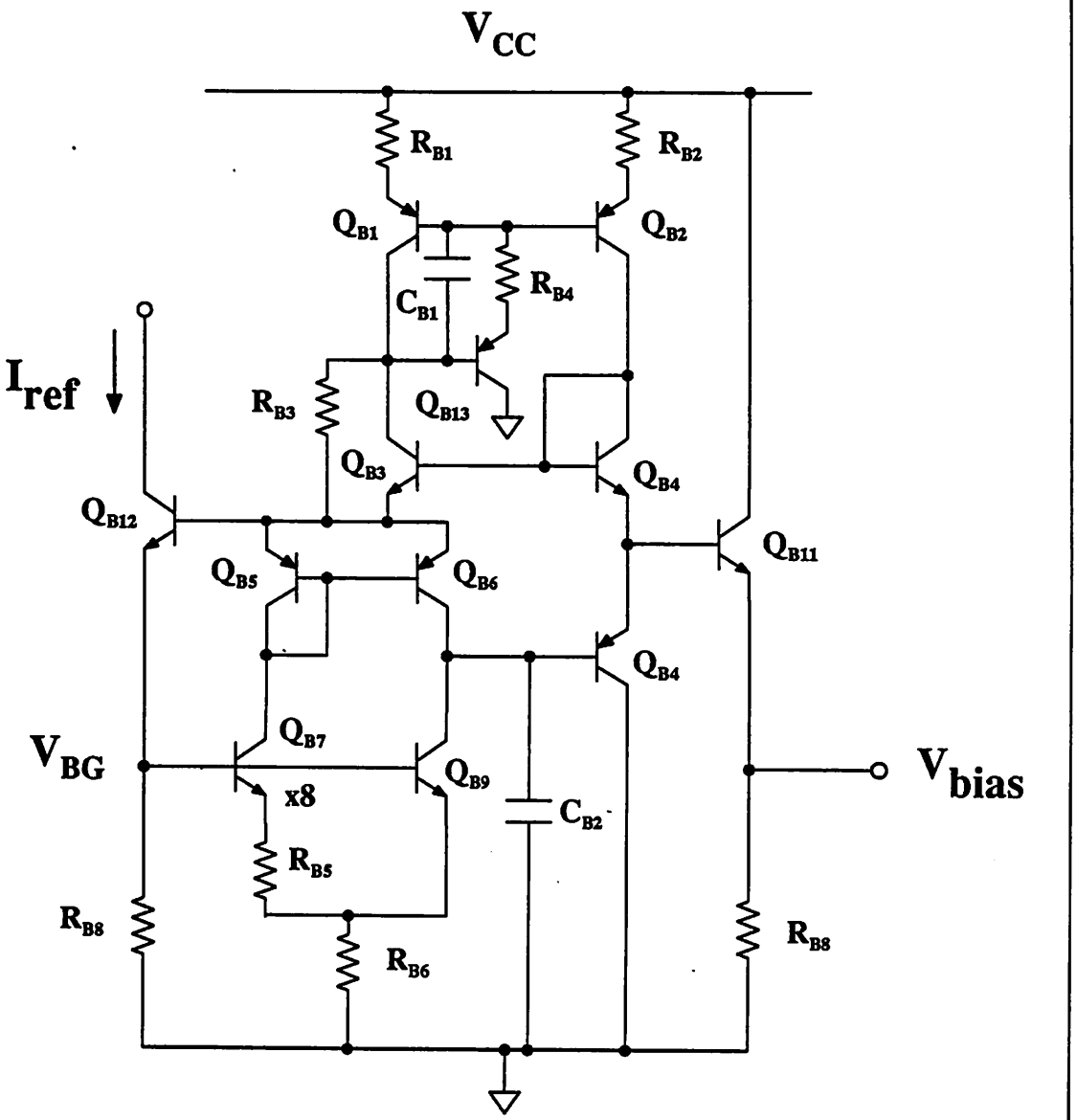


Figure 4.9 - Bandgap reference

tage V_{BE} on the absolute temperature T by adding an opposite linear term with the same magnitude to V_{BE}.[4,36] If base currents are negligible, the voltage across resistor R_{B5} is V_T ln 8 since both transistors Q_{B7} and Q_{B9} conduct the same amount of current due to the *pnp* current mirrors Q_{B5}–Q_{B6} while their emitter area ratio is 8:1, Furthermore, the voltage drop across R_{B6} is $\frac{2R_{B6}}{R_{B5}} V_T$ ln 8. Therefore, the bandgap voltage is

$$V_{BG} = V_{BE,B12} + \frac{2R_{B6}}{R_{B5}} V_T \ln 8 \tag{4.29}$$

The computer simulations show that the corresponding $\frac{R_{B6}}{R_{B5}}$ for the optimum V_{BG} of Equation (4.29) is 4.3 for the process fabricating the prototype VCO. A 1% error in the resistor ratio $\frac{R_{B6}}{R_{B5}}$, however, will result in a TC of 11 ppm/°C. This circuit also generates another bandgap voltage, V_{bias}, which serves as the biasing voltage for the current sources in other sections of the prototype VCO. Besides transistors Q_{B1}–Q_{B2}, and Q_{B3}–Q_{B4} used to help balance the circuit, different resistor values for R_{B7} and R_{B8} should be used to take into account the loading on the V_{bias} from other sections. C_{CB1} and C_{CB2} are on-chip capacitors to compensate the excessive phase shifts associted with *pnp* transistors to insure the stability. R_{B3} is an ion-implant start-up resistor with 100 kΩ resistance.

The voltage reference V_{ref} in the reference loop can then be derived from the bandgap voltage V_{BG} by forcing the current in resistor R_{B8} flowing in another resistor. V_{ref} is thus related to V_{BG} with a resistor ratio.

4.7. Crystal Oscillator

Another reference needed in the reference loop is the frequency. Again, although this may be derived from the system clock when the VCO is integrated with a large system, a Pierce crystal oscillator is included in the prototype for the sake of integrity. The circuit schematic of the crystal oscillator, along with the Schmitt trigger, is illustrated in Figure 4.10. This is essentially identical to Figure 2.11 with the differential pair Q_{C1}–Q_{C2} acting as the transconductance stage. Resistors $R_{C3} - R_{C6}$ are used to bias the differential pair such that it never enters the saturation region. Capacitors C_1 and C_2 are external to the circuit and the ratio $\frac{C_2}{C_1}$ is designed to be 8:3 to produce a sinusoidal wave across C_1 with an peak-to-peak voltage of 500 mV. A 20 MHz crystal is connected between C_1 and C_2 to provide an inductive feedback path at the oscillation frequency. Since the differential pair is driven by a sinewave of large amplitude, a near-square wave is available at the collector of Q_{C1}.

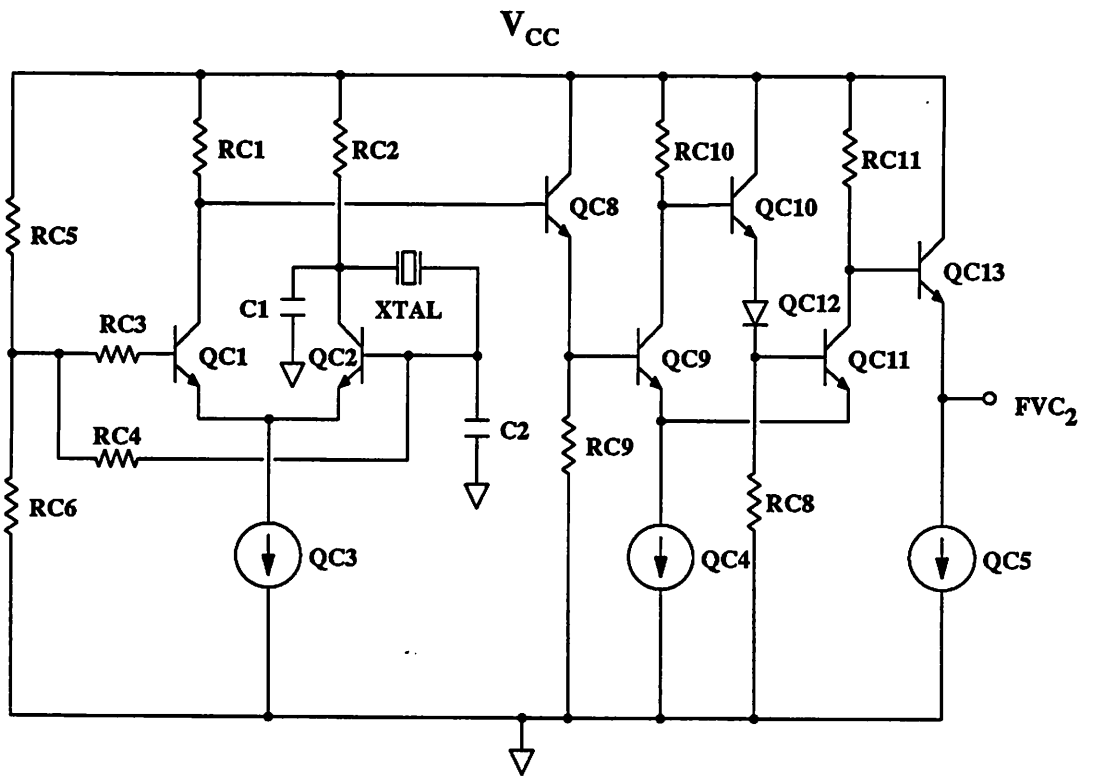


Figure 4.10 - Circuit diagram of crystal oscillator

A Schmitt trigger $Q_{C9} - Q_{C12}$ is inserted between the crystal oscillator and the FVC in the reference loop to further condition the output waveform from the crystal oscillator. Resistor R_{C11} and current source I_{C4} are identical to their counterpart R_{14} and I_2 in the ECO of Figure 4.9 to minimize the mismatch between two FVCs.

4.8. Voltage-to-Current Converter

Since the prototype VCO operates from a single positive power supply, a level-shift circuit is needed to transform the reference of original input control voltage V_{in} from ground potential to a higher level close to power supply V_{CC}. This can be achieved by using the circuit shown in Figure 4.11, where a simple op amp A_3 with negative feedback around resistor R_{A1} is used to convert V_{in} to current and then reflect it to the top, the same way V_{ref} is derived from the bandgap voltage. The realization of the

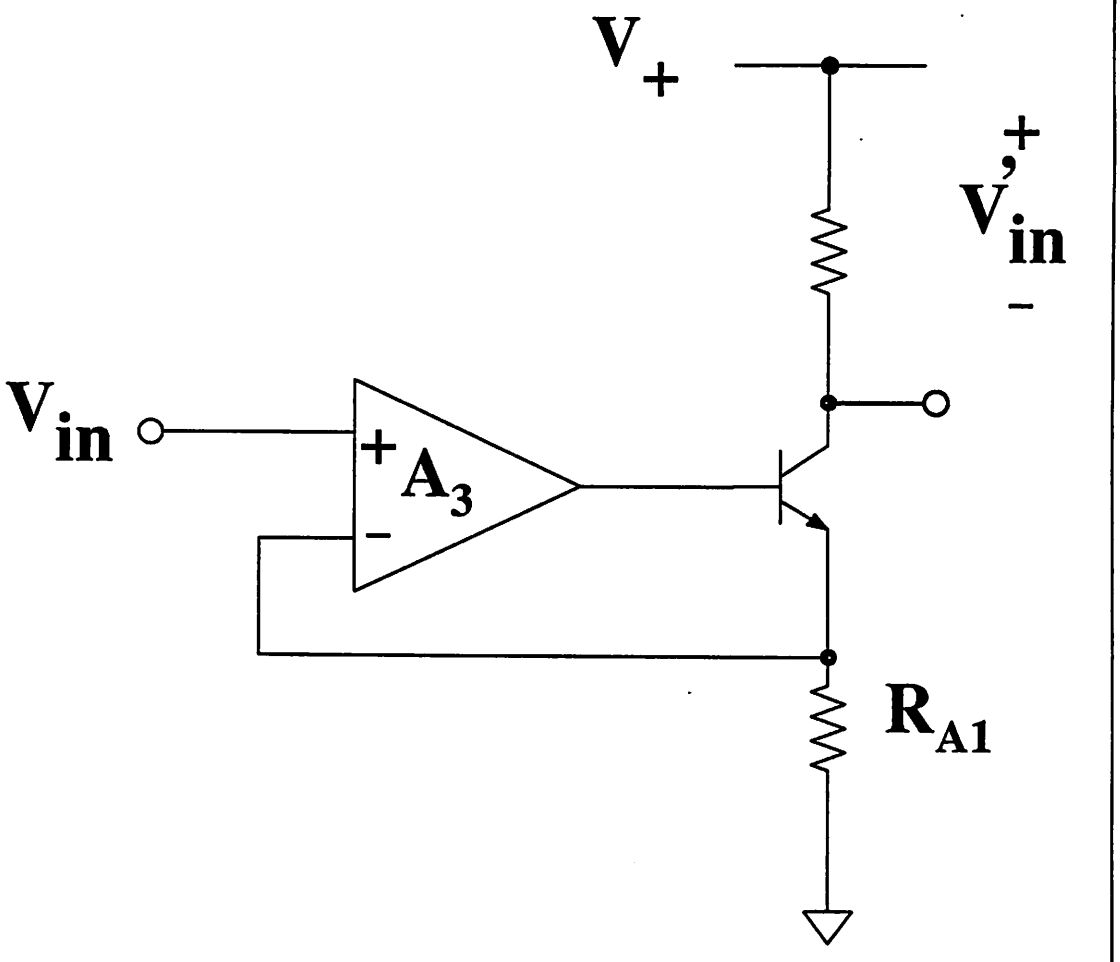


Figure 4.11 - Voltage-to-current converter

voltage-to-current converter is illustrated in Figure 4.12.

The input transistors Q_{A1} and Q_{A2} are vertical *pnp* transistors which allow V_{in} to swing close to ground potential. The low-frequency open-loop voltage gain of op amp A_3 is

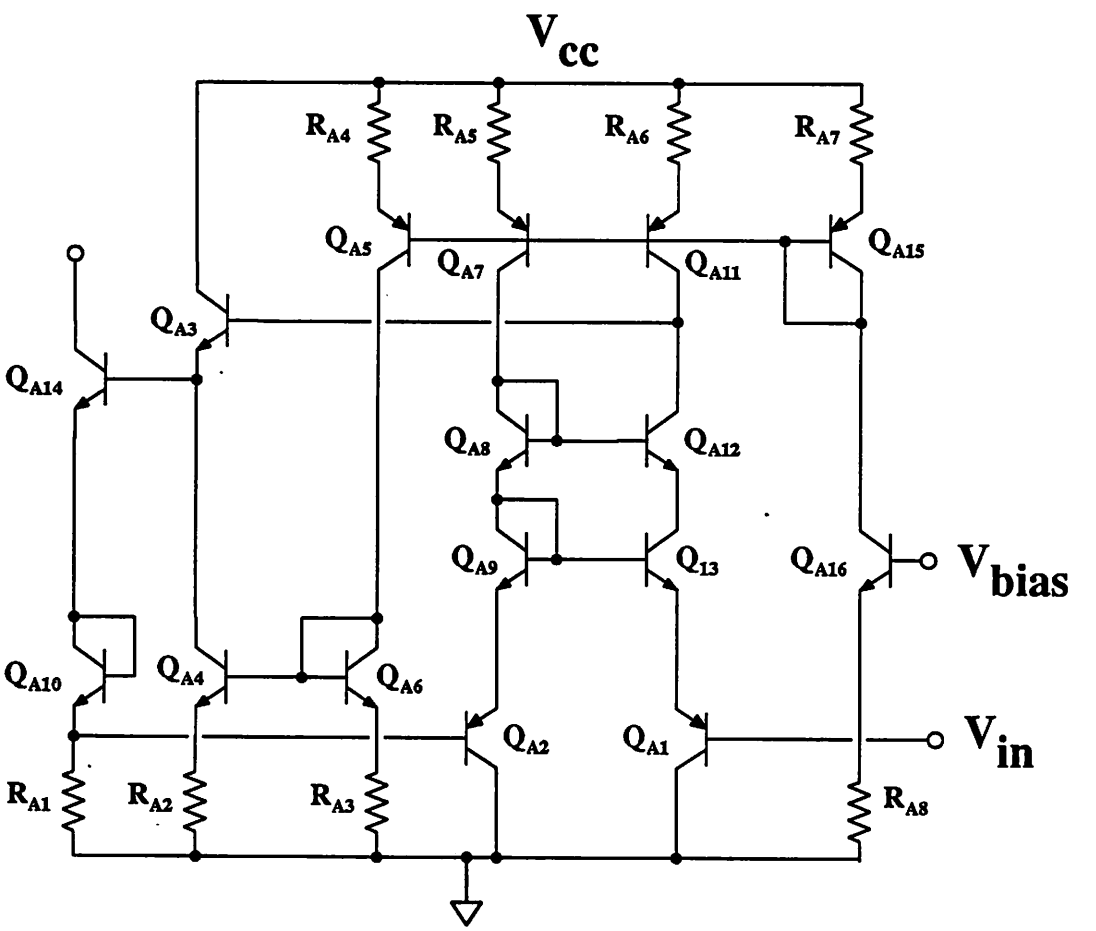


Figure 4.12 - Circuit diagram of op amp A3

$$A_{03} = \frac{g_{m1} r_{o11} (1 + g_{m11} R_{A6})}{4} \tag{4.30}$$

where g_{m1} and g_{m11} *are the transconductances* for Q_{A1} and Q_{A11} and r_{o11} *is the output impedance of* Q_{A11}

since the impedance seen looking into the collector of Q_{A12} is much greater than $r_{o11}(1 + g_{m11} R_{A6})$. Similar to the op amps used in both loops, A_3 uses the base-collector capacitance C_{A11} of Q_{A11} as the compensation capacitance. The SPICE promises a gain of 58 db and unity gain frequency of 150 MHz for A_3 when input biased at 0.1 mA. Q_{A14} is the output transistor whose collector current is converted back to the voltage through resistor R, which is connected between V_{CC} and the noninverting input of op

amp A_1 in the control loop.

CHAPTER 5

EXPERIMENTAL RESULTS

5.1. Introduction

An experimental closed-loop VCO based on the design techniques of Chapter 4 was fabricated in a 2-μm oxide-isolated, high-frequency bipolar process at Signetics Corporation. The unity-gain frequency f_T of the *npn* transistors used is 8 GHz. Transistors with a higher f_T are available, but the matching is not as good. The minimum emitter width is 2-μm. The block diagram of the prototype is illustrated in Figure 5.1. Capacitors C_{int}, C_z, C_F, and C_t, and crystal are external to the circuit. C_z is used to cancel the forward zero generated by C_{int}. The bandgap reference also provides the current biasing needed in the circuit, in addition to a stable, constant voltage for the reference loop. The op amp A_2 is a single-ended version of A_1. Because the current switching is accomplished by using *npn* transistors only, the conversion gain k_f of the FVC is actually negative. As a result, the ECO is connected to A_1 in such a way that a negative conversion gain k_f is attained. This is done by simply reversing the input polarity of the ECO.

A photograph of a prototype chip is shown in Figure 5.2. The die size is 40 mils by 55 mils. Of this, 1200 $mils^2$ is the active area. Two levels of metal are available for interconnections in the chip. The prototype was carefully laid out to minimize thermal gradients on the chip. Two crucial building blocks, the FVCs, are closely placed across the symmetric center line of the chip to improve temperature and process tracking. The top half of the die accommodates the control loop, whereas the bottom half is assigned to the reference loop to assure symmetry between two loops. Each building block is powered from its own V_{CC} pad to minimize high-frequency coupling and to ease testing, although a single 5V power supply is used to distribute the power to each pad. The parasitic inductances associated with the package leads and bonding wires help the high-frequency decoupling. Because of the large number of test pads, the prototype resides in a 40-pin dual-in-line ceramic package. The IC was mounted on a one-sided PC board with a 40-pin socket for testing. Six samples were available for measurements, and four of them were functioning properly.

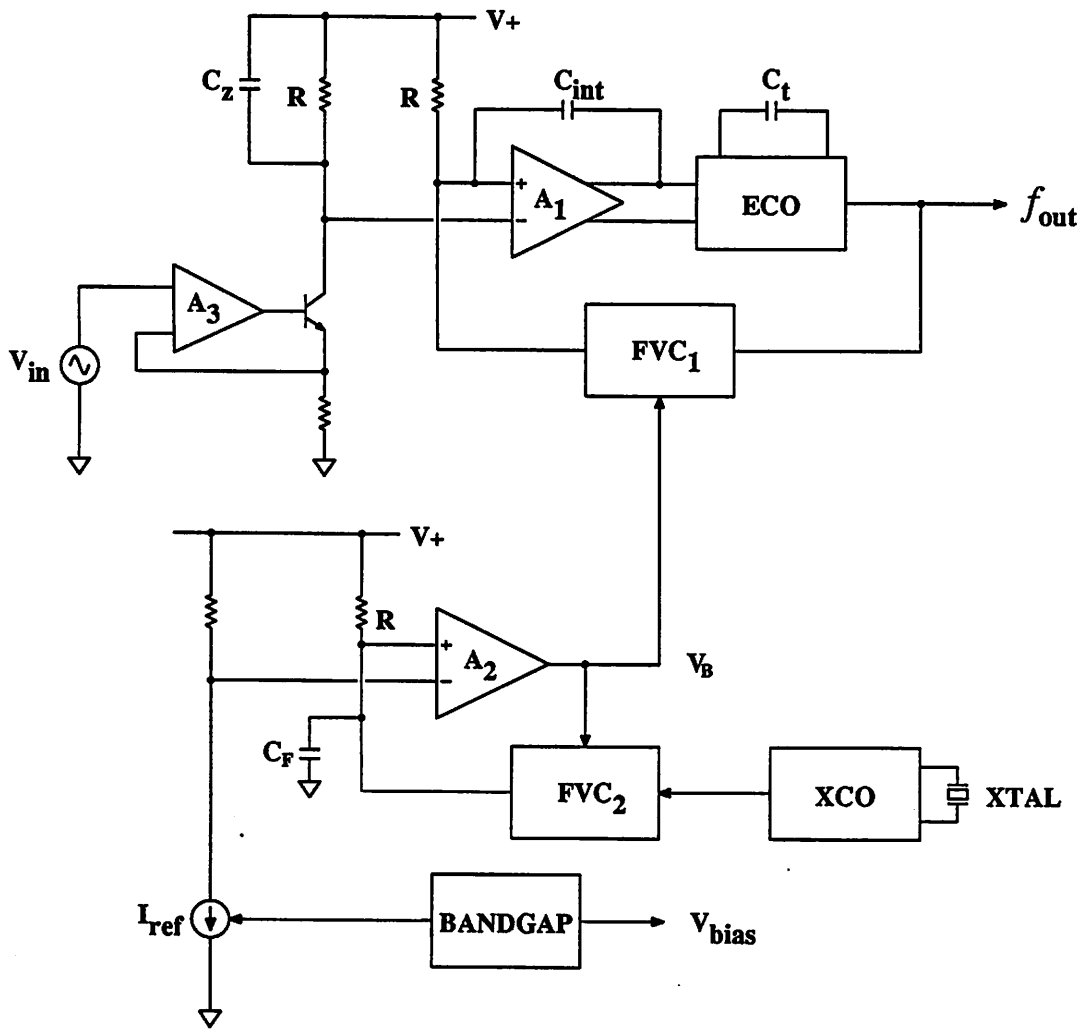


Figure 5.1 - Block diagram of VCO prototype

The prototype has been undergone the static and dynamic tests. In the static test, the stability of oscillation frequency with temperature and power supply variations, and the linearity of the frequency control characteristic were measured. In the dynamic test, the modulation bandwidth for the input signal was measured. The results vary little from sample to sample. Unless specified, the tests were conducted at the room temperature of 20°C and $V_{CC} = 5V$.

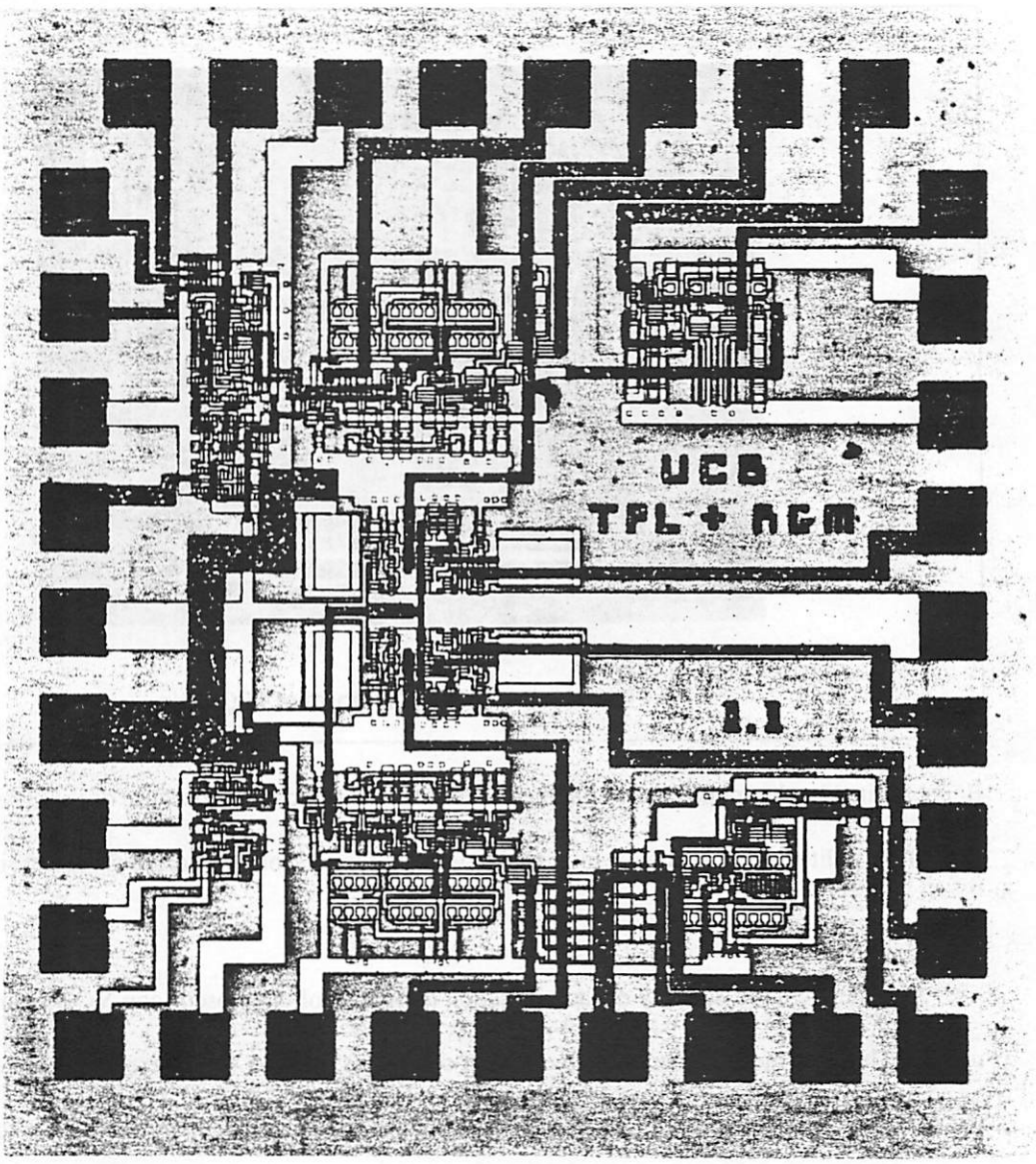


Figure 5.2 - Microphotograph of the experimental chip

5.2. TC Measurements

A Tektronix oscilloscope 7904 with a 500 MHz bandwidth as well as a 7D15 counter (up to 248 MHz) was used for the static measurements. Figure 5.3 shows the VCO waveform at 250 MHz.

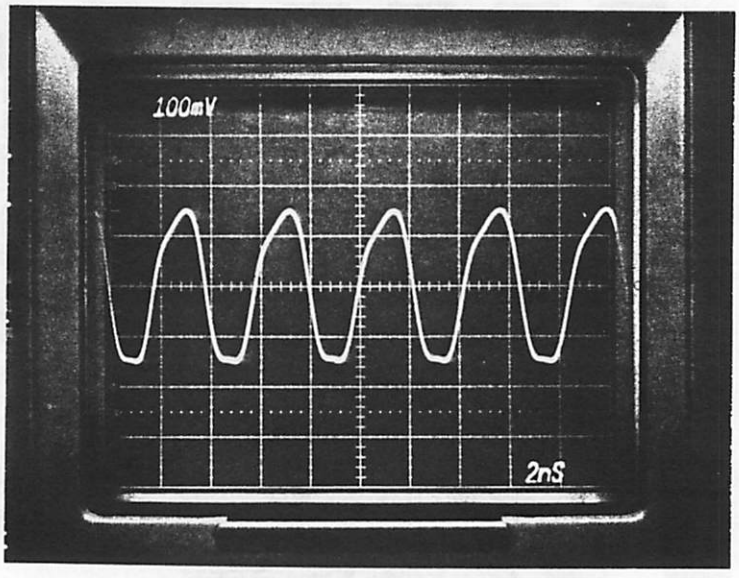


Figure 5.3 - VCO waveform at 250 MHz

Being limited by the scope bandwidth, the waveform is sinusoidal-like because of the absence of harmonics. The amplitude is also significantly reduced due to the lack of 50 Ω drive capability in the VCO output stage.

The temperature stability of the oscillation frequency of the closed-loop VCO is illustrated in Figure 5.4. This was measured under two different conditions: with an on-chip reference, and with an external reference. The measured TC of frequency using the internal bandgap voltage as the reference is -220 ppm/°C at 200 MHz as temperature varied between 20°C to 80°C. This is more than twice the theoretically predicted worst case TC given in Chapter 3. However, the measured TC with an external reference override is substantially reduced to -65 ppm/°C, close to the predicted value described in section 3.5.1. This notable difference in the measured TC suggests that the TC of the internal bandgap voltage may not be as low as designed. Figure 5.5 displays the on-chip bandgap voltage V_{BG} as a function of temperature.

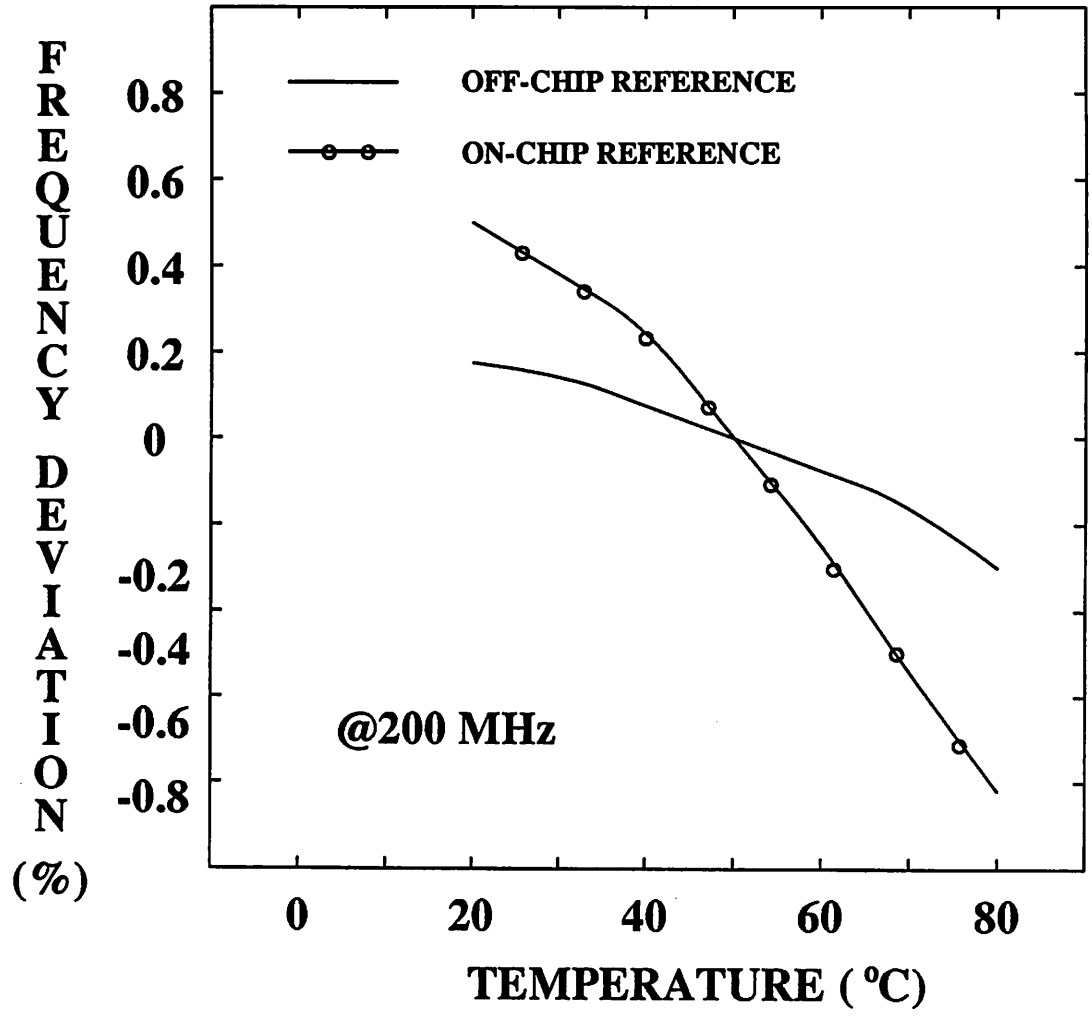


Figure 5.4 - VCO frequency vs. temperature

The TC of V_{BG} is unexpectedly high, being +180 ppm/°C, and according to Equation (3.18), a TC of -180 ppm/°C is contributed to the TC of frequency by the reference voltage *alone*. This explains the difference in two tests. The positive TC of V_{BG} signifies the proportional-to-absolute-temperature (PTAT) term in Equation (4.29) has more influence than the V_{BE} term. This is believed to be the result of the actual resistor ratio $\frac{R_{B6}}{R_{B5}}$ in the bandgap reference circuit deviating from the optimum value, due to an error in the design equations used for resistors. Note that a 10% error in the resistor ratio gives rise to a TC of ±110 ppm/°C. The measured TC of the reference frequency f_R generated by the crystal oscillator is less than 1

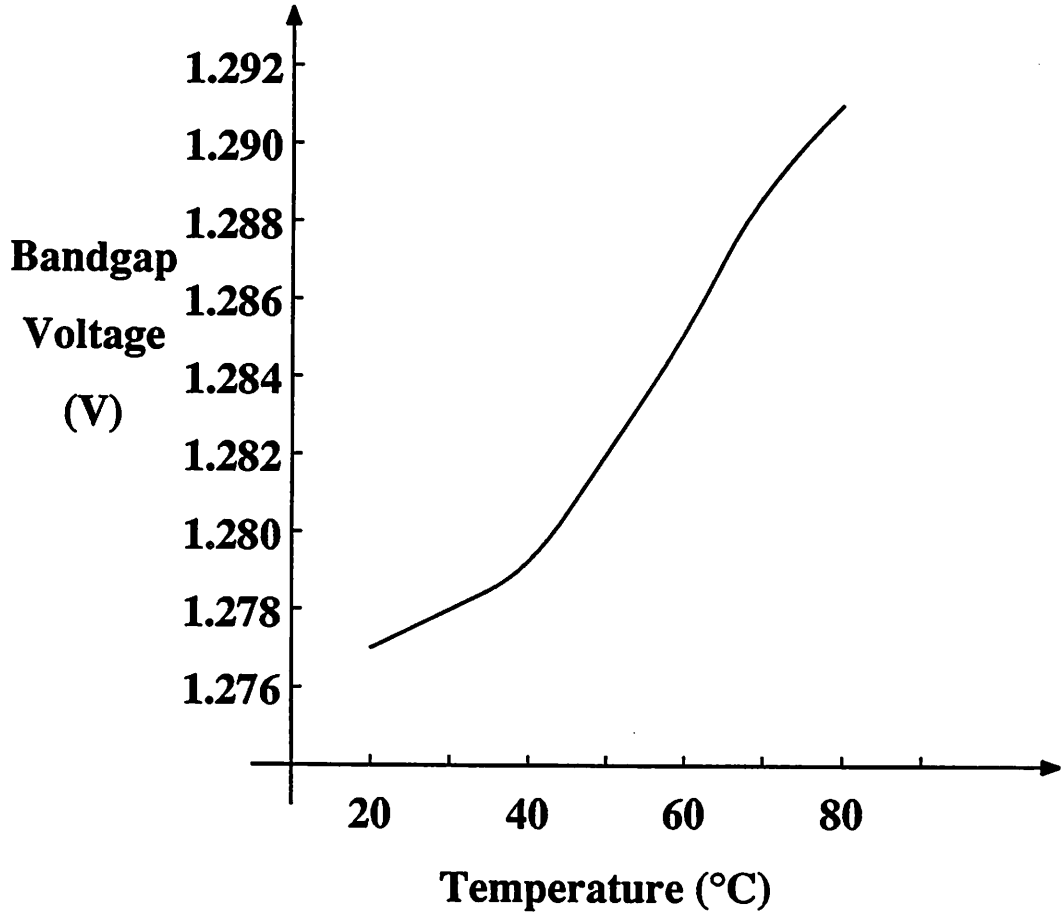


Figure 5.5 - On-chip bandgap voltage vs. temperature

ppm/°C.

The measured TC of frequency at oscillation frequencies 250 MHz and above deteriorates rapidly. This is because the FVC is not functioning properly at those frequencies since the measured pulse width of the one-shot circuit is about 2 nS, as explained in the preceding chapter. As a result, two FVCs cannot track each other and result in a large TC at high frequencies. The operation range can be extended by generating a narrower pulse width through the use of a smaller value of C_{82} in the one-shot shown in Figure 4.4. For temperature above 80°C, the test board used did not provide reliable connections because of the closely placed solder. Although the TC measurements were conducted from 20°C to 80°C, the results

clearly demonstrate the effectiveness of the closed-loop architecture in the stabilization of oscillation frequency with temperature.

5.3. Linearity Measurements

The measured voltage-to-frequency control characteristic is shown in Figure 5.6.

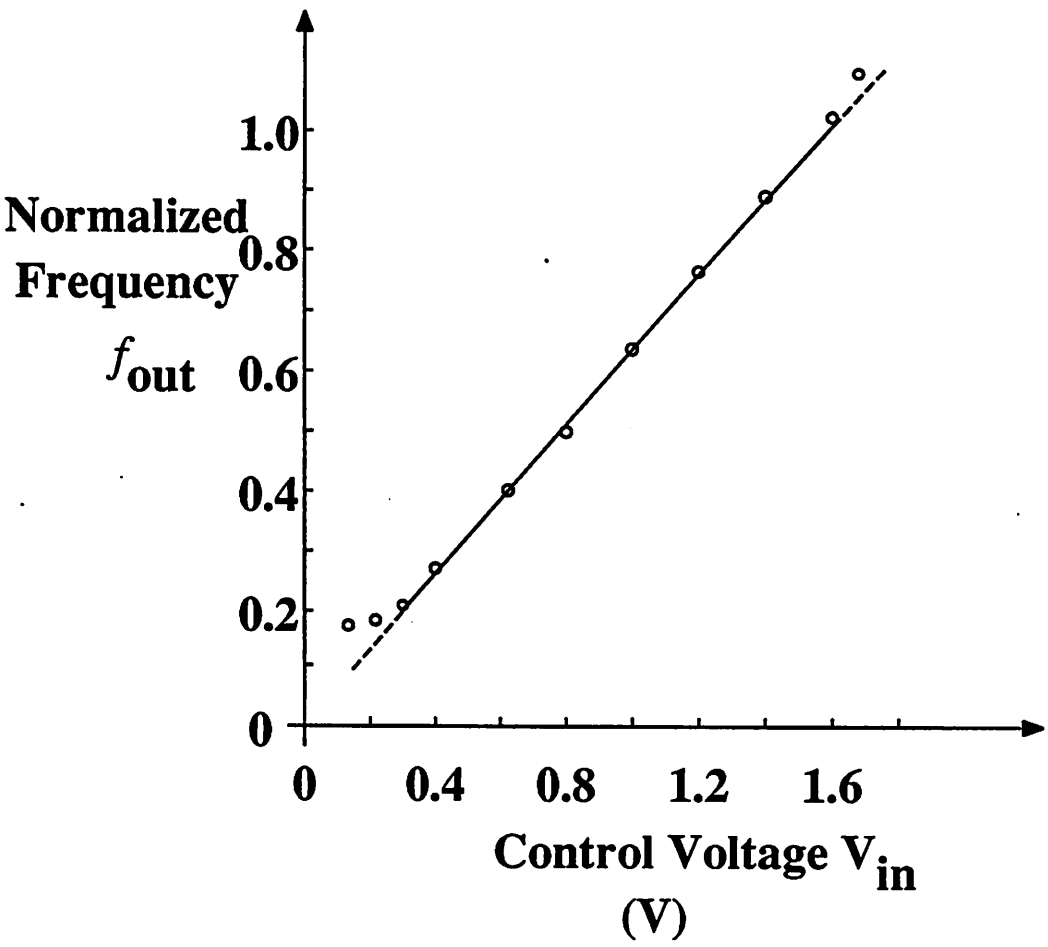


Figure 5.6 - VCO frequency-to-voltage control characteristic

The frequency is normalized to 250 MHz, whereas the input control voltage is varied between 0.2 V and 1.6 V. The prototype displays a nonlinearity of 2% over a 5:1 frequency control range. Such a performance is acceptable in many high frequency applications. For example, the nonlinearity requirement on the VCO used in PLL receivers to demodulate video signals from a 70 MHz carrier in satellite

communication is 4%.

The nonlinearity is, however, larger than expected. This may be caused by several different error sources. First, the triggering signal of the one-shot circuit may exhibit some degree of dependence on the VCO frequency. This results in the variation of the pulse width t_0 and hence the linearity error. Second, because the voltage at the noninverting node of A_1 is not constant, the finite output impedance of the transistor in the current switching section contributes errors in the integration current. Another error source is the charge injection. Again, due to variations of the voltage at the noninverting node, different amount of charges is injected to that node and this can cause the linearity error.

Furthermore, at the both ends of the transfer characteristic the measured results deviate from the projected straight line. The error occurring at high frequencies is due to the high frequency limitation on the FVC in the control loop. As seen in Figure 4.6, the effective k_f is reduced at high frequencies, and this gives rise to the upward bended characteristics. On the other hand, the oscillation frequency with a small V_{in} is approximately constant, resulting from the use of two auxiliary current sources I_4 and I_5 in the ECO shown in figure 4.8. Both current sources can be turned off to extend the linear range, if a large value of C_{int} is used. However, as described in Chapter 4, the leakage currents in the FVCs impose the ultimate limitations on the low frequency operation, if offset voltages of op amps are neglected.

5.4. Stability with Power Supply

Figure 5.7 shows the measured stability of the VCO center frequency with power supply. The percentage of frequency deviation from the VCO center frequency (200 MHz) is plotted as a function of power supply voltage. The power supply was varied between 4.75 V and 5.25 V. Over this range, the measured power supply rejection is 0.4%/V. It can be seen that the stability of frequency is inferior for supply voltage below 5.1 V. This is believed to be related to the op amp common-mode voltage V_{com} whose design value is 3.5 V. Due to the error in the resistor design equations, V_{com} might be larger than designed. A low supply voltage then might bring the *pnp* current sources in the op amp to the edge of saturation and therefore result in the degradation of the op amp gain. For this reason, the VCO frequency is more insensitive to larger supply voltages. The supply rejection for $V_{CC} \geq 5.1$ V is 0.1%/V, four times

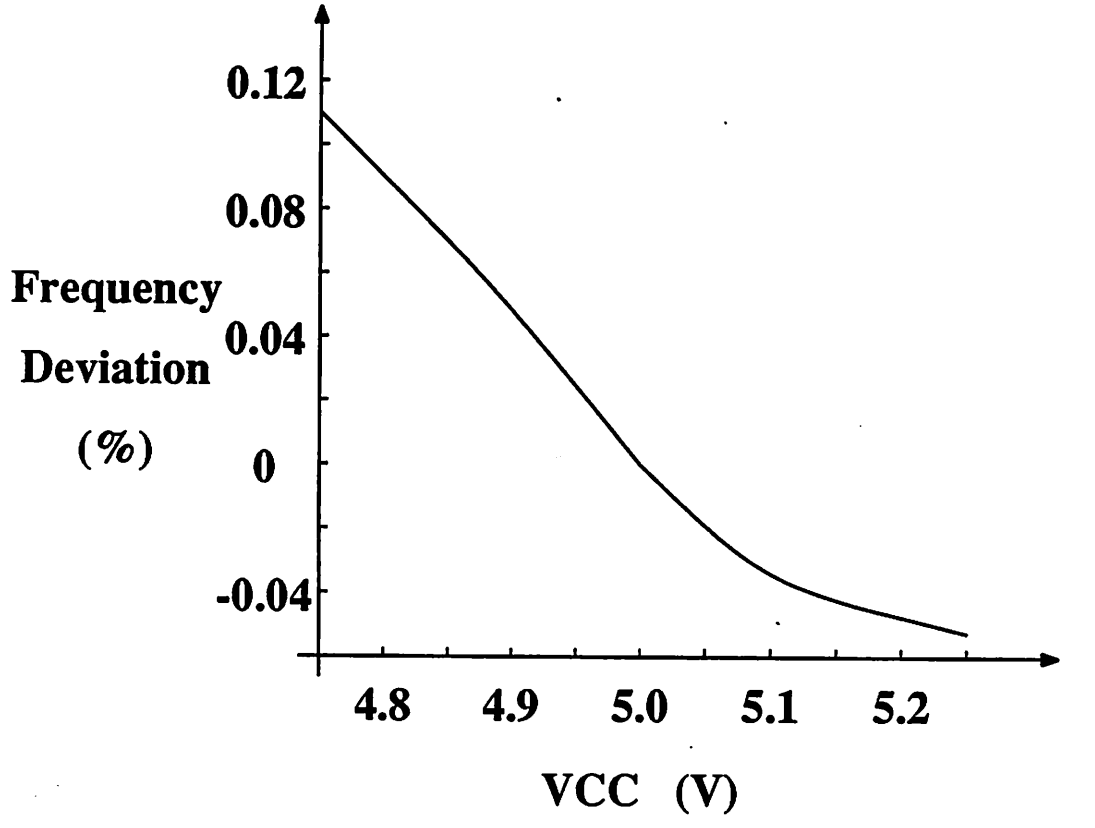


Figure 5.7 - VCO frequency vs. power supply

improvement. Therefore, a supply rejection of 0.1% should be attained if the op amp is properly biased.

5.5. Modulation Bandwidth

The measured modulation bandwidth of the VCO prototype is in excess of 12 MHz by using a PLL (Signetics 568) to demodulate a 70 MHz carrier which was generated by modulating the VCO with a frequency-variable sinusoidal source. Figure 5.8 shows the spectrum of demodulated FM signal with a 12 MHz modulating frequency and 70 MHz carrier frequency. For $k_f k_V = 2, R = 2$ K, $C_{int} = 10$ pF, and $A_0 p_1 = 2\pi \times 250 \times 10^6$ rad/s, the modulation bandwidth of the prototype given by Equation (4.9b) is 15.4 MHz. This is in good agreement with the measured modulation bandwidth.

Since the prototype provides a wide modulation bandwidth and good voltage-to- frequency linear-

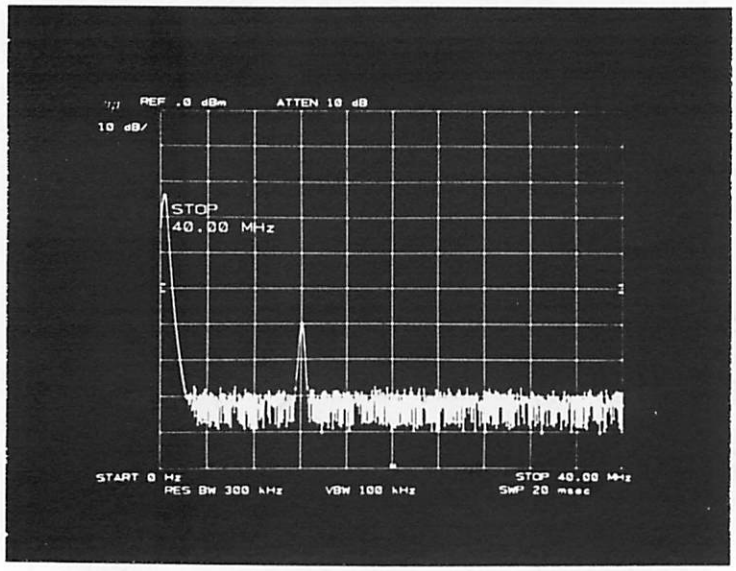


Figure 5.8 - Demodulated FM signal with 12 MHz modulating frequency

ity, it is ideally suited for PLL applications such as demodulation of video signals from a 70 MHz carrier in satellite receivers.

The performance of the prototype VCO is summarized in Table 5.1.

Maximum Oscillation frequency	250 MHz
TC of Frequency	-65 ppm/°C
Nonlinearity of Voltage-to-Frequency	2%
Drift with Power Supply	-0.4%/V
Modulation Bandwidth	> 12 MHz
Supply Voltage	5V
Power Dissipation	220 mW
Chip Area (Active / Total)	1,200 / 2,200 $mils^2$

Table 5.1 - Summary of experimental results

CHAPTER 6

CONCLUSIONS

6.1. Summary of Research

Circuit design techniques for implementing precision high-frequency monolithic voltage-controlled oscillators (VCO's) have been developed. The precision VCO incorporates a closed-loop configuration where a frequency-to-voltage converter (FVC) acts as feedback element to correct errors in oscillation frequency. Closed-loop VCO's have several important advantages over conventional open-loop VCO's. First, the oscillation frequency of the closed-loop VCO is temperature-insensitive and has a small temperature coefficient (TC) even at high frequencies because of the use of a feedback loop stabilizing the conversion gain of the FVC. Second, the linearity of the VCO voltage-to-frequency characteristic is also improved because of the use of negative feedback and high speed linear FVC's. Third, since the FVC conversion gain relies on voltage and frequency references which can be derived from an on-chip precision bandgap reference and a stable, accurate clock frequency, very precise VCO frequencies can be attained which are insensitive to power supply and processing variations.

The performance of the closed-loop VCO, in terms of the TC of frequency, linearity of voltage-to-frequency characteristic, and frequency accuracy, has been analyzed. It shows that the performance is limited by the matching of components on the same die, if op amps with moderate gain of 1000 or more are used in feedback loops. The relationship between the frequency response of the closed-loop VCO and the ripple voltage at the output of FVC has been investigated. A compromise between the VCO output duty cycle and modulation bandwidth of the VCO can be made to fulfill specific applications.

An experimental closed-loop VCO prototype has been designed and fabricated in a high speed bipolar process to verify the feasibility of the proposed architecture. The measured experimental results demonstrated low TC of frequency, good linearity, insensitivity to power supply variations, and wide modulation bandwidth which is suitable for video applications. The circuit consumes a small active area, and this can be further reduced if integrated with large systems where both voltage and frequency refer-

ences are usually available.

6.2. Future Topics

Although the closed-loop approach was applied to implement the high frequency emitter-coupled oscillator in bipolar technology in this research to demonstrate the validity of theory, it may be of potential interest for other VCO configurations and technologies. Several areas which future research may be directed are: (1) high speed FVC's capable of operating at frequencies of GHz and above; (2) low offset, moderate gain, high unity gain op amps; (3) ring oscillator-based closed loop VCOs; (4) emitter-coupled VCOs using parasitic capacitances as the timing element, and (5) high frequency MOS VCO's.

Appendix

Time-Domain Analysis of the Control Loop

In this appendix, we analyze the dynamic behavior of the control loop in the time domain, and specifically the relationship between the output oscillation frequency f_{out} and input control voltage V_{in}.

To keep the analysis simple and mathematically manageable, we assume an ideal op amp A_1 used in the control loop. Summing the currents at the inverting node of A_1 in Figure 4.1,

$$C_{int}\frac{d}{dt}\left[v_1 - V_{in}\right] + I_1 - \frac{V_{in}}{R} = 0 \tag{A.1}$$

Integrating Equation (A.1) from $t = 0$ to $t = t$ where $t_n \le t \le t_{n+1}$, we obtain

$$C_{int}\left[(v_1(t) - v_1(0)) - (V_{in}(t) - V_{in}(0))\right] + n\, I_0 t_0 + h(t) = \frac{\int_{t=0}^{t} V_{in}\,dt}{R} \tag{A.2}$$

$$where\ \ h(t) = \begin{cases} I_0(t - t_n)/t_0 & \text{if } t_n \le t \le t_n + t_0 \\ I_0 t_0 & \text{if } t_n + t_0 \le t \le t_{n+1} \end{cases}$$

Using the initial conditions at $t_0 = 0$

$$k_V v_1(0) = f_0 \tag{A.3}$$

and

$$I_0 t_0 f_0 R = V_{in}(0) \tag{A.4}$$

$$where\ f_0 = steady\ state\ oscillation\ frequency \text{ for } t \le 0$$

Equation (A.2) can be rewritten as

$$v_1(t) = \frac{G(t)}{RC_{int}} - \frac{nV_{in}(0)}{RC_{int}f_0} - \frac{h(t)}{C_{int}} + \frac{f_0}{k_V} + V_{in}(t) - V_{in}(0) \tag{A.5}$$

$$where\ G(t) \equiv \int_{t=0}^{t} V_{in}(t)\,dt$$

The n^{th} period of the VCO is related to the average value of $v_1(t)$ during that interval. More specifically,

$$\frac{1}{t_{n+1}-t_n} = k_V v_1^{*}(t) = k_V \frac{\int_{t=t_n}^{t_{n+1}} v_1(t)\,dt}{t_{n+1}-t_n} \tag{A.6}$$

or

$$k_V \int_{t=t_n}^{t_{n+1}} v_1(t)\,dt = 1 \tag{A.7}$$

Integrating both sides of Equation (A.5) and using Equation (A.7), we arrive at

$$\frac{1}{k_V} = \frac{1}{RC_{int}} \int_{t=t_n}^{t_{n+1}} G(t)\,dt + \int_{t=t_n}^{t_{n+1}} V_{in}(t)\,dt - \left[V_{in}(0)\left(1 + \frac{n}{RC_{int} f_0}\right) - \frac{f_0}{k_V} \right](t_{n+1}-t_n) \tag{A.8}$$
$$- \frac{I_0 t_0}{2C_{int}} \left[2(t_{n+1}-t_n) - t_0 \right]$$

Note that the first and second term on the right side of Equation (A.8) cannot be linear terms of $(t_{n+1} - t_n)$ since they are related by integration. As a result, Equation (A.7) is a nonlinear difference equation for t_n and hence the control loop is a nonlinear discrete system.

References

1. W. H. Eccles and F. W. Jordan, "A Trigger Relay Utilising Three Electrode Thermionic Vacuum Tubes," *Radio Review*, pp. 143-146, 1919.

2. A. B. Grebene, "The Monolithic Phase Locked Loop: a versatile building block," *IEEE Spectrum*, pp. 38-49, March, 1971.

3. R. R. Cordell and W. G. Garrett, "A Highly Stable VCO for Applications in monolithic Phase-Locked Loops," *IEEE Journal of Solid-State Circuits*, pp. 480-485, December, 1975.

4. J. K. Kukielka and R. G. Meyer, "A High-Frequency Temperature-Stable Monolithic VCO," *IEEE Journal of Solid-State Circuits*, pp. 1214-1219, December, 1982.

5. A. A. Abidi and R. G. Meyer, "Noise in Relaxation Oscillators," *IEEE Journal of Solid-State Circuits*, pp. 794-802, December, 1983.

6. A. B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design*, Wiley, New York, 1984.

7. K. Matsumoto, E. Ishii, H. Yamagishi, N. Amano, and M. Sugawara, "A 700 MHz Monolithic Phased-locked Demodulator," *Digest of Technical Papers, 1985 IEEE International Solid-State Circuits Conference, New York, NY*, pp. 22-23, February, 1985.

8. R. A. Blauschild and R. G. Meyer, "A Low Power, 5V, 150MHz PLL with Improved Linearity," *Digest of Technical Papers, 1985 IEEE International Consumer Electronics Conference*, pp. 122-123, June, 1985.

9. L. Strauss, *Wave Generation and Shaping, Second Edition*, McGraw-Hill, New York, 1970.

10. K. K. Clarke and D. T. Hess, *Communication Circuits: Analusis and Design*, Addison-Wesley, New York, 1971.

11. H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Enginnering*, Wiley, New York, 1980.

12. B. Parzen, *Design of Crystal and Other Harmonic Oscillators*, Wiley, New York, 1983.

13. R. G. Meyer, *Nonlinear Analog Integrated Circuits, EE240 Class Notes*, University of California, Berkeley, 1979.

14. A. A. Abidi, *Effects of Random & Periodic Excitations on Relaxation Oscillators*, University of California at Berkeley, September, 1981. Memo Number UCB/ERL M81/80

15. B. N. Scott, M. Wurtele, and B. B. Creggar, "A GaAs Monolithic Voltage Controlled Oscillator," *Digest of Technical Papers, 1984 IEEE International Solid-State Circuits Conference, San Francisco, CA*, pp. 74-75, February, 1984.

16. M. E. Freking, *Crysatl Oscillator Design and Temperature Compensation*, Van Norstrand Reinhold, New York, 1978.

17. E. A. Vittoz and M. G. Degrauwe, "High-Performance Crystal Oscillator Circuits: Theory and Application," *IEEE Journal of Solid-State Circuits*, to be published. June, 1988.

18. F. M. Gardner, *Phaselock Techniques, second Edition*, Wiley, New York, 1979.

19. R. G. Meyer, W. M. C. Sansen, S. Liu, and S. Peeters, "The Differential Pair as a Triangular-sine Wave Converter," *IEEE Journal of Solid-State Circuits*, pp. 418-420, June, 1976.

20. B. Gilbert, "A Versatile Voltage-to-frequency Converter," *IEEE Journal of Solid-State Circuits*, pp. 852-864, December, 1976.

21. D. -K. Jeong, G. Forriello, D. A. Hodges, and R. H. Katz, "Design of PLL-Based Clock Generation Circuits," *IEEE Journal of Solid-State Circuits*, pp. 255-261, April, 1987.

22. S. K. Enam and A. A. Abidi, "Decision and Clock Recovery Circuits for Gigahertz Optical Fiber Receivers in Silicon NMOS," *IEEE Journal of Lightwave Technology*, pp. 367-372, March, 19874.

23. W. D. Liewellyn, M. M. H. Wong, G. W. Tietz, and P. A. Tucci, "A 33Mb/s Data Synchronizing Phase-Locked Loop Circuit," *Digest of Technical Papers, 1988 IEEE International Solid-State Circuits Conference, San Francisco, CA*, pp. 12-13, February, 1988.

24. R. H. Leonowich and J. M. Steininger, "A 45-MHz CMOS Phase/Frequency-Locked Loop Timing

Recovery circuit," *Digest of Technical Papers, 1988 IEEE International Solid-State Circuits Conference, San Francisco, CA*, pp. 14-15, February, 1988.

25. S. Sasaki, "Higher Harmonic Generation in CMOS/SOS Ring Oscillators"," *IEEE Trans. Electron Devices*, pp. 280-283, February, 1982.

26. E. N. Murthi, "A Monolithic Phase-Locked Loop with Post Detection Processor," *IEEE Journal of Solid-State Circuits*, pp. 155-161, February, 1979.

27. A. J. Viterbi, *Principles of Coherent Communication*, McGraw-Hill, New York, 1966.

28. P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits, Second Edition*, John Wiley & Sons, New York, 1984.

29. M. H. Wakayama and A. A. Abidi, "A 30-MHz Low-Jitter High-Linearity CMOS Voltage-Controlled Oscillator," *IEEE Journal of Solid-State Circuits*, pp. 1074-1081, December, 1987.

30. G. M. Meijer, P. C. Schmale, and K. V. Zalinge, "A New Curvature-Corrected Bandgap Reference," *IEEE Journal of Solid-State Circuits*, pp. 1139-1143, December, 1982.

31. B. -S. Song and P. R. Gray, "A Precision Curvature-Compensated CMOS Bandgap Reference," *IEEE Journal of Solid-State Circuits*, pp. 634-643, December, 1983.

32. M. Banu, "A 100KHz-1GHz NMOS Variable-Frequency Oscillator with Analog and Digital Control," *Digest of Technical Papers, 1988 IEEE International Solid-State Circuits Conference, San Francisco, CA*, pp. 20-21, February, 1988.

33. B. Kuo, *Automatic Control Systems, Second Edition*, Prentice-Hall, New York, 1967.

34. J. Millman and H. Taub, *Pulse, Digital, and Switching Waveforms*, McGraw-Hill, New York, 1965.

35. L. W. Nagel, *SPICE2, A Computer Program to Simulate Semiconductor Circuits*, University of California at Berkeley, May, 1975. Memo Number UCB/ERL M520

36. A. P. Brokaw, "A Simple Three-Terminal IC Bandgap Reference," *IEEE Journal of Solid-State Circuits*, pp. 388-393, December, 1974.