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TUNING A STATISTICAL PROCESS SIMULATOR TO A BERKELEY CMOS PROCESS

by

Paul M. Krueger

Memorandum No. UCB/ERL M88/82

15 December 1988

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TUNING A STATISTICAL PROCESS SIMULATOR TO A BERKELEY CMOS PROCESS

Paul M. Krueger

Department of Electrical Engineering and Computer Sciences
University of California, Berkeley

ABSTRACT

A test chip containing devices necessary for the extraction of process disturbances has been constructed and fabricated for the purposes of tuning the statistical process and device simulator, FABRICS II, to a Berkeley CMOS process. The simulator has been recompiled to run a Berkeley version of a CMOS fabrication process. A description of the test chip and the process steps are presented. Measurement results and the tuning process are described.

I. INTRODUCTION

In the past 15 years, the minimum feature size for typical integrated circuit fabrication processes has steadily decreased. Minimum MOS channel lengths of 5 micrometers (μm), common in the 1970's, are now 1.5 μm and smaller. This reduction of feature size has brought about the benefits of increased circuit density and much greater functionality for a given die area. Increases in wafer size have correspondingly increased the number of die that may be fabricated per wafer. High precision fabrication equipment which allows the definition of finer features contributes to greater circuit density. Equipment of considerable complexity is necessary to manufacture these larger, denser chips. The quality of the fabrication process must be high and the control of the individual steps must be maintained in order for working circuits to be produced.

Increasing competition has accompanied the rising cost of manufacturing. Low-yielding fabrication lines are no longer profitable in today's marketplace. This situation has lead to interest in computer integrated manufacturing. Computer integrated manufacturing includes areas such as automated data collection and storage, unique methods of accessing and relating process and die test data, software tools for control and prediction of fabrication processes, and high-level monitoring of fabrication line work flows. This paper deals with the application of a set of software tools which can simulate and predict physical and electrical parameters for devices produced from an integrated circuit fabrication process. These tools center around the FABRICS II [1] statistical process and device simulator.

This report outlines the steps taken to tune this statistical process and device simulator to a 2-micron p-well CMOS process used in the Microfabrication Laboratory at the University of California, Berkeley. The results of the work will be presented, along with an explanation of the steps required to tune the simulator.

II. SIMULATOR BACKGROUND

The simulator used in this project is the FABRICS II process and device simulator, developed at Carnegie-Mellon University (CMU). FABRICS II is the core of a set of programs combined into a software package called the Process Engineer's Workbench [2]. Supporting programs that are used in the tuning process include a process editor and compiler, PED-PI/C [3] [4], and a statistical extraction package, Prometheus [5]. These programs run on a Digital Equipment Corporation VAXStation II, running the Ultrix version of UNIX[1].

In a given fabrication process, random disturbances will effect the final physical and electrical characteristics of the devices. Each device produced will have slightly differing parameters, even though the devices were fabricated with the same steps, the same parameters, using the same equipment, even on the same wafer. These disturbances are not directly measurable. Examples of disturbances are linewidth variations and differences in diffusivity of an impurity in the silicon. However, if these disturbances are known, they can be used to predict how the device parameters will vary about a mean.

A process simulator may use the disturbances along with a process description to imitate the actual process. Since the simulator acts like the process, the control variables of one or more of the steps may be changed and the resulting effect on physical and electrical parameters may be observed. Note that this is changing an existing step's control parameters, not adding or deleting a step which may change the disturbances. Another example would be to use the information to derive a set of model parameters for a circuit simulator. Designers can use these models to simulate over the range of expected variations, thus assuring that the circuit will function within the intended specification through the actual process variations. Simulation under these circumstances gives more realistic results rather than assuming possible worst or best cases for all model parameters which may never happen in reality. This will give less pessimistic yield estimates than circuits simulated using inconsistent model parameters.

FABRICS II is a process and device simulator which takes into account the statistical variation of an actual fabrication process. Figure 1 [5] shows how FABRICS can be used to imitate the variations found in an integrated circuit fabrication process. Random disturbances affect the final output parameters for the actual process. Similarly, disturbances are entered into the FABRICS process supervisor. The idea is to have the final output from FABRICS mimic the real process. Since FABRICS will simulate the process many times in order to arrive at the final parameter distributions, the equations that the program uses must be able to be rapidly evaluated. This is where FABRICS differs from other familiar process simulators, such as SUPREM [6]. The equations used in FABRICS are analytical, rather than requiring an algorithm to solve sets of non-linear equations. This drastically decreases the amount of CPU time needed for process simulation.

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1. UNIX is a trademark of AT&T Bell Laboratories.

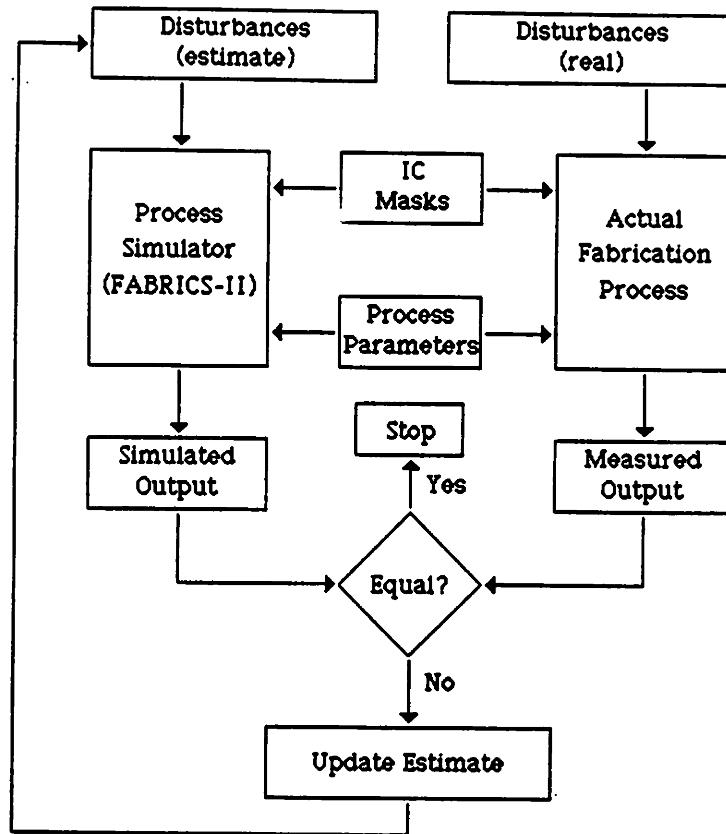

Figure 1. IC Process Characterization

Once the FABRICS output agrees with the measured output, or FABRICS is "tuned" to the process, further evaluation of the fabrication process may take place. As discussed above, device model parameters can be derived from the simulator output. A common example of this is SPICE [7] model parameters. Further along this line, a circuit may be evaluated using these derived model parameters over the range in which the process varies. In another example, a process step may be modified to see the effect on the final process parameters. This is not as drastic as increasing or decreasing the number of process steps, but changing the parameters of one or more process steps. Since deleting or adding a process step alters the disturbances, it is not allowed without retuning the simulator. A new set of SPICE model parameters, say, may be obtained with the altered process step(s). This can aid a process engineer in deciding how to modify an existing process to obtain some desired final characteristics.

To assist in tuning the simulator to a process, other supporting software has been developed at CMU. These programs include a process editor and compiler, and a statistical parameter extraction program.

The process editor and compiler, PED-PI/C, is a graphical and textual interface to allow the rapid input of process steps. The user chooses a silicon substrate of a given doping type,

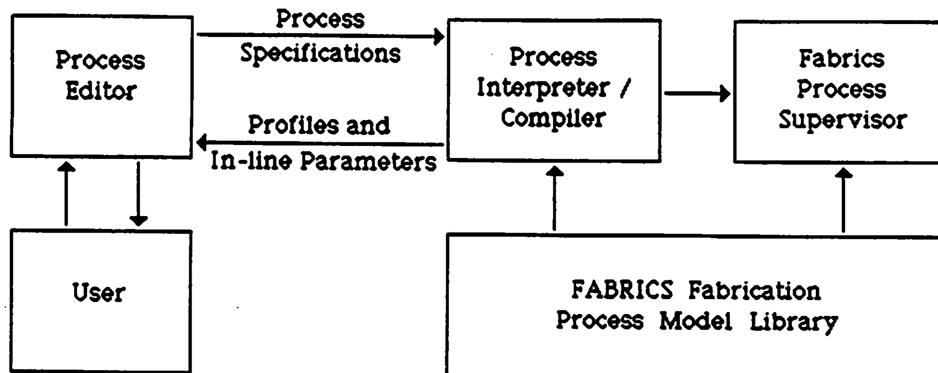

Figure 2. The Process Editor and Compiler, PED-PI/C

and then enters a series of process steps that correspond to the actual process run sheet. Examples of the process steps include etching, photolithography, ion implantation, and oxidation. These steps are chosen by a menu pick. When a process step is picked, the program responds with a textual template which gives default values for that step's parameters. Any of these values may be edited to correspond to the actual parameters used in the process. At this time an "in-line" flag may be set which immediately simulates the process up to that step and then prompts the user for a location on the mask where the in-line parameters are to be measured. Once a location is chosen, the various parameters at that point may be displayed, such as an oxide thickness, a junction depth, or a sheet resistivity. This can be helpful when adjusting the process step parameters to come close to the actual measured values.

Along with the step editor is a basic graphics editor to allow the definition of devices with a set of masks. Since only a few devices are needed to verify the process, a powerful editor is not needed.

At any time in the editing session, the designer may simulate up through a given step. The process interpreter calls the appropriate FABRICS routines for the process steps and for the redistribution of the impurities in the substrate. (See Figure 2 [3]) The results of the simulation may be viewed in a cross-section through the defined devices or in an impurity profile at a given location in the silicon. Thus, the results of the process steps may be rapidly visualized for identification and adjustment. When the designer is satisfied with the steps that have been entered, the process compiler can be invoked. This generates the c-code that will later be compiled and made a part of FABRICS. For instance, one can redefine the CMOS process (FABRICS has a default) and later when FABRICS is recompiled, this new version of the CMOS process will be the one that the simulator uses.

The next supporting program is Prometheus, the statistical parameter extraction package. The interface to Prometheus allows one to chose which input parameters will be the ones disturbed in the tuning process and the limits of the disturbance variations. It also allows the definition of which electrical and physical parameters will be the target during tuning.

For example, the diffusivity of phosphorus, the dry oxide growth coefficients, and the segregation coefficient of arsenic in Si/SiO_2 may be chosen as the input parameters to disturb, and the threshold voltage and gate oxide thickness for an NMOS device may be chosen as the output parameters. When fully tuning an actual process, a greater number of input and output parameters may be chosen. Finally, the parameters that control the tuning, such as the number of iterations, may be set by using the interface to Prometheus.

In section VI, the sequence of steps that were taken during this tuning will be described in more detail. In the next section, a description of the test chip used for obtaining the process parameters is described.

III. DESIGN OF THE TEST CHIP

In tuning FABRICS to an integrated circuit fabrication process, a number of test devices are necessary for the measurement of process parameters and the extraction of device electrical characteristics. The devices may be grouped together to form a test chip, or may be included in some excess space near or on the die of a regular chip. If the devices form a separate chip, it may be replicated across an entire wafer or it may replace a few die in selected locations on the wafer. A separate wafer containing only the test chip may be fabricated in a separate lot or in a lot with other wafers containing other chips. At UC Berkeley, the two most common methods for producing test devices are grouping devices together in a test chip and replicating it across the whole wafer, and test devices that are included along with complex circuits on the same die. In this project, a number of wafers that contained only the test chip were fabricated in a separate lot. More variation is likely to be found if test devices are measured from wafers in different lots. Due to time considerations, data could not be collected over multiple fabrication runs.

In assembling the devices needed for the tuning process, it is desirable to choose those which isolate one disturbance from another. Ihao Chen, in his report on test structure design [8], analyzes the MOS current-voltage equations and looks at how these parameters may be derived from sets of test structures. The paper describes in detail the types of measurements that may be taken to extract a full set of physical and electrical parameters to tune FABRICS to a typical NMOS process. However, some of these measurements are not practical in a fabrication facility. Some of the measurements are too time-consuming and laborious to be taken regularly in practice. In these cases, either different devices must be used, or the measurement may have to include one or more disturbances which must be separated out by the extraction package later.

The devices chosen for the test chip used in this project are a combination of features suggested by Chen and some that have previously been successfully fabricated at UC Berkeley. This chip also included a number of structures that have been regularly included on test chips in the past at Berkeley. They are used as process monitors but are not directly associated with the tuning of FABRICS. It was desired to construct a chip that would be practical for use in tuning FABRICS, but that could also be used for other purposes, such as process monitoring and data collection on the process. It is anticipated that this chip, or structures taken from this chip, will be used as the basis for the test structures on future circuits fabricated with this CMOS process. Some devices have already been used for new process development purposes.

All the electrically measurable devices on the chip were constructed using a 2 by 5 matrix of pads. These pads are 100 μm on a side and are spaced apart by 100 μm. For an example of this, refer to Figure 9 in Appendix 1. This is to facilitate measurement by automatic probing equipment. On a number of previous test structures constructed at UC Berkeley, the devices were on many different pad layouts. The pads were of various sizes, and the spacing and placement were highly irregular. This not only made manual probing of more than a few devices very tedious, but hampered statistical data collection to a great degree. On this test chip, all the devices are labeled with the structure names and device sizes to allow ease of

recognition through alignment microscopes. This proved to be a valuable addition to the chip during the measurement phase. The devices discussed below are described in additional detail in Appendix 1, with plots of the structures.

The structures and devices which are used to tune FABRICS to a CMOS process will first be presented. The devices contained on the chip include sets of NMOS and PMOS transistors. A matrix of various widths and lengths are included for each polarity device. Lengths of 25, 10, 5, 4, 3.5, 3, 2.5, 2, 1.5, 1.3, and 1 μm are used, along with widths of 400, 200, 100, 50, 10, and 5 μm. Most of these sizes had been on previous test chips, but the transistors with a length of 25 μm were added for the FABRICS tuning in order to have some devices of very long length. Some of the transistors were reconstructed to minimize possible process faults. All the devices have separate source, drain, and gate pads. This is done to insure independent control over each device during measurement, and to minimize device interaction. Suitable transistors can be chosen from the above set for the extraction of the MOS model parameters.

Sets of capacitors using various layer combinations are on the chip. The capacitors are either 290 by 290 μm square, or 300 by 300 μm square. This large size is to minimize the effects of edge capacitance. A few are diffusion capacitors which are described later. Many different capacitances may be measured with these structures, but the gate oxide capacitors of polysilicon-1 over the substrate and the p-well are of primary interest for obtaining the oxide thickness. In advanced tuning stages, the diffusion capacitors may be helpful.

The next set of devices are used for the measurement of sheet resistivity, linewidth, and spacing of a layer. The sheet resistivity devices are a 60 by 60 μm square of material. The Van der Pauw devices, for linewidth and spacing, are constructed along with these using a 15 μm-wide strip of material 100 μm long. This allows a space of 5 μm, 100 μm long, to be used for spacing extraction. The layers that can be characterized with these devices are p-well, n+ diffusion, p+ diffusion, polysilicon, polysilicon with p+ implant, polysilicon-2, metal-1, and metal-2. The polysilicon-2 and metal-2 structures are necessary for processes which include these layers.

Contact resistors with various size cuts are included. Contact hole sizes of 6, 5, 4, 3, 2, and 1.5 μm on a side are used. The contact resistance for these structures can be measured for metal to polysilicon 1, metal to p+ diffusion, and metal to n+ diffusion.

The last structures used in the tuning process are the misalignment devices. These structures measure the misalignment in the x- and y-direction. Misalignment of contact to diffusion, contact to polysilicon, metal 1 to diffusion, metal 1 to polysilicon, polysilicon to diffusion, via to metal 1, and metal 2 to via are on the chip. The structure of the polysilicon to diffusion misalignment device is noteworthy [9]. See Figure 13 in Appendix 1 for a plot of this device. The structure proposed by Chen involves a more complex measurement and evaluation. This may introduce sources of measurement error. The device presented here is much more easily measured and reduces the possible error introduced.

Structures are included which are not used for tuning, but are here for use as process monitors. Among these devices are sets of transistors with a width of 50 μm, and lengths of 10,

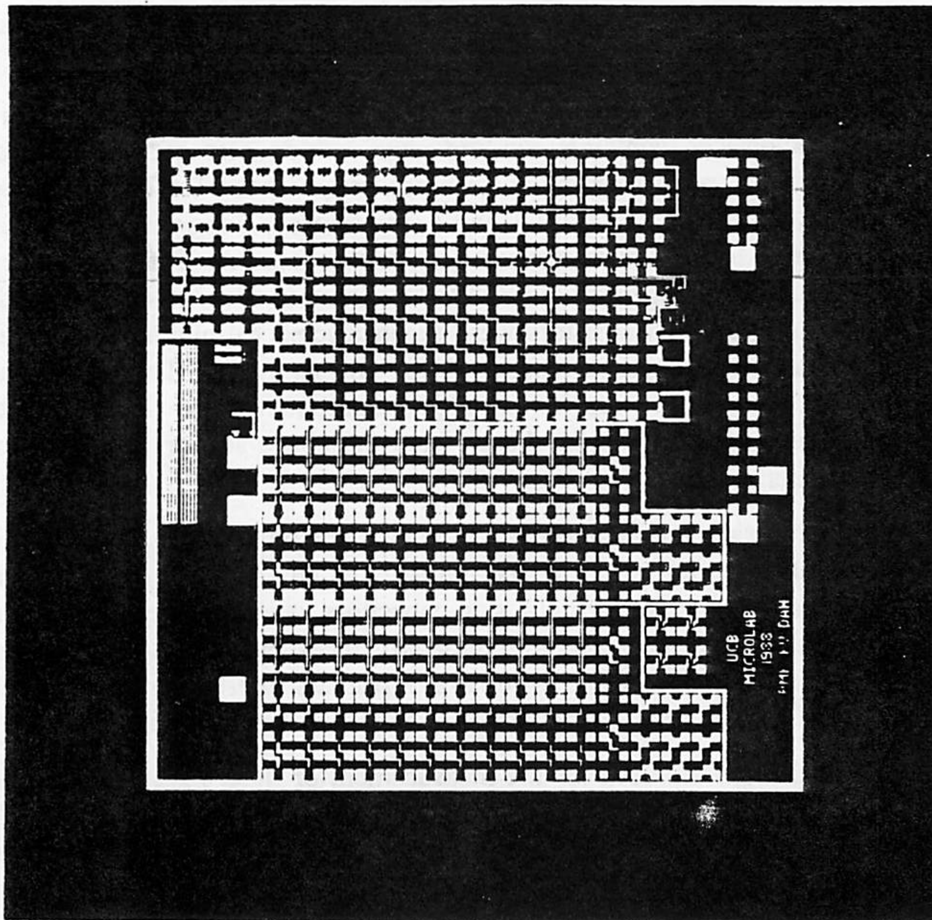

Figure 3. Photograph of the Test Chip

5, 4, 3.5, 3, 2.5, 2, 1.5, and 1 μm with large contact areas. They are used for probing the devices after contact cut to check for transistor performance during fabrication. Large devices of 100 by 100 μm over gate and field oxide with small and large contact cuts are included for field monitoring and in-process measurement.

A number of large capacitors are on the test chip. Since it is desirable to have this same chip work with processes that include a second layer of polysilicon and/or metal, the capacitors include appropriate structures for these processes. These variations on the basic CMOS process used for this project are available as tested processes in the Berkeley Microfabrication Laboratory. The layer combinations are polysilicon-1 over well (gate oxide), polysilicon-1 over substrate (gate oxide), polysilicon-1 over well (field oxide), polysilicon-1 over substrate (field oxide), metal-1 over substrate, metal-1 over polysilicon-1, polysilicon-2 over polysilicon-1, metal-2 over polysilicon-1, metal-2 over metal-1, p-well to substrate, n+ to well, and p+ to substrate. Included with these structures are three capacitors used to separate

out the sidewall capacitance of diffusions. These have 15 "fingers" of diffusion or well, with each "finger" 10 μm wide. The capacitors are n+ to well, p+ to substrate, and well to substrate.

Additional devices include large gated diodes, 250 μm on a side, to the substrate and p-well. Various size resistors for polysilicon, n+ diffusion, p+ diffusion, and p-well are on the chip. Latch-up devices with different diffusion/well spacings for process diagnosis are incorporated. Metal-2 to metal-1 via chains with a number of via size/overlap combinations which may be used to monitor the via integrity and control are included. Contact chains of metal 1 to polysilicon, metal 1 to n+ diffusion, metal 1 to p+ diffusion, and metal 1 to n+ in separate wells are on the chip, for 3, 2, 1.5, 1.3 and 1 μm contact cut sizes. Contact resistors of sizes 6, 5, 4, 3, 2.5, and 2 μm are included for metal 2 to metal 1 vias. Finally, combs of metal-1, metal-2, polysilicon-1, and polysilicon-2 over strips of diffusion and polysilicon are used to monitor the photolithography and etch steps.

Some structures are on the chip which may be used to monitor the performance of two common circuits likely to be fabricated on a regular complex circuit chip. The first of these devices is a simple operational amplifier. It requires a second layer of polysilicon for AC measurement of the circuit, and can be analyzed when the chip is used in a fabrication run on that variation of the CMOS process. CMOS inverters with three different size combinations of NMOS and PMOS transistors for circuit comparison measurements are also incorporated on the chip.

The non-electrically measurable devices include wide transistors suitable for cutting for SEM cross-sections, elbows for each of the mask layers for visual linewidth monitoring, alignment verniers, test hole patterns, and GCA alignment structures.

These devices were leveraged from previous designs to a fair extent. A number of the devices were reconstructed, and many were changed so that all devices followed a consistent set of rules. Some of the dimensions were adjusted to produce as a more optimal measurement or to reduce the potential of process faults, and the contact sizes were made uniform. For example, the misalignment devices are sized such that the width is as small as possible while still maintaining a reasonable dimension around the contact to the layer. This is done so that additional faults would not be introduced by pushing a limit on the processing. Here it can be expected that no fault will occur because the contact partially missed the layer underneath. In another example, the polysilicon to diffusion misalignment structures are made long in order to show as great a voltage difference as possible while remaining a reasonable size for on the test chip.

CIF plots of the chip and examples of the various structures are given in Appendix 1 for further reference. The connection of the pad to the device is usually obvious from the layout, and the device/structure sizes are labeled next to the structure for measurement calculations. The chip contains over 325 independent electrically-measurable devices, and the die size is 6.9 by 6.9 mm.

IV. PROCESS DESCRIPTION

The process used for the FABRICS tuning is a 2 micron, p-well CMOS process. The process uses single layers of polysilicon and metal. This process was chosen because it is the simplest of several variations of CMOS processes available at UC Berkeley. MOS devices fabricated with this process have target threshold voltages of ± 0.8V and gate oxide thicknesses of about 500 Å. In the normal course of processing, all the fabrication steps are carried out in the Microfabrication Laboratory at UC Berkeley. The processes available are described in greater detail in a report by Katalin Voros and Ping K. Ko [10].

Below is a set of steps that briefly describe the CMOS process through the contact definition step. Since the processing after these steps is all low-temperature, negligible redistribution of the impurities will occur. Thus, the metalization steps are not strictly necessary when tuning FABRICS II to this process, if tuning to the transistor parameters is of primary interest. Target values for the process are also given along with the steps.

Phosphorus Substrate
4.5×10^{14} cm^{-3}

1) Dry Oxidation
300 seconds at 1273.15 K
ρ_{O_2} : 1, ρ_{HCl}: 0

2) Wet Oxidation
600 seconds at 1273.15 K
ρ_{O_2} : 1, ρ_{HCl}: 0

3) Dry Oxidation
300 seconds at 1273.15 K
ρ_{O_2} : 1, ρ_{HCl}: 0

t_{ox} = 1000 Å

4) Annealing
1200 seconds at 1273.15 K

5) Phosphorus Implantation
1.2×10^{12} /cm^2 at 145 keV

6) Lithography
CW mask using positive resist
1.3 μm thick
150 mJ/cm^2 dose
60 seconds development time

7) Boron Implantation
3×10^{12} /cm^2 at 80 keV

8) Resist Etch
13.2 seconds at 1×10^{-5} cm/s

9) Dry Oxidation
14400 seconds at 1423.15 K
ρ_{O_2} : 1, ρ_{HCl}: 0

10) Annealing
18000 seconds at 1423.15 K

X_j (well) = 4 μm
t_{ox} = 3000 Å

11) Oxide Etch
222 seconds at 1.6667×10^{-7} cm/s

12) Dry Oxidation
1680 seconds at 1223.15 K
ρ_{O_2} : 1, ρ_{HCl}: 0

t_{ox} = 200 Å

13) Annealing
1200 seconds at 1223.15 K

14) Nitride Deposition
1.4962×10^{-8} cm/s for
1320 seconds at 1073.15 K

t_{ox} = 1000 Å

15) Lithography
CD mask using positive resist
1.3 μm thick
150 mJ/cm^2 dose
60 seconds development time

16) Nitride Etch
480 seconds at 4.1667×10^{-8} cm/s

17) Resist Etch
13.2 seconds at 1×10^{-5} cm/s

18) Lithography
CW mask using positive resist
1.3 μm thick
150 mJ/cm^2 dose
60 seconds development time

19) Boron Implantation
1×10^{13} /cm^2 at 100 keV

20) Resist Etch
13.2 seconds at 1×10^{-5} cm/s

21) Annealing
300 seconds at 1023.15 K

22) Lithography
CW mask using negative resist
1.3 μm thick
150 mJ/cm^2 dose
60 seconds development time

23) Phosphorus Implantation
5×10^{12} /cm^2 at 40 keV

24) Resist Etch
13.2 seconds at 1×10^{-5} cm/s

25) Oxide Etch
60 seconds at 3.3333×10^{-8} cm/s

26) Dry Oxidation
300 seconds at 1223.15 K
ρ_{O_2} : 1, ρ_{HCl}: 0

27) Wet Oxidation
16800 seconds at 1223.15 K
ρ_{O_2} : 1, ρ_{HCl}: 0

28) Dry Oxidation
300 seconds at 1223.15 K
ρ_{O_2} : 1, ρ_{HCl}: 0

t_{ox} = 6500 Å

29) Annealing
1200 seconds at 1223.15 K

30) Oxide Etch
60 seconds at 8.3333×10^{-8} cm/s

31) Nitride Etch
1800 seconds at 1.1×10^{-8} cm/s

32) Dry Oxidation
1680 seconds at 1223.15 K
ρ_{O_2} : 1, ρ_{HCl}: 0

t_{ox} = 200 Å

33) Annealing
1200 seconds at 1223.15 K

34) Boron Implantation
9×10^{11} /cm^2 at 30 keV

35) Oxide Etch
90 seconds at 8.3333×10^{-8} cm/s

36) Dry Oxidation
7800 seconds at 1223.15 K
p_{O_2} : 1, p_{HCl}: 0

t_{ox} = 500 Å

37) Annealing
1200 seconds at 1223.15 K

38) Polysilicon Deposition
6.2444×10^{-9} cm/s
8100 seconds at 923.15 K

t_{ox} = 4500 Å

39) Lithography
CP mask using positive resist
1.3 μm thick
150 mJ/cm^2 dose
60 seconds development time

40) Polysilicon Etch
75 seconds at 6.744×10^{-7} cm/s

41) Resist Etch
13.2 seconds at 1×10^{-5} cm/s

42) Dry Oxidation
1800 seconds at 1223.15 K
p_{O_2} : 1, p_{HCl}: 0

t_{ox} = 800 Å on polysilicon
t_{ox} = 500 Å on source and drain

43) Annealing
600 seconds at 1223.15 K

44) Lithography
CS mask using negative resist
1.3 μm thick
150 mJ/cm^2 dose
60 seconds development time

45) Arsenic Implantation
5×10^{15} /cm^2 at 160 keV

46) Resist Etch
13.2 seconds at 1×10^{-5} cm/s

47) Annealing
4500 seconds at 1223.15 K

48) Lithography
CS mask using positive resist
1.3 μm thick
150 mJ/cm^2 dose
60 seconds development time

49) Boron Implantation
2×10^{15} /cm^2 at 50 keV

50) Resist Etch
13.2 seconds at 1×10^{-5} cm/s

51) Annealing
900 seconds at 1173.15 K

52) Oxide Deposition
3.64×10^{-8} cm/s
1800 seconds at 800 K

t_{ox} = 800 Å

53) Dry Oxidation
300 seconds at 1223.15 K
p_{O_2} : 1, p_{HCl}: 0

54) Wet Oxidation
1800 seconds at 1223.15 K
p_{O_2} : 1, p_{HCl}: 0

55) Dry Oxidation
300 seconds at 1223.15 K
p_{O_2} : 1, p_{HCl}: 0

56) Lithography
CC mask using positive resist
1.3 μm thick
150 mJ/cm^2 dose
60 seconds development time

57) Oxide Etch
78 seconds at 1.1667×10^{-6} cm/s

58) Resist Etch
13.2 seconds at 1×10^{-5} cm/s

V. FABRICATION AND MEASUREMENT

A set of wafers were fabricated in the Berkeley Microlab. Ten wafers which contained only the test chip were fabricated at the same time. A total of 52 possible die sites are measurable on each wafer. All the fabrication steps were carried out here with the exception of the gate threshold implant. Since the ion implanter in the Microlab is somewhat inaccurate at lower dosage implants, it was decided to send the wafers to an ion implant service for this step. The wafers were fabricated in about four weeks time.

At the measurement phase, a number of manual measurements were taken to form the base of data from which the parameter distributions could be calculated. Ideally, most or all of these measurements would be carried out by computer-controlled automatic probing equipment. Such equipment is available in the Device Characterization Laboratory and has successfully been developed for use in a DC-measurement analysis program, the BSIM extraction system [11] [12]. This equipment also has the capability of doing AC measurements. This would be appropriate for the CV measurements necessary for tuning purposes. However, an analysis of the accuracy of such measurements, which takes into consideration the long connection lines and the close proximity of the probes on the probe card, had not been previously carried out. In addition, extensive modifications to existing measurement programs would have been necessary to develop a suitable program for the measurement of the sets of devices necessary for this project. Since these modifications were a major task, it was decided to take a smaller sample size of the parameters by manual measurement.

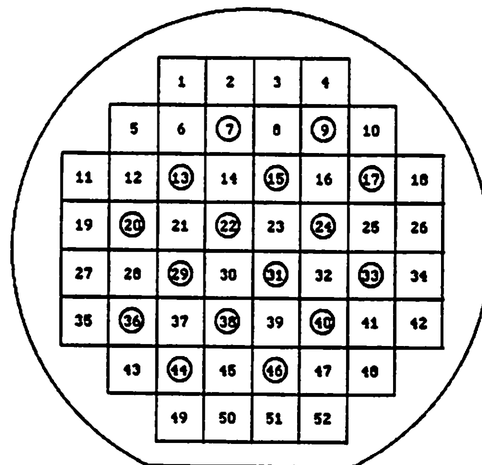

Figure 4. Example of Die Measured on Wafer

The measurements taken manually were evenly distributed across the center area of the die. An example is shown in Figure 4. The measurements were taken on alternating die sites in order to cover a reasonable sample of the devices. To calculate a reasonable sample size for a given parameter, some prior data collection is generally required. No database of measurements on devices previously fabricated using this version of the CMOS process

existed. It was decided to sample 16 of the dies within the center area of the wafer as a basis for the tuning. The equipment used for measuring the devices was a Hewlett-Packard 4280A Impedance Analyzer and a Hewlett-Packard 4145 Parameter Analyzer.

Appendix 2 is a set of data sheets used to record the measurements on the devices. Using these sheets in conjunction with the equations given in Appendix 3 [13], a complete set of parameters may be obtained for use in tuning the simulator. The resulting parameters are used in the SPICE Level 2 models [7]. In this project, FABRICS derives the SPICE models and these are compared with the measured SPICE parameters.

After fabrication it was discovered that the threshold voltage of the NMOS and PMOS transistors was different from the target values. The NMOS transistors have a threshold voltage of approximately 0.6V while the PMOS transistors have a threshold voltage of about 1.1V. The target values for these voltages is ±0.8V. The probable cause for this is a light doping of the p-well and a possible variation on the initial blanket implant and/or the threshold implant. The gate oxide thicknesses were within reasonable range (about 550 Å), and the n+ and p+ diffusions show no significant variation from target. This threshold voltage variation caused difficulty later on, not only in device parameter measurement and extraction, but more significantly in the tuning phase. For example, one of the basic measurements on the transistor parameters is threshold voltage under body bias. Some of the wafers had such light well doping that a maximum of 400 mV of body bias could be applied before the leakage current became large enough to significantly effect the accuracy of the measurement. This also made it hard to reliably measure the capacitance of the large polysilicon to p-well capacitors. The conduction of current from the well to the substrate caused the capacitance values to include unwanted parasitics, making an accurate measurement of the gate capacitance difficult. In this case, the large 100 by 100 μm transistors were biased into strong inversion and the capacitance of the gate to the source/drain/inversion layer was measured. Although this measurement is expected to be less accurate than measuring the large capacitor, it was the only repeatable measurement of the gate oxide thickness that could be made. Since other MOS parameters are derived from these values, the accuracy of the derived parameters will accumulate some error.

Nevertheless, all the expected parameters were extracted with the exception of the metal linewidth variation. The resistance of the probes to the pads caused enough variation in the final values that they could not be accepted as accurate. Although the metal linewidth variation could give additional information on process disturbances, its value is not critical when tuning the simulator for MOS transistor parameters, which is the case here.

Using the set of measurements and parameters derived from them as shown in Appendix 2, the important device electrical characteristics may be determined. When measured in the order given on the data sheets, the parameters that need to be derived may be obtained from previous measurements and parameters that have already been derived. Most of the mathematical manipulation is straight-forward.

A previous parameter extraction program for the automatic prober has since been rewritten. It is now available to be used in a more general fashion than in the past. In future

fabrications for tuning purposes, this equipment and the computer program may be used for device parameter extraction. The accuracy of AC measurements on this equipment still remains to be determined. However, the fact that the DC parameters may be taken in a much more rapid manner than the manual probing will significantly decrease the time needed to obtain the measurements. Also, it will be easier to tune the simulator from a larger database of parameters.

Along these same lines, it is possible to transfer test files from the computer which controls the automatic prober onto a mainframe computer or workstation. This facilitates the use of a computer program to calculate the device parameters automatically. It is also possible to use FABRICS in such a way as to directly match points on IV curves after taking some preliminary physical measurements. A program must be used which can plot and compare the measured and the actual IV curves. This method is more feasible when using the automatic prober and a computer for the data collection. In this project, the device parameters were calculated with a Hewlett-Packard calculator which had been programmed for the equations and iterations on equations. Although the calculator did an excellent job, a computer program would be faster, it would not require manual entry of the measurements, and the data could be entered into a controlled database for correlation and future reference.

After the electrical and process parameters were measured, the distributions for each of these parameters were calculated. This data served as the basis for the tuning phase of the project. The following is a summary of the parameters measured and calculated for the CMOS process. Figure 5 shows the directions of the misalignment in relation to the wafer flat. The transistors parameters are for MOS devices with a drawn width of 5 μm and a drawn length of 3 μm.

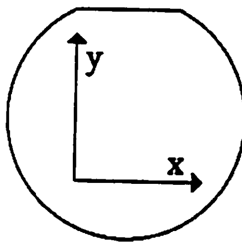

Figure 5. X and Y Directions in Relation to Wafer Flat

5/3 NMOS Transistor Parameters			
Parameter	Symbol	$\overline{x}$	S_x
Threshold Voltage	V_{TO} (V)	0.626	0.021
Gate Oxide Thickness	t_{ox} (Å)	562.79	3.37
Transconductance Parameter	K' ($\times 10^{-6}$ A/V^2)	34.64	1.00
Surface Potential	ϕ_f (V)	-0.2975	0.0059
Bulk Threshold Parameter	γ (V$^{1/2}$)	0.4108	0.0444
Flat-band Voltage	V_{FB} (V)	-0.3828	0.0416
Substrate Doping	N_{ave} ($\times 10^{15}$ cm^{-3})	1.934	0.397
Surface Mobility	μ_O (cm^2/V $\cdot$ s)	564.76	15.94
Channel Length Change	ΔL (μm)	0.296	0.088
Channel Width Change	ΔW (μm)	1.424	0.065
Depletion Layer Width	W_C (μm)	1.0803	0.1753
Source/Drain Junction Depth	X_j (μm)	0.1445	0.0724

5/3 PMOS Transistor Parameters			
Parameter	Symbol	$\overline{x}$	S_x
Threshold Voltage	V_{TO} (V)	-1.075	0.058
Gate Oxide Thickness	t_{ox} (Å)	573.47	3.01
Transconductance Parameter	K' ($\times 10^{-6}$ A/V^2)	8.78	0.14
Surface Potential	ϕ_f (V)	0.3229	0.0003
Bulk Threshold Parameter	γ (V$^{1/2}$)	0.6886	0.0005
Flat-band Voltage	V_{FB} (V)	0.0928	0.0218
Substrate Doping	N_{ave} ($\times 10^{15}$ cm^{-3})	5.176	0.051
Surface Mobility	μ_O (cm^2/V $\cdot$ s)	145.86	2.48
Channel Length Change	ΔL (μm)	1.496	0.082
Channel Width Change	ΔW (μm)	1.408	0.108
Depletion Layer Width	W_C (μm)	0.3377	0.0634
Source/Drain Junction Depth	X_j (μm)	0.0920	0.0528

Sheet Resistivity / Linewidth			
Parameter	Symbol	$\overline{x}$	S_x
Sheet Resistivity, p+ polysilicon	R_S p+ poly (Ω - cm)	24.4639	0.5818
Sheet Resistivity, n+ polysilicon	R_S n+ poly (Ω - cm)	23.6029	0.4071
Sheet Resistivity, p+ diffusion	R_S p+ (Ω - cm)	85.3626	0.5844
Sheet Resistivity, n+ diffusion	R_S n+ (Ω - cm)	36.2351	0.4620
Sheet Resistivity, p-well	R_S p-well (kΩ - cm)	6.8149	0.1724
Linewidth Variation, p+ polysilicon	ΔL_W p+ poly (μm)	-0.9169	0.1435
Linewidth Variation, n+ polysilicon	ΔL_W n+ poly (μm)	-0.8839	0.1012
Linewidth Variation, p+ diffusion	ΔL_W p+ (μm)	-0.6644	0.0475
Linewidth Variation, n+ diffusion	ΔL_W n+ (μm)	-0.7498	0.0505
Linewidth Variation, p-well	ΔL_W p-well (μm)	-0.5794	0.2212
Linewidth Variation, contact to p+	ΔL p+ contact (μm)	-0.9314	0.1872
Linewidth Variation, contact to n+	ΔL n+ contact (μm)	-0.8567	0.1024
Linewidth Variation, contact to polysilicon	ΔL poly contact (μm)	-1.0793	0.0942

Misalignment			
Parameter	Symbol	$\overline{x}$	S_x
Misalignment, polysilicon to active, x-direction	$M_{x,pol}$ (μm)	0.363	0.198
Misalignment, polysilicon to active, y-direction	$M_{y,pol}$ (μm)	-0.184	0.159
Misalignment, contact to polysilicon, x-direction	$M_{x,poc}$ (μm)	0.4094	0.2450
Misalignment, contact to polysilicon, y-direction	$M_{y,poc}$ (μm)	0.0075	0.2679
Misalignment, contact to diffusion, x-direction	$M_{x,dic}$ (μm)	-0.368	0.230
Misalignment, contact to diffusion, y-direction	$M_{y,dic}$ (μm)	0.386	0.178
Misalignment, metal to polysilicon contact, x-direction	$M_{x,met}$ (μm)	0.5363	0.2994
Misalignment, metal to polysilicon contact, y-direction	$M_{y,met}$ (μm)	-0.3463	0.2986

VI. TUNING

In order to tune the simulator, a statistical parameter extraction package is needed. The process disturbances will affect the final output of the process. Each of the physical and electrical parameters in the output has some statistical variation. The variation may depend on one or more underlying process disturbances. The challenge in making the simulator mimic the actual IC fabrication process lies in finding out what disturbances to the equations used to predict the fabrication output will make the simulator match what is actually measured. This is the function of the statistical parameter extraction package. Working in conjunction with the simulator, the extractor will run FABRICS and examine the resulting parameters. These are compared to the actual measured values. The disturbances which must be readjusted in order for the output to more closely match the real figures are determined. New values for the disturbances are calculated. FABRICS is then run with the new disturbances.

The output from FABRICS is again compared to the real figures and the process repeats. Here it is obvious why it is desirable to have a simulator in which the equations can be rapidly evaluated: the simulator is run many times in order to obtain distributions for the process and device parameters. If each simulation run was very long, this would take an unreasonable amount of time. As mentioned before, the extraction package used in conjunction with FABRICS is Prometheus, the program developed by Professor Costas Spanos while at CMU.

In tuning the simulator to a process, two steps are taken with the extraction package. First, the simulator is run to tune it to the nominal process values. Once it can match the nominal values of the parameters, it is then run to tune it to the statistical variation in those parameters.

Initially when using the process editor (PED), by using the in-line options and the cross-section plotting capabilities, the user can examine how close the simulator is coming to the actual values. An example is the initial oxidation growth step. As the wafers are being run through the fabrication line, intermediate values may be available to the process engineer. By editing the file PED references for the coefficients to the process equations it uses, one may "pre-tune" FABRICS to the mean value. Before reaching the final tuning phase of the project, one could already have pre-tuned the process to some of the initial and intermediate process parameters, thus reducing the complexity of the problem for Prometheus to handle. This method is discussed in a paper by Mozumder, Strojwas, and Bell [14].

In this project, the wet and dry oxide growth coefficients were initially pre-tuned using measurements taken during fabrication. This allowed the program to already predict oxide thicknesses for the important parameters, such as the gate oxide thickness to within 5% for the nominal case. This was done by adjusting the oxide growth coefficients and using the in-line option in PED to measure the oxide. Prometheus may also be used for the pre-tuning.

Another area in which the user has control over the extraction process is in the disturbances which are adjusted in the tuning process. CMU has added a menu-driven interface on to the Prometheus package which simplifies, to some extent, the specification of the input and output parameters for Prometheus. For example, the user can specify the input

parameters which are to be manipulated during the extraction process, the mean value of these parameters, and the bounds about which Prometheus will search for values when they are disturbed. The output parameters may also be specified. One may choose any number of the parameters to tune to. For example, the threshold voltage of the N and P transistors may be used initially to see how close the program will match the actual process. Later tuning phases may tune to all the transistor parameters. The input parameters which are to be disturbed should be chosen such that they correspond to the output targets. Although all the input parameters may be chosen, those which are known not to influence the outputs under consideration should be eliminated in order to help Prometheus separate out which are important. This can significantly speed up the computation, although Prometheus should come up with similar results in either case.

When tuning the simulator using the extraction package, the first step is to tune to the nominal case. This involves entering the nominal values of the measured process parameters and instructing the extraction package to only tune to the deterministic case. Since there had been the problems with the light implantations during fabrication, another additional difficulty was introduced to the problem. Implantation doses and energies were given to the process editor when constructing the process recipe. The NMOS threshold voltage was low and the PMOS threshold voltage was high because one or more of the actual implants were different from the target value as discussed in the measurement section. However, manually adjusting three or four implant values in order to come up with a threshold voltage for both N- and P-channel transistors while maintaining the other transistor and device parameters is very difficult, if not next to impossible. It is possible to run Prometheus in this mode to search for process parameters which will fit given output measurements rather than doing adjustments by hand. However, FABRICS is depending on the doses and energies given to the simulator to be very close to the actual value. If this is the case, adjusting the equation coefficients should be enough to bring the simulated output into agreement with the measured output.

First, no adjustments were made to the specified implantation values. Prometheus was run on the nominal process parameters for both NMOS and PMOS transistors. The initial attempt was to tune to just a few of the major transistor parameters, such as the threshold voltage, the transconductance parameter, K', and the gate oxide thickness. It had some difficulty extracting the device parameters. Most likely this was due to the implant values being different from the actual values when the wafers were fabricated. The gate oxide thickness was close to the actual value, and this was expected due to the pre-tuning.

Some minor adjustments were then made to the implant values, and the extraction was run for only the NMOS or PMOS values alone. This approach was somewhat successful, especially considering the possible solution space to the problem. The program could get the threshold voltage to under 5% error from the measured nominal value with the transconductance parameter over 100% off. Again, it could adjust the inputs so that K' was under 5% in error with V_{TO} over 75% in error.

Some final adjustments were made to the implant values, and Prometheus was run on both NMOS and PMOS transistors. The output parameter targets were the threshold voltage, the gate oxide thickness and the transconductance parameter. One oxide etch step was also

changed to see how this would effect the final parameters, since there will be some segregation of the impurities into the oxide. In this case, the oxide thicknesses could be predicted to within 15% error from the measured values, the PMOS V_{TO} to within 7%, the PMOS K' to about 40% error, the NMOS V_{TO} to about 30% error, and the NMOS K' to under 4% error. It was clear that since the implant values were significantly different from the values input to the program, that it would be much more difficult to tune even to the nominal process case.

At this point in the tuning process, after the deterministic case is solved by Prometheus, statistical variation would be introduced into the problem, and the package would adjust for matching with the statistical variation. This was not possible with this project, since time was limited and the deterministic case had not been completely solved. The oxide thicknesses for the deterministic case were matching to under 5%, and the threshold voltage could be simulated to within 5%, but with the KP being very far away from the measured value, it did not make sense to continue to try to match the other transistor parameters.

Since the simulator could not match the measured parameters, but the actual values used for some of the process steps were suspect, a firm conclusion on the ability of the simulator's equations to match the processing at UCB could not be reached. Time did not permit adjustment of the equations used to model the process steps to see if they would permit a closer match to the actual fabrication process.

VII. CONCLUSIONS

The goals of this project were to see what is involved in tuning FABRICS to a CMOS process at UC Berkeley, how well the simulator can match the actual fabrication process, and to see how best the simulator can be integrated with the other CIM tools in development here.

This project laid a strong foundation for future work with the simulator. First, the software was brought up on the system, through several revisions from CMU in the time from the beginning of this project to the end. A number of details in taking the software through the whole process of defining the process steps in the editor to recompilation and linking up of the new CMOS version were noted.

Next, a test chip was constructed for purposes of tuning, process evaluation, and monitoring. This chip is currently in use at UCB, and structures from it have been transferred to other test chips for process development. This chip leveraged from previous chips done at UCB, but also refined structures that were known to have problems, and added all the structures necessary for tuning the FABRICS simulator to a one- or two-level metal and one- or two-level polysilicon process. Further, all the structures were put on a common grid system, simplifying the measurement procedure for any future manual measurements. More importantly, the common grid system allows the use of one probe card and the automatic prober to collect statistical data from the chip. It is anticipated that much use will be made of the chip in future wafers fabricated in the UC Berkeley Microlab.

The process steps were input into the simulator and refined. A few bugs in the software were encountered and were brought to the attention of the programmers at CMU who rapidly found and fixed them. This has the benefit of increasing the overall dependability of the program as it now stands.

A measurement procedure was defined and tested which sets up the protocol for future measurement and extraction. Any future work can use this as a template for the parameters needed and the order in which they can be extracted.

The statistical simulator was recompiled with the new CMOS version which reflects the UCB CMOS process. The statistical extraction interface and package were exercised with the measured parameters. The goal of seeing what is involved in order to tune the simulator to a process at UCB was reached. The majority of work involved in order to do this again to the same process or a slightly modified process has been completed.

The simulator was unable to match the UCB fabrication process. However, because of the problems with the doping, and not knowing exactly where the actual fabrication deviated from the process specifications and by how much, it cannot be concluded that the process simulator cannot imitate the process. In fact, since the oxide thicknesses and at least a few of the device characteristics could be matched, it can be said that the simulator can match the fabrication process to a fair extent. Due to time constraints, another set of wafers could not be fabricated, measured, and the parameters entered into the extraction package for tuning. In order for this to be done, however, a minimum amount of development time needs to be invested. The existing masks can be used for the fabrication, the automatic prober and

program are now able to be used, the procedure and plan for measurement is in place, and FABRICS is recompiled with the Berkeley CMOS process.

Through using this program the CIM group has a good idea of the capabilities, needed inputs, and resulting outputs from the program. It can now be evaluated in the context of how it will fit into the integration of new and existing CIM tools at UCB.

The goals of the project were met as close as possible within the time allowed for the project. The author learned much about test structures and processing. A number of software issues had to be dealt with throughout the time of the project. Overall, the project has been worthwhile, a good learning experience, and it is hoped that others will be able to benefit from the work done here.

VIII. APPENDIX 1: TEST CHIP REFERENCE

Introduction

This appendix documents and explains the use of the test chip constructed for the purpose of tuning FABRICS II, a statistical process and device simulator, to a CMOS process at UC Berkeley. Although the test chip was used for tuning the simulator, many of the devices are general process test structures which can be used for other purposes. In addition to these devices, test structures were added for process monitoring and diagnosis. The chip can be used for one- or two-level metal, and one- or two-level polysilicon variations of the basic CMOS process. Most of the structures are self-explanatory. No attempt is made to address the theory behind the structures.

This test chip is a variation of previous test chips done at UC Berkeley [9] [10]. Many of the structures were taken from a former test chip and modified for use here. Some devices were reconstructed to minimize possible process faults. Contacts to the structures were made a uniform size (except when the structure requires different contact sizes as part of its purpose). Devices were added for tuning FABRICS. A noteworthy difference between this chip and most previous chips is the placement of the pads. In order to facilitate automatic probing of the devices, the structures were constructed using a 2 by 5 grid of pads. Although the automatic prober was the motivation for this setup, it also greatly facilitates manual probing of the devices. Use of this grid of pads is highly encouraged for future test device development. Another distinguishing feature of this test chip is the labeling of all the devices. This is usually done to some extent on all chips. Labels are included on this chip for the device function, the relevant layers involved (or an abbreviation), and the device sizes. This helps in locating the devices under a probing microscope. Labeling of future test devices is also highly encouraged.

The 2 by 5 grid of pads was used for the electrically measurable devices. These pads are 100 μm on a side, and are spaced 100 μm apart. Pads may be reliably made as small as 80 μm square for automatic probing purposes, but some margin was included for safety. For chips which will be manually probed, the pads may also be smaller than 100 μm on a side, but then more time must be spent on adjusting the probes to contact the pads. There is a trade off between area and time involved in probing. This must be decided by available area on the test chip. The same can be said for the use of the common grid system for the pads. For new test chip development, it is advised to check with the Microlab staff as to which probe cards are available for use with the Electroglas Probe Station. Doing this early in the chip development stage will allow the designer to either use a suitable pattern and a probe card that is already available, or to decide on a pad placement pattern and order the card(s) early enough so that they are ready before the measurements must begin.

The test chip is 6900 μm on a side. The overall area is also a major consideration for future test chips. Allowed chip area, due to the aperture limitation of the GCA wafer stepper, is 1 cm x 1 cm.

The first run of this test chip was named CMOS12. Use this designation when inquiring of the Microlab staff for the chip information. A magnetic tape with the structures in KIC format is available which may be borrowed. The structures may also be in a directory on one

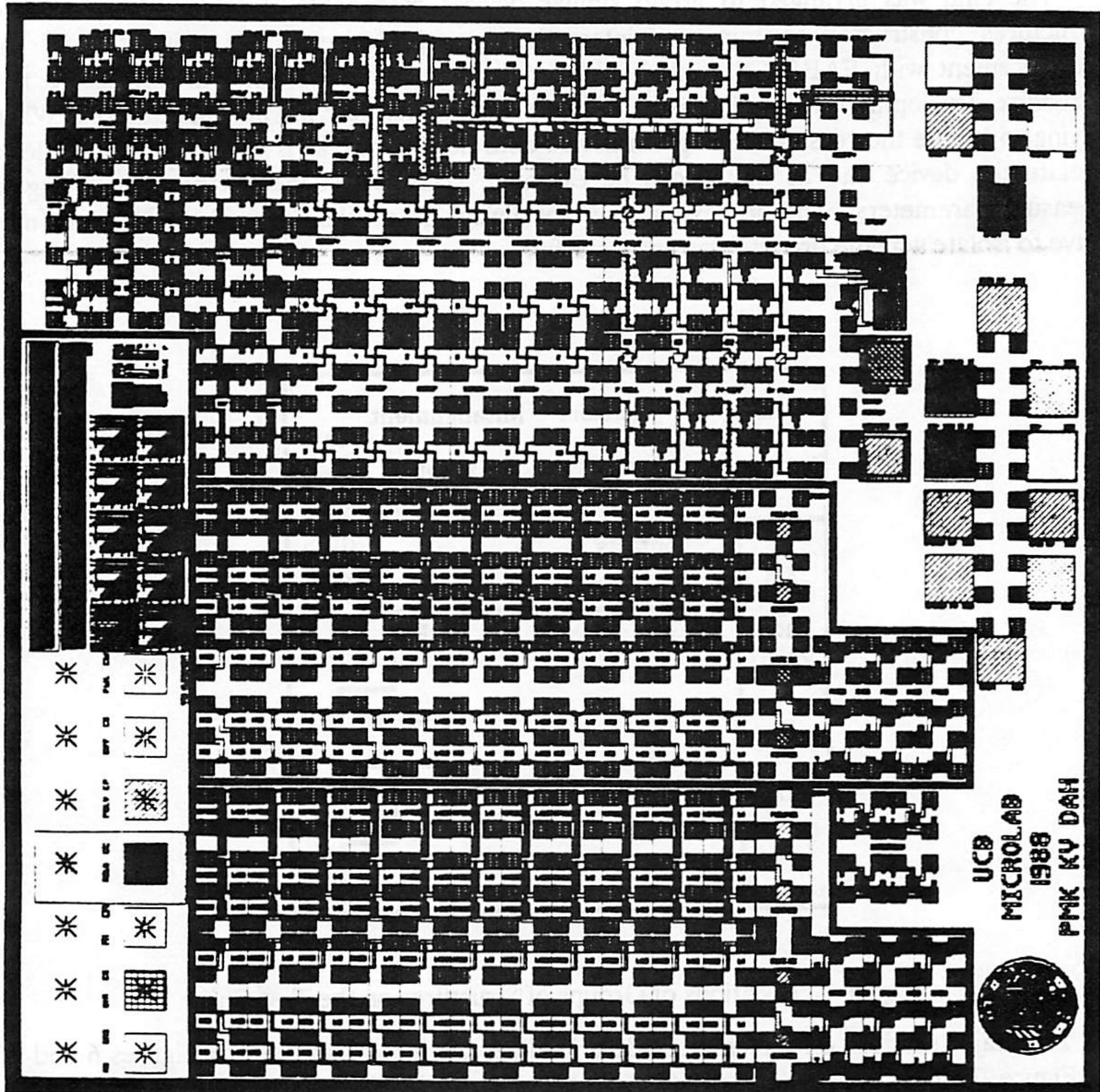

Figure 6. Plot of the Test Chip

or more computers. If the designer intends to use some of these structures, or needs to view them, check with the Microlab staff as to how they may be obtained. Note that they can easily be translated into CIF (Caltech Intermediate Format) if an application uses this format.

Test Chip Overview

The chip was arranged to group similar devices reasonably close together, and the structures constructed to minimize interaction among devices. This was essential for measurement with FABRICS, and should be taken into consideration in any future test structure development to see if it is a necessary requirement for the new application. When trying to isolate the reason that a given device does not operate as is expected, being able to isolate the device and its inputs can be essential. This is also necessary when trying to measure parameters. The processing may not always go as planned and the de-igner may have to isolate why the process was unsuccessful.

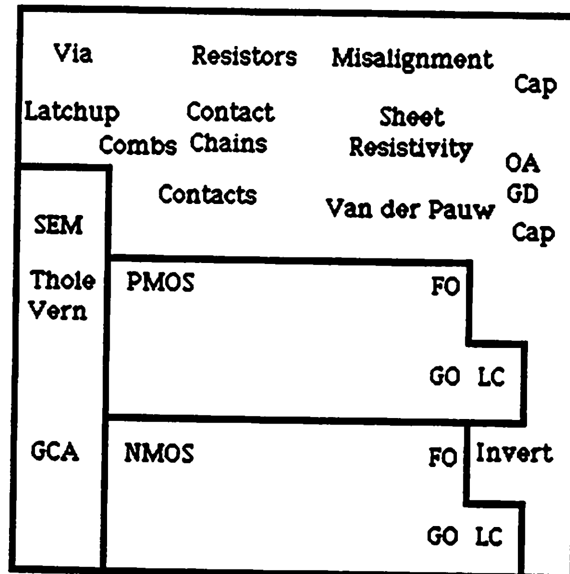

Figure 7. Locations of Groups of Structures on the Test Chip

The major sections on the chip are described here. Please also refer to Figures 6 and 7. In Figure 7, the abbreviations used are OA for operational amplifier, GD for the gated diodes, FO for the large field oxide devices, GO for the large gate oxide devices, and LC for the transistors with large contact openings. Starting in the upper left corner, the first row contains metal-2 to metal-1 via chains using different layout rules on overlap of metal-2 and metal-1 around the via area, and different via cut area. (Figures 8 and 9) Next to these are sets of large resistors for the diffusion layers, well and polysilicon. (Figure 10) To the right are misalignment resistors in the x- and y-directions. (Figures 11, 12, and 13) The various misalignments of the masks from polysilicon over active area on up to the metal-2 layer can be obtained from these devices.

In the second row, a set of latch up devices with different spacings between the well and diffusion is first. (Figure 14) Next to these devices are some metal-1 and metal-2 combs over

strips of polysilicon and diffusion. Similarly, combs of polysilicon, layers 1 and 2, are found. (Figure 15) Next to the combs (continuing in this row and the row below) are contact chains of metal-1 to the various layers it might contact: p+ diffusion, n+ diffusion, polysilicon (layer 1), and p+ in the p-well. (Figure 16) Continuing to the right in these two rows, are individual contacts from metal-1 to the various layers it might contact. (Figures 17 and 18) Near the contact resistors are Van der Pauw resistors and sheet resistance structures. The Van der Pauw structures are modified structures allowing the measurement of both the linewidth and spacing variation of the layer. (Figures 19 and 20) The final structures on the end of these two rows are an operational amplifier using the second layer of polysilicon for capacitors (Figures 21 and 22), and a set of gated diodes in the well and substrate (Figure 23).

Below the first two rows, along the left side of the chip, is a section of visual structures for alignment and visual verification of the process. These are: two wide transistors for SEM cross-section evaluation; hole patterns to test for via hole etch integrity; verniers for visual offset measurements of one layer over another; elbows for visually measuring linewidth/space integrity; and a set of clear and dark field alignment marks for the GCA wafer stepper. (Figure 24)

The next large section in the middle of the test chip to the right of the visual alignment devices is a matrix of PMOS transistors. (Figures 25 and 27) To the right of this matrix is a column of large devices 100 μm wide and 100 μm long. Two are over field oxide and two are over gate oxide. (Figures 28 and 29) To the right of these devices, on the bottom of the two rows, are nine devices, each with a width of 50 μm. They have large contact cut holes to allow for probing during processing. (Figure 30)

Just below this set of PMOS transistors is a similar set of NMOS transistors. (Figure 26) The same sizes and placement as the PMOS devices are found for these transistors.

Along the right side of the chip are capacitors and inverters. There are 15 capacitors of either one layer over another, or of a diffusion-type capacitor. (Figures 31, 32, and 33) The inverters are the last devices towards the bottom on the right side. They are regular CMOS inverters with different transistor sizes. (Figure 34)

Detailed Explanation

In this section, a more detailed explanation of some of the devices will be given, to explain layer combinations, or the sizing used (particularly on some of the via structures). The groups of structures are discussed starting in the upper left corner of the chip.

Metal-2 to Metal-1 Via Chains - Figures 8 and 9

There are two basic kinds of structures here. The first is where metal-1 is just over field oxide, and the second where metal-1 is over a layer of polysilicon. The numbers near the common pads (two of the pads are common in each set of ten pads) are the overlap of metal-1 and metal-2 around the via cut. The number near the other pads is the size of the via cut. For example, on the structure in Figure 9, one of the common pads is labeled 2 - 5. This means there are 2 μm of metal-1 surrounding the via cut, and 5 μm of metal-2 surrounding the via. The numbers near the pad just above it are 4 3. The via cut is 4 μm wide and 3 μm long. Near the pad just above this one is the number 3. The via cut is 3 μm long and wide. There are a number of different via size and overlap combinations. Each chain has 20 contacts. On the last two chains are some via resistors from metal-2 to metal-1 and back (two total via cuts) with the sizes marked near the vias.

Resistors - Figure 10

The resistors are long resistors with the length and width marked near the pads.

Misalignment Devices - Figures 11, 12, and 13

The misalignment devices are used to measure the misalignment of one mask to another layer below it. Using all of these misalignment structures, and measuring first the misalignment of polysilicon to the active area, the overall misalignment of any mask above the active mask can be calculated, using appropriate calculations and the values measured. The exceptions are the p+ or n+ implant mask, since these are oversized to fully cover the active cut openings. The structures are appropriately labeled to reflect the misalignment being measured, e.g. CON POLY measures the misalignment of the contact mask to the polysilicon mask. The length of the layer is near the pads which probe it (70 or 140 μm). The 140 μm is constant in all cases, and the 70 μm is the distance between the probe points to the layers if alignment was perfect. The smaller number, 7, is the drawn width of the layer being probed in μm. The device in Figure 13, of a somewhat different structure, is the polysilicon to active area alignment pattern. The probes are spaced 400 μm apart (the length) and 4 μm is the drawn width, if alignment was perfect. A sheet resistivity structure was added to this device, since some extra pads were available.

Latch-up Devices - Figure 14

The latch-up devices were originally constructed by Hans Zappe. The notation near the pads is the designation of the layer that is being contacted. "W" is contact to the well, "p" is the contact to p+, and "n" is the contact to n+. Lat2 stands for 2 μm spacing between the diffusions and well in the substrate, and Lat3 stands for 3 μm spacing.

Metal and Polysilicon Combs - Figure 15

The metal and polysilicon combs are used to test for continuity and the integrity of the etch process. Two combs are found for each of the layers. The layers cross over strips of diffusion and polysilicon to vary the vertical topology. Two combs are found for each of the metal-1, metal-2, polysilicon-1, and polysilicon-2 layers. One comb is with 3 μm lines and 3 μm spacing between the lines, the other is with 2 μm lines and spacing.

Contact Chains - Figure 16

The contact chains are to test for contact continuity from metal-1 to the various layers it may contact. These layers are p+ diffusion, n+ diffusion, polysilicon-1, and p+ in the p-well. The number next to each pad is the size of the square contact. The p+ diffusion, n+ diffusion, and polysilicon chains have 16 contacts in each chain. The chain to p+ in the p-well has 10 contacts in each chain.

Individual Contacts - Figures 17 and 18

The individual contacts are used to measure the resistance of a single contact. The contacts have different cut sizes, ranging from 1.5 to 6 μm. Usually, 2 or 3 μm contacts are used for this process for reliability. The 1.5 μm contacts were included for a check for the etch on this size. The layers contacted are p+ diffusion, n+ diffusion, and polysilicon. Included is a set of metal-2 to metal-1 via cuts, from 2 to 6 μm cut sizes.

Van der Pauw Resistors and Sheet Resistance Devices - Figures 19 and 20

The Van der Pauw resistors are used to measure the linewidth and spacing variation of the layer. These were constructed so that the sheet resistance can be measured at the same time as the Van der Pauw resistor, using a probe card. This may allow a computer program to automatically calculate the linewidth and spacing of the layer without an intermediate step.

Operational Amplifier - Figures 21 and 22

The original operational amplifier layout was done by K. Y. Toh. It uses the second layer of polysilicon for the capacitors. Figure 22 is the circuit diagram, which was extracted from the layout.

Gated Diodes - Figure 23

There are two gated diodes; one in the substrate (p+/n) and one in the p-well (n+/p).

Visual Alignment and Visual Verification Structures - Figure 24

These structures are included as standard devices on most of the UCB chips. Elbow line/space sizes increase from 0.5 μm to 2 μm in 0.25 μm increments; after that the sizes are 2.25, 2.5, 3, 3.5, 4, and 5 μm. The square hole sizes increase from 1 μm to 10 μm in 1 μm increments.

PMOS and NMOS Transistors - Figures 25, 26, and 27

NMOS and PMOS transistors are laid out in two identical matrices. Transistors with widths of 400, 200, 100, 50, 10, and 5 μm are constructed along the rows of the matrix. Composing the columns are devices having lengths of 25, 10, 5, 4, 3.5, 3, 2.5, 2, 1.5, 1.3, and 1 μm for each row of different width. Included with each grid of pads is a pad to contact the substrate or well.

Large Field and Gate Oxide Transistors - Figures 28 and 29

Large transistors over gate and field oxide are placed to the right of each matrix. Each device is 100 μm wide by 100 μm long. There are two versions of each field and each gate oxide device. One has regular-sized contacts, and the other has large contacts to allow the probing of the devices during processing, just after the contact etch.

Transistors with Large Contact Cuts - Figure 30

A set of devices with large contact cuts, for probing after the contact etch step, are included to the right of the large devices. The transistors all have a width of 50 μm, and lengths of 10, 5, 4, 3.5, 3, 2.5, 2, 1.5, and 1 μm.

Capacitors - Figures 31, 32, and 33

Capacitors with various layer combinations have been included on this chip. Most of the capacitors are either 300 or 290 μm on a side. This is to minimize the effects of edge capacitance. The rest are structures used to measure sidewall capacitance, and are composed of 15 "fingers" of diffusion, with each "finger" being 10 μm wide and 300 μm long. The capacitances that can be measured are polysilicon-1 over well (gate oxide), polysilicon-1 over substrate (gate oxide), polysilicon-1 over well (field oxide), polysilicon-1 over substrate (field oxide), metal-1 over substrate, metal-1 over polysilicon-1, polysilicon-2 over polysilicon-1, metal-2 over polysilicon-1, metal-2 over metal-1, p-well to substrate, n+ to well, and p+ to substrate. The sidewall capacitances that can be measured are n+ to p-well, p+ to substrate, and well to substrate.

Inverters - Figure 34

Three different inverters, constructed of different device sizes are the last set of structures to be described. The NMOS transistors are all 50 μm wide, with the PMOS devices twice the width, 100 μm. All transistors have lengths of 1.5, 2, and 3 μm.

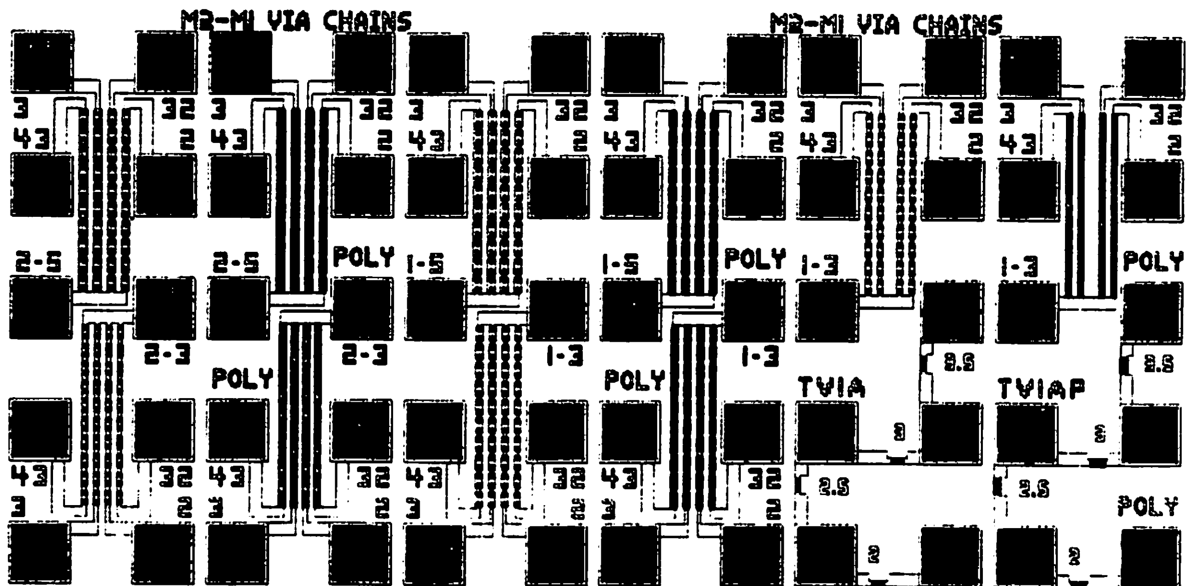

Figure 8. Metal-2 to Metal-1 Via Chains

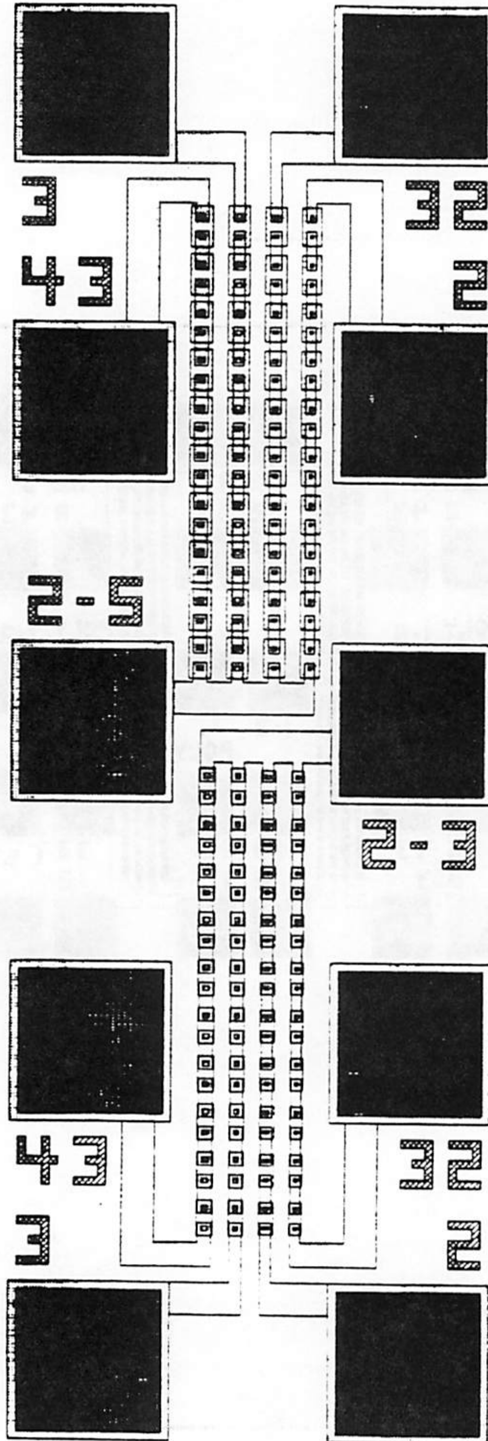

Figure 9. Metal-2 to Metal-1 Via Chain Example

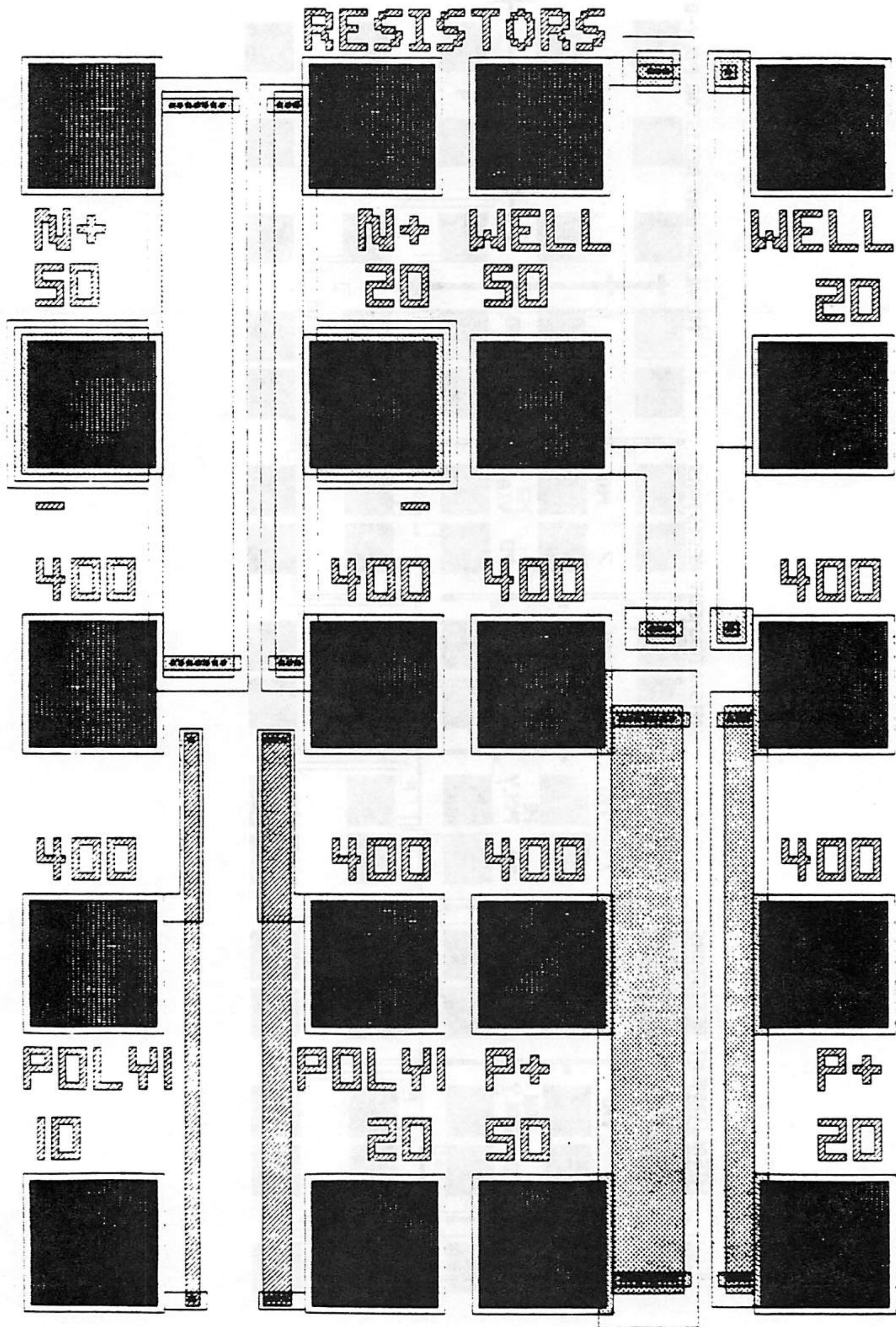

Figure 10. Resistors

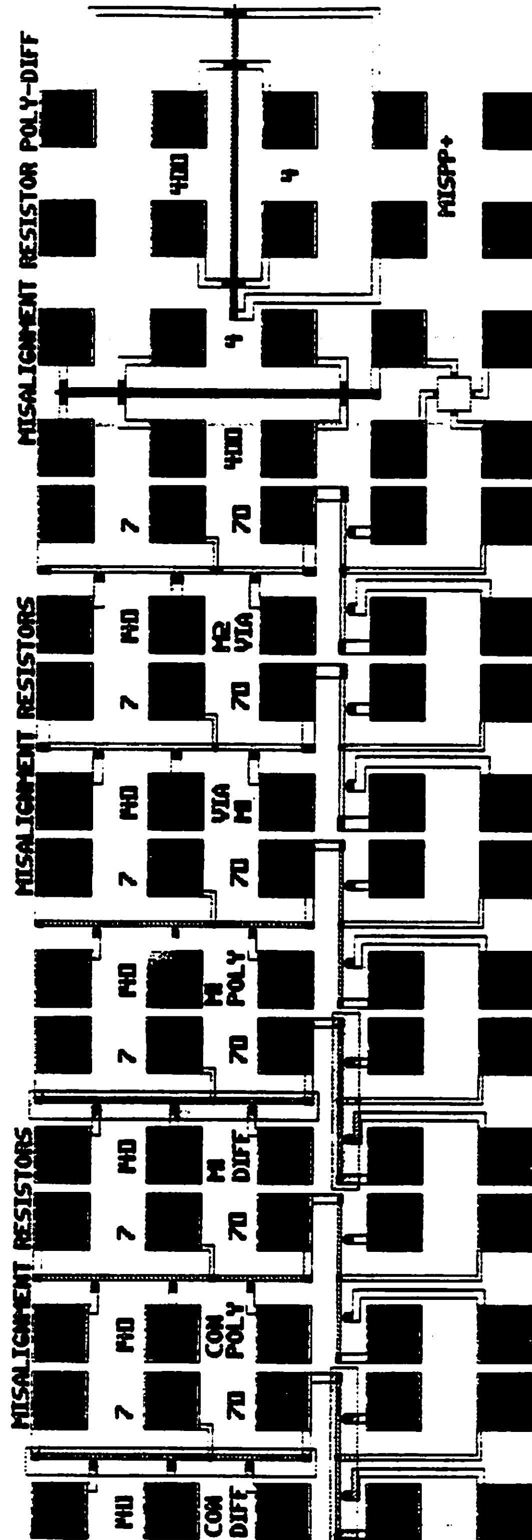

Figure 11. Misalignment Resistors

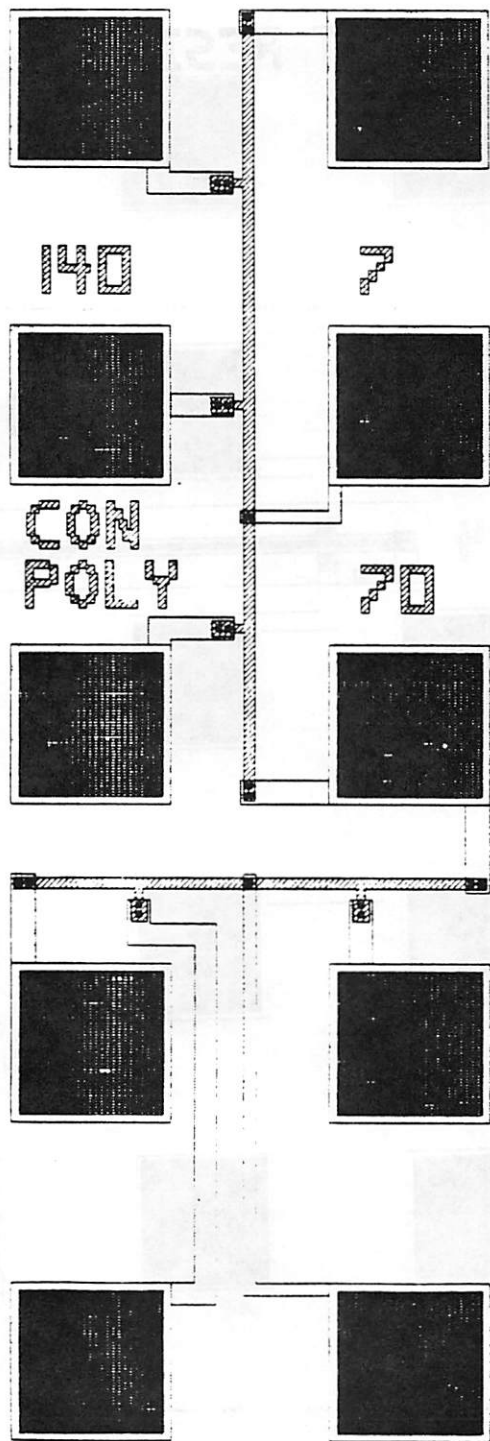

Figure 12. Misalignment Resistor Example - Contact to Polysilicon

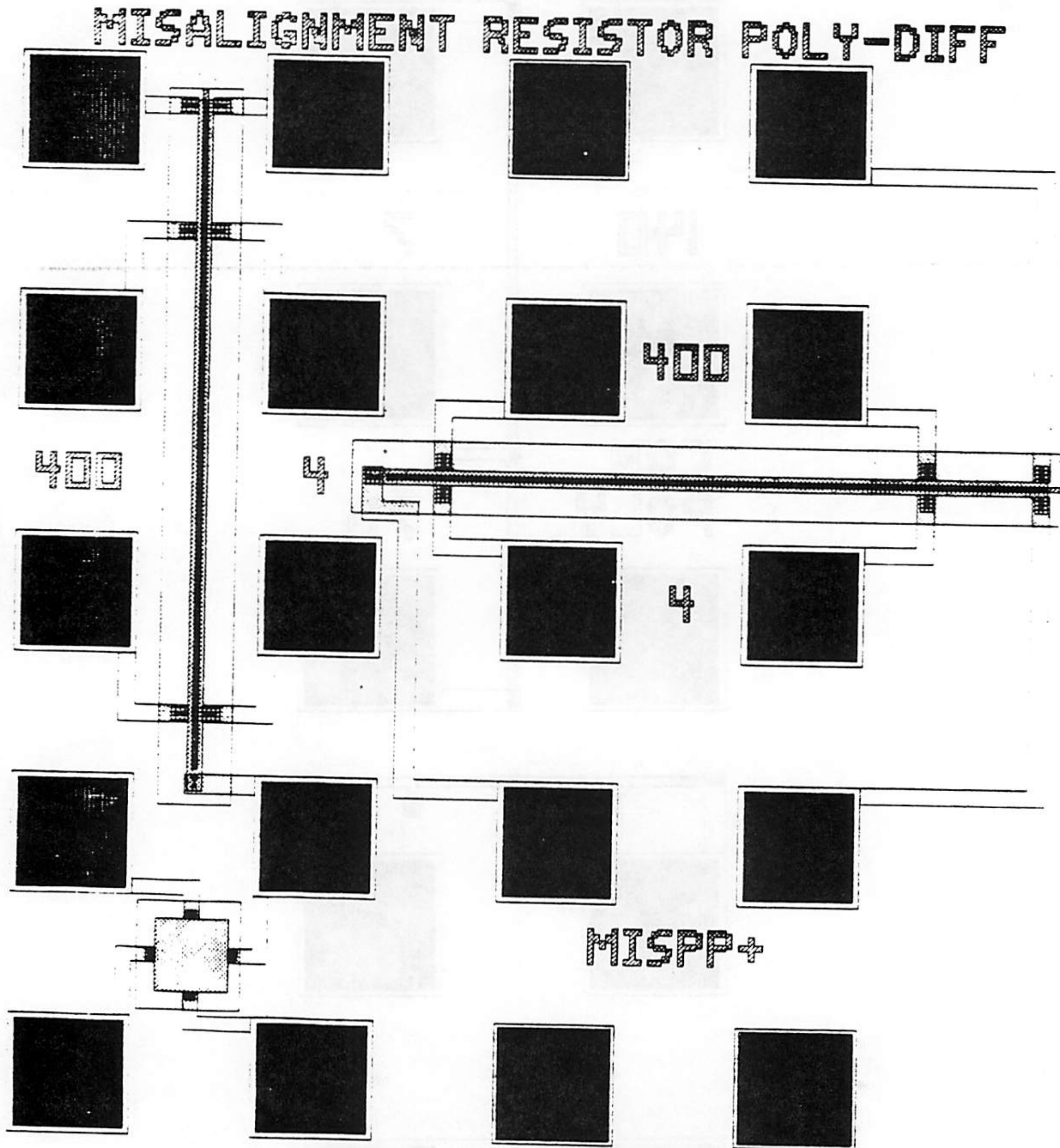

Figure 13. Polysilicon to Active Area Misalignment Resistor

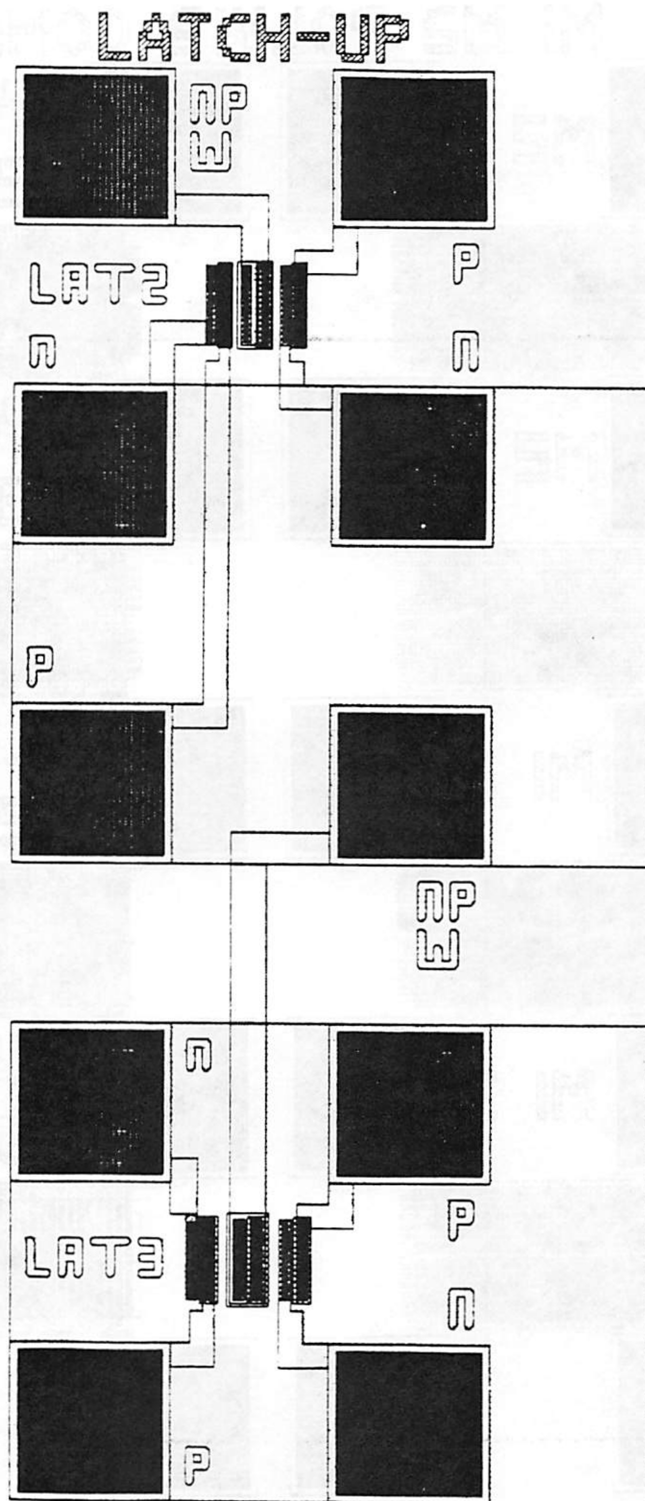

Figure 14. Latch-up Structure

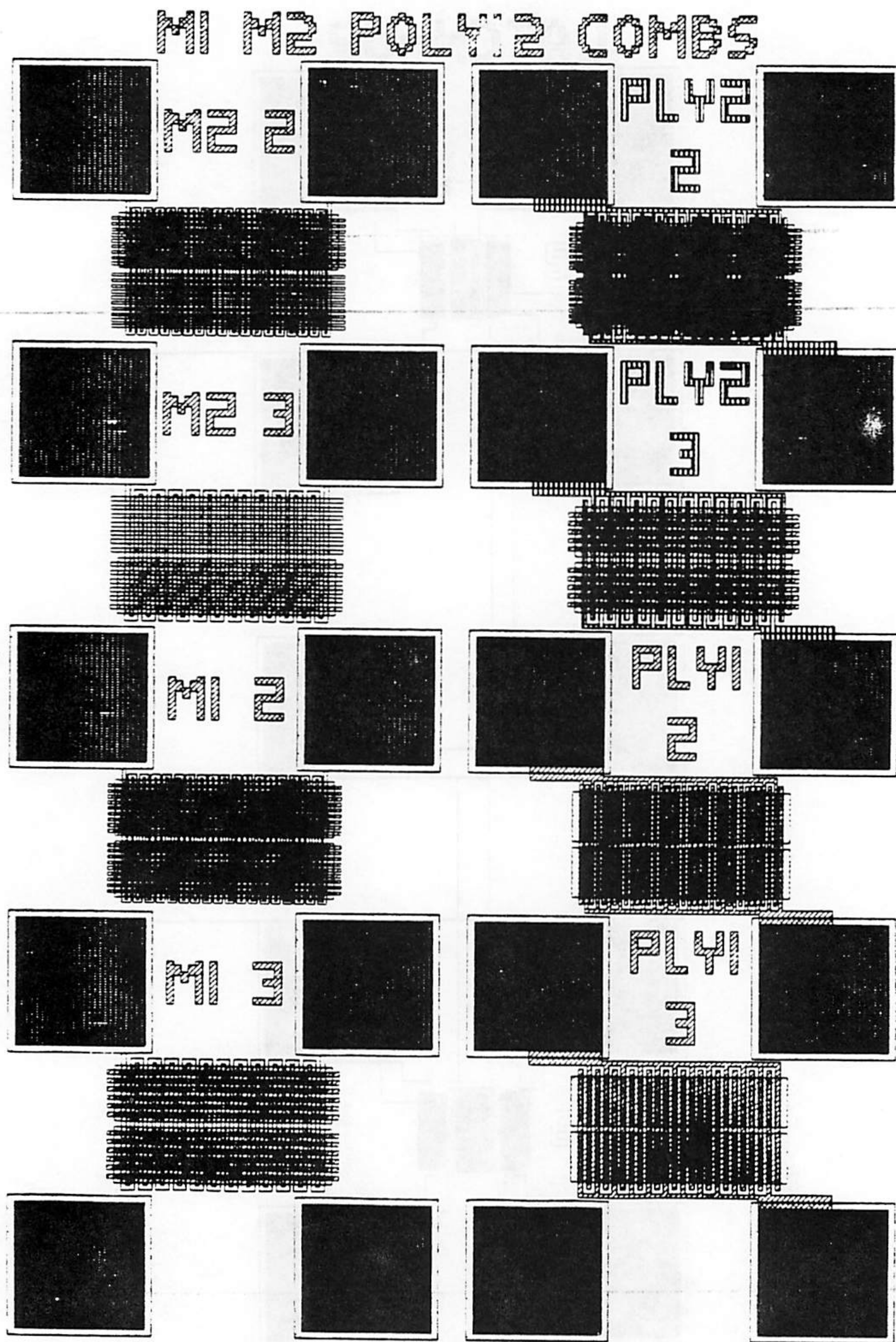

Figure 15. Metal and Polysilicon Combs

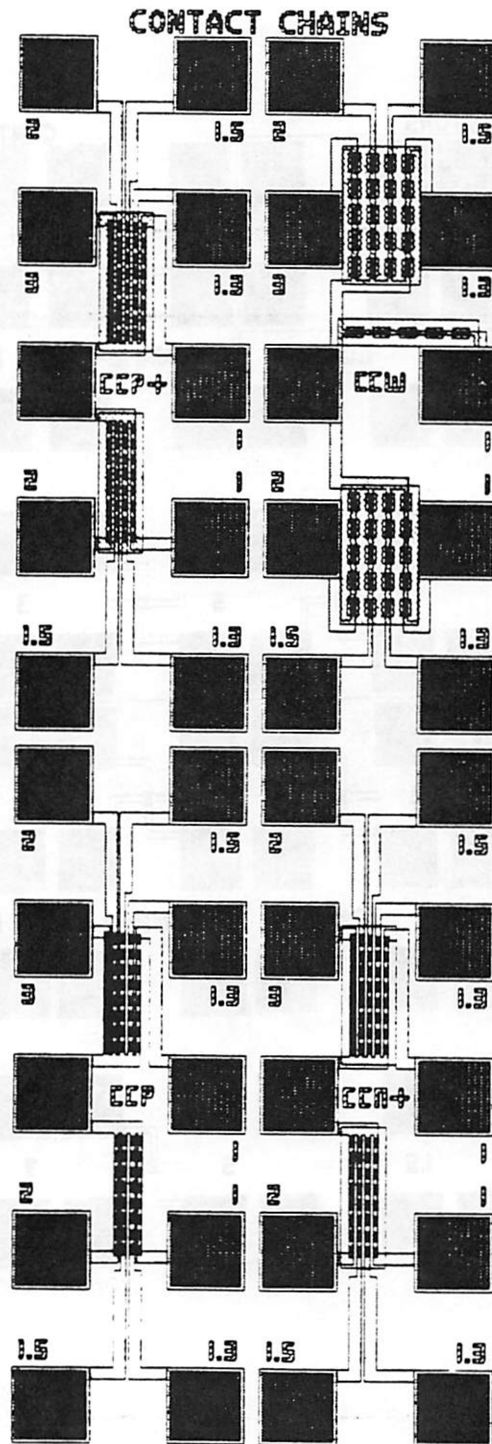

Figure 16. Contact Chains to Polysilicon and Diffusion

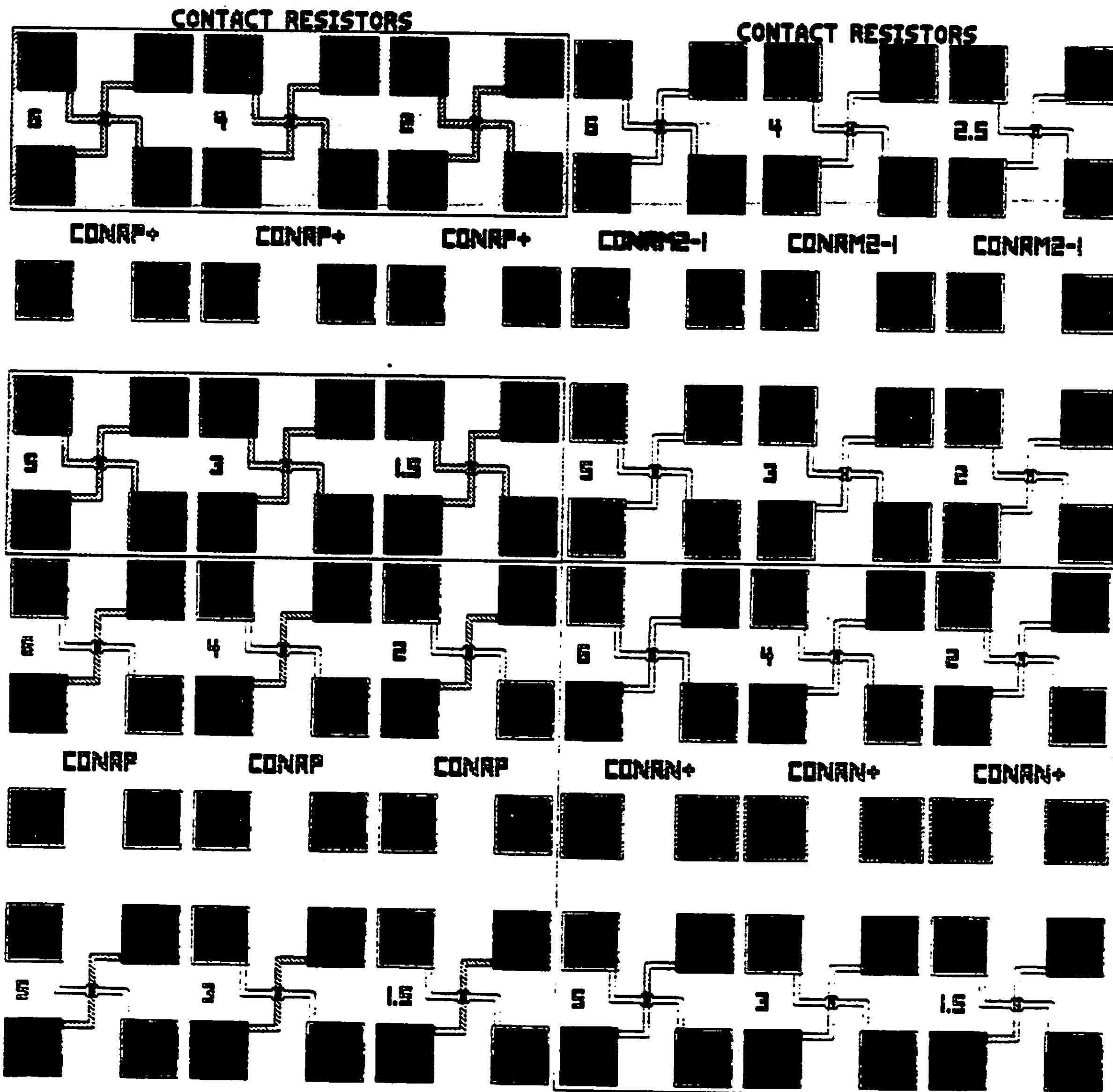

Figure 17. Individual Contacts

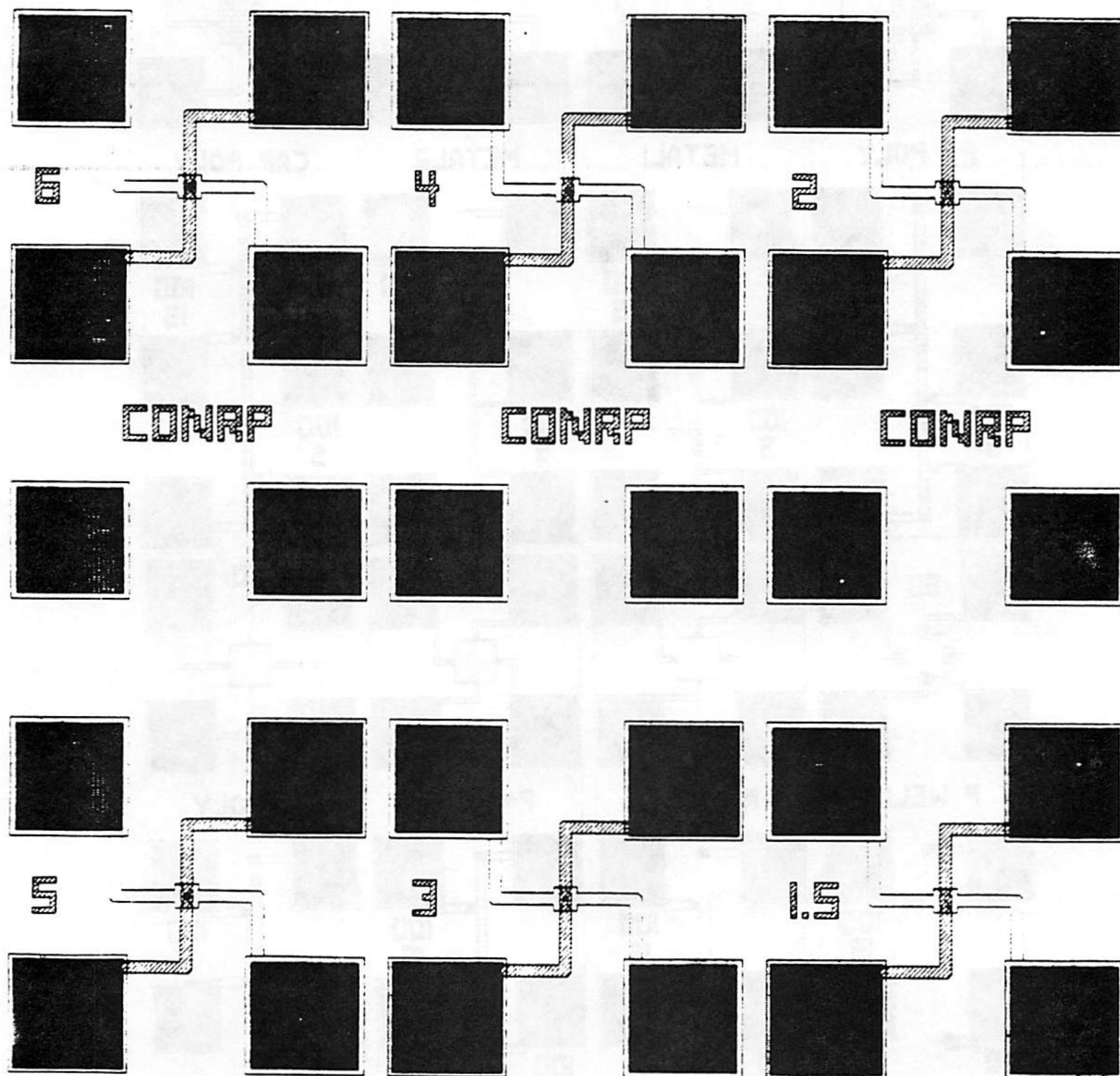

Figure 18. Individual Contact Example - Polysilicon Contact Resistor

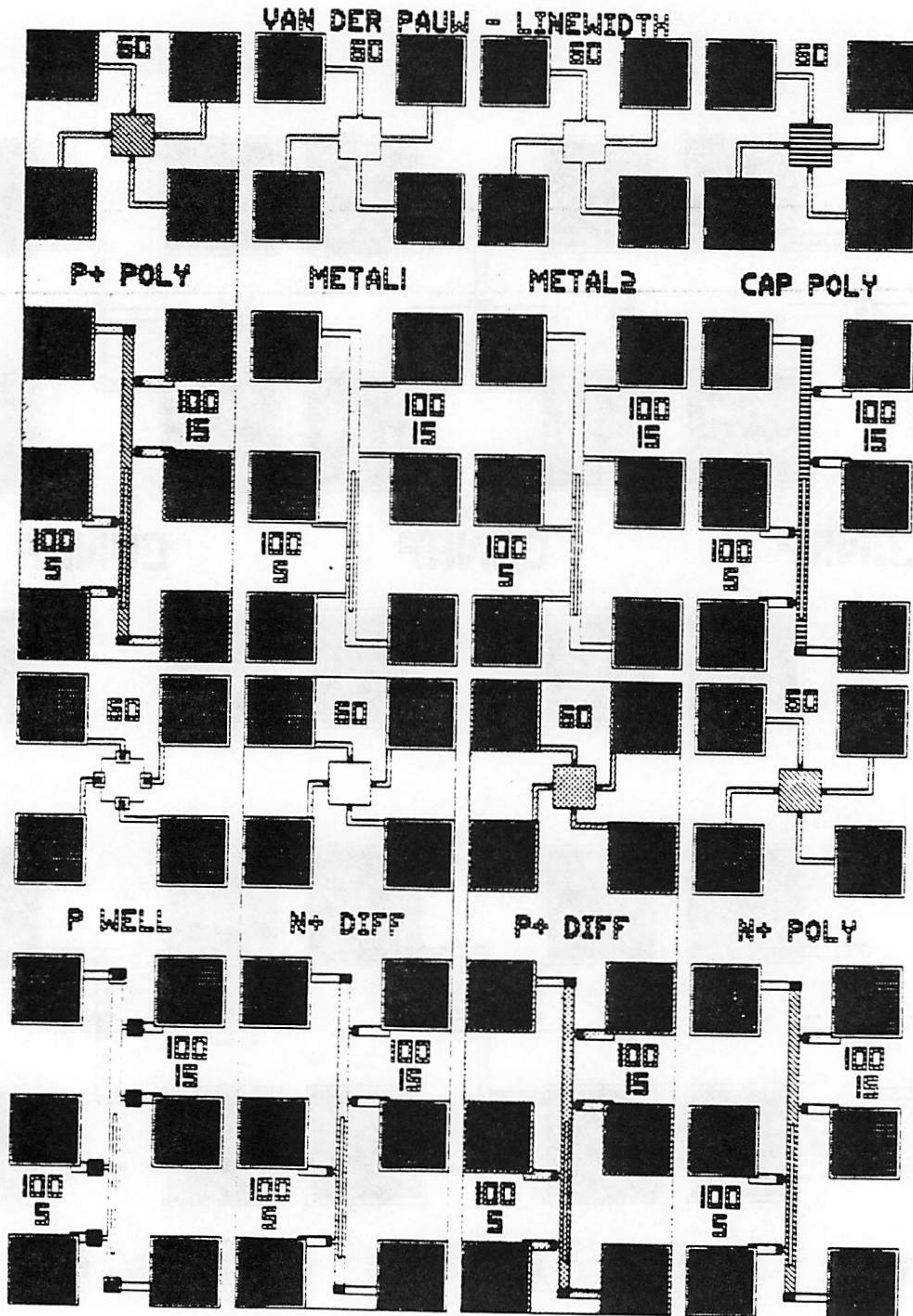

Figure 19. Sheet Resistivity and Van der Pauw Structures

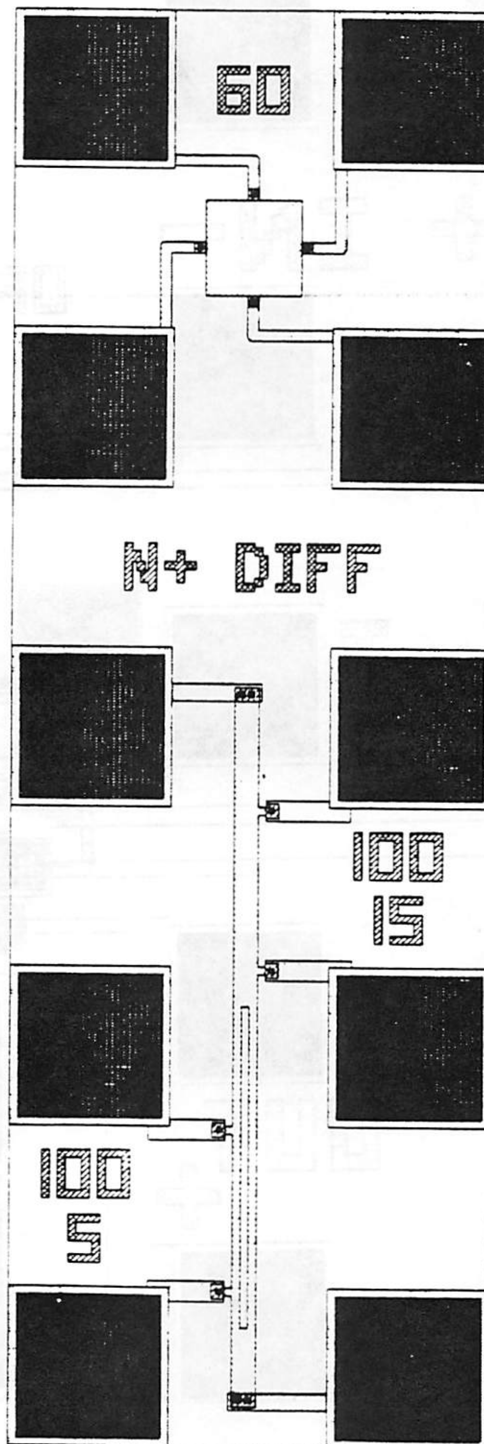

Figure 20. Sheet Resistivity and Van der Pauw Structure Example - n+ Diffusion

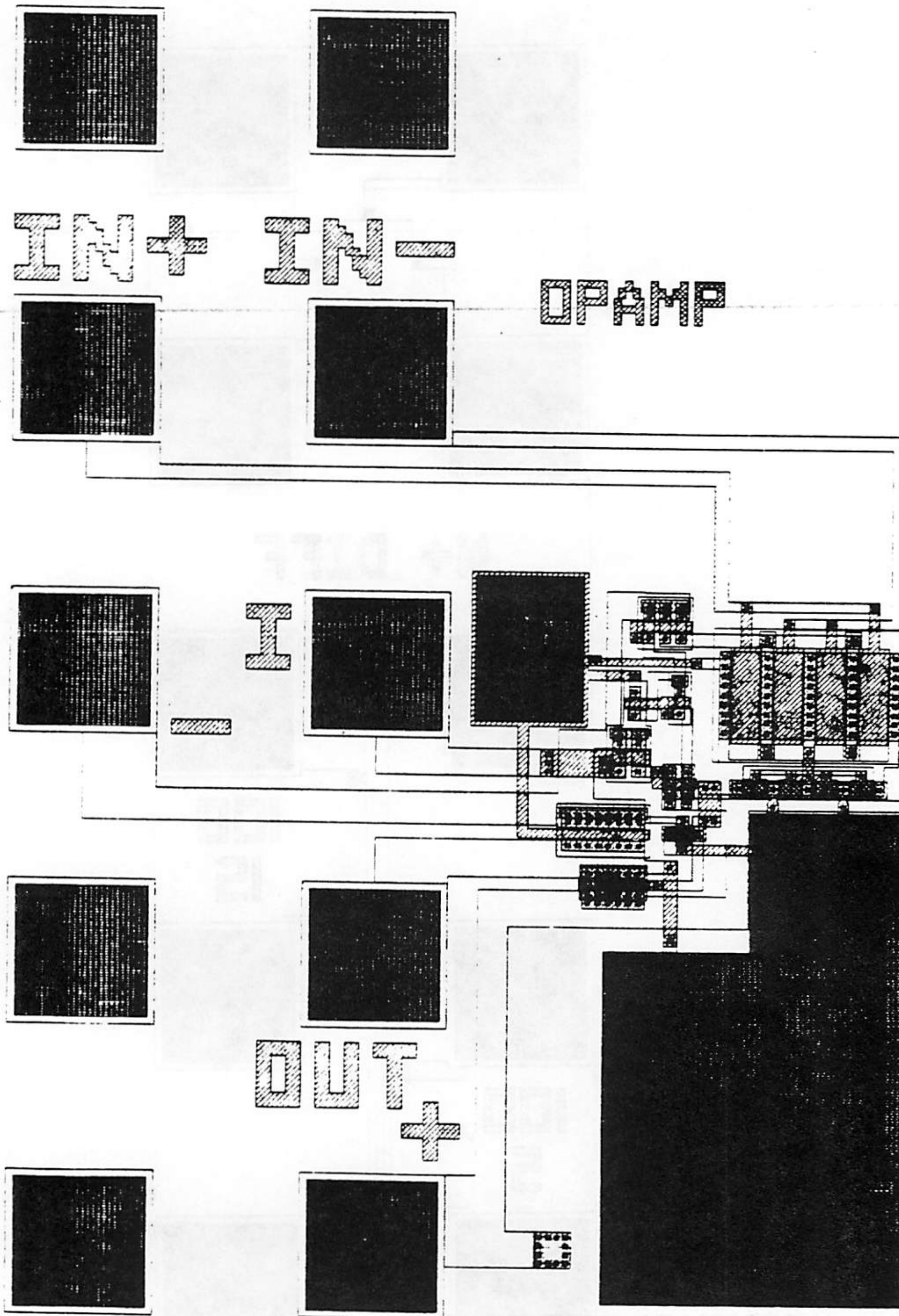

Figure 21. Operational Amplifier

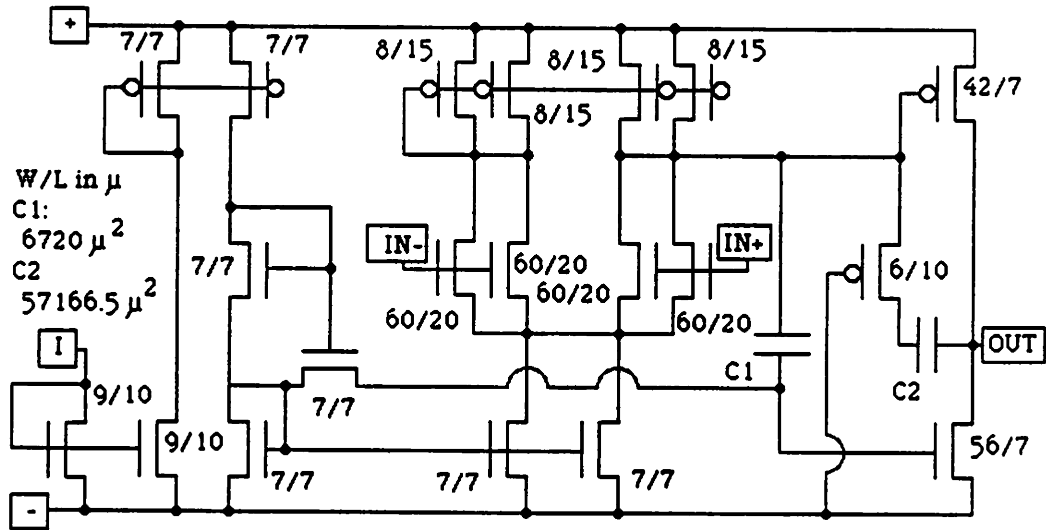

Figure 22. Operational Amplifier Schematic

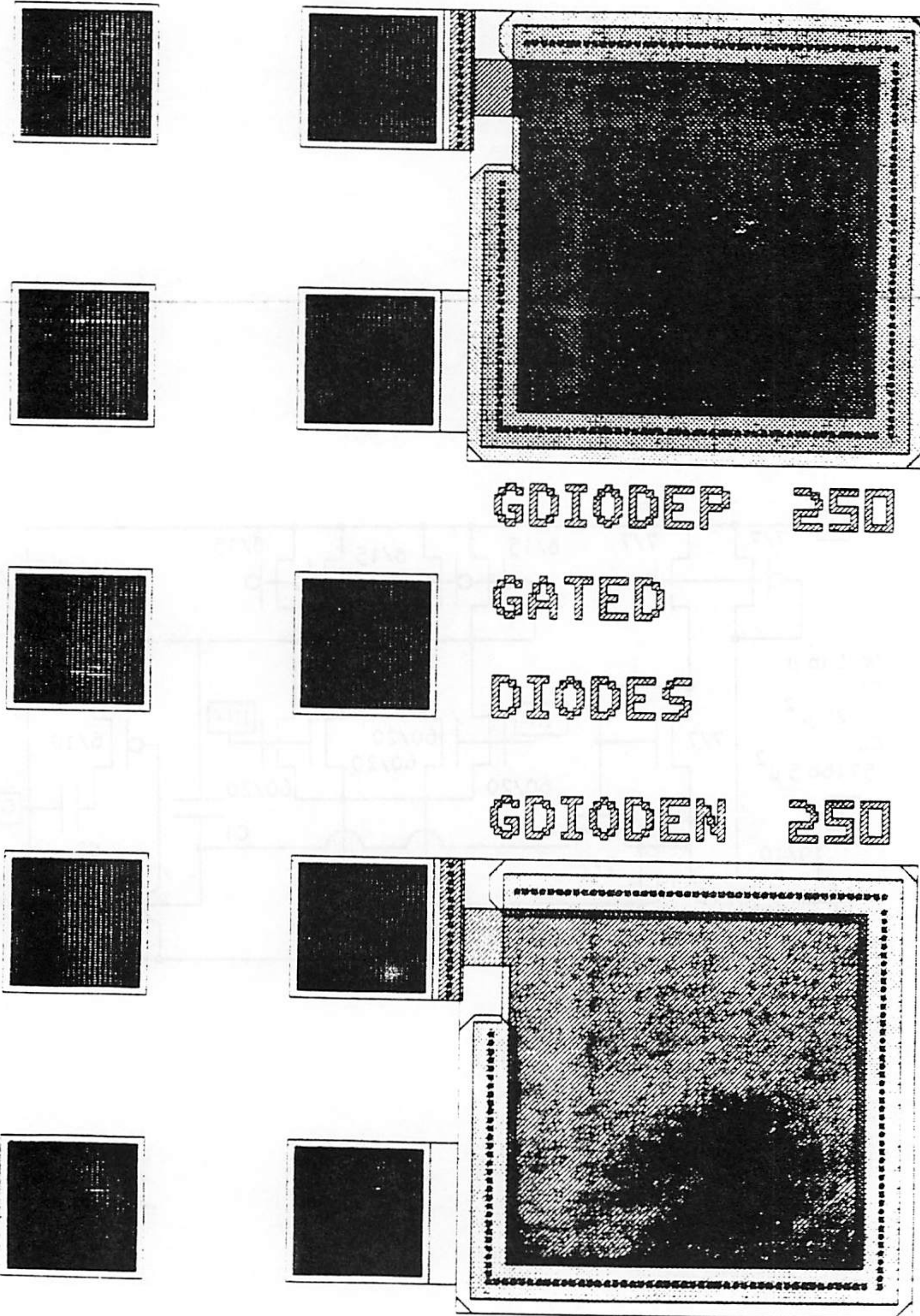

Figure 23. Gated Diodes

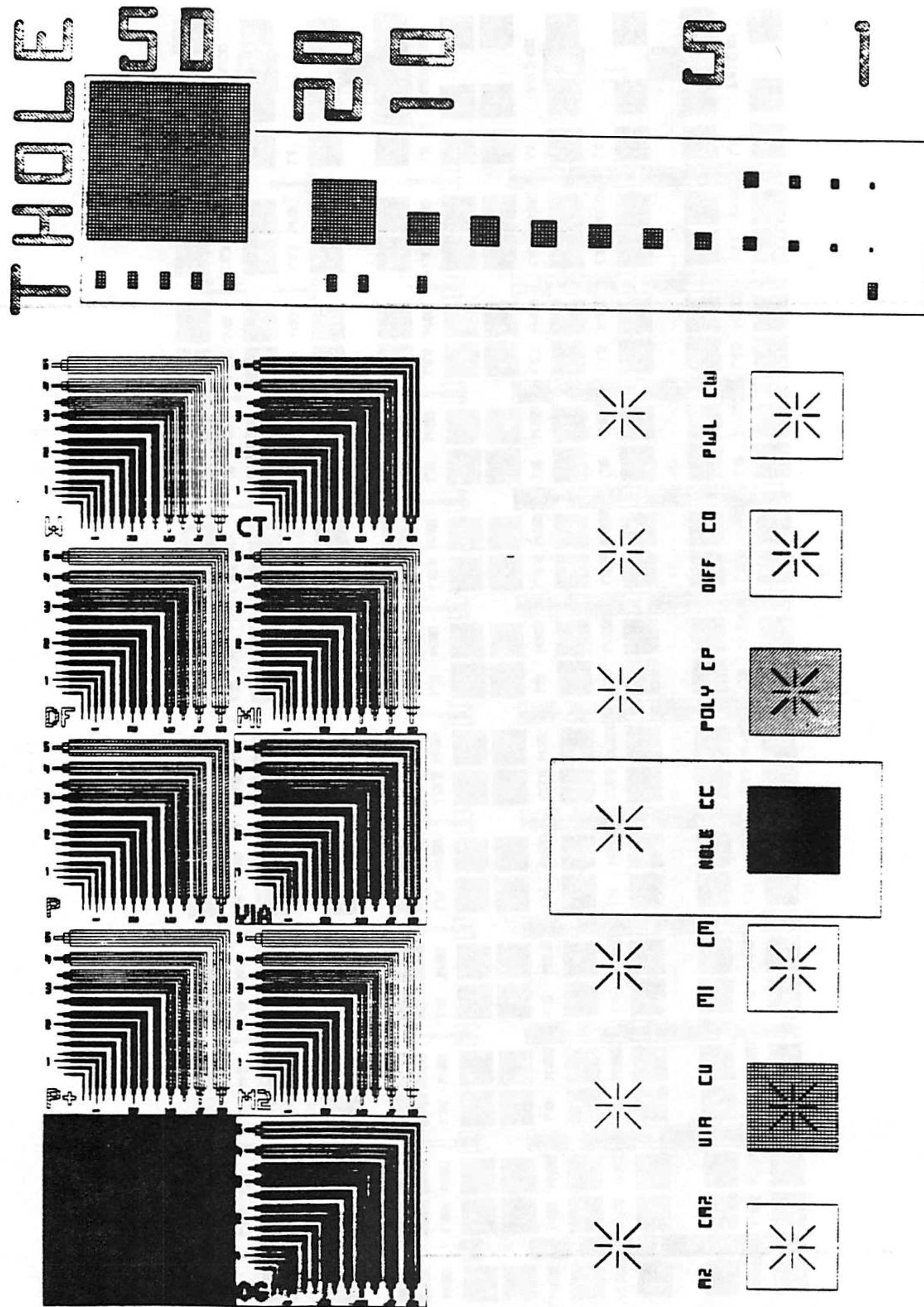

Figure 24. Alignment Pattern and Visual Verification Structures

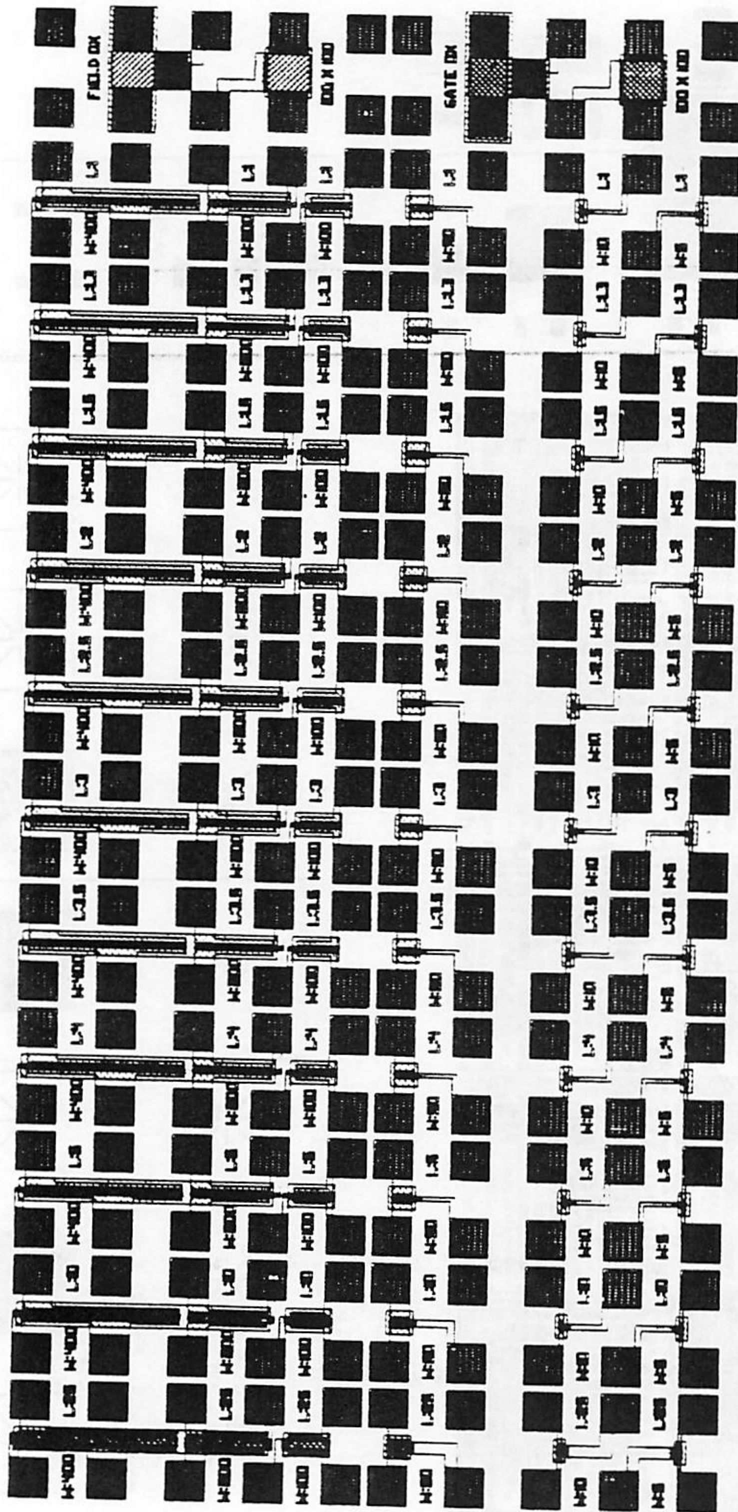

Figure 25. PMOS Transistor Matrix

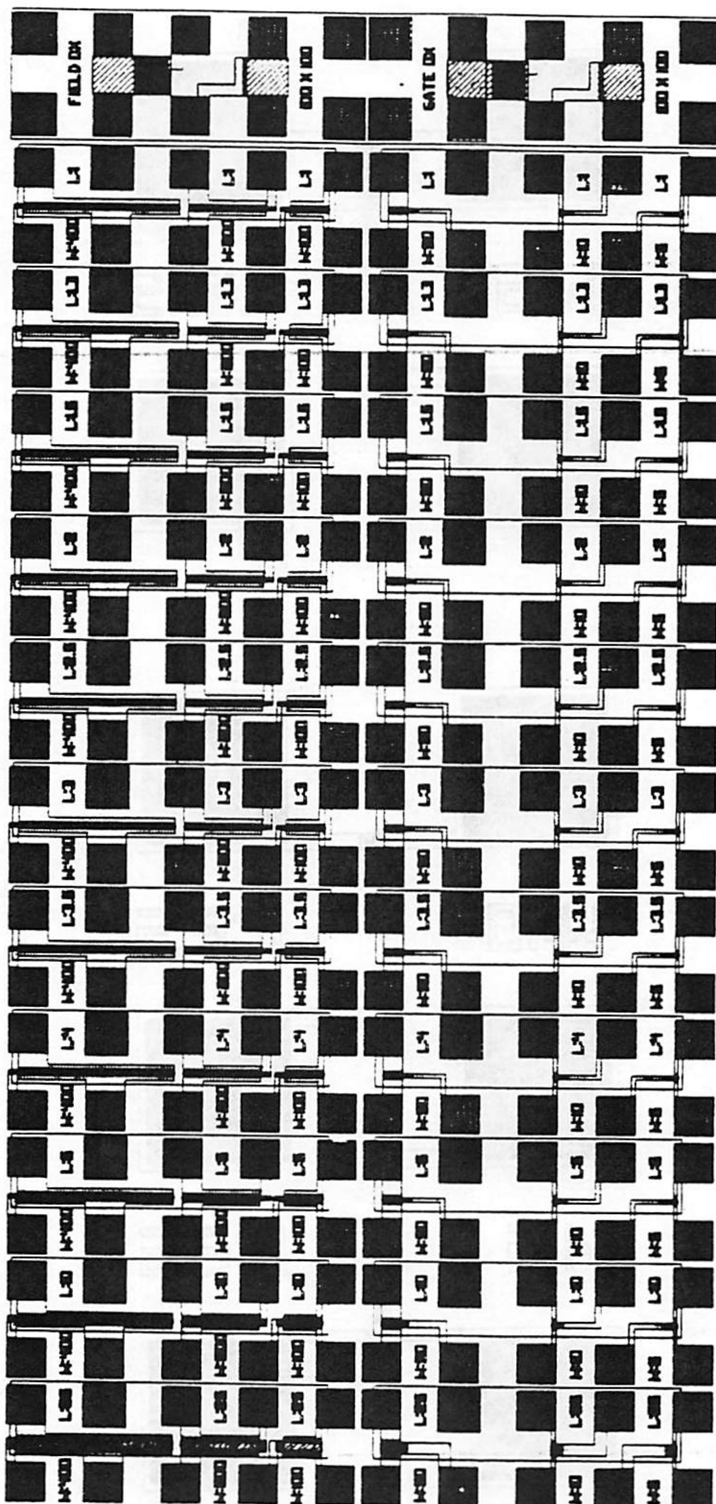

Figure 26. NMOS Transistor Matrix

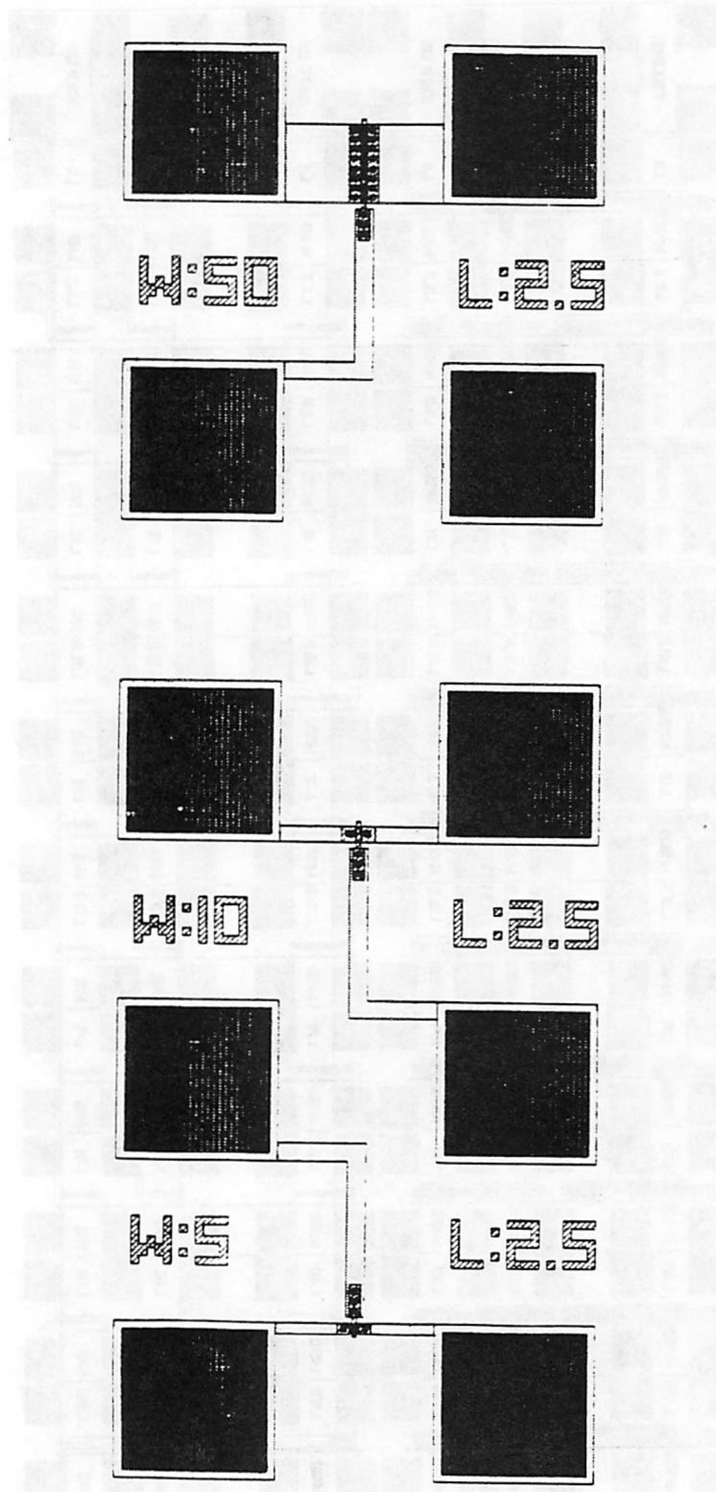

Figure 27. Transistor Structure

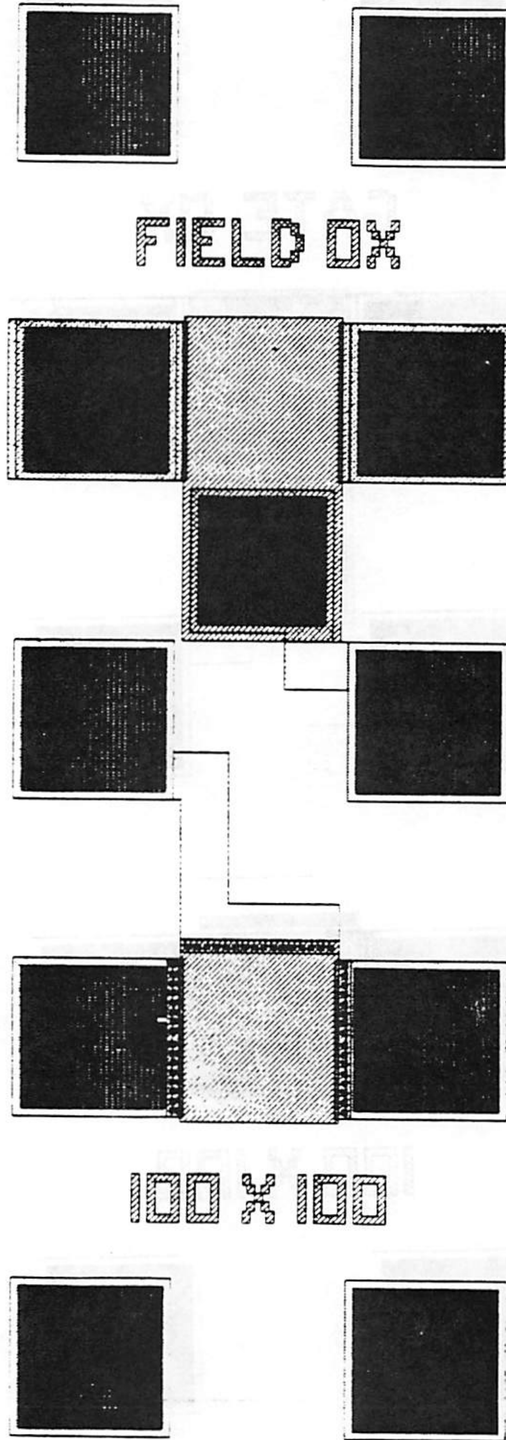

Figure 28. Large Field Oxide Devices

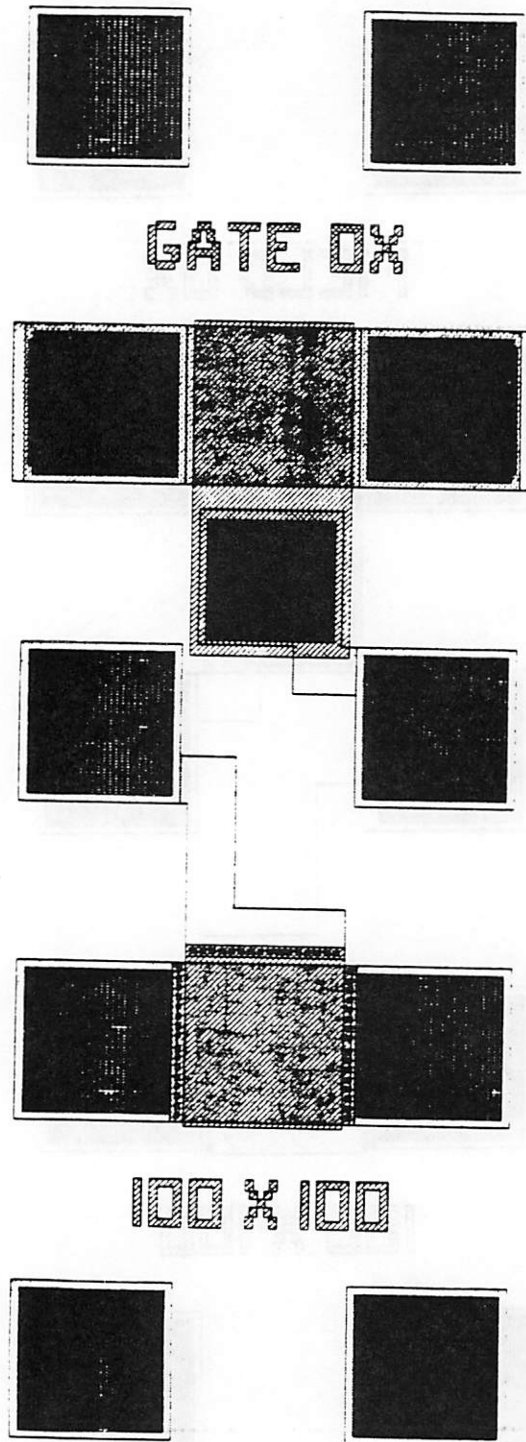

Figure 29. Large Gate Oxide Devices

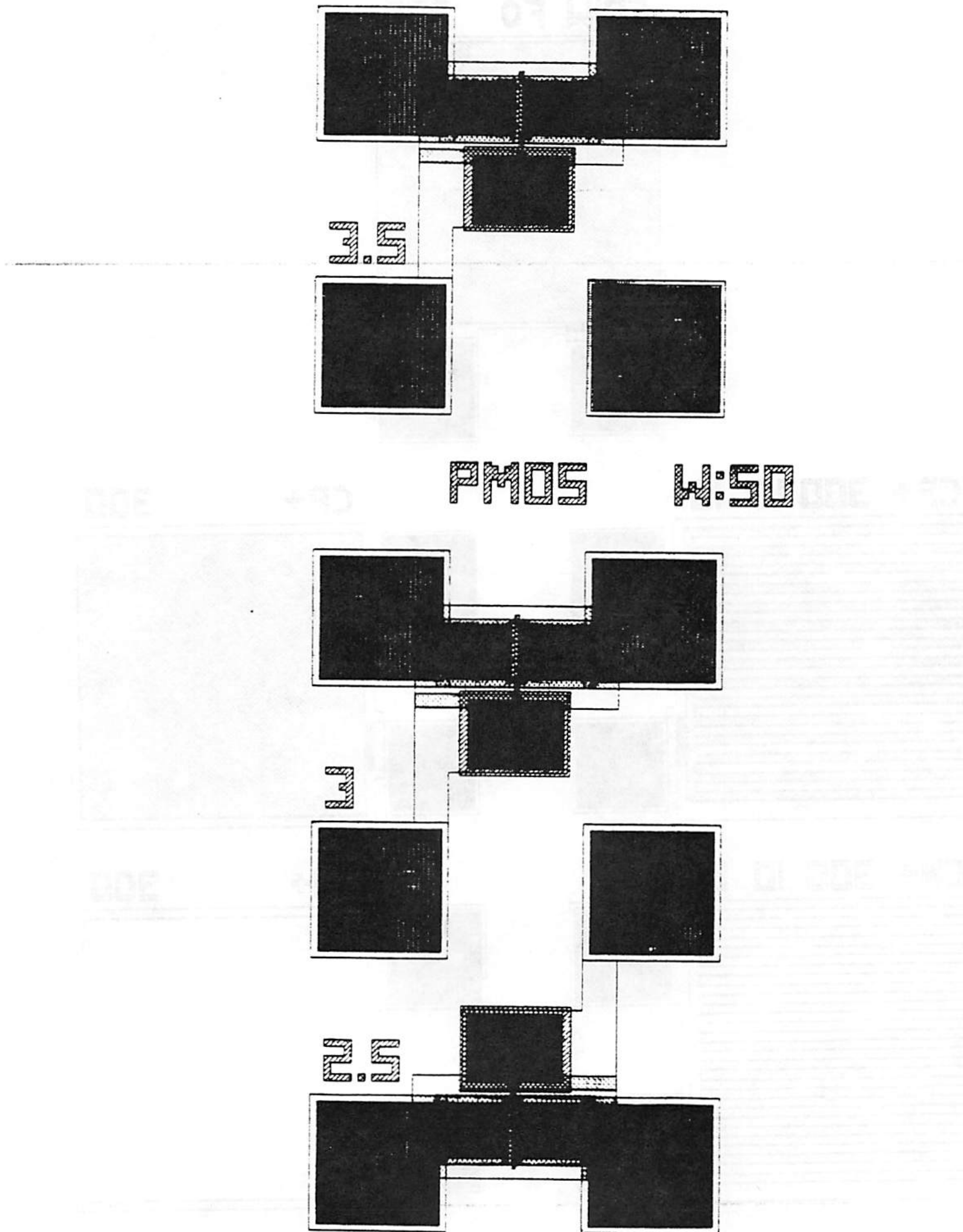

Figure 30. Devices with Large Contact Cuts

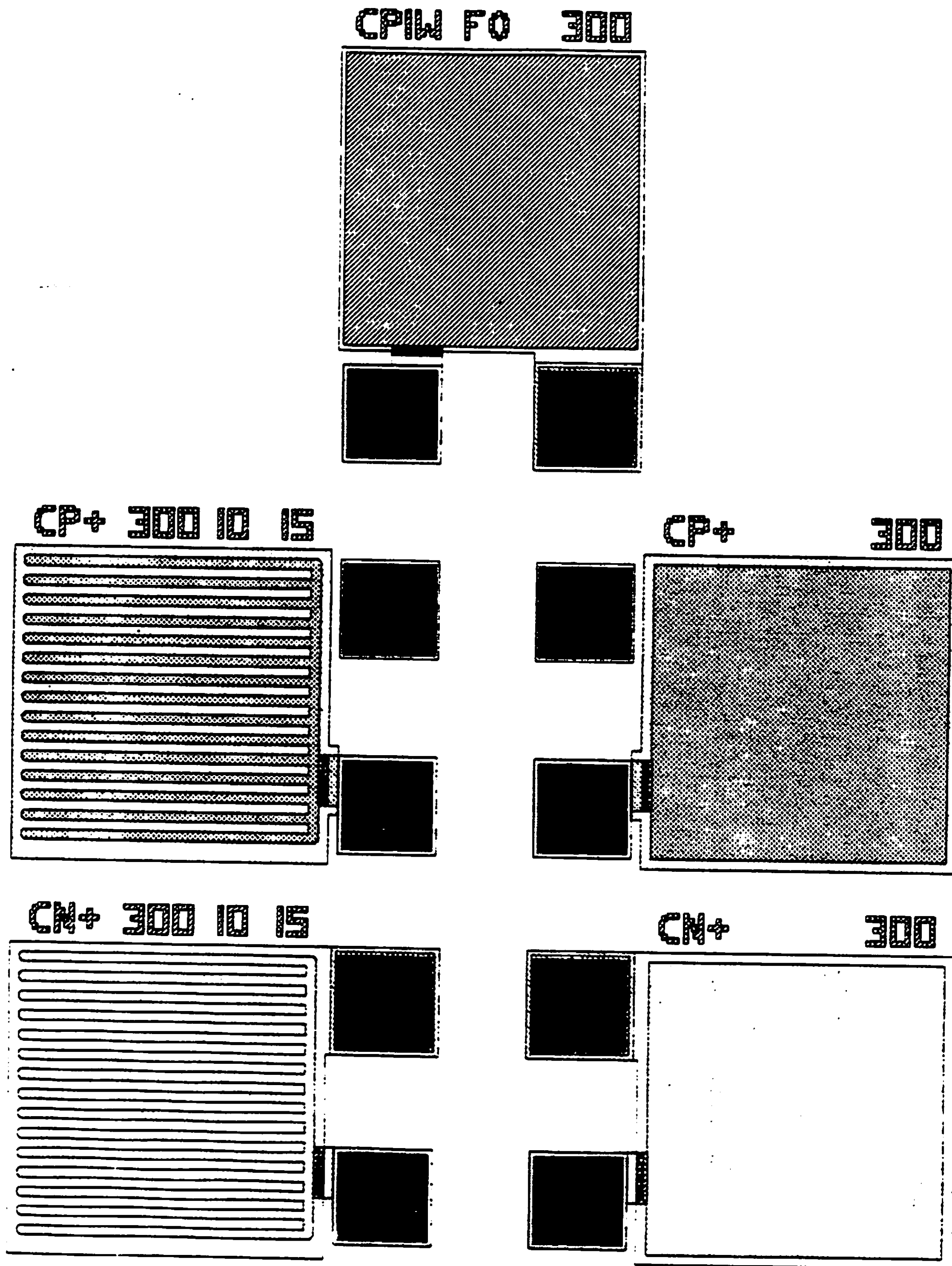

Figure 31. Capacitors - Set 1

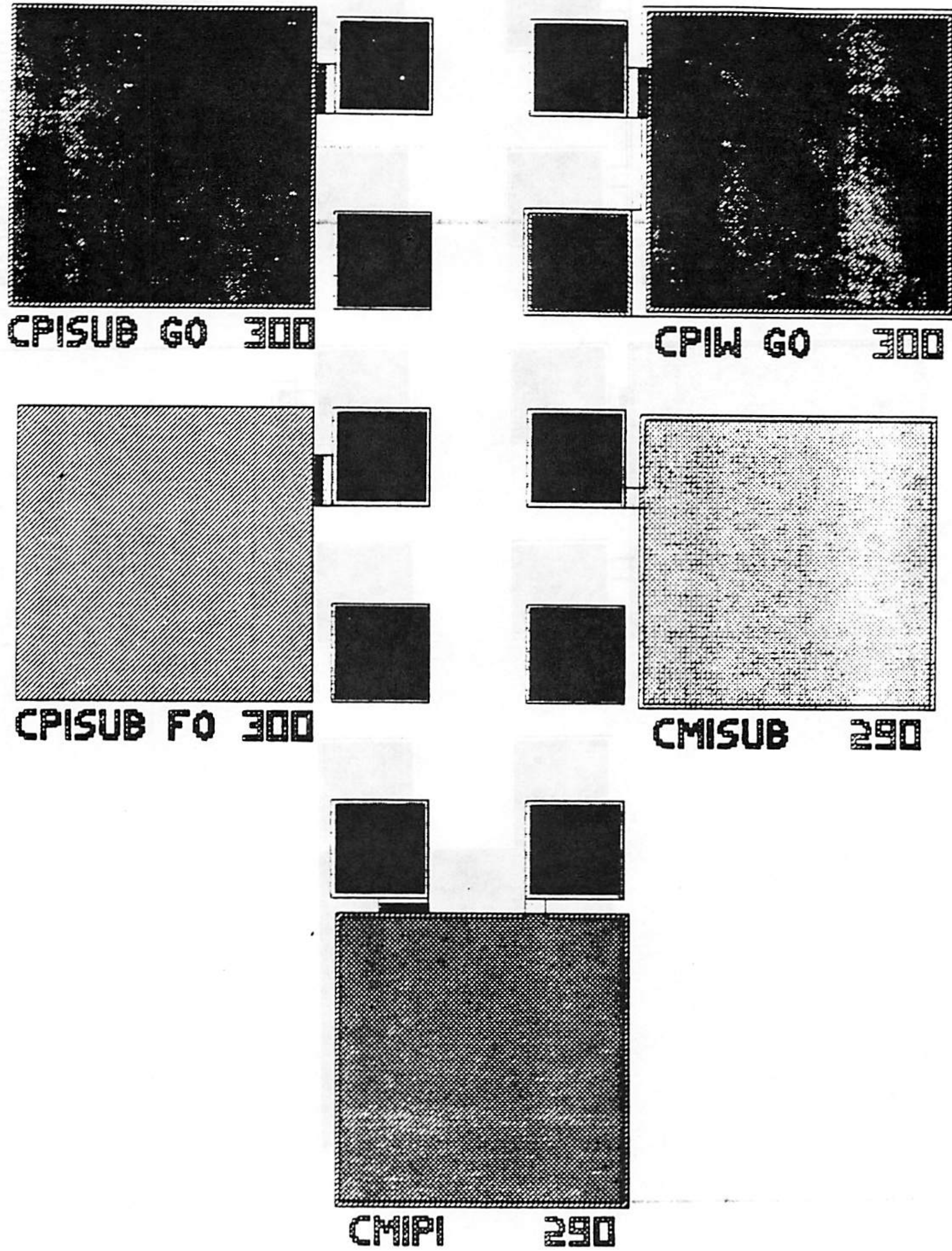

Figure 32. Capacitors - Set 2

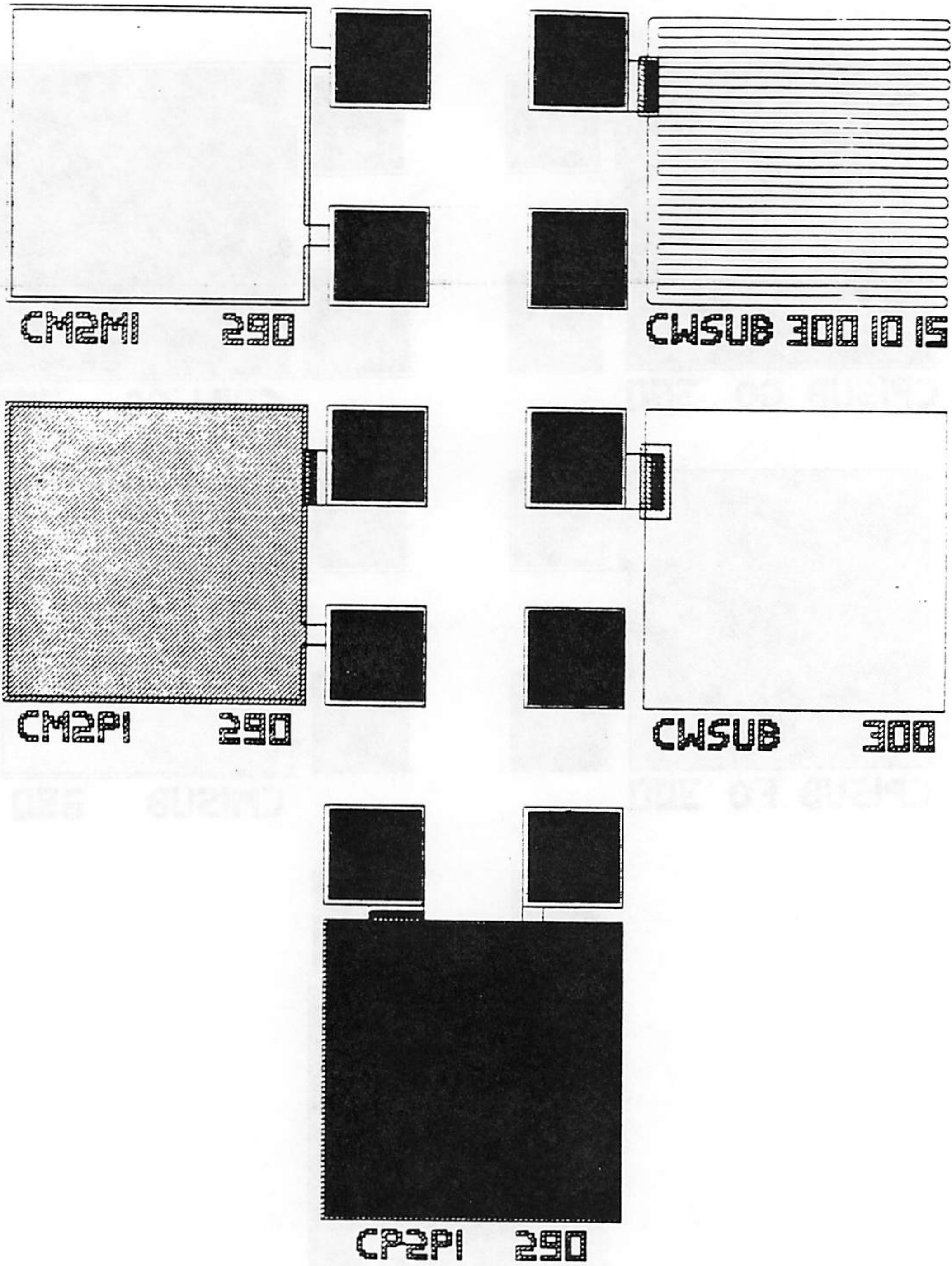

Figure 33. Capacitors - Set 3

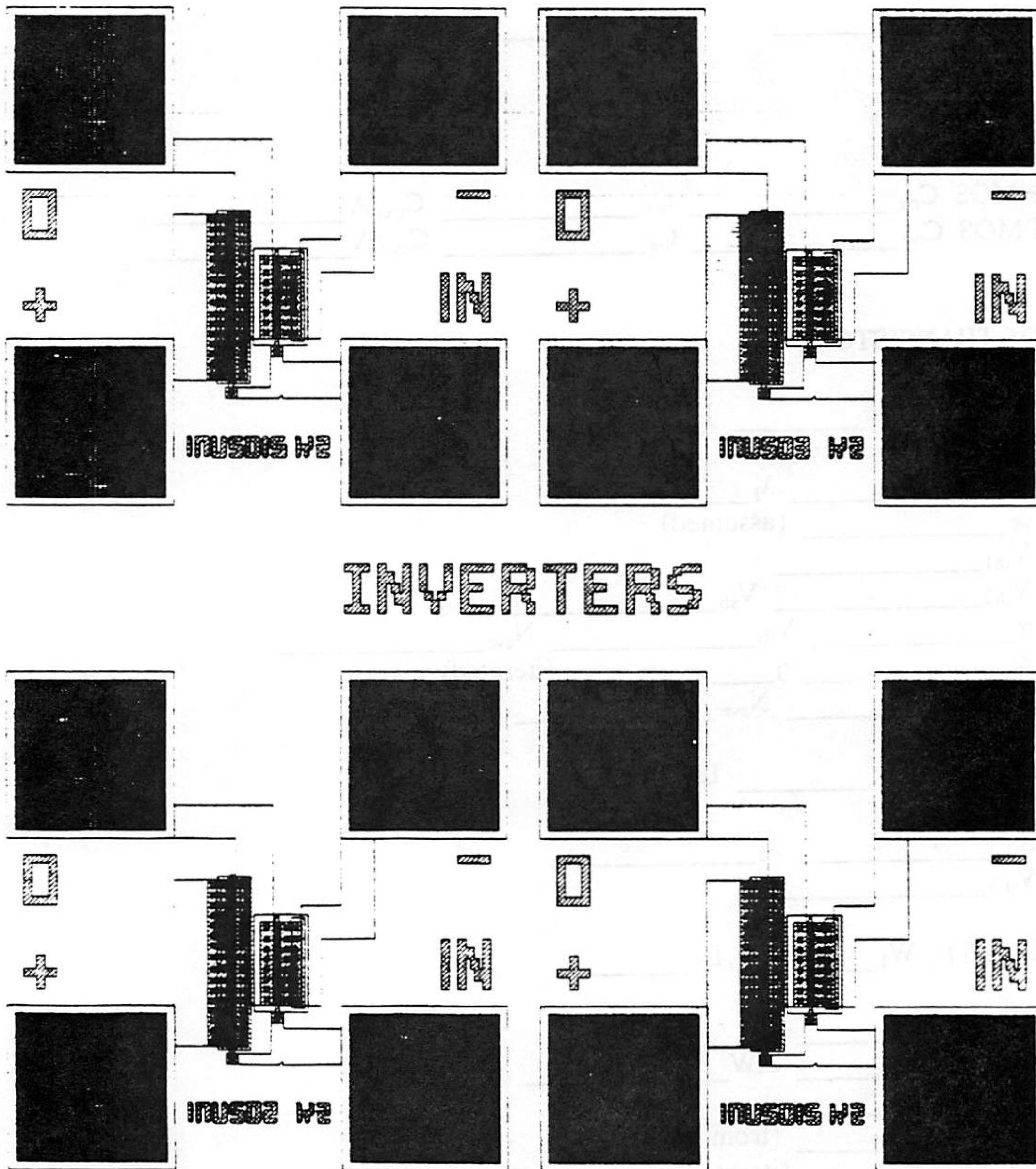

Figure 34. Inverters

IX. APPENDIX 2: DATA SHEETS

WAFER__________ **DIE**__________

CAPACITORS

NMOS C_{ox}__________ t_{ox}__________ C_{ox}/A__________
PMOS C_{ox}__________ t_{ox}__________ C_{ox}/A__________

NMOS TRANSISTORS

(L_1, W_1) W_1________ L_1________

K_1__________ λ_1__________
ϕ_f__________ (assumed)
V_{th1}__________
V_{th2}__________ V_{sb}__________
γ__________ V_{fb}__________ N_{ave}__________
ϕ_f__________ γ__________ (iterated)
V_{fb}__________ N_{ave}__________ (iterated)

(L_1, W_2) W_2________ L_1________

K_2__________ λ_2__________
V_{th3}__________

(L_2, W_1) W_1________ L_2________

K_3__________ λ_3__________
ΔL__________ ΔW__________
V_{th4}__________
W_c__________ (from V_{th3})
X_j__________ (iterated)
Q_{ss}__________ (from V_{fb} - get N_{poly} first)

PMOS TRANSISTORS

(L_1, W_1) W_1________ L_1________

K_1____________ λ_1____________
ϕ_f____________ (assumed)
V_{th1}____________
V_{th2}____________ V_{sb}____________
γ____________ V_{fb}____________ N_{ave}____________
ϕ_f____________ γ____________ (iterated)
V_{fb}____________ N_{ave}____________ (iterated)

(L_1, W_2) W_2________ L_1________

K_2____________ λ_2____________
V_{th3}____________
(L_2, W_1) W_1________ L_2________

K_3____________ λ_3____________
ΔL____________ ΔW____________
V_{th4}____________
W_c____________ (from V_{th3})
X_j____________ (iterated)
Q_{ss}____________ (from V_{fb} - get N_{poly} first)

VAN DER PAUW / LINEWIDTH

P+ poly	R_S____________	L_W____________
M_1	R_S____________	L_W____________
P well	R_S____________	L_W____________
N+	R_S____________	L_W____________
P+	R_S____________	L_W____________
N+ poly	R_S____________	L_W____________

MISALIGNMENT

cont-act

V_1____________ V_2____________ V_3____________
M_V____________
V_4____________ V_5____________
M_H____________

cont-ply

V_1____________ V_2____________ V_3____________
M_V____________
V_4____________ V_5____________
M_H____________

M_1-act

V_1____________ V_2____________ V_3____________
M_V____________
V_4____________ V_5____________
M_H____________

M_1-poly

V_1____________ V_2____________ V_3____________
M_V____________
V_4____________ V_5____________
M_H____________

poly-act

I____________ V_1____________ V_2____________
M_V____________
I____________ V_3____________ V_4____________
M_H____________

CONTACTS

P+

L_1____________ L_2____________
R_{C1}____________ R_{C2}____________ ΔL____________

N+

L_1____________ L_2____________
R_{C1}____________ R_{C2}____________ ΔL____________

Poly

L_1____________ L_2____________
R_{C1}____________ R_{C2}____________ ΔL____________

X. APPENDIX 3: EQUATIONS

CAPACITORS

$$t_{ox} = \frac{31.078 \times 10^3}{C_{ox}\,(pF)}$$

NMOS TRANSISTORS

K_1 from plot

λ_1 from plot

$$\phi_f = 0.025256 \ln\left(\frac{1.45 \times 10^{10}}{N_A}\right)$$

$$\gamma = \frac{V_{th1} - V_{fb} - 2\phi_f}{\sqrt{2\phi_f}}$$

$$V_{fb} = \frac{V_{th2} - 2\phi_f - \left(\frac{V_{th1} - 2\phi_f}{\sqrt{2\phi_f}}\right)\left(\sqrt{2\phi_f - V_{BS}}\right)}{\left(1 - \frac{1}{\sqrt{2\phi_f}}\right)\left(\sqrt{2\phi_f - V_{BS}}\right)}$$

$$N_{ave} = \frac{\gamma^2 C_{ox}^2}{2\varepsilon_{Si} q}$$

$$\Delta L = \frac{K_3 L_2 - K_1 L_1}{K_3 - K_1}$$

$$\Delta W = \frac{K_2 W_1 - K_1 W_2}{K_2 - K_1}$$

$$W_{eff} = W_2 - \Delta W$$

$$L_{eff} = L_2 - \Delta L$$

$$W_C = W_{eff}\left(\frac{V_{th3} - V_{fb} - 2\phi_f}{\gamma\sqrt{2\phi_f}} - 1\right)$$

$$V_{th4} = V_{fb} + 2\phi_f + \gamma\left(1 - \frac{X_j}{L_{eff}}\left(\sqrt{1 + \frac{2W_C}{X_j}} - 1\right)\right)\sqrt{2\phi_f}$$

$$Q_{SS} = C_{ox}\left(0.025256\right)\left(\ln\left(\frac{N_{poly}}{n_i}\right) - \ln\left(\frac{N_{ave}}{n_i}\right)\right) - C_{ox}V_{fb}$$

PMOS TRANSISTORS

K_1 from plot

λ_1 from plot

$$\phi_f = 0.025256 \ln\left(\frac{N_D}{1.45 \times 10^{10}}\right)$$

$$\gamma = \frac{V_{th1} - V_{fb} - 2\phi_f}{\sqrt{2\phi_f}}$$

$$V_{fb} = \frac{V_{th2} - 2\phi_f - \left(\dfrac{V_{th1} - 2\phi_f}{\sqrt{2\phi_f}}\right)\left(\sqrt{2\phi_f - V_{BS}}\right)}{\left(1 - \dfrac{1}{\sqrt{2\phi_f}}\right)\left(\sqrt{2\phi_f - V_{BS}}\right)}$$

$$N_{ave} = \frac{\gamma^2 C_{ox}^2}{2\varepsilon_{Si} q}$$

$$\Delta L = \frac{K_3 L_2 - K_1 L_1}{K_3 - K_1}$$

$$\Delta W = \frac{K_2 W_1 - K_1 W_2}{K_2 - K_1}$$

$$W_{eff} = W_2 - \Delta W$$

$$L_{eff} = L_2 - \Delta L$$

$$W_C = W_{eff}\left(\frac{V_{th3} - V_{fb} - 2\phi_f}{\gamma\sqrt{2\phi_f}} - 1\right)$$

$$V_{th4} = V_{fb} + 2\phi_f + \gamma\left(1 - \frac{X_j}{L_{eff}}\left(\sqrt{1 + \frac{2W_C}{X_j}} - 1\right)\right)\sqrt{2\phi_f}$$

$$Q_{SS} = C_{ox}\left(0.025256\right)\left[\ln\left(\frac{N_{poly}}{n_i}\right) - \ln\left(\frac{N_{ave}}{n_i}\right)\right] - C_{ox}V_{fb}$$

VAN DER PAUW / SHEET RESISTIVITY

$$R_S = \frac{\pi}{\ln 2}\frac{\Delta V}{I}$$

$$L_W = R_S L \frac{I}{\Delta V}$$

MISALIGNMENT

$$M_V = \frac{L_{ref}}{V_1}\left(V_2 - V_3\right)$$

$$M_H = \frac{L_{ref}}{V_1}\left(V_4 - V_5\right)$$

$$M_V = IR_S 400\left(\frac{1}{V_1} - \frac{1}{V_2}\right) \quad \text{(poly-active misalignment)}$$

$$M_H = IR_S 400\left(\frac{1}{V_3} - \frac{1}{V_4}\right) \quad \text{(poly-active misalignment)}$$

CONTACTS

$$\Delta L = \frac{L_{O2}\sqrt{R_{C2}} - L_{O1}\sqrt{R_{C1}}}{\sqrt{R_{C2}} - \sqrt{R_{C1}}}$$

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