BENCHMARK CIRCUITS: RESULTS FOR SPICE3

by

Thomas L. Quarles

Memorandum No. UCB/ERL M89/47

24 April 1989

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ELECTRONICS RESEARCH LABORATORY

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Preface

This memo is one of six containing the text of the Ph.D. dissertation *Analysis of Performance and Convergence Issues for Circuit Simulation.* The dissertation itself is available as UCB/ERL Memorandum M89/42. The other appendices are available as:

Memo number	Title
UCB/ERL M89/43	The Front End to Simulator Interface
UCB/ERL M89/44	The SPICE3 Implementation Guide
UCB/ERL M89/45	Adding Devices to SPICE3
UCB/ERL M89/46	SPICE3 Version 3C1 Users Guide

This memo was originally Appendix G of the dissertation and provides details of the results of running SPICE3 on the set of benchmark circuits collected to evaluate the performance of SPICE3 in comparison with other simulators. These results correcpond to SPICE3, version 3C1 and SPICE2, version 2G.6 as indicated in each section.

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CHAPTER 1

Benchmark Circuits

An extensive set of benchmark circuits has been collected to evaluate SPICE3. These circuits come from a variety of sources, ranging from simple test circuits designed to exercise a single characteristic to large industrial circuits used for performance comparisons. Included are numerous circuits that have been sent to Berkeley over the years as demonstrations of particular SPICE problems. Listings of the circuits are not included here, but may be obtained in machine readable form from The University of California at Berkeley, Department of Electrical Engineering and Computer Science, Industrial Liaison Program, software office.

1.1. Naming Conventions

The names of the circuits are formed from the descriptions and thus provide some important information themselves without having to consult the circuit itself or this chapter for details. Each name is make up of four or five components in the form:

{Device type} {Device count} {Circuit type} [Distinguishing number] {Analysis type}

Where the components are as described below.

Device type

Device type is a single letter,

N for an NMOS circuit
C for a CMOS circuit
Q for a bipolar circuit
H for a mixed MOS/bipolar circuit
T for a transmission line circuit
O for all other circuits

Device count

Device count is the number of devices of the type given by the device type that are contained

in the circuit.

Circuit type

Circuit type is a single letter that distinguishes between digital and analog circuits.

A for an analog circuit
D for a digital circuit
M for a mixed analog and digital circuit

Circuits which are actually digital circuits, but which were designed to test the analog characteristics of the circuit are classed as analog.

Distinguishing number

The distinguishing number is an optional small integer used to distinguish between circuits whose names would otherwise be identical.

Analysis type

The analysis type is one *or more* of:

O for an operating point analysis
T for a transient analysis
A for an ac analysis
D for a dc transfer curve analysis
P for a pole-zero analysis

1.2. Circuit Summary

The following table contains a brief description of the circuits used. Note that circuits with an asterisk (*) to the right of their description are circuits obtained from industry sites which contain proprietary data and will not be included in the machine readable set of benchmarks released by Berkeley.

Name	# of Nodes	# of Equations	# of BJTs	# of Diodes	# of JFETs	# of MOSFETs	# of MESFETs	# of Other
Q180Do	262	451	180	108	0	0	0	158
Q180D2o	262	451	180	108	0	0	0	158
Q2At	7	13	2	0	0	0	0	8
O9Aa	6	7	0	0	0	0	0	7
O1024Ao	2	2	0	0	0	0	0	1024
N48Dt	31	36	0	0	0	48	0	5

Name	# of Nodes	# of Equations	# of BJTs	# of Diodes	# of JFETs	# of MOSFETs	# of MESFETs	# of Other	
N5At	7	10	0	0	0	5	0	6	
N5A2t	7	10	0	0	0	5	0	6	
O10At	7	10	0	0	0	0	0	10	
Q6Ao	11	13	6	0	0	0	0	7	
Q6A2o	11	13	6	0	0	0	0	7	
Q4Ao	11	15	4	0	0	0	0	13	
N1Aot	5	9	0	0	0	1	0	4	
N1A2ot	5	9	0	0	0	1	0	4	
N1A3ot	5	9	0	0	0	1	0	4	
O8At	5	8	0	2	0	0	0	6	
Q1Ado	7	10	1	0	0	0	0	6	
Q1A2t	6	9	1	0	0	0	0	6	
Q5Atd	10	12	5	0	0	0	0	17	
C25Ao	20	24	0	0	0	25	0	9	
C27Ao	28	34	0	0	0	27	0	19	
C7Ao	11	14	0	0	0	7	0	7	
C4Dto	5	7	0	0	0	4	0	2	
C22Dt	16	68	0	0	0	22	0	17	
C22D2o	16	68	0	0	0	22	0	17	
T2At	6	15	0	0	0	0	0	6	
Q7Ao	14	15	7	0	0	0	0	12	
N116Dt	66	75	0	116	0	116	0	82	*
N2Dod	4	6	0	0	0	2	0	2	
Q4At	10	17	4	0	0	0	0	8	
Q8Atd	18	39	8	2	0	0	0	15	
Q4A1t	9	20	4	0	0	0	0	10	
C4D1to	6	9	0	0	0	4	0	4	
Q4a2t	8	11	4	0	0	0	0	6	
Q10At	60	148	10	20	0	0	0	129	
O3At	3	5	0	0	0	0	0	3	
N10Dto	9	12	0	0	0	10	0	3	
N10D2to	9	12	0	0	0	10	0	3	
N10Ato	9	12	0	0	0	10	0	3	
N1A4d	4	6	0	0	0	1	0	4	
Q7Aat	16	19	7	0	10	0	0	9	
Q3At	10	24	3	0	0	0	0	17	
O15ata	5	9	0	0	0	0	0	15	
Q11atd	23	51	11	4	0	0	0	20	
O5At	4	6	0	0	0	0	1	5	
N27Aaod	21	25	0	0	0	27	0	6	
N27A2t	21	25	0	0	0	27	0	6	
N27A3o	21	25	0	0	0	27	0	6	
N27A4o	21	25	0	0	0	27	0	6	
N27A5o	21	25	0	0	0	27	0	6	
N27A6aod	21	25	0	0	0	27	0	6	
N12At	10	14	0	0	0	12	0	4	
N8Ao	14	23	0	0	0	8	0	18	
N2Ao	7	15	0	0	0	2	0	16	
O6At	4	7	0	0	0	0	0	6	
N1A5d	5	8	0	0	0	1	0	6	
N6At	10	15	0	0	0	6	0	10	

Name	# of Nodes	# of Equations	# of BJTs	# of Diodes	# of JFETs	# of MOSFETs	# of MESFETs	# of Other	
Q11Atad	19	33	11	0	0	0	0	15	
Q5Ao	7	8	5	0	0	0	0	6	
Q2Dtd	7	13	2	0	0	0	0	6	
O66At	44	85	0	3	0	0	0	63	
N2Dtdo	5	8	0	0	0	2	0	3	
Q8Dtd	27	57	8	11	0	0	0	16	
Q4A3t	9	19	4	0	0	0	0	11	
Q50At	73	148	50	0	0	0	0	115	
O5A1t	4	5	0	0	0	0	0	5	
C38Da	30	36	0	0	0	38	0	8	
C38D2a	30	36	0	0	0	38	0	8	
O6A1t	3	5	0	0	0	0	0	6	
O3Ap	3	3	0	0	0	0	0	3	
O7Ap	5	6	0	0	0	0	0	7	
T1Atad	3	7	0	0	0	0	0	3	
T2A1t	4	13	0	0	0	0	0	5	
T1A1t	3	7	0	0	0	0	0	2	
t1A2t	2	6	0	0	0	0	0	2	
T3At	5	18	0	0	0	0	0	6	
T3A2t	5	18	0	0	0	0	0	6	
Q5Dtd	14	29	5	3	0	0	0	8	
Q5D1td	14	29	5	3	0	0	0	8	
Q7Dtd	16	34	7	2	0	0	0	9	
Q6Dtd	15	31	6	2	0	0	0	10	
Q5D2td	14	29	5	3	0	0	0	8	
Q4A5ta	15	55	4	0	0	0	0	27	
Q15atad	26	44	15	0	0	0	0	24	
Q22Atad	36	62	22	0	0	0	0	31	
Q22A2tad	36	62	22	0	0	0	0	31	
Q11Ata	24	38	11	0	0	0	0	21	
Q11Ao	23	25	11	0	0	0	0	20	
Q22A3tad	27	52	22	0	0	0	0	18	
Q22A4tad	28	98	22	0	0	0	0	19	
Q22A5tad	27	52	22	0	0	0	0	18	
O3A1t	3	5	0	0	0	0	0	3	
N9At	15	23	0	0	0	9	0	10	
O38Aa	20	29	0	0	0	0	0	38	
C18At	17	55	0	0	0	18	0	10	
C18A1t	17	55	0	0	0	18	0	10	
Q18A2t	17	141	0	0	0	18	0	10	
N4Ada	8	12	0	0	0	4	0	5	
C14Dt	11	14	0	0	0	14	0	10	
N804Dt	396	403	0	333	0	804	0	60	*
T1At	3	8	0	0	0	0	0	2	
C19Mt	18	66	0	0	0	19	0	14	
C68Dt	39	179	0	0	0	68	0	9	
C9Ao	22	38	0	0	0	9	0	18	
C82Dt	20	23	0	0	0	32	0	19	
C2At	4	10	0	0	0	2	0	2	
C37Dt	37	59	0	0	0	37	0	24	
N27At	21	25	0	0	0	27	0	6	

Name	# of Nodes	# of Equations	# of BJTs	# of Diodes	# of JFETs	# of MOSFETs	# of MESFETs	# of Other	
N698Dt	385	391	0	0	0	698	0	390	
Q6At	12	18	6	0	0	0	0	10	
C7Atd	9	27	0	0	0	7	0	6	
C52Aa	56	76	0	0	0	52	0	38	
Q340t	636	2024	340	1	0	0	0	1306	
C54Dt	197	204	0	54	0	54	0	317	
N1190Mt	664	688	0	0	0	1190	0	201	*
C31Dt	25	90	0	0	0	31	0	3	
Q2A1t	7	17	2	0	0	0	0	11	
C119At	74	77	0	105	0	119	0	163	*
C6Dt	7	10	0	0	0	6	0	6	
Q2A2t	7	9	2	0	0	0	0	8	
Q6A1t	8	9	6	0	0	0	0	10	
Q4A4ta	15	55	4	0	0	0	0	27	
O4Ao	4	7	0	0	0	0	0	4	
H44Aa	54	167	18	0	0	26	0	36	*
Q10Ao	18	53	10	0	0	0	0	17	
C77Mt	65	81	0	0	0	77	0	51	*
Q4Af	9	13	4	0	0	0	0	7	
N2Aa	8	16	0	0	0	2	0	11	
N1Ad	4	9	0	0	0	1	0	3	
O5A2t	4	5	0	0	0	0	0	5	
O2At	2	2	0	0	0	0	0	2	
O2A2t	2	2	0	0	0	0	0	2	
C205At	123	127	0	0	0	205	0	7	*
T2A2t	7	18	0	0	0	0	0	11	
C26At	37	79	0	80	0	26	0	77	
N1At	3	5	0	0	0	1	0	2	
C37At	32	38	0	0	0	37	0	36	
N3At	7	17	0	0	0	3	0	4	
C6D1t	8	10	0	0	0	6	0	7	
Q86Aa	96	357	86	0	0	0	0	46	
C640Dt	334	342	0	0	0	640	0	490	
C1060Mt	420	429	0	0	0	1060	0	156	
Q14Ao	17	63	14	0	0	0	0	11	
C28Dt	19	23	0	0	0	28	0	19	
C23Dt	18	67	0	0	0	23	0	3	
O20At	11	18	0	0	0	0	0	18	
C277Mt	151	160	0	344	0	277	0	55	*
C277M2t	151	160	0	344	0	277	0	55	*
C42Dt	20	107	0	0	0	42	0	20	
C7Ad	11	31	0	0	0	7	0	7	
C14D1t	14	48	0	0	0	14	0	13	
Q84At	478	1014	84	144	0	0	0	801	*
Q50A1t	73	148	50	0	0	0	0	115	*
O20A1t	9	16	0	4	0	0	0	16	

1.3. Raw Results

The following sections present tables providing the results of running SPICE3, SPICE2, and an industrial simulator on the benchmark set with various combinations of compilers and bypass options. Each section consists of several tables simply due to page width limitations; They are best considered a single table. Entries marked with a "-" indicate that that number is unavailable because the corresponding run could not be completed. All times given are in seconds unless otherwise indicated and were measured on a VAX 8650 running Ultrix 3.0.

1.3.1. SPICE3 with bypass

Figure 1.1
SPICE3 with bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
1	Q180Do	10.45	53	197.17
2	Q180D2o	10.53	53	198.68
3	Q2At	3.02	800	3.77
4	O9Aa	0.07	3	23.33
5	O1024Ao	0.09	3	30.00
6	N48Dt	153.33	2586	59.29
7	N5At	1.71	205	8.34
8	N5A2t	1.68	195	8.62
9	O10At	1.03	456	2.26
10	Q6Ao	0.07	13	5.38
11	Q6A2o	-	-	-
12	Q4Ao	0.07	7	10.00
13	N1Aot	0.37	124	2.98
14	N1A2ot	0.32	124	2.58
15	N1A3ot	0.32	124	2.58
16	O8At	0.50	166	3.01
17	Q1Ado	0.14	66	2.12
18	Q1A2t	0.55	193	2.85
19	Q5Atd	2.36	424	5.57
20	C25Ao	2.60	155	16.77
21	C27Ao	2.80	141	19.86
22	C7Ao	0.89	138	6.45
23	C4Dto	3.05	498	6.12
24	C22Dt	9.70	226	42.92
25	C22D2o	0.54	14	38.57
26	T2At	0.44	125	3.52
27	Q7Ao	0.09	13	6.92
28	N116Dt	146.56	1328	110.36
29	N2Dod	0.56	216	2.59
30	Q4At	0.99	168	5.89
31	Q8Atd	7.42	600	12.37
32	Q4A1t	1.80	262	6.87
33	C4D1to	1.75	259	6.76
34	Q4a2t	0.70	123	5.69
35	Q10At	10.76	201	53.53
36	O3At	0.20	127	1.57
37	N10Dto	4.30	282	15.25
38	N10D2to	4.03	273	14.76
39	N10Ato	3.96	273	14.51
40	N1A4d	0.09	59	1.53
41	Q7Aat	5.04	340	14.82
42	Q3At	1.20	142	8.45
43	O15ata	0.87	154	5.65
44	Q11atd	8.31	507	16.39
45	O5At	0.36	151	2.38
46	N27Aaod	7.76	317	24.48

Figure 1.1
SPICE3 with bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
47	N27A2t	20.94	527	39.73
48	N27A3o	3.03	147	20.61
49	N27A4o	3.25	147	22.11
50	N27A5o	21.34	500	42.68
51	N27A6aod	5.52	275	20.07
52	N12At	2.79	240	11.63
53	N8Ao	0.17	8	21.25
54	N2Ao	0.03	9	3.33
55	O6At	0.26	127	2.05
56	N1A5d	0.09	41	2.20
57	N6At	3.81	427	8.92
58	Q11Atad	10.59	667	15.88
59	Q5Ao	0.03	15	2.00
60	Q2Dtd	1.81	538	3.36
61	O66At	-	-	-
62	N2Dtdo	1.36	405	3.36
63	Q8Dtd	10.55	614	17.18
64	Q4A3t	2.29	341	6.72
65	Q50At	144.75	2208	65.56
66	O5A1t	0.23	151	1.52
67	C38Da	9.91	453	21.88
68	C38D2a	4.57	167	27.37
69	O6A1t	0.24	127	1.89
70	O3Ap	0.02	6	3.33
71	O7Ap	0.04	6	6.67
72	T1Atad	0.73	219	3.33
73	T2A1t	1.47	503	2.92
74	T1A1t	0.49	324	1.51
75	t1A2t	0.26	204	1.27
76	T3At	1.42	122	11.64
77	T3A2t	1.42	122	11.64
78	Q5Dtd	6.24	733	8.51
79	Q5D1td	6.09	762	7.99
80	Q7Dtd	7.45	743	10.03
81	Q6Dtd	6.86	743	9.23
82	Q5D2td	6.27	745	8.42
83	Q4A5ta	45.48	1630	27.90
84	Q15atad	10.62	412	25.78
85	Q22Atad	16.60	430	38.60
86	Q22A2tad	15.21	431	35.29
87	Q11Ata	5.11	202	25.30
88	Q11Ao	0.10	8	12.50
89	Q22A3tad	13.61	489	27.83
90	Q22A4tad	14.73	351	41.97
91	Q22A5tad	13.61	429	31.72
92	O3A1t	0.14	117	1.20
93	N9At	184.59	12798	14.42
94	O38Aa	0.38	3	126.67
95	C18At	12.26	492	24.92

Figure 1.1
SPICE3 with bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
96	C18A1t	9.39	517	18.16
97	Q18A2t	10.26	549	18.69
98	N4Ada	0.86	41	20.98
99	C14Dt	-	-	-
100	N804Dt	-	-	-
101	T1At	0.20	141	1.42
102	C19Mt	36.72	846	43.40
103	C68Dt	623.20	4501	138.46
104	C9Ao	0.21	9	23.33
105	C82Dt	-	-	-
106	C2At	1.03	155	6.65
107	C37Dt	81.17	1176	69.02
108	N27At	11.00	281	39.15
109	N698Dt	1837.14	3446	533.12
110	Q6At	416.57	58500	7.12
111	C7Atd	3.75	250	15.00
112	C52Aa	89.99	927	97.08
113	Q340t	2820.81	2300	1226.44
114	C54Dt	98.71	867	113.85
115	N1190Mt	-	-	-
116	C31Dt	95.96	1292	74.27
117	Q2A1t	19.41	4620	4.20
118	C119At	-	-	-
119	C6Dt	3.67	254	14.45
120	Q2A2t	8.20	2401	3.42
121	Q6A1t	14.07	1743	8.07
122	Q4A4ta	-	-	-
123	O4Ao	0.02	3	6.67
124	H44Aa	-	-	-
125	Q10Ao	0.24	12	20.00
126	C77Mt	-	-	-
127	Q4Af	0.03	9	3.33
128	N2Aa	0.36	6	60.00
129	N1Ad	0.28	111	2.52
130	O5A2t	0.16	129	1.24
131	O2At	0.15	231	0.65
132	O2A2t	0.06	118	0.51
133	C205At	993.12	6940	143.10
134	T2A2t	0.56	125	4.48
135	C26At	14.46	257	56.26
136	N1At	0.25	117	2.14
137	C37At	112.94	1254	90.06
138	N3At	3.82	595	6.42
139	C6D1t	1.40	248	5.65
140	Q86Aa	10.36	9	1151.11
141	C640Dt	1839.28	1611	1141.70
142	C1060Mt	735.25	788	933.06
143	Q14Ao	0.32	14	22.86
144	C28Dt	60.68	1779	34.11

Figure 1.1
SPICE3 with bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
145	C23Dt	12.26	472	25.97
146	O20At	0.67	227	2.95
147	C277Mt	670.45	2784	240.82
148	C277M2t	25.43	88	288.98
149	C42Dt	211.26	3268	64.65
150	C7Ad	2.58	250	10.32
151	C14D1t	45.90	1661	27.63
152	Q84At	1325.41	3575	370.74
153	Q50A1t	144.98	2208	65.66
154	O20A1t	4.21	939	4.48
144	total	13431.35	158489	
	average	93.27	1100	84.75

Figure 1.2
SPICE3 with bypass, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
1	Q180Do	-	-	-
2	Q180D2o	-	-	-
3	Q2At	3.00	790	3.80
4	O9Aa	-	-	-
5	O1024Ao	-	-	-
6	N48Dt	152.55	2568	59.40
7	N5At	1.55	179	8.66
8	N5A2t	1.53	169	9.05
9	O10At	1.03	453	2.27
10	Q6Ao	-	-	-
11	Q6A2o	-	-	-
12	Q4Ao	-	-	-
13	N1Aot	0.35	118	2.97
14	N1A2ot	0.30	118	2.54
15	N1A3ot	0.29	118	2.46
16	O8At	0.50	166	3.01
17	Q1Ado	-	-	-
18	Q1A2t	0.54	184	2.93
19	Q5Atd	1.41	195	7.23
20	C25Ao	-	-	-
21	C27Ao	-	-	-
22	C7Ao	-	-	-
23	C4Dto	2.92	468	6.24
24	C22Dt	9.15	211	43.36
25	C22D2o	-	-	-
26	T2At	0.40	122	3.28
27	Q7Ao	-	-	-
28	N116Dt	144.05	1294	111.32
29	N2Dod	-	-	-
30	Q4At	0.96	160	6.00
31	Q8Atd	5.03	379	13.27
32	Q4A1t	1.72	254	6.77
33	C4D1to	1.62	237	6.84
34	Q4a2t	0.67	114	5.88
35	Q10At	10.07	189	53.28
36	O3At	0.19	124	1.53
37	N10Dto	3.88	248	15.65
38	N10D2to	3.56	239	14.90
39	N10Ato	3.50	239	14.64
40	N1A4d	-	-	-
41	Q7Aat	3.29	258	12.75
42	Q3At	1.09	124	8.79
43	O15ata	0.41	148	2.77
44	Q11atd	5.01	278	18.02
45	O5At	0.34	147	2.31
46	N27Aaod	-	-	-
47	N27A2t	16.88	381	44.30
48	N27A3o	-	-	-

Figure 1.2
SPICE3 with bypass, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
49	N27A4o	-	-	-
50	N27A5o	19.67	429	45.85
51	N27A6aod	-	-	-
52	N12At	2.62	220	11.91
53	N8Ao	-	-	-
54	N2Ao	-	-	-
55	O6At	0.25	124	2.02
56	N1A5d	-	-	-
57	N6At	3.77	424	8.89
58	Q11Atad	6.41	440	14.57
59	Q5Ao	-	-	-
60	Q2Dtd	1.15	315	3.65
61	O66At	-	-	-
62	N2Dtdo	0.60	156	3.85
63	Q8Dtd	6.60	339	19.47
64	Q4A3t	2.25	333	6.76
65	Q50At	142.93	2167	65.96
66	O5A1t	0.22	148	1.49
67	C38Da	-	-	-
68	C38D2a	-	-	-
69	O6A1t	0.23	124	1.85
70	O3Ap	-	-	-
71	O7Ap	-	-	-
72	T1Atad	0.23	132	1.74
73	T2A1t	1.46	500	2.92
74	T1A1t	0.49	324	1.51
75	t1A2t	0.25	204	1.23
76	T3At	0.41	116	3.53
77	T3A2t	0.45	116	3.88
78	Q5Dtd	4.09	434	9.42
79	Q5D1td	4.04	457	8.84
80	Q7Dtd	4.92	454	10.84
81	Q6Dtd	4.42	438	10.09
82	Q5D2td	4.43	504	8.79
83	Q4A5ta	42.15	1620	26.02
84	Q15atad	3.86	173	22.31
85	Q22Atad	6.50	185	35.14
86	Q22A2tad	5.94	188	31.60
87	Q11Ata	3.32	186	17.85
88	Q11Ao	-	-	-
89	Q22A3tad	7.51	250	30.04
90	Q22A4tad	9.48	235	40.34
91	Q22A5tad	5.43	187	29.04
92	O3A1t	0.13	114	1.14
93	N9At	184.37	12783	14.42
94	O38Aa	-	-	-
95	C18At	11.84	474	24.98
96	C18A1t	8.68	464	18.71
97	Q18A2t	9.50	496	19.15

Figure 1.2
SPICE3 with bypass, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
98	N4Ada	-	-	-
99	C14Dt	-	-	-
100	N804Dt	-	-	-
101	T1At	0.20	138	1.45
102	C19Mt	36.35	838	43.38
103	C68Dt	621.49	4493	138.32
104	C9Ao	-	-	-
105	C82Dt	-	-	-
106	C2At	0.99	147	6.73
107	C37Dt	80.58	1166	69.11
108	N27At	10.42	264	39.47
109	N698Dt	1822.58	3409	534.64
110	Q6At	416.52	58489	7.12
111	C7Atd	2.69	160	16.81
112	C52Aa	-	-	-
113	Q340t	2647.79	2168	1221.31
114	C54Dt	97.03	862	112.56
115	N1190Mt	-	-	-
116	C31Dt	92.49	1233	75.01
117	Q2A1t	19.39	4620	4.20
118	C119At	-	-	-
119	C6Dt	3.59	247	14.53
120	Q2A2t	8.17	2393	3.41
121	Q6A1t	14.03	1734	8.09
122	Q4A4ta	-	-	-
123	O4Ao	-	-	-
124	H44Aa	-	-	-
125	Q10Ao	-	-	-
126	C77Mt	-	-	-
127	Q4Af	-	-	-
128	N2Aa	-	-	-
129	N1Ad	-	-	-
130	O5A2t	0.16	126	1.27
131	O2At	0.14	228	0.61
132	O2A2t	0.05	114	0.44
133	C205At	991.19	6926	143.11
134	T2A2t	0.54	122	4.43
135	C26At	13.57	240	56.54
136	N1At	0.24	114	2.11
137	C37At	112.02	1242	90.19
138	N3At	3.75	585	6.41
139	C6D1t	1.31	228	5.75
140	Q86Aa	-	-	-
141	C640Dt	1819.28	1599	1137.76
142	C1060Mt	684.03	713	959.37
143	Q14Ao	-	-	-
144	C28Dt	60.37	1764	34.22
145	C23Dt	12.09	465	26.00
146	O20At	0.67	227	2.95

Figure 1.2
SPICE3 with bypass, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
147	C277Mt	669.78	2784	240.58
148	C277M2t	24.80	88	281.82
149	C42Dt	114.75	1242	92.39
150	C7Ad	-	-	-
151	C14D1t	45.85	1661	27.60
152	Q84At	1308.16	3543	369.22
153	Q50A1t	143.15	2167	66.06
154	O20A1t	4.19	936	4.48
105	total	12772.79	146400	
	average	121.65	1394	87.25

Figure 1.3
SPICE3 with bypass, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
1	Q180Do	4.34	2.06	2.10	1.22
2	Q180D2o	4.47	2.15	2.02	1.16
3	Q2At	1.76	0.01	0.30	0.24
4	O9Aa	0.00	0.00	0.00	0.00
5	O1024Ao	0.01	0.00	0.00	0.00
6	N48Dt	134.22	0.06	4.67	2.80
7	N5At	1.12	0.00	0.08	0.07
8	N5A2t	1.15	0.00	0.06	0.06
9	O10At	0.38	0.00	0.08	0.06
10	Q6Ao	0.04	0.00	0.01	0.00
11	Q6A2o	-	-	-	-
12	Q4Ao	0.00	0.01	0.01	0.00
13	N1Aot	0.12	0.01	0.01	0.01
14	N1A2ot	0.12	0.00	0.03	0.02
15	N1A3ot	0.14	0.00	0.01	0.02
16	O8At	0.20	0.00	0.04	0.04
17	Q1Ado	0.06	0.00	0.02	0.02
18	Q1A2t	0.28	0.00	0.03	0.02
19	Q5Atd	1.27	0.02	0.20	0.08
20	C25Ao	1.90	0.05	0.34	0.18
21	C27Ao	2.19	0.05	0.20	0.23
22	C7Ao	0.74	0.01	0.08	0.02
23	C4Dto	2.17	0.01	0.09	0.08
24	C22Dt	6.59	0.10	0.88	0.44
25	C22D2o	0.29	0.08	0.06	0.01
26	T2At	0.03	0.02	0.10	0.02
27	Q7Ao	0.05	0.01	0.01	0.00
28	N116Dt	101.34	0.23	6.40	4.61
29	N2Dod	0.37	0.00	0.00	0.00
30	Q4At	0.55	0.01	0.09	0.03
31	Q8Atd	3.43	0.06	1.19	0.66
32	Q4A1t	0.89	0.01	0.16	0.11
33	C4D1to	1.18	0.01	0.03	0.07
34	Q4a2t	0.37	0.00	0.01	0.06
35	Q10At	3.83	0.41	2.24	1.25
36	O3At	0.03	0.00	0.01	0.06
37	N10Dto	3.37	0.00	0.08	0.09
38	N10D2to	3.15	0.02	0.09	0.09
39	N10Ato	3.09	0.01	0.06	0.12
40	N1A4d	0.04	0.00	0.00	0.00
41	Q7Aat	2.75	0.04	0.23	0.19
42	Q3At	0.46	0.03	0.18	0.10
43	O15ata	0.11	0.01	0.06	0.03
44	Q11atd	4.13	0.07	1.02	0.64
45	O5At	0.18	0.00	0.01	0.03
46	N27Aaod	5.55	0.04	0.33	0.23
47	N27A2t	17.18	0.03	0.71	0.60
48	N27A3o	2.61	0.05	0.17	0.12

Figure 1.3
SPICE3 with bypass, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
49	N27A4o	2.72	0.02	0.22	0.18
50	N27A5o	17.45	0.03	0.64	0.52
51	N27A6aod	3.44	0.03	0.23	0.17
52	N12At	1.82	0.01	0.06	0.05
53	N8Ao	0.11	0.02	0.00	0.00
54	N2Ao	0.00	0.02	0.00	0.01
55	O6At	0.10	0.00	0.00	0.01
56	N1A5d	0.05	0.00	0.01	0.01
57	N6At	2.59	0.02	0.06	0.21
58	Q11Atad	5.30	0.07	0.86	0.47
59	Q5Ao	0.03	0.00	0.00	0.00
60	Q2Dtd	0.80	0.02	0.14	0.11
61	O66At	-	-	-	-
62	N2Dtdo	0.81	0.00	0.01	0.02
63	Q8Dtd	5.33	0.08	1.37	0.80
64	Q4A3t	1.22	0.02	0.24	0.15
65	Q50At	83.84	0.37	20.78	11.89
66	O5A1t	0.03	0.01	0.00	0.02
67	C38Da	7.87	0.08	1.12	0.70
68	C38D2a	3.34	0.20	0.58	0.33
69	O6A1t	0.09	0.00	0.00	0.00
70	O3Ap	0.00	0.00	0.00	0.00
71	O7Ap	0.00	0.00	0.00	0.00
72	T1Atad	0.03	0.02	0.04	0.01
73	T2A1t	0.20	0.01	0.13	0.22
74	T1A1t	0.08	0.00	0.03	0.01
75	t1A2t	0.06	0.00	0.01	0.01
76	T3At	0.05	0.01	0.06	0.02
77	T3A2t	0.06	0.02	0.10	0.04
78	Q5Dtd	3.12	0.04	0.90	0.58
79	Q5D1td	3.07	0.02	0.77	0.56
80	Q7Dtd	3.73	0.06	1.00	0.78
81	Q6Dtd	3.40	0.04	0.83	0.85
82	Q5D2td	3.14	0.04	0.75	0.56
83	Q4A5ta	9.10	0.40	22.06	5.89
84	Q15atad	3.77	0.11	1.14	0.65
85	Q22Atad	7.17	0.21	1.57	0.85
86	Q22A2tad	5.79	0.17	1.56	1.06
87	Q11Ata	1.87	0.06	0.47	0.22
88	Q11Ao	0.04	0.02	0.02	0.00
89	Q22A3tad	6.73	0.17	1.53	0.77
90	Q22A4tad	5.53	0.25	1.74	1.33
91	Q22A5tad	5.53	0.15	1.33	0.74
92	O3A1t	0.03	0.00	0.00	0.02
93	N9At	144.41	0.02	11.08	7.14
94	O38Aa	0.00	0.03	0.00	0.00
95	C18At	6.39	0.13	2.34	0.96
96	C18A1t	5.02	0.11	1.45	0.86
97	Q18A2t	5.56	0.11	1.57	1.18

Figure 1.3
SPICE3 with bypass, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
98	N4Ada	0.22	0.00	0.00	0.02
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	0.01	0.00	0.01	0.01
102	C19Mt	27.43	0.09	2.21	1.77
103	C68Dt	459.86	0.78	67.39	36.42
104	C9Ao	0.14	0.02	0.00	0.01
105	C82Dt	-	-	-	-
106	C2At	0.64	0.01	0.05	0.02
107	C37Dt	68.71	0.07	2.01	1.75
108	N27At	8.46	0.02	0.26	0.25
109	N698Dt	1149.88	4.17	160.90	84.82
110	Q6At	301.71	0.00	30.96	24.64
111	C7Atd	3.09	0.00	0.07	0.04
112	C52Aa	45.59	2.05	25.61	4.99
113	Q340t	936.10	69.93	1286.26	234.46
114	C54Dt	43.18	1.49	29.62	10.87
115	N1190Mt	-	-	-	-
116	C31Dt	75.70	0.19	7.04	4.66
117	Q2A1t	9.69	0.00	3.24	1.48
118	C119At	-	-	-	-
119	C6Dt	3.17	0.00	0.01	0.04
120	Q2A2t	5.33	0.01	0.53	0.43
121	Q6A1t	10.67	0.00	0.66	0.64
122	Q4A4ta	-	-	-	-
123	O4Ao	0.00	0.00	0.00	0.00
124	H44Aa	-	-	-	-
125	Q10Ao	0.09	0.06	0.03	0.00
126	C77Mt	-	-	-	-
127	Q4Af	0.01	0.01	0.00	0.00
128	N2Aa	0.03	0.00	0.00	0.00
129	N1Ad	0.18	0.00	0.01	0.02
130	O5A2t	0.06	0.00	0.01	0.00
131	O2At	0.02	0.00	0.01	0.00
132	O2A2t	0.00	0.00	0.00	0.00
133	C205At	737.60	0.57	83.79	44.31
134	T2A2t	0.15	0.01	0.06	0.05
135	C26At	8.16	0.25	2.00	0.87
136	N1At	0.13	0.00	0.00	0.00
137	C37At	93.46	0.30	7.84	2.35
138	N3At	3.08	0.00	0.09	0.09
139	C6D1t	0.77	0.00	0.07	0.11
140	Q86Aa	0.48	1.11	0.24	0.11
141	C640Dt	1159.93	17.07	456.18	52.36
142	C1060Mt	563.13	8.55	72.93	21.72
143	Q14Ao	0.15	0.05	0.03	0.03
144	C28Dt	44.01	0.02	1.66	1.32
145	C23Dt	9.88	0.01	0.37	0.22
146	O20At	0.12	0.00	0.03	0.08

Figure 1.3
SPICE3 with bypass, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
147	C277Mt	471.68	0.58	37.05	22.00
148	C277M2t	20.61	2.01	1.15	0.60
149	C42Dt	161.43	0.48	22.22	13.65
150	C7Ad	1.39	0.02	0.21	0.22
151	C14D1t	38.05	0.01	1.11	1.17
152	Q84At	491.09	14.63	327.42	162.34
153	Q50A1t	83.78	0.36	20.14	12.99
154	O20A1t	1.64	0.01	0.60	0.27
144	total	7719.76	133.82	2755.38	801.05
	average	53.61	0.93	19.13	5.56

1.3.2. SPICE3 without bypass

Figure 1.4
SPICE3 without bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
1	Q180Do	11.27	53	212.64
2	Q180D2o	11.51	53	217.17
3	Q2At	3.51	917	3.83
4	O9Aa	0.09	3	30.00
5	O1024Ao	0.10	3	33.33
6	N48Dt	209.88	2570	81.67
7	N5At	1.88	206	9.13
8	N5A2t	1.80	195	9.23
9	O10At	1.08	456	2.37
10	Q6Ao	0.06	13	4.62
11	Q6A2o	-	-	-
12	Q4Ao	0.06	7	8.57
13	N1Aot	0.55	188	2.93
14	N1A2ot	0.51	188	2.71
15	N1A3ot	0.53	188	2.82
16	O8At	0.35	166	2.11
17	Q1Ado	0.12	66	1.82
18	Q1A2t	0.61	193	3.16
19	Q5Atd	2.47	424	5.83
20	C25Ao	3.48	155	22.45
21	C27Ao	3.72	141	26.38
22	C7Ao	0.95	138	6.88
23	C4Dto	2.96	469	6.31
24	C22Dt	10.76	226	47.61
25	C22D2o	0.60	14	42.86
26	T2At	0.38	125	3.04
27	Q7Ao	0.08	13	6.15
28	N116Dt	162.55	1320	123.14
29	N2Dod	0.65	216	3.01
30	Q4At	1.16	168	6.90
31	Q8Atd	7.81	605	12.91
32	Q4A1t	1.77	258	6.86
33	C4D1to	1.70	259	6.56
34	Q4a2t	0.71	123	5.77
35	Q10At	10.59	189	56.03
36	O3At	0.24	127	1.89
37	N10Dto	5.36	274	19.56
38	N10D2to	4.91	259	18.96
39	N10Ato	4.86	259	18.76
40	N1A4d	0.08	59	1.36
41	Q7Aat	5.22	338	15.44
42	Q3At	1.25	142	8.80
43	O15ata	0.82	154	5.32
44	Q11atd	8.71	505	17.25
45	O5At	0.38	151	2.52
46	N27Aaod	9.59	309	31.04

Figure 1.4
SPICE3 without bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
47	N27A2t	22.96	533	43.08
48	N27A3o	3.84	147	26.12
49	N27A4o	3.83	147	26.05
50	N27A5o	22.85	556	41.10
51	N27A6aod	6.03	265	22.75
52	N12At	2.78	240	11.58
53	N8Ao	0.19	8	23.75
54	N2Ao	0.05	9	5.56
55	O6At	0.28	127	2.20
56	N1A5d	0.10	41	2.44
57	N6At	4.14	427	9.70
58	Q11Atad	11.38	685	16.61
59	Q5Ao	0.05	15	3.33
60	Q2Dtd	1.66	477	3.48
61	O66At	-	-	-
62	N2Dtdo	1.44	400	3.60
63	Q8Dtd	10.73	612	17.53
64	Q4A3t	2.45	357	6.86
65	Q50At	158.24	2244	70.52
66	O5A1t	0.19	151	1.26
67	C38Da	15.00	544	27.57
68	C38D2a	5.53	167	33.11
69	O6A1t	0.23	127	1.81
70	O3Ap	0.02	6	3.33
71	O7Ap	0.05	6	8.33
72	T1Atad	0.62	219	2.83
73	T2A1t	1.41	503	2.80
74	T1A1t	0.53	324	1.64
75	t1A2t	0.31	204	1.52
76	T3At	1.44	122	11.80
77	T3A2t	1.46	122	11.97
78	Q5Dtd	6.16	733	8.40
79	Q5D1td	6.26	759	8.25
80	Q7Dtd	7.76	742	10.46
81	Q6Dtd	7.94	975	8.14
82	Q5D2td	6.17	698	8.84
83	Q4A5ta	52.25	1805	28.95
84	Q15atad	10.90	408	26.72
85	Q22Atad	17.77	423	42.01
86	Q22A2tad	15.89	421	37.74
87	Q11Ata	5.15	185	27.84
88	Q11Ao	0.13	8	16.25
89	Q22A3tad	14.13	466	30.32
90	Q22A4tad	13.38	279	47.96
91	Q22A5tad	13.36	410	32.59
92	O3A1t	0.11	117	0.94
93	N9At	274.21	16619	16.50
94	O38Aa	0.38	3	126.67
95	C18At	12.13	490	24.76

Figure 1.4
SPICE3 without bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
96	C18A1t	9.59	538	17.83
97	Q18A2t	9.80	547	17.92
98	N4Ada	0.92	41	22.44
99	C14Dt	-	-	-
100	N804Dt	-	-	-
101	T1At	0.25	141	1.77
102	C19Mt	41.83	846	49.44
103	C68Dt	763.43	4505	169.46
104	C9Ao	0.23	9	25.56
105	C82Dt	-	-	-
106	C2At	1.08	155	6.97
107	C37Dt	92.71	1184	78.30
108	N27At	14.28	300	47.60
109	N698Dt	2018.23	3454	584.32
110	Q6At	452.03	60280	7.50
111	C7Atd	4.22	250	16.88
112	C52Aa	18.40	135	136.30
113	Q340t	2950.75	2160	1366.09
114	C54Dt	109.63	902	121.54
115	N1190Mt	-	-	-
116	C31Dt	108.50	1327	81.76
117	Q2A1t	2806.07	715358	3.92
118	C119At	-	-	-
119	C6Dt	3.72	254	14.65
120	Q2A2t	8.51	2401	3.54
121	Q6A1t	14.18	1743	8.14
122	Q4A4ta	-	-	-
123	O4Ao	0.01	3	3.33
124	H44Aa	-	-	-
125	Q10Ao	0.23	12	19.17
126	C77Mt	-	-	-
127	Q4Af	0.04	9	4.44
128	N2Aa	0.40	6	66.67
129	N1Ad	0.31	111	2.79
130	O5A2t	0.15	129	1.16
131	O2At	0.18	231	0.78
132	O2A2t	0.09	118	0.76
133	C205At	1108.77	6918	160.27
134	T2A2t	0.62	125	4.96
135	C26At	15.53	257	60.43
136	N1At	0.27	117	2.31
137	C37At	113.85	1233	92.34
138	N3At	4.07	598	6.81
139	C6D1t	1.32	246	5.37
140	Q86Aa	10.48	9	1164.44
141	C640Dt	1944.77	1618	1201.96
142	C1060Mt	966.41	691	1398.57
143	Q14Ao	0.32	14	22.86
144	C28Dt	65.12	1771	36.77

Figure 1.4
SPICE3 without bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
145	C23Dt	14.13	482	29.32
146	O20At	0.76	227	3.35
147	C277Mt	849.80	2882	294.86
148	C277M2t	34.57	88	392.84
149	C42Dt	216.48	3268	66.24
150	C7Ad	2.91	250	11.64
151	C14D1t	49.94	1555	32.12
152	Q84At	1420.36	3545	400.67
153	Q50A1t	160.79	2244	71.65
154	O20A1t	4.06	939	4.32
144	total	17656.64	874437	
	average	122.62	6072	20.19

Figure 1.5
SPICE3 without bypass, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
1	Q180Do	-	-	-
2	Q180D2o	-	-	-
3	Q2At	3.49	907	3.85
4	O9Aa	-	-	-
5	O1024Ao	-	-	-
6	N48Dt	208.53	2552	81.71
7	N5At	1.68	180	9.33
8	N5A2t	1.62	169	9.59
9	O10At	1.06	453	2.34
10	Q6Ao	-	-	-
11	Q6A2o	-	-	-
12	Q4Ao	-	-	-
13	N1Aot	0.50	182	2.75
14	N1A2ot	0.50	182	2.75
15	N1A3ot	0.50	182	2.75
16	O8At	0.35	166	2.11
17	Q1Ado	-	-	-
18	Q1A2t	0.58	184	3.15
19	Q5Atd	1.50	195	7.69
20	C25Ao	-	-	-
21	C27Ao	-	-	-
22	C7Ao	-	-	-
23	C4Dto	2.84	439	6.47
24	C22Dt	10.09	211	47.82
25	C22D2o	-	-	-
26	T2At	0.38	122	3.11
27	Q7Ao	-	-	-
28	N116Dt	159.95	1286	124.38
29	N2Dod	-	-	-
30	Q4At	1.11	160	6.94
31	Q8Atd	5.32	384	13.85
32	Q4A1t	1.74	250	6.96
33	C4D1to	1.58	237	6.67
34	Q4a2t	0.68	114	5.96
35	Q10At	9.85	177	55.65
36	O3At	0.21	124	1.69
37	N10Dto	4.77	240	19.88
38	N10D2to	4.36	225	19.38
39	N10Ato	4.30	225	19.11
40	N1A4d	-	-	-
41	Q7Aat	3.51	256	13.71
42	Q3At	1.13	124	9.11
43	O15ata	0.38	148	2.57
44	Q11atd	5.28	276	19.13
45	O5At	0.36	147	2.45
46	N27Aaod	-	-	-
47	N27A2t	17.75	387	45.87
48	N27A3o	-	-	-

Figure 1.5
SPICE3 without bypass, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
49	N27A4o	-	-	-
50	N27A5o	19.18	410	46.78
51	N27A6aod	-	-	-
52	N12At	2.64	220	12.00
53	N8Ao	-	-	-
54	N2Ao	-	-	-
55	O6At	0.26	124	2.10
56	N1A5d	-	-	-
57	N6At	4.08	424	9.62
58	Q11Atad	7.11	458	15.52
59	Q5Ao	-	-	-
60	Q2Dtd	0.97	254	3.82
61	O66At	-	-	-
62	N2Dtdo	0.64	151	4.24
63	Q8Dtd	6.69	337	19.85
64	Q4A3t	2.42	349	6.93
65	Q50At	156.21	2203	70.91
66	O5A1t	0.19	148	1.28
67	C38Da	-	-	-
68	C38D2a	-	-	-
69	O6A1t	0.21	124	1.69
70	O3Ap	-	-	-
71	O7Ap	-	-	-
72	T1Atad	0.18	132	1.36
73	T2A1t	1.40	500	2.80
74	T1A1t	0.52	324	1.60
75	t1A2t	0.30	204	1.47
76	T3At	0.41	116	3.53
77	T3A2t	0.46	116	3.97
78	Q5Dtd	4.05	433	9.35
79	Q5D1td	4.15	461	9.00
80	Q7Dtd	5.19	453	11.46
81	Q6Dtd	4.44	436	10.18
82	Q5D2td	4.34	457	9.50
83	Q4A5ta	48.89	1795	27.24
84	Q15atad	4.25	169	25.15
85	Q22Atad	7.21	178	40.51
86	Q22A2tad	6.18	178	34.72
87	Q11Ata	3.29	169	19.47
88	Q11Ao	-	-	-
89	Q22A3tad	7.64	227	33.66
90	Q22A4tad	7.63	163	46.81
91	Q22A5tad	5.31	168	31.61
92	O3A1t	0.10	114	0.88
93	N9At	273.96	16604	16.50
94	O38Aa	-	-	-
95	C18At	11.67	472	24.72
96	C18A1t	8.82	485	18.19
97	Q18A2t	9.08	494	18.38

Figure 1.5
SPICE3 without bypass, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
98	N4Ada	-	-	-
99	C14Dt	-	-	-
100	N804Dt	-	-	-
101	T1At	0.23	138	1.67
102	C19Mt	41.39	838	49.39
103	C68Dt	761.52	4497	169.34
104	C9Ao	-	-	-
105	C82Dt	-	-	-
106	C2At	1.02	147	6.94
107	C37Dt	91.93	1174	78.30
108	N27At	13.61	283	48.09
109	N698Dt	2002.32	3417	585.99
110	Q6At	451.95	60269	7.50
111	C7Atd	2.98	160	18.63
112	C52Aa	-	-	-
113	Q340t	2757.04	2009	1372.34
114	C54Dt	107.95	897	120.35
115	N1190Mt	-	-	-
116	C31Dt	104.09	1268	82.09
117	Q2A1t	2806.06	715358	3.92
118	C119At	-	-	-
119	C6Dt	3.60	247	14.57
120	Q2A2t	8.48	2393	3.54
121	Q6A1t	14.11	1734	8.14
122	Q4A4ta	-	-	-
123	O4Ao	-	-	-
124	H44Aa	-	-	-
125	Q10Ao	-	-	-
126	C77Mt	-	-	-
127	Q4Af	-	-	-
128	N2Aa	-	-	-
129	N1Ad	-	-	-
130	O5A2t	0.15	126	1.19
131	O2At	0.18	228	0.79
132	O2A2t	0.08	114	0.70
133	C205At	1106.50	6904	160.27
134	T2A2t	0.58	122	4.75
135	C26At	14.62	240	60.92
136	N1At	0.26	114	2.28
137	C37At	112.73	1221	92.33
138	N3At	3.97	588	6.75
139	C6D1t	1.25	226	5.53
140	Q86Aa	-	-	-
141	C640Dt	1921.67	1606	1196.56
142	C1060Mt	877.84	620	1415.87
143	Q14Ao	-	-	-
144	C28Dt	64.72	1756	36.86
145	C23Dt	13.92	475	29.31
146	O20At	0.74	227	3.26

Figure 1.5
SPICE3 without bypass, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
147	C277Mt	849.13	2882	294.63
148	C277M2t	33.85	88	384.66
149	C42Dt	118.48	1242	95.39
150	C7Ad	-	-	-
151	C14D1t	49.91	1555	32.10
152	Q84At	1401.75	3513	399.02
153	Q50A1t	158.85	2203	72.11
154	O20A1t	4.01	936	4.28
105	total	16979.44	862749	
	average	161.71	8216	19.68

Figure 1.6
SPICE3 without bypass, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
1	Q180Do	5.08	2.09	2.13	1.24
2	Q180D2o	5.40	2.11	2.11	1.18
3	Q2At	2.10	0.00	0.47	0.19
4	O9Aa	0.00	0.00	0.00	0.00
5	O1024Ao	0.02	0.00	0.00	0.00
6	N48Dt	190.68	0.05	4.89	3.36
7	N5At	1.42	0.01	0.02	0.02
8	N5A2t	1.50	0.00	0.02	0.02
9	O10At	0.39	0.00	0.09	0.07
10	Q6Ao	0.01	0.01	0.02	0.00
11	Q6A2o	-	-	-	-
12	Q4Ao	0.01	0.02	0.00	0.00
13	N1Aot	0.21	0.01	0.04	0.04
14	N1A2ot	0.25	0.00	0.04	0.03
15	N1A3ot	0.25	0.00	0.01	0.01
16	O8At	0.14	0.01	0.01	0.02
17	Q1Ado	0.04	0.00	0.01	0.01
18	Q1A2t	0.36	0.00	0.03	0.03
19	Q5Atd	1.41	0.00	0.17	0.16
20	C25Ao	2.99	0.04	0.22	0.12
21	C27Ao	3.10	0.05	0.30	0.15
22	C7Ao	0.75	0.02	0.05	0.05
23	C4Dto	2.17	0.00	0.08	0.11
24	C22Dt	7.78	0.12	0.80	0.38
25	C22D2o	0.37	0.09	0.03	0.01
26	T2At	0.06	0.00	0.02	0.05
27	Q7Ao	0.05	0.01	0.00	0.00
28	N116Dt	117.58	0.27	6.41	4.86
29	N2Dod	0.42	0.00	0.02	0.02
30	Q4At	0.72	0.02	0.02	0.06
31	Q8Atd	3.94	0.05	1.06	0.58
32	Q4A1t	0.89	0.01	0.27	0.13
33	C4D1to	1.15	0.02	0.07	0.05
34	Q4a2t	0.37	0.01	0.04	0.03
35	Q10At	3.95	0.45	2.09	1.06
36	O3At	0.15	0.00	0.01	0.00
37	N10Dto	4.59	0.01	0.07	0.07
38	N10D2to	4.06	0.00	0.09	0.10
39	N10Ato	3.98	0.00	0.09	0.05
40	N1A4d	0.00	0.00	0.01	0.01
41	Q7Aat	3.01	0.02	0.24	0.18
42	Q3At	0.47	0.04	0.15	0.08
43	O15ata	0.14	0.02	0.06	0.01
44	Q11atd	4.55	0.08	0.88	0.57
45	O5At	0.16	0.00	0.00	0.03
46	N27Aaod	7.54	0.03	0.27	0.26
47	N27A2t	19.58	0.07	0.72	0.42
48	N27A3o	3.40	0.02	0.13	0.17

Figure 1.6
SPICE3 without bypass, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
49	N27A4o	3.29	0.03	0.23	0.14
50	N27A5o	18.94	0.06	0.76	0.49
51	N27A6aod	3.85	0.03	0.24	0.16
52	N12At	1.74	0.00	0.11	0.07
53	N8Ao	0.15	0.03	0.00	0.00
54	N2Ao	0.04	0.00	0.00	0.00
55	O6At	0.07	0.00	0.01	0.03
56	N1A5d	0.05	0.00	0.00	0.02
57	N6At	2.91	0.02	0.13	0.11
58	Q11Atad	6.01	0.04	0.89	0.54
59	Q5Ao	0.02	0.01	0.00	0.00
60	Q2Dtd	0.75	0.01	0.07	0.10
61	O66At	-	-	-	-
62	N2Dtdo	0.86	0.00	0.05	0.08
63	Q8Dtd	5.35	0.08	1.55	0.90
64	Q4A3t	1.31	0.00	0.27	0.22
65	Q50At	96.55	0.35	20.35	12.95
66	O5A1t	0.08	0.00	0.01	0.00
67	C38Da	12.88	0.08	1.10	0.75
68	C38D2a	4.15	0.18	0.80	0.27
69	O6A1t	0.06	0.00	0.03	0.01
70	O3Ap	0.00	0.00	0.00	0.01
71	O7Ap	0.01	0.00	0.00	0.00
72	T1Atad	0.03	0.01	0.04	0.06
73	T2A1t	0.17	0.01	0.24	0.09
74	T1A1t	0.10	0.00	0.03	0.06
75	t1A2t	0.04	0.00	0.02	0.02
76	T3At	0.02	0.03	0.09	0.04
77	T3A2t	0.05	0.03	0.08	0.04
78	Q5Dtd	3.23	0.04	0.73	0.52
79	Q5D1td	3.27	0.04	0.94	0.51
80	Q7Dtd	4.30	0.06	0.88	0.65
81	Q6Dtd	4.52	0.03	0.99	0.65
82	Q5D2td	3.35	0.01	0.60	0.44
83	Q4A5ta	11.31	0.39	25.93	6.31
84	Q15atad	4.26	0.12	1.18	0.67
85	Q22Atad	8.27	0.19	1.78	0.85
86	Q22A2tad	6.37	0.19	1.49	1.03
87	Q11Ata	1.94	0.07	0.40	0.15
88	Q11Ao	0.07	0.02	0.00	0.00
89	Q22A3tad	7.06	0.16	1.57	0.78
90	Q22A4tad	5.58	0.28	1.61	0.92
91	Q22A5tad	5.62	0.14	1.25	0.69
92	O3A1t	0.03	0.00	0.00	0.01
93	N9At	221.77	0.03	13.76	10.07
94	O38Aa	0.00	0.01	0.00	0.01
95	C18At	6.08	0.14	2.25	1.06
96	C18A1t	5.43	0.10	1.66	0.54
97	Q18A2t	5.73	0.13	1.58	0.48

Figure 1.6
SPICE3 without bypass, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
98	N4Ada	0.26	0.01	0.02	0.02
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	0.03	0.01	0.01	0.03
102	C19Mt	32.41	0.11	2.29	1.92
103	C68Dt	604.47	0.80	64.79	36.11
104	C9Ao	0.15	0.03	0.01	0.00
105	C82Dt	-	-	-	-
106	C2At	0.68	0.01	0.07	0.05
107	C37Dt	81.05	0.08	1.64	1.62
108	N27At	11.49	0.04	0.30	0.19
109	N698Dt	1343.73	4.11	156.70	83.01
110	Q6At	336.88	0.01	29.30	23.79
111	C7Atd	3.48	0.02	0.10	0.09
112	C52Aa	9.88	0.87	1.91	0.71
113	Q340t	1150.56	70.34	1211.07	221.62
114	C54Dt	51.06	1.49	31.82	11.28
115	N1190Mt	-	-	-	-
116	C31Dt	87.58	0.21	7.34	4.64
117	Q2A1t	1611.55	0.00	482.72	301.89
118	C119At	-	-	-	-
119	C6Dt	3.15	0.01	0.08	0.01
120	Q2A2t	5.63	0.00	0.63	0.51
121	Q6A1t	11.20	0.00	0.55	0.41
122	Q4A4ta	-	-	-	-
123	O4Ao	0.00	0.01	0.00	0.00
124	H44Aa	-	-	-	-
125	Q10Ao	0.07	0.06	0.04	0.01
126	C77Mt	-	-	-	-
127	Q4Af	0.02	0.00	0.00	0.00
128	N2Aa	0.01	0.00	0.00	0.00
129	N1Ad	0.17	0.00	0.01	0.04
130	O5A2t	0.04	0.01	0.00	0.00
131	O2At	0.04	0.00	0.01	0.00
132	O2A2t	0.02	0.00	0.01	0.01
133	C205At	847.95	0.58	87.83	43.96
134	T2A2t	0.06	0.03	0.06	0.09
135	C26At	9.10	0.27	2.05	0.72
136	N1At	0.18	0.00	0.00	0.00
137	C37At	94.30	0.25	7.83	2.65
138	N3At	3.12	0.00	0.19	0.13
139	C6D1t	0.76	0.01	0.08	0.05
140	Q86Aa	0.53	1.12	0.24	0.14
141	C640Dt	1253.07	17.44	466.35	52.78
142	C1060Mt	810.38	8.84	65.53	19.33
143	Q14Ao	0.14	0.04	0.04	0.02
144	C28Dt	47.95	0.02	1.75	1.43
145	C23Dt	11.76	0.00	0.24	0.24
146	O20At	0.17	0.00	0.03	0.08

Figure 1.6
SPICE3 without bypass, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
147	C277Mt	645.95	0.63	38.82	22.46
148	C277M2t	29.62	2.05	1.04	0.71
149	C42Dt	165.77	0.43	22.05	14.07
150	C7Ad	1.72	0.02	0.26	0.15
151	C14D1t	42.18	0.01	1.21	1.15
152	Q84At	574.42	15.67	335.01	163.86
153	Q50A1t	99.40	0.35	20.11	13.20
154	O20A1t	1.69	0.02	0.55	0.32
144	total	10860.69	134.92	3152.65	1084.99
	average	75.42	0.94	21.89	7.53

1.3.3. SPICE3 with bypass using the gcc compiler

Figure 1.7
SPICE3 with bypass using the gcc compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
1	Q180Do	10.05	53	189.62
2	Q180D2o	10.00	53	188.68
3	Q2At	2.85	800	3.56
4	O9Aa	0.08	3	26.67
5	O1024Ao	0.09	3	30.00
6	N48Dt	134.19	2586	51.89
7	N5At	1.54	205	7.51
8	N5A2t	1.50	195	7.69
9	O10At	0.94	456	2.06
10	Q6Ao	0.04	13	3.08
11	Q6A2o	-	-	-
12	Q4Ao	0.03	7	4.29
13	N1Aot	0.33	124	2.66
14	N1A2ot	0.32	124	2.58
15	N1A3ot	0.32	124	2.58
16	O8At	0.42	166	2.53
17	Q1Ado	0.13	66	1.97
18	Q1A2t	0.54	193	2.80
19	Q5Atd	2.16	424	5.09
20	C25Ao	2.37	155	15.29
21	C27Ao	2.43	141	17.23
22	C7Ao	0.86	138	6.23
23	C4Dto	2.66	498	5.34
24	C22Dt	8.66	226	38.32
25	C22D2o	0.49	14	35.00
26	T2At	0.43	125	3.44
27	Q7Ao	0.11	13	8.46
28	N116Dt	132.18	1328	99.53
29	N2Dod	0.48	216	2.22
30	Q4At	1.08	168	6.43
31	Q8Atd	6.97	600	11.62
32	Q4A1t	1.69	262	6.45
33	C4D1to	1.51	259	5.83
34	Q4a2t	0.65	123	5.28
35	Q10At	10.04	201	49.95
36	O3At	0.18	127	1.42
37	N10Dto	3.84	282	13.62
38	N10D2to	3.53	273	12.93
39	N10Ato	3.53	273	12.93
40	N1A4d	0.10	59	1.69
41	Q7Aat	4.85	340	14.26
42	Q3At	1.13	142	7.96
43	O15ata	0.76	154	4.94
44	Q11atd	8.07	507	15.92
45	O5At	0.34	151	2.25
46	N27Aaod	6.95	317	21.92

Figure 1.7
SPICE3 with bypass using the gcc compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
47	N27A2t	18.55	527	35.20
48	N27A3o	2.70	147	18.37
49	N27A4o	2.66	147	18.10
50	N27A5o	18.55	500	37.10
51	N27A6aod	4.93	275	17.93
52	N12At	2.52	240	10.50
53	N8Ao	0.18	8	22.50
54	N2Ao	0.04	9	4.44
55	O6At	0.25	127	1.97
56	N1A5d	0.10	41	2.44
57	N6At	3.32	427	7.78
58	Q11Atad	10.69	667	16.03
59	Q5Ao	0.07	15	4.67
60	Q2Dtd	1.71	538	3.18
61	O66At	-	-	-
62	N2Dtdo	1.15	405	2.84
63	Q8Dtd	9.93	614	16.17
64	Q4A3t	2.23	341	6.54
65	Q50At	137.46	2208	62.26
66	O5A1t	0.20	151	1.32
67	C38Da	8.90	453	19.65
68	C38D2a	3.91	167	23.41
69	O6A1t	0.21	127	1.65
70	O3Ap	0.02	6	3.33
71	O7Ap	0.04	6	6.67
72	T1Atad	0.61	219	2.79
73	T2A1t	1.27	503	2.52
74	T1A1t	0.48	324	1.48
75	t1A2t	0.26	204	1.27
76	T3At	1.39	122	11.39
77	T3A2t	1.38	122	11.31
78	Q5Dtd	5.58	733	7.61
79	Q5D1td	5.89	762	7.73
80	Q7Dtd	6.98	743	9.39
81	Q6Dtd	6.17	743	8.30
82	Q5D2td	6.11	745	8.20
83	Q4A5ta	42.97	1630	26.36
84	Q15atad	10.07	412	24.44
85	Q22Atad	15.98	430	37.16
86	Q22A2tad	14.43	431	33.48
87	Q11Ata	4.88	202	24.16
88	Q11Ao	0.11	8	13.75
89	Q22A3tad	12.89	489	26.36
90	Q22A4tad	14.26	351	40.63
91	Q22A5tad	13.16	429	30.68
92	O3A1t	0.11	117	0.94
93	N9At	171.24	12798	13.38
94	O38Aa	0.39	3	130.00
95	C18At	11.62	492	23.62

Figure 1.7
SPICE3 with bypass using the gcc compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
96	C18A1t	8.23	517	15.92
97	Q18A2t	8.84	549	16.10
98	N4Ada	0.83	41	20.24
99	C14Dt	-	-	-
100	N804Dt	-	-	-
101	T1At	0.20	141	1.42
102	C19Mt	33.22	846	39.27
103	C68Dt	562.27	4501	124.92
104	C9Ao	0.22	9	24.44
105	C82Dt	-	-	-
106	C2At	0.98	155	6.32
107	C37Dt	73.37	1176	62.39
108	N27At	9.84	281	35.02
109	N698Dt	1649.64	3446	478.71
110	Q6At	405.52	58500	6.93
111	C7Atd	3.34	250	13.36
112	C52Aa	84.03	927	90.65
113	Q340t	2731.82	2300	1187.75
114	C54Dt	92.90	867	107.15
115	N1190Mt	-	-	-
116	C31Dt	90.57	1292	70.10
117	Q2A1t	18.45	4620	3.99
118	C119At	-	-	-
119	C6Dt	3.24	254	12.76
120	Q2A2t	7.82	2401	3.26
121	Q6A1t	13.89	1743	7.97
122	Q4A4ta	-	-	-
123	O4Ao	0.00	3	0.00
124	H44Aa	-	-	-
125	Q10Ao	0.21	12	17.50
126	C77Mt	-	-	-
127	Q4Af	0.03	9	3.33
128	N2Aa	0.34	6	56.67
129	N1Ad	0.23	111	2.07
130	O5A2t	0.18	129	1.40
131	O2At	0.17	231	0.74
132	O2A2t	0.08	118	0.68
133	C205At	939.80	6940	135.42
134	T2A2t	0.56	125	4.48
135	C26At	13.51	257	52.57
136	N1At	0.22	117	1.88
137	C37At	104.02	1254	82.95
138	N3At	3.33	595	5.60
139	C6D1t	1.25	248	5.04
140	Q86Aa	9.98	9	1108.89
141	C640Dt	1674.17	1611	1039.21
142	C1060Mt	654.28	788	830.30
143	Q14Ao	0.32	14	22.86
144	C28Dt	53.36	1779	29.99

Figure 1.7
SPICE3 with bypass using the gcc compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
145	C23Dt	11.44	472	24.24
146	O20At	0.74	227	3.26
147	C277Mt	638.20	2784	229.24
148	C277M2t	21.88	88	248.64
149	C42Dt	198.54	3268	60.75
150	C7Ad	2.43	250	9.72
151	C14D1t	40.14	1661	24.17
152	Q84At	1269.34	3575	355.06
153	Q50A1t	134.13	2208	60.75
154	O20A1t	3.71	939	3.95
144	total	12525.78	158489	
	average	86.98	1100	79.03

Figure 1.8
SPICE3 with bypass using the gcc compiler, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
1	Q180Do	-	-	-
2	Q180D2o	-	-	-
3	Q2At	2.82	790	3.57
4	O9Aa	-	-	-
5	O1024Ao	-	-	-
6	N48Dt	133.47	2568	51.97
7	N5At	1.38	179	7.71
8	N5A2t	1.34	169	7.93
9	O10At	0.94	453	2.08
10	Q6Ao	-	-	-
11	Q6A2o	-	-	-
12	Q4Ao	-	-	-
13	N1Aot	0.29	118	2.46
14	N1A2ot	0.29	118	2.46
15	N1A3ot	0.30	118	2.54
16	O8At	0.40	166	2.41
17	Q1Ado	-	-	-
18	Q1A2t	0.51	184	2.77
19	Q5Atd	1.29	195	6.62
20	C25Ao	-	-	-
21	C27Ao	-	-	-
22	C7Ao	-	-	-
23	C4Dto	2.56	468	5.47
24	C22Dt	8.18	211	38.77
25	C22D2o	-	-	-
26	T2At	0.40	122	3.28
27	Q7Ao	-	-	-
28	N116Dt	129.85	1294	100.35
29	N2Dod	-	-	-
30	Q4At	1.02	160	6.38
31	Q8Atd	4.72	379	12.45
32	Q4A1t	1.62	254	6.38
33	C4D1to	1.41	237	5.95
34	Q4a2t	0.58	114	5.09
35	Q10At	9.37	189	49.58
36	O3At	0.17	124	1.37
37	N10Dto	3.44	248	13.87
38	N10D2to	3.14	239	13.14
39	N10Ato	3.13	239	13.10
40	N1A4d	-	-	-
41	Q7Aat	3.10	258	12.02
42	Q3At	0.99	124	7.98
43	O15ata	0.33	148	2.23
44	Q11atd	4.86	278	17.48
45	O5At	0.32	147	2.18
46	N27Aaod	-	-	-
47	N27A2t	14.86	381	39.00
48	N27A3o	-	-	-

Figure 1.8
SPICE3 with bypass using the gcc compiler, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
49	N27A4o	-	-	-
50	N27A5o	17.10	429	39.86
51	N27A6aod	-	-	-
52	N12At	2.37	220	10.77
53	N8Ao	-	-	-
54	N2Ao	-	-	-
55	O6At	0.25	124	2.02
56	N1A5d	-	-	-
57	N6At	3.25	424	7.67
58	Q11Atad	6.49	440	14.75
59	Q5Ao	-	-	-
60	Q2Dtd	1.09	315	3.46
61	O66At	-	-	-
62	N2Dtdo	0.57	156	3.65
63	Q8Dtd	6.20	339	18.29
64	Q4A3t	2.18	333	6.55
65	Q50At	135.73	2167	62.63
66	O5A1t	0.19	148	1.28
67	C38Da	-	-	-
68	C38D2a	-	-	-
69	O6A1t	0.21	124	1.69
70	O3Ap	-	-	-
71	O7Ap	-	-	-
72	T1Atad	0.16	132	1.21
73	T2A1t	1.26	500	2.52
74	T1A1t	0.47	324	1.45
75	t1A2t	0.26	204	1.27
76	T3At	0.39	116	3.36
77	T3A2t	0.41	116	3.53
78	Q5Dtd	3.63	434	8.36
79	Q5D1td	3.92	457	8.58
80	Q7Dtd	4.63	454	10.20
81	Q6Dtd	4.09	438	9.34
82	Q5D2td	4.41	504	8.75
83	Q4A5ta	39.67	1620	24.49
84	Q15atad	3.74	173	21.62
85	Q22Atad	6.25	185	33.78
86	Q22A2tad	5.70	188	30.32
87	Q11Ata	3.18	186	17.10
88	Q11Ao	-	-	-
89	Q22A3tad	7.06	250	28.24
90	Q22A4tad	9.13	235	38.85
91	Q22A5tad	5.34	187	28.56
92	O3A1t	0.10	114	0.88
93	N9At	171.02	12783	13.38
94	O38Aa	-	-	-
95	C18At	11.21	474	23.65
96	C18A1t	7.62	464	16.42
97	Q18A2t	8.23	496	16.59

Figure 1.8
SPICE3 with bypass using the gcc compiler, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
98	N4Ada	-	-	-
99	C14Dt	-	-	-
100	N804Dt	-	-	-
101	T1At	0.20	138	1.45
102	C19Mt	32.88	838	39.24
103	C68Dt	560.70	4493	124.79
104	C9Ao	-	-	-
105	C82Dt	-	-	-
106	C2At	0.95	147	6.46
107	C37Dt	72.83	1166	62.46
108	N27At	9.30	264	35.23
109	N698Dt	1635.79	3409	479.84
110	Q6At	405.46	58489	6.93
111	C7Atd	2.42	160	15.13
112	C52Aa	-	-	-
113	Q340t	2562.25	2168	1181.85
114	C54Dt	91.21	862	105.81
115	N1190Mt	-	-	-
116	C31Dt	87.29	1233	70.79
117	Q2A1t	18.44	4620	3.99
118	C119At	-	-	-
119	C6Dt	3.16	247	12.79
120	Q2A2t	7.80	2393	3.26
121	Q6A1t	13.83	1734	7.98
122	Q4A4ta	-	-	-
123	O4Ao	-	-	-
124	H44Aa	-	-	-
125	Q10Ao	-	-	-
126	C77Mt	-	-	-
127	Q4Af	-	-	-
128	N2Aa	-	-	-
129	N1Ad	-	-	-
130	O5A2t	0.16	126	1.27
131	O2At	0.17	228	0.75
132	O2A2t	0.07	114	0.61
133	C205At	937.92	6926	135.42
134	T2A2t	0.54	122	4.43
135	C26At	12.70	240	52.92
136	N1At	0.22	114	1.93
137	C37At	103.20	1242	83.09
138	N3At	3.27	585	5.59
139	C6D1t	1.18	228	5.18
140	Q86Aa	-	-	-
141	C640Dt	1655.40	1599	1035.27
142	C1060Mt	608.43	713	853.34
143	Q14Ao	-	-	-
144	C28Dt	53.10	1764	30.10
145	C23Dt	11.27	465	24.24
146	O20At	0.72	227	3.17

Figure 1.8
SPICE3 with bypass using the gcc compiler, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
147	C277Mt	637.52	2784	228.99
148	C277M2t	21.22	88	241.14
149	C42Dt	109.49	1242	88.16
150	C7Ad	-	-	-
151	C14D1t	40.11	1661	24.15
152	Q84At	1252.94	3543	353.64
153	Q50A1t	132.55	2167	61.17
154	O20A1t	3.68	936	3.93
105	total	11904.96	146400	
	average	113.38	1394	81.32

Figure 1.9
SPICE3 with bypass using the gcc compiler, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
1	Q180Do	4.20	1.91	2.04	1.17
2	Q180D2o	4.25	2.01	1.91	1.15
3	Q2At	1.56	0.01	0.36	0.17
4	O9Aa	0.00	0.00	0.00	0.00
5	O1024Ao	0.02	0.00	0.00	0.00
6	N48Dt	116.24	0.06	4.38	3.14
7	N5At	1.06	0.01	0.05	0.05
8	N5A2t	1.02	0.00	0.06	0.05
9	O10At	0.32	0.00	0.09	0.09
10	Q6Ao	0.02	0.00	0.00	0.00
11	Q6A2o	-	-	-	-
12	Q4Ao	0.00	0.01	0.01	0.00
13	N1Aot	0.09	0.02	0.02	0.01
14	N1A2ot	0.09	0.00	0.00	0.01
15	N1A3ot	0.07	0.00	0.03	0.02
16	O8At	0.19	0.00	0.02	0.03
17	Q1Ado	0.03	0.00	0.02	0.00
18	Q1A2t	0.25	0.01	0.07	0.02
19	Q5Atd	1.19	0.00	0.17	0.11
20	C25Ao	1.91	0.02	0.22	0.14
21	C27Ao	1.89	0.06	0.24	0.11
22	C7Ao	0.76	0.00	0.03	0.04
23	C4Dto	1.97	0.00	0.09	0.08
24	C22Dt	5.94	0.10	0.72	0.49
25	C22D2o	0.22	0.08	0.04	0.04
26	T2At	0.03	0.01	0.07	0.06
27	Q7Ao	0.06	0.01	0.00	0.01
28	N116Dt	90.38	0.26	6.40	4.77
29	N2Dod	0.31	0.00	0.02	0.02
30	Q4At	0.60	0.01	0.09	0.04
31	Q8Atd	3.12	0.04	0.98	0.83
32	Q4A1t	0.80	0.02	0.15	0.15
33	C4D1to	1.06	0.01	0.04	0.04
34	Q4a2t	0.29	0.00	0.02	0.03
35	Q10At	3.41	0.41	2.17	1.22
36	O3At	0.04	0.00	0.01	0.01
37	N10Dto	2.97	0.01	0.08	0.08
38	N10D2to	2.73	0.00	0.08	0.05
39	N10Ato	2.62	0.00	0.18	0.12
40	N1A4d	0.04	0.00	0.01	0.00
41	Q7Aat	2.61	0.03	0.36	0.19
42	Q3At	0.43	0.03	0.19	0.04
43	O15ata	0.05	0.00	0.01	0.04
44	Q11atd	3.77	0.07	0.99	0.80
45	O5At	0.16	0.00	0.02	0.01
46	N27Aaod	4.82	0.03	0.29	0.25
47	N27A2t	15.36	0.02	0.69	0.35
48	N27A3o	2.21	0.04	0.21	0.14

Figure 1.9
SPICE3 with bypass using the gcc compiler, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
49	N27A4o	2.31	0.03	0.15	0.10
50	N27A5o	15.08	0.05	0.52	0.48
51	N27A6aod	2.93	0.01	0.23	0.26
52	N12At	1.71	0.00	0.10	0.03
53	N8Ao	0.12	0.02	0.01	0.00
54	N2Ao	0.02	0.00	0.01	0.00
55	O6At	0.06	0.00	0.01	0.05
56	N1A5d	0.02	0.01	0.00	0.01
57	N6At	2.23	0.01	0.16	0.10
58	Q11Atad	5.38	0.04	0.85	0.72
59	Q5Ao	0.03	0.01	0.01	0.00
60	Q2Dtd	0.82	0.00	0.20	0.13
61	O66At	-	-	-	-
62	N2Dtdo	0.64	0.00	0.04	0.09
63	Q8Dtd	4.69	0.06	1.52	0.93
64	Q4A3t	1.17	0.00	0.21	0.15
65	Q50At	79.80	0.34	19.23	12.26
66	O5A1t	0.03	0.00	0.01	0.00
67	C38Da	7.23	0.07	0.86	0.63
68	C38D2a	2.66	0.16	0.77	0.20
69	O6A1t	0.01	0.00	0.02	0.01
70	O3Ap	0.00	0.00	0.00	0.00
71	O7Ap	0.00	0.00	0.00	0.00
72	T1Atad	0.05	0.02	0.05	0.01
73	T2A1t	0.15	0.01	0.19	0.14
74	T1A1t	0.05	0.01	0.03	0.06
75	t1A2t	0.03	0.01	0.01	0.03
76	T3At	0.05	0.02	0.10	0.00
77	T3A2t	0.04	0.04	0.06	0.06
78	Q5Dtd	2.85	0.02	0.73	0.39
79	Q5D1td	3.16	0.02	0.67	0.50
80	Q7Dtd	3.54	0.05	1.11	0.62
81	Q6Dtd	3.25	0.03	0.76	0.46
82	Q5D2td	3.22	0.04	0.75	0.41
83	Q4A5ta	8.12	0.32	20.99	5.95
84	Q15atad	3.56	0.12	1.32	0.55
85	Q22Atad	7.04	0.15	1.33	1.16
86	Q22A2tad	5.58	0.16	1.47	0.98
87	Q11Ata	1.80	0.07	0.32	0.30
88	Q11Ao	0.00	0.02	0.00	0.03
89	Q22A3tad	6.35	0.12	1.40	0.86
90	Q22A4tad	5.58	0.24	1.78	1.24
91	Q22A5tad	5.30	0.13	1.33	0.84
92	O3A1t	0.02	0.00	0.00	0.00
93	N9At	131.77	0.02	10.61	8.44
94	O38Aa	0.00	0.02	0.00	0.00
95	C18At	5.72	0.10	2.42	0.96
96	C18A1t	4.55	0.10	1.58	0.41
97	Q18A2t	4.89	0.09	1.62	0.45

Figure 1.9
SPICE3 with bypass using the gcc compiler, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
98	N4Ada	0.19	0.00	0.02	0.01
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	0.01	0.00	0.00	0.01
102	C19Mt	24.66	0.10	2.06	1.58
103	C68Dt	411.38	0.69	60.22	35.56
104	C9Ao	0.13	0.01	0.00	0.01
105	C82Dt	-	-	-	-
106	C2At	0.64	0.00	0.02	0.02
107	C37Dt	62.15	0.05	1.70	1.77
108	N27At	7.48	0.03	0.29	0.19
109	N698Dt	1019.73	3.78	153.60	83.43
110	Q6At	299.56	0.02	27.52	22.71
111	C7Atd	2.65	0.01	0.10	0.07
112	C52Aa	41.80	1.86	24.01	5.39
113	Q340t	866.72	68.27	1286.07	233.35
114	C54Dt	37.97	1.45	29.76	11.14
115	N1190Mt	-	-	-	-
116	C31Dt	71.34	0.17	6.65	4.49
117	Q2A1t	9.51	0.00	2.85	1.87
118	C119At	-	-	-	-
119	C6Dt	2.77	0.01	0.02	0.07
120	Q2A2t	5.16	0.01	0.41	0.39
121	Q6A1t	10.88	0.00	0.63	0.48
122	Q4A4ta	-	-	-	-
123	O4Ao	0.00	0.00	0.00	0.00
124	H44Aa	-	-	-	-
125	Q10Ao	0.09	0.06	0.00	0.00
126	C77Mt	-	-	-	-
127	Q4Af	0.02	0.00	0.00	0.01
128	N2Aa	0.02	0.00	0.00	0.00
129	N1Ad	0.07	0.00	0.02	0.00
130	O5A2t	0.06	0.00	0.01	0.01
131	O2At	0.03	0.00	0.01	0.01
132	O2A2t	0.02	0.00	0.01	0.00
133	C205At	696.92	0.52	81.09	43.92
134	T2A2t	0.10	0.01	0.09	0.06
135	C26At	7.57	0.24	1.94	0.81
136	N1At	0.07	0.01	0.00	0.01
137	C37At	85.15	0.24	7.50	2.73
138	N3At	2.59	0.00	0.12	0.16
139	C6D1t	0.79	0.00	0.04	0.06
140	Q86Aa	0.43	0.97	0.25	0.15
141	C640Dt	996.97	16.42	464.63	52.76
142	C1060Mt	488.01	8.11	72.30	21.95
143	Q14Ao	0.15	0.05	0.03	0.02
144	C28Dt	37.16	0.02	1.74	1.50
145	C23Dt	9.28	0.02	0.21	0.25
146	O20At	0.16	0.01	0.06	0.05

Figure 1.9
SPICE3 with bypass using the gcc compiler, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
147	C277Mt	454.16	0.56	35.59	21.00
148	C277M2t	17.31	1.81	1.07	0.64
149	C42Dt	151.38	0.38	20.27	13.37
150	C7Ad	1.36	0.01	0.20	0.16
151	C14D1t	32.79	0.01	1.04	1.07
152	Q84At	447.87	13.93	324.44	160.63
153	Q50A1t	75.99	0.31	18.82	12.51
154	O20A1t	1.34	0.02	0.51	0.29
144	total	6997.36	128.21	2727.09	793.84
	average	48.59	0.89	18.94	5.51

1.3.4. SPICE3 with bypass using the vcc compiler

Figure 1.10
SPICE3 with bypass using the vcc compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
1	Q180Do	10.12	53	190.94
2	Q180D2o	10.26	53	193.58
3	Q2At	3.03	800	3.79
4	O9Aa	0.08	3	26.67
5	O1024Ao	0.07	3	23.33
6	N48Dt	139.50	2586	53.94
7	N5At	1.66	205	8.10
8	N5A2t	1.52	195	7.79
9	O10At	0.96	456	2.11
10	Q6Ao	0.10	13	7.69
11	Q6A2o	-	-	-
12	Q4Ao	0.05	7	7.14
13	N1Aot	0.30	124	2.42
14	N1A2ot	0.33	124	2.66
15	N1A3ot	0.34	124	2.74
16	O8At	0.42	166	2.53
17	Q1Ado	0.14	66	2.12
18	Q1A2t	0.54	193	2.80
19	Q5Atd	2.25	424	5.31
20	C25Ao	2.36	155	15.23
21	C27Ao	2.58	141	18.30
22	C7Ao	0.82	138	5.94
23	C4Dto	2.74	498	5.50
24	C22Dt	8.98	226	39.73
25	C22D2o	0.50	14	35.71
26	T2At	0.41	125	3.28
27	Q7Ao	0.09	13	6.92
28	N116Dt	131.14	1328	98.75
29	N2Dod	0.49	216	2.27
30	Q4At	1.04	168	6.19
31	Q8Atd	7.39	600	12.32
32	Q4A1t	1.75	262	6.68
33	C4D1to	1.57	259	6.06
34	Q4a2t	0.68	123	5.53
35	Q10At	10.12	201	50.35
36	O3At	0.19	127	1.50
37	N10Dto	3.83	282	13.58
38	N10D2to	3.55	273	13.00
39	N10Ato	3.53	273	12.93
40	N1A4d	0.08	59	1.36
41	Q7Aat	4.85	340	14.26
42	Q3At	1.22	142	8.59
43	O15ata	0.78	154	5.06
44	Q11atd	8.29	507	16.35
45	O5At	0.26	151	1.72
46	N27Aaod	7.11	317	22.43

Figure 1.10
SPICE3 with bypass using the vcc compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
47	N27A2t	19.18	527	36.39
48	N27A3o	2.77	147	18.84
49	N27A4o	2.86	147	19.46
50	N27A5o	19.59	500	39.18
51	N27A6aod	5.04	275	18.33
52	N12At	2.46	240	10.25
53	N8Ao	0.15	8	18.75
54	N2Ao	0.04	9	4.44
55	O6At	0.23	127	1.81
56	N1A5d	0.11	41	2.68
57	N6At	3.47	427	8.13
58	Q11Atad	10.50	667	15.74
59	Q5Ao	0.05	15	3.33
60	Q2Dtd	1.83	538	3.40
61	O66At	-	-	-
62	N2Dtdo	1.22	405	3.01
63	Q8Dtd	10.25	614	16.69
64	Q4A3t	2.37	341	6.95
65	Q50At	140.95	2208	63.84
66	O5A1t	0.21	151	1.39
67	C38Da	9.13	453	20.15
68	C38D2a	4.16	167	24.91
69	O6A1t	0.20	127	1.57
70	O3Ap	0.01	6	1.67
71	O7Ap	0.04	6	6.67
72	T1Atad	0.67	219	3.06
73	T2A1t	1.31	503	2.60
74	T1A1t	0.48	324	1.48
75	t1A2t	0.26	204	1.27
76	T3At	1.32	122	10.82
77	T3A2t	1.32	122	10.82
78	Q5Dtd	5.93	733	8.09
79	Q5D1td	6.06	762	7.95
80	Q7Dtd	7.43	743	10.00
81	Q6Dtd	6.81	743	9.17
82	Q5D2td	6.51	745	8.74
83	Q4A5ta	45.31	1630	27.80
84	Q15atad	10.48	412	25.44
85	Q22Atad	16.76	430	38.98
86	Q22A2tad	15.22	431	35.31
87	Q11Ata	5.04	202	24.95
88	Q11Ao	0.10	8	12.50
89	Q22A3tad	13.30	489	27.20
90	Q22A4tad	15.40	351	43.87
91	Q22A5tad	13.76	429	32.07
92	O3A1t	0.16	117	1.37
93	N9At	178.23	12798	13.93
94	O38Aa	0.38	3	126.67
95	C18At	11.24	492	22.85

Figure 1.10
SPICE3 with bypass using the vcc compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
96	C18A1t	8.54	517	16.52
97	Q18A2t	8.98	549	16.36
98	N4Ada	0.86	41	20.98
99	C14Dt	-	-	-
100	N804Dt	-	-	-
101	T1At	0.23	141	1.63
102	C19Mt	34.67	846	40.98
103	C68Dt	588.64	4501	130.78
104	C9Ao	0.21	9	23.33
105	C82Dt	-	-	-
106	C2At	0.96	155	6.19
107	C37Dt	76.33	1176	64.91
108	N27At	10.15	281	36.12
109	N698Dt	1623.54	3446	471.14
110	Q6At	430.55	58500	7.36
111	C7Atd	3.41	250	13.64
112	C52Aa	-	-	-
113	Q340t	2805.02	2300	1219.57
114	C54Dt	92.55	867	106.75
115	N1190Mt	-	-	-
116	C31Dt	89.31	1292	69.13
117	Q2A1t	20.19	4620	4.37
118	C119At	-	-	-
119	C6Dt	3.28	254	12.91
120	Q2A2t	8.55	2401	3.56
121	Q6A1t	14.63	1743	8.39
122	Q4A4ta	-	-	-
123	O4Ao	0.00	3	0.00
124	H44Aa	-	-	-
125	Q10Ao	0.24	12	20.00
126	C77Mt	-	-	-
127	Q4Af	0.04	9	4.44
128	N2Aa	0.38	6	63.33
129	N1Ad	0.22	111	1.98
130	O5A2t	0.17	129	1.32
131	O2At	0.15	231	0.65
132	O2A2t	0.07	118	0.59
133	C205At	914.09	6940	131.71
134	T2A2t	-	-	-
135	C26At	13.33	257	51.87
136	N1At	0.25	117	2.14
137	C37At	106.19	1254	84.68
138	N3At	3.50	595	5.88
139	C6D1t	1.27	248	5.12
140	Q86Aa	9.83	9	1092.22
141	C640Dt	1707.58	1611	1059.95
142	C1060Mt	682.89	788	866.61
143	Q14Ao	0.32	14	22.86
144	C28Dt	55.98	1780	31.45

Figure 1.10
SPICE3 with bypass using the vcc compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Total CPU per iteration (msec)
145	C23Dt	11.90	472	25.21
146	O20At	0.72	227	3.17
147	C277Mt	626.44	2784	225.01
148	C277M2t	22.69	88	257.84
149	C42Dt	-	-	-
150	C7Ad	2.48	250	9.92
151	C14D1t	39.92	1614	24.73
152	Q84At	1277.82	3575	357.43
153	Q50A1t	146.43	2208	66.32
154	O20A1t	3.79	939	4.04
141	total	12427.61	154123	
	average	88.14	1093	80.63

Figure 1.11
SPICE3 with bypass using the vcc compiler, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
1	Q180Do	-	-	-
2	Q180D2o	-	-	-
3	Q2At	3.00	790	3.80
4	O9Aa	-	-	-
5	O1024Ao	-	-	-
6	N48Dt	138.78	2568	54.04
7	N5At	1.50	179	8.38
8	N5A2t	1.36	169	8.05
9	O10At	0.95	453	2.10
10	Q6Ao	-	-	-
11	Q6A2o	-	-	-
12	Q4Ao	-	-	-
13	N1Aot	0.28	118	2.37
14	N1A2ot	0.31	118	2.63
15	N1A3ot	0.30	118	2.54
16	O8At	0.41	166	2.47
17	Q1Ado	-	-	-
18	Q1A2t	0.51	184	2.77
19	Q5Atd	1.39	195	7.13
20	C25Ao	-	-	-
21	C27Ao	-	-	-
22	C7Ao	-	-	-
23	C4Dto	2.62	468	5.60
24	C22Dt	8.44	211	40.00
25	C22D2o	-	-	-
26	T2At	0.40	122	3.28
27	Q7Ao	-	-	-
28	N116Dt	128.99	1294	99.68
29	N2Dod	-	-	-
30	Q4At	0.99	160	6.19
31	Q8Atd	5.00	379	13.19
32	Q4A1t	1.69	254	6.65
33	C4D1to	1.48	237	6.24
34	Q4a2t	0.65	114	5.70
35	Q10At	9.42	189	49.84
36	O3At	0.17	124	1.37
37	N10Dto	3.44	248	13.87
38	N10D2to	3.16	239	13.22
39	N10Ato	3.19	239	13.35
40	N1A4d	-	-	-
41	Q7Aat	3.13	258	12.13
42	Q3At	1.10	124	8.87
43	O15ata	0.36	148	2.43
44	Q11atd	5.03	278	18.09
45	O5At	0.26	147	1.77
46	N27Aaod	-	-	-
47	N27A2t	15.42	381	40.47
48	N27A3o	-	-	-

Figure 1.11
SPICE3 with bypass using the vcc compiler, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
49	N27A4o	-	-	-
50	N27A5o	18.11	429	42.21
51	N27A6aod	-	-	-
52	N12At	2.32	220	10.55
53	N8Ao	-	-	-
54	N2Ao	-	-	-
55	O6At	0.22	124	1.77
56	N1A5d	-	-	-
57	N6At	3.42	424	8.07
58	Q11Atad	6.50	440	14.77
59	Q5Ao	-	-	-
60	Q2Dtd	1.17	315	3.71
61	O66At	-	-	-
62	N2Dtdo	0.52	156	3.33
63	Q8Dtd	6.49	339	19.14
64	Q4A3t	2.30	333	6.91
65	Q50At	139.30	2167	64.28
66	O5A1t	0.19	148	1.28
67	C38Da	-	-	-
68	C38D2a	-	-	-
69	O6A1t	0.19	124	1.53
70	O3Ap	-	-	-
71	O7Ap	-	-	-
72	T1Atad	0.19	132	1.44
73	T2A1t	1.30	500	2.60
74	T1A1t	0.48	324	1.48
75	t1A2t	0.26	204	1.27
76	T3At	0.39	116	3.36
77	T3A2t	0.41	116	3.53
78	Q5Dtd	3.90	434	8.99
79	Q5D1td	3.98	457	8.71
80	Q7Dtd	4.94	454	10.88
81	Q6Dtd	4.43	438	10.11
82	Q5D2td	4.68	504	9.29
83	Q4A5ta	41.99	1620	25.92
84	Q15atad	3.93	173	22.72
85	Q22Atad	6.75	185	36.49
86	Q22A2tad	6.17	188	32.82
87	Q11Ata	3.33	186	17.90
88	Q11Ao	-	-	-
89	Q22A3tad	7.49	250	29.96
90	Q22A4tad	9.88	235	42.04
91	Q22A5tad	5.67	187	30.32
92	O3A1t	0.14	114	1.23
93	N9At	178.04	12783	13.93
94	O38Aa	-	-	-
95	C18At	10.86	474	22.91
96	C18A1t	7.90	464	17.03
97	Q18A2t	8.33	496	16.79

Figure 1.11
SPICE3 with bypass using the vcc compiler, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
98	N4Ada	-	-	-
99	C14Dt	-	-	-
100	N804Dt	-	-	-
101	T1At	0.23	138	1.67
102	C19Mt	34.29	838	40.92
103	C68Dt	587.08	4493	130.67
104	C9Ao	-	-	-
105	C82Dt	-	-	-
106	C2At	0.92	147	6.26
107	C37Dt	75.78	1166	64.99
108	N27At	9.63	264	36.48
109	N698Dt	1610.75	3409	472.50
110	Q6At	430.47	58489	7.36
111	C7Atd	2.49	160	15.56
112	C52Aa	-	-	-
113	Q340t	2633.67	2168	1214.79
114	C54Dt	90.93	862	105.49
115	N1190Mt	-	-	-
116	C31Dt	86.07	1233	69.81
117	Q2A1t	20.19	4620	4.37
118	C119At	-	-	-
119	C6Dt	3.16	247	12.79
120	Q2A2t	8.50	2393	3.55
121	Q6A1t	14.58	1734	8.41
122	Q4A4ta	-	-	-
123	O4Ao	-	-	-
124	H44Aa	-	-	-
125	Q10Ao	-	-	-
126	C77Mt	-	-	-
127	Q4Af	-	-	-
128	N2Aa	-	-	-
129	N1Ad	-	-	-
130	O5A2t	0.17	126	1.35
131	O2At	0.14	228	0.61
132	O2A2t	0.07	114	0.61
133	C205At	912.26	6926	131.72
134	T2A2t	-	-	-
135	C26At	12.50	240	52.08
136	N1At	0.23	114	2.02
137	C37At	105.32	1242	84.80
138	N3At	3.43	585	5.86
139	C6D1t	1.19	228	5.22
140	Q86Aa	-	-	-
141	C640Dt	1689.05	1599	1056.32
142	C1060Mt	635.61	713	891.46
143	Q14Ao	-	-	-
144	C28Dt	55.67	1765	31.54
145	C23Dt	11.75	465	25.27
146	O20At	0.72	227	3.17

Figure 1.11
SPICE3 with bypass using the vcc compiler, part 2

Circuit number	Circuit name	Transient CPU time	Transient iterations	Transient CPU per iteration (msec)
147	C277Mt	625.81	2784	224.79
148	C277M2t	22.01	88	250.11
149	C42Dt	-	-	-
150	C7Ad	-	-	-
151	C14D1t	39.89	1614	24.71
152	Q84At	1261.22	3543	355.98
153	Q50A1t	144.70	2167	66.77
154	O20A1t	3.75	936	4.01
103	total	11974.13	144990	
	average	116.25	1407	82.59

Figure 1.12
SPICE3 with bypass using the vcc compiler, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
1	Q180Do	4.28	1.93	1.95	1.22
2	Q180D2o	4.42	2.00	1.91	1.19
3	Q2At	1.80	0.00	0.29	0.26
4	O9Aa	0.01	0.00	0.00	0.00
5	O1024Ao	0.01	0.00	0.00	0.00
6	N48Dt	120.41	0.04	4.80	3.40
7	N5At	1.27	0.00	0.05	0.02
8	N5A2t	1.04	0.00	0.05	0.06
9	O10At	0.25	0.01	0.07	0.10
10	Q6Ao	0.05	0.01	0.00	0.00
11	Q6A2o	-	-	-	-
12	Q4Ao	0.01	0.00	0.00	0.01
13	N1Aot	0.13	0.00	0.02	0.02
14	N1A2ot	0.09	0.00	0.00	0.03
15	N1A3ot	0.11	0.00	0.01	0.03
16	O8At	0.19	0.00	0.03	0.01
17	Q1Ado	0.07	0.00	0.01	0.02
18	Q1A2t	0.31	0.00	0.02	0.02
19	Q5Atd	1.29	0.02	0.12	0.11
20	C25Ao	1.99	0.04	0.14	0.13
21	C27Ao	1.98	0.06	0.20	0.22
22	C7Ao	0.67	0.02	0.06	0.03
23	C4Dto	2.00	0.00	0.08	0.10
24	C22Dt	6.19	0.12	0.62	0.48
25	C22D2o	0.26	0.09	0.03	0.04
26	T2At	0.04	0.01	0.06	0.04
27	Q7Ao	0.06	0.00	0.00	0.00
28	N116Dt	88.86	0.23	5.92	4.63
29	N2Dod	0.26	0.00	0.02	0.02
30	Q4At	0.55	0.01	0.14	0.06
31	Q8Atd	3.48	0.06	1.14	0.63
32	Q4A1t	0.96	0.02	0.10	0.07
33	C4D1to	1.07	0.03	0.03	0.04
34	Q4a2t	0.38	0.02	0.03	0.06
35	Q10At	3.42	0.41	2.25	1.16
36	O3At	0.06	0.01	0.01	0.00
37	N10Dto	3.00	0.02	0.16	0.09
38	N10D2to	2.79	0.03	0.09	0.08
39	N10Ato	2.67	0.02	0.15	0.13
40	N1A4d	0.00	0.00	0.00	0.01
41	Q7Aat	2.67	0.03	0.30	0.14
42	Q3At	0.54	0.06	0.10	0.07
43	O15ata	0.08	0.00	0.05	0.02
44	Q11atd	3.89	0.07	1.00	0.70
45	O5At	0.18	0.00	0.03	0.03
46	N27Aaod	4.87	0.04	0.46	0.29
47	N27A2t	15.83	0.02	0.71	0.51
48	N27A3o	2.34	0.02	0.15	0.13

Figure 1.12
SPICE3 with bypass using the vcc compiler, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
49	N27A4o	2.51	0.01	0.16	0.06
50	N27A5o	15.81	0.03	0.80	0.50
51	N27A6aod	2.89	0.03	0.26	0.33
52	N12At	1.47	0.00	0.11	0.03
53	N8Ao	0.11	0.01	0.00	0.00
54	N2Ao	0.01	0.01	0.00	0.00
55	O6At	0.07	0.00	0.01	0.00
56	N1A5d	0.05	0.00	0.00	0.01
57	N6At	2.40	0.00	0.11	0.17
58	Q11Atad	5.29	0.06	0.94	0.58
59	Q5Ao	0.04	0.00	0.01	0.00
60	Q2Dtd	0.72	0.00	0.19	0.12
61	O66At	-	-	-	-
62	N2Dtdo	0.74	0.01	0.03	0.05
63	Q8Dtd	5.23	0.07	1.09	0.99
64	Q4A3t	1.39	0.03	0.20	0.15
65	Q50At	83.23	0.30	18.28	12.46
66	O5A1t	0.04	0.00	0.01	0.02
67	C38Da	7.03	0.09	1.10	0.78
68	C38D2a	2.87	0.18	0.67	0.32
69	O6A1t	0.06	0.00	0.02	0.02
70	O3Ap	0.00	0.00	0.00	0.00
71	O7Ap	0.01	0.00	0.00	0.00
72	T1Atad	0.01	0.00	0.03	0.02
73	T2A1t	0.20	0.00	0.16	0.10
74	T1A1t	0.02	0.00	0.06	0.06
75	t1A2t	0.04	0.00	0.01	0.01
76	T3At	0.06	0.02	0.04	0.08
77	T3A2t	0.02	0.03	0.07	0.08
78	Q5Dtd	3.08	0.05	0.71	0.49
79	Q5D1td	3.27	0.03	0.56	0.54
80	Q7Dtd	4.10	0.03	0.94	0.61
81	Q6Dtd	3.68	0.02	0.82	0.53
82	Q5D2td	3.51	0.05	0.67	0.61
83	Q4A5ta	8.75	0.33	22.58	5.96
84	Q15atad	3.86	0.14	1.17	0.68
85	Q22Atad	7.55	0.16	1.61	0.90
86	Q22A2tad	6.13	0.17	1.54	0.90
87	Q11Ata	1.97	0.03	0.36	0.17
88	Q11Ao	0.04	0.02	0.00	0.00
89	Q22A3tad	6.66	0.14	1.44	0.87
90	Q22A4tad	5.86	0.25	1.75	1.64
91	Q22A5tad	5.71	0.13	1.18	0.86
92	O3A1t	0.05	0.00	0.00	0.01
93	N9At	138.81	0.03	10.49	7.84
94	O38Aa	0.01	0.01	0.00	0.00
95	C18At	5.26	0.11	2.34	1.02
96	C18A1t	4.83	0.09	1.43	0.47
97	Q18A2t	4.79	0.09	1.66	0.62

Figure 1.12
SPICE3 with bypass using the vcc compiler, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
98	N4Ada	0.22	0.00	0.00	0.01
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	0.03	0.01	0.02	0.03
102	C19Mt	25.63	0.10	2.02	1.83
103	C68Dt	434.69	0.68	60.05	37.25
104	C9Ao	0.14	0.01	0.00	0.00
105	C82Dt	-	-	-	-
106	C2At	0.60	0.00	0.04	0.07
107	C37Dt	64.51	0.08	1.61	2.15
108	N27At	7.67	0.02	0.25	0.32
109	N698Dt	977.86	3.88	151.70	84.96
110	Q6At	322.53	0.01	27.28	23.28
111	C7Atd	2.78	0.00	0.06	0.07
112	C52Aa	-	-	-	-
113	Q340t	932.90	67.63	1271.89	248.71
114	C54Dt	38.11	1.41	28.72	11.05
115	N1190Mt	-	-	-	-
116	C31Dt	69.86	0.17	6.16	4.66
117	Q2A1t	10.87	0.01	3.10	2.10
118	C119At	-	-	-	-
119	C6Dt	2.75	0.01	0.06	0.05
120	Q2A2t	6.02	0.01	0.51	0.42
121	Q6A1t	11.68	0.00	0.51	0.38
122	Q4A4ta	-	-	-	-
123	O4Ao	0.00	0.00	0.00	0.00
124	H44Aa	-	-	-	-
125	Q10Ao	0.03	0.06	0.06	0.02
126	C77Mt	-	-	-	-
127	Q4Af	0.01	0.01	0.00	0.00
128	N2Aa	0.02	0.00	0.00	0.00
129	N1Ad	0.11	0.00	0.01	0.00
130	O5A2t	0.05	0.00	0.01	0.02
131	O2At	0.02	0.00	0.01	0.00
132	O2A2t	0.02	0.00	0.00	0.00
133	C205At	665.74	0.50	79.25	44.74
134	T2A2t	-	-	-	-
135	C26At	7.35	0.23	1.82	0.81
136	N1At	0.10	0.00	0.00	0.01
137	C37At	87.20	0.25	7.22	2.57
138	N3At	2.66	0.02	0.10	0.17
139	C6D1t	0.80	0.00	0.05	0.02
140	Q86Aa	0.39	1.02	0.25	0.16
141	C640Dt	1046.15	15.61	448.82	52.41
142	C1060Mt	517.52	8.02	69.53	22.23
143	Q14Ao	0.13	0.05	0.03	0.02
144	C28Dt	39.55	0.03	1.61	1.54
145	C23Dt	9.63	0.02	0.26	0.28
146	O20At	0.13	0.01	0.07	0.04

Figure 1.12
SPICE3 with bypass using the vcc compiler, part 3

Circuit number	Circuit name	Total load time	Total reorder time	Total LU decomposition time	Total solve time
147	C277Mt	436.42	0.52	35.26	22.02
148	C277M2t	17.93	1.90	1.10	0.70
149	C42Dt	-	-	-	-
150	C7Ad	1.31	0.01	0.18	0.19
151	C14D1t	32.95	0.02	1.13	0.87
152	Q84At	465.65	14.10	315.03	162.71
153	Q50A1t	88.00	0.31	18.29	12.59
154	O20A1t	1.65	0.02	0.51	0.39
141	total	6967.44	124.95	2633.55	799.92
	average	49.41	0.89	18.68	5.67

1.3.5. SPICE2 with bypass

Figure 1.13
SPICE2 with bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
1	Q180Do	22.47	53	0	423.96
2	Q180D2o	22.53	53	0	425.09
3	Q2At	4.62	948	938	4.87
4	O9Aa	0.30	2	0	150.00
5	O1024Ao	-	-	-	-
6	N48Dt	134.22	992	978	135.30
7	N5At	2.98	160	140	18.63
8	N5A2t	3.00	162	142	18.52
9	O10At	-	-	-	-
10	Q6Ao	0.30	13	0	23.08
11	Q6A2o	0.88	147	0	5.99
12	Q4Ao	0.33	7	0	47.14
13	N1Aot	1.22	142	134	8.59
14	N1A2ot	1.68	228	220	7.37
15	N1A3ot	1.27	182	174	6.98
16	O8At	0.93	220	220	4.23
17	Q1Ado	0.37	70	0	5.29
18	Q1A2t	1.18	360	351	3.28
19	Q5Atd	3.08	419	193	7.35
20	C25Ao	1.93	34	0	56.76
21	C27Ao	2.73	43	0	63.49
22	C7Ao	0.98	44	0	22.27
23	C4Dto	5.30	421	403	12.59
24	C22Dt	16.83	208	180	80.91
25	C22D2o	2.07	16	0	129.38
26	T2At	1.75	386	384	4.53
27	Q7Ao	0.40	13	0	30.77
28	N116Dt	295.80	1565	1497	189.01
29	N2Dod	1.48	231	0	6.41
30	Q4At	1.73	166	158	10.42
31	Q8Atd	7.12	605	375	11.77
32	Q4A1t	2.37	258	250	9.19
33	C4D1to	4.18	305	275	13.70
34	Q4a2t	1.12	123	114	9.11
35	Q10At	14.48	199	187	72.76
36	O3At	0.25	126	124	1.98
37	N10Dto	9.87	291	249	33.92
38	N10D2to	9.28	285	243	32.56
39	N10Ato	8.73	259	217	33.71
40	N1A4d	0.22	61	0	3.61
41	Q7Aat	6.57	337	255	19.50
42	Q3At	1.48	142	124	10.42
43	O15ata	1.58	142	138	11.13
44	Q11atd	8.25	528	277	15.63
45	O5At	-	-	-	-
46	N27Aaod	12.32	292	0	42.19

Figure 1.13
SPICE2 with bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
47	N27A2t	28.90	441	424	65.53
48	N27A3o	1.43	17	0	84.12
49	N27A4o	1.43	17	0	84.12
50	N27A5o	28.73	426	418	67.44
51	N27A6aod	8.98	247	0	36.36
52	N12At	5.58	310	262	18.00
53	N8Ao	0.92	10	0	92.00
54	N2Ao	0.52	10	0	52.00
55	O6At	0.45	126	124	3.57
56	N1A5d	0.43	53	0	8.11
57	N6At	6.15	401	398	15.34
58	Q11Atad	11.18	756	499	14.79
59	Q5Ao	0.33	15	0	22.00
60	Q2Dtd	2.77	562	313	4.93
61	O66At	34.78	1706	1689	20.39
62	N2Dtdo	8.68	1218	460	7.13
63	Q8Dtd	10.38	628	343	16.53
64	Q4A3t	3.22	337	329	9.55
65	Q50At	153.93	2229	2192	69.06
66	O5A1t	0.57	150	148	3.80
67	C38Da	-	-	-	-
68	C38D2a	-	-	-	-
69	O6A1t	0.32	126	124	2.54
70	O3Ap	-	-	-	-
71	O7Ap	-	-	-	-
72	T1Atad	1.43	342	256	4.18
73	T2A1t	2.62	900	898	2.91
74	T1A1t	0.83	328	328	2.53
75	t1A2t	0.68	328	328	2.07
76	T3At	2.03	300	296	6.77
77	T3A2t	1.92	300	296	6.40
78	Q5Dtd	6.63	753	460	8.80
79	Q5D1td	6.78	779	466	8.70
80	Q7Dtd	7.90	737	455	10.72
81	Q6Dtd	7.20	745	440	9.66
82	Q5D2td	6.72	762	482	8.82
83	Q4A5ta	-	-	-	-
84	Q15atad	12.42	496	167	25.04
85	Q22Atad	17.10	446	176	38.34
86	Q22A2tad	14.85	449	178	33.07
87	Q11Ata	5.47	183	167	29.89
88	Q11Ao	0.52	8	0	65.00
89	Q22A3tad	14.78	549	254	26.92
90	Q22A4tad	13.78	340	230	40.53
91	Q22A5tad	13.38	475	178	28.17
92	O3A1t	-	-	-	-
93	N9At	15.62	619	591	25.23
94	O38Aa	0.80	2	0	400.00
95	C18At	-	-	-	-

Figure 1.13
SPICE2 with bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
96	C18A1t	24.43	549	523	44.50
97	Q18A2t	26.40	598	570	44.15
98	N4Ada	1.42	70	0	20.29
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	-	-	-	-
102	C19Mt	-	-	-	-
103	C68Dt	397.07	1661	1652	239.05
104	C9Ao	-	-	-	-
105	C82Dt	-	-	-	-
106	C2At	1.88	175	169	10.74
107	C37Dt	-	-	-	-
108	N27At	18.57	322	306	57.67
109	N698Dt	3257.62	3553	3469	916.86
110	Q6At	454.33	52240	52229	8.70
111	C7Atd	9.97	326	185	30.58
112	C52Aa	-	-	-	-
113	Q340t	5023.77	2346	2188	2141.42
114	C54Dt	177.82	857	851	207.49
115	N1190Mt	-	-	-	-
116	C31Dt	-	-	-	-
117	Q2A1t	1404.27	284785	284786	4.93
118	C119At	-	-	-	-
119	C6Dt	7.02	252	244	27.86
120	Q2A2t	10.02	2325	2317	4.31
121	Q6A1t	16.18	1774	1765	9.12
122	Q4A4ta	-	-	-	-
123	O4Ao	-	-	-	-
124	H44Aa	-	-	-	-
125	Q10Ao	1.23	37	0	33.24
126	C77Mt	-	-	-	-
127	Q4Af	0.32	9	0	35.56
128	N2Aa	0.62	6	0	103.33
129	N1Ad	0.58	125	0	4.64
130	O5A2t	0.32	128	126	2.50
131	O2At	0.18	114	114	1.58
132	O2A2t	0.23	117	114	1.97
133	C205At	-	-	-	-
134	T2A2t	0.82	170	168	4.82
135	C26At	28.28	273	256	103.59
136	N1At	0.62	120	114	5.17
137	C37At	-	-	-	-
138	N3At	-	-	-	-
139	C6D1t	-	-	-	-
140	Q86Aa	14.02	9	0	1557.78
141	C640Dt	-	-	-	-
142	C1060Mt	-	-	-	-
143	Q14Ao	1.25	14	0	89.29
144	C28Dt	-	-	-	-

Figure 1.13
SPICE2 with bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
145	C23Dt	-	-	-	-
146	O20At	-	-	-	-
147	C277Mt	1317.30	3385	3385	389.16
148	C277M2t	2503.52	5003	5003	500.40
149	C42Dt	-	-	-	-
150	C7Ad	-	-	-	-
151	C14D1t	-	-	-	-
152	Q84At	1316.45	3496	3465	376.56
153	Q50A1t	154.77	2229	2192	69.43
154	O20A1t	5.88	1204	1200	4.88
117	total	17260.48	399136	390700	
	average	147.53	3411	3339	43.24

Figure 1.14
SPICE2 with bypass, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
1	Q180Do	8.35	1.38	52	3.92
2	Q180D2o	8.30	1.32	52	3.87
3	Q2At	0.52	0.48	719	2.17
4	O9Aa	0.00	0.00	1	0.00
5	O1024Ao	-	-	-	-
6	N48Dt	2.63	1.27	727	127.55
7	N5At	0.02	0.05	90	1.73
8	N5A2t	0.05	0.03	92	1.87
9	O10At	-	-	-	-
10	Q6Ao	0.02	0.00	12	0.07
11	Q6A2o	0.18	0.02	146	0.43
12	Q4Ao	0.03	0.00	6	0.00
13	N1Aot	0.03	0.05	74	0.32
14	N1A2ot	0.02	0.02	117	0.57
15	N1A3ot	0.03	0.05	94	0.35
16	O8At	0.07	0.03	152	0.18
17	Q1Ado	0.07	0.02	48	0.03
18	Q1A2t	0.05	0.02	264	0.47
19	Q5Atd	0.28	0.10	236	1.32
20	C25Ao	0.18	0.03	33	0.92
21	C27Ao	0.22	0.03	42	1.42
22	C7Ao	0.07	0.02	43	0.50
23	C4Dto	0.12	0.03	272	3.87
24	C22Dt	1.10	0.42	144	12.50
25	C22D2o	0.28	0.05	15	0.63
26	T2At	0.25	0.08	193	0.12
27	Q7Ao	0.05	0.00	12	0.05
28	N116Dt	12.98	6.08	1090	217.03
29	N2Dod	0.03	0.00	129	0.78
30	Q4At	0.17	0.07	108	0.45
31	Q8Atd	1.33	0.47	389	3.38
32	Q4A1t	0.28	0.03	167	0.85
33	C4D1to	0.10	0.07	197	2.82
34	Q4a2t	0.07	0.03	65	0.33
35	Q10At	4.97	1.05	129	3.48
36	O3At	0.00	0.00	63	0.05
37	N10Dto	0.17	0.08	202	8.30
38	N10D2to	0.08	0.12	197	7.77
39	N10Ato	0.17	0.05	177	7.13
40	N1A4d	0.00	0.00	34	0.07
41	Q7Aat	0.28	0.32	271	3.32
42	Q3At	0.15	0.07	79	0.48
43	O15ata	0.13	0.03	72	0.07
44	Q11atd	1.38	0.60	336	4.03
45	O5At	-	-	-	-
46	N27Aaod	0.48	0.22	190	9.40
47	N27A2t	0.92	0.33	299	24.12
48	N27A3o	0.13	0.03	16	0.60

Figure 1.14
SPICE2 with bypass, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
49	N27A4o	0.12	0.02	16	0.63
50	N27A5o	0.73	0.47	284	24.07
51	N27A6aod	0.33	0.20	145	6.32
52	N12At	0.22	0.10	199	3.80
53	N8Ao	0.07	0.00	9	0.25
54	N2Ao	0.03	0.02	9	0.05
55	O6At	0.02	0.02	63	0.05
56	N1A5d	0.03	0.00	41	0.13
57	N6At	0.30	0.20	247	4.02
58	Q11Atad	1.28	0.82	511	5.87
59	Q5Ao	0.02	0.00	14	0.05
60	Q2Dtd	0.20	0.18	365	0.80
61	O66At	7.75	3.32	891	6.07
62	N2Dtdo	0.33	0.15	915	4.92
63	Q8Dtd	2.25	0.80	425	4.98
64	Q4A3t	0.37	0.18	220	1.20
65	Q50At	27.95	10.98	1604	82.55
66	O5A1t	0.00	0.00	75	0.03
67	C38Da	-	-	-	-
68	C38D2a	-	-	-	-
69	O6A1t	0.02	0.00	63	0.05
70	O3Ap	-	-	-	-
71	O7Ap	-	-	-	-
72	T1Atad	0.08	0.00	172	0.08
73	T2A1t	0.22	0.28	450	0.27
74	T1A1t	0.07	0.03	163	0.08
75	t1A2t	0.10	0.07	163	0.05
76	T3At	0.22	0.12	151	0.08
77	T3A2t	0.23	0.12	151	0.07
78	Q5Dtd	1.12	0.52	532	3.07
79	Q5D1td	1.28	0.55	562	3.18
80	Q7Dtd	1.50	0.80	524	3.60
81	Q6Dtd	1.40	0.63	533	3.12
82	Q5D2td	1.32	0.72	528	2.82
83	Q4A5ta	-	-	-	-
84	Q15atad	2.55	0.77	336	4.18
85	Q22Atad	2.50	0.98	287	7.70
86	Q22A2tad	2.45	0.87	290	5.55
87	Q11Ata	0.52	0.15	110	1.68
88	Q11Ao	0.07	0.00	7	0.05
89	Q22A3tad	2.75	0.88	348	6.77
90	Q22A4tad	3.12	1.00	214	5.05
91	Q22A5tad	2.05	0.72	309	5.52
92	O3A1t	-	-	-	-
93	N9At	0.87	0.57	460	12.08
94	O38Aa	0.05	0.00	1	0.02
95	C18At	-	-	-	-
96	C18A1t	6.55	1.22	418	13.47
97	Q18A2t	6.92	1.38	456	14.35

Figure 1.14
SPICE2 with bypass, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
98	N4Ada	0.07	0.00	58	0.68
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	-	-	-	-
102	C19Mt	-	-	-	-
103	C68Dt	36.57	14.58	1258	318.43
104	C9Ao	-	-	-	-
105	C82Dt	-	-	-	-
106	C2At	0.05	0.03	114	1.40
107	C37Dt	-	-	-	-
108	N27At	0.53	0.37	201	14.95
109	N698Dt	216.48	71.88	2377	2497.40
110	Q6At	49.33	30.38	41820	294.85
111	C7Atd	0.58	0.25	233	7.60
112	C52Aa	-	-	-	-
113	Q340t	3476.08	261.22	1821	955.88
114	C54Dt	60.22	13.42	663	80.90
115	N1190Mt	-	-	-	-
116	C31Dt	-	-	-	-
117	Q2A1t	332.93	171.17	246534	711.47
118	C119At	-	-	-	-
119	C6Dt	0.05	0.05	166	5.65
120	Q2A2t	1.18	0.52	1794	5.78
121	Q6A1t	1.28	0.60	1290	10.87
122	Q4A4ta	-	-	-	-
123	O4Ao	-	-	-	-
124	H44Aa	-	-	-	-
125	Q10Ao	0.47	0.08	36	0.10
126	C77Mt	-	-	-	-
127	Q4Af	0.02	0.02	8	0.02
128	N2Aa	0.02	0.02	5	0.00
129	N1Ad	0.08	0.00	69	0.28
130	O5A2t	0.00	0.00	64	0.00
131	O2At	0.00	0.00	56	0.02
132	O2A2t	0.00	0.02	59	0.03
133	C205At	-	-	-	-
134	T2A2t	0.18	0.03	85	0.07
135	C26At	5.43	1.00	183	13.93
136	N1At	0.02	0.00	62	0.22
137	C37At	-	-	-	-
138	N3At	-	-	-	-
139	C6D1t	-	-	-	-
140	Q86Aa	3.60	0.17	8	0.30
141	C640Dt	-	-	-	-
142	C1060Mt	-	-	-	-
143	Q14Ao	0.20	0.10	13	0.12
144	C28Dt	-	-	-	-
145	C23Dt	-	-	-	-
146	O20At	-	-	-	-

Figure 1.14
SPICE2 with bypass, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
147	C277Mt	76.85	28.70	2476	956.60
148	C277M2t	119.85	43.80	3734	1976.20
149	C42Dt	-	-	-	-
150	C7Ad	-	-	-	-
151	C14D1t	-	-	-	-
152	Q84At	321.30	124.07	2241	437.12
153	Q50A1t	27.88	10.27	1604	83.80
154	O20A1t	1.12	0.87	794	1.62
117	total	4859.07	818.57	330933	9074.25
	average	41.53	7.00	2828	77.56

1.3.6. SPICE2 without bypass

Figure 1.15
SPICE2 without bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
1	Q180Do	22.93	53	0	432.64
2	Q180D2o	22.65	53	0	427.36
3	Q2At	3.97	875	865	4.54
4	O9Aa	0.27	2	0	135.00
5	O1024Ao	-	-	-	-
6	N48Dt	119.93	992	978	120.90
7	N5At	2.63	160	140	16.44
8	N5A2t	2.60	162	142	16.05
9	O10At	-	-	-	-
10	Q6Ao	0.25	13	0	19.23
11	Q6A2o	0.90	147	0	6.12
12	Q4Ao	0.27	7	0	38.57
13	N1Aot	1.17	142	134	8.24
14	N1A2ot	1.57	228	220	6.89
15	N1A3ot	1.07	182	174	5.88
16	O8At	0.82	220	220	3.73
17	Q1Ado	0.37	70	0	5.29
18	Q1A2t	1.22	360	351	3.39
19	Q5Atd	2.83	419	193	6.75
20	C25Ao	1.78	34	0	52.35
21	C27Ao	2.55	43	0	59.30
22	C7Ao	0.68	44	0	15.45
23	C4Dto	4.42	403	383	10.97
24	C22Dt	13.97	208	180	67.16
25	C22D2o	1.92	16	0	120.00
26	T2At	1.53	386	384	3.96
27	Q7Ao	0.38	13	0	29.23
28	N116Dt	324.95	1562	1494	208.03
29	N2Dod	1.20	229	0	5.24
30	Q4At	1.78	166	158	10.72
31	Q8Atd	7.17	611	382	11.73
32	Q4A1t	2.03	256	248	7.93
33	C4D1to	3.58	308	278	11.62
34	Q4a2t	1.03	123	114	8.37
35	Q10At	12.42	189	177	65.71
36	O3At	0.23	126	124	1.83
37	N10Dto	8.17	287	245	28.47
38	N10D2to	7.78	281	239	27.69
39	N10Ato	8.15	260	218	31.35
40	N1A4d	0.25	61	0	4.10
41	Q7Aat	6.30	337	255	18.69
42	Q3At	1.35	142	124	9.51
43	O15ata	1.25	142	138	8.80
44	Q11atd	7.63	527	276	14.48
45	O5At	-	-	-	-
46	N27Aaod	11.48	292	0	39.32

Figure 1.15
SPICE2 without bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
47	N27A2t	23.55	392	375	60.08
48	N27A3o	1.05	17	0	61.76
49	N27A4o	1.22	17	0	71.76
50	N27A5o	22.12	366	358	60.44
51	N27A6aod	7.38	247	0	29.88
52	N12At	5.62	309	266	18.19
53	N8Ao	0.72	10	0	72.00
54	N2Ao	0.48	10	0	48.00
55	O6At	0.38	126	124	3.02
56	N1A5d	0.30	53	0	5.66
57	N6At	5.33	385	382	13.84
58	Q11Atad	10.10	722	465	13.99
59	Q5Ao	0.33	15	0	22.00
60	Q2Dtd	2.28	503	254	4.53
61	O66At	28.18	1680	1663	16.77
62	N2Dtdo	6.98	1218	460	5.73
63	Q8Dtd	9.95	621	341	16.02
64	Q4A3t	2.92	352	344	8.30
65	Q50At	160.00	2273	2236	70.39
66	O5A1t	0.48	150	148	3.20
67	C38Da	-	-	-	-
68	C38D2a	-	-	-	-
69	O6A1t	0.28	126	124	2.22
70	O3Ap	-	-	-	-
71	O7Ap	-	-	-	-
72	T1Atad	1.28	342	256	3.74
73	T2A1t	2.15	898	896	2.39
74	T1A1t	0.82	328	328	2.50
75	t1A2t	0.78	328	328	2.38
76	T3At	1.72	300	296	5.73
77	T3A2t	1.50	300	296	5.00
78	Q5Dtd	6.30	731	437	8.62
79	Q5D1td	6.52	765	471	8.52
80	Q7Dtd	7.73	736	454	10.50
81	Q6Dtd	7.42	830	438	8.94
82	Q5D2td	6.33	738	458	8.58
83	Q4A5ta	-	-	-	-
84	Q15atad	13.28	526	164	25.25
85	Q22Atad	16.48	446	176	36.95
86	Q22A2tad	14.17	447	176	31.70
87	Q11Ata	4.78	183	167	26.12
88	Q11Ao	0.43	8	0	53.75
89	Q22A3tad	13.60	527	232	25.81
90	Q22A4tad	12.08	272	161	44.41
91	Q22A5tad	13.53	463	166	29.22
92	O3A1t	-	-	-	-
93	N9At	12.98	595	567	21.82
94	O38Aa	0.68	2	0	340.00
95	C18At	-	-	-	-

Figure 1.15
SPICE2 without bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
96	C18A1t	23.10	571	547	40.46
97	Q18A2t	23.92	579	551	41.31
98	N4Ada	1.32	70	0	18.86
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	-	-	-	-
102	C19Mt	-	-	-	-
103	C68Dt	329.48	1655	1646	199.08
104	C9Ao	-	-	-	-
105	C82Dt	-	-	-	-
106	C2At	1.42	175	169	8.11
107	C37Dt	-	-	-	-
108	N27At	19.65	325	309	60.46
109	N698Dt	3734.77	3546	3468	1053.23
110	Q6At	430.42	52412	52401	8.21
111	C7Atd	8.18	327	186	25.02
112	C52Aa	-	-	-	-
113	Q340t	3927.57	1925	1797	2040.30
114	C54Dt	154.58	833	827	185.57
115	N1190Mt	-	-	-	-
116	C31Dt	-	-	-	-
117	Q2A1t	25.80	5379	5379	4.80
118	C119At	-	-	-	-
119	C6Dt	5.13	252	244	20.36
120	Q2A2t	8.62	2169	2161	3.97
121	Q6A1t	15.83	1800	1791	8.79
122	Q4A4ta	-	-	-	-
123	O4Ao	-	-	-	-
124	H44Aa	-	-	-	-
125	Q10Ao	1.17	37	0	31.62
126	C77Mt	-	-	-	-
127	Q4Af	0.25	9	0	27.78
128	N2Aa	0.53	6	0	88.33
129	N1Ad	0.53	125	0	4.24
130	O5A2t	0.27	128	126	2.11
131	O2At	0.17	114	114	1.49
132	O2A2t	0.22	117	114	1.88
133	C205At	-	-	-	-
134	T2A2t	0.53	170	168	3.12
135	C26At	25.38	282	265	90.00
136	N1At	0.57	120	114	4.75
137	C37At	-	-	-	-
138	N3At	-	-	-	-
139	C6D1t	-	-	-	-
140	Q86Aa	12.58	9	0	1397.78
141	C640Dt	-	-	-	-
142	C1060Mt	-	-	-	-
143	Q14Ao	1.03	14	0	73.57
144	C28Dt	-	-	-	-

Figure 1.15
SPICE2 without bypass, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
145	C23Dt	-	-	-	-
146	O20At	-	-	-	-
147	C277Mt	1583.70	3309	3309	478.60
148	C277M2t	2833.18	4589	4589	617.39
149	C42Dt	-	-	-	-
150	C7Ad	-	-	-	-
151	C14D1t	-	-	-	-
152	Q84At	1189.62	3576	3545	332.67
153	Q50A1t	159.93	2273	2236	70.36
154	O20A1t	4.70	1204	1200	3.90
117	total	15577.79	118588	110097	
	average	133.14	1013	941	131.36

Figure 1.16
SPICE2 without bypass, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
1	Q180Do	7.85	1.30	52	4.85
2	Q180D2o	7.67	1.22	52	4.82
3	Q2At	0.48	0.30	664	2.25
4	O9Aa	0.00	0.00	1	0.00
5	O1024Ao	-	-	-	-
6	N48Dt	2.78	1.15	727	113.68
7	N5At	0.05	0.00	90	1.55
8	N5A2t	0.08	0.02	92	1.58
9	O10At	-	-	-	-
10	Q6Ao	0.02	0.03	12	0.02
11	Q6A2o	0.10	0.08	146	0.37
12	Q4Ao	0.00	0.00	6	0.02
13	N1Aot	0.03	0.02	74	0.42
14	N1A2ot	0.00	0.03	117	0.62
15	N1A3ot	0.02	0.05	94	0.37
16	O8At	0.02	0.03	152	0.17
17	Q1Ado	0.02	0.02	48	0.05
18	Q1A2t	0.13	0.12	264	0.43
19	Q5Atd	0.10	0.12	236	1.42
20	C25Ao	0.20	0.05	33	0.83
21	C27Ao	0.25	0.03	42	1.33
22	C7Ao	0.02	0.00	43	0.43
23	C4Dto	0.12	0.05	257	3.23
24	C22Dt	1.10	0.32	144	10.47
25	C22D2o	0.22	0.07	15	0.52
26	T2At	0.27	0.15	193	0.17
27	Q7Ao	0.05	0.02	12	0.03
28	N116Dt	10.95	5.05	1089	277.70
29	N2Dod	0.07	0.00	127	0.58
30	Q4At	0.13	0.08	108	0.62
31	Q8Atd	1.22	0.50	394	3.82
32	Q4A1t	0.17	0.03	165	1.00
33	C4D1to	0.05	0.02	197	2.65
34	Q4a2t	0.05	0.00	65	0.43
35	Q10At	4.25	0.95	120	3.90
36	O3At	0.02	0.00	63	0.07
37	N10Dto	0.08	0.18	198	6.73
38	N10D2to	0.12	0.13	193	6.58
39	N10Ato	0.15	0.07	176	6.83
40	N1A4d	0.00	0.03	34	0.07
41	Q7Aat	0.47	0.20	271	3.48
42	Q3At	0.27	0.05	79	0.33
43	O15ata	0.12	0.00	72	0.08
44	Q11atd	1.18	0.68	335	4.48
45	O5At	-	-	-	-
46	N27Aaod	0.48	0.28	190	8.73
47	N27A2t	0.80	0.32	268	20.35
48	N27A3o	0.12	0.05	16	0.38

Figure 1.16
SPICE2 without bypass, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
49	N27A4o	0.07	0.00	16	0.52
50	N27A5o	0.73	0.43	245	18.90
51	N27A6aod	0.43	0.23	145	4.78
52	N12At	0.10	0.03	193	4.23
53	N8Ao	0.05	0.00	9	0.15
54	N2Ao	0.03	0.00	9	0.05
55	O6At	0.00	0.03	63	0.03
56	N1A5d	0.02	0.00	41	0.15
57	N6At	0.23	0.07	239	3.75
58	Q11Atad	1.02	0.57	483	6.20
59	Q5Ao	0.02	0.00	14	0.03
60	Q2Dtd	0.12	0.15	318	0.80
61	O66At	7.12	2.98	876	6.32
62	N2Dtdo	0.25	0.15	915	4.12
63	Q8Dtd	1.97	0.85	418	5.48
64	Q4A3t	0.32	0.17	231	1.25
65	Q50At	24.92	9.82	1631	107.60
66	O5A1t	0.02	0.00	75	0.05
67	C38Da	-	-	-	-
68	C38D2a	-	-	-	-
69	O6A1t	0.03	0.00	63	0.02
70	O3Ap	-	-	-	-
71	O7Ap	-	-	-	-
72	T1Atad	0.08	0.00	172	0.07
73	T2A1t	0.32	0.22	449	0.27
74	T1A1t	0.08	0.05	163	0.12
75	t1A2t	0.08	0.02	163	0.05
76	T3At	0.10	0.15	151	0.12
77	T3A2t	0.07	0.20	151	0.07
78	Q5Dtd	0.85	0.62	516	3.38
79	Q5D1td	1.03	0.60	547	3.45
80	Q7Dtd	1.33	0.68	523	4.18
81	Q6Dtd	1.50	0.45	618	4.00
82	Q5D2td	0.88	0.62	510	3.48
83	Q4A5ta	-	-	-	-
84	Q15atad	2.63	0.75	367	5.67
85	Q22Atad	2.25	0.65	287	8.73
86	Q22A2tad	2.13	0.73	288	6.47
87	Q11Ata	0.48	0.10	110	2.07
88	Q11Ao	0.05	0.00	7	0.07
89	Q22A3tad	1.87	0.73	336	7.88
90	Q22A4tad	2.32	0.73	183	5.32
91	Q22A5tad	2.22	0.57	303	6.50
92	O3A1t	-	-	-	-
93	N9At	0.65	0.45	442	10.33
94	O38Aa	0.05	0.00	1	0.02
95	C18At	-	-	-	-
96	C18A1t	5.58	1.35	436	13.93
97	Q18A2t	5.93	1.20	439	14.62

Figure 1.16
SPICE2 without bypass, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
98	N4Ada	0.05	0.00	58	0.58
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	-	-	-	-
102	C19Mt	-	-	-	-
103	C68Dt	31.90	12.70	1255	269.42
104	C9Ao	-	-	-	-
105	C82Dt	-	-	-	-
106	C2At	0.03	0.00	114	0.97
107	C37Dt	-	-	-	-
108	N27At	0.33	0.18	200	16.68
109	N698Dt	186.50	66.47	2370	3163.82
110	Q6At	38.45	27.05	41941	300.80
111	C7Atd	0.45	0.30	235	6.10
112	C52Aa	-	-	-	-
113	Q340t	2507.92	185.28	1462	928.87
114	C54Dt	49.70	10.68	646	80.15
115	N1190Mt	-	-	-	-
116	C31Dt	-	-	-	-
117	Q2A1t	4.90	2.57	4204	13.80
118	C119At	-	-	-	-
119	C6Dt	0.10	0.10	166	4.00
120	Q2A2t	0.80	0.47	1661	5.22
121	Q6A1t	0.97	0.60	1318	11.78
122	Q4A4ta	-	-	-	-
123	O4Ao	-	-	-	-
124	H44Aa	-	-	-	-
125	Q10Ao	0.40	0.07	36	0.17
126	C77Mt	-	-	-	-
127	Q4Af	0.03	0.02	8	0.00
128	N2Aa	0.02	0.00	5	0.03
129	N1Ad	0.00	0.07	69	0.27
130	O5A2t	0.00	0.02	64	0.02
131	O2At	0.00	0.00	56	0.02
132	O2A2t	0.00	0.00	59	0.07
133	C205At	-	-	-	-
134	T2A2t	0.10	0.05	85	0.08
135	C26At	4.67	0.60	190	14.53
136	N1At	0.00	0.00	62	0.17
137	C37At	-	-	-	-
138	N3At	-	-	-	-
139	C6D1t	-	-	-	-
140	Q86Aa	3.17	0.17	8	0.43
141	C640Dt	-	-	-	-
142	C1060Mt	-	-	-	-
143	Q14Ao	0.20	0.02	13	0.12
144	C28Dt	-	-	-	-
145	C23Dt	-	-	-	-
146	O20At	-	-	-	-

Figure 1.16
SPICE2 without bypass, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
147	C277Mt	62.07	23.55	2426	1382.73
148	C277M2t	92.20	35.15	3415	2537.43
149	C42Dt	-	-	-	-
150	C7Ad	-	-	-	-
151	C14D1t	-	-	-	-
152	Q84At	296.40	112.90	2288	521.98
153	Q50A1t	24.60	10.32	1631	105.08
154	O20A1t	1.05	0.57	794	1.90
117	total	3419.19	530.04	87711	10130.89
	average	29.22	4.53	749	86.59

1.3.7. SPICE2 with bypass using the fort compiler

Figure 1.17
SPICE2 with bypass using the fort compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
1	Q180Do	16.47	53	0	310.75
2	Q180D2o	16.23	53	0	306.23
3	Q2At	2.63	945	935	2.78
4	O9Aa	0.18	2	0	90.00
5	O1024Ao	-	-	-	-
6	N48Dt	56.05	992	978	56.50
7	N5At	1.47	160	140	9.19
8	N5A2t	1.37	162	142	8.46
9	O10At	-	-	-	-
10	Q6Ao	0.22	13	0	16.92
11	Q6A2o	0.57	147	0	3.88
12	Q4Ao	0.23	7	0	32.86
13	N1Aot	0.67	142	134	4.72
14	N1A2ot	0.92	228	220	4.04
15	N1A3ot	0.68	182	174	3.74
16	O8At	0.50	220	220	2.27
17	Q1Ado	0.25	70	0	3.57
18	Q1A2t	0.73	360	351	2.03
19	Q5Atd	1.78	419	193	4.25
20	C25Ao	1.12	34	0	32.94
21	C27Ao	1.53	43	0	35.58
22	C7Ao	0.50	44	0	11.36
23	C4Dto	2.65	423	403	6.26
24	C22Dt	8.03	208	180	38.61
25	C22D2o	1.23	16	0	76.88
26	T2At	1.08	386	384	2.80
27	Q7Ao	0.28	13	0	21.54
28	N116Dt	146.18	1564	1496	93.47
29	N2Dod	0.72	231	0	3.12
30	Q4At	1.03	166	158	6.20
31	Q8Atd	4.53	605	375	7.49
32	Q4A1t	1.28	258	250	4.96
33	C4D1to	2.23	305	275	7.31
34	Q4a2t	0.63	123	114	5.12
35	Q10At	9.42	199	187	47.34
36	O3At	0.17	126	124	1.35
37	N10Dto	4.17	291	249	14.33
38	N10D2to	4.02	285	243	14.11
39	N10Ato	3.88	259	217	14.98
40	N1A4d	-	-	-	-
41	Q7Aat	4.02	337	255	11.93
42	Q3At	0.82	142	124	5.77
43	O15ata	0.88	142	138	6.20
44	Q11atd	5.13	528	277	9.72
45	O5At	-	-	-	-
46	N27Aaod	6.42	292	0	21.99

Figure 1.17
SPICE2 with bypass using the fort compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
47	N27A2t	12.95	402	385	32.21
48	N27A3o	0.83	17	0	48.82
49	N27A4o	0.92	17	0	54.12
50	N27A5o	11.40	349	341	32.66
51	N27A6aod	4.75	247	0	19.23
52	N12At	2.97	310	262	9.58
53	N8Ao	0.58	10	0	58.00
54	N2Ao	0.33	10	0	33.00
55	O6At	0.23	126	124	1.83
56	N1A5d	0.23	53	0	4.34
57	N6At	3.13	401	398	7.81
58	Q11Atad	7.27	756	499	9.62
59	Q5Ao	0.18	15	0	12.00
60	Q2Dtd	1.72	562	313	3.06
61	O66At	22.22	1669	1652	13.31
62	N2Dtdo	4.30	1218	460	3.53
63	Q8Dtd	6.65	628	343	10.59
64	Q4A3t	1.93	337	329	5.73
65	Q50At	93.63	2228	2191	42.02
66	O5A1t	0.38	150	148	2.53
67	C38Da	-	-	-	-
68	C38D2a	-	-	-	-
69	O6A1t	0.22	126	124	1.75
70	O3Ap	-	-	-	-
71	O7Ap	-	-	-	-
72	T1Atad	0.97	342	256	2.84
73	T2A1t	1.82	898	896	2.03
74	T1A1t	0.67	328	328	2.04
75	t1A2t	0.53	328	328	1.62
76	T3At	1.22	300	296	4.07
77	T3A2t	1.18	300	296	3.93
78	Q5Dtd	3.93	753	460	5.22
79	Q5D1td	4.12	782	466	5.27
80	Q7Dtd	5.03	737	455	6.82
81	Q6Dtd	4.45	745	440	5.97
82	Q5D2td	4.33	762	482	5.68
83	Q4A5ta	-	-	-	-
84	Q15atad	8.32	496	167	16.77
85	Q22Atad	11.02	446	176	24.71
86	Q22A2tad	9.72	449	178	21.65
87	Q11Ata	3.28	183	167	17.92
88	Q11Ao	0.32	8	0	40.00
89	Q22A3tad	9.32	549	254	16.98
90	Q22A4tad	9.17	340	230	26.97
91	Q22A5tad	9.18	475	178	19.33
92	O3A1t	-	-	-	-
93	N9At	7.92	619	591	12.79
94	O38Aa	0.48	2	0	240.00
95	C18At	-	-	-	-

Figure 1.17
SPICE2 with bypass using the fort compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
96	C18A1t	13.57	575	549	23.60
97	Q18A2t	-	-	-	-
98	N4Ada	0.75	70	0	10.71
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	-	-	-	-
102	C19Mt	-	-	-	-
103	C68Dt	184.13	1661	1652	110.85
104	C9Ao	-	-	-	-
105	C82Dt	-	-	-	-
106	C2At	0.90	175	169	5.14
107	C37Dt	-	-	-	-
108	N27At	9.23	322	306	28.66
109	N698Dt	1606.67	3536	3469	454.38
110	Q6At	263.30	52289	52278	5.04
111	C7Atd	4.52	326	185	13.87
112	C52Aa	-	-	-	-
113	Q340t	6092.68	4144	4028	1470.24
114	C54Dt	-	-	-	-
115	N1190Mt	-	-	-	-
116	C31Dt	-	-	-	-
117	Q2A1t	833.07	278030	278031	3.00
118	C119At	-	-	-	-
119	C6Dt	2.97	252	244	11.79
120	Q2A2t	5.83	2294	2286	2.54
121	Q6A1t	9.00	1725	1716	5.22
122	Q4A4ta	-	-	-	-
123	O4Ao	-	-	-	-
124	H44Aa	-	-	-	-
125	Q10Ao	0.80	37	0	21.62
126	C77Mt	-	-	-	-
127	Q4Af	0.17	9	0	18.89
128	N2Aa	0.42	6	0	70.00
129	N1Ad	0.28	125	0	2.24
130	O5A2t	0.20	128	126	1.56
131	O2At	0.10	114	114	0.88
132	O2A2t	0.17	117	114	1.45
133	C205At	-	-	-	-
134	T2A2t	0.52	170	168	3.06
135	C26At	-	-	-	-
136	N1At	0.42	120	114	3.50
137	C37At	-	-	-	-
138	N3At	-	-	-	-
139	C6D1t	-	-	-	-
140	Q86Aa	9.82	9	0	1091.11
141	C640Dt	-	-	-	-
142	C1060Mt	-	-	-	-
143	Q14Ao	0.68	14	0	48.57
144	C28Dt	-	-	-	-

Figure 1.17
SPICE2 with bypass using the fort compiler, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
145	C23Dt	-	-	-	-
146	O20At	-	-	-	-
147	C277Mt	653.88	3451	3451	189.48
148	C277M2t	1253.00	5002	5002	250.50
149	C42Dt	-	-	-	-
150	C7Ad	-	-	-	-
151	C14D1t	-	-	-	-
152	Q84At	807.42	3496	3465	230.96
153	Q50A1t	91.17	2228	2191	40.92
154	O20A1t	3.27	1204	1200	2.72
113	total	12435.64	392277	384007	
	average	110.05	3471	3398	31.70

Figure 1.18
SPICE2 with bypass using the fort compiler, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
1	Q180Do	5.80	1.13	52	2.82
2	Q180D2o	6.02	0.92	52	2.70
3	Q2At	0.37	0.27	716	1.18
4	O9Aa	0.00	0.00	1	0.00
5	O1024Ao	-	-	-	-
6	N48Dt	2.10	0.75	727	51.52
7	N5At	0.00	0.07	90	0.68
8	N5A2t	0.00	0.02	92	0.67
9	O10At	-	-	-	-
10	Q6Ao	0.02	0.00	12	0.05
11	Q6A2o	0.12	0.02	146	0.25
12	Q4Ao	0.02	0.00	6	0.02
13	N1Aot	0.05	0.00	74	0.13
14	N1A2ot	0.05	0.05	117	0.25
15	N1A3ot	0.00	0.00	94	0.15
16	O8At	0.05	0.05	152	0.10
17	Q1Ado	0.00	0.05	48	0.02
18	Q1A2t	0.03	0.05	264	0.27
19	Q5Atd	0.18	0.15	236	0.83
20	C25Ao	0.12	0.03	33	0.45
21	C27Ao	0.18	0.08	42	0.60
22	C7Ao	0.03	0.02	43	0.22
23	C4Dto	0.08	0.07	274	1.80
24	C22Dt	0.93	0.47	144	5.15
25	C22D2o	0.22	0.00	15	0.28
26	T2At	0.23	0.10	193	0.07
27	Q7Ao	0.03	0.00	12	0.02
28	N116Dt	7.37	3.57	1089	110.37
29	N2Dod	0.00	0.02	129	0.38
30	Q4At	0.12	0.02	108	0.30
31	Q8Atd	0.67	0.33	389	2.55
32	Q4A1t	0.08	0.08	167	0.65
33	C4D1to	0.03	0.08	197	1.40
34	Q4a2t	0.02	0.02	65	0.25
35	Q10At	3.70	0.73	129	2.30
36	O3At	0.00	0.03	63	0.03
37	N10Dto	0.03	0.13	202	3.28
38	N10D2to	0.08	0.08	197	3.10
39	N10Ato	0.08	0.02	177	3.08
40	N1A4d	-	-	-	-
41	Q7Aat	0.28	0.18	271	1.82
42	Q3At	0.18	0.05	79	0.20
43	O15ata	0.02	0.00	72	0.03
44	Q11atd	0.88	0.55	336	2.68
45	O5At	-	-	-	-
46	N27Aaod	0.32	0.22	190	4.40
47	N27A2t	0.73	0.18	279	10.42
48	N27A3o	0.07	0.00	16	0.33

Figure 1.18
SPICE2 with bypass using the fort compiler, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
49	N27A4o	0.08	0.02	16	0.30
50	N27A5o	0.58	0.30	232	8.95
51	N27A6aod	0.25	0.22	145	2.75
52	N12At	0.08	0.12	199	1.95
53	N8Ao	0.03	0.00	9	0.10
54	N2Ao	0.02	0.00	9	0.02
55	O6At	0.00	0.00	63	0.03
56	N1A5d	0.00	0.02	41	0.10
57	N6At	0.12	0.07	247	2.00
58	Q11Atad	0.77	0.37	511	3.98
59	Q5Ao	0.02	0.00	14	0.03
60	Q2Dtd	0.20	0.13	365	0.53
61	O66At	5.98	2.28	872	4.28
62	N2Dtdo	0.22	0.13	915	2.18
63	Q8Dtd	1.58	0.67	425	3.13
64	Q4A3t	0.17	0.22	220	0.70
65	Q50At	18.52	7.87	1604	53.47
66	O5A1t	0.02	0.00	75	0.05
67	C38Da	-	-	-	-
68	C38D2a	-	-	-	-
69	O6A1t	0.00	0.00	63	0.02
70	O3Ap	-	-	-	-
71	O7Ap	-	-	-	-
72	T1Atad	0.08	0.00	172	0.07
73	T2A1t	0.35	0.08	449	0.17
74	T1A1t	0.05	0.03	163	0.02
75	t1A2t	0.08	0.00	163	0.02
76	T3At	0.17	0.03	151	0.05
77	T3A2t	0.08	0.02	151	0.10
78	Q5Dtd	0.67	0.48	532	1.85
79	Q5D1td	0.60	0.37	565	2.13
80	Q7Dtd	1.08	0.42	524	2.60
81	Q6Dtd	0.87	0.43	533	2.08
82	Q5D2td	0.72	0.37	528	2.15
83	Q4A5ta	-	-	-	-
84	Q15atad	1.55	0.60	336	3.03
85	Q22Atad	1.88	0.65	287	4.70
86	Q22A2tad	1.63	0.67	290	3.70
87	Q11Ata	0.42	0.20	110	0.90
88	Q11Ao	0.05	0.00	7	0.02
89	Q22A3tad	1.93	0.52	348	4.17
90	Q22A4tad	2.35	0.62	214	3.10
91	Q22A5tad	1.38	0.42	309	3.82
92	O3A1t	-	-	-	-
93	N9At	0.55	0.35	460	5.85
94	O38Aa	0.05	0.00	1	0.00
95	C18At	-	-	-	-
96	C18A1t	4.08	1.08	439	6.62
97	Q18A2t	-	-	-	-

Figure 1.18
SPICE2 with bypass using the fort compiler, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
98	N4Ada	0.02	0.03	58	0.20
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	-	-	-	-
102	C19Mt	-	-	-	-
103	C68Dt	24.73	9.33	1258	137.28
104	C9Ao	-	-	-	-
105	C82Dt	-	-	-	-
106	C2At	0.03	0.02	114	0.57
107	C37Dt	-	-	-	-
108	N27At	0.50	0.25	201	7.03
109	N698Dt	141.72	48.63	2360	1165.93
110	Q6At	28.73	17.93	41862	170.03
111	C7Atd	0.32	0.20	233	3.03
112	C52Aa	-	-	-	-
113	Q340t	4562.23	361.58	3463	892.88
114	C54Dt	-	-	-	-
115	N1190Mt	-	-	-	-
116	C31Dt	-	-	-	-
117	Q2A1t	215.57	106.42	230795	389.23
118	C119At	-	-	-	-
119	C6Dt	0.15	0.03	166	2.02
120	Q2A2t	0.57	0.33	1765	3.23
121	Q6A1t	0.95	0.27	1248	5.73
122	Q4A4ta	-	-	-	-
123	O4Ao	-	-	-	-
124	H44Aa	-	-	-	-
125	Q10Ao	0.30	0.07	36	0.07
126	C77Mt	-	-	-	-
127	Q4Af	0.02	0.00	8	0.02
128	N2Aa	0.00	0.00	5	0.00
129	N1Ad	0.00	0.02	69	0.13
130	O5A2t	0.00	0.03	64	0.02
131	O2At	0.02	0.00	56	0.00
132	O2A2t	0.00	0.02	59	0.02
133	C205At	-	-	-	-
134	T2A2t	0.07	0.03	85	0.08
135	C26At	-	-	-	-
136	N1At	0.00	0.02	62	0.12
137	C37At	-	-	-	-
138	N3At	-	-	-	-
139	C6D1t	-	-	-	-
140	Q86Aa	2.57	0.13	8	0.25
141	C640Dt	-	-	-	-
142	C1060Mt	-	-	-	-
143	Q14Ao	0.17	0.03	13	0.07
144	C28Dt	-	-	-	-
145	C23Dt	-	-	-	-
146	O20At	-	-	-	-

Figure 1.18
SPICE2 with bypass using the fort compiler, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Matrix solve time	Number of matrix solves	Total load time
147	C277Mt	51.43	19.07	2523	485.15
148	C277M2t	77.98	30.77	3735	998.10
149	C42Dt	-	-	-	-
150	C7Ad	-	-	-	-
151	C14D1t	-	-	-	-
152	Q84At	225.35	84.60	2241	280.45
153	Q50A1t	17.58	7.03	1604	52.07
154	O20A1t	0.78	0.37	794	1.12
113	total	5432.35	717.54	315432	4944.35
	average	48.07	6.35	2791	43.76

1.3.8. Industrial Simulator on a VAX 8800

Figure 1.19
Industrial Circuit Simulator running on a VAX 8800, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
1	Q180Do	14.50	46	0	315.22
2	Q180D2o	13.73	46	0	298.48
3	Q2At	4.32	1139	1129	3.79
4	O9Aa	1.70	2	0	850.00
5	O1024Ao	-	-	-	-
6	N48Dt	34.97	810	795	43.17
7	N5At	-	-	-	-
8	N5A2t	-	-	-	-
9	O10At	-	-	-	-
10	Q6Ao	1.03	13	0	79.23
11	Q6A2o	-	-	-	-
12	Q4Ao	1.07	7	0	152.86
13	N1Aot	-	-	-	-
14	N1A2ot	-	-	-	-
15	N1A3ot	-	-	-	-
16	O8At	2.67	518	518	5.15
17	Q1Ado	-	-	-	-
18	Q1A2t	1.88	210	201	8.95
19	Q5Atd	4.62	299	286	15.45
20	C25Ao	-	-	-	-
21	C27Ao	-	-	-	-
22	C7Ao	-	-	-	-
23	C4Dto	3.15	503	495	6.26
24	C22Dt	10.33	258	246	40.04
25	C22D2o	1.92	13	0	147.69
26	T2At	2.12	220	218	9.64
27	Q7Ao	1.07	13	0	82.31
28	N116Dt	-	-	-	-
29	N2Dod	-	-	-	-
30	Q4At	2.50	217	209	11.52
31	Q8Atd	-	-	-	-
32	Q4A1t	3.13	311	303	10.06
33	C4D1to	-	-	-	-
34	Q4a2t	2.02	175	166	11.54
35	Q10At	16.23	426	414	38.10
36	O3At	1.07	186	184	5.75
37	N10Dto	-	-	-	-
38	N10D2to	-	-	-	-
39	N10Ato	-	-	-	-
40	N1A4d	-	-	-	-
41	Q7Aat	-	-	-	-
42	Q3At	-	-	-	-
43	O15ata	-	-	-	-
44	Q11atd	-	-	-	-
45	O5At	-	-	-	-
46	N27Aaod	-	-	-	-

Figure 1.19
Industrial Circuit Simulator running on a VAX 8800, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
47	N27A2t	-	-	-	-
48	N27A3o	-	-	-	-
49	N27A4o	-	-	-	-
50	N27A5o	-	-	-	-
51	N27A6aod	-	-	-	-
52	N12At	4.77	357	347	13.36
53	N8Ao	-	-	-	-
54	N2Ao	1.12	10	0	112.00
55	O6At	1.77	182	180	9.73
56	N1A5d	-	-	-	-
57	N6At	5.18	379	376	13.67
58	Q11Atad	-	-	-	-
59	Q5Ao	0.98	15	0	65.33
60	Q2Dtd	-	-	-	-
61	O66At	8.72	705	688	12.37
62	N2Dtdo	-	-	-	-
63	Q8Dtd	-	-	-	-
64	Q4A3t	3.60	391	383	9.21
65	Q50At	66.67	1994	1958	33.44
66	O5A1t	1.93	258	256	7.48
67	C38Da	-	-	-	-
68	C38D2a	-	-	-	-
69	O6A1t	1.03	202	200	5.10
70	O3Ap	-	-	-	-
71	O7Ap	-	-	-	-
72	T1Atad	-	-	-	-
73	T2A1t	2.12	420	418	5.05
74	T1A1t	-	-	-	-
75	t1A2t	1.55	362	362	4.28
76	T3At	-	-	-	-
77	T3A2t	-	-	-	-
78	Q5Dtd	-	-	-	-
79	Q5D1td	-	-	-	-
80	Q7Dtd	-	-	-	-
81	Q6Dtd	-	-	-	-
82	Q5D2td	-	-	-	-
83	Q4A5ta	-	-	-	-
84	Q15atad	-	-	-	-
85	Q22Atad	-	-	-	-
86	Q22A2tad	-	-	-	-
87	Q11Ata	-	-	-	-
88	Q11Ao	1.38	8	0	172.50
89	Q22A3tad	-	-	-	-
90	Q22A4tad	-	-	-	-
91	Q22A5tad	-	-	-	-
92	O3A1t	-	-	-	-
93	N9At	6.07	326	296	18.62
94	O38Aa	1.67	2	0	835.00
95	C18At	12.12	549	520	22.08

Figure 1.19
Industrial Circuit Simulator running on a VAX 8800, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
96	C18A1t	11.18	508	464	22.01
97	Q18A2t	10.98	503	461	21.83
98	N4Ada	2.57	80	0	32.13
99	C14Dt	-	-	-	-
100	N804Dt	-	-	-	-
101	T1At	1.08	166	164	6.51
102	C19Mt	-	-	-	-
103	C68Dt	313.92	4675	4667	67.15
104	C9Ao	-	-	-	-
105	C82Dt	-	-	-	-
106	C2At	1.48	145	140	10.21
107	C37Dt	-	-	-	-
108	N27At	16.22	657	644	24.69
109	N698Dt	-	-	-	-
110	Q6At	248.37	58527	58516	4.24
111	C7Atd	6.18	212	189	29.15
112	C52Aa	-	-	-	-
113	Q340t	-	-	-	-
114	C54Dt	-	-	-	-
115	N1190Mt	-	-	-	-
116	C31Dt	-	-	-	-
117	Q2A1t	-	-	-	-
118	C119At	-	-	-	-
119	C6Dt	4.03	287	282	14.04
120	Q2A2t	-	-	-	-
121	Q6A1t	-	-	-	-
122	Q4A4ta	9.38	5	0	1876.00
123	O4Ao	-	-	-	-
124	H44Aa	-	-	-	-
125	Q10Ao	-	-	-	-
126	C77Mt	-	-	-	-
127	Q4Af	0.93	9	0	103.33
128	N2Aa	1.22	15	0	81.33
129	N1Ad	-	-	-	-
130	O5A2t	1.10	128	126	8.59
131	O2At	-	-	-	-
132	O2A2t	0.93	111	108	8.38
133	C205At	-	-	-	-
134	T2A2t	4.88	2002	2000	2.44
135	C26At	-	-	-	-
136	N1At	1.42	114	111	12.46
137	C37At	-	-	-	-
138	N3At	-	-	-	-
139	C6D1t	2.27	178	151	12.75
140	Q86Aa	10.77	9	0	1196.67
141	C640Dt	-	-	-	-
142	C1060Mt	-	-	-	-
143	Q14Ao	1.63	14	0	116.43
144	C28Dt	-	-	-	-

Figure 1.19
Industrial Circuit Simulator running on a VAX 8800, part 1

Circuit number	Circuit name	Total CPU time	Total iterations	Transient iterations	Total CPU per iteration (msec)
145	C23Dt	-	-	-	-
146	O20At	-	-	-	-
147	C277Mt	-	-	-	-
148	C277M2t	-	-	-	-
149	C42Dt	-	-	-	-
150	C7Ad	-	-	-	-
151	C14D1t	21.88	1079	1079	20.28
152	Q84At	-	-	-	-
153	Q50A1t	-	-	-	-
154	O20A1t	-	-	-	-
57	total	917.13	80996	80250	
	average	16.09	1420	1407	11.32

Figure 1.20
Industrial Circuit Simulator running on a VAX 8800, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Total load time
1	Q180Do	0.00	2.05
2	Q180D2o	1.48	2.13
3	Q2At	0.52	0.97
4	O9Aa	0.00	0.00
5	O1024Ao	-	-
6	N48Dt	1.03	29.65
7	N5At	-	-
8	N5A2t	-	-
9	O10At	-	-
10	Q6Ao	0.00	0.03
11	Q6A2o	-	-
12	Q4Ao	0.00	0.00
13	N1Aot	-	-
14	N1A2ot	-	-
15	N1A3ot	-	-
16	O8At	0.03	0.38
17	Q1Ado	-	-
18	Q1A2t	0.03	0.08
19	Q5Atd	0.03	0.77
20	C25Ao	-	-
21	C27Ao	-	-
22	C7Ao	-	-
23	C4Dto	0.08	1.47
24	C22Dt	0.60	4.62
25	C22D2o	0.05	0.12
26	T2At	0.00	0.02
27	Q7Ao	0.02	0.02
28	N116Dt	-	-
29	N2Dod	-	-
30	Q4At	0.08	0.40
31	Q8Atd	-	-
32	Q4A1t	0.15	0.65
33	C4D1to	-	-
34	Q4a2t	0.03	0.23
35	Q10At	0.00	4.70
36	O3At	0.00	0.03
37	N10Dto	-	-
38	N10D2to	-	-
39	N10Ato	-	-
40	N1A4d	-	-
41	Q7Aat	-	-
42	Q3At	-	-
43	O15ata	-	-
44	Q11atd	-	-
45	O5At	-	-
46	N27Aaod	-	-
47	N27A2t	-	-
48	N27A3o	-	-

Figure 1.20
Industrial Circuit Simulator running on a VAX 8800, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Total load time
49	N27A4o	-	-
50	N27A5o	-	-
51	N27A6aod	-	-
52	N12At	0.07	1.75
53	N8Ao	-	-
54	N2Ao	0.02	0.03
55	O6At	0.03	0.02
56	N1A5d	-	-
57	N6At	0.10	1.48
58	Q11Atad	-	-
59	Q5Ao	0.00	0.03
60	Q2Dtd	-	-
61	O66At	1.52	1.32
62	N2Dtdo	-	-
63	Q8Dtd	-	-
64	Q4A3t	0.13	0.67
65	Q50At	12.33	42.18
66	O5A1t	0.02	0.05
67	C38Da	-	-
68	C38D2a	-	-
69	O6A1t	0.02	0.05
70	O3Ap	-	-
71	O7Ap	-	-
72	T1Atad	-	-
73	T2A1t	0.13	0.10
74	T1A1t	-	-
75	t1A2t	0.07	0.10
76	T3At	-	-
77	T3A2t	-	-
78	Q5Dtd	-	-
79	Q5D1td	-	-
80	Q7Dtd	-	-
81	Q6Dtd	-	-
82	Q5D2td	-	-
83	Q4A5ta	-	-
84	Q15atad	-	-
85	Q22Atad	-	-
86	Q22A2tad	-	-
87	Q11Ata	-	-
88	Q11Ao	0.02	0.00
89	Q22A3tad	-	-
90	Q22A4tad	-	-
91	Q22A5tad	-	-
92	O3A1t	-	-
93	N9At	0.18	2.75
94	O38Aa	0.00	0.00
95	C18At	1.73	6.07
96	C18A1t	1.77	5.42
97	Q18A2t	1.67	5.32

Figure 1.20
Industrial Circuit Simulator running on a VAX 8800, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Total load time
98	N4Ada	0.03	0.25
99	C14Dt	-	-
100	N804Dt	-	-
101	T1At	0.07	0.02
102	C19Mt	-	-
103	C68Dt	42.48	247.57
104	C9Ao	-	-
105	C82Dt	-	-
106	C2At	0.00	0.28
107	C37Dt	-	-
108	N27At	0.68	12.05
109	N698Dt	-	-
110	Q6At	28.73	159.67
111	C7Atd	0.15	1.27
112	C52Aa	-	-
113	Q340t	-	-
114	C54Dt	-	-
115	N1190Mt	-	-
116	C31Dt	-	-
117	Q2A1t	-	-
118	C119At	-	-
119	C6Dt	0.02	1.57
120	Q2A2t	-	-
121	Q6A1t	-	-
122	Q4A4ta	0.00	0.02
123	O4Ao	-	-
124	H44Aa	-	-
125	Q10Ao	-	-
126	C77Mt	-	-
127	Q4Af	0.00	0.03
128	N2Aa	0.00	0.03
129	N1Ad	-	-
130	O5A2t	0.02	0.00
131	O2At	-	-
132	O2A2t	0.00	0.00
133	C205At	-	-
134	T2A2t	0.77	0.57
135	C26At	-	-
136	N1At	0.02	0.17
137	C37At	-	-
138	N3At	-	-
139	C6D1t	0.08	0.67
140	Q86Aa	0.22	0.27
141	C640Dt	-	-
142	C1060Mt	-	-
143	Q14Ao	0.05	0.08
144	C28Dt	-	-
145	C23Dt	-	-
146	O20At	-	-

Figure 1.20
Industrial Circuit Simulator running on a VAX 8800, part 2

Circuit number	Circuit name	Total reorder and LU decomposition time	Total load time
147	C277Mt	-	-
148	C277M2t	-	-
149	C42Dt	-	-
150	C7Ad	-	-
151	C14D1t	2.15	15.57
152	Q84At	-	-
153	Q50A1t	-	-
154	O20A1t	-	-
57	total	99.41	555.75
	average	1.74	9.75