PLANAR MULTILEVEL METALLIZATION USING ADDITIVE PATTERN TRANSFER

by

Don E. Lyons

Memorandum No. UCB/ERL M89/75

19 June 1989

PLANAR MULTILEVEL METALLIZATION USING ADDITIVE PATTERN TRANSFER

by

Don E. Lyons

Memorandum No. UCB/ERL M89/75

19 June 1989

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

PLANAR MULTILEVEL METALLIZATION USING ADDITIVE PATTERN TRANSFER

by

Don E. Lyons

Memorandum No. UCB/ERL M89/75

19 June 1989

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

Planar Multilevel Metallization Using Additive Pattern Transfer

Don E. Lyons

ABSTRACT

This report investigates the use of evaporation and a high resolution liftoff process to achieve planar metallization structures. Features are initially defined in a dielectric and filled by evaporation, with the undesired material removed by liftoff. Important features of this process were notch formation during deposition due to shadowing, and etchback of the metal film during the liftoff process. The relationship between sidewall angle and deposition system geometry and the effect on notching is explored using simple geometrical modeling and simulation using the SAMPLE program. A suitable process window was found where notching could be avoided. The process was then evaluated experimentally using an e-beam evaporation system. The metal etchback during liftoff was found to be difficult to control. A post-liftoff dip was used to correct this effect. Within the process window predicted by simulation, 3.0 μm pitch metal lines and spaces were fabricated with a planar final profile.

Dedicated with love to my brother John

Acknowledgments

Many people have offered assistance and support during the course of this project. Professor William G. Oldham, as my research advisor, should be thanked first for giving me the opportunity to work in this area and for his experience and ideas throughout my time here. I would also like to thank Professor Andy R. Neureuther for his interest and assistance with cooperative projects. I was very fortunate as well to work with visiting scholar Yosi Y. Shacham-Diamand and benefit from his energy and experience.

My fellow students have been of invaluable assistance to me here at Berkeley. Gino Addiego has given me a wealth of assistance in a variety of areas. Carl Galewski has been a considerable help in the lab. Pei-Lin Pai gave me my initial exposure to the processing lab and to additive pattern transfer. Pantas Sutardja provided excellent computer tools and expertise. Kenny Toh, Alex Wong, Ed Scheckler, Nelson Tam and Sherman Kwok, along with numerous others, have been helpful as well. A special thanks goes to Bill Partlo, Dean Drako, Alisa Scherer, and Dr. Christopher Spence for their friendship and support.

The staff of the UC Berkeley Microlab have been of tremendous help. Tom Booth taught me how to operate every piece of equipment I ever needed to use. James Parrish, Phil Guillery, Steve Hoagland and Robert Norman helped me with various equipment challenges that I faced. Sam Higginbotham, Jose Rivera and the rest of the machine shop staff have displayed tremendous patience with my poor mechanical design skills.

I would also like to thank my family, who have supported me with their encouragement and love throughout my academic career.

Table of Contents

Chapter 1. Introduction

A limiting factor in the increasing density of integrated circuits is the area devoted to device interconnections. One way to more densely pack interconnections is to expand the IC into the third dimension, i.e. use multiple layers of interconnections. Multilevel metallization has not been an easily accomplished goal, however.

Conventional metallization processes are subtractive, meaning a layer of metal is deposited, photoresist is applied and patterned, and the metal etched (subtracted) away to define the conducting lines. A dielectric is then deposited on top of the metal. Using a process such as this introduces steps and other topography on the surface, however. The situation becomes worse with each subsequent layer, making more than just a few layers very difficult without complex planarizing steps in between layers.

Additive processing is an alternative that offers more potential. In this type of processing the dielectric material is deposited first and trenches are etched into the surface where conducting lines or vias are desired. Metal is then added in these pre-defined features, with no steps or other topography introduced. An arbitrary number of interconnect levels is then theoretically possible with a reliable additive technology.

Several examples of additive technologies already exist. Liftoff can be considered an additive technology because pattern definition is done previous to film deposition and no etching is required [1]. Selective deposition techniques offer additional promise as additive processes. Chemical vapor deposition of tungsten can be made to selectively deposit on silicon or tungsten and not on silicon dioxide [2,3]. Electroless plating is a process that can be used to selectively plate on a conducting material and not on a dielectric material [3,4,5]. Additive technologies such as these have already been explored as ways to fill vias and contacts. A process that is modular and that could be used for both vias and interconnect

layers would be a good potential multilevel metallization process.

This report investigates a possible approach to additive processing using evaporation and liftoff to fill predefined features. For this scheme, the process window is first explored using simulation and simple geometrical modeling. The process is then evaluated experimentally using an e-gun evaporation system.

Chapter 2. Directional Evaporation and Liftoff to Fill Predefined Features

One example of additive pattern transfer that can be easily implemented is liftoff. This technology has already been used to produce multiple layer metallization processes [7]. As interconnect dimensions are gradually reduced, higher resolution liftoff processes become necessary. This work focuses on an in-depth analysis of the LOPED [8] process and it's application towards producing embedded conducting wires and vias in a dielectric.

Process Flow

A simple process flow was designed to test the potential of this liftoff scheme to planar metallization. This process is shown schematically in figure 1. First, a thick layer of silicon dioxide is grown. A layer of photoresist is then applied and patterned and used as a mask to etch features into the oxide dielectric. The resist is retained to act as a liftoff medium. A metal deposition step follows this. The first step of the liftoff process is to spin on a second sacrificial layer of photoresist. Shrinkage of this polymer causes the coverage at the edges of features to be thinner. This fact can be taken advantage of by performing a partial isotropic etchback of the resist to expose, or detect, the underlying metal edges. These metal edges are then etched out isotropically to expose the underlying patterned (liftoff) resist. The liftoff resist is then exposed to a solvent and washed out, lifting off the undesired metal.

Modeling the Deposition

To fill predefined features on a wafer material incident upon the wafer (during physical vapor deposition) should arrive at normal or near normal incidence to the wafer surface. If a significant portion of the incident material arrives at a feature at large angles from normal to the wafer surface, then the sides of the predefined feature will shadow a significant portion of this incident material. Topography will be generated in the form of notches at the

edges of the feature where shadowing occurred. It is possible to accomplish nearly normal incidence deposition with evaporation from a very small source (such as an e-gun evaporator). A diagram depicting this situation is shown in figure 2, where a single wafer is held suspended above an e-gun source.

Several different deposition cases can be observed for features at differing locations on the wafer, as shown in figure 2. For features directly above or nearly directly above the wafer, the feature can be filled by evaporation with some sidewall coverage. The sidewall coverage may be thicker on one side of the feature however. For features far from directly above the source, the angle of deposition is large and two phenomenon occur. The feature is shadowed on one side and a notch is formed during deposition. On the other side of the feature, the sidewall coverage is very thick, compared to elsewhere on the wafer. This analysis is based on a stationary wafer and source.

Shadowing and notch formation begin to occur when the angle of deposition is greater than the angle the sidewall makes with the wafer normal. This can be seen in the leftmost feature of figure 2. The evaporant path from the source is clearly seen to be shadowed from the bottom of the feature. Immediately, trade-offs between various parameters become evident.

To increase the range of deposition angles that allow smooth, continuous deposition, the sidewall angle must be considered. A negative sidewall slope (where the opening at the top of the feature is narrower than at the base of the feature) would shadow the deposition more so than a positive sidewall slope (where the top of the feature is wider than the base). A greater amount of positive sidewall slope (a smaller sidewall angle relative to the wafer surface) broadens the range of deposition angles that gives a notch free film deposition. The amount of sidewall slope possible is limited by packing density issues however.

Along with decreasing the sidewall angle, shadowing can be reduced by decreasing the angle of deposition. As can be seen in figure 3, this can be brought on by increasing

the source to wafer separation (z) or by reducing the equivalent source size (s). The maximum angle of deposition (for no shadowing) is:

$$\theta_{max} = \arctan\left(\frac{r + \frac{s}{2}}{z}\right)$$

This relationship can be used to describe the process window for non-shadowed deposition. Figure 4 shows, for a fixed sidewall angle of 80° with respect to the wafer surface, the allowable range of source size and separation from the wafer. Three areas are shown in this figure, corresponding to the parameter range for a single 2" wafer, 4" wafer and 6" wafer. It can be seen that the ideal (non-shadowed) situation has a weak dependence on source size for small sources and a relatively strong dependence on separation distance. This relationship can be used to determine the dependence on sidewall angle as well. Figure 5 shows the necessary relationship between source size and separation distance for three different sidewall angles (to guarantee no shadowing for a 4" wafer). A strong dependence on sidewall angle is predicted by this analysis.

It is possible to extend the process window for deposition if some shadowing and notch formation is considered allowable. To predict the deposition topography in this case, more complex analysis is necessary. Various physical vapor deposition models are available in the process simulation program SAMPLE, including one for simple evaporation [9]. For evaporation from a small source onto a stationary feature, the hemispherical source model is appropriate. Using this model the input parameters to SAMPLE are the initial profile, the time and rate of the deposition, and the maximum and minimum angles of deposition, as defined in figure 3. The feature is assumed to be very small relative to the source for calculation of these angles.

The numerical algorithms in SAMPLE can then be used to obtain final deposited profiles. In figure 6, example simulation results are given for a feature directly above the

source (a) and also for a feature near the perimeter of a wafer -- past the onset point of shadowing (b). A more detailed understanding of the effects of source size and radial position can be obtained using simulation results for a variety of different situations. Figure 7 presents the type of information obtained. The notch depth, as a fraction of the metal film thickness, is graphed as a function of source size (a) and radial position on the wafer (b). To learn how much the process window is expanded by allowing some notch formation, the data in figure 7 can be used to determine the relationship between source size and separation for a selected wafer size, wall angle and amount of notch formation allowed. In figure 8, the enlarged process window is graphed for an allowable notch formation of 40% of the metal film thickness (with the wall angle set at 80°). The dotted lines in this figure correspond to the process window for no shadowing allowed. Approximately a 6.4% increase in the process window is observed when this 40% notch formation is viewed as tolerable.

Another consideration during the deposition is the uniformity of the deposited film across the wafer. If the sidewall angles are lowered to expand the process window (as suggested by figure 5) and allow a much shorter source to wafer separation, then the uniformity across the wafer will degrade. Using a standard cosine distribution for evaporation from a small source allows an understanding of this constraint. In figure 9 the situation for a 6" wafer is plotted. The spacing between wafer and source can be reduced but only at the cost of the coating uniformity.

Modeling Liftoff

The liftoff used in this process (LOPED) involves two etchback steps, one in a sacrificial resist and the other through the deposited metal. Using the nonplanar etchback capability of SAMPLE [10] it is possible to simulate these process steps along with the deposition. The metal etchback step is particularly critical because it not only is used to expose the liftoff mask, but it has a critical effect on the final topography.

The initial profile is taken from the output of the SAMPLE deposition simulation. The second, sacrificial resist is applied using an exponential calculation based on typical observed spin-on profiles [11]. A profile showing the resist etchback step is presented in figure 10. The simulation is continued with the metal etchback, which is shown in figure 11. For this application of the LOPED process, the metal and resist etchback steps must be carefully controlled to achieve a smooth final profile.

Experimental System and Results

To provide experimental verification of this process, an e-gun evaporation system was used. A schematic of this system is shown in figure 12. A single 4" wafer is suspended 25 cm. above the e-gun crucible, which has an approximate spot size of 5 mm. A crystal thickness monitor and shutter are included to carefully control the deposited film thickness.

For these experiments, a 1.0 μm SiO_2 film was thermally grown on (100) 4" silicon wafers. KTI 820 photoresist was spun on and patterned using a GCA-Mann step and repeat aligner. A LAM fluorine-based plasma etching system was used to transfer the patterns into the oxide. Aluminum was then deposited in the aforementioned e-gun evaporation system. AZ 1400-21 photoresist was used as the second resist. It was spun to a thickness of 6000 A and etched back to approximately 1000 A in a Technics oxide plasma etching system. The aluminum etchback was performed using an etchant based on heated phosphoric acid. Liftoff was accomplished in acetone using ultrasonic agitation.

The goal of the experiments was to confirm the feasibility of the process and compare results with the model and simulation. Qualitative analysis using scanning electron micrographs was used to gauge performance of the process.

Initial experiments were performed to explore the process window for notch-free deposition. Micrographs are presented in figure 13 for different deposition situations. In figure 13 (a), a symmetric deposition is shown for a feature nearly directly above the source. Fig-

ure 13 (b) shows a notched deposition where the notch (on the left) reaches halfway into the deposited film. The film is continuous for a region encircling the point directly above the evaporation source. The approximate radius for this region is 3 cm. Using the geometrical relationship between source size, radial position and source to wafer separation, this corresponds to sidewalls of 82.5°, which is approximately what is observed on the samples studied.

Controlling the metal etchback step during this process is difficult. There is no in-process monitor during this step to get feedback and no etchstop either. A timed etch was used initially. Typical results for this approach are shown in figure 14. For this case, both edges are left rough with small spikes protruding upwards. A way to correct this situation is to perform a post-liftoff dip to etch away the spikes. A slight overfill of the feature is done during the deposition to account for the amount of metal etched off. Figure 15 shows a profile view before and after this short etch. The improvement is significant, but not without cost. The etch is accelerated at the metal/oxide interface and thus cracks form at each side of every feature. This could be a problem with overlay of vias, requiring widened via pads for vias to align to, to avoid the possible positioning of a via over the edge crack. This etch step leaves the features across the die looking very similar. A series of features from four dies across a wafer (center to edge) is shown in figure 16. It is possible to avoid this problem of accelerated etching at the interface by performing an anneal (400°C in N_2/10% H_2. Figure 17 shows a sample that had an anneal prior to the etchback step. A notch from shadowing is evident on the left side of the line, but the etching was not accelerated at either edge.

Features that have edges in both directions along the wafer are shown in figure 18. No difference is seen for edges running in either direction, as would be expected. Note, this sample was not annealed before the final dip to remove edge roughness.

Conclusions

This liftoff process was explored using simulation and an experimental evaporation system. Using simple geometrical relationships, an idea of the operating window was obtained. With the program SAMPLE is was possible to obtain simulated profiles that accurately predicted the effects of shadowing. Actual experiments verified the approximate process window calculations. Also, a post liftoff dip to remove edge roughness was explored. With this technique it was possible to overcome some of the edge roughness that resulted from the loped metal corner etch, which was difficult to control and make uniform.

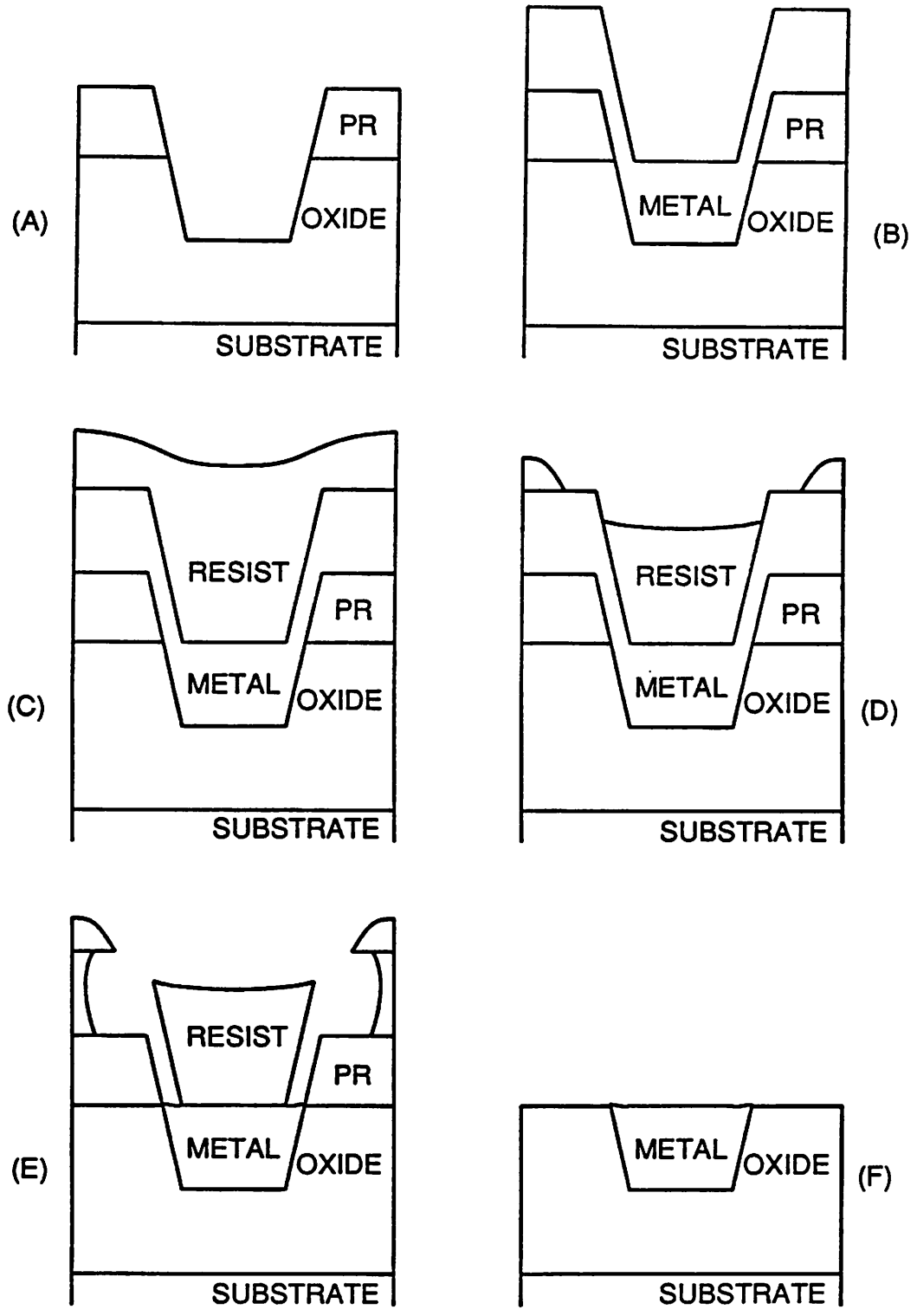


Figure 1. Evaporation and liftoff process flow. The process steps are: (A) pattern definition, (B) metal deposition, (C) second resist application, (D) resist etchback to expose metal edges, (E) metal etchback to expose photoresist mask, and (F) resulting final profile.

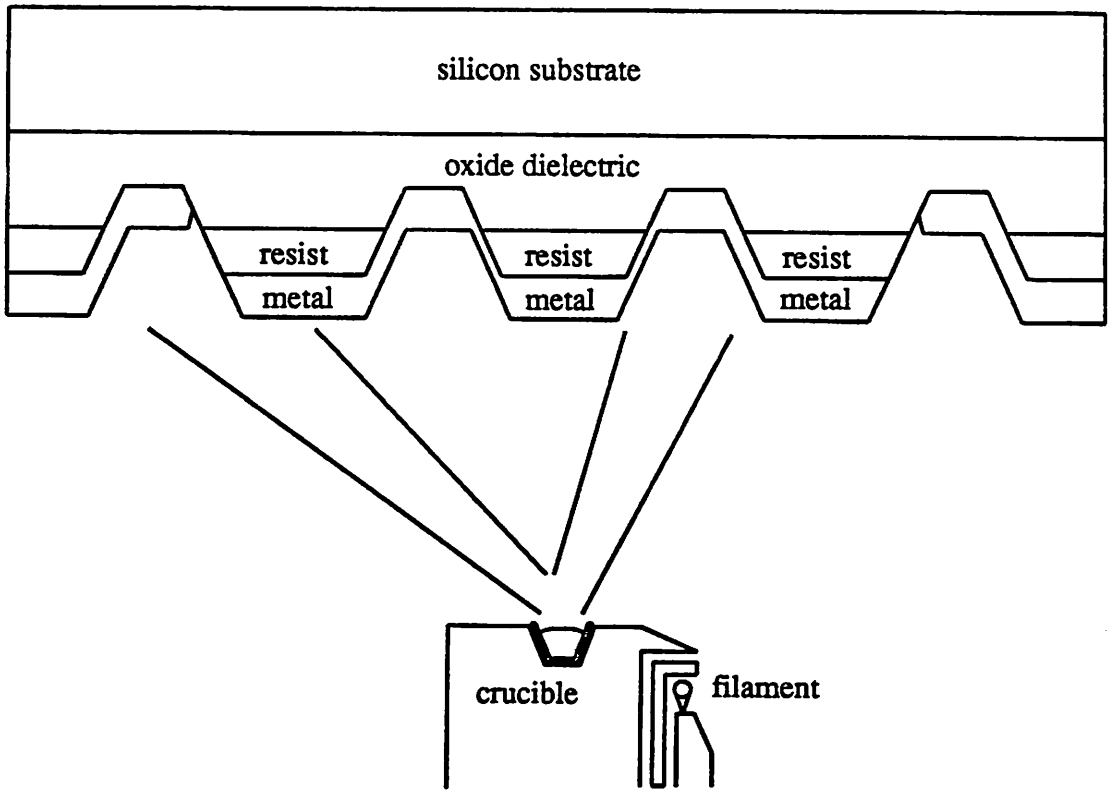


Figure 2. Deposition situations for a wafer suspended above an e-gun evaporator.

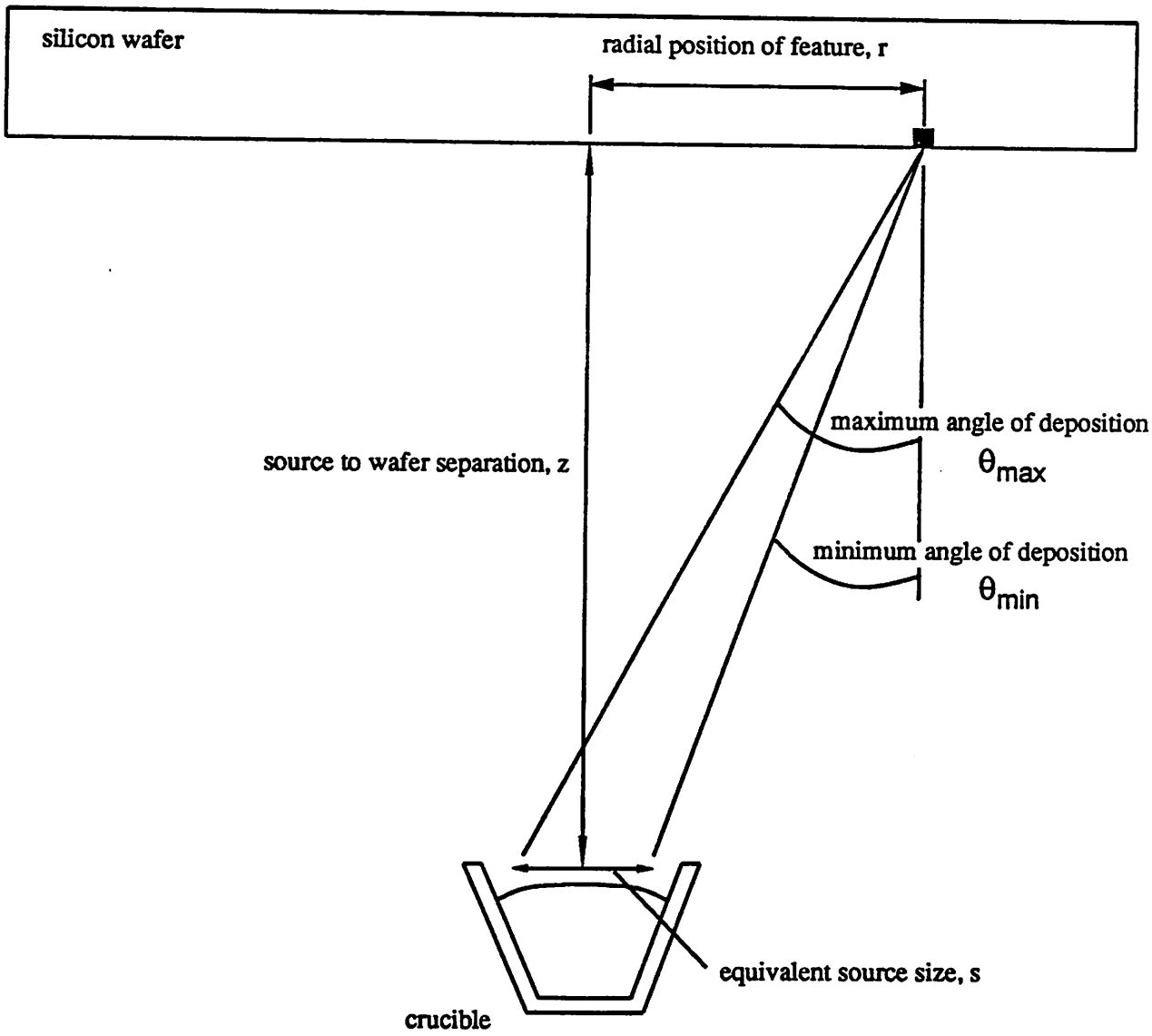


Figure 3. Evaporation model for a feature at a particular position on wafer.

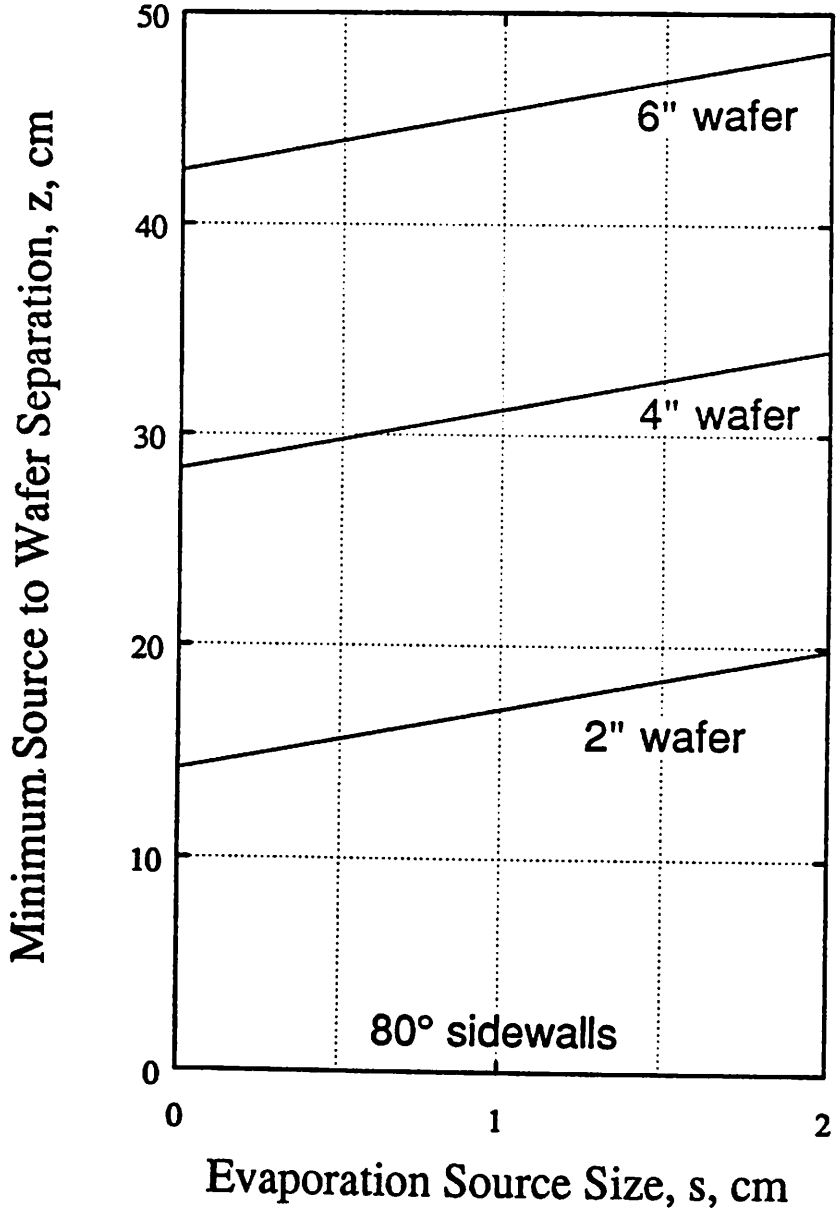


Figure 4. Process window for non-shadowed deposition based on geometrical analysis of evaporation system.

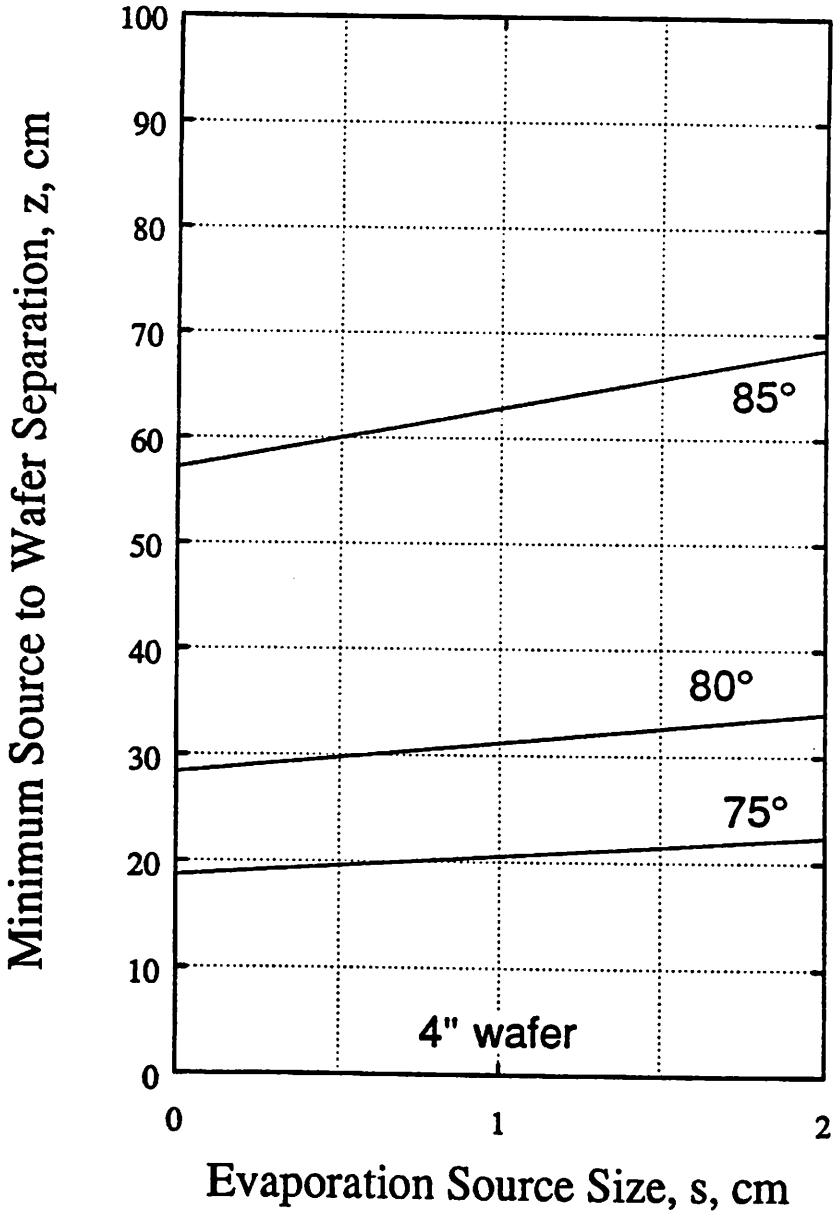
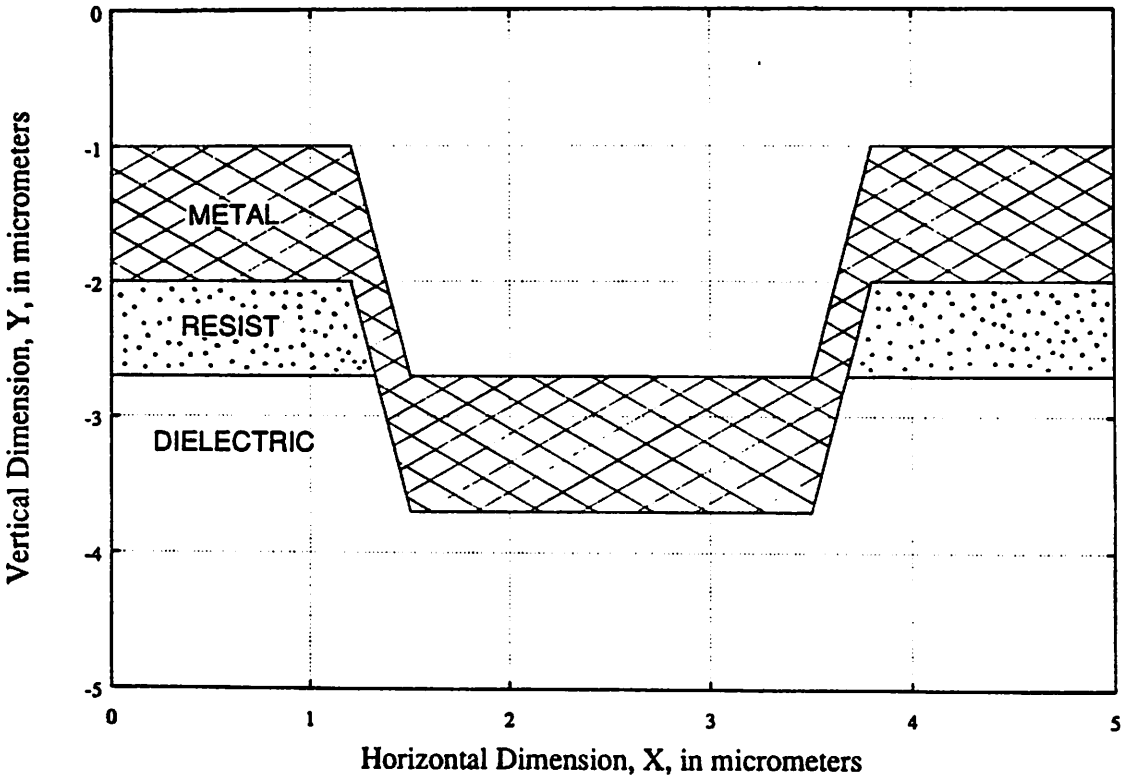


Figure 5. Process window for non-shadowed deposition for three different sidewall angles.

(A)



(B)

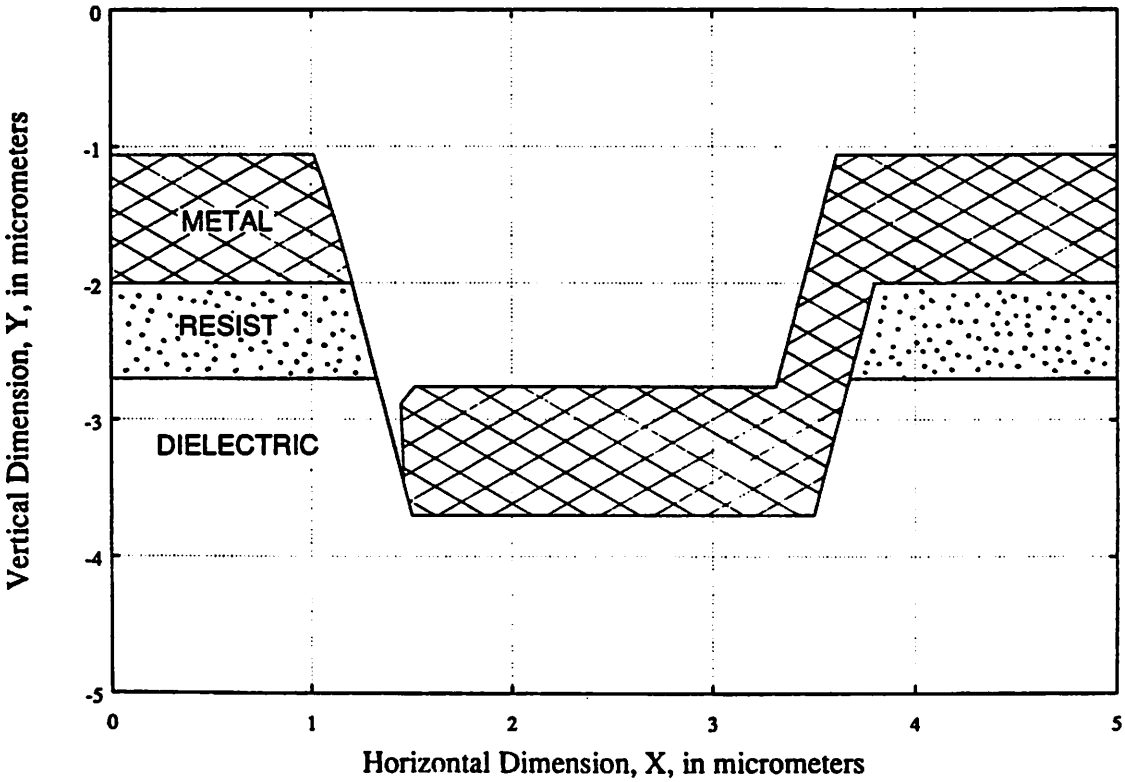
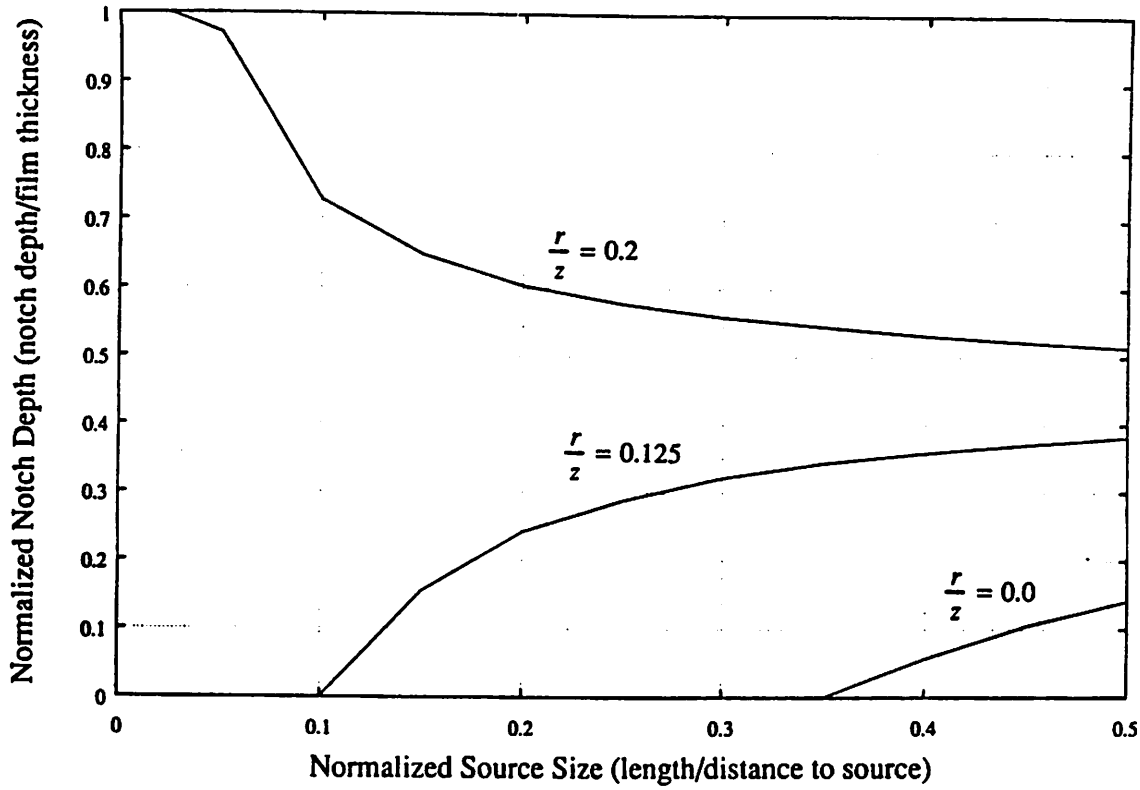


Figure 6. Simulated profiles from the SAMPLE program. Two situations are presented: (A) feature directly above source and (B) feature past the onset point of shadowed deposition.

(A)



(B)

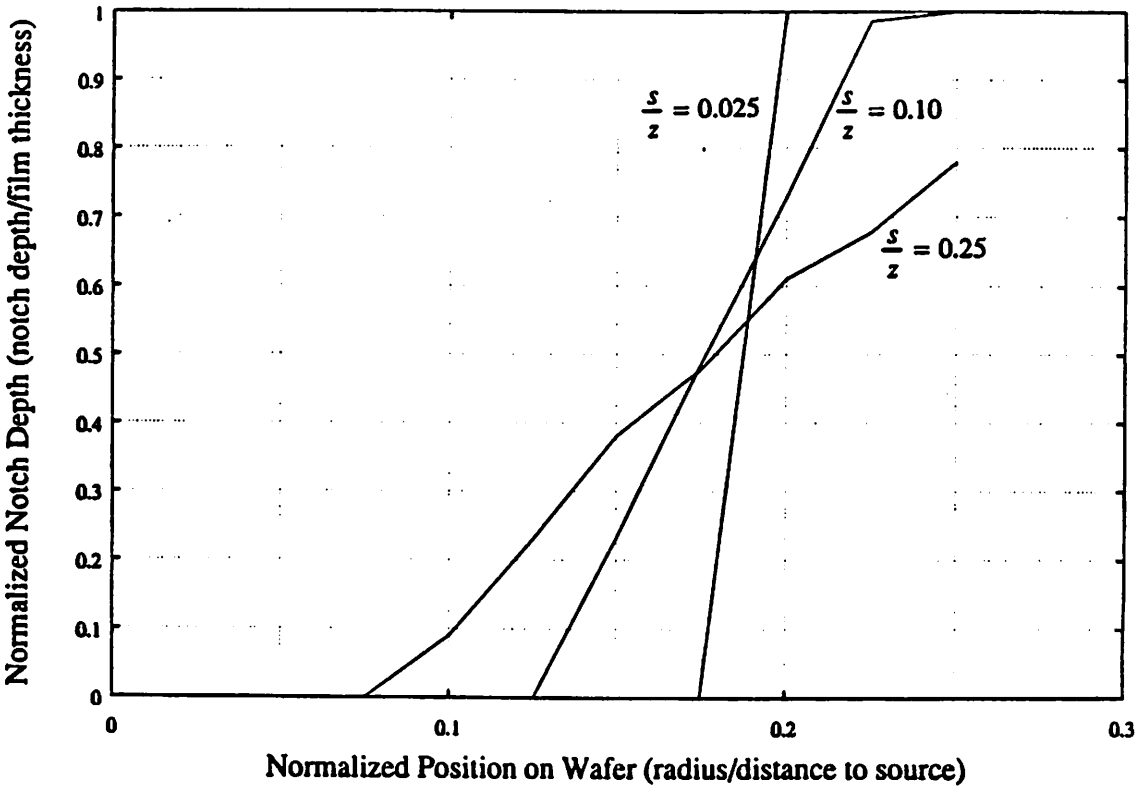


Figure 7. Notch depth observed from SAMPLE simulations. Notch depth is plotted as a function of (A) source size and (B) radial position. Sidewall angle is 80°.

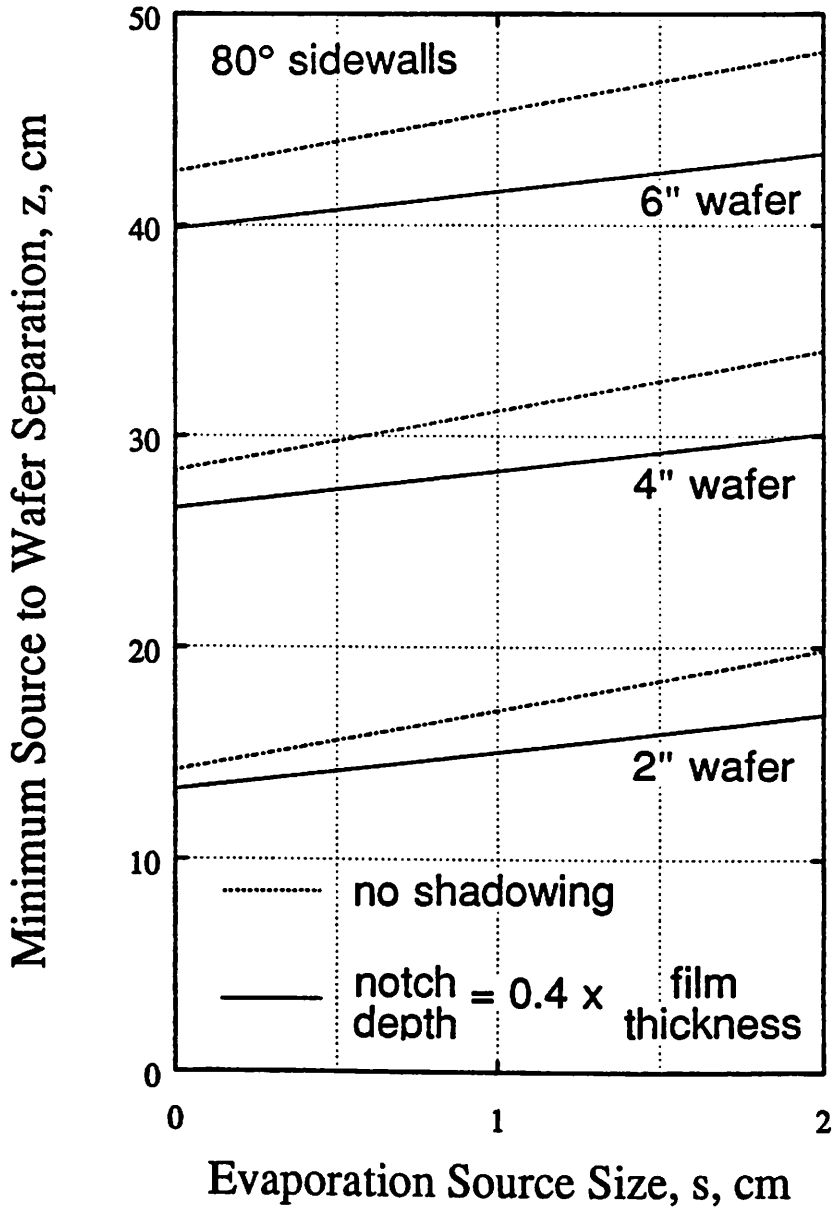


Figure 8. Enlargement of process window if notch formation is allowed to be 40% of film thickness.

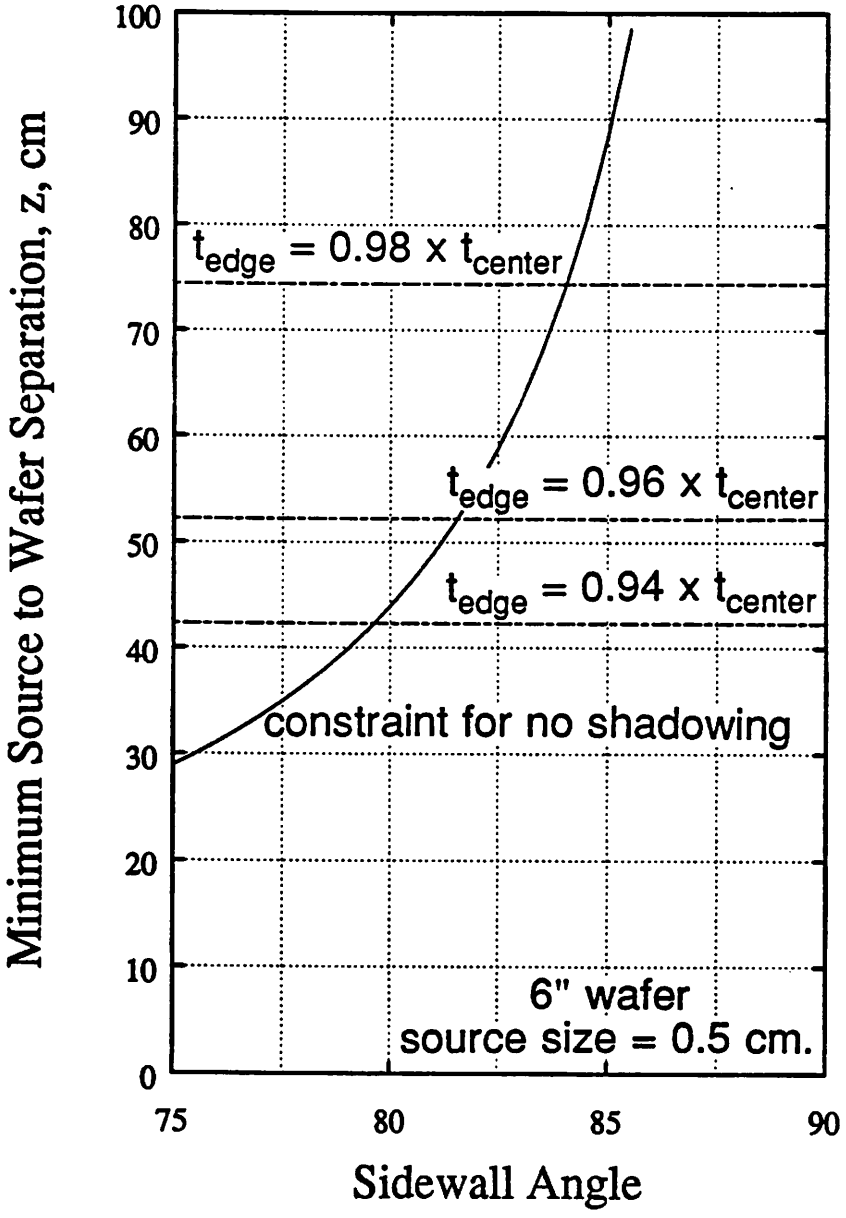


Figure 9. Process window for 6" wafer as a function of sidewall angle. Thickness variation for various source to wafer separations is graphed based on the standard cosine evaporation distribution.

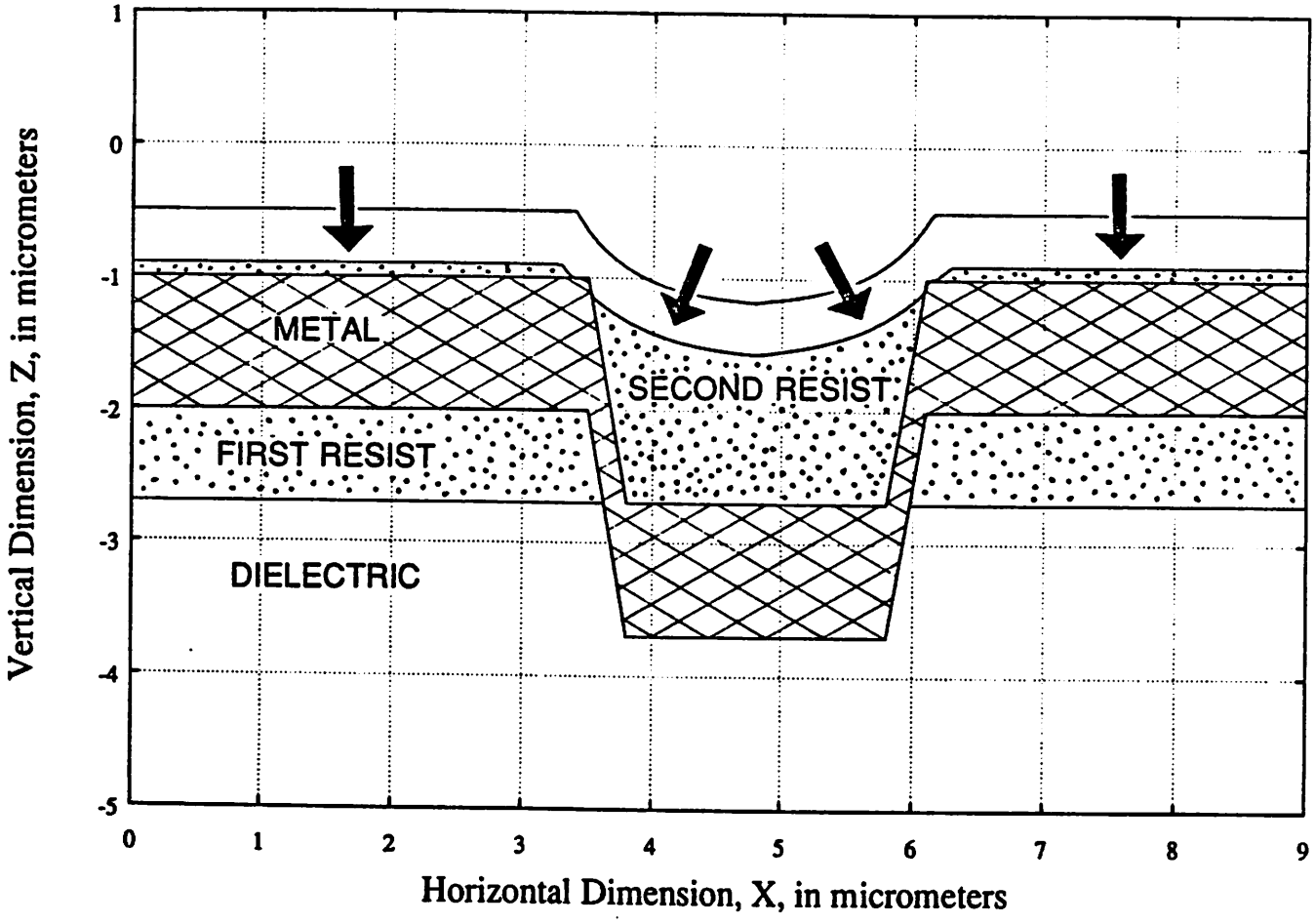


Figure 10. SAMPLE simulation of resist etchback during the loped liftoff process.

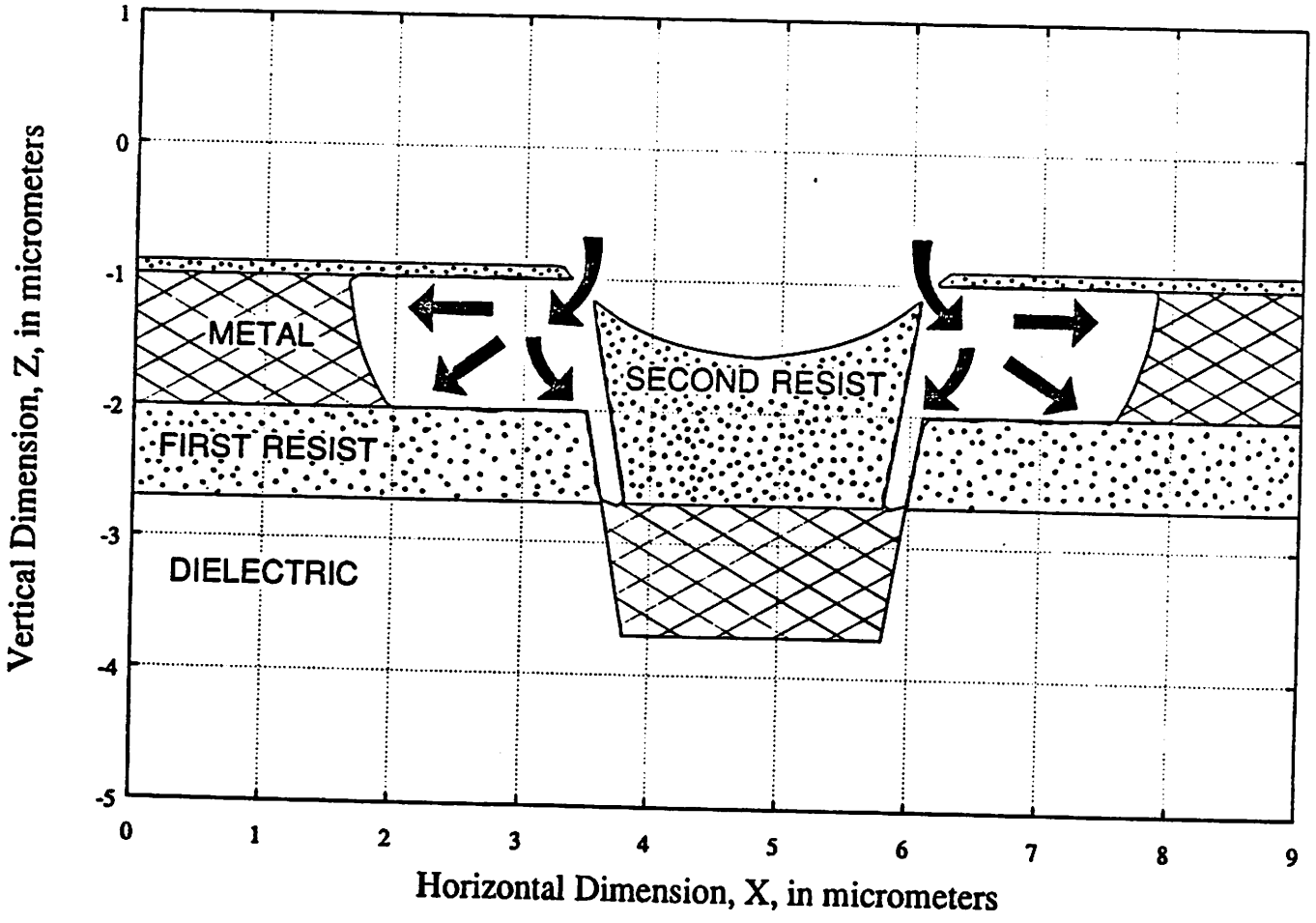


Figure 11. SAMPLE simulation of metal etchback during the loped liftoff process.

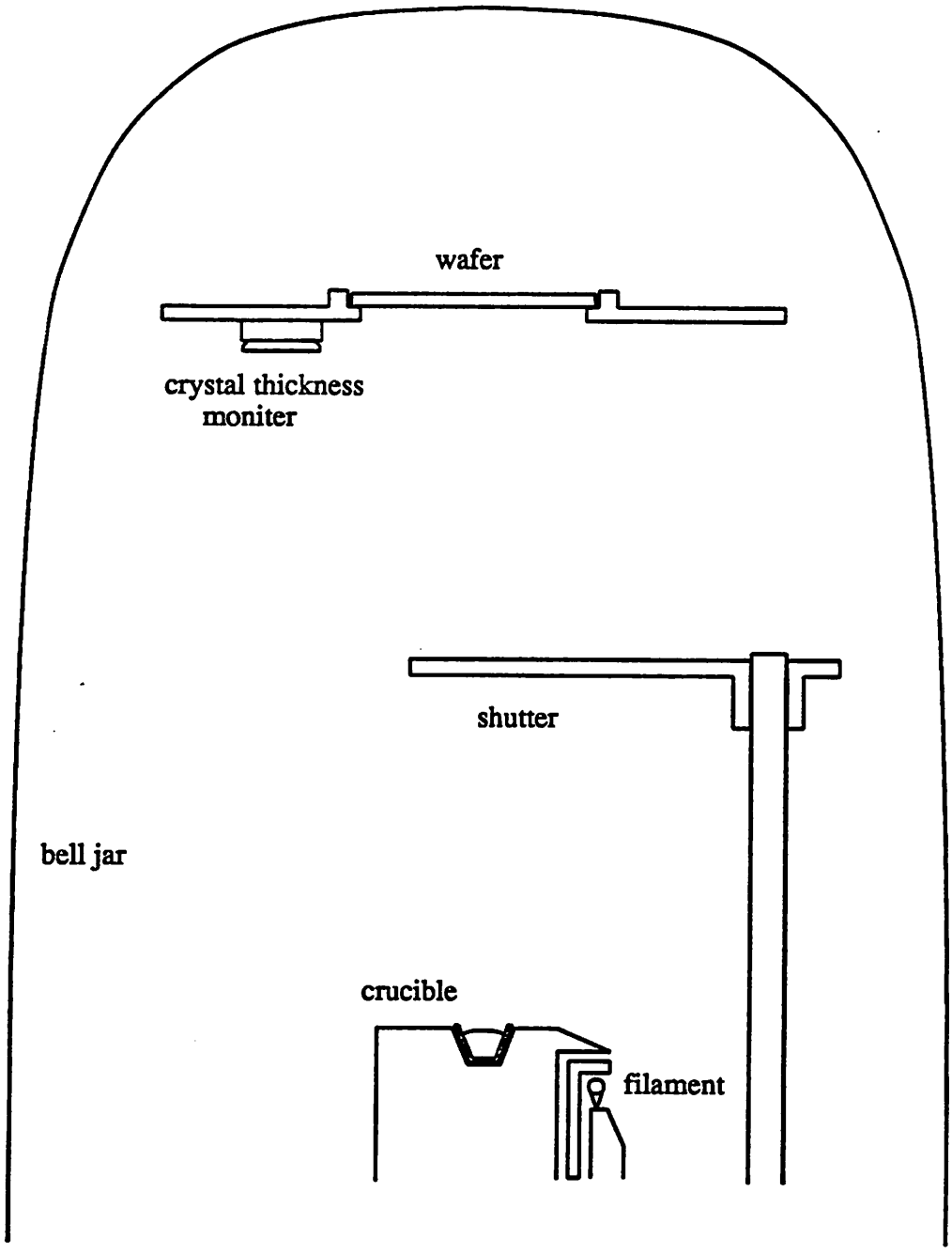
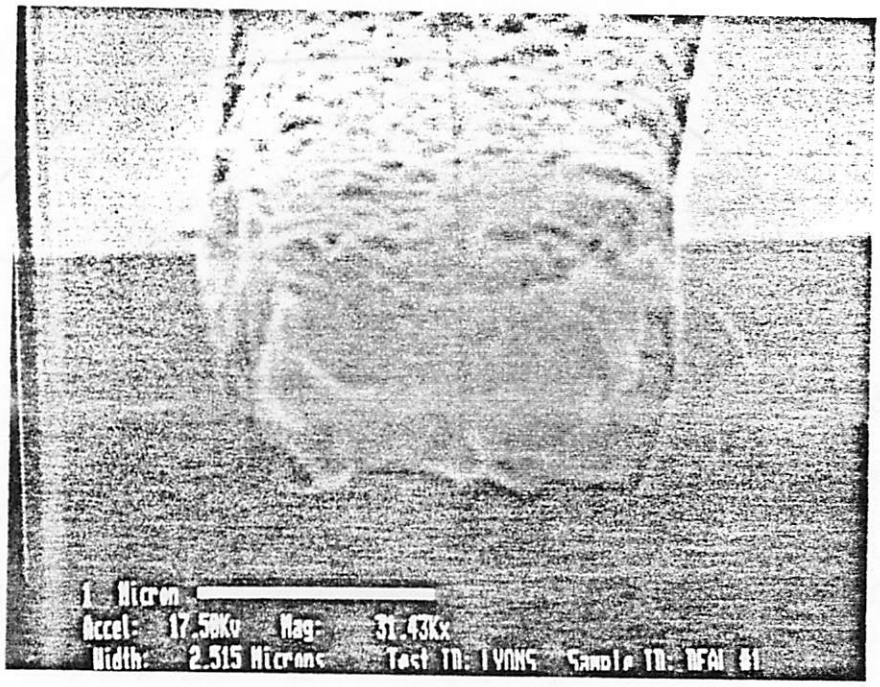


Figure 12. The evaporation system configuration.

(A)



(B)

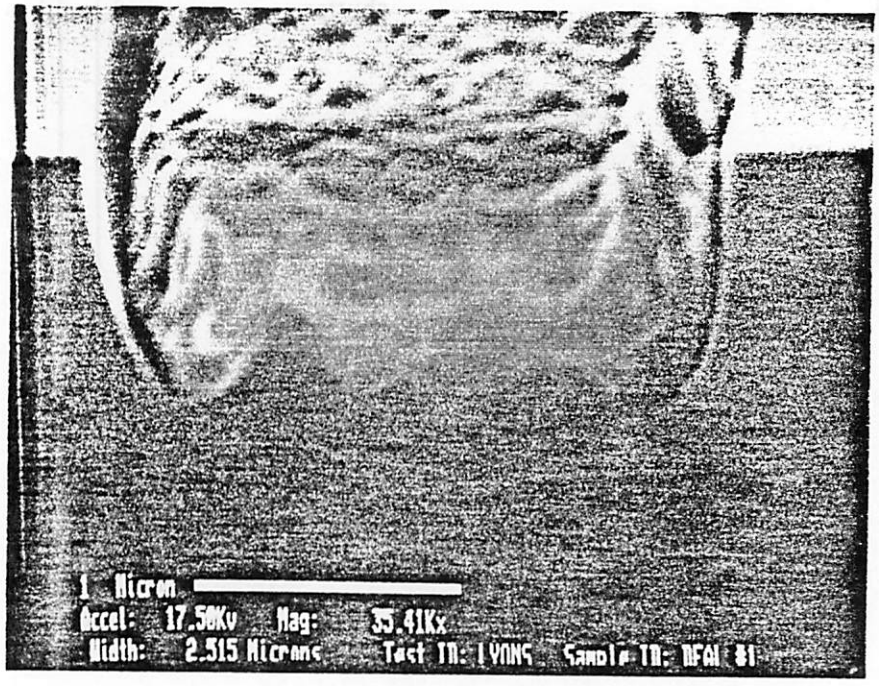


Figure 13. Example final profiles for two different deposition situations: (A) non-shadowed deposition and (B) notched deposition resulting from shadowing on the left side. Lines are 1.5μm.

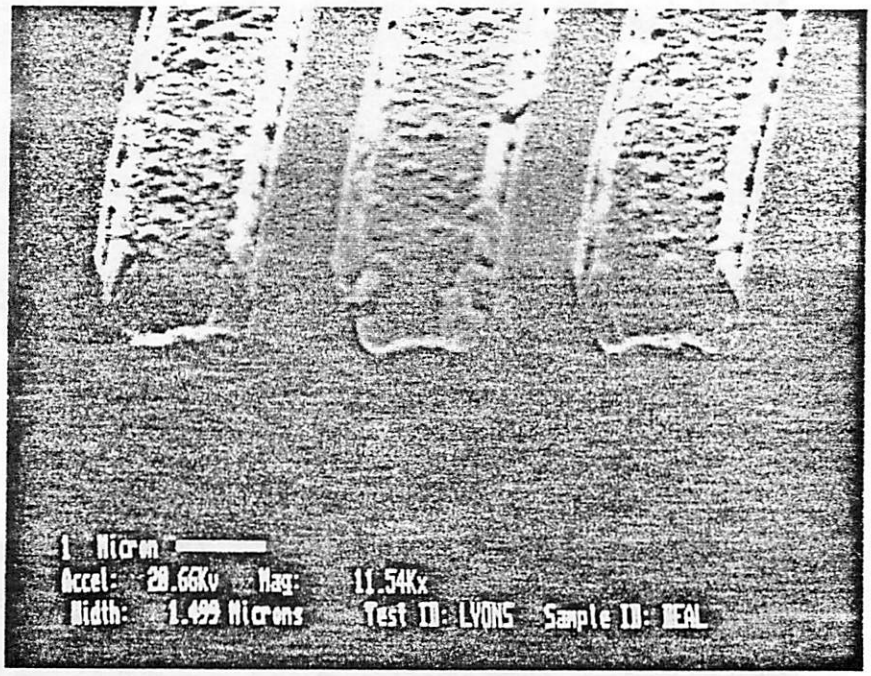
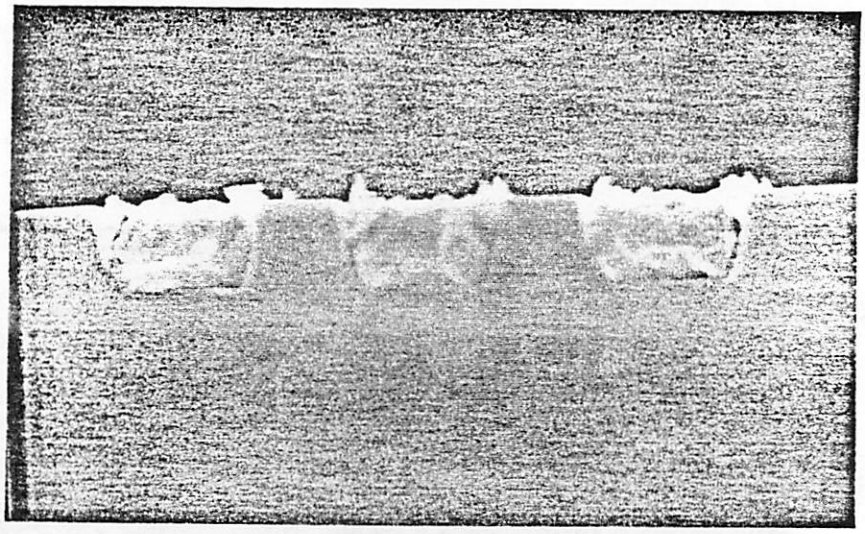
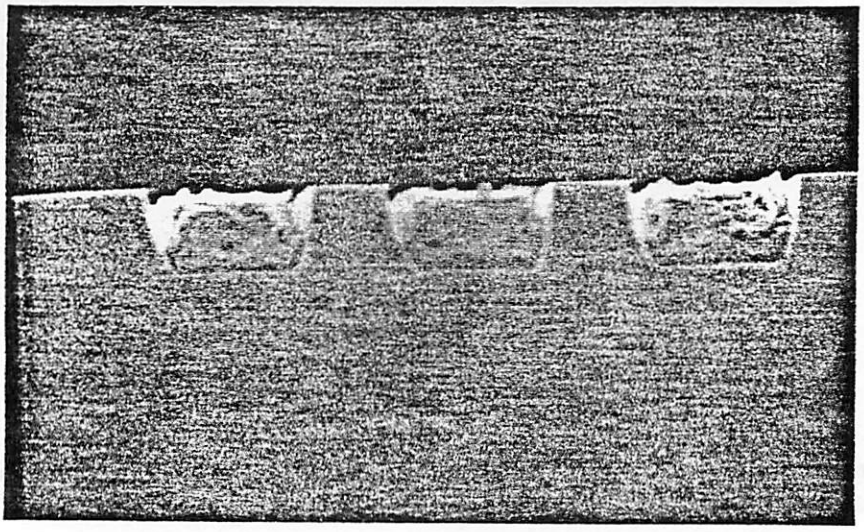


Figure 14. Typical line/space array showing rough edges as a result of the loped metal etch step. Lines are 1.5µm.

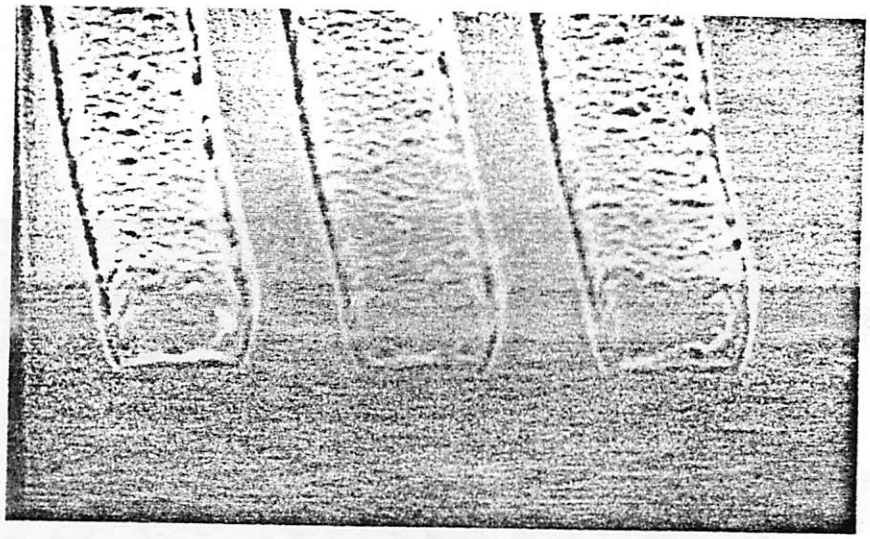


(A)

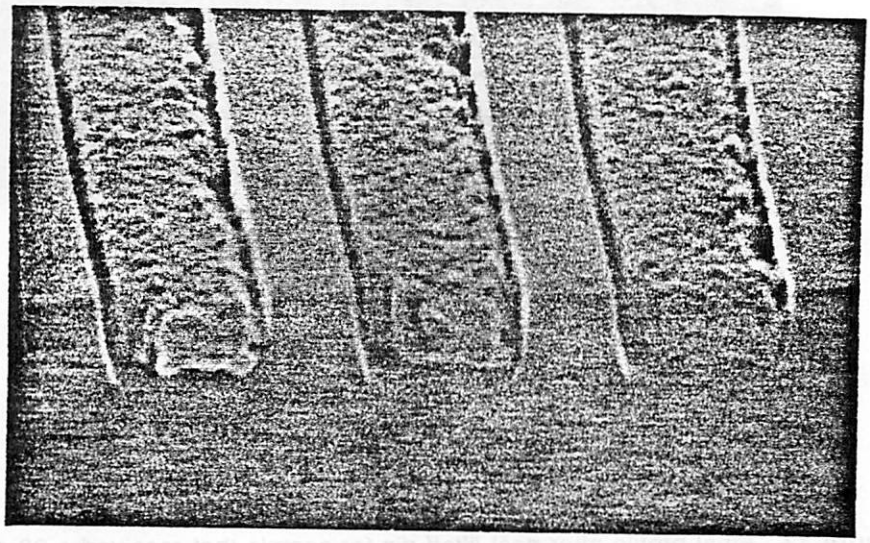


(B)

Figure 15. View of (A) before and (B) after a post-liftoff dip, used to remove edge roughness. Accelerated etching is observed at the aluminum/oxide interface. Lines are 1.5μm.



(A)



(B)

Figure 16. View of features moving from center (A) to perimeter (B) of 4" wafer, without post-liftoff dip. Lines are 1.5μm.

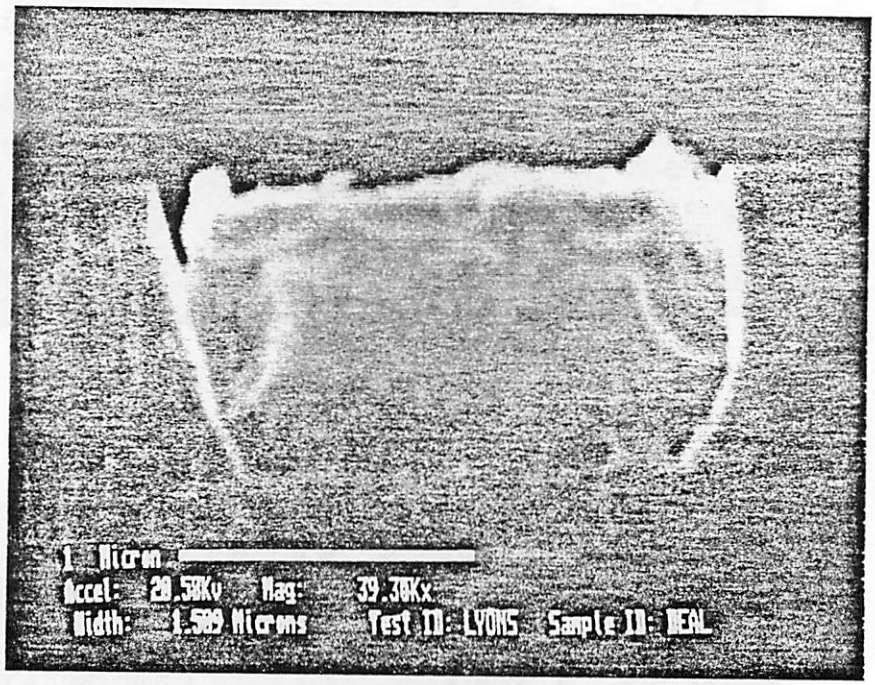


Figure 17. Final profile after post-liftoff dip for sample that received a 20 minute anneal at 400°C. Accelerated etching at the aluminum/oxide interface is not observed. Notch on left is a result of shadowed deposition. Line is 1.5µm.

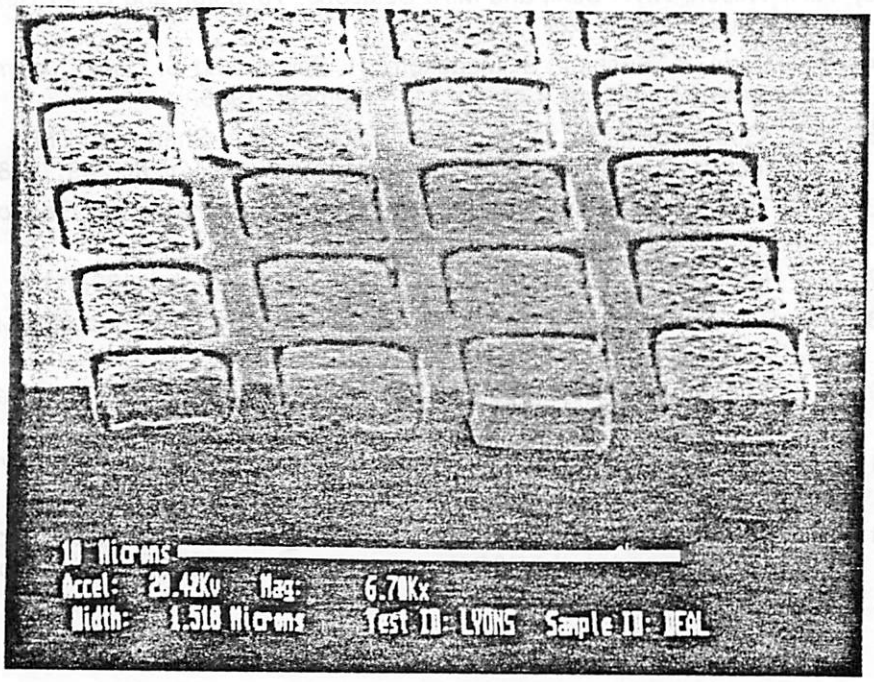


Figure 18. Features that display good edge quality in both x and y directions. Feature is 2.5µm x 4.0µm.

References

[1] M. Hatzakis, B.J. Canavello, and J.M. Shaw, *IBM Journal of Research and Development,* vol. 24, no. 4, July, 1980.

[2] K.C. Saraswat, *Tungsten and Other Refractory Metals for VLSI Applications, Vol. I,* 465, (1986).

[3] R.H. Wilson, R.W. Stoll, and M.A. Calacone, *Tungsten and Other Refractory Metals for VLSI Applications, Vol. I,* 35, (1986).

[4] Y. Harada, K. Fushimi, S. Madokoro, H. Sawai, and S. Ushio, *Journal of the Electrochemical Society,* vol. 133, no. 11, November, 1986.

[5] G.E. Georgiou, H.S. Luftman, F.A. Baiocchi, T.T. Sheng, and M.J. Vasile, *Tungsten and Other Refractory Metals for VLSI Applications, Vol. III,* 249, (1987).

[6] C.H. Ting, M. Paunovic, P.L. Pai, and G. Chiu, *Journal of the Electrochemical Society,* vol. 136, no. 2, February, 1989.

[7] L.B. Rothman, *Journal of the Electrochemical Society,* vol. 130, no. 8, August, 1983.

[8] P.L. Pai, and W.G. Oldham, *IEEE Transactions on Semiconductor Manufacturing,* vol. 1, no. 1, 1988.

[9] W.G. Oldham, A.R. Neureuther, C. Sung, J.L. Reynolds, and S.N. Nandgaonkar, *IEEE Transactions on Electron Devices,* vol. ED-27, no. 8, 1986.

[10] D.E. Lyons, S.F. Meier, L. Winemberg, A.R. Neureuther, and W.G. Oldham, *KTI Microelectronics Seminar,* November, 1988.

[11] P.L. Pai, *Multilivel Interconnection Technologies -- A Framework and Examples,* PhD. Thesis, Department of EECS, University of California, Berkeley, October, 1987.

Appendix 1: Ultek E-Gun Evaporation System

1. Introduction

The Ultek evaporation system is a specialized system configured to give optimum trench and via filling using a liftoff scheme.

The materials used in this system are aluminum, copper, titanium and palladium. Other materials that can be evaporated are possible, however materials compatible with silicon processing are preferred.

2. Operating Procedure

2.1 Procedure to Load Wafer

1. Fill the two styrofoam dewers for the sorption pumps with liquid nitrogen.

2. Open the chamber isolation hi-vac valve.

3. Slowly open the nitrogen vent valve. A rush of air should be heard when the valve opens. Slowly vent the system to atmosphere, taking approximately 1-2 minutes. Watch the low vacuum gauge carefully, slowing the flow of nitrogen when the pressure approaches atmosphere (zero inches vacuum). The bell jar may jump off the chamber somewhat violently.

4. Lift the bell jar from the chamber. Care should be taken so that the rubber o-ring does not come off the bell jar, as it often sticks to the top of the chamber.

5. Remove wafer (if any) from top of platter and load new sample.

6. Make preparations to do the desired evaporation. This may involve loading a new crucible liner and desired material(s) shot and selecting the desired crucible (positioning it next to the e-gun filament). At this time, the crucible closest to the front is used for Ti, the center crucible for Cu and the far crucible for Al. Vitreous carbon crucible liners are being used for all target materials. The crystal in the thickness rate monitor may need to be replaced, if necessary do so at this time.

7. Replace glass slides in hanging rod supports.

8. Gently lower bell jar on to chamber. Make sure that the coated portions of the bell jar line up with the edges of the metal collar and that no more of the bell jar will be coated.

9. Start the pump-down cycle by closing the nitrogen vent valve. Plug in the diaphragm roughing pump and open the roughing valve. Hold down the bell jar to make sure that a seal is made. Note: the roughing pump will not start if a residual vacuum exists on the line. If this happens, open the roughing valve before starting the pump.

10. Wait for the roughing pump to pump down the chamber to approximately 29" Hg. This will take a few minutes. When this point is

reached, shut the roughing valve and unplug the roughing pump.

11. Open the valve to adsorption pump #1 and wait for the TC gauge on the main rack to read 30-40 mTorr. This will take about a minute. When this point is reached, close the valve to this pump. Note: the adsorption pumps need at least 20 minutes after being filled with LN to fully cool so they pump at their maximum speed.

12. After closing adsorption pump #1, open pump #2. This should pump down the system to somewhere in the 1-5 mTorr range within a minute or two.

13. Select the next sublimation filament on the pump control unit in the equipment rack and turn on the power to the sublimation pump. The pump should be in cycle mode with a cycle time of around 10 minutes (a fixed 2 minute on time with a 10 minute cycle between cycles) to begin. At this time the ion gauge can be turned on.

14. Let the sublimation pump cycle at least twice before attempting to turn on the ion pumps. The best way to turn on the ion pumps is to wait until the end of a sublimation cycle, then shut the chamber isolation hi-vac valve (the adsorption pumps degas at such a rate that they cannot bring the system below about 5×10^{-4} Torr). The chamber pressure should fall below 5×10^{-4} Torr before turning on the ion pumps (if this does not occur then open the chamber isolation valve and let the sublimation pump cycle through again).

15. Turn on the power to the ion pumps. To avoid damage to the equipment, leave the pumps in 'run' mode at all times. The pressure (read on the ion pump gauge) should quickly go down into the 10^{-5} Torr range. The pressure may not fall very far and may rise again when the plates of the ion pump become heated and begin outgassing. If this occurs, shut off the power to the ion pumps and open the chamber isolation hi-vac valve and go through the sublimation pump cycle again. The ion pumps may display this same behavior the first time the sublimation pump cycles through after crossover. It may be necessary to shut off the ion pumps after this as well and repeat the sublimation process.

16. Once crossover to the ion pumps is accomplished, be sure to close the hi-vac valve for adsorption pump #2. Also, set the sublimation cycle time to 30 minutes to promote the lifetime of the sublimation filaments. The base pressure without using sublimation is about 2×10^{-6} Torr; with sublimation it is about 2×10^{-7} Torr or lower. The system will take several hours to pump to this base pressure depending on the care taken to keep the chamber clean.

2.2 E-Gun Operation

1. Turn on the water cooling using the water flow valve on the e-gun water inlet. This provides water cooling to the e-gun and the thickness monitor crystal sensor.

2. Connect the thickness monitor. At present this means connect the cable (inside the storage box under the main chamber) to the XTM unit of the Top Gun. The XTM will need to be programmed for the density of the material being evaporated and the tooling factor (107% typically) of the system.

3. Turn on the main power of the e-gun control unit. If the interlock light becomes lit then there is a problem. The ultek has both a water interlock detector and a vacuum interlock (26" Hg) connected in series. Eliminate this problem before continuing.

4. Press the high voltage button on the e-gun control unit. If there is a short, the current will jump to a large value and the unit will shut itself off. A short can be caused by anything providing electrical connection between the crucible (nominally ground) and the filament & lead-ins (nominally -5 kV). If a short occurs, do not operate the system until the problem is solved. If the power does not come on, check that the remote power switch is set to

5. Set the power switch on the remote control to the 'on' position. Select the desired power using the variac. The variac zero position is below the actual zero position shown on the dial. For most materials, the variac can be set initially around 1.00. The evaporation can be monitored through the glass slide window until a few hundred angstroms of material is evaporated.

6. When the desired evaporation rate is obtained, open the shutter and proceed with the deposition. Usually the shutter is positioned so that the evaporation rate increases slightly after the shutter is moved out of the way. When the deposition is complete close the shutter and shut down the power in the reverse order of start-up. If a serial deposition of more than one material is desired, allow the e-gun to cool before moving to the next crucible. The crucibles are separated by 12 and 1/2 turns on the linear position adjustment knob.

7. For high power evaporations, monitor the water temperature closely (feel the water output of the e-gun) to make sure that it does not get too high. The pressure should be watched throughout the deposition also, so that it does not get too high and cause the ion pumps to shut off.

8. Vent the system as you would were you loading a wafer. If no wafer is to be loaded at least pump down the system with the mechanical pump so that a vacuum is maintained and the chamber is easier to pump down the next time.

9. After the e-gun has sufficiently cooled, turn of the water flow valve. Also, don't forget to disconnect the cable to the Top Gun XTM unit.

3. Material Considerations

The interaction of this system with the various materials evaporated in it should be considered by prospective users. Raw material (shot) is kept in the storage box beneath the chamber and should be reordered when supplies run low. Extra crucible liners and XTM crystals are also kept on hand.

Aluminum is a straight forward material to evaporate and films up to a micron thick have been successfully evaporated in the ultek. To evaporate at a high rate (above 10-20 A/sec) results in significant heating and can also cause a significant pressure rise inside the chamber during evaporation. Care should be taken also to avoid filling the crucible liner too full, so as to not crack the liner on cooldown.

The copper shot used in this system has had a tendency to outgas as it is heated (especially when first cycled) so the pressure has to be carefully monitored. After the

initial evaporation, it has been relatively trouble free however.

Titanium presents an interesting situation in that it prefers to sublime rather than melt and evaporate. It can be melted however so that the shot forms a nice pool in the crucible liner. A long, low power heating will accomplish this. Titanium tends to outgas considerably on heating (and continues to do so after the initial conditioning) but once it begins to evaporate the chamber walls become coated with a great gettering source and the pressure drops quite quickly.

4. Maintenance

As users will quickly learn, the ultek is notoriously underpumped. Considerable care should be taken to preserve the somewhat delicate components of the system.

The adsorption pumps should be baked out periodically. This can be done using the heating tapes stored in the box beneath the chamber. These tapes can be plugged directly into 120V and left for an hour (do not leave them unguarded, however). Any longer and they will overheat. Do not wrap them over themselves either, as that will also produce overheating. Wrapping aluminum foil around them helps distribute the heat more uniformly and also insulates them, so you loose less heat to the air. Wrapping them around the adsorption pumps will cause a pressure buildup and the corks will pop. Replace the corks before letting the pumps cool.

The filaments for the sublimators will need to be replaced periodically as well. Spare filaments and copper crush gaskets are kept in the storage box.

A hi-vac valve and port are dedicated to be used for leak checking as necessary. The helium leak detector can be connected directly to this valve.

The Thermionics e-gun documentation is located in the ultek equipment file. The only major consideration here is the position of the filament. Currently the filament is aligned so that the 'hot spot' of the deposition is on the side of the crucible near to the filament. This can present problems during depositions and needs to be closely monitored so that the electron beam heats the target material and not the crucible or crucible liner.

A low power electrical feedthrough has also been installed in the ultek. This can be used as a feedthrough for a thermocouple for example. One test using a thermocouple attached to the back of a wafer gave a wafer temperature of 50-60 /(deC during a moderate power aluminum deposition (10-20 A/sec.).

Appendix 2: Process Parameters

- Test grade 100 silicon 4" wafers
- Thermal oxide growth. Tylan tube 1 or 2. SWETOXB recipe. 3 hours @ 1000°C gives 1.0 μm.
- Spin on KTI 820 photoresist @ 4600 rpm using the Eaton wafertrack recipe 10.
- Pattern using GCA stepper at nominal focus and dose. Standard 60 second development in KTI 934 Developer (50% diluted with water) using the MTI spin developer.
- Etch pattern into oxide using Lam2 standard recipe (power = 850 W, He = 120 sccm, CHF_3 = 30 sccm, CF_4 = 35 sccm, and electrode gap spacing = 3.8 mm). Etch rate is 2000-4000 A/min.
- Deposit metal (aluminum) in the Ultek evaporation system.
- Spin on AZ 1400-21 photoresist at 6000 rpm to give a thickness of approximately 6000 A.
- Etch back top resist in oxide plasma in Technics-C. Use a power setting of 50 W for 6.3 minutes to etchback to about 1000 A.
- Etch back metal corners in Al etchant in sink 8. Etchrate is nominally 100 A/sec @ 50°C. Monitor closely.
- Liftoff in acetone using ultrasonic agitation. Heat if necessary.

For the experiments in this report, the MET3 mask of the N-level mask set developed by Dean Drako and Don Lyons was used. This level has SEM lines of pitch 3.0 μm down to 1.4 μm and also large area contact pads.