TEST STRUCTURES FOR N-LEVEL METAL

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Dean M. Drako and Don E. Lyons

Memorandum No. UCB/ERL M89/76

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Abstract

A one centimeter square layout was completed containing test structures for N-Level metal process development and control. The layout includes three "wire" levels and two "via" levels. With proper interleaving of these levels test structures can be constructed for any (N) number of metal layers. Emphasis was placed upon electrical testing where possible.

Table of Contents

1. N-Level Metal Overall Design

This section describes some of the overall consideration of the N-Level Metal Test Chip Layout and Test Structure Design.

1.1. Floorplan Design

The N-Level Metal Test Chip is designed for a 1cm by 1cm die size. The majority of the die is designed for Electrical Test probing. The Electrical Test portion occupies the exact center of the die and measures 9.6mm by 9.6mm. This leaves a border of .2mm on all sides of the electrical test structures. The border area is utilized for visual test structures and for alignment marks. Neither of these structures require electrical probing.

The electrical test portion of the die is further divided into 30 rows and 6 columns. This yields 180 blocks which measure 1600um by 320um each. Each block can be utilized as an electrical test structure. Each block if utilized as an electrical test structure will contain a standard padset. The standard padset is shown below:

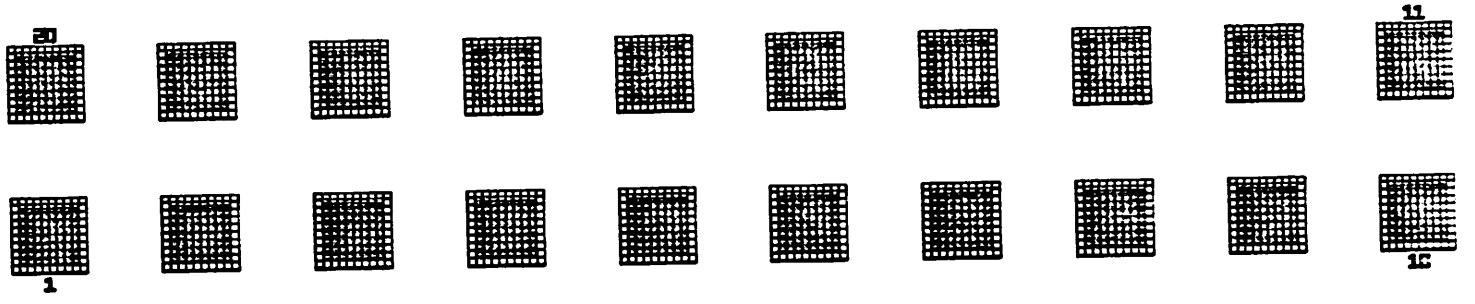


Figure 1. Standard Padset

Each padset consists of 20 pads. The pads are numbered as shown. Each pad measures 80um by 80um and are placed on 160um centers. Not all block locations are occupied by padsets. Some of the padsets have been eliminated to allow for larger test structures. The test structure may occupy a block and the padset to obtain measurements located in an adjacent block. This is the case for many large test structures. Visual test structures placed in the electrical test area do not have any pads.

1.2. Floorplan

The floorplan of the N-Level Metal Test Chip is shown below.

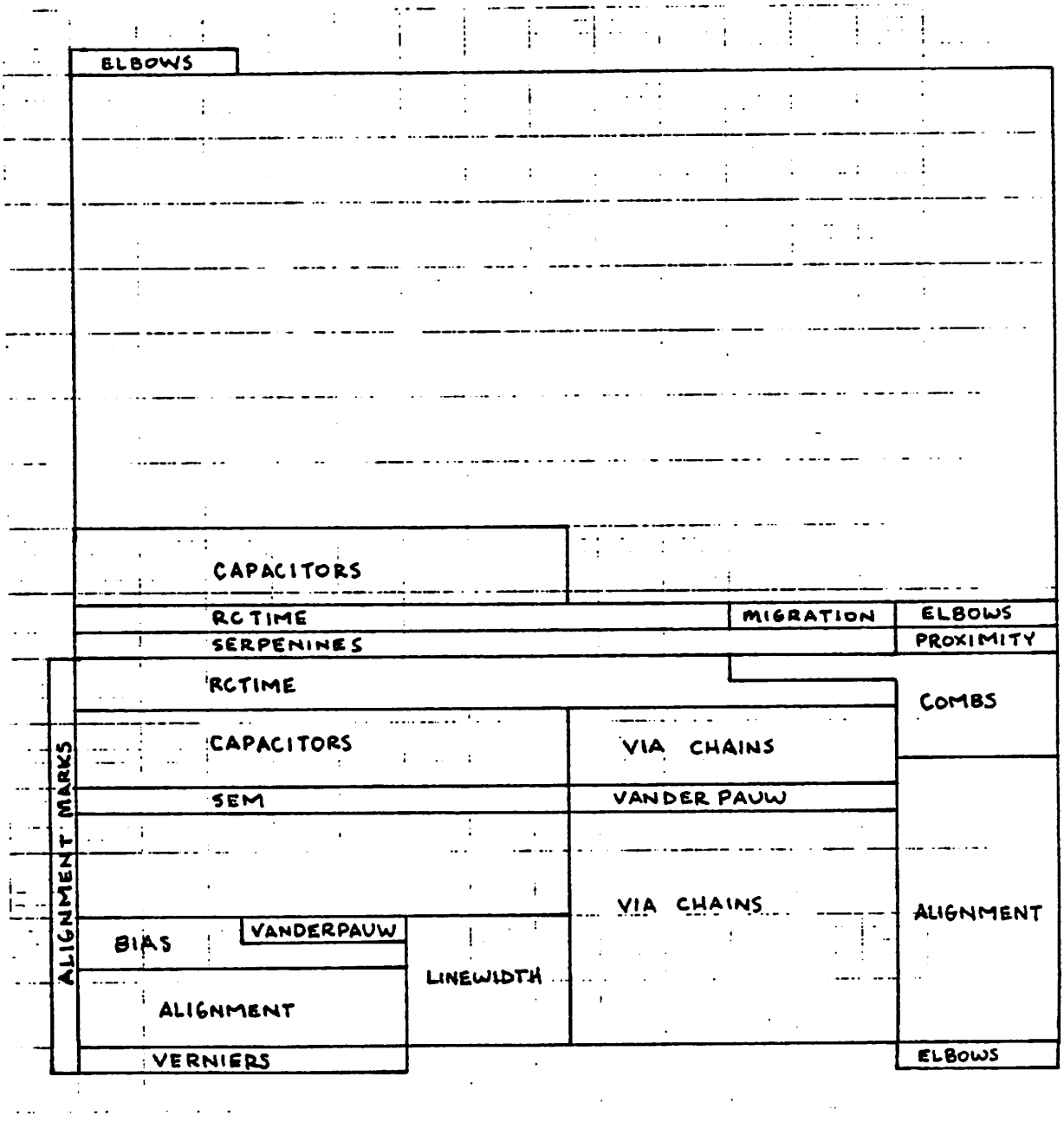


Figure 2. N-Level Metal Floor Plan

1.3. Layout Layers

This report includes a number of test structure plots. The key to these plots is shown below:

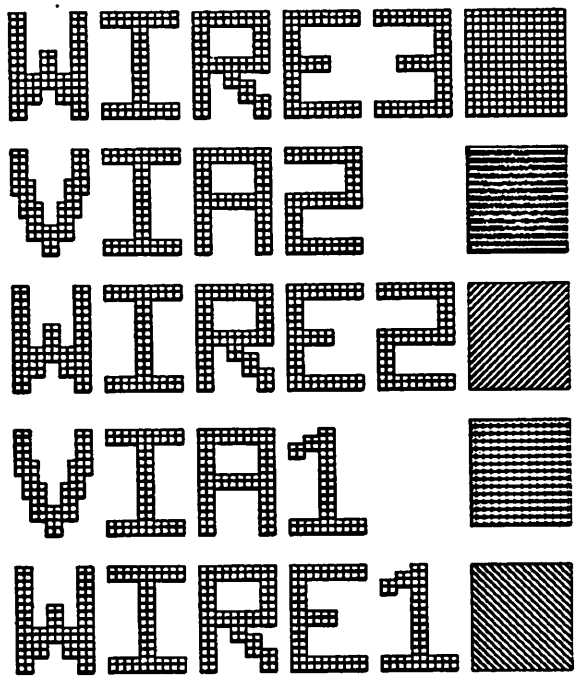


Figure 3. Key to Layout Plots

1.4. Layout OCT/VEM Mapping

The layouts for the N-Level design were completed using the U.C. Berkeley OCT/VEM system. The standard SCMOS design palette was utilized. The layer definitions of the N-Level Mask set and their corresponding Vem-SCMOS Layout layers are listed below:

N-Level Metal Test Chip to SCMOS Layers	
N-Level Metal Layer	SCMOS Layer
Wire1	Met1
Wire2	Met2
Wire3	Poly
Via1	CONS
Via2	COND

Table 1. N-Level Metal to VEM-SCMOS Layer Mapping

2. Summary of Test Structures

The test structures on the N-Level Metal Test Chip are summarized below.

N-Level Metal Test Structures				
Structure	Purpose	Filename	Row	Column
Elbows	visual linewidth measurement	elbows	Border	1 & 6
			17	6
Verniers	visual measurement of alignment	verniers	Border	1
Van Der Pauw	measure sheet resistance of layers	sheet1	6	2
Via Res	measure via resistance	contactres	10	3 & 4
Via Chains	measure via yield, resistance	con	1-13	4 & 5
Combs	measure metal isolation, capacitance	combs	16	1-5
Serpentines	measure metal isolation, planarity, yield	snakes	12-15	6
Capacitors	determine defect density, dielectric thickness, breakdown voltage, interlevel cap, fringe cap	cap	7-13	1-3
			18-20	1-3
Linewidth	Electrically measure linewidth	liwi	1-6	3
Bias	Measure metal process bias	bias	4-6	1 & 2
Align	Electrically measure alignment between layers	align	1-11	6
			1-3	1 & 2
Rctime	Directly measure rc time constants	rctime	14-15	1-5
			17	1-4
Sem	sem lines for profile measurements	sem	10	1-3
Proximity	Measure feature proximity effects	proximity	16	6
Electromig	Measure electromigration properties of metal	migration	17	5

Table 2. Summary of Test Structures

3. N-Level Metal Process Outline

Version 0.0

3.1. General Process Outline:

3.1.1. Wafer Preparation

3.1.2. Initial Oxidation

wet thermal oxidation; 140 min. at 1100 C, ~1um
measure oxide thickness

3.1.3. Metal Layer Wire1 Application

1. PECVD oxide deposition ~5000A
   measure oxide thickness
2. photolithography <WIRE1>
3. oxide plasma etch ~5000A
   visual inspection
4. Al-Si sputtering ~5000A
5. lift-off process using edge detection (LOPED)
   visual inspection

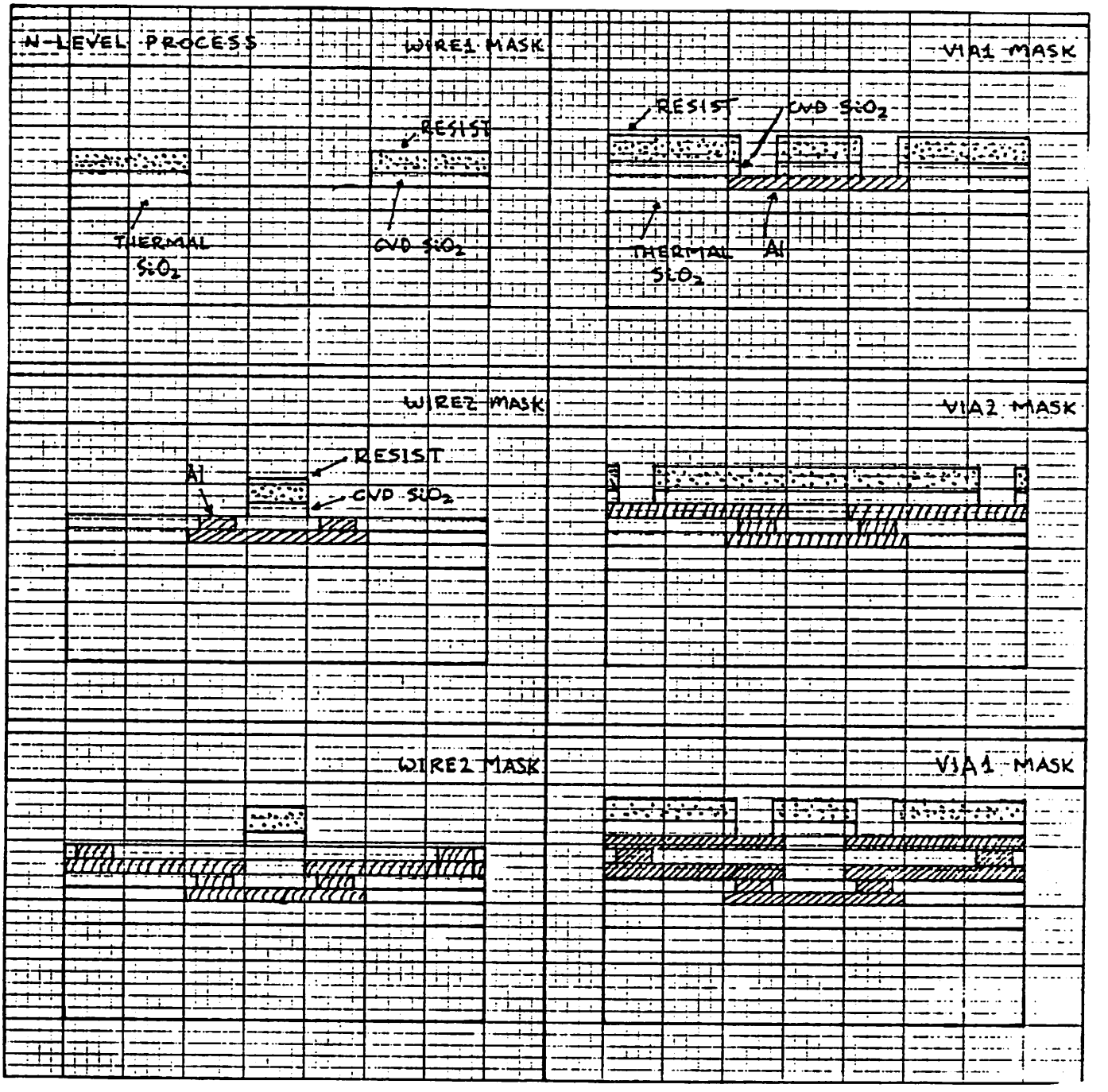
3.1.4. Metal Layer Via1 Application

1. PECVD oxide deposition ~5000A
   measure oxide thickness
2. photolithography <VIA1>
3. oxide plasma etch ~5000A
   visual inspection
4. Al-Si sputtering ~5000A
5. lift-off process using edge detection (LOPED)
   visual inspection

3.1.5. Metal Layer Wire3 Application

1. PECVD oxide deposition ~5000A
   measure oxide thickness
2. photolithography <WIRE3>
3. oxide plasma etch ~5000A
   visual inspection
4. Al-Si sputtering ~5000A
5. lift-off process using edge detection (LOPED)
   visual inspection

3.1.6. General Process Cross-sectional Schematics:

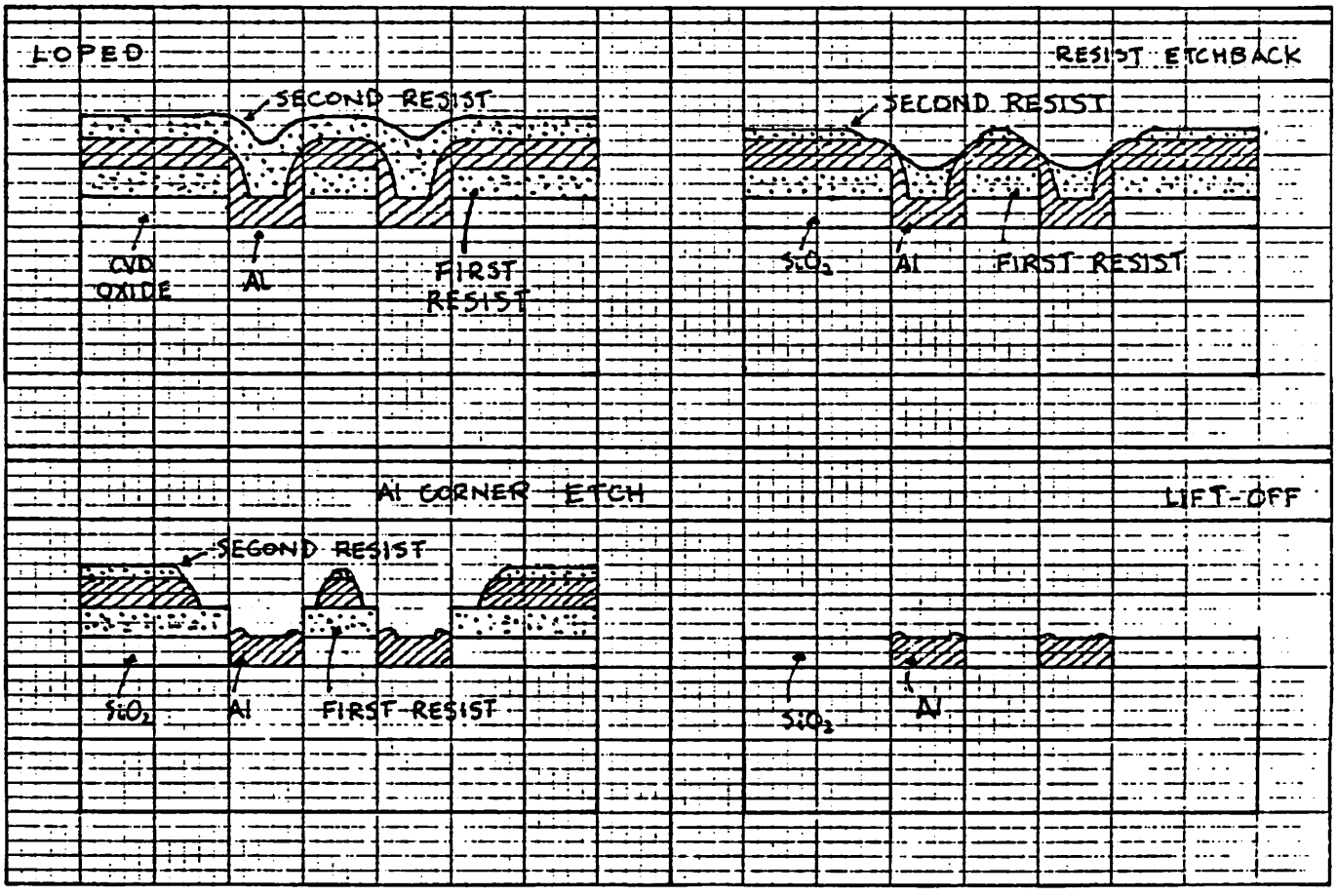


3.2. LOPED Outline:

3.2.1. Lift-off Process Using Edge Detection (LOPED)

1. resist spin ~6000A
2. resist etchback to ~1000A
3. Al corner wet-etch
4. lift-off

3.2.2. LOPED Cross-Sectional Schematics:



4. Discussion of Test Structures

This section gives some background on each of the test structures which was implemented on the N-Level Metal Test Chip. It is divided into sections corresponding to the items in the summary table of section 2.

4.1. Elbows

The Elbow Test Structure consists of various size and format elbows for visual inspection. Elbow sets with varying pitch, varying space, equal line space, and varying line & space are included. The elbows are repeated for all five layout layers. The via layers are included for additive metal processing. Note that both vertical and horizontal linewidth can be compared. The Elbows are repeated on the die three times in order to observe any field uniformity problems.

4.2. Verniers

The Vernier test structures can be used to visually inspect alignment between any two layers over a +-1 um range with .1um resolution. The verniers are grouped into 5 sets. Each set corresponds to a single layer. For example set #1 is for the Wire1 level. It contains verniers between Wire1 & Via1, Wire1 & Wire2, Wire1 & Via2, Wire1 & Wire3, and Wire1 & Wire1. The members of a set are located near each other allowing the alignment accuracy to all other layers to be quickly ascertained for the layer of interest. Note that redundancy is included in this system. This was considered advantageous because it allows the verniers to be quickly located and compared. Verniers between the same level might prove useful when doing N-Level processing (the same mask is repeated).

Two types of verniers are included on the layout. The two types are the standard staggered block and the tapered column. The tapered column is a new idea and its accuracy can be compared with the standard technique.

Both types of verniers are capable of measuring alignment to +- 1um in .1um steps. The tapered column structure may prove easier to read (it might not too). The tapered column measurement is made by finding two identical biases. This may remove some of the judgmental problems found with standard block structure.

4.3. Van Der Pauw -- Sheet Resistance

Van Der Pauw structures are included for each level. These allow the measurement of sheet resistance. The sheet resistance can then be utilized in other measurements. Two types of Van Der Pauws (large square and small square) were included. The large square versions are included with the process bias test structure. All Van Der Pauw structures have four identical pads. The sheet resistance can be determined by measuring the voltage between pads 3 & 4 while forcing current through pads 1 & 2. The sheet resistance is given by:

Sheet Resistance = (V * pi) / (I * ln(2))

The measurement should be repeated by forcing current through pads 2 & 3 and measuring voltage between 4 & 1. The results are averaged in order to eliminate any process/lithography introduced bias.

4.4. Via Resistance

Four terminal structures were also included to measure via resistance. Varying size vias were included utilizing both Via1 and Via2 layers. The measurement technique is the same as above. The via resistance, however, is given by:

Via Resistance = V / I = Pc / (d * d)

where V is the measured voltage and I the forced current. The contact resistivity, Pc can be determined from this if the square contact size is know (d by d).

As with Van Der Pauws the measurement should be repeated using different terminals and the results averaged.

4.5. Via Chains

The Via Chains on the N-Level Metal Test Chip are generally configured for multiple levels of metal. They will, however, still function if the the simple two level metal process is utilized. Three structures are utilized for the via chains. Two of the structures are shown below:

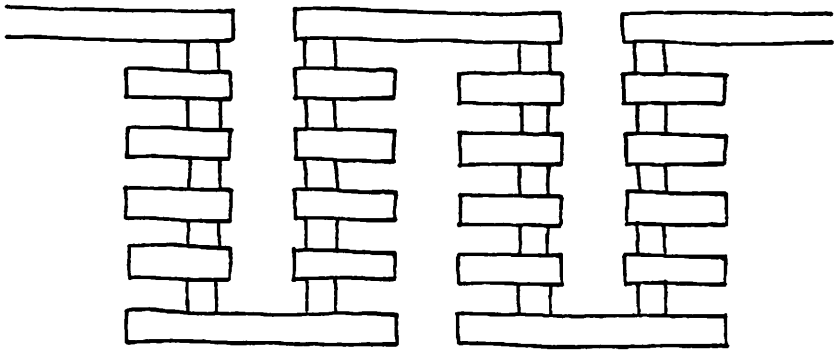


Figure 4. Vertical Via Chain Structure

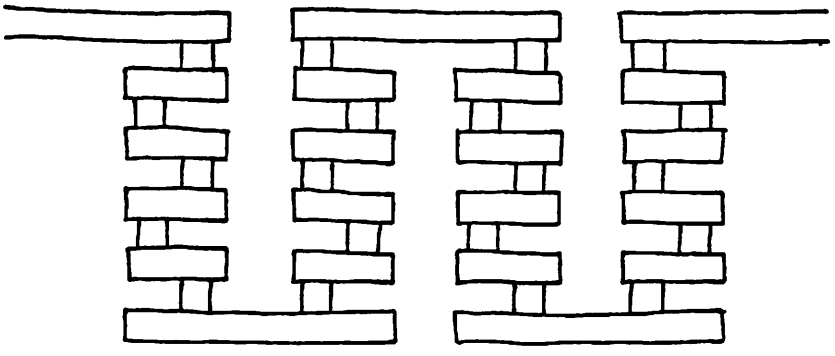


Figure 5. Staggered Via Chain Structure

If the simplest processing sequence is utilized (two levels of metal) both structures degenerate into a similar two level via chain. The via chains are replicated utilizing different size vias in order to determine the feasiblility of any particular via size. Each via chain consists of 3600 via sets. A via set consists of vias to travel through the total number of layers. Measurement points are provided from each via chain at the following points: 40, 80, 160, 320, 640, 1280, 2560, and 3200 vias. In addition to the above two types of via chains a third type is included. This is a simple two layer via chain. A two layer via chain will always result regardless of the number of layers processed. This can be utilized for comparison against the N-Level case.

4.5.1. Via Chain -- via yield

The via chains can be utilized to measure the reliability of the vias in a given process. The staggered via chain, the vertical via chain, and the standard two level via chain can all be compared. The yield is effectively determined by measuring the resistance of the chain. If the resistance is above a set value the via chain can be said to contain a failing via. The probability of a via failing can then be obtained knowing the number of vias measured. The via chains contain "taps" at various points allowing a wide range of yields to be measured. This will prove useful in early process development.

4.5.2. Via Chain -- via resistance

The average via resistance can be determined by measuring the resistance of a long chain of vias and dividing by the number of vias measured:

Average Via Resistance = Clength * (N - 1) / R

where Clength is the length of the contact chain, N is the number of wire layers, and R is the measured resistance.

4.6. Metal Interleaved Combs

These structures are designed to expose shorts between closely spaced metal lines. During electroless plating it is possibile to overfill a trench due to nonuniform nucleation, too long a time in the plating bath, and other reasons. There is a possibility that two overfilled lines, closely spaced, will short to each other on top of the dielectric surface. During an additive lift-off process, there is the possibility that some areas between closely spaced lines will not lift completely. Metal bridges can be formed from one line to an adjacent one, thus creating a short. The comb test structures have varying spaces (0.6, 0.8, 1.0, 1.2, 1.5 um) between lines to give information about the amount of overfilling or the allowable dimensions for lift-off.

Comb structures are stacked above each other in perpendicular directions. Testing for shorts between levels due to dialectric fault or topography introduced problems can be done by probing the resistance between pads attached to the Wire1 level and the Wire2 level, etc.

4.6.1. Combs -- Wire1 to Wire1 capacitance

A measure of capacitance between parallel lines can be obtained from interleaved combs. An approximate reference value for the probe capacitance can be obtained by probing a pair of unused pads.

4.7. Multi Level Serpentines

Long meandering serpentine structures are used to detect openings in metal lines. Various linewidths are used (0.6, 0.8, 1.0, 1.2, 1.5 um). Electroless plating presents a problem due to areas with little or no nucleation. These areas can form opens in long metal lines. More conventional techniques using aluminum can have problems with cracking, step coverage, etc.

4.7.1. Serpentines -- yield

A statistical calculation of yield can be made from open/short measurements using this structure.

4.7.2. Serpentines -- planarity

Due to stacking of serpentines of perpendicular directions atop one another, a measure of planarity and the effects of steps on metal continuity can be obtained.

4.8. Capacitors

The N-Level Metal Test Chip contains a large number of test capacitors. These are designed to measure a number of process parameters. The measurements are described in this section. The capacitors vary in size for yield measurements. Fringe type capacitors are also included.

Capacitors were included in all possible layer combinations. These included the via layers for additive metal processing.

4.8.1. Capacitors -- defect density

The defect density of the interlevel dialectric can be determined using the varying size capacitors. A statistical analysis of the number of capacitors of a particular size that are shorted vs. the number of capacitors tested will yield the defect density.

4.8.2. Capacitors -- dielectric thickness

Assuming a value for the dialectric constant of the dielectric material, the thickness of the dielectric can be determined from the measurement of the capacitance. The thickness is:

dielectric thickness = dielectric constant * area / capacitance

4.8.3. Capacitors -- breakdown voltage

By increasing the voltage across the plates of a capacitor until a breakdown occurs, the breakdown voltage of the dialectric material can be determined.

4.8.4. Capacitors -- Etch rate measurement

For additive metal processes, there is a requirement that the etch of a trench in the dialectric material (to be filled by electroless plating or a lift-off technology, etc.) be well controlled and monitered. Since there is no easy way of in-situ monitering, a process control test structure can be used to measure afterwards. Capacitors between the various layers serve this function well. The thickness of the remaining dialectric after the etch can be determined from the capacitance measurement. The etch depth is computed using the relative capacitance difference from levels A to B and levels A to C.

4.8.5. Capacitors -- fringe capacitance

Fringe capacitance can be determined by using a flat capacitor and a normal test capacitor. The equation that applies is

C fringe = (Cmeasured - Cflat * L * W) / (2 * L).

4.9. Linewidth

The structure is a Cross Bridge. The bridge length is 160um for each of the three linewidth bridges. These bridges also funtion as Van Der Pauw structures of drawn dimensions 0.6, 0.8, 1.0, 1.2, 1.4, and 1.6. The Van Der Pauw should be used to measure sheet resistance. The linewidth is given by+

Line width = length * sheetresistance * I / V

I is the forced current and V is the sensed voltage.

4.10. Bias

The process bias can be obtained using this test structure. First the resistance of a line section without a space is measured. Then a section of the same length, with a space printed down the center of the line, is measured for resistance. The process bias, or how large a section of the wide line was taken up by the space, can then be determined.

Linewidth = length * sheetresistance * I / V

Spacewidth = Linewidth - 2 * (length * sheetresistance * I / V)

Length is the length of the wide line between pads, sheetresistance is the measured sheet resistance of the layer, I is the forced current, and V is the measured voltage difference.

4.11. Electrical Alignment

A new alignment test structure which is better suited for electrical alignment measurements when a high resistivity material (such as poly) is not available has been designed. Furthermore, the new electrical alignment structure should not require any special measurement equipment in order to measure micro volt signals. Only micro volt signals should need to be measured. The structures are laid out in a fashion which eleminates any difficulties due to process bias.

The N-Level Metal Test Chip contains twelve structures for measurement of alignment. Six of these structures are utilized for vertical alignment and six are used for horizontal alignment. Some of the six structures are used for additive type processing and others are used for subtractive processing. Some can be used for both.

The design of the electrical alignment test structures is shown below:

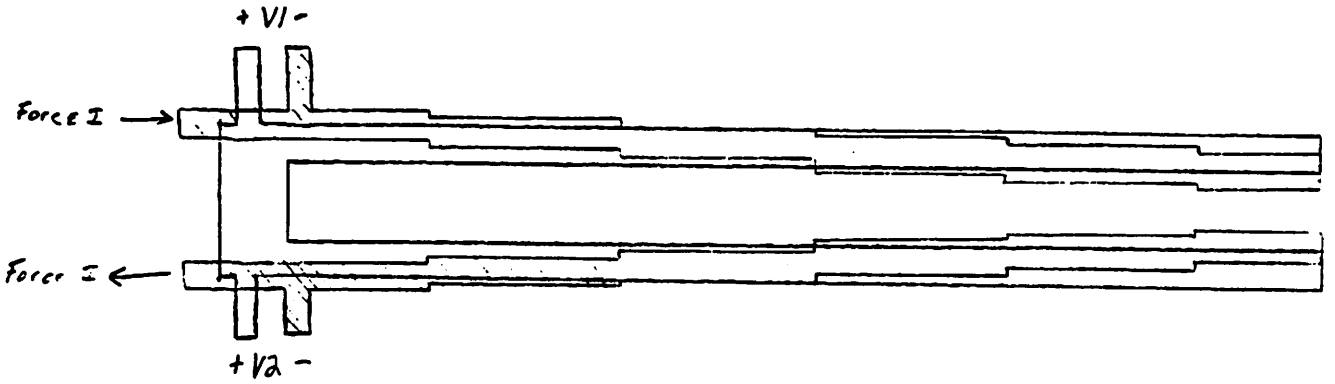


Figure 6. Electrical Alignment Structure (not to scale)

The alignment measurement is made by forcing a current and then measuring the voltage developed across the two sense pads. Two voltages should be measured. These will be termed V1 and V2. The alignment error is given by:

Alignment Error = (V1 - V2) * (.1um) / ((Rsh1*10 + Rsh2*50) * I)

Where Rsh1 is the sheet resistance of the first layer and Rsh2 is the resistance of the second layer, I is the forced current, and V1 and V2 are the measured voltages. The above equation is for subtractive type processing.

4.12. RC Time Constants

Using meandering serpentines, lines much longer than the size of a single die can be made to get some estimate of the RC time delay introduced by long interconnect lines. These type of lines would be present in various types of wafer scale integration or very large die sizes. Two sets of longer serpentines were included, varying the line size and length.

4.13. SEM

Various lines of different levels were layed out to explore topography of metalization techniques. Lines stacked directly on top of each other, lines staggered at different levels, narrow lines between wide features, etc. were layed out. Also, a staggered via chain was included to gain a view of via filling between metal layers. These structures allow the wafer to be cleaved and the cross sections to be viewed using a scanning electron microscope.

4.14. Proximity

Effects of contact density and size and proximity to large features (pads) and lines can be determined by this structure. Visual inspection of the quality of contact filling can be determined

on a small scale. Continuity of nearby lines can be checked electrically also.

4.15. Electro-Migration

A simple electromigration structure was included to give some basic information concerning the electromigration resistance of newly developed metalization techniques, such as electroless plating copper or nickel. A wide line was used with notchs cut out of it on one or both sides and in the corners. At the narrow points left in the line, one expects electromigration to occur. The amount of line left was varied to explore the level of current density needed to produce electromigration.

5. Functional Description of Test Patterns

This section describes each test pattern placed on the N-Level Metal Test Layout.

5.1. Elbows

5.1.1. Filename:

elbows

5.1.2. Purpose:

Visual measurement of both horizontal and vertical linewidth. Visual measurement of process bias. Visual measurement of corner resolution.

5.1.3. Description:

Four different set of elbows containing appropriate sized lines and spaces. The size of the lines and spaces varies from 0.6 um to 3.0 um. The four different sets are:

1) Equal size space, varied size line (upper left)

2) Equal size line, varied size space (upper right)

3) Varied size line, varied size space (lower left)

4) Equal size space, equal size line (lower right)

Each set of four elbows is repeated for each of the five layout layers. The entire structure of elbows is placed on the test chip in three locations to make some determination of field uniformity.

5.1.4. Testing Method:

Visual inspection.

5.1.5. Test Pad Assignments:

none

5.1.6. Location:

Column 1, Row 32; Column 6, Row 1; Column 6, Row 18

5.1.7. References:

E290O test structures (partial)

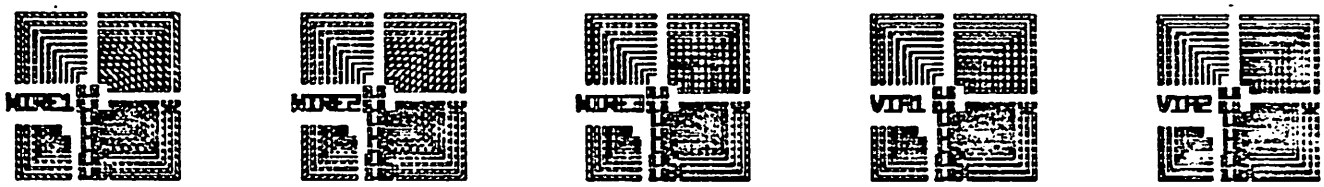


Figure 7. Layout of Elbow Structures

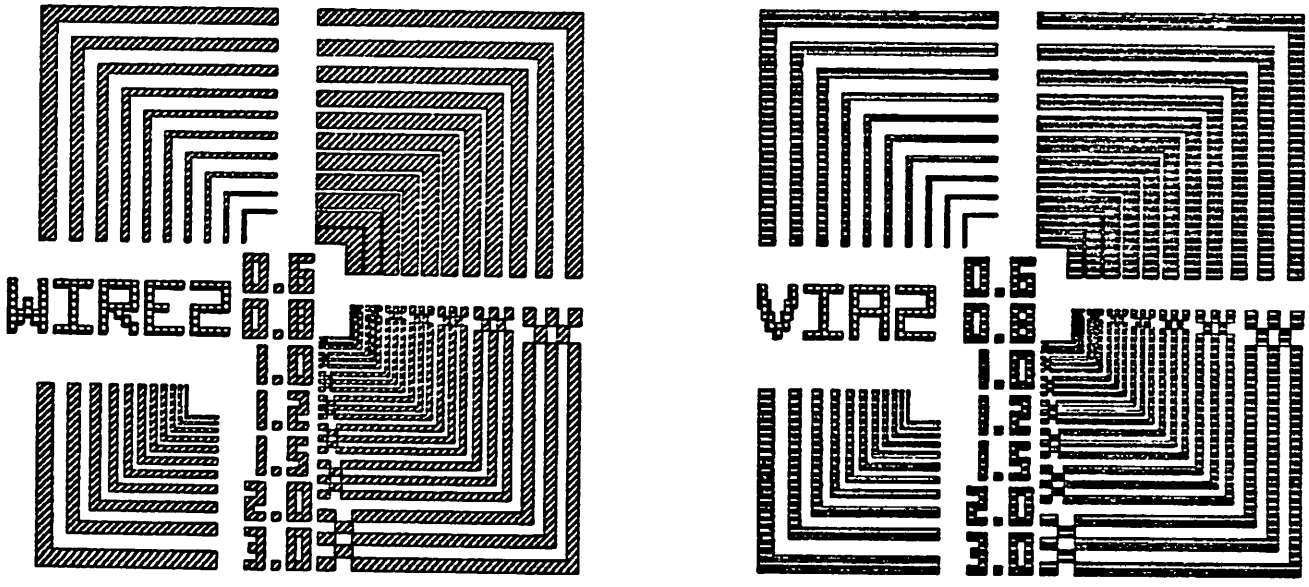


Figure 8. Expanded Layout of two Elbow Structures

5.2. Verniers

5.2.1. Filename:

verniers

5.2.2. Purpose:

Measure the alignment between layers. Determine usefulness of new vernier structure.

5.2.3. Description:

Two types of vernier structures are included on the test chip. Both types are layed out in a new fashion which allows one to easily determine the alignment of a particular layer. The location of the structures is very consistant which allows them to be easily located on the die. Each level of the layout has its own complete set of verniers. This provides some redundancy, but allows the desired vernier structure to be easily located.

The two types of vernier structures are the Tapered Column Structure and the Standard Offset Block Structure. Both types are included for all levels for comparison purposes.

5.2.4. Testing Method:

Visual inspection of which pair of blocks line up the best. The distance from the center (larger block) indicates the number of .1um steps of misalignment. For the tapered columns the distance from the center of the symmetrical points on either side divided by two indicate the number of .1um steps of misalignment.

5.2.5. Test Pad Assignments:

none

5.2.6. Location:

Column 1, Row 1

5.2.7. References:

E290O test structures (block structures only)

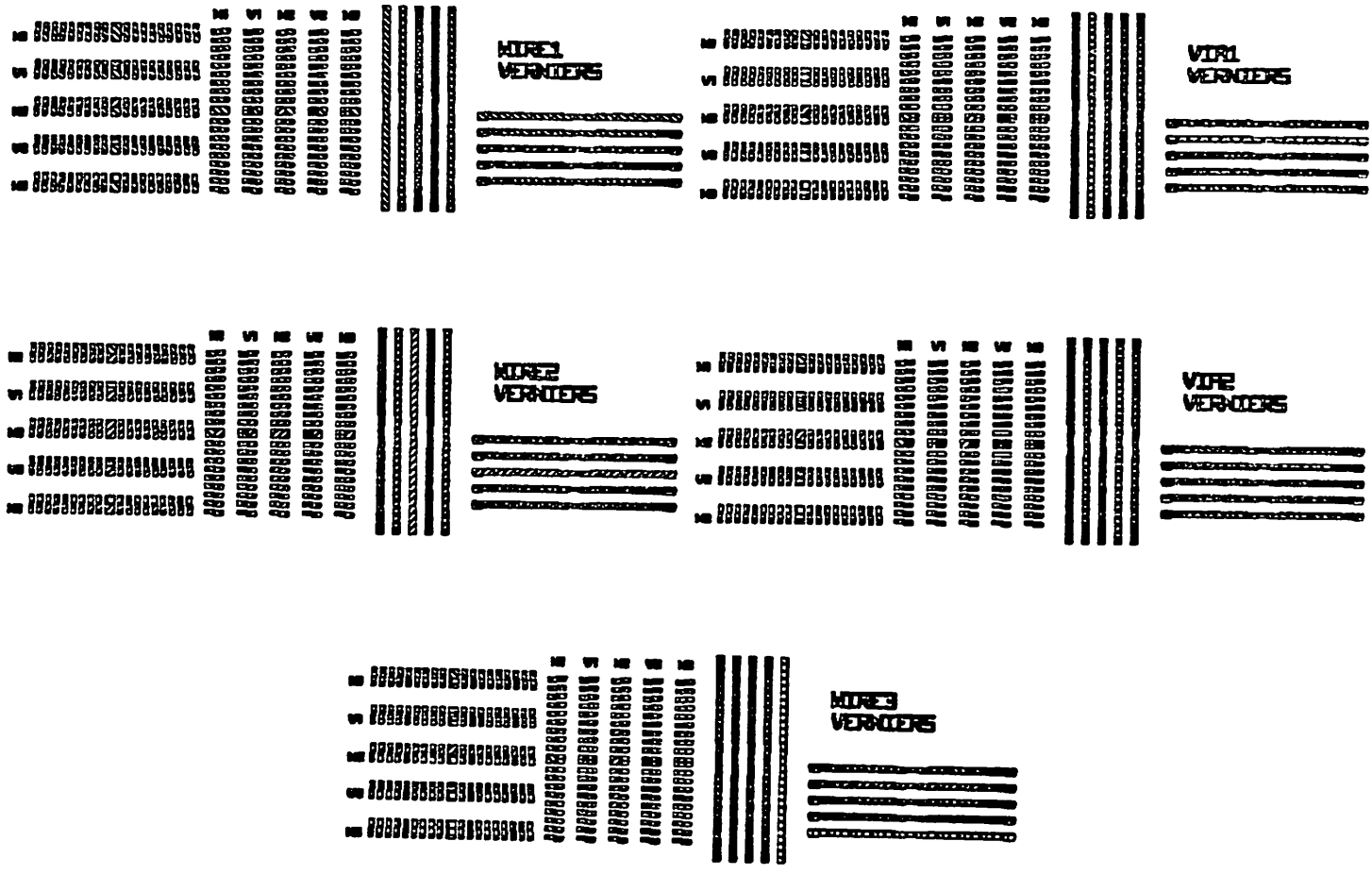


Figure 9. Layout of Vernier Structures

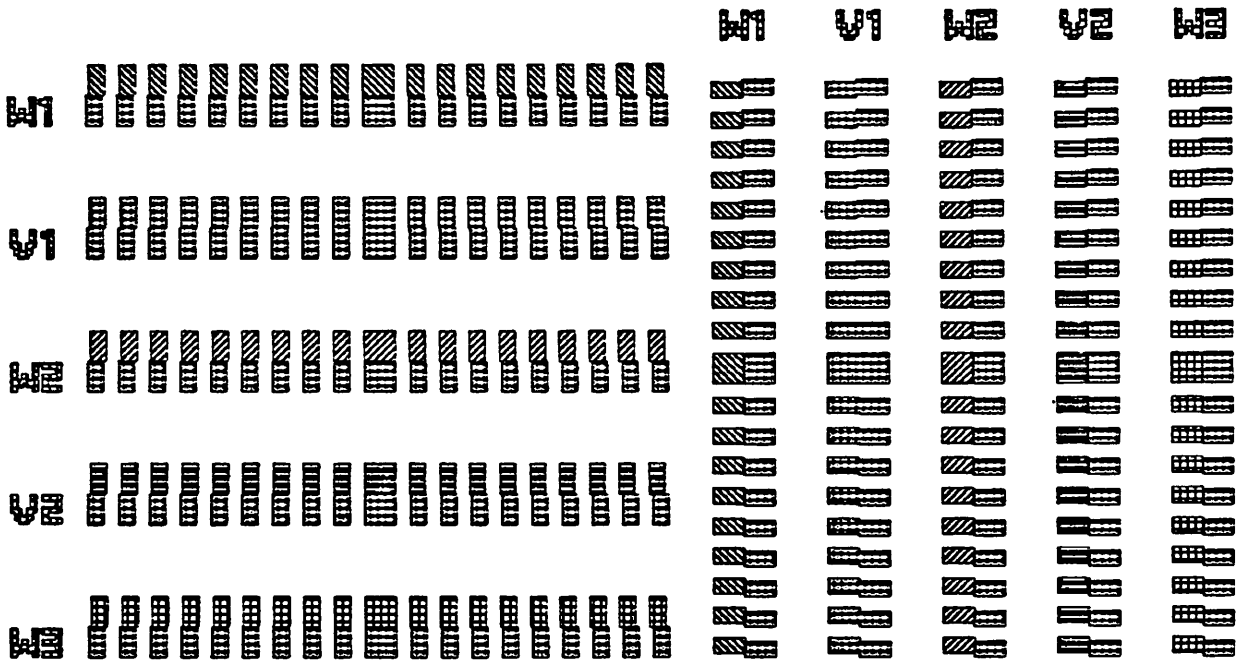


Figure 10. Expanded Layout of a single Standard Vernier Structure

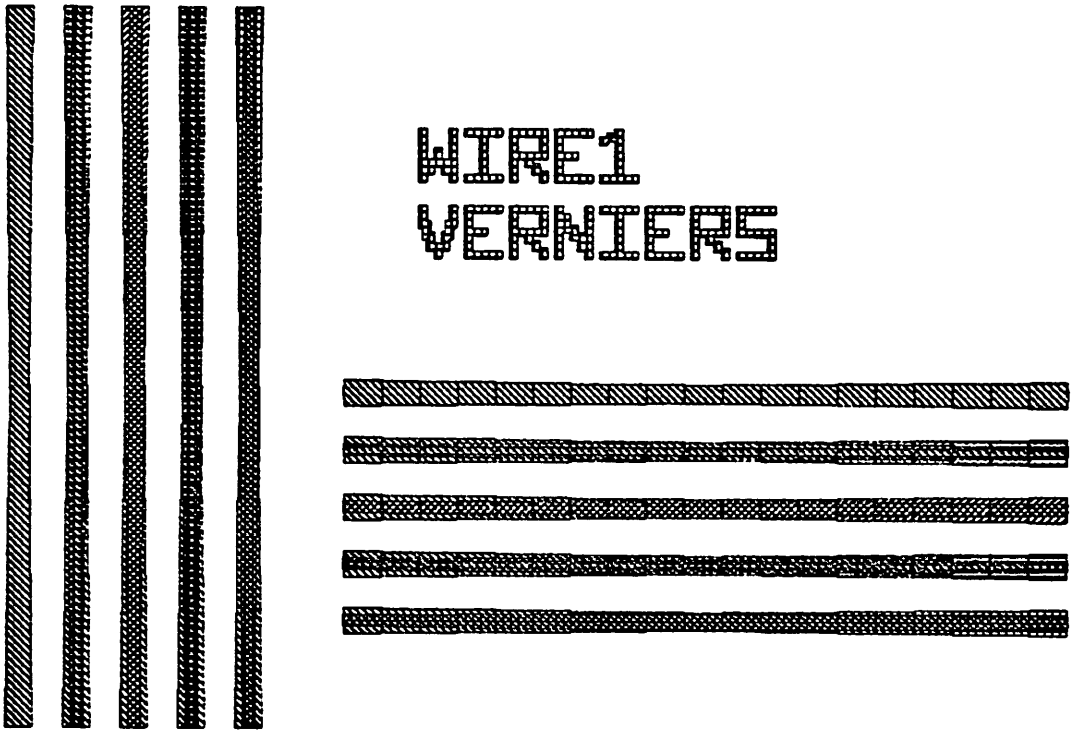


Figure 11. Expanded Layout of a single Tapered Column Structure

5.3. Van Der Pauws -- Sheet Resistance

5.3.1. Filename:

sheet1

5.3.2. Purpose:

Measure the sheet resistance of any of the five layers

5.3.3. Description:

Standard Van Der Pauw four point symmetrical structure

5.3.4. Testing Method:

Force current through two of four pads and measure voltage at the other two. See Discussion Section for details. The sheet resistance is given by:

Sheet Resistance = ((V1 - V2) / I) * pi / ln(2)

Where I is the forced current through two adjacent pads and V1 and V2 are the voltages sensed at the other two pads. Note that multiple measurements should be taken and averaged.

5.3.5. Test Pad Assignments:

Van Der Pauw -- Sheet Resistance			
Padset	Pad	Name	Function
1	1	W1PAD1	Wire1 level Pad #1
	2	W1PAD2	Wire1 level Pad #2
	3	W2PAD1	Wire2 level Pad #1
	4	W2PAD2	Wire2 level Pad #2
	5	W3PAD1	Wire3 level Pad #1
	6	W3PAD2	Wire3 level Pad #2
	7	V1PAD1	Via1 level Pad #1
	8	V1PAD2	Via1 level Pad #2
	9	V2PAD1	Via2 level Pad #1
	10	V2PAD2	Via2 level Pad #2
	11	V2PAD3	Via2 level Pad #3
	12	V2PAD4	Via2 level Pad #4
	13	V1PAD3	Via1 level Pad #3
	14	V1PAD4	Via1 level Pad #4
	15	W3PAD3	Wire3 level Pad #3
	16	W3PAD4	Wire3 level Pad #4
	17	W2PAD3	Wire2 level Pad #3
	18	W2PAD4	Wire2 level Pad #4
	19	W1PAD3	Wire1 level Pad #3
	20	W1PAD4	Wire1 level Pad #4

Table 3. Van Der Pauw Pad Assignments

5.3.6. Location:

Column 2, Row 7

5.3.7. References:

E290O test structures

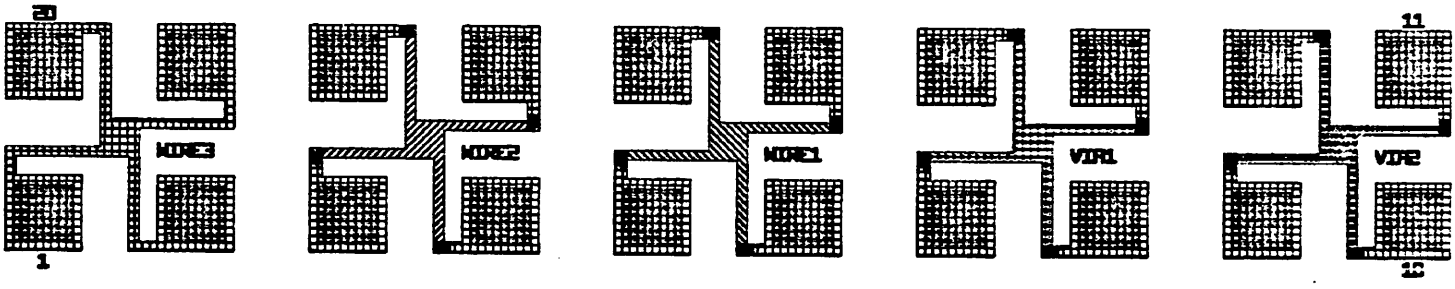


Figure 12. Layout of Van Der Pauw Structures

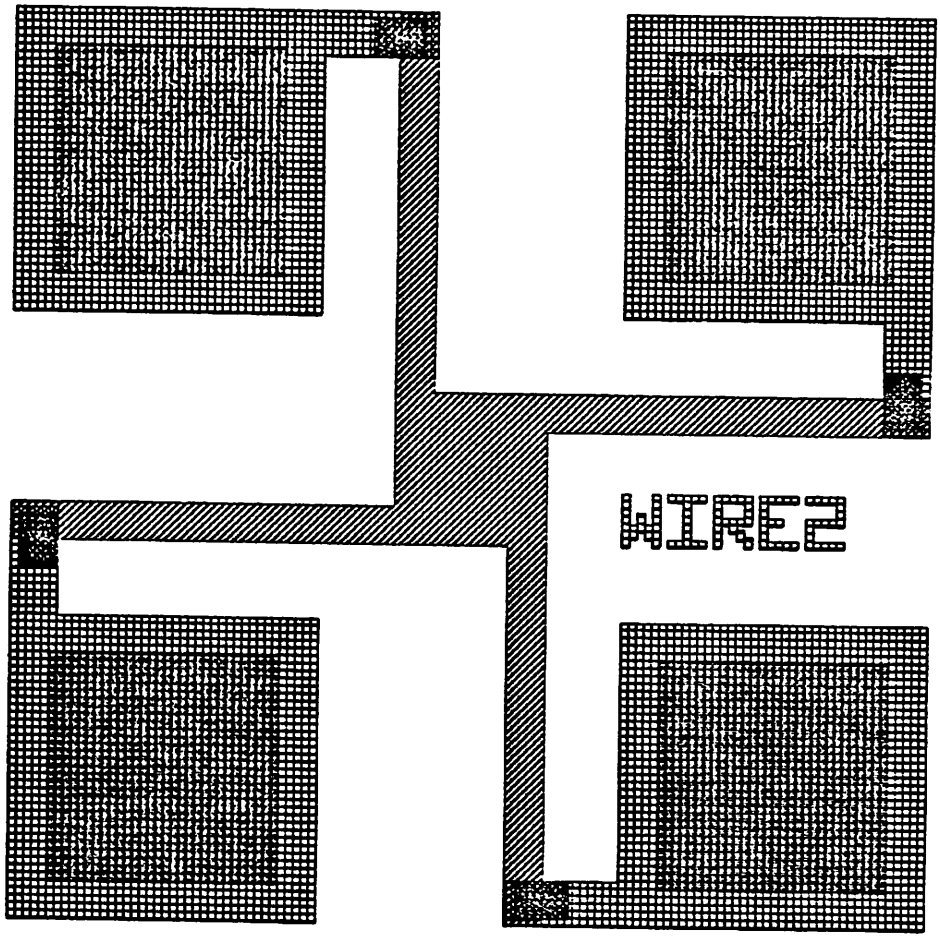


Figure 13. Expanded Layout of a single Van Der Pauw Structure

5.4. Via Resistance

5.4.1. Filename:

contactres1, contactres2

5.4.2. Purpose:

Measure the resistance of various size vias in the Via1 and Via2 layers

5.4.3. Description:

Standard four probe structure. Force current and measure voltage.

5.4.4. Testing Method:

Force current through two of four pads and measure voltage at the other two. See Discussion Section for details

5.4.5. Test Pad Assignments:

Via Resistance for Via1 level			
Padset	Pad	Name	Function
1	1	Via1PAD1	4um via Pad #1
	2	Via1PAD2	4um via Pad #2
	3	Via2PAD1	3um via Pad #1
	4	Via2PAD2	3um via Pad #2
	5	Via3PAD1	2um via Pad #1
	6	Via3PAD2	2um via Pad #2
	7	Via4PAD1	1.6um via Pad #1
	8	Via4PAD2	1.6um via Pad #2
	9	Via5PAD1	1.2um via Pad #1
	10	Via5PAD2	1.2um via Pad #2
	11	Via5PAD3	1.2um via Pad #3
	12	Via5PAD4	1.2um via Pad #4
	13	Via4PAD3	1.6um via Pad #3
	14	Via4PAD4	1.6um via Pad #4
	15	Via3PAD3	2um via Pad #3
	16	Via3PAD4	2um via Pad #4
	17	Via2PAD3	3um via Pad #3
	18	Via2PAD4	3um via Pad #4
	19	Via1PAD3	4um via Pad #3
	20	Via1PAD4	4um via Pad #4

Table 4. Via Resistance Pad Assignments for Via1 Level

The Via2 level pad assignments are identical.

5.4.6. Location:

Column 4, Row 10
Column 4, Row 11

5.4.7. References:

Finetti et. al.

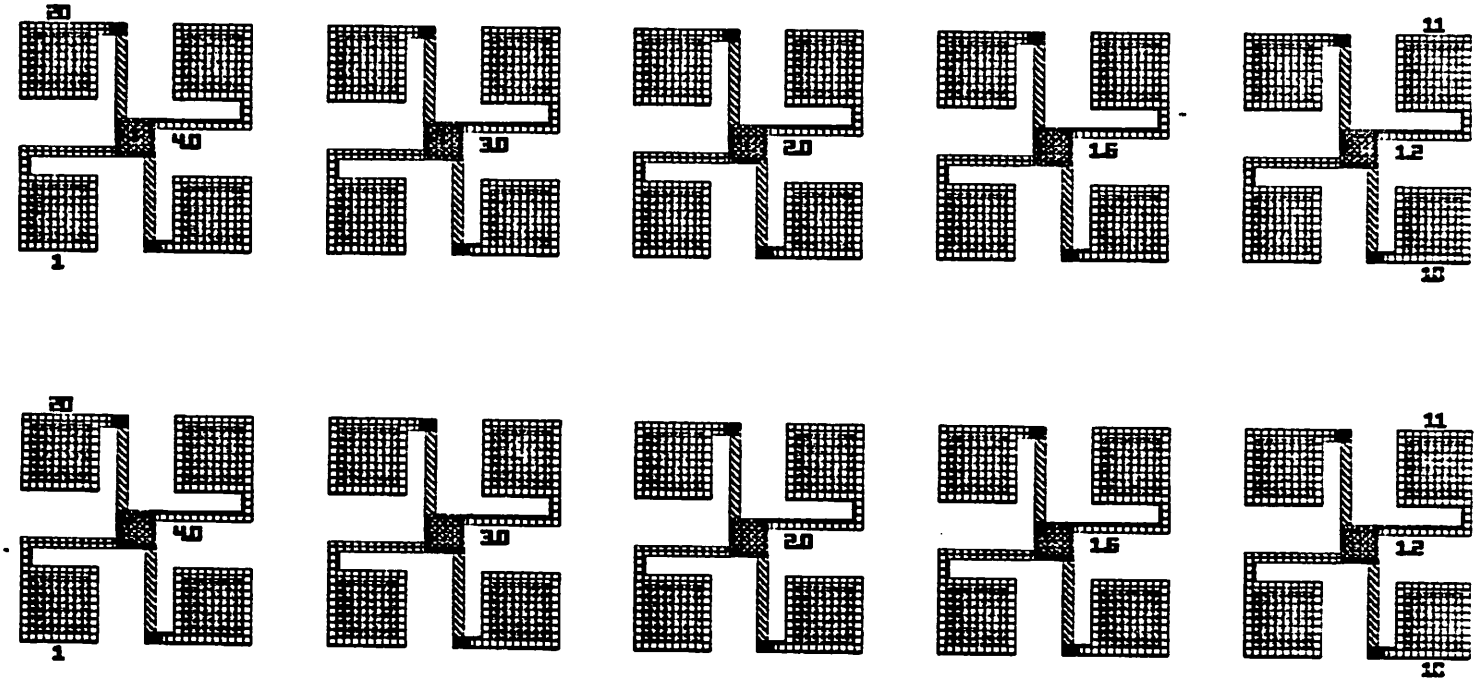


Figure 14. Layout of Via Resistance Structures (Via1 top, Via2 bottom)

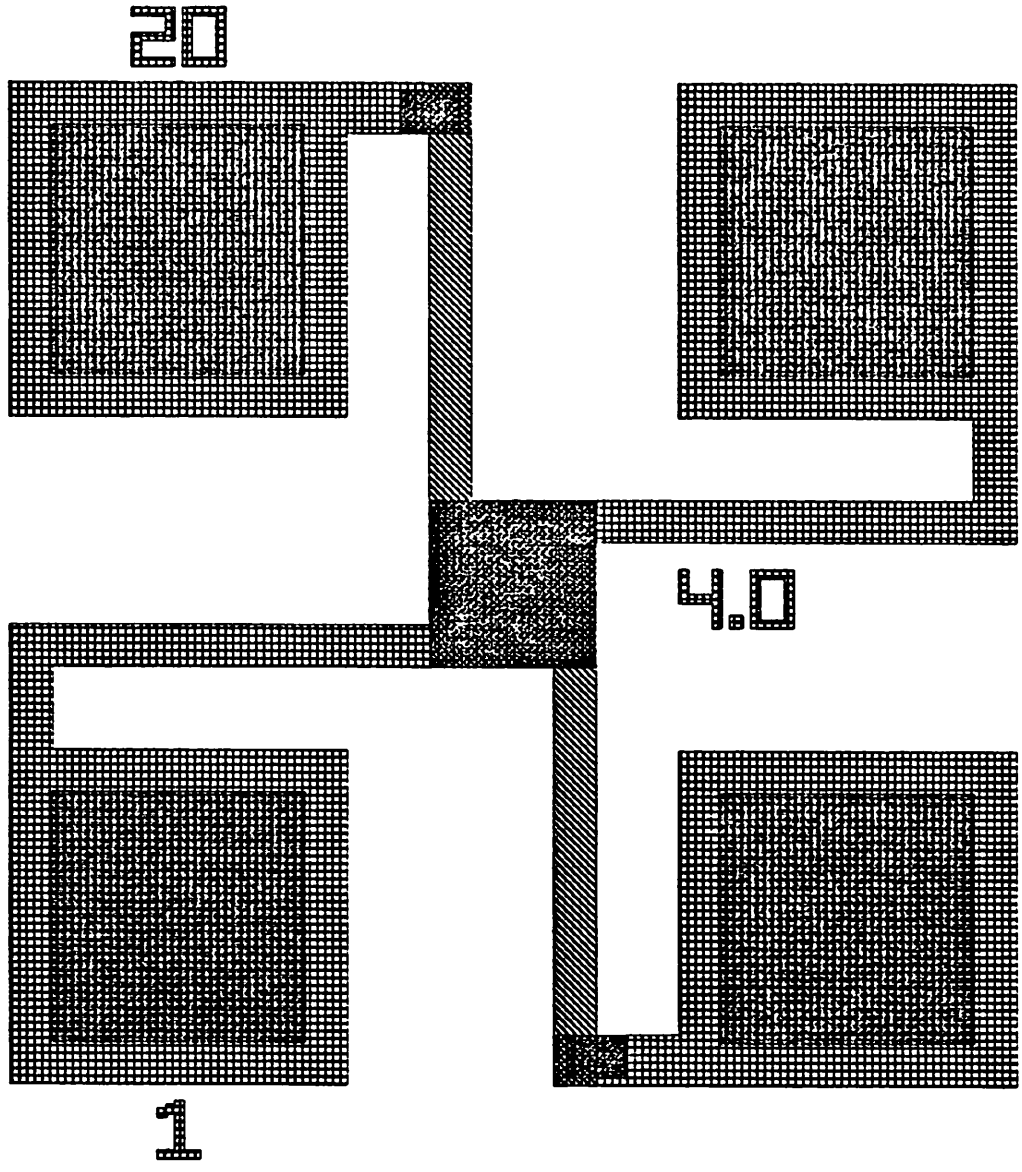


Figure 15. Expanded Layout of a single Via Resistance Structure

5.5. Via Chains

5.5.1. Filename:

con1,con2,con3,con4,con5,con6,con7,con8

5.5.2. Purpose:

Determine the reliability of various size vias. Determine the via yield. Determine the average via resistance. Monitor N-Level Metal Planarity. Determine feasibility of stacked vias.

5.5.3. Description:

A large arrays of vias forming a chains. Three types of via structures are included: Multi-Level Staggered Vias, Multi-Level Vertical Vias, and Two Level Vias. See discussion section for details on via chain types. Each type of via includes chains with via sizes of 4.0um, 3.0um, 2.0um, 1.5um, and 1.2um.

5.5.4. Testing Method:

Testing is accomplished by simply reading the resistance of the vias from two points on the chain. Any two points on the chain may be utilized depending upon the number of contacts one desires to measure.

5.5.5. Test Pad Assignments:

The pad assignments for the via chains are established as follows. Each location listed in the table below contains a pad set. The pad set contains the pads for two via chains (termed upper and lower). The via chains connected to each pad set are listed below. A table immediately after indicates which pads are connected to which points on which via chain.

Via Chain Location and Type			
Padset			
Row	Column	Upper Chain type	Lower Chain Type
2	4	3.0um Vertical	4.0um Vertical
2	5	2.0um Vertical	1.6um Vertical
5	4	1.2um Vertical	3.0um Vertical
5	5	3.0um Two-Level	4.0um Two-Level
8	4	2.0um Two-Level	1.6um Two-Level
8	5	1.2um Two-Level	1.2um Staggered
12	4	3.0um Staggered	4.0um Staggered
12	5	2.0um Staggered	1.6um Staggered

Table 5. Via Chain Type and Location

Via Chain Pad Assignments			
Padset	Pad	Name	Function
1	1	start	Start of upper via chain
	20	utap1	upper via chain 40 contact tap
	2	utap2	upper via chain 80 contact tap
	19	utap3	upper via chain 160 contact tap
	3	utap4	upper via chain 320 contact tap
	18	utap5	upper via chain 640 contact tap
	4	utap6	upper via chain 1280 contact tap
	17	utap7	upper via chain 3200 contact tap
	16	utap8	upper via chain 2560 contact tap
	11	lstart	Start of lower via chain
	10	ltap1	lower via chain 40 contact tap
	12	ltap2	lower via chain 80 contact tap
	9	ltap3	lower via chain 160 contact tap
	13	ltap4	lower via chain 320 contact tap
	8	ltap5	lower via chain 640 contact tap
	14	ltap6	lower via chain 1280 contact tap
	7	ltap7	lower via chain 3200 contact tap
	6	ltap8	lower via chain 2560 contact tap

Table 6. Via Chain Pad Assignments

5.5.6. Location:

Column 4-5, Row 1-13

5.5.7. References:

none

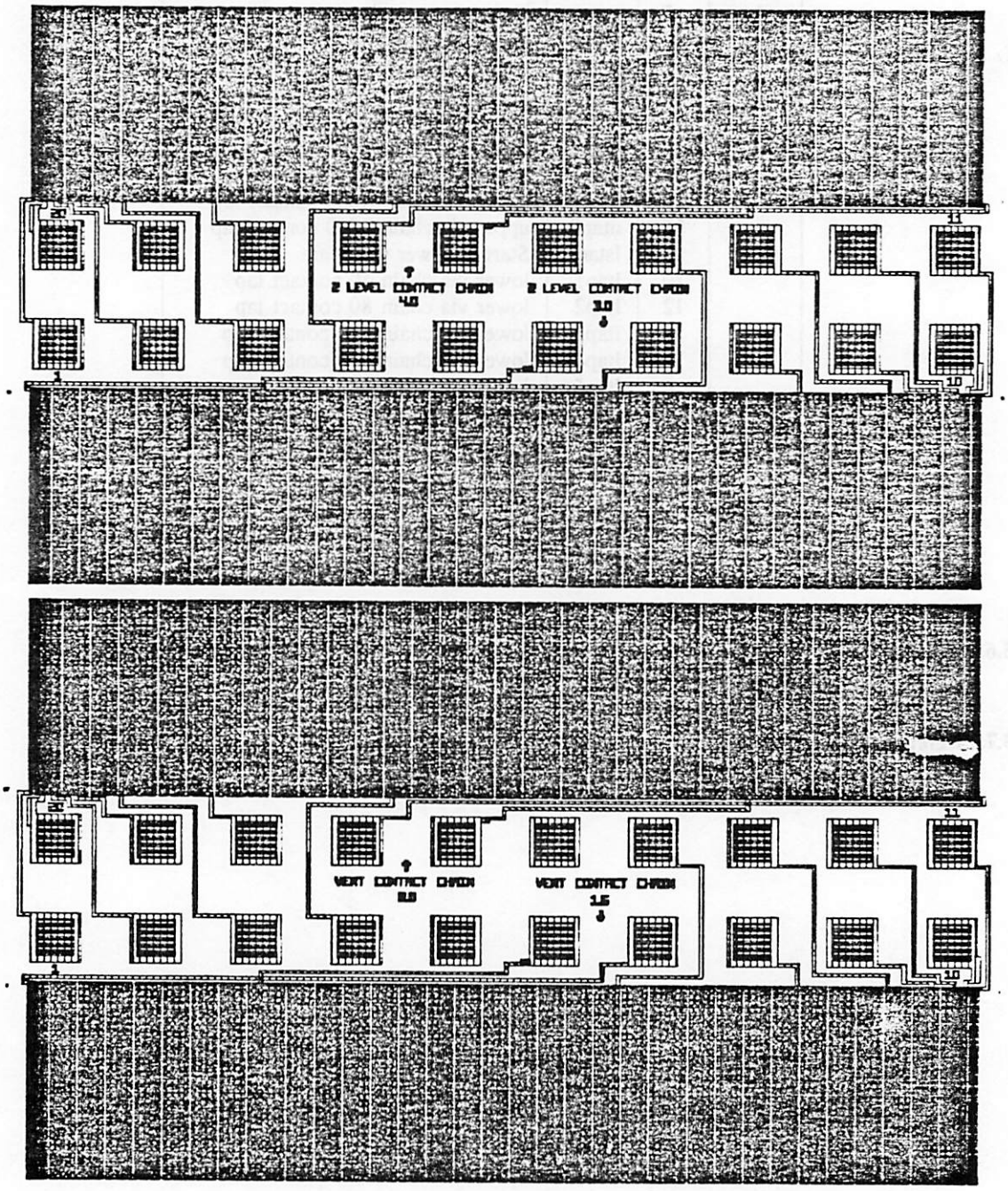


Figure 16. Layout of Via Chain

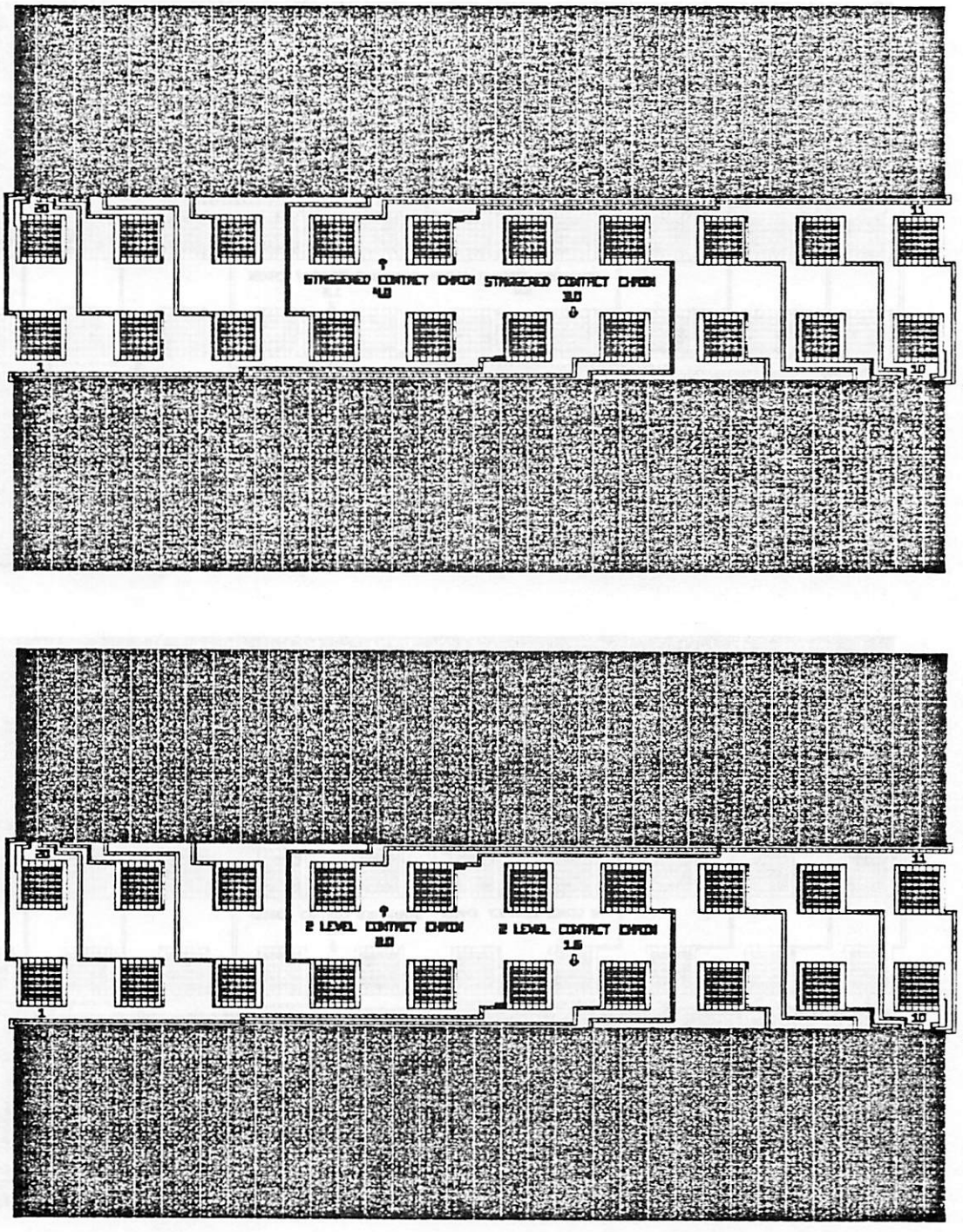


Figure 17. Layout of Via Chain (continued)

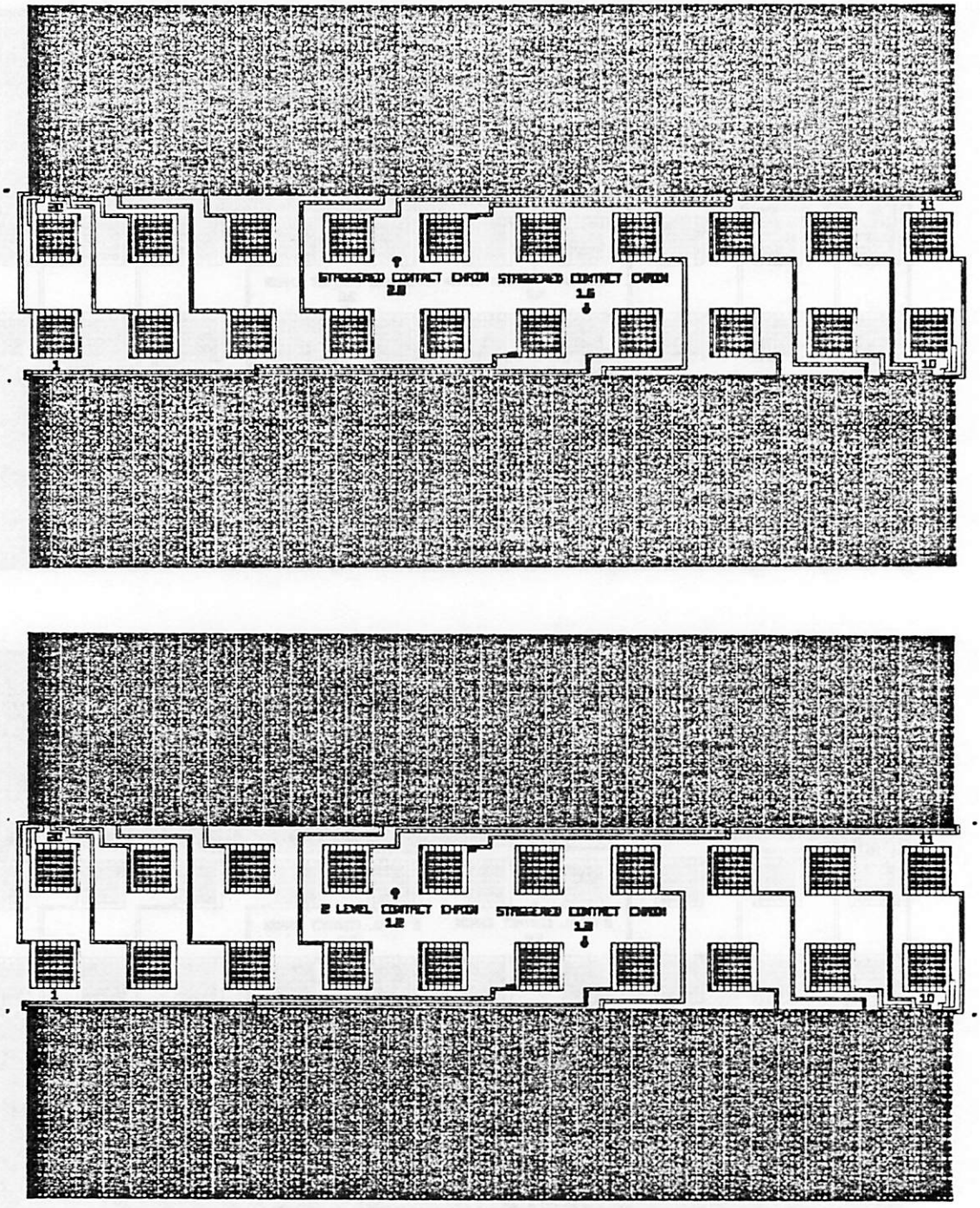


Figure 18. Layout of Via Chain (continued)

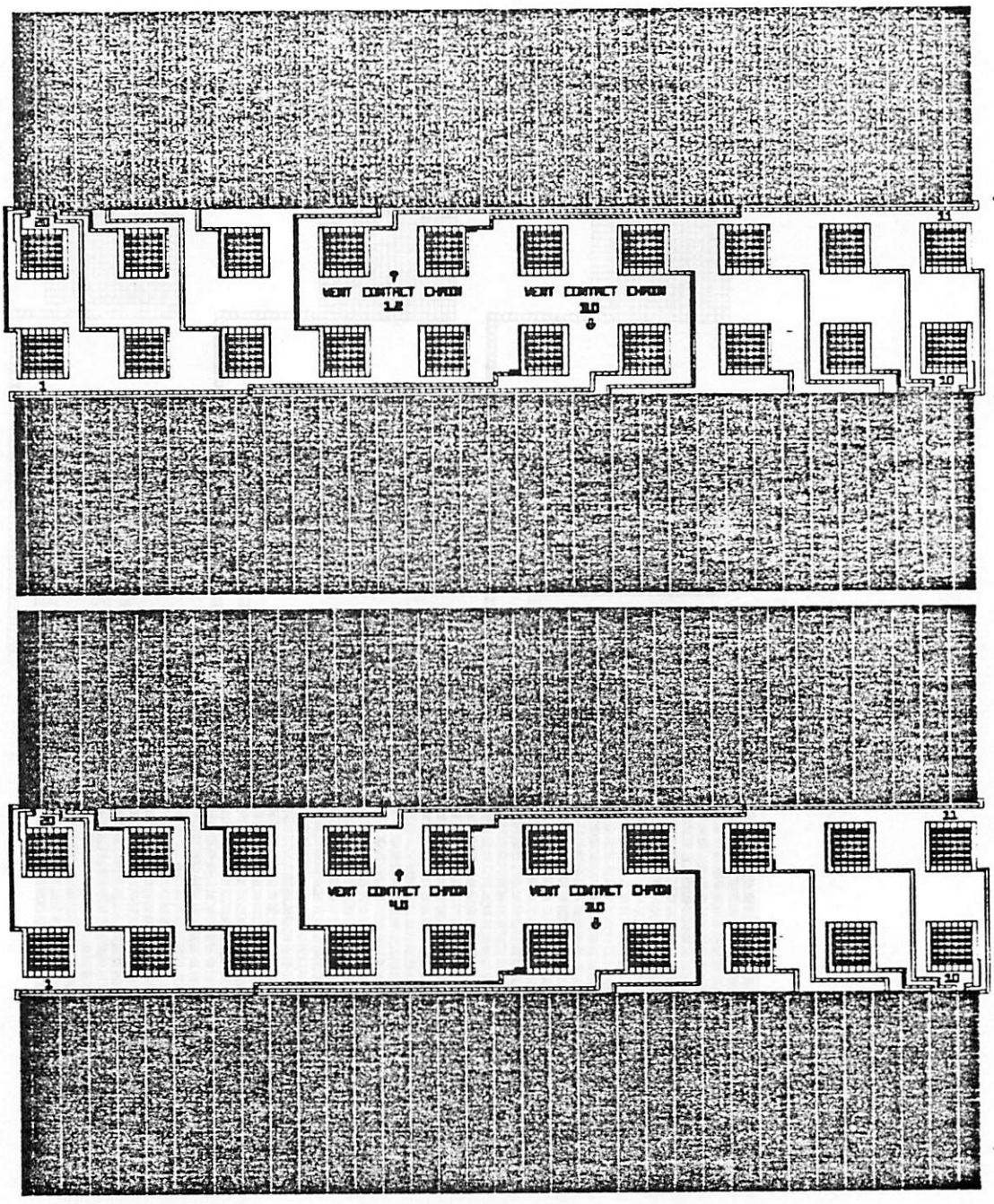


Figure 19. Layout of Via Chain (continued)

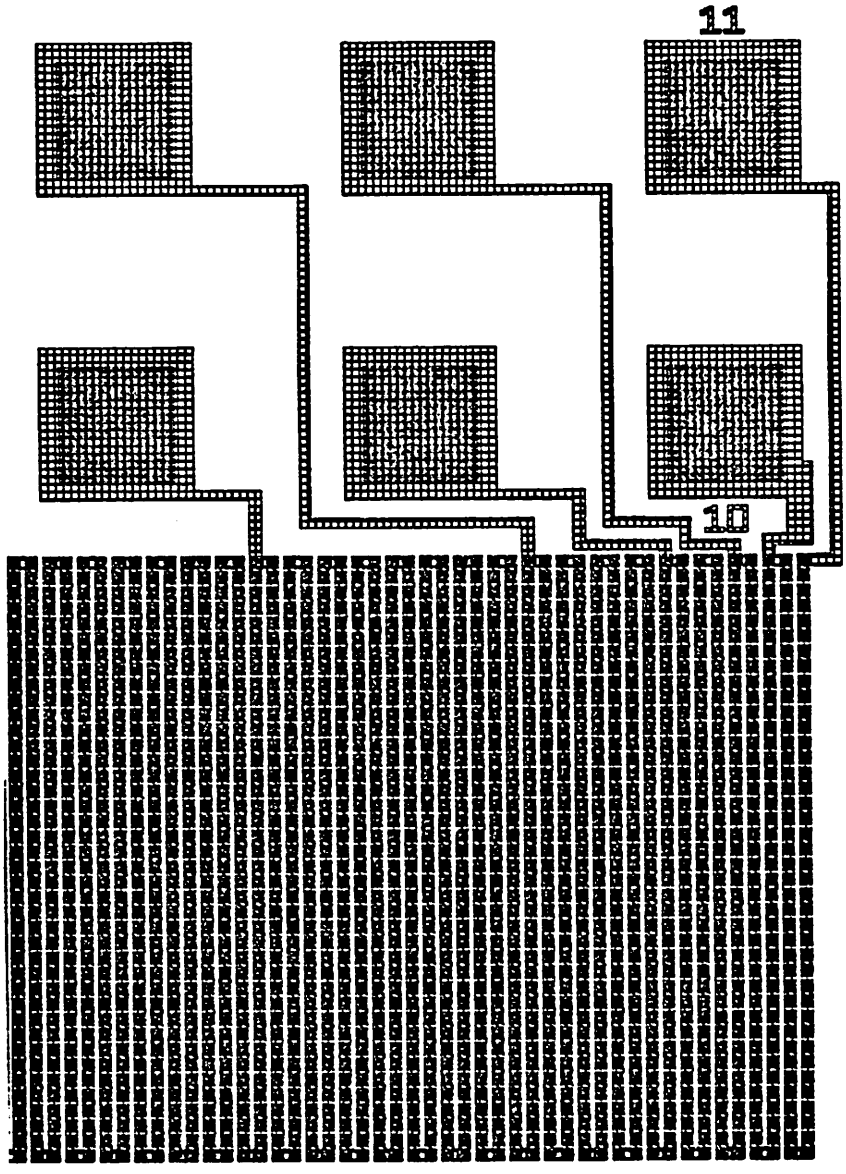


Figure 20. Expanded Layout of Via Chain

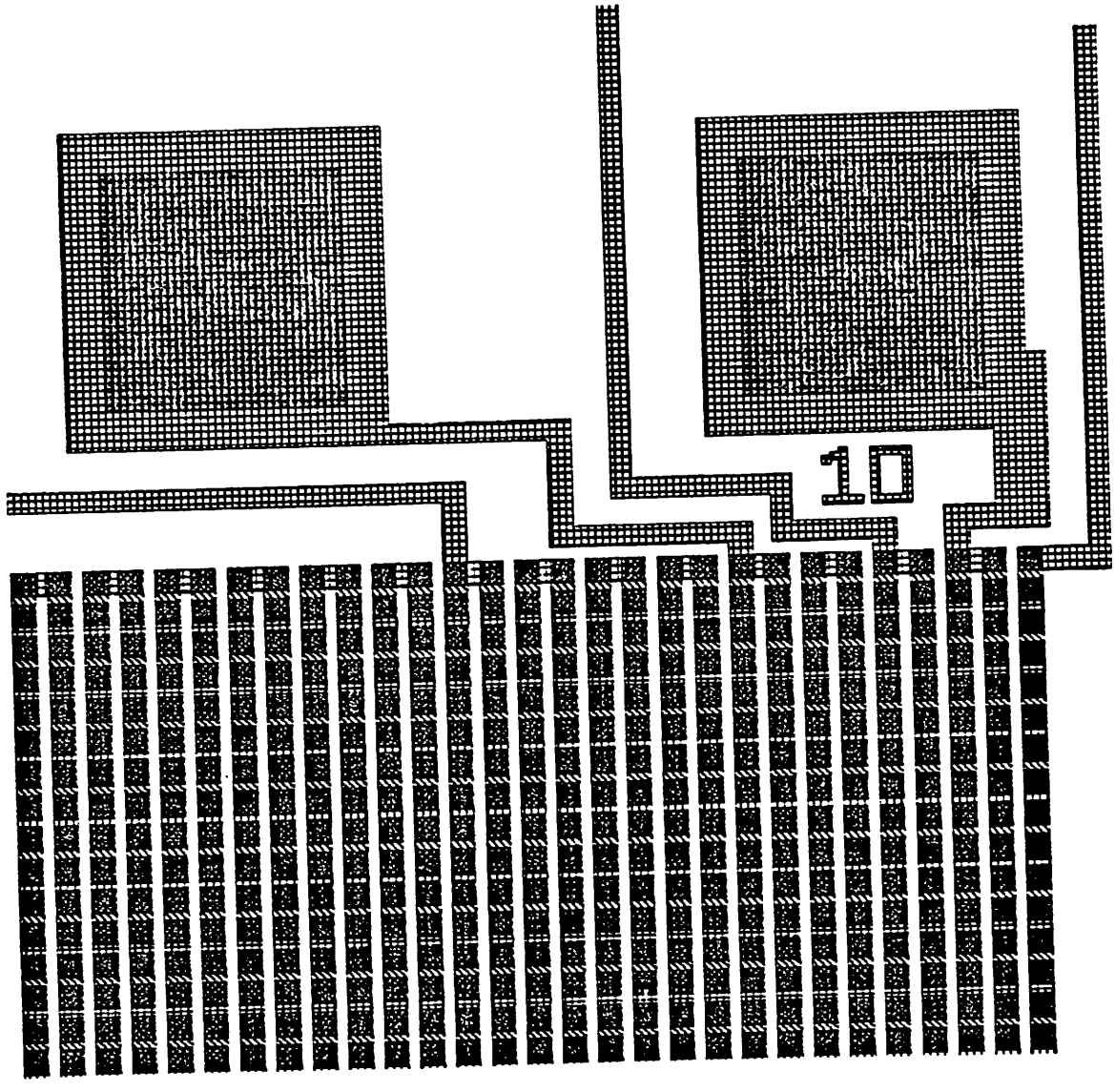


Figure 21. Expanded Layout of Via Chain

5.6. Metal Interleaved Combs

5.6.1. Filename:

combs.s06, combs.s08, combs.s10, combs.s12, combs.s15

5.6.2. Purpose:

Detect overfilled metal channels for electroless plating. Detect unlifted bridges from adjacent metal lines for a lift-off process. Detect interlevel shorts over topography. Determine capacitance between parallel metal lines.

5.6.3. Description:

Two sets of interleaved combs. One set parallel to padset, one perpendicular on next level.

5.6.4. Testing Method:

Apply voltage between two pads and check for open or short.

5.6.5. Test Pad Assignments:

Interleaved Combs			
Padset	Pad	Name	Function
1	1	W1W3PAD1	Wire1, Wire3 levels Pad #1
	20	W1W3PAD2	Wire1, Wire3 levels Pad #2
	2	W2PAD1	Wire2 level Pad #1
	19	W2PAD2	Wire2 level Pad #2

Table 7. Interleaved Combs Pad Assignments

5.6.6. Location:

Column 16, Row 1-5

5.6.7. References:

E2900 test structures

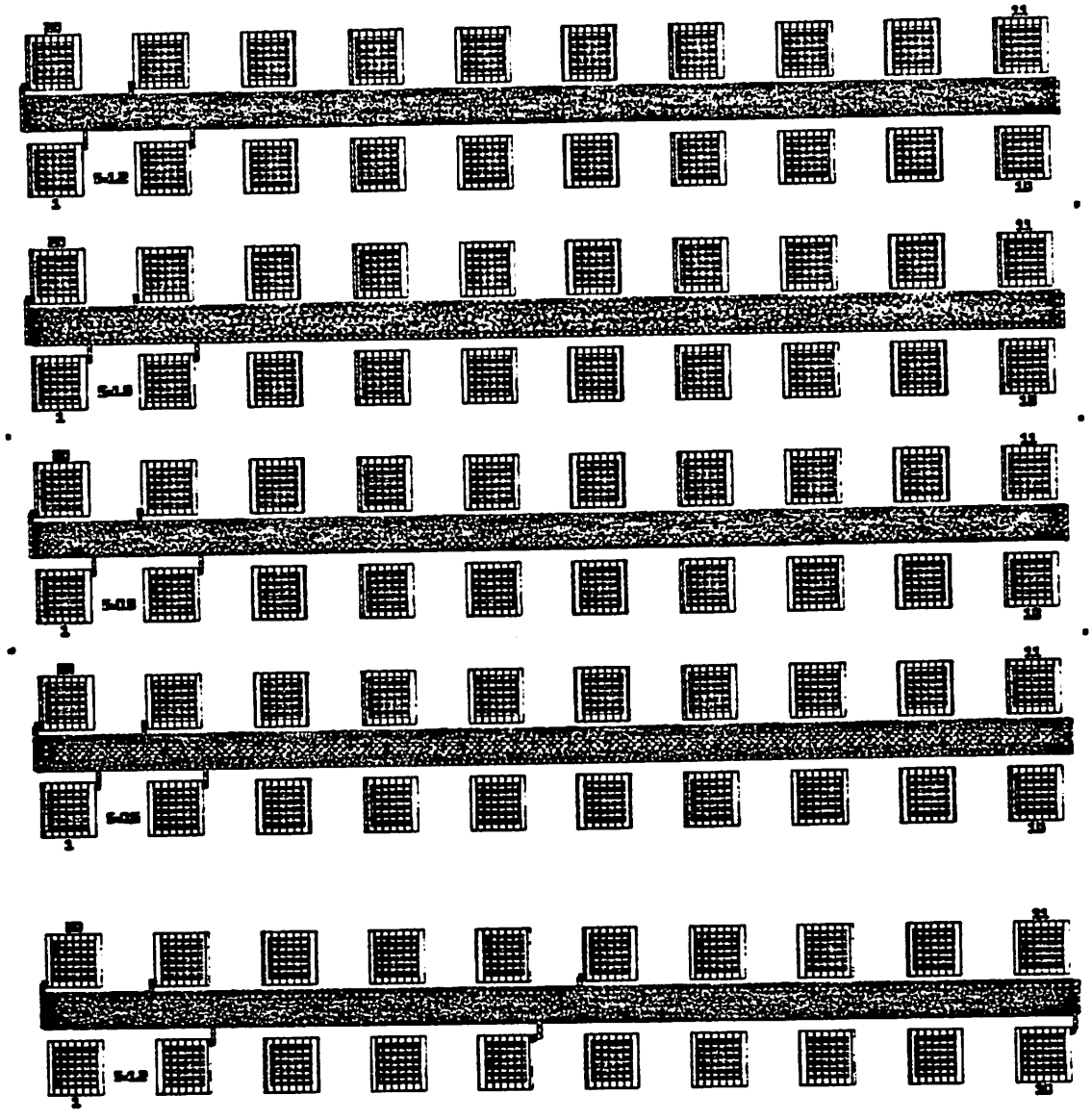


Figure 22. Layout of Interleaved Combs

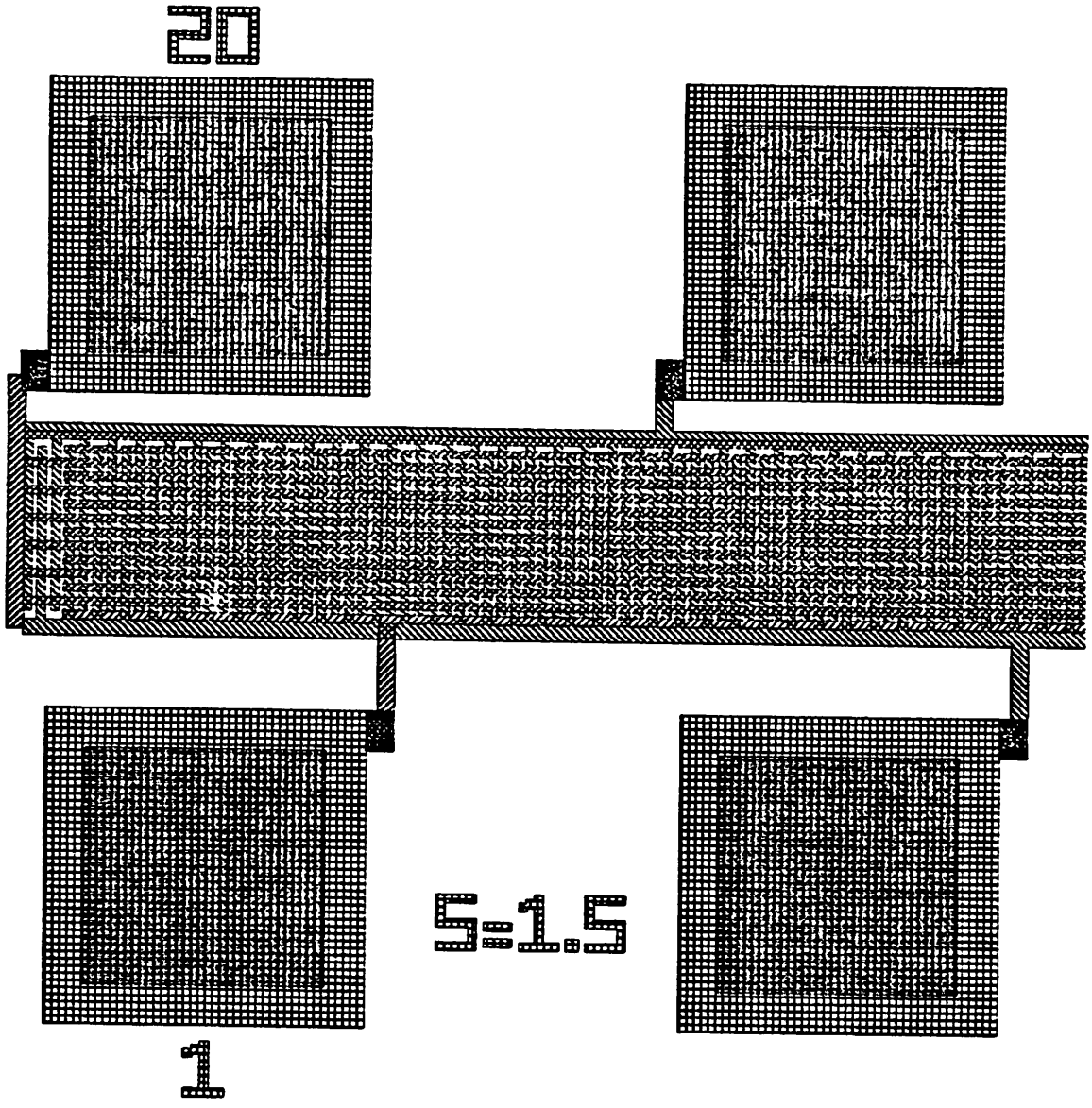


Figure 23. Expanded Layout of Interleaved Combs

5.7. Multi Level Serpentines

5.7.1. Filename:

snakes.s06, snakes.s08, snakes.s10, snakes.s12, snakes.s15

5.7.2. Purpose:

Detect openings in long metal lines, with and without underlying topography. Detect shorts between levels.

5.7.3. Description:

Long meandering lines running in one direction on one level and in perpendicular direction on next level so step coverage can be examined.

5.7.4. Testing Method:

Apply voltage between two pads and check for open or short.

5.7.5. Test Pad Assignments:

Multi Level Serpentines			
Padset	Pad	Name	Function
1	10	W1W3PAD1	Wire1, Wire3 levels Pad #1
	20	W1W3PAD2	Wire1, Wire3 levels Pad #2
	2	W2PAD1	Wire2 level Pad #1
	19	W2PAD2	Wire2 level Pad #2

Table 8. Multi Level Serpentines Pad Assignments

5.7.6. Location:

Column 12-15, Row 6

5.7.7. References:

E2900 test structures

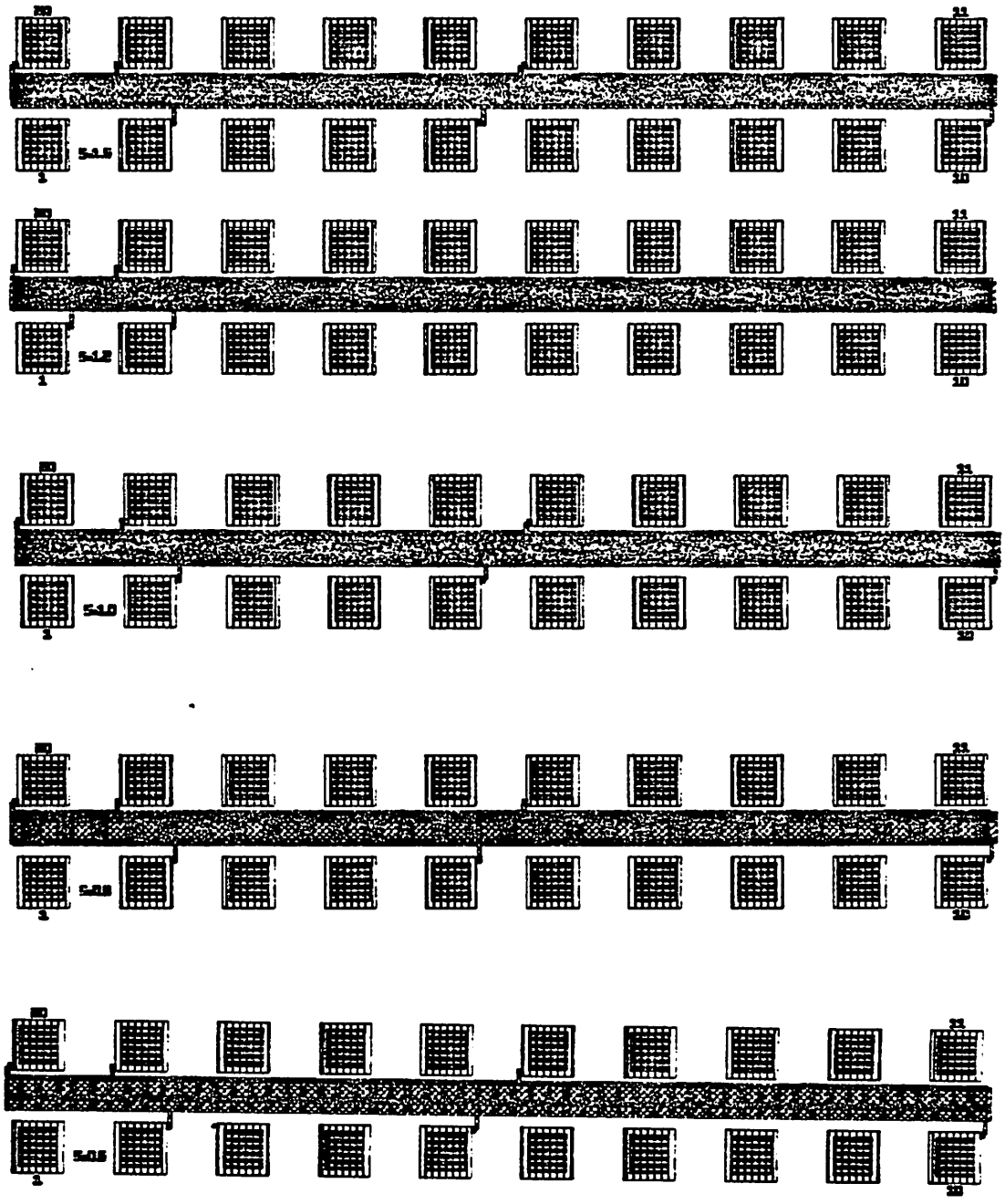


Figure 24. Layout of Multi Level Serpentines

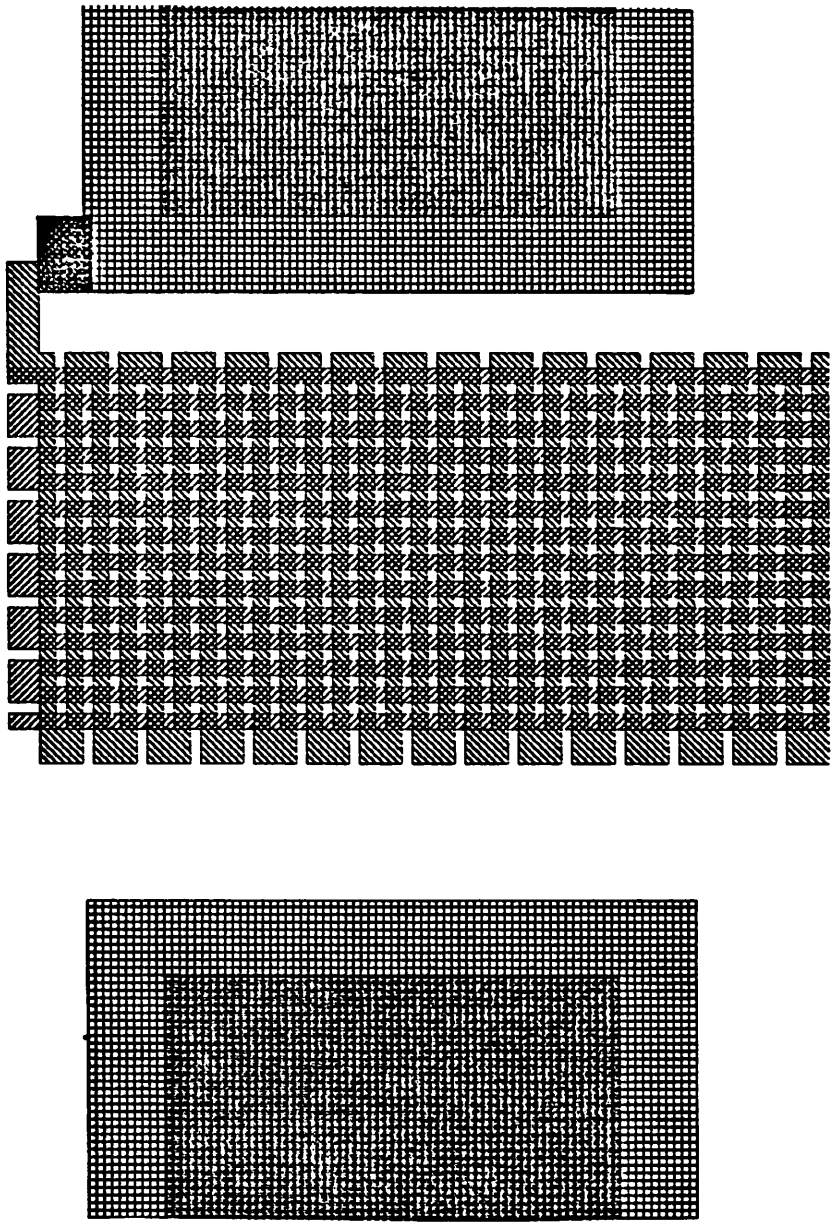


Figure 25. Expanded Layout of Multi Level Serpentines

5.8. Capacitors

5.8.1. Filename:

cap1, cap2, cap4, cap5

5.8.2. Purpose:

Measure the dielectric thickness, breakdown voltage, defect density, interlevel capacitance, and fringe capacitance.

5.8.3. Description:

Parallel plate capacitors between all possible layers varying in size. Fringe capacitors between all possible layers.

5.8.4. Testing Method:

Measure capacitance between to test pads. Subtract capacitance measured on two reference pads to obtain actual between two layers. The dielectric thickness can be determined from the area of the capacitor (known) and the measure of capacitance.

Capacitance = Area * Eox / Tox

Where Eox is the dielectric constant and Tox is the thickness of the dielectric. Area is the effective area of the capacitor. The fringe capacitance is determine per unit length from the following:

C fringe = (Cmeasured - Cflat * L * W) / (2 * L)

Where Cmeasured is the measured value of capacitance, Cflat is the flat capacitor measurement obtained from the flat capacitor (per unit area), L is the length of the lines (see data below) and W is the width of the lines (4 microns).

Breakdown voltage can be measured by increasing the voltage on the two pads until a large increase in current occurs.

Defect density can be measured by probing capacitors on wafer and taking statistics on the number of capacitors which are shorted.

5.8.5. Test Pad Assignments:

Flat Capacitors				
Padset				
Row	Column	Pad	Name	Function
8	1	1	W1W3.1	Wire1 to Wire3 Capacitor 226256 Square microns
		20	W1W3.2	Wire1 to Wire3 Capacitor 226256 Square microns
		6	W1W3.1	Wire1 to Wire3 Capacitor Reference
		15	W1W3.2	Wire1 to Wire3 Capacitor Reference
		8	W2W3.1	Wire2 to Wire3 Capacitor 226256 Square microns
		13	W2W3.2	Wire2 to Wire3 Capacitor 226256 Square microns
		3	W2W3.1	Wire2 to Wire3 Capacitor Reference
		18	W2W3.2	Wire2 to Wire3 Capacitor Reference
8	2	1	W1W2.1	Wire1 to Wire2 Capacitor 226256 Square microns
		20	W1W2.2	Wire1 to Wire2 Capacitor 226256 Square microns
		6	W1W2.1	Wire1 to Wire2 Capacitor Reference
		15	W1W2.2	Wire1 to Wire2 Capacitor Reference
		8	V1W3.1	Via1 to Wire3 Capacitor 226256 Square microns
		13	V1W3.2	Via1 to Wire3 Capacitor 226256 Square microns
		3	V1W3.1	Via1 to Wire3 Capacitor Reference
		18	V1W3.2	Via1 to Wire3 Capacitor Reference
8	3	1	W1V2.1	Wire1 to Via2 Capacitor 226256 Square microns
		20	W1V2.2	Wire1 to Via2 Capacitor 226256 Square microns
		6	W1V2.1	Wire1 to Via2 Capacitor Reference
		15	W1V2.2	Wire1 to Via2 Capacitor Reference
		8	V1V2.1	Via1 to Via2 Capacitor 226256 Square microns
		13	V1V2.2	Via1 to Via2 Capacitor 226256 Square microns
		3	V1V2.1	Via1 to Via2 Capacitor Reference
		18	V1V2.2	Via1 to Via2 Capacitor Reference

Table 9. Capacitor Pad Assignments

Fringe Capacitors				
Padset				
Row	Column	Pad	Name	Function
12	1	1	W1W3.1	Wire1 to Wire3 Capacitor 54000 microns
		20	W1W3.2	Wire1 to Wire3 Capacitor 54000 microns
		6	W1W3.1	Wire1 to Wire3 Capacitor Reference
		15	W1W3.2	Wire1 to Wire3 Capacitor Reference
		8	W2W3.1	Wire2 to Wire3 Capacitor 54000 microns
		13	W2W3.2	Wire2 to Wire3 Capacitor 54000 microns
		3	W2W3.1	Wire2 to Wire3 Capacitor Reference
		18	W2W3.2	Wire2 to Wire3 Capacitor Reference
12	2	1	W1W2.1	Wire1 to Wire2 Capacitor 54000 microns
		20	W1W2.2	Wire1 to Wire2 Capacitor 54000 microns
		6	W1W2.1	Wire1 to Wire2 Capacitor Reference
		15	W1W2.2	Wire1 to Wire2 Capacitor Reference
		8	V1W3.1	Via1 to Wire3 Capacitor 54000 microns
		13	V1W3.2	Via1 to Wire3 Capacitor 54000 microns
		3	V1W3.1	Via1 to Wire3 Capacitor Reference
		18	V1W3.2	Via1 to Wire3 Capacitor Reference
12	3	1	W1V2.1	Wire1 to Via2 Capacitor 54000 microns
		20	W1V2.2	Wire1 to Via2 Capacitor 54000 microns
		6	W1V2.1	Wire1 to Via2 Capacitor Reference
		15	W1V2.2	Wire1 to Via2 Capacitor Reference
		8	V1V2.1	Via1 to Via2 Capacitor 54000 microns
		13	V1V2.2	Via1 to Via2 Capacitor 54000 microns
		3	V1V2.1	Via1 to Via2 Capacitor Reference
		18	V1V2.2	Via1 to Via2 Capacitor Reference

Table 10. Fringe Capacitor Pad Assignments

Flat Capacitors (smaller sizes)				
Padset Row	Padset Column	Pad	Name	Function
19	1	1	W1W3.1	Wire1 to Wire3 Capacitor 4500 square microns
		20	W1W3.2	Wire1 to Wire3 Capacitor 4500 square microns
		2	W1W3.1	Wire1 to Wire3 Capacitor 4500 square microns
		19	W1W3.2	Wire1 to Wire3 Capacitor 4500 square microns
		3	W1W3.1	Wire1 to Wire3 Capacitor 2250 square microns
		18	W1W3.2	Wire1 to Wire3 Capacitor 2250 square microns
		4	W1W3.1	Wire1 to Wire3 Capacitor 1125 square microns
		17	W1W3.2	Wire1 to Wire3 Capacitor 1125 square microns
		7	W2W3.1	Wire2 to Wire3 Capacitor 4500 square microns
		14	W2W3.2	Wire2 to Wire3 Capacitor 4500 square microns
		8	W2W3.1	Wire2 to Wire3 Capacitor 4500 square microns
		13	W2W3.2	Wire2 to Wire3 Capacitor 4500 square microns
		9	W2W3.1	Wire2 to Wire3 Capacitor 1125 square microns
		12	W2W3.2	Wire2 to Wire3 Capacitor 1125 square microns
		10	W2W3.1	Wire2 to Wire3 Capacitor 2250 square microns
		11	W2W3.2	Wire2 to Wire3 Capacitor 2250 square microns

Table 11. Capacitor Pad Assignments

The pad assignments for the capacitors located at Row 19, Column 2 and Row 19, Column 3 are the same. The capacitor types are the same as for the Flat Capacitors.

5.8.6. Location:

Column 7-13, Row 1-3
Column 18-20, Row 1-3

5.8.7. References:

none

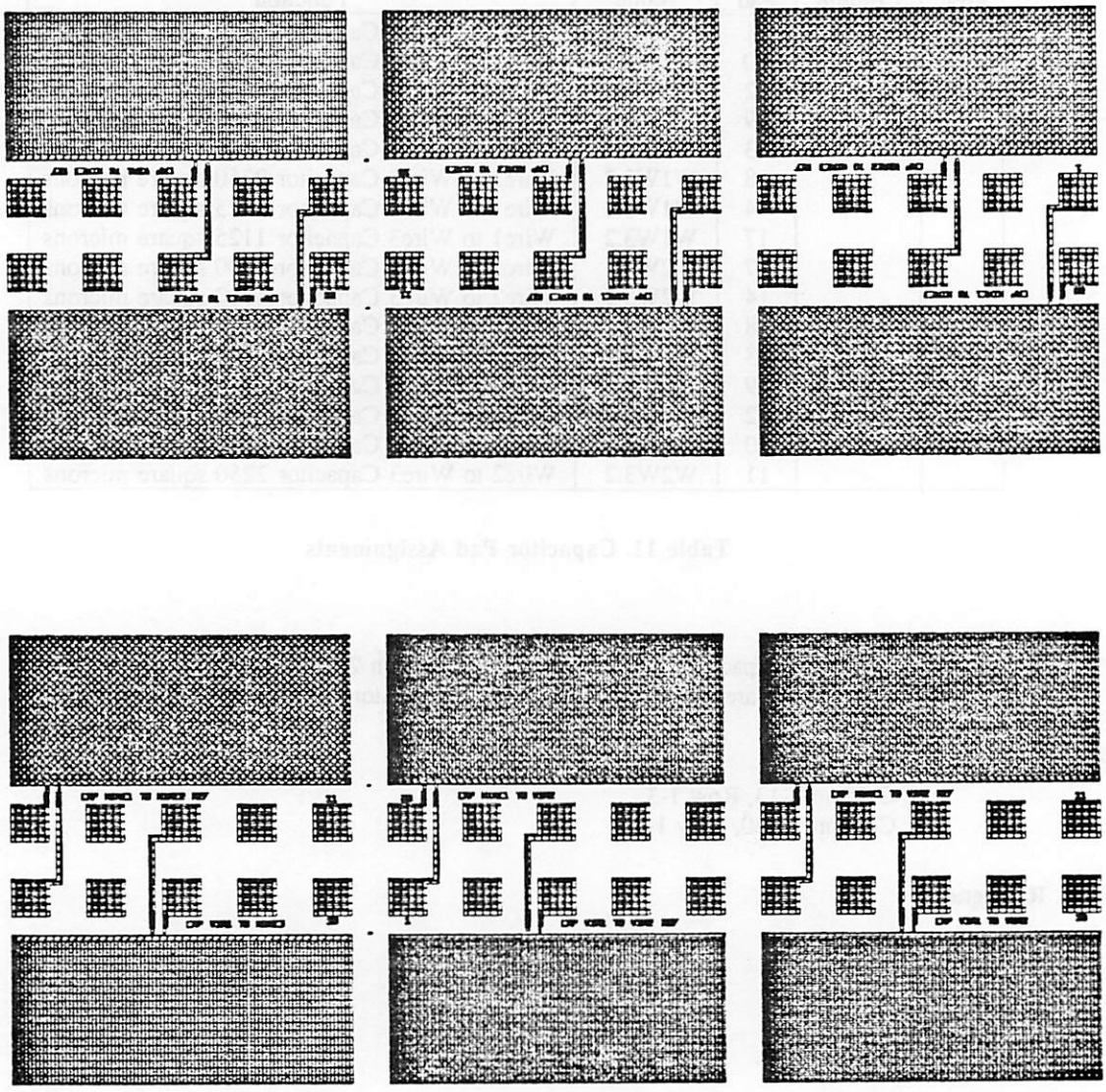


Figure 26. Layout of Flat Capacitor Structures

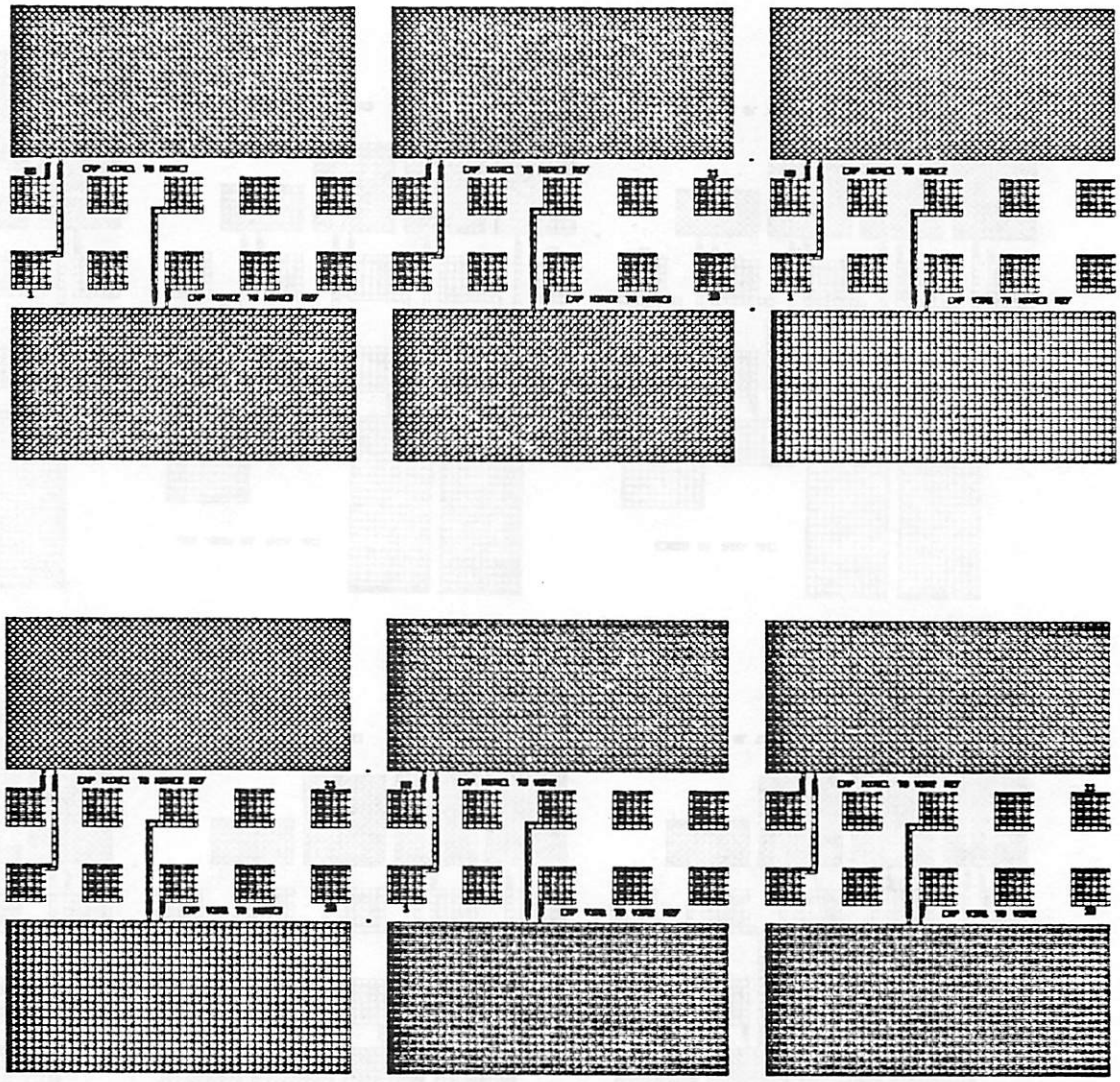


Figure 27. Layout of Fringe Capacitor Structures

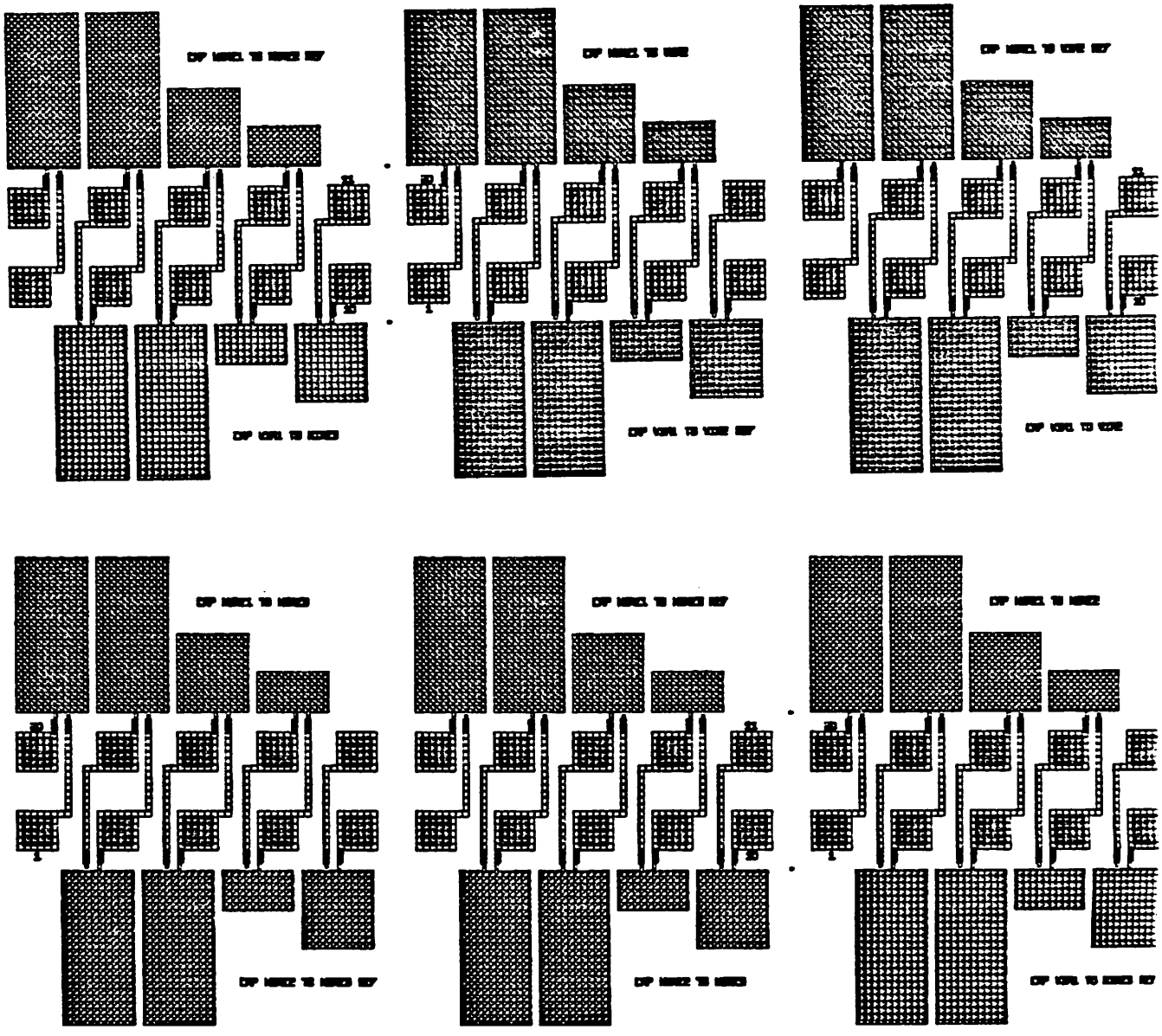


Figure 28. Layout of Small Capacitor Structures

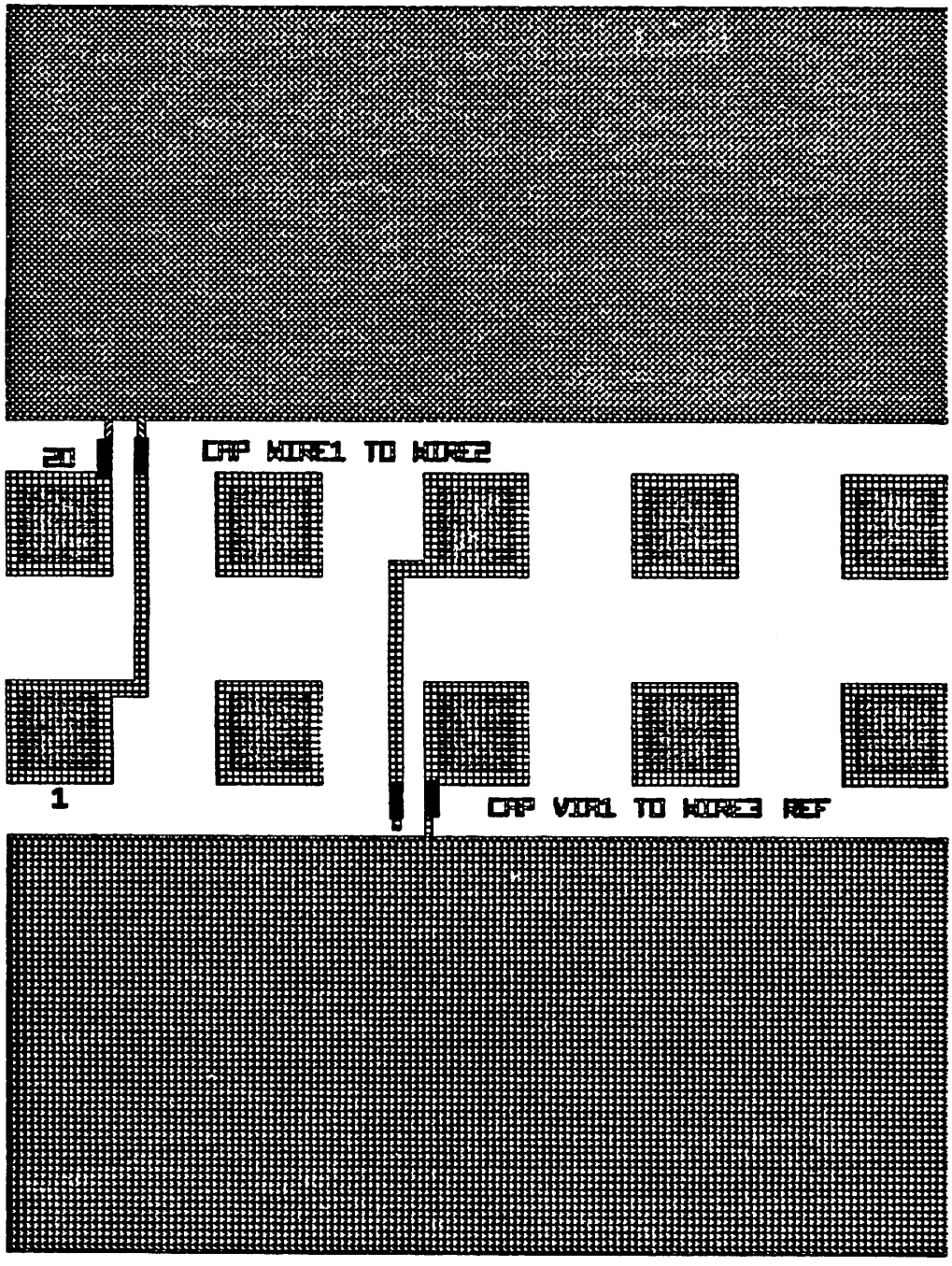


Figure 29. Expanded Layout of Flat Capacitor Structure

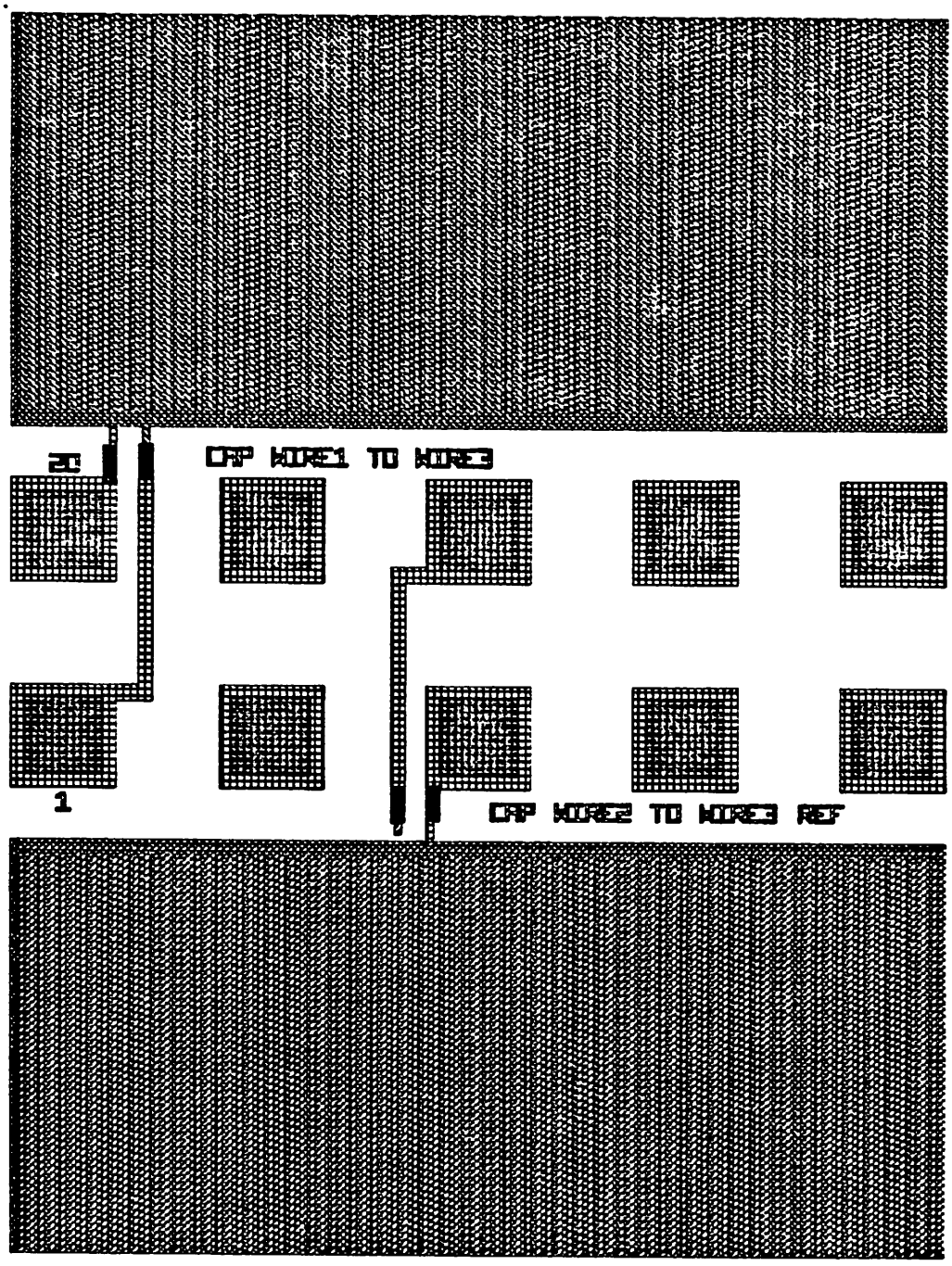


Figure 30. Expanded Layout of Fringe Capacitor Structure

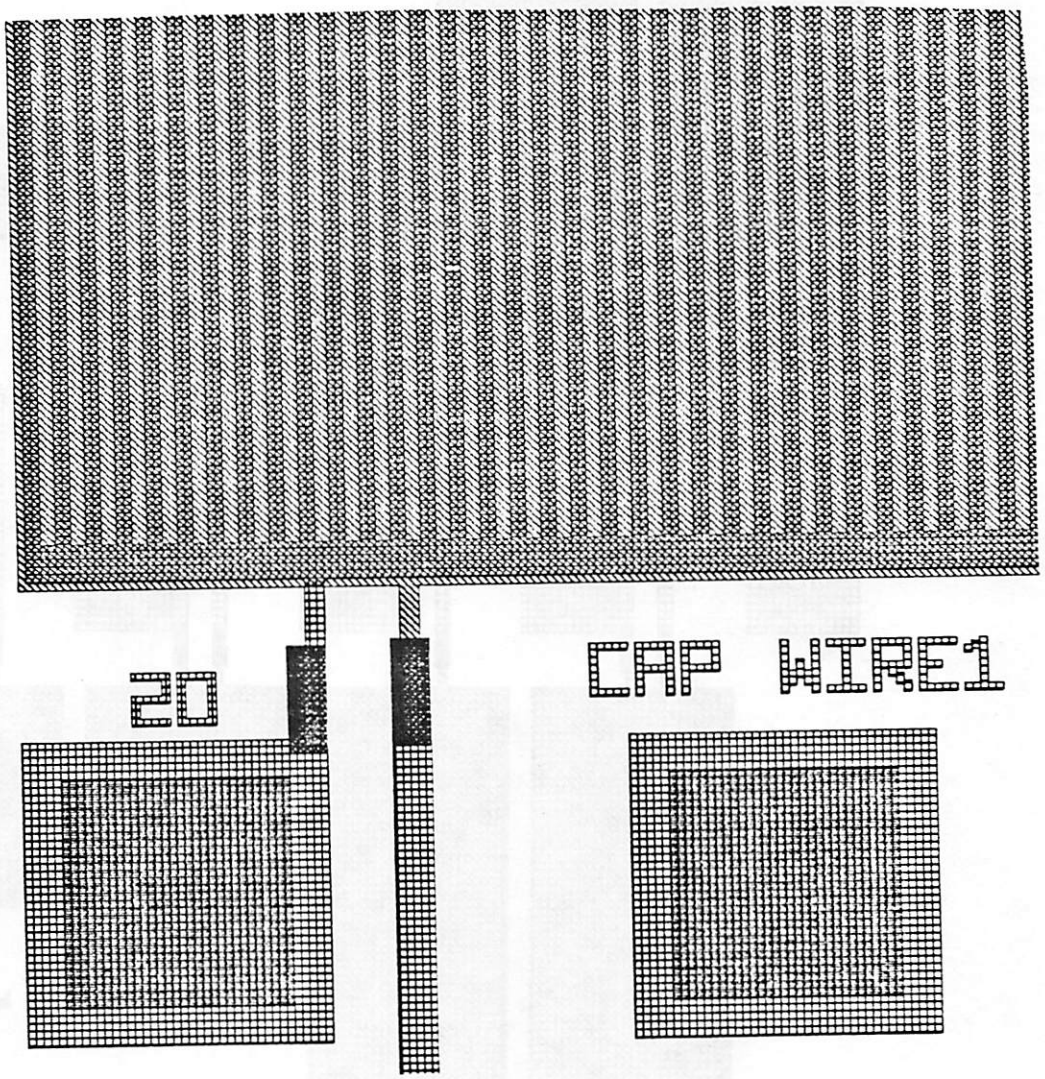


Figure 31. Expanded Layout of Fringe Capacitor Structure

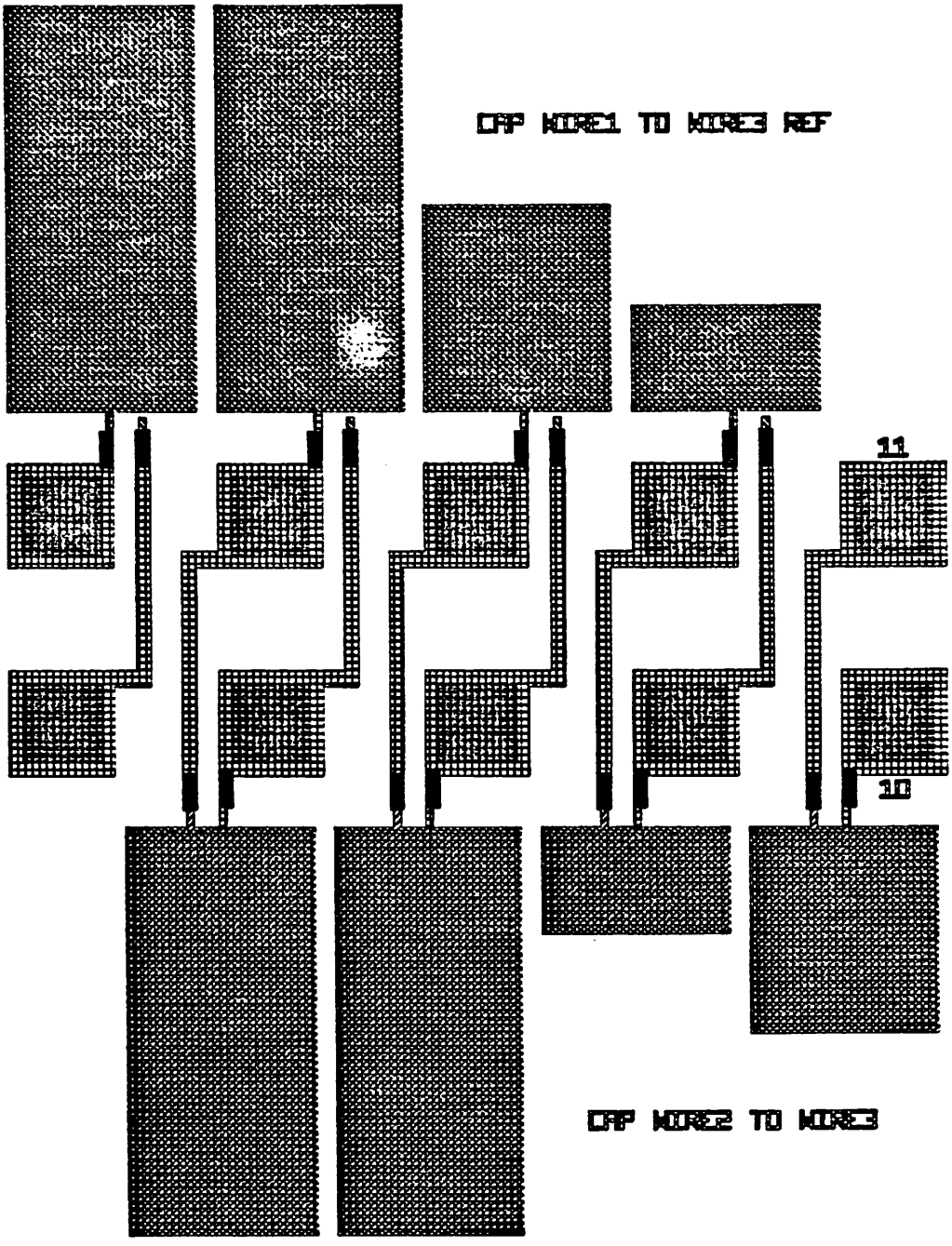


Figure 32. Expanded Layout of Small Capacitor Structure

5.9. Linewidth Measurement

5.9.1. Filename:

liwi1, liwi2, liwi3

5.9.2. Purpose:

Measure the sheet resistance of the metal. Measure the resistance of various size lines, determine the printability of metal lines of various widths.

5.9.3. Description:

The structure is a cross bridge. The bridge is 160um for each of the line lengths. The bridges also function as Van Der Pauw structures in order to determine sheet resistance. The drawn dimensions of the structures are:

5.9.4. Testing Method:

The Van Der Pauw structure is used to measure sheet resistance. The sheet resistance is then used to calculate the actual electrical line width. The line width is given by:

Line width = length * sheetresistance * I / (V2 - V1)

Where length is the length of the structure (160um), sheetresistance is the sheet resistance determined from the nearby Van Der Pauw, I is the forced current, and V2 & V1 are the measured voltages. The Van Der Pauws are measured using the the Force1, V2, VP1 and VP2 pads. The line measurements are made by forcing current between the Force1 and Force2 pads while sensing voltage on the V1 and V2 pads.

5.9.5. Test Pad Assignments:

Linewidth for Wire1			
Padset	Pad	Name	Function
1(bottom)	1	Force1	Current force for .6um wire1
	2	VP1	Van Der Pauw pad for .6um wire1
	3	Force2	Current force for .6um wire1
	18	V1	Voltage sense for .6um wire1
	19	V2	Voltage sense for .6um wire1
	20	VP2	Van Der Pauw pad for .6um wire1
	4	Force1	Current force for .8um wire1
	5	VP1	Van Der Pauw pad for .8um wire1
	6	Force2	Current force for .8um wire1
	15	V1	Voltage sense for .8um wire1
	16	V2	Voltage sense for .8um wire1
	17	VP2	Van Der Pauw pad for .8um wire1
	7	Force1	Current force for 1.0um wire1
	8	VP1	Van Der Pauw pad for 1.0um wire1
	9	Force2	Current force for 1.0um wire1
	12	V1	Voltage sense for 1.0um wire1
	13	V2	Voltage sense for 1.0um wire1
	14	VP2	Van Der Pauw pad for 1.0um wire1
2(top)	1	Force1	Current force for 1.2um wire1
	2	VP1	Van Der Pauw pad for 1.2um wire1
	3	Force2	Current force for 1.2um wire1
	18	V1	Voltage sense for 1.2um wire1
	19	V2	Voltage sense for 1.2um wire1
	20	VP2	Van Der Pauw pad for 1.2um wire1
	4	Force1	Current force for 1.4um wire1
	5	VP1	Van Der Pauw pad for 1.4um wire1
	6	Force2	Current force for 1.4um wire1
	15	V1	Voltage sense for 1.4um wire1
	16	V2	Voltage sense for 1.4um wire1
	17	VP2	Van Der Pauw pad for 1.4um wire1
	7	Force1	Current force for 1.6um wire1
	8	VP1	Van Der Pauw pad for 1.6um wire1
	9	Force2	Current force for 1.6um wire1
	12	V1	Voltage sense for 1.6um wire1
	13	V2	Voltage sense for 1.6um wire1
	14	VP2	Van Der Pauw pad for 1.6um wire1

Table 12. Line Width Pad Assignments

The pad assignments for the Wire2 and Wire3 levels are the same as the Wire1 level.

5.9.6. Location:

Column 3, Row 1-6

5.9.7. References:

E290O test structures

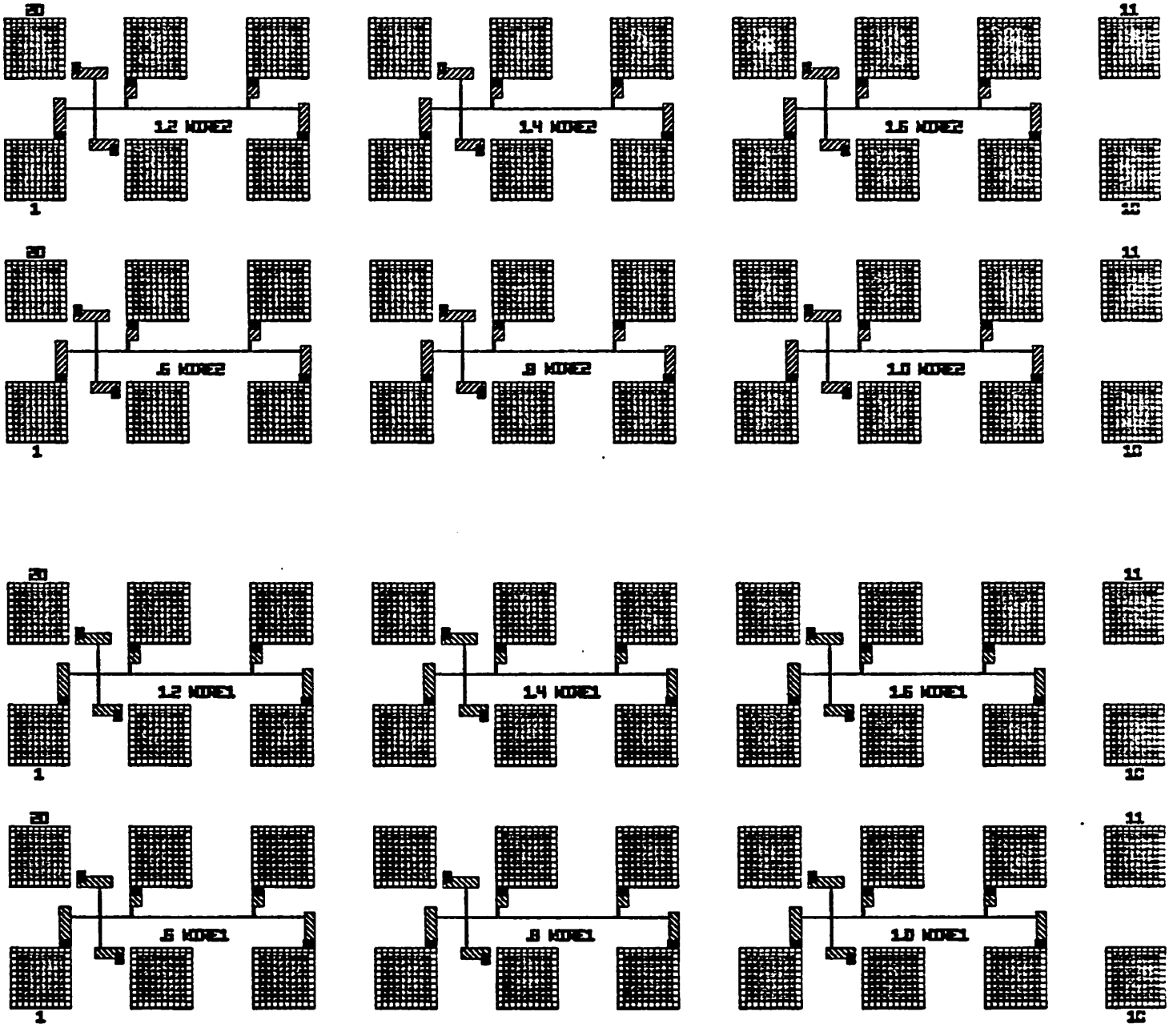
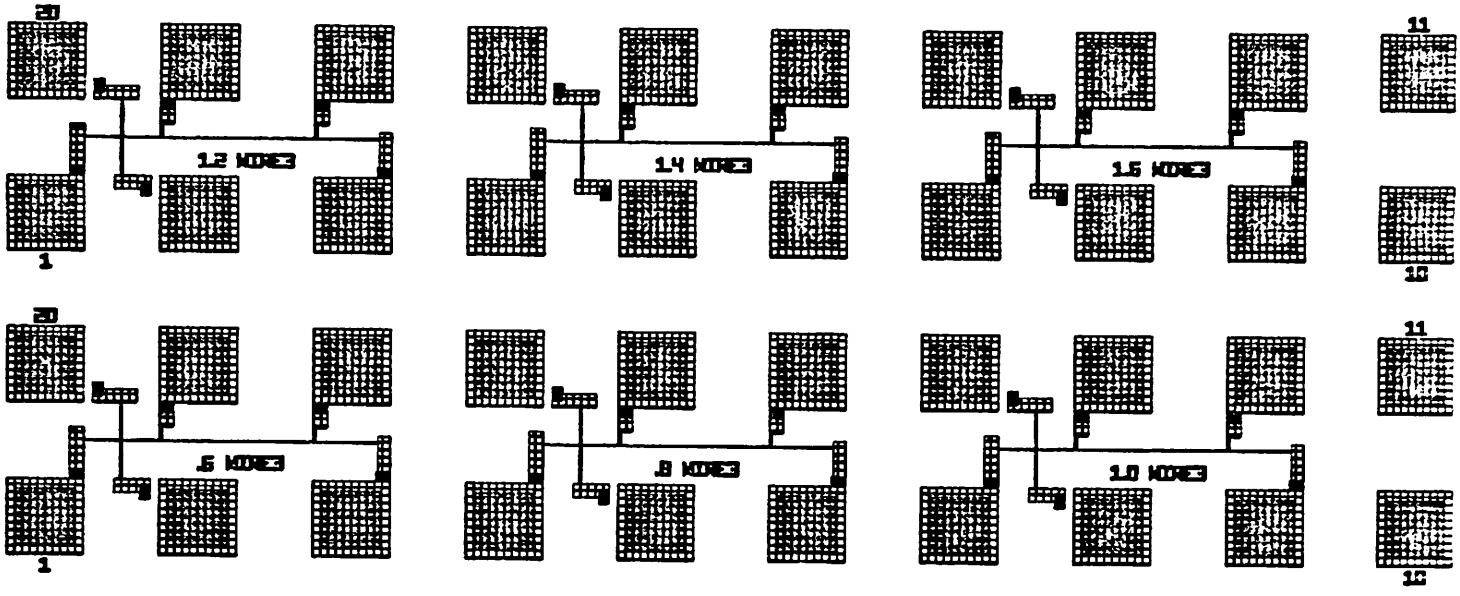


Figure 33. Layout of Line Width Structures for Wire1



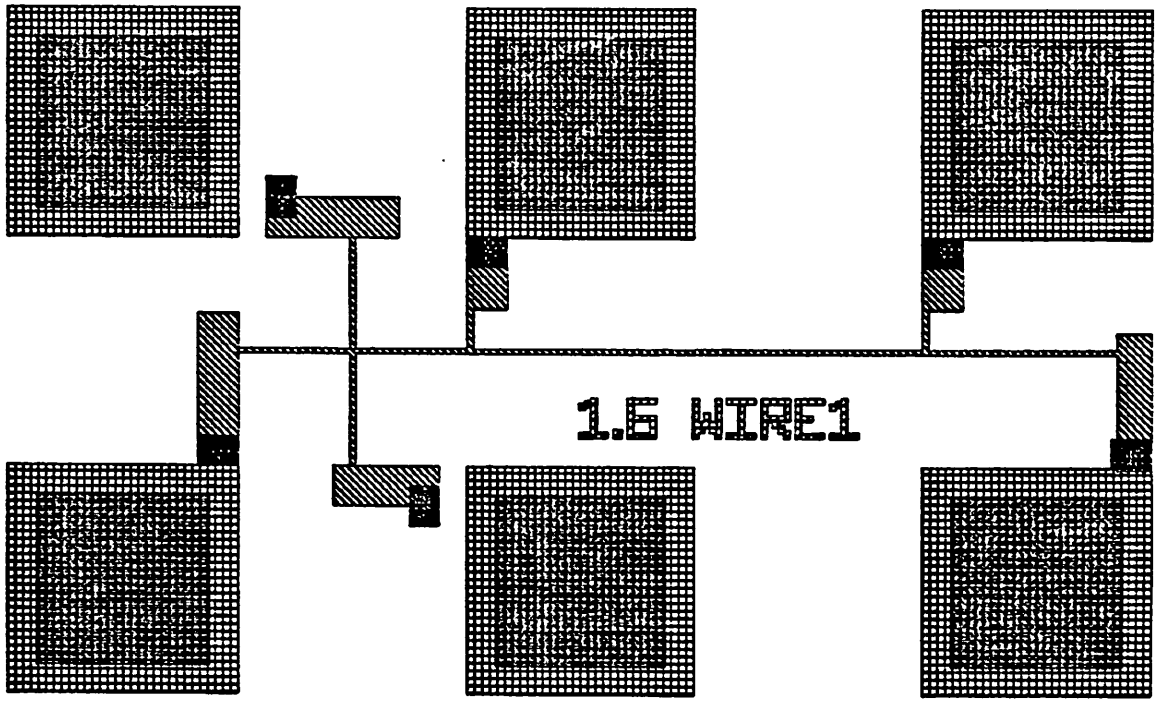


Figure 34. Expanded Layout of a single Linewidth Structure

5.10. Process Bias

5.10.1. Filename:

bias1, bias2, bias3, bias4, bias5

5.10.2. Purpose:

Measure the process bias. Measure linewidth and spacing.

5.10.3. Description:

Standard Van Der Pauw four point symmetrical structure. Long Narrow line with and without space in the center. Both the portion with and without the space are 500um long.

5.10.4. Testing Method:

Force a known current through the structure and measure the voltage difference along the portion without a space in the center. Measure voltage along portion with space also. The line and space width are given by:

Line width = length * sheetresistance * I / (V2 - V1)

Spacewidth = Linewidth - 2 * (length * sheetresistance * I / (V2 - V1))

Where length is the length of the structure (500um), I is the forced current, V2 and V1 are the measured voltages for either space or line width, and sheetresistance is the sheet resistance measured at the nearby Van Der Pauw.

The process bias can be determine by comparing the spacewidth and the linewidth.

5.10.5. Test Pad Assignments:

Bias and Van Der Pauw			
Padset	Pad	Name	Function
1	1	VP1	Van Der Pauw Pad #1
	2	VP2	Van Der Pauw Pad #2
	20	VP3	Van Der Pauw Pad #3
	19	VP4	Van Der Pauw Pad #4
	8	Force1	Current force Pad 1
	15	Force2	Current force Pad 2
	6	VSP1	Voltage sense point #1 for Space
	7	VSP2	Voltage sense point #2 for Space
	13	VLI1	Voltage sense point #1 for linewidth
	14	VLI2	Voltage sense point #2 for linewidth

Table 13. Bias Pad Assignments

5.10.6. Location:

Column 1-2, Row 4-6

5.10.7. References:

E290O test structures (partial)

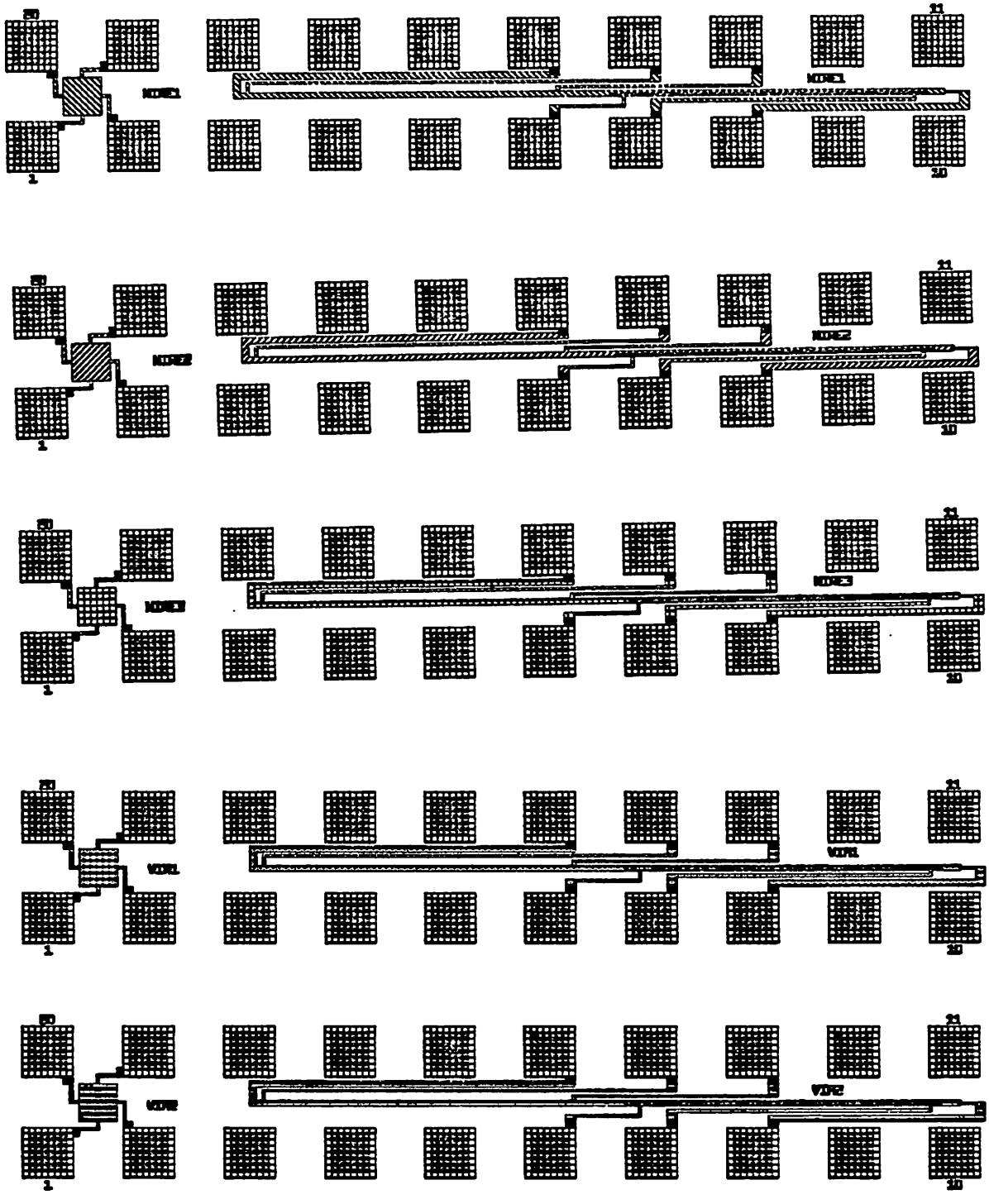


Figure 35. Layout of Bias Structures

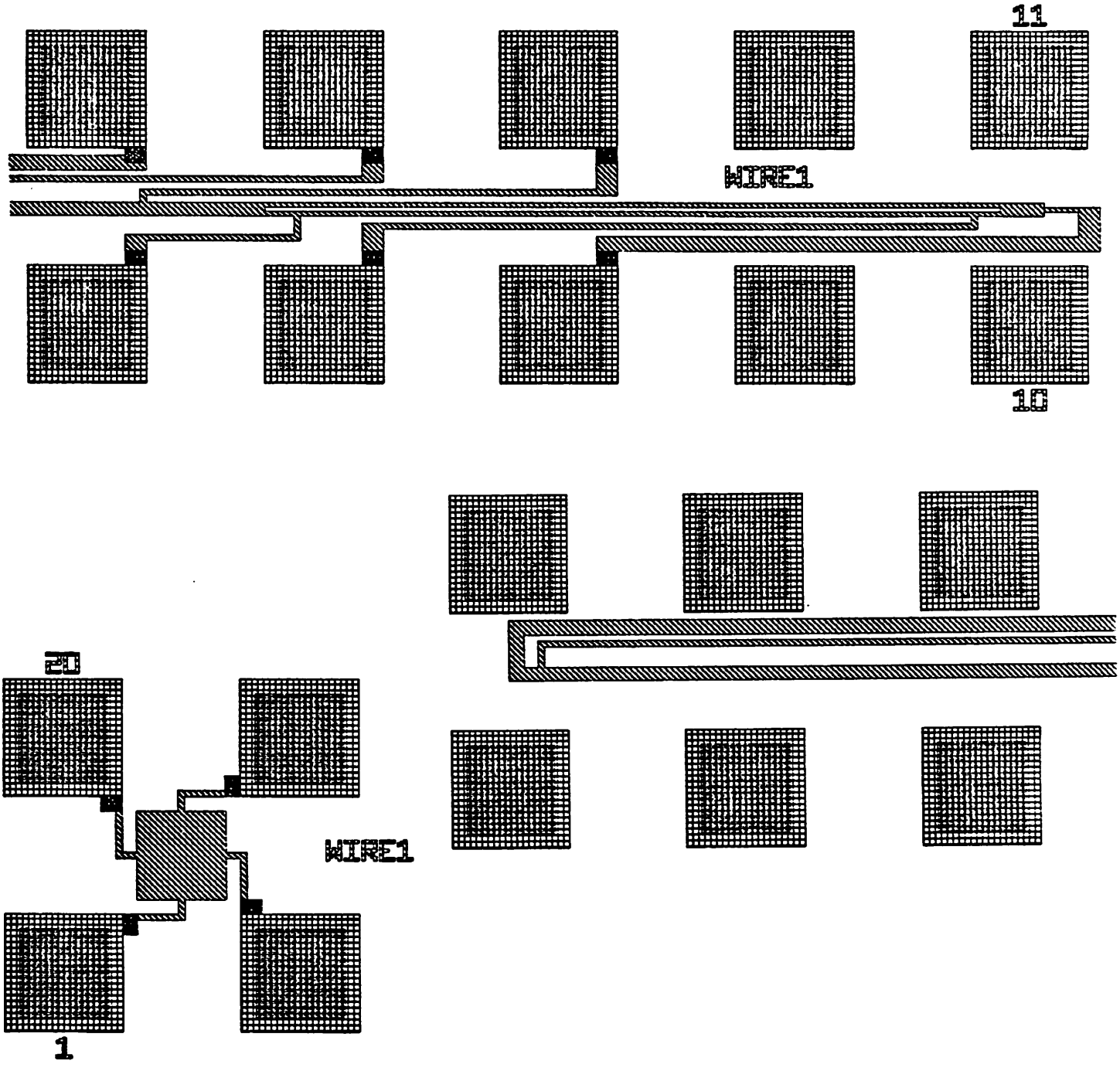


Figure 36. Expanded Layout of a single Bias Structure

5.11. Electrical Alignment

5.11.1. Filename:

align1, align2, align3, align4

5.11.2. Purpose:

Electrically measure the alignment between masking layers

5.11.3. Description:

Staggered symmetrical columns with current force pads and voltage sense pads.

5.11.4. Testing Method:

Force current through two of four pads and measure voltage at the other two. See Discussion Section for details. Current is forced between ForceA and ForceB. The voltage difference between V1-V2 and V3-V4 are compared in order to determine mis-alignment.

5.11.5. Test Pad Assignments:

Alignment Test Pad Locations		
Padset		
Row	Column	Alignment between which layers
1	1	vertical wire2 to via1
1	2	vertical wire2 to via2
2	1	vertical wire3 to via1
2	2	vertical wire1 to via1
3	1	vertical wire3 to via2
3	2	vertical wire1 to via2
1	6	horizontal wire2 to via1
1	6	horizontal wire2 to via2
2	6	horizontal wire3 to via1
2	6	horizontal wire1 to via1
3	6	horizontal wire3 to via2
3	6	horizontal wire1 to via2

Table 14. Location of Alignment Pad Sets

Vertical Electrical Alignment Test Structures			
Padset	Pad	Name	Function
1(left)	2	ForceA	Current Force Point A
	19	ForceB	Current Force Point B
	1	Vsense1	Voltage Sense Point #1
	20	Vsense2	Voltage Sense Point #2
	3	Vsense3	Voltage Sense Point #3
	18	Vsense4	Voltage Sense Point #4
2(right)	9	ForceA	Current Force Point A
	12	ForceB	Current Force Point B
	10	Vsense1	Voltage Sense Point #1
	11	Vsense2	Voltage Sense Point #2
	8	Vsense3	Voltage Sense Point #3
	13	Vsense4	Voltage Sense Point #4

Table 15. Electrical Alignment Pad Assignments

The pad assignments for the other 2 sets of padsets are identical.

Horizontal Electrical Alignment Test Structures			
Padset	Pad	Name	Function
1	2	ForceA	Current Force Point A
	19	ForceB	Current Force Point B
	1	Vsense1	Voltage Sense Point #1
	20	Vsense2	Voltage Sense Point #2
	3	Vsense3	Voltage Sense Point #3
	18	Vsense4	Voltage Sense Point #4
1	6	ForceA	Current Force Point A
	15	ForceB	Current Force Point B
	5	Vsense1	Voltage Sense Point #1
	16	Vsense2	Voltage Sense Point #2
	7	Vsense3	Voltage Sense Point #3
	14	Vsense4	Voltage Sense Point #4
2	3	ForceA	Current Force Point A
	18	ForceB	Current Force Point B
	2	Vsense1	Voltage Sense Point #1
	19	Vsense2	Voltage Sense Point #2
	4	Vsense3	Voltage Sense Point #3
	17	Vsense4	Voltage Sense Point #4
2	7	ForceA	Current Force Point A
	14	ForceB	Current Force Point B
	6	Vsense1	Voltage Sense Point #1
	15	Vsense2	Voltage Sense Point #2
	8	Vsense3	Voltage Sense Point #3
	13	Vsense4	Voltage Sense Point #4
3	4	ForceA	Current Force Point A
	17	ForceB	Current Force Point B
	3	Vsense1	Voltage Sense Point #1
	18	Vsense2	Voltage Sense Point #2
	5	Vsense3	Voltage Sense Point #3
	16	Vsense4	Voltage Sense Point #4
3	8	ForceA	Current Force Point A
	13	ForceB	Current Force Point B
	7	Vsense1	Voltage Sense Point #1
	14	Vsense2	Voltage Sense Point #2
	9	Vsense3	Voltage Sense Point #3
	12	Vsense4	Voltage Sense Point #4

Table 16. Horizontal Electrical Alignment Pad Assignments

5.11.6. Location:

Column 1-2, Row 1-3
Column 6, Row 1-11

5.11.7. References:

none

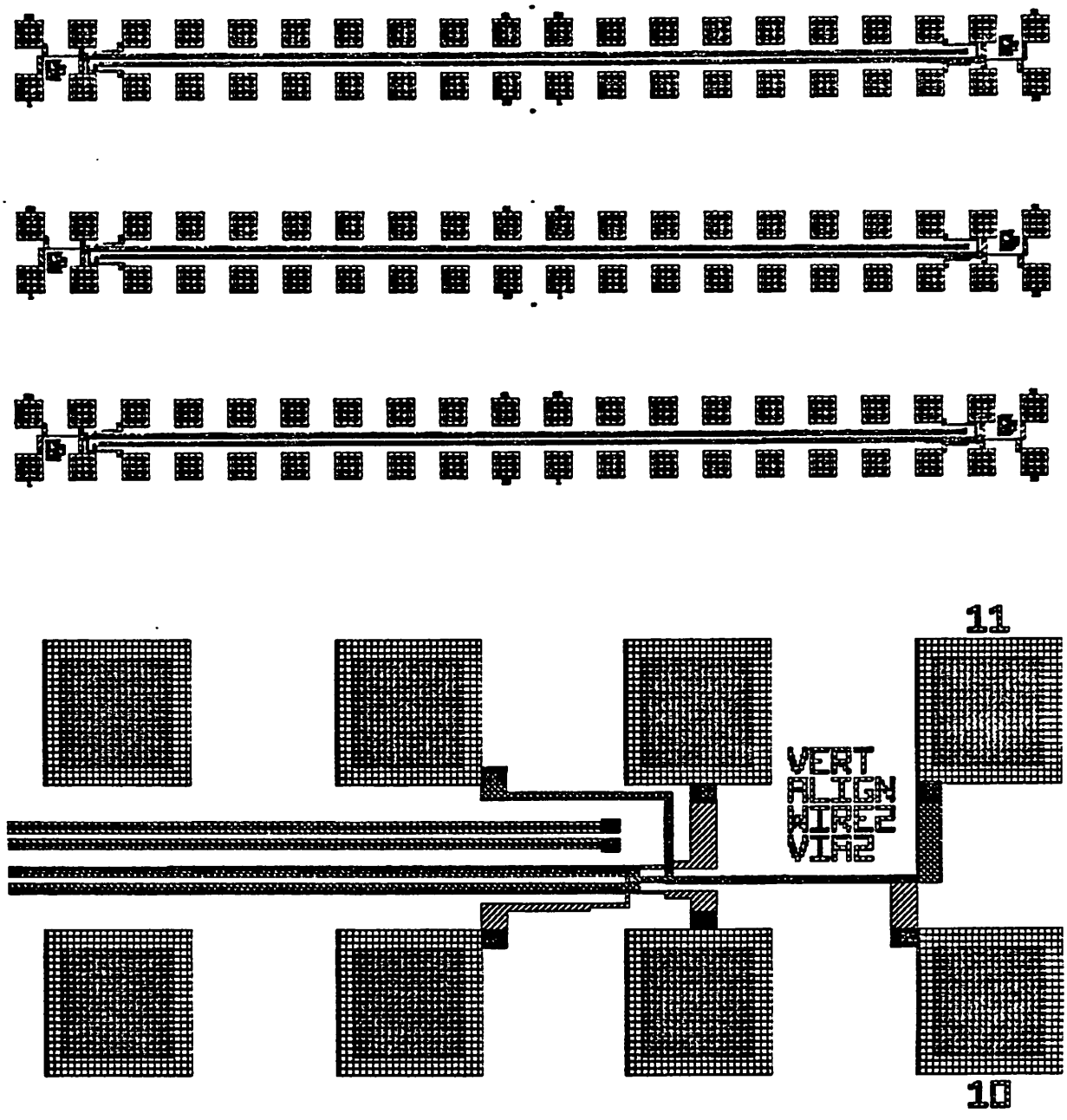


Figure 37. Layout of Alignment Test Structures

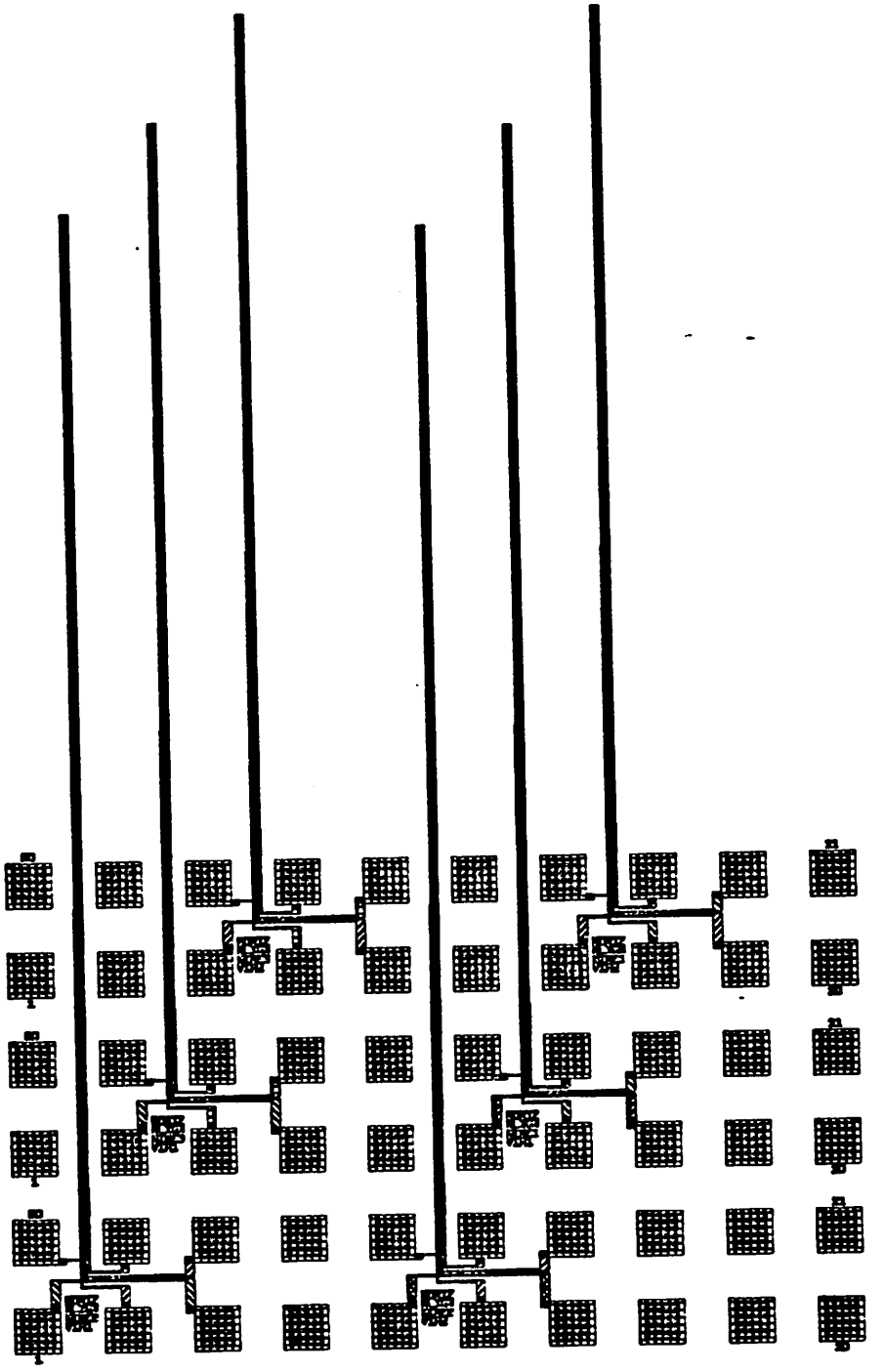


Figure 38. Layout of Alignment Test Structures

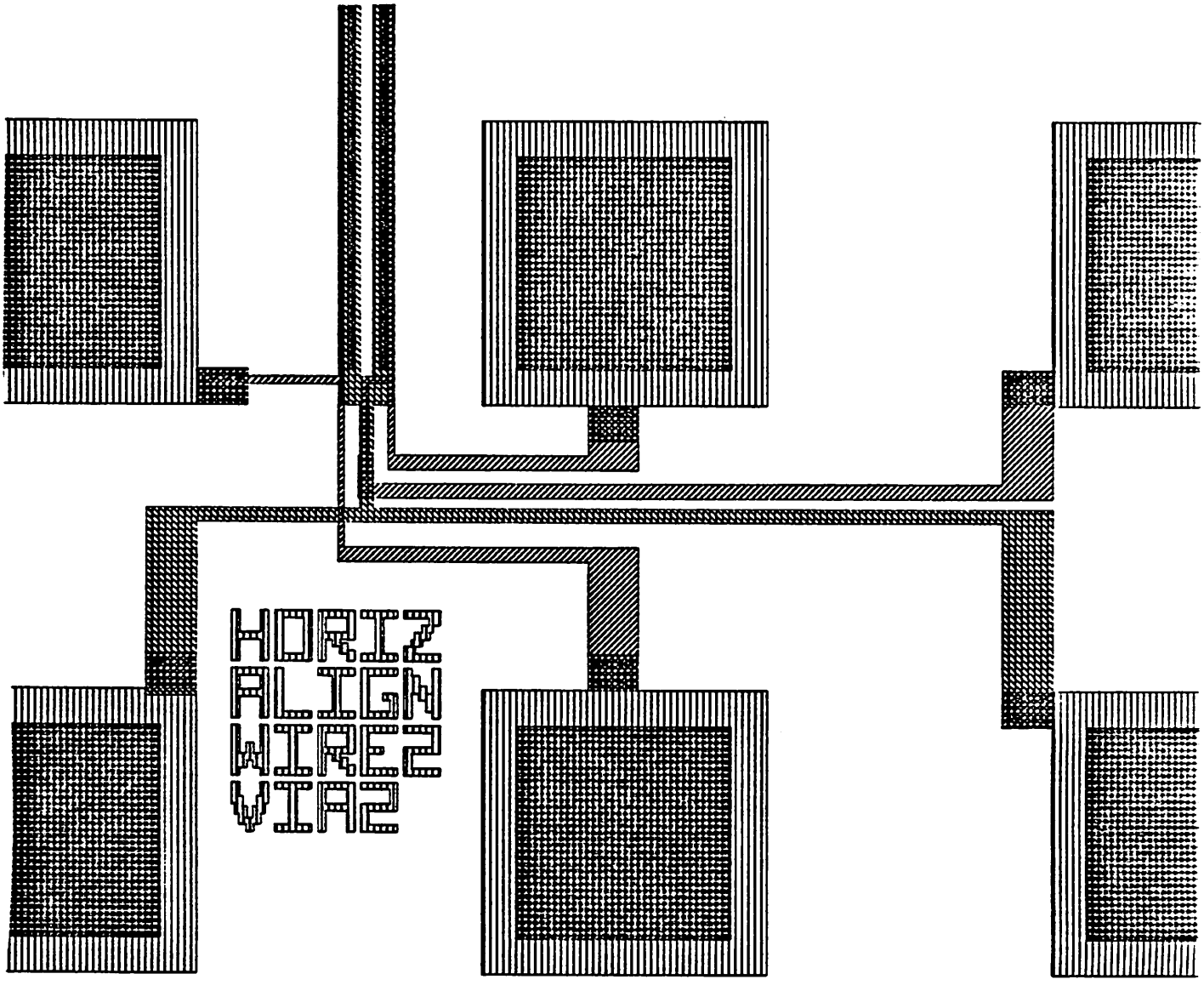


Figure 39. Expanded Layout of Alignment Structures

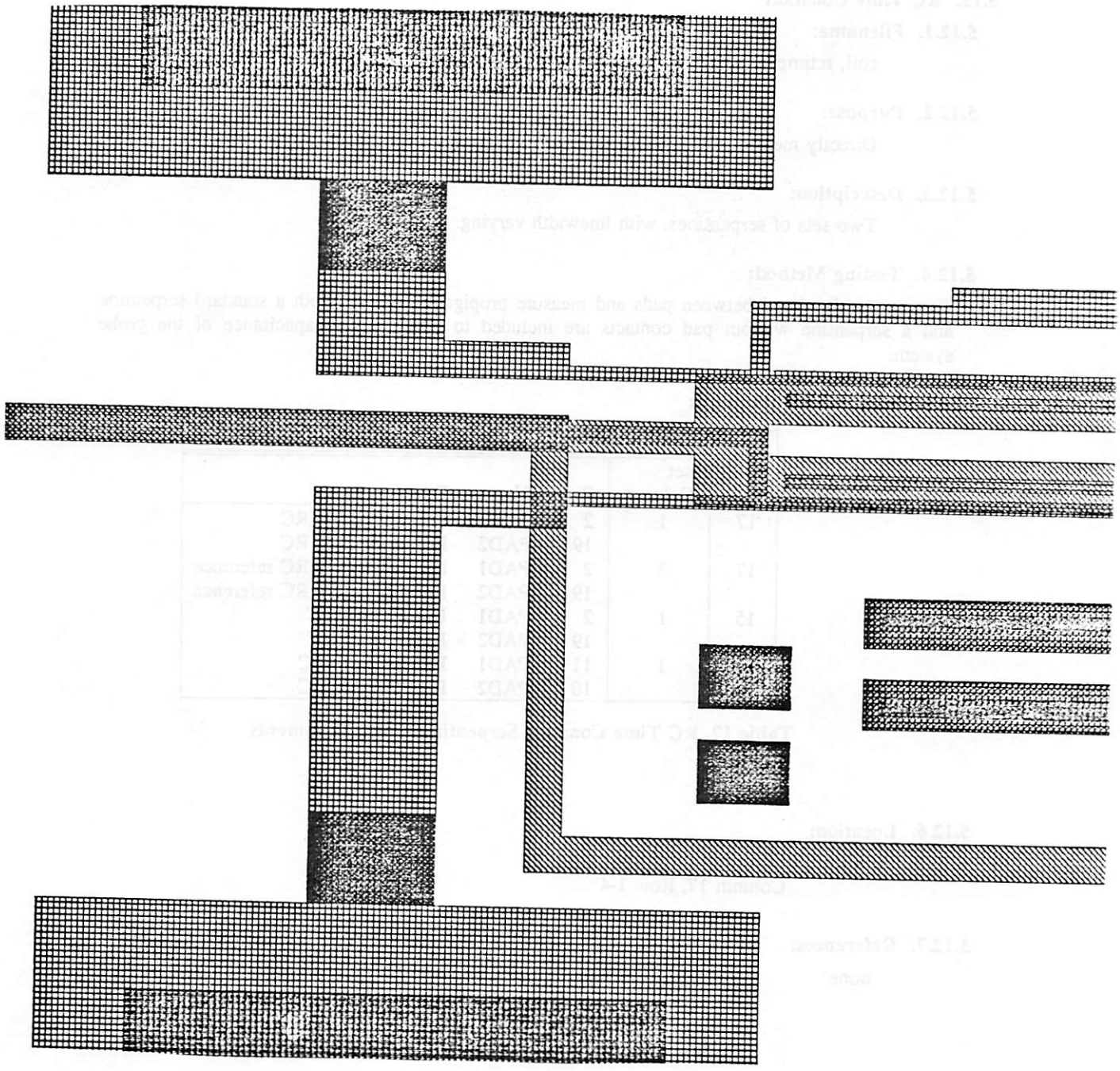


Figure 40. Expanded Layout of Alignment Structures

5.12. RC Time Constant

5.12.1. Filename:

coil, rctime

5.12.2. Purpose:

Directly measure RC time constant of long interconnect lines.

5.12.3. Description:

Two sets of serpentines, with linewidth varying.

5.12.4. Testing Method:

Apply signal between pads and measure propigation delay. Both a standard serpentine and a serpentine without pad contacts are included to measure the capacitance of the probe system.

5.12.5. Test Pad Assignments:

RC Time Constant Serpentines				
Padset				
Row	Column	Pad	Name	Function
17	1	2	PAD1	Pad #1 Narrow RC
		19	PAD2	Pad #2 Narrow RC
17	3	2	PAD1	Pad #1 Narrow RC reference
		19	PAD2	Pad #2 Narrow RC reference
15	1	2	PAD1	Pad #1 long RC
		19	PAD2	Pad #2 long RC
14	1	11	PAD1	Pad #1 Wide RC
		10	PAD2	Pad #2 Wide RC

Table 17. RC Time Constant Serpentines Pad Assignments

5.12.6. Location:

Column 14-15, Row 1-5
Column 17, Row 1-4

5.12.7. References:

none

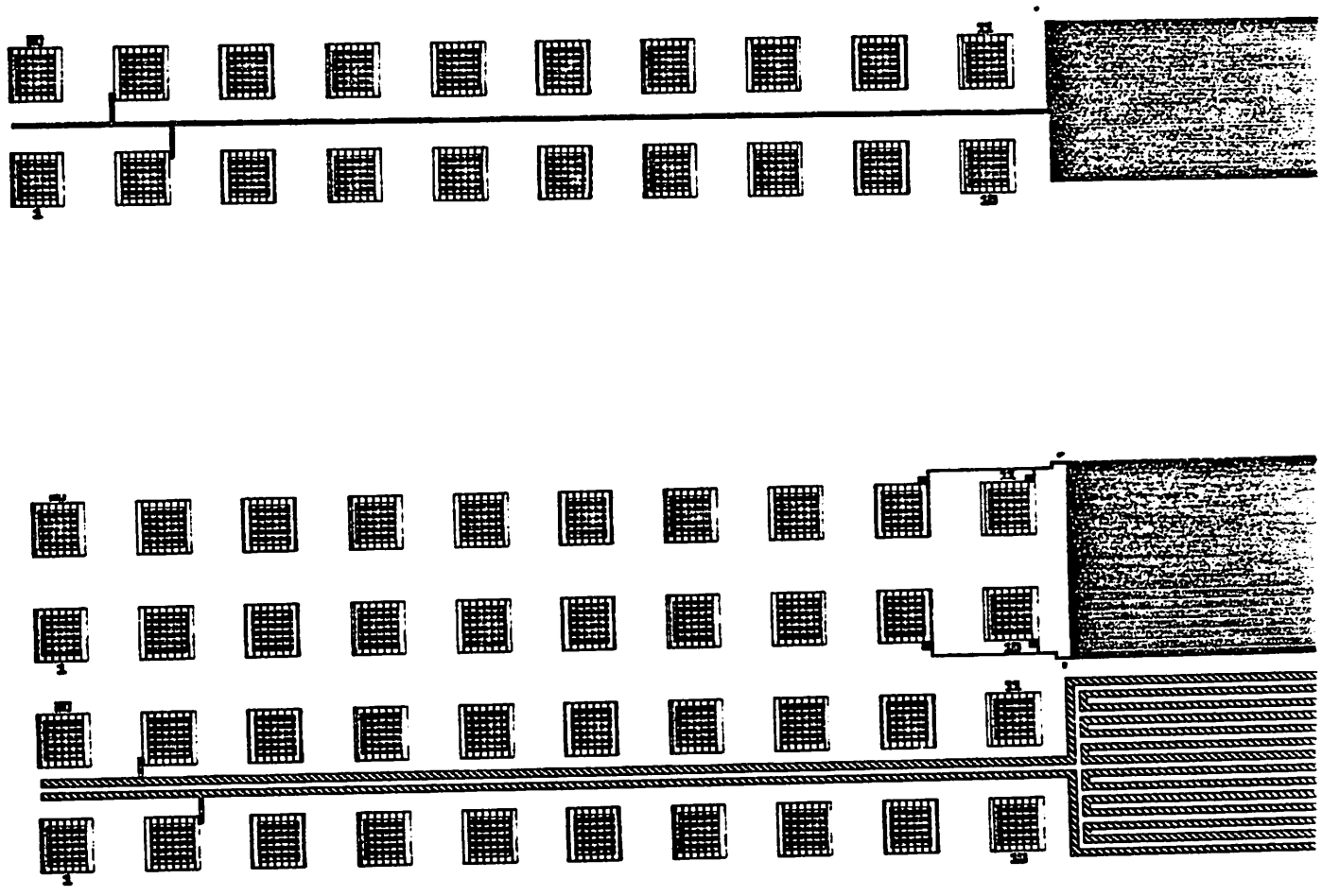


Figure 41. Layout of RC Time Constant Serpentines

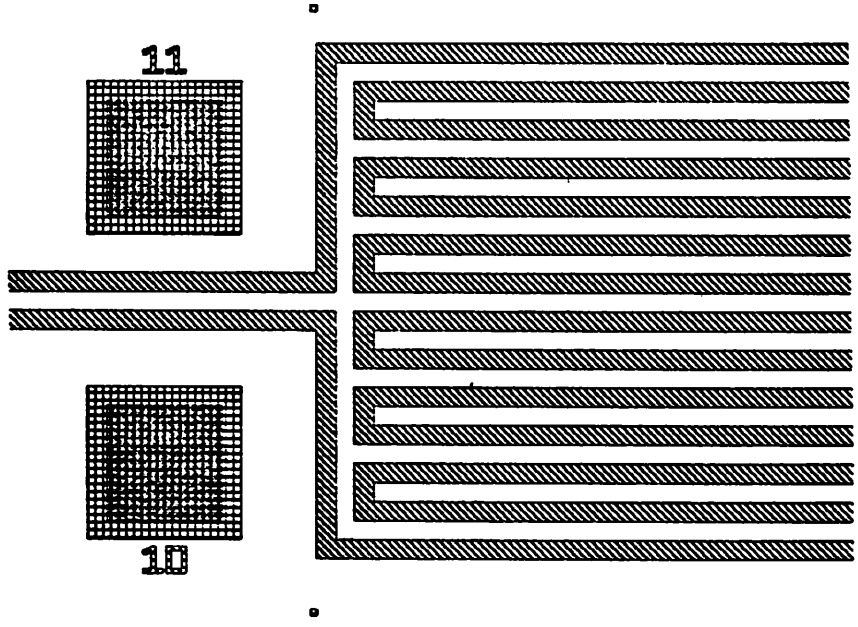


Figure 42. Expanded Layout of RC Time Constant Serpentines

5.13. SEM Lines

5.13.1. Filename:

sem

5.13.2. Purpose:

Provide lines for sem cross-sections. Interested in planarity of of N-Level Metal and vias

5.13.3. Description:

.5 cm long lines in all layers creating useful cross-sections. Staggered via chains for viewing cross-sections of actual single vias. Special structures were especially included for viewing planarity under varying circumstances. Different constant line-space patterns were included varying in size from .6um to 10um.

5.13.4. Testing Method:

Break wafer and view in sem.

5.13.5. Test Pad Assignments:

none

5.13.6. Location:

Column 1-3, Row 10

5.13.7. References:

none

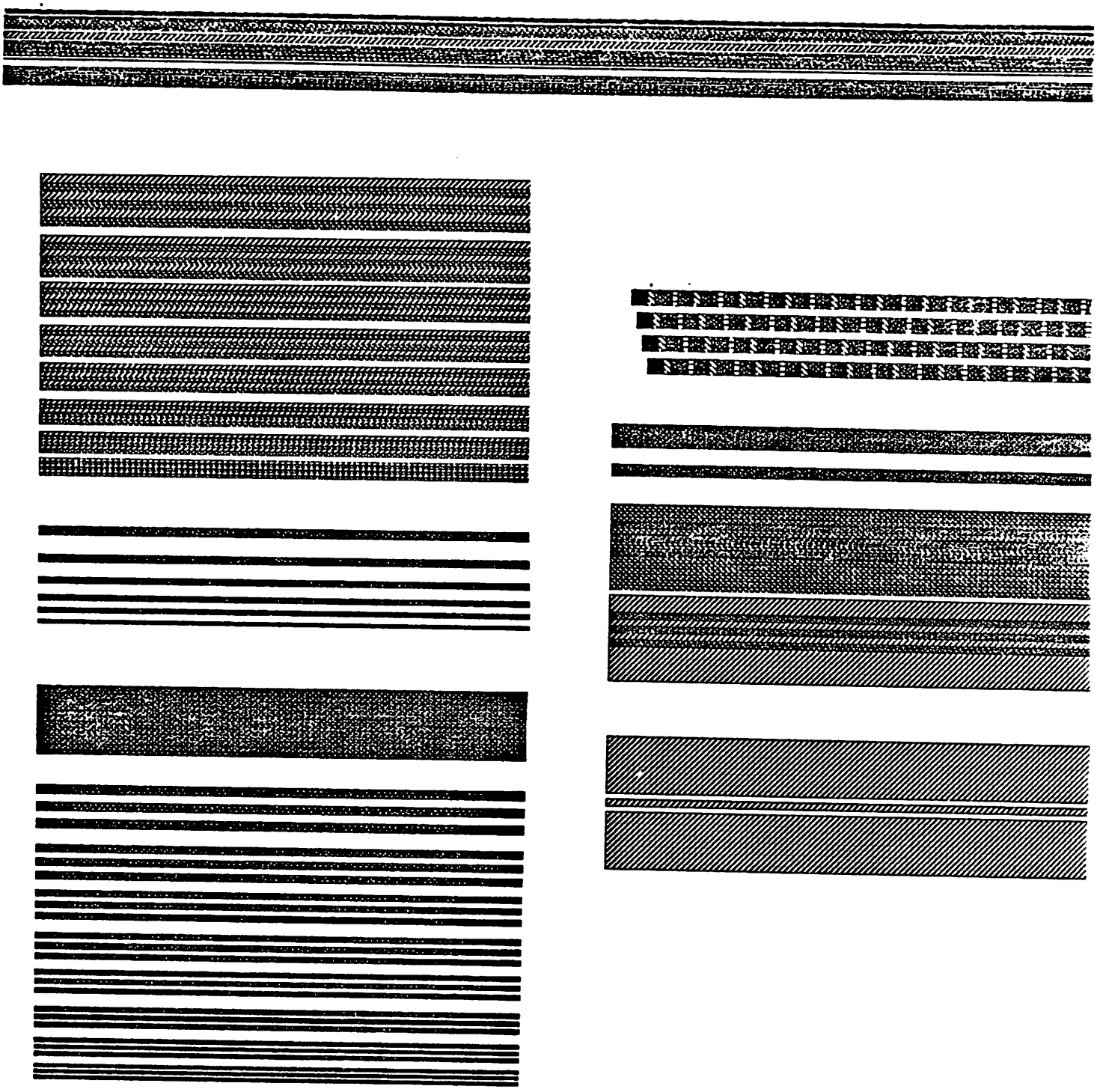


Figure 43. Layout of SEM Structures

5.14. Proximity

5.14.1. Filename:

proximity

5.14.2. Purpose:

Determine the effect of proximity on new metalization processes.

5.14.3. Description:

Varying sizes and densities of contacts (2 - 4 um) are located nearby lines and pads.

5.14.4. Testing Method:

Visual inspection of contact filling. Electrical test of line filling possible from any pad to any other pad.

5.14.5. Test Pad Assignments:

Proximity Structure			
Padset	Pad	Name	Function
1	1	PAD1	Pad #1
	2	PAD2	Pad #2
	3	PAD3	Pad #3
	4	PAD4	Pad #4
	5	PAD5	Pad #5
	6	PAD6	Pad #6
	7	PAD7	Pad #7
	8	PAD8	Pad #8
	9	PAD9	Pad #9
	10	PAD10	Pad #10
	11	PAD11	Pad #11
	12	PAD12	Pad #12
	13	PAD13	Pad #13
	14	PAD14	Pad #14
	15	PAD15	Pad #15
	16	PAD16	Pad #16
	17	PAD17	Pad #17
	18	PAD18	Pad #18
	19	PAD19	Pad #19
	20	PAD20	Pad #20

Table 18. Proximity Structure Pad Assignments

5.14.6. Location:

Column 16, Row 6

5.14.7. References:

none

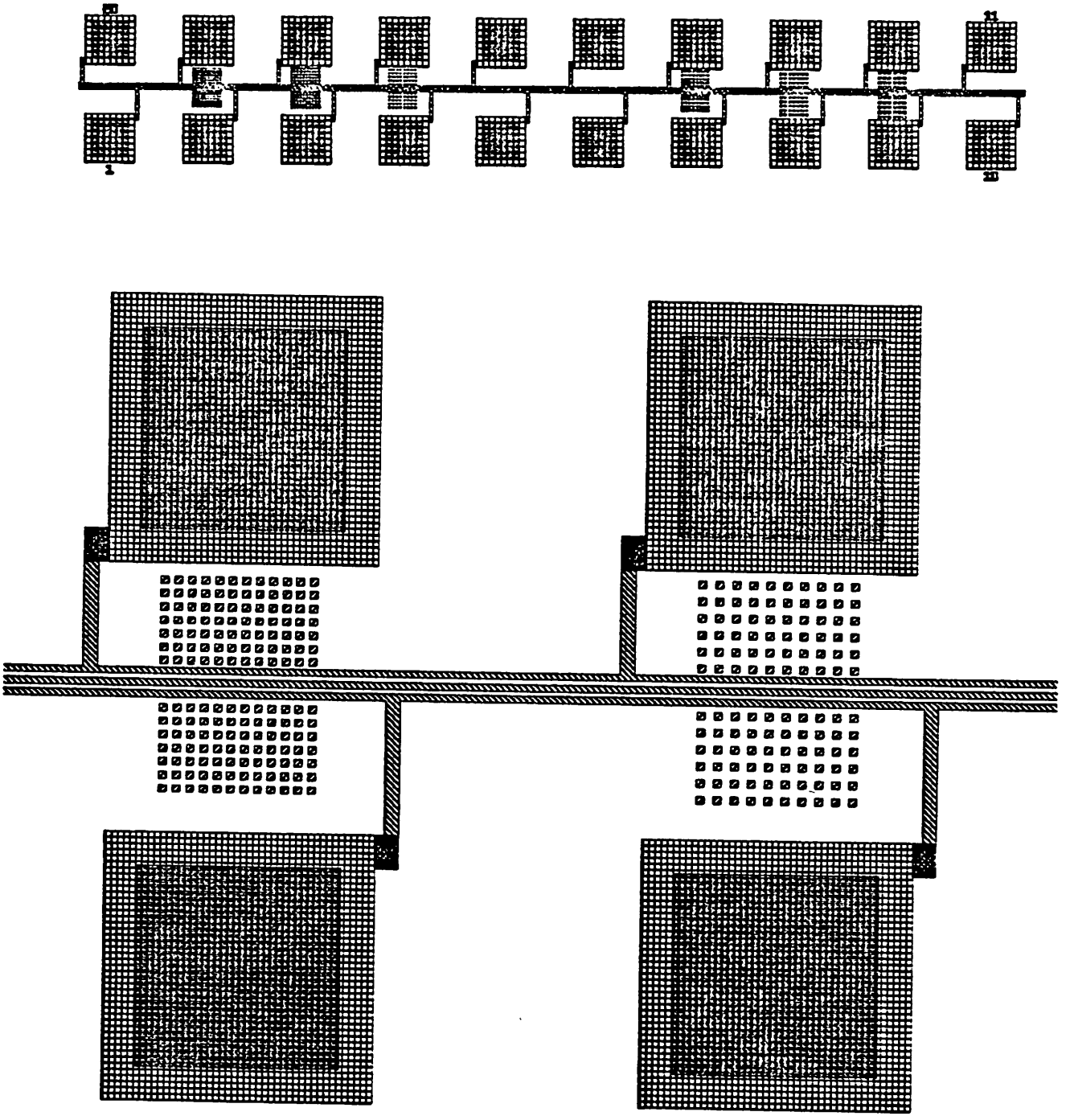


Figure 44. Proximity Structure Layout

5.15. Migration

5.15.1. Filename:

migration

5.15.2. Purpose:

Determine the electromigration resistance of new metalization processes as a function of linesize and current density.

5.15.3. Description:

Lines are notched at the sides and corners, leaving different thicknesses of lines (2.0, 1.8, 1.6, 1.4, 1.2, 1.0, 0.8, 0.7, 0.6, 0.5 um) to determine the electromigration as a function of current density.

Current Density = I * A = I * linewidth * film thickness.

5.15.4. Testing Method:

Force current through line, slowly increasing current until open occurs. Compare critical current levels for varying sized lines.

5.15.5. Test Pad Assignments:

Migration Structure			
Padset	Pad	Name	Function
1	1	PAD1	2.0 um linewidth Pad #1
	20	PAD20	2.0 um linewidth Pad #2
	2	PAD2	1.8 um linewidth Pad #1
	19	PAD19	1.8 um linewidth Pad #2
	3	PAD3	1.6 um linewidth Pad #1
	18	PAD18	1.6 um linewidth Pad #2
	4	PAD4	1.4 um linewidth Pad #1
	17	PAD17	1.4 um linewidth Pad #2
	5	PAD5	1.2 um linewidth Pad #1
	16	PAD16	1.2 um linewidth Pad #2
	6	PAD6	1.0 um linewidth Pad #1
	15	PAD15	1.0 um linewidth Pad #2
	7	PAD7	0.8 um linewidth Pad #1
	14	PAD14	0.8 um linewidth Pad #2
	8	PAD8	0.7 um linewidth Pad #1
	13	PAD13	0.7 um linewidth Pad #2
	9	PAD9	0.6 um linewidth Pad #1
	12	PAD12	0.6 um linewidth Pad #2
	10	PAD10	0.5 um linewidth Pad #1
	11	PAD11	0.5 um linewidth Pad #2

Table 19. Migration Structure Pad Assignments

5.15.6. Location:

Column 17, Row 5

5.15.7. References:

none

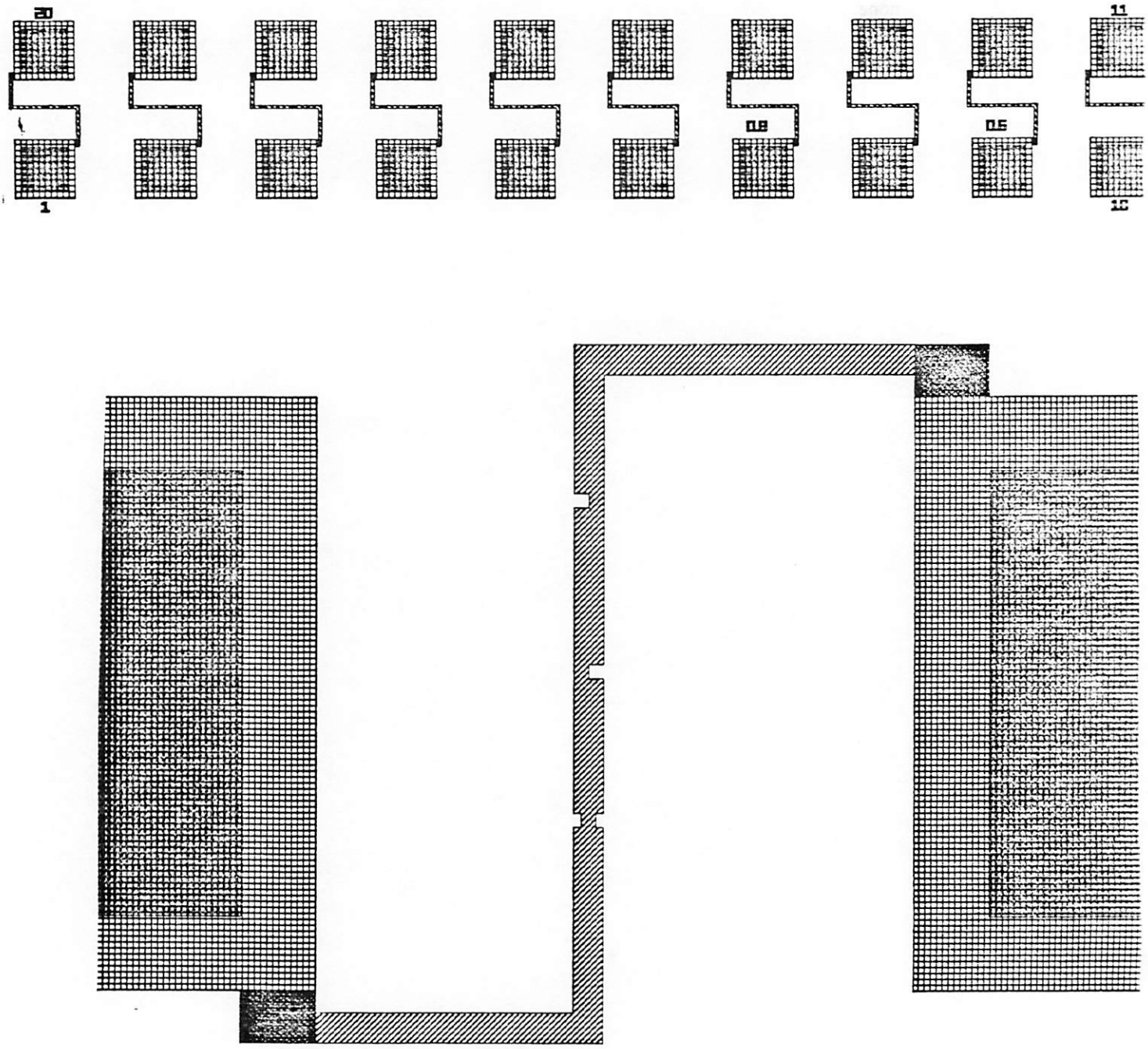


Figure 45. Migration Structure Layout

6. VEM file Description

The VEM/OCT System was utilized to do the layout of the N-Level Metal Test Chip. The Final file was titled "nlevel". This file, however, is only contains instantiations of the simpler test structures. Each Test structure was developed in its own file.

6.1. Text and Labels

A large number of text and label files were developed in order to clearly label all structures on the N-Level Test Chip. This was considered desirable especially for the visual test patterns. The following files were utilized for the labels. Note that all the text file names end in a ".t". These files are utilized by nearly all other test structures in some form or another.

0.6.t
0.8.t
0.t
1.0.t
1.2.t
1.4.t
1.5.t
1.6.t
1.t
2.0.t
2.t
2contactchain.t
3.0.t
3.t
4.0.t
4.t
6.t
8.t
a.t
align.t
arrow
c.t
cap.t
caplabel.t
contactchain.t
d.t
d6.t
d8.t
dec.t
f.t
g.t
h.t
horiz.t
i.t
n.t
nlevel.t
p.t
r.t
ref.t
s.t
scontactchain.t
sequals
t.t
to.t

v.t
v1.t
v2.t
vert.t
verniers.t
via.t
via1.t
via1.t.via1
via2.t.via2
via2.t
w.t
w1.t
w2.t
w3.t
wire.t
wire1.t
wire1.t.wire1
wire2.t
wire2.t.wire2
wire3.t
z.t
zero.t

6.2. Padsets

The files PAD.K and PADSET.K describe the complete padset utilized in all the electrical test structures. These two files are included in almost all the test structures.

6.3. File Organization

The organization of the remaining files utilized for the layout of the N-Level Metal Test Chip is shown below:

align1
align2
align3
align4
    aligncol.met1
    aligncol.met2
    aligncol.met3
alignmark1
alignmark2
    alignmark.via1
    alignmark.via2
    alignmark.wire1
    alignmark.wire2
    alignmark.wire3
    alignpec.met1
    alignpec.met2
    alignpec.met3
    alm.via1
    alm.via2
    alm.wire1
    alm.wire2
    alm.wire3
bias1

bias2
bias3
bias4
bias5
cap1
cap2
cap3
cap4
cap5

capconnect

coil

coillines.100

combs.s06
combs.s08
combs.s10
combs.s12
combs.s15

combs.h06
combs.h08
combs.h10
combs.h12
combs.h15
combs.p06
combs.p08
combs.p10
combs.p12
combs.p15
combs.v06
combs.v08
combs.v10
combs.v12
combs.v15

con1
con2
con3
con4
con5
con6
con7
con8

con.c1.1.2
con.c1.1.6
con.c1.2
con.c1.2.4
con.c1.3
con.c1.4
con.c2.1.2
con.c2.1.6
con.c2.2
con.c2.3
con.c2.4
con.c3.1.2
con.c3.1.6
con.c3.2
con.c3.3

con.c3.4
con.c4.1.2
con.c4.1.6
con.c4.2
con.c4.3
con.c4.4
con.m1
con.m1.2
con.m2
con.m2.2
con.m3
con.m3.2
conc.c1.1.2
conc.c1.1.6
conc.c1.2
conc.c1.2.4
conc.c1.3
conc.c1.4
conc.c2.1.2
conc.c2.1.6
conc.c2.2
conc.c2.2.4
conc.c2.3
conc.c2.4
conc.c3.1.2
conc.c3.1.6
conc.c3.2
conc.c3.3
conc.c3.4
conc.c4.1.2
conc.c4.1.6
conc.c4.2
conc.c4.3
conc.c4.4
conc.m1
conc.m1.2
conc.m2
conc.m2.2
conc.m3
conc.m3.2
contact1
contact1.1.2
contact1.1.6
contact1.2
contact1.3
contact1.4
contact2.1.2
contact2.1.6
contact2.2
contact2.3
contact2.4
contactset
contactset1
contactres1
contactres2

contactrespad
elbows
levels
line.h
linecap
linecapref
lines.h15
liwi1
liwi2
liwi3
longsnakes.h15
migration
prox
proximity
prxcntcts
rctime
sem
sheet1
snakes.s06
snakes.s08
snakes.s10
snakes.s12
snakes.s15
snakes.h06
snakes.h08
snakes.h10
snakes.h12
snakes.h15
snakes.p06
snakes.p08
snakes.p10
snakes.p12
snakes.p15
snakes.v06
snakes.v08
snakes.v10
snakes.v12
snakes.v15
verniers
vern1.con1
vern1.con2
vern1.met1
vern1.met2
vern1.met3
vern2
vern2.con1
vern2.con2
vern2.met1
vern2.met2
vern2.met3
verniers.labels
via
viaset

6.4. Via and Viaset

"via" and "viaset" are used in all of the test structures when making connections between levels. They are designed to be extra reliable.