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**BERT - CIRCUIT OXIDE RELIABILITY
SIMULATOR (CORS)**

by

Elyse Rosenbaum, Peter M. Lee, Reza Moazzami,
P. K. Ko, and C. Hu

Memorandum No. UCB/ERL M90/4

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Abstract

CORS (Circuit Oxide Reliability Simulator) is a fully integrated part of BERT (BERkeley Reliability Tools). CORS projects the probability of oxide breakdown induced circuit failure as a function of operating time, temperature, power supply voltage and input waveforms. CORS can also simulate the effects of burn-in on subsequent yield and lifetime. The user is required to provide the simulator with test capacitor breakdown statistics.

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Table of Contents

I. Introduction	2
II. Circuit Failure Model and Implementation	3
A. Oxide Breakdown Model	3
B. Temperature Dependence of Oxide Breakdown	3
C. Determination of $V_{ox}(t)$	4
D. Calculation of X_{eff}	5
E. Calculation of t_{BD} after Burn-In	6
F. Failure Probability Calculations	6
III. Characterizing Defect Density using Program DEFECT	8
A. Using DEFECT to Obtain Area Density of Defects	8
B. Using DEFECT to Obtain Defect Density per Unit Length	10
IV. CORS Command Summary	12
A. Invoke CORS (.TTF card)	12
B. Associate Device Model with Defect Density Datafile (.XEFF card)	13
C. Capacitors	13
D. MOSFETs	13
E. The .ALTMODEL Card	14
F. Print Failure Probability for each Device (.EACHPROB card)	14
G. Project Failures for Large Circuits with Identical Cells (.LSI card)	14
H. Simulate Burn-In (.BURNIN card)	15
I. .TRAN Card	15
J. Temperature Setting (.OPTIONS card)	15
V. Examples	16
References	17
Appendix A. CORS Simulations	18
Appendix B. Error Messages	19
Figures and Examples	25

I. Introduction

CORS (Circuit Oxide Reliability Simulator) is a fully integrated part of BERT (BERkeley Reliability Tools). CORS projects the probability of oxide breakdown induced circuit failure as a function of operating time, temperature, power supply voltage and input waveforms. CORS can also simulate the effects of burn-in on subsequent yield and lifetime. The user is required to provide the simulator with test capacitor breakdown statistics and an input deck which describes the circuit using SPICE commands. The input deck will also contains commands which instruct BERT to execute the CORS module. The input deck may also contain CAS (hot electron module) and EM (electromigration module) specific commands [1][2]. CORS consists of a pre- and post-processor for SPICE; Figure 1 shows a block diagram.

Appendix A should be read by the user unfamiliar with the capabilities of CORS. This appendix discusses the capabilities of CORS and provides the user with several examples of CORS output. Section II discusses the equations implemented in CORS. Section III describes the procedure for obtaining test capacitor breakdown data and also details the use of program DEFECT which is provided to the user along with BERT. DEFECT formats test capacitor breakdown data for use by CORS. Section IV contains the actual user's guide for all of the CORS commands. Finally, Section V contains examples of BERT input decks containing CORS commands and the corresponding output listings. The user who needs information on executing BERT, should obtain a copy of [1].

II. Circuit Failure Model and Implementation

A. Oxide Breakdown Model

Oxide intrinsic lifetime (t_{BD}) is [3]

$$t_{BD} = \tau \exp \left[\frac{GX_{ox}}{V_{ox}} \right] \quad (1)$$

where X_{ox} is oxide thickness, V_{ox} is oxide voltage, G and τ are proportionality constants. Large area capacitors generally experience "defect-related" breakdown which causes them to have a non-deterministic lifetime. Defect-related breakdown is modeled as [4]

$$t_{BD} = \tau \exp \left[\frac{GX_{eff}}{V_{ox}} \right]. \quad (2)$$

Note that the random variable X_{eff} has been substituted for X_{ox} in the above expression. The probability that a device undergoes oxide breakdown before a given t_{BD} is related to the probability that the oxide contains a specific value of X_{eff} . This is discussed in greater depth later in this section.

Using a quasi-static approach, we have extended this model for use with time varying voltages [5],

$$1 = \frac{1}{\tau} \int_0^{t_{BD}} \exp \left[\frac{-GX_{eff}}{V_{ox}(t)} \right] dt. \quad (3)$$

Inside CORS, $V_{ox}(t)$ is derived from SPICE node voltages and the integral in (3) is evaluated numerically using the Trapezoidal Rule. The integral is not actually evaluated for large t_{BD} , such as 10 years; instead, it is evaluated for the period, T , of SPICE simulation and then multiplied by a factor of $\frac{t_{BD}}{T}$. This places a constraint on the simulation results; they are derived assuming repetitive input waveforms.

B. Temperature Dependence of Oxide Breakdown

Time-to-breakdown (t_{BD}) decreases with increasing operating temperature. The G and τ parameters in (3) are temperature dependent to account for this effect [6]. Specifically, G and τ are defined as follows.

$$G(T) = G_{300} \left[1 + \frac{\delta}{k_B} \left[\frac{1}{T} - \frac{1}{300} \right] \right] \quad (4)$$

$$\tau(T) = \tau_{300} \exp \left[\frac{-E_b}{k_B} \left[\frac{1}{T} - \frac{1}{300} \right] \right] \quad (5)$$

T has units of K° . Default values of G_{300} , τ_{300} , δ and E_b are provided or the user may provide values derived from intrinsic oxide studies of his/her technology (Section IV.A).

C. Determination of $V_{ox}(t)$

The voltage drop across a capacitor oxide is set equal to

$$V_{ox}(t) = V_1(t) - V_2(t)$$

where $V_1(t)$ and $V_2(t)$ are the SPICE node voltages for the capacitor electrodes. It is assumed that both electrodes are made from similar materials (so there is no work function difference) and that both electrodes are highly conductive (so there is no voltage drop across a depletion region). These are reasonable assumptions for VLSI capacitors.

The voltage drop across a MOSFET oxide is not as straightforward to determine. The voltage drop across the substrate depletion region must be accounted for and work function differences must be considered. Furthermore, when current flows along the channel, the surface potential becomes a function of position and, consequently, so does the oxide electric field. In the first release of CORS, the position dependence of the oxide field along a MOSFET channel is neglected and the oxide voltage is set equal to the maximum of V_{gs} and V_{gd} , minus the depletion region voltage drop. Specifically, the oxide voltage along the channel is calculated as follows.

N-channel MOSFET

Inversion ($V_{gs} > V_t$):

Surface potential is near conduction band edge when there is appreciable gate current. Therefore,

$$V_{ox} = | V_{gs} - \phi_{ms} - \frac{E_g}{2} - \frac{\phi}{2} |$$

where ϕ equals the SPICE parameter PHI (surface potential) and ϕ_{ms} is the work function difference between the gate and substrate materials.

Accumulation ($V_g - V_b < V_{fb}$):

Surface potential is near valence band edge when there is appreciable gate current. Therefore,

$$V_{ox} = | V_g - V_b - \phi_{ms} + \frac{E_g}{2} - \frac{\phi}{2} |$$

Depletion:

$$V_{ox} \approx 0.0$$

P-channel MOSFET

Inversion ($V_{gs} < V_t$):

$$V_{ox} = | V_{gs} - \phi_{ms} + \frac{E_g}{2} + \frac{\phi}{2} |$$

Accumulation ($V_g - V_b > V_{fb}$):

$$V_{ox} = | V_g - V_b - \phi_{ms} - \frac{E_g}{2} + \frac{\phi}{2} |$$

Depletion:

$$V_{ox} \approx 0.0$$

Examination of these equations will show that the difference between the applied and the oxide voltage is zero or E_g , depending on the gate material employed and the operating regime. Additionally, the oxide voltage along the device edges must be calculated for the user who provides the simulator with statistics for defect density per unit length along diffusion and field oxide edges. V_{ox} along the field oxide edges is identical to that in the channel. The field at the source/drain edges is different from that in the channel because these regions have a different surface potential from the channel region due to the different carrier concentrations and types. The voltage at a diffusion, (say, drain) edge is calculated as follows.

N-channel MOSFET

n+ poly gate:

$$V_{ox} = | V_g - V_d |$$

p+ poly gate:

$$V_{ox} = | V_d - V_g + E_g |$$

P-channel MOSFET

p+ poly gate:

$$V_{ox} = | V_g - V_d |$$

n+ poly gate:

$$V_{ox} = | V_g - V_d + E_g |$$

D. Calculation of X_{eff}

For a given time-to-breakdown (t_{BD}), X_{eff} is calculated from (3) using Newton-Raphson's method. The X_{eff} thus derived is the maximum thickness (least severe defect) which is predicted to fail by t_{BD} . This calculation is repeated for eight different values of t_{BD} . These calculations take up the bulk of the CORS computation time. An alternative algorithm, called "quick," has been added for the user who wishes to reduce execution time and is willing to sacrifice some accuracy (about 2% - see section V). The quick algorithm replaces an expression of the form $f(V_{ox}(t))$ with an expression of the form $A \cdot f(V_{max})$. When "quick" is desired, CORS calculates X_{eff} corresponding the smallest t_{BD} from (3); these are denoted X_{eff}^0 and t_{BD}^0 . The remaining X_{eff} 's are calculated directly using

$$1 = \frac{t_{BD}^i}{t_{BD}^0} \exp \left[\frac{G}{V_{max}} (X_{eff}^0 - X_{eff}^i) \right]. \quad (6)$$

E. Calculation of t_{BD} after Burn-In

Circuit lifetime after burn-in may be projected by using CORS in a two-pass mode (Section IV.H). During the first pass, SPICE provides CORS with the node voltages during burn-in; during the second pass, SPICE provides CORS with the node voltages under normal operating conditions. If burn-in is performed, the expression for predicted lifetime, (3), must be modified to account for oxide wear incurred during the burn-in process [7].

$$1 = \frac{1}{\tau_{op}} \int_0^{t_{BD}} \exp \left[\frac{-G_{op} X_{eff}}{V_{ox}(t)} \right] dt + \frac{1}{\tau_{bi}} \int_0^{t_{bi}} \exp \left[\frac{-G_{bi} X_{eff}}{V_{ox}(t)} \right] dt \quad (7)$$

This equation is implemented in CORS using an approximation to save storage space and computation time. With the approximation, the equation becomes

$$1 = \frac{1}{\tau_{op}} \int_0^{t_{BD}} \exp \left[\frac{-G_{op} X_{eff}}{V_{ox}(t)} \right] dt + \exp \left[\frac{G_{bi}}{V_{max}^{bi}} (X_{bi} - X_{eff}) \right] \quad (8)$$

where X_{bi} is the maximum X_{eff} screened out by the burn-in trial (calculated during pass one of CORS). (8) is solved for X_{eff} using Newton-Raphson's method.

The user may choose to invoke a "quick" algorithm, rather than using (8), to calculate X_{eff} . Accuracy is sacrificed, typically on the order of 50% (see Section V). This loss of accuracy will be acceptable the user who is only interested in an order-of-magnitude estimate of failure probability. "Quick" always errs on the conservative side. If "quick" has been invoked, the simulator calculates X_{bi} during the first pass. It also calculates a X_{no_bi} during the second pass, which is the X_{eff} that would correspond to t_{BD}^0 if no burn-in had been performed. CORS proceeds to calculate X_{eff} using

$$1 = \frac{t_{BD}^i}{t_{BD}^0} \exp \left[\frac{G_{op}}{V_{max}} (X_{no_bi} - X_{eff}) \right] + \exp \left[\frac{G_{bi}}{V_{max}^{bi}} (X_{bi} - X_{eff}) \right]. \quad (9)$$

F. Failure Probability Calculations

CORS assumes that defects are distributed uniformly and independently across the test wafers and actual circuits. This allows the use of the Poisson distribution to describe the defect density (see Section III). The probability that a device fails at or before a specified t_{BD} is equal to the probability that the device contains one or more defects of size X_{eff} or smaller, where X_{eff} was calculated from (3) for the specified t_{BD} . Using the Poisson distribution, this probability may be expressed as

$$P(\text{failure}) = 1 - e^{-AD(X_{eff})} \quad (10)$$

where $D(X_{eff})$ is the area density of defects size X_{eff} or smaller (recall smaller X_{eff} 's are more severe defects) which has been provided by program DEFECT (Section III).

The probability that a circuit fails at or before time t_{BD} is equal to the probability that at least one device in the circuit fails by time t_{BD} . This may be expressed as

$$P(\text{circuit failure}) = 1 - \prod_{i=1}^n e^{-AD(X_{eff}^i)} \quad (11)$$

where n is the number of MOS devices in the circuit, $D(X_{eff}^i)$ is the defect density for the i^{th} device and X_{eff}^i yields t_{BD} for the particular waveform found at device i .

When a burn-in trial is simulated in addition to normal operation, (11) must be modified to account for the circuits lost during the burn-in test. The expression for failure probability after burn-in is

$$P(\text{circuit failure}) = \prod_{i=1}^n \frac{e^{-AD(X_{bi}^i)} - e^{-AD(X_{op}^i)}}{e^{-AD(X_{bi}^i)}} \quad (12)$$

where X_{bi}^i is calculated for device i from (3) with t_{BD} set equal to the burn-in duration, and X_{op}^i is calculated for device i from (8).

III. Characterizing Defect Density using Program DEFECT

A. Using DEFECT to Obtain Area Density of Defects

DEFECT takes raw data from a test capacitor breakdown experiment and formats it for use by CORS. There are two commonly used methods for characterizing oxide breakdown statistics, the time-to-breakdown test and the ramp-voltage-breakdown test. DEFECT will accept data from either of these experiments. In the absence of experimental data, the user may provide DEFECT with parameters for a statistical distribution which is thought to represent the oxide breakdown statistics.

A time-to-breakdown test is performed by applying a constant voltage to an ensemble of identical large-area capacitors. The oxide voltage used is larger than the designed power supply voltage because one wishes to observe failures in a short amount of time (see equation (2)). The fraction of devices which have failed is recorded as a function of time. For each observed breakdown time, DEFECT derives X_{eff} using (2). Next, DEFECT obtains the area density, $D(X_{\text{eff}})$, from (10). An ordered list of X_{eff} versus $D(X_{\text{eff}})$ is generated by DEFECT and is stored in a user-named output file which will be referenced by a .XEFF card in the CORS input deck (Section IV.B). Following is a description of the format in which time-to-breakdown data should be placed in the DEFECT input file.

Line 1: Oxide Thickness (\AA)

Line 2: Area of test structure (cm^2)

Line 3: Test temperature ($^{\circ}\text{C}$)

Line 4: 0.0

*The value 0.0 notifies DEFECT that
time-to-breakdown data will be provided*

Line 5: Voltage difference between V_{applied} and $V_{\alpha\alpha}$.
*This value will be subtracted from V_{applied}
by DEFECT to yield $V_{\alpha\alpha}$. This value may be
estimated using the equations in Section II.C.*

Line 6: V_{applied} (+ volts, the voltage applied to the test capacitor terminals)

Lines 7-: t_{BD} (sec), cumulative percent failed
*Lines 7- should consist of ordered pairs
ranging from from minimum t_{BD} on
line 7 to the maximum on the final line of the file.*

A DEFECT input file listing containing time-to-breakdown data may be found in Example 1 and a DEFECT output file listing is provided in Example 2.

A ramp-voltage-breakdown test is performed by applying a linearly increasing voltage waveform to an ensemble of identical large-area capacitors. A record of breakdown voltage (V_{BD}) versus the fraction of capacitors failed is generated.

V_{BD} may be related to X_{eff} by

$$1 = \frac{V_{BD}^2}{RG\tau X_{eff}} \exp \left[\frac{-GX_{eff}}{V_{BD}} \right] \quad (13)$$

which can be derived from (3). DEFECT subsequently derives $D(X_{eff})$ using (10). The input file format needed for DEFECT to process ramp-voltage-breakdown data is as follows.

Line 1: Oxide Thickness (\AA)

Line 2: Area of test structure (cm^2)

Line 3: Test temperature ($^{\circ}\text{C}$)

Line 4: Ramp rate (V/sec)

Line 5: Voltage difference between $V_{applied}$ and V_{ox} .
 *$V_{applied}$ is the ramp voltage at a given time.
The difference between this value and V_{ox}
may be inferred from the equations in Section II.C.
The value listed on line 5 will be subtracted from V_{BD} .*

Line 6: 0.0
*This is a dummy number, not used by DEFECT when V_{BD}
is being provided.*

Lines 7- V_{BD} (volts), cumulative percent failure
*Lines 7- should consist of ordered pairs ranging
from minimum V_{BD} on line 7 to the
largest observed V_{BD} on the final line
of the file.*

A DEFECT input file listing containing V_{BD} data may be found in Example 3. The DEFECT output file will be similar to that shown in Example 2.

If test capacitor breakdown data is not available, yet a CORS projection of circuit reliability is desired, the user may provide DEFECT with a statistical distribution which is believed to model the time-to-breakdown statistics for the oxide of interest. Specifically, the user may describe his/her hypothetical breakdown data with a one or two population lognormal or Weibull distribution. The parameters for these distributions are placed in a file which is then input to DEFECT to be properly formatted for use by CORS. The input file should be formatted as follows.

Line 1: Oxide Thickness (\AA)

Line 2: Area of test structure (cm^2)

Line 3: Test temperature ($^{\circ}\text{C}$)
The data on lines 1-3 is, of course, hypothetical.

Line 4: 0.0

Line 5: the voltage difference between V_{applied} (hypothetical)
and V_{ox} .
*See format description for time-to-breakdown data (above)
for an explanation.*

Line 6: V_{applied} (+ volts, the voltage applied to the hypothetical test capacitors)

Line 7: Lognormal
-or-
Weibull

Line 8: Number of populations (1 or 2)

Line 9: (if Lognormal) t50 *median*
-or-
(if Weibull) alpha *location parameter*

Line 10: (if Lognormal) sigma *shape parameter*
-or-
(if Weibull) beta " "
*If line 8 reads "2", then the information contained
on lines 9 and 10 pertains to one population of samples
and the following lines must be included to describe
the other population.*

Line 11: Fraction of samples following distribution #1
A number between 0 and 1.

Line 12: (if Lognormal) t50 *for population #2*
-or-
(if Weibull) alpha " "

Line 13: (if Lognormal) sigma *for population #2*
-or-
(if Weibull) beta " "

*****All parameters have units of seconds.*****

A sample DEFECT input file following the above format is contained in Example 4 along with the generated output file.

B. Using DEFECT to Obtain Defect Density per Unit Length

The user may also wish to provide CORS with data about the defect density per unit length along diffusion and/or field oxide edges. We will describe two possible techniques for obtaining these defect densities. The first method is to conduct a breakdown test on an ensemble of test capacitors which have a very large ratio of perimeter to area. If one can assume that the probability that one of these capacitors encompasses a severe area defect is negligible, the user may simply substitute the perimeter of the structures (cm) on line 2 of the DEFECT input

file. DEFECT will then output $D(X_{\text{eff}})$ values which have units of cm^{-1} . A second method for determining the density of defects along edges is to conduct breakdown tests on two ensembles of capacitors, each with identical area but different perimeter. The mathematics are as follows.

$$Y = 1 - F \quad Y \text{ is yield, } F \text{ is cumulative fraction failed}$$

Y_1 will represent the yield at some t_{BD} (or V_{BD}) for structures with area A and perimeter P_1 while Y_2 will represent the yield for structures with area A and perimeter P_2 ($P_1 > P_2$).

$$Y_1 = \exp \left[AD_A + P_1 D_P \right]$$

$$Y_2 = \exp \left[AD_A + P_2 D_P \right]$$

$$\frac{Y_1}{Y_2} = \exp \left[-(P_1 - P_2) D_P \right]$$

$$F' = 1 - \frac{Y_1}{Y_2}$$

The user should enter the value of $P_1 - P_2$ on line 2 of the DEFECT input file and should place the values of F' on line 7 and up.

IV. CORS Command Summary

A. Invoke CORS (.TTF card)

General form:

.TTF <G=G₃₀₀> <TAU=τ₃₀₀> <EB= E_b> <DELTA = δ > <QUICK> <t_{BD}¹ ... t_{BD}⁸>

Examples:

.TTF

.TTF G=300 TAU=10p QUICK

.TTF 3600 86400 2.59M 5.18M 7.77M 31.54M 63.07M .315G

The .TTF card must be present for CORS to be invoked by BERT. If it is not in the input deck, all other CORS commands will be ignored. G and TAU, which characterize time dependent dielectric breakdown for a particular technology, are obtained by conducting an intrinsic oxide breakdown study (instructions are included with Figure 2). EB and DELTA, which characterize the temperature acceleration of oxide breakdown, are obtained by conducting a study of the temperature dependence of breakdown (instructions are included with Figure 3). The inclusion of the QUICK option indicates that user wants the "quick" algorithm used (detailed in Sections II.D and II.E) which decreases the CORS run-time with some loss of accuracy. t_{BD}¹ through t_{BD}⁸ are the operating times for which the failure statistics will be generated. If the user wishes to specify the values of t_{BD}, he/she must specify all eight values.

name	parameter	units	default
G	G ₃₀₀	MV/cm	350
TAU	τ ₃₀₀	sec	1.0E-11
EB	E _b	eV	.28
DELTA	δ	eV	.0167
QUICK	-	-	not quick
-	t _{BD} ¹	sec	1 month
-	t _{BD} ²	sec	3 months
-	t _{BD} ³	sec	6 months
-	t _{BD} ⁴	sec	1 year
-	t _{BD} ⁵	sec	2 years
-	t _{BD} ⁶	sec	5 years
-	t _{BD} ⁷	sec	10 years
-	t _{BD} ⁸	sec	20 years

B. Associate Device Model with Defect Density Datafile (.XEFF card)

General form:

.XEFF MNAME FILENAME=areadata <DIFFEDGE=diffdata> <OXEDGE=foxdata>

Examples:

.XEFF POLYCAP FILENAME=DEFDATA

.XEFF NMOS1 FILENAME=MOSDATA DIFFEDGE=DRAINDATA OXEDGE=OXDATA

MNAME is the model name listed on a .MODEL (SPICE) or .ALTMODEL (CORS) card for a MOSFET or capacitor. There must be one .XEFF card for each MOSFET model name defined in the input deck. Each capacitor which the user wishes included in the breakdown projections will be associated with a model name which must also be found in a .XEFF card. The file named after keyword FILENAME should contain defect density (cm^{-2}) data appropriate for devices described by MNAME. The file named after keyword DIFFEDGE should contain defect density (cm^{-1}) data for the diffusion (source/drain) edges of a MOSFET or for the width-wise edges of a capacitor. The file named after keyword OXEDGE should contain defect density (cm^{-1}) data for the field oxide edges of a MOSFET or the length-wise edges of a capacitor. All data files should have been formatted by program DEFECT.

C. Capacitors

General form:

SPICE 2 or 3:

CXXXXXXXX N+ N- VALUE <IC=INCOND> <TBDMODEL=MNAME L=length W=width>

SPICE 3 only:

CXXXXXXXX N+ N- MNAME L=length <W=width> <IC=INCOND> <TBDMODEL=MNAME>

Examples:

C1 4 0 1.4P TBDMODEL=CMODEL L=10U W=50U

CABC 10 3 CAPMOD L=10U W=50U IC=5V TBDMODEL=CAPMOD

A capacitor is included in the dielectric breakdown calculations only if the TBDMODEL keyword is included on the card which defines the capacitor. If the first capacitor card format illustrated above is used, then an .ALTMODEL card which defines MNAME must be included in the deck.

D. MOSFETs

If the Level 1, 2 or 3 SPICE MOSFET model is being used, then no changes need be made to accommodate CORS. If the Level 4 model (BSIM) is being used, then an .ALTMODEL card must be created for each model (or "process") name which appears on a MOSFET definition card.

E. The .ALTMODEL Card

General form:

.ALTMODEL MNAME TYPE <parameters>

Examples:

.ALTMODEL NM1 NMOS VTO=.7 GAMMA=.4 TOX=20N PHI=.6 TPG=1
.ALTMODEL CAP1 C TOX=12.5N

MNAME is a model name which is also found on one or more MOSFET or capacitor definition cards. TYPE is the type of device, NMOS, PMOS or C (capacitor).

name	parameter	units	default
VTO	zero-bias threshold voltage	V	1.0
TOX	oxide thickness	meter	1.0e-7
GAMMA	bulk threshold parameter	V	0.0
PHI	surface potential	V	.6
TPG	type of gate material:	-	1
	+1 opposite of substrate		
	-1 same as substrate		
	0 Al gate		

F. Print Failure Probability for each Device (.EACHPROB card)

General form:

.EACHPROB <NUM>

Examples:

.EACHPROB
.EACHPROB 10

The .EACHPROB card, with no arguments following, appends a listing of the failure probability for each device to the CORS output. These individual failure probabilities are calculated for an operating time of t_{BD}^7 (default 10 years). If a value of NUM is specified, then the failure probabilities for just the NUM devices most likely to fail are provided.

G. Project Failures for Large Circuit with Identical Cells (.LSI card)

General form:

.LSI <num1> <num2> <num3>

Example:

.LSI 256K 1M

The .LSI card may be used to print out failure probabilities for large circuits which are constructed of cells identical to the circuit described in the input deck. The arguments (up to three) specify the number of cells in the large circuit(s).

H. Simulate Burn-In (.BURNIN card)

General form:

.BURNIN <TIME=burntime> <TEMP=burntemp>

Example:

.BURNIN TIME=14400 TEMP=150

The presence of a .BURNIN card indicates that the user wishes to have the effects of burn-in simulated. *The user may not request CAS or EM analysis along with burn-in. All other CORS commands are compatible with CAS and EM commands.* TIME is the duration of the burn-in trial, it has units of seconds. TEMP is the temperature (C°) during the burn-in trial.

To simulate burn-in, CORS must be run in a two-pass mode. During the first pass, the user should adjust the power supply voltage values defined in the input deck to the values used during burn-in. If the user typically performs burn-in using different signal waveforms from those during normal operation, the burn-in waveforms should be defined in the input deck during the first pass. During the second pass, the power supply voltage values defined in the input deck should be set to their normal operating values and signal waveforms should be those expected under normal conditions. *Except for voltage source cards, the input deck should be identical during both simulator passes.* Output is only generated after the second pass. Two temporary files are created during the first pass and not erased until the completion of the second pass; these are named rawtdb and rawburn.

I. .TRAN Card

General form:

.TRAN TSTEP TSTOP <TSTART<TMAX>>

Example:

.TRAN .1N 50N

The SPICE .TRAN card must be present in any BERT input deck. This card instructs SPICE to simulate the time-dependent behavior of the circuit described in the input deck. See a SPICE user's guide for more details on the .TRAN card.

J. Temperature Setting (.OPTIONS card)

General form:

.OPTIONS OPT1=optval OPT2=optval . . .

Example:

.OPTIONS TNOM=55

Simulation of circuit reliability at a given ambient temperature can be specified by using the SPICE .OPTIONS card as illustrated above. TNOM has units of C°.

V. Examples

Example 5 shows a CORS input deck for a simple RC circuit and the subsequent output. This example illustrates the proper use of the .ALTMODEL card. (The oxide defect density distribution used for this simulation is listed in Example 2.) Example 6 shows a CORS input deck and subsequent output for a 4-input nand gate. This example illustrates the proper use of the .EACHPROB and .LSI cards. The input deck shown in Example 7 is identical to that in Example 6 except that the QUICK option is specified on the .TTF card. Note that the failure projections are not very different from those in Example 6. Example 8 shows the proper use of the .BURNIN card. Example 9 is identical to Example 8 except that the QUICK option was requested. The user should compare the output listings in Example 8 and Example 9 to determine if the error introduced by using QUICK during a burn-in simulation is acceptable for his/her application.

References

- [1] P.M. Lee et al., "BERT - Circuit Aging Simulator (CAS)," University of California, Berkeley, Electronics Research Laboratory Memorandum UCB/ERL M90/2, January 1990.
- [2] B. K. Liew et al., "BERT - Circuit Electromigration Reliability Simulator," University of California, Berkeley, Electronics Research Laboratory Memorandum UCB/ERL M90/3, January 1990.
- [3] I. C. Chen et al., *IEEE Journal of Solid-State Circuits*, Vol. 20, pp. 333, Feb 1985.
- [4] J. Lee et al., *IEEE Transactions on Electron Devices*, Vol. 35, p. 2268, Dec. 1988.
- [5] E. Rosenbaum et al., *IEDM Technical Digest*, p. 331, Dec. 1989.
- [6] R. Moazzami et al., *IEEE Transactions on Electron Devices*, Vol. 36, p. 2462, Nov. 1989.
- [7] R. Moazzami et al., *VLSI Symposium Technical Digest*, May 1989.

Appendix A. CORS Simulations

This section provides the user with examples of the various kinds of studies which may be performed with CORS. All simulations were performed for CMOS circuits operating at 5.5V and 125C, unless otherwise stated.

Figure A.1 shows simulated reliability of 10K gate array after burn-in. (Each cell in the gate array is identical to the one described by the input deck listed in Example 6.) Power supply voltage during burn-in was 7 volts. These studies are useful for balancing conflicting goals such as cost, avoidance of hot electron degradation and reduction of field failures due to oxide breakdown in choosing the burn-in condition for a product.

CORS has an option for printing out the breakdown probability for individual devices. This is illustrated in Figure A.2.

Figure A.3 shows the effect of operating temperature on the reliability of a SRAM cell array. The results shown are for a circuit in which every memory cell is undergoing continuous read operations. Previous simulations were performed for a SRAM cell in the idle state as well as one undergoing continuous precharge and read operations. Both cells have nearly identical failure statistics. The simulator showed that under each of these conditions the same two transistors in the SRAM cell dominate circuit breakdown. The oxide field across those two transistors does not change appreciably during a read operation.

Figure A.4 shows the dramatic effect of oxide quality on the expected circuit lifetime of a 10K gate array (the input deck for this simulation was similar to the one listed in Example 6). Figure A.5 shows that the inclusion of edge defects can change the predicted lifetime depending on the relative density and severity of the edge defects (circuit simulated was the same as in Figure A.4). If the reader is unfamiliar with the variable X_{eff} plotted in Figure A.5, he/she can find a discussion of it in Section II.

Appendix B. Error Messages

Following is a list of the error codes generated by CORS. All have an identifier of the form Tnn<n>. CAS error messages can be recognized by the identifier Cnn<n>, EM error messages by Enn<n> [1][2]. Error messages with a 2-digit identifier (Tnn) are generated by the pre-processor; those with a 3-digit identifier (Tnnn) come from the post processor. In addition to the one line error message which is printed out by CORS, the following list contains suggestions for the user who may be puzzled by the occurrence of an error message. It also contains the source code location of each error message.

T01: Cannot open rawtddb file!

Line 52, tddb.c

This error usually occurs when the user who wishes to do a burn-in simulation accidentally deletes file rawtddb between the first and second CORS runs.

T02: Cannot open rawtddb file!

Line 60, tddb.c

User's computer will not allow CORS to open a new file for writing.

T03: Cannot open rawinp2 file!

Line 72, tddb.c

User's computer will not allow CORS to open a new file for writing.

T04: Not enough time-to-breakdown values on .TTF card!

Line 169, tddb.c

CORS requires that zero or eight time-to-breakdown values be specified on a .TTF card.

T05: Burnin card formatted incorrectly.

Line 266, tddb.c

CORS found a keyword on a .BURNIN card that was neither TIME nor TEMP.

T06: No .TRAN card. Cannot do tddb analysis!

Line 353, tddb.c

CORS did not find a .TRAN card in the input deck. This SPICE command must be specified for CORS or CAS to run.

T07: Insufficient memory space. Reduce the number of MOS models!

Line 395, tddb.c

User's file system ran out of memory during execution of pre-processor. The user should try to free additional memory space. Simulation of a smaller circuit may be feasible.

T08: Not enough arguments on a .XEFF card!

Line 418, tddb.c

T09: Not enough arguments on a .XEFF card!

Line 435, tddb.c

T10: .XEFF card formatted incorrectly!

Line 447, tddb.c

CORS did not find keyword FILENAME in its expected position.

T11: .XEFF card formatted incorrectly!

Line 456, tddb.c

CORS did not find a user provided file name after keyword FILENAME.

T12: .XEFF card formatted incorrectly!

Line 465, tddb.c

CORS did not find a "=" after keyword FILENAME.

- T13: .XEFF card formatted incorrectly!
Line 474, tddb.c
CORS did not find a user provided file name after keyword FILENAME.
- T14: Insufficient memory space. Reduce the number of transistors.
Line 541, tddb.c
See T07.
- T15: No model name specified on a MOSFET definition card!
Line 560, tddb.c
- T16: Capacitor card in deck not formatted correctly.
Line 611, tddb.c
Some capacitor definition card does not contain the minimum number of parameters required by SPICE.
- T17: Capacitor card in deck not formatted correctly.
Line 643, tddb.c
Keyword TBDMODEL may be spelled incorrectly.
- T18: Insufficient memory space. Reduce # of tddb capacitors.
Line 657, tddb.c
See T07.
- T19: Missing an XEFF statement for some MOS model!
Line 1104, tddb.c
CORS found a model name on a .MODEL card for a MOSFET and did not find a .XEFF card which contains this same model name. Every MOSFET model name must appear on a .XEFF card.
- T20: A tddb data file can not be found!
Line 1213, tddb.c
CORS can not find a file which was named on .XEFF card. Spelling errors are a common cause of this problem or the user may have the file stored in a directory different from the one CORS is searching.
- T21: A tddb data file can not be found!
Line 1133, tddb.c
See T20.
- T22: A tddb data file can not be found!
Line 1144, tddb.c
See T20.
- T23: Insufficient memory space. Reduce the number of transistors.
Line 1581, tddb.c
See T07.
- T24: Insufficient memory space. Reduce the number of capacitors.
Line 1588, tddb.c
See T07.
- T101: Can not open file rawtddb!
Line 43, postddb.c
User may have deleted file rawtddb between execution of pre- and post-processor or maybe never ran the pre-processor.
- T102: Insufficient memory space. Reduce the number of transistors.
Line 72, postddb.c
User's file system ran out of memory during execution of post-processor. The user

should try to free additional memory space. Simulation of a smaller circuit may be feasible.

T103:Insufficient memory space. Reduce the number of models.

Line 79, postddb.c

See T102.

T104:Insufficient memory space. Reduce the number of capacitors.

Line 87, postddb.c

See T102.

T105:Insufficient memory space. Reduce the number of MOS devices.

Line 104, postddb.c

See T102.

T106:Cannot open file rawburn!!!

Line 146, postddb.c

There are two causes of this error. The user may have deleted file rawburn between runs 1 and 2 of a burn-in simulation. Alternately, CORS may have detected a rawtddb file from a previous failed run (this file is automatically deleted after successful runs). CORS now assumes it is doing pass 2 of a burn-in simulation. The solution is to delete all the raw**** files and retry CORS.

T107:Rawtddb not formatted correctly!

Line 160, postddb.c

T108:Cannot open file rawburn for writing.

Line 170, postddb.c

User's computer will not allow CORS to open a new file for writing.

T109:Can not open rawout1 file!

Line 206, postddb.c

CORS can not find file rawout1 which should have been created in postbert.c (CAS).

T110:Can not create rawout2 file.

Line 212, postddb.c

See T108.

T111:Can not create outtddb file.

Line 218, postddb.c

See T108.

T112:Voltage node printout for tddb analysis not found

Line 284, postddb.c

Header in SPICE output can not be located. User may be using a version of SPICE other than those CORS was developed for.

T113:Division by zero in reading times.

Line 295, postddb.c

Step size specified on .TRAN card is so small that a divide-by-zero error is anticipated.

T114:Insufficient memory space. Reduce the number of timesteps.

Line 309, postddb.c

See T102.

T115:Insufficient memory space. Reduce the number of timesteps.

Line 315, postddb.c

See T102.

T116:Insufficient memory space. Reduce the number of timesteps.

Line 321, postddb.c

See T102.

T117:Insufficient memory space. Reduce the number of timesteps.

Line 327, postddb.c

See T102.

T118:Insufficient memory space. Reduce the number of timesteps.

Line 333, postddb.c

See T102.

T119:Voltage node printout for tddb analysis not found.

Line 346, postddb.c

See T112.

T120:Division by zero in reading times.

Line 358, postddb.c

See T113.

T121:Timesteps too small in reading voltages.

Line 385, postddb.c

Try a larger step-size on .TRAN card.

T122:Voltage printout for TDDB analysis not found.

Line 408, postddb.c

See T112.

T123:Voltage printout for TDDB analysis not found.

Line 415, postddb.c

See T112.

T124:Voltage printout for TDDB analysis not found.

Line 427, postddb.c

See T112.

T125:Division by zero in reading times.

Line 437, postddb.c

See T113.

T126:Voltage node printout for tddb analysis not found.

Line 488, postddb.c

See T112.

T127:Division by zero in reading times.

Line 499, postddb.c

See T113.

T128:Insufficient memory space. Reduce the number of timesteps.

Line 513, postddb.c

See T102.

T129:Insufficient memory space. Reduce the number of timesteps.

Line 519, postddb.c

See T102.

T130:Insufficient memory space. Reduce the number of timesteps.

Line 525, postddb.c

See T102.

T131:Voltage node printout for tddb analysis not found.

Line 538, postddb.c

See T112.

T132:Division by zero in reading times.

Line 550, postddb.c

See T113.

T133:Timesteps too small in reading voltages.

Line 577, postddb.c

See T121.

T134:Can not open a defect density data file!

Line 1038, postddb.c

CORS can not find one of the file names originally listed on a .XEFF card with keyword FILENAME.

T135:Can not open a defect density data file!

Line 1078, postddb.c

CORS can not find one of the filenames originally listed on a .XEFF card with keyword DIFFEDGE.

T136:Can not open a defect density data file!

Line 1115, postddb.c

CORS can not find one of the filenames originally listed on a .XEFF card with keyword OXEDGE.

T137:Can not open a defect density data file!

Line 1146, postddb.c

See T134.

T138:Can not open a defect density data file!

Line 1190, postddb.c

See T136.

T139:Can not open a defect density data file!

Line 1219, postddb.c

See T135.

T140:Could not find model name.

Line 1282, postddb.c

CORS found a model name on a MOSFET definition card without finding a corresponding .MODEL card to define the model. Or the error may have arisen in CORS's storage of this information.

T141:Could not find model name.

Line 1717, postddb.c

CORS found a model name on a capacitor definition card without finding a corresponding .MODEL card to define the model. Or the error may have arisen in CORS's storage of this information

T201:N-R method did not converge within .01 percent in tddb calc.

Line 140, nrcalcs.c

CORS solves for Xeff iteratively, using Newton-Raphson's method. The calculations had not converged after 100 iterations.

T202:N-R method did not converge within .01 percent in tddb calc.

Line 204, nrcalcs.c

CORS solves for Xeff iteratively, using Newton-Raphson's method. The calculations had not converged after 100 iterations.

T203:N-R method did not converge within .01 percent in tddb calc.

Line 241, nrcalcs.c

CORS solves for X_{eff} iteratively, using Newton-Raphson's method. The calculations had not converged after 100 iterations.

CORS Flow Chart

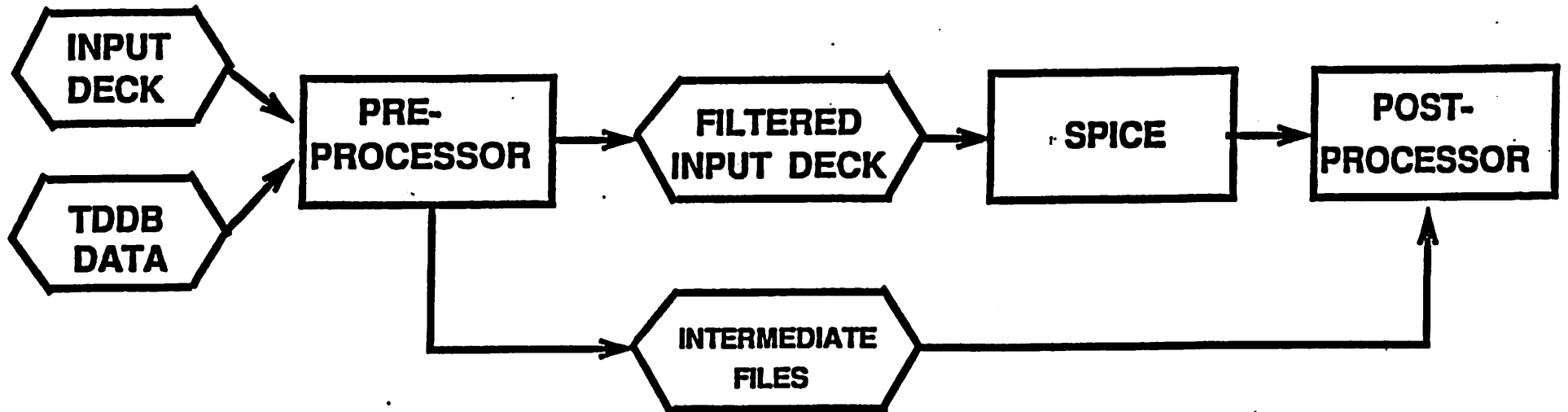


Figure 1

125
.1
27
0.0
1.2
9
.2,13.3
.4,16.7
.6,20
1.6,23.3
1.8,25
2,26.7
2.4,28.3
3.4,30
4,31.7
4.2,33.3
6,35
6.4,36.7
7.8,38.3
9.4,40
12,41.7
12.2,43.3
13.4,45
13.8,46.7
14,50
16.6,51.7
17.2,53.3
20.8,55
24.4,56.7
32.4,58.3
36.6,60
39.4,61.7
50,63.3
51.8,65
53.4,66.7
68.2,68.3
68.6,70
84.4,71.7
87,73.3
138,75
230,76.7
275,78.3
650,81.7
673,83.3
1100,85
1165,86.7
1209,88.3
1250,90

Example 1

Listing of input file for DEFECT. Contains time-to-breakdown data.

52.859482 1.427163
54.404210 1.827216
55.307817 2.231436
57.493666 2.652685
57.756153 2.876821
57.990957 3.106096
58.397273 3.326794
59.173500 3.566749
59.535685 3.812604
59.644417 4.049652
60.439293 4.307829
60.583122 4.572849
61.023990 4.828863
61.439810 5.108256
61.984021 5.395681
62.020858 5.673960
62.229939 5.978370
62.295490 6.292339
62.327557 6.931472
62.707183 7.277386
62.786313 7.614260
63.209838 7.985077
63.565586 8.370176
64.197553 8.746691
64.469194 9.162907
64.633478 9.597203
65.164452 10.023934
65.243270 10.498221
65.311064 10.996128
65.856248 11.488535
65.869281 12.039728
66.331208 12.623084
66.398824 13.205066
67.426966 13.862944
68.565377 14.567168
68.963604 15.278579
70.880624 16.982691
70.958118 17.897615
72.053060 18.971200
72.181005 20.174062
72.263623 21.455813
72.337946 23.025851

Example 2

Listing of DEFECT output file. Input file is displayed in Ex. 1. This oxide has an unacceptably high defect density for commercial applications!

125
.1
27
1
1.2
0
7.8,1.8
8.4,3.6
8.6,8.9
8.8,10.7
9,19.6
9.4,26.8
9.6,37.5
9.8,39.3
10,41.1
10.2,46.4
10.4,50
10.6,57.1
10.8,66.1
11,69.6
11.2,76.8
11.4,78.6
13,80.4
13.6,82.1
13.8,83.9
14,87.5
15.2,89.3
15.6,91.1

Example 3.

Listing of DEFECT input file containing ramp-voltage-breakdown data.

***Input file ***

125
.01
27
0
0
9
Lognormal
1
20
2

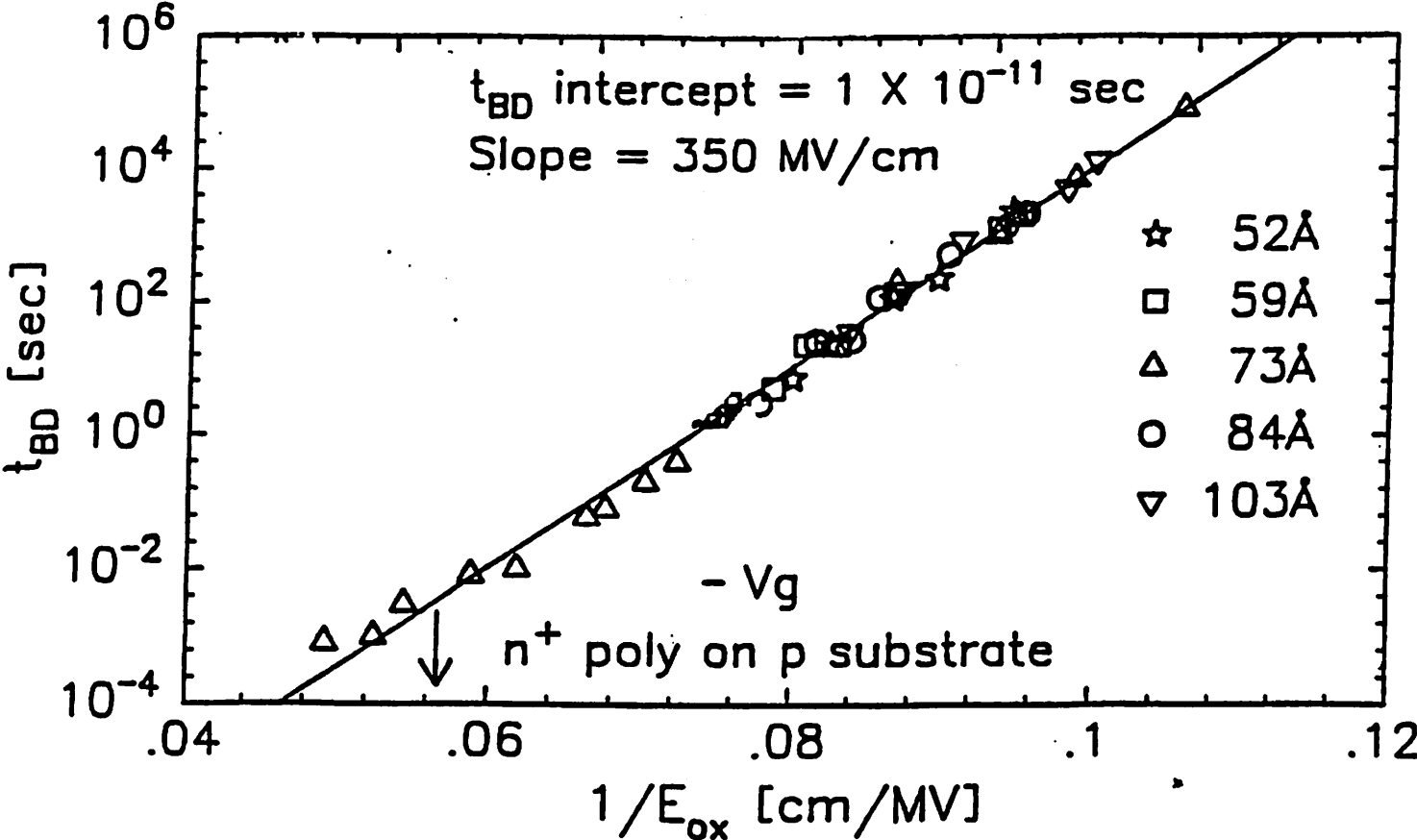
*** Output file ***

Temp= 27
Vox= 9.000000
Area= 0.010000
Lognormal
numpop= 1
t50_1/sigma1: 20 2

Example 4

Listings of DEFECT input and output files containing parameters for a lognormal time-to-breakdown distribution.

Measuring G_{300} and τ_{300}

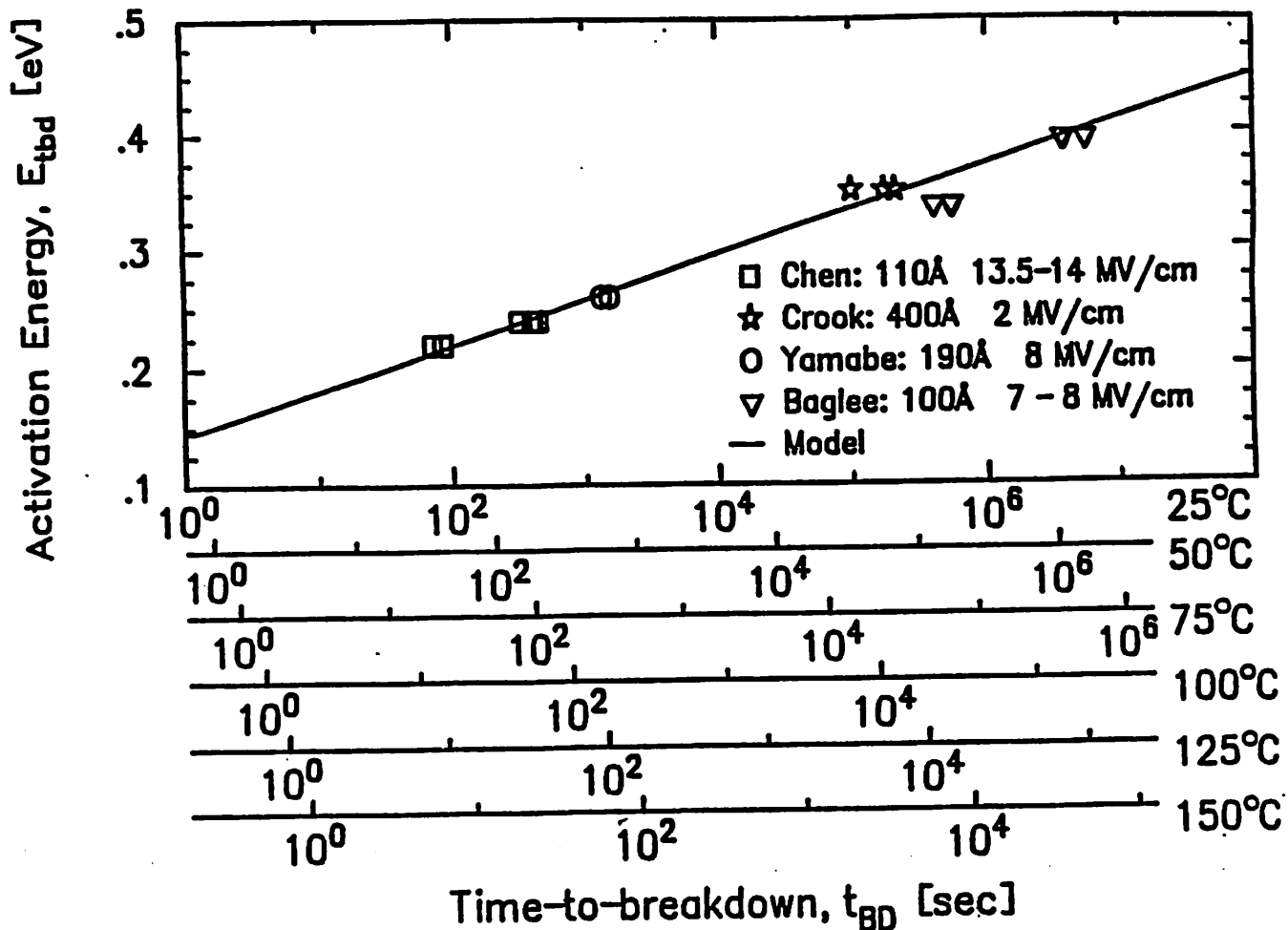


-30-

Figure 2

Take an ensemble of *small* area capacitors and measure intrinsic time-to-breakdown as a function of electric field at room temperature. Plot $\log(t_{BD})$ vs $\frac{1}{E_{ox}}$ shown above. The slope is G_{300} and the y-intercept is τ_{300} .

Determination of E_b and δ



$$\text{Activation Energy: } E_{tbd} = k_B \frac{d(\ln(t_{BD}))}{d\left(\frac{1}{T}\right)}$$

Figure 3 The t_{BD} in the above equation is measured for some arbitrary breakdown test yield. E_{tbd} was plotted (above) for several researchers' data and consistent results were found. Solving (4) and (5) for E_{tbd} , one finds

$$E_{tbd} = \frac{\ln\left[\frac{t_{BD}(T)}{\tau}\right] + \frac{E_b}{k_B} \left[\frac{1}{T} - \frac{1}{300}\right]}{1 + \frac{\delta}{k_B} \left[\frac{1}{T} - \frac{1}{300}\right]} * \delta - E_b$$

$\delta = .0167\text{eV}$ and $E_b = .28\text{eV}$ are obtained from the linear fit shown in the above figure. These are believed to be valid for all oxides at temperatures 25-150° C. However, the user may repeat this experiment and provide CORS with different values of δ and E_b .

Input Deck

```
SAMPLE CIRCUIT
C1 2 0 1.4P
+ TBDMODEL=CMOD L=10U W=50U
R1 1 2 1K
VIN 1 0 PULSE(0 5 5n 5n 5n 10n 30n)
.ALTMODEL CMOD C TOX=12.5N
.TRAN .5N 60N
.XEFF CMOD FILENAME=data125
.TTF
.PRINT tran v(1) v(2)
.END
```

CORS Output

TDDB STATISTICS
Operating Temperature=

```
number seconds 2.592e+06
number seconds 7.776e+06
number seconds 1.66752e+07
number seconds 3.1536e+07
number seconds 6.3072e+07
number seconds 1.5768e+08
number seconds 3.1536e+08
number seconds 6.3072e+08
```

SAMPLE CIRCUIT

27

```
fraction failed 2.131181e-05
fraction failed 2.779222e-05
fraction failed 3.983974e-05
fraction failed 4.368089e-05
fraction failed 5.299287e-05
fraction failed 6.692421e-05
fraction failed 7.033430e-05
fraction failed 7.523625e-05
```

Example 5

```

FOUR INPUT CMOS NAND GATE
MPA 2 3 1 1 MODP W=20U L=1U
MPB 2 4 1 1 MODP W=20U L=1U
MPC 2 5 1 1 MODP W=20U L=1U
MPD 2 6 1 1 MODP W=20U L=1U
MNA 9 3 0 0 MODN W=32U L=1U
MNB 8 4 9 0 MODN W=32U L=1U
MNC 7 5 8 0 MODN W=32U L=1U
MND 2 6 7 0 MODN W=32U L=1U
CLOAD 2 0 30F
.MODEL MODP PMOS VTO=-.7 TOX=12.5N KP=8U GAMMA=.4 TPG=-1
.MODEL MODN NMOS VTO=.7 TOX=12.5N KP=20U GAMMA=.4
VDD 1 0 5.5
VA 3 0 PWL(0 5.5 79N 5.5 80N 0 85N 0 87N 5.5 117N 5.5 119N 0 160N 0)
VB 4 0 5.5
VD 6 0 5.5
VC 5 0 PWL(0 0 5N 0 7N 5.5 37N 5.5 39N 0 80N 0 81N 5.5 160N 5.5)
.TRAN 1N 160N
.TTF
.XEFF MODP FILENAME=data125
.XEFF MODN FILENAME=data125
.LSI 16K 64K
.EACHPROB
.options reltol=.01 abstol=1e-9 vntol=.0001 itl1=2000 itl2=500
.END

```

Example 6

FOUR INPUT CMOS NAND GATE

TDDB STATISTICS

Operating Temperature= 27

number seconds 2.592e+06	fraction failed 7.841907e-06
number seconds 7.776e+06	fraction failed 1.080054e-05
number seconds 1.66752e+07	fraction failed 1.297638e-05
number seconds 3.1536e+07	fraction failed 1.547089e-05
number seconds 6.3072e+07	fraction failed 1.743291e-05
number seconds 1.5768e+08	fraction failed 1.953538e-05
number seconds 3.1536e+08	fraction failed 2.104177e-05
number seconds 6.3072e+08	fraction failed 2.297238e-05

TDDB STATISTICS FOR 16000 IDENTICAL CELLS

number seconds 2.592e+06	fraction failed 0.117919
number seconds 7.776e+06	fraction failed 0.158702
number seconds 1.66752e+07	fraction failed 0.187487
number seconds 3.1536e+07	fraction failed 0.219278
number seconds 6.3072e+07	fraction failed 0.243406
number seconds 1.5768e+08	fraction failed 0.268435
number seconds 3.1536e+08	fraction failed 0.285857
number seconds 6.3072e+08	fraction failed 0.30758

TDDB STATISTICS FOR 64000 IDENTICAL CELLS

number seconds 2.592e+06	fraction failed 0.394611
number seconds 7.776e+06	fraction failed 0.499045
number seconds 1.66752e+07	fraction failed 0.564166
number seconds 3.1536e+07	fraction failed 0.628477
number seconds 6.3072e+07	fraction failed 0.672319
number seconds 1.5768e+08	fraction failed 0.713574
number seconds 3.1536e+08	fraction failed 0.7399
number seconds 6.3072e+08	fraction failed 0.770132

Probability of Failure at 3.1536e+08 seconds

MNB 5.244740e-06
MNA 5.174992e-06
MND 4.932426e-06
MNC 4.912059e-06
MPA 3.906532e-07
MPC 3.870731e-07
MPB 0.000000e+00
MPD 0.000000e+00

Example 6

```

FOUR INPUT CMOS NAND GATE
MPA 2 3 1 1 MODP W=20U L=1U
MPB 2 4 1 1 MODP W=20U L=1U
MPC 2 5 1 1 MODP W=20U L=1U
MPD 2 6 1 1 MODP W=20U L=1U
MNA 9 3 0 0 MODN W=32U L=1U
MNB 8 4 9 0 MODN W=32U L=1U
MNC 7 5 8 0 MODN W=32U L=1U
MND 2 6 7 0 MODN W=32U L=1U
CLOAD 2 0 30F
.MODEL MODP PMOS VTO=-.7 TOX=12.5N KP=8U GAMMA=.4 TPG=-1
.MODEL MODN NMOS VTO=.7 TOX=12.5N KP=20U GAMMA=.4
VDD 1 0 5.5
VA 3 0 PWL(0 5.5 79N 5.5 80N 0 85N 0 87N 5.5 117N 5.5 119N 0 160N 0)
VB 4 0 5.5
VD 6 0 5.5
VC 5 0 PWL(0 0 5N 0 7N 5.5 37N 5.5 39N 0 80N 0 81N 5.5 160N 5.5)
.TRAN 1N 160N
.TTF QUICK
.XEFF MODP FILENAME=data125
.XEFF MODN FILENAME=data125
.LSI 16K 64K
.EACHPROB
.options reltol=.01 abstol=1e-9 vntol=.0001 itl1=2000 itl2=500
.END

```

Example 7

FOUR INPUT CMOS NAND GATE

TDDB STATISTICS

Operating Temperature= 27

number seconds 2.592e+06	fraction failed 7.841907e-06
number seconds 7.776e+06	fraction failed 1.091490e-05
number seconds 1.66752e+07	fraction failed 1.314527e-05
number seconds 3.1536e+07	fraction failed 1.571562e-05
number seconds 6.3072e+07	fraction failed 1.757264e-05
number seconds 1.5768e+08	fraction failed 1.979985e-05
number seconds 3.1536e+08	fraction failed 2.145751e-05
number seconds 6.3072e+08	fraction failed 2.350215e-05

TDDB STATISTICS FOR 16000 IDENTICAL CELLS

number seconds 2.592e+06	fraction failed 0.117919
number seconds 7.776e+06	fraction failed 0.16024
number seconds 1.66752e+07	fraction failed 0.18968
number seconds 3.1536e+07	fraction failed 0.222329
number seconds 6.3072e+07	fraction failed 0.245096
number seconds 1.5768e+08	fraction failed 0.271524
number seconds 3.1536e+08	fraction failed 0.290592
number seconds 6.3072e+08	fraction failed 0.313424

TDDB STATISTICS FOR 64000 IDENTICAL CELLS

number seconds 2.592e+06	fraction failed 0.394611
number seconds 7.776e+06	fraction failed 0.502698
number seconds 1.66752e+07	fraction failed 0.568852
number seconds 3.1536e+07	fraction failed 0.634251
number seconds 6.3072e+07	fraction failed 0.675237
number seconds 1.5768e+08	fraction failed 0.718382
number seconds 3.1536e+08	fraction failed 0.746729
number seconds 6.3072e+08	fraction failed 0.777795

Probability of Failure at 3.1536e+08 seconds

MNB 5.549167e-06
MNA 5.200911e-06
MND 4.994622e-06
MNC 4.923741e-06
MPA 4.019757e-07
MPC 3.872671e-07
MPB 0.000000e+00
MPD 0.000000e+00

Example 7

**** Input deck used during pass #1. ****

FOUR INPUT CMOS NAND GATE

MPA 2 3 1 1 MODP W=20U L=1U

MPB 2 4 1 1 MODP W=20U L=1U

MPC 2 5 1 1 MODP W=20U L=1U

MPD 2 6 1 1 MODP W=20U L=1U

MNA 9 3 0 0 MODN W=32U L=1U

MNB 8 4 9 0 MODN W=32U L=1U

MNC 7 5 8 0 MODN W=32U L=1U

MND 2 6 7 0 MODN W=32U L=1U

CLOAD 2 0 30F

.MODEL MODP PMOS VTO=-.7 TOX=12.5N KP=8U GAMMA=.4 TPG=-1

.MODEL MODN NMOS VTO=.7 TOX=12.5N KP=20U GAMMA=.4

VDD 1 0 7

VA 3 0 PWL(0 7 79N 7 80N 0 85N 0 87N 7 117N 7 119N 0 160N 0)

VB 4 0 7

VD 6 0 7

VC 5 0 PWL(0 0 5N 0 7N 7 37N 7 39N 0 80N 0 81N 7 160N 7)

.TRAN 1N 160N

.TTF

.XEFF MODP FILENAME=data125

.XEFF MODN FILENAME=data125

.LSI 64K

.BURNIN TIME=28800 TEMP=125

.options reftol=.01 abstol=1e-9 vntol=.0001 itl1=2000 itl2=500

.END

**** Input deck used during pass #2. ****

FOUR INPUT CMOS NAND GATE

MPA 2 3 1 1 MODP W=20U L=1U

MPB 2 4 1 1 MODP W=20U L=1U

MPC 2 5 1 1 MODP W=20U L=1U

MPD 2 6 1 1 MODP W=20U L=1U

MNA 9 3 0 0 MODN W=32U L=1U

MNB 8 4 9 0 MODN W=32U L=1U

MNC 7 5 8 0 MODN W=32U L=1U

MND 2 6 7 0 MODN W=32U L=1U

CLOAD 2 0 30F

.MODEL MODP PMOS VTO=-.7 TOX=12.5N KP=8U GAMMA=.4 TPG=-1

.MODEL MODN NMOS VTO=.7 TOX=12.5N KP=20U GAMMA=.4

VDD 1 0 5.5

VA 3 0 PWL(0 5.5 79N 5.5 80N 0 85N 0 87N 5.5 117N 5.5 119N 0 160N 0)

VB 4 0 5.5

VD 6 0 5.5

VC 5 0 PWL(0 0 5N 0 7N 5.5 37N 5.5 39N 0 80N 0 81N 5.5 160N 5.5)

.TRAN 1N 160N

.TTF

.XEFF MODP FILENAME=data125

.XEFF MODN FILENAME=data125

.LSI 64K

.BURNIN TIME=28800 TEMP=125

.options reftol=.01 abstol=1e-9 vntol=.0001 itl1=2000 itl2=500

.END

Example 8

TDDB STATISTICS

Operating Temperature=

27

Prior to Operation, Burn In was Conducted for
seconds= 28800.000000 temperature= 125

*** The Yield after Burn-In was 0.999847 ***

number seconds	2.592e+06	fraction failed	5.719652e-09
number seconds	7.776e+06	fraction failed	1.713684e-08
number seconds	1.66752e+07	fraction failed	3.674918e-08
number seconds	3.1536e+07	fraction failed	6.950972e-08
number seconds	6.3072e+07	fraction failed	1.388086e-07
number seconds	1.5768e+08	fraction failed	3.460567e-07
number seconds	3.1536e+08	fraction failed	6.883102e-07
number seconds	6.3072e+08	fraction failed	1.361870e-06

TDDB STATISTICS FOR 64000 IDENTICAL CELLS

number seconds	2.592e+06	fraction failed	0.000365991
number seconds	7.776e+06	fraction failed	0.00109616
number seconds	1.66752e+07	fraction failed	0.00234918
number seconds	3.1536e+07	fraction failed	0.00443874
number seconds	6.3072e+07	fraction failed	0.00884441
number seconds	1.5768e+08	fraction failed	0.0219042
number seconds	3.1536e+08	fraction failed	0.0430957
number seconds	6.3072e+08	fraction failed	0.0834693

Example 8

**** Input deck used during pass #1. ****

FOUR INPUT CMOS NAND GATE

MPA 2 3 1 1 MODP W=20U L=1U
MPB 2 4 1 1 MODP W=20U L=1U
MPC 2 5 1 1 MODP W=20U L=1U
MPD 2 6 1 1 MODP W=20U L=1U
MNA 9 3 0 0 MODN W=32U L=1U
MNB 8 4 9 0 MODN W=32U L=1U
MNC 7 5 8 0 MODN W=32U L=1U
MND 2 6 7 0 MODN W=32U L=1U
CLOAD 2 0 30F

.MODEL MODP PMOS VTO=-.7 TOX=12.5N KP=8U GAMMA=.4 TPG=-1

.MODEL MODN NMOS VTO=.7 TOX=12.5N KP=20U GAMMA=.4

VDD 1 0 7

VA 3 0 PWL(0 7 79N 7 80N 0 85N 0 87N 7 117N 7 119N 0 160N 0)

VB 4 0 7

VD 6 0 7

VC 5 0 PWL(0 0 5N 0 7N 7 37N 7 39N 0 80N 0 81N 7 160N 7)

.TRAN 1N 160N

.TTF QUICK

.XEFF MODP FILENAME=data125

.XEFF MODN FILENAME=data125

.LSI 64K

.BURNIN TIME=28800 TEMP=125

.options reltol=.01 abstol=1e-9 vntol=.0001 itl1=2000 itl2=500

.END

**** Input deck used during pass #2. ****

FOUR INPUT CMOS NAND GATE

MPA 2 3.1 1 1 MODP W=20U L=1U
MPB 2 4 1 1 MODP W=20U L=1U
MPC 2 5 1 1 MODP W=20U L=1U
MPD 2 6 1 1 MODP W=20U L=1U
MNA 9 3 0 0 MODN W=32U L=1U
MNB 8 4 9 0 MODN W=32U L=1U
MNC 7 5 8 0 MODN W=32U L=1U
MND 2 6 7 0 MODN W=32U L=1U
CLOAD 2 0 30F

.MODEL MODP PMOS VTO=-.7 TOX=12.5N KP=8U GAMMA=.4 TPG=-1

.MODEL MODN NMOS VTO=.7 TOX=12.5N KP=20U GAMMA=.4

VDD 1 0 5.5

VA 3 0 PWL(0 5.5 79N 5.5 80N 0 85N 0 87N 5.5 117N 5.5 119N 0 160N 0)

VB 4 0 5.5

VD 6 0 5.5

VC 5 0 PWL(0 0 5N 0 7N 5.5 37N 5.5 39N 0 80N 0 81N 5.5 160N 5.5)

.TRAN 1N 160N

.TTF QUICK

.XEFF MODP FILENAME=data125

.XEFF MODN FILENAME=data125

.LSI 64K

.BURNIN TIME=28800 TEMP=125

.options reltol=.01 abstol=1e-9 vntol=.0001 itl1=2000 itl2=500

.END

Example 9

TDDB STATISTICS

Operating Temperature=

27

Prior to Operation, Burn In was Conducted for
seconds= 28800.000000 temperature= 125

*** The Yield after Burn-In was 0.999847 ***

number seconds	2.592e+06	fraction failed	8.079108e-09
number seconds	7.776e+06	fraction failed	2.427901e-08
number seconds	1.66752e+07	fraction failed	5.197523e-08
number seconds	3.1536e+07	fraction failed	9.837406e-08
number seconds	6.3072e+07	fraction failed	1.963456e-07
number seconds	1.5768e+08	fraction failed	4.887101e-07
number seconds	3.1536e+08	fraction failed	9.697074e-07
number seconds	6.3072e+08	fraction failed	1.909520e-06

TDDB STATISTICS FOR 64000 IDENTICAL CELLS

number seconds	2.592e+06	fraction failed	0.000516929
number seconds	7.776e+06	fraction failed	0.00155265
number seconds	1.66752e+07	fraction failed	0.00332089
number seconds	3.1536e+07	fraction failed	0.00627616
number seconds	6.3072e+07	fraction failed	0.0124875
number seconds	1.5768e+08	fraction failed	0.0307934
number seconds	3.1536e+08	fraction failed	0.0601747
number seconds	6.3072e+08	fraction failed	0.115037

Example 9

Lifetime after Burn-In

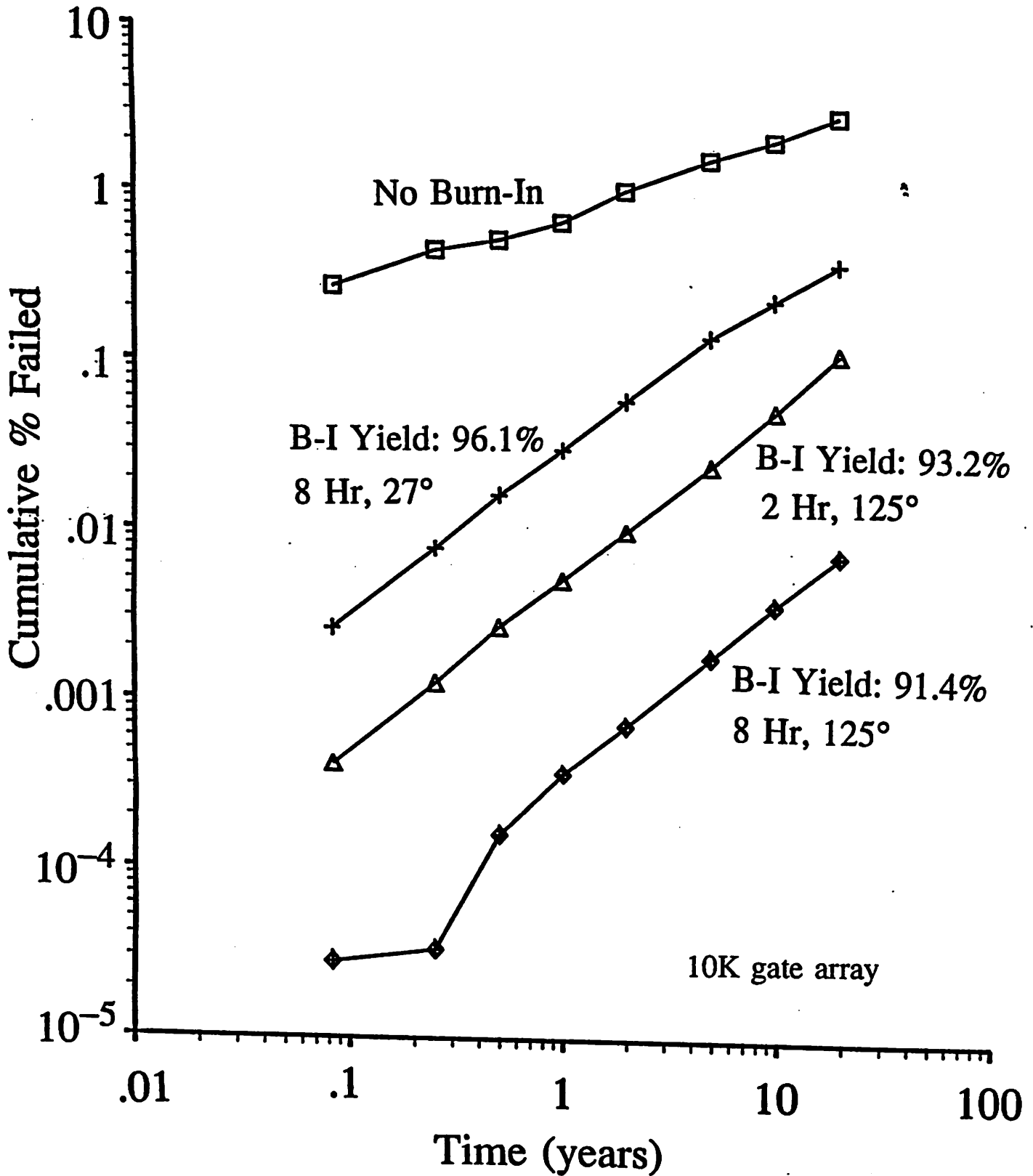


Figure A.1

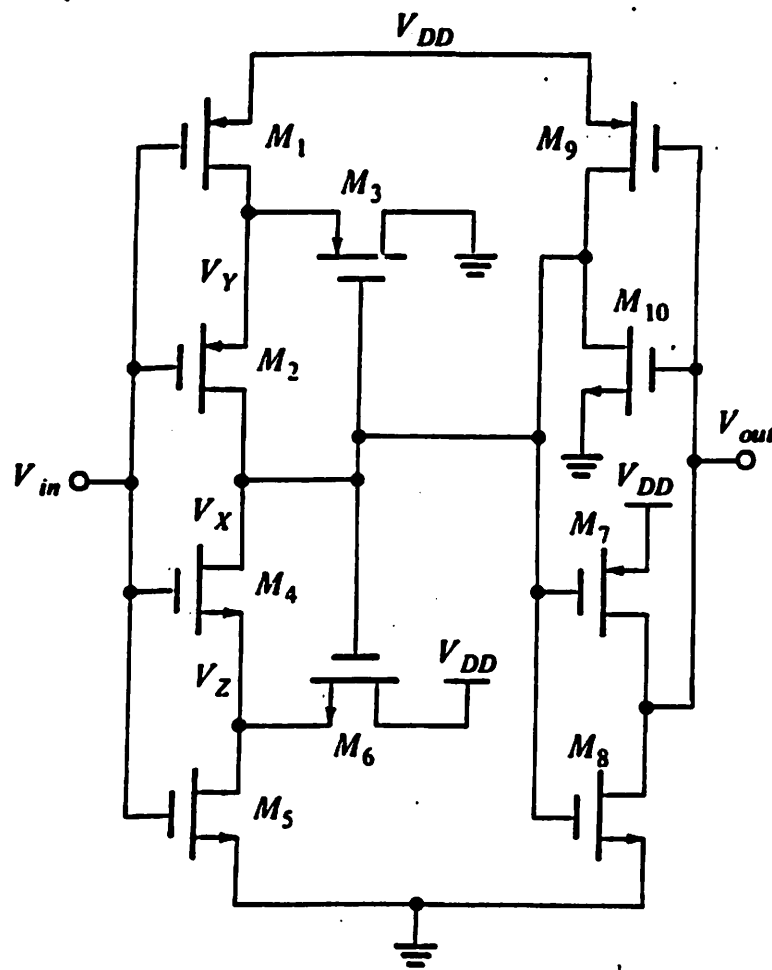
Device Failure Probabilities

$$\left(\frac{W}{L}\right)_{4,5,8} = \frac{10}{1}$$

$$\left(\frac{W}{L}\right)_{6,10} = \frac{1}{1}$$

$$\left(\frac{W}{L}\right)_{1,2,7} = \frac{20}{1}$$

$$\left(\frac{W}{L}\right)_{3,9} = \frac{2}{1}$$



Schmitt Trigger

cumulative % circuits failed

	CF% at 10 yrs
M1	1.08×10^{-8}
M2	1.11×10^{-8}
M3	1.43×10^{-9}
M4	5.10×10^{-9}
M5	5.40×10^{-9}
M6	3.53×10^{-13}
M7	1.43×10^{-8}
M8	1.23×10^{-8}
M9	2.80×10^{-9}
M10	1.23×10^{-9}

Figure A.2

Temperature Effects

256K SRAM

PERCENT CIRCUITS FAILED

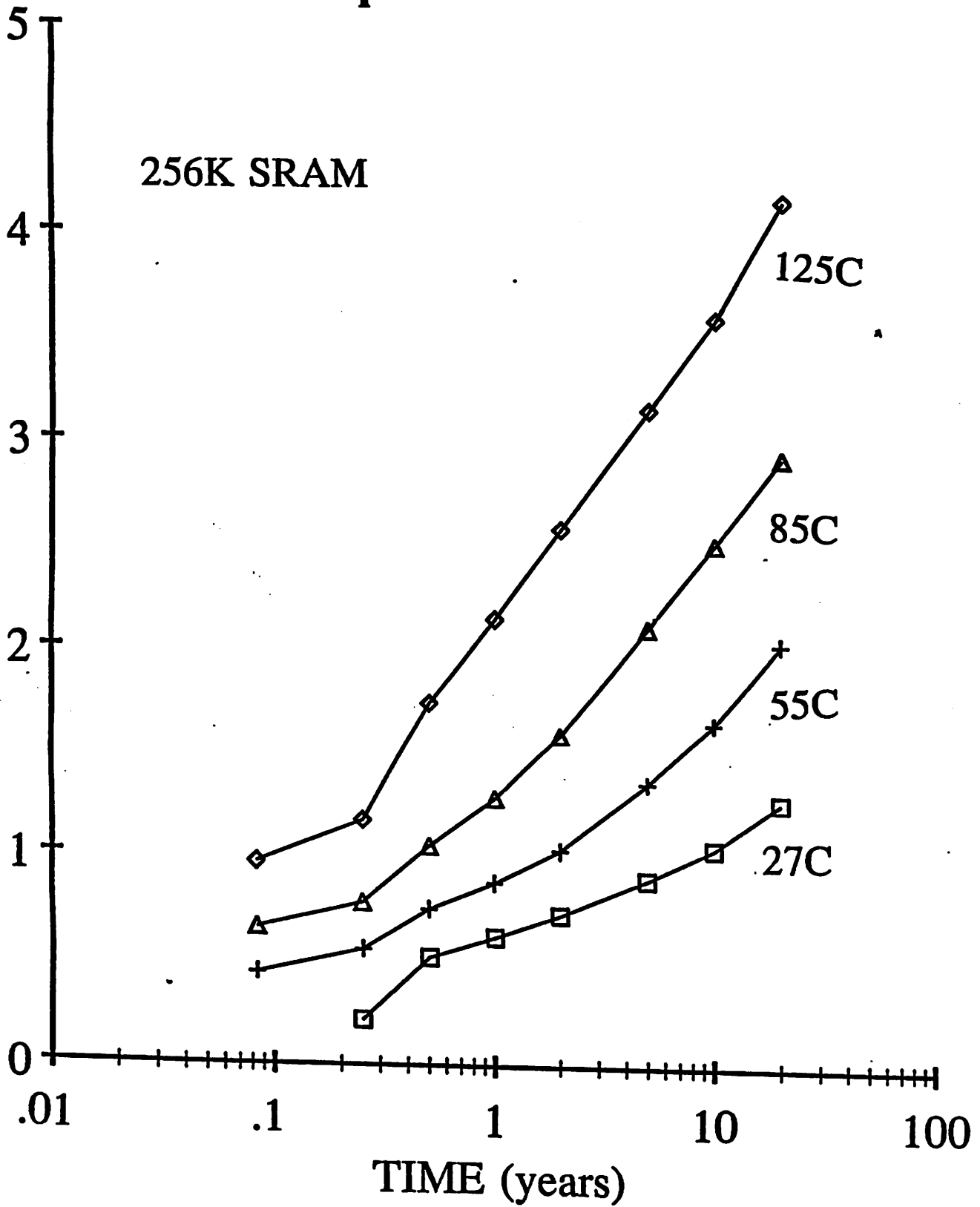
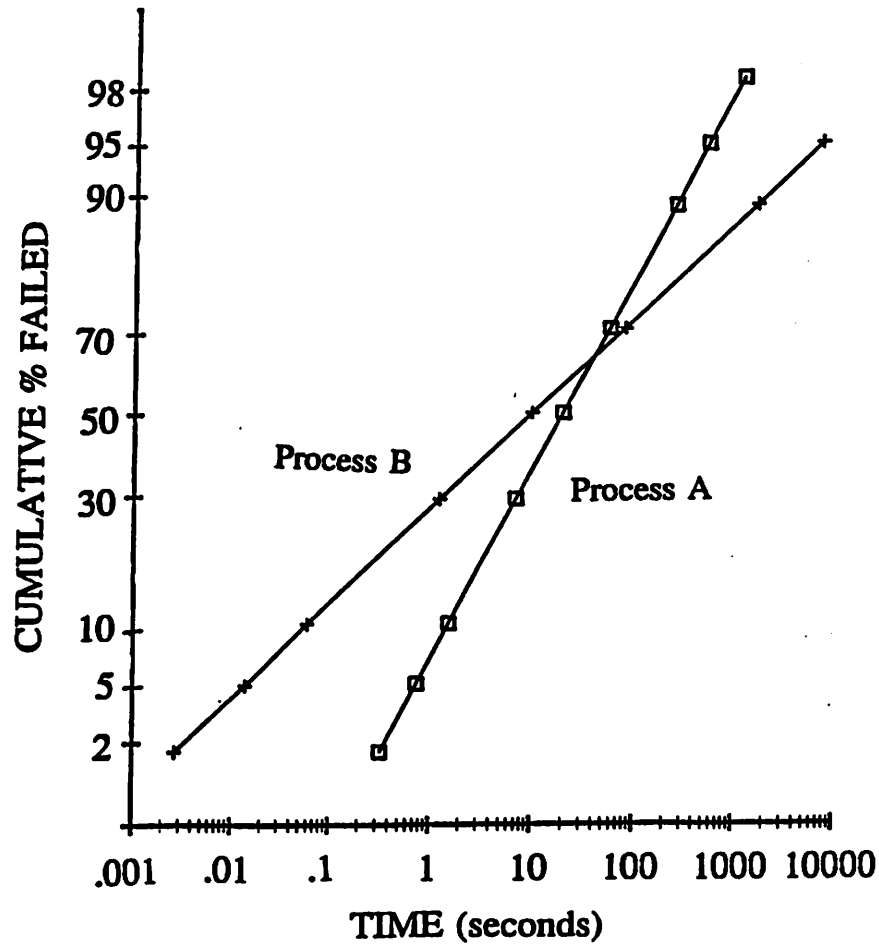


Figure A.3

Effect of Oxide Quality on Lifetime

test capacitor breakdown data (hypothetical)



CORS simulation

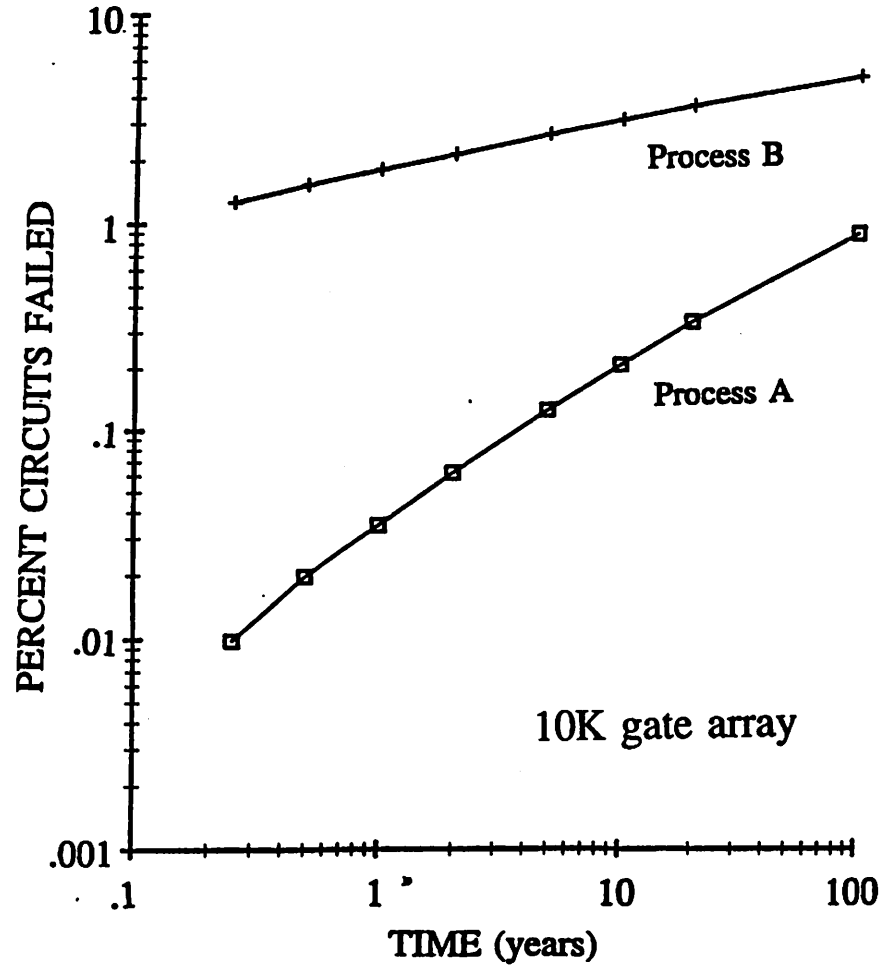


Figure A.4

Effect of Device Edge Defects

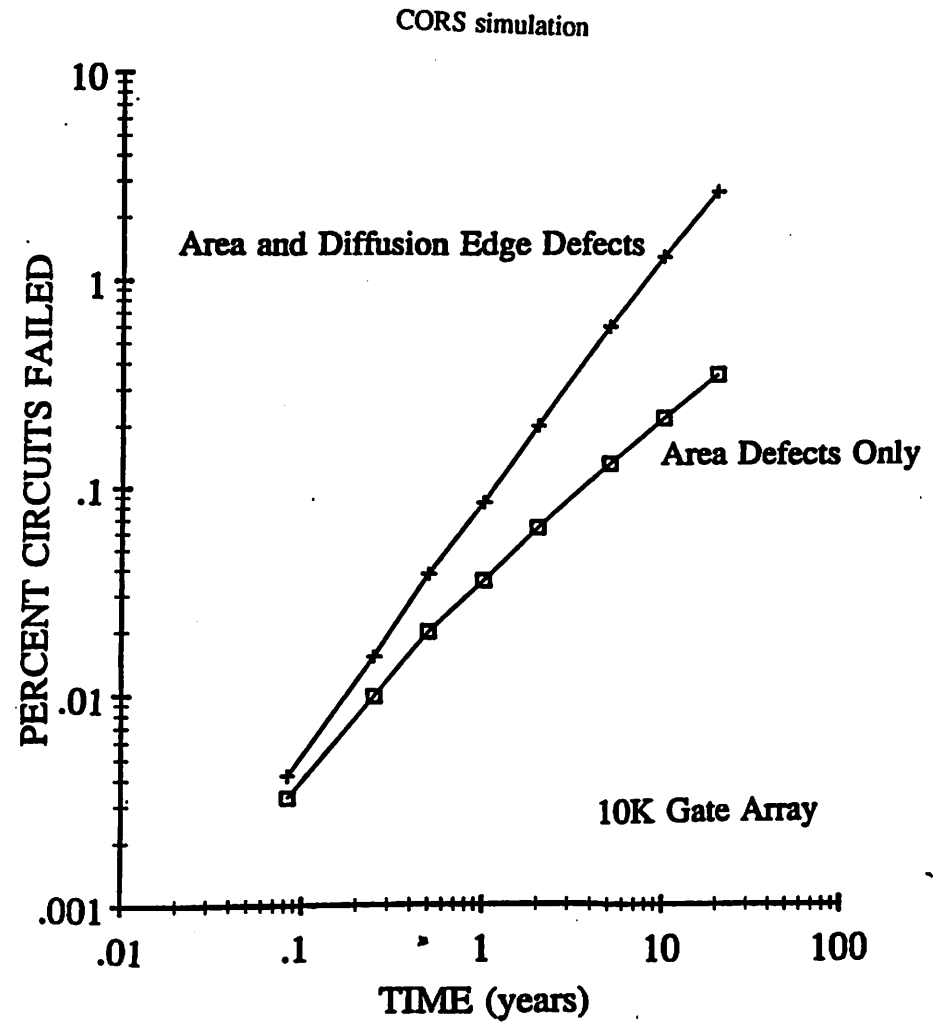
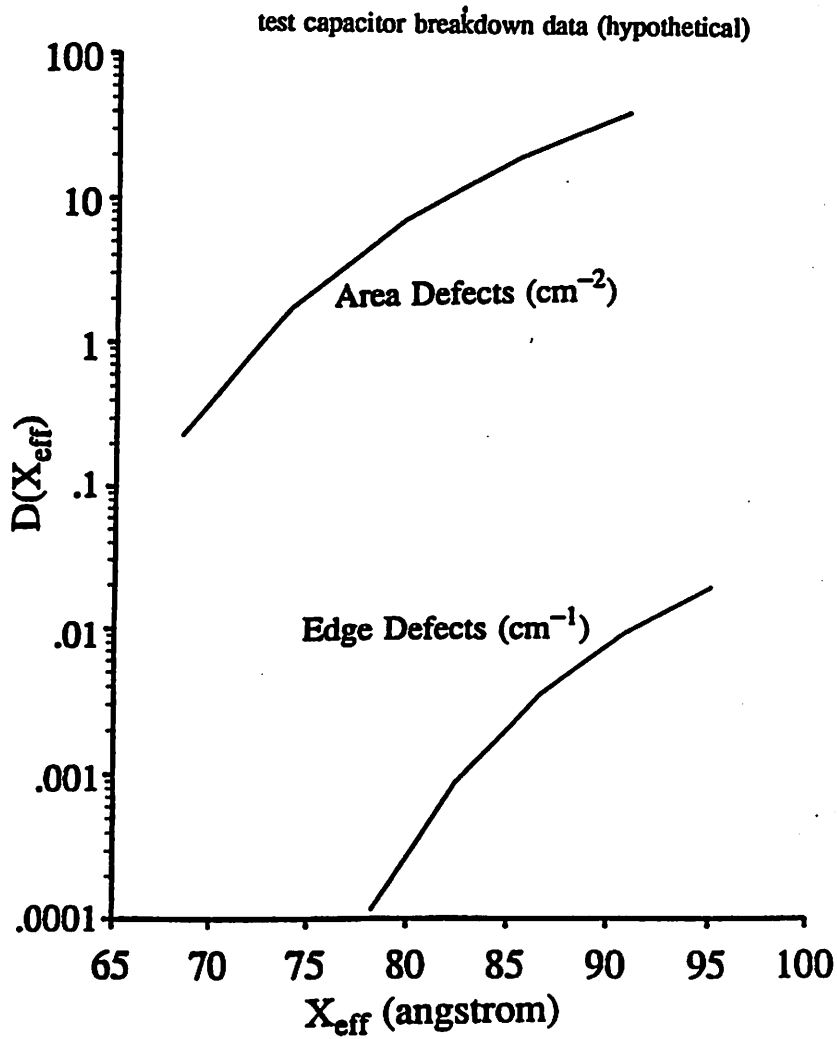


Figure A.5