Copyright © 1990, by the author(s).
All rights reserved.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission.

PLASMA IMMERSION ION IMPLANTATION FOR VLSI FABRICATION

by

X. Y. Qian, N. W. Cheung, and M. A. Lieberman

Memorandum No. UCB/ERL M90/84

13 September 1990

PLASMA IMMERSION ION IMPLANTATION FOR VLSI FABRICATION

by

X. Y. Qian, N. W. Cheung, and M. A. Lieberman

Memorandum No. UCB/ERL M90/84

13 September 1990

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

TITLE PAGE

PLASMA IMMERSION ION IMPLANTATION FOR VLSI FABRICATION

by

X. Y. Qian, N. W. Cheung, and M. A. Lieberman

Memorandum No. UCB/ERL M90/84

13 September 1990

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

PLASMA IMMERSION ION IMPLANTATION

FOR VLSI FABRICATION:

1. APPARATUS
2. SUB-100 nm P+/N JUNCTION FORMATION
3. CONFORMAL IMPLANTATION FOR TRENCH DOPING
4. PALLADIUM SEEDING FOR ELECTROLESS Cu PLATING

Presented at the VIII International Conference on Ion Implantation Technology, July 31 – August 3, 1990, University of Surrey, United Kingdom

A PLASMA IMMERSION ION IMPLANTATION REACTOR FOR ULSI FABRICATION

X. Y. Qian, D. Carl, J. Benasso, N. W. Cheung and M. A. Lieberman,

Plasma Assisted Materials Processing Laboratory,

Department of Electrical Engineering and Computer Sciences,

University of California, Berkeley, CA 94720, USA

I. G. Brown, J. E. Galvin and R. A. MacGill,

Lawrence Berkeley Laboratory, University of California,

Berkeley, CA 94720, USA

M. I. Current,

Applied Materials Inc., Implant Division: MS0907,

3050 Bowers Avenue, Santa Clara, CA 95054, USA

ABSTRACT

A Plasma Immersion Ion Implantation reactor compatible with integrated circuit fabrication has been developed. Using this system, metallic impurity gettering with a noble gas plasma, sub-100nm P+/N junction formation with SiF_4 plasma for preamorphization and BF_3 plasma for doping, trench conformal P+ doping, and Pd ion seeding implantation for selective Cu electroless plating were successfully carried out.

The PIII system consists of an electron cyclotron resonance plasma source, a processing chamber with wafer bias supply, a sputtering target with bias supply, gas handling and plasma diagnostic tools. The apparatus will be described in this paper. Plasma characterization and reactor performance will also be presented.

1. INTRODUCTION

Plasma Immersion Ion Implantation (PIII) has been used to implant nitrogen and metallic impurities into the surfaces of machine parts to improve corrosion and wear resistance [1,2]. PIII possesses several desirable characteristics such as large dose rate (up to tens mA/cm^2), large implant area, and a wide range of implantation energy (eV to 100 keV). PIII is also capable of implanting target with irregular shapes, and allows for rapid changing or combination of various ion species and adjustment of beam angular distribution by varying the gas pressure. These properties make PIII very attractive for fabricating ultra-large scale integration (ULSI) device structures.

A prototype PIII reactor dedicated to integrated circuit processing has been developed at the University of California. This system has successfully demonstrated metallic impurity gettering with noble gas implantation [3,4], sub-100nm P+/N junction formation with SiF_4 plasma for preamorphization and BF_3 plasma for P+ doping [5], trench conformal doping with BF_3 plasma [6], and seeding layer implantation using Pd ions sputtered from a solid target for selective Cu electroless plating [7].

2. REACTOR DESCRIPTION AND ION DENSITY MEASUREMENT

Figure 1 shows a schematic of the prototype PIII reactor. The system consists of five subsystems: 1) a 2.45 GHz microwave power supply with power adjustable from 0 to 800 W and a matching network; 2) an electron cyclotron resonance (ECR) plasma source; 3) a processing chamber with wafer holder and bias supply; 4) gas handling units; and 5) plasma diagnostic tools. Both the ECR chamber and the processing chamber were fabricated with aluminum. The inner diameter of ECR chamber was 7.6 cm. To compensate for plasma heating, the source chamber was constructed with a cooling water jacket. Microwave from the power supply was transmitted via WR284 rectangular waveguide into the ECR chamber through a quartz window. The reactor was pumped to a base pressure of 10^{-7} Torr before the working gas was introduced. The gas pressure in the ECR chamber could be controlled in the 0.1 mTorr to 10 mTorr range with a pressure controller. An ECR zone was generated at the center of the source chamber by an applied magnetic field of 875 Gauss with a mirror field configuration. The plasma density was adjusted by varying the microwave power. The processing chamber could accommodate three different wafer holders designed for 2 inch and 4 inch wafers and irregular slices. The wafer holders were made of Al blocks for heat absorption; no special wafer cooling was used. The wafer holder could be biased with a negative pulsed high voltage (pulsed mode) or a negative DC voltage (DC mode), as discussed later.

Langmuir probe measurements using Laframboise's analysis [8] were carried out to evaluate the ion density in the reactor. It was found that the ion density was a sensitive function of microwave power, magnetic field strength, gas pressure and species, probing position and

microwave tuning condition. For a full-power Ar plasma, a density of $10^{12}/cm^3$ in the ECR chamber near the resonance zone and $10^{11}/cm^3$ at the centerline of the processing chamber near the wafer can be achieved. Figure 2(a) shows the ion density dependence near the wafer versus forward microwave power for a BF_3 plasma. The magnet coil current was set at 125 A, and the Langmuir probe was 3.2 cm from the centerline at the plane where wafer sits during normal implantation. The measured ion density increased linearly with microwave power, and no saturation was observed. This behabior has been observed from other similar systems with different gases [9, 10]. Figure 2(b) shows the ion density dependence versus BF_3 pressure for a forward microwave power of 490 W. The measurements were taken at the same position as for Figure 2(a). The ion density increased rapidly with pressure from 0.1 mTorr to 1 mTorr. However, beyond a critical pressure around 1 mTorr, the ion density dropped as pressure increased, most probably due to ambipolar ion diffusion (to the chamber wall) at high pressures.

3. SYSTEM PERFORMANCE

A. Pulsed Mode

A negative high voltage pulser using an LC pulse line and a high-voltage step-up pulse transformer was connected to the wafer holder to supply the bias voltage for implantation. The pulse width was approximately 1 microsecond, and the pulse repetition frequency was adjustable up to 1 kHz. Shown in Figure 3(a) is a schematic of the monitoring circuit. The applied voltage was measured with an oscilloscope through a 1000:1 high voltage probe. The charge flow per pulse, including ions and secondary electrons, was measured with an integrator connected to a

1 Ampere-to-1 Volt current transformer (Rogowski loop). Since the input voltage to the integrator, V_i, was much larger than its output, V_Q, the charge flow, Q, per pulse through the wafer holder was equal to RCV_Q, or 2.2×10^{-4} V_Q. Thus the dose rate per pulse (in C/cm^2) was 2.75×10^{13} V_Q (in Volts) for a 50 cm^2 wafer holder surface area. The total dose was later calibrated against the number of pulses. Shown in Figure 3(b) are typical voltage pulse and implantation charge pulse measured with this circuit for a BF_3 plasma powered at 250 W. The measured total charge per pulse was 1.9 μC, or a dose rate per pulse of 2.34×10^{11}/cm^2 with a -6.4 kV wafer bias.

Figure 4(a) shows the dose rate dependence on the forward microwave power with various applied bias for a BF_3 plasma. The pressure was set at 1 mTorr and the magnet coil current was 125 A. The abrupt change in dose rate between 200 W and 300 W was due to a plasma mode switch. Very similar results were obtained for an Ar plasma as shown in Figure 4(b).

B. DC Mode

As an alternative means of wafer biasing, a DC negative voltage can be directly applied to the wafer holder as shown in the inset of Figure 5. The bias voltage was measured with a digital voltmeter through a 1000:1 high voltage probe. The dose rate was monitored by a mA meter serially connected in the circuit. In this configuration, an extremely high dose rate can be achieved. For example, the current density was 6.1 mA/cm^2 for a -2 kV bias at a microwave power of 650 W, corresponding to a dose rate of 3.8×10^{16}/cm^2·sec. This high dose rate capability is very attractive for some applications in ULSI processing such as backside impurity gettering.

When precise dose control is needed or wafer heating has to be minimized, a lower dose rate can be used by reducing the microwave power.

4. CONCLUSIONS

A Plasma Immersion Ion Implantation (PIII) reactor suitable for integrated circuit fabrication has been developed. The ion density can reach $10^{12}/cm^3$ in the ECR chamber and $10^{11}/cm^3$ in the processing chamber. The dose rate can be varied up to $5\times10^{11}/cm^2$ per pulse for a -6 kV bias or as high as $3.8\times10^{16}/cm^2\cdot sec.$ for a -2 kV DC bias. The bias potential can be adjusted from zero to -70 kV.

This work was supported by Applied Materials, Inc. and a grant from the California State MICRO program.

REFERENCES

[1] J. R. Conrad, J. L. Radtke, R. A. Dodd, F. J. Worzala and N. C. Tran, *J. Appl. Phys.* **62**, 4591, (1987).

[2] J. Tendys, I. J. Donnelly, M. J. Kenny and J. T. A. Pollock, *Appl. Phys. Lett.* **53** (22), 2143, (1988).

[3] H. Wong, X. Y. Qian, D. Carl, N. W. Cheung, M. A. Lieberman, I. G. Brown and K. M. Yu, MRS Proceedings, **147**, PP91-96 (1989).

[4] X. Y. Qian, H. Wong, D. Carl, N. W. Cheung, M. A. Lieberman, I. G. Brown and K. M. Yu, presented in Electrochemical Society 1989 Fall Meeting and to be published in the proceedings.

[5] X. Y. Qian, N. W. Cheung, M. A. Lieberman, M. I. Current, P. K. Chu, W. L. Harrington, C. W. Magee and E. M. Botnick, to be published in the VIII International Conference on Ion Implantation Technology, July 31 - Aug. 3, 1990, Univ. of Surrey, UK.

[6] X. Y. Qian, N. W. Cheung, M. A. Lieberman, R. Brennen, M. I. Current and N. Jha, to be published in the VIII International Conference on Ion Implantation Technology, July 31 - Aug. 3, 1990, Univ. of Surrey, UK.

[7] X. Y. Qian, M. H. Kiang, J. Huang, D. Carl, N. W. Cheung, M. A. Lieberman, I. G. Brown, K. M. Yu and M. I. Current, to be published in the VIII International Conference on Ion Implantation Technology, July 31 - Aug. 3, 1990, Univ. of Surrey, UK.

[8] J. G. Laframboise, Inst. for Aero. Stud., Univ. of Toronto, Rep. No. 100 (1966).

[9] J. Forster and W. Holber, *J. Vac. Tech.* A, **7** (3), 899 (1989).

[10] D. A. Carl, D. W. Hess and M. A. Lieberman, *J. Vac. Sci. Tech.* A, **8** (3), 2924 (1990).

FIGURE CAPTIONS

Fig.1 Schematic of Plasma Immersion Ion Implantation apparatus.

Fig.2 (a) Ion density dependence on forward microwave power for p = 0.1 mTorr, 1 mTorr and 10 mTorr BF_3 plasma. (b) ion density dependence on BF_3 pressure with 490 W forward microwave power. In both cases, the magnet coil current was 125 A. The Langmuir probe

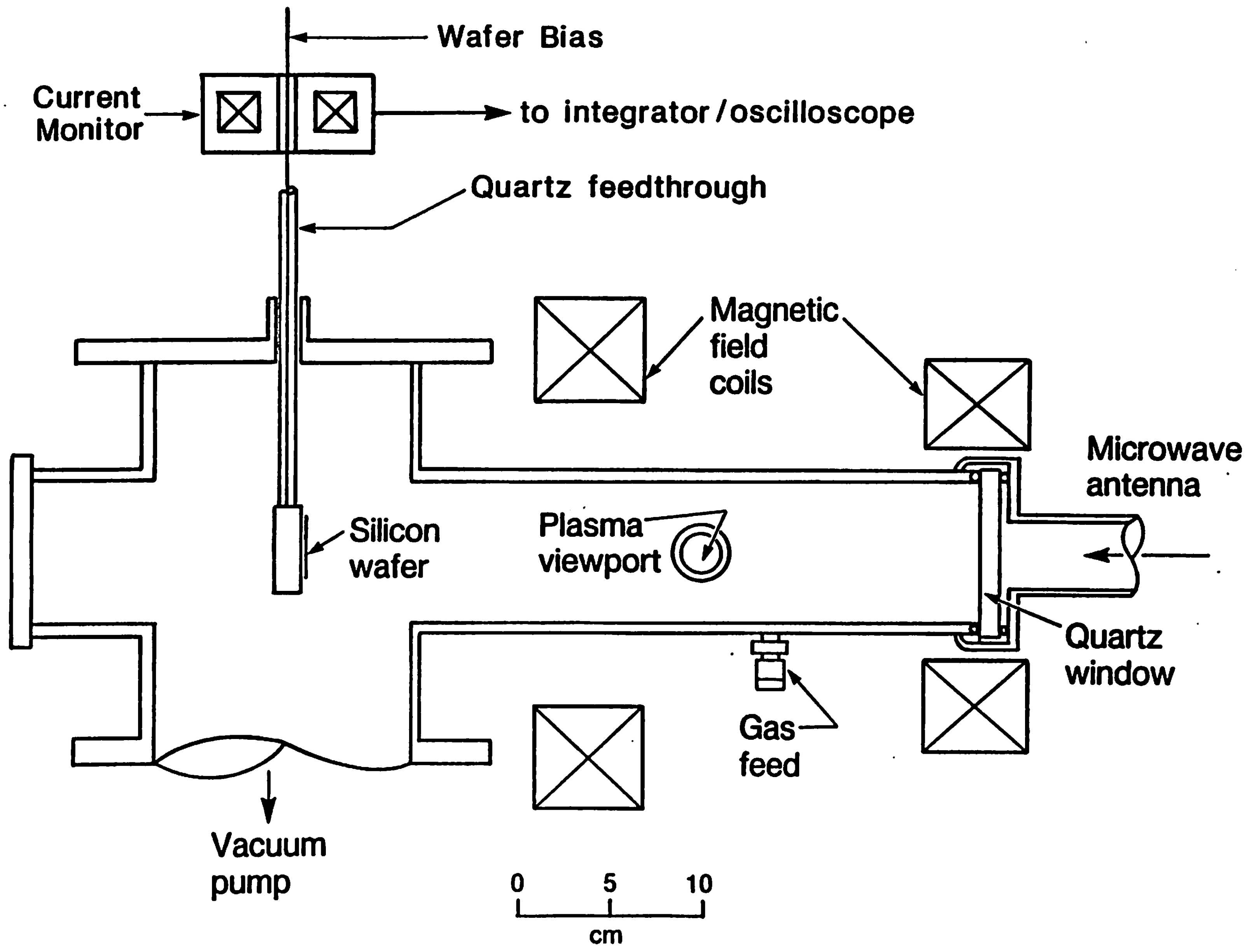
was 3.2 cm from the centerline at the plane where the wafer sits during normal implantation. BF_2^+ ions were assumed for the ion density calculation.

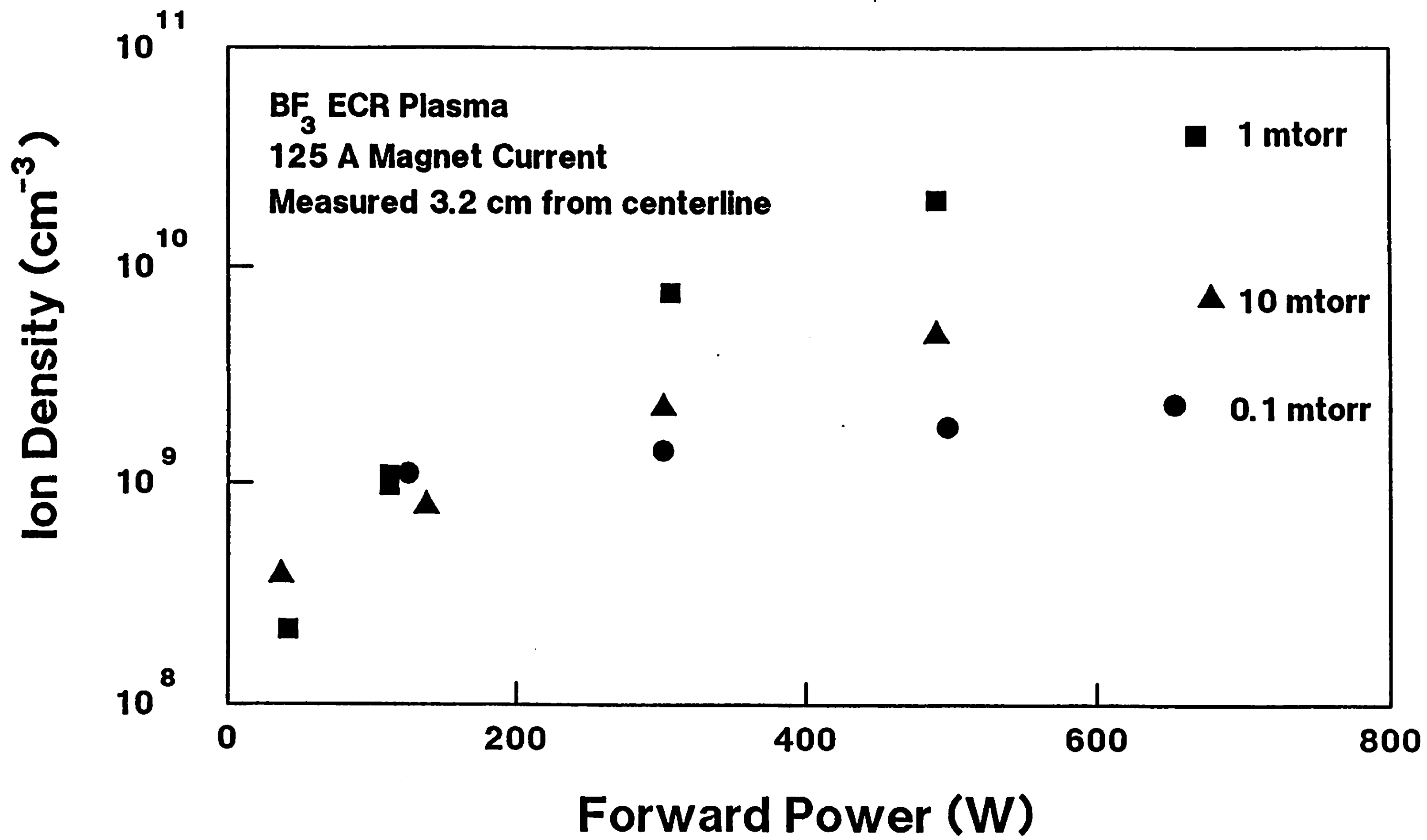
Fig.3 (a) Monitoring circuit of the pulsed mode. The applied voltage was measured with an oscilloscope through a 1000:1 high voltage probe. The charge flow per pulse was measured with an integrator connected to a 1 Ampere-to-1 Volt Rogowski loop.

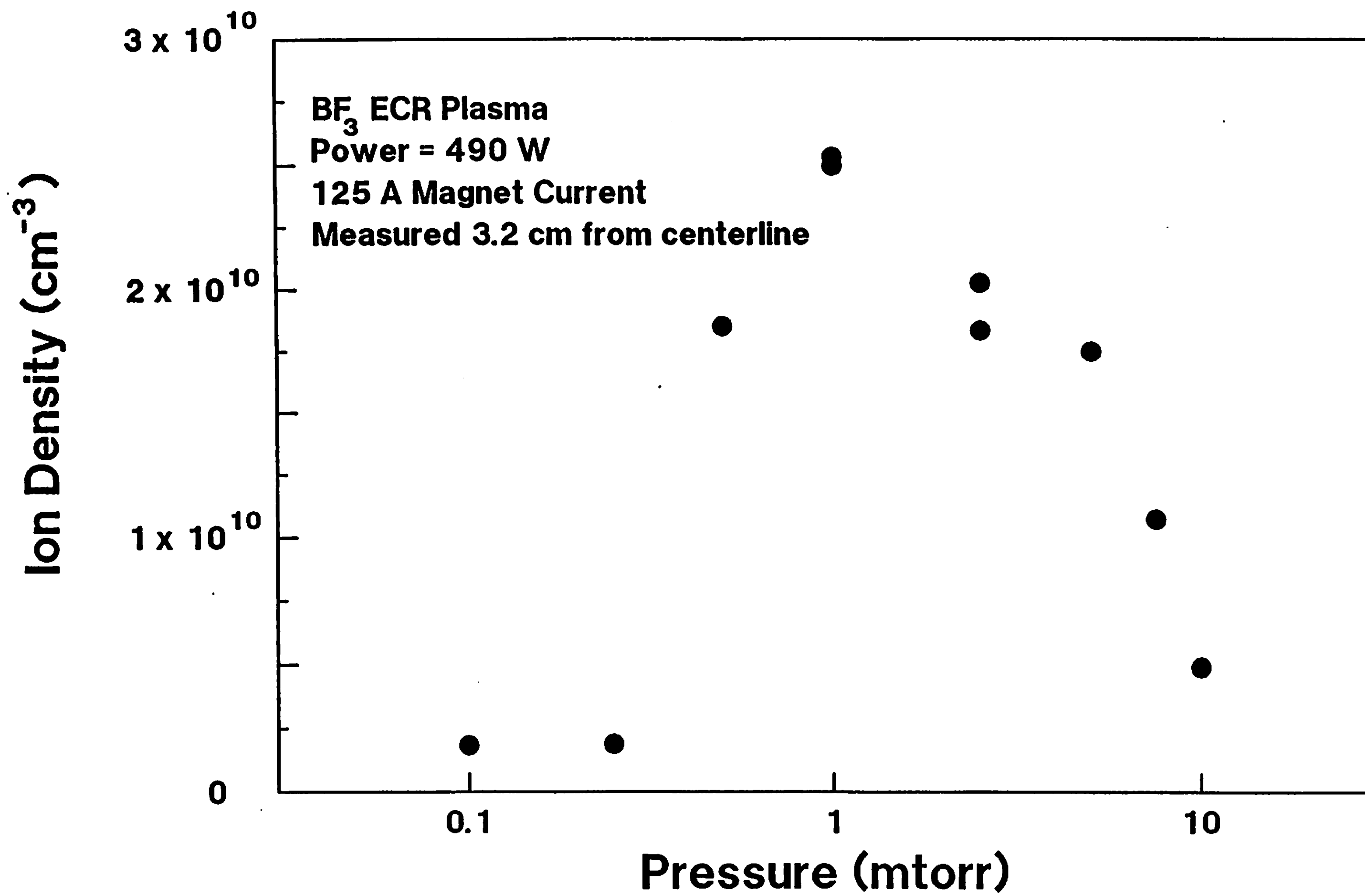
(b) A typical voltage pulse and implantation charge pulse measured with the circuit shown in (a).

Fig.4 Dose rate dependence on forward microwave power with wafer biases at -2 kV, -4 kV and -6 kV for a BF_3 plasma (a) and Ar plasma (b). The pressure was set at 1 mTorr and magnet coil current at 125 A.

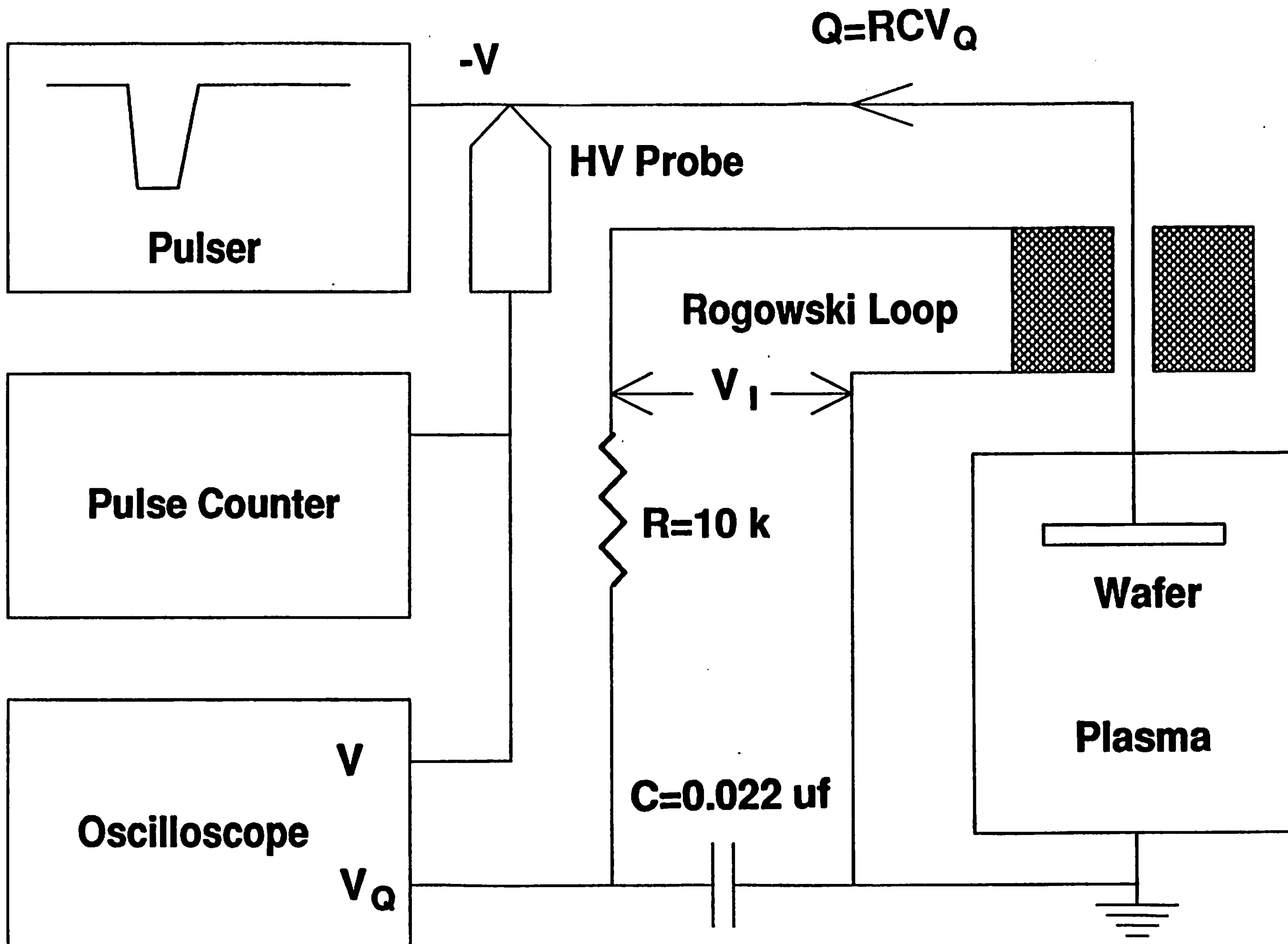
Fig.5 Implantation current density dependence on forward microwave power with BF_3 plasma in DC mode. The bias voltage was measured with a digital voltmeter through a 1000:1 high voltage probe. The dose rate was monitored by a mA meter serially connected in the circuit as shown in the inset.

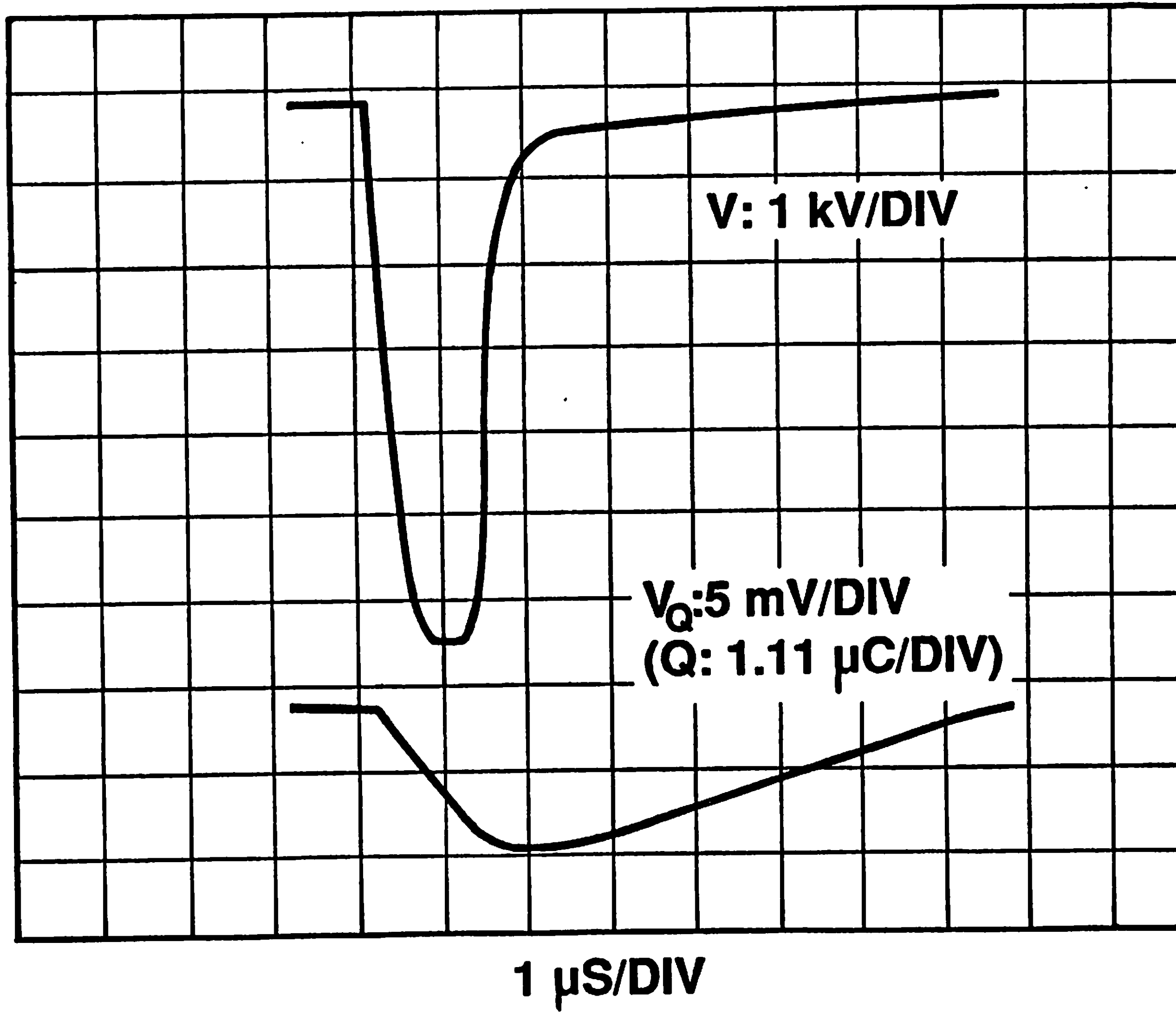

Wafer Bias
Current Monitor
to integrator/oscilloscope
Quartz feedthrough
Magnetic field coils
Microwave antenna
Silicon wafer
Plasma viewport
Quartz window
Gas feed
Vacuum pump
0
5
10
cm

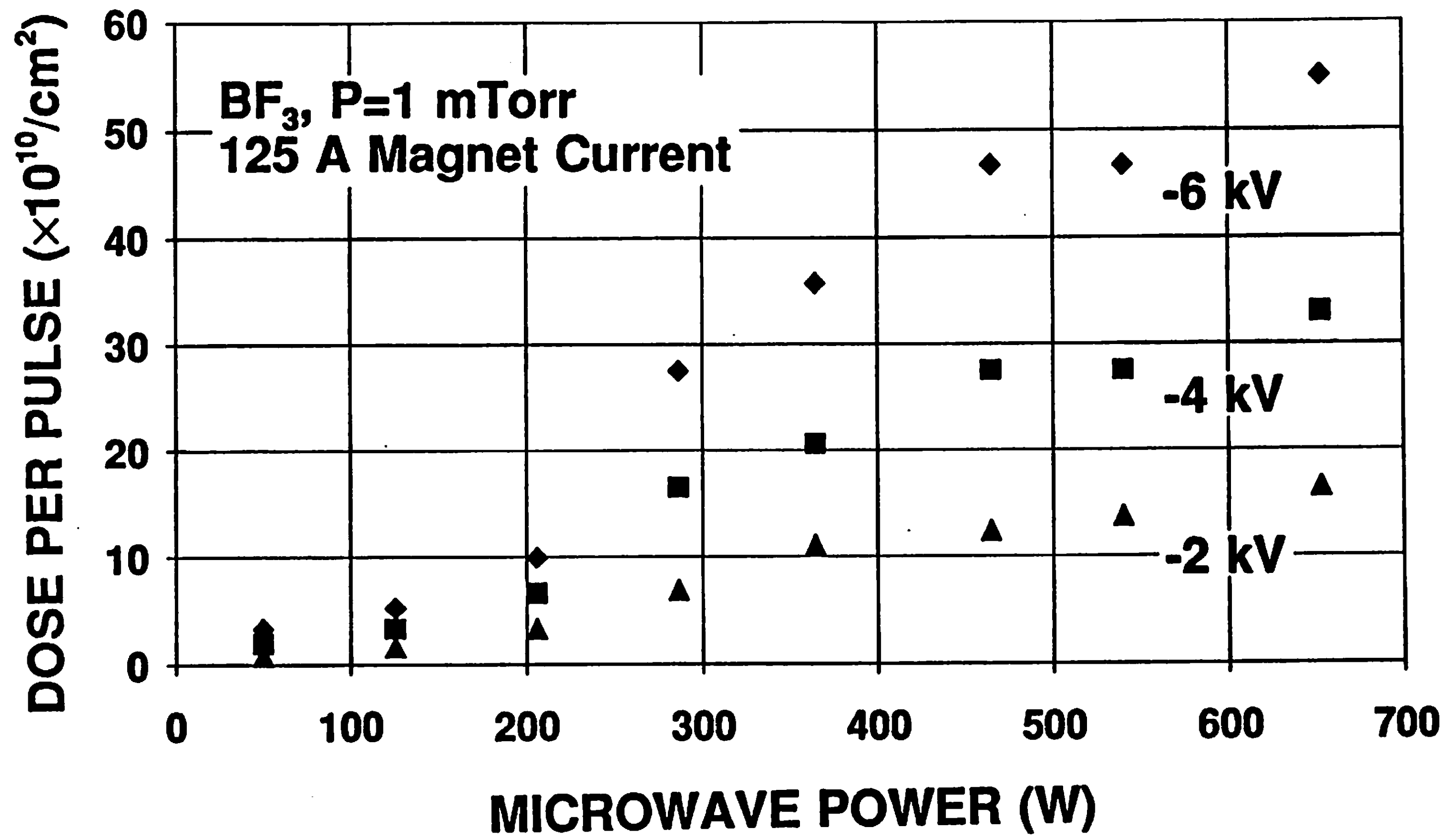

BF3 ECR Plasma
125 A Magnet Current
Measured 3.2 cm from centerline
1 mtorr
10 mtorr
0.1 mtorr
10^11
10^10
10^9
10^8
Ion Density (cm^-3)
0
200
400
600
800
Forward Power (W)



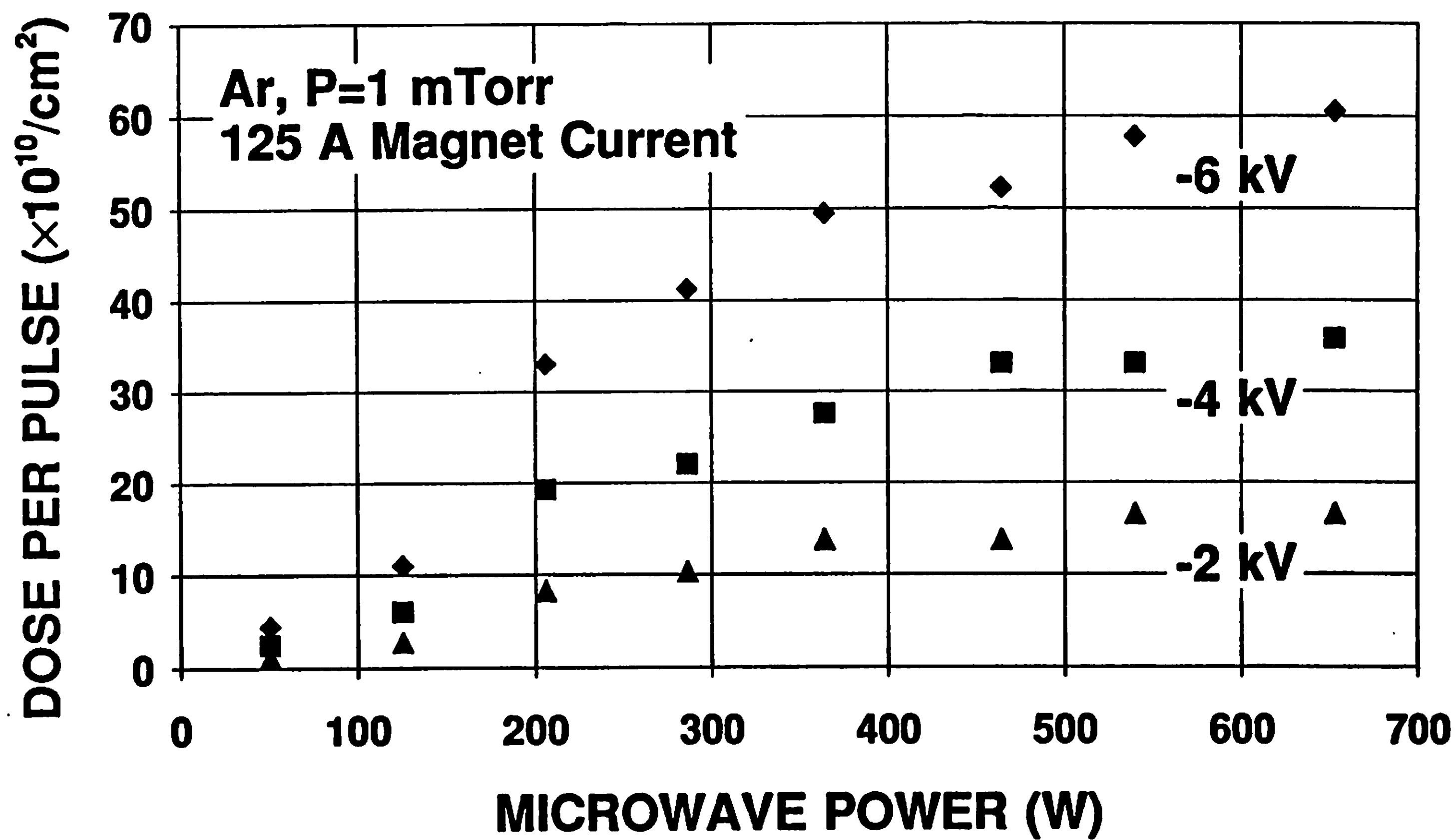
BF3 ECR Plasma
Power = 490 W
125 A Magnet Current
Measured 3.2 cm from centerline
3 x 10^10
2 x 10^10
1 x 10^10
0
0.1
1
10
Ion Density (cm^-3)
Pressure (mtorr)


Q=RCV$_Q$
-V
HV Probe
Pulser
Rogowski Loop
V$_I$
Pulse Counter
R=10 k
Wafer
Plasma
V
Oscilloscope
C=0.022 uf
V$_Q$

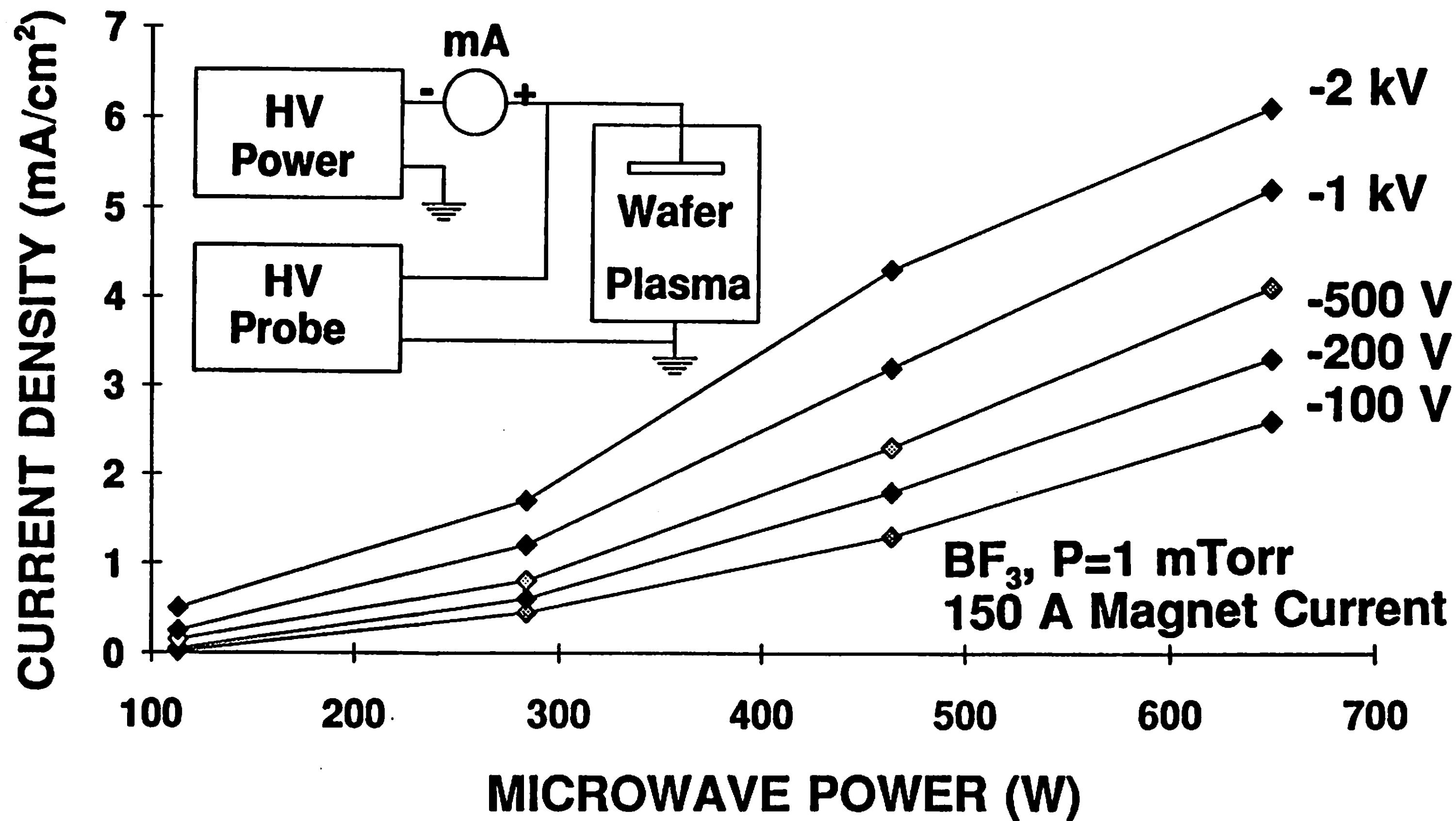

V: 1 kV/DIV
V_Q:5 mV/DIV
(Q: 1.11 μC/DIV)
1 μS/DIV



BF3, P=1 mTorr
125 A Magnet Current
-6 kV
-4 kV
-2 kV
DOSE PER PULSE (×10^10/cm^2)
MICROWAVE POWER (W)
0
10
20
30
40
50
60
0
100
200
300
400
500
600
700



Ar, P=1 mTorr
125 A Magnet Current
-6 kV
-4 kV
-2 kV
DOSE PER PULSE (×10^10/cm^2)
MICROWAVE POWER (W)
0
10
20
30
40
50
60
70
0
100
200
300
400
500
600
700


mA
HV Power
HV Probe
Wafer
Plasma
-2 kV
-1 kV
-500 V
-200 V
-100 V
BF$_3$, P=1 mTorr
150 A Magnet Current
CURRENT DENSITY (mA/cm^2)
MICROWAVE POWER (W)
0
1
2
3
4
5
6
7
100
200
300
400
500
600
700

SUB-100nm P+/N JUNCTION FORMATION USING PLASMA IMMERSION ION IMPLANTATION

X. Y. Qian, N. W. Cheung and M. A. Lieberman,

Plasma Assisted Materials Processing Laboratory,

Department of Electrical Engineering and Computer Sciences,

University of California, Berkeley, CA 94720, USA

M. I. Current,

Applied Materials, Inc., Implant Division: MS0907,

3050 Bowers Avenue, Santa Clara, CA 95054, USA

P. K. Chu,

Charles Evans & Associates, 301 Chesapeake Drive, Redwood City, CA 94063, USA

W. L. Harrington, C. W. Magee and E. M. Botnick,

Evans East, Inc., The Office Center, 666 Plainsboro Road, Suite 1236,

Plainsboro, NJ 08536, USA

ABSTRACT

Using plasma immersion ion implantation (PIII), sub-100nm p+/n junctions were fabricated with SiF_4 preamorphization followed by BF_3 doping. With this technique, the dose rate

can be as high as $10^{16}/cm^2$ per second. The silicon wafer was immersed in SiF_4 or BF_3 plasma and biased with a negative voltage. The positively charged ions were accelerated by the electric field in the plasma sheath and implanted into the wafer. The junction depth can be controlled by varying the negative voltage applied to the wafer holder and thermal annealing conditions.

1. INTRODUCTION

Extremely shallow (less than 100nm) P+/N junction formation is a key issue in the development of sub-micron CMOS technology. With conventional ion implanters, molecular ion BF_2^+ has been used as the implant species to lower the boron effective kinetic energy[1]. In order to reduce the channeling effect and to activate dopants without excessive diffusion, an implantation step to preamorphize the silicon substrate prior to BF_2^+ implantation is also required [2]. Since relatively large doses are needed for both preamorphization and doping, the overall implantation process can be time consuming.

A large dose rate ion implantation technique, plasma immersion ion implantation (PIII), has been used to implant nitrogen and other ion species into the surface of machine parts to improve wear or corrosion resistance [3-4]. Recently, a prototype plasma PIII apparatus dedicated to integrated circuit processing has been developed, and was successfully applied to implant noble gas ions into Si for metallic impurity gettering [5,6]. In this paper, we show that PIII can be used for sub-100nm P+/N junction fabrication. Both SiF_4 preamorphization and BF_3 doping were carried out in sequential steps by switching the plasma gases.

2. EXPERIMENT

Shown in Figure 1 is a schematic of p+/n junction fabrication process using the PIII technique. The silicon wafer was immersed in a SiF_4 plasma for preamorphization, then in a BF_3 plasma for doping. The wafer was biased with a DC or pulsed negative voltage. A plasma sheath around the wafer was generated by the applied negative potential. The positively charged ions were accelerated by electric field in the sheath and implanted into the wafer. The plasma was excited in an electron cyclotron resonance (ECR) discharge chamber with an 800 W, 2.45 GHz microwave power supply. The charge flow per pulse, including ions and secondary electrons, was measured with a current transformer (Rogowski loop) connected to an integrator. The total dose was later calibrated against the number of pulses. When a DC bias is used, the dose was monitored with a current meter serially connected in the circuit. For this shallow P+/N junction study, we have investigated both DC and pulsed bias methods. To avoid wafer heating and to obtain better dose control, a lower microwave power of 100 Watts was used. A detailed description of the PIII apparatus has been presented elsewhere [7].

After the PIII doping process, the Si wafer was rapid thermal annealed (RTA) to activate the boron dopant. RTA was performed in a N_2 ambient at a flow rate of 3 sccm to prevent sample surface oxidation. Sheet resistance was then measured with a four point probe, and the carrier profiles were measured using the spreading resistance (SPR) technique. Secondary ion mass spectroscopy (SIMS) was used to analyze the implant depth profiles before and after annealing.

3. RESULTS AND DISCUSSION

Experimental results of sheet resistance and junction depth dependence on dosage and bias potential are presented in Figures 2, 3 and 4. P-type CZ wafers with resistivity of 10-50 Ω-cm were used. The BF_3 gas pressure was set at 1 mTorr. A DC voltage from -500 V to -20 kV was applied as the wafer bias. After PIII, all samples were annealed for 20 seconds at various temperatures.

Figure 2 shows the sheet resistance dependence on PIII dose as charge per unit wafer area. The wafer bias was set at -5 kV for this group of samples. As shown in Figure 3, the sheet resistance decreases monotonically with the dose. As the dose was raised from 0.05 mC/cm^2 to 0.5 mC/cm^2, the sheet resistance dropped from 1050 Ω/□ to 100 Ω/□. However, the curve flattened out as the dose exceeded 4 mC/cm^2. The minimum sheet resistance obtained was 50 Ω/□ with -5 kV bias and RTA at 1060 C° for 20 seconds. From SIMS and SPR profile studies, it was found that the boron atomic concentration near the silicon surface of the samples was well above the activation limit of $2\times10^{20}/cm^2$ at 1060 °C [8]. Lower sheet resistance was achieved by annealing these samples at higher temperature or for a longer time, because a larger fraction of boron atoms was driven-in to a concentration below the activation limit. With our experimental PIII system, the standard deviation of sheet resistance across a two inch wafer was about 40% when a pulsed bias was used. In DC mode, the uniformity is poorer, especially when the bias voltage is high. A much better uniformity is expected with the recently constructed ten inch reactor in UC Berkeley.

Sheet resistance dependence on wafer bias is shown in Figure 3. At a dose of 4 mC/cm^2, sheet resistance dropped from 250 Ω/□ to 50 Ω/□ as the negative bias increased from 500 V to 5 kV. Using SIMS analysis, it was found that a large portion of boron atoms was localized near the surface region with a concentration above the activation limit for the -500 V and -2 kV samples, so that higher sheet resistances were observed in these samples. However, in higher biased samples, dopants were more evenly distributed due to the deeper penetration of the more energetic ions, which led to a higher percentage of activated boron. Further raising of the voltage did not affect the resistance much for this particular dose condition because a full activation was nearly reached.

Shown in Figure 4 is the effect of bias voltage on electrical junction depth, as defined by a junction carrier concentration of $10^{15}/cm^3$. As expected, the higher bias potential increased the implantation ion energy, which in turn resulted in a deeper junction. However, the junction depth in all samples annealed at 1060 C° for 20 seconds was much deeper than the prediction of LSS theory [9]. Moreover, extrapolation of x_j to zero bias voltage gives a value of 140nm. The apparently high x_j with a low energy implantation suggests that sub-100nm P+/N junction formation in crystalline Si substrate with above annealing condition is not feasible even when the applied bias voltage is reduced to zero.

A pair of SIMS profiles from a sample before and after annealing are presented in Figures 5(a) and 5(b). BF_3 PIII doping was performed at 3 mTorr gas pressure with a DC bias of -2 kV. The dose was 4 mC/cm^2. As shown in Figure 5(a), the boron profile peak was very close to the wafer surface. The boron concentration decreased by three orders of magnitude to $1.5\times10^{19}/cm^3$

at a depth of 30nm below the surface. However, this boron concentration was located at 130nm after a thermal annealing at 1060 °C for 20 seconds as shown in Figure 5(b). This rapid diffusion of shallow implanted boron during annealing is in agreement with observations in conventional implantation experiments [10,11]. Apparently, a shorter RTA cycle or lower annealing temperature is required for sub-100nm P+/N junction fabrication.

An interesting observation to be noted from the SIMS measurements was the fluorine depth distribution of the as-implanted samples. Due to a moderate electron temperature of 4-8 eV in ECR plasmas, most ions generated are presumably in the form of one fluorine stripped, singly charged BF_2^+. However, the total amount of fluorine measured in Figure 5(a) was much less than boron dose. The existence of a small concentration of double fluorine stripped ions and fluorine out-diffusion during PIII may be responsible. As shown in Figure 5(b), most fluorine out-diffused after RTA at 1060 °C for 20 seconds.

To check the effect of ion channeling during the PIII process, we have compared the SIMS profiles of BF_3 PIII into crystalline and amorphous CVD silicon samples. A steeper decay of the SIMS profile tail for the amorphous sample indicates that a preamorphization step will help to reduce the junction depth.

To demonstrate the feasibility of fabricating sub-100nm P+/N junction, we have used SiF_4 PIII preamorphization followed by BF_3 PIII doping. To show the real P+/N junction, N-type CZ wafers with resistivity of 8-12 Ω-cm were used in this experiment. DC wafer bias was applied for both implantation steps. The preamorphization was performed in SiF_4 plasma with a -4 kV

DC wafer bias at the gas pressure of 3 mTorr. A preamorphization dose of $3\times10^{15}/cm^2$ was obtained in about 10 seconds. The doping implantation was then performed in BF_3 plasma at a bias of -2 kV to a dose of $1.2\times10^{15}/cm^2$. The post-implantation annealing was performed at 1060 C° for 1 second. As shown in the SPR profile of Figure 6, the observed peak carrier concentration is $1\times10^{20}/cm^3$. The electrical junction depth is only 80nm and the sheet resistance is 447 Ω/□.

4. CONCLUSION

Sub-100nm p+/n junctions were fabricated with PIII. Using PIII, the dose rate can be much larger than with conventional ion implanters. The sheet resistance and junction depth can be regulated with implantation dosage, wafer bias and RTA conditions. For extremely shallow P+/N junction formation, sample preamorphization, moderate boron dose and short cycle RTA are required. With SiF_4 PIII preamorphization followed by a -2 kV BF_3 PIII at a dose of $1.2\times10^{15}/cm^2$ and RTA at 1060 °C for 1 second, 80nm P+/N junctions were successfully obtained.

This work was supported by Applied Materials, Inc. and a grant from the California State MICRO program.

REFERENCES

[1] S. N. Hong, G. A. Ruggles, J. J. Paulos, J. J. Wortman, and M. C. Ozturk, *Appl. Phys. Lett.* **53**, 1741 (1988).

[2] C. M. Lin, A. J. Steck and T. P. Chow, *Appl. Phys. Lett.*, **54**, 1790 (1989).

[3] J. R. Conrad, J. L. Radtke, R. A. Dodd, F. J. Worzala and N. C. Tran, *J. Appl. Phys.* **62**, 4591, (1987).

[4] J. Tendys, I. J. Donnelly, M. J. Kenny and J. T. A. Pollock, *Appl. Phys. Lett.* **53** (22), 2143 (1988).

[5] H. Wong, X. Y. Qian, D. Carl, N. W. Cheung, M. A. Lieberman, I. G. Brown and K. M. Yu, MRS proceeding, **147**, PP91-96 (1989).

[6] X. Y. Qian, H. Wong, D. Carl, N. W. Cheung, M. A. Lieberman, I. G. Brown and K. M.Yu, presented in ECS 1989 fall meeting and to be published in the proceedings.

[7] X. Y. Qian, D. Carl, J. Benasso, N. W. Cheung, M. A. Lieberman, I. G. Brown, J. E.Galvin, R. A. MacGill and M. I. Current, to be published in the VIII International Conference on Ion Implantation technology, July 31 - Aug. 3, 1990, Univ. of Surrey, UK.

[8] H. Ryssel, K. Muller, K. Haberger, R. Henkelmann, and F. Jahael, *Appl. Phys.*, **22**, 3 (1980).

[9] J. Lindhard, M. Scharff and H. Schiott, "Range Concepts and Heavy Ion Ranges," *Mat. Fys. Med. Dan. Vid. Selsk* **33**, No. 14, 1 (1963).

[10] T. E. Seidel, D, J. Lischner, C. S. Pai, R. V. Knoell, D. M. Maher, and D. C. Jacobson, *Nucl. Instrum. Methods, Phys. Rev.* **B7/8,** 251 (1985).

[11] R. T. Hodgson, V. R. Deline, S. Mader, and J. C. Gelpey, *Appl. Phys. Lett.*, **44**, 589 (1984).

FIGURE CAPTIONS

Fig.1 Schematic of P+/N junction fabrication process using plasma immersion ion implantation.

Fig.2 The sheet resistance dependence on BF_3 PIII dose. The wafer bias was -5 kV and RTA was performed at 1060 °C for 20 seconds for this group of samples. The minimum sheet resistance obtained was 50 Ω/□ under this condition.

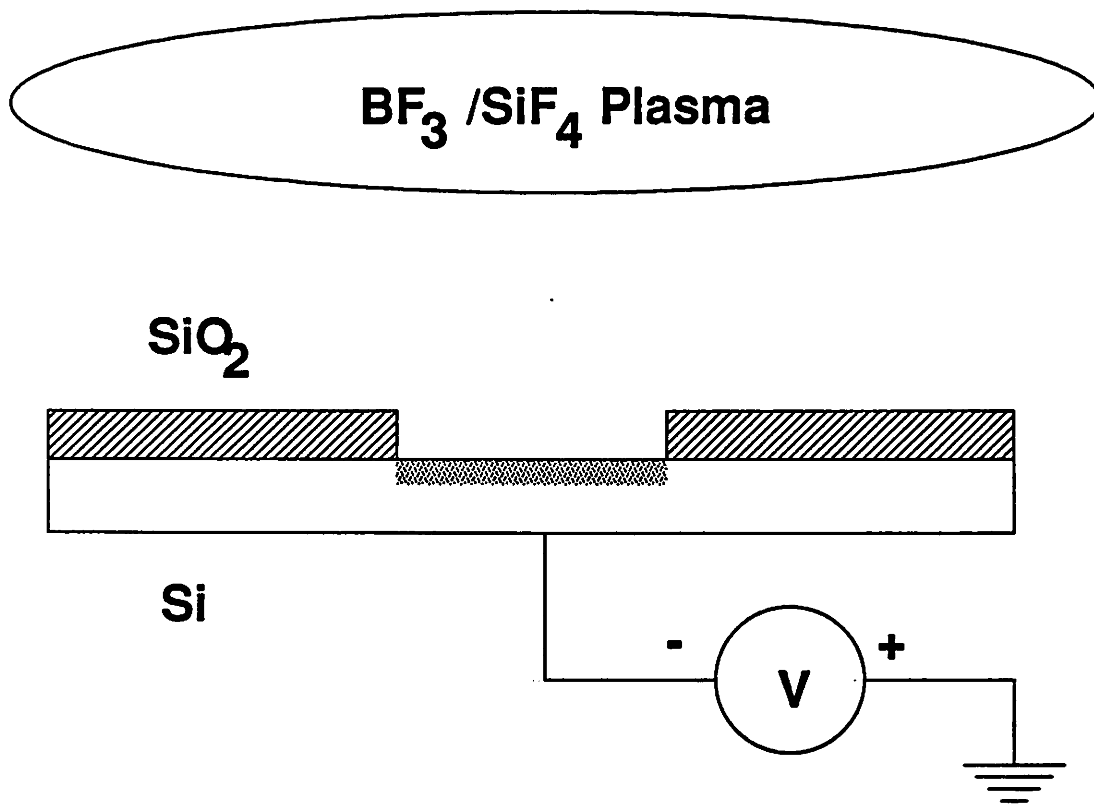
Fig.3 The sheet resistance dependence on wafer bias voltage. Samples were implanted with BF_3 PIII at a dose of 4 mC/cm^2 and annealed at 1060 °C for 20 seconds. A DC bias from -500 V to -20 kV was applied during implantation.

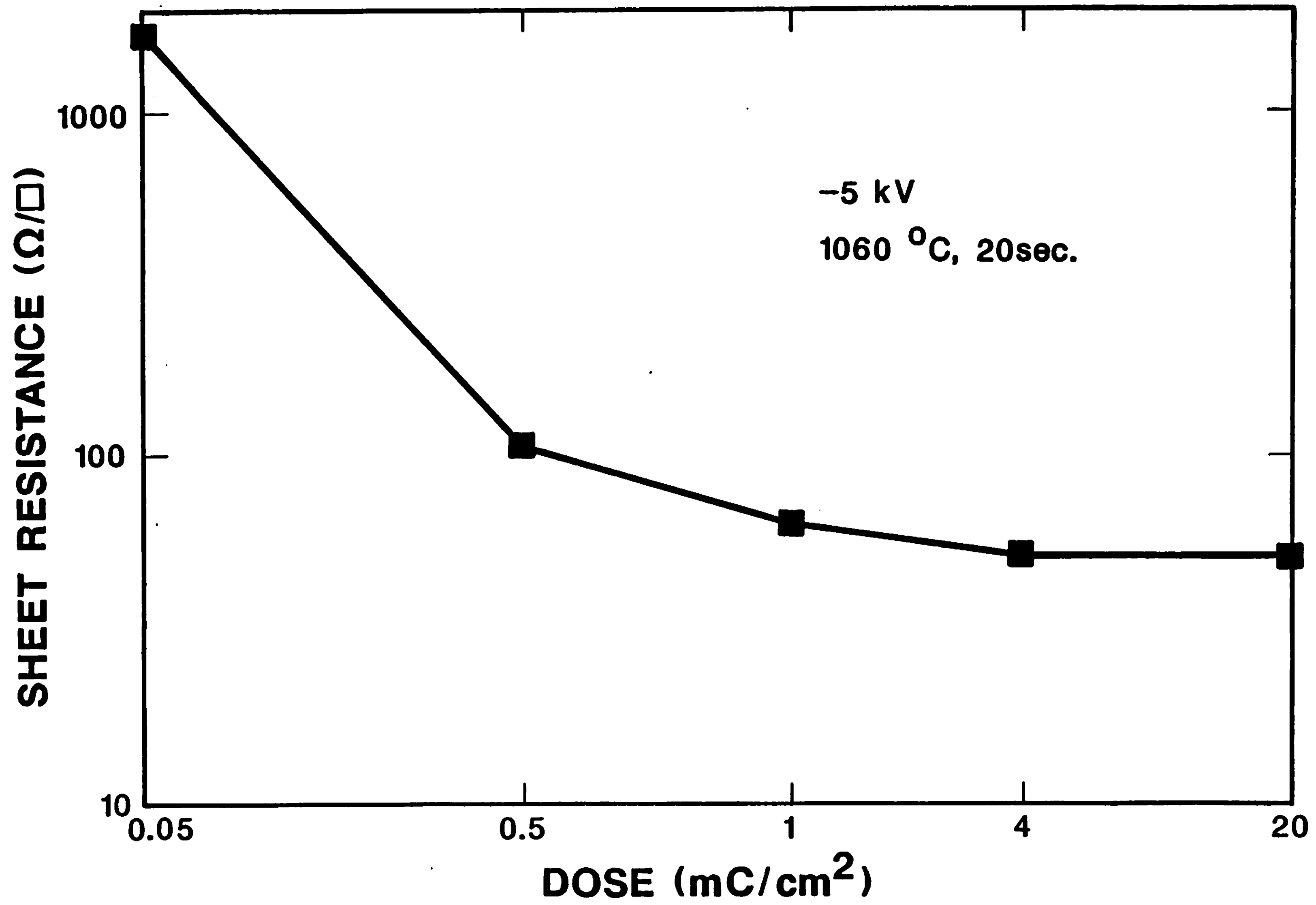
Fig.4 The electrical junction depth dependence on wafer bias. Samples were implanted with bias from -500 V to -10 kV at a fixed dosage of 4 mC/cm^2 and annealed at 1060 °C for 20 seconds.

Fig.5 SIMS profiles of BF_3 plasma immersion ion implanted Si wafers before (a) and after (b) thermal annealing. The "B" and "F" in the Figures represent boron and fluorine concentrations respectively. The doping was carried out at a -2 kV DC bias with gas pressure of 3 mTorr. The implantation dose was 4 mC/cm^2. The sample in (b) was annealed at 1060 C° for 20 seconds.

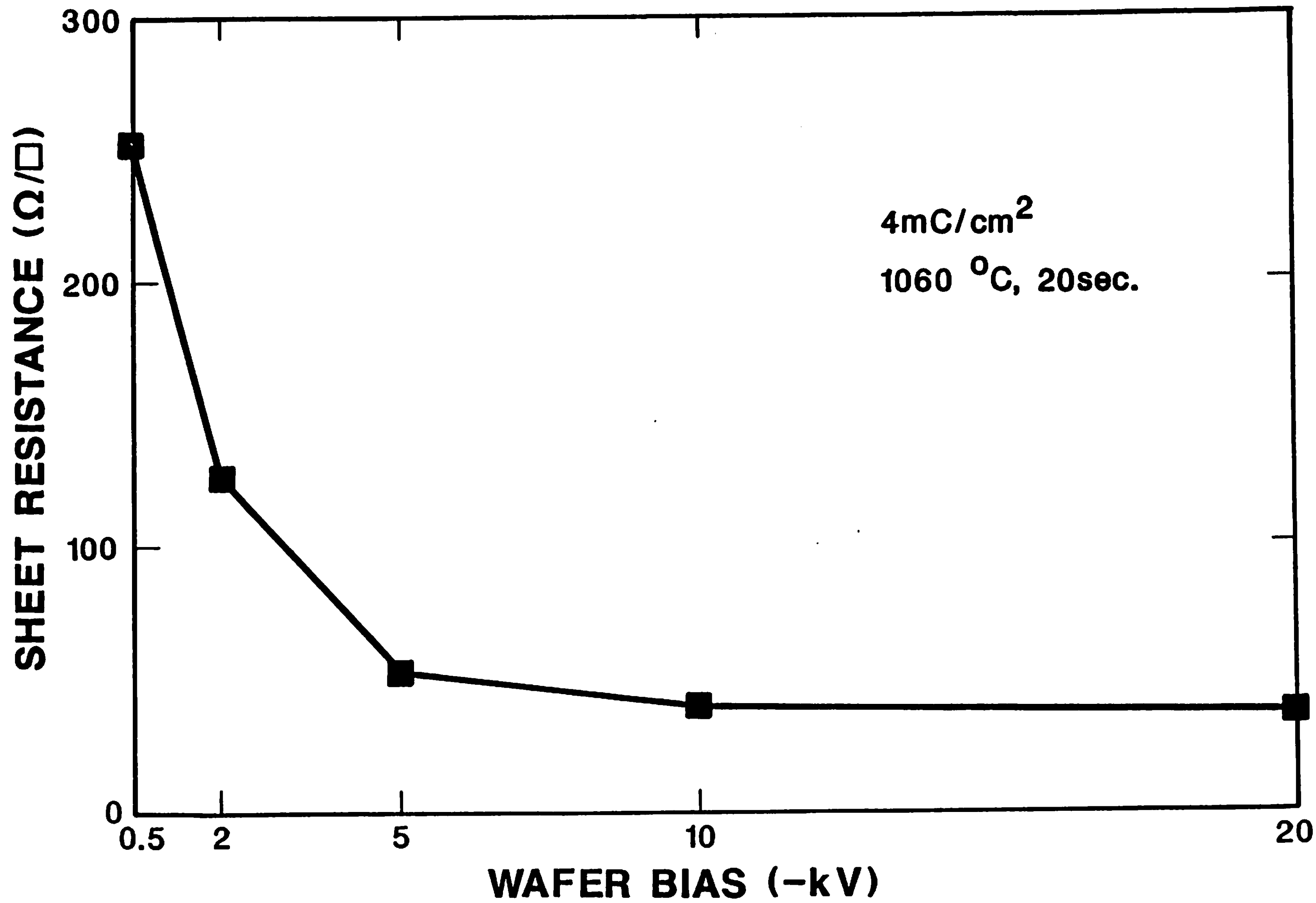
Fig.6 The SPR profile of sub-100nm P+/N junctions fabricated with PIII. The preamorphization was performed in SiF_4 plasma at -4 kV DC bias with a dose of 3×10^{15}/cm^2. The doping implantation was then performed in BF_3 plasma at -2 kV DC bias with a dose of 1.2×10^{15}/cm^2. The post-implantation annealing was performed at 1060 C° for 1 second.

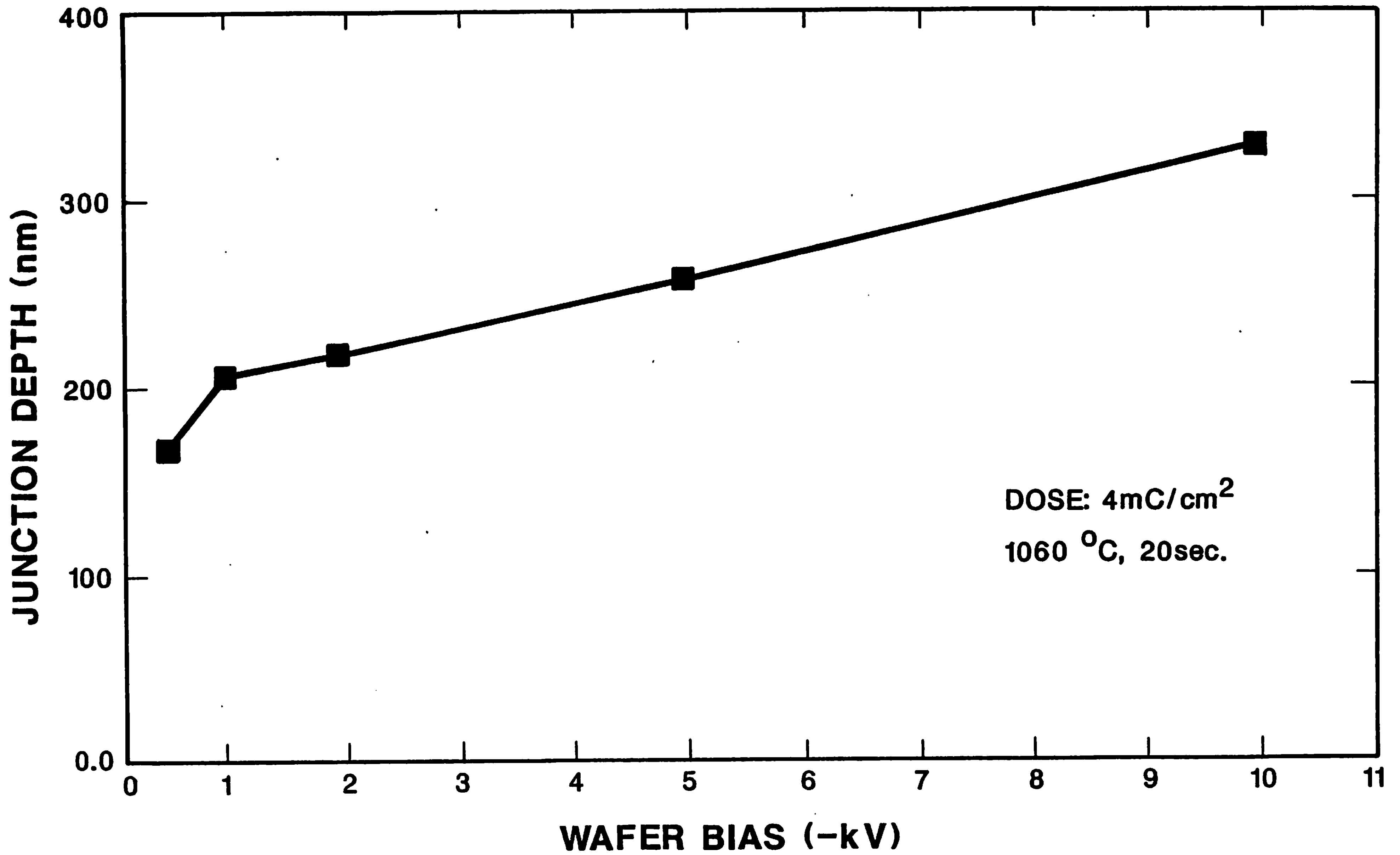
PIII Shallow P+/N Junction Fabrication Process

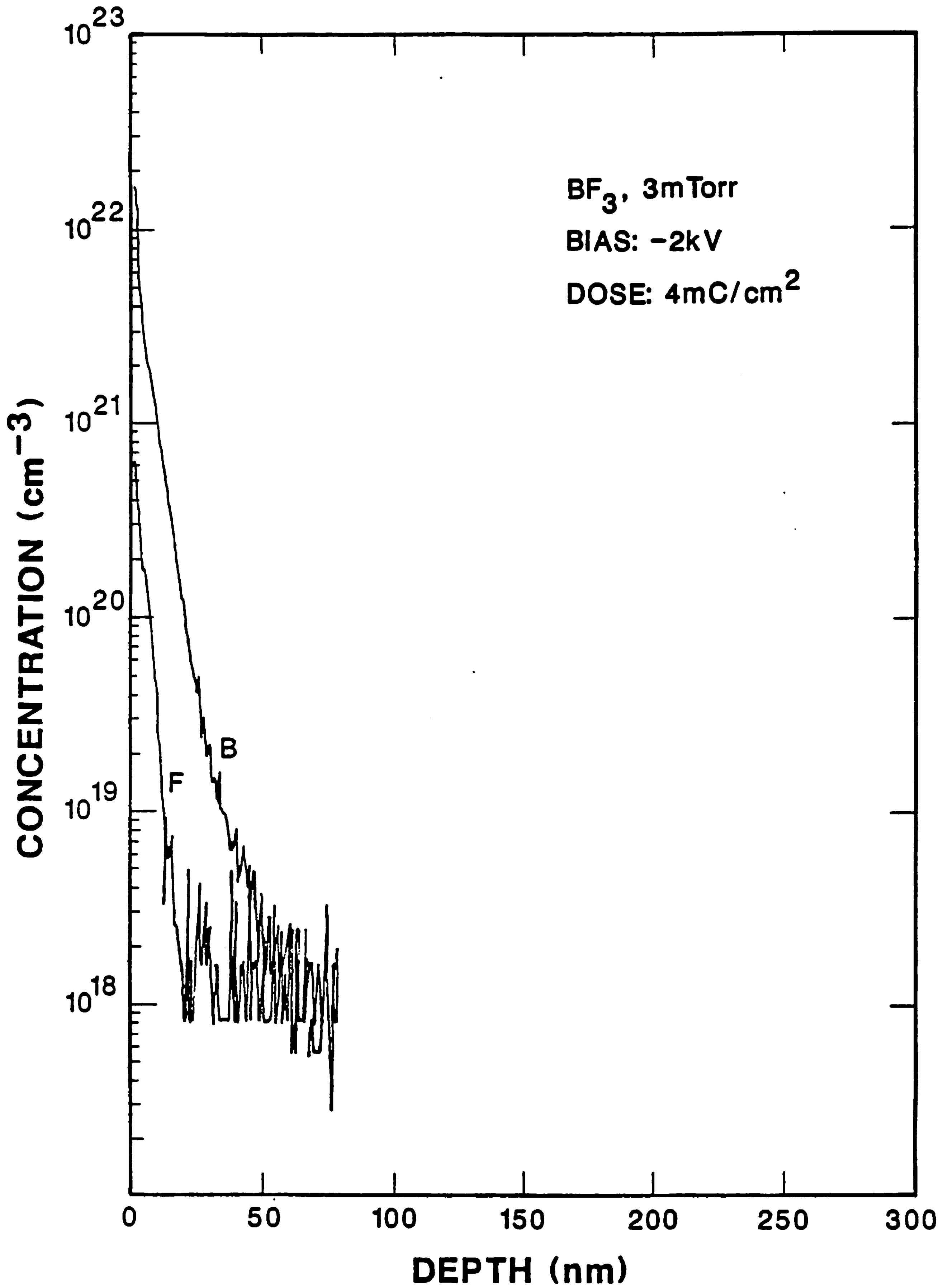




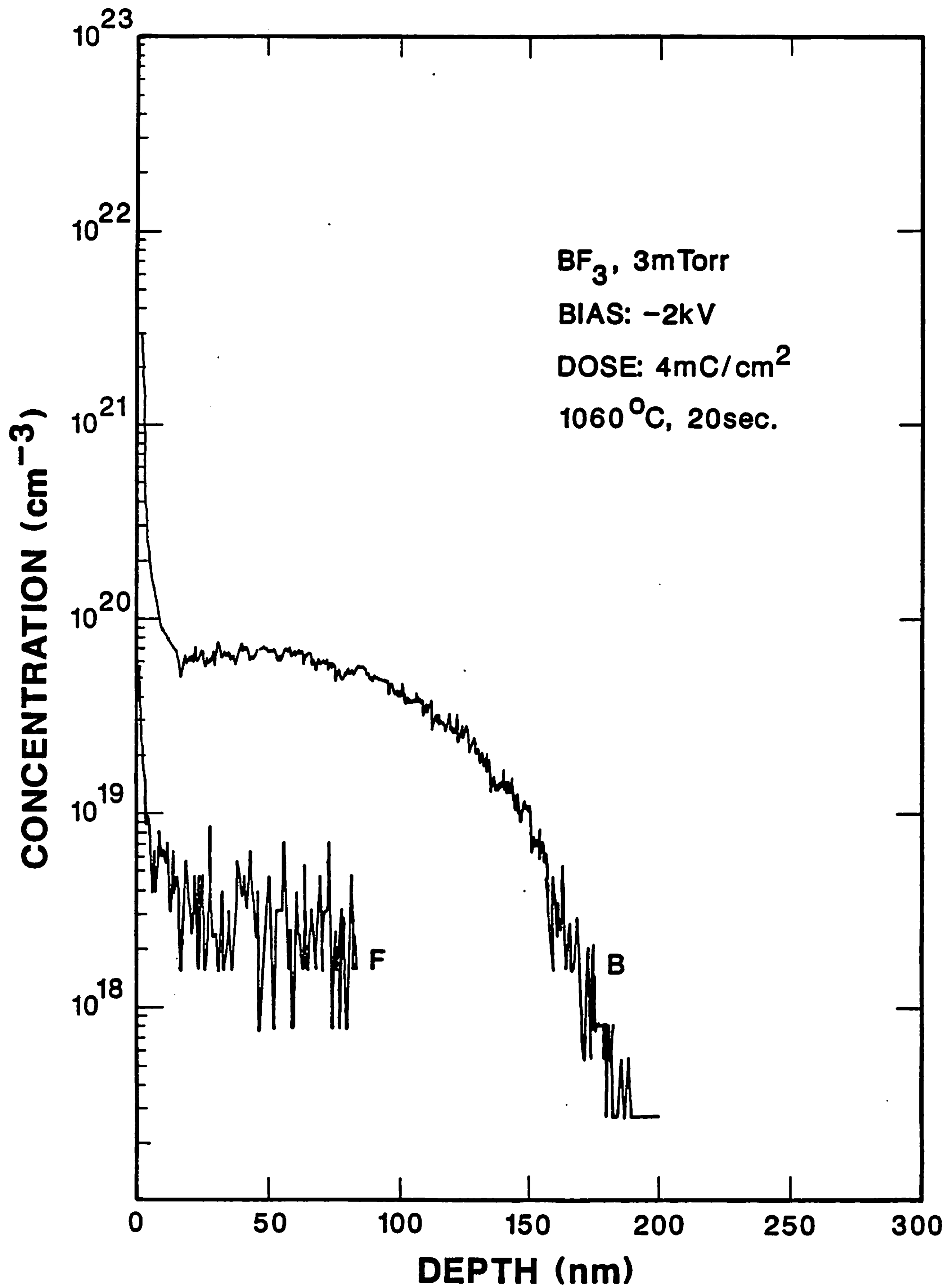
SHEET RESISTANCE (Ω/□)
1000
100
10
0.05
0.5
1
4
20
DOSE (mC/cm2)
-5 kV
1060 °C, 20sec.


300
200
100
0
SHEET RESISTANCE (Ω/□)
4mC/cm2
1060 °C, 20sec.
0.5
2
5
10
20
WAFER BIAS (-kV)

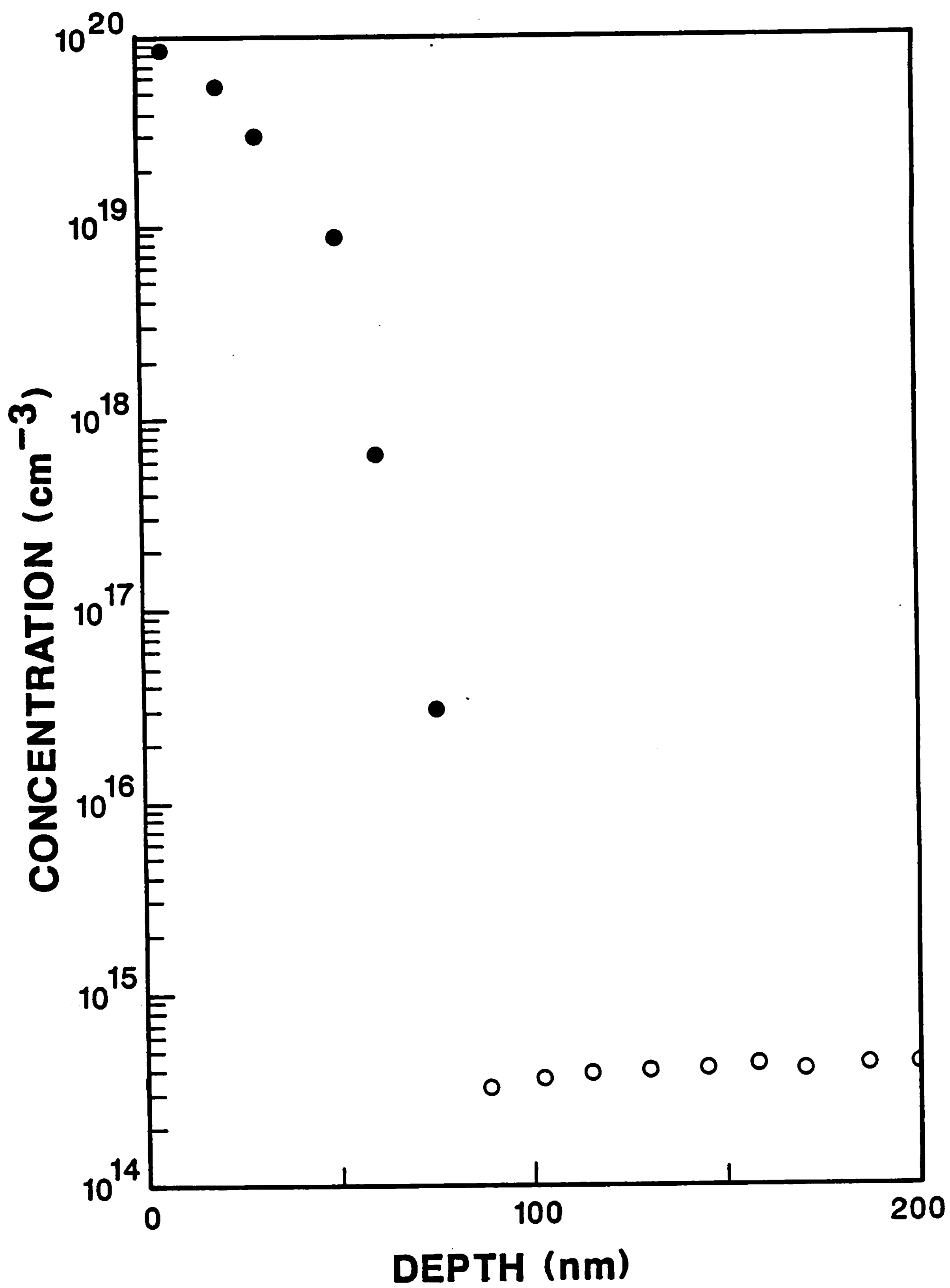

400
300
200
100
0.0
JUNCTION DEPTH (nm)
0
1
2
3
4
5
6
7
8
9
10
11
WAFER BIAS (-kV)
DOSE: 4mC/cm2
1060 OC, 20sec.



BF3, 3mTorr
BIAS: -2kV
DOSE: 4mC/cm2
CONCENTRATION (cm-3)
10^23
10^22
10^21
10^20
10^19
10^18
B
F
0
50
100
150
200
250
300
DEPTH (nm)



10^{23}
10^{22}
10^{21}
10^{20}
10^{19}
10^{18}
CONCENTRATION (cm^{-3})
BF_3, 3mTorr
BIAS: −2kV
DOSE: 4mC/cm^2
1060 ^oC, 20sec.
F
B
0
50
100
150
200
250
300
DEPTH (nm)



10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
10^{14}
CONCENTRATION (cm^{-3})
0
100
200
DEPTH (nm)

CONFORMAL IMPLANTATION FOR TRENCH DOPING WITH PLASMA IMMERSION ION IMPLANTATION

X. Y. Qian, N. W. Cheung and M. A. Lieberman

Plasma Assisted Materials Processing Laboratory,

Department of Electrical Engineering and Computer Sciences,

University of California, Berkeley, CA 94720, USA

R. Brennan,

Solecon Laboratory, Inc.,

2241 Paragon Drive, San Jose, CA 95131, USA

M. I. Current and N. Jha,

Applied Materials, Inc.,

3050 Bowers Avenue, Santa Clara, CA 95054, USA

ABSTRACT

Taking advantage of the moderate beam divergence angle of plasma immersion ion implantation (PIII), we demonstrated conformal doping of boron in high aspect ratio Si trenches. A uniformly doped P+ layer all around the side walls and bottom of trenches with an aspect ratio of 6:1 was observed with scanning electron microscopy (SEM) after junction staining.

To test the limit of this conformal doping technique, an extremely high aspect ratio macroscopic trench model (0.5 mm wide and 12.5 mm deep) made with Si wafer slices was implanted using similar PIII conditions. After rapid thermal annealing, sheet resistance along trench top and sidewalls were evaluated with four-point probe method. The average sheet resistance of trench sidewalls was about twice of that of the trench top. The deviation of the sidewall sheet resistance was ±60% with respect to the mean value.

1. INTRODUCTION

Doping of trench capacitors by ion implantation has focused on the use of multi-step implants at controlled beam incidence angles [1-4]. This approach has led to development of a number of implanter designs for control of implantation angle and changes in wafer orientation [5]. With conventional ion implantation techniques, using a collimated ion beam at energies of 50 to 150 keV, effects of ion reflection, sputtering and damage compound the stringent alignment requirements imposed by the high aspect ratio geometries of trench capacitors [4, 5].

This work describes a fundamentally different approach to trench doping using a directly extracted beam from a plasma, referred to as plasma immersion ion implantation (PIII), to achieve conformal doping profiles throughout the trench sidewall surface area [6]. The use of PIII has been demonstrated for metallurgical surfaces and semiconductor processing [7-10]. Since the PIII beam is believed to have an angular divergence of at least several degrees with operation in the mTorr pressure range, it will have an advantage over conventional implantation with collimated beams. Figure 1 shows the schematic of the trench doping technique using the beam

divergence characteristics of PIII. The trench samples were immersed in a BF_3 plasma, with a negative high voltage applied to the substrate. Ions in the plasma sheath generated by the negative potential were accelerated and implanted into the wafer. Since the gas pressure was maintained in the mTorr range, the accelerated ions presumably have a mean free path of several cm due to charge transfer and elastic scattering. Therefore, a certain angular distribution of bombarding ions is expected. The full width at half maximum of this angular distribution was found to be about 3 degrees at a gas pressure of 1 mTorr with -500 Volts bias according to computer simulation results from a Monte Carlo simulator PDP1 developed at UC Berkeley [11].

2. EXPERIMENT AND RESULTS

The prototype PIII reactor used in this study consists of: 1) an 800 W, 2.45 GHz microwave power supply, 2) an electron cyclotron resonance (ECR) source, 3) a processing chamber with wafer holder and bias supply, and 4) gas handling and diagnostic tools. The reactor was pumped to a base pressure at 10^{-7} Torr before BF_3 was introduced into the chamber. The gas pressure was controlled in the mTorr range. An ECR zone was generated at the center of the source chamber by an applied magnetic field of 875 Gauss. The plasma density was adjusted by varying the microwave power input to the ECR chamber. A negative DC or pulsed high voltage was connected to the wafer holder to supply the bias voltage for implantation. In pulsed mode, the charge flow per pulse was measured with an integrator connected to a current transformer (Rogowski loop). The total dose was later calibrated against the number of pulses. When a DC bias is used, the dose rate was monitored by a current meter serially connected in the circuit. To avoid wafer heating and to obtain better dose control, a lower microwave power of 100-200

Watts with a current density of 0.5-1 mA/cm^2 was used for the DC mode. The detailed description of PIII apparatus has been presented elsewhere [12].

N-type Si wafers were etched with reactive ion etching to form 1 μm wide and 5-6 μm deep trenches. After boron implantation in the PIII reactor, rapid thermal annealing (RTA) in a N_2 ambient at 1060 C° for 30 seconds was used to activate the dopant. The annealed sample was carefully cleaved to expose the trench cross sections. A Si etchant of 30 (HNO_3): 1 (HF) solution was then used to stain the P+/n junction. The boron dopant uniformity and P+/n junction depth along the trench after staining were examined with a scanning electron microscope (SEM). Figure 2 is a SEM picture showing the cross section of the doped trench. This sample was biased with a -10 kV DC voltage during PIII. The BF_3 gas pressure was kept at 5 mTorr. The accumulated areal charge of the implantation current was 4 mC/cm^2. As seen from SEM pictures, the trench top, sidewalls and bottom were uniformly doped. The thickness of the doped layer is about 2500-3000 Å. Uniformly doped layers were observed in samples implanted with -4 kV and -2 kV DC bias or -3.6 kV pulsed bias. There was not much difference in doped layer thickness as observed with SEM within this bias range. However, the doped layer thickness increased to 4500 Å for a sample with ten times the dose. This is probably due to the fact that the implantation profiles in all cases were very shallow, the dopant distribution was dominantly controlled by a driven-in mechanism during RTA, which is concentration dependent. This transient rapid diffusion of shallow boron dopant has been reported by Qian et al. [13].

3. MACROSCOPIC TRENCH SIMULATION

We have also investigated the limit of PIII conformal doping with extremely high aspect ratio. Since it is difficult to determine the dopant profile or carrier concentration on a 1 μm wide, 6 μm deep trench sidewall, a macroscopic trench of aspect ratio 25:1, made with Si slices, was used for the study. Shown in Figure 3 is the illustration of the macroscopic trench. N-type CZ wafers with resistivity of 10 Ω-cm were used to form the trench. The width and depth of the trench were 0.5 mm and 12.5 mm respectively. BF_3 PIII was carried out with same bias as for the microscopic trench sample shown in Figure 2. After RTA at 1060 °C for 1 second, sheet resistance along trench top and sidewalls were evaluated with the four-point probe method. The sheet resistance of the doped layer on the trench top was 225 Ω/□, while the average value on the sidewall was 436 Ω/□. The variation of sheet resistance along trench sidewall is shown in Figure 4. The area near the trench bottom was doped heavier than the area near the trench top. This could be understood as a result of ion multi-reflection from trench sidewalls and bottom. It is well known that when an incident ion collides with a surface at a glancing angle, the reflection probability is high. A large portion of the ion beam hitting the sidewall was presumably reflected, leaving the top part of the sidewall lightly doped. The large dose on the lower sidewall can be attributed to reflected ions from the trench bottom as well as from the top part of the sidewalls.

With our experimental PIII system, the standard deviation of sheet resistance across a two inch wafer was about 40% with a pulsed bias. The uniformity was poorer in the DC mode, especially when the bias voltage was high. A much better uniformity is expected with the

recently constructed ten inch reactor in UC Berkeley.

4. CONCLUSIONS

We have demonstrated conformal doping of boron in high aspect ratio Si trenches using PIII. A uniformly doped P+ layer all around the sidewalls and bottom of trenches of aspect ratio 6:1 was observed with scanning electron microscopy after junction staining. To test the limit of PIII for conformal doping, the macroscopic trench results showed that the average sheet resistance of trench sidewalls was about twice of that of the trench top and the deviation of the sheet resistance of sidewall was ±60% with an aspect ratio of 25:1.

This work was supported by Applied Materials, Inc. and a grant from the California State MICRO program.

REFERENCES

[1] R. Kakoschke, H. Binder, S. Rohl, K. Masseli, I. W. Rangelow, S. Saler and R. Kassing, *Nuc. Instr. Meth.* **b21** (1987) 142-147.

[2] G. Fuse, H. Umimoto, S. Okanaka, M. Wakabayashi, M. Fukumoto and T. Ohzone, *J. Electrochem. Soc.* **133** (1986) 996-998.

[3] G. Fuse, K. Tateiwa, S. Odanaka, T. Yamada, I. Nakao, H. Shimoda, O. Shippou, M. Fuumoto, J. Yasui, Y. Naito, and T. Ohzone, 19th conf. on Solid State Devices and Materials, Tokyo (1987) 11-14.

[4] G. Fuse, H. Ogawa, K. Tamura, Y. Naito and H. Iwasaki, *Appl. Phys. Lett.* **54** (16) (1989) 1534-1536.

[5] R. E. Kaim, *Solid State Technology* **33** (2) (Feb. 1990) 103-107.

[6] M. A. Lieberman, *J. Appl. Phys.* **66** (7) (1989) 2926-2929.

[7] J. R. Conrad, J. L. Radtke, R. A. Dodd, F. J. Worzala and N. C. Tran, *J. Appl. Phys.* **62** (11) (1987) 4591-4596.

[8] Bi Mizuno, I. Nakayama, N. Aoi, M. Kubota and T. Komeda, *Appl. Phys. Lett.* **53** (21) (1988) 2059-2061.

[9] H. Wong, X. Y. Qian, D. Carl, N. W. Cheung, M. A. Lieberman, I. G. Brown and K. M. Yu, MRS proceedings, **147**, 91-96 (1989).

[10] X. Y. Qian, H. Wong, D. Carl, N. W. Cheung, M. A. Lieberman, I. G. Brown and K. M. Yu, presented in ECS 1989 fall meeting and to be published in the proceedings.

[11] V. Vahedi, M. A. Lieberman, M. A. Alves, J. P. Verboncoeur, and C. K. Birdsall, "A Collisional Model for Plasma Immersion Ion Implantation", 1990 IEEE International Conference on Plasma Science, May 21-23, 1990, Oakland, California, USA.

[12] X. Y. Qian, D. Carl, J. Benasso, N. W. Cheung, M. A. Lieberman, I. G. Brown, J. E. Galvin, R. A. MacGill and M. I. Current, to be published in the VIII International Conference on Ion Implantation Technology, July 31 - Aug. 3, 1990, Univ. of Surrey, UK.

[13] X. Y. Qian, N. W. Cheung, M. A. Lieberman and M. I. Current, to be published in the VIII International Conference on Ion Implantation Technology, July 31 - Aug. 3, 1990, Univ. of Surrey, UK.

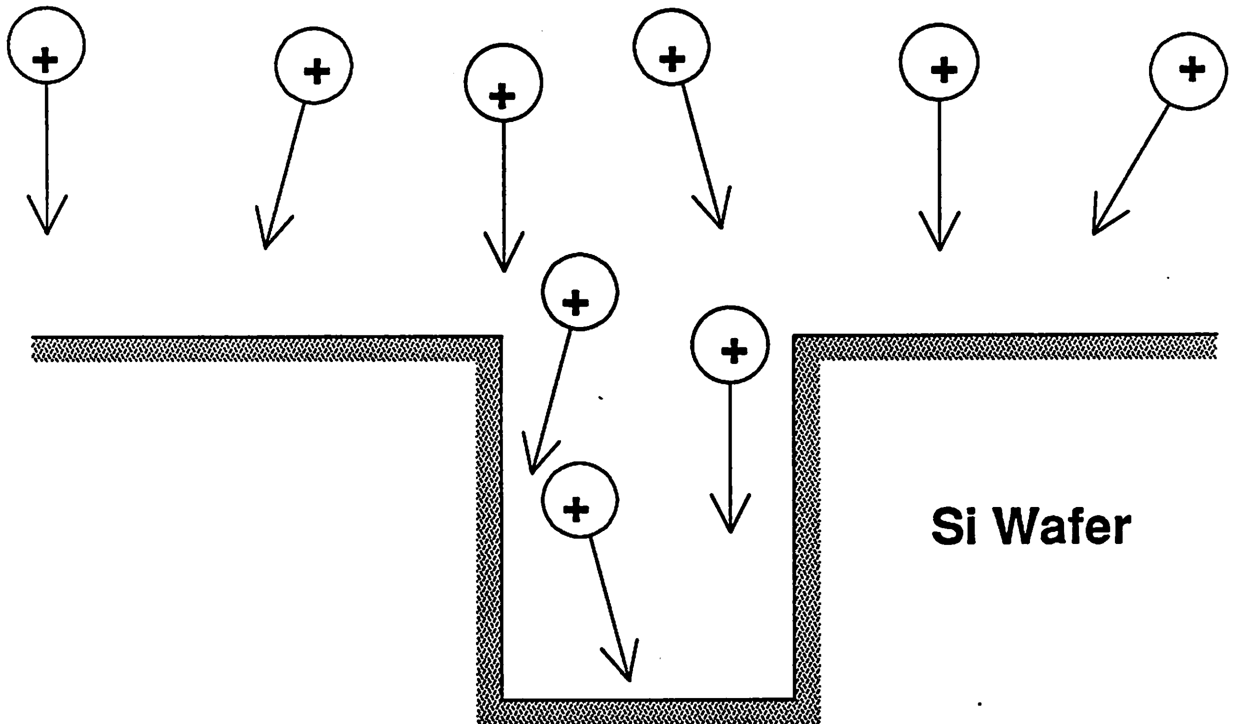
FIGURE CAPTIONS

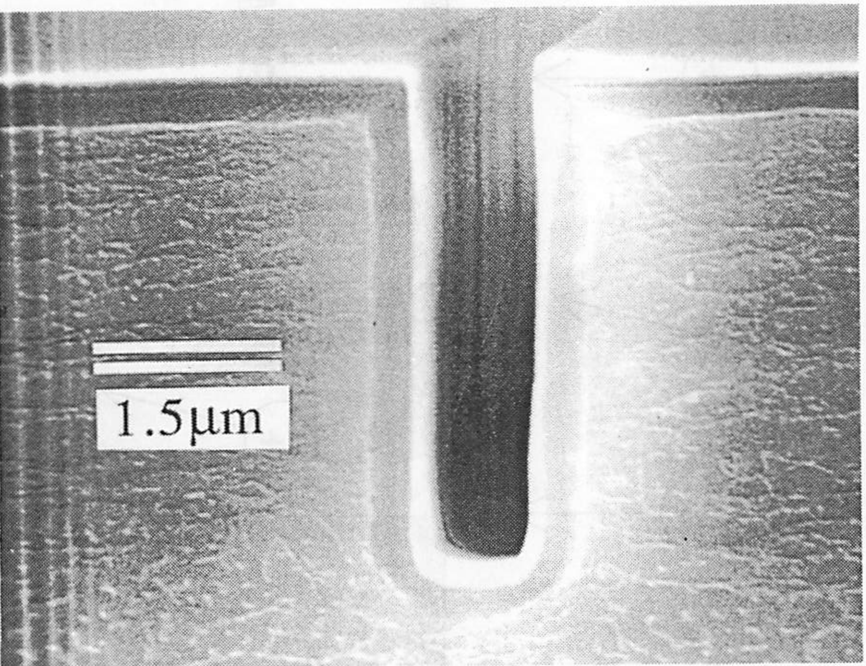
Fig.1 Schematic showing trench conformal doping with plasma immersion ion implantation.

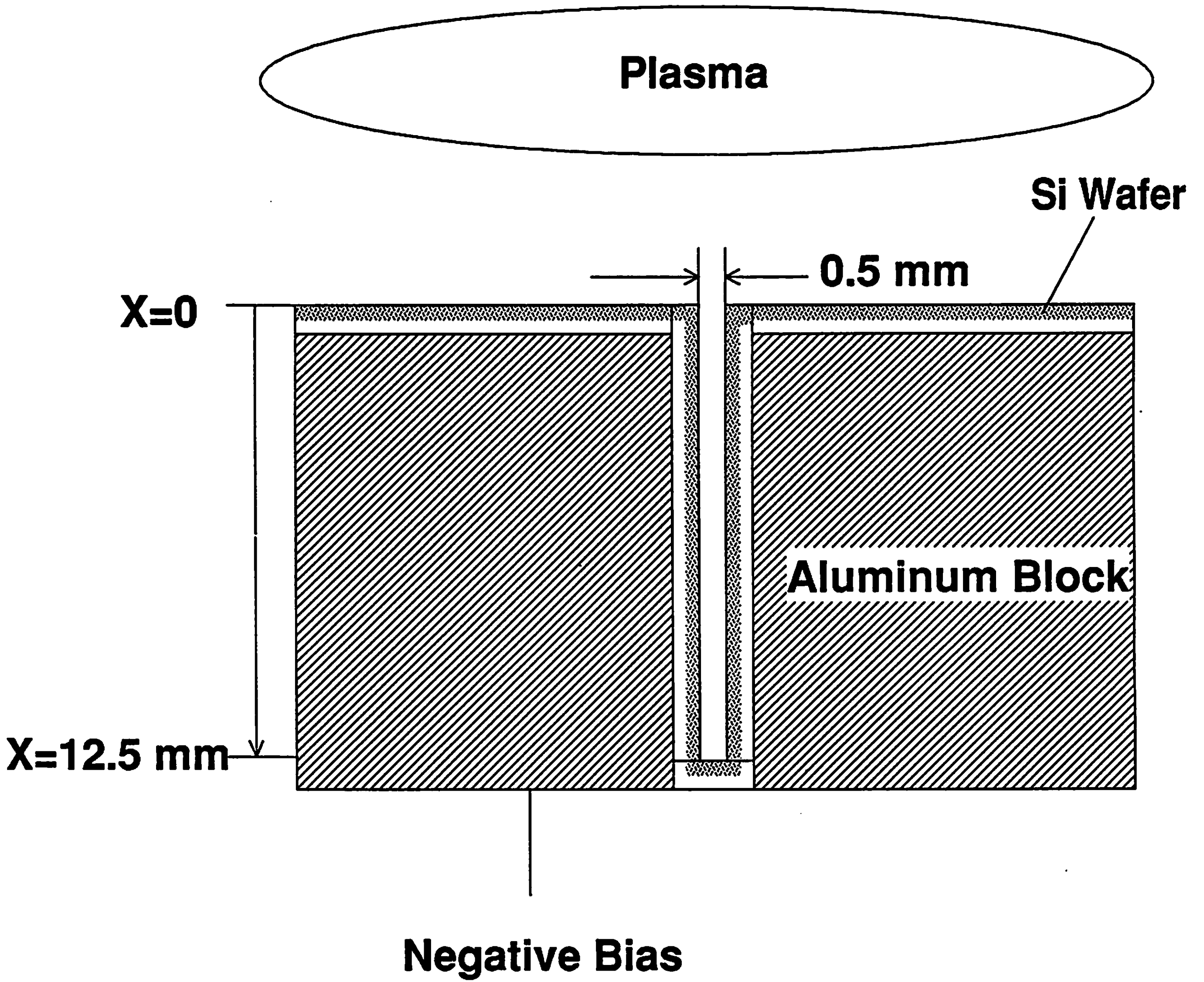
Fig.2 Cross section SEM picture of Si trench doped in BF_3 plasma using PIII. The pressure was maintained at 5 mTorr and the wafer bias was -10 kV during PIII. The wafer accumulated charge was 4 mC/cm^2.

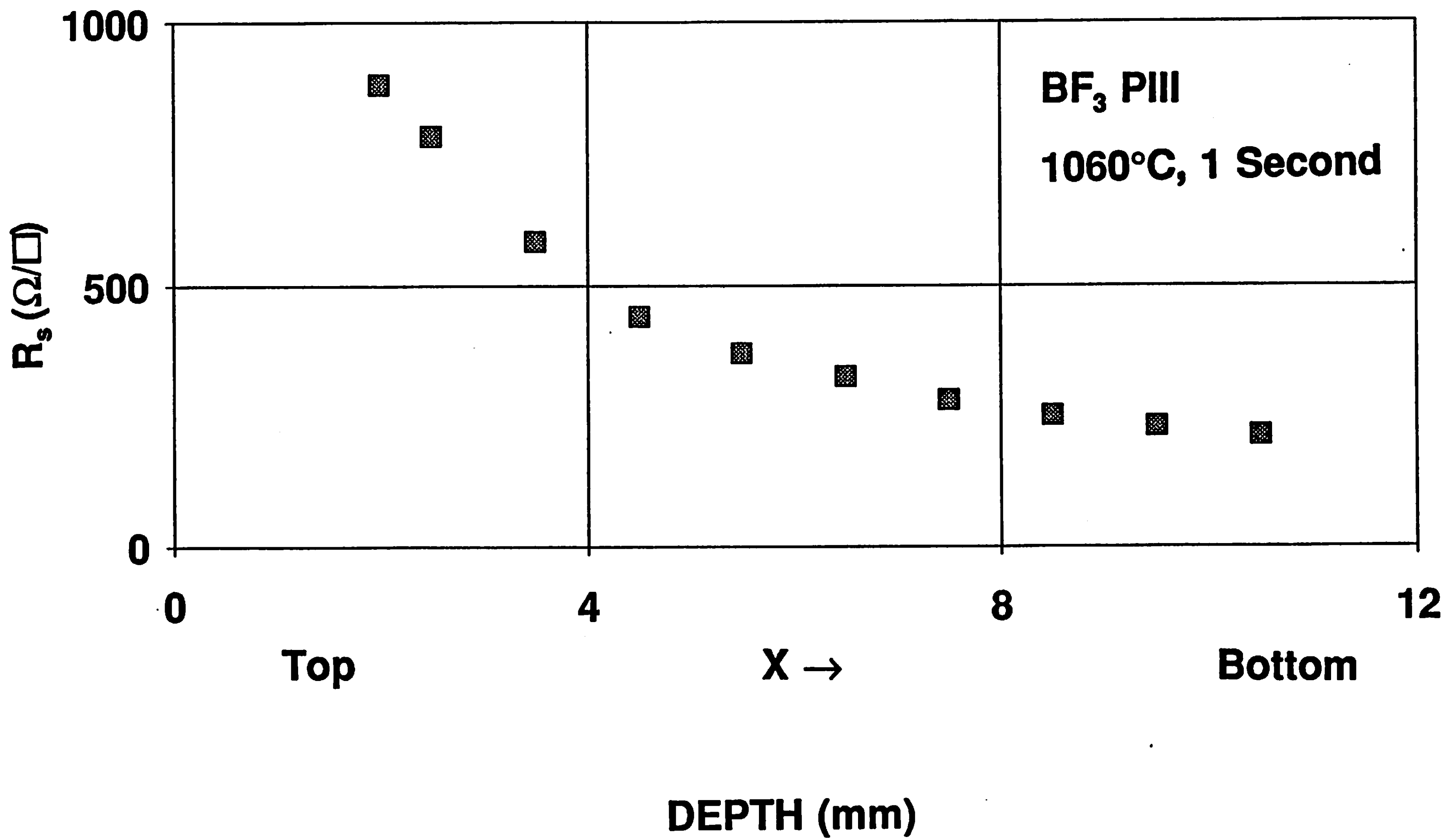
Fig.3 Sample geometry to simulate the trench on a macroscopic scale.

Fig.4 Sheet resistance of the doped layer along a sidewall of the macroscopic model trench.


Plasma
Si Wafer
Negative Bias


1.5μm


Plasma
Si Wafer
0.5 mm
X=0
Aluminum Block
X=12.5 mm
Negative Bias


1000
500
0
0
4
8
12
Top
X →
Bottom
DEPTH (mm)
R_s (Ω/□)
BF_3 PIII
1060°C, 1 Second

PLASMA IMMERSION Pd ION IMPLANTATION SEEDING PATTERN FORMATION FOR SELECTIVE ELECTROLESS Cu PLATING

X. Y. Qian, M. H. Kiang, J. Huang, D. Carl, N. W. Cheung and M. A. Lieberman,

Plasma Assisted Materials Processing Laboratory,

Department of Electrical Engineering and Computer Sciences,

University of California, Berkeley, CA 94720, USA

I. G. Brown and K. M. Yu,

Lawrence Berkeley Laboratory, University of California, Berkeley, CA 94720, USA

M. I. Current,

Applied Materials, Inc., Implant Division: MS0907,

3050 Bowers Avenue, Santa Clara, CA 95054, USA

ABSTRACT

Selective plating of Cu interconnects has been carried out using plasma immersion Pd ion implantation and Cu electroless plating. Pd atoms were sputtered from a negatively biased target and ionized in an Ar electron cyclotron resonance (ECR) plasma. The Pd ions were implanted into the SiO_2 substrates biased with negative pulsed high voltages. In our studies, we found the required Pd seeding dose for Cu plating was on the order of $5\times10^{14}/cm^2$. With this direct Pd implantation technique, an intermediate activation step using a $PdCl_2$ solution was eliminated.

1. INTRODUCTION

Because of its low electrical resistivity and good electromigration property, copper has been proposed as the interconnect material of choice for submicron IC metallization [1]. However, reactive ion etching of copper is difficult because the etching products are usually non-volatile. This constraint leads to some recent investigation in selective copper deposition by chemical vapor deposition [2] or electroless plating [1]. To initiate the nucleation process for electroless plating, catalyst atoms are required as the seeds on the SiO_2 substrate to be plated. Plasma immersion ion implantation (PIII) technique is well suited for this purpose [3-5]. With PIII, seed metallic materials can be supplied directly from a sputtering target and implanted into the substrate. The implantation dose rate of PIII can be much higher than with a conventional implanter. In addition, by choosing the proper substrate bias voltage, the peak concentration of implanted ions can be on the surface so that no intermediate etching steps are needed to expose the profile peak for Cu plating. The gradual transition from a Pd-rich surface to a pure SiO_2 substrate is also expected to improve the adhesion of the plated Cu film. In this paper, we report the feasibility of using PIII to form seeding patterns for selective electroless Cu plating on SiO_2, and direct Cu plating is feasible without an intermediate $PdCl_2$ solution activation process.

2. EXPERIMENTS

A schematic of the plasma immersion Pd ion implanter developed at the University of California, Berkeley is shown in Figure 1. A Pd target was introduced into an electron cyclotron resonance (ECR) Ar plasma. The plasma was generated with 700 W microwave power at 2.45

GHz. The magnetic field needed for the electron cyclotron resonance was supplied with two coils surrounding the ECR chamber. The Ar gas pressure was regulated with a pressure controller in the 1-10 mTorr range. A DC negative bias from 50 Volts to 400 Volts was applied to the Pd sputtering target; sputtered Pd atoms were ionized in the Ar plasma. An optical emission spectrometer was used to monitor photoemission from neutral and ionized species. A pulsed negative bias of several kV was applied to a Si wafer in the downstream plasma to facilitate the implantation process.

Blanket and patterned SiO_2 substrates were used for this Pd PIII implantation study. The SiO_2 substrate film was formed on Si wafers with wet oxidation at 1000 °C for 2 hours. Rutherford Backscattering Spectroscopy (RBS) was used to analyze implanted Pd and Ar profiles. The electroless Cu plating was performed in a mixture of $CuSO_4$ and KCN solution [6]. In the case of a patterned SiO_2 substrates, a photoresist stripping step was added before Cu plating.

3. RESULTS AND DISCUSSION

Optical emission spectroscopy was carried out with Ar plasma at various gas pressures and target biases. Shown in Figure 2 is a pair of differential spectra where the emission from Ar has been subtracted. Emission lines at wavelengths 244.7nm, 247.6nm and 276.3nm from excited Pd neutral atoms are prominent. The intensities from these peaks are similar for Ar pressures of 1 mTorr and 10 mTorr. However, emission lines from Pd ions at 248.9nm and 249.0nm, 249.9nm and 250.6nm, and 255.2nm for the case of Ar pressure of 10 mTorr in Figure 2(a) are more pronounced than at 1 mTorr as shown in Figure 2(b). This increase of Pd ionization with higher

gas pressure is in agreement with the ion density measurements where a higher plasma density has been found in a 10 mTorr Ar plasma [7].

Blanket Si wafers with 1 μm SiO_2 were used for the initial PIII and plating condition studies. Shown in Figures 3(a) and 3(b) are RBS spectra of two samples implanted with Pd and Ar using PIII. Both samples were implanted in a 10 mTorr Ar plasma at 700 W. The Pd target was connected to a DC power supply at -60 Volts; 500 mA target current was measured. The wafer was biased to a -6 kV peak potential at 1 kHz with a high voltage pulser. The pulse width was 1 μs. It was found that for such a low energy, both Ar and Pd were implanted in the SiO_2 surface. The electroless Cu plating was performed at 72 °C with a pH value of the plating solution equals to 13. No plating of Cu was observed with more than 30 minutes of plating time for the samples with a Pd dose of $1.8\times10^{14}/cm^2$ as measured by RBS. However, the sample with a slightly higher Pd dose $4.5\times10^{14}/cm^2$ rapidly seeded Cu. Figure 4 shows that a threshold Pd dose at $3\text{-}4\times10^{14}/cm^2$ is required for Cu plating to occur. The plated Cu films are continuous with mirror finishes.

For multilevel interconnection technology, maintaining a planar interconnect structure will improve lithography definition and metal step-coverage. The process flow of planarized Cu interconnect based on electroless plating is shown in Figure 5. Si wafers with 1 μm thermal SiO_2 were patterned with photoresist. Then, 4500 Å deep trenches on the SiO_2 layer were formed with dry etching. Pd ion implantation was carried out in the PIII reactor with the patterned photoresist as implantation mask. After the mask was stripped, Cu electroless plating was performed. Figure 6(a) shows an optical micrograph of the Cu film grown in the Pd implanted trenches. The Cu

plated lines shown were 2 μm wide and no Cu plating was found on the SiO_2 surface. In Figure 6(b), the scanning electron microscopy micrograph shows that the plated Cu was about 2000 Å thick.

4. CONCLUSION

We have demonstrated the selective plating of Cu interconnects using Pd PIII for the seeding process. The required Pd PIII dose is on the order of $3\text{-}4\times10^{14}/cm^2$. With direct Pd implantation, an intermediate activation step using a $PdCl_2$ solution is not necessary. Other implanted species such as Pt, Au and Cu are also expected to work with this selective plating process.

This work was supported by Applied Materials, Inc. and a grant from the California State MICRO program.

REFERENCES

[1] P. L. Pai and C. H. Ting, *IEEE Electron Device Lett.*, **10** (9), pp. 423, Sep. 1989.

[2] A. Awaya and Y. Arita, Proceedings of VLSI Symposium, Kyoto, Japan, May 22-25, 1989, pp. 103-104.

[3] J. R. Conrad, J. L. Radtke, R. A. Dodd, F. J. Worzala and N. C. Tran, *J. Appl. Phys.* **62**, 4591, (1987).

[4] J. Tendys, I. J. Donnelly, M. J. Kenny and J. T. A. Pollock, *Appl. Phys. Lett.* **53** (22),

2143, (1988).

[5] X. Y. Qian, D. Carl, J. Benasso, N. W. Cheung, M. A. Lieberman, I. G. Brown, J. E. Galvin, R. A. MacGill and M. I. Current, to be published in the VIII International Conference on Ion Implantation Technology, July 31 - Aug. 3, 1990, Univ. of Surrey, UK.

[6] X. Y. Qian, M. H. Kiang, N. W. Cheung, M. A. Lieberman, I. G. Brown, X. Godechot and K. M. Yu, to be published in the VIII International Conference on Ion Implantation Technology, July 31 - Aug. 3, 1990, Univ. of Surrey, UK.

[7] D. Carl, private communication.

FIGURE CAPTIONS

Fig.1 Schematic of plasma immersion Pd ion implanter for selective Cu plating seeding layer formation.

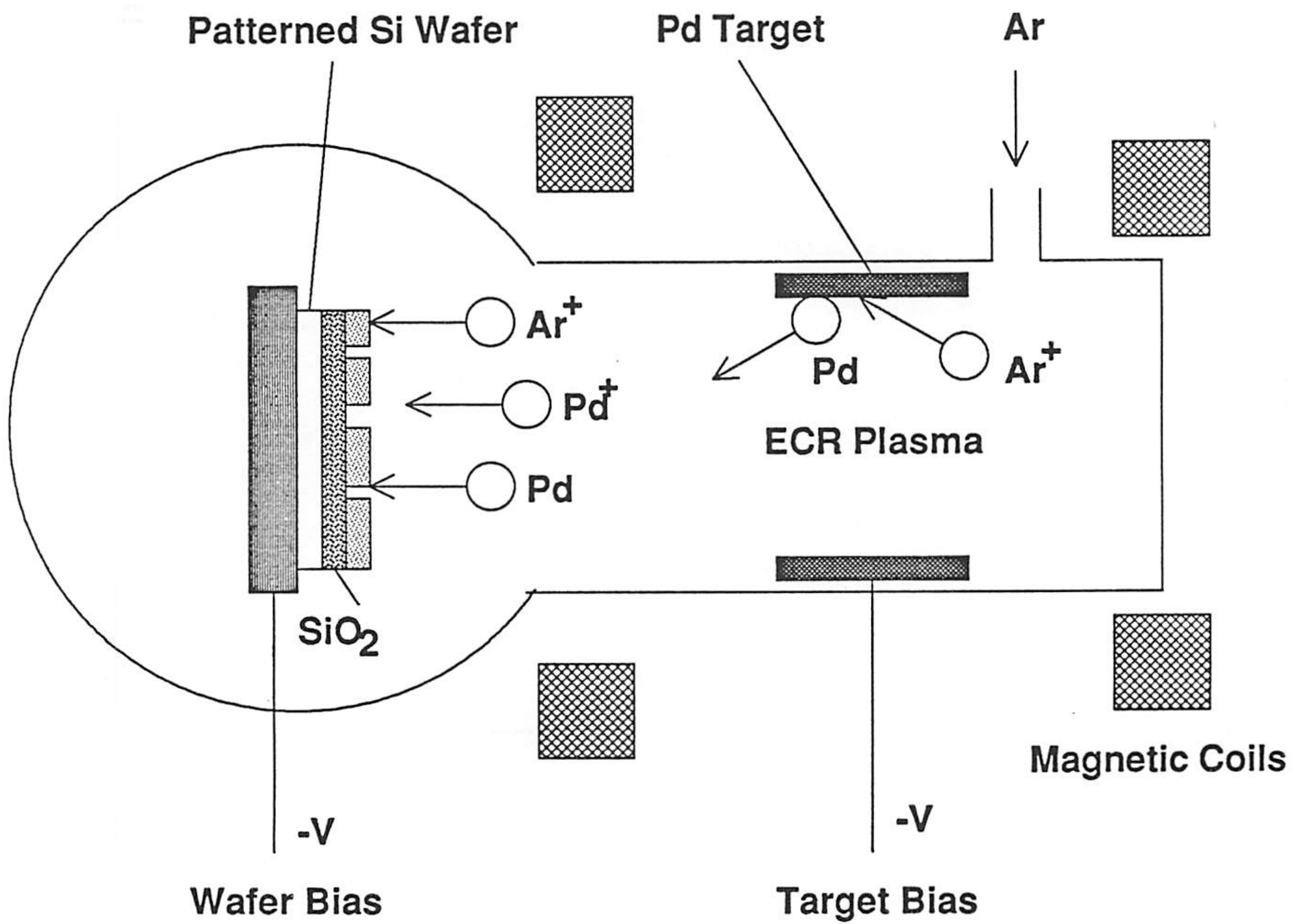
Fig.2 Differential optical emission spectra from plasma immersion Pd ion implanter with Ar pressures at 10 mTorr (a) and 1 mTorr (b). The emission from Ar has been subtracted. Strong emission peaks from excited Pd neutral atoms and Pd^+ ions are marked.

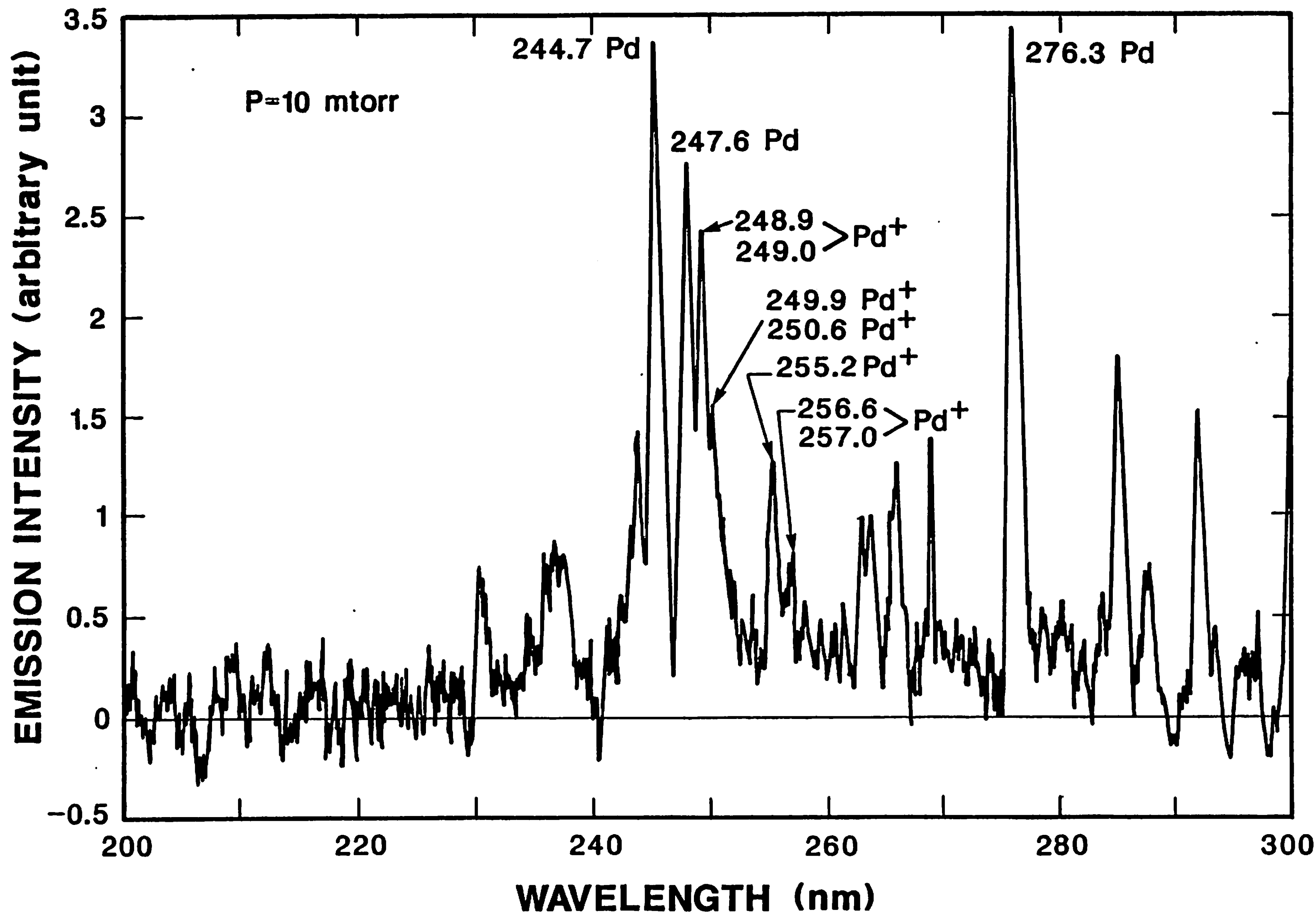
Fig.3 RBS spectra of two samples implanted with Pd and Ar using PIII. Both samples were implanted in a 10 mTorr Ar plasma. The Pd target bias was -60 Volts DC. The wafer was biased with 1 μs pulses at 1 kHz. The pulse peak was at -6 kV. RBS spectra were taken with a 2 MeV He beam at a normal incident angle to the wafer surface. No plating of Cu was observed in 30 minutes for the samples with a Pd dose of $1.8\times10^{14}/cm^2$ (a). The sample with Pd dose of $4.5\times10^{14}/cm^2$ rapidly seeded Cu (b).

Fig.4 Threshold Pd PIII dose for electroless Cu plating.

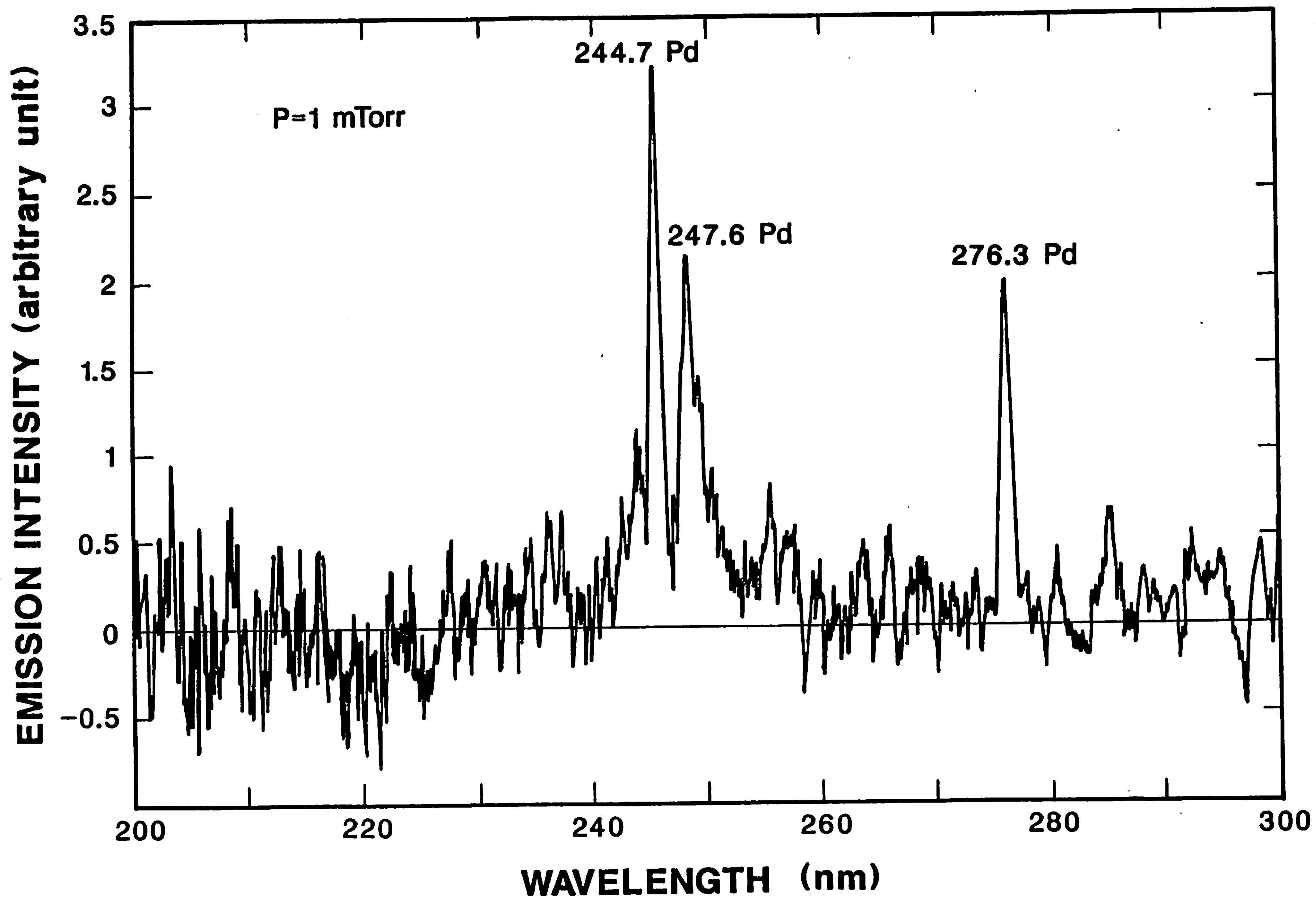
Fig.5 Process sequence of selective Cu plating: 1. Wet oxidation followed by photoresist patterning and reactive ion etching;. 2. Pd ion implantation and photoresist removal; 3. Electroless Cu plating.

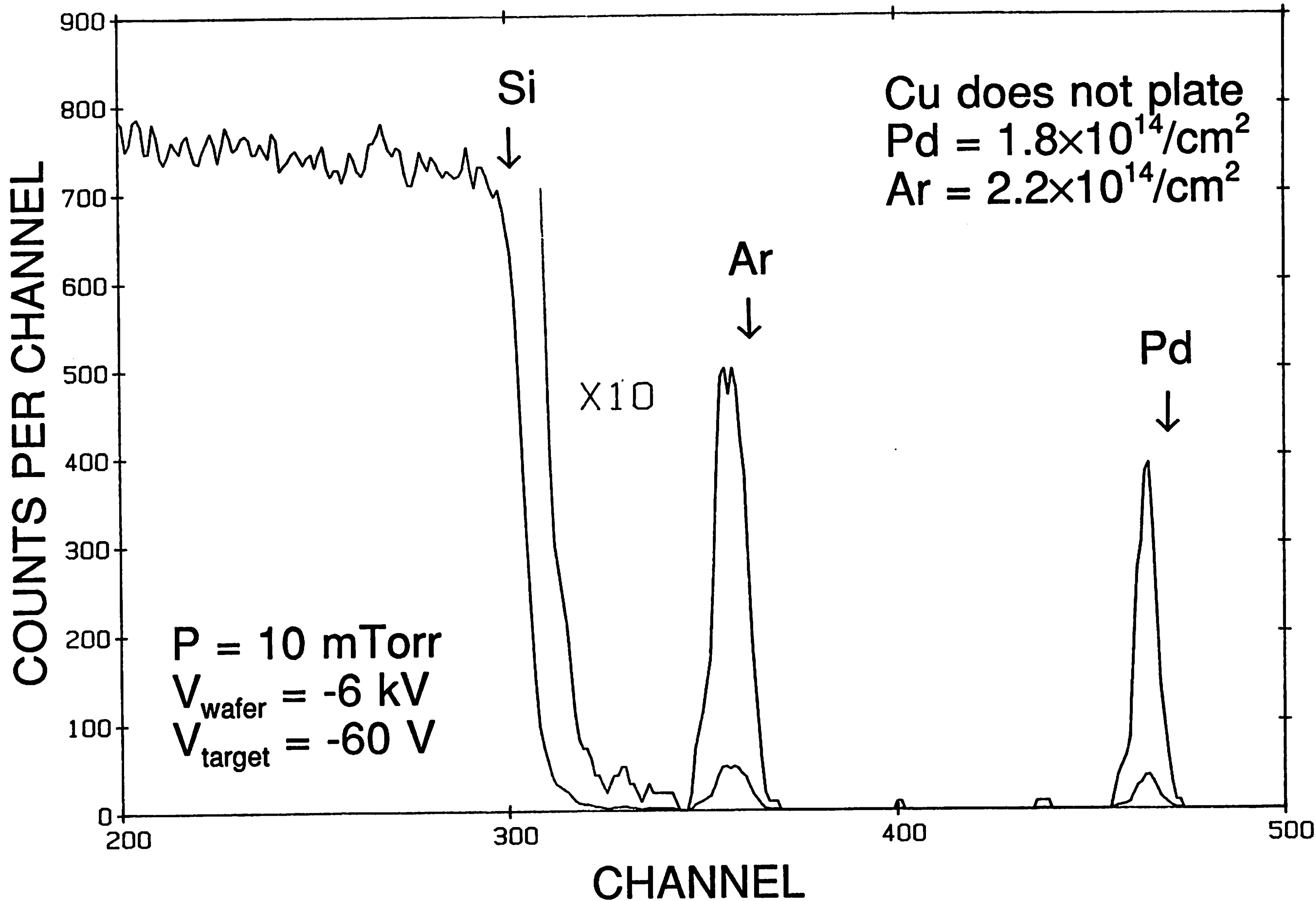
Fig.6 (a) Optical, and (b) scanning electron microscopy pictures of Cu plated trenches.


Patterned Si Wafer
Pd Target
Ar
Ar+
Pd+
Pd
Pd
Ar+
ECR Plasma
SiO2
Magnetic Coils
-V
-V
Wafer Bias
Target Bias

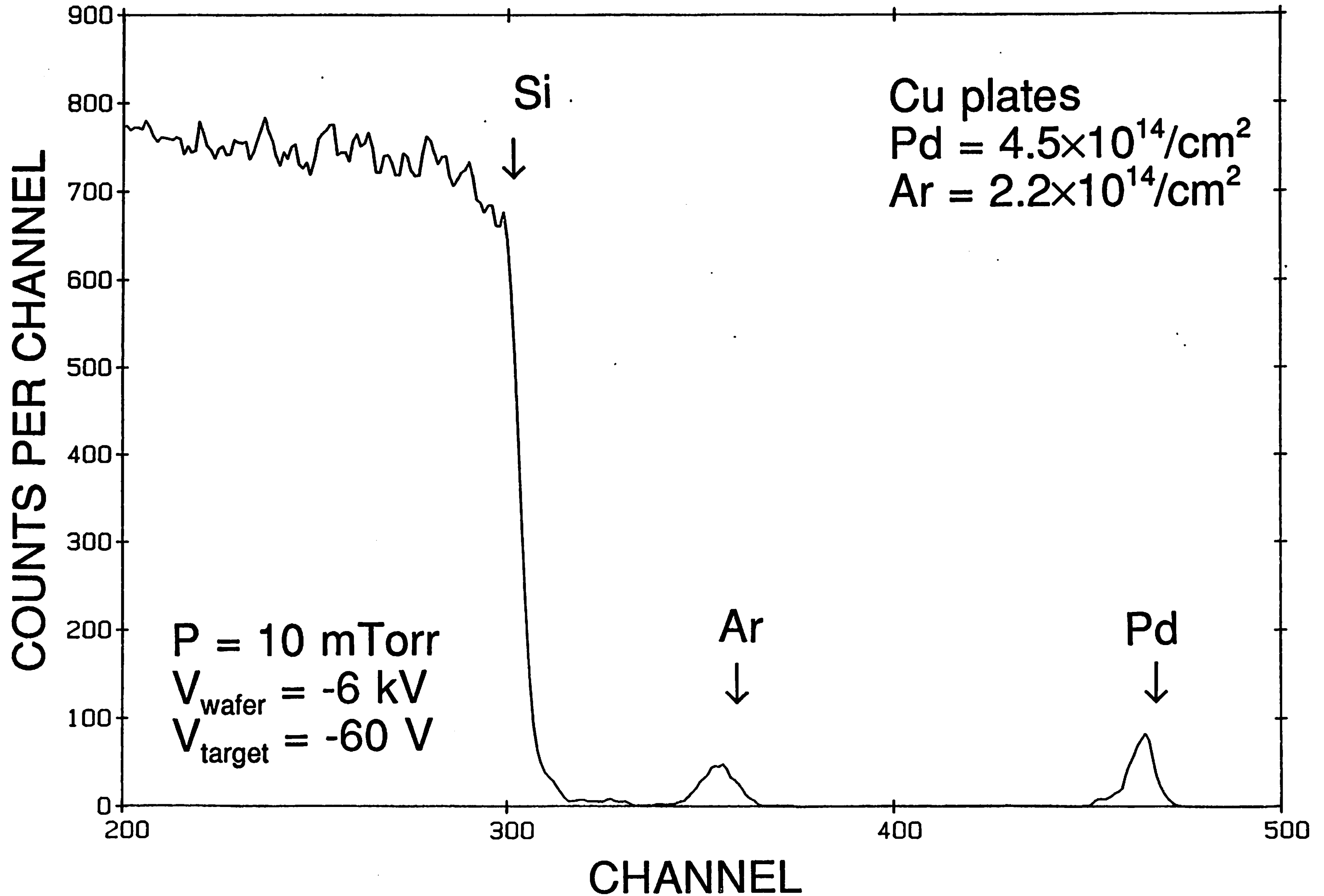


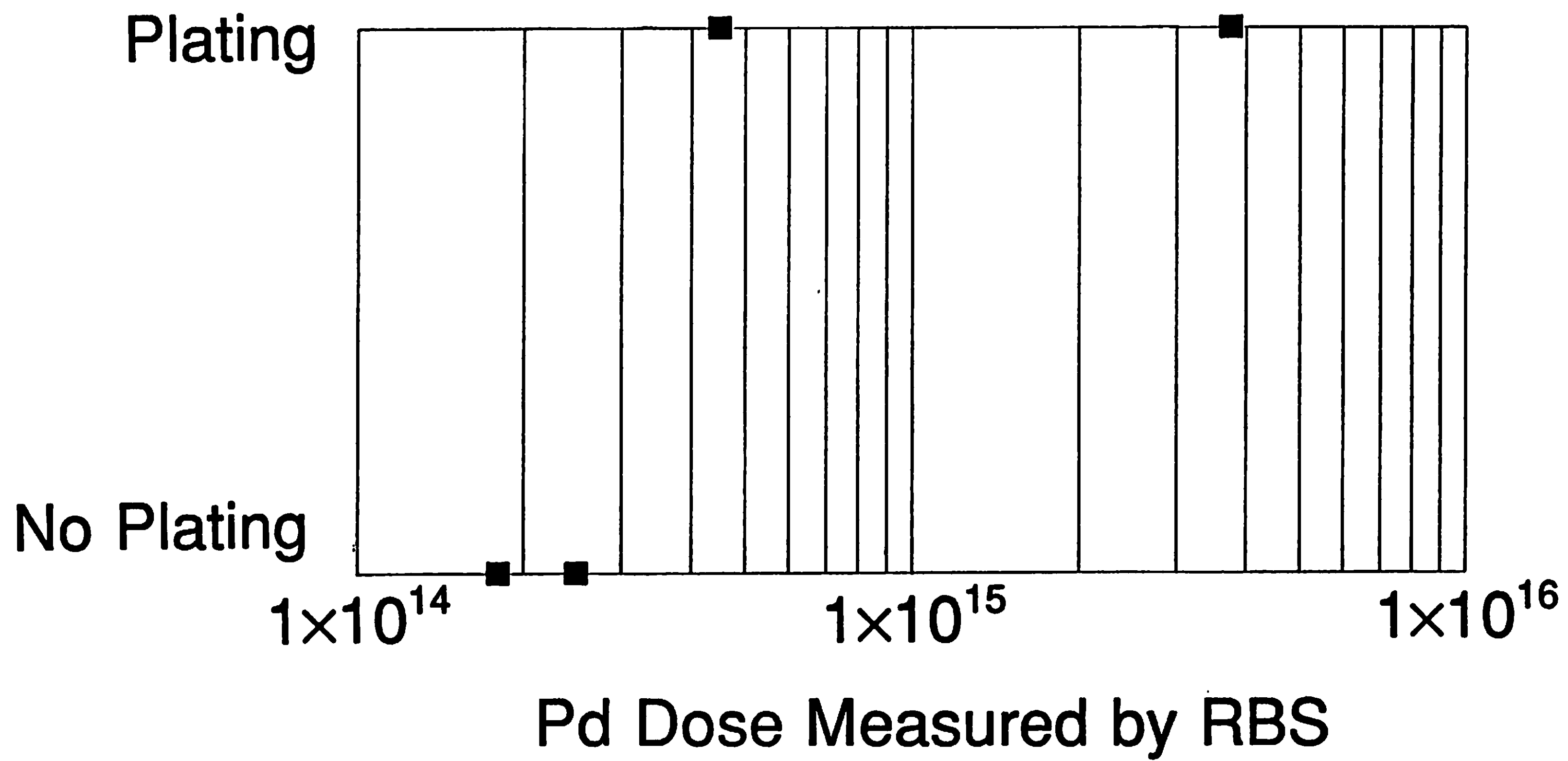
EMISSION INTENSITY (arbitrary unit)
WAVELENGTH (nm)
P=10 mtorr
244.7 Pd
247.6 Pd
248.9
249.0
Pd+
249.9 Pd+
250.6 Pd+
255.2 Pd+
256.6
257.0
Pd+
276.3 Pd
3.5
3
2.5
2
1.5
1
0.5
0
−0.5
200
220
240
260
280
300


EMISSION INTENSITY (arbitrary unit)
WAVELENGTH (nm)
P=1 mTorr
244.7 Pd
247.6 Pd
276.3 Pd
3.5
3
2.5
2
1.5
1
0.5
0
−0.5
200
220
240
260
280
300



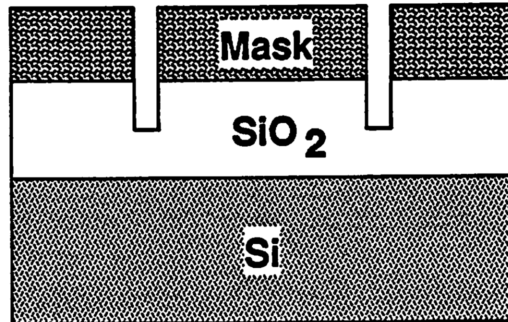
Si
Cu does not plate
Pd = 1.8×10^14/cm^2
Ar = 2.2×10^14/cm^2
Ar
Pd
X10
P = 10 mTorr
V_wafer = -6 kV
V_target = -60 V
COUNTS PER CHANNEL
CHANNEL
0
100
200
300
400
500
600
700
800
900
200
300
400
500


Si
Cu plates
Pd = 4.5×10^14/cm^2
Ar = 2.2×10^14/cm^2
P = 10 mTorr
V_wafer = -6 kV
V_target = -60 V
Ar
Pd
COUNTS PER CHANNEL
CHANNEL
0
100
200
300
400
500
600
700
800
900
200
300
400
500

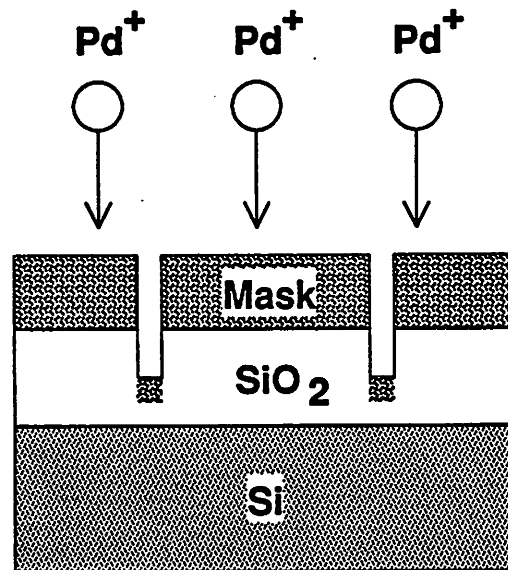


Plating
No Plating
1×10^14
1×10^15
1×10^16
Pd Dose Measured by RBS

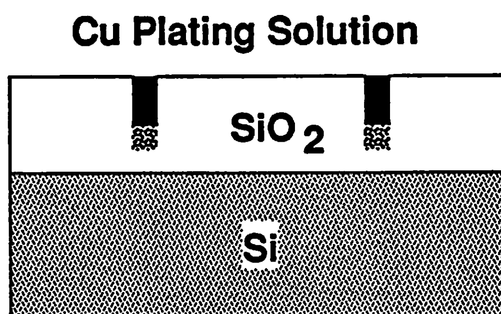
1.

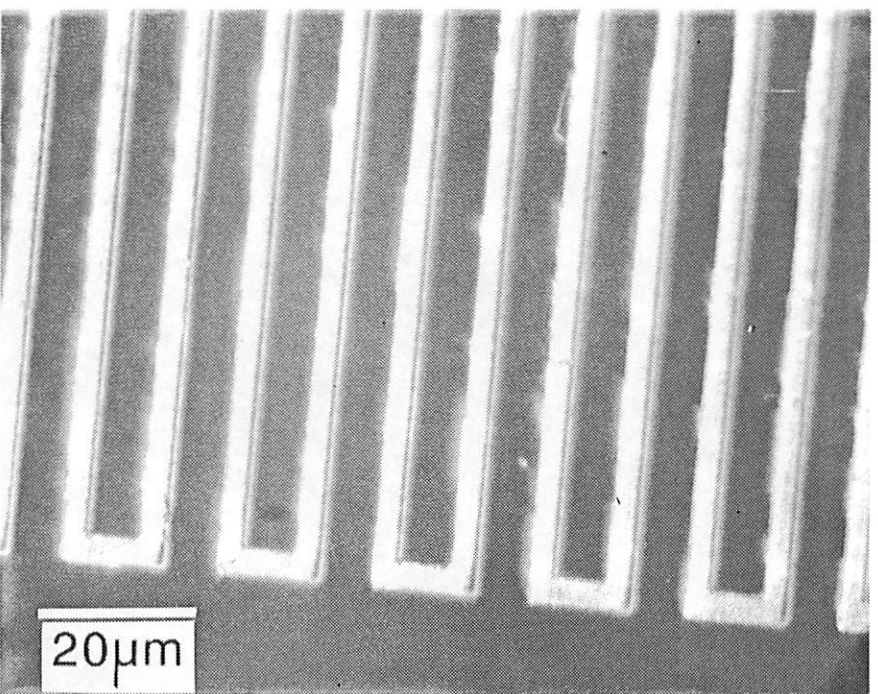


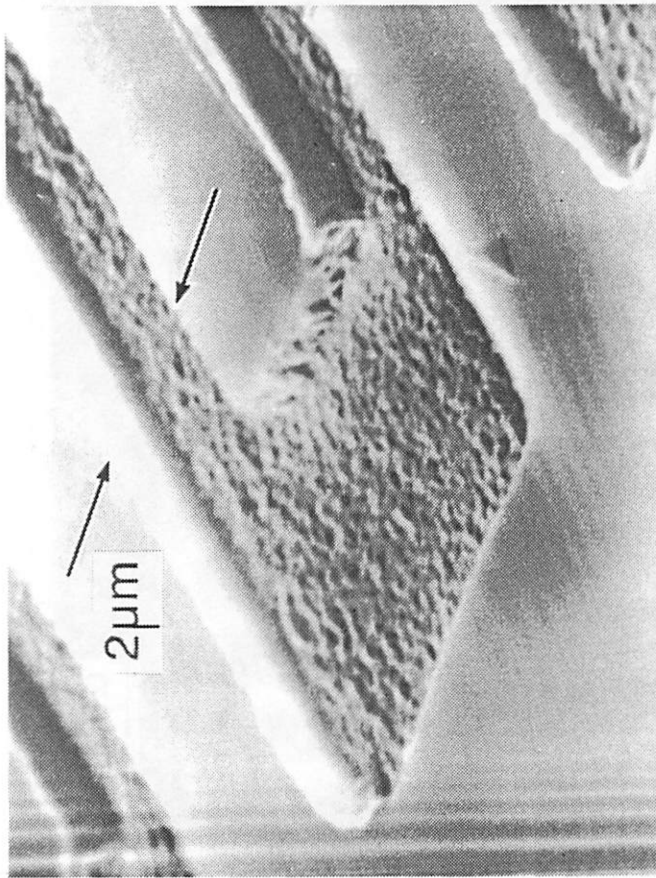
2.



3.




20μm


2μm