PLASMA IMMERSION ION IMPLANTATION (PIII) FOR INTEGRATED CIRCUIT MANUFACTURING

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M.A. Lieberman and N.W. Cheung

Memorandum No. UCB/ERL M91/26

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College of Engineering
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First Quarterly Progress Report
December 18, 1990 - March 17, 1991

PLASMA IMMERSION ION IMPLANTATION (PIII) FOR INTEGRATED CIRCUIT MANUFACTURING

CCTP Contract # C90-071

Applied Materials Inc.

Project Managers:	M.A. Lieberman, UCB
	N.W. Cheung, UCB
Product Manager:	W.J. Wriggins, Applied Materials
Program Manager:	P.R. Klein, CA Office of Competitive Technology

FINANCIAL REVIEW

CompTech Program
Plasma Immersion Ion Implantation for Integrated Circuit Processing
Grant No. C90-071
First Quarterly Report
December 18, 1990 - March 17, 1991*

Participant	To Date Planned	To Date Actual	Percent Actual of Planned	This Quarter Planned	This Quarter Actual	Percent Actual of Planned	Next Quarter Planned
CompTech	31,753	54,188	1.70	31,753	54,188	1.70	35,501
Applied Materials							
Cash	16,624	50,791	3.05	16,624	50,791	3.05	13,155
In-kind	3,750	4,000	1.06	3,750	4,000	1.06	3,750

*Financial report goes through the end of March as UC Berkeley's financial information is reported to the Departments in monthly amounts.

The amounts include indirect costs.

PERSONNEL

N.W. Cheung	Project Manager	UCB
M.A. Lieberman	Project Manager	UCB
W.J. Wriggins	Product Manager	Applied Materials
P.R. Klein	Program Manager	OCT
R.A. Stewart	Postdoctoral Research	UCB
C.A. Pico	Postdoctoral Research	UCB
J. Tao	Visiting Scholar	UCB
M.S. Kiang	Graduate Student	UCB
C. Yu	Graduate Student	UCB
V. Vahedi	Graduate Student	UCB
B. Troyanovsky	Undergraduate Student	UCB
W. En	Undergraduate Student	UCB
E. Jones	Undergraduate Student	UCB
J. Benasso	Technician	UCB

PROJECT REVIEW

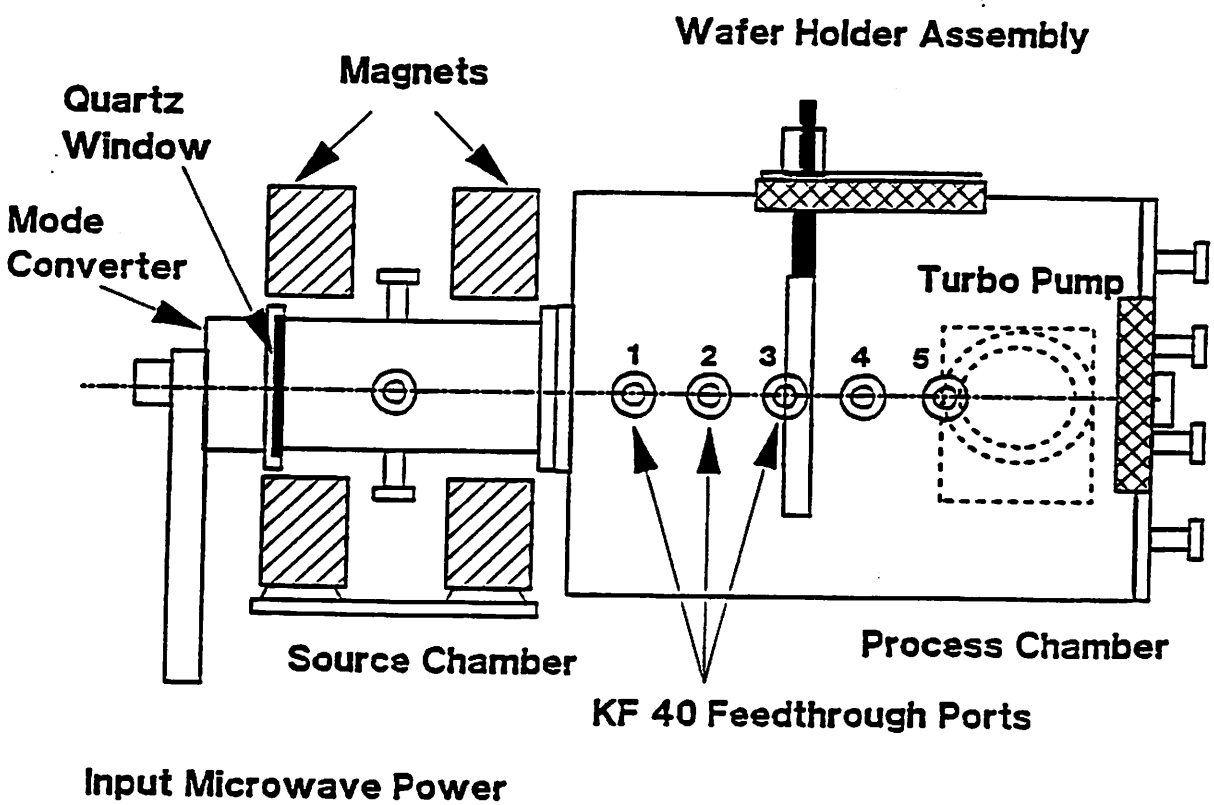
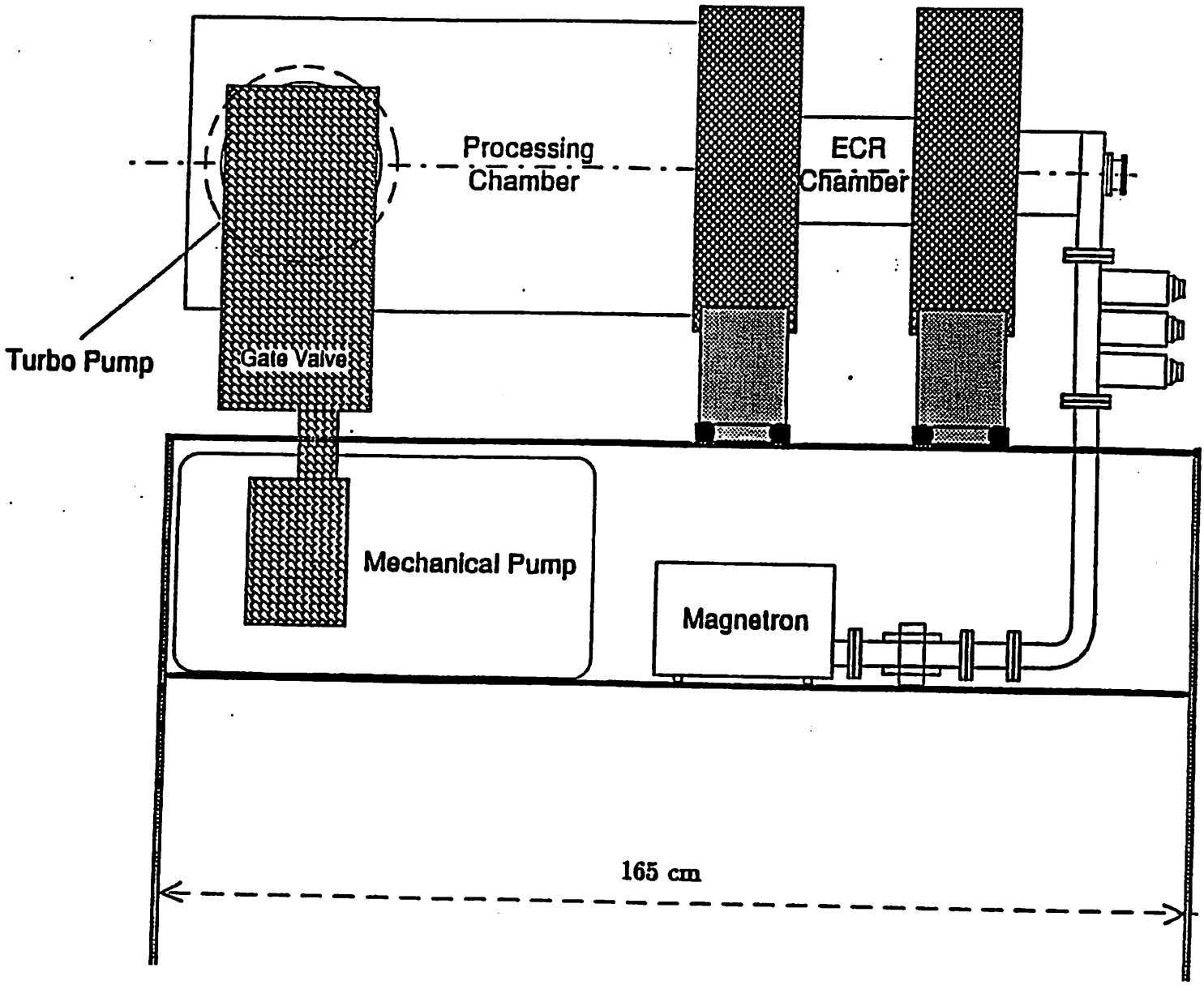
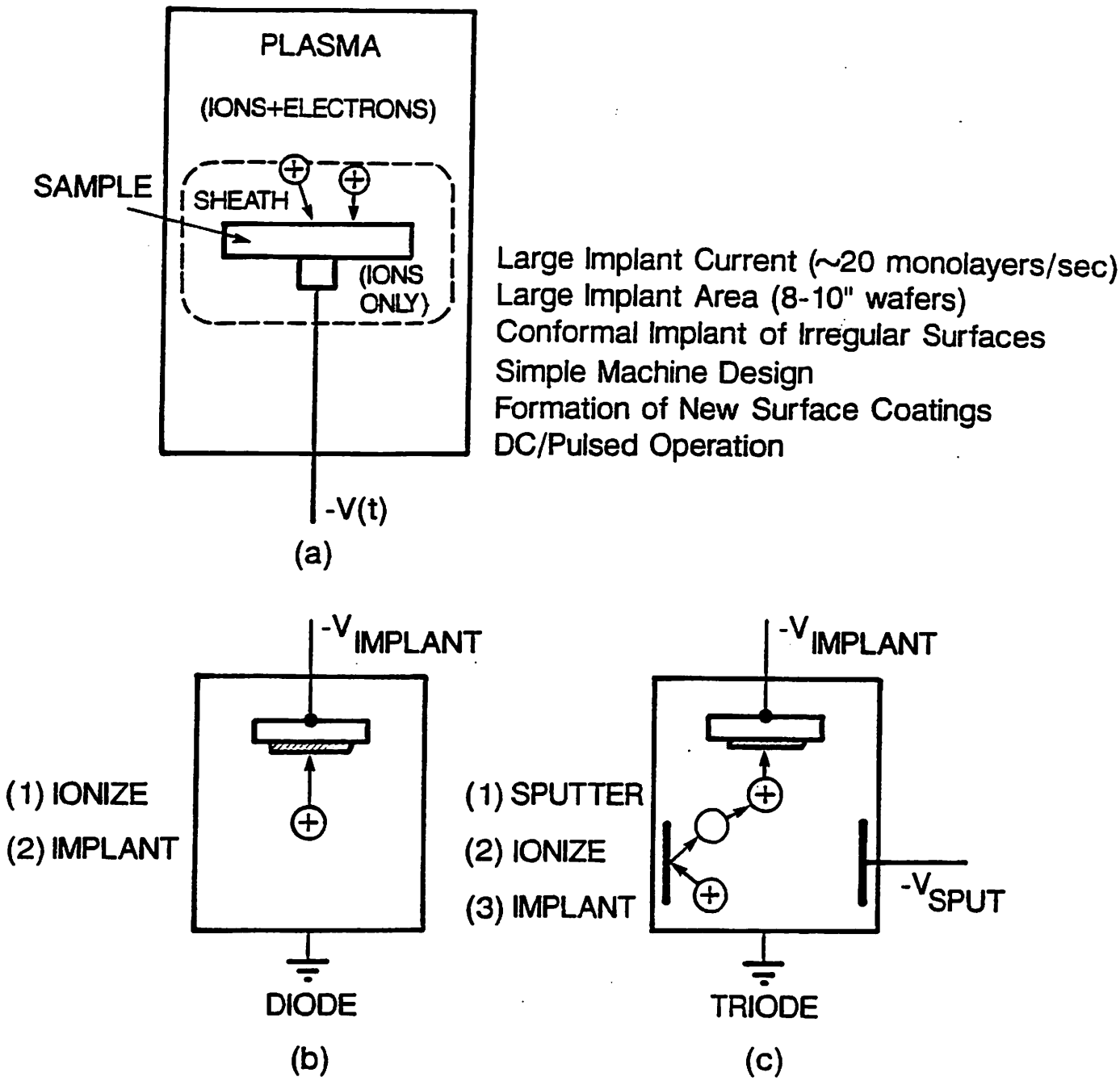


Fig. 1: Schematic side view of the PIII Reactor



Scale: 1/10 (1 cm ⇒ 10 cm)

Fig. 2: Scaled Diagram of the PIII Reactor



Figs. 3 (a), (b), (c): Unique Features of PIII

I. INTRODUCTION

Ion implantation is an important technique in integrated circuit fabrication. Due to the continuing trend toward smaller, faster and more densely packed circuitry, conventional ion implantation technology faces several challenges. Two major challenges are throughput, which is limited by the available ion current, and the production of very low energy ion beams for shallow implants. Other important concerns include charging, channeling, shadowing and damage.

An alternative to conventional ion implantation that may eliminate several of the above problems is *plasma immersion ion implantation* (PIII). We have successfully applied PIII to semiconductor device fabrication for a number of VLSI applications including sub–100 nm p+/n junction formation, conformal implantation for trench doping, and palladium seeding for electroless Cu plating. The PIII process is illustrated in Figs. 1-3.

Ions that are created in an electron cyclotron resonance (ECR) plasma source, diffuse into a process chamber where they are extracted directly from the process plasma in which the wafer holder is located (Fig. 1). The substrate holder is biased to a high negative voltage (either pulsed or DC) and the ions are accelerated to the wafer through a high-voltage plasma sheath (Figs. 3a, 3b). Since the ion energy is controlled by the applied voltage, very low energy implants ($\leq$ 1 keV) are possible. In addition, since PIII operates with an ECR plasma discharge, a range of pressures from 0.1–100 mTorr may be used. Thus, the angular distribution of the implanted ions can be adjusted simply by varying the gas pressure. This feature is very attractive for conformal doping of nonplanar surface topographies such as high-aspect-ratio trenches.

PIII can also operate in a triode (Fig. 3c) by introducing a sputtering target near to or within the ECR source chamber. The sputtering rate can be controlled by applying a suitable bias to the target. This technique provides the capacity of implanting any solid material into the substrate as long as the material has reasonable sputtering and ionization rates. In addition, dual ion implantations of both the

source and sputtered atomic species can be achieved by varying the target and wafer holder biases.

Several features of PIII make it an attractive alternative to conventional ion implantation. With the high current capability of PIII, the throughput of present integrated circuit steps can be substantially increased. Also, the intermediate step of the ion source and all of its support equipment is completely eliminated, leading to a simple reactor design that is compatible with the cluster tool concept.

The PIII program at Berkeley in 1990-91 is supported by a $70,000 cash and $15,000 in-kind grant from Applied Materials, Inc., and a $140,000 contract from the State of California Office of Competitive Technology. The goal of the project is to transfer the PIII process under development at Berkeley to Applied Materials, Inc.

The three critical issues for transfer of the PIII technology to Applied Materials are:

A. Process Demonstration. Demonstrate PIII processes that are more cost effective than conventional ion implantation.

B. Process Integration. Demonstrate PIII process compatibility with conventional IC processes to fabricate a complete integrated circuit.

C. Reactor Demonstration. Demonstrate a reactor that meets the required process uniformity and lack of oxide breakdown over a 200 mm wafer.

To address the first critical issue, three processes are being developed to demonstrate PIII superiority over conventional ion implantation: (1) We have demonstrated the formation of 800 angstrom thick pn junctions with leakage currents less than 25 nA/cm^2 and low interfacial defect densities, comparable to the best commercial pn junction fabrication processes. The process consists of a 10kV SiF_4 pre-amorphization PIII implant followed by a 5kV BF_3 boron implant, followed by a one second rapid thermal anneal to activate the dopant (see Fig. 4). However, an obstacle to pn junction fabrication is condensation of BF_3 polymer, which interferes with both the implant and the measurement of implant dose. Safety considerations preclude our using di-borane (B_2H_6) or any arsenic or phosphorous-containing gases in our laboratory at Berkeley. Reduction of BF_3 condensates is described in Sec. II, and is currently one thrust of our work on pn junction formation. Electrical characterization of pn junction devices is also under way.

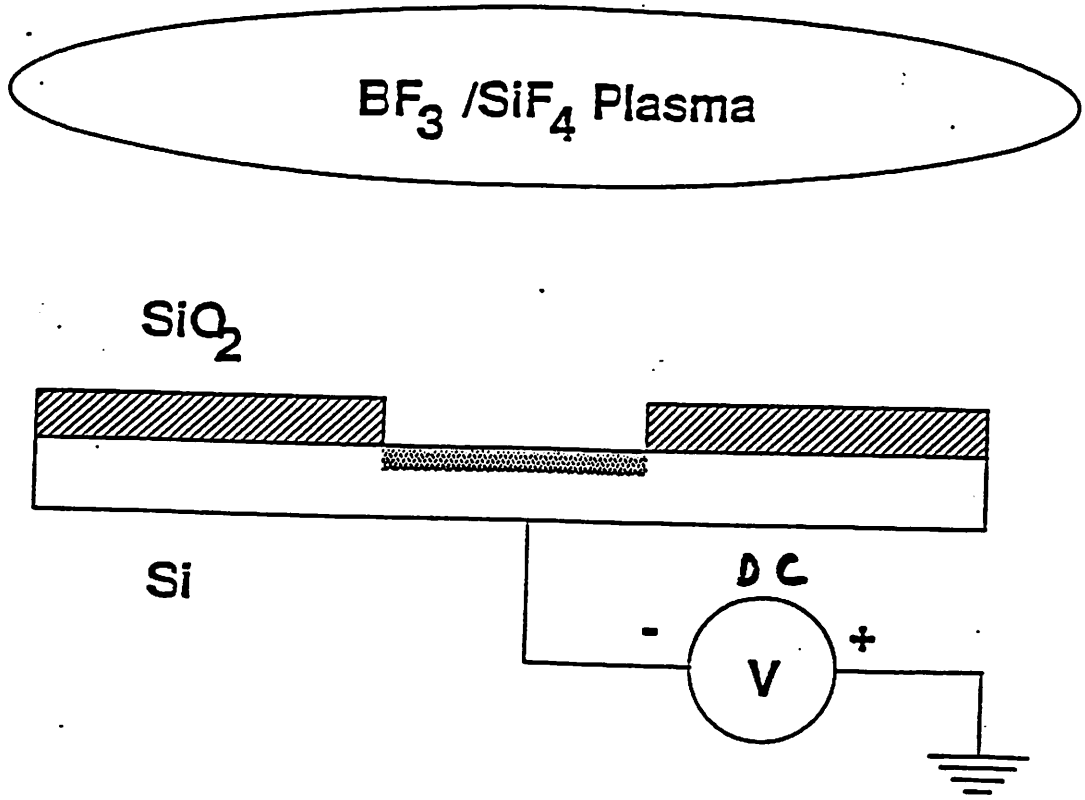


Fig. 4: PIII Shallow P+/N Junction Fabrication Process

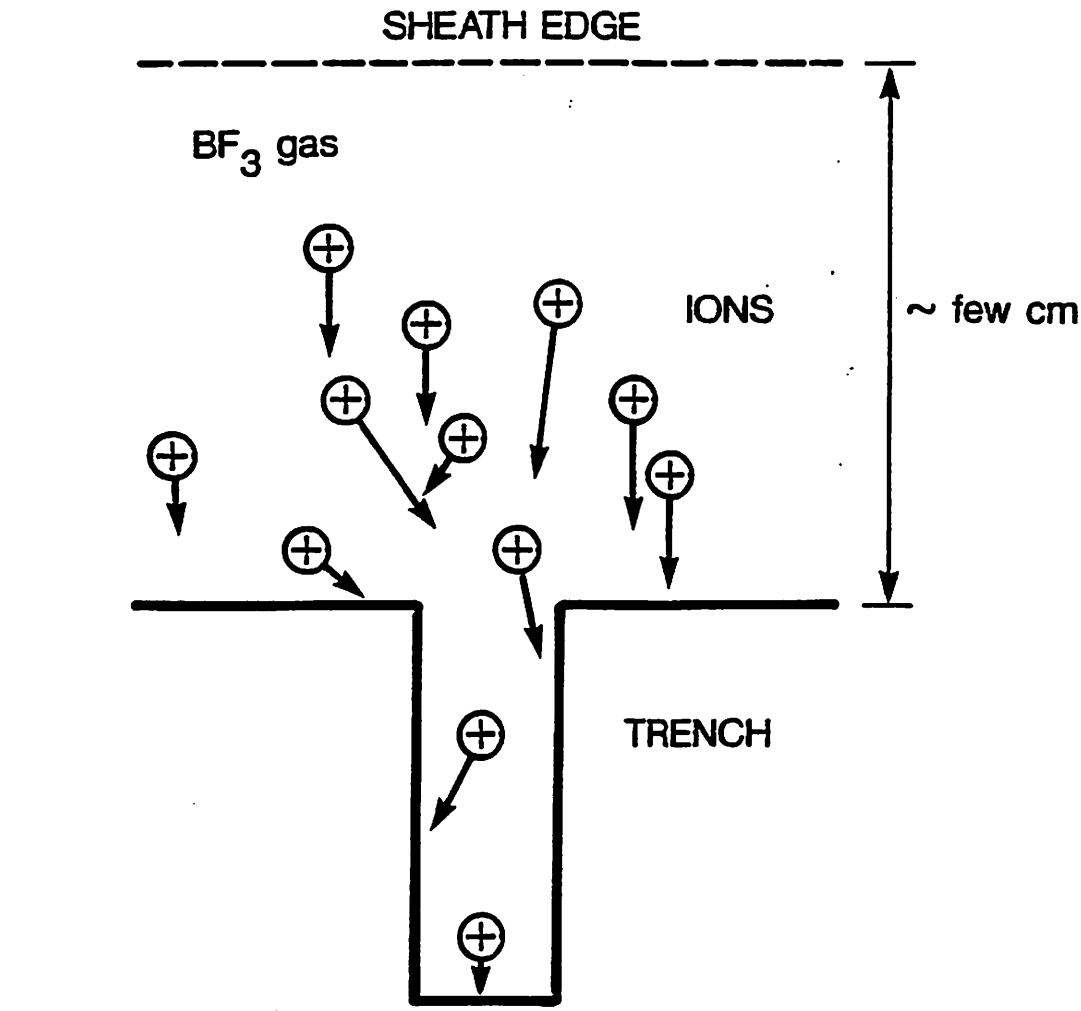
The second process being developed is conformal doping of trenches for trench capacitor or trench isolation. We have demonstrated conformal doping of trenches using a high-pressure (~5 mTorr) BF_3 PIII process (Fig. 5), with the doping boundary delineated by a crude staining technique (Fig. 6). As described in Sec. III, we are refining our staining technique to delineate simultaneously a number of equiconcentration contours.

The third process being developed is the formation of a metal seed layer for selective, electroless copper plating of oxide trenches. This process, which is a demonstration of the triode PIII configuration (see Fig. 3c), is described in Sec. IV.

To address the second critical issue (Process Integration) and part of the third critical issue (Oxide Breakdown), we are developing a complete PIII processing compatibility test chip to investigate wafer charging as a cause of oxide breakdown and the use of poly-silicon as a p+ doping source. The test chip will be a PMOS process including inverters and ring oscillators, in which PIII will be used for at least two of the process steps. The complete chip is being designed and simulated and will be fabricated at Berkeley. Capacitor breakdown tests will be performed on the test chip, as described in Sec. V.

To address the remainder of the third critical issue (Process Uniformity), we are using analysis, computer simulation, and experiments to model the formation of the PIII process plasma, its injection into the process chamber, and the actual implantation process itself. We have developed a model of the implantation for pulses with finite rise- and fall-times. We have developed a 2D simulation code to model the injection of the source plasma into the process chamber. We have begun experiments using a multidipole plasma confinement system on the process chamber to achieve implant uniformity over a wide range of pressures and ECR source powers. This work is described in Sec. VI.

The milestones are shown in Fig. 7. The Month 1 Milestone was met ahead of schedule, as described in *Electronics Research Laboratory Report UCB/ERL M90/100*, 12 November 1990, entitled "Characterization of the Processing Plasma in an Engineering Prototype Reactor for Plasma Immersion Ion Implantation". The highlight of that report is the achievement of ± 5% plasma uniformity over a 200mm wafer at one particular power and pressure in argon gas.



PRESSURE	λm	
10^{-5}t	8m	
10^{-4}t	80cm	
10^{-3}t	8cm	OPERATING
10^{-2}t	8mm	PRESSURE

Fig. 5: Conformal Trench Doping

- 10 kV
- 200 mC
- 5 mT

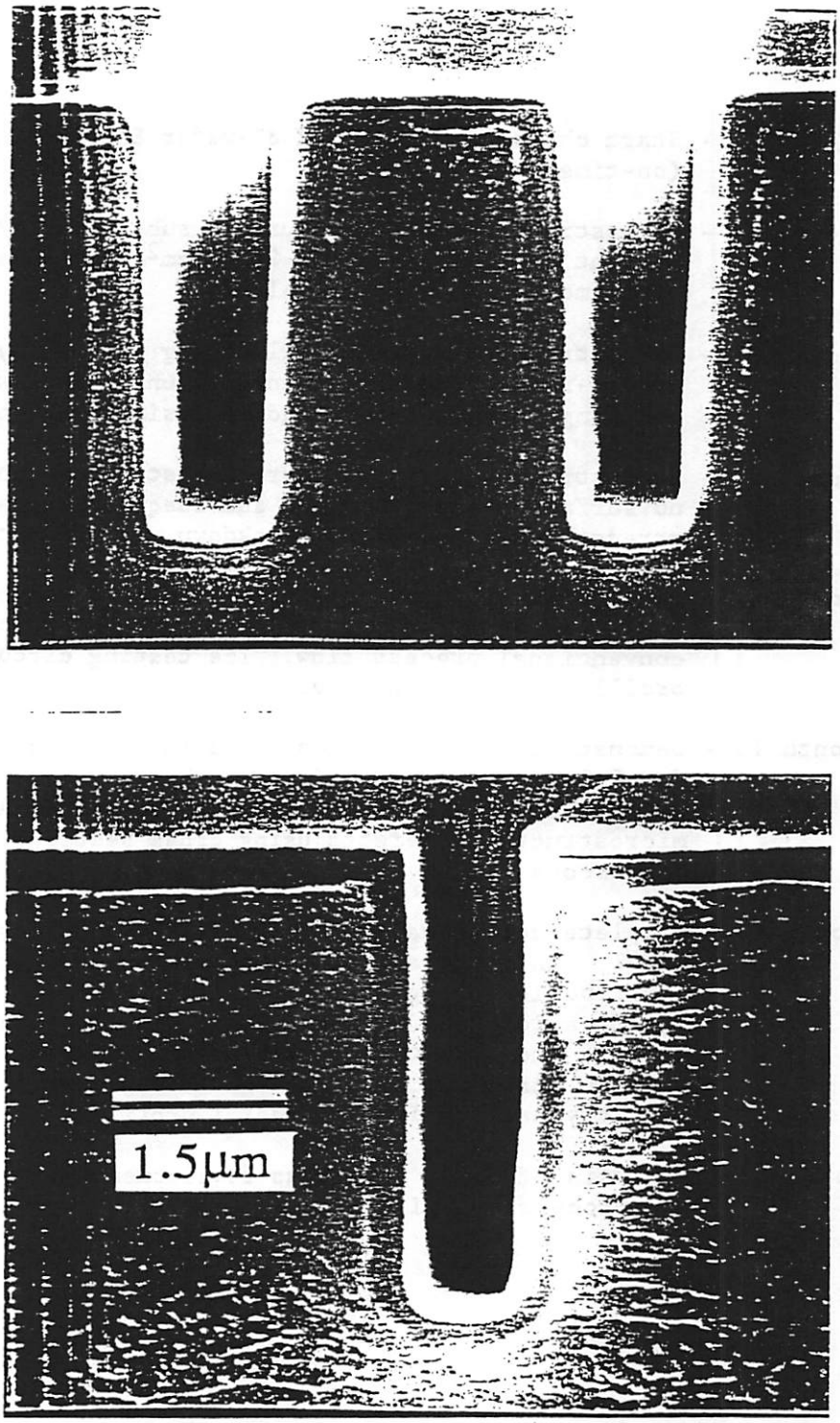


Fig. 6: PIII BF_3 Doped Trenches

Month 1 - Start characterization of 8"-wafer Engineering PIII Reactor. (on-time)

Month 3 - Demonstrate low leakage current sub-100nm p+/n junctions with current density less than 25 nA/cm^2 at a reverse bias of -5V. (goal met on November 15, 1990)

Month 5 - Demonstrate trench sidewall doping uniformity to $\pm$ 50% for 7:1 aspect-ratio trenches. Junction uniformity will be measured by staining methods and spreading resistance measurements.

Month 8 - Demonstrate electrical characteristics of doped trenches showing no surface state inversion and adequate oxide breakdown strengths using C-V and breakdown measurements.

Month 9 - Completion of a testing integrated circuit using PIII for sub-100nm junction formation to show compatibility with conventional process flow. The testing circuit will be a ring oscillator or an inverter.

Month 10 - Demonstrate planarization of Cu interconnects using PIII seeding for 2:1 aspect-ratio oxide trenches. Verify electromigration reliability and adequate adhesion to oxide, and examine microstructural defects using cross sectional scanning electron microscopy.

Month 12 - Complete collisonal modeling of PIII and first-order 2-D PIII model. Includes analytical model of ion energy and angular distribution along with particle-in-cell computer simulation verification, ion current versus time for realistic PIII pulse shapes, and analytical and static 2D simulation of plasma density distribution in a magnetic bucket process chamber geometry and ion implant radial profiles.

Month 12 - Analysis of Phase I process development progress. Fine tuning for process optimization.

Fig. 7: Milestones

The Month 3 Milestone was met ahead of schedule. A manuscript describing the excellent low leakage properties of the junctions has been submitted for publication to *Applied Physics Letters*. The results are at least as good as those achievable using any other commercial process.

The Month 5 Milestone is due on 18 May 1991 and has not been met. There has been some delay in obtaining trenches from Applied, but these problems have been solved. Nevertheless, achieving this milestone may be delayed somewhat, due to the late start, the required development of a new staining method, and the as yet unknown side wall doping uniformity provided by the PIII process.

A good start has been made on Month 8, 9, 10 and 12 Milestones. At this time, there are no anticipated delays in meeting these milestones.

II. SHALLOW PN JUNCTION IMPLANTS USING BF_3

The condensation of BF_3 is proving to be the primary obstacle to fabricating pn junctions (see Fig. 8). This condensate interferes with both the actual implantation and the measurement of implant dose.

The principal drive in our work is to demonstrate the viability of creating pn junctions using the PIII process. For safety reasons only BF_3 has been considered as a doping source gas. In our process BF_3 is ionized and subsequently implanted into n-type Si wafers. The implantation of the pedestrian fluorine atoms is believed to be noninterfering to our results. After B implantation the wafers are annealed to activate the boron in the wafers. The sheet resistances of these wafers are then measured and the implanted B dose is extracted.

Two mechanisms exist for the introduction of B into the Si wafers: implantation and surface adsorption. The sheet resistance properties are indistinquishable with respect to these two mechanisms after annealing. Unfortunately, the amount of B from surface adsorption can be as high as a dose of $10^{15}/cm^2$ or more and can overwhelm the intended implantation doses at or below $10^{15}/cm^2$.

We have tested the effects of various plasma parameters in an attempt to circumvent surface adsorption of BF_3 during PIII processing. Parameters changed were BF_3 gas pressure and the ionizing microwave power. The growth of the BF_3 condensate was then measured as a function of processing

Problem: Implant Gas Forms B-F Compound

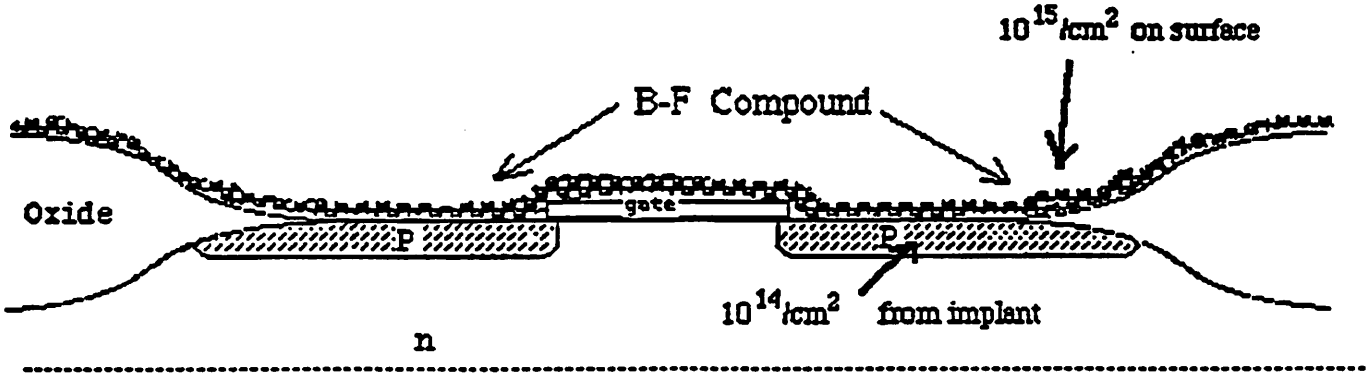


Fig. 8: Condensation of B-F Compound in BF_3 PIII

time using ellipsometry to quantify the growth and optical microscopy as a general inspection tool. We find that the condensate growth properties are characterized by a nucleation and growth phenomena. The nuclei grow as large as 10μm (Fig.9). The growth of the condensate is plotted in Fig. 10 using the same index of refraction as SiO_2. The net condensate is seen to increase with time for a processing pressure of 1 mTorr. This is presumably due to the increased surface area that BF_3 adheres to after its initial nucleation. By lowering the processing pressure to 0.8 mTorr or below, the film growth is avoided. This is best reflected in the change of sheet resistance contours of the annealed wafers.

While we have demonstrated that BF_3 can be implanted without disruption from a surface condensation layer, the properties of the plasma as a function of pressure and power have proven to be variable for identical processing conditions. At present we are unable to control the surface condensate problem for this reason. Alternative approaches will be tested in the near future. One alternative is to heat the wafer holder to 70°C during processing. This should avoid BF_3 condensation as demonstrated by manufacturers (Applied, Varian) of conventional ion beam implantation equipment and allow implantation to proceed unperturbed. However, we expect the chamber to become coated with BF_3 at the source region. This may be addressed later. A second alternative is to mix H_2 with BF_3 during processing. This should interfere with the layered growth by allowing the H_2 to passivate reactive sites to which the BF_3 adheres.

In addition to studies of BF condensation, the work in progress includes the ongoing fabrication of new sets of p+/n diodes to test the amount and causes of leakage current in the devices. We have devised a new test structure to minimize the leakage of the diodes. This structure uses local oxidation to lower the curvature of the junction interface, which will raise the breakdown voltage of the diode. Also, large area diodes are being fabricated to minimize the effect of peripheral leakage on the measured current. The mask set includes sets of diodes with equal areas and varying perimeters so that the leakage due to edge and bulk effects may be differentiated and analyzed.

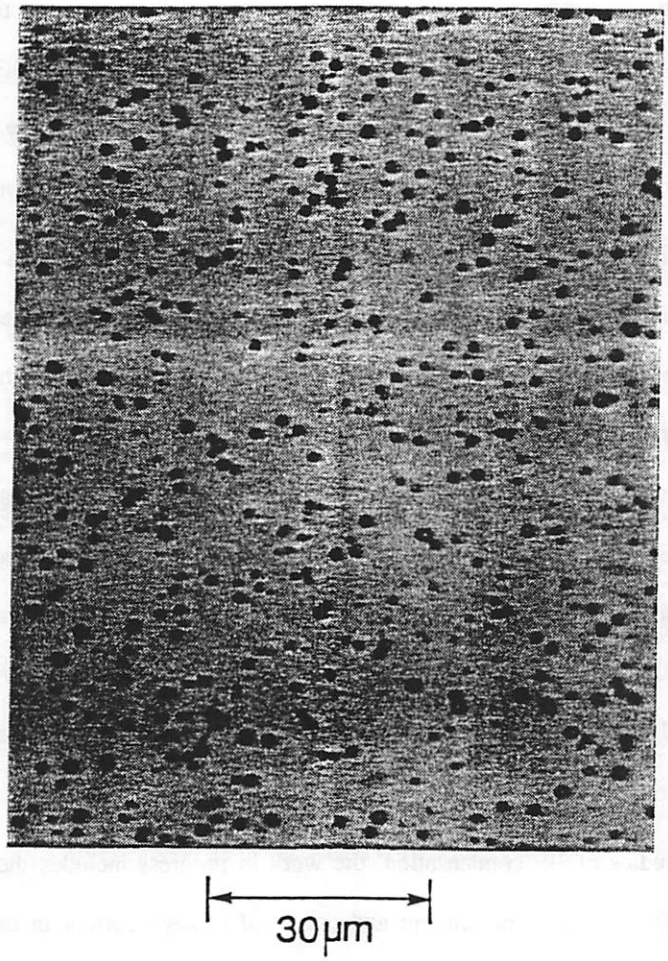


Fig. 9: BF_3 Polymer Formation

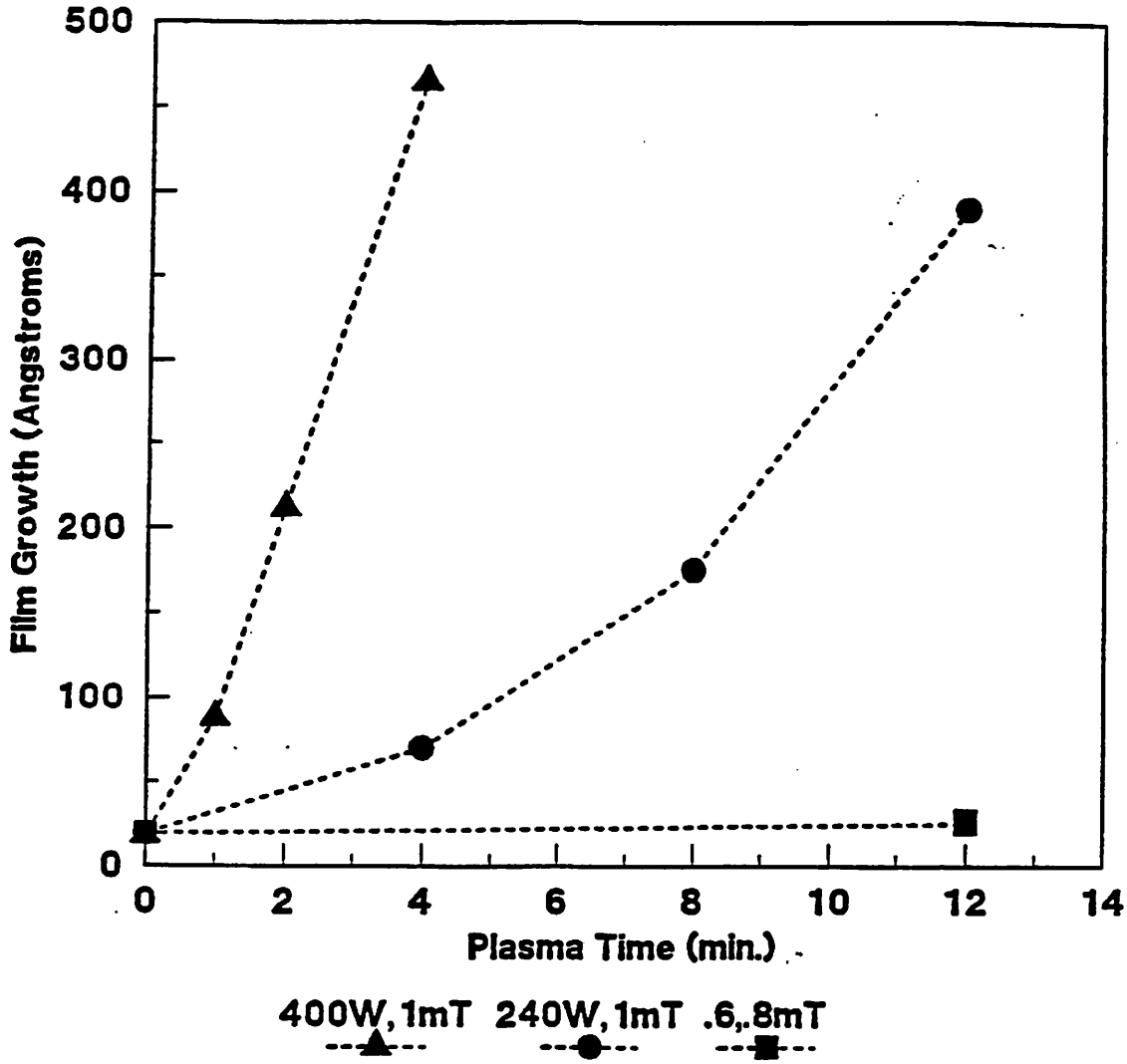


Fig. 10: B-F Compound Growth Vs. Plasma Conditions

III. 2-D DOPANT DELINEATION FOR PIII TRENCHES

PIII can be used to conformally implant trench structures. Currently, there is no convenient way of characterizing the two-dimensional dopant distribution of implants. Conventional electrical means are best suited for implants into flat topography with the concentration of dopants varying in one direction only. Although some electrical means, such as CV measurements, can be adapted to extract some information about implant profiles and dose in trench structures, these methods involve complicated numerical data processing and the accuracy of the results is limited.

We are developing a technique which will selectively delineate equiconcentration contours in sample cross-section. Originally reported by Gong ("Simulation of Lateral Spread of Implanted Ions: Experiments", *ESSDERC '89*, Berlin), this technique uses HF (50%), HNO_3 (70%), and CH_3COOH (100%). Under strong white light, a two-step reaction occurs which is responsible for selectivity: (1) $Si+2O \rightarrow SiO_2$ and (2) $SiO_2 + 6HF \rightarrow SiF_6^{2-} + 2H_2O + 2H^+$. For low resistivity silicon, (1) is much faster. Thus, the difference in etch rates yields equiconcentration contours which can be observed under SEM. We have been able to consistently reproduce a contour at approximately $6x10^{16}/cm^3$. This technique is being refined to yield a higher concentration contour at $1.5x10^{19}$. Eventually, this technique could be used in conjunction with a pn junction stain and yield up to 3 contours on one sample.

An angle-lapping technique has been developed to enhance the delineation technique. Polishing the cross section of the samples at an angle effectively magnifies the surface. Using a 1 degree lapping angle, approximately 50x magnification can be achieved. By this technique, the dose uniformity of PIII trench implants can be verified. With more refinement and the delineation of more contours, the two-dimensional implanted dopant distribution can be extracted.

IV. METAL SEED LAYER FOR ELECTROLESS COPPER PLATING

In its application to VLSI processing, PIII is used to form the seed layer for selective Cu plating of interconnects. Fig. 11 shows the process sequence: (1) one μm thick oxide is grown by wet oxidation, followed by photoresist patterning and reactive ion etching to make trenched patterns; (2) implant metal ions and then remove the photoresist that acted as the mask for implantation in this step; and, (3)

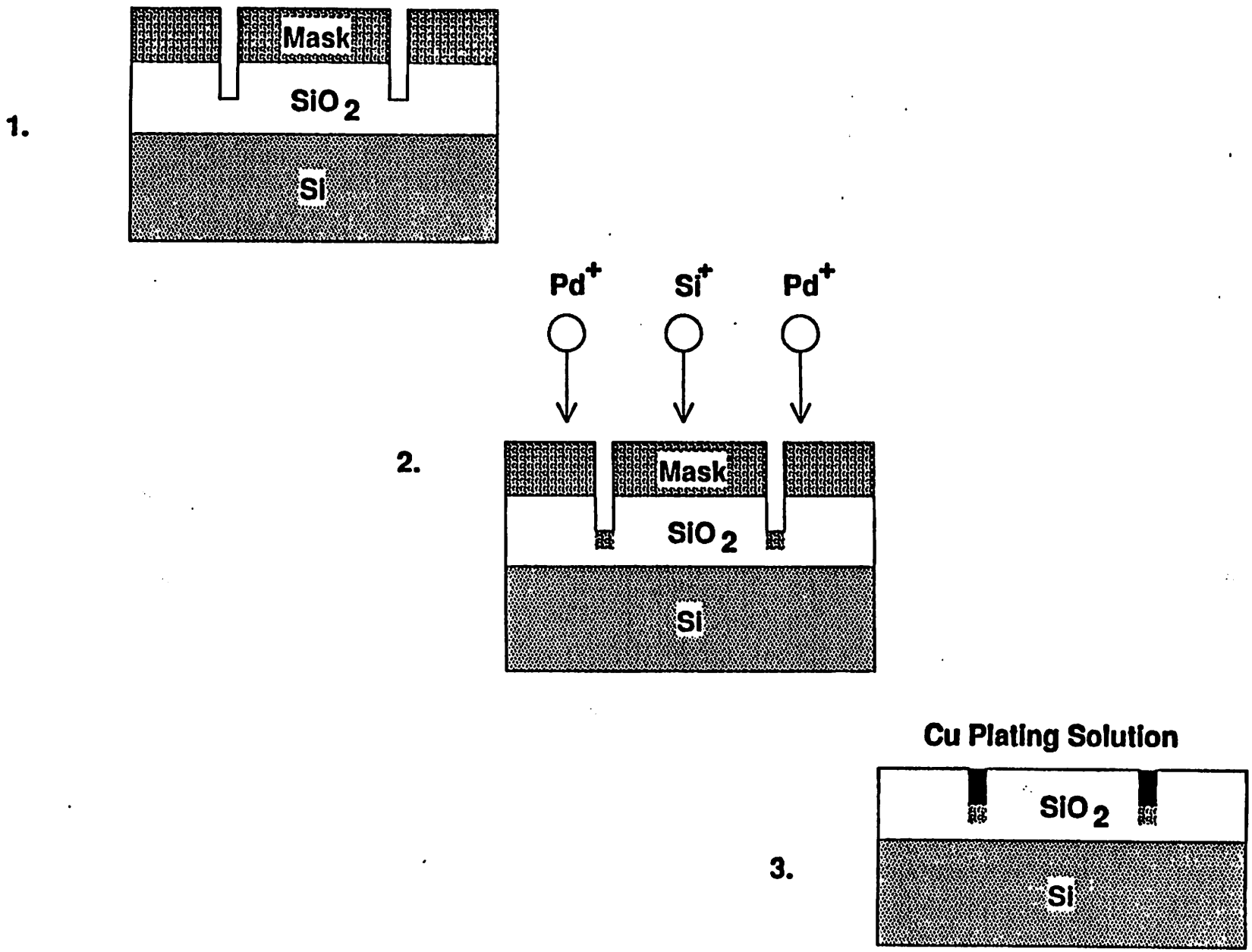


Fig. 11: Process for Selective, Electroless Copper Plating

immersion of the patterned wafers into electroless Cu plating solution to fill up the oxide trenches.

We have first conducted studies on material properties in order to choose the implantation species. We found Pd, Cu, Co, Ni, and Pb can all act as the catalyst needed for electroless Cu plating. There are also some other elements such as Pt, Au, Ag, Fe etc. that are reportedly able to seed Cu plating. Elements with lower electronegativities, including Cr, Ti, W, and Si, can not function as the catalytic seed. We have chosen Pd as the first seed material to study. In addition, some silicon is included in the sputtering target to improve the adhesion of plated Cu lines to the oxide substrate.

Shown in Fig. 12 is a schematic of the plasma immersion Pd ion implanter developed in our lab at U.C. Berkeley. A Pd/Si target is introduced into the electron cyclotron resonance (ECR) Ar source plasma. Sputtered Pd and Si atoms are ionized in the Ar plasma. A pulsed negative bias applied to the Si wafer downstream of the plasma accelerates the ions, and the ions are thus implanted into the substrate.

A threshold Pd dose at 3–4 x $10^{14}/cm^2$ was found necessary for Cu plating to occur (Fig. 13). Using this process, continuous Cu films were obtained, as seen in the SEM picture of Fig. 14. The plated trenches were 2 μm in width and the thickness of the Cu films was around 2000 Å. Further studies on the implantation conditions and species are under investigation to improve the film quality and adhesion.

V. PROCESSING COMPATIBILITY TEST CHIP

A chip will be developed to test compatibility of PIII with other IC production processes. The chip is a PMOS version of an NMOS layout (see Fig. 15) that is used as an instructional laboratory test chip to teach IC fabrication techniques. Process simulation for fabricating this chip is currently under way. The chip will be used to demonstrate the use of poly-silicon as a p+ doping source, and to study wafer charging effects that can lead to oxide breakdown. For the latter, the PIII reactor will be used to implant argon at several different energies and the change in the capacitor threshold voltage will be measured.

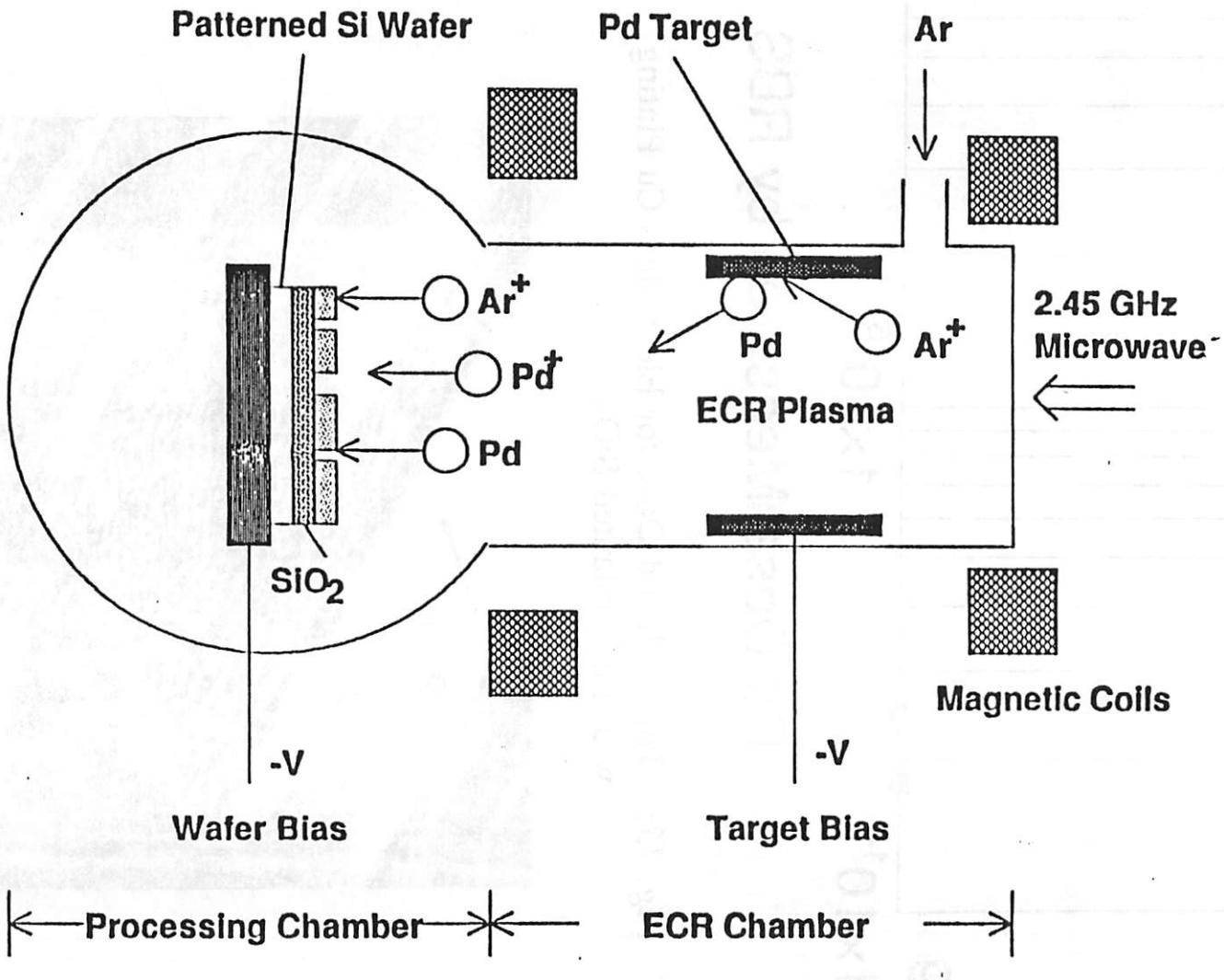


Fig. 12: Schematic of the Palladium, PIII Process

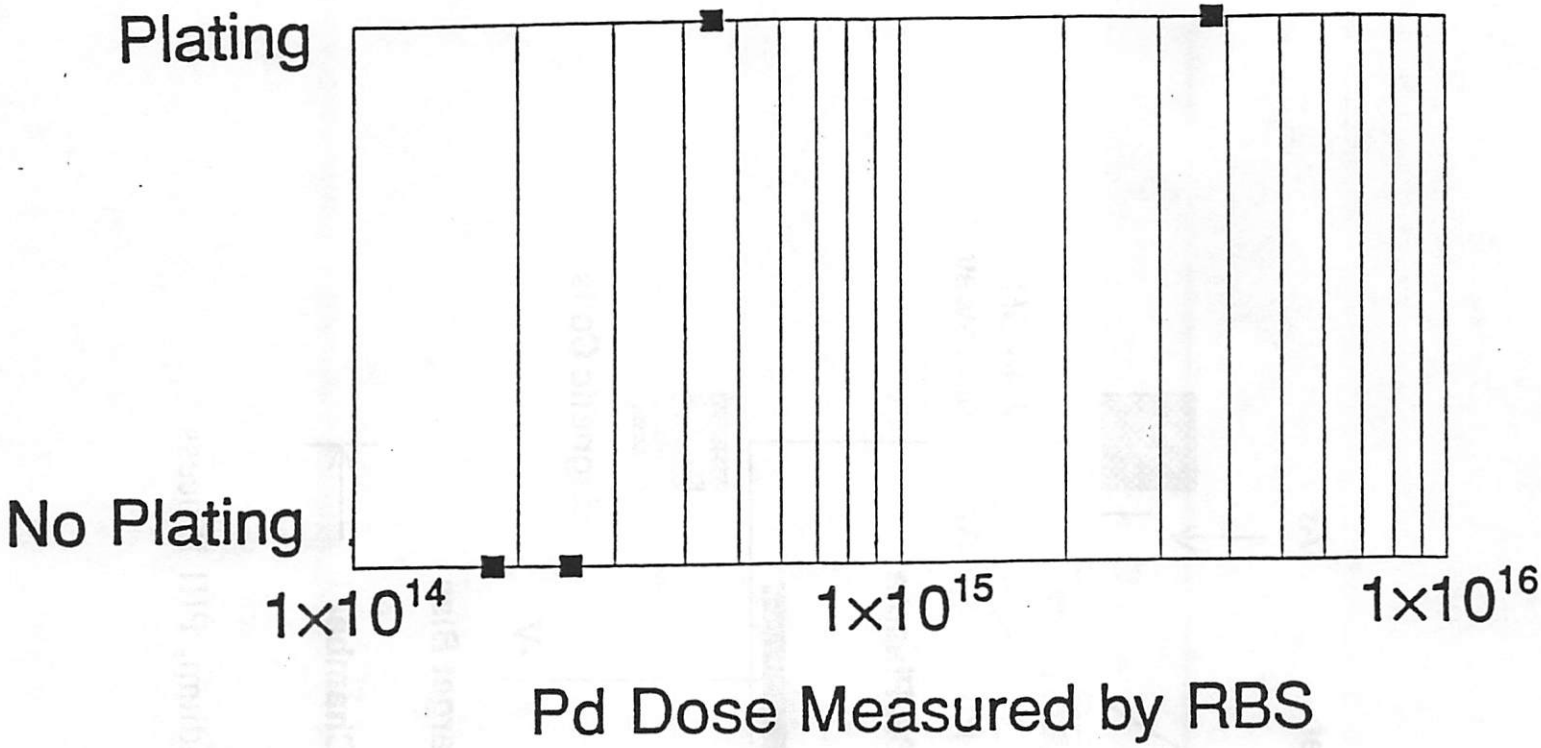


Fig. 13: Threshold Pd Dose for Electroless Cu Plating with Pd Implanted SiO_2

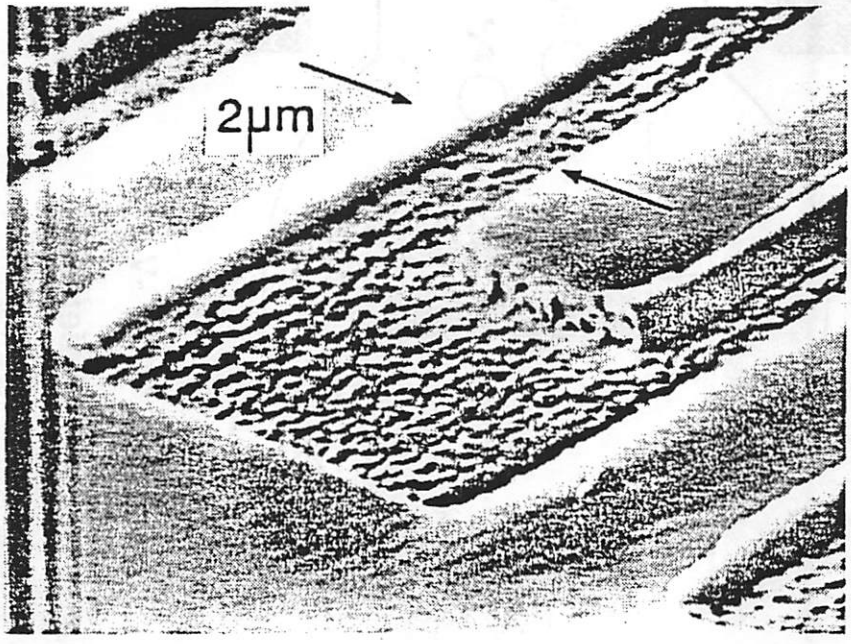


Fig. 14: SEM Showing Pd-seeded, Cu-filled SiO_2 Trenches.

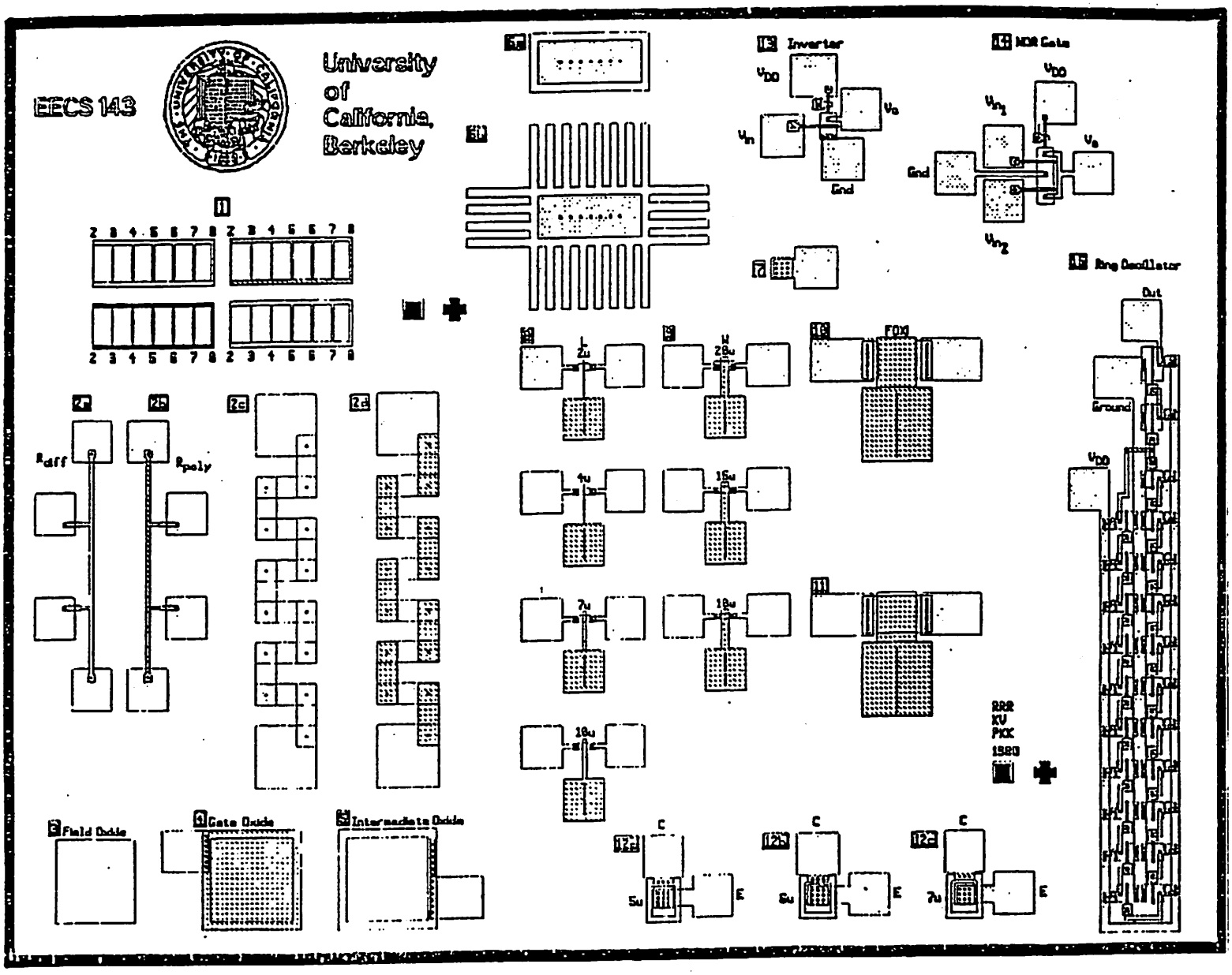


Fig. 15: PMOS PIII Processing Compatibility Test Chip

CV measurements have been completed on n doped p substrate capacitors using the HP 4140B pA ammeter and the 4280 CV analyzer to get both high frequency and low frequency measurements. We plan on implanting argon into the samples at varying energies to test the effects of implantation on the oxide. The dose, frequency and pressure will be held constant. We will especially be looking for breakdown due to charge buildup. Along with the different energy samples, we will be doing a DC implant to demonstrate that it causes oxide breakdown. As a control experiment, we will also expose a sample to the plasma without any bias, to test the plasma effects on capacitors. Theoretically, the plasma should not affect the sample unless a reverse bias is placed on the wafer (see Fig. 16).

To aid in studying the implantation, we have used a simple linear model of the dark space region between the plasma and the wafer (Fig. 17). With this model we can get an approximation of the voltages seen across the oxide.

VI. REACTOR DEMONSTRATION

Studies of the ion implantation process and the uniformity of the process chamber plasma are in progress. First, we have examined a model of plasma immersion ion implantation for voltage pulses with finite rise- and fall-times. The goal of this work is to develop an analytical description of the PIII process to aid in understanding the physics of the implantation and to provide a tool for designing implantation experiments. Desired information includes the time evolution of the implanted ion current, the energy distribution implanted ions, total implanted dose, and how these quantities scale with system parameters. The model accounts for voltage pulses with finite rise- and fall-times, as exist in real PIII experiments. The model calculates the sheath motion and implantation current $j(t)$ by assuming the quasistatic Child Law current is supplied by ions entering the sheath.

The energy distribution of dN/dW is calculated by keeping track of ions implanted with energy equal to the voltage across the sheath when the ion first enters the sheath, consistent with the frozen sheath assumption. Also calculated is f, the fraction of ions implanted with energy $W < W_{min} < V_o$.

Comparison of results obtained from the model is made with a numerical code developed by G. A. Emmert at the University of Wisconsin. The code numerically solves nonlinear partial differential equations for particle and momentum conservation, along with Poisson's equation. The electron density

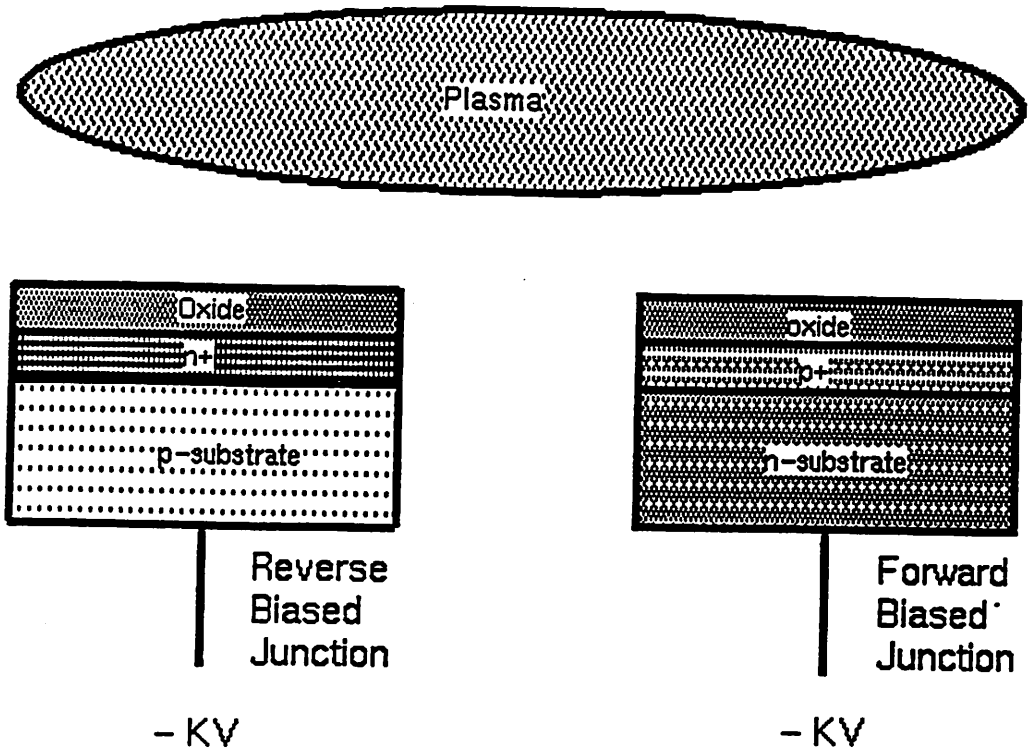


Fig. 16: PIII for N-on-P and P-on-N Substrates

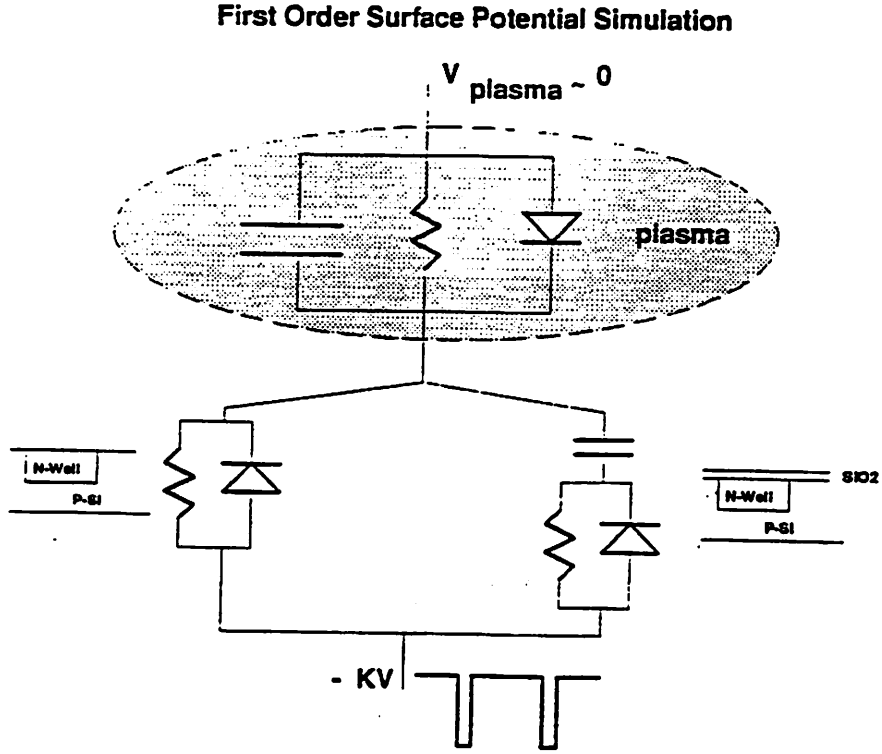


Fig. 17: Model of Wafer Charging Effects

is related to the potential by assuming that the electrons are in thermal equilibrium. The input waveform to the numerical code is trapezoidal with user-specified rise- and fall-times.

The accuracy of the model is characterized by a single parameter $\beta = t'/t_r$ where t' is the ion flight time corresponding to the instant $j(t) = j_{max}$ and t_r is the rise-time of the pulse. Fig. 18 compares the analytical model for $j(t)$ with the numerical code for a specific value of β and demonstrates that β characterizes the closeness of the fit. Comparison of f predicted by both the model and the numerical code is shown for a specific example in Fig. 19.

This work has been completed, as described in *Electronics Research Laboratory Report UCB/ERL* M91/94, 21 February 1991, entitled "Model of Plasma Immersion Ion Implantation with Finite Rise- and Fall-Times". The work has been submitted for publication in the *Journal of Applied Physics.*

A second study has been initiated to improve the process plasma uniformity by means of multidipole plasma confinement. Fig. 20 shows a typical PIII plasma source. The plasma from the ECR source streams into a cylindrical process chamber of radius R and length L in which the substrate (wafer) is located. Portions of the process chamber surface can be covered with permanent magnets to enhance the plasma uniformity near the wafer surface. These magnets can be arranged as a set of M linear multidipoles around the exterior cylindrical surface, and portions of one or both cylinder ends.

As a first step, we are studying the diffusion equation solution for a process chamber geometry as shown in Fig. 21. The plasma from the source is assumed to have a uniform radial profile $n(r) = n_0$ for $r < a$. The remaining part of the top face and the entire bottom face of the cylindrical chamber are assumed to have perfectly absorbing boundary conditions; the latter might model the wafer holder as well as the actual bottom face of the process chamber. Multidipoles are assumed to be arranged along the cylindrical sidewalls, leading to a mixed boundary condition at $r = R$.

Analysis of the solution with mixed boundary conditions will be made to gain insight into the scaling of the uniformity with parameters. The assumption of a uniform plasma source for $r < a$ will also be relaxed to see the effect of a nonuniform source on the uniformity.

A code is being developed to solve the two-dimensional (r,z) diffusion equation

$$\nabla^2 n + k^2 n = G$$

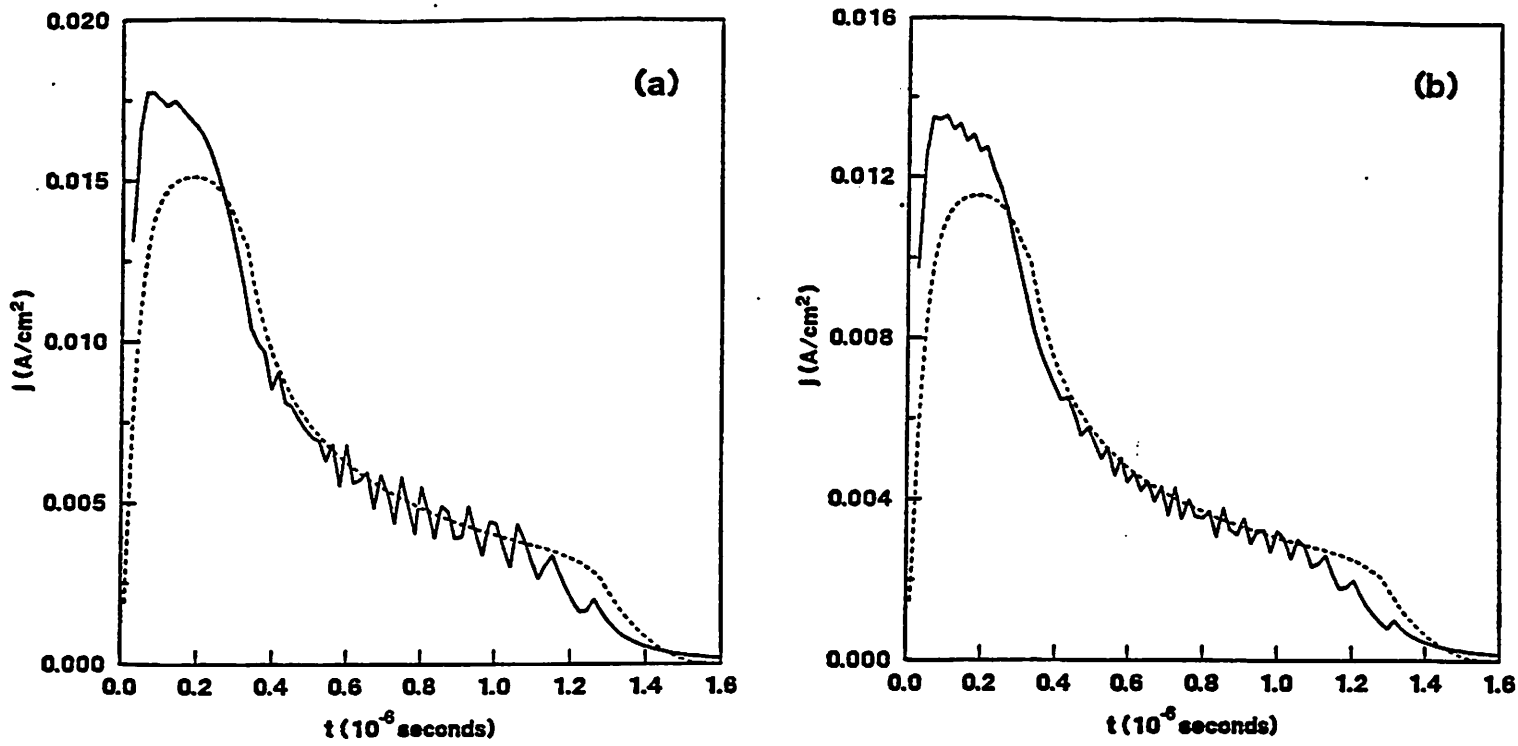


Fig. 18: Current density versus time for $\beta = 0.5$, $V_o = 30$ kV, $t_r = 0.2$ μs, $t_p = 0.8$ μs, $t_f = 0.3$ μs, and (a) $n_o = 1.7 \times 10^{10}$ cm^{-3}, $M = 40$ amu; (b) $n_o = 10^{10}$ cm^{-3}, $M = 24$ amu (— numerical solution; --- analytical solution).

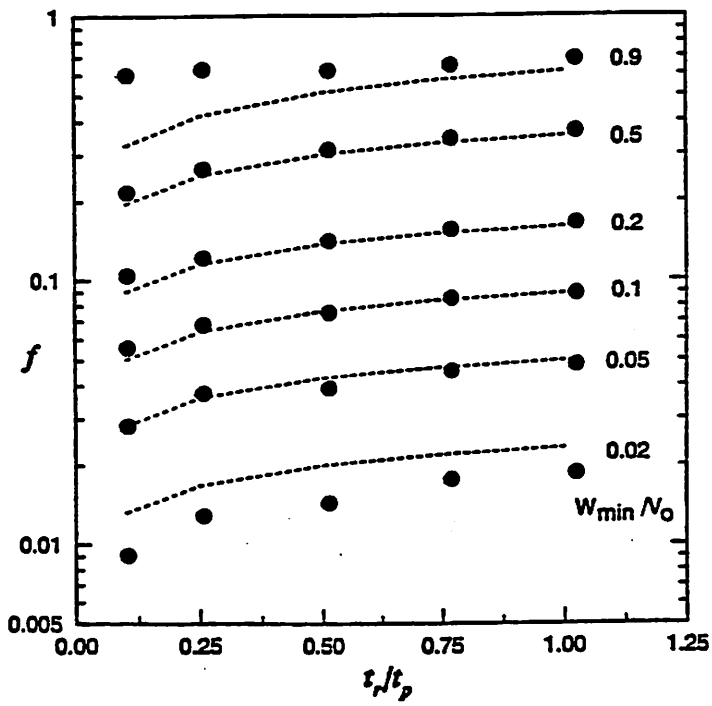


Fig. 19: Fraction f of ions hitting the target with energies $W < W_{min}$ versus t_r/t_p, with W_{min}/V_o as a parameter, for the example of $t_r = t_f$, $t_r + t_p = 1.0$ μs, $V_o = 30$ kV, $n_o = 10^{10}$ cm^{-3}, and $M = 40$ amu (• numerical solution; — analytical solution).

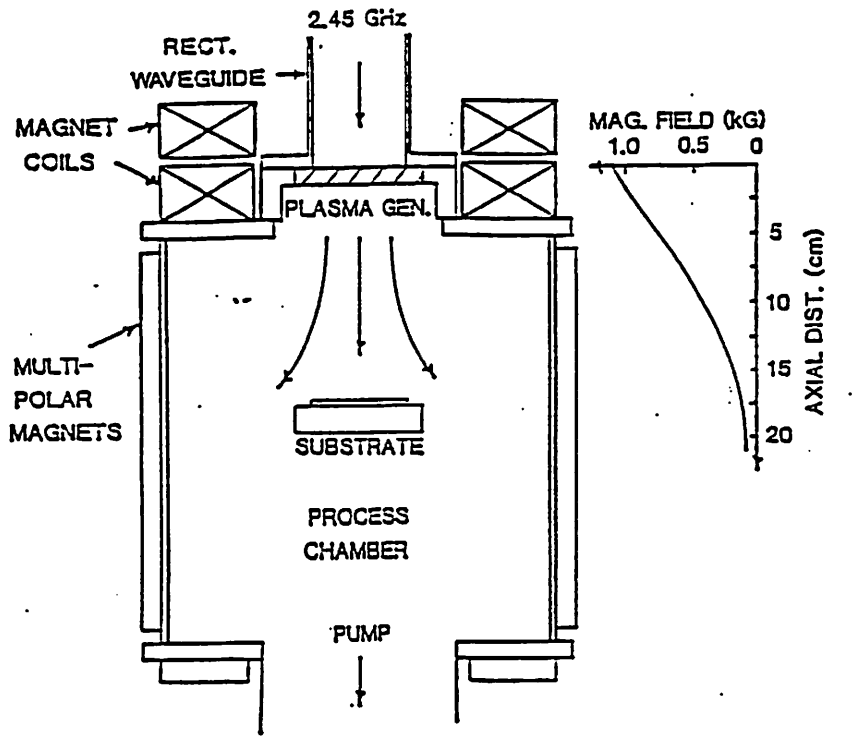


Fig. 20: Schematic of Multidipole Confined ECR Reactor

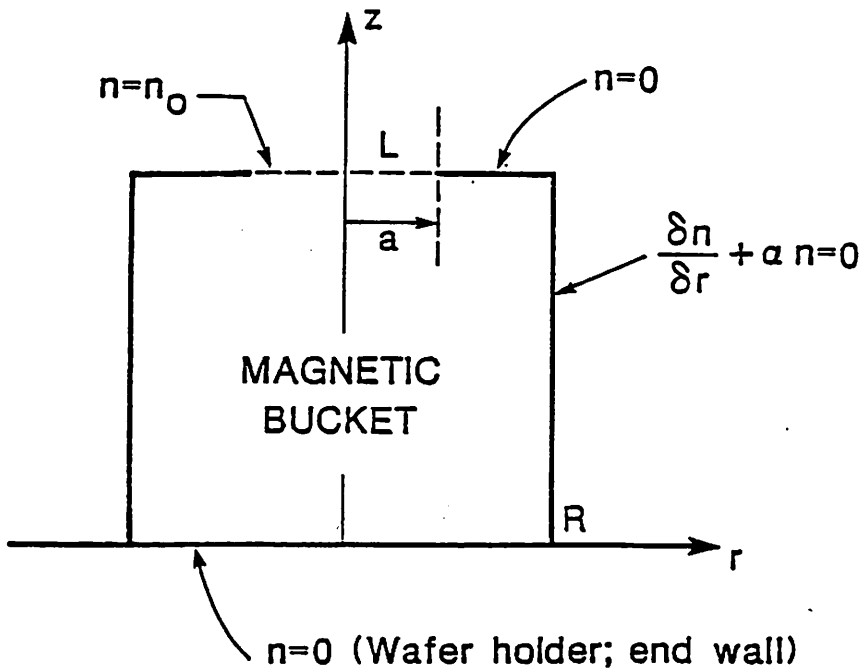


Fig. 21: Analytical Model of Multidipole Confinement

where $k^2(r,z)$ accounts for plasma electron-neutral ionization within the source chamber and $G(r,z)$ accounts for hot electron-neutral ionization (if present). The full range of boundary conditions from $n = 0$ to $\nabla n = 0$ to mixed boundary conditions will be accommodated on both top and bottom faces and cylindrical side walls of the process chamber. Provision is made for a wafer holder within the process chamber having arbitrary size, shape and boundary conditions. These conditions allow a reasonably accurate determination of plasma properties within the process chamber, even in the very low pressure regime for which the ion mean free path $\lambda_i \sim R, L$, when the wafer holder within the chamber strongly perturbs the solution, and when there is ionization within the process chamber itself.

The 6" diameter ECR source injects plasma into an 18" diameter, 30" long process chamber having a variable position, 11" diameter wafer holder (see Fig. 1). The process chamber has been equipped with a set of linear multidipole magnets, and preliminary measurements of axial and radial plasma density have been performed using Langmuir probes in argon gas. The objective of this work is to characterize the plasma density, confinement and uniformity for this particular chamber, wafer holder system, and range of gas types. We plan to correlate these measurements with both the analytical modeling and the results of the computer simulation code.

VII. PUBLICATIONS AND TALKS

1. M.A. Lieberman, "Model of Plasma Immersion Ion Implantation", *J. Appl. Phys.* 66, 2926 (1989)

2. V. Vahedi, M.A. Lieberman, M.V. Alves, J.P. Verboncoceur and C.K. Birdsall, "A One Dimensional Collisional Model for Plasma Immersion Ion Implantation", to appear in *Journal of Applied Physics* 1990.

3. X.Y. Qian, D.A. Carl, J. Benasso, N.W. Cheung, M.A. Lieberman, I. Brown, J.E. Galvin, R.A. MacGill and M.I. Current, "A Plasma Immersion Ion Implantation Reactor for ULSI Fabrication", *Nuclear Instrument and Methods*, (1990).

4. X.Y. Qian, N.W. Cheung, M.A. Lieberman, M.I. Current, P.K. Chu, W.L. Harrington, C.W. Magee and E.M. Botnick, "Sub-100nm P+/N Junction Formation Using Plasma Immersion Ion Implantation", *Nuclear Instrument and Methods*, (1990).

5. X.Y. Qian, N.W. Cheung, M.A. Lieberman, R. Brennan, M.I. Current and N. Jha, "Conformal Implantation for Trench Doping with Plasma Immersion Ion Implantation", *Nuclear Instrument and Methods*, (1990).

6. X.Y. Qian, M.H. Kiang, J. Huang, D.A. Carl, N.W. Cheung, M.A. Lieberman, I.G. Brown, K.M. Yu and M.I. Current, "Plasma Immersion Pd Ion Implantation Seeding Pattern Formation for Selective Electroless Cu Plating", *Nuclear Instrument and Methods*, (1990).

7. X.Y. Qian, M.H. Kiang, I. Brown, N.W. Cheung, X. Godechot, J.E. Galvin, R.A. MacGill and K.M. Yu, "Metal Vapor Vacuum Arc Ion Implantation for Seeding of Electroless Cu Plating", *Nuclear Instrument and Methods*, (1990).

8. N.W. Cheung, "Plasma Immersion Ion Implantation for ULSI Fabrication", *Nuclear Instrument and Methods*, (1990).

9 R.A. Stewart and M.A. Lieberman, "Model of Plasma Immersion Ion Implantation for Voltage Pulses with Finite Rise- and Fall-Times", submitted to *Journal of Applied Physics*, also *Report UCB/ERL*, M91/14, 21 February 1991.

10. R.A. Stewart, X.Y. Qian, D.A. Carl, B. Lake, Jr., J. Benasso, R. Lynch, C.A. Pico, M.A. Lieberman and N.W. Cheung, "Characterization of the Processing Plasma in an Engineering Prototype Reactor for Plasma Immersion Ion Implantation", *Report UCB/ERL*, M90/100, 12 November 1990.

11. R.A. Stewart and M.A. Lieberman, "Model of Plasma Immersion Ion Implantation for Voltage Pulses with Finite Rise- and Fall-Times", to be presented at the *18th IEEE International Conference on Plasma Science*.

12. R.A. Stewart, B. Troyanovsky and M.A. Lieberman, "Modeling Magnetic Bucket Confinement in an ECR Plasma Processing Reactor", to be presented at the *18th IEEE International Conference on Plasma Science*.

13. C.A. Pico, X.Y. Qian, R.A. Stewart, M.A. Lieberman and N.W. Cheung, "Shallow P-N Junction Fabrication by Plasma Immersion Ion Implantation", to be presented at the *Materials Research Society Meeting*, in Anaheim, CA., April 29-May 3, 1991.

14. M.H. Kiang, C.A. Pico, J. Tao, R.A. Stewart, N.W. Cheung and M.A. Lieberman, "Selective Copper Plating in Silicon Dioxide Trenches with Metal Plasma Immersion Ion Implantation", to be presented at the *MRS Meeting*, in Anaheim, CA., April 29-May 3, 1991.

15. C.A. Pico, J. Tao, R.A. Stewart, M.A. Lieberman and N.W. Cheung, "Plasma Immersion Ion Implantation for Al Hillock Suppression and Electromigration Resistance in VLSI Devices", to be presented at the *MRS Meeting* , in Anaheim, CA., April 29-May 3, 1991.

16. C.A. Pico, "Properties of Integrated Circuit Devices Fabricated Using PIII", to be presented at the *Electronics Materials Conference*, Boulder, CO, June 19-21, 1991.