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**PLASMA IMMERSION ION IMPLANTATION (PIII)
FOR INTEGRATED CIRCUIT MANUFACTURING:
SECOND QUARTERLY PROGRESS REPORT**

Memorandum No. UCB/ERL M91/63

March 18, 1990 – June 17, 1991

COVER PAGE

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by

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J. Tao, M.H. Kiang, C. Yu, V. Vahedi, B. Troyanovsky,
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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
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**Second Quarterly Progress Report
March 18, 1990 - June 17, 1991**

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FOR INTEGRATED CIRCUIT MANUFACTURING**

CCTP Contract # C90-071

Applied Materials Inc.

Project Managers:	N.W. Cheung, UCB
	M.A. Lieberman, UCB
Product Manager:	W.J. Wriggins, Applied Materials
Program Manager:	P.R. Klein, CA Office of Competitive Technology

FINANCIAL REVIEW

CompTech Program
Plasma Immersion Ion Implantation for Integrated Circuit Processing
Grant No. C90-071
First Quarterly Report
March 18, 1991 - June 17, 1991

Participant	To Date Planned	To Date Actual	Percent Actual of Planned	This Quarter Planned	This Quarter Actual	Percent Actual of Planned	Next Quarter Planned
CompTech	67,254	101,962	1.51	35,501	34,708	.97	37,605
Applied Materials							
Cash	29,779	39,024	1.31	13,155	9,245	.7	12,989
In-kind	7,500	4,000	.53	3,750	0	0	3,750

The amounts in the table include indirect costs.

**Second Quarterly Progress Report
March 18, 1990 - June 17, 1991**

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PERSONNEL

N.W. Cheung	Project Manager	UCB
M.A. Lieberman	Project Manager	UCB
W.J. Wriggins	Product Manager	Applied Materials
P.R. Klein	Program Manager	OCT
R.A. Stewart	Postdoctoral Research	UCB
C.A. Pico	Postdoctoral Research	UCB
J. Tao	Visiting Scholar	UCB
M.H. Kiang	Graduate Student	UCB
C. Yu	Graduate Student	UCB
V. Vahedi	Graduate Student	UCB
B. Troyanovsky	Undergraduate Student	UCB
W. En	Undergraduate Student	UCB
E. Jones	Undergraduate Student	UCB
J. Benasso	Technician	UCB

Collaboration with Other Research Groups

Dr. Ian Brown	Research Scientist	Lawrence Berkeley Lab
Dr. Kin-Man Yu	Research Scientist	Lawrence Berkeley Lab
Dr. Andy Keenan	Research Manager	Prometrix Inc.

PROJECT REVIEW

I. INTRODUCTION

Ion implantation is an important technique in integrated circuit fabrication. Due to the continuing trend toward smaller, faster and more densely packed circuitry, conventional ion implantation technology faces several challenges. Two major challenges are throughput, which is limited by the available ion current, and the production of very low energy ion beams for shallow implants. Other important concerns include charging, channeling, shadowing and damage.

An alternative to conventional ion implantation that may eliminate several of the above problems is *plasma immersion ion implantation* (PIII). We have successfully applied PIII to semiconductor device fabrication for a number of VLSI applications including sub-100 nm p⁺n junction formation, conformal implantation for trench doping, and palladium seeding for electroless Cu plating. The PIII process is illustrated in Figs. 1 and 2.

Ions are created in an electron cyclotron resonance (ECR) plasma source and diffuse into a process chamber, where they are extracted directly from the process plasma in which the wafer holder is located (Fig. 1). The substrate holder is biased to a high negative voltage (either pulsed or DC) and the ions are accelerated to the wafer through a high-voltage plasma sheath (Figs. 2a, 2b). Since the ion energy is controlled by the applied voltage, very low energy implants (≤ 1 keV) are possible. In addition, since PIII operates with an ECR plasma discharge, a range of pressures from 0.1–100 mTorr may be used. Thus, the angular distribution of the implanted ions can be adjusted by varying the gas pressure. This feature is very attractive for conformal doping of nonplanar surface topographies such as high-aspect-ratio trenches.

PIII can also operate in a triode mode (Fig. 2c) by introducing a sputtering target near to or within the ECR source chamber. The sputtering rate can be controlled by applying a suitable bias to the target. This technique provides the capacity of implanting any solid material into the substrate as long as the material has reasonable sputtering and ionization rates. In addition, dual ion implantations of both the source and sputtered atomic species can be achieved by varying the target and wafer holder biases.

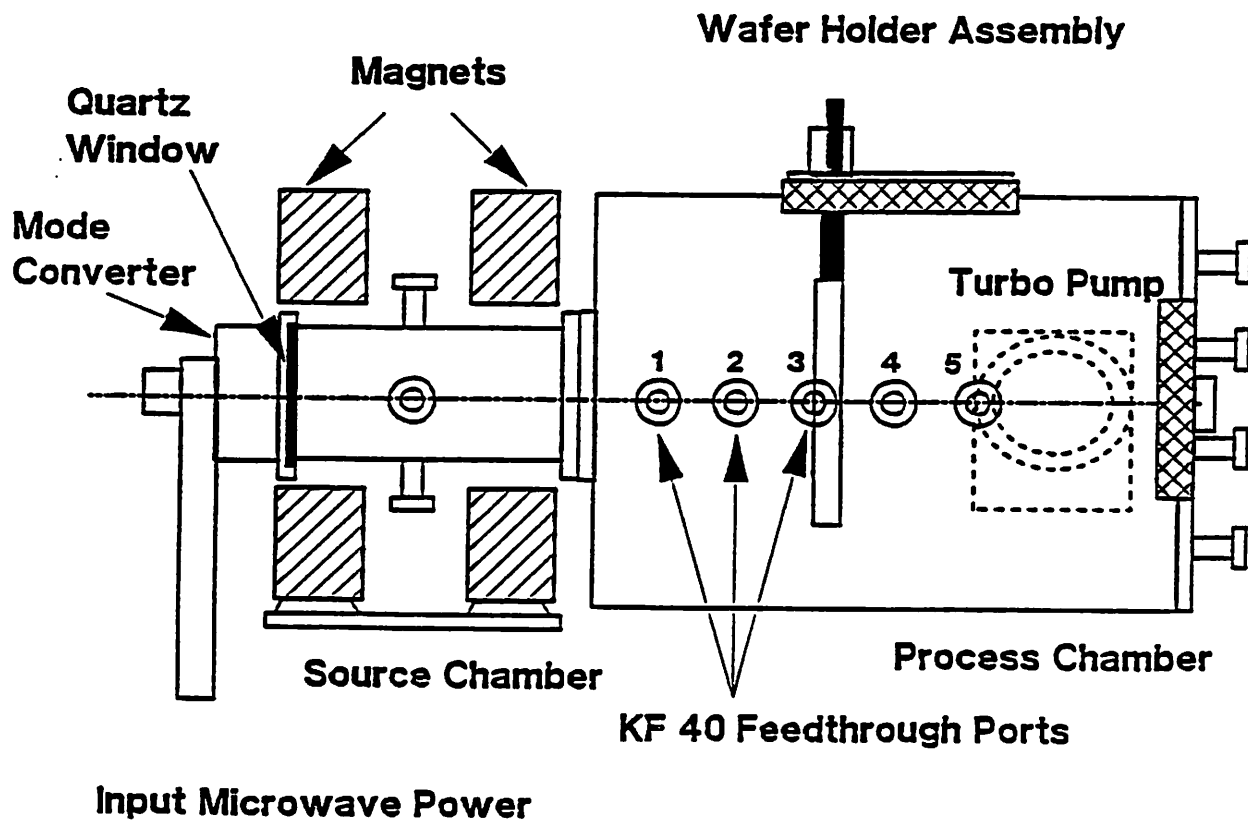
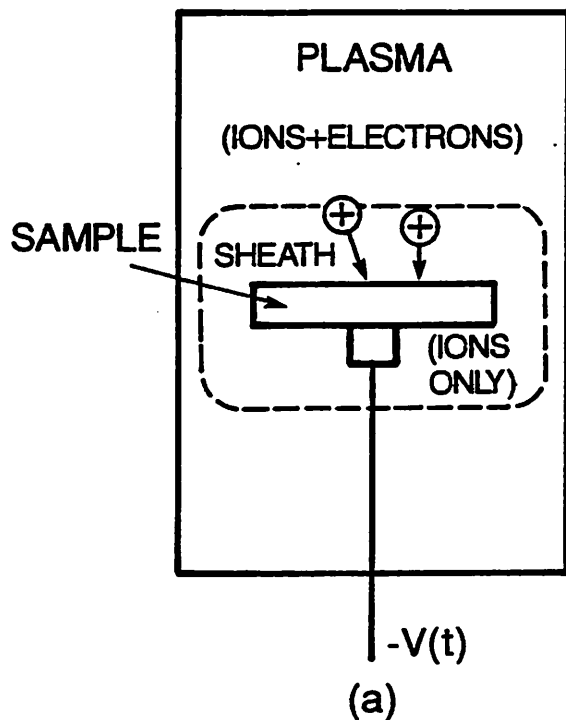
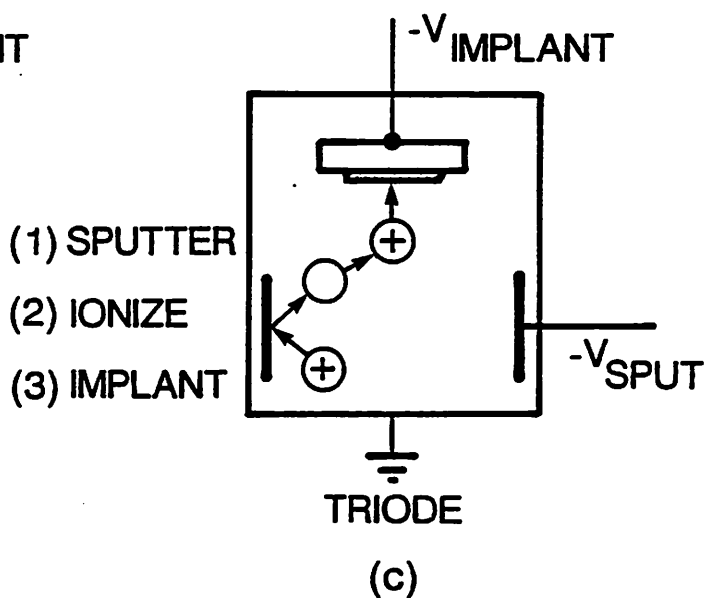
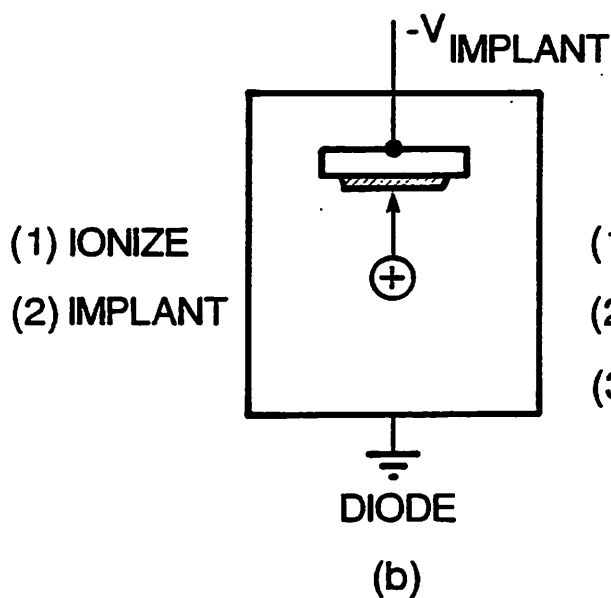


Fig. 1: Schematic side view of the PIII Reactor



Large Implant Current (~ 20 monolayers/sec)
 Large Implant Area (8-10" wafers)
 Conformal Implant of Irregular Surfaces
 Simple Machine Design
 Formation of New Surface Coatings
 DC/Pulsed Operation



Figs. 2 (a), (b), (c): Unique Features of PIII

Several features of PIII make it an attractive alternative to conventional ion implantation. With the high current capability of PIII, the throughput of present integrated circuit steps can be substantially increased. Also, the intermediate step of the ion source and all of its support equipment is completely eliminated, leading to a simple reactor design that is compatible with the cluster tool concept.

The PIII program at Berkeley in 1990-91 is supported by a \$70,000 cash and \$15,000 in-kind grant from Applied Materials, Inc., and a \$140,000 contract from the State of California Office of Competitive Technology. The goal of the project is to transfer the PIII process under development at Berkeley to Applied Materials, Inc.

II. SUMMARY OF PROGRESS

The three critical issues for transfer of the PIII technology to Applied Materials are:

- A. Process Demonstration. Demonstrate PIII processes that are more cost effective than conventional ion implantation.
- B. Process Integration. Demonstrate PIII process compatibility with conventional IC processes to fabricate a complete integrated circuit.
- C. Reactor Demonstration. Demonstrate a reactor that meets the required process uniformity and lack of oxide breakdown over a 200 mm wafer.

To address the first critical issue, three processes are being developed to demonstrate PIII superiority over conventional ion implantation:

(1) We have demonstrated the formation of 800 Å thick pn junctions with leakage currents less than 25 nA/cm² and low interfacial defect densities, comparable to the best commercial pn junction fabrication processes. The process consists of a 10kV SiF₄ pre-amorphization PIII implant followed by a 5kV BF₃ boron implant, followed by a one second rapid thermal anneal to activate the dopant (see Fig. 3). However, an obstacle to pn junction fabrication is condensation of BF₃ polymer, which interferes with both the implant and the measurement of implant dose. Safety considerations preclude our using di-borane (B₂H₆) or any arsenic or phosphorous-containing gases in our laboratory at Berkeley. Reduction of BF₃ condensates is described in Sec. III, and is currently one thrust of our work on pn

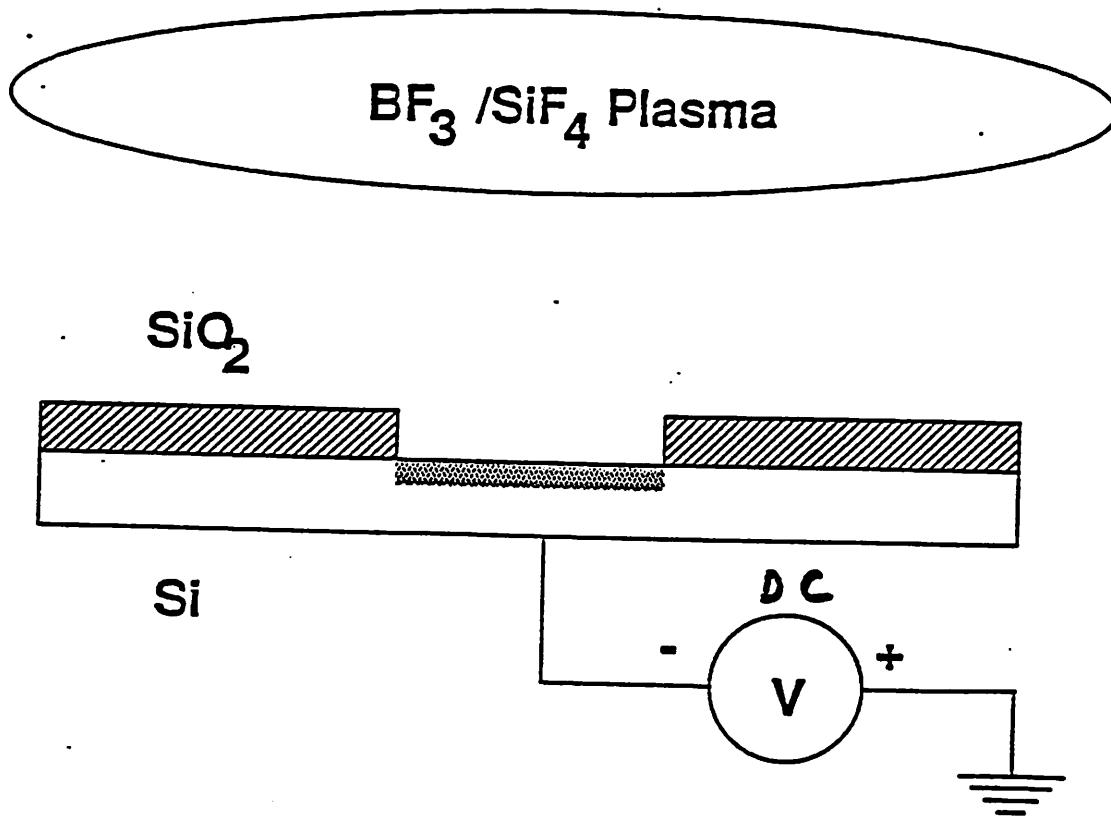


Fig. 3: PIII Shallow p⁺n Junction Fabrication Process

junction formation. Electrical characterization of pn junction devices is also under way.

(2) The second process being developed is conformal doping of trenches for trench capacitor or trench isolation. We have demonstrated conformal doping of trenches using a high-pressure (~5 mTorr) BF_3 PIII process (Fig. 4), with the doping boundary delineated by a crude staining technique (Fig. 5). As described in Sec. IV, we are refining our staining technique to delineate simultaneously a number of equiconcentration contours.

(3) The third process being developed is the formation of a metal seed layer for selective, electroless copper plating of oxide trenches. This process, which is a demonstration of the triode PIII configuration (see Fig. 2c), is described in Sec. V and the Appendix.

To address the second critical issue (Process Integration) and part of the third critical issue (Oxide Breakdown), we have developed a complete PIII processing compatibility test chip to investigate wafer charging as a cause of oxide breakdown and the use of poly-silicon as a p^+ doping source. The test chip is a PMOS process including inverters and ring oscillators, in which PIII is used for all (two) p^+ doping process steps. The complete chip has been designed, simulated and fabricated at Berkeley, and working devices (e.g., inverters) have been obtained. Capacitor breakdown tests will be performed on the test chip, as described in Sec. VI.

To address the remainder of the third critical issue (Process Uniformity), we are using analysis, computer simulation, and experiments to model the formation of the PIII process plasma, its injection into the process chamber, and the actual implantation process itself. We have developed a model of the implantation for pulses with finite rise- and fall-times. We have developed and are using a 2D simulation code to model the injection of the source plasma into the process chamber. We have characterized experimentally the plasma uniformity using a multidipole plasma confinement system on the process chamber in argon gas over a range of pressures and ECR source powers. We have achieved a density uniformity over an 8" wafer diameter of $\pm 1\%$. This work is described in Sec. VII.

A key test of uniformity is actual implanted dose. We have used PIII to implant 4" wafers, having an n^+ doped surface layer, with argon ions. We then determine the implant uniformity by measuring the increase in the resistivity of the layer due to the damage induced by the implanted argon ions.

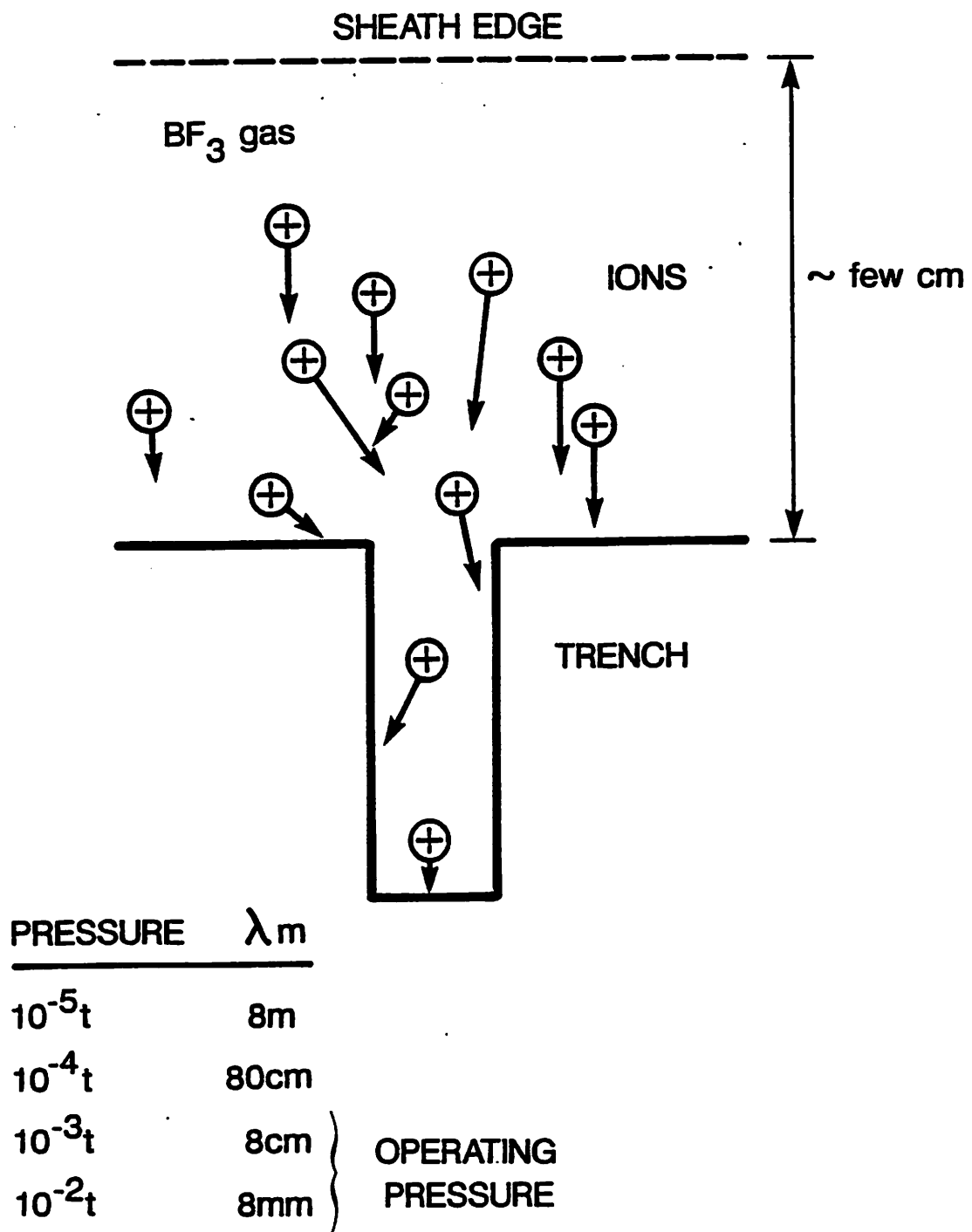


Fig. 4: Conformal Trench Doping

- 10 kV
- 200 mC
- 5 mT

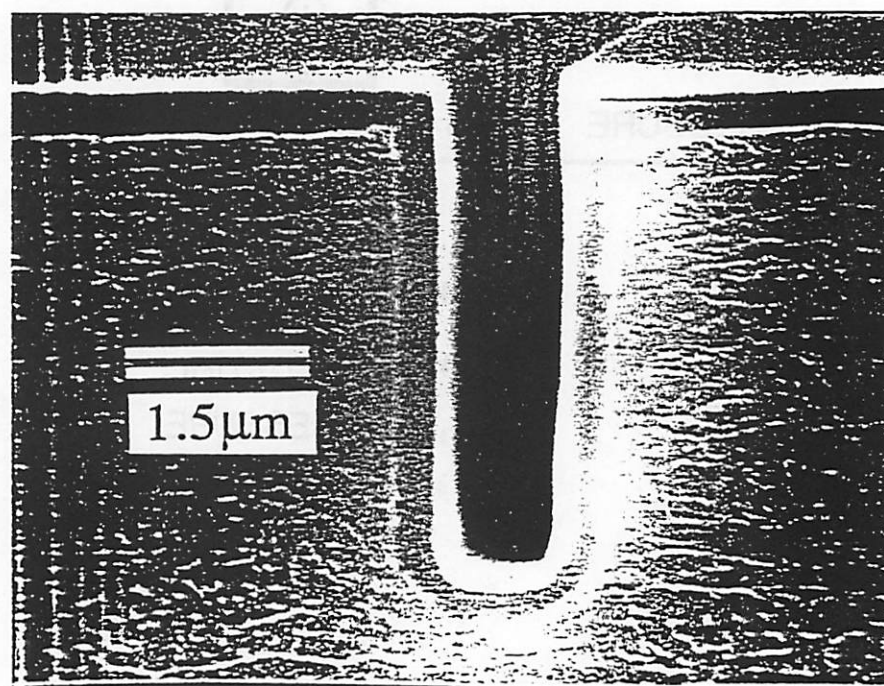
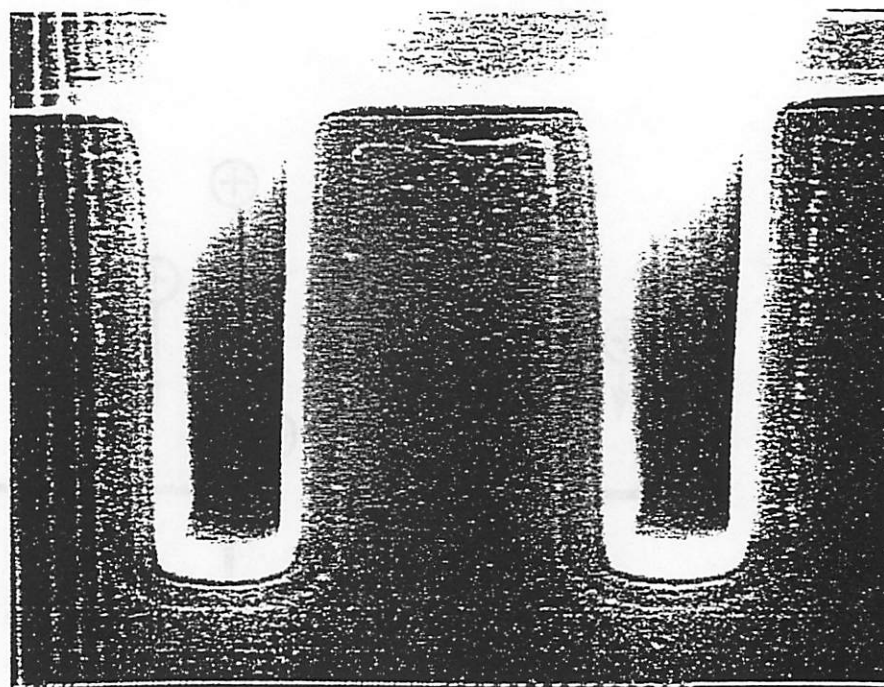


Fig. 5: PIII BF_3 Doped Trenches

Our preliminary results show that implant uniformities of $\pm 3\%$ can be achieved. Our major limitation to achieving even better implant uniformities appears to be the non-optimized (non-axisymmetric) design of the wafer holder (particularly, the wafer holder clips), and not any limitation arising from the PIII process itself. This work is described in Sec. III. Overall progress has been excellent and is summarized in Table 1.

The milestones are shown in Table 2. The Month 1 Milestone was met ahead of schedule.

The Month 3 Milestone was met ahead of schedule. A manuscript describing the excellent low leakage properties of the junctions will appear in *Applied Physics Letters*. The results are at least as good as those achievable using any other commercial process.

The Month 5 Milestone was due on 18 May 1991 and was not met. There continues to be a delay in obtaining trenches, as described in Sec. VI. The Month 8 milestone, which is a follow-on to the Month 5 milestone, is due on 18 August and will probably not be met. Hence we are behind schedule on the trench sidewall doping project.

The Month 9 milestone is due on 18 September. We are close to satisfying this milestone, as described in Sec. IV. We have designed and fabricated a PMOS test chip, and have obtained working inverter circuits. We need to complete the testing of this chip. We expect there will be no difficulty in satisfying this milestone.

Progress on the Month 10 milestone, due on 18 October, is described in Sec. V and Appendix A. We have already demonstrated planarization of copper interconnects. We need to complete examination of electromigration reliability, adhesion to oxide, and structural defects. We expect no difficulty in meeting this milestone.

The Month 12 milestone deals with collisional modeling of the PIII implantation process and with the two-dimensional modeling and computer simulation of plasma and implant radial profiles. At the request of Dr. W.J. Wriggins, Product Manager from Applied, we have given the work on plasma and implant uniformity a high priority during the second quarter, and have achieved very favorable results, as described in Sections III and VII. We are now confident that we have a process with adequate uniformity, as demonstrated by both experimental measurements and modeling results.

Table 1

Summary of Second Quarter Progress

- $\pm 1\%$ plasma uniformity over 8" diameter
- $\pm 3\text{-}4\%$ implant uniformity over 4" wafer
- Complete planarization of copper-filled trenches using PIII Pd/Si seed layer
- Complete PMOS test chip fabricated using (1) p^+ poly doping and (2) shallow p^+n junction formation
- High dose, 30 kV PIII implant demonstrated compatible with MOS processing
- Masking and processing completed for Applied trench etches

Table 2

Milestones

Month 1

Start characterization of 8" wafer Engineering PIII Reactor.

Month 3

Demonstrate low leakage current sub-100nm p^+n junctions with current density less than 25 nA/cm^2 at a reverse bias of -5V.

Month 5

Demonstrate trench sidewall doping uniformity to $\pm 50\%$ for 7:1 aspect-ratio trenches. Junction uniformity will be measured by staining methods and spreading resistance measurements.

Month 8

Demonstrate electrical characteristics of doped trenches showing no surface state inversion and adequate oxide breakdown strengths using C-V and breakdown measurements.

Month 9

Completion of a testing integrated circuit using PIII for sub-100nm junction formation to show compatibility with conventional process flow. The testing circuit will be a ring oscillator or an inverter.

Month 10

Demonstrate planarization of Cu interconnects using PIII seeding for 2:1 aspect-ratio oxide trenches. Verify electromigration reliability and adequate adhesion to oxide, and examine microstructural defects using cross sectional scanning electron microscopy.

Month 12

Complete collisional modeling of PIII and first-order 2-D PIII model. Includes analytical model of ion energy and angular distribution along with particle-in-cell computer simulation verification, ion current versus time for realistic PIII pulse shapes, and analytical and static 2D simulation of plasma density distribution in magnetic bucket process chamber geometry and ion implant radial profiles.

Month 12

Analysis of Phase I process development progress. Fine tuning for process optimization.

III. SHALLOW PN JUNCTION IMPLANTS USING BF_3 (C.A. Pico)

A. Introduction

The principal drive in our work is to demonstrate the viability of creating pn junctions using the PIII process. For safety reasons only BF_3 has been considered as a doping source gas. In our process BF_3 is ionized and subsequently implanted into n-type Si wafers. The implantation of the pedestrian fluorine atoms is believed to be noninterfering to our results. After B implantation the wafers are annealed to activate the boron in the wafers. The sheet resistances of these wafers are then measured and the implanted B dose is extracted.

Two mechanisms exist for the introduction of B into the Si wafers: implantation and surface adsorption. The sheet resistance properties are indistinguishable with respect to these two mechanisms after annealing. Unfortunately, the amount of B from surface adsorption can be as high as a dose of $10^{15}/\text{cm}^2$ or more and can overwhelm the intended implantation doses at or below this level.

At the end of the last reviewing period, we reported that the primary obstacle to fabricating controllable pn junctions using BF_3 implants had been the formation of a boron containing condensate (see Fig. 6). Such a condensate represents, at a minimum of one monolayer, a dose of $\sim 5 \times 10^{14}/\text{cm}^2$ of B. At high pressure ($\sim 1 \text{ mTorr}$) and high power ($> 300 \text{ W}$ microwave input power) conditions, this condensate grows increasingly thick with time. This surface growth layer results in a dose $10^{15}/\text{cm}^2$ to $5 \times 10^{15}/\text{cm}^2$ of B incorporation after rapid thermal anneal (RTA) as measured by sheet resistance measurements. Clearly, this high dose overwhelms our ability to produce $< 10^{15}/\text{cm}^2$ boronated shallow ($< 1000 \text{ \AA}$) junctions. More optimistically, the measured sheet resistance uniformity after RTA achieved under the surface condensation condition was less than 3% across a 4" wafer, and such a result could be useful in applications such as Poly-Si doping and conformal trench doping where higher (while less controlled) doses are preferred.

In addition, we reported initial observations indicating that this film growth could be avoided by lowering the BF_3 plasma pressure to below 0.8 mTorr and reducing the input microwave power to less than 200 W for our particular reactor. The bulk of our work done since using BF_3 has been under these conditions. We have investigated the relationship between the actual implanted dose (as measured by

Problem: Implant Gas Forms B-F Compound

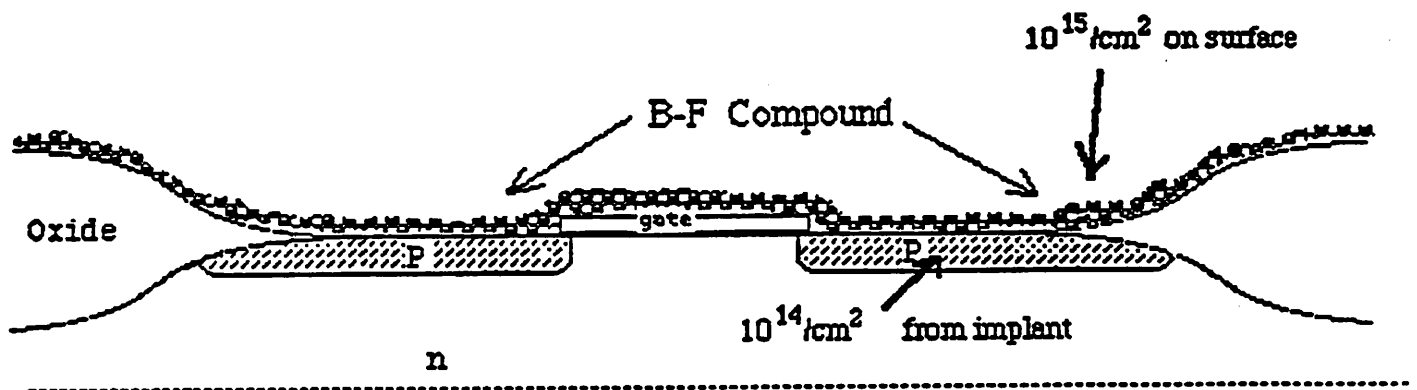


Fig. 6: Condensation of B-F Compound in BF_3 PIII

the electrical current during implant) as a function of the electrical implanted dose (as measured by sheet resistance measurements). From these results we have extracted the dose/pulse, dose as a function of time, and implant uniformity. These results are summarized below.

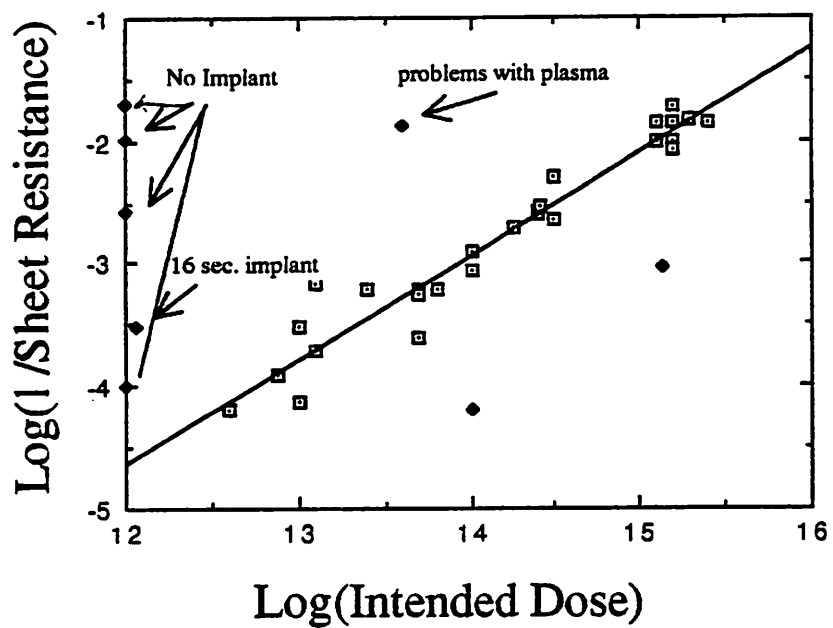
Finally, we have initiated studies using Ar^+ implants to compare with the BF_3 . This comparison allows us to decipher results that may be anomalous to surface contributions rather than outright implants.

B. Dose Rate Characterization

Two sets of implants were done. One used BF_3 and the other used Ar . The actual implant doses were determined by measuring the total currents into the samples during implant, using a calibration point as a standard. A RTA at 1060°C for 20 seconds was used to activate the implanted B atoms. The electrically active dose is extracted from subsequent sheet resistance measurements. This extracted electrical dose will be less than the implant dose because only a fraction of the total implanted atoms will become electrically activated.

The electrical dose of BF_3 implants, represented by the inverse sheet resistance, is plotted as a function of implanted dose in Fig. 7. We find that the total electrical B dose increases monotonically with the actual dose. Included in Fig. 7 are points labeled as "bad". These are points that do not lie near the best fit line. Four of the points, those lying on the actual dose line of $1 \times 10^{12}/\text{cm}^2$, correspond to actual implant doses of zero (i.e. no implant, just exposure). Yet these points indicate a significant dose of B incorporation (i.e. lower sheet resistance). This indicates that, at $t=0$ seconds of implantation, a surface layer exists. Apparently, this surface layer sublimates off during implant since the "best fit" data points do not intersect the point of a bare wafer even when moved to a dose of $10^{12}/\text{cm}^2$ (from 0).

Only two non-zero implant points lie above the "best fit" line. One, located at $2 \times 10^{12} \text{ cm}^{-2}$, was a 16 second implant. Apparently, a longer or higher dose implant is needed to "evaporate" off the condensate. This conclusion is reinforced by the trend in Fig. 8 in which the dose/pulse becomes constant for longer times. The other high "bad" data point located at $5 \times 10^{13} \text{ cm}^{-2}$ originated from a sample that was implanted using a problematic plasma. An initial conclusion is that a stable plasma operating at low pressure/power is required to avoid surface deposition. Only two other points do not fit on the



$1/R = 0.84 \times \text{Log}(\text{intended dose})$
 □ 32 Samples from Nov. Through Feb.
 "bad" → ♦ 8 Samples Either No Implant or Unusual

Fig. 7: Implant Dose Vs. Electrical Dose

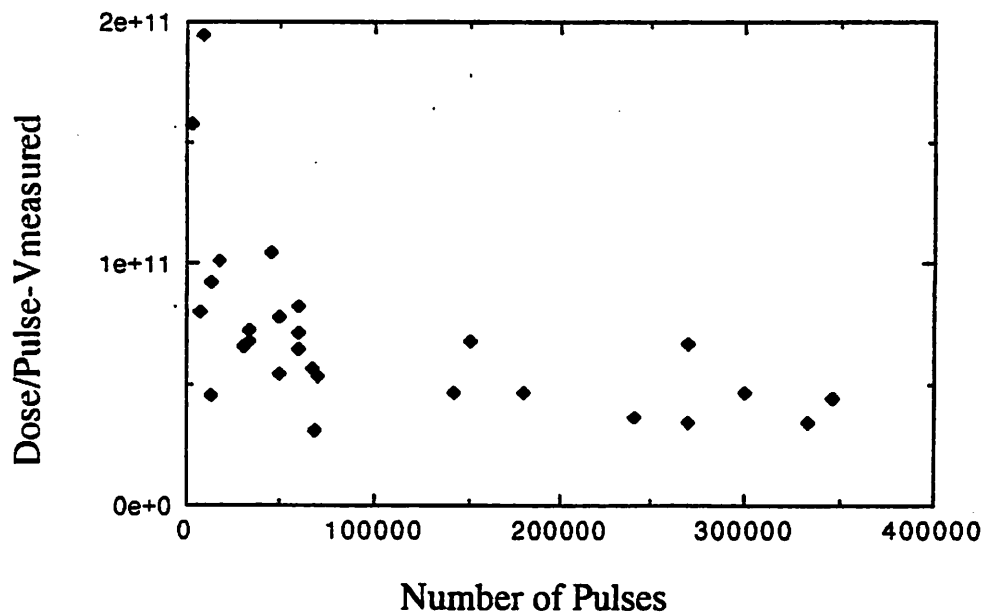


Fig. 8 (a): Dose Vs. Pulse

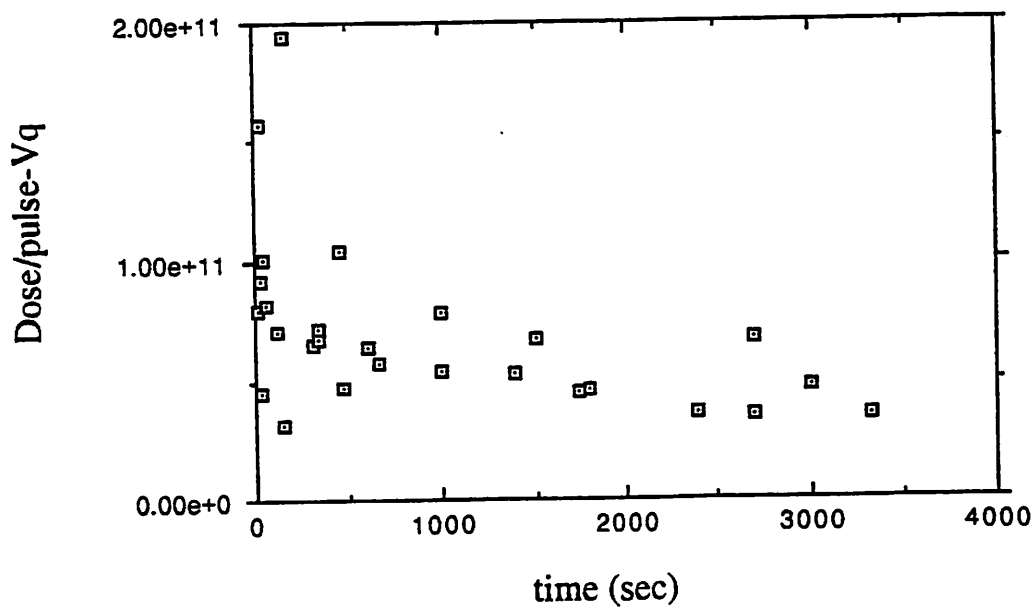


Fig. 8 (b): Dose Vs. Implant Time

"best fit" line. These have a lower dose and should be thrown out due to experimental error (such as the plasma going out or a misreading). This leaves 90% of the points intact as a "good" data set.

Within the "good" data we find the electrical dose is proportional to the 0.8th power of the actual dose. Ideally, it should be proportional to the 1st power. Several scenarios could explain this discrepancy. The first is that there is a mixture of surface and implanted B. However, one would expect this case to have a minimum value corresponding to, say, a single monolayer that did not desorb from the surface. This is not seen. A second is that, because the implant is very shallow ($\sim 100 \text{ \AA}$), some B diffuses out to the surface during annealing, leaving the electrical dose not inversely proportional to the actual dose. A third is that both sputtering and implant are occurring simultaneously. This would result in a superimposed set of clipped Gaussian implant profiles of B. Such a set would result in a slightly less than linear relationship to the actual implant dose. However, the data in Fig. 7 is plotted without regard to implant voltage. These voltages range from 5 kV to 30 kV, energies in which the sputtering effects should vary strongly. No voltage effect is seen, as shown in Fig. 9 that plots the implant electrical dose/pulse as a function of energy. For comparison, Ar was implanted into conventional ion beam implanted pn junction wafers. We find initially that the sheet resistance is linearly related to the intended dose (see Fig. 10).

C. Uniformity

The sheet resistance was measured at 45 sites using an automated Prometrix four point probe mapping station. Shown in Fig. 11 is the sheet resistance map of a 4" wafer achieved using a BF_3 surface condensate only (i.e. no implant). Note the circular sheet resistance profile and the near perfect uniformity. Such a result may be beneficial for very high dose applications such as trenches or Poly-Si doping. No attempt was made to measure repeatability in this case.

The uniformity of BF_3 implanted wafers was measured first without and then with magnetic multipole buckets (without the soft iron shields). These are represented in the sheet resistance maps shown in Figs. 12a and 12b. The range in the standard deviation dropped from 15-35% to 4-15%. Since then, soft iron magnetic shields have been installed. No uniformity measurement with respect to implant has been made under these present conditions.

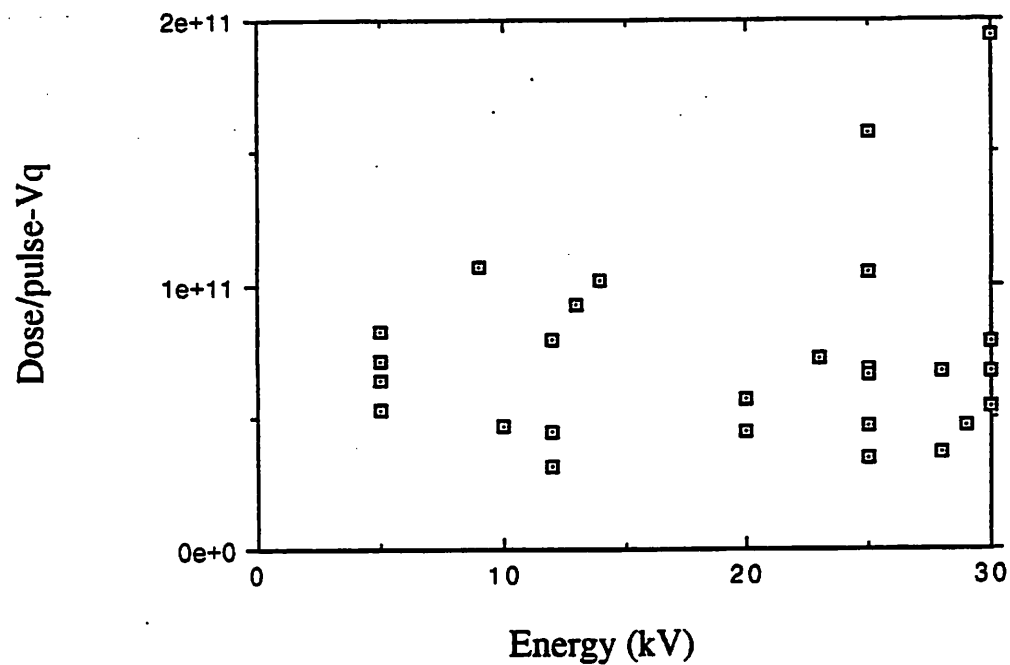
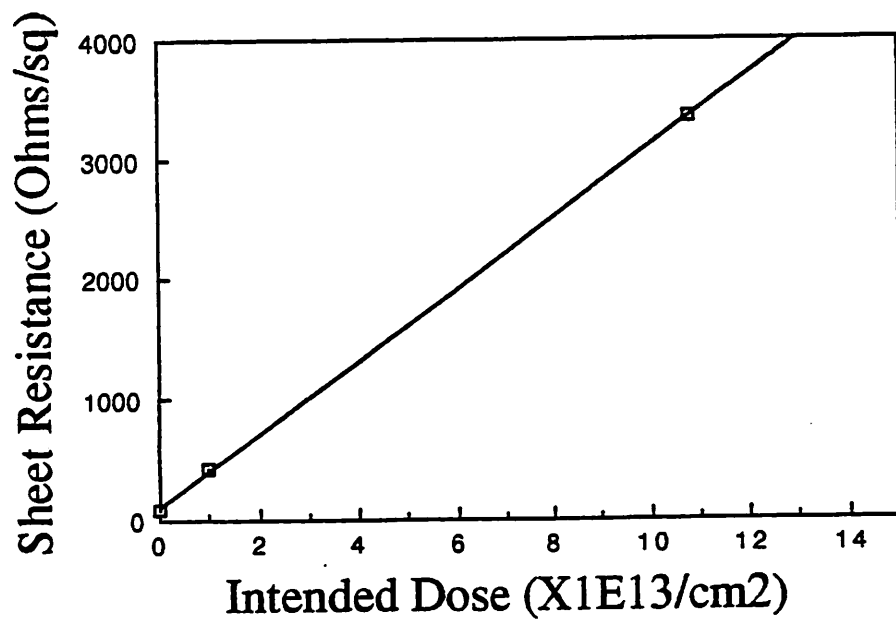


Fig. 9: Dose Vs. Energy

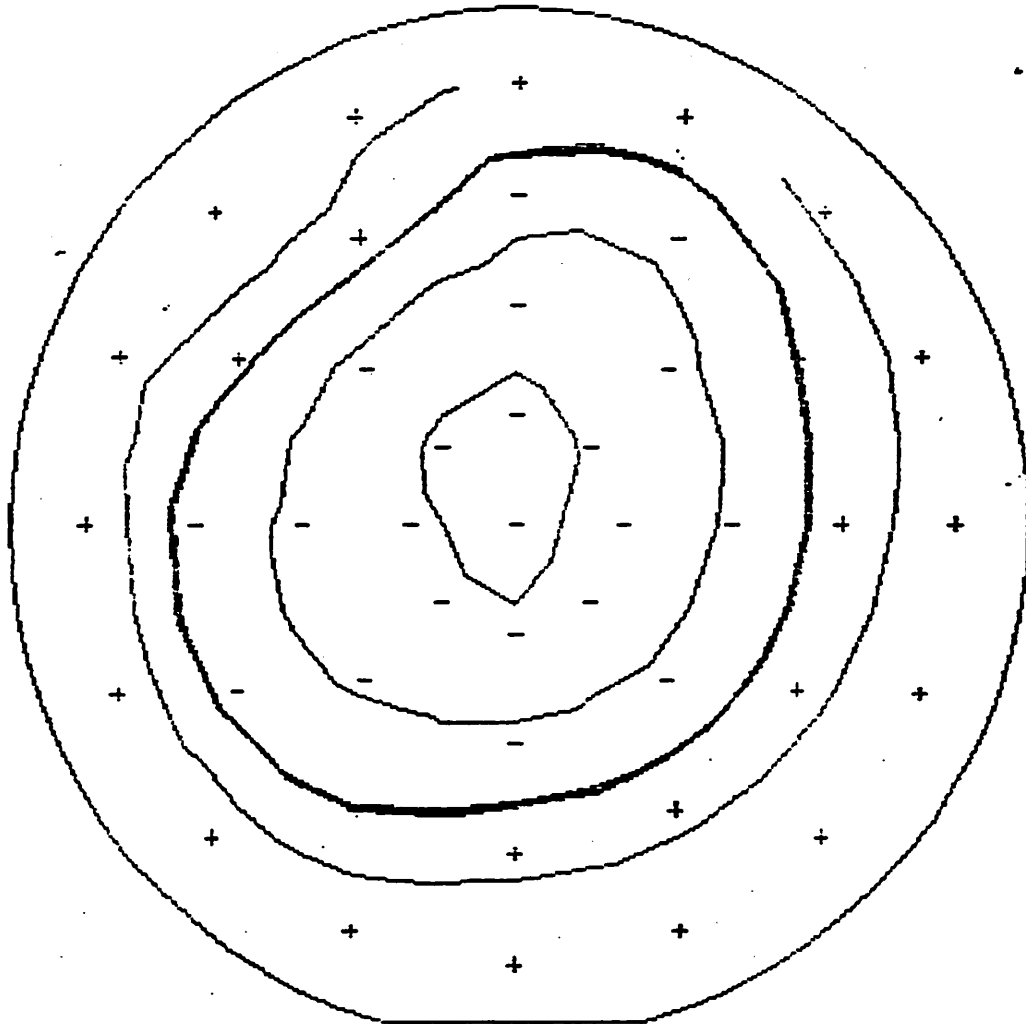


Voltage: 25 kV
 Pressure: 1 mTorr of Ar
 Substrate: 80 keV Sb, 5E14

Fig. 10: Sheet Resistance Vs. Intended Dose

Prometrix * OmniMap
Resistivity Mapping System

PROD0533A



SAMPLE I.D.: 11-20-90-4

DATE: 12-DEC-90
FILE NO.: 41
SOURCE: BF3
PROCESS: EXPOSED

AVE. VALUE: 51.24 ohms/sq
STD. DEV.: 1.56%
CONT. INT.: 1.00%
TEST DIAM.: 3.50 in.

1111,0.040,100gm 1mA,2mV,2.60 45/45

Fig. 11: Resistivity Mapping

Prometrix * OmniMap
Resistivity Mapping System

PROD0633A



SAMPLE I.D.: 10-30-91-4

DATE:	21-FEB-91	AVE. VALUE:	121.1 ohms/sq
FILE NO.:	44	STD. DEV.:	24.93%
SOURCE:	BF3NO DX	CONT. INT.:	5.00%
PROCESS:	25KV 1E15	TEST DIAM.:	3.50 in.

B111,0.040,100gm 100uA,2mV,9.50 45/45

Fig. 12 (a): Resistivity Map without Magnetic Buckets

Prometrix * OmniMap
Resistivity Mapping System

PR000833A



SAMPLE I.D.: 2-22-91-6

DATE: 14-MAR-91
FILE NO.: 51
SOURCE: BF3
PROCESS: NO DX

AVE. VALUE: 1602. ohms/sq
STD. DEV.: 3.72%
CONT. INT.: 1.00%
TEST DIAM.: 3.50 in.

B111,0.040,100gm 10uA,2mV,7.00 45/45

Dose is $3 \times 10^{13}/\text{cm}^2$

Prometrix * OmniMap
Resistivity Mapping System

PR000833A



SAMPLE I.D.: 2-22-91-18

DATE: 19-MAR-91
FILE NO.: 62
SOURCE: BF3
PROCESS: NO DX

AVE. VALUE: 188.9 ohms/sq
STD. DEV.: 9.49%
CONT. INT.: 1.00%
TEST DIAM.: 3.50 in.

B111,0.040,100gm 100uA,2mV,6.50 45/45

Dose is $4 \times 10^{14}/\text{cm}^2$

Fig. 12 (b): Resistivity Maps with Magnetic Buckets

Because of the uncertainty of surface condensate, Ar was used as an implant species into pre-formed pn junction for uniformity studies. Figure 13 shows a typical sheet resistance mapping profile after Ar implant. The standard deviations of the sheet resistances increase from 1-2% before Ar implant to 2-5% after Ar implant. This result shows that excellent uniformity can be achieved with PIII processing. In addition, initial experiments indicate little or no change in implant uniformity with respect to microwave power or gas pressure.

D. Effects of BF_3 , Ar, and N_2 Implants on Al Reliability

Earlier we had reported that N_2 and O_2 implants could suppress thermal hillock formation in Al films. We have extended this study to include an inert gas, Ar, and an alloying gas, B from BF_3 . The results of its effectiveness in suppressing hillocks is summarized in Table 3. In addition, the electromigration resistance of the implanted samples was measured as a function of implant species. These are shown in Figs. 14a and 14b. We find that the electromigration resistance characteristics are degraded by implantation.

Both thermal hillocks and electromigration properties are understood to be related to grain boundary diffusion. It follows that the hillock suppression and electromigration performance degradation using very shallow ($\sim 100 \text{ \AA}$) implants cannot be explained by the conventional theory of grain boundary diffusion. Clearly, surfaces play a much larger role in these reliability issues than previously thought. This demonstrates that PIII is a useful tool for fundamental scientific investigation.

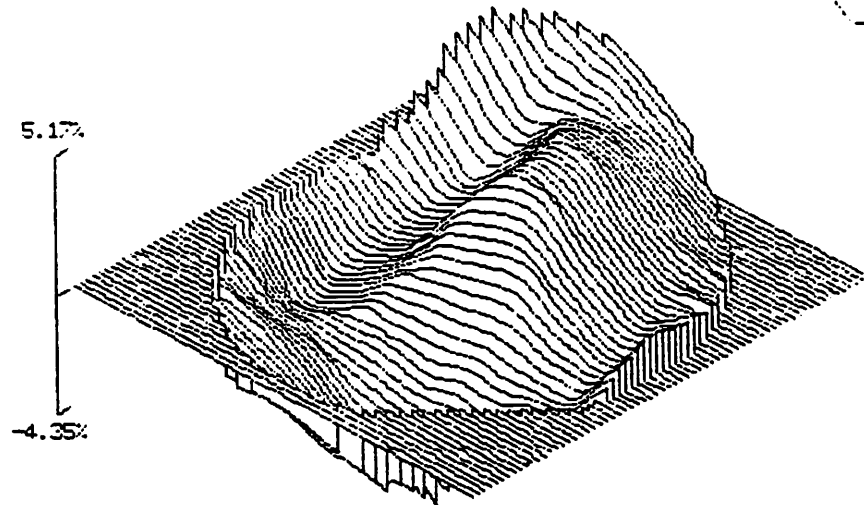
IV. CONFORMAL DOPING CHARACTERIZATION (C. Yu)

PIII can be used to conformally implant trench structures. Currently, there is no convenient way of characterizing the two-dimensional dopant distribution of implants. Conventional electrical means are best suited for implants into flat topography with the concentration of dopants varying in one direction only. Although some electrical means, such as CV measurements, can be adapted to extract some information about implant profiles and dose in trench structures, these methods involve complicated numerical data processing and the accuracy of the results is limited.

Prometrix * OmniMap
Resistivity Mapping System

PROD0533A

Rotated 0 deg.
Tilted 30 deg.



SAMPLE I.D.: AS-1 AFTER

DATE: 17-MAY-91
FILE NO.: 82
SOURCE:
PROCESS:

AVE. VALUE: 403.4 ohms/sq
STD. DEV.: 2.43%
TEST DIAM.: 3.50 in.

8111,0.040,100ga 1mA,20mV,2.90 45/45

Fig. 13: Resistivity Map for Ar Implanted Wafer.
Initial uniformity was 1%.

Table 3
Conditions of Implantation and Hillocks

Implanted Gas	Peak PIII Voltage (kV)	Calculated Rp (Å)	Calculated ΔRp	Nominal Dose (atom/cm ²)	Hillocks?
N ₂ (N atoms)	0	(Exposed to Plasma)		—	Yes
	-2.5	50	30	6X10 ¹⁵	Yes
	-10	145	75	1.5X10 ¹⁶	No
	-30	392	170	3X10 ¹⁶	No
O ₂ (O atoms)	-30	380	165	3X10 ¹⁶	No
Ar	-4	60	30	6X10 ¹⁵	No
	-15	190	80	1.5X10 ¹⁶	No
	-25	325	130	2.5X10 ¹⁶	No
BF ₃ (F atoms)	-7	60	30	6X10 ¹⁵	Yes
	-23	160	75	1.5X10 ¹⁶	Yes

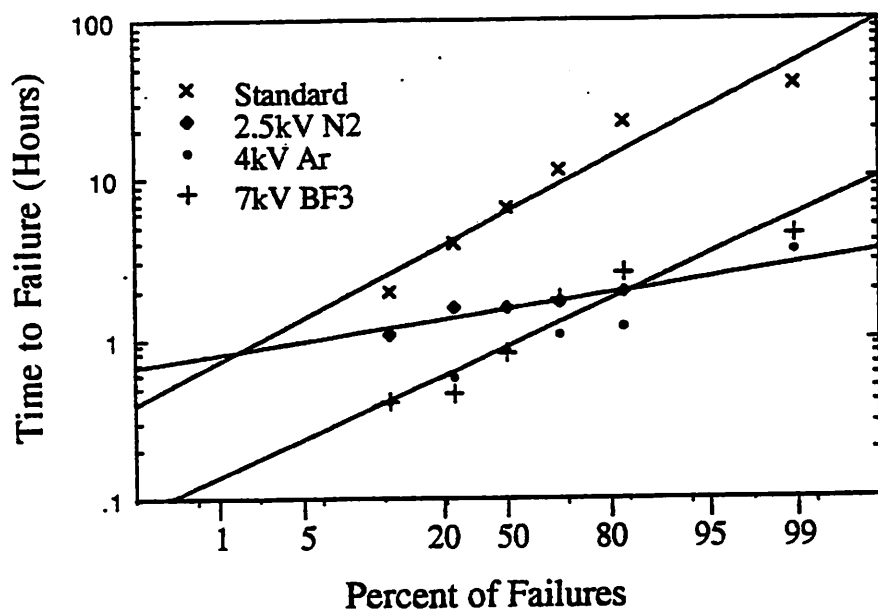


Fig. 14 (a): EM Failure Vs. Species for $R_p \approx 60 \text{ \AA}$

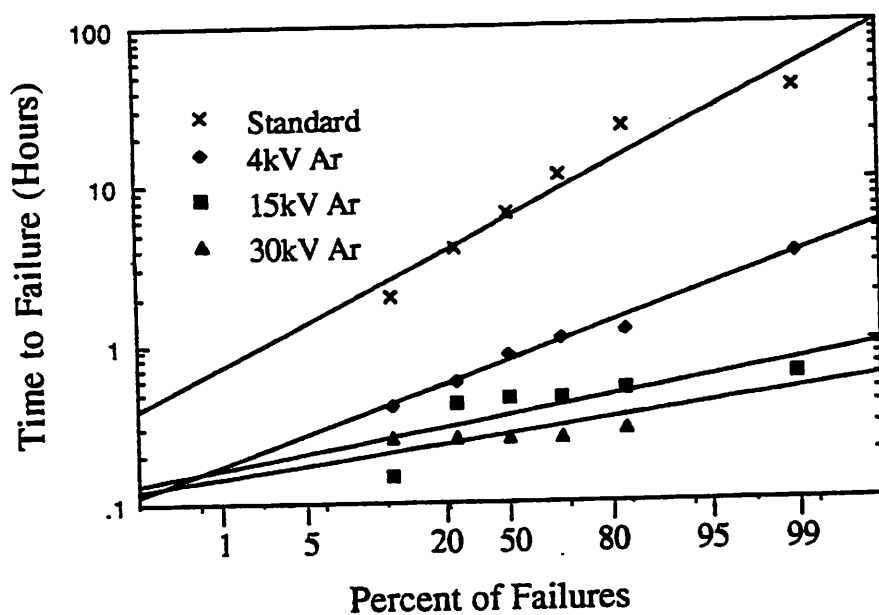


Fig. 14 (b): EM Failure Vs. Ar Implant Energy

We are developing a technique which will selectively delineate equiconcentration contours in sample cross-section. Originally reported by Gong ("Simulation of Lateral Spread of Implanted Ions: Experiments", *ESSDERC '89*, Berlin), this technique uses HF (50%), HNO₃ (70%), and CH₃COOH (100%). Under strong white light, a two-step reaction occurs which is responsible for selectivity: (1) $\text{Si} + 2\text{O} \rightarrow \text{SiO}_2$ and (2) $\text{SiO}_2 + 6\text{HF} \rightarrow \text{SiF}_6^{2-} + 2\text{H}_2\text{O} + 2\text{H}^+$. For low resistivity silicon, (1) is much faster. Thus, the difference in etch rates yields equiconcentration contours which can be observed under SEM. We have been able to consistently reproduce a contour at approximately $6 \times 10^{16}/\text{cm}^3$. This technique is being refined to yield a higher concentration contour at 1.5×10^{19} . Eventually, this technique could be used in conjunction with a pn junction stain and yield up to 3 contours on one sample.

During the last quarter, we have been able to delineate two sets of equiconcentration contours on high energy boron implants as well as p⁺ diffusion implants. Calibration of these contours is being pursued by comparison with known implant profiles.

An angle-lapping technique has been developed to enhance the delineation technique. Polishing the cross section of the samples at an angle effectively magnifies the surface. Using a one degree lapping angle, approximately 50x magnification can be achieved. By this technique, the dose uniformity of PIII trench implants can be verified. With more refinement and the delineation of more contours, the two-dimensional implanted dopant distribution can be extracted.

A mask for trench test structures was made. Trenches have been patterned into groups of various widths so that different aspect ratios of trenches can be obtained after RIE. The pattern was transferred onto 15 wafers with $\sim 1\mu\text{m}$ oxide hard mask. The patterned wafers were sent to Applied's Etch Application Lab, with whom we established contact in April through George Lecouras of the Implant Division. Unfortunately, the Si etcher at Applied is being taken down and our samples could not be scheduled despite the efforts of the Applied Etch Applications Lab persons involved. We would like to express our appreciation for the efforts of Zhara Amini and Zhilin Huang of the Etch Lab at Applied who went out of their way to try to schedule our samples in before the etcher went down. The scheduled delay is approximately one month from the end of May 1991. In the meantime, a matrix of

experiments is being prepared to examine the effects of pressure and bias during implant on the implant uniformity.

When the trench samples are ready, the matrix of wafers implanted at various conditions will be generated. To confirm conformal doping into trenches by PIII, the previously reported results will first be reproduced by standard pn junction staining. Then a more detailed study of the two-dimensional dopant distribution in trenches will be carried out using the dopant delineation technique described above in conjunction with angle lapping.

V. METAL SEED LAYER FOR ELECTROLESS COPPER PLATING (M.H. Kiang)

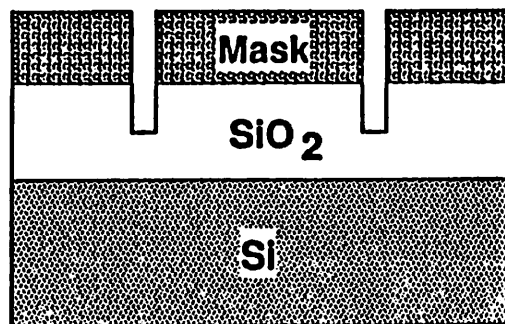
In its application to VLSI processing, PIII is used to form the seed layer for selective Cu plating of interconnects. Figure 15 shows the process sequence: (1) one μm thick oxide is grown by wet oxidation, followed by photoresist patterning and reactive ion etching to make trenched patterns; (2) implant metal ions and then remove the photoresist that acted as the mask for implantation in this step; and, (3) immersion of the patterned wafers into electroless Cu plating solution to fill up the oxide trenches.

Planarized Cu interconnects using Pd/Si PIII to form the seed layer in 1:2 aspect-ratio oxide trenches have been demonstrated. A summary of this work appears as Appendix A. In continuation of the effort to fabricate planarized oxide trenches of higher aspect-ratios, we continue to study some processing issues and their influences:

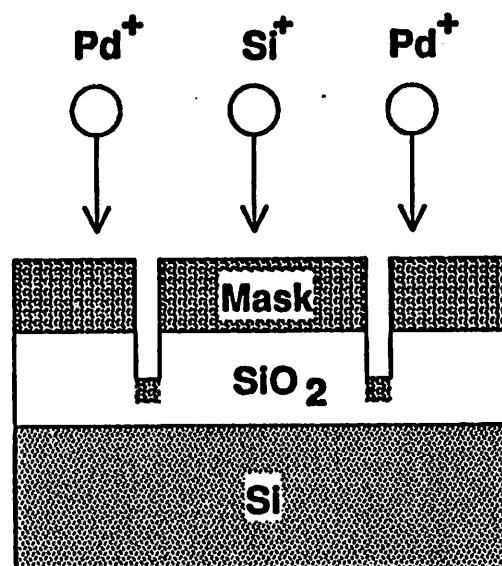
(1) *Cu deposition on the trench sidewalls:* We suggested that the observed deposition was a result of high Pd dose (larger than the threshold dose) due to the sloped trench sidewalls. The non-vertical sidewall could be caused by mask erosion or by an etchant loading effect during the RIE etching of the oxide trenches. For the former case, we may have to consider the use of other masking materials, e.g. silicon nitride, instead of the photoresist that has been used.

(2) *1-step PIII versus 2-step PIII:* Their effects on the adherence of the plated Cu films to the substrates are yet to be investigated and verified by further experiments. The resistivity of the plated

1.



2.



3.

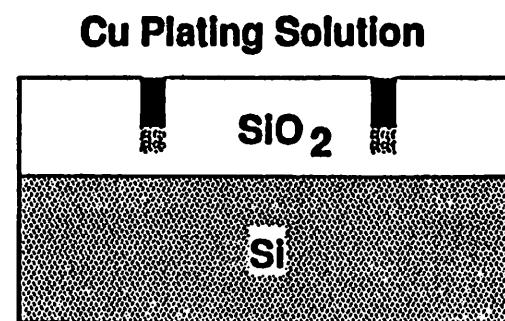


Fig. 15: Process for Selective, Electroless Copper Plating

thin copper films (several hundred angstroms thick) we have obtained is about $4\ \mu\Omega\text{-cm}$. More measurements of the plated Cu lines under different plating conditions will be carried out to optimize the processes.

VI. PROCESSING COMPATIBILITY TEST CHIP

A. Integrated Circuit Device Fabrication Using PIII (C.A. Pico)

We have completed and have begun testing a test chip (Fig. 16) demonstrating the compatibility of PIII with IC processing. This is a single level metal test chip with minimum design dimensions of $2\mu\text{m}$ using a PMOS process. A gate oxide of $650\ \text{\AA}$, much thicker than typical $100\text{-}200\ \text{\AA}$ gate oxides, was so chosen to create a much more sensitive oxide for the detection of trapped charges from the PIII process. To further enhance gate damage with respect to previous PIII oxide tests, the implant voltage was chosen to be 30kV (significantly higher than the $2\ \text{kV}$ used in previous experiments). PIII of BF_3 was used to create p^+ regions in a medium doped ($0.01\text{-}0.1\ \text{ohm-cm}$) n-type wafer and for poly-Si gates and interconnects. In both cases, the doping level was $1\times 10^{15}\ \text{cm}^{-2}$. This dose is low for $3500\ \text{\AA}$ poly-Si films, but is sufficient to demonstrate its feasibility. Figure 17 shows the high frequency capacitance properties of a $650\ \text{\AA}$ capacitor scanned from $+4\text{V}$ to -4V and from -4V to $+4\text{V}$. We see no change in the C-V features indicating that no interface charge is created from the process. In addition, no change is seen with sinter indicating no change in the trapped charge in the bulk of the oxide. Finally, we have extracted an electrically active substrate carrier dose of $3\times 10^{16}/\text{cm}^3$, in agreement with the substrate doping level.

Forward and reverse leakage measurements were made on pn diodes. The subthreshold swing for the diodes was 66mV/decade (i.e. an ideality factor of 1.15). The reverse leakage was measured to be $80\ \text{nA/cm}^2$. While this is not state-of-the art, it is respectable with respect to that achieved using the identical process flow using conventional ion beam implantation and an NMOS process.

Transistor characteristics were measured. These are shown in Fig. 18. A plot of $\sqrt{I_D}$ versus V_G shows a V_t of -1.7V . This value agrees with that predicted by S.M. Sze for a $650\ \text{\AA}$ oxide with a substrate doping of $\sim 2.7\times 10^{16}/\text{cm}^3$.

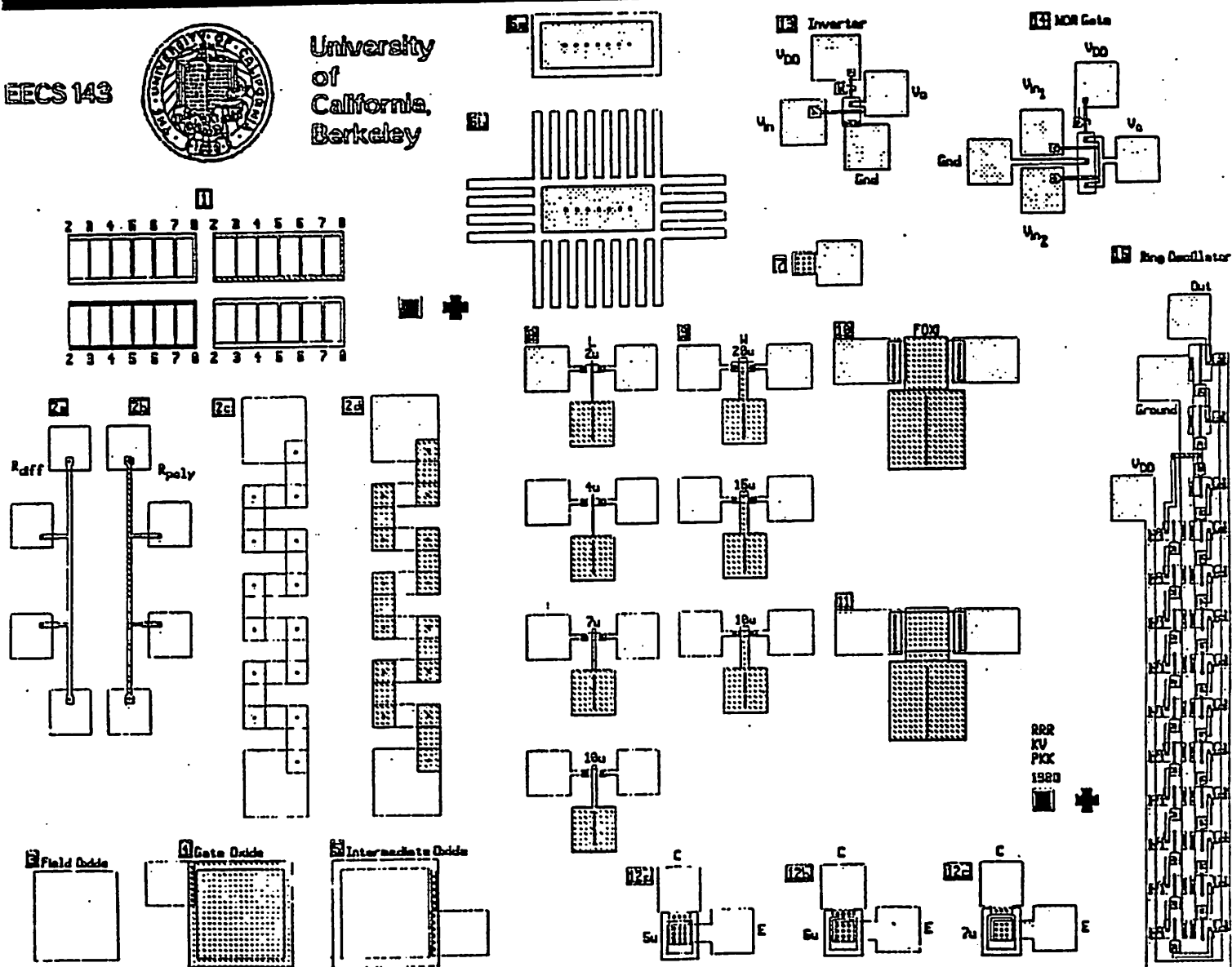


Fig. 16: PMOS PIII Processing Compatibility Test Chip

C-HF vs. V-GATE

DEV. I.D.: 143-1 GATE-OX BEF SI₃N₄ EXP. I.D.:

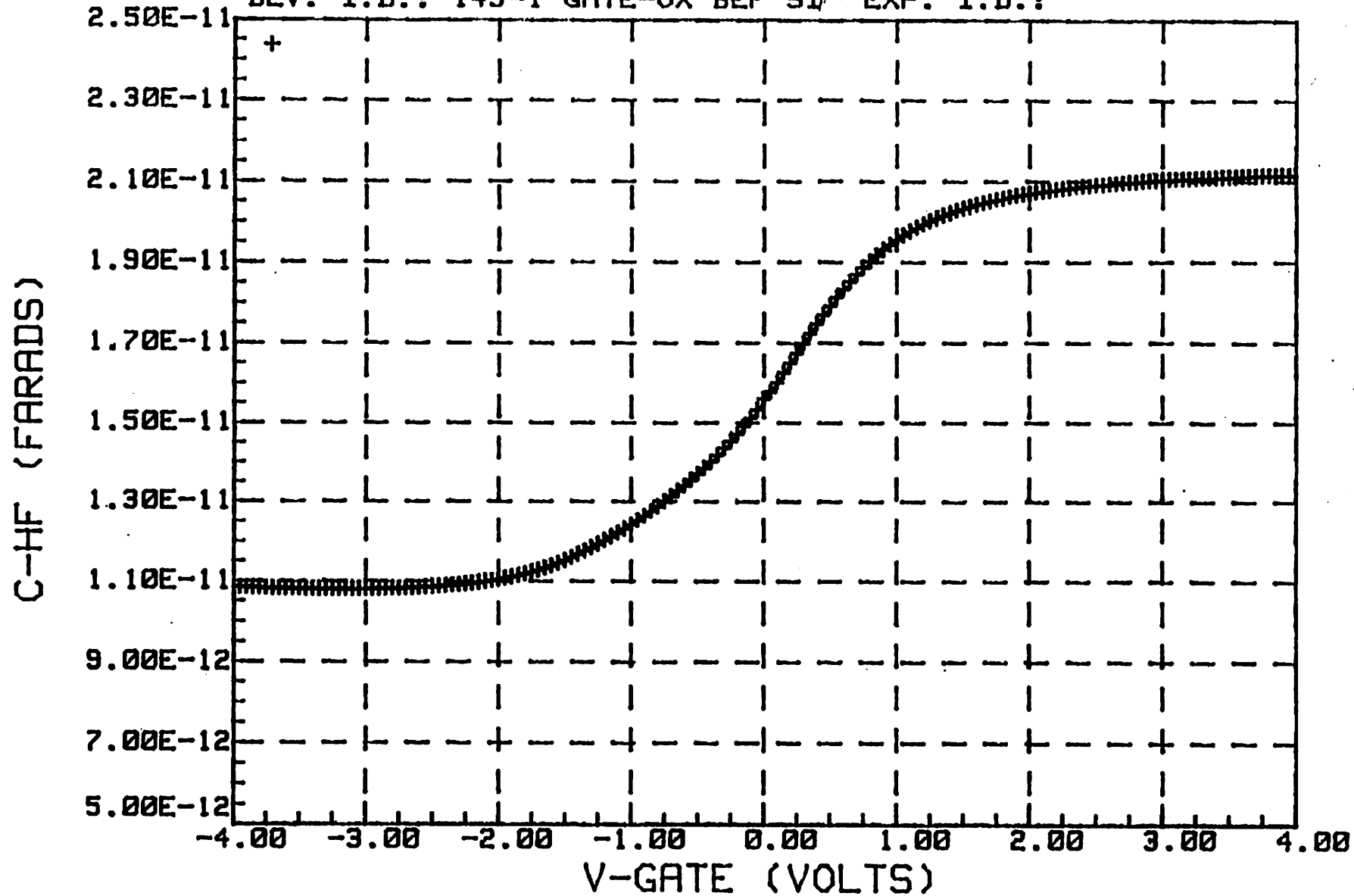
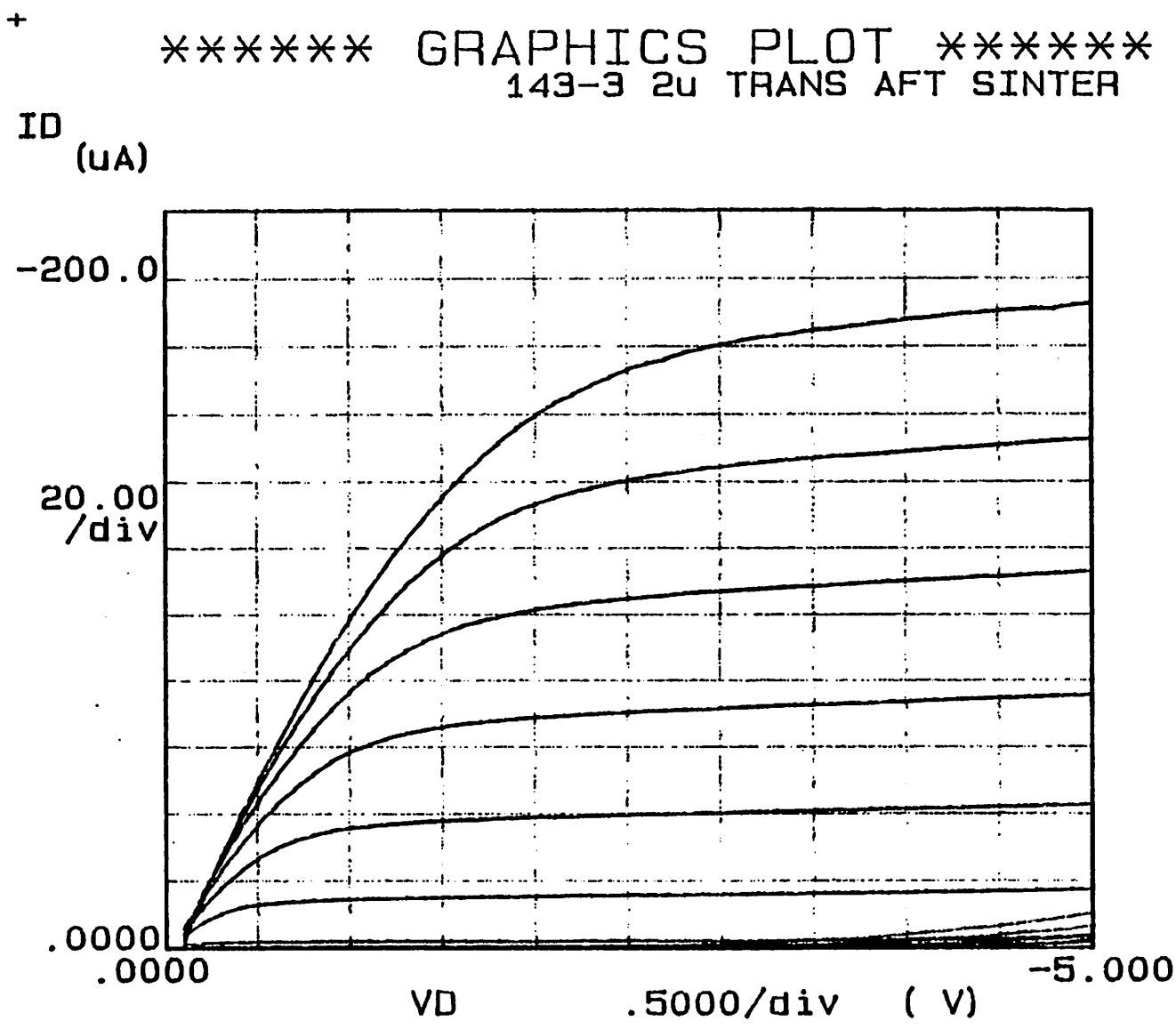


Fig. 17: High Frequency PIII Capacitor Properties



Variable1:
VD -Ch2
Linear sweep
Start .0000V
Stop -5.0000V
Step -.1000V

Variable2:
VG -Ch3
Start .0000V
Stop -5.0000V
Step -.5000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

Fig. 18: Forward and Reverse Leakage on PIII pn Junction

Finally, we have achieved the stated objective of a complete IC fabrication process. This is demonstrated in the output characteristics of a PMOS inverter and PMOS NOR gate (Figs. 19 and 20).

B. Capacitor Charging Effects (W. En)

To aid our study of capacitor charging, we are using SPICE3, a circuit simulator, to simulate the plasma conditions during implantation. The simulator will show how the time-varying surface potential on the wafer varies with respect to the input waveform. A non-linear capacitor will represent the capacitance across the dark-space (implantation sheath) region. Since the dark-space region width will vary with respect to the voltage applied, the capacitance will vary as well. The other non-linear element will represent the I-V characteristics of the plasma. To help characterize the simulation, we will be making measurements of the surface potential on a wafer in the chamber during implantation. Figure 21 shows the test structure we plan to use. A chip will be developed to test compatibility of PIII with other IC production processes. The chip is a PMOS version of an NMOS layout (see Fig. 16) that is used as an instructional laboratory test chip to teach IC fabrication techniques. Process simulation for fabricating this chip is currently under way. The chip will be used to demonstrate the use of poly-silicon as a p+ doping source, and to study wafer charging effects that can lead to oxide breakdown. For the latter, the PIII reactor will be used to implant argon at several different energies and the change in the capacitor threshold voltage will be measured.

VII. UNIFORMITY STUDIES (R.A. Stewart)

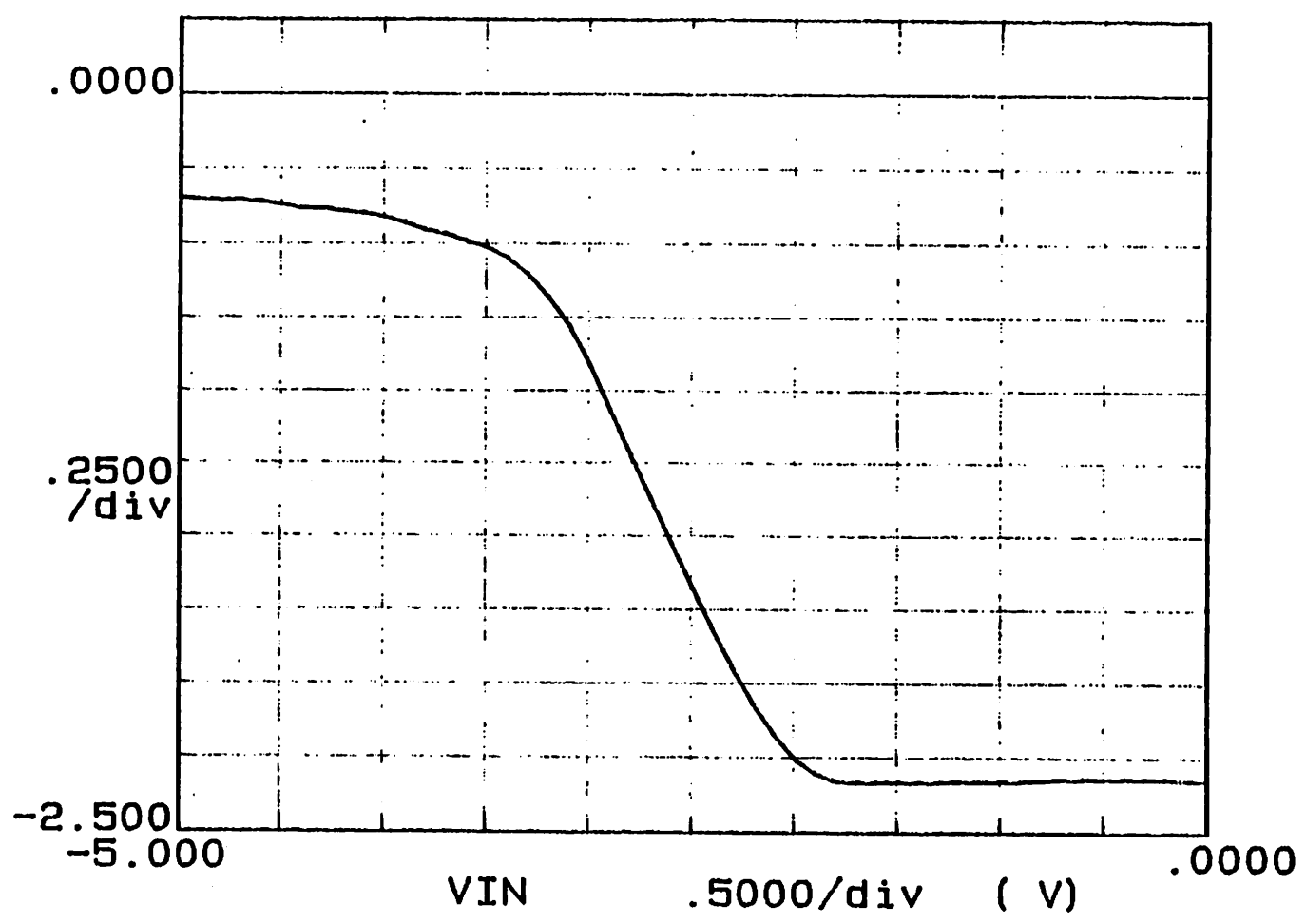
A study is in progress to improve the process plasma uniformity by means of multidipole plasma confinement. Figure 22 shows a sideview of a typical PIII plasma source. The plasma from the ECR source streams into a cylindrical process chamber of radius R and length L in which the substrate (wafer) is located. Portions of the process chamber surface may be covered with permanent magnets to enhance the plasma uniformity near the wafer surface. These can be arranged as a set of M linear multidipoles around the exterior cylindrical surface, and portions of one or both cylinder walls.

+

+

***** GRAPHICS PLOT *****
143-3 INVERTER

VOUT
(V)

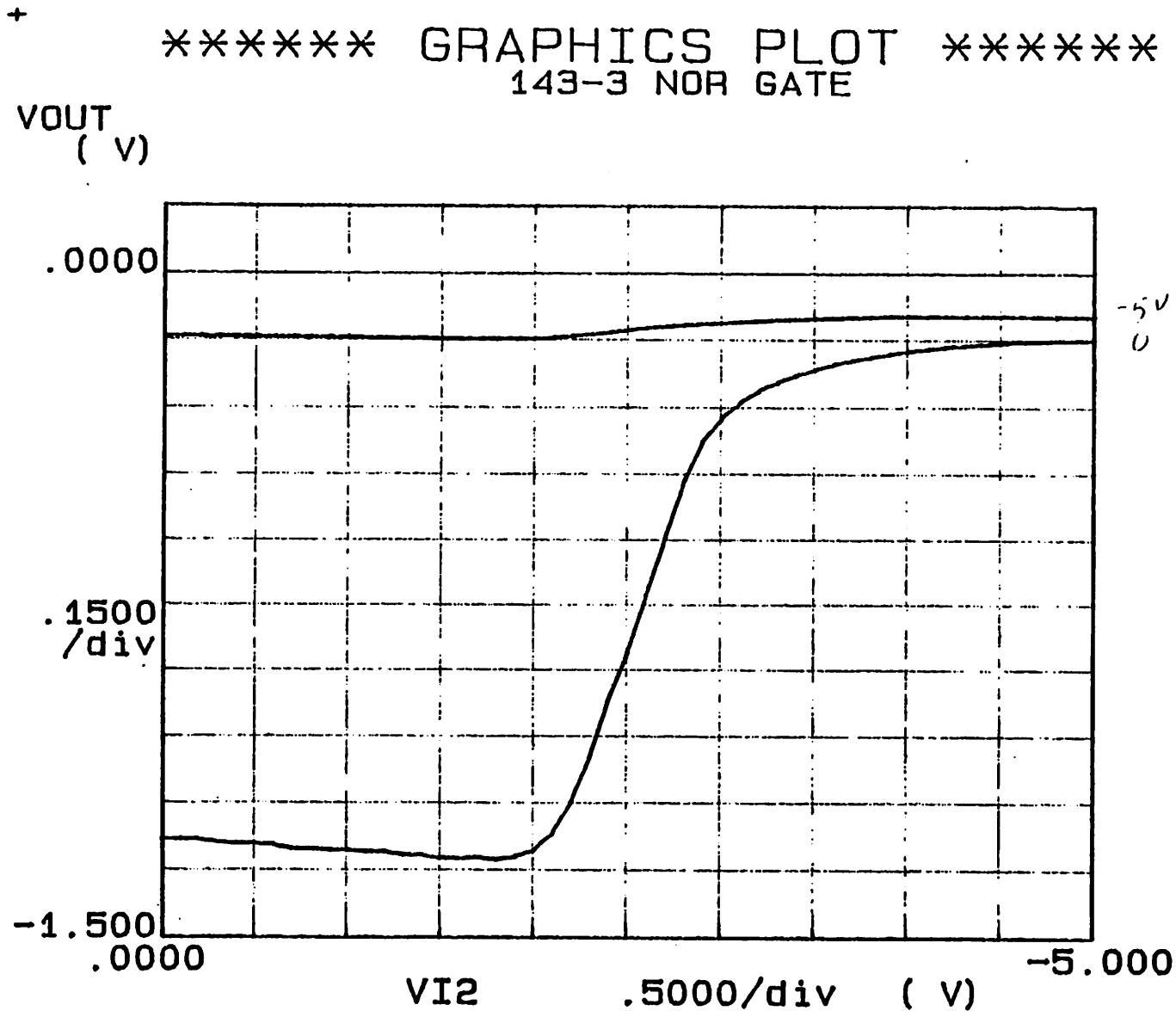


Variable1:
VIN -Ch3
Linear sweep
Start .0000V
Stop -5.0000V
Step - .1000V

Variable2:
VD -Ch2
Start -7.0000V
Stop -7.0000V
Step .0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

Fig. 19: PIII PMOS Inverter



Variable1:
 VI2 -Ch4
 Linear sweep
 Start .0000V
 Stop -5.0000V
 Step - .1000V

Variable2:
 VI1 -Ch3
 Start .0000V
 Stop -5.0000V
 Step -5.0000V

Constants:
 VS -Ch1 .0000V
 VDD -Ch2 -5.0000V
 H -Vs1 10.000V
 L -Vs2 -10.000V

Fig. 20: PIII PMOS NOR Gate

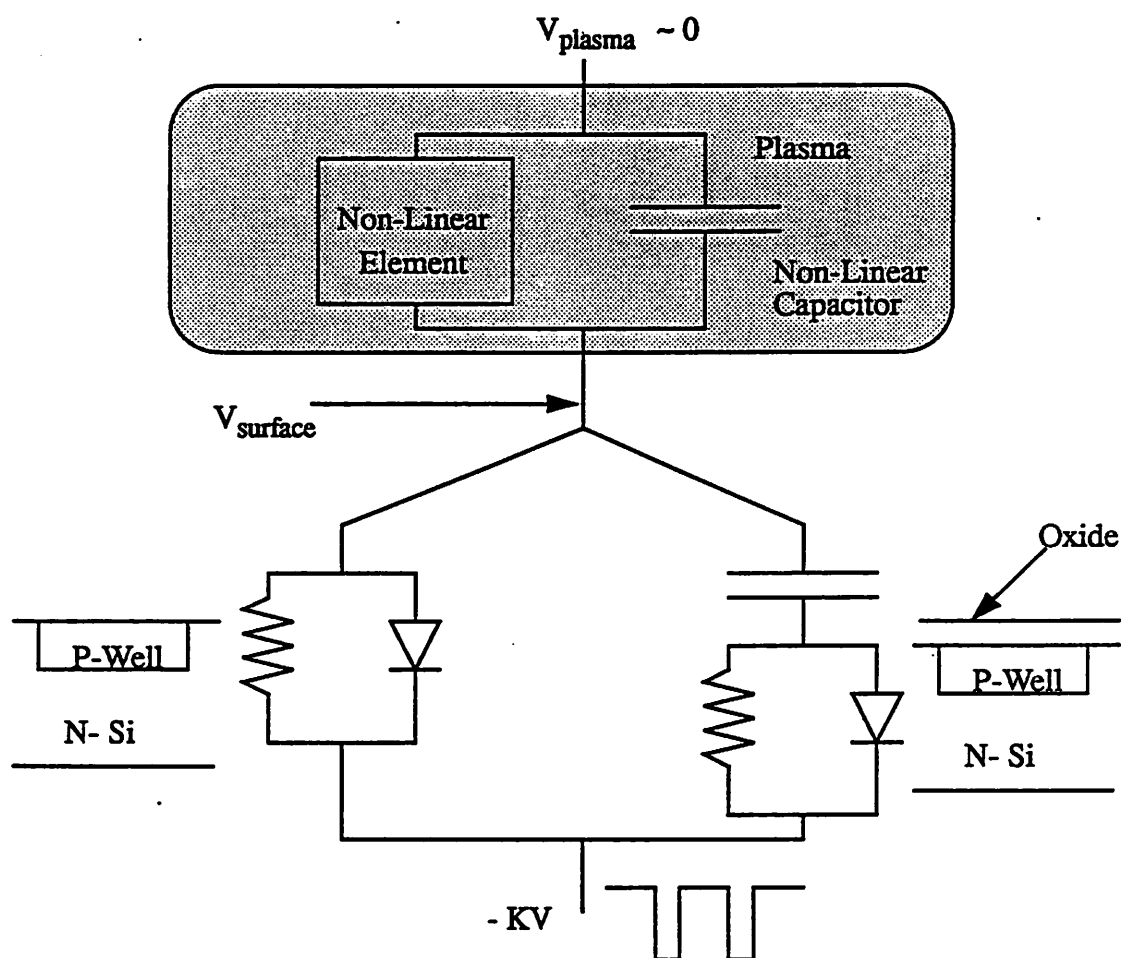


Fig. 21: Test Structure and Nonlinear Circuit Model

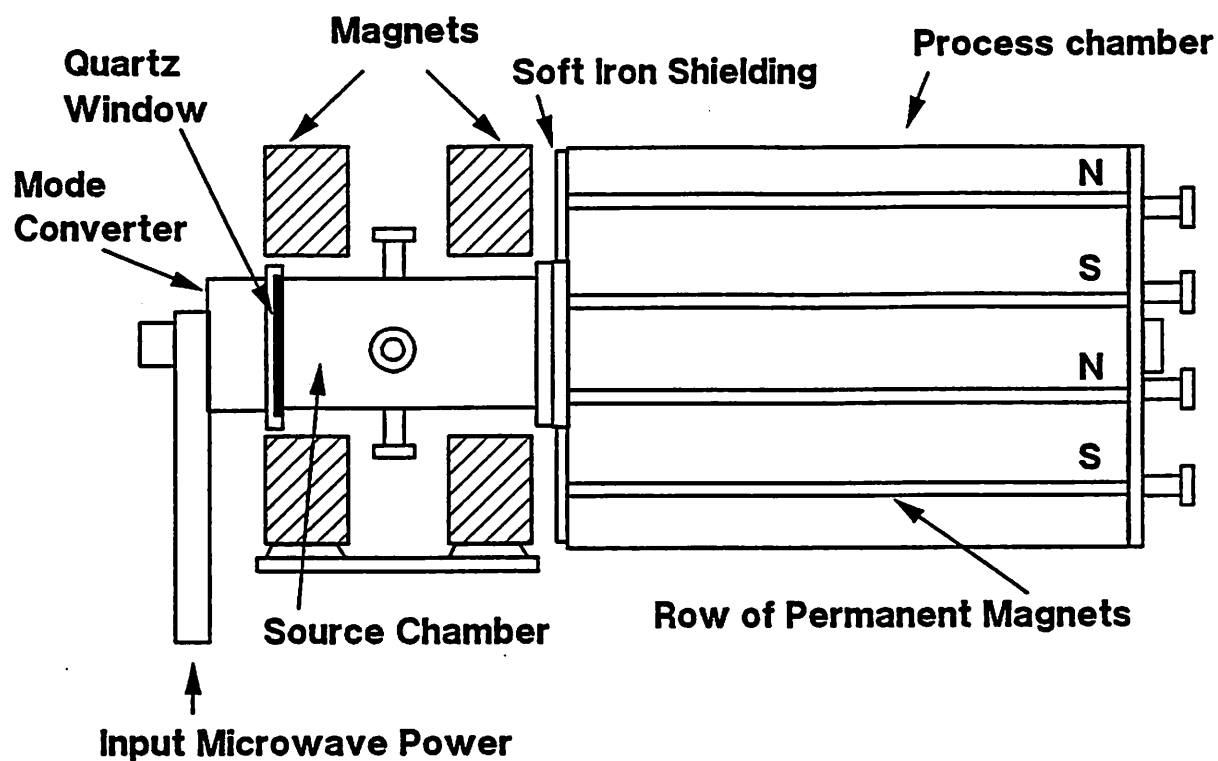


Fig. 22: ECR Plasma Processing Reactor with Multidipole Magnetic Bucket and Magnetic Shield

As a first step, we have studied the diffusion equation solution for a process chamber geometry as shown in Fig. 23. The plasma from the source is assumed to have a parabolic radial profile $n(r) = n_0 (1 - r^2/a^2)$ for $r < a$. The remaining part of the top face and the entire bottom face are assumed to have perfectly absorbing boundary conditions. Multipoles are assumed to be arranged along the cylindrical sidewalls, leading to a partially reflecting (mixed) boundary condition at $r = R$

$$\frac{\partial n}{\partial r} + \alpha n = 0$$

where

$$\alpha = \frac{\sqrt{3}}{\lambda_i} \frac{1 - \rho}{1 + \rho}$$

and λ_i is the ion-neutral mean free path. The reflection coefficient ρ can be expressed as

$$\rho = 1 - \frac{M w_i}{2\pi R}$$

where M is the number of multipoles, w_i is the leak width, and R is the process chamber radius. For the portion of the top face $r > a$ and the bottom face, the boundary condition is

$$\frac{\partial n}{\partial z} + \alpha n = 0$$

where $\alpha = \sqrt{3}/\lambda_i$ since we assume $\rho = 1$ on these surfaces.

A code has been developed to solve the two-dimensional (r, z) diffusion equation

$$\nabla^2 n + k^2 n + G = 0$$

where $k^2(r, z)$ accounts for plasma electron-neutral ionization within the source chamber and $G(r, z)$ accounts for hot electron-neutral ionization (if present). The full range of boundary conditions from $\rho = 0$ to $\rho = 1$ can be accommodated on both top and bottom faces and cylindrical sidewalls of the process chamber. Provision has been made for a wafer holder within the process geometry having arbitrary size, shape and boundary conditions. These conditions allow a reasonably accurate determination of plasma properties within the process chamber, even in the very low pressure regime for which the ion mean free path $\lambda_i \sim R, L$, when the wafer holder within the chamber strongly perturbs the solution, and when there is ionization within the process chamber itself.

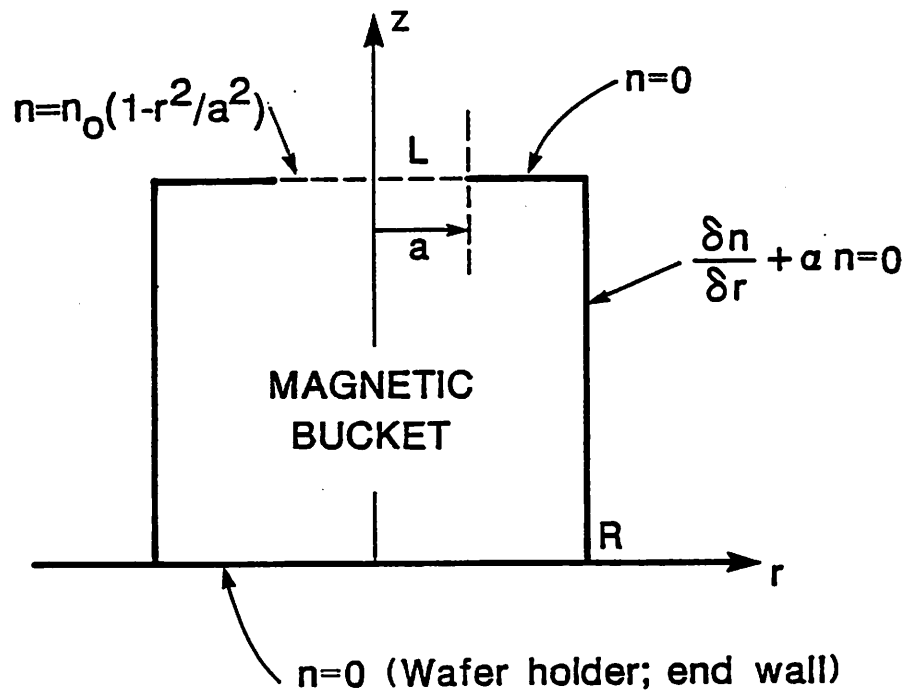


Fig. 23: Analytical Model of Multidipole Confinement

The 6" diameter ECR source injects plasma into an 18" diameter, 30" long precess chamber having a variable position, 11" diameter wafer holder (see Fig. 1). The process chamber has been equipped with a set of linear multidipole magnets and soft iron shielding at the source-process chamber interface (see Fig. 22). The shielding is designed to reduce the strength of the diverging magnetic field in the process chamber created by the ECR magnets, hence improving radial uniformity.

Numerical simulations and measurements using Langmuir probes have been made to determine radial plasma density for an argon plasma without the presence of a wafer holder. For the simulations we let the peak plasma density entering the process chamber equal $n_0 = 10^{11} \text{ cm}^{-3}$, the reflection coefficient vary from $\rho = 0.5-0.95$ for the sidewall, and $\rho = 0$ for the top and bottom faces. The pressure is varied from 0.1-10 mTorr in the simulations and from 0.25-10 mTorr for the measurements. In addition, for the measurements, the microwave power was varied from 300-1000 watts and measurements were taken with three configurations: (1) without the multidipole magnets and without shielding, (2) with the multidipole magnets and without shielding, and (3) with the multidipole magnets and the shielding. Measurement results reported below are with configuration (3) unless otherwise stated. Radial plasma uniformity was determined over a diameter of 200 mm according to the definition

$$\% \text{ uniformity} = 100 \frac{n_{\max} - n_{\min}}{2n_{\max}}$$

Figure 24 shows a typical contour plot of plasma density obtained from the simulation program. This plot corresponds to sidewall boundary conditions of $\rho = 0.9$ and a pressure of 1.0 mTorr. The increased radial uniformity with increasing distance from the source chamber (decreasing z) is clearly evident. Figure 25 further illustrates the variation of uniformity with distance from the ECR source chamber at 1.0 mTorr computed for sidewall reflection coefficients $\rho = 0.5, 0.75, 0.90$ and 0.95 . Also plotted is the measured uniformity for a microwave power of 500 W. Comparison of the measured and computed uniformities indicates that the multidipole magnets provide very good ion confinement in our process chamber (for these plasma conditions).

The variation of uniformity with pressure is shown in Fig. 26. For both simulations and measurements the uniformity improves with decreasing pressure as expected due to the increased mean free

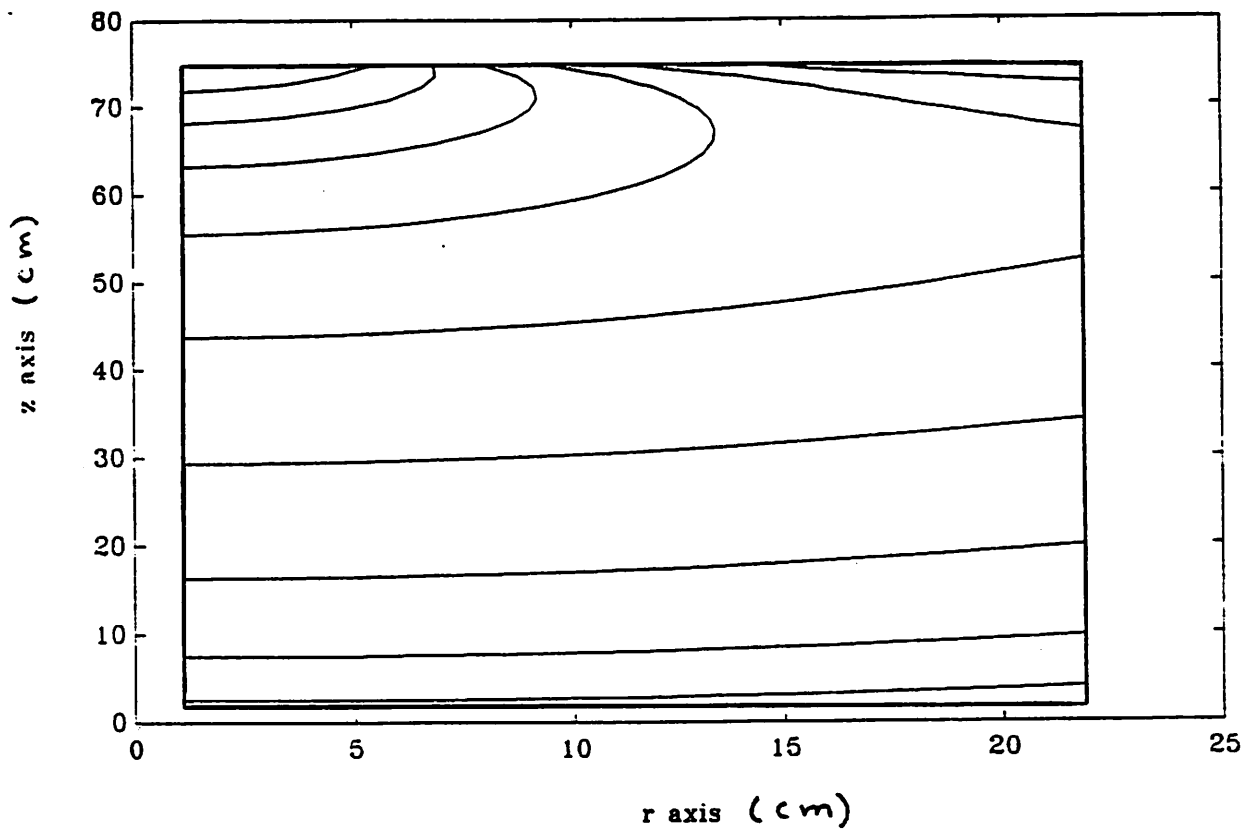


Fig. 24: Computed Argon Plasma Density Contours at $p = 1$ mTorr and With a Sidewall Reflectivity, $\rho = 0.9$

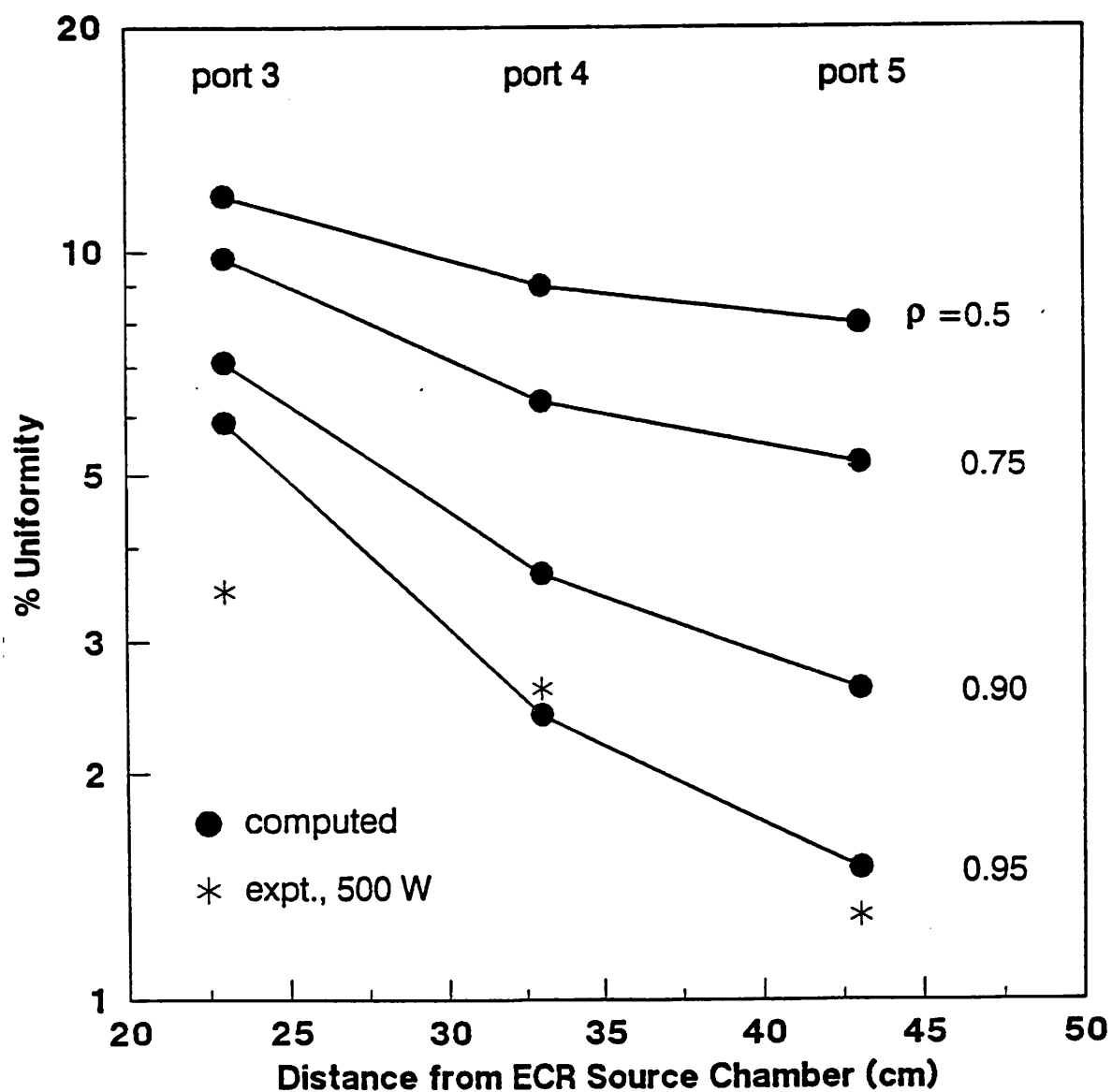


Fig. 25: Computed and Measured Argon Plasma Uniformity Vs. Axial Distance Across a 200 mm Diameter at $p = 1$ mTorr

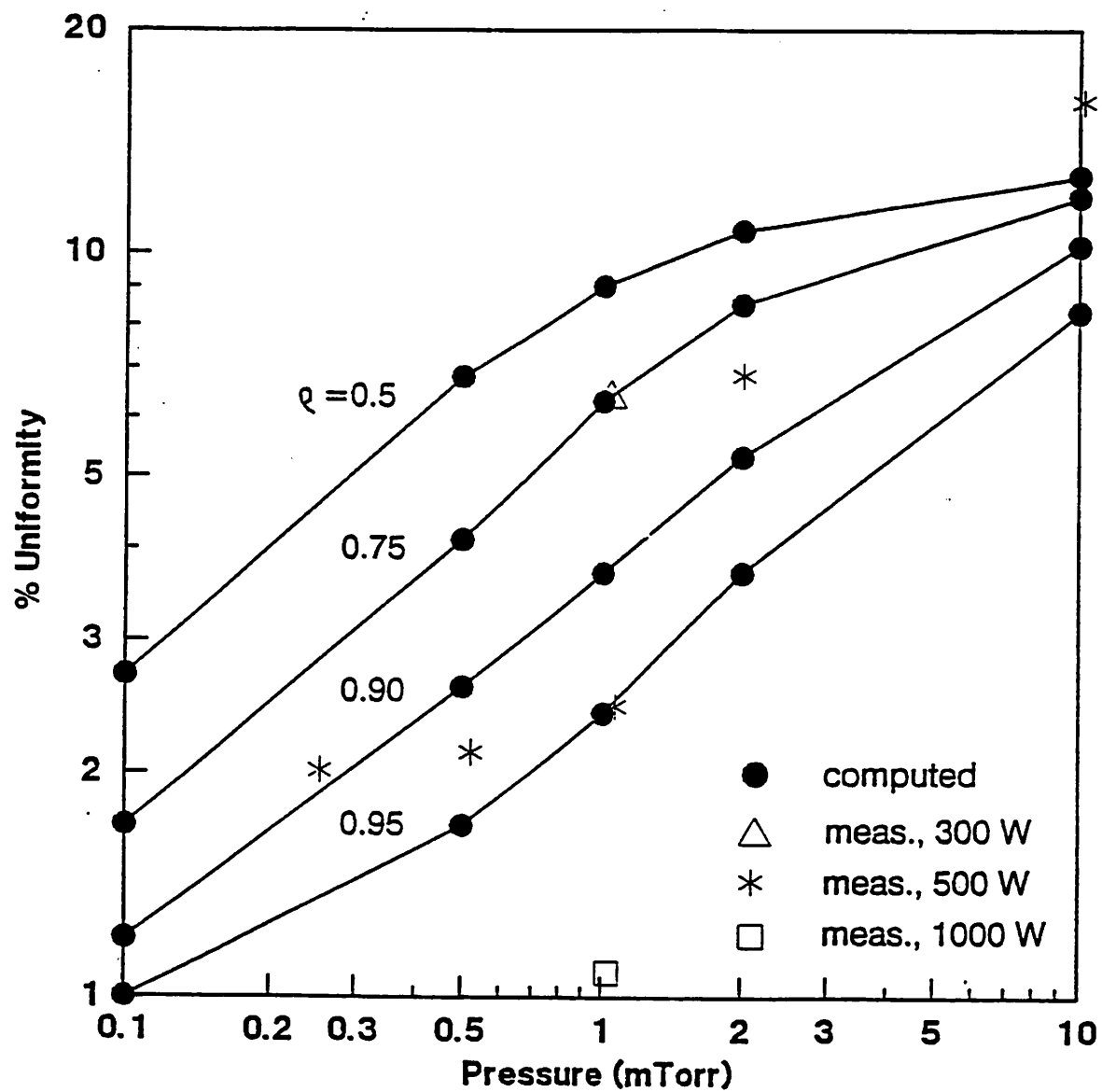


Fig. 26: Computed and Measured Argon Plasma Uniformity Vs. Pressure Across a 200 mm Diameter at Port 4.

path and resulting decrease in α . The measured variation of uniformity with microwave power at 1 mTorr is also shown. A uniformity of 1% is obtained for 1000 W microwave power and $p \leq 1.0$ mTorr.

In Fig. 27 the effect of the multidipole magnets and the iron shielding is shown by comparing the uniformity for the three configurations indicated above. The addition of the multidipole magnets results in improved uniformity over the entire pressure range, especially for $p \leq 1$ mTorr. The addition of the iron shielding results in a uniformity of 2-2.5% over the pressure range of 0.25-1.0 mTorr and 500 W microwave power.

Further studies of uniformity will be carried out with a wafer holder present in the process chamber. The simulations will be used to optimize the shape and location of the holder for the best uniformity and measurements will be made with an optimized wafer holder design.

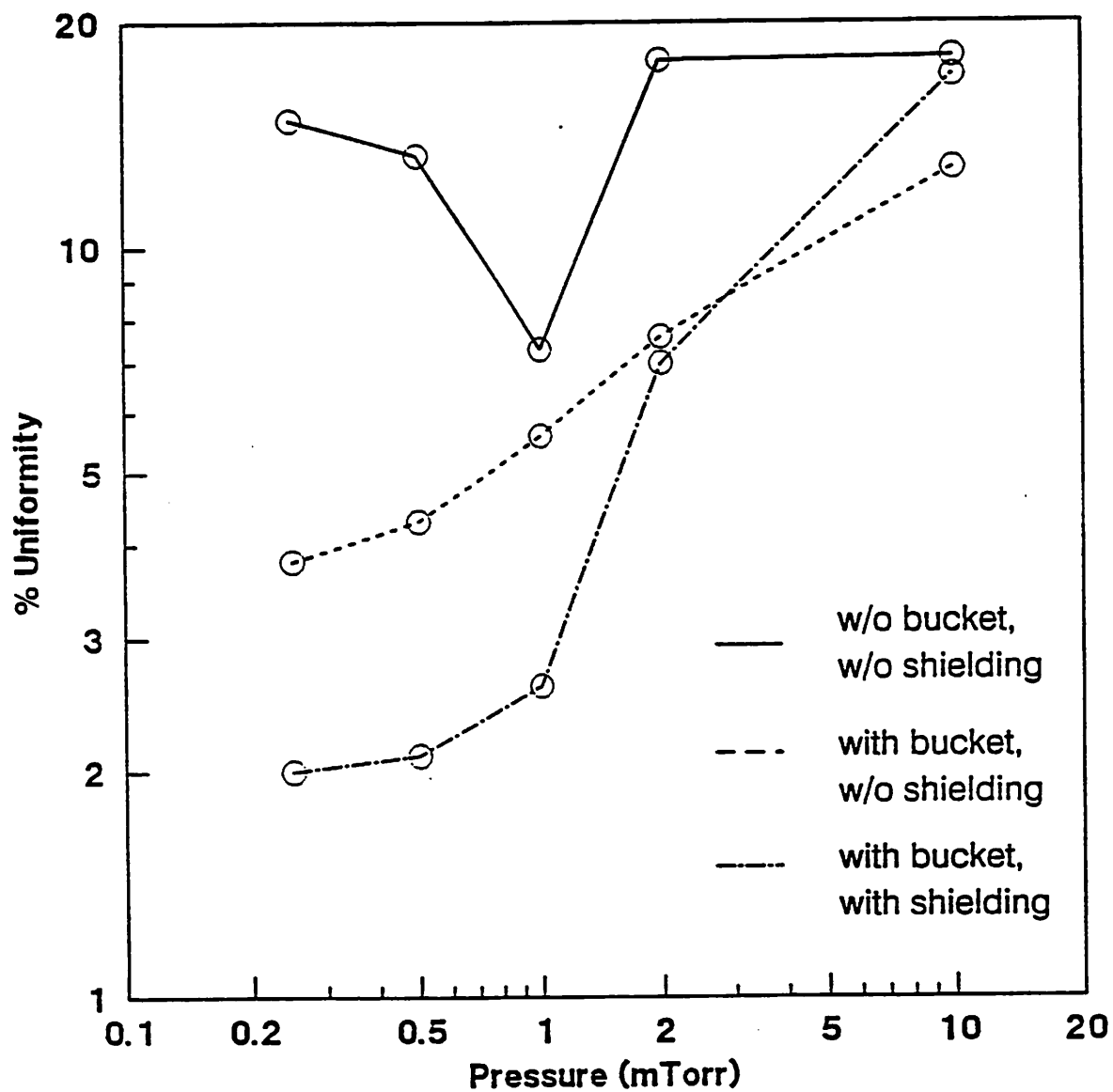


Fig. 27: Measured Argon Plasma Uniformity Vs. Pressure Across a 200 mm Diameter at Port 4 with 500 W Microwave Power

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3. X.Y. Qian, D.A. Carl, J. Benasso, N.W. Cheung, M.A. Lieberman, I. Brown, J.E. Galvin, R.A. MacGill and M.I. Current, "A Plasma Immersion Ion Implantation Reactor for ULSI Fabrication", *Nuclear Instrument and Methods*, B 55 (1990).
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9. R.A. Stewart and M.A. Lieberman, "Model of Plasma Immersion Ion Implantation for Voltage Pulses with Finite Rise- and Fall-Times", to appear in *Journal of Applied Physics*, see also *Report UCB/ERL*, M91/14, 21 February 1991.
10. R.A. Stewart, X.Y. Qian, D.A. Carl, B. Lake, Jr., J. Benasso, R. Lynch, C.A. Pico, M.A. Lieberman and N.W. Cheung, "Characterization of the Processing Plasma in an Engineering Prototype Reactor for Plasma Immersion Ion Implantation", *Report UCB/ERL*, M90/100, 12 November 1990.
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12. R.A. Stewart, B. Troyanovsky and M.A. Lieberman, "Modeling Magnetic Bucket Confinement in an ECR Plasma Processing Reactor", presented at the *18th IEEE International Conference on Plasma Science*.

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14. M.H. Kiang, C.A. Pico, J. Tao, R.A. Stewart, N.W. Cheung and M.A. Lieberman, "Selective Copper Plating in Silicon Dioxide Trenches with Metal Plasma Immersion Ion Implantation", to be published in the *Materials Research Society Proceedings*, Volume 223, Anaheim, CA., April 29-May 3, 1991.
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APPENDIX A

SELECTIVE COPPER PLATING IN SILICON DIOXIDE TRENCHES WITH METAL PLASMA IMMERSION ION IMPLANTATION

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ABSTRACT

Selective deposition of copper in SiO₂ trenches has been carried out using plasma immersion ion implantation and electroless Cu plating. To form the seed layer for electroless Cu plating on SiO₂, sputtered Pd and Si atoms were partially ionized by the Ar plasma and then deposited at bottoms of SiO₂ trenches; Ar ions also assisted the ion beam mixing of the deposited Pd/Si films with the SiO₂ substrate. We found a threshold Pd dose of $2-3 \times 10^{14}/\text{cm}^2$ is required to initiate the electroless plating of Cu. By controlling the Pd dose and the tapering angle of the SiO₂ trench sidewalls, 1 μm wide Cu filled lines with flat surfaces suitable for planarized multilevel metallization were successfully fabricated.

1. INTRODUCTION

Because of its low resistivity and good electromigration property, copper has been proposed as the interconnect material of choice for multilevel IC metallization and wafer-level packaging. Using Cu at the interconnection level and wiring metallization, such applications avoid its use in close proximity to silicon and thus eliminate the concerns over its effect on active devices in silicon [1]. However, the difficulty in patterning Cu has long presented a problem; reactive ion etching of Cu is difficult because the etching products are usually non-volatile. This constraint leads to some recent investigations in selective Cu deposition by chemical vapor deposition [2] or electroless plating [3]. To electroless plate Cu onto SiO₂ substrates, surface catalysts such as Pd are required as seeds to initial the plating process.

For multilevel interconnection technology, maintaining a planar structure improves lithography definition and metal step-coverage. This can be accomplished by selective metal filling of SiO₂ trenches. To seed the bottom of trenches without seeding the trench sidewalls, a directional deposition of the seeding layer is usually required over a large substrate area. Intermixing of the seed layer with the SiO₂ substrate will also improve the adhesion of the plated metal to SiO₂. These two requirements clearly show the advantage of ion-assisted deposition as compared with conventional evaporation or sputtering deposition techniques.

In our previous studies, we have demonstrated that by implanting W into SiO₂ trenches as a seeding layer, we can planarize the trenches by selective tungsten chemical vapor deposition [4]. We have also used plasma immersion ion implantation (PIII) of Pd into SiO₂ trenches to seed electroless plating of Cu [5]. The PIII technique has the following processing advantages: (1) It can provide a high dose rate of 10^{16} ions/cm²-sec over a large implanted area; (2) Using a triode configuration, metallic materials can be sputtered from a target and deposited on the

substrate; (3) Ions from the plasma gas (e.g. Ar) provides ion-beam mixing of the deposited materials with the substrate; (4) Part of the sputtered atoms will be ionized in the plasma and will be implanted into the substrate [6]. The resultant metal depth profile is a gradual transition from a metal-rich SiO₂ surface to pure SiO₂ substrate with a typical penetration depth of several hundred angstroms. This gradual transition of metal content is expected to improve the adhesion of the plated Cu film.

2. EXPERIMENTS

Shown in Figure 1 is a schematic of the PIII apparatus we used to produce the Pd/Si seeding layer with plasma immersion ion implantation. A sputtering target consisting of Pd and Si was introduced into the Ar plasma that was regulated at a pressure of 1-10 mTorr. We used an RF (8.4 MHz) power supply to bias the target negatively 200-260 V with respect to the chamber walls; Pd and Si atoms were sputtered off, with a small percent of them being ionized by the Ar plasma. A pulsed negative bias of 25 kV was applied to the wafer holder sitting in the downstream plasma to facilitate both the implantation and ion mixing processes. The pulses had a frequency of 100 Hz and a pulse duration of 2 μ sec.

Results from our previous experiments [5] showed that plated Cu films do not adhere well to pure Pd implanted SiO₂ substrates. In this experiment, we studied the use of Pd/Si alloy as the seeding layer. Figure 2 shows the process sequences of our experiments. 1 μ m thick SiO₂ films were grown on Si wafers by wet oxidation at 1100 °C for 2.5 hours. We used photoresist to pattern the oxide, and then made the oxide trenches to a depth of approximately 5500 Å by reactive ion etching (RIE) in a CF₄:CHF₃:He plasma ambient. Using the patterning photoresist on the oxide substrate as the implantation mask, we performed Pd/Si PIII to form the catalytic seed layer and then removed the photoresist with acetone. To investigate the effect of Pd depth profile on Cu film adherence, two different process flows were employed during PIII:

(1) One-step deposition. The RF target bias and the pulsed wafer bias were applied simultaneously, i.e., Pd and Si deposition and implantation will occur simultaneously. Ar ion bombardment will facilitate ion-mixing.

(2) Two-step deposition. The target was biased while no high voltage pulse was applied to the wafer. Sputtered Pd and Si atoms were deposited onto the wafer. The RF power to the Pd/Si target was turned off after the deposition had proceeded for a certain period. By applying negative high voltage pulses to the wafer, Ar ion bombardment will facilitate ion-mixing of the deposited Pd/Si film with the SiO₂ substrate.

After PIII, the samples were rinsed in deionized water and subsequently immersed in an electroless Cu plating solution [7] which was kept at a temperature of about 60 °C. The pH value of the solution was 13, and the rate of electroless Cu deposition under this condition is about 1.3 μ m/hour.

To determine the areal density of the deposited/implanted Pd and Si doses, we used bare silicon wafers and carbon substrates as monitors which were analyzed by Rutherford Backscattering Spectroscopy (RBS). The depth profiles of Pd and Ar can be characterized by RBS when a glancing angle detector is used.

3. RESULTS AND DISCUSSIONS

A catalytic surface is needed for the electroless deposition of Cu to take place. In order to determine the seeding possibilities, we investigated various material substrates (e.g. metal foils) by immersing them in the plating solution for 30 minutes. We found that several substrate materials can initiate electroless Cu plating process. The results are listed in Table I.

Table I					
Results of Electroless Cu Plating Initiation					
Does plate	Pd	Cu	Co	Ni	Pb
Does not plate	Cr	Al	Ti	W	Si

Pd was chosen as the seed layer material in order to eliminate the need for PdCl₂ treatment conventionally employed to activate the substrate on which Cu is to be plated [8]. Si was also

included in the target in the effort to improve the adhesion of implanted Pd with oxide substrates; we, in fact, observed better adhesion of the plated Cu films to Pd/Si implanted substrates than to substrates that were implanted with only Pd. We have also tested Ar implanted oxide substrates and found no seeding of Cu to occur on those samples. This observation suggests that surface chemistry rather than ion-induced damage is responsible for initiation of the Cu plating process.

Samples treated by PIII with various plasma and bias conditions were cleaned and dipped into electroless Cu plating solution. Figure 3 shows the observations after 30 minutes of Cu plating and the corresponding Pd doses measured by RBS. We see a threshold Pd dose of $2-3 \times 10^{14}/\text{cm}^2$ is required for Cu plating to occur. The threshold dose for Cu plating is found to be insensitive to the Si doses. Figure 4 are examples of implanted trenches that have nearly vertical sidewalls and a nominal Pd dose of $5.8 \times 10^{15}/\text{cm}^2$ filled by electroless Cu after plated for 25 minutes. With Si doses around $3 \times 10^{16}/\text{cm}^2$, adhesion of the Cu is excellent. The scanning electron microscopy (SEM) micrographs show a flat surface of the Cu film for trenches of 1 μm and 3 μm in widths, respectively.

In Figure 5, we show RBS analysis of plated samples that have been plated for 5 minutes at 70 °C. A threshold Pd dose is again observed around $2 \times 10^{14}/\text{cm}^2$. A linear dependence of the deposited Cu thickness on the Pd dose implies that electroless Cu nucleates at separate Pd sites into islands of hundreds of angstroms in diameter before they connect to each other and form a continuous layer. This mechanism is verified by SEM (Figure 6(a)) of some plated trenches: sporadic Cu grains were forming on the sidewall of the trench, while its bottom is completely covered by continuous Cu. For oxide trenches having slightly tapered sidewalls ($\theta \geq 0^\circ$, see insert of Figure 7) created by mask erosion during RIE, the areal density of Pd dose on the sidewall is proportional to $\sin\theta$. With a maximum Pd dose at the bottom of the trench ($\theta = 90^\circ$) greatly exceeds the threshold dose, the sidewall dose may acquire a value around the threshold dose if θ is larger than zero. In some severe events such as Figure 6(b) showing SEM micrograph taken at another site of the same wafer, the trench sidewall have already been covered by deposited Cu. Therefore, to avoid Cu nucleating on the sidewall which would eventually lead to keyhole formation in filled oxide trenches, care must be taken to achieve nearly vertical trench sidewalls and not to use an excessive dose of Pd.

With a plasma gas pressure at 1 mTorr, the mean free paths between gas molecules collisions is about 4 cm, which is much larger than the sheath thickness between the substrate and the plasma. Therefore, we can assume near-normal incidence of the impinging ions. The plot of Figure 7 presents the calculated maximum allowed tapering angle θ_M versus Pd dose such that the sidewall Pd dose ($\propto \sin\theta$) does not exceed the threshold of $3 \times 10^{14}/\text{cm}^2$.

RBS analysis of Pd profiles of the two deposition procedures shows different depth distributions (Figure 8). For the 1-step process, the Pd peak concentration is located at about 80 Å beneath the surface. For the 2-step process, the Pd profile extends into the substrate to a depth of ≈ 400 Å. With the two-step process, Cu can be plated to a larger thickness before peeling off from the substrate. We therefore propose that by a more thorough mixing of the deposited Pd/Si film with SiO_2 substrate instead of having a sharp transition at the interface, better mechanical support was obtained to improve the adhesion.

4. CONCLUSION

We demonstrated plasma immersion ion implantation is a feasible technology to form the seed layer on SiO_2 for selective Cu plating. With proper RIE process control of oxide trench sidewalls and a suitable choice of Pd dose, planarized Cu-filled SiO_2 trenches were successfully obtained.

5. ACKNOWLEDGEMENTS

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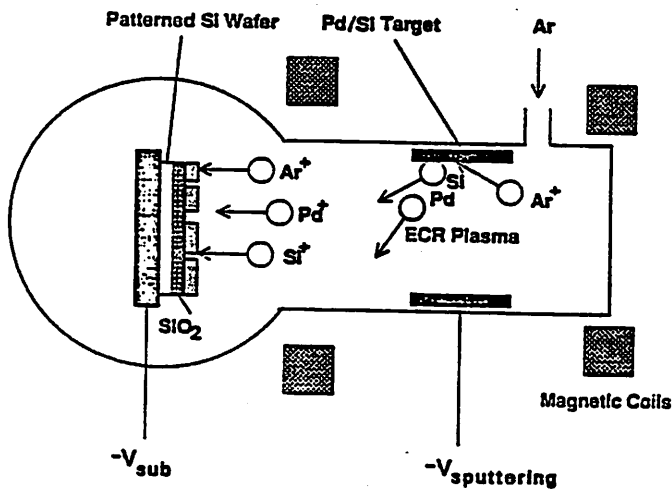


Fig. 1 Schematic of Pd/Si plasma immersion ion implantation for selective Cu plating seed layer formation.

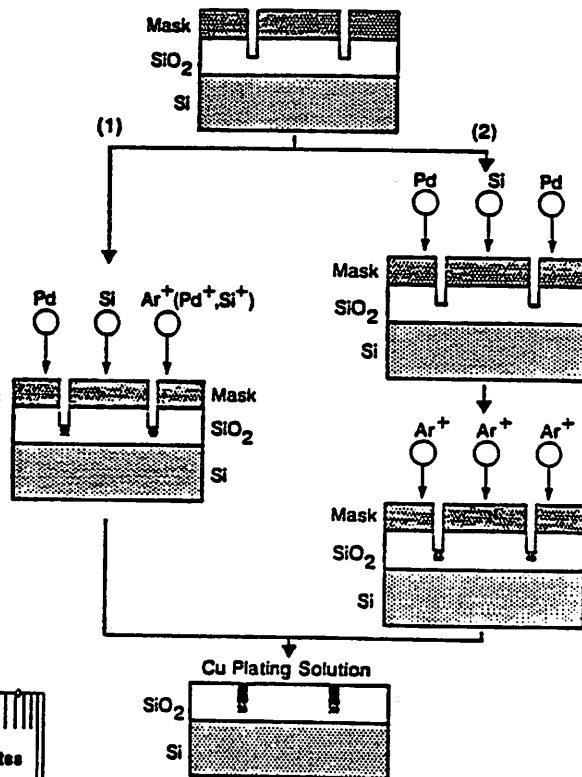


Fig. 2 Process sequences: (1) One-step deposition: Simultaneous Pd/Si deposition and ion-mixing. (2) Two-step deposition: Pd/Si film deposition followed by Ar^+ ion-mixing.

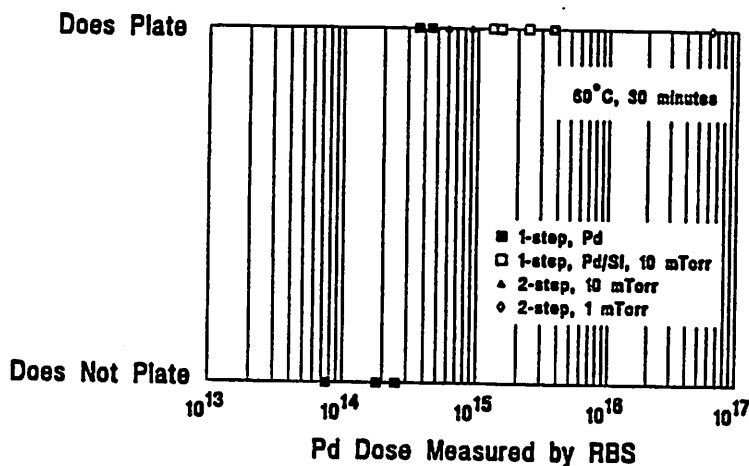
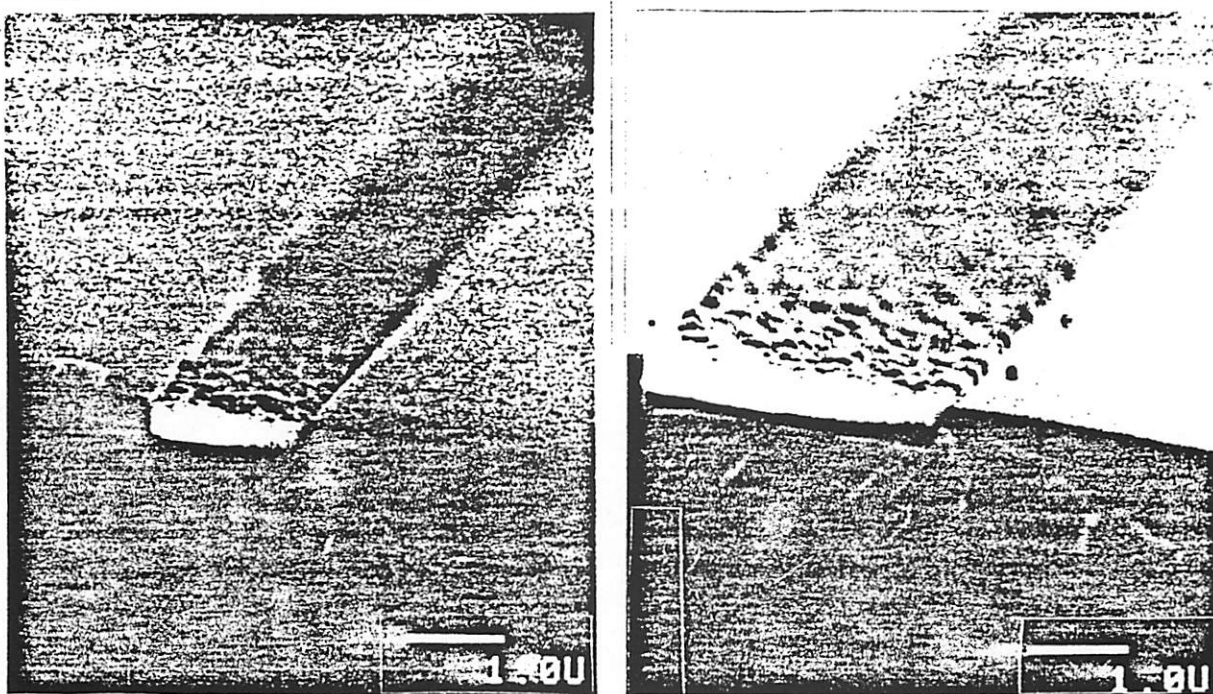


Fig. 3 Diagram showing the dependence of Cu plating on Pd dose. The threshold Pd PIII dose is about $2\text{--}3 \times 10^{14} \text{ cm}^{-2}$. Samples treated by PIII were immersed in Cu plating solution for 30 minutes at 60°C .

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(a)

(b)

Fig. 4 SEM micrographs of cross-sections of trenches filled with Cu. The SiO₂ trenches are 0.55 μm deep, (a) 1 μm wide, and (b) 3 μm wide, respectively. The trenches were treated by the two-step Pd/Si PIII process. The nominal doses for the Pd and Si are $5.8 \times 10^{15}/\text{cm}^2$, and $3 \times 10^{16}/\text{cm}^2$ respectively.

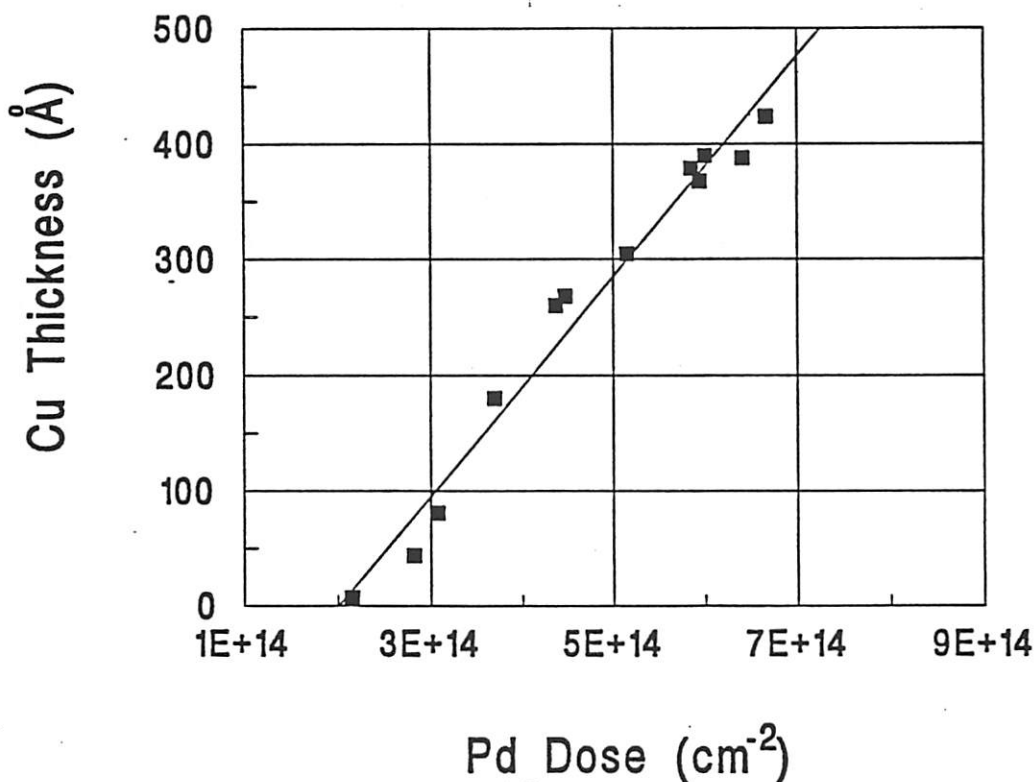


Fig. 5 Deposited Cu thickness versus Pd dose. Electroless Cu was plated for 5 minutes at 70°C.