THE SELECTIVE EPITAXY OF SILICON AT LOW TEMPERATURES

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Jen-Chung Lou

Memorandum No. UCB/ERL M91/70

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Dedicated to my wife, Judy,
and my children, Kai-Ming, Kai-Jye, and Kevin

The Selective Epitaxy of Silicon at Low Temperatures

Jen-Chung Lou

Ph.D. Dissertation

Department of Electrical Engineering and Computer Sciences

Abstract

This dissertation has developed a process for the selective epitaxial growth (SEG) of silicon at low temperatures using a dichlorosilane-hydrogen mixture in a hot-wall low pressure chemical vapor deposition (LPCVD) reactor. Some basic issues concerning the quality of epilayers--substrate preparation, ex-situ and in-situ cleaning, and deposition cycle, have been studied.

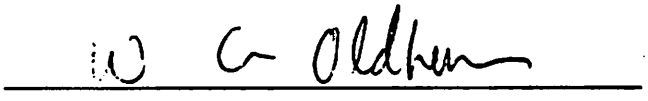
We find it necessary to use a plasma etch to open epitaxial windows for the SEG of Si. A cycled plasma etch, a thin sacrificial oxide growth, and an oxide etching step can completely remove plasma-etch-induced surface damage and contaminants, which result in high quality epilayers.

A practical wafer cleaning step is developed for low temperature Si epitaxial growth. An ex-situ HF vapor treatment can completely remove chemical oxide from the silicon surface and retard the reoxidation of the silicon surface. An in-situ low-concentration DCS cycle can aid in decomposition of surface oxide during a 900°C H_2 prebake step. An HF vapor treatment combined with a low-concentration of DCS cycle consistently achieves defect-free epilayers at 850°C and lower temperatures. We also show that a BF_2^+ or F^+ ion implantation is a potential ex-situ wafer cleaning process for SEG of Si at low temperatures.

The mechanism for the formation of surface features on Si epilayers is also

discussed. Based on O^+ ion implantation, we showed that the oxygen incorporation in silicon epilayers suppresses the Si growth rate. Therefore, we attribute the formation of surface features to the local reduction of the Si growth rate due to the dissolution of oxide islands at the epi/substrate interface.

Finally, with this developed process for the SEG of silicon, defect-free overgrown epilayers are also obtained. This achievement demonstrates the feasibility for the future silicon-on-oxide (SOI) manufacturing technology.



Professor William G. Oldham

Committee Chairman

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Chapter 1

Introduction

As integrated circuit technology progresses to meet submicron ultra-large scale integration (ULSI) applications, enhancing the ability to increase the packing density and further improve the down-scaling has become urgent. An example is the isolation application. Many isolation techniques have been developed to reduce the spacing required for the electrical isolation of adjacent devices. Recently, an alternative isolation scheme using selective epitaxial growth (SEG) has been developed. It is a very promising device isolation technology for fabricating integrated circuit devices in the submicron regime [1-7]. Selective epitaxial growth is an epitaxial technology wherein a silicon layer can be selectively grown on an exposed substrate, but not on an oxide field area. The growth limitation is due to the suppression of poly-Si nucleation on the oxide. The epitaxial regions are used to fabricate active devices, while the oxide serves as a lateral electrical isolation. A major characteristic of SEG is the reduction of process steps over other methods [8], which improves yield. The SEG process requires only four process steps -- one oxidation for isolation, one plasma etching step to define the epitaxial windows, one sacrificial oxide to remove the surface damage and one low pressure chemical vapor deposition (LPCVD) epitaxial process to grow Si epilayers.

The motivation for the use of the selective epitaxial growth (SEG) of silicon is the desire to fabricate novel devices with high performance, as well as to improve the device isolation in integrated circuits. There are several attractive applications for the SEG of Si in the areas of advanced devices. Some are: 1) refilling the epitaxial Si into the Si wells of opposite conductivity type for CMOS and BICMOS device fabrication, 2) formation of Si pedestals contacted with doped

poly-Si from sidewalls for high speed bipolar transistors. 3) growing silicon epilayers in the trenches or in the grooves which are etched in a silicon substrate and are coated with a dielectric film, 4) growth of silicon islands inside the window of dielectric film on the Si substrate, and 5) formation of the lateral overgrowth of silicon over the dielectric film. High quality Si epilayers are required for these applications.

Selective epitaxial growth of Si requires low temperature and low pressure growth techniques. The key issues for obtaining high quality selective epitaxial grown Si epilayers at low temperatures are, 1) ex-situ wafer-clean process, 2) reactor environment, and 3) process cycle. Improper process steps result in defective epilayers which show undercuts, voids, microtwins, dislocations, interfacial oxide islands, pits, and textured surface features [9-11]. Therefore, the goal of this study is to illustrate the basic issues in the selective epitaxy of silicon, and then correlate these issues with the wafer preparation, the deposition cycle, and the growth parameters to develop a process to grow high quality epilayers at low temperatures.

The most important two factors in controlling the epitaxial quality are the ex-situ and the in-situ wafer-clean processes. After the pre-epitaxial clean step and the wafer loading into the reactor, we previously employed a high temperature prebake (at 1000°C) in H_2 to remove the surface oxide for obtaining good epilayers. However, a high temperature prebake can cause large undercuts [12] which result in rough pattern edges. Therefore, a low temperature prebake (at or below 900°C) is necessary. But with a low temperature prebake, the quality of epilayers is more seriously influenced by the adsorption of gas-phase components (e.g. background H_2O and O_2) which can result in oxide patches on the Si surface prior to the deposition [13,14]. Consequently, defective epilayers are obtained. In order to obtain high quality epilayers at lower temperatures, a systematic study about the wafer preparation, the deposition cycle, and the growth parameters is carried out. In this

study we have developed an ex-situ HF vapor treatment and an in-situ low-concentration of dichlorosilane (DCS) step to enhance the surface oxide removal prior to the deposition, resulting in high quality epilayers [15,16]. Defect-free epilayers deposited at 850°C after a 900°C prebake are obtained. Chapter 2 describes a matrix experiment which reveals the necessity of the ex-situ HF vapor treatment and determines the time to start the addition of a small DCS in the deposition cycle. Chapter 3 deals with the details of the HF vapor treatment. The influence of the compositon of H_2O:HF mixtures and the exposure duration on the quality of epilayers, and the mechanism to explain the effect of the fluorine incorporation on the surface oxide removal are also discussed. Chapter 4 concerns the plasma etch effects on the quality of epilayers. It is found that a sacrificial oxide layer is necessary for the removal of the plasma-etch-induced near-surface defects and contaminants. A 5 nm sacrificial oxide film is shown to be adequate to achieve high quality epilayers. In chapter 5, microstructural analysis reveals the relationship between surface morphology of epilayers and oxide islands at the epi/substrate interface. It shows that the dissolution of interfacial oxide islands can locally depress the Si growth rate and result in pits or textured features on the surface of epilayers. Chapter 6 discusses future works in the selective epitaxial growth of silicon. Finally, in chapter 7 we summarize results of this study.

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Chapter 2

Effects of Ex-situ and In-situ Clean Processes on the Quality of Low-Temperature Selectively Grown Si Epilayers

The characteristics of low-temperature selective epitaxial growth (SEG) of silicon using a dichlorosilane-hydrogen mixture in a low pressure chemical vapor deposition (LPCVD) hot-wall reactor are discussed with respect to the wafer preparation and the deposition cycle. With lower process temperatures, the epitaxial quality is highly sensitive to the non-volatile contaminants on the wafer surface. We find that a clean surface with a minimum of "native" oxide is necessary outside the reactor, and also a suitable prebake cycle used to remove residual oxide films prior to the deposition is inevitable inside the reactor. The purpose of this chapter is to present an ex-situ and an in-situ clean processes for the growth of high quality epi-layers at low temperatures. A simple HF vapor treatment with regard to the removal of surface oxide as well as the hydrogen and the fluorine passivation of Si surface prior to reactor loading has been employed to improve the epitaxial quality. Inside the reactor the addition of a low-concentration of dichlorosilane to the H_2 ambient in the deposition cycle is also applied to get further improvement. Using crystallgraphic defect analyses, the mechanism and the optimal time to apply a low concentration of dicholorsilane (DCS) in the deposition cycle are studied in detail to get high quality epitaxial layers. With these two process improvements, defect-free selectively overgrown Si epitaxial layers are obtained at 850°C and lower deposition temperatures.

2.1 The Motivation to Study the Ex-Situ and the In-Situ Clean Processes

Low temperature processing and down-scaling are main avenues to submicron technology development. With the potential of making compact structures; therefore, the use of selective epitaxial growth (SEG) of silicon has recently been developed as an important manufacturing technology for submicron ULSI applications [1-4]. The major advantage of SEG is in the reduction of process steps because this technique needs only one oxidation for isolation, one plasma etch to define the active area spacing, a thin sacrificial oxide to remove surface damage and one low pressure chemical vapor deposition (LPCVD) process to achieve the selective epitaxial growth of Si.

If wafers are loaded from an environment containing O_2 and H_2O, a finite amount of "native" oxide is unavoidable. Although a high temperature prebake can remove "native" oxide films to achieve SEG of Si, significant undercuts are obtained by the reduction of H_2 to SiO_2 at the SiO_2/Si interface [5]. Furthermore, this high temperature prebake can result in serious interdiffusion in abrupt juctions and shallow junctions, thus degrading the device performance. In order to eliminate the formation of undercuts and the interdiffusion of juctions, a low temperature SEG of Si is required. The three key issues for obtaining high quality SEG at low temperatures are the surface preparation of wafers so that an oxide- and carbon-free surface is presented in the start of the deposition cycle, the prebake cycle to volitalize interfacial oxide films, and the control of the reactor environment so that no surface contamination occurs in the reactor prior to or during growth.

It is found that the epitaxial quality is seriously influenced by the background concentration of H_2O and O_2 in the reactor. As a way to reduce the background concentration of H_2O and O_2 during the low temperature deposition cycle, we have found that the addition of a low concentration of dicholorsilane (DCS) immediately during or after the prebake can improve the epitaxial growth at 850°C. However, this modification is still insufficient to completely remove the surface

oxide to achieve high quality epilayers. Recently, we also have shown a simple HF vapor treatment performed prior to the loading of wafers into the reactor can remove "native" oxide [6-7]. In particular, a 5 second exposure to a vapor of a 1:2 mixture of H_2O:HF was found very effective when followed by a 900°C hydrogen prebake prior to the epitaxial deposition. With an ex-situ HF vapor treatment; however, we found the quality of epilayers still highly depend on the time to start the addition of a low-concentration of DCS in the deposition cycle. Epitaxial results varied from defect-free area to large numbers of visible and decoratable features, especially along the oxide sidewalls. Therefore, the object of this paper is to show the beneficial role of an ex-situ HF vapor treatment and a low concentration of DCS prior to ramp down to the growth temperature. With macrostructure and microstructure analyses, it is found that the DCS cycle combined with the ex-situ HF vapor treatment allows for defect-free overgrown Si epitaxial layers deposited at 850°C and lower temperatures.

2.2 Substrate Preparation and Experimental Procedure

The growth of epitaxial films is carried out in a horizontal hot-wall reactor using dichlorosilane (DCS) and H_2 gases. The epitaxial substrates are 4-inch P-type (100) Si wafers with 30-50 ohm-cm resistivity. A 570 nm thermal oxide layer is grown at 1000°C. A conventional photolithography step is used to delineate the bare and oxide-covered regions. In order to minimize the sidewall direction induced defects, the structures on the test pattern mask have been aligned along the <100> direction instead of the commonly used <110> direction [8]. After plasma etching and photoresist removal, a 25 nm sacrificial oxide is grown at 900°C and stripped by dilute HF soltuion to eliminate any plasma etch induced surface damage. The standard pre-epitaxial clean steps consists of two H_2SO_4-H_2O_2 cleaning treatments. separated by a dilute HF dip that removes the sacrificial oxide. After the clean, the

wafers are exposed to the vapor over a 1:2 mixture of H_2O:49% HF for 5 seconds to remove the chemical oxide resulting from the second piranha clean, then immediately loaded into the hot-wall reactor at 525°C. All wafers are subjected to a 15 min 900°C prebake in a 6 torr H_2 ambient prior to ramping down the temperature to the deposition temperature. The ramp down to the growth temperature of 850°C takes 20 min. Deposition takes place in a 7.4% DCS mixed in H_2 at 0.6 torr. The basic process cycle is illustrated in Fig. 1 where the time T_1 is used to represent that we add a 0.025% low-concentration flow of DCS prior to the deposition step in some of the experiments.

The surface morphology of epitaxial films is inspected by Nomarski microscopy and the electron scanning microscopy (SEM). The epitaxial film thickness is measured by AS-200 Alpha Step. The crystallgraphic defects are studied by dilute Schimmel etch [9], plane-view and cross-sectional transmission electron microscopy (TEM). The concentration profile of impurities in epitaxial layers is determined by secondary ion mass spectroscopy (SIMS) analysis.

2.3. The Selective Epitaxial Growth Using an Ex-Situ and an In-Situ Clean Processes

For the purpose of showing the effects of an ex-situ HF vapor treatment and also revealing the function of an in-situ low concentration of DCS in the prebake and the ramp down steps, control experiments are performed to explore their effects. The growth parameters are listed in Table 1.

2.3.1 The Necessity of HF vapor Treatment in the Selective Epitaxial Growth of Si at Low Temperatures

In the Exp. N_1, the ex-situ HF vapor treatment and the addition of a low concentration of DCS are not applied. The Nomarski micrograph in Fig. 2 illus-

trates a rough surface morphology on the whole wafer. Most of areas show dense hillocks of epitaxial Si. The sidewall of hillocks is along <110> directions. Because of the high partial pressure of background oxidants, it is believed that the 900°C prebake and the ramp down steps can never efficiently remove the "native" oxide film but only create dense pinholes of exposed Si on continuous oxide areas. Since the epitaxy of silicon is highly selective, the deposition starts on these small exposed Si areas only, thereafter, forms dense hillocks of Si on the unremoved oxide films. In addition, the edges at masking oxide/substrate interface become very rough after the deposition. It is believed that the attack by H_2 on the masking oxide/substrate interface occurs in the prebake and the ramp down steps, and then results in roughening edge profiles of the mask [5].

In the Exp. N_2, the ex-situ HF vapor treatment is not applied but a low-concentration of DCS is added in the 900°C prebake and the ramp down steps. As shown in Fig. 3(a), the Nomarski micrograph of the epitaxial Si layer deposited at 850°C indicates a textured surface morphology on the whole wafer. Furthermore, the cross-sectional transmission electron microscopy (XTEM) micrograph shown in Fig. 3(b) indicates a non-specular epilayer with a high density of oxide islands at the epi/substrate interface and many threading dislocations that originate near the interface. The size of oxide islands is between 0.5 um and 5 um. It is believed that Si starts to deposit on exposed Si areas only, then laterally grows over these discrete oxide islands completely. Consequently, it shows concave overgrown Si layers right top over oxide islands. It is obvious that these interfacial oxide islands result in a rough surface morphology. In addition, SIMS analysis in Fig. 4 shows a large oxygen peak of about 1.5×10^{20} cm^{-3}, a carbon peak, and a fluorine peak at the epi/substrate interface. It is believed that this fluorine peak is attributed to the HF dip in the wafer clean step. Comparing these results with those in Fig.2, they indicate that the addition of a small concentration of DCS in the 900°C prebake and the

ramp down steps can speed the removal of interfacial oxide film and result in more exposed Si areas, but many discrete oxide islands exist at the interface. The presence of these oxide islands does not prevent epitaxy but leads to the formation of defects at the epi/substrate interface, at the epi/oxide sidewall interface and in epitaxial layers. Consequently, a textured epilayer is obtained. The possible effect of a low DCS on the improvement of Si epitaxy will be discussed later.

2.3.2 Effects of a Small DCS on the Quality of Epilayers

As mentioned above, it is understood that in the absence of an ex-situ HF vapor treatment, applying the conventional wafer clean process with or without an addition of a low concentration of DCS in the subsequent 900°C prebake and ramp down steps is not efficient to remove the native oxide prior to the deposition. We therefore apply an ex-situ HF vapor treatment for the following W_N series experiments to see if the surface oxide can be efficiently removed.

In the Exp. W_1 with the ex-situ HF vapor treatment only but without any low concentration of DCS in the prebake and the ramp down steps, the surface morphology shown in Fig. 5 is more textured than that of wafer in Fig.3 which received no HF vapor treatment but a low-concentration of DCS during the prebake and the ramp down steps. Also, the dimension of these concave areas is smaller than that of wafers in Fig. 3. This suggests a high density of smaller interfacial oxide islands at the epi/substrate interface for the HF vapor exposed wafers. Plane-view TEM micrograph shows that an oxide island is delineated underneath every concave area. SIMS analyses in Fig. 6 show an O_2 peak with the concentration of $3x10^{18}cm^{-3}$ and $4x10^{19}cm^{-3}$ at the epi/substrate interface for the textured epilayers in the center and near the peripheral of wafers, respectively. Because this O_2 peak is about 1 order or 2 orders of magnitude smaller than the O_2 peak observed for wafers not receiving an HF vapor treatment, the ex-situ HF vapor treatment presents

the success in reducing the total amount of interfacial oxide on the wafers that must be removed during the prebake and the ramp down steps.

In the Exp. W_2 the small concentration of DCS is turned on during the ramp down step only. As shown in Fig. 7(a), the deposition produces largely planar epilayers with no visible defects in the center of wafers. However, the epitaxial film along the edges of the oxide patterns is slightly rough. In addition, the plane-view TEM in Fig. 7(b) also clearly reveals this roughness of edges. It is believed that the presence of oxide undercuts, formed during the 900°C prebake step, along the bottom edge of the oxide patterns result in the roughness of edges. For these planar areas in the center of wafers, as shown in Fig. 7(c) to 7(f), the cross-sectional TEM, dilute Schimmel etch and SIMS do not show any interfacial oxide islands. In addition, there are also areas on the wafers where the epitaxial silicon displays another type of surface feature called square patterns. As illustrated in Fig.8, after a dilute Schimmel etch it shows a high density of etch pits at the epi/substrate interface in areas with square patterns. SIMS analysis in Fig. 9 indicates a weak O_2 peak of $1.5x10^{18}cm^{-3}$ at the epi/substrate interface for these areas with square patterns. Dilute Schimmel etch and SIMS results suggest that these etched pits decorate small interfacial oxide islands buried by the epitaxial layer. Furthermore, the peripheral areas of wafers show a textured surface morphology. In between there is a ringed area with concave pits. It is believed that the oxygen depletion along the counter-radial direction yields a defect-free area in the center of wafers, textured epilayers near the peripheral region, and epilayers with pits in the ringed region. The Nomarski micrograph in Fig. 10(a) shows a specular surface with concave pits in which the edges are along the <110> directions. The dimension of pits is around 1 um. It is further found that there are sparse pits in the inner region of this ringed area, but dense pits in the outer region of this ringed areas. Interestingly, dilute Schimmel etch in Fig. 10(b), 10(c) and 10(d) shows the same scale of the number of etched

pits at the epi/substrate interface in the inner and the outer regions of the ringed area. SIMS analysis in Fig. 11 also shows the same order of magnitude of oxide signal of $2x10^{19}cm^{-3}$ in the whole area of this ringed area where the density of pits ranging from 10^4cm^{-2} to $5x10^6cm^{-2}$. It is proposed that in the inner region of the ringed area there are more smaller oxide islands but few larger oxide islands; however, in the outer region of the ringed area there are more larger oxide islands but few smaller oxide islands. Because most of smaller interfacial oxide islands are buried after the deposition, it illustrates a planar surface with sparse pits in the inner region of the ringed area, but dense pits in the outer region of the ringed area. Based on the results of the dilute Schimmel etch and SIMS analysis, it indicates that with this kind of deposition cycle as long as pits are observed on the epitaxial films, there are dense oxide islands at the epi/substrate interface.

It is found in Exp. W_3 that initiating a low concentration of DCS earlier during the prebake cycle can further improve the epitaxial quality. Fig. 12 shows the surface of a typical wafer in which the addition of a low concentration of DCS is begun at the start of the 15 minutes prebake at 900°C. There are no pits or visible defects on the epitaxial surface, and the epitaxial edges along the oxide sidewalls are very smooth. Plane-view TEM in Fig. 13(a) shows very smooth epi/oxide edges even at a very high magnification and also show no oxide islands at epi/substrate interface. Cross-sectional TEM's in Fig. 13(b) verifies the absence of any defects in the epitaxial layers. It further shows no undercuts at corners of oxide. SIMS analysis in Fig. 14 does not indicate any oxygen peak at the epi/substrate interface, and the dilute Schimmel etch in Fig. 15(a) and 15(b) reveals no oxide-island-related etched pits at the epi/substrate interface either. Comparing with the results in the Exp. W_2, it is understood that, besides the addition of a low-concentration of DCS in the ramp down step, a small concentration of DCS in the 900°C prebake step is also necessary to further enhance the removal of the native

oxide and results in a clean surface prior to the deposition.

With the same deposition cycle of the Exp. W_3, overgrowth of small oxide features is also achieved for extended deposition duration. The Nomarski micrograph in Fig. 16(a) illustrates the high quality of a 3.3 um thick film grown during a 10 hour deposition at 850°C. It shows specular overgrown epilayers on areas with narrower oxide lines. Also, for wider oxide features, it shows no Si nuclei on oxide regions. The cross-sectional SEM micrograph of the same sample in Fig. 16(b) further indicates a specular overgrown epilayer. In addition, the cross-sectional TEM micrograph in Fig. 16(c) verifies the defect-free nature of epitaxial film which in this region completely covers a series of oxide lines. With different reflection g vectors to study the quality of this overgrown epilayer, no oxide undercut can be observed, and no oxide islands and other defects are found at the epi/substrate interface. Also, no seams and dislocations are observed where the overgrown fronts have joined above the middle of each oxide line. It is obvious that this overgrown epilayer deposited at 850°C is defect-free.

Based on the results of Exp. W_2 and W_3, it is found that the complete removal of surface oxide prior to the deposition and the edge roughness of epilayers are dependent on the addition of a small DCS in the deposition cycle. However, the detail in the initial stage is still unclear. In order to further understand the effect of a small amount of DCS to the epitaxial growth during the 900°C prebake and the ramp down steps, short time deposition in the prebake and the ramp down steps using a low-concentration of DCS (2 cc/min) is investigated. The deposition cycle is shown in Fig. 17. In the Exp. W_{AB}, as illustrated in Fig. 18(a), a thin epitaxial layer resulted from the deposition of a low-concentration of DCS in the 900°C prebake (step A) and the ramp down (step B) steps shows a specular surface morphology with smooth epi/patterned oxide edges on the whole wafer. The film thickness is between 10 nm and 60 nm. After the patterned oxide is stripped by a dilute HF

solution, in Fig. 18(b) it still shows an epilayer with smooth edges and a specular surface morphology. However, for the Exp. W_B, as shown in Fig. 19(a), adding the low-concentration of DCS only during the ramp down step yields dense pits and rough edges on most of areas of wafers. These pits are either buried oxide island related or partially overgrown oxide islands related. The film thickness is between 10 nm and 40 nm. After the patterned oxide is stripped by a dilute HF solution, in Fig. 19(b), it reveals dense Si irregularities at edges of patterned oxide areas. It is believed that these Si irregularities are attributed to undercuts at the Si substrate/patterned oxide interface. As the small DCS is not applied, during the 900°C prebake step hydrogen reacts with SiO_2 at the oxide/substrate interface to form volatile SiO and results in undercuts. Because the undercutting rate is less than 2 nm/min and the duration is 15 minutes only, these undercuts appear randomly at edges but not form undercut lines along edges. The subsequent small DCS deposition in the ramp down step then starts to fill these undercuts with Si. As a result, rough pattern edges are obtained. After removing these oxide stripes, we hence observe these Si irregularities at edges of patterned oxide lines. Comparing the results of Exp. W_{AB} to those of Exp. W_B, it is understood that the addition of a low-concentration of DCS in the 900°C prebake and the ramp down steps can efficiently remove the surface oxide and result in a clean surface for the subsequent deposition. Furthermore, this low-concentration of DCS can fill undercuts to smooth edges.

With the purpose of further exploring the effect of the 900°C prebake and the addition of a low-concentration of DCS on the roughness of edges, a 75 minute 900°C prebake followed by a 20 minute ramp from 900°C to 850°C is applied. In Exp. W_4 a low concentration of DCS is turned on immediately just 15 minute before the ramp down step. The Nomarski micrograph in Fig. 20 illustrates smooth epilayers with rougher edges at the epi/patterned oxide interface on most of areas of

wafers. Near the center of wafers, the cross-sectional TEM micrograph in Fig. 21(a) shows a defect-free epitaxial layer. The plane-view TEM micrograph in Fig. 21(b) shows that the edge is rougher than that of Exp. W_2. SIMS analysis in Fig. 22 does not show any oxygen signal in planar areas. The undercutting rate at 900°C is less than 2 nm/min [5]; however, the growth of the undercut is proportional to the prebake duration. Therefore, it is believed that this extra 1 hour no DCS 900°C prebake causes bigger undercuts at the SiO_2/Si substrate interface, and results in rougher pattern edges. In addition, we occasionally observe degraded epilayers with square patterns and pits near the peripheral areas of wafers. In Fig. 23(a) the Nomarski micrograph of the as-grown epilayer shows concave pits near the peripheral region. After a 90 second dilute Schimmel etch, the Nomarski micrograph in Fig. 23(b) then illustrates more oxide-island-related etched pits at the epi/substrate interface. This result is similar to that in Exp. W_2. Therefore, it is believed in the Exp. W_4 that the smaller oxide islands are buried after the deposition, and only the larger interfacial oxide islands are decorated by pits on the surface. As a result, with a dilute Schimmel etch, these buried smaller oxide islands are then revealed. For epilayers with square patterns, as shown in Fig. 24, a Schimmel etch also reveals many oxide island related etched pits at the epi/substrate interface. SIMS analysis in Fig. 25 shows a weak oxygen peak of $2x10^{17}cm^{-3}$ in areas with square patterns. We believe that, in the first 60 minutes, prebaking at 900°C without a small DCS removes some native oxide. This yields dense small pinholes exposing Si surface on the oxide layer and rough pattern edges resulted from undercuts near corners of SiO_2/Si substrate. A small DCS applied in the subsequent 15 minutes 900°C prebake and the followed ramp down step can extract most of oxidants to favor the further removal of residual oxide islands and produce to a clean Si surface in most areas prior to the deposition. Based on above observation, it is obvious that the prebake and the ramp down steps applied in Exp. W_4 can efficiently remove native

oxide and results in specular epilayers in most areas. However, the long duration with no DCS prebake causes rougher edges in the Si epitaxial layers.

In Exp. W_5, a low concentration of DCS is added as the temperature is raised to 850°C in the ramp up step. The Nomarski micrograph in Fig. 26(a) shows pits with the density of $2x10^4cm^{-2}$ and square patterns on most of areas of the as-deposited epilayers. After a dilute Schimmel etch, as shown in Fig. 26(b), there are more smaller etched pits revealed at the epi/substrate interface. The density of these smaller etched pits is about $9x10^9cm^{-2}$. We also obtain specular epilayers near the center of wafers; however, SIMS analysis in Fig. 27 still shows a weak oxygen signal of $3x10^{17}cm^{-3}$ at the interface for these specular areas. It manifests that there are many smaller interfacial oxide islands buried under these specular epilayers. From above results, it suggests that unremoved oxide islands are distributed on the whole wafer surface as the temperature just reaches to 850°C in the ramp up step. The addition of a low concentration of DCS not only extracts most oxidants in the reactor to favor the removal of surface oxide but also buries these residual oxide islands in the ramp up step from 850°C to 900°C, then in the prebake step and the ramp down step. It is known that the competition among the burying, the shrinkage, and the removal of residual oxide islands is determined by the dimension of residual oxide islands, the prebake temperatures, the prebake durations, and the partial pressure of oxidants. In this case, it is believed that at 850°C the dimension and the density of residual oxide islands is larger and higher, respectively. Thus most of unremoved oxide islands are buried by Si epitaxial growth instead of being removed by the prebake step. Therefore, even in specular areas, SIMS analysis still shows a weak O_2 peak. The above experiments reveal that T_1 the time a low concentration of DCS is added in the prebake, is critical to the growth of high quality epilayers.

2.4 The Mechanism of the Surface Oxide Removal with HF Vapor Treatment and a Small DCS

Based on our previous results [6], it is found that high temperature prebake can efficiently remove the surface oxide prior to the deposition, and then leads to good epilayers but with undercuts. However, as the prebake temperature drops to 900°C, as shown in the Exp. N_1, we speculate that the high background partial pressure of oxidants impedes the removal of surface oxide, and then yields Si hillocks. Although Ghidini et al [10] and Friedrich et al [11] indicate that it is necessary to reduce the partial pressure of oxidants at low temperatures to achieve high quality epilayers, the question is how to reduce the partial pressure of oxidants in the reactor efficienly and economically. The results of the Exp. N_2 suggest that the in-situ addition of a low-concentration of DCS can improve the removal of the surface oxide, though the Si epitaxial film is textured with oxide islands at the epi/substrate interface and threading dislocations in the epilayer. Here we propose that a small amount of DCS can extract most of background H_2O and O_2 in the reactor through the following reactions:

$$SiH_2Cl_2(g) + O_2(g) \rightarrow SiO_2(s) + 2HCl(g) \quad (1)$$

$$SiH_2Cl_2(g) + 2H_2O(g) \rightarrow SiO_2(s) + 2HCl(g) + H_2(g) \quad (2)$$

where the byproduct SiO_2 particles are then swept away by the high flow rate of H_2. This extraction significantly drops the background concentration of H_2O and O_2, then changes the equilibrium between the growth and the shrinkage of interfacial oxide islands. Consequently, the whole reaction starts to favor the removal of interfacial oxide islands through the following reactions [5]:

$$2H_2(g) + SiO_2 \rightarrow Si^* + 2H_2O(g) \quad (3)$$

$$Si^* + SiO_2 \rightarrow 2SiO(g) \quad (4)$$

where Si^* is the absorbed silicon atom which reacts with its neighboring interfacial SiO_2 to form SiO(g) leaving undercuts at Si/SiO_2 interface. Liehr et al [12] and Hofmann et al [13] also indicate that the oxide decomposition starts at defect sites near the SiO_2/Si substrate interface and the pinhole number is almost unchanged with continuing anneal. Therefore, it is obvious that raising the prebake temperature to increase the undercutting rate or adding the defect sites to increase the pinhole density can enhance the removal of the surface oxide. The undercutting rate is less than 2 nm/min at 900°C. Hence, it is presumable in the Exp. N_2 that the number of defect sites near the SiO_2/Si substrate interface is not high enough to generate sufficient pinholes in the oxide to favor the invasion of H_2 to undercut the surface oxide. To extend the duration of the 900°C prebake may completely remove the surface oxide layer; however, big undercuts can result in rough pattern edges on epilayers. It seems that to increase the number of defect sites at the SiO_2/Si substrate interface is an effective approach to get an oxide-free Si surface prior to the deposition.

It is found in the W_N series experiments that an ex-situ HF vapor treatment can further improve the quality of epilayers resulted from a more efficient surface oxide removal. We therefore propose that this HF vapor treatment can remove the chemical oxide, can passivate the Si surface, and especially can provide more defect sites to generate sufficient pinholes to enhance the removal of the surface oxide. The proposed mechanism is as follows. After the HF vapor treatment the presence of a hydrogen- and fluorine-terminated Si surface can retard the oxidation [16-18].

However, during the ramp up step, the reactivity of Si surface with the background oxidants increases with the temperature because of the passivation desorption. Consequently, a fluorinated thin surface oxide (several nm) is formed while passivating fluorine atoms may desorb out of the Si surface, diffuse into the surface oxide film, or stay at the SiO_2/Si substrate interface. Fluorine atoms in the surface oxide layer may cleave Si-O bonds to form Si-F bonds. Some of Si-F bonds may further form volatile SiF_4 which then desorb out of the oxide and create many microchannels in the surface oxide layer. These microchannels can favor the invasion of hydrogen to the SiO_2/Si substrate interface and the transport of SiO through the oxide. The residual fluorine atoms at the SiO_2/Si substrate interface can form defect sites initiating the decomposition of the surface oxide, and then form pinholes through these microchannels. Once pinholes form, hydrogen enters into these pinholes to reduce SiO_2 at the SiO_2/Si substrate interface. As a result, dense small exposed Si areas appear in the continuous surface oxide layer, then grow up and gradually merge together to result in isolated oxide islands on Si surface. With a proper deposition cycle, the oxide islands can be completely removed prior to the deposition, as shown in Exp. W_3, then the subsequent deposition can yield defect-free epilayers.

2.5 The Burial of Tiny Oxide Islands Due to a Small DCS

Based on above results, it is obvious that with an ex-situ HF vapor treatment the addition of a small amount of DCS is beneficial to improve the epitaxial quality. However, in some cases it is found that this low concentration of DCS buries some smaller interfacial oxide islands instead of removing them completely. The detail is explained as follows. According to Exp. W_{AB} and Exp. W_B, a low-concentration of DCS can grow a very thin epilayer on exposed Si areas before the regular deposition. In case the reduction of SiO_2 to volatile SiO can not completely remove interfacial oxide islands in time, the subsequent deposition buries residual

oxide islands and degrades the epitaxial quality. Therefore, the determination of the time T_1 to add a small concentration of DCS becomes very critical to the removal of interfacial oxide islands completely or the burial of residual oxide islands. For example in Exp.W_2, a low-concentration of DCS applied only in the ramp down step can not completely remove interfacial oxide islands. In addition, it shows in Exp. W_5 that an early small DCS deposition can bury most of un-removed interfacial oxide islands. Consequently, degraded epilayers are obtained. Therefore, if the time T_1 starting to add a low-concentration of DCS is too early (e.g. Exp. W_5) or too late (e.g. Exp. W_2), the burial of un-removed oxide islands result in defective epilayers with pits. In Exp. W_3, the small DCS starts to extract background H_2O as well as O_2 in the 900°C prebake step and favors the reduction of SiO_2 to volatile SiO. Empirical results show that this kind of 15 min 900°C prebake and ramp down can completely remove the native oxide before the deposition, then result in high quality epilayers.

2.6 The Formation of Square Patterns

In Exp. W_2, Exp. W_4 and Exp. W_5, square patterns are observed. It is presumable that these square patterns are attributed to the low-concentration DCS deposition. It is understood [12-13] that during the ramp up and the prebake steps, the surface oxide decomposition starts at defect sites near the SiO_2/Si substrate interface through the following reaction

$$Si + SiO_2 \rightarrow SiO\uparrow \tag{5}$$

then initiates many small pinholes in the surface oxide layer. Subsequently, hydrogen starts to undercut the surface oxide from these small pinholes. With the results of Exp. W_{AB} and Exp. W_B, it is also found that the addition of a low-concentration

of DCS can achieve a thin Si growth. We therefore propose that this small low-concentration of DCS can selectively deposit a very thin Si layer in these small exposed Si areas only while the oxide layer is being gradually removed. As a result, many Si plateaus with finite thickness are formed after the removal of the surface oxide. This is the reason why we observe many convex square patterns on the surface of epilayers. However, if the number of pinholes is big enough, it only takes a very short time to completely remove the surface oxide before any obvious Si plateaus form. The followed deposition then smoothes the whole surface of epilayers. Hence, as obtained in the Exp. W_3, a specular epilayer with no convex square patterns is achieved. Furthermore, dilute Schimmel etch just reveals etched pits, resulted from interfacial oxide islands, near these convex square patterns or other areas. It never shows etched pits in convex square patterns. Therefore, it is believed that there is no interfacial oxide island underneath these convex square patterns. Consequently, these square patterns can decorate early exposed Si areas in the prebake step. Moreover, in the Exp. W_1 we observe many Si hillocks instead of continuous epilayers because the higher background partial pressure of oxidants impedes the removal of the surface oxide. With the same explanation, it is believed that Si only selectively deposits in these small exposed Si areas, resulted from the decomposition of surface oxide at some defect sites located at the SiO_2/Si substrate interface, then attributes to the Si hillocks on the surface.

2.7 Summary

The selective epitaxy of Si using a dichlorosilane-hydrogen mixture is achieved with a hot-wall reactor at 850°C and lower temperatures. The HF vapor treatment as well as the addition of a low concentration of DCS in the deposition cycle are studied. In summary, the HF vapor treatment resulting in a passivation of hydrogen and fluorine on the Si surface can retard the oxidation rate of Si during

the temperature ramp up step. Furthermore, fluorine in the surface oxide can generate more microchannels in oxide to favor the transport of hydrogen and SiO through the oxide layer. Also, fluorine at the SiO_2/substrate interface can form more defect sites to enhance the decomposition of surface oxide. Therefore, this ex-situ HF vapor treatment can reduce the H_2 prebake temperatures and eliminate the formation of undercuts. A low-concentration of DCS in the prebake and the ramp down steps not only can enhance the remove of oxide on Si surface by extracting most of background H_2O and O_2 through the gaseous reaction, but also can smooth the epitaxial edges along the oxide sidewalls. However, an inadequate DCS cycle buries interfacial oxide islands instead of removing them. A suitable addition of small DCS cycle can completely remove oxide layers prior to the deposition. Experimental results show that an ex-situ HF vapor treatment combined with an in-situ low concentration of DCS cycle in the 15 min 900°C prebake and the ramp down from 900°C to the deposition temperatures can consistently lead to high quality Si epilayers through an economical hot-wall CVD reactor at 850°C and lower temperatures. SIMS profiles and the dilute Schimmel etch for these epilayers indicate no interfacial oxide islands at the epi/substrate interface. TEM analyses further show defect-free epilayers and no oxide undercut at oxide/substrate. With the extension of deposition duration, specular, seamless, undercut-free and defect-free epitaxial layers are also obtained. These perfect overgrown Si epitaxial layers are very promising for silicon-on-insulator (SOI) manufacturing technology.

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Table 1

The Growth Parameters of Epilayers

Experiment	HF Vapor	The Addition of A Small DCS	Results
N_1	no	no small DCS in the prebake or the ramp down steps.	Si hillocks
N_2	no	a small DCS in the prebake and the ramp down steps.	Textured
W_1	yes	no small DCS in the prebake or the ramp down steps.	Textured
W_2	yes	a small DCS in the ramp down step.	Pits, square patterns
W_3	yes	a small DCS in the prebake and the ramp down steps.	Defect-free
W_4	yes	after a 60 min no DCS prebake, add a small DCS in the subsequent prebake (15 min) and the ramp down steps.	Pits, square patterns
W_5	yes	a small DCS in the ramp up (above 850°C), the prebake, and the ramp down steps.	Pits, square patterns
W_A	yes	a small DCS in the ramp down step.	Pits
W_{AB}	yes	a small DCS in the prebake and the ramp down steps.	Defect-free

Fig. 1. The deposition cycle used for the selective epitaxial growth of Si. T_1 is the time at which a low-concentration of dichlorosilane is added. A: load, B: ramp up, C: bake, D: ramp down, E: deposition, F: ramp down, G: unload.

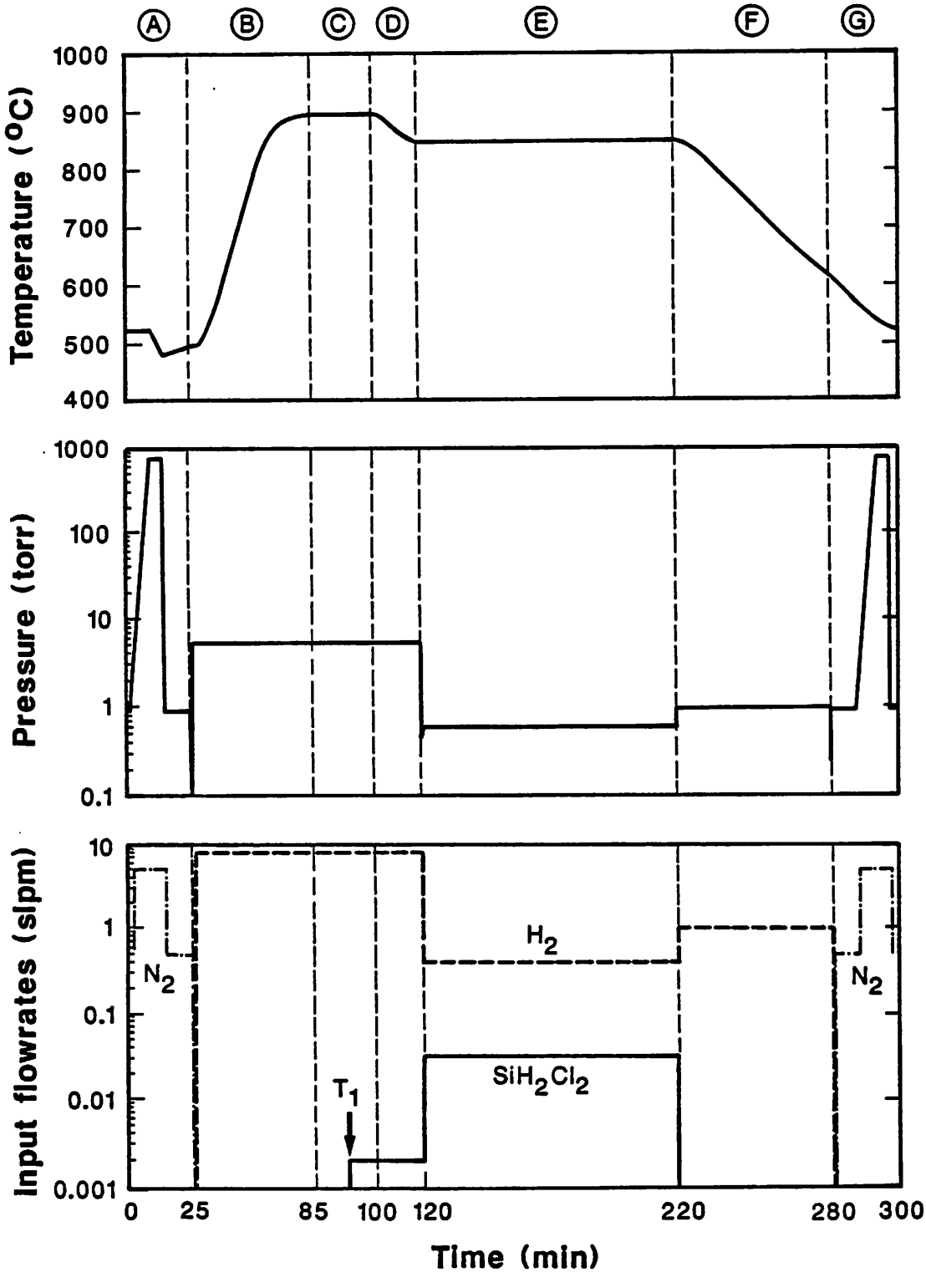


Fig. 2. In the absence of a HF vapor treatment and an addition of a low-concentration of DCS, the Narmarski micrograph (1000X) shows dense Si hillocks and rough pattern edges.

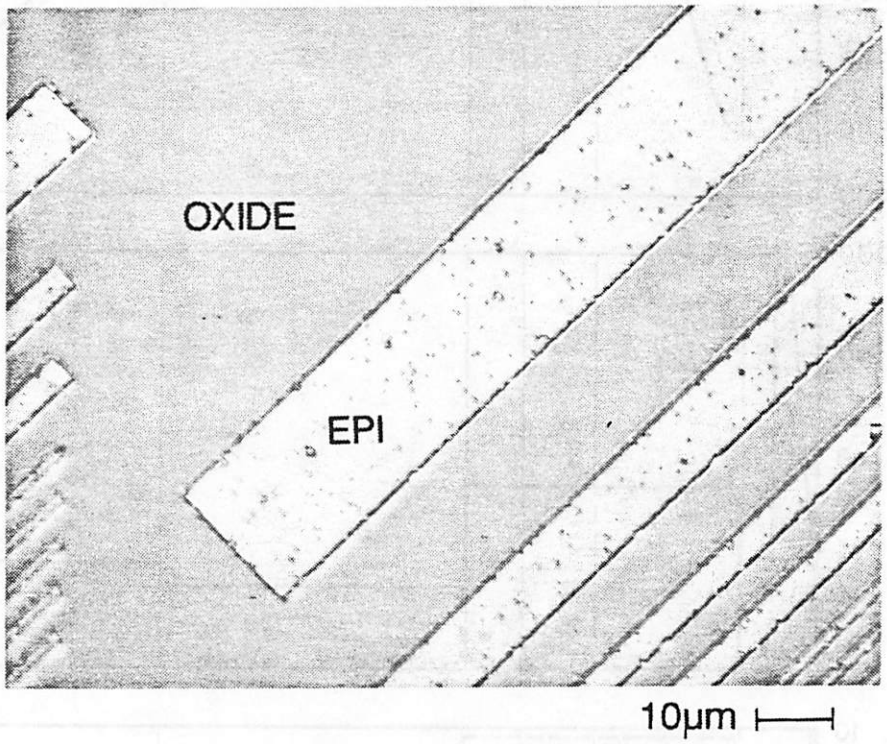


Fig. 3. In the absence of a HF vapor treatment, a low-concentration of DCS is applied in the prebake and the ramp down steps. (a) The Nomarski micrograph (1000X) illustrates a textured epilayer deposited at 850°C. (b) The XTEM micrograph of the same specimen in Fig. 3(a) shows a defective epilayer with dense oxide islands at the epi/substrate interface and threading dislocations in the epilayer.

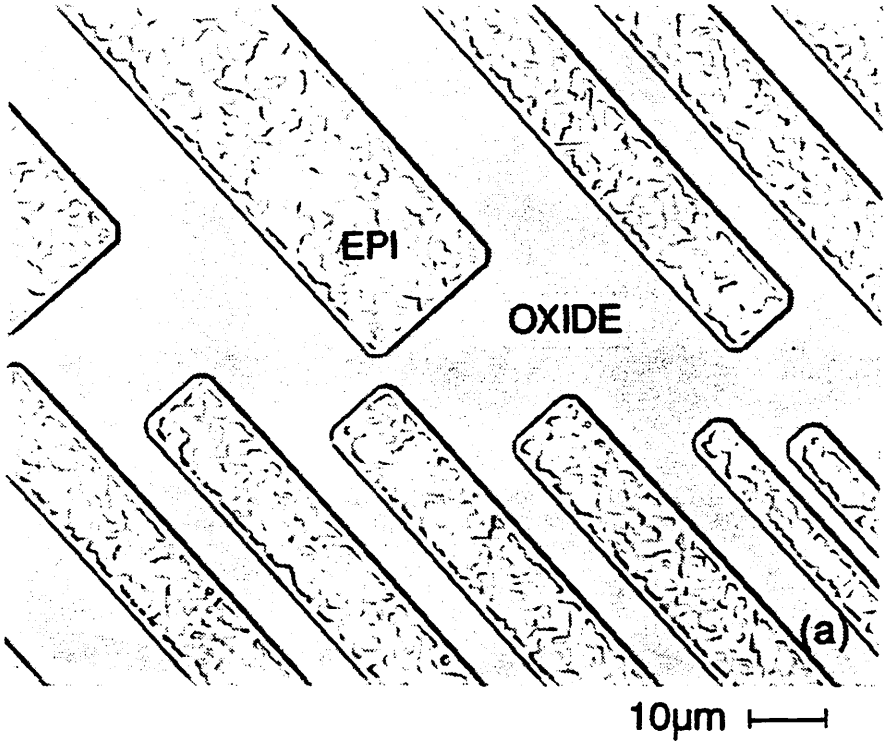


Fig. 3. (cont.)

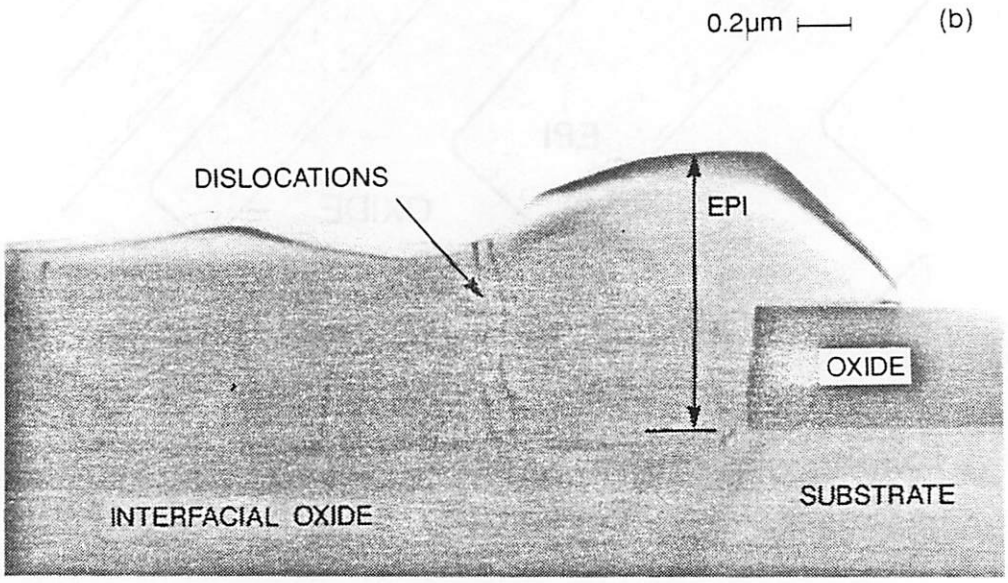

0.2μm
(b)
DISLOCATIONS
EPI
OXIDE
SUBSTRATE
INTERFACIAL OXIDE

Fig. 4. SIMS results of the specimen in Fig. 3 shows large oxygen, carbon, and fluorine peaks at the epi/substrate interface.

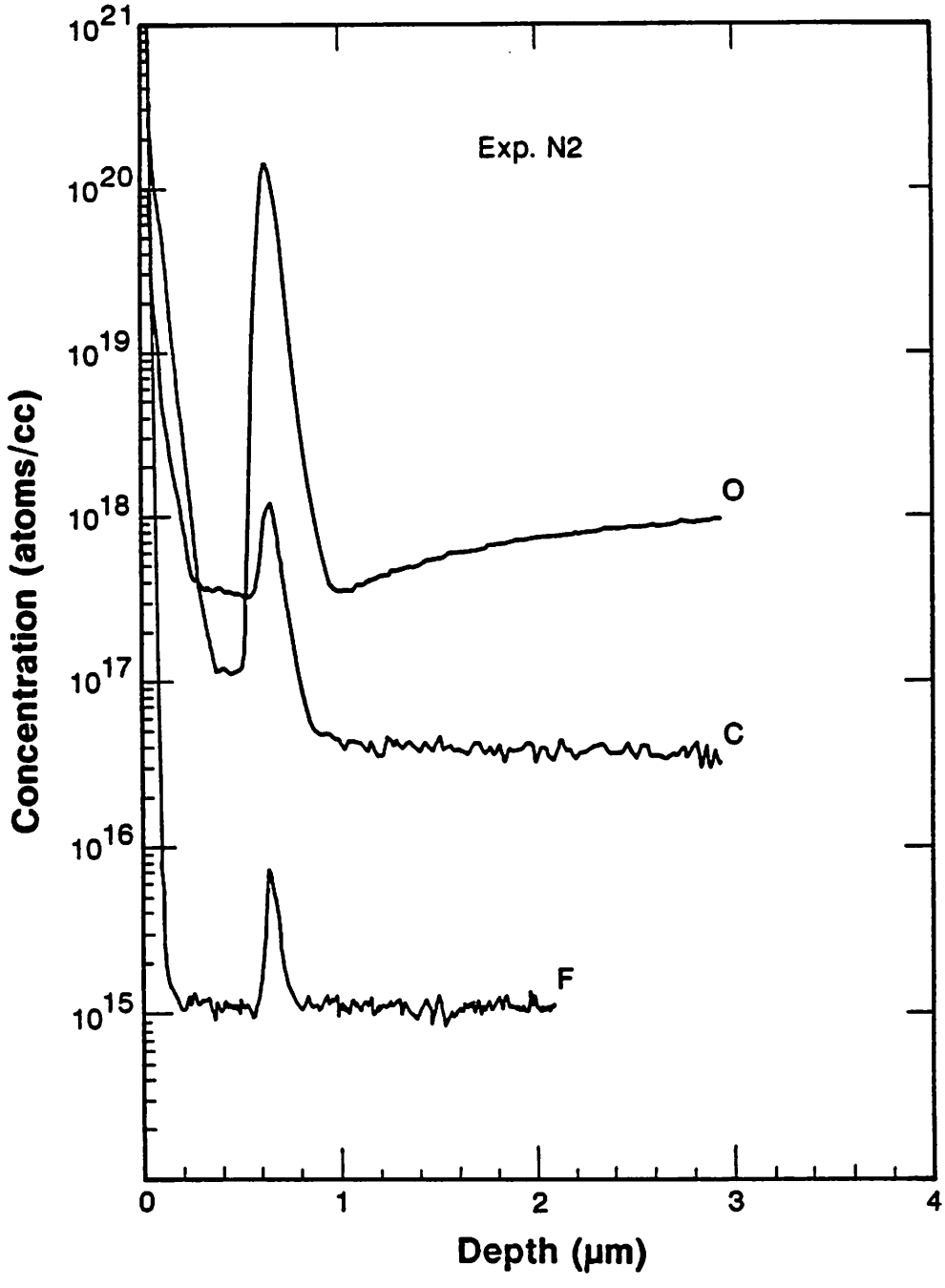


Fig. 5. With an ex-situ HF vapor treatment before the wafer loading, a low-concentration of DCS is not applied in the prebake and the ramp down steps. The Nomarski micrograph (1000X) shows a more textured surface morphology.

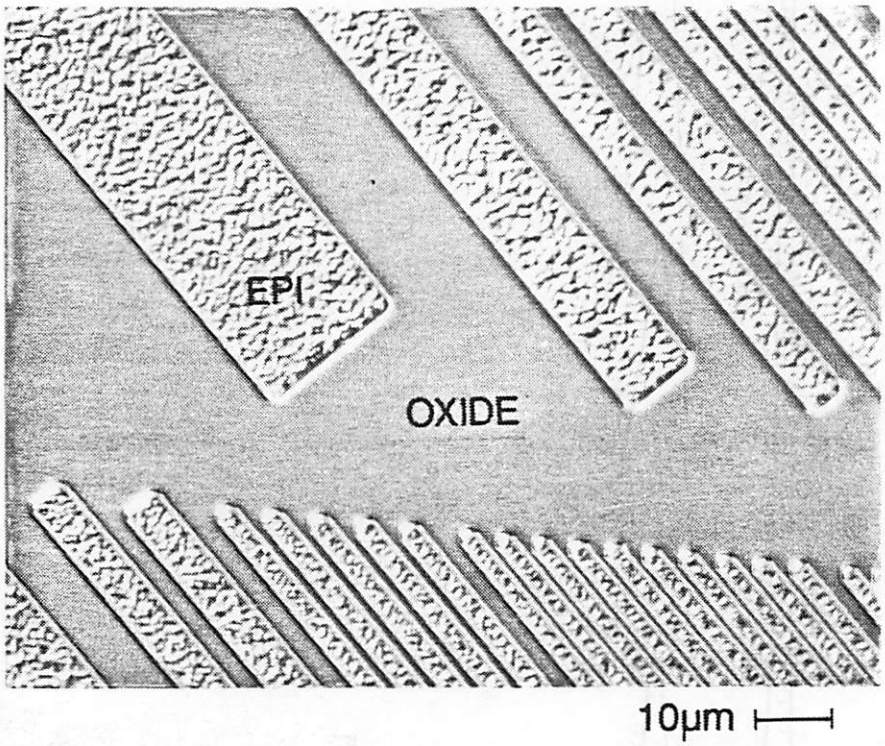


Fig. 6. SIMS analyses for the sample of Fig. 5 show a strong and a weak oxygen peak near the periphery and the center of the wafer, respectively.

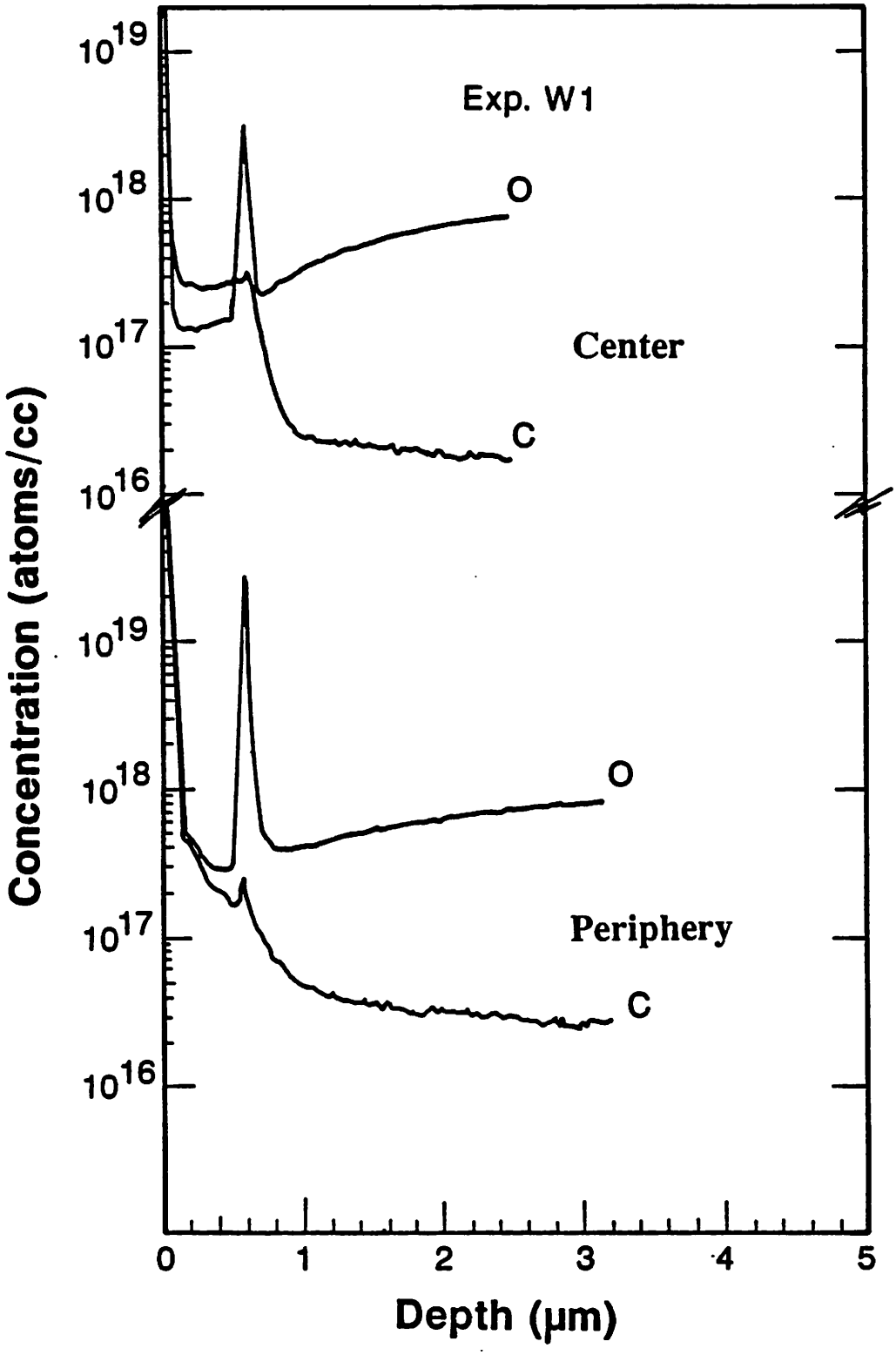


Fig. 7. With a HF vapor treatment, a low-concentration of DCS is applied only in the ramp down step. (a) The Nomarski micrograph (1000X) shows a specular epi-layer with rough pattern edges. (b) A plane-view TEM illustrates the rougher edges resulted from the undercut along the pattern edges. (c) A XTEM micrograph shows a defect-free epilayer in the center of the wafer. (d) Before the dilute Schimmel etch the Nomarski micrograph (1000X) shows a specular epilayer in the center of the wafer. (e) After the dilute Schimmel etch the Nomarski micrograph (1000X) shows no etched pits at the epi/substrate interface for the specimen in (d). (f) SIMS analysis of the same specimen in (d) shows no oxygen and carbon peaks at the epi/substrate interface.

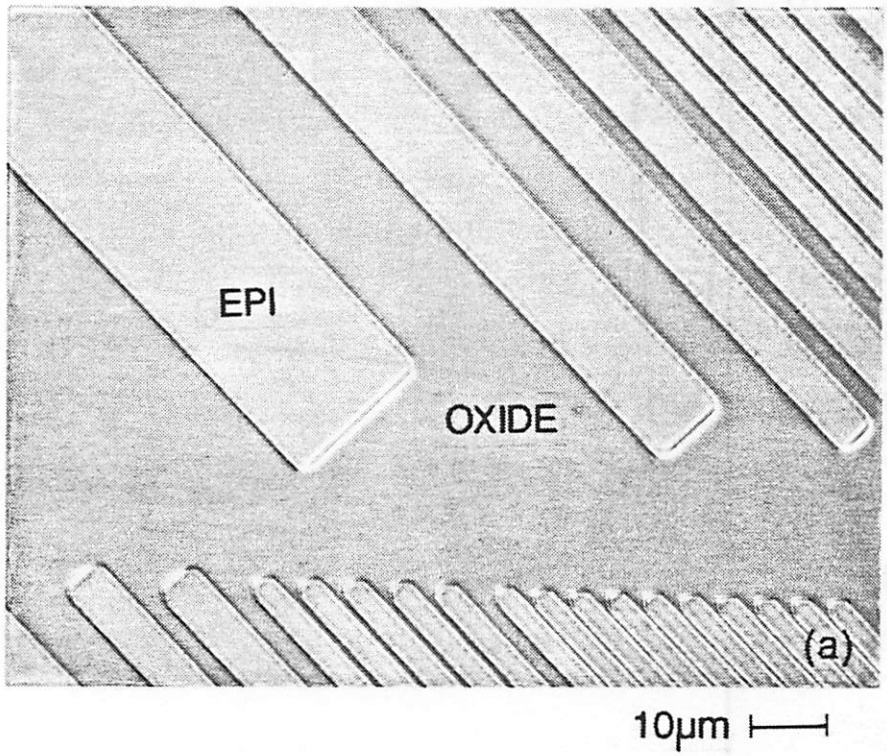


Fig. 7. (cont.)

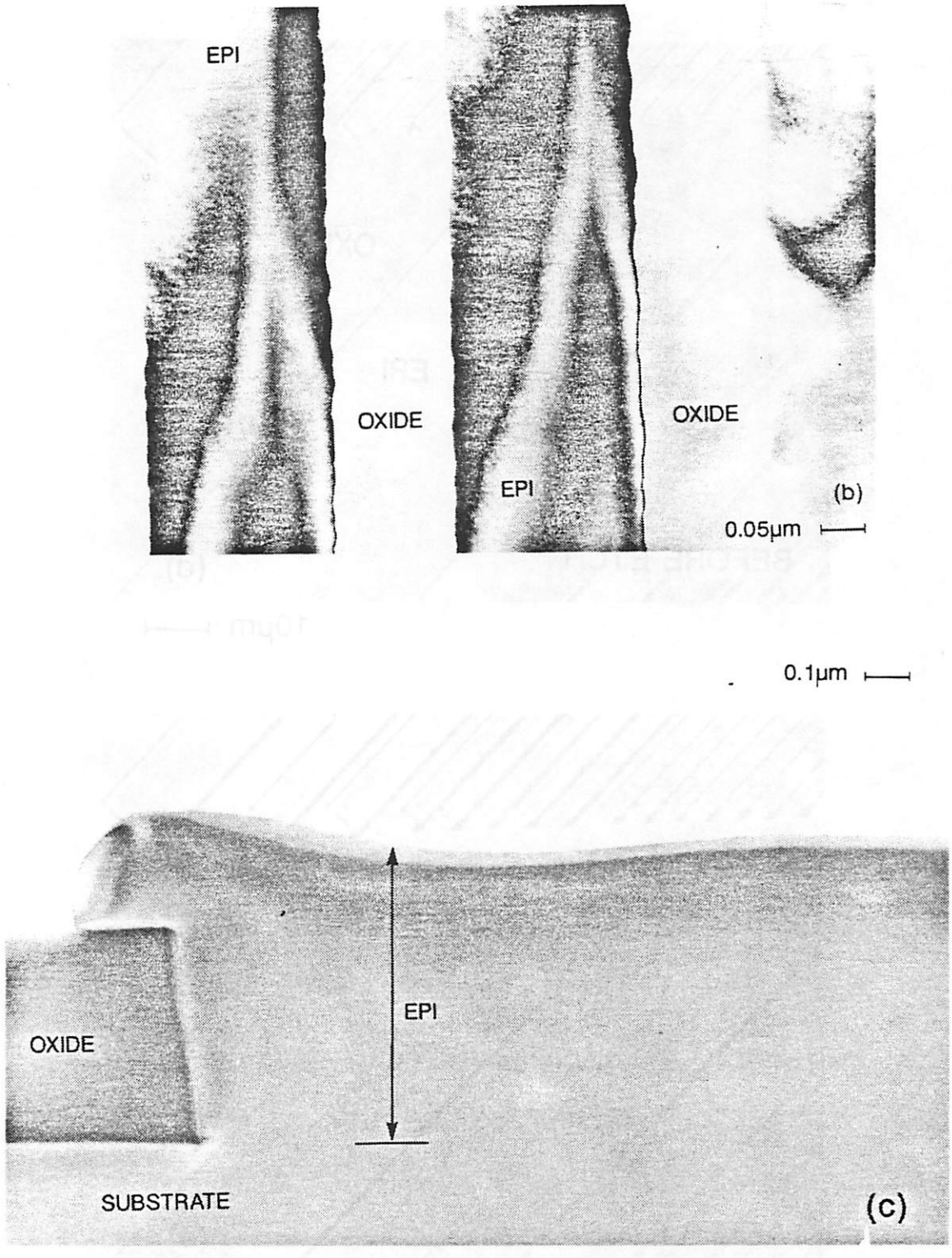
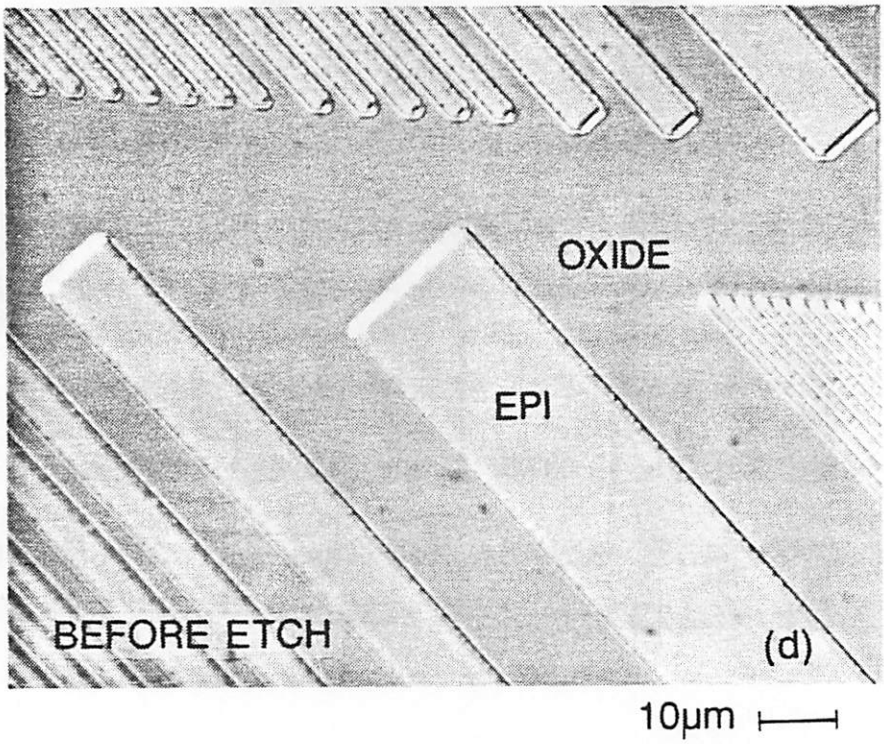


Fig. 7. (cont.)


OXIDE
EPI
BEFORE ETCH
(d)
10μm

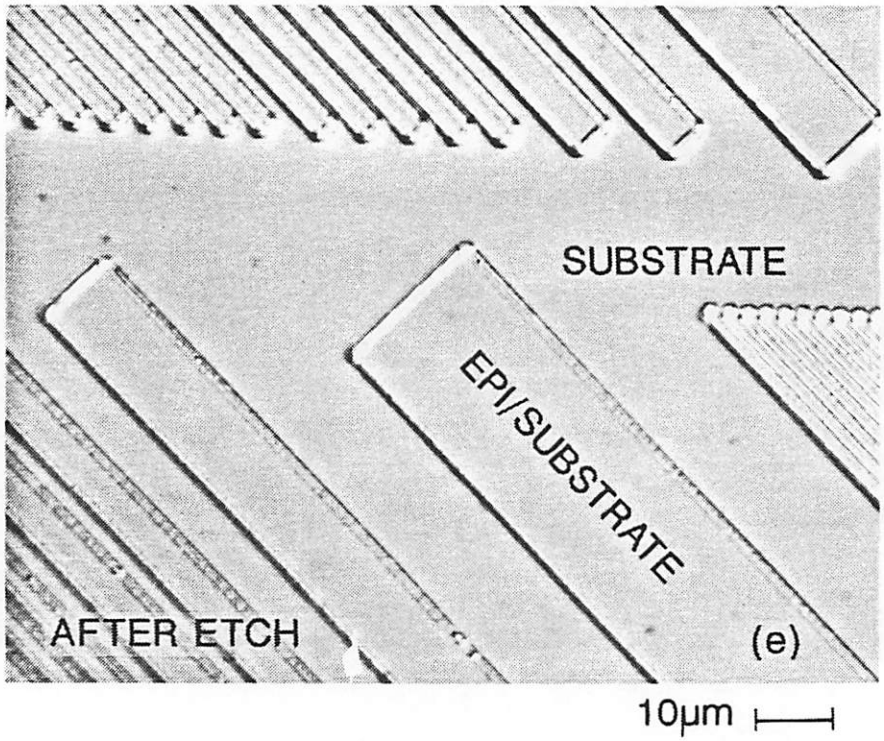

SUBSTRATE
EPI/SUBSTRATE
AFTER ETCH
(e)
10μm

Fig. 7. (cont.)

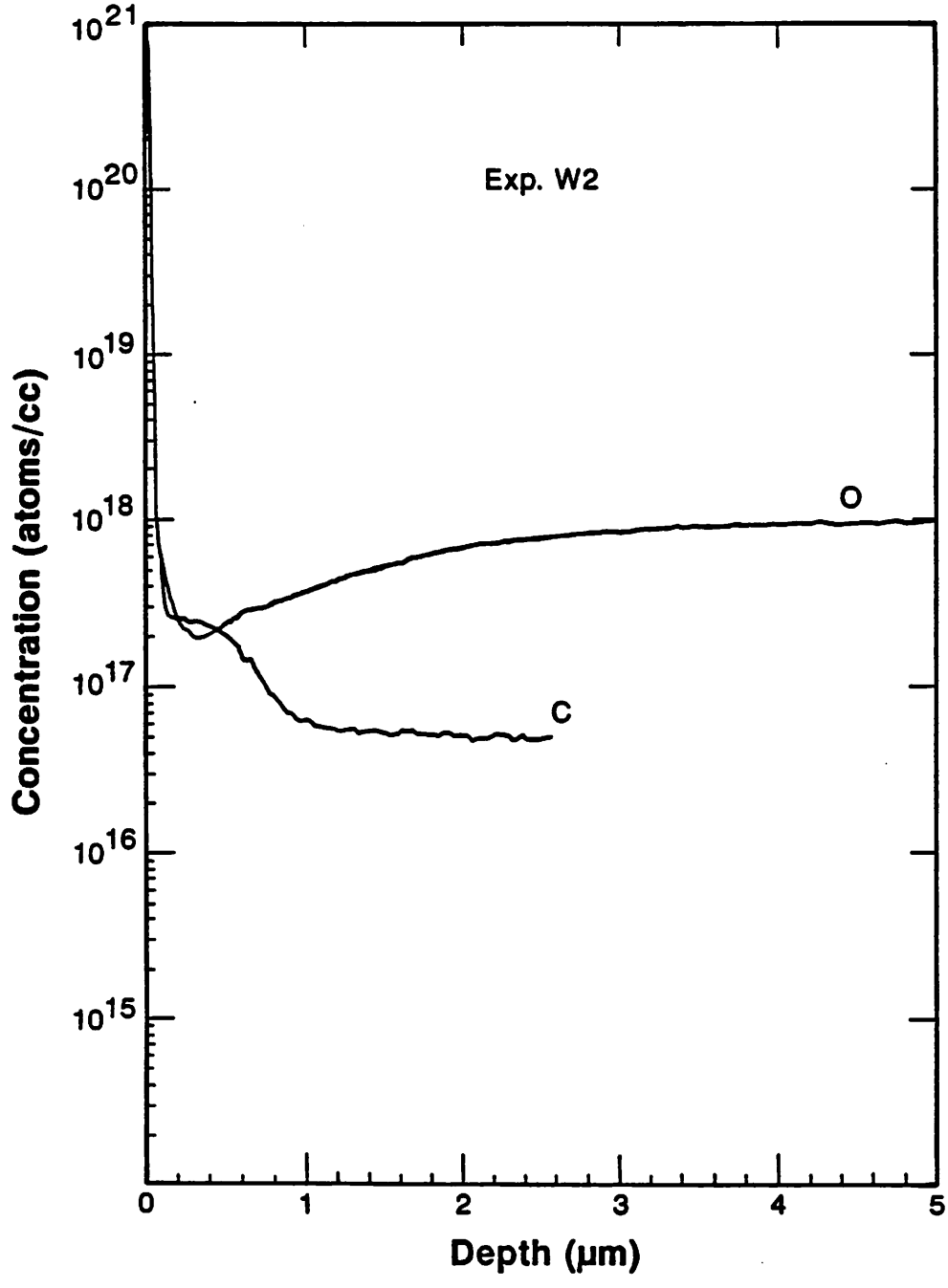

Exp. W2
O
C
Concentration (atoms/cc)
Depth (μm)
10^21
10^20
10^19
10^18
10^17
10^16
10^15
0
1
2
3
4
5

Fig. 8. Nomarski micrographs (1000X) of the epilayer in the area with square patterns. (a) Before the dilute Schimmel etch it shows only square patterns on the surface. (b) After the dilute Schimmel etch it shows more etched pits at the epi/substrate interface.

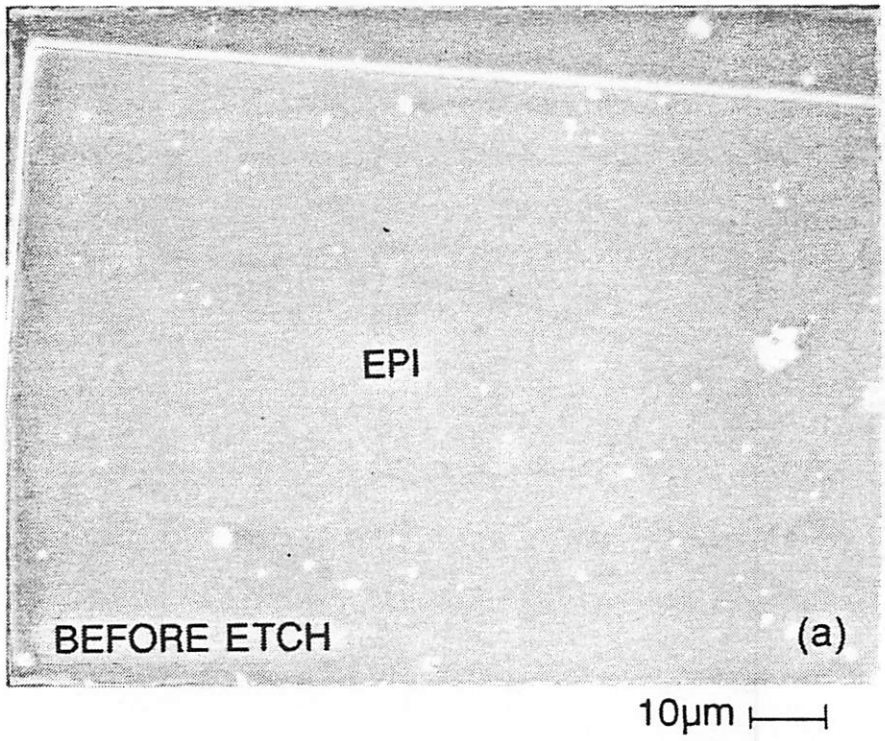


Fig. 8. (cont.)

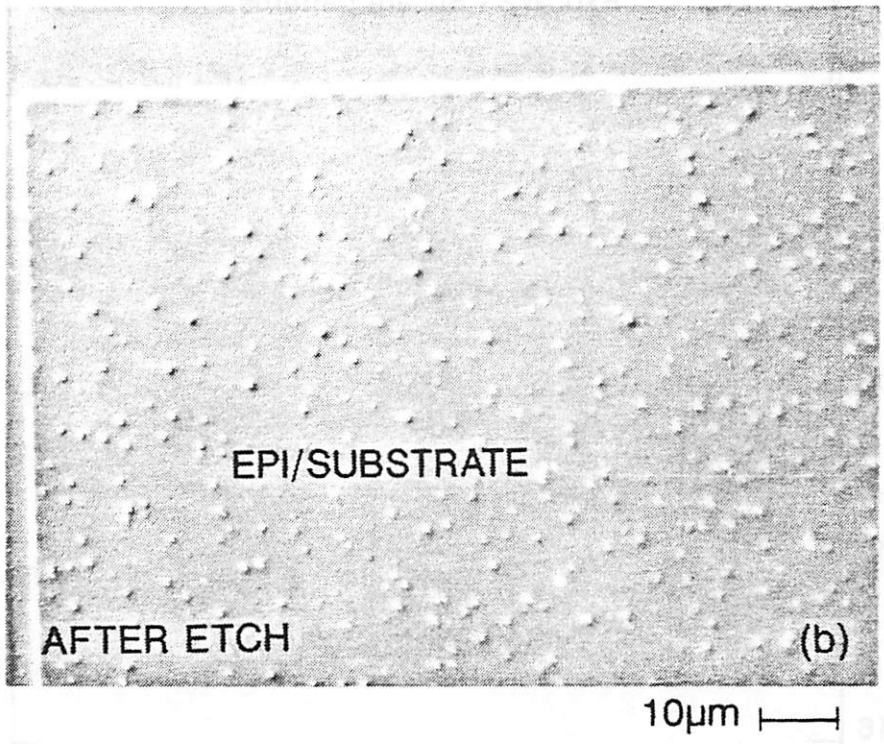


Fig. 9. SIMS analysis of the specimen in Fig. 8 indicates an oxygen peak and a carbon peak at the epi/substrate interface.

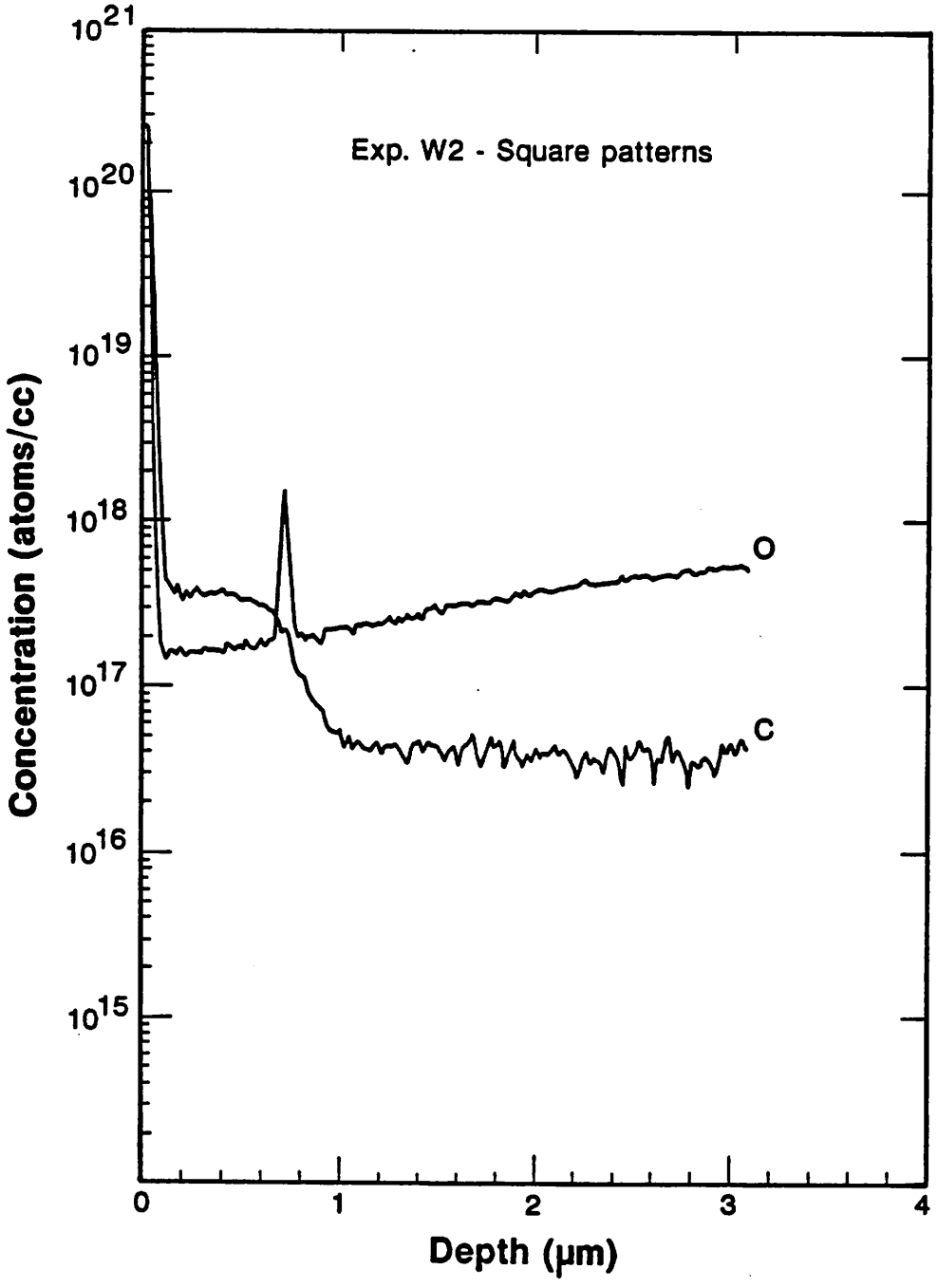


Fig. 10. Nomarski micrographs (1000X) of the epilayer in the ringed area. (a) Before the dilute Schimmel etch and (b) after the dilute Schimmel etch for the epilayer in the outer region of the ringed area. (c) Before the dilute Schimmel etch and (d) after the dilute Schimmel etch for the epilayer in the inner region of the ringed area.

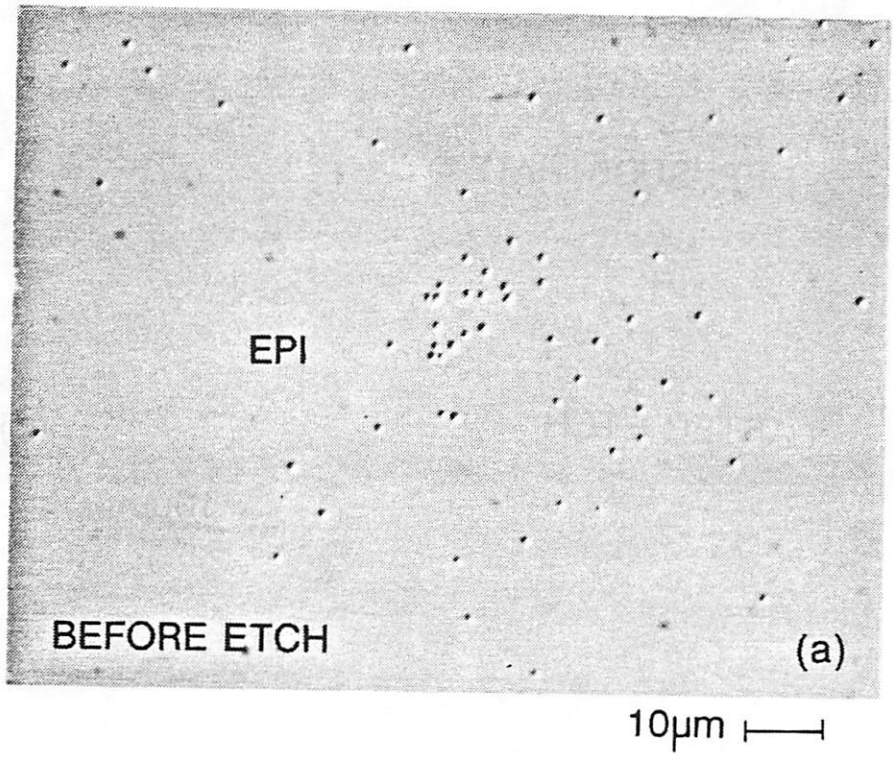


Fig. 10. (cont.)

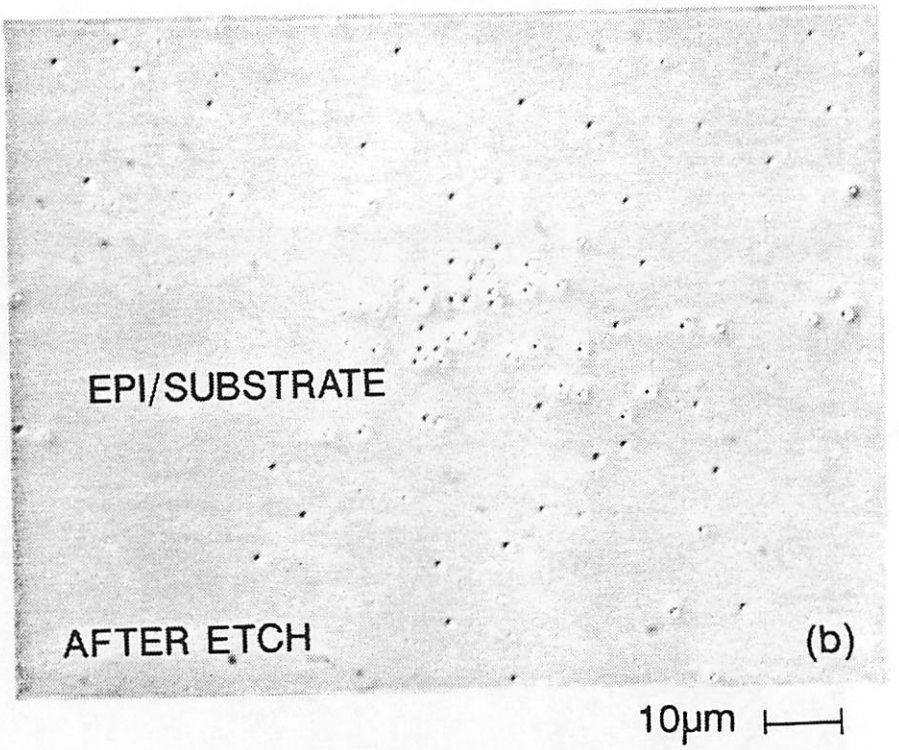


Fig. 10. (cont.)

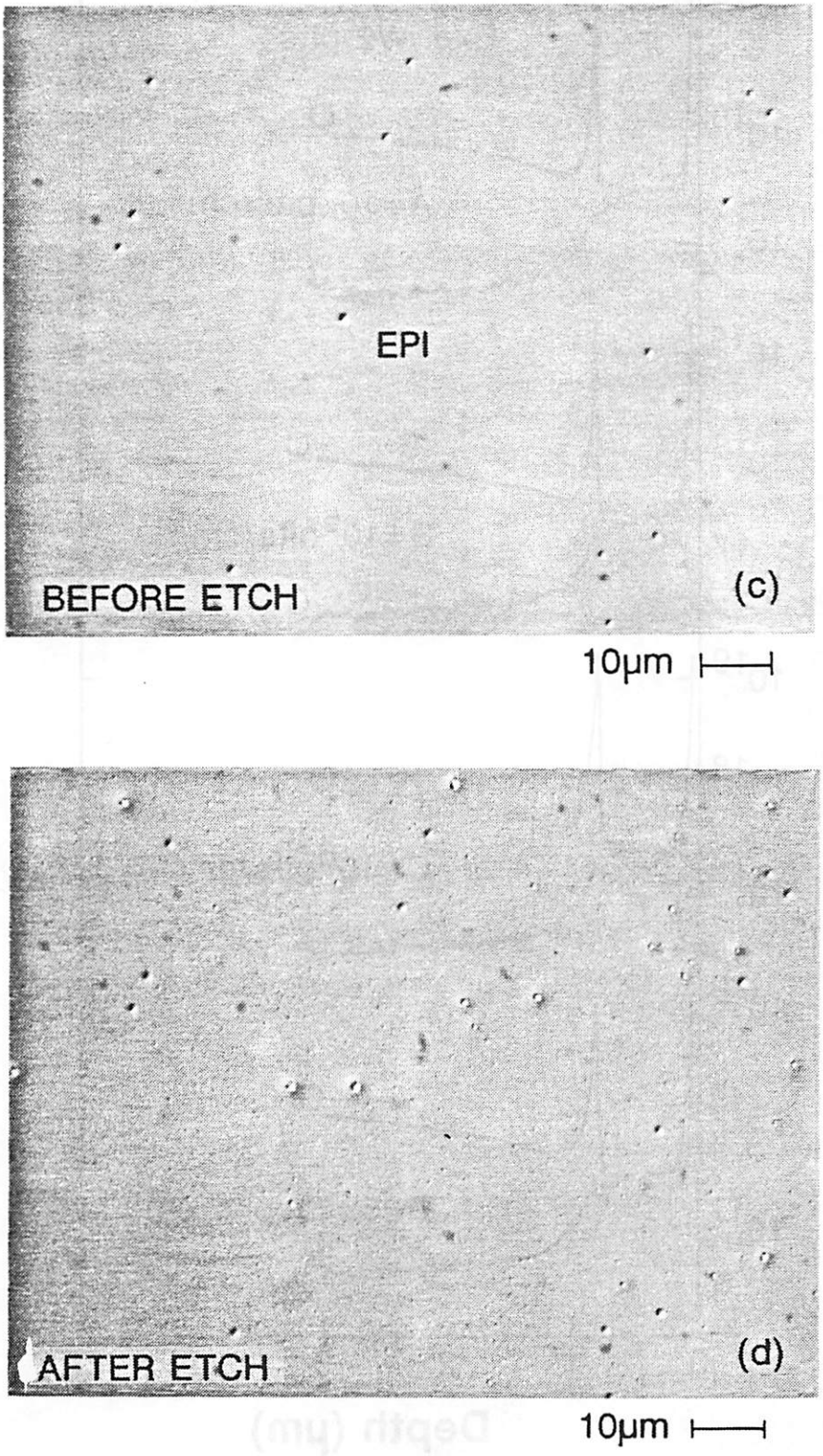


Fig. 11. SIMS results of epilayers with dense pits. The density of pits; curve A: $10^4 cm^{-2}$; curve B: $10^5 cm^{-2}$; curve C: $10^6 cm^{-2}$; and curve D: $5x10^6 cm^{-2}$.

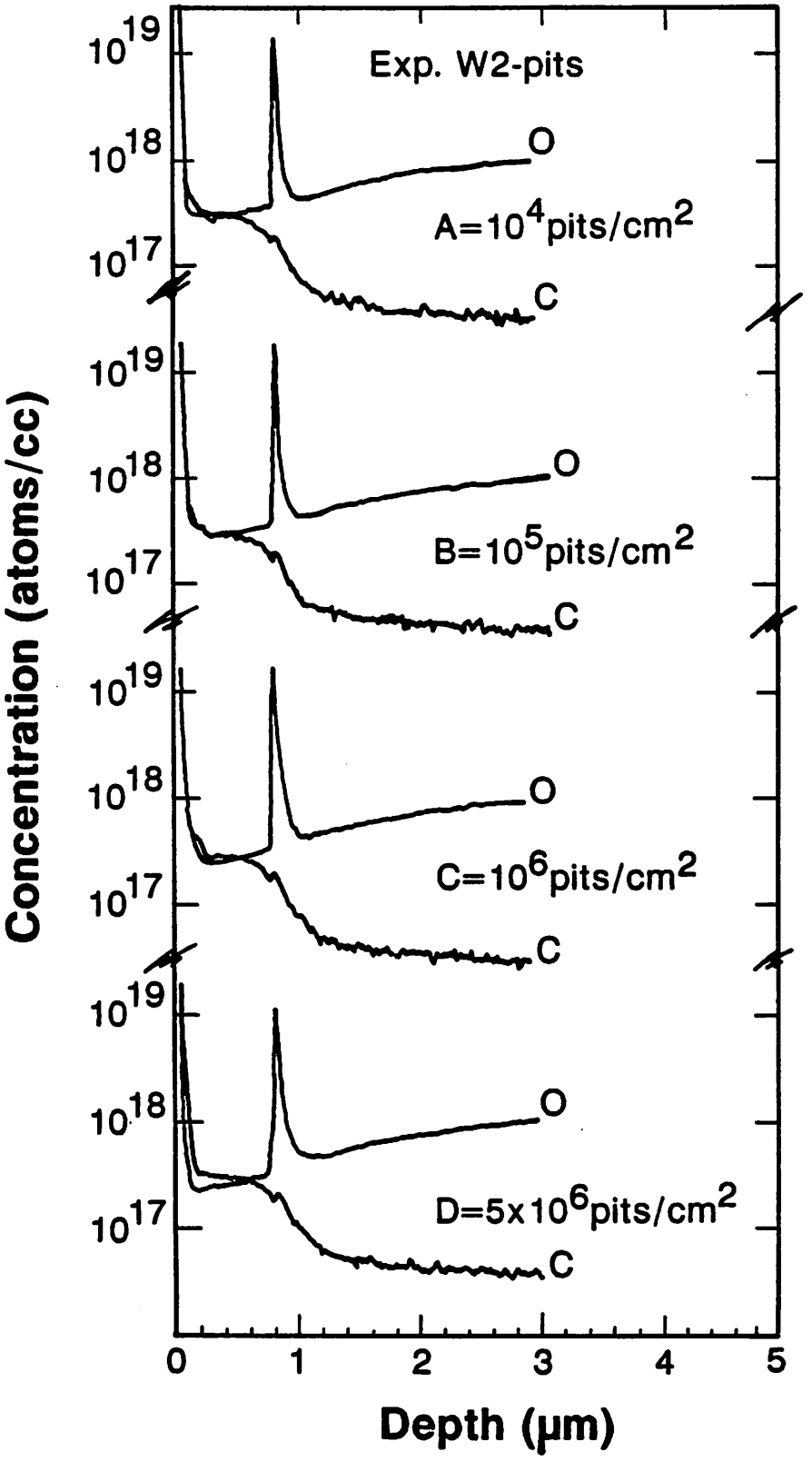


Fig. 12. The Nomarski micrograph (1000X) shows a specular epilayer with smooth edges.

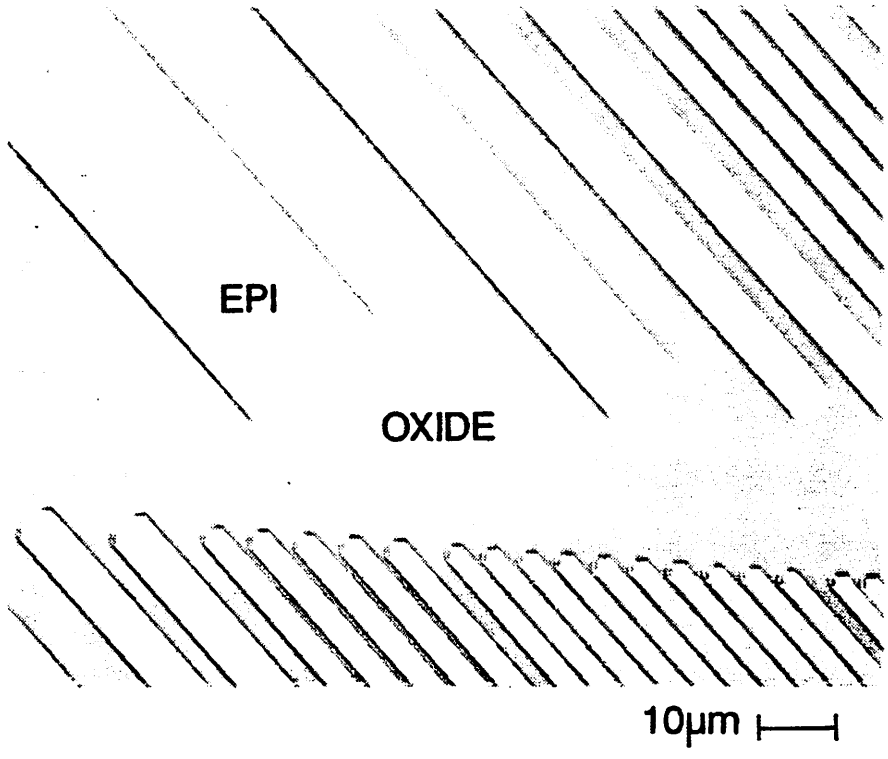


Fig. 13. (a) A plane-view TEM micrograph (100K) shows a smooth epi/oxide edges. (b) The XTEM micrograph shows no defects in the epilayer and no under-cuts along the edge of pattern oxide.

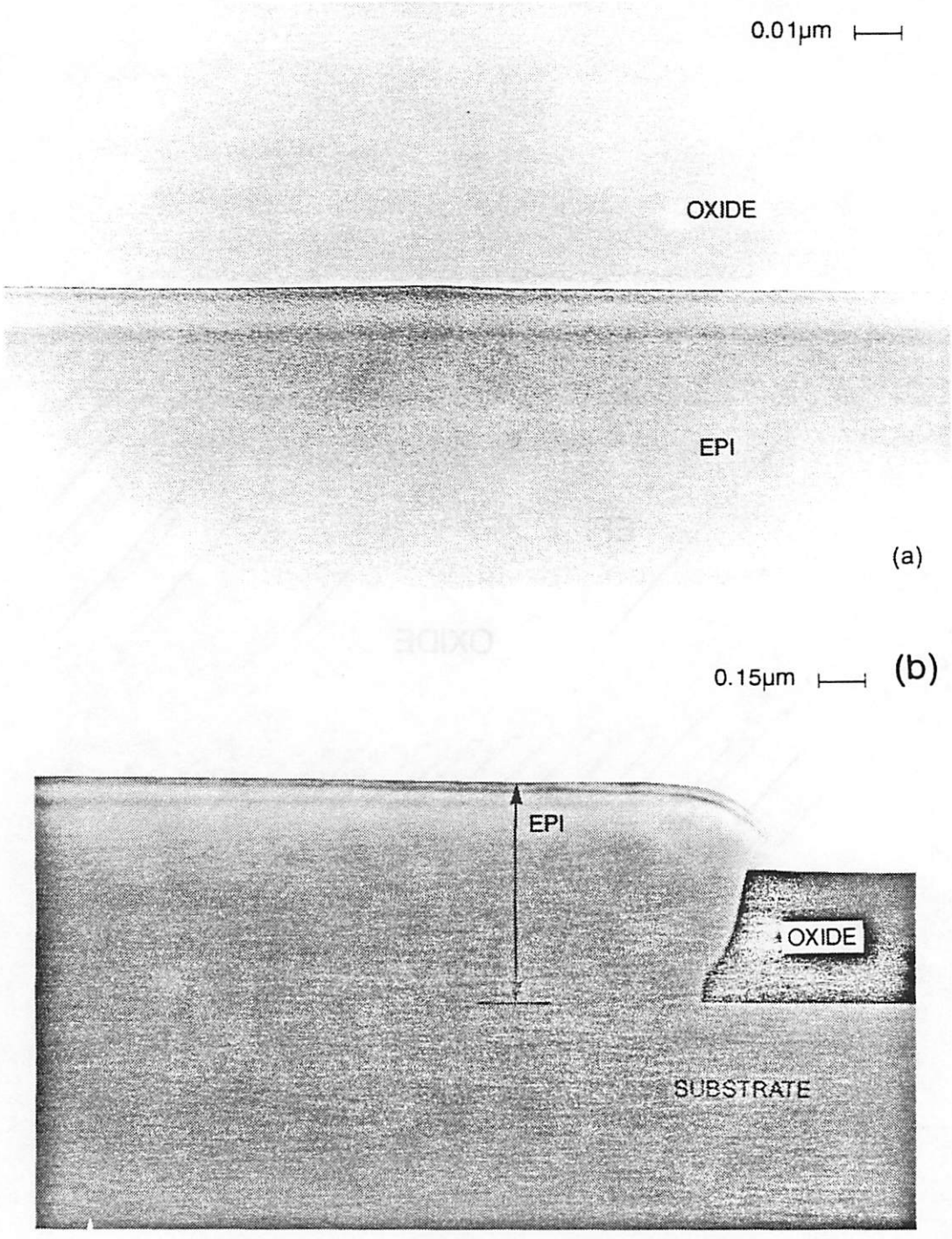


Fig. 14. SIMS analysis shows no oxygen, carbon, or fluorine peak at the epi/substrate interface.

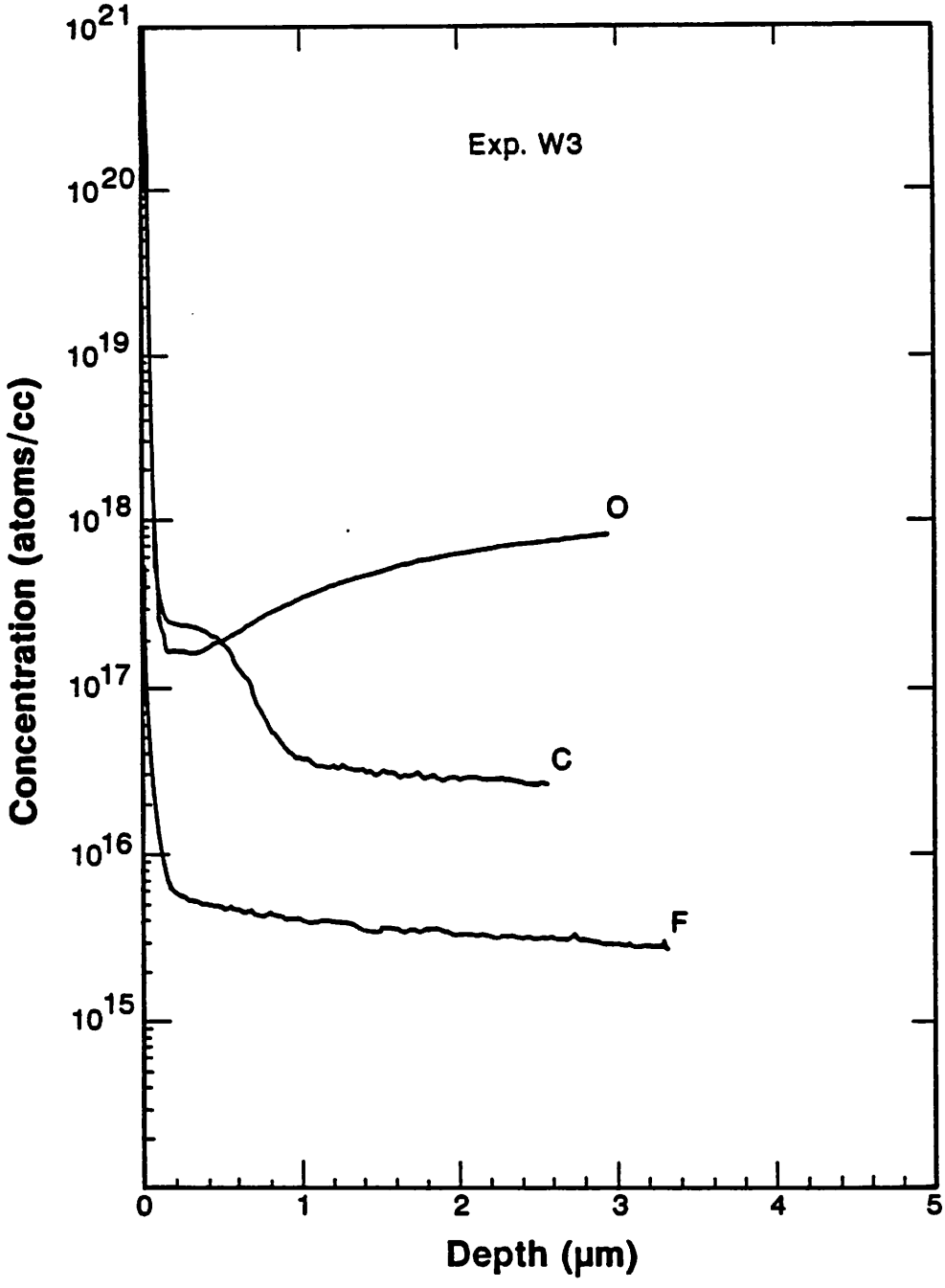


Fig. 15. (a) The Nomarski micrograph (1000X) shows the epilayer of the Exp. W_3 before the dilute Schimmel etch. (b) After the dilute Schimmel etch it reveals no etched pits at the epi/substrate interface.

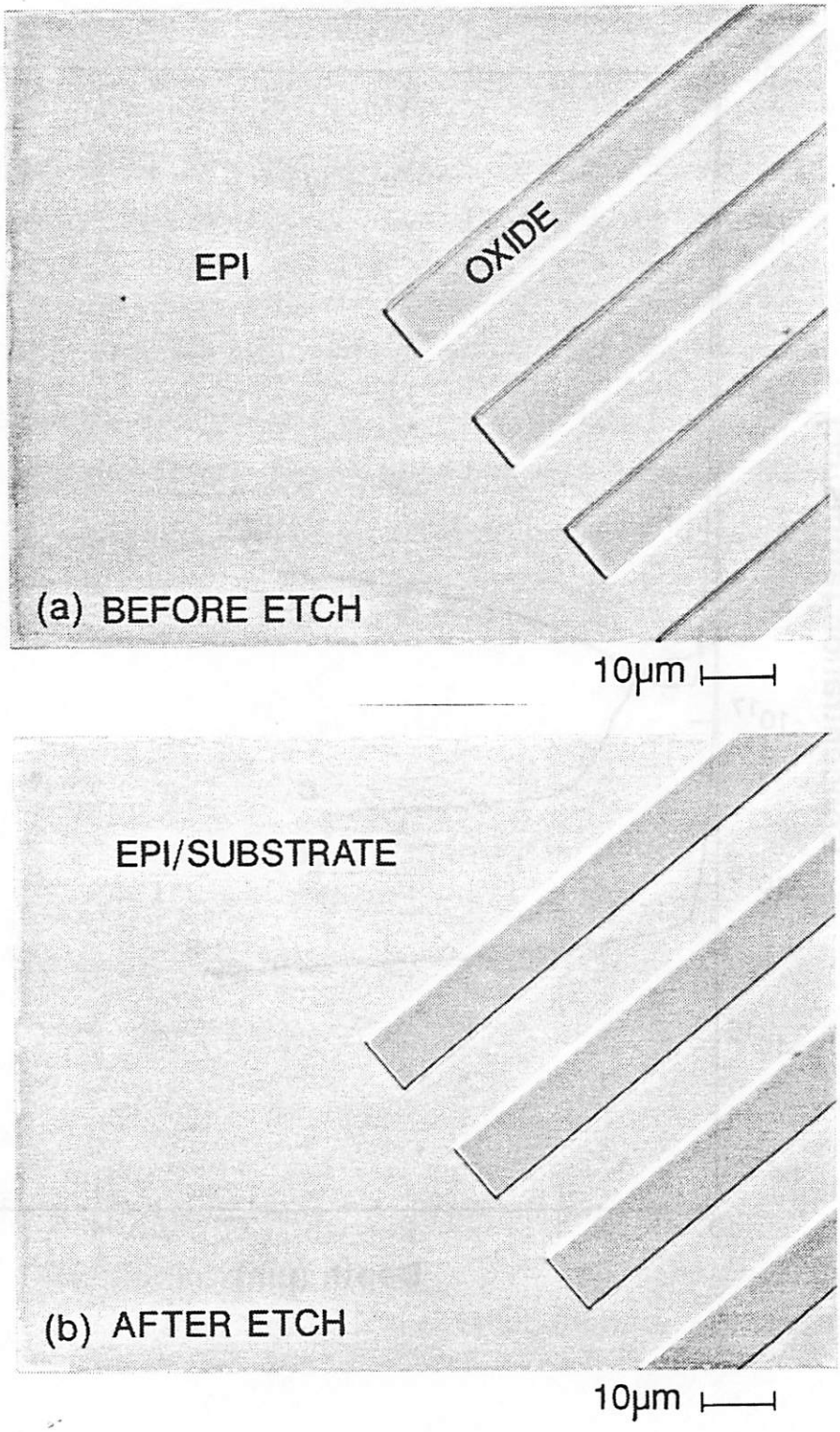


Fig. 16. (a) The Nomarski micrograph (1000X) shows a specular overgrown epilayer with no Si nuclei on oxide areas. (b) The cross-sectional SEM micrograph reveals a specular overgrown epilayer. (c) The XTEM micrograph illustrates no defects in the epitaxial windows and no defects in the overgrown regions. Also, it shows no undercuts along edges of oxide patterns.

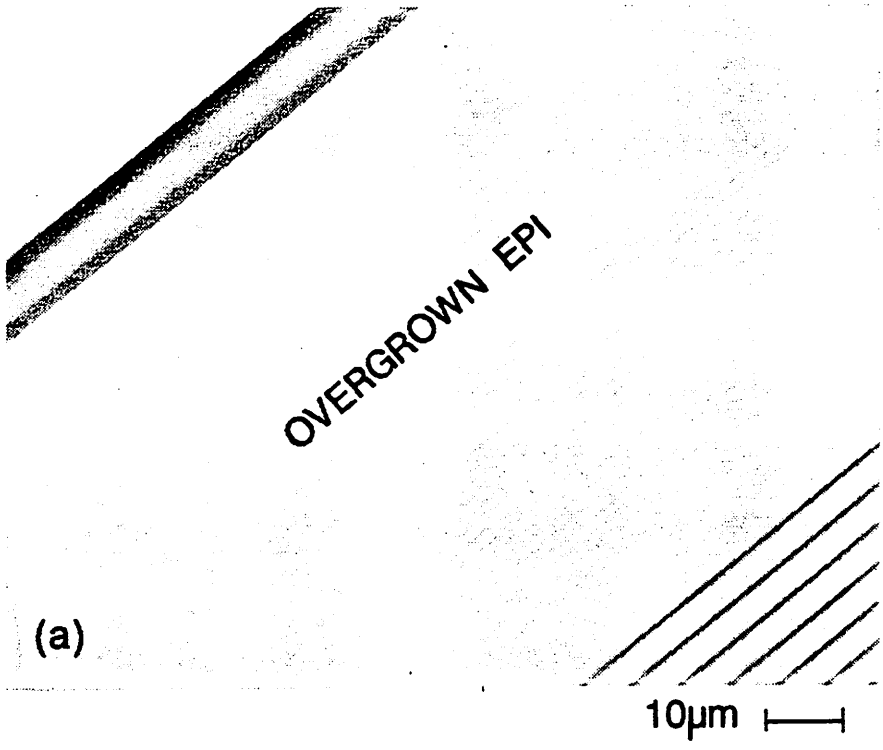
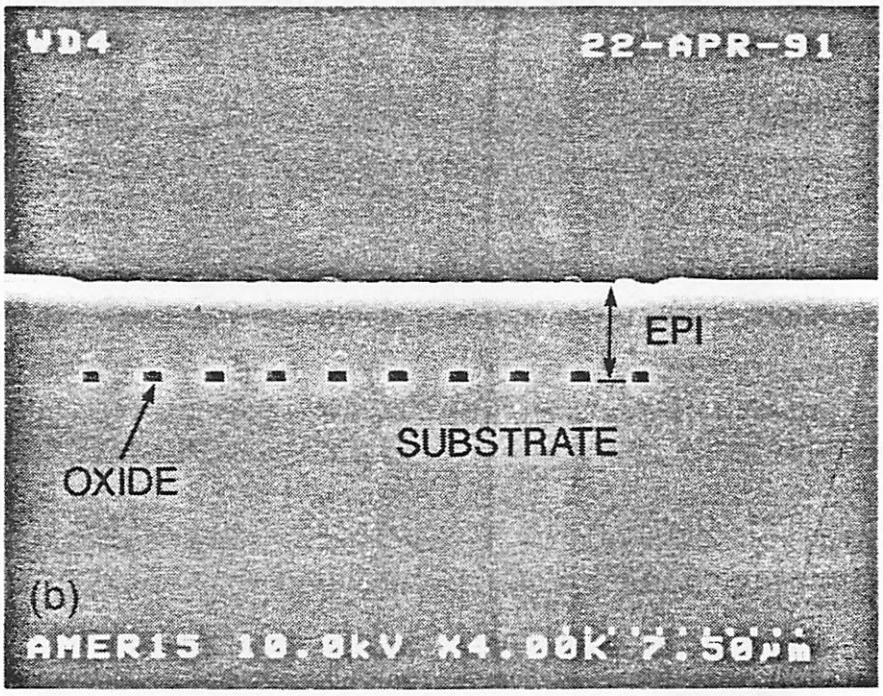


Fig. 16. (cont.)


WD4
22-APR-91
EPI
SUBSTRATE
OXIDE
(b)
AMERIS 10.0kV X4.00K 7.50µm

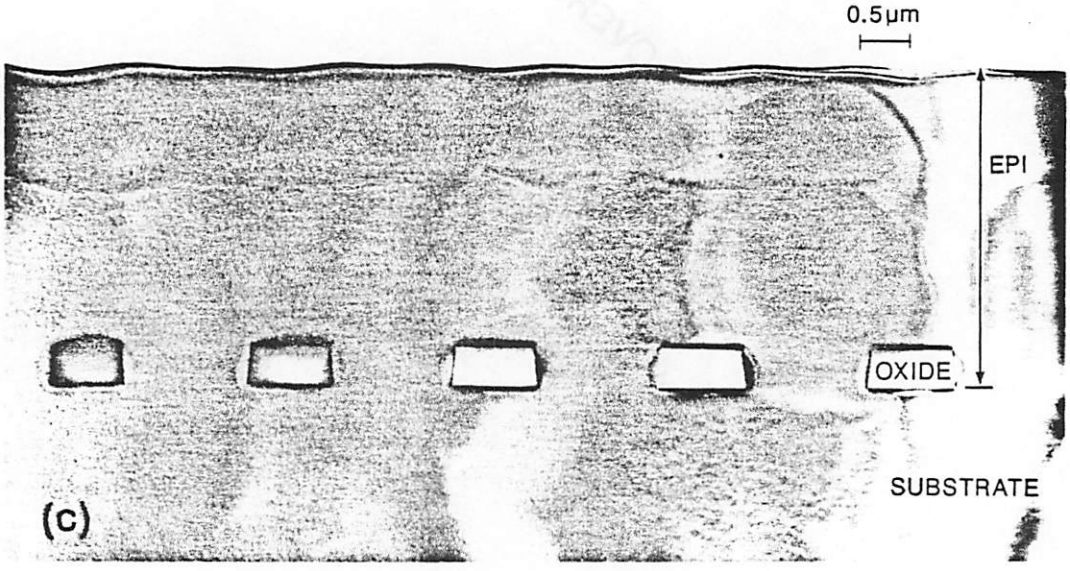

0.5µm
EPI
OXIDE
SUBSTRATE
(c)

Fig. 17. The deposition cycle of a short time epitaxial growth. The flow rate of DCS and H_2 is 2 cc/min and 8000 cc/min, respectively.

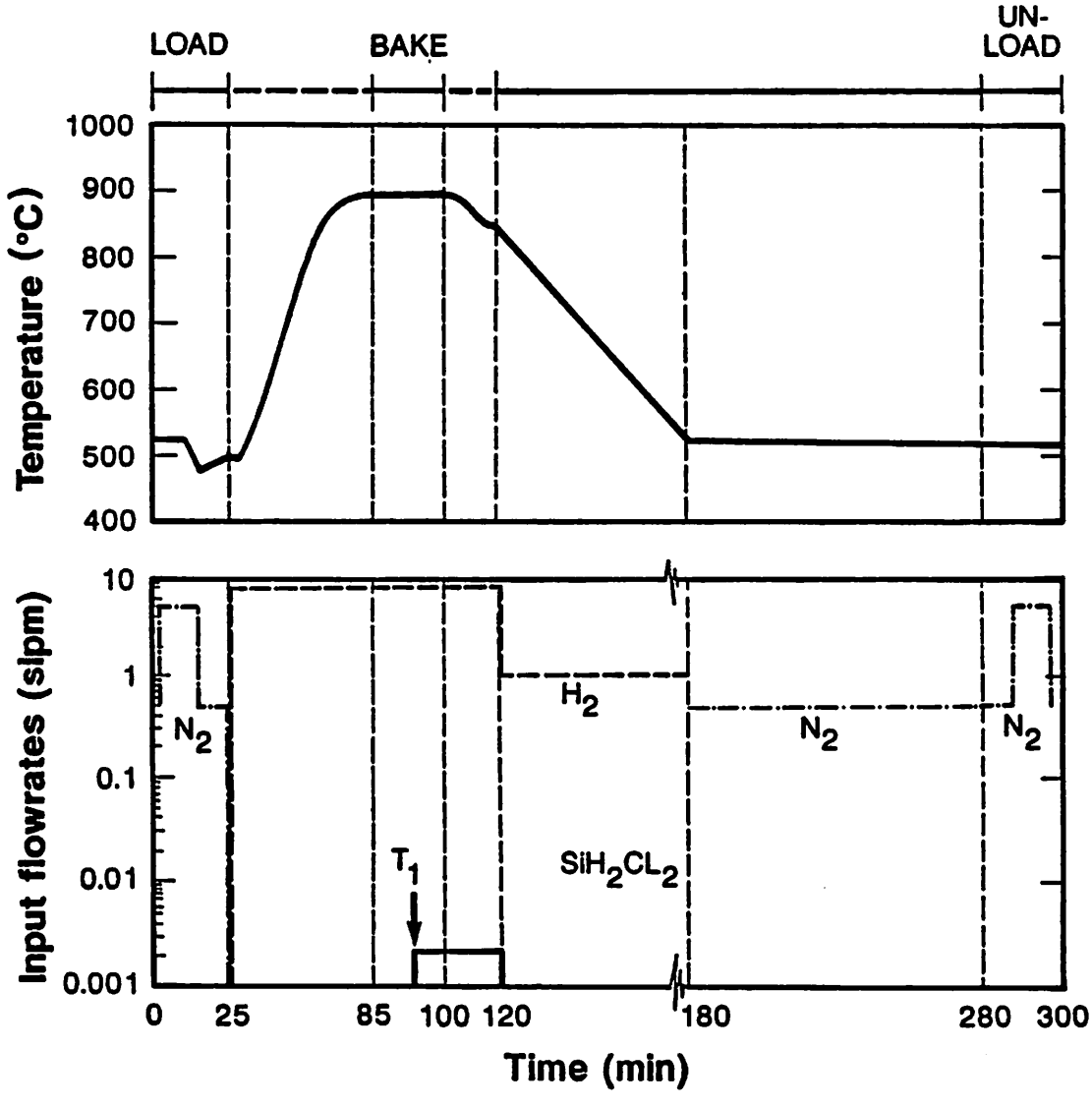
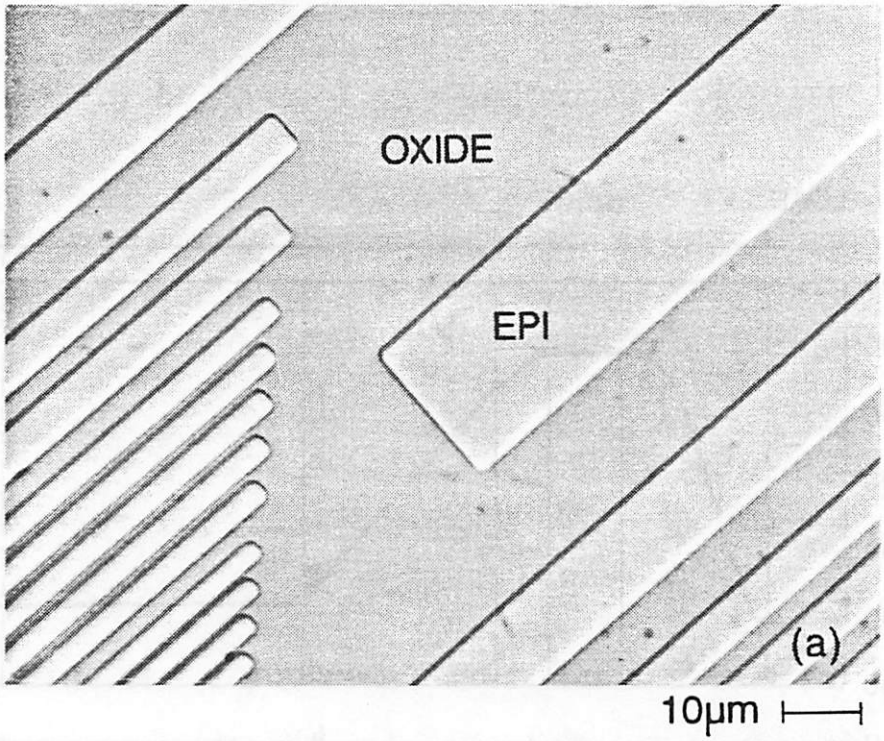


Fig. 18. Nomarski micrographs of a thin epilayer deposited by a low-concentration of DCS in the prebake and the ramp down steps. (a) as-deposited epilayer, (b) after the patterned oxide strip.



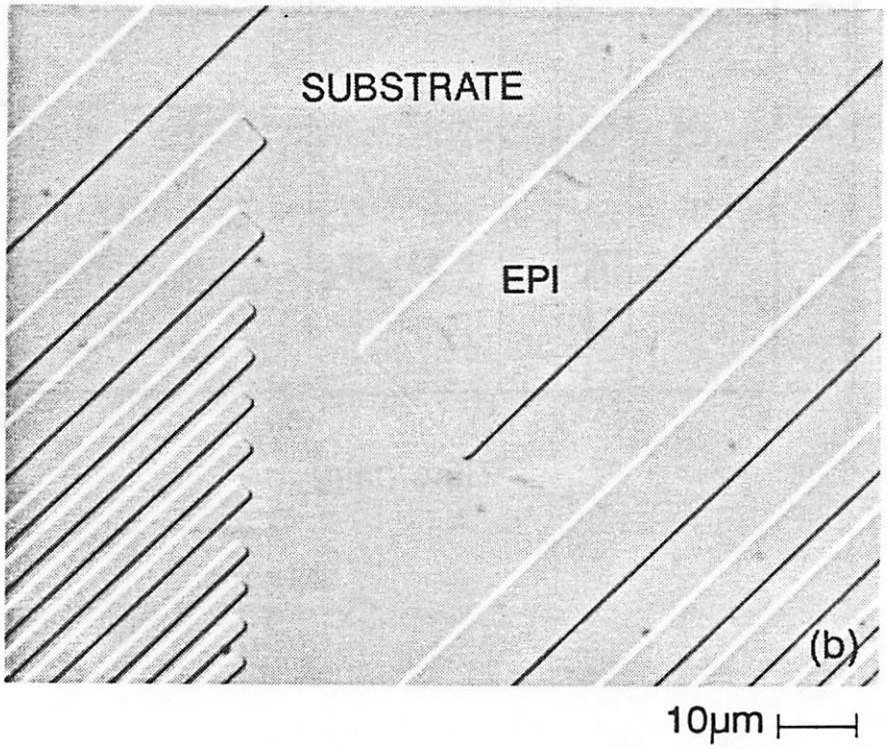


Fig. 19. Nomarski micrographs of the epilayer deposited by a low-concentration of DCS only in the ramp down step . (a) as-deposited epilayer, (b) after the patterned oxide strip.

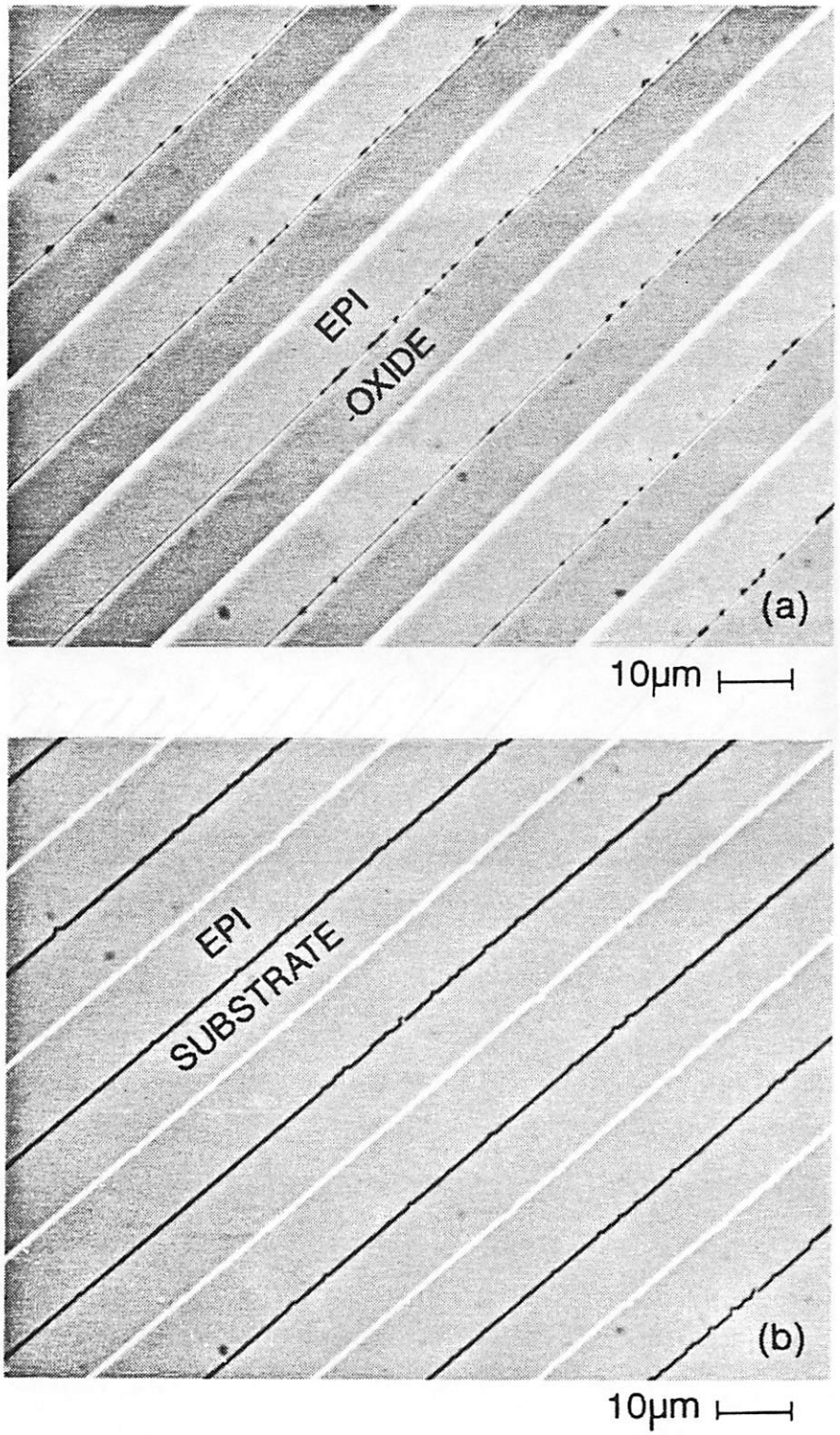


Fig. 20. With an extra 60 min no DCS prebake the Nomarski micrograph shows an epilayer with specular surface morphology and rougher pattern edges.

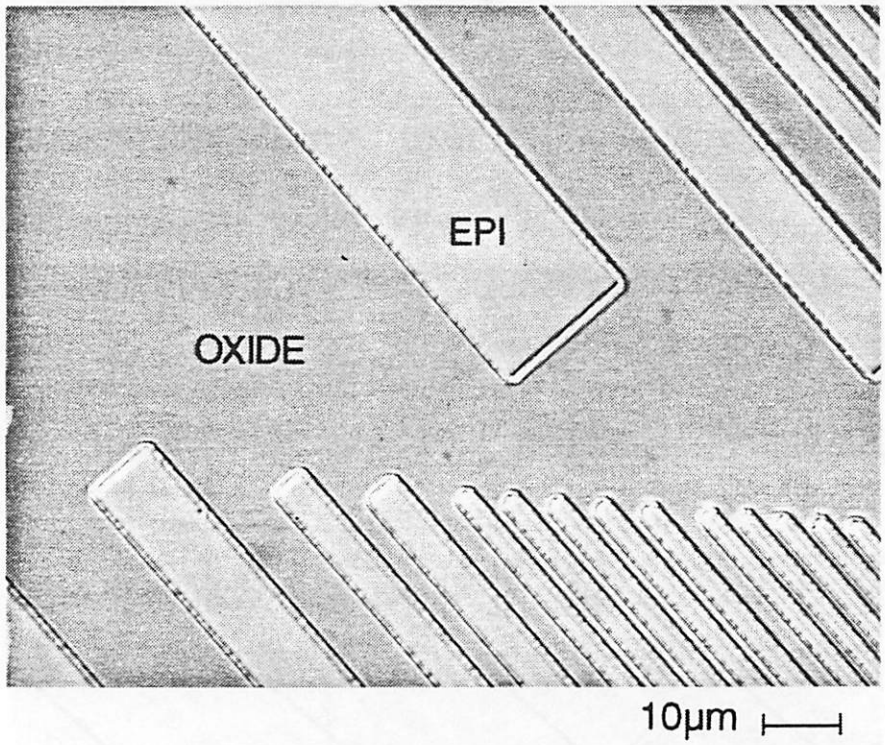


Fig. 21. (a) The XTEM micrograph shows a defect-free epilayer and (b) the plane-view TEM micrograph illustrates a rougher pattern edges for the same specimen in Fig. 20.

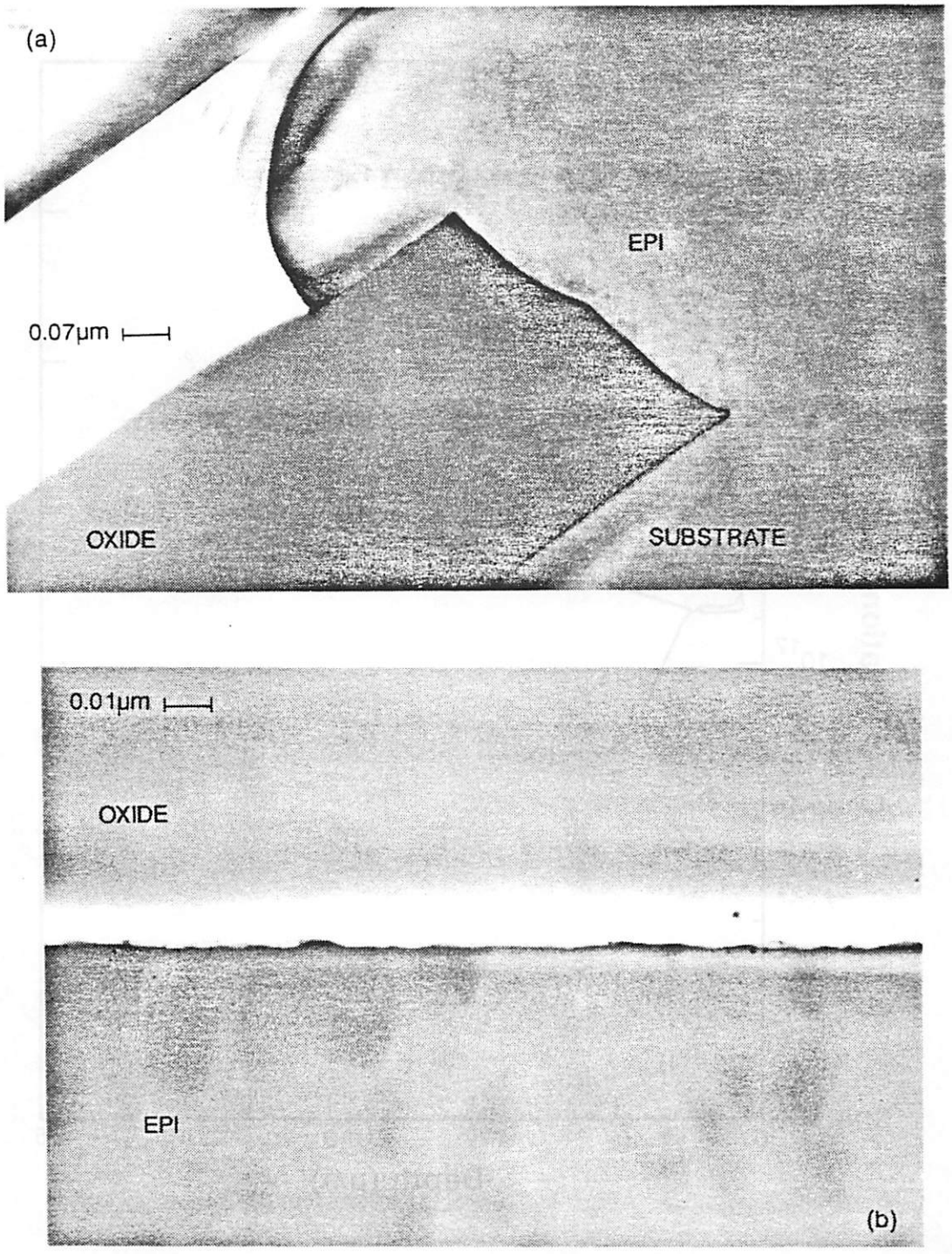


Fig. 22. SIMS analysis indicates no oxygen or carbon peak at the epi/substrate interface for the same specimen in Fig. 20.

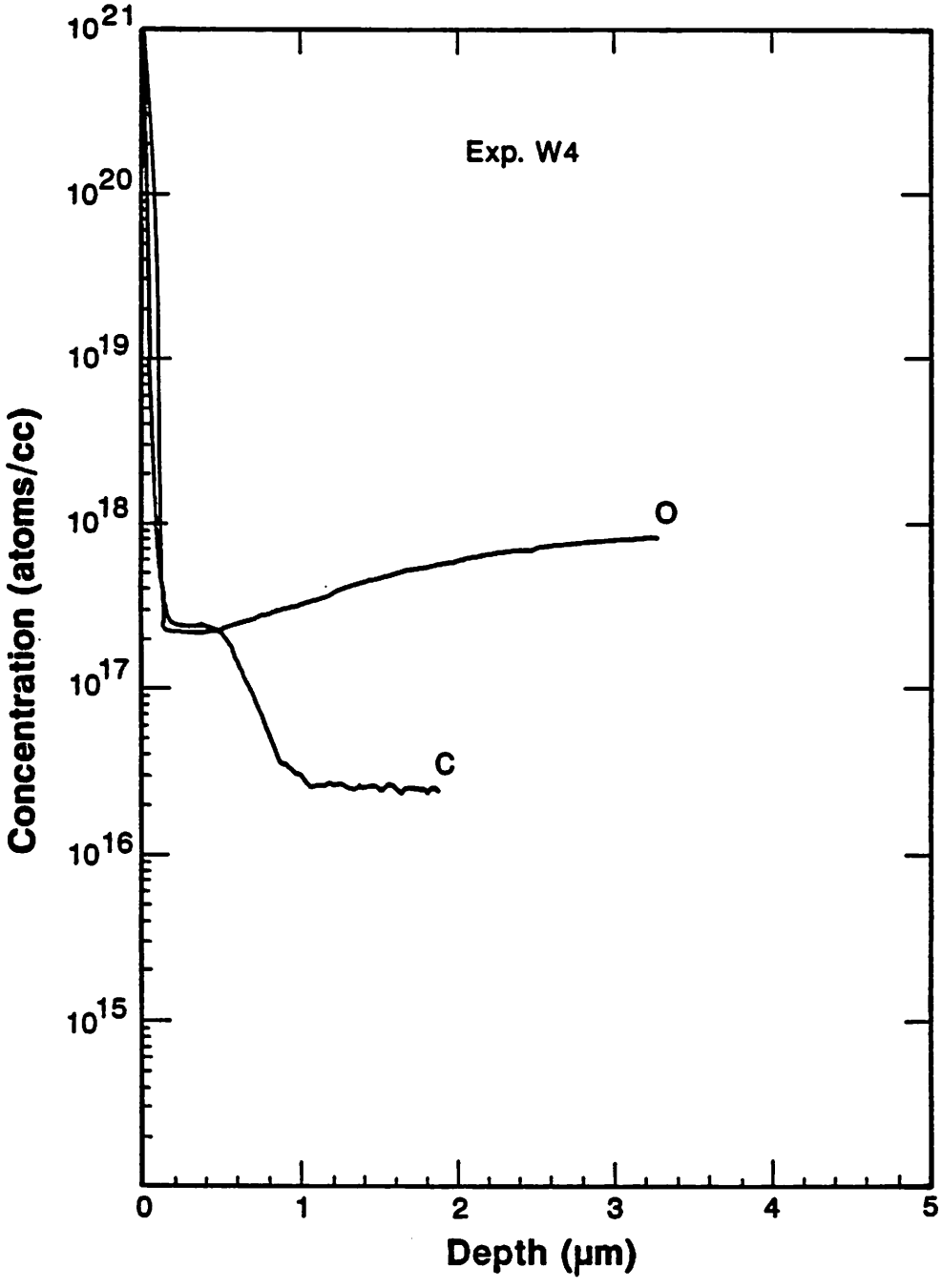


Fig. 23. For the epilayer in the Exp. W_4, (a) the Nomarski micrograph (1000X) of the as-deposited epilayer shows pits near the peripheral area of wafers. (b) After a dilute Schimmel etch it reveals more etched pits at the epi/substrat interface for the same specimen in (a).

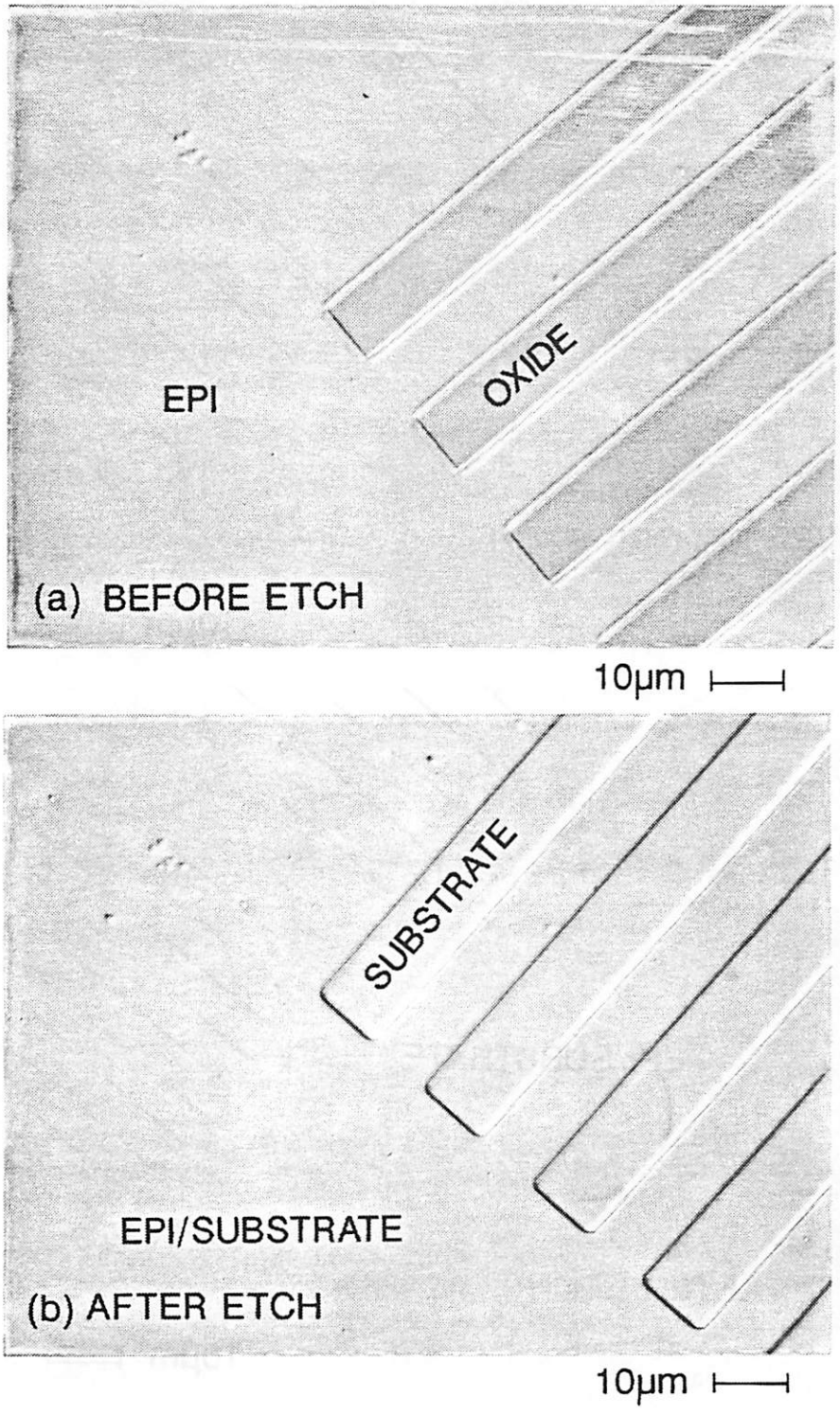
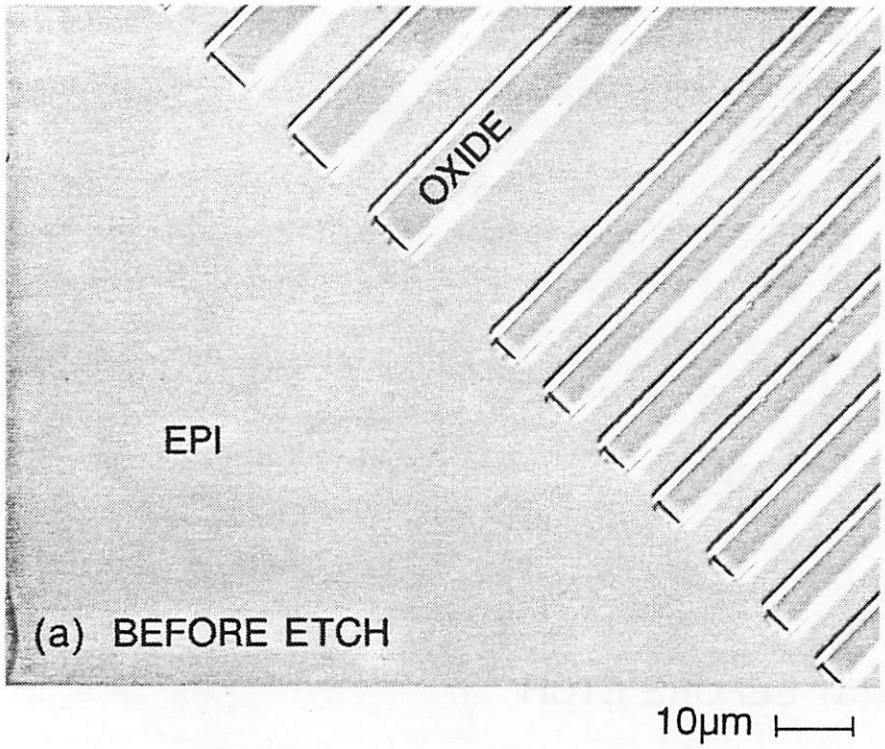


Fig. 24. Nomarski micrographs (1000X) of the epilayer in the Exp. W_4, (a) as-deposited epilayer with square patterns. (b) After a dilute Schimmel etch it shows more etched pits at the epi/substrate interface.



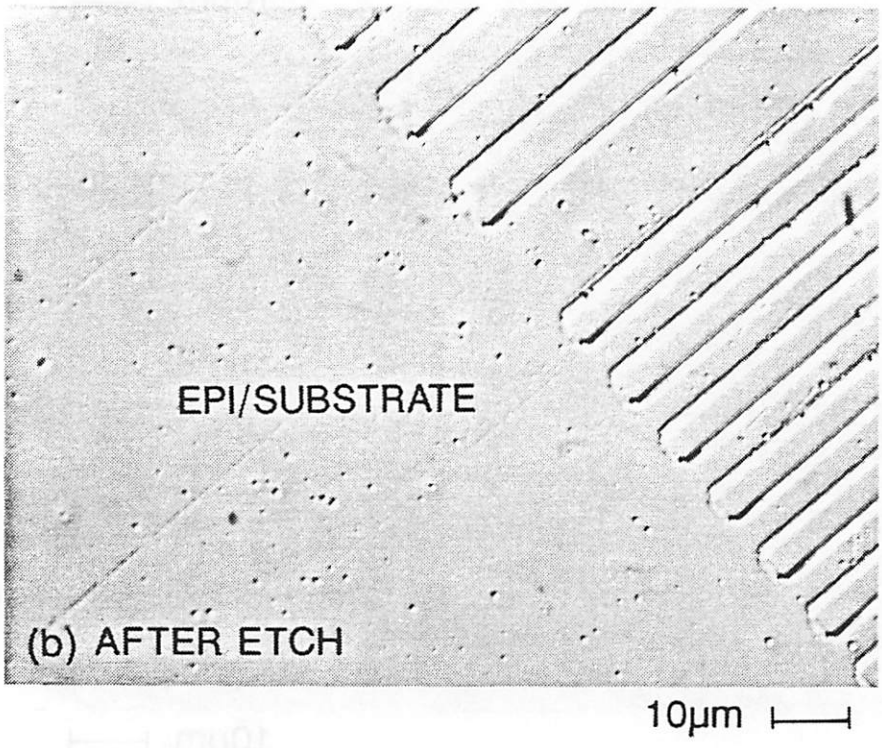


Fig. 25. SIMS analysis of the specimen in Fig. 24 indicates a weak oxygen peak at the epi/substrate interface.

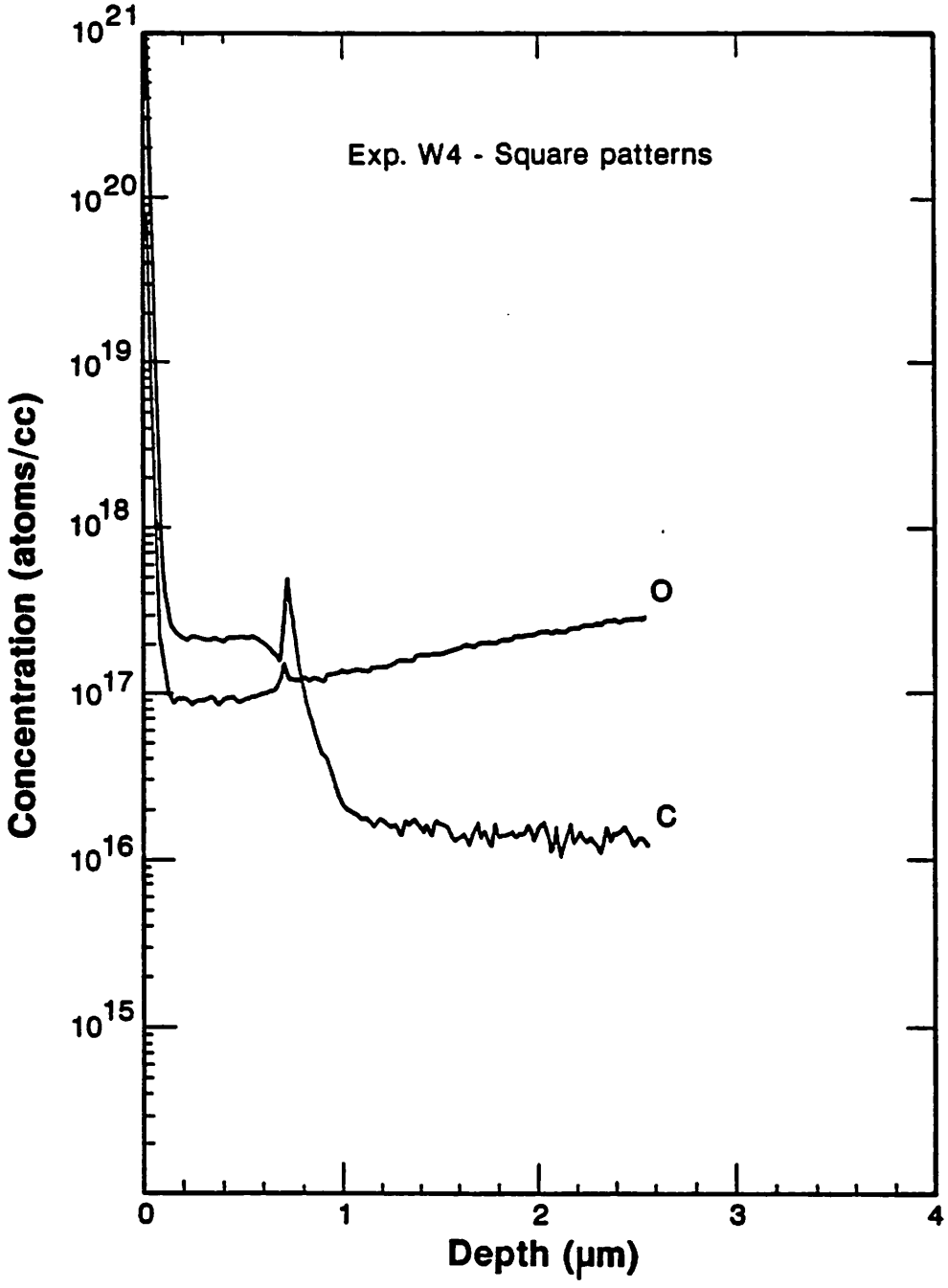


Fig. 26. Nomarski micrographs (1000X) of the epilayer in the Exp. W_5. (a) As-deposited epilayer with pits and square patterns. (b) After a dilute Schimmel etch it reveals more etched pits at the epi/substrate interface.

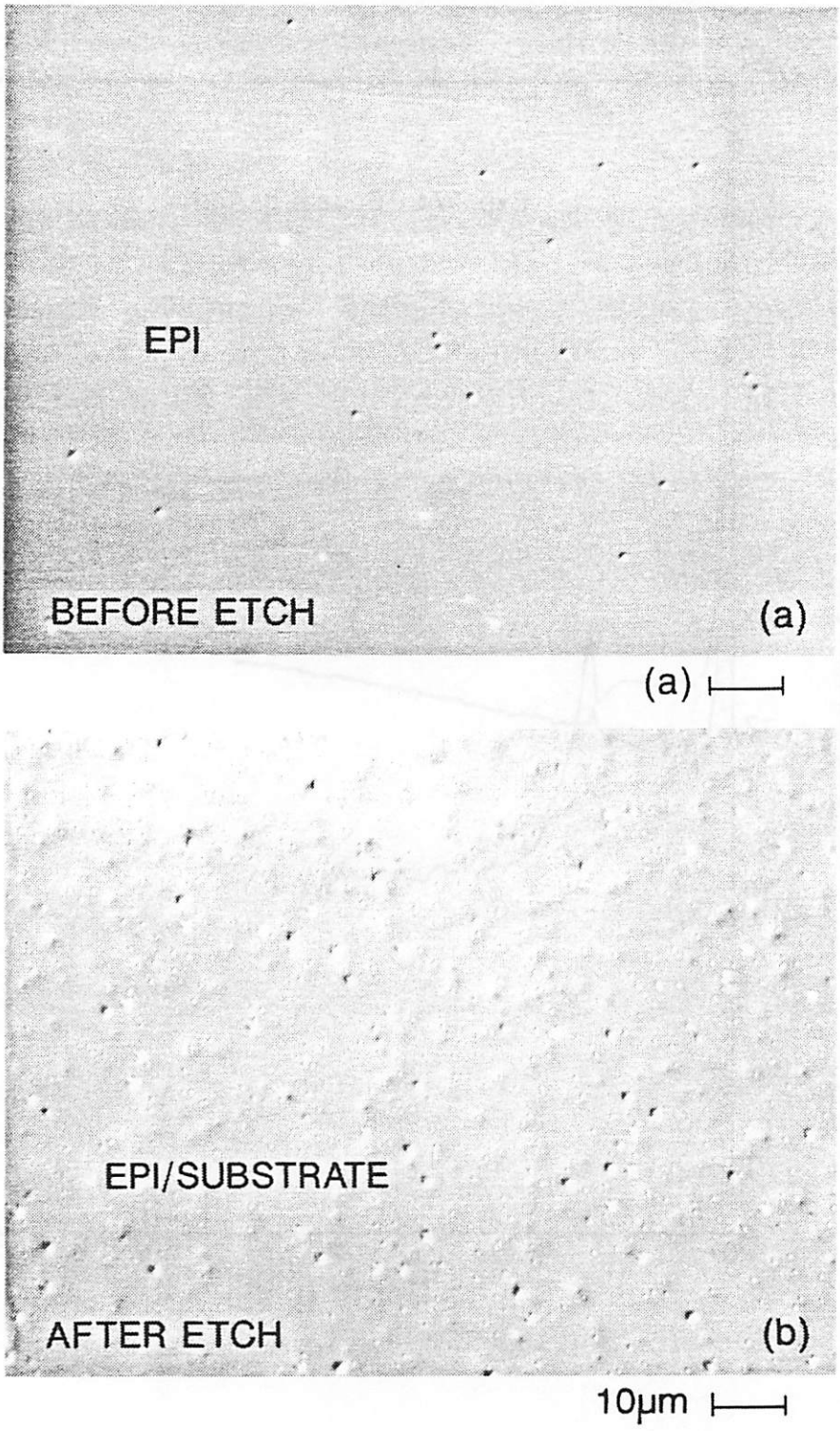
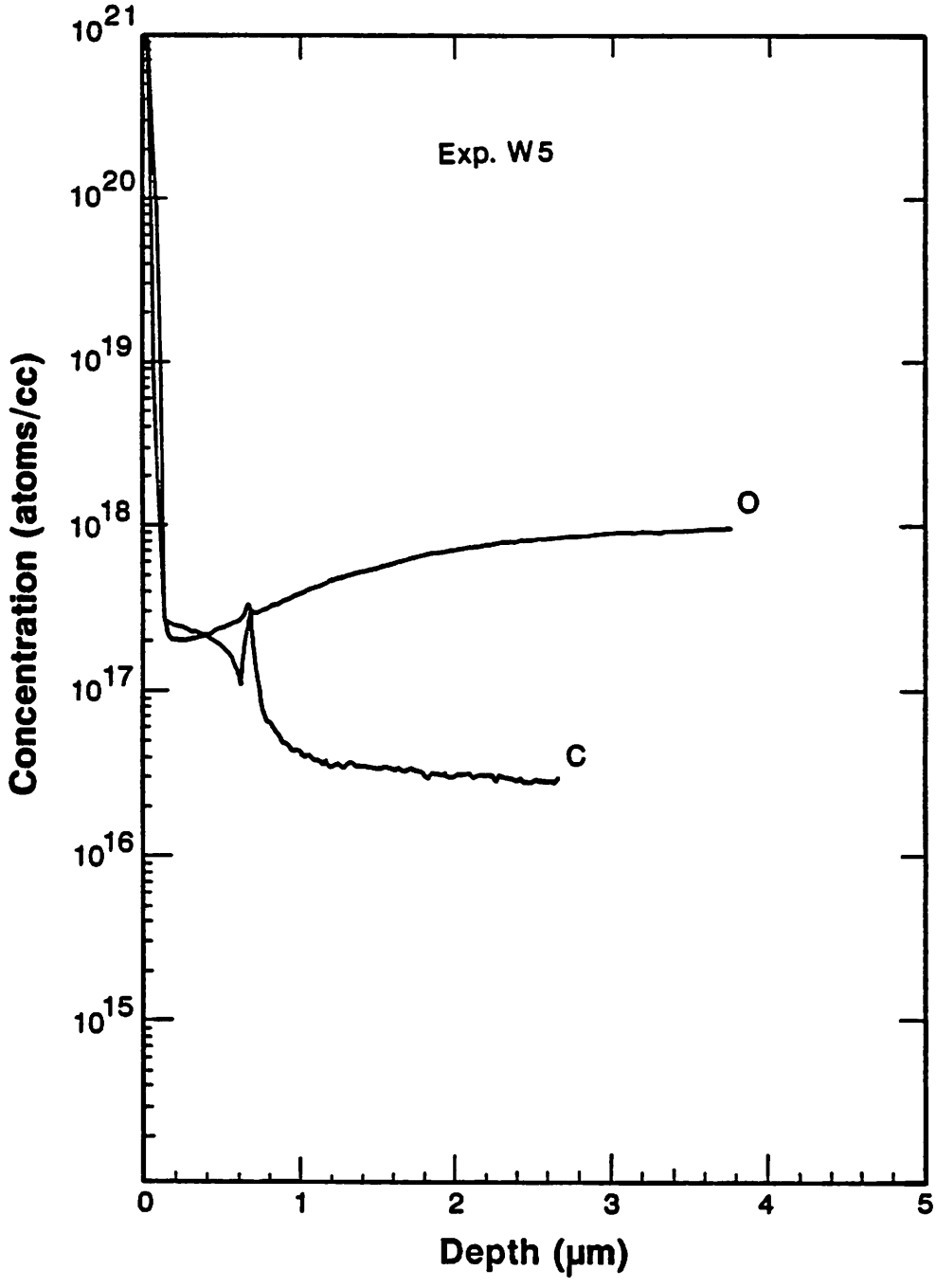


Fig. 27. SIMS results of the epilayer in the Exp. W_5 indicate a weak oxygen peak in the center area of the wafer.



Chapter 3

The Effect of HF Vapor Treatment on the Quality of Epilayers

The presence of surface oxide layers on Si substrates degrades the quality of selectively grown silicon epilayers. We find that an ex-situ HF vapor treatment can overcome this obstacle to achieve high quality epilayers deposited at 850°C after a 900°C prebake. The purpose of this chapter is to present the characteristics of the HF vapor treatment for the selective epitaxial growth of Si. The influence of the composition of H_2O:HF mixtures and the exposure time on the quality of selective epitaxial grown Si epilayers is studied first. BF_2^+ and F^+ ion implantation are also employed to study the fluorine incorporation effect. Finally, the mechanism to explain the effect of the fluorine incorporation on the surface oxide removal is also proposed.

3.1 The Motivation to Study the HF Vapor Treatment

As stated in chapter 2, in the selective epitaxial growth (SEG) of Si, there exists a unique problem of the surface oxide removal. The presence of surface oxide films on Si substrates may prohibit the epitaxial growth, or result in defective epilayers [1-2]. In the past, one way of improving the removal of surface oxide was to use a high-temperature prebake. This could cause significant undercuts [3], due to the decomposition of SiO_2 at the SiO_2/Si substrate interface in H_2, which results in rough pattern edges. An example of the XTEM micrograph of an epi-layer deposited at 850°C after a 1000°C prebake is shown in Fig. 1. The epilayer is defect-free; however, a 1000°C prebake step results in a 1.7 um undercut in which the undercutting rate is about 100 nm/min. Moreover, a high temperature prebake step can degrade the abrupt junction, and thus the device performance.

In order to avoid the formation of undercuts and the degradation of abrupt junctions, a low temperature 900°C prebake is necessarily employed in which the undercutting rate is less than 2 nm/min. However, in doing so, the efficiency of the surface oxide removal is sacrified. This troublesome efficiency loss is due to the relatively higher partial pressure of oxidants in the reactor during the 900°C prebake step [4], making it difficult to remove the surface oxide layers, which prohibits the epitaxial growth. Although a low concentration of dichlorosilane (DCS) is introduced in the prebake and the ramp down steps to improve the epitaxial growth [1-2], an epilayer with dense oxide islands at the epi/substrate interface and threading dislocations in the epilayer still results.

For the purpose of completely removing surface oxide films prior to the deposition and achieving the high quality epilayers, an HF vapor treatment [5] is applied before the wafer loading into the reactor. In this study, we find that the quality of epilayers highly depends on the composition of H_2O:HF mixtures and the exposure duration. Furthermore, it shows that the passivation resluting from the HF vapor treatment can last several hours in the air before the loading the wafers into the reactor. High quality epilayers still can be achieved. In addition, the BF_2^+ and the F^+ ion implantations suggest that fluorine in the oxide layer and at the SiO_2/Si substrate interface plays a major role in the surface oxide removal. For that reason, the goal of this study is to characterize the HF vapor treatment as well as to explore the mechanism of HF passivation and the fluorine incorporation in the surface oxide removal.

3.2 Mechanism for SiO_2 Etch Using HF Vapor

A 1 um thick thermal oxide layer grown at 1000°C on P-type (100) Si substrates is used to characterize the anhydrous HF etching study. The etching of silicon dioxide proceeds through the HF vapor exposure over mixtures of H_2O:49%

HF. The HF vapor is obtained from the equilibrium vapor pressure of HF over mixtures in a plastic beaker in which the diameter of the mouth of the beaker corresponds to that of the wafer. The thickness of silicon dioxide is determined by the ellipsometer and the Nanospec.

The HF vapor etching mechanism involves several steps [6-7]. First, the reactants have to adsorb on the SiO_2 surface. Once the reactants are on the surface, the etching reaction occurs. Subsequently, the products desorb from the surface and diffuse into the gas phase as the reaction is complete. The overall reaction can be written as follows[6-7]:

$$SiO_2 + 4HF \xrightarrow{H_2O(initiator)} SiF_4 + 2H_2O \quad (1)$$

Intermediate reactions include:

$$SiO_2 + 2H_2O \xrightarrow{HF} Si(OH)_4 \quad (2)$$

and,

$$Si(OH)_4 + 4HF \rightarrow SiF_4 + 4H_2O \quad (3)$$

Water vapor must be introduced to initiate the reaction. The presence of water vapor can form a hydrated silicon dioxide $Si(OH)_4$ intermediate which promotes a uniform fluorine adsorption[7]. HF is used as a catalyst in the hydrating reaction (2). Once $Si(OH)_4$ is formed, the etching reaction proceeds. As can be seen from the reaction (3), water is also a byproduct as the reaction proceeds. In this study, the thickness of oxide removed as a function of exposure time to the vapor over three mixtures of H_2O:49% HF is shown in Fig. 2. The amounts of thermal oxide removed are linear with exposure time. The etching rate is 0.26 nm/sec, 0.53 nm/sec, and 1.73 nm/sec for 1:1, 1:2, and 0:1 mixtures of H_2O:49% HF, respectively. This indicates that the HF concentration appears to play a major role in

determining the etch rate.

With inadequate HF vapor treatments; e.g., improper composition of H_2O:HF mixtures or longer exposure durations, we frequently observe water droplets on HF vapor exposed wafer surfaces. In order to understand the origin of the water droplets, a collimated beam of light is employed to reveal the presence of water generated on wafers after an exposure to the HF vapor. The amounts of generated water can be estimated by measuring the time it takes to completely evaporate the water from the wafer surface after each HF vapor exposure. As shown in Fig. 3, the water evaporation time versus the amount of oxide removed after each HF vapor exposure illustrates a linear relationship for both mixtures of H_2O:HF. The longer the exposure of wafers to the HF vapor, the more water is generated on wafer surfaces. This result suggests that the generated water on wafer surfaces indeed results from the oxide etching in reaction (3).

In our study it is found that the thickness of chemical oxide attributed to the piranha immersion is about 1~2 nm. For the purpose of preventing water droplet accumulation on wafer surface and developing a controllable process step, we chose a 5 second exposure over a 1:2 mixture of H_2O:49% HF to remove these chemical oxide layers and also to passivate wafer surfaces with fluorine and hydrogen, while the thermal oxide of patterned areas is removed by about 2.5 nm by this etch. Empirically, this 5 second HF vapor treatment can produce minimal amounts of water on oxide areas and achieve defect-free epilayers deposited at 850°C after a 900°C prebake. As shown in Fig. 4, after a standard HF vapor treatment (5 sec exposure over a 1:2 mixture of H_2O:49% HF), the wafer surface shows no water-droplet-induced residues. However, after a long duration exposure (e.g., 45 seconds), the whole oxide surface is covered by a water layer (H_2O+HF) produced by the reaction (3), as shown by a sequence of Nomarski micrographs in Fig. 5. Because of the evaporation of water, this water layer immediately starts to shrink

into many water droplets on the oxide surface while the oxide etching reaction still proceeds in these water-droplet covered areas. But areas uncovered by water are not etched. As a result, we observe many concave textured spots due to the local overetch on the oxide areas. Etching residues in these spots can initiate nucleation sites for poly-Si during the epitaxial growth. Although a 10 second exposure over 1:1 mixture or a 2 second exposure over 0:1 mixture of H_2O:49% HF can also completely remove the chemical oxide, they occasionally leave water droplets on wafer surfaces which results in poly-Si nucleation on oxide areas after the deposition. In addition, long duration exposure over a 1:1 or 0:1 mixture of H_2O: 49% HF also leaves many water-droplet-induced spots on oxide areas. For that reason, the exposure over a 1:1 mixture of H_2O:49% HF is not preferred even through the exposure step is more controllable.

Finally, wafers with an IR lamp preheat prior to the HF vapor treatment were prepared to demonstrate the effect of water introduction on the initiation of oxide etch. In this experiment, an IR lamp was used to heat the wafer for 10 seconds just prior to the HF vapor exposure. In order to achieve different substrate temperatures, the distance between the IR lamp and the wafer was varied at 5.5", 12.25", and 15". As shown in Fig. 6, The wafers, preheated by an IR lamp at a distance of 5.5", 12.25", and 15" show an induction period of 50 sec, 25 sec, and 5 sec, respectively, to initiate the etching reaction. It is believed that the preheat step can prevent condensation of H_2O on the wafer surface. For that reason, the oxide etch will not proceed until the wafer cools down and allowing enough H_2O desorption. As a result, the induction period observed in etching IR lamp preheated wafers is attributed to the time required for the adsorption of enough H_2O to start the oxide etch on the wafer surface. Also, the rate of adsorption of H_2O is related to the substrate temperatures. Therefore, there exists a longer induction period for wafers with a shorter IR lamp illumination distance. It is obvious that the most important factor

affecting the oxide etch to HF is the amount of H_2O on the oxide surface.

3.3 The Selective Epitaxial Growth Using HF Vapor Treatment

It was found in this study that an ex-situ HF vapor treatment can offer numerous advantages which improve the quality of epilayers grown with a deposition cycle shown in Fig. 7. The most important advantage is to decrease the prebake temperature to 900°C because the fluorine incorporation can enhance the decomposition of surface oxide. Also, this HF vapor treatment can ease the chemical oxide removal and retard the growth of surface oxide before the wafer loading into the reactor. On the other hand, it shows that the quality of epilayers is significantly affected by the composition of H_2O:HF mixtures and the exposure durations. With an inadequate HF vapor treatment, we occassionally observe pits in epilayers and poly-Si nuclei on patterned oxide areas. Hence, this section will discuss the factors of HF vapor treatment affecting the quality of epilayers. A comparision of the quality of epilayers with an adequate or an inadequate HF vapor treatment is also made to give a perspective view of this ex-situ wafer cleaning step. In addition, instead of using the HF vapor treatment, BF_2^+ or F^+ ion implantation is employed to study the effect of the fluorine incorporation. Based on these results, we propose a model to explain the mechanism of the decomposition of fluorine incorporated surface oxide films. It suggests that fluorine in the oxide layer and at the SiO_2/Si substrate interface play a role in the surface oxide removal.

3.3.1 Substrate Preparation for the Selective Epitaxial Growth

P-type boron-doped (100) Si wafers of resistivity 30-50 ohm-cm were used as epitaxial substrates. A photolithographic step was used to define the epitaxial windows on a 570 nm thermal oxide layer grown at 1000°C. Subsequently, the plasma etch process is continued to reach to a depth of 40 nm below the SiO_2/Si

substrate interface to expose epitaxial windows. After the plasma etching and the photoresist removal, a 25 nm sacrificial oxide film was grown at 900°C to eliminate any plasma-etching-induced surface contaminants and damage. The wafers were then subject to a pre-epitaxial clean step consisting of two piranha (H_2SO_4-H_2O_2) cleaning treatments seperated by a dilute HF dip that removes the sacrificial oxide. A very thin chemical surface oxide SiO_x was grown to protect the wafer surface in the second piranha immersion. With a DI water rinse (over 17 mega-ohm) and a spin-dry step, the wafers were subsequently exposed to the HF vapor over a mixtures of H_2O:49% HF for several seconds to removal the chemical oxide and to passivate the wafer surface. The wafers were then immediately loaded into a horizontal hot-wall reactor at 525°C. The deposition cycle is shown in Fig. 7. All wafers were ramped up to 900°C for a 15 minute prebake in a 6 torr H_2 ambient prior to ramping down to the deposition temperature 850°C. A low-concentration flow of DCS was applied in the prebake and the ramp down steps.

Controlled wafers with no thermal oxide layer, patterned by conventional photolithography, were also prepared for BF_2^+ and F^+ ion implantation experiments. The photoresist was used as the mask for the ion implantation. BF_2^+ ions were implanted at the energy of 40 Kev (projected range of 35 nm) in three different fluxes of $10^{12}/cm^2$, $10^{13}/cm^2$, or $10^{14}/cm^2$ into Si (100) wafers at room temperature. F^+ was implanted into (100) Si wafers at the energy of 20 Kev (projected range of 35 nm) in the fluxes of $10^{13}/cm^2$, $10^{14}/cm^2$, and $10^{15}/cm^2$, respectively. Thereafter, a resist strip and a pre-epitaxial clean step were applied. Before the wafer loading into the reactor, the HF vapor treatment was not employed for these BF_2^+ or F^+ implanted controlled wafers. The deposition cycle applied for controlled wafers was the same as that in Fig. 7.

3.3.2 The Quality of Epilayers with HF Vapor Treatment

With our standard HF vapor treatment (5 second exposure over a 1:2 mixture of H_2O:49% HF), high quality epilayers are obtained. The Nomarski micrograph in Fig. 8 shows a specular epilayer with smooth edges. There are no poly-Si nuclei on the oxide surface. Furthermore, XTEM micrographs, as illustrated in Fig. 9, shows no undercuts near corners, no oxide islands at the epi/substrate interface, or threading dislocations in the epilayer. In Fig. 10 The dilute Schimmel etch reveals no etched pits as the etching front approaches the epi/substrate interface. SIMS analysis, as shown in Fig. 11, indicates no oxygen, carbon, or fluorine peak at the epi/substrate interface. It is obvious that this epilayer is defect-free and specular.

However, with inadequate HF vapor treatments, the quality of epilayers is degraded. As shown in Fig. 12(a), with a 45 second exposure over the 1:1 mixture of H_2O:49% HF, we observe pits in epilayers and poly-Si nuclei on the oxide surface. The edges of the epilayer are very rough. We propose that water residues, attributed to the evaporation of water from the mixture, retards the removal of chemical oxide from the Si surface or reoxidizes passivated Si surface. This yields pits in epilayers, while the water-droplet-induced residues in oxide areas yields poly-Si nuclei on oxide surface after the deposition. A long duration exposure over the 2:1 or 0:1 mixtures also yields epilayers with rough edges, and poly-Si nuclei on oxide surface, as shown in Fig. 12(b) and 12(c). Fig. 13 shows a round-shaped trace resulted from the shrinkage of water droplet after the HF vapor treatment. Nanospec measurement indicates that the oxide thickness inside this round-shaped area is about 25 nm thinner than those outside this area. It is evident that the oxide etch still proceeds in the water droplet covered area while the water droplet shrinks. An overetch induced spot is formed in the center of this round-shaped area. Poly-Si is deposited at this spot after the epitaxial growth.

3.3.3 Air Exposure Effect After the HF Vapor Treatment

The Si surface is known to be passivated after the HF vapor treatment. The presence of a hydrogen- and fluorine-terminated Si surface can retard oxidation [8-9]. For the purpose of studying HF passivation, some substrates with a standard HF vapor treatment were exposed to the air in the class 100 clean room for several hours before the loading into the reactor. After the epitaxial growth, wafers with an 18 hour air exposure had specular epilayers with smooth edges, as indicated by the Nomarski micrograph in Fig. 14. However, for longer air exposure, pits were observed in the epilayers and the edges become rough. As shown in Fig. 15, with a 61 hour air exposure after the HF vapor treatment, epilayers with dense small pits and rough edges were obtained. Moreover, with a 73 hour air exposure, epilayers were almost textured. It is understood that the initial Si surface is passivated by hydrogen (Si-H) and fluorine (Si-F). At room temperature the Si-H bonds on the surface are more stable against the oxidation than Si-F bonds due to the higher electronegativity of fluorine [10]. Fluorine can gradually desorb from the Si surface through the hydrolysis or the oxidation reaction during an air exposure. On the other hand, Yu et al [11] indicate that in the absence of water (<1 ppm) or in a very clean environment the amount of desorption of fluorine from HF treated Si surface is negligible. Therefore, we believe that with the air exposure, there are rapid reactions between Si-F and H_2O or between Si-F and oxygen to form Si-OH or Si-O bonds on Si surface. Consequently, SiO_2 nuclei result. The size of the oxide patches increases with exposure duration. For that reason, the advantage of the HF vapor treatment is no longer maintained on these patchy oxide areas. Our previous results [1] indicate that once there is an oxide layer before the loading, epilayers with interfacial oxide islands form even with a low-concentration of DCS in the prebake and the ramp down steps. We therefore obtain defective epilayers with pits or textured features after the epitaxial growth for substrates with a long

duration air exposure. In addition, most of the interfacial oxide islands are decorated by pits on the Si surface. The textured surface morphology is caused by a high density of fine pits.

3.3.4 BF_2^+/cm^2 and F^+/cm^2 Ion Implantation

For wafers with a low-flux 40 Kev BF_2^+ ion implantation (e.g., $10^{12}/cm^2$, and $10^{13}/cm^2$), Nomarski micrographs in Fig. 16 show textured surface morphology on the implanted and un-implanted regions. However, for the flux of $10^{14}/cm^2$, as illustrated in Fig. 17(a), the wafers show specular epilayers on implanted areas and textured epilayers on un-implanted areas. Furthermore, the XTEM micrograph in Fig. 17(b) highlights the interface between the implanted and the un-implanted regions. It shows a defect-free epilayer on the implanted region, and a defective epilayer with interfacial oxide islands, voids, and threading dislocations on the un-implanted region. The structural configuration of the defective epilayer is the same as the previous results [1-2]. As shown in Fig. 18, secondary ion mass spectroscopy (SIMS) results of defective epilayers indicate large oxygen, carbon, and fluorine peaks at the epi/substrate interface. It is believed that this fluorine peak is attributed to the HF dip in the wafer clean step. On the other hand, it indicates no oxygen, carbon, or fluorine peak at the epi/substrate interface on the regions implanted with $10^{14}/cm^2$ BF_2^+ ions. As a result, it is evident that BF_2^+ ion implantation of suitable fluxes is a powerful method which improves the surface oxide removal prior to the deposition, and then results in high quality epilayers grown at 850°C after a 900°C prebake.

In order to further understand the effect of fluorine on the quality of epilayers, 20 Kev F^+ ion implantation was also employed. The F^+ ion implanation shows results similar to BF_2^+. For an implantation flux of $10^{14}/cm^2$ or less, as illustrated in Fig. 19, wafers show a textured surface morphology on implanted and un-

implanted regions. However, for an implantation flux of $10^{15}/cm^2$, as shown in Fig. 20(a), the layers are specular on implanted regions and textured on un-implanted regions. The XTEM micrograph of the interface between the implanted and the un-implanted regions in Fig. 20(b) again exhibits a defect-free epilayer on the implanted region and a defective epilayer on the un-implanted region. It illustrates a high density of oxide islands and voids at the epi/substrate interface, and threading dislocations in the epilayer of the un-implanted region. Again, no interfacial oxide islands, voids, or threading dislocations are observed in the epilayer on the region implanted with $10^{15}/cm^2$ F^+ ions. SIMS results of the same specimen, shown in in Fig. 21, further indicates no oxygen, carbon, or fluorine peak at the epi/substrate interface. The examination of several specimens consistently shows high quality epilayers on BF_2^+ of F^+ implanted regions with suitable ion fluxes, but defective epilayers on un-implanted regions. Based on these observation and our HF vapor treatment results [1,5], we hypothesize that the fluorine atoms may be helpful for removing of surface oxide films during the prebake and achieving a clean Si surface prior to the deposition.

3.3.5 The Mechanism of Surface Oxide Removal with Fluorine Incorporation

After the wafer clean, the Si surface is covered with a very thin chemical oxide (1 nm SiO_x) grown in the second H_2SO_4-H_2O_2 immersion step. This thin chemical oxide layer may grow thicker through the subsequent air exposure before the wafer loading into the reactor and/or the oxidation due to the oxidants in the reactor during the ramp up, prebake, and ramp down step. Our previous results [2] show that the thickness of oxide islands at the epi/substrate interface is about 6-7 nm. During the thermal cycle, it is understood [12-15] that at the prebake temperature there exists a critical pressure below which the decomposition of surface oxide

take place by the reaction

$$Si + SiO_2 \rightarrow 2SiO\uparrow \quad (4)$$

Liehr et al [14] and Hofmann et al [15] further indicate that the oxide decomposition process starts at defect sites near the SiO_2/Si interface which forms pinholes in oxide layer. Also, the amount of pinholes is almost unchanged with continuous anneal. Therefore, as the annealing step proceeds, the size of pinholes increases and results in isolate oxide islands on the substrate surface. As a result, the surface oxide is completely removed. However, if oxidants are present in the annealing ambient, the SiO formed at the interface can be reoxidized by the reaction

$$2SiO + O_2 \rightarrow 2SiO_2 \quad (5)$$

The competition between the reactions shown in Eq. (4) and Eq. (5) determines if the decomposition of surface oxide proceeds. Therefore, it is obvious that the partial pressure of oxidants in the reactor controls the efficiency in the decomposition of surface oxide. Even through the decomposition of SiO_2 is preferred, in case where the partial pressure of oxidants is high, the decomposition of surface oxide becomes less efficient than those with lower partial pressure of oxidants. As a result, fewer pinholes appear in the surface oxide and the size of pinholes may be smaller. In this study, the hydrogen induced undercutting effect [3] also plays an important role in removing the surface oxide layer. For that reason, we propose an explanation for the surface oxide removal in our hydrogen prebake step. First, the decomposition of surface oxide occurs at defect sites near the SiO_2/substrate interface and subsequently results in pinholes. Once pinholes appear in the thin surface oxide layer, hydrogen starts to laterally undercut the surface oxide from these pinholes, which shrinks the area of this thin surface oxide layer. However, whether this surface oxide can be completely removed prior to the deposition depends on these issues:

(1) the density of pinholes which is determined by the defect concentration at the SiO_2/Si interface, (2) the transport of SiO through the surface oxide layer, (3) the reoxidation rate which is dependent on the partial pressure of oxidants, (4) the undercutting rate which is prebake temperature dependent, (5) the prebake duration, and (6) the outgassing rate of oxidants which were previously absorbed on the reactor wall. Hence, for a short prebake or an increasing oxidant pressure, there still may be many SiO_2 patches prior to the deposition which can result in defective epilayers. Also, in the ramp-up and the prebake steps, the outgassing rate on the cool ends of the reactor may increase and change the equilibrium condition between the Eq. (4) and the Eq. (5) which retards the surface oxide removal rate. Although we add a low-concentration of DCS in the prebake and the ramp-down periods to drop the partial pressure of oxidants, from the results of textured epilayers, there appears to be many unremoved oxide patches prior to the deposition [1-2]. With the same deposition cycle, we believe that issues from (2) to (6) will not play major roles in changing the removal rate of the surface oxide.

One method to enhance the surface oxide removal rate is to increase the concentration of defect sites at the SiO_2/Si substrate interface. We hypothesize that the HF vapor treatment can introduce fluorine at the SiO_2/Si substrate interface and in the surface oxide. Fluorine atoms at the SiO_2/Si substrate interface can act as defect sites for the decomposition of surface oxide which increases the pinhole density in the surface oxide during the thermal cycle. Consequently, the removal rate of surface oxide increases. Furthermore, with suitable ion fluxes, BF_2^+ and F^+ ion implantation employed to study this hypothesis also show the enhancement in the surface oxide removal and higher quality epilayers. Based on these results, we therefore believe that the fluorine incorporation plays a major role in yielding a clean Si surface prior to the deposition, and in achieving high quality epilayers deposited at 850°C after a 900°C prebake.

It was found [16] that fluorine is a fast diffusant. After the anneal, most of fluorine atoms may diffuse out of Si surface and segregate in the SiO_2 layer. Fluorine atoms in the surface oxide layer may cleave Si-O bonds to form Si-F bonds [16]. Some of Si-F bonds may further become volatile SiF_4 molecules which then desorb out of the oxide layer and create more pinholes in the surface oxide layer. This more porous surface oxide layer can favor the invasion of hydrogen to the SiO_2/substrate interface and the transport of volatile SiO through the oxide. The residual fluorine atoms near the SiO_2/substrate interface form defect sites initiating the decomposition of the surface oxide layer. Consequently, the increase in the concentration of defect sites, which are attributed to the fluorine incorporation, can produce more pinholes in the surface oxide layer. The exact amount of residual fluorine atoms near the SiO_2/substrate interface is unknown. However, we can roughly calculate the minimum required amount of residual fluorine atoms at the SiO_2/substrate interface. Because the undercutting rate is about 2 nm/min at 900°C [3], each isolated fluorine atom initiating a defect site near the SiO_2/substrate interface can produce a round-shaped hole with a radius of 30 nm on oxide layer after a 15 minute prebake. If the residual fluorine atoms are uniformly distributed at the SiO_2/substrate interface, then there must exist at least a residual fluorine atom in the center of each hexagon with a edge of 30 nm prior to the prebake. Hence, it requires at least $5x10^{10}$ fluorines/cm^2 at the SiO_2/substrate interface to completely remove the surface oxide layer. Therefore, with fluxes not generating enough residual fluorine atoms at the SiO_2/substrate interface prior to the prebake, defective epilayers are always obtained.

Now the question is whether other kinds of ions can also create defect sites at the SiO_2/Si substrate interface to enhance the decomposition of surface oxide layers. According to Liehr et. el. [14] and Hofmann et. al. [15], metal impurities can also serve as defect sites for the pinhole formation. However, metal impurities

do not form volatile molecules in the oxide and change the structure of surface oxide layer to a more porous oxide. On the other hand, Eq.(4) indicates that the decomposition of surface oxide is also affected by the transport of SiO from the interface to the oxide surface. Hence, even with metal impurities acting as defect sites for the decomposition of the surface oxide layer at the SiO_2/Si substrate interface, the densified surface oxide layer may slow the SiO to break and/or diffuse through the overlying oxide layer which retards the decomposition rate of the surface oxide in Eq. (4). Although a high temperature and long duration anneal can improve the removal of surface oxide layer, the significant interdiffusion and outdoping effect may degrade the device performance. In order to meet the requirements of ultralarge-scale integration (ULSI) applications, a low temperature (e.g., 900°C), short duration thermal cycle to remove the surface oxide layer is necessary. As mentioned above, with the incorporation of fluorine atoms, the segregation of fluorine atoms in the surface oxide can form volatile SiF_4 to achieve a more porous surface oxide, which enhances the SiO transport through the oxide and the invasion of hydrogen to the SiO_2/Si substrate interface. As a result, fluorine incorporation in the reaction of the surface oxide decomposition would be more efficient than the other impurities.

3.4 Summary

The characteristics of the HF vapor treatment through the reaction of the chemical oxide removal before the wafer loading into the reactor is discussed. The mechanism of fluorine incorporation through the reaction of the surface oxide decomposition during the thermal cycle is also presented.

It is found that water vapor on the oxide surface is the most important factor to initiate the oxide etch reaction. Also, the concentration of HF in the mixtures plays a major role in determining the oxide etch rate. Basically, the amounts of

thermal oxide removed are linear with the exposure time. Water droplets are occasionally observed on oxide after the HF vapor treatment. These water droplets dissolving HF can still proceed with the etching reaction while shrinking, which results in nucleation sites for poly-Si. Empirically, we find that a 5 second exposure over the 1:2 mixture of H_2O:49% HF can not only completely remove the chemical oxide layer but also generate minimum water moisture on substrates, and consequently results in defect-free epilayers. We also find that HF passivation can last about 18 hours in the air to yield high quality epilayers. However, substrates with longer air exposure duration (over 18 hours) after the HF vapor treatment show epilayers with pits and/or textured features.

There are several issues controlling the surface oxide removal. The most important issue in our LPCVD selective epitaxial growth is the defect sites initiating the decomposition of surface oxide at the SiO_2/Si substrate interface. We propose that the HF vapor treatment can increase the concentration of defect sites at the SiO_2/substrate interface which enhances the decomposition of surface oxide, and also results in a more porous surface oxide to favor the invasion of H_2 and the transport of SiO through the surface oxide layer. With BF_2^+ and F^+ ion implantation instead of the HF vapor treatment, defect-free epilayers are obtained at 850°C. These results show that fluorine incorporation is helpful to the surface oxide removal during the thermal cycle and results in a oxide-free Si surface prior to the deposition.

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Fig. 1. The XTEM micrograph of an epilayer deposited at 850°C after a 1000°C prebake. It shows no defects in the epilayer or at the epi/substrate interface. There is a high temperature prebake induced undercut along the oxide/substrate interface.

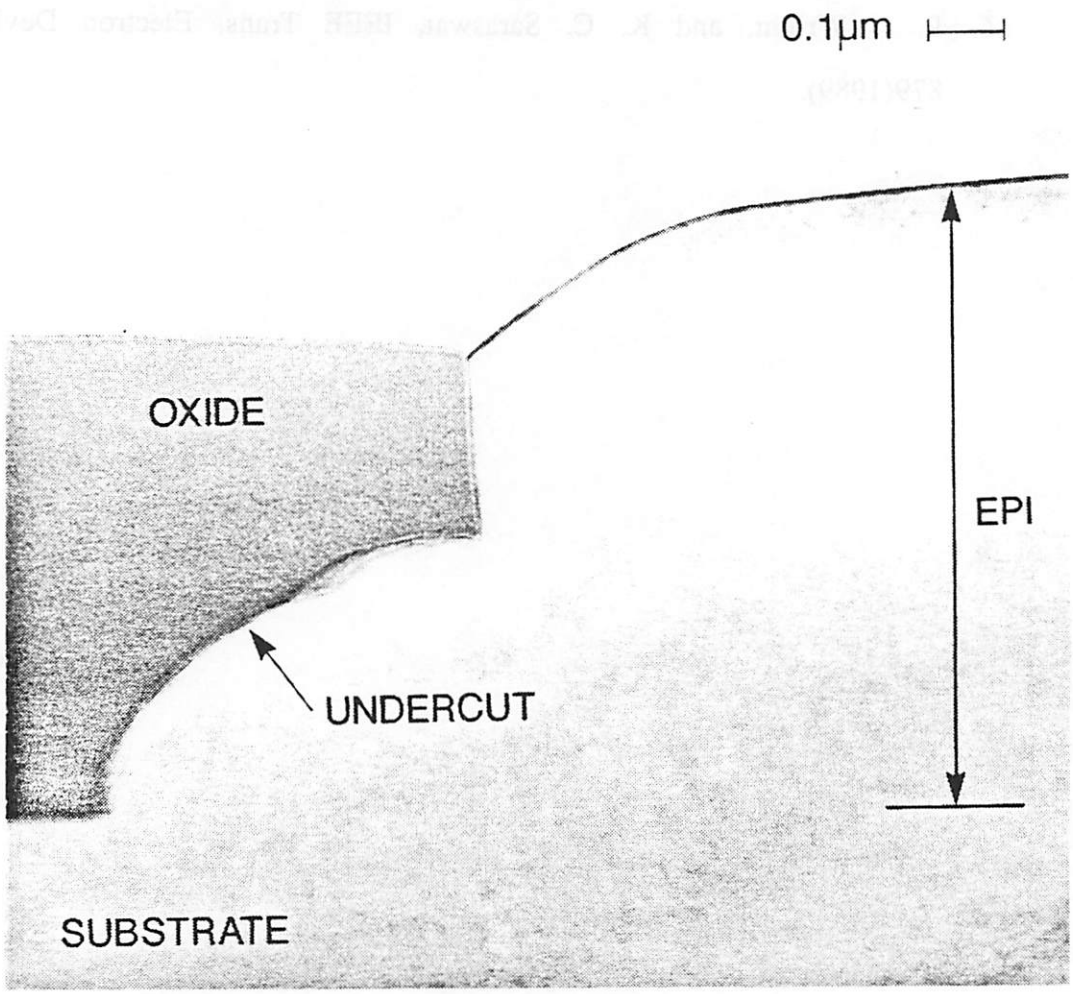


Fig. 2. The amounts of thermal oxide removed versus exposure time to the vapor over three mixtures of H_2O:49% HF. The etch rate is highly HF concentration dependent.

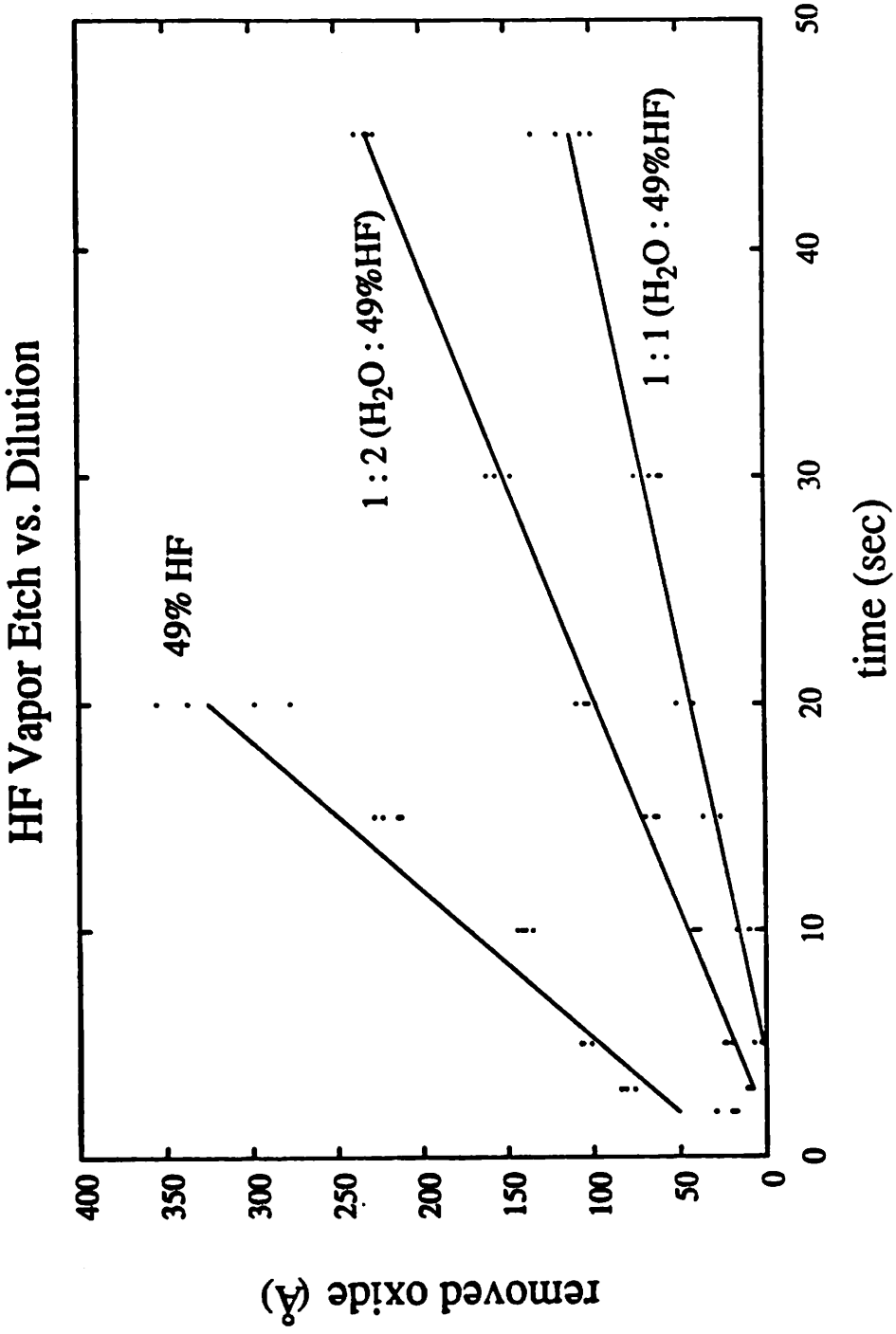


Fig. 3. Effects of the amount of oxide removed on the time required to completely evaporate water moisture from substrate surface after each HF vapor exposure.

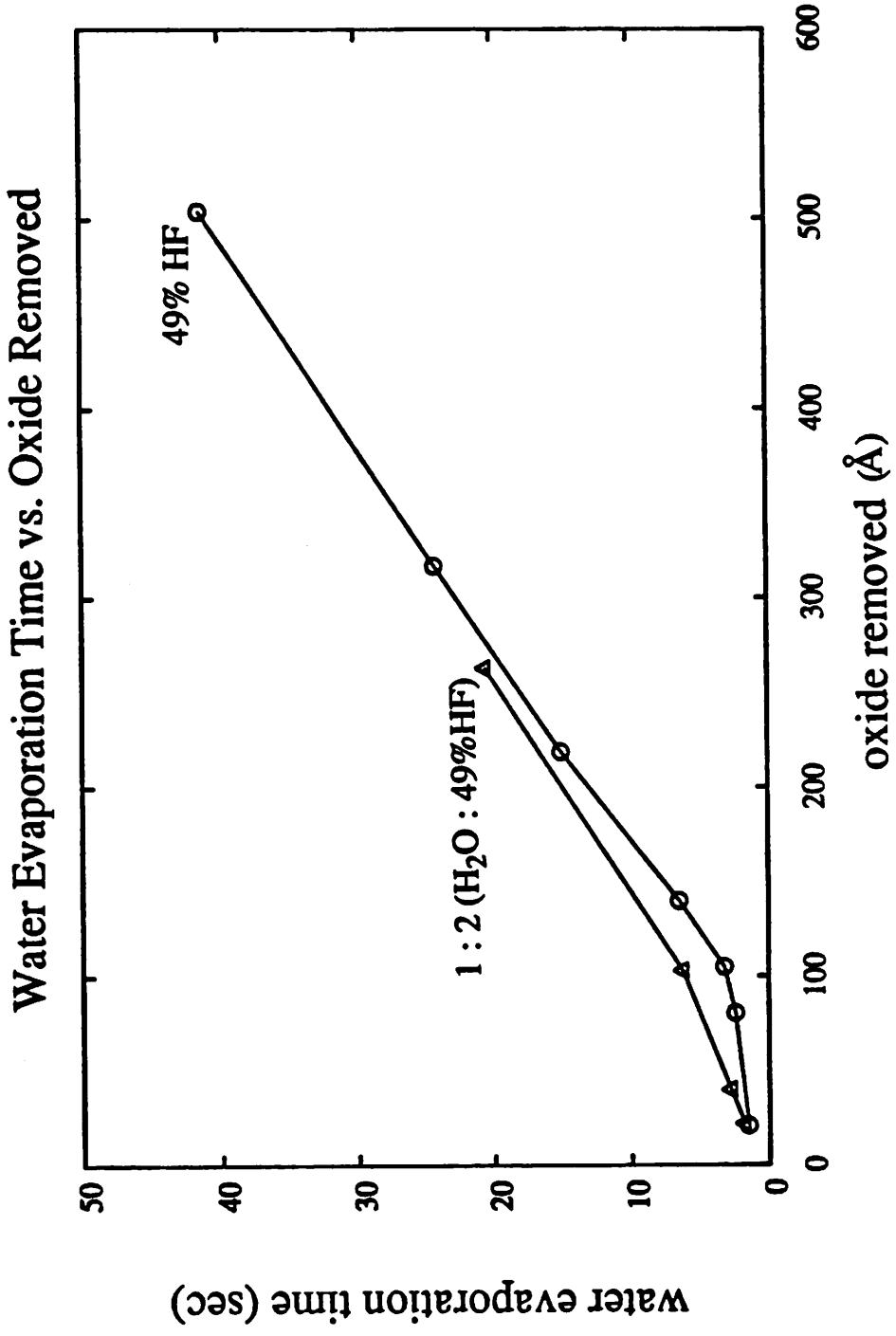


Fig. 4. After a 5 second exposure over a 1:2 mixture of H_2O:49% HF, the Nomarski micrograph shows no HF vapor-etch-induced residuals on Si areas or oxide areas.

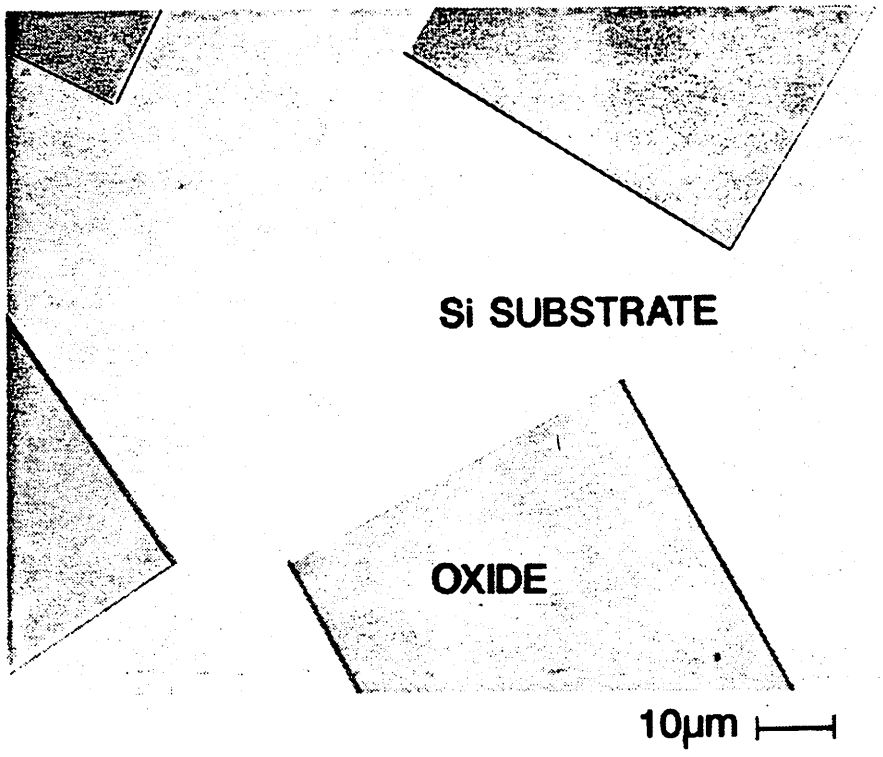


Fig. 5(a). After a 45 second exposure over a 1:2 mixture of H_2O:49% HF, Nomarski micrographs show that most of the oxide surface is covered by water just after the HF vapor treatment. Also, there exist many small water droplets on Si surface.

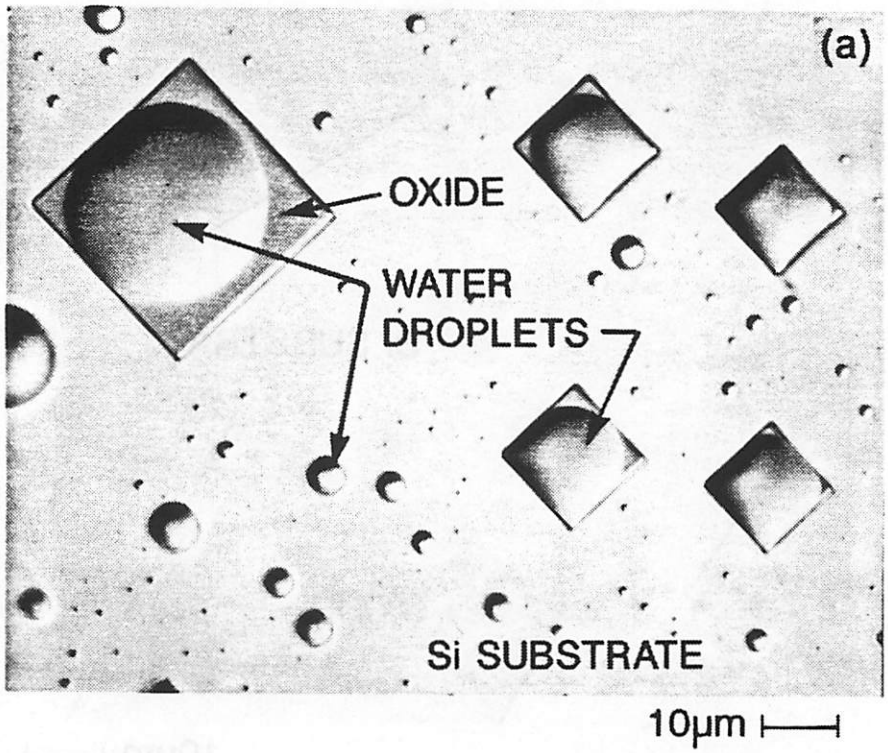
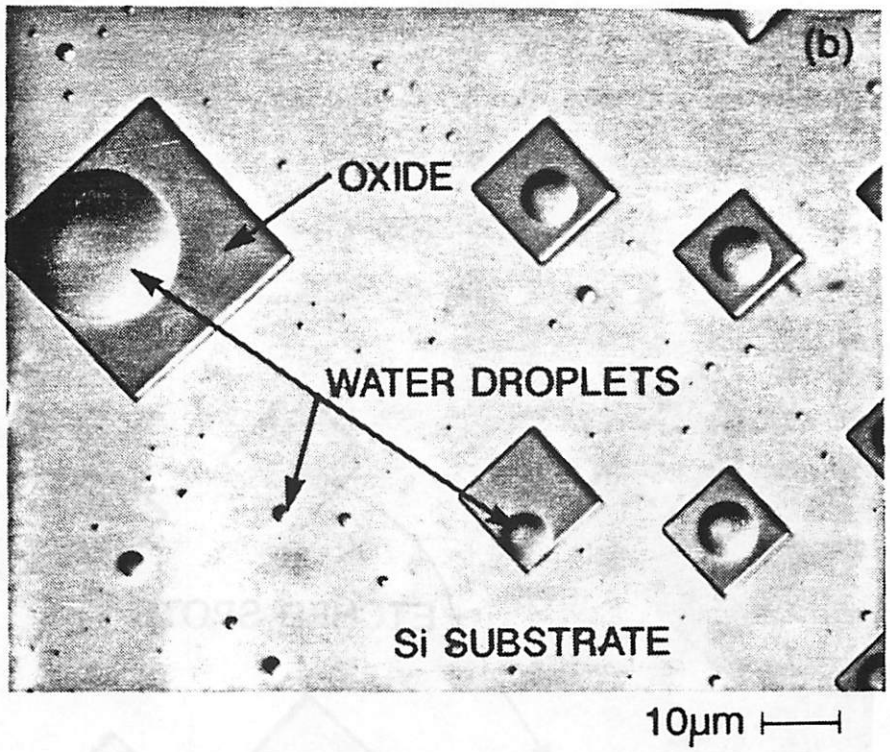


Fig. 5(b) and Fig. (c). The evaporation of water results in the shrinkage of water droplets on oxide areas and Si areas.



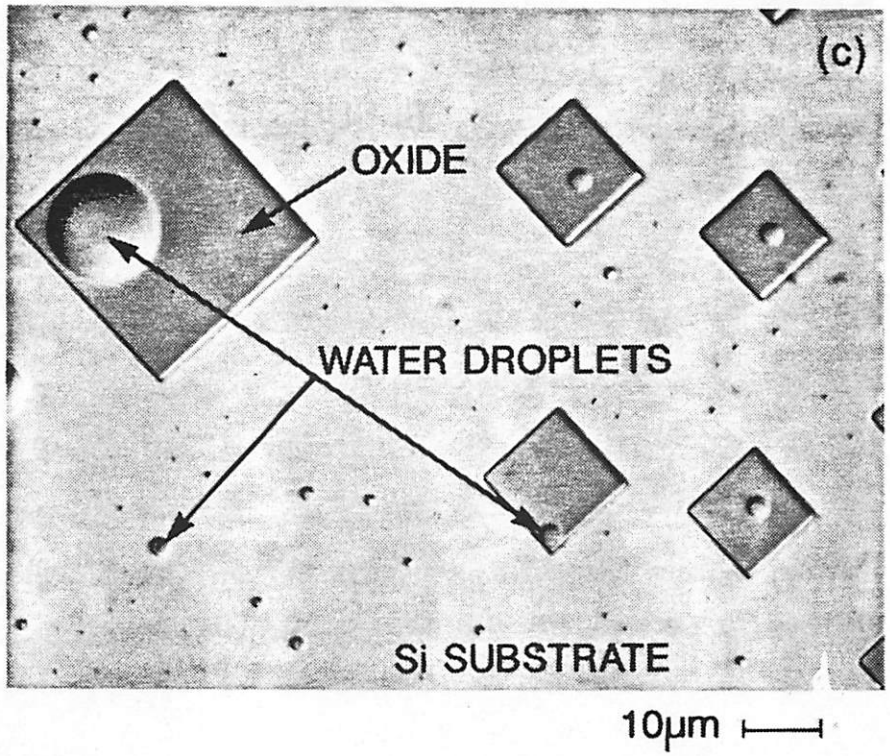


Fig. 5(d). Water droplets proceed local overetch and result in many concave textured spots on the oxide surface and the Si area.

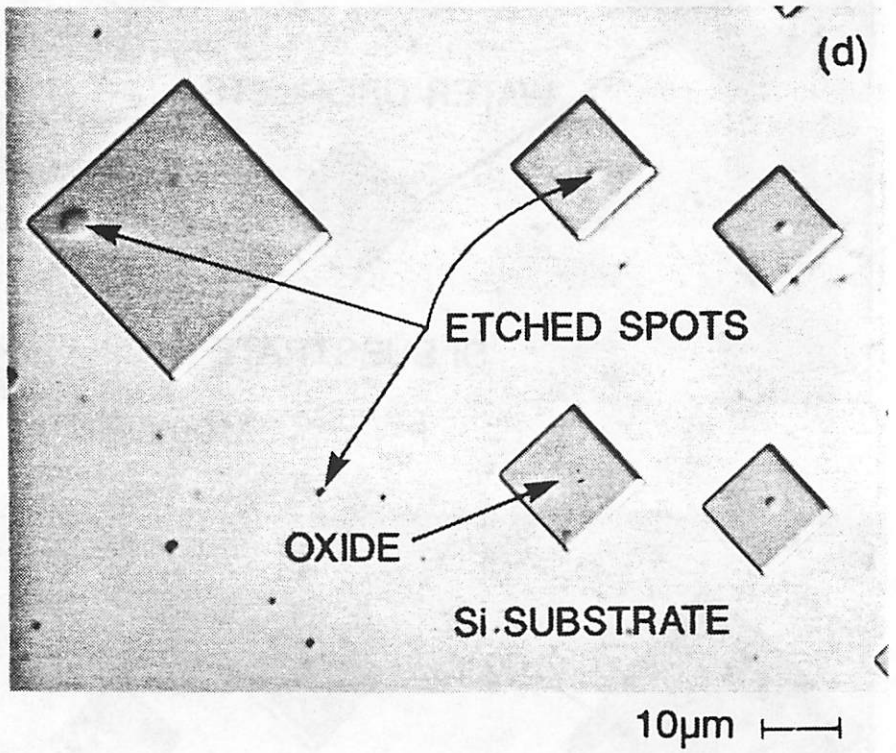


Fig. 6. Preheat effects on patterned Si substrates show an induction period to start the oxide etching reaction.

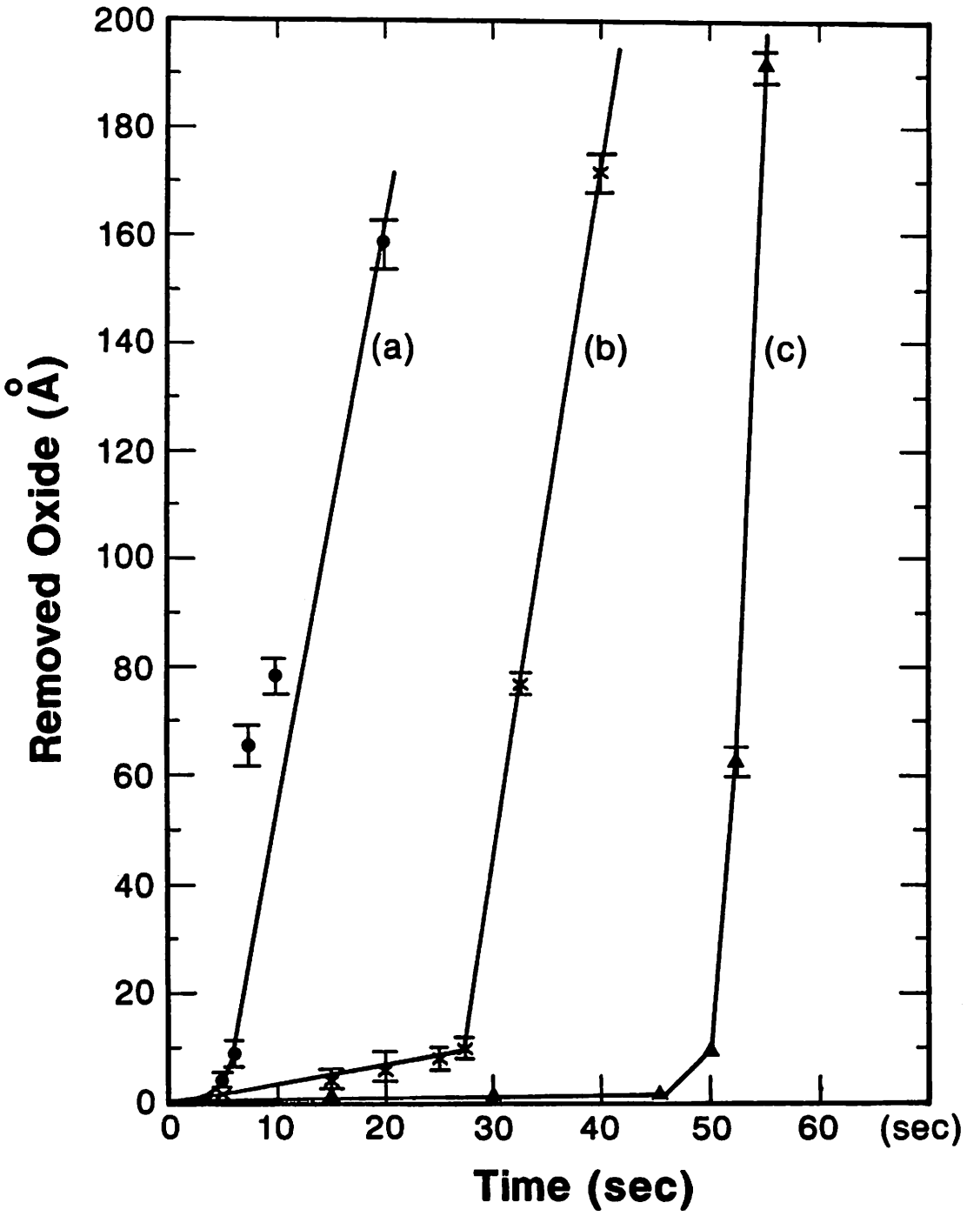


Fig. 7. The deposition cycle for the selective epitaxial growth at 850°C. A low-concentration of DCS is applied in the prebake and the ramp-down steps.

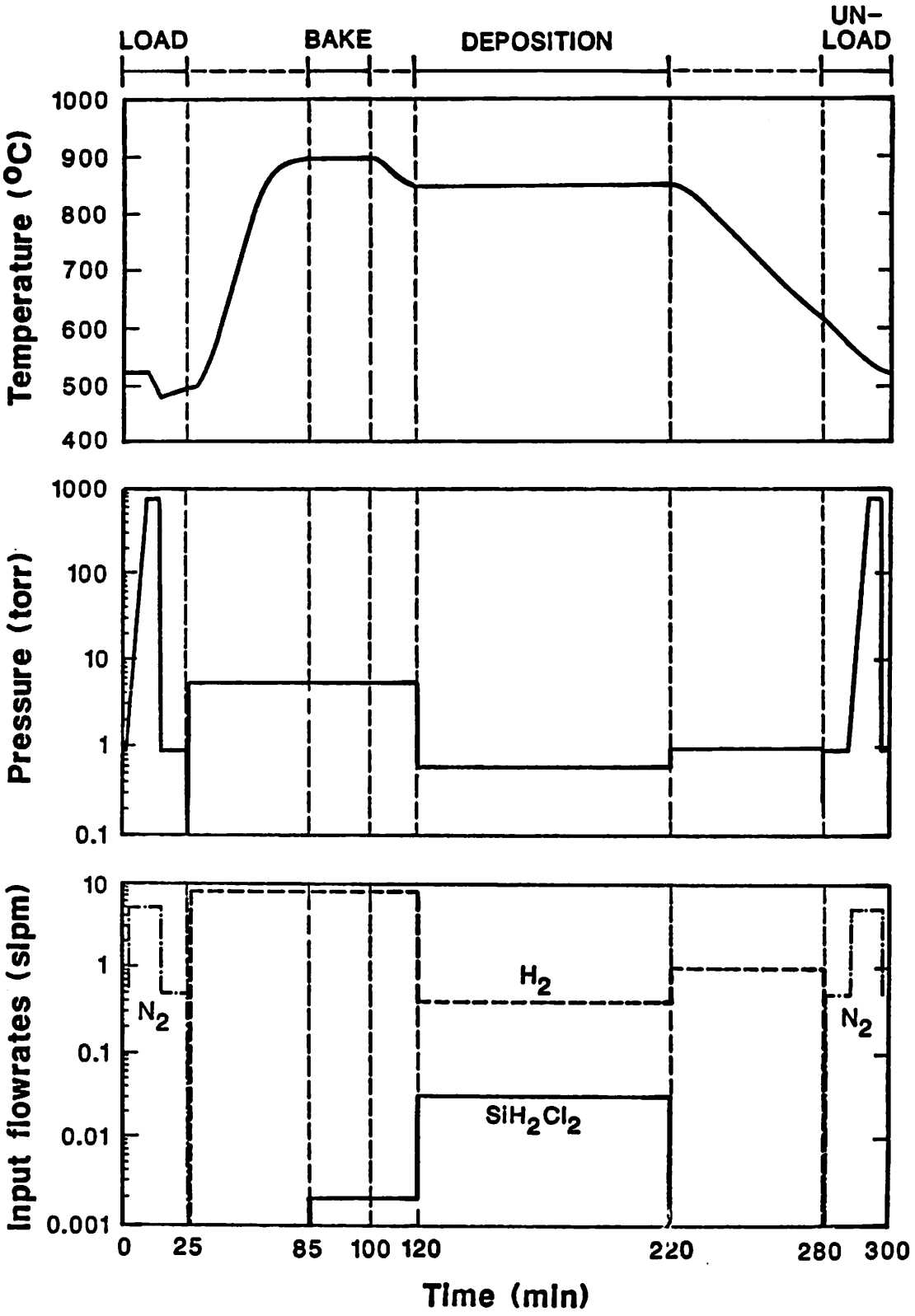


Fig. 8. With a standard HF vapor treatment, the Nomarski micrograph (1000X) shows a specular epilayer with smooth edges. There is no poly-Si nuclei on oxide surface.

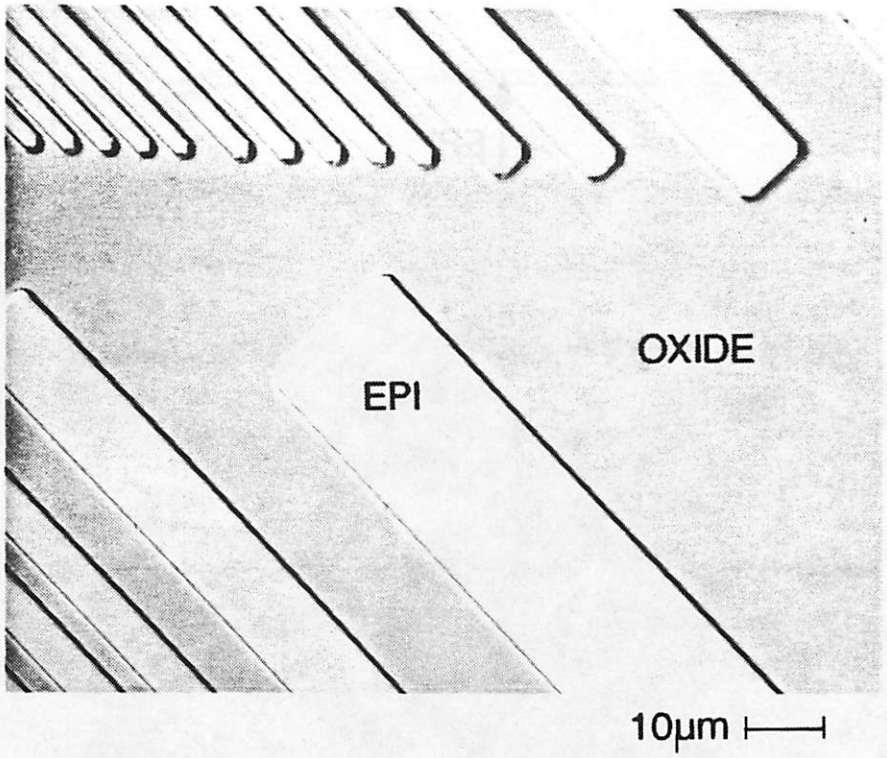


Fig. 9. The XTEM micrograph of the same specimen in Fig. 8 shows no defects in the epilayer or at the epi/substrate interface. Also, it shows no undercut along the oxide/substrate interface.

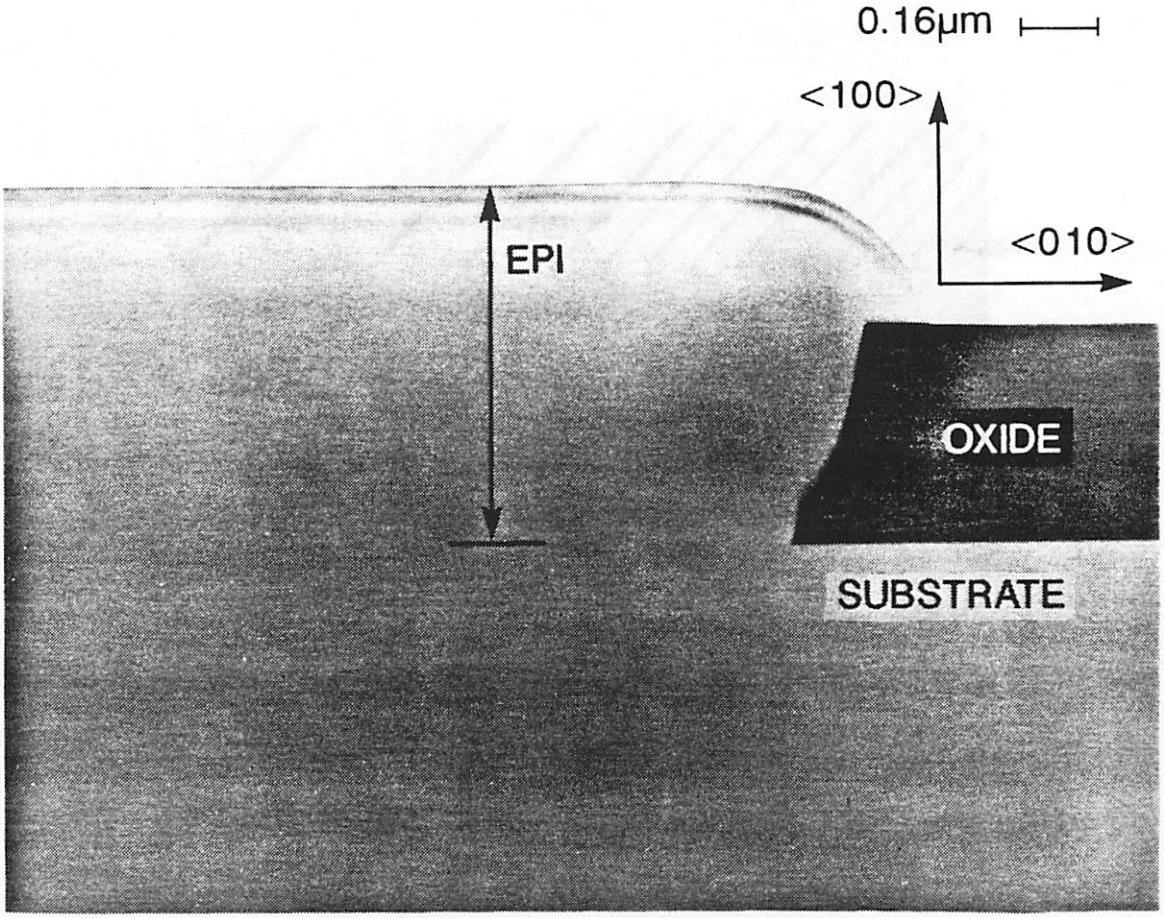


Fig. 10. After the dilute Schimmel etch, the Nomarski micrograph (1000X) shows no etched pits at the epi/substrate interface for the specimen in "Fig. 8."

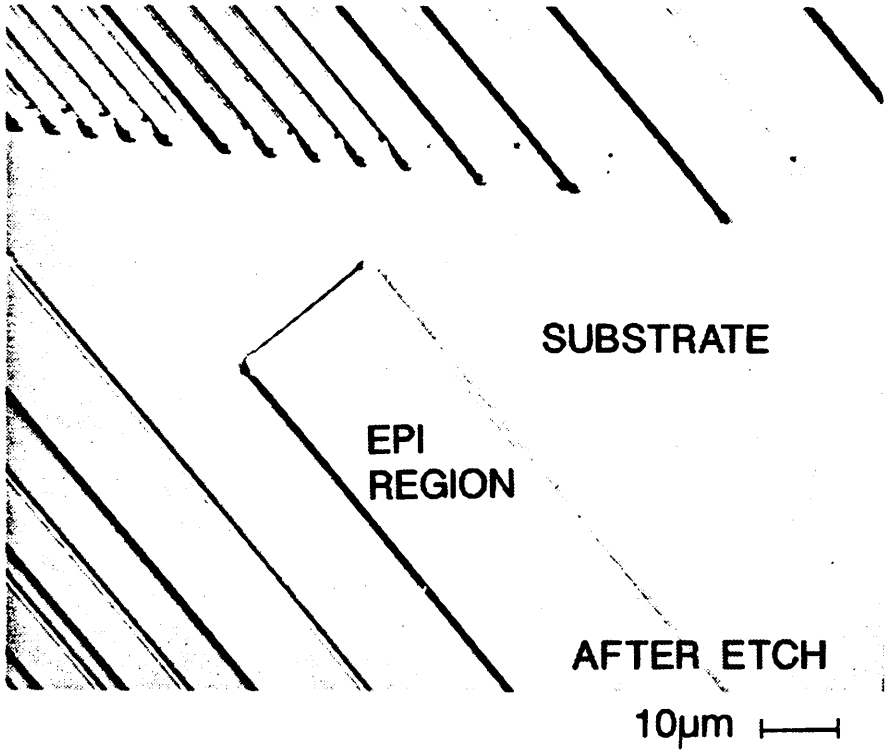


Fig. 11. SIMS results of the same specimen in Fig. 8 indicates no oxygen, carbon, or fluorine peak at the epi/substrate interface.

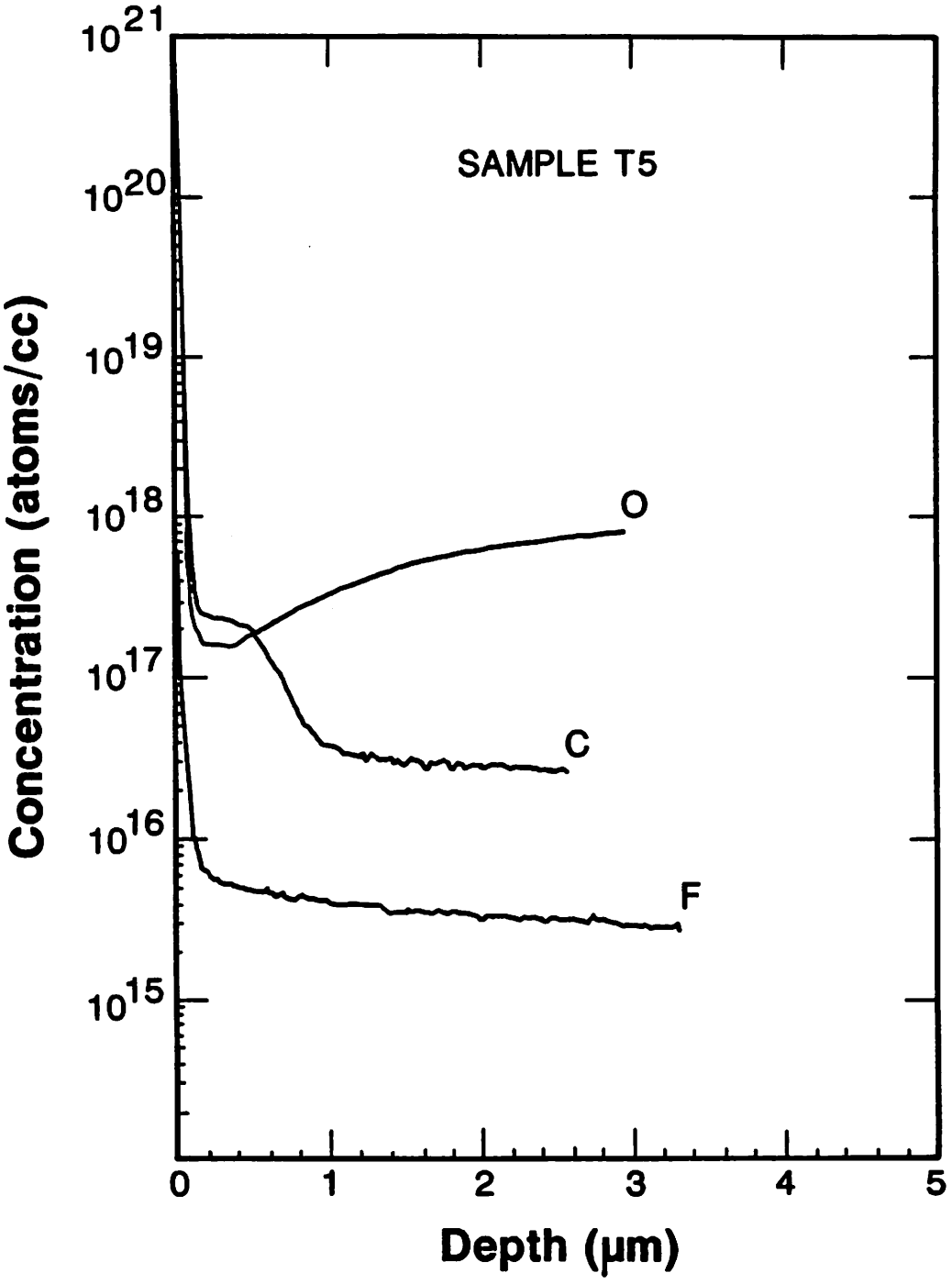


Fig. 12(a). With a 45 second exposure over the 1:1 mixture of H_2O:49% HF before the wafer loading into the reactor, the Nomarski micrograph (1000X) shows pits in epilayers, poly-Si nuclei on oxide surface, and rough edges of epilayers.

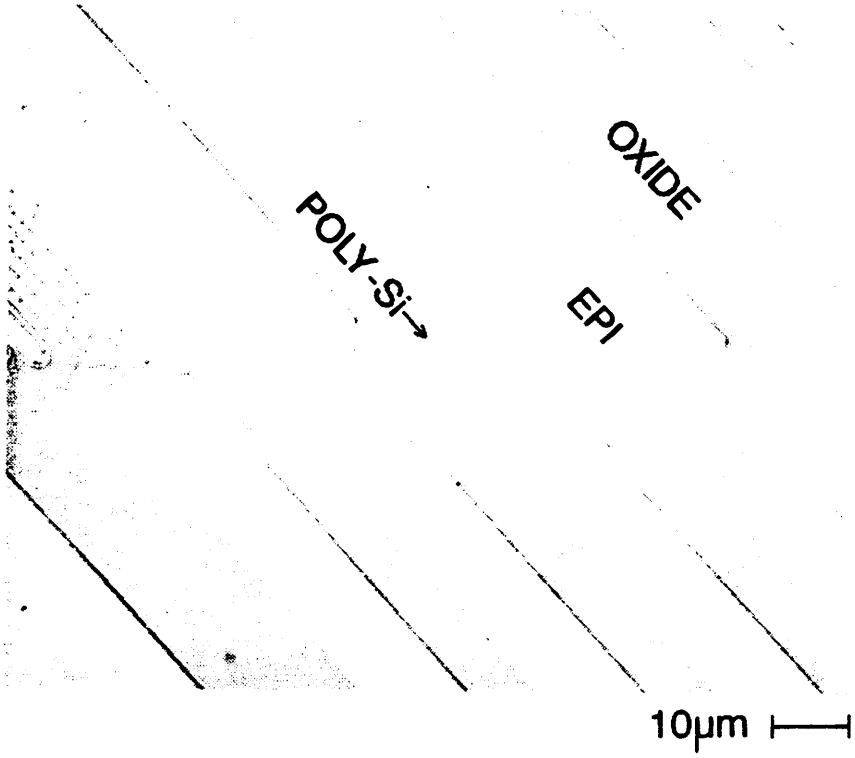


Fig. 12(b). With a 45 second exposure over the 1:2 mixture of H_2O:49% HF before the wafer loading, the Nomarski micrograph (1000X) shows rough edges of epilayers and poly-Si nuclei on oxide surface.

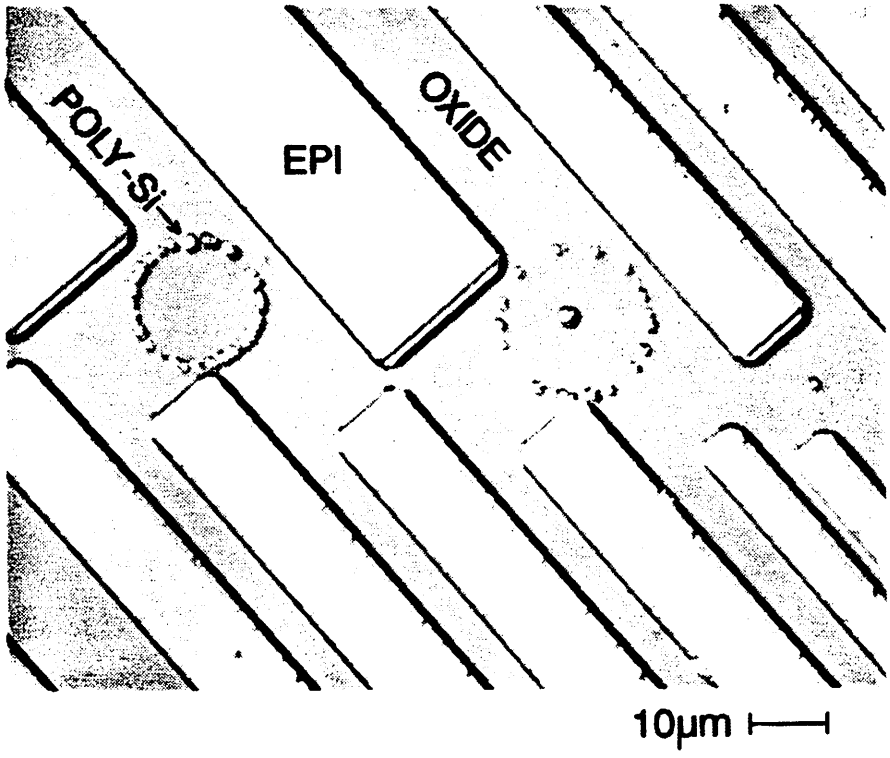


Fig. 12(c). With a 16 second exposure over the 49% HF before the wafer loading, the Nomarski micrograph (1000X) shows epilayers with rough edges, and poly-Si nuclei on oxide areas.

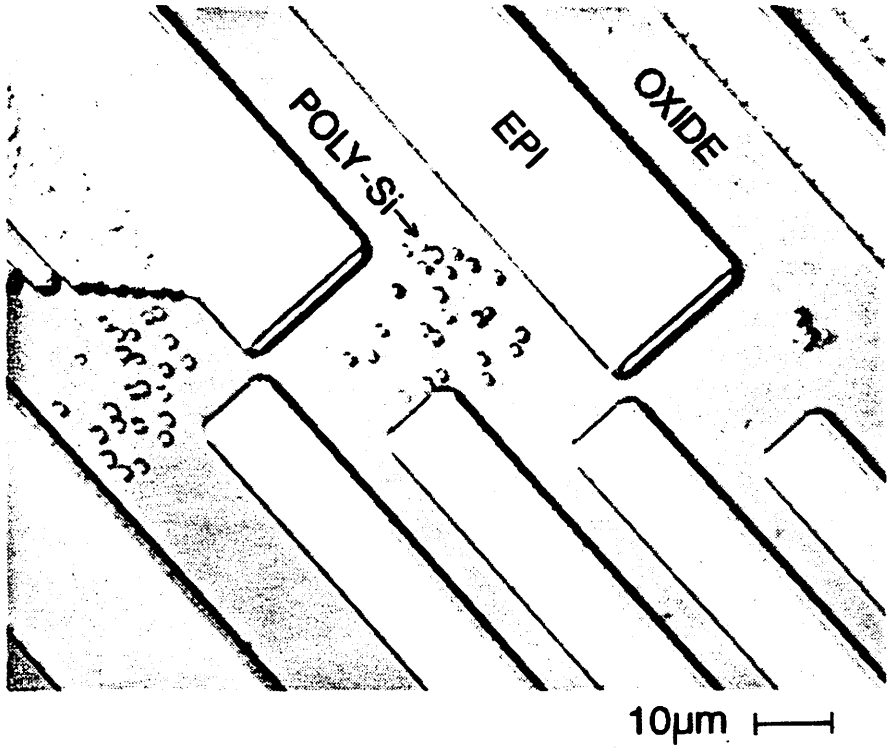


Fig. 13. The Nomarski micrograph (1000X) indicates the growth of poly-Si in the center of a round-shaped trace due to the overetch of a water droplet on oxide surface.

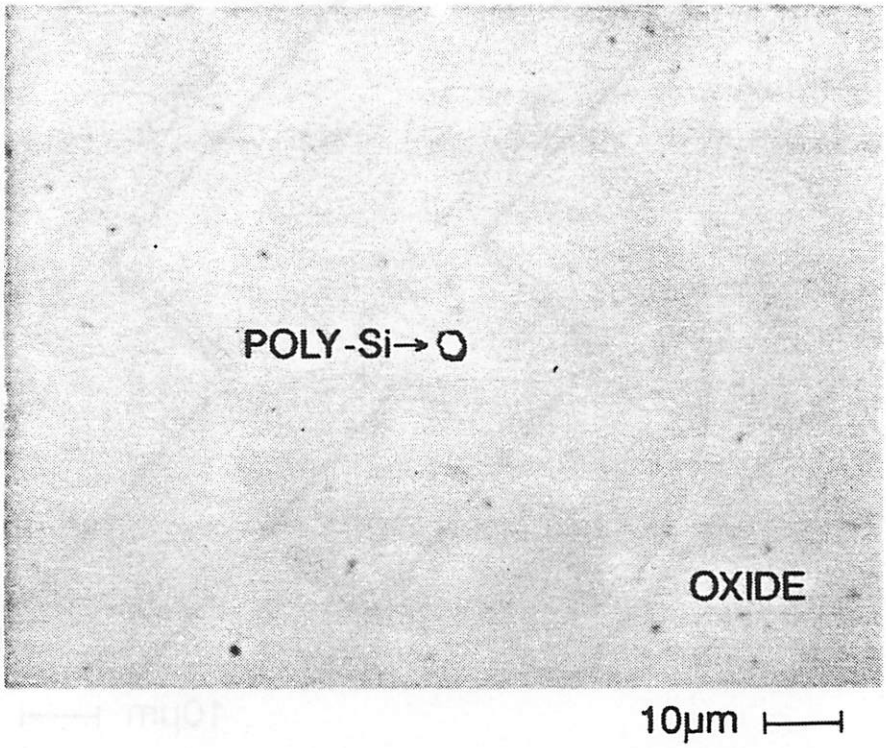


Fig. 14 With an 18 hour air exposure after a standard HF vapor treatment, the Nomarski micrograph (1000X) still shows a specular epilayer with smooth edges. No poly-Si is observed on oxide surface.

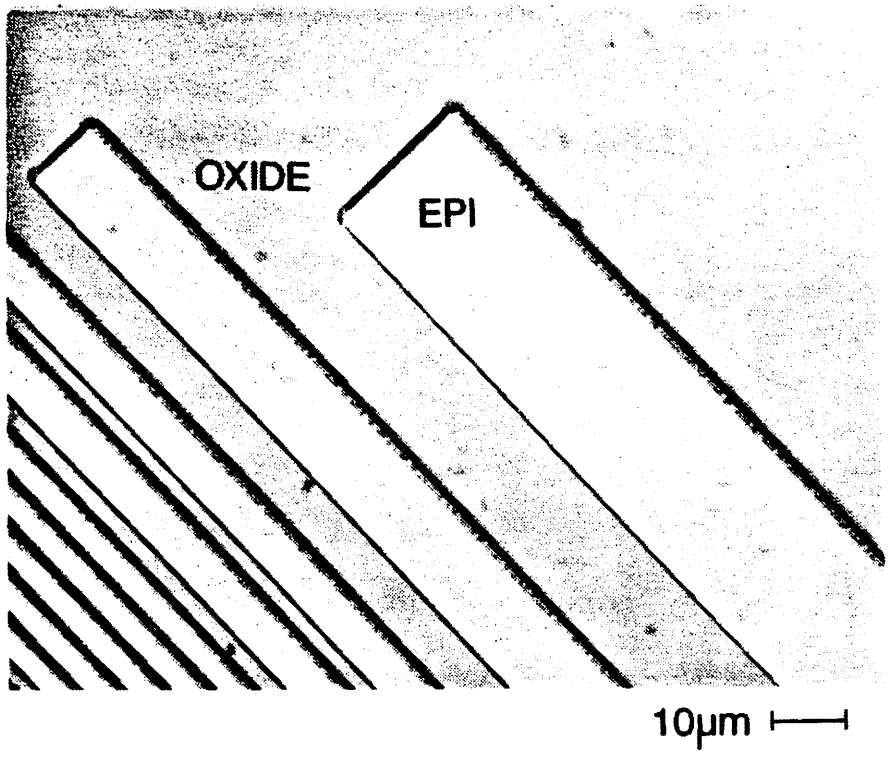


Fig. 15(a). With a 61 hour air exposure after a standard HF vapor treatment, it shows many fine pits on the surface but no poly-Si nuclei on oxide areas.

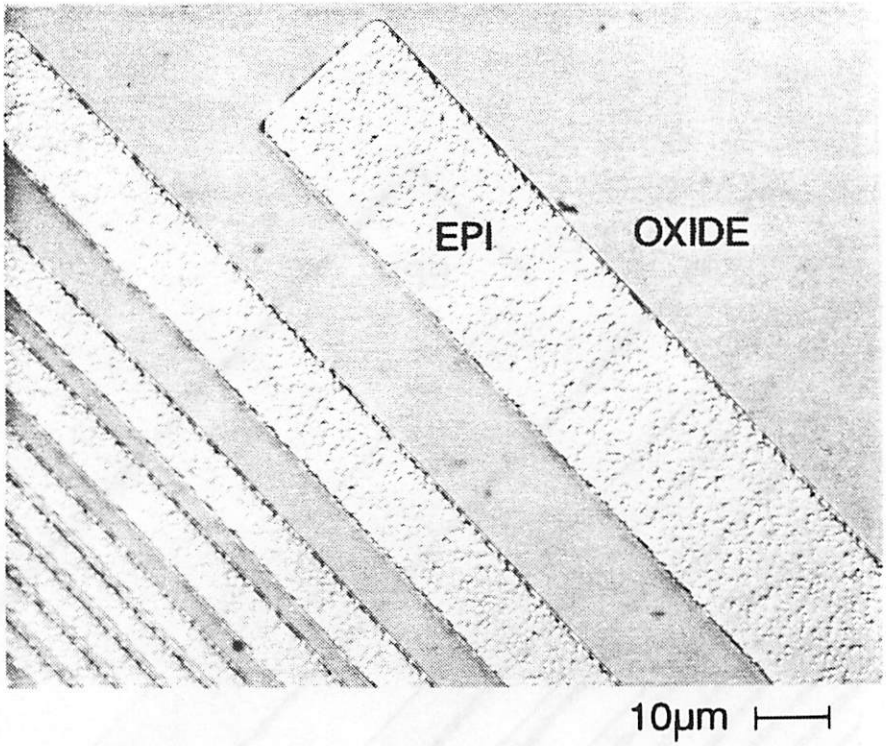


Fig. 15(b). With a 73 hour air exposure after a standard HF vapor treatment, a textured epilayer is obtained. However, there is no poly-Si nuclei on oxide areas.

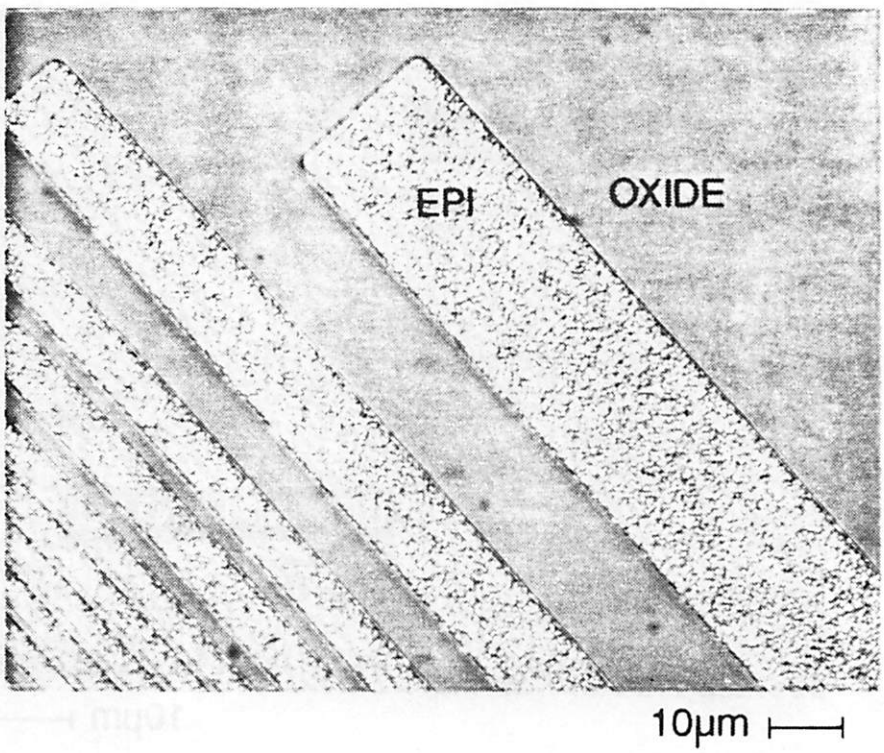


Fig. 16. With an ex-situ low-flux 40 Kev $10^{13}/cm^2$ BF_2^+ ion implantation, Nomarski micrographs show textured epilayers on the whole wafer.

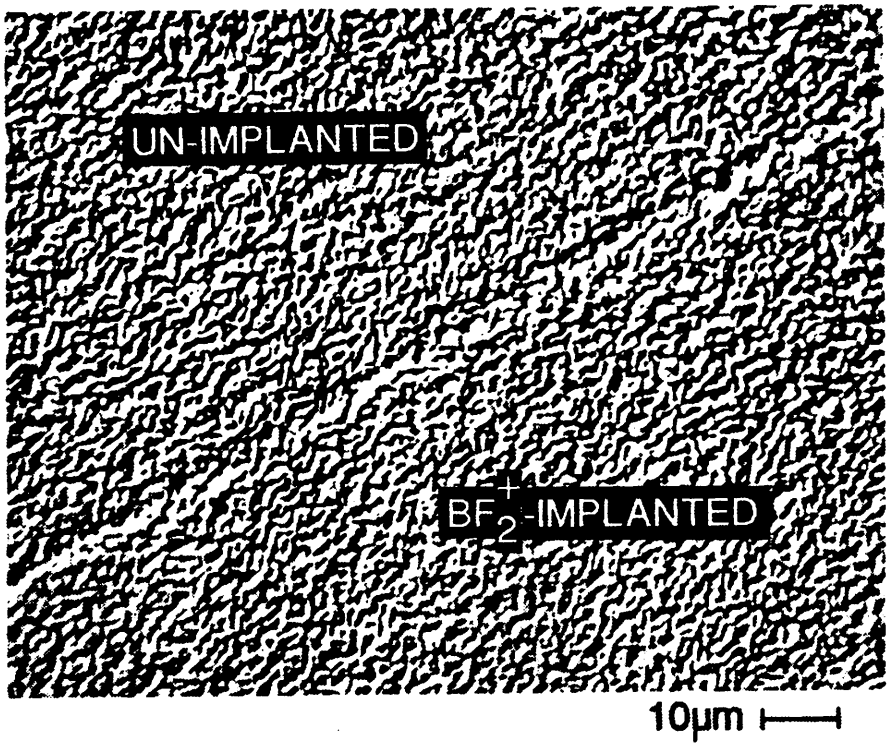


Fig. 17(a). With an ex-situ BF_2^+ ion implantation (40 Kev, $10^{14}/cm^2$), the epi-layer is grown at 850°C after a 900°C prebake. The Nomarski micrograph (1000X) shows a specular epilayers on BF_2^+ implanted regions but textured epilayers on un-implanted regions.

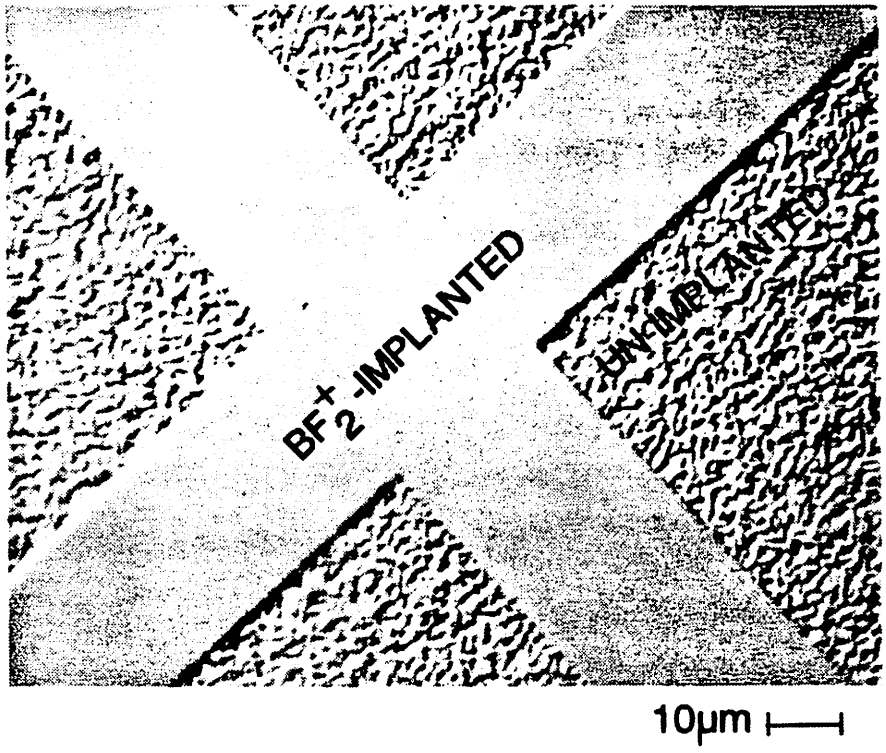


Fig. 17(b). The XTEM micrograph of the same specimen in Fig. 17(a) illustrates a defect-free epilayer on the BF_2^+ implanted region but a defective epilayer on the un-implanted region.

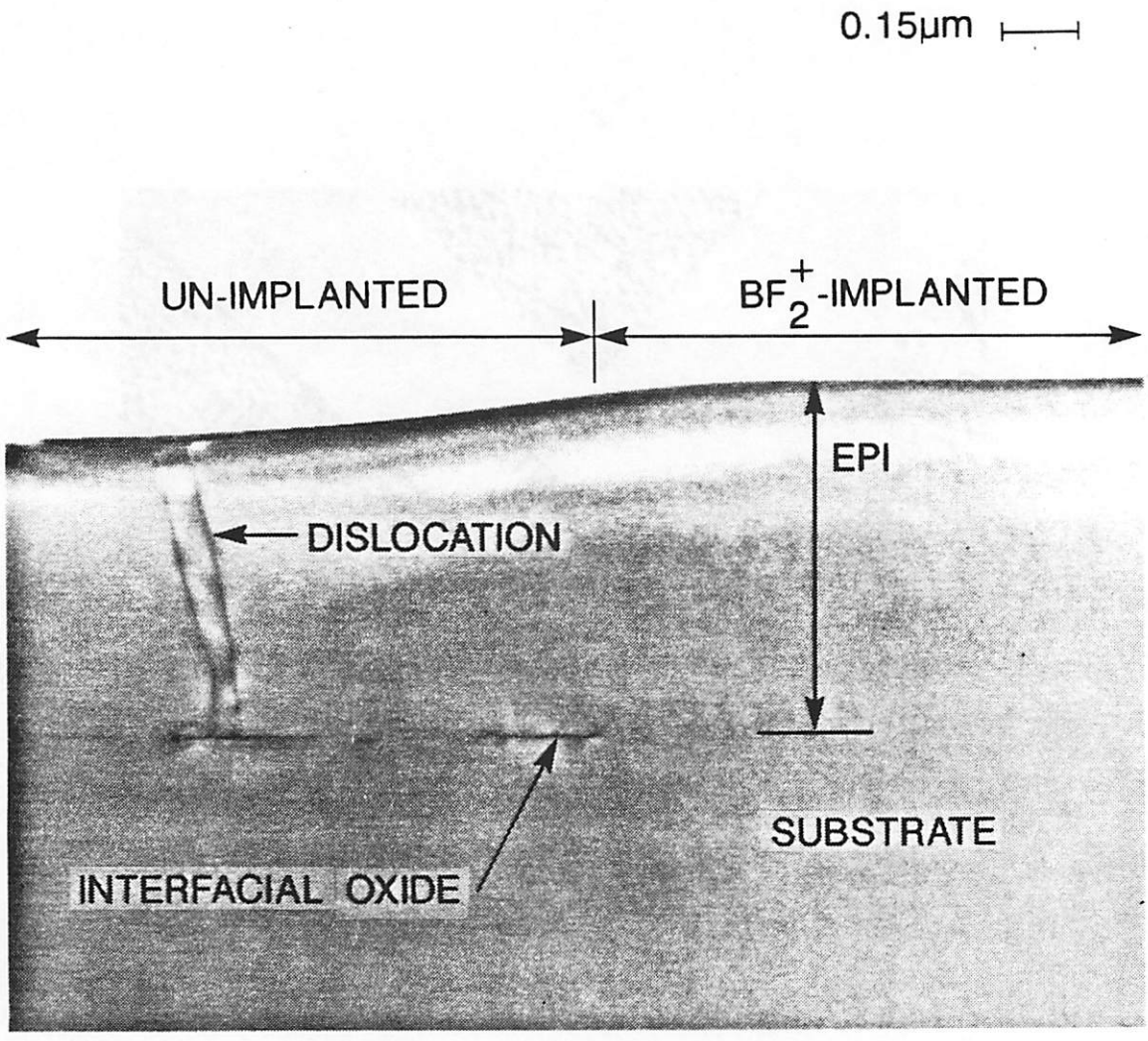


Fig. 18(a). SIMS analysis shows no oxygen, carbon, or fluorine peak in the epilayer grown on the BF_2^+ implanted region.

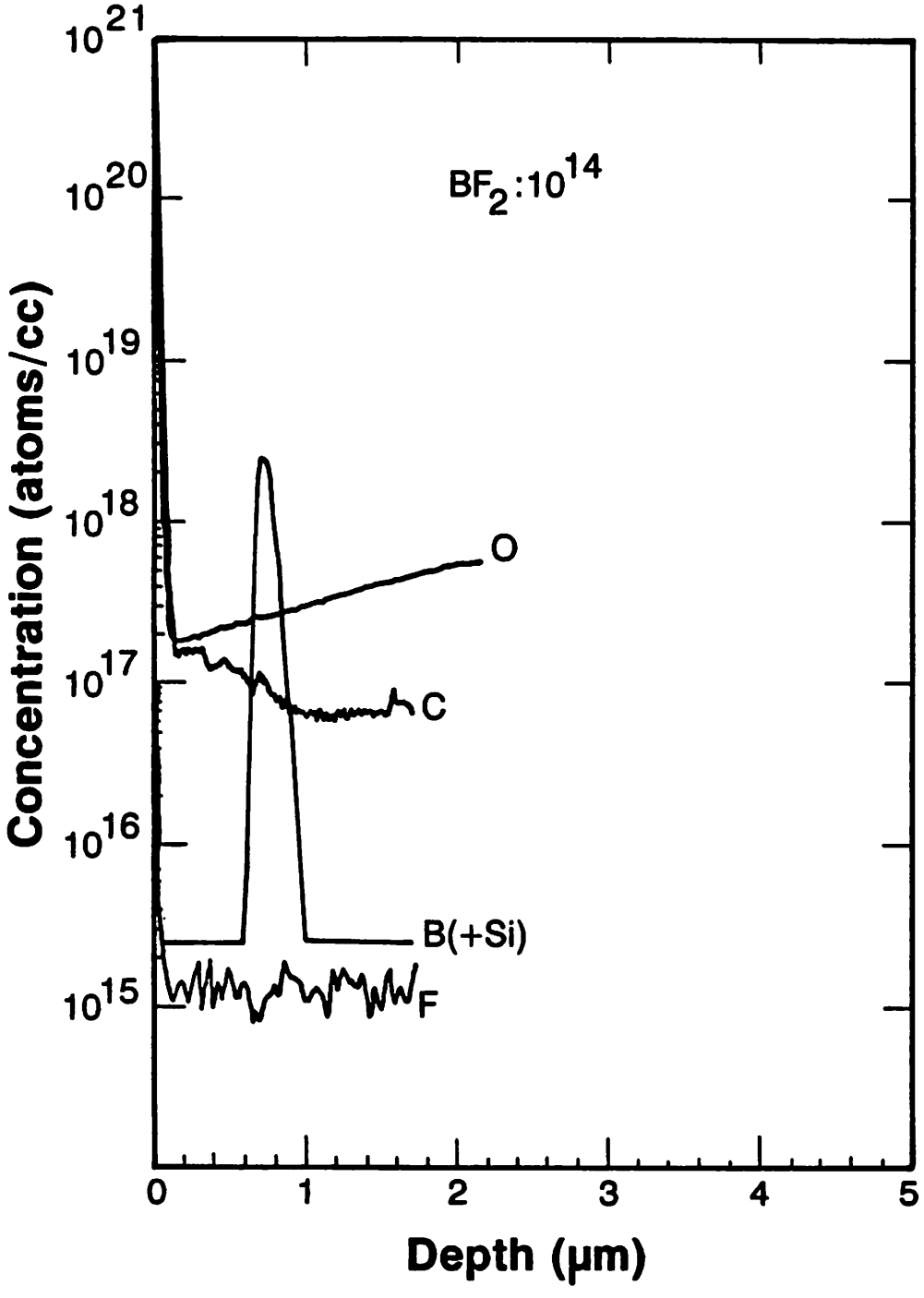


Fig. 18(b). SIMS analysis indicates significant oxygen peak, carbon peak, and fluorine peak in the epilayer deposited on the un-implanted region.

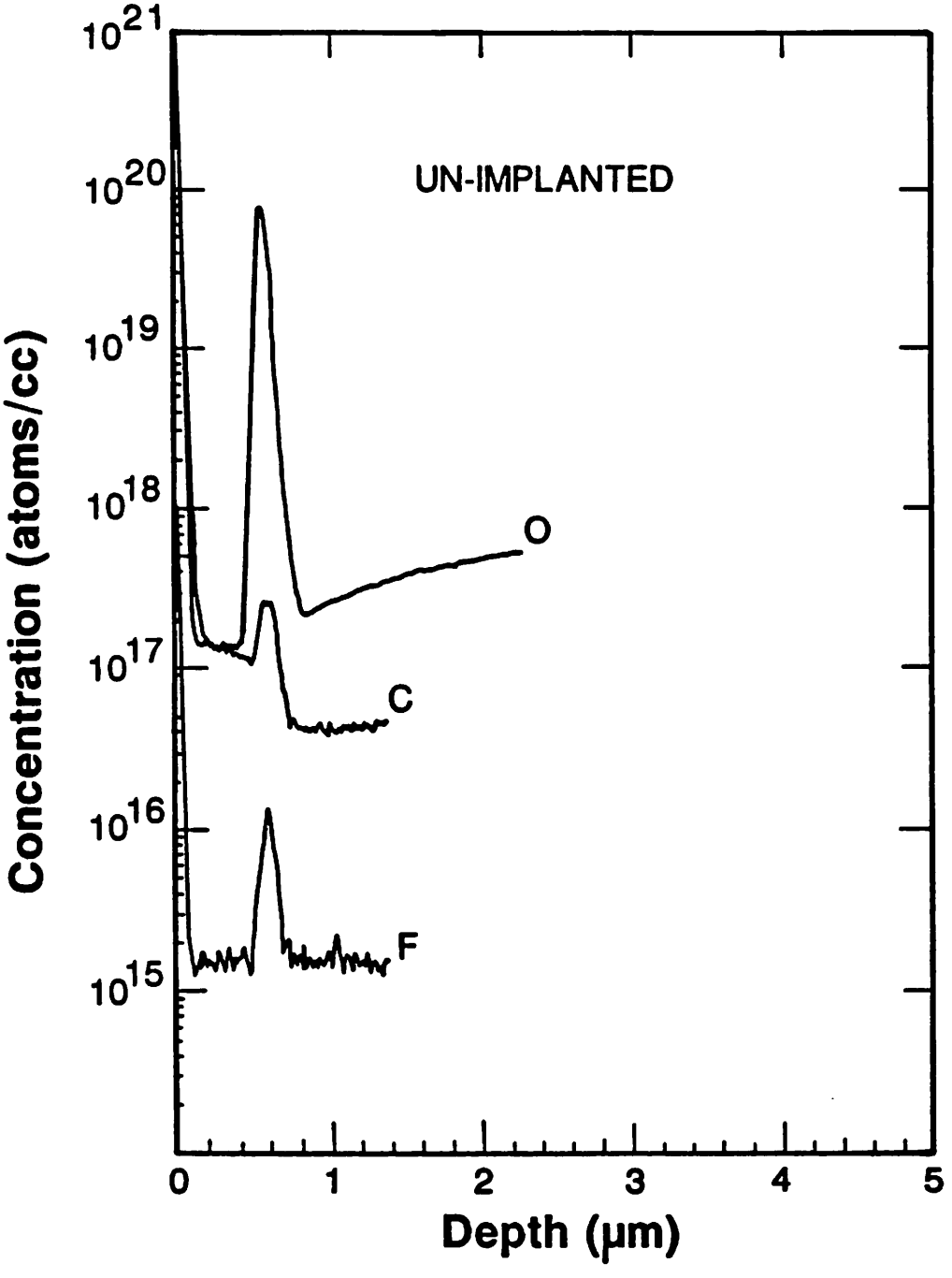


Fig. 19. With the ex-situ low-flux 20 Kev F^+ ion implantation, Nomarski micrographs show textured surface morphology on the whole wafer. (a) $10^{13}/cm^2$. (b) $10^{14}/cm^2$.

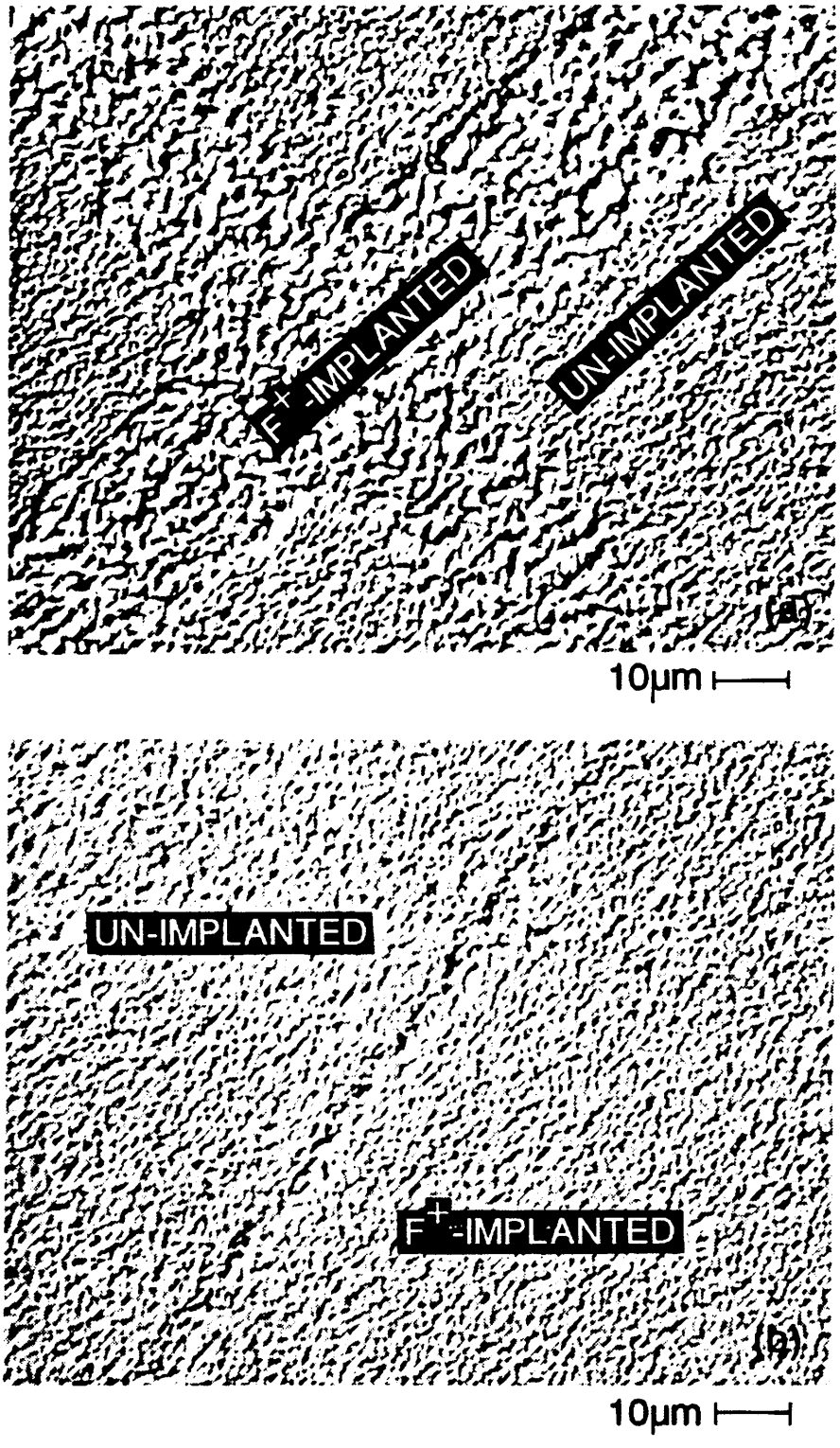


Fig. 20(a). With an ex-situ F^+ ion implantation (20 Kev, $10^{15}/cm^2$) and the deposition cycle shown in Fig. 7, the Nomarski micrograph (1000X) shows specular epilayer on the F^+ implanted region but textured epilayer on the un-implanted regions.

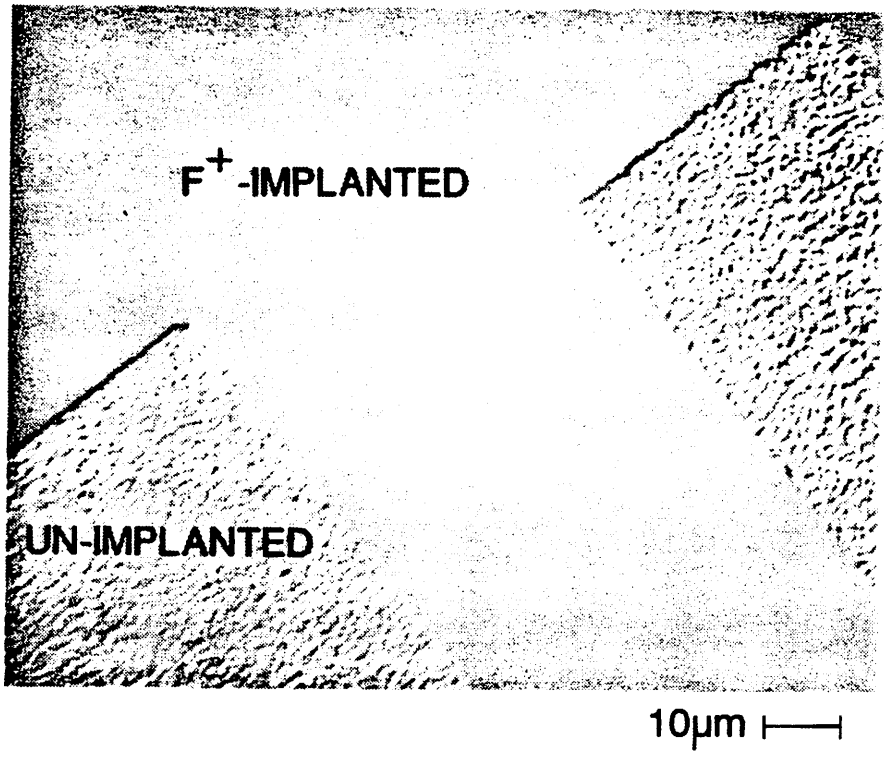


Fig 20(b). The XTEM micrograph of the same specimen in Fig. 20(a). It shows a defect-free epilayer on the F^+ implanted region but a defective epilayer on the un-implanted region.

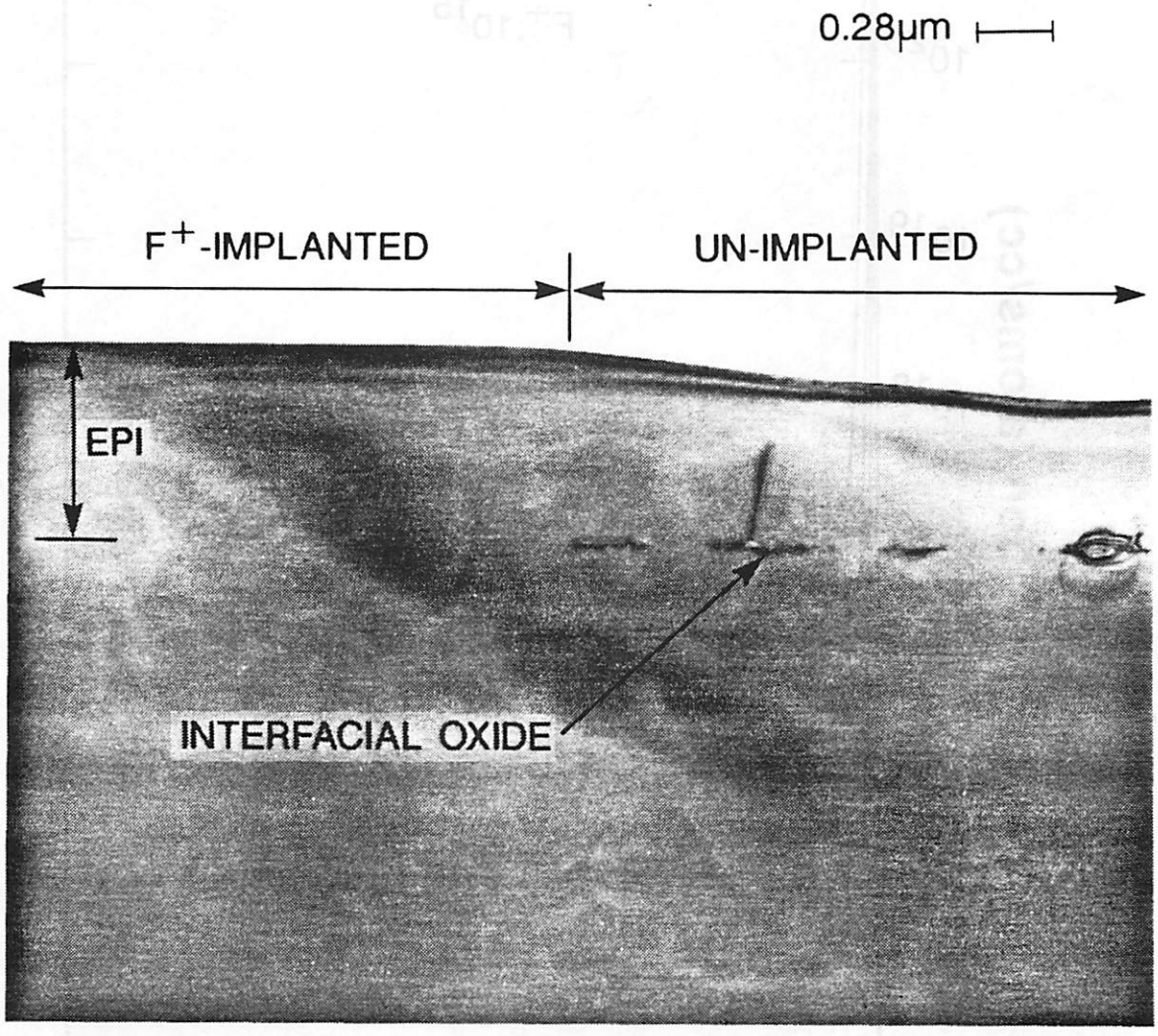
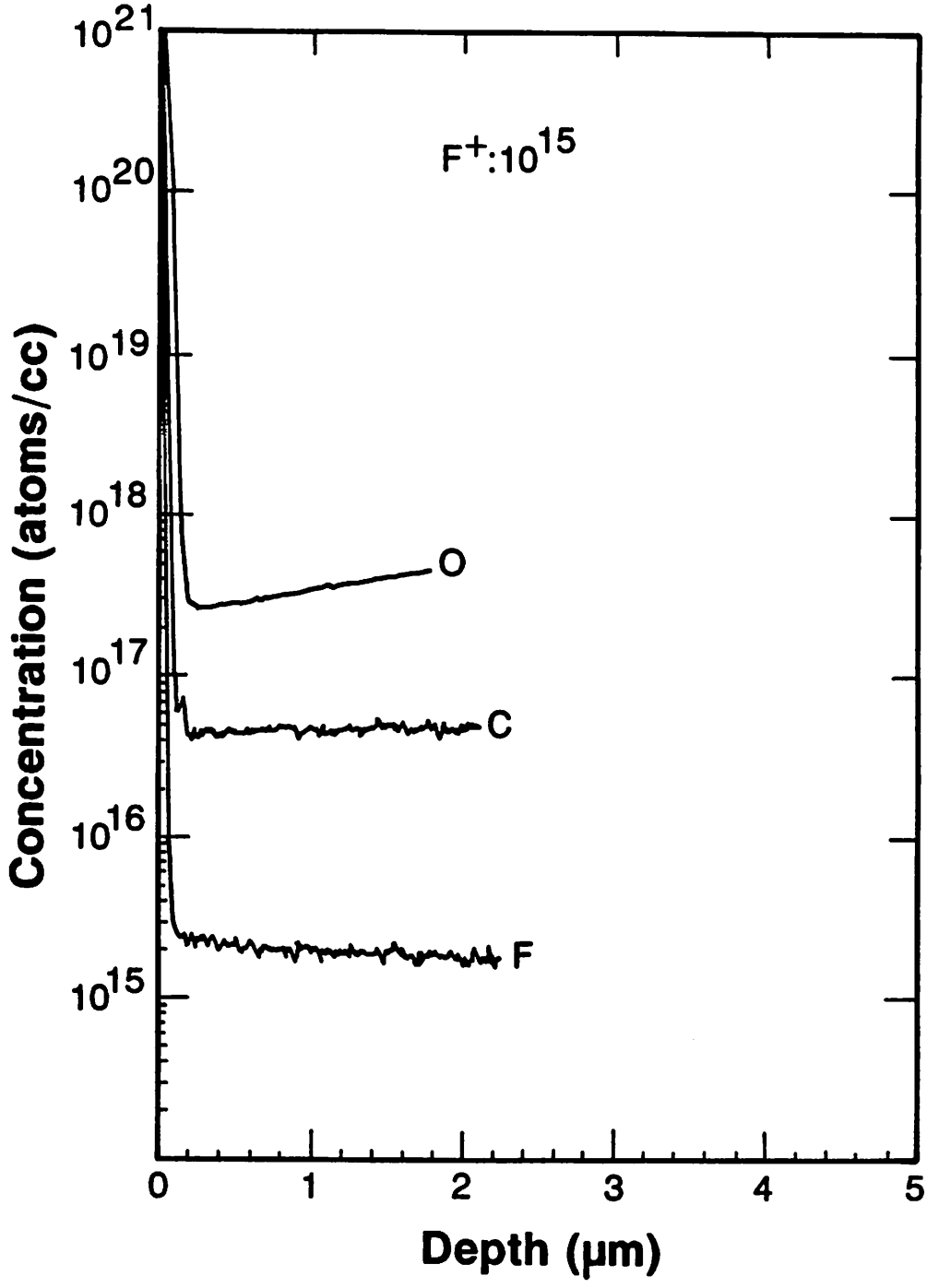


Fig. 21. SIMS analysis indicates no oxygen, carbon, or fluorine peak at the epi/substrate interface for the F^+ implanted regions.



Chapter 4

Plasma Etch Effects on Low-Temperature Selective Epitaxial Growth of Silicon

In this chapter, the quality of epitaxial silicon grown on regions exposed to plasma etching using He, CHF_3 and CF_4 etching gases has been studied. We find that plasma-etch-induced surface damage leads to defects in the epilayers. Dislocation loops and precipitates at the epi/substrate interface are always observed. High temperature prebake can further lead to microtwins and threading dislocations. We propose that the formation of defects in epilayers is mainly attributed to the ion-bombardment-induced surface/subsurface defects and the reactive-ion-induced contaminants on exposed Si areas. A 900°C grown sacrificial oxide film can efficiently remove both near-surface defects and contaminants to get a clean SiO_2/Si interface, and result in high quality Si epilayers. A 5 nm sacrificial oxide is adequate. We further find that an air exposure in between several plasma etch cycles is also important in suppressing polymer accumulation on substrates. Development of this modified plasma-etch technique and a thin sacrificial oxide layer shows promise of enabling the growth of high quality Si epilayers.

4.1 The Motivation to Study the Plasma Etch

Low-temperature selective epitaxial growth (SEG) of silicon can be key for fabrication of future devices for submicron ULSI applications [1-4]. The quality of epilayers is significantly affected by the wafer preparation and the deposition cycle. "Improper" process steps can result in a variety of problems including undercuts, voids, microtwins, dislocation loops, threading dislocations, and interfacial oxide islands. Our previous studies [5-7] have shown that both an ex-situ wafer-clean pro-

cess and an in-situ prebake step with dichlorosilane (DCS) improve the quality of epilayers. This study is concerned with the etching step defining epitaxial windows which can also degrade the epitaxial quality unless a post-etch process is used to eliminate defect precursors.

For the purpose of opening oxide windows, wet chemical etches have high selectivity to the Si substrate. However, wet etches, being isotropic, lead to sloped sidewall profiles and are limited to large feature sizes. The near cylindrical profiles present almost all possible interfacial planes between vertical and (100). Certain planes, such as (111) lead to microtwins; consequently, it is difficult to grow defect-free layers through wet-etched windows. Fig. 1 shows cross-sectional TEM (XTEM) micrographs of epilayers grown through wet-etched windows. As shown in Fig. 1(a), sidewall directions of patterns defined along <110> directions, reveal {111} planes on SiO_2 sidewalls and produce microtwins near the oxide sidewalls. For sidewall directions of patterns along <100>, {110} planes are revealed on the sidewalls after the wet etch. Again, as shown in Fig. 1(b), microtwins appear.

Plasma etching processes are now universally employed for highly directional etching techniques in ULSI circuit fabrication [8-10]. However, it is found [11-12] that the plasma etch step can result in surface damage on Si substrates. In critical situations such as gate oxide growth it is common to grow and remove a 20-40 nm sacrificial oxide layer, which, for reasons which are not completely clear, mitigates the surface damage. In the case of epitaxial growth an important question, for example, is whether the ion bombardment induces sub-surface defects (e.g. point-defect complexes) or whether the reactive-ion-induced impurity contamination (e.g. complexes of carbon, fluorine and hydrogen) play the main role in nucleating defects in epilayers. Lehmann et al [13] used Ar + CF_4 + CHF_3 to get a large etch selectivity of SiO_2 over Si. Oehrlein et al [14-15] employing CF_4 + H_2 also obtained a good oxide-to-silicon etch selectivity. They further indicated that the

plasma etch (CF_4 + H_2) results in a fluorocarbon film on Si substrates, an amorphous-like damaged Si layer (3-5 nm thick) near the Si surface, and a region of ion-bombardment induced point defects to a depth of several tens of nanometers. We find that epitaxial growth on such plasma-etched substrates is highly defective, presumably because of the contamination or damage noted above. However, a thermally grown sacrificial oxide can eliminate the detrimental effects of plasma etching. In this paper we present the results of a transmission electron microscopy (TEM) study of the plasma-etch induced degradation of epitaxial growth, and its dependence on prebake and growth temperature.

4.2 Wafer Preparation and Experimental Procedure

Boron doped (100) Si wafers of resistivity 30-50 ohm-cm were used as substrates for the selective epitaxial growth. A 570 nm thermal oxide layer was grown at 1000°C. A photolithographic step was used to define the bare and oxide-covered regions. Pattern features were aligned along <100> directions or <110> directions. The oxide was plasma etched in a LAM 590 AutoEtch system using He + CHF_3 + CF_4, with the full recipe given in Table 1. To achieve vertical sidewalls the power level is 900 watts, resulting in a etch rate of approximately 300 nm/min. It is found that a continuous etching step results in very tenacious damage which can survive even a 25 nm sacrificial oxidation. However, a sequence of short etches consisting of four 2 sec cycles followed by four 30 sec cycles can achieve excellent anisotropy, but with more manageable surface damage. Wafers were exposed to the air after each plasma etch cycle. The process is continued to reach to a depth of 40 nm below the Si/SiO_2 interface. After plasma etching and photoresist removal, sacrificial oxide films with different thickness (0, 5, 10, 15, 20, and 25 nm, respectively) were grown at 900°C. The wafers were then subject to a pre-epitaxial clean consisting of two piranha cleaning treatments separated by a

dilute HF dip that removes the sacrificial oxide. Afterwards, the wafers were exposed to HF vapor over a 1:2 mixture of H_2O:49% HF for 5 seconds to remove the chemical oxide and passivate the wafer surface[5], then immediately loaded into a horizontal hot-wall reactor at 525°C. The deposition cycle for different growth temperatures is shown in Fig. 2. All wafers were prebaked at either 1000°C or 900°C in a 6 torr H_2 ambient prior to the deposition. The deposition is carried out in a mixture of 7.4% DCS in H_2 at 0.6 torr. In most runs a 0.025% low-concentration flow of DCS is initiated during the in-situ prebake cycle [6].

The surface morphology of epitaxial films was inspected by Nomarski microscopy. The epitaxial film thickness was determined from a measurement of oxide thickness and a surface profile measured on wet-etched wafers included in each run. Crystallographic defects were studied by microscopy follwing a dilute Schimmel etch [16], as well as plane-view and cross-sectional transmission electron microscopy (XTEM). The identification and the profile of impurities in epitaxial layers were determined by energy dispersive X-ray spectroscopy(EDX) and secondary ion mass spectroscopy (SIMS) analyses, respectively.

4.3 Effects of Plasma Etch on the Quality of Si Epilayers

The quality of the epitaxial Si layers on substrates with or without the various sacrificial oxide films were measured and compared. The results are summarized in Table 2. A study of the XTEM's reveal further details about the nature of the defect structures. Fig. 3 shows XTEM micrographs of epilayers deposited at 850°C after a 1000°C prebake. Specimens with or without a sacrificial oxide growth after the plasma etch show a large undercut [17] of the masking oxide owing to the rapid Si-SiO_2 reaction in H_2 at 1000°C. In the absence of a sacrificial oxide, as shown in Fig. 3 (a), dense dislocation loops and precipitates † are seen at the

† In the absence of impurities, as shown in the SIMS analysis, these precipi-

epi/substrate interface as well as dense microtwins and dislocations in the epilayer. On the other hand, with the sacrificial oxide, the epilayers are defect-free; an example is shown in Fig. 3(b).

If a 900°C prebake instead of 1000°C is employed prior to the deposition, the formation of undercut is avoided; furthermore, the defect behavior is modified. In the absence of a sacrificial oxide growth for the 900°C deposited epilayer, XTEM analysis, Fig. 4, shows dense dislocation loops and precipitates (about 14-20 nm in size) at the epi/substrate interface. However, no microtwins are observed in the epilayer. Fig. 5 shows Nomarski micrographs of the epilayer before and after a dilute Schimmel etch. It does not reveal any surface features until the etch removes a 0.75 um Si layer. After a 3 minute etch which removes a 1 um Si layer, many pits appear. Thus the strain fields near the dislocation loops and precipitates shown in Fig. 4 locally accelerate the Si etch rate and resulting in many small etch-pits as the etch front approaches the epi/substrate interface. This examination is consistent with that of XTEM in which no microtwin is observed in epilayers. SIMS analysis further shows only a fluorine peak at the epi/substrate interface; oxygen and carbon are below the detection limits. The examination of several specimens prepared from different regions of the wafers show similar results. Thus these "precipitates" are not the usual Si-O complexes, they consist only of damage clusters and Si-F complexes.

Again, with the sacrificial oxide, XTEM's show that the epilayers grown after the 900°C prebake are defect-free; an example is shown in Fig. 6 for a 5 nm sacrificial oxide thickness. The effectiveness of a 5 nm oxidation (removing about 2.2 nm of Si) is somewhat surprising in light of the much thicker damaged layer reported for plasma etching [14-15]. A 3.5 minute dilute Schimmel etch reveals no

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tates could be damage clusters, or impurity-damage cluster formed complexes.

etch-pits near the epi/substrate interface, consistent with the XTEM. Furthermore, SIMS analysis shows no O, C or F peak at the epi/substrate interface. For substrates with thicker sacrificial oxide films (10, 15, 20, and 25 nm, respectively), XTEM, dilute Schimmel and SIMS analyses consistently show the elimination of all interfacial damage.

Epilayers deposited at 850°C after a 900°C prebake in H_2 show similar results to the 900°C grown films. In the absence of sacrificial oxide, the XTEM micrograph in Fig. 7(a) shows dense interfacial dislocation loops and small precipitates about half the size of those observed in Fig. 4 for 900°C growth. Schimmel etch studies again do not reveal any etch-pits in the epilayer until the etch front approaches the epi/substrate interface. As for 900°C growth, the use of a sacrificial oxide, 5 nm or thicker, completely eliminates the interfacial defects. An XTEM of an overgrown epilayer following a 5 nm sacrificial oxide treatment is shown in Fig. 7(b).

4.4 The Characteristics of Plasma-Etch-Induced Defects in Si Epilayers

The observation of precipitates and dislocation loops in samples etched in He, CH_4 and CHF_3 plasmas suggests the interaction of point defects with impurities (possibly C, F, H or He in our experiments) during prebake and deposition. In studies of the anneal of defects, Seidel et al [18], Queirolo et al [19], and Carter et al [20] have shown that most of intrinsic point defects and clusters can be annealed out in the temperature range from 700°C to 1000°C. Kim et al [21] further indicate that intrinsic dislocations can be removed after anneal of 25 to 250 sec at 1000°C or $2x10^3$ to $2x10^4$ sec at 900°C. The stability of defects seen in Fig. 3(a) therefore requires interaction with impurities or precipitates. During the ramp up and the prebake steps, there is extensive motion of vacancies and interstitial Si, as well as of

the plasma-etch-induced impurities, but conditions favor defect agglomeration and growth rather than elimination or dissolution. Because of limited solubilities of these impurities in Si, they may either nucleate precipitates or diffuse to decorate dislocation loops. For 900°c prebaked Si substrates, as shown in Fig. 4 and Fig. 7(b), dislocation loops and precipitates are observed only at the epi/substrate interface after the epitaxial growth. But after a 1000°C prebake, we also observe the formation of microtwins. Possible factors which can account for the latter include: (1) the more favorable conditions for facet formation in the vicinity of the large precipitates formed at 1000°C. (2) the temperature dependence of mechanical properties of silicon. For epilayers with a 900°C prebake, it is possible that the dimension of precipitates near the Si surface is less than the critical dimension required to form microtwins during the epitaxial growth. For example we observe larger precipitates in 900°C deposited epilayers (average dimension is 14-20 nm), and smaller precipitates in 850°C epilayers (average dimension is about 6-14 nm). The second possible factor relates the strong (activated) temperature dependence of the motion of extended defects in Si. Again, the nucleation of microtwins may be enhanced at higher temperatures by the relatively easier motion of defect precursors during the bake cycle. In any case the plasma-etch-induced surface contaminants and ion-bombardment-induced surface defects can result in the formation of precipitates and dislocation loops at the epi/substrate interface, as well as dislocations and microtwins in epilayers.

We have also analyzed epilayers deposited on substrates for which the oxide is patterned by a continuous plasma etch. If a sacrificial oxidation is performed, apparently, defect-free epitaxial films are grown. However, XTEM analysis shows that the epi-substrate interface is not completely free of defects; a "stringer-like" precipitate is observed near the pattern edges. Fig. 8 shows a typical example. EDX studies show that these inclusions are SiO_2. Even a 25 nm sacrificial oxide is

inadequate for the elimination of whatever contaminants cause these inclusions. It is believed that the a build up of the polymer responsible for anisotropy occurs in the corners. Such a polymer can mask removal of oxide during the sacrificial process. The tenacity of the polymer film was demonstrated by experiments in which even a three hour fresh H_2SO_4 +H_2O_2 immersion and a three minute HF dip after the sacrificial oxidation did not eliminate the inclusions. We attribute the superior performance of cycled plasma etching to the interaction of oxygen or water in air with the polymer films.

4.5 Summary

The influence of plasma etch (He + CHF_3 + CF_4) on the substrate surface prior to low temperature selective epitaxy has been studied. With a low temperature (900°C) prebake process, plasma exposure results in dislocation loops and precipitates at the epi/substrate interface. For a high temperature (1000°C) prebake, larger precipitates, microtwins, and dislocation lines are also observed. XTEM and SIMS analyses show that these defects are attributed to the plasma-etch-induced surface damage and contaminants on substrates. During the prebake these contaminants either form precipitates or segregate at dislocations, It is found that a sacrificial oxide film can efficiently remove plasma-etch-induced surface damage and contaminants on substrates. However, a long duration plasma etch can accumulate a tenacious polymer film at the pattern edges resulting in oxide inclusion along the edges. A cycled plasma etch can avoid the thick polymer accumulation. With this plasma etch modification, a sacrificial oxide growth, and oxide removal step, defect-free epilayers are obtained. Dilute Schimmel etch, SIMS and XTEM analyses indicate that a 5 nm 900°C grown sacrificial oxide is thick enough to completely remove plasma-etch-induced surface damage and contaminants after a HF dip, and achieve high quality SEG Si epilayers at low deposition temperatures.

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Table 1

The Recipe of Plasma Etch

Parameters	Isotropic Etch	Anisotropic Etch
Time	2 sec	30 sec
Pressure	2.8 Torrs	3.0Torrs
RF Power	850 Watts	900 Watts
Gap Spacing	0.38 cm	0.40 cm
CF_4	90 sccm	40 sccm
CHF_3	30 sccm	45 sccm
He	120 sccm	120 sccm

Table 2

The Quality of Epilayers Observed by SIMS and XTEM

Prebake	Deposition	Sac. Oxide	SIMS	XTEM
1000°C	850°C	no	--	Microtwins and dislocations in the epilayer, precipitates and dislocation loops at the epi/Si substrate interface.
1000°C	850°C	25 nm	--	Defect-free.
900°C	900°C	no	F peak	Precipitates and dislocation loops at the epi/Si substrate interface.
900°C	900°C	5 nm	--	Defect-free.
900°C	850°C	no	O peak	Precipitates and dislocation loops at the epi/Si substrate interface.
900°C	850°C	5 nm	--	Defect-free.

Fig. 1. XTEM micrographs of epilayers deposited in wet-etched-epitaxial windows at 850°C. Microtwins are apparent near the edge of the epi/SiO_2 sidewall. The sidewall direction is <110> in 1(a) and <100> in 1(b), respectively.

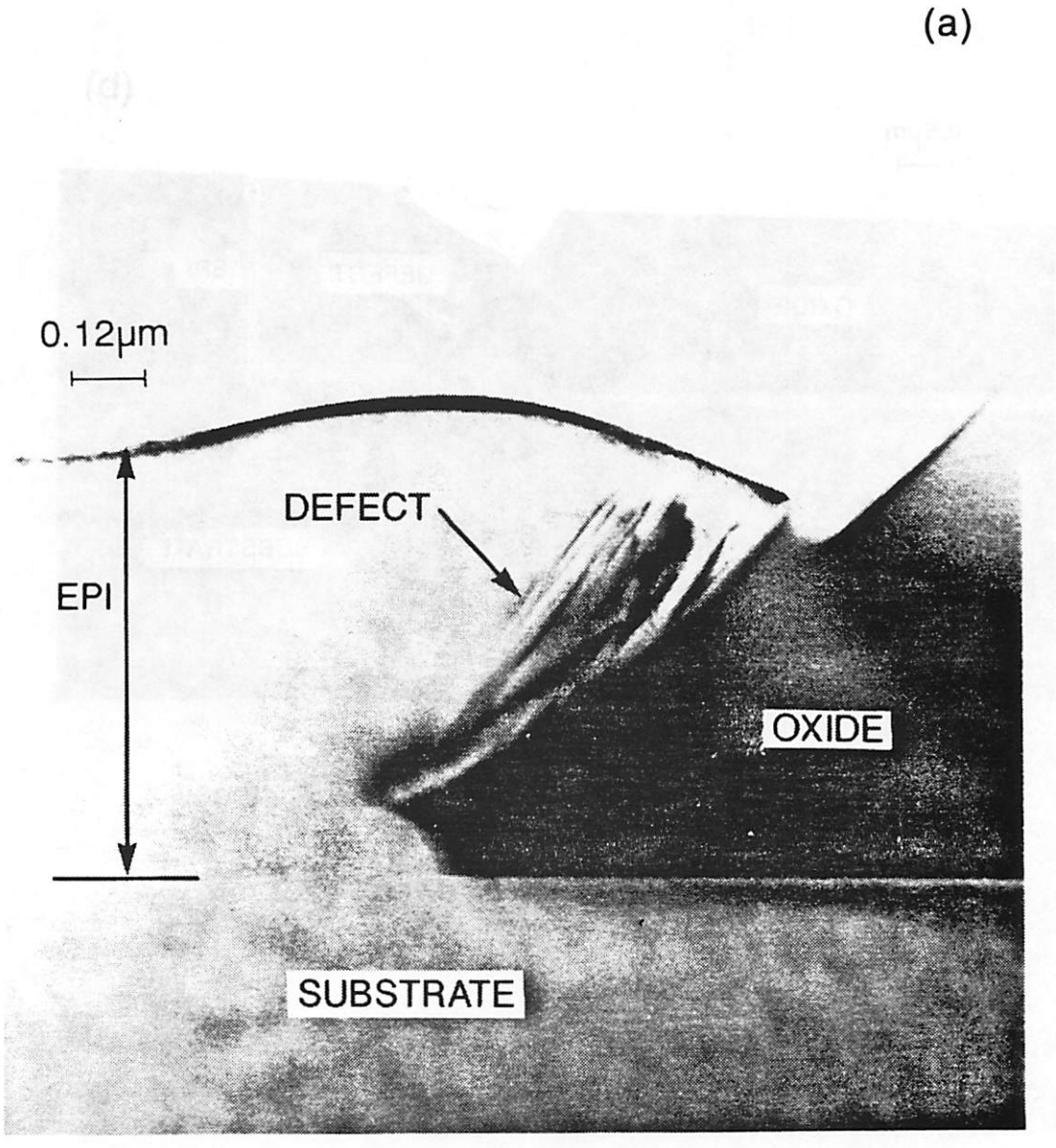


Fig. 1. (cont.)

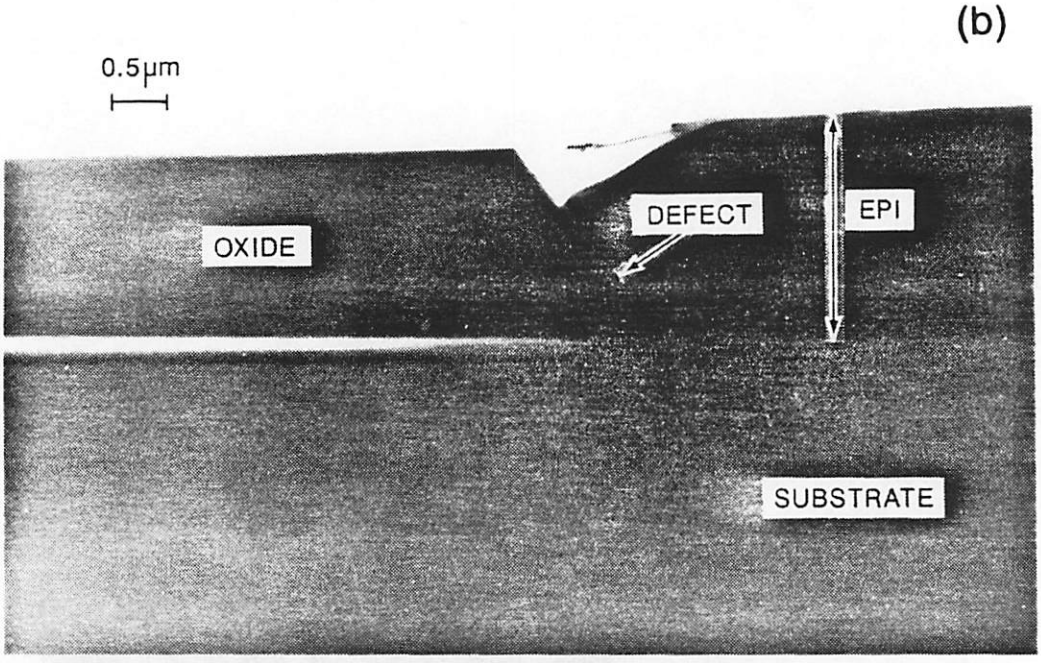


Fig. 2. The deposition cycle for the selective epitaxial growth. (a) Epilayers deposited at 850°C after a 1000°C prebake. (b) Epilayers deposited at 900°C or 850°C after a 900°C prebake.

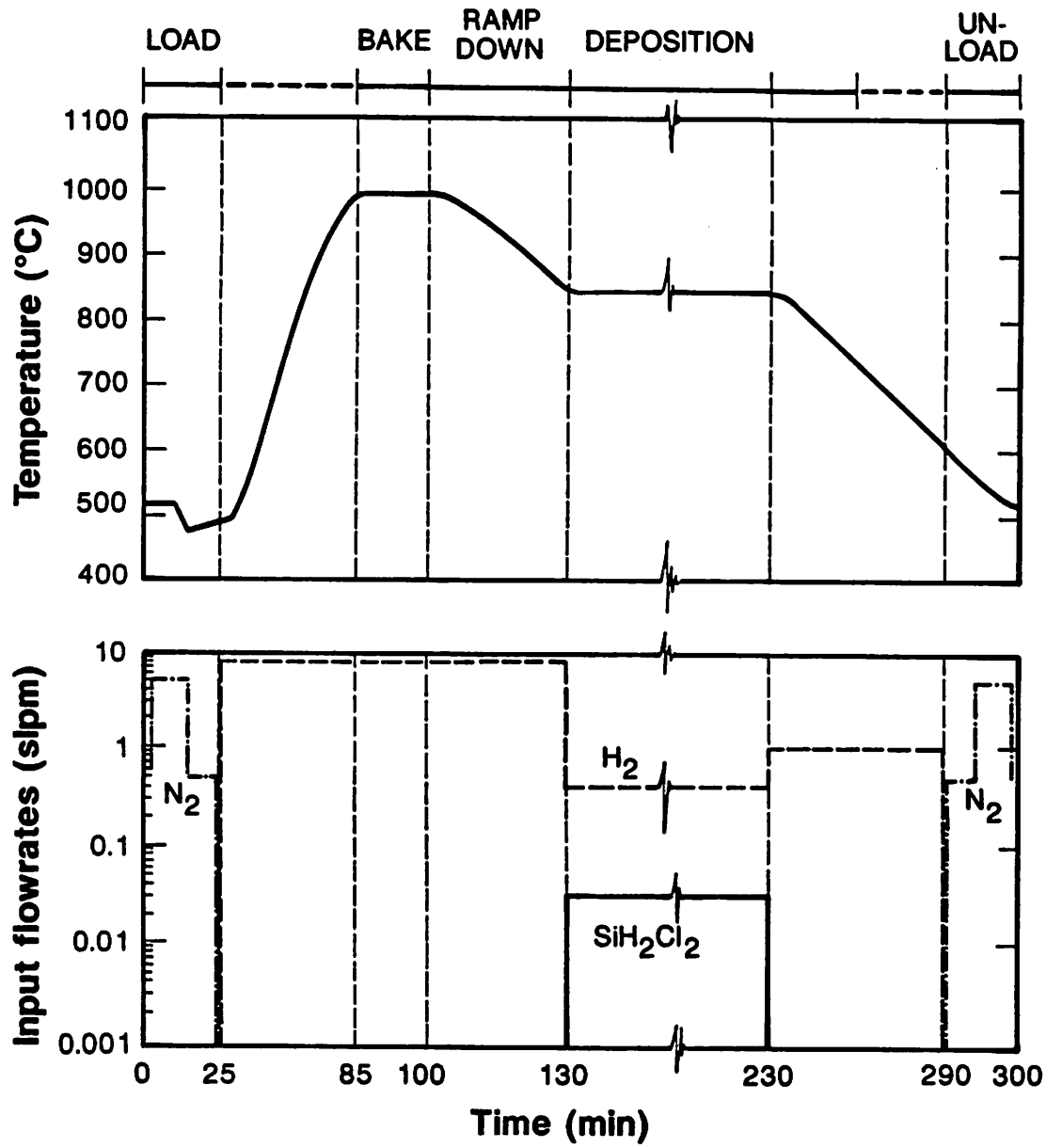


Fig. 2. (cont.)

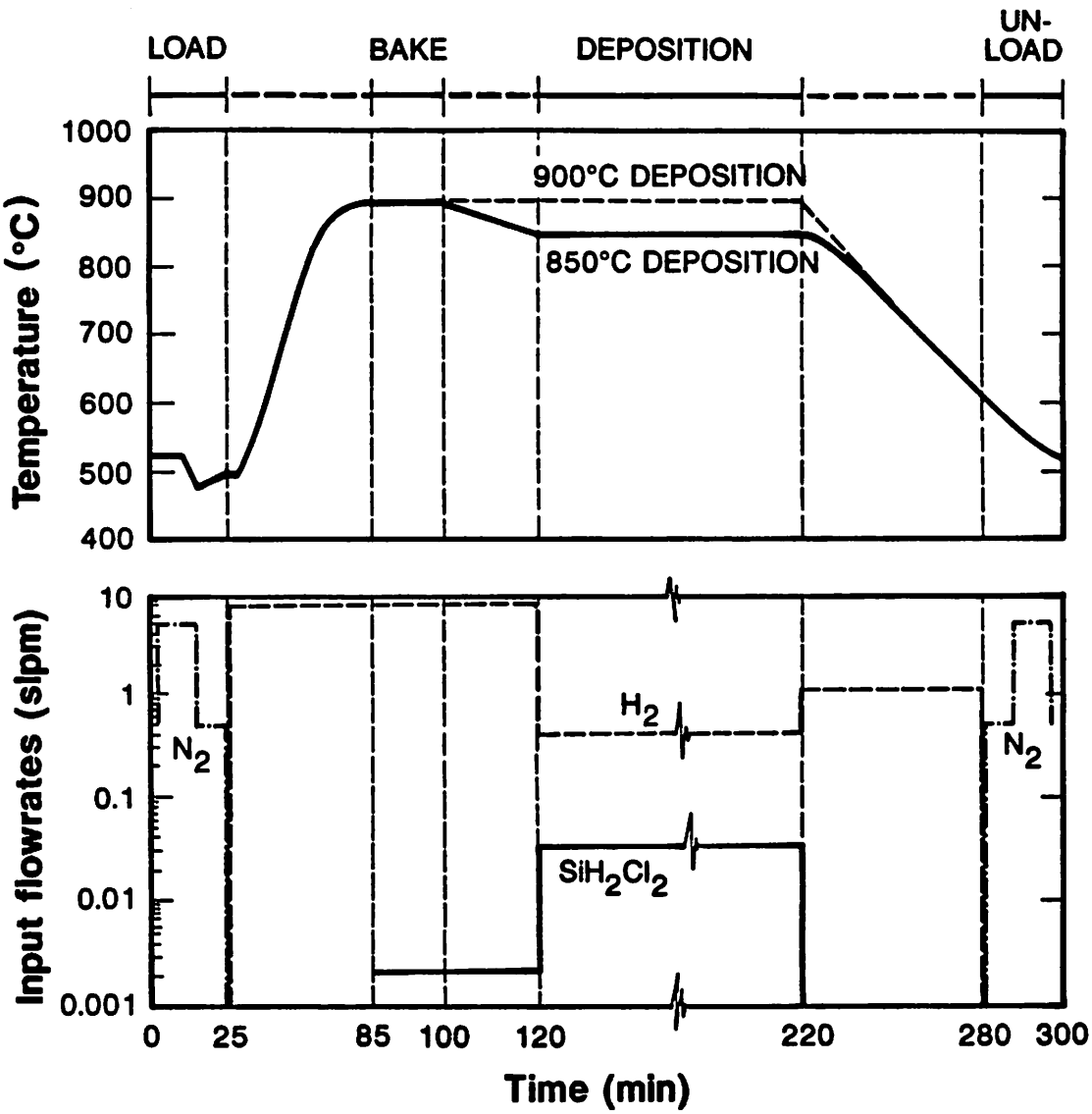

LOAD
BAKE
DEPOSITION
UN-LOAD
1000
900
800
700
600
500
400
Temperature (°C)
900°C DEPOSITION
850°C DEPOSITION
10
1
0.1
0.01
0.001
Input flowrates (slpm)
N2
H2
SiH2Cl2
N2
0
25
85
100
120
220
280
300
Time (min)

Fig. 3. XTEM micrographs of epilayers deposited at 850°C after a 1000°C H_2 pre-bake. (a) There is no sacrificial oxide growth after the plasma etch. The epilayer is defective. (b) With a 25 nm 900°C grown sacrificial oxide it shows no defect in the epilayer.

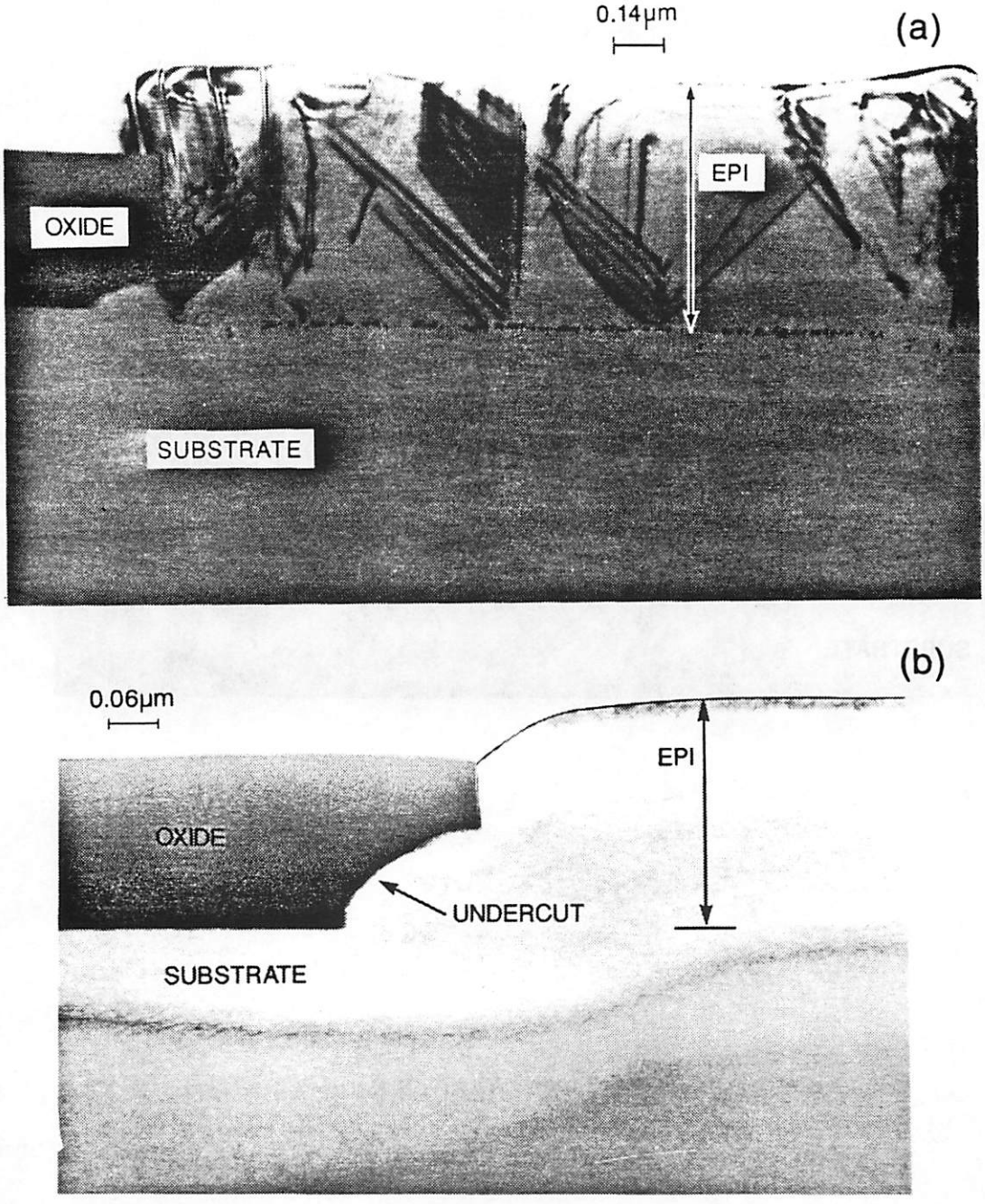


Fig. 4. The XTEM micrograph of an epilayer deposited at 900°C after a 900°C H_2 prebake. With no sacrificial oxide growth the epilayer shows disloaction loops and precipitates at the epi/substrate interface.

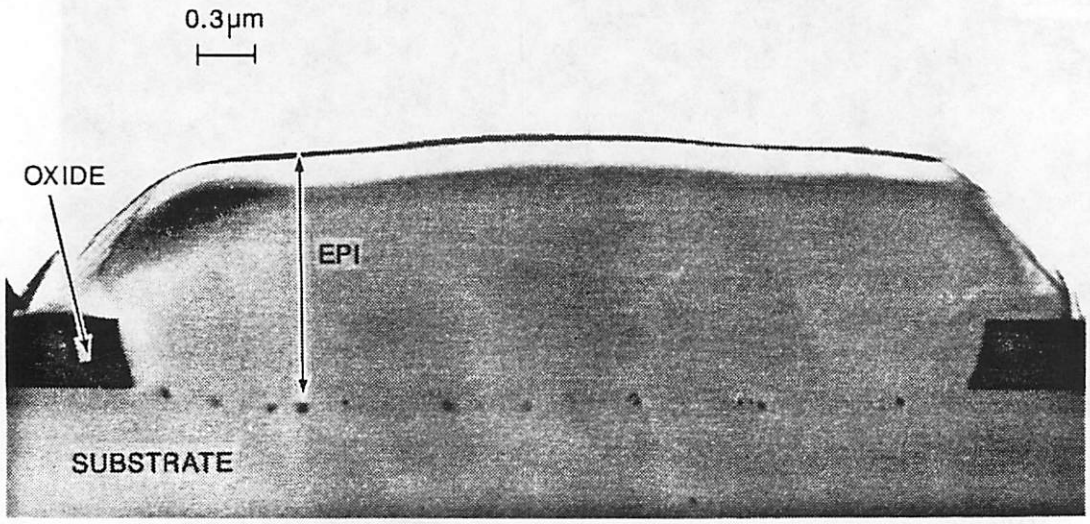


Fig. 5. Nomarski micrographs(1000X) of the epilayer of Fig. 4. (a) Before the dilute Schimmel etch. (b) After a 3 minute dilute Schimmel etch, it reveals dense etched pits near the epi/substrate interface.

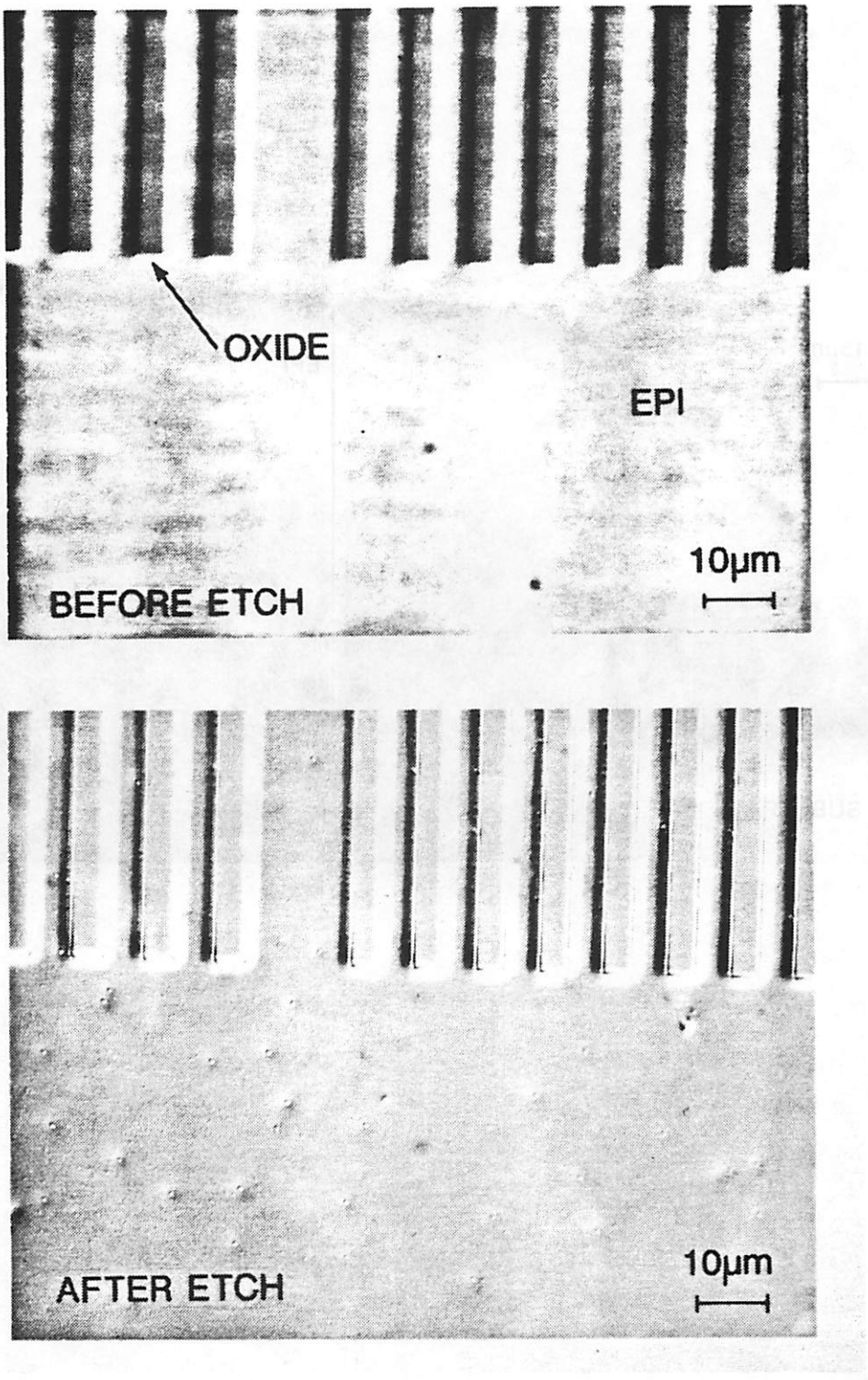


Fig. 6. The XTEM micrograph of an epilayer deposited at 900°C after a 900°C prebake. The sacrificial oxide thickness is 5 nm. It shows a defect-free epilayer.

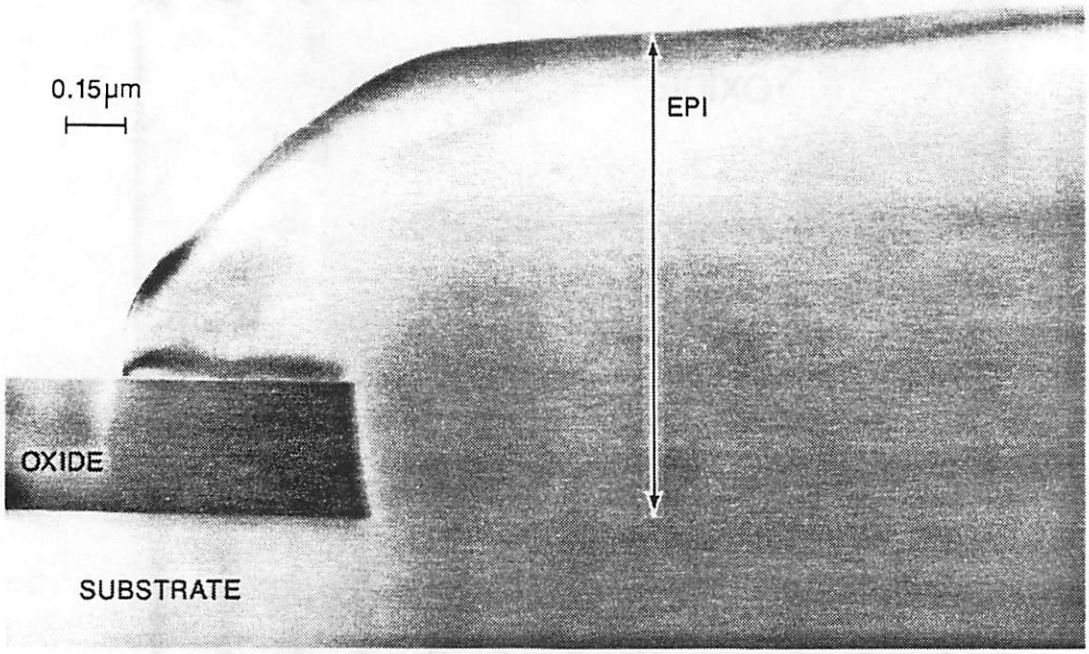


Fig. 7. The XTEM micrograph of an epilayer deposited at 850°C after a 900°C H_2 prebake. (a) With no sacrificial oxide growth it shows dense dislocation loops and precipitates at the epi/substrate interface. (b) The sacrificial oxide is 5 nm thick. The epilayer is defect-free.

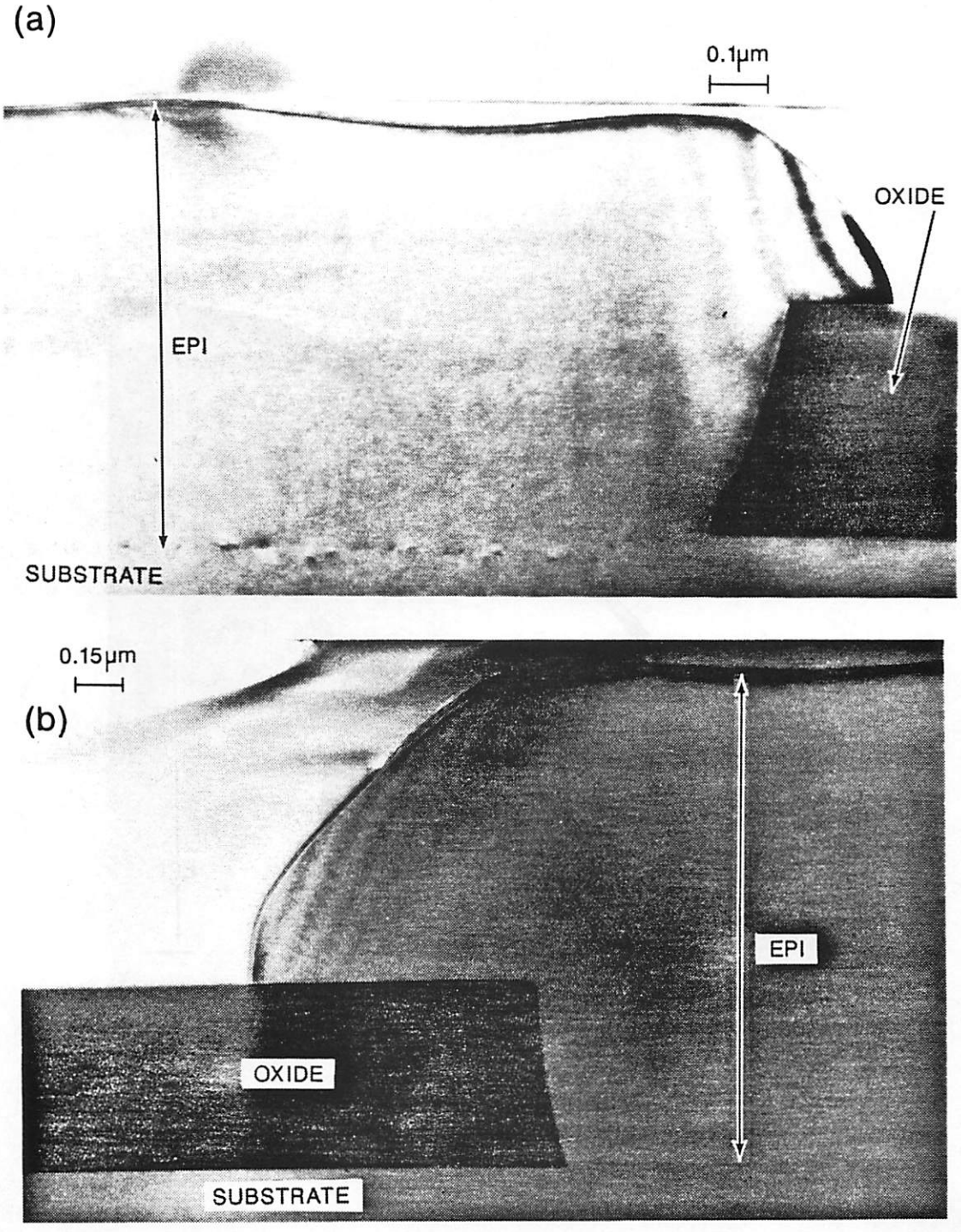
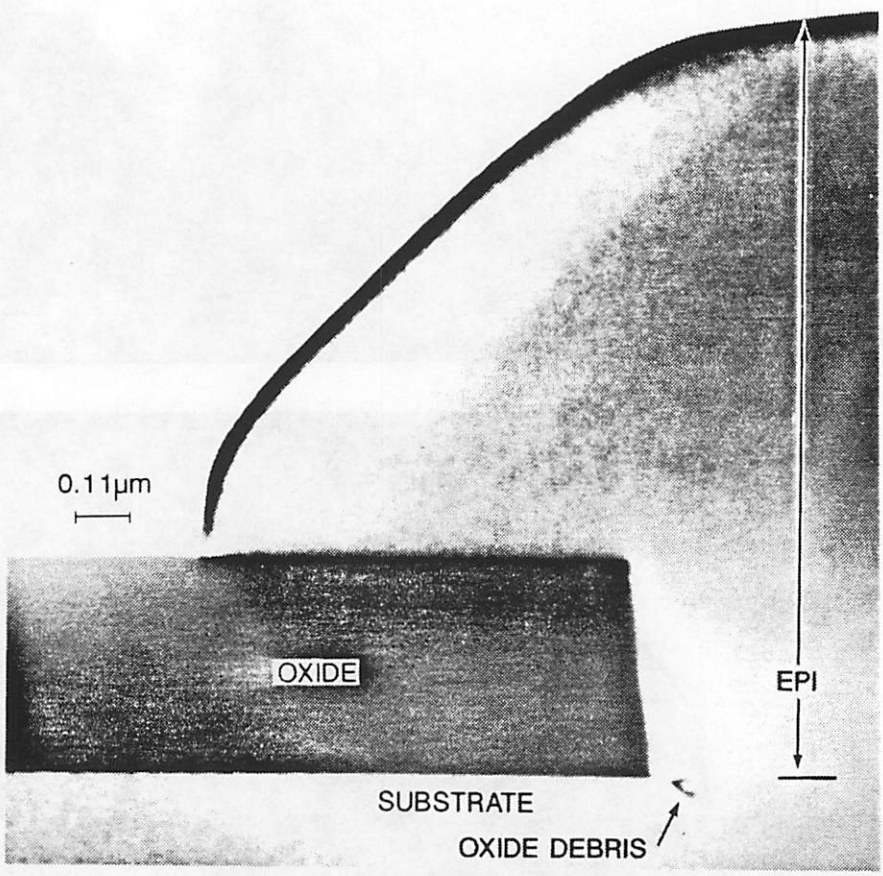


Fig. 8. The XTEM of an epilayer deposited at 900°C after a 900°C H_2 prebake. Although a 25 nm thick sacrificial oxide film is grown after the plasma etch of continuous mode, it still shows oxide inclusions near corners of epi/SiO_2 sidewalls.



Chapter 5

The Surface Morphology of Selectively-Grown Epitaxial Silicon

The low temperature epitaxial growth of Si under conditions in which no nucleation occurs on SiO_2 (selective growth) results in interesting new surface morphology. We find in this study that for substrates free of non-volatile surface contaminants, specular defect free films are obtained at 850°C. Surprisingly, small residual oxide islands can also be tolerated because of epitaxial lateral overgrowth. However, for islands greater than about 50 nm, shallow surface pits on an otherwise specular surface are observed. For these reasons, the goal of this chapter is to correlate these surface features to wafer preparation, deposition temperatures, and deposition cycle for understanding the formation of pits and textured morphology on the surface of Si epilayers. Based on experiments which show a reducing in growth rate in oxygen implanted region, we attribute these surface depression to an oxygen effect. If the interfacial oxide islands are of such high density that they merge into a semi-continuous film, a textured surface morphology is observed, although the film is epitaxial and can be defect-free. At even higher levels of interfacial contamination, threading dislocations and other defects are observed.

5.1 Introduction and Background

The chemical vapor deposition (CVD) epitaxy process is widely used in the fabrication of integrated circuits [1-3]. The conventional atmospheric pressure CVD epitaxial process (APCVD) generally is associated with high deposition temperatures, resulting in undesirable interdiffusion at the epi/substrate interface and autodoping from the substrate. If the growth temperature decreases below 1000°C, the epitaxial quality is degraded [4-5]. Recently, it is found that low-pressure epi-

taxial growth has several advantages as compared to atmospheric-pressure epitaxy [6-7]. There are (1) the decrease in the deposition temperature, (2) the improvement of deposition uniformity (resistivity and thickness), (3) the reduction of gas phase autodoping, (4) the increase in deposition rate and (5) the improvement of pattern integrity. Therefore, silicon epitaxial layers with abrupt dopant profiles for high performance integrated circuit applications are commonly achieved through low pressure chemical vapor deposition (LPCVD). The trend is toward lower deposition temperatures, where the surface cleanliness becomes even more critical. At lower deposition temperatures the epitaxial quality is seriously influenced by the adsorption of gas-phase components on the substrate surface prior to the deposition [8-11].

The object of this paper is to shed further light on the relationship between surface preparation, deposition temperature, and reaction conditions on film quality. In particular, the formation of pits and textured morphology on the surface of silicon epilayers is related to surface conditions prior-to and during deposition. With adequate control of surface it is possible to grow high quality silicon epilayers in the selective epitaxial growth (SEG) mode at 850°C. In this study, it is found that non-volatile surface contaminants are responsible for the drastic variations in the surface morphology of Si epitaxial layers. Most of the visible defects on the surface are pits associated with residual patches of oxide at the substrate surface. Moreover, it is revealed that textured and hazy surface morphology are caused by a high density of fine pits. Evidence suggests that the dissolution of interfacial oxide islands and the subsequent diffusion of oxygen atoms in epilayers play a role in the reduction of the Si growth rate and the formation of pits on the Si surface. The existence, the density, and the size of oxide islands at the epi/substrate interface highly depends on both the pre-epitaxial "bake" and the growth temperatures. For defective Si epilayers grown at 850°C, most of interfacial oxide islands are decorated by a pit on the surface. However, if the dimension of interfacial oxides is

small, e.g. less than 50 nm, the surface remains specular. For defective epilayers grown at 900°C, interfacial oxide islands are generally not observed associated with surface pits, suggesting they may be dissolved in the overgrowth and then result in pits on the surface. The case of the ex-situ HF vapor treatment combined with an in-situ "native" oxide removal bake [12-13] in the presence of a low concentration of SiH_2Cl_2 minimizes the residual interface oxide prior to the deposition, and high quality specular Si epilayers are achieved at low growth temperatures (820°C-850°C).

5.2 Wafer Preparation and Experimental Procedure

The silicon wafers used for SEG were P-type (100) with resistivity of 30-50 ohm-cm. A 570 nm thermal oxide layer is grown at 1000°C. The test pattern defining bare and oxide-covered areas is aligned along <100> directions. After plasma etch and resist removal, a 25 nm sacrifical oxide is grown at 900°C and removed to eliminate any plasma-etching-induced surface damage. The standard pre-epitaxial clean steps consists two piranha cleaning treatments separated by a dilute HF dip that removes the sacrifical oxide. Subsequently, the wafers are exposed to the HF vapor over 1:2 mixture of H_2O: 49% HF for 5 seconds to remove the chemical oxide and passivate the wafer surface [12], then immediately loaded into a horizontal hot-wall reactor at 525°C. The deposition cycle is illustrated in Fig.1. All wafers are ramped up to 900°C for a prebake in a 6 torr H_2 ambient prior to ramping down to the deposition temperature. In those runs in which a 0.025% low-concentration flow of DCS is used as part of the in-situ prebake cycle, the time T_1, Fig.1, is the initiation point.

The surface morphology of Si epilayers is inspected by Nomarski microscopy. Interfacial oxide islands are most simply revealed by means of a diluted Schimmel etch [14], transmission electron microscopy (TEM) is used both for

correlation of oxide inclusions with Schimmel-related defects and in general for higher resolution, less ambiguous identification. The profile of impurities in the films at the substrate-film interface and in the substrate are determined by secondary ion mass spectroscopy (SIMS).

5.3 Defective Epilayers Deposited at 850°C

It is found that with the HF vapor treatment and the addition of a low-concentration of DCS during the ramp-down step, the prebake temperature can be minimized to avoid the formation of an undercut while retaining the ability to grow single crystalline Si epitaxial layers [12-13]. However, the Si epitaxial films are not always perfect. Pits are sometimes observed near the centers of the wafers, and a textured surface observed near the peripheral areas of epitaxial wafers. In order to reveal the mechanism responsible for pits or textured structures on the surface of epilayers and improve the epitaxial quality, several experiments have been carried out to grow both defective and perfect epitaxial layers.

If a small concentration of DCS is added in the ramp down step only (T_1=100 minutes in Fig. 1), the wafer centers are nearly defect-free. However, the peripheral areas show a textured surface morphology. In between there are areas with dense pits. The Nomarski optical micrograph in Fig.2 illustrates a specular surface with some concave pits in which the edges are along the <110> directions. The dimension of the pits is about 1 um. The SIMS analysis of this sample, shown in Fig.3, shows an oxygen peak of $4x10^{18}$/ cm^3 in the areas with pits. Since the width of the interfacial peak is less than the resolution of the instrument, the area under the peak is a meaningful number. For this sample it is approximately $7x10^4$ pits/cm^2; corresponding to about $3x10^{-3}$ monolayer of SiO_2. It is believed that these pits are oxide-related. TEM studies indicate the association of buried oxide islands with concave pits. Fig.4, for example, shows a cross-section in which an

interfacial oxide inclusion is found beneath the pit. High magnification TEM analysis under diffraction conditions fails to reveal any defects around such interfacial oxide islands. The lateral dimensions of the pits in the TEM micrograph are consistent with the dimensions observed by Nomarski interference microscope. The depth of the pits is less than 100 nm, and most show low-angle facets. From the TEM we find that for this sample the oxide islands are bowl-shaped, about 85 nm wide and 7 nm thick, much smaller than the size of the concave pits. Furthermore, we find that smaller oxide inclusion do not lead to observable surface pits, e.g., as shown in Fig. 5. The critical dimension of interfacial oxide islands, below which pits are not seen on the surface of this 0.7 um thick Si epilayer is about 40 nm. Dilute Schimmel etching of such epilayers consistently reveals many more etched pits near the epi/substrate interface than are evident from surface examination. It is believed that these etched pits are interfacial oxide related. Fig. 6, for example, compares Nomarski images of a sample before and after a 2 minute Schimmel etch which removes a 0.8 um Si layer (the epi thickness is 0.7 um).

Near the peripherial areas of the wafer, it is found that the density of pits increases and the epitaxial surface quality becomes worse. SIMS analysis shows a direct correlation with residual interfacial oxygen concentration. A sequence of pictures shown in Fig.7 illustrates the change in the surface morphology. In Fig.7(a), the Nomarski micrograph shows the slightly hazy area with high density of fine pits. The density of these isolated pits is about $1.6 \times 10^6/cm^2$. At densities exceeding about $10^7/cm^2$, as shown in Fig.7(b), pits start to merge together to form a textured or hazy surface. Both the dimension of the pits, and the size of the oxide inclusions are much larger for heavily textured samples; Fig. 7(c) shows the surface morphology and the Fig.8 the cross-sectional TEM in a region with pit density ~ $10^8/cm^2$. Such samples show a peak O_2 concentration in the range of $10^{20}/cm^3$ in SIMS analysis. Concave areas also show large angle facets. The observation that the

dimensions of the oxide islands are consistent with the dimensions of the concave areas observed in Nomarski optical micrographs, is quite different from the observation of relatively large concave pits induced by small, isolated interfacial oxide islands. In addition, one observes, as in Fig.8, that a high density of threading dislocations originating at epi/oxide interface of textured samples. Interfacial voids are also seen. the origin of the voids propably lies in the geometry of the growth fronts as the larger oxide islands are buried. Alternatively, they could be generated at a later stage by the decomposition of buried or nearly-buried oxide inclusions.

5.4 Defective Epilayers Deposited at 900°C

A similar examination of films grown at 900°C shows significantly different results. The growth cycle used is the same as in Fig. 1 expect for the higher growth temperature and consequent lack of a ramp-down from the 900°C prebake in H_2. In these studies T_1 is 100 min. Low-defect epilayers are obtained in the center with increasing defects (pits) with radius. A textured surface morphology is observed near the peripheral areas of wafers. The Nomarski micrograph of Fig. 9, taken at a radius where the pit density is about $10^5/cm^2$, reveals large concave pits oriented with <110> edges. The dimension of these pits is from 1 um to 5 um across. A TEM cross-section of such a surface pit, shown in Fig.10, reveals the dimension of one pit is 4 um wide and 75 nm deep, consistent with the Nomarski micrograph. However, there is no interfacial oxide island underneath this concave pit. In fact TEM studies of larger areas indicate that concave pits on the surface are not associated with oxide islands at interface. Because XTEM's only investigate a limited volume of Si, there is only a statistical probability that we would observe a small inclusion. For a 0.1 um thick cross-sectional sample, and concave pit of 1 to 5 um diameter, the examination of dozens of pit cross-sections without observing a single inclusion implies either they are very small, or non-existent.

SIMS analysis of these areas also shows no oxygen peak at epi/substrate interface. A study of morphology as a function of radius on the 900°C samples, analogous to Fig. 7, shows some interesting differences. Fig. 11 shows the surface appearance in regions where the pit density is (a) $5x10^5/cm^2$, (b) $1x10^6/cm^2$, 1(c) $>10^7/cm^2$. In the latter, almost at the wafer periphery, the pits merge together to form textured surface. Unlike the 850°C case, TEM studies, as shown in Fig. 12, indicates a significant roughness on the surface but no oxide islands at the interface. Moreover, no microstructural defects are found in the epitaxial layer and SIMS analysis does not reveal any oxygen peak at epi/substrate interface of textured epilayers.

5.5 Oxygen Ion Implantation

Despite the absence of detectable residual oxide at the interface for 900°C films, the 850°C results lead us to suspect that interfacial oxide may play a major role in surface morphology. In order to explore this possibility an oxygen-ion-implantation experiment was performed. Wafers were patterned conventionally and the photoresist used as an mask for an O^+ ion implantation at 20 Kev (projected range of 43 nm). The fluxes chosen were $10^{12}/cm^2$, $10^{13}/cm^2$, $10^{14}/cm^2$, and $10^{15}/cm^2$. The O diffusivity and corresponding diffusion lenth ($\sqrt{Dt}$) for 100 min diffusion at 850°C and 900°C are $8x10^{-5}um^2/sec$ (0.7 um) and $2.3x10^{-4}um^2/sec$ (1.2 um), respectively [15-16]. With such large diffusivity, it is believed that the implanted oxygen atoms can diffuse from the substrate into the Si epilayer during the Si epitaxial growth. For doses of $10^{14}/cm^2$ or greater, a difference in growth rate on implanted and un-implanted regions is observed. For a dose of $10^{14}/cm^2$, the thickness of a 0.7 um film grown at 850°C is 0.04 um less in O^+ implanted area. Fig. 13 shows Nomarski micrographs of a 850°C film at two positions on the wafer. In the center, Fig. 13(a), only a step is visible. Near the periphery, Fig. 13(b), pits are found in the implanted areas. The incorporation of oxygen both retards the Si

epitaxial growth rate and enhances pit formation. We speculate that the implanted oxygen atoms diffuse from the substrate to the film/substrate interface where they either precipitate or slow the dissolution of oxide islands already present. In any case the behavior adds to the evidence suggesting that the formation of pits is oxide-related.

5.6 A Model for the Formation of Surface Features

A simple model which explains most of the observations is based on two observations: (1) the presence of oxide inclusions at the interface, and (2) the role of oxygen depressing the Si growth rate. If small islands of oxide remain on the Si surface at the start of deposition, they may be overgrown to form inclusions, e.g., as seen in Fig. 4. While the exact physical basis for the presence of oxide islands at a Si-vapor interface is not understood, such islands have been directly observed in the experiments of Ghidini and Smith [17]. By slightly extrapolating these data to 900°C, the Si surface is partially covered with patches of oxide for a H_2O vapor pressures in the range of $7x10^{-6}$ to $7x10^{-4}$ torr. Although these results do not apply to our hot-wall reactor, especially with our higher H_2 pressures, they do establish solid evidence of a transition region, rather than a sharp boundary, between oxide-covered surfaces (at high H_2O partial pressures) and oxide-free surfaces (at low H_2O partial pressures). In this surprisingly broad transition region, stable SiO_2 islands are present on the Si surface. Because of the high selectivity under our reactor conditions, no nucleation occurs on such oxide islands and the overgrowth can be defect-free. However, the oxide inclusions can act as a source for oxygen, saturating the Si locally with oxygen at the solubility limit, and depress the growth rate.

A simple one-dimensional analysis can provide some insight. At a growth rate of v_g um/sec, the flux of oxygen required to keep the Si saturated at the solu-

bility limit N^*, is just $v_g N^*$. Comparing this with the diffusion-limited flux to the surface $D_0 N^*/d$ (where D_0 is the oxygen diffusivity, and d is the epilayer thickness), suggests that oxygen diffusion to growth surface will be important if $D_0/d >> v_g$. This expression is conservative since any barrier to oxygen evaporation would reduce the inequality. In fact the oxygen would exit as SiO, and the evaporation coefficient" of SiO is known to be less than unity [17]. For published diffusivities values of $8.0 \times 10^{-5} um^2/sec$, and $2.3 \times 10^{-4} um^2/sec$, respectively[15–16], the condition above implies oxygen saturation for epitaxial layer thickness of $d < 0.73$ um at 850°C and $d < 1.6$ um at 900°C.

At higher temperatures, or under lower H_2O partial pressures, the size and density of oxide islands decreases. If they are sufficiently small, they can be completely dissolved in the epitaxial growth during the deposition (presumably with the influx of Si interstitially from, and the loss of O to, the moving epitaxial surface). The 900°C results, shown in Fig. 10, are consistent with such small islands, which although completely dissolved at the time of observation, depressed the growth rate locally.

Finally, if pregrowth conditions produce sufficiently small oxide islands, and/or the growth rate is sufficiently high, and/or the film is thick enough, then specular and defect-free films result. An example is shown in Fig. 14 in which a 3 um thick layer completely covered a series of patterned oxide lines (1 um lines and spaces) [13]. This area is inspected under a series of relections including $\vec{g}$=(220), $(\bar{2}\ 20)$ and other $\vec{g}$ vectors. No oxide islands or other defects are found at the epi/substrate interface. Furthermore, there is no seam at the intersection of the two overgrowth fronts above the oxide.

5.7 Summary

The formation of pits and textured morphology on the surface of SEG silicon films is studied. Near the wafer periphery a textured Si surface results from the high density of fine pits. SIMS and TEM analyses show that these pits are associated with interfacial oxide islands. Dilute Schimmel etch and TEM analysis indicate that such interfacial oxide inclusions of less than 40 nm in dimension do not degrade a specular epitaxial surface. We attribute the formation of pits to the local depression of the Si growth rate resulting from the dissolution of interfacial oxide islands. With a combination of ex-situ and in-situ cleans to minimize residual oxide, high quality specular SEG Si films are obtained at 850°C.

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Fig. 1. The standard deposition cycle for selective epitaxial growth at 850°C. T_1 is the time at which a low-concentration flow of DCS is initiated.

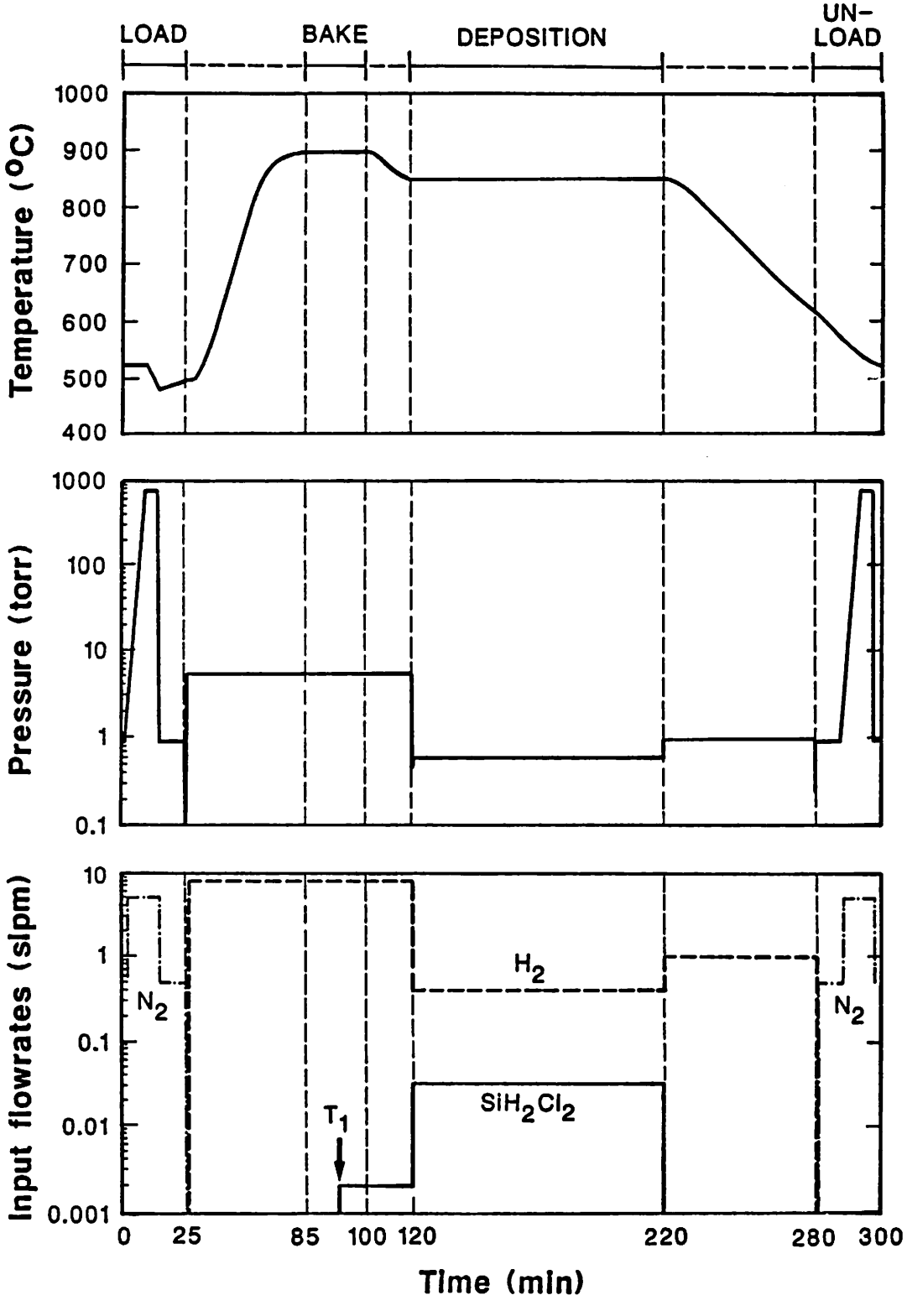


Fig. 2. The surface morphology(1000X) for regions of an epilayer containing about $7x10^4$ pits/cm^2. The low-concentration DCS flow is initiated at the start of ramp down from the 900°C bake (T_1=100 min).

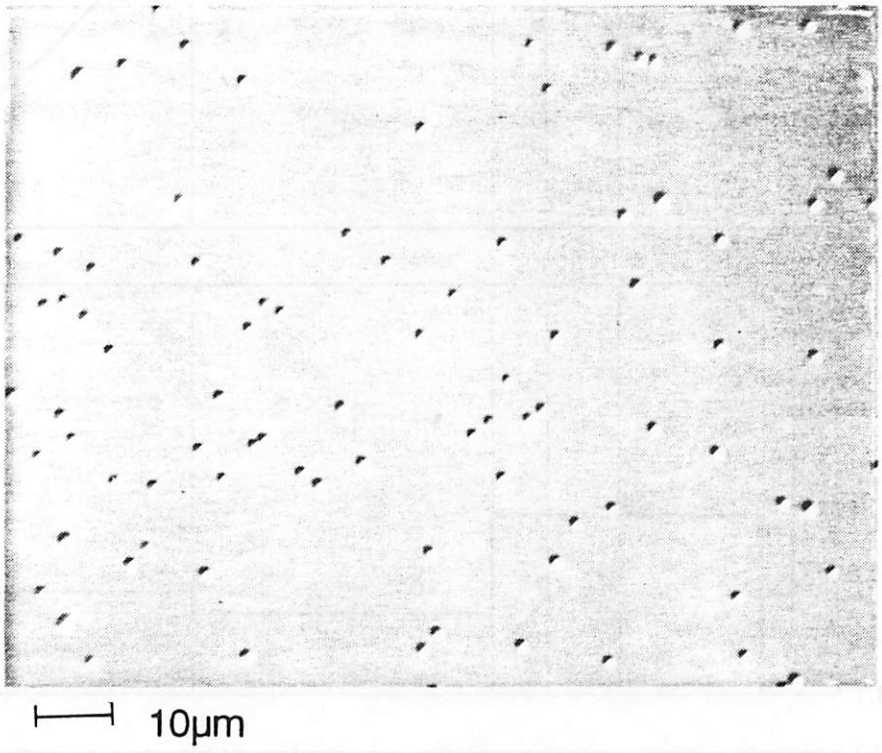


Fig. 3. SIMS profiles of oxygen and carbon for the sample of Fig.2.

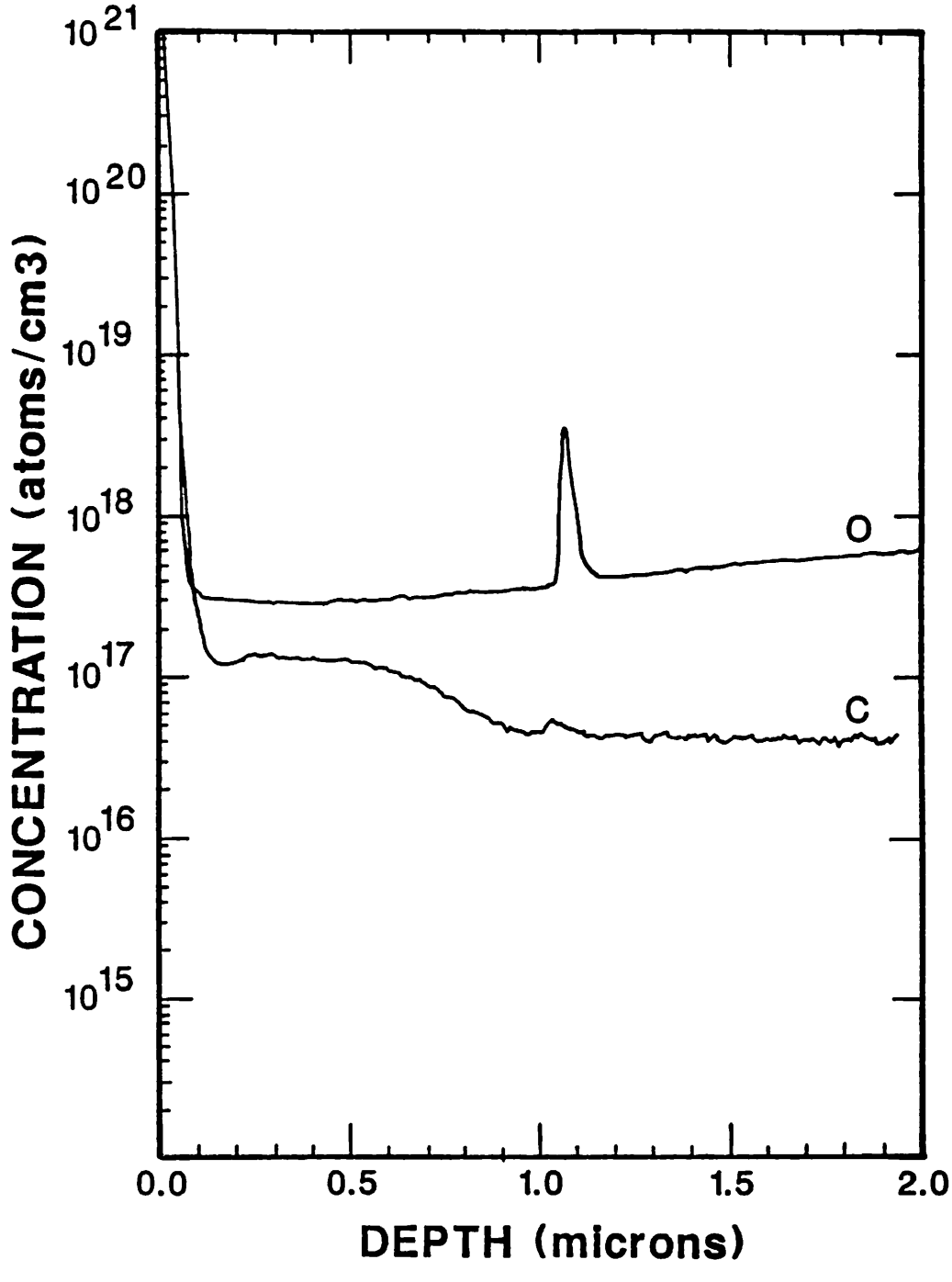


Fig. 4. An XTEM micrograph of the sample of Fig.2. The concave pit is centered above a thin interfacial oxide island.

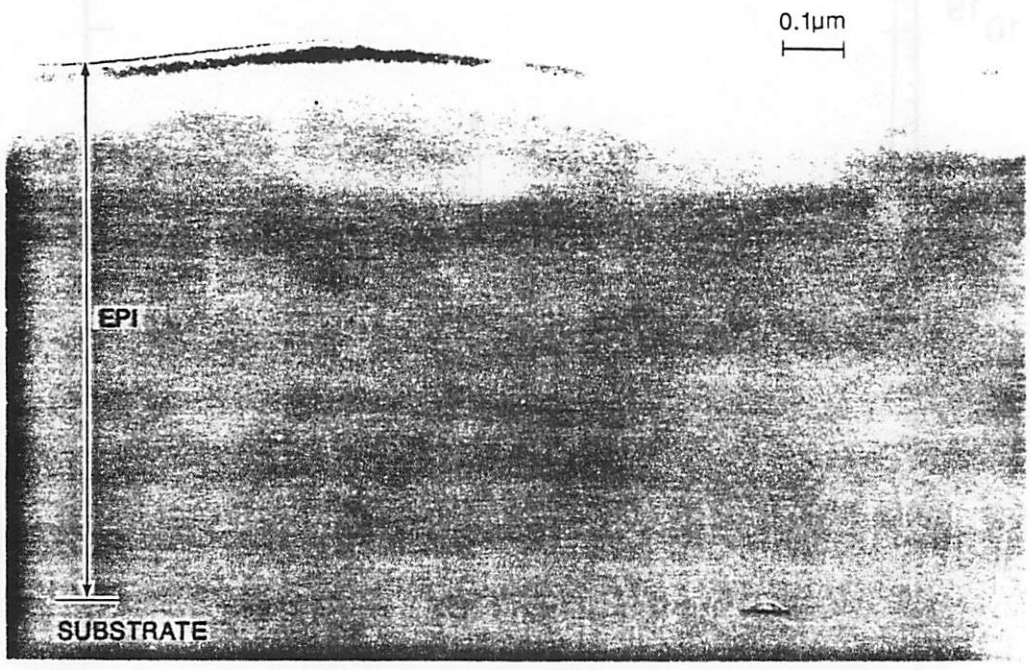


Fig. 5. An XTEM micrograph in the vicinity of a smaller oxide inclusion. The surface morphology is specular if the lateral dimension of the oxide islands are less than 40 nm.

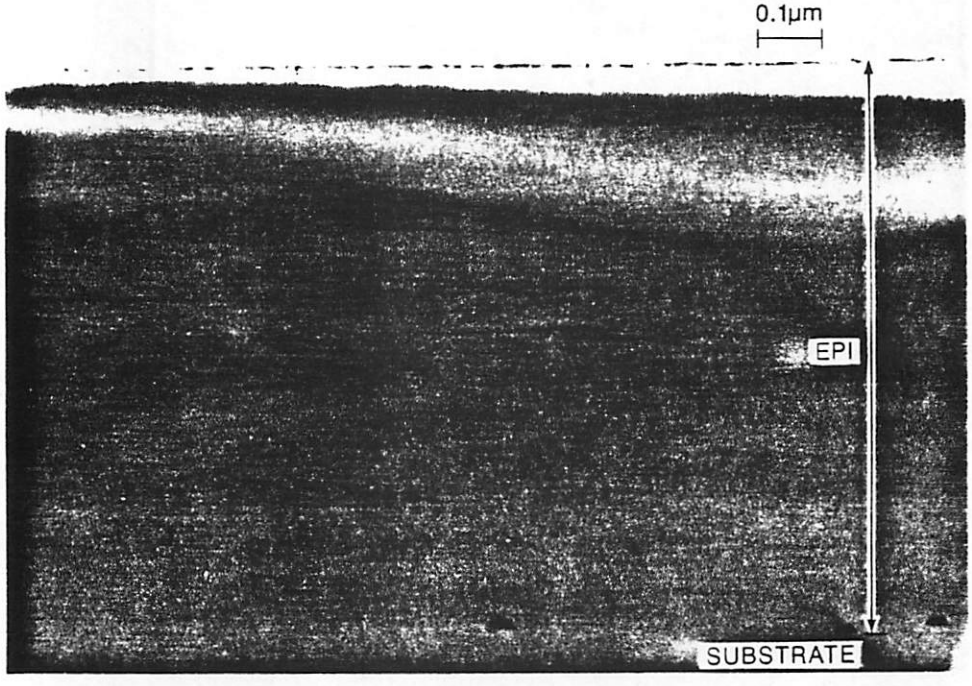
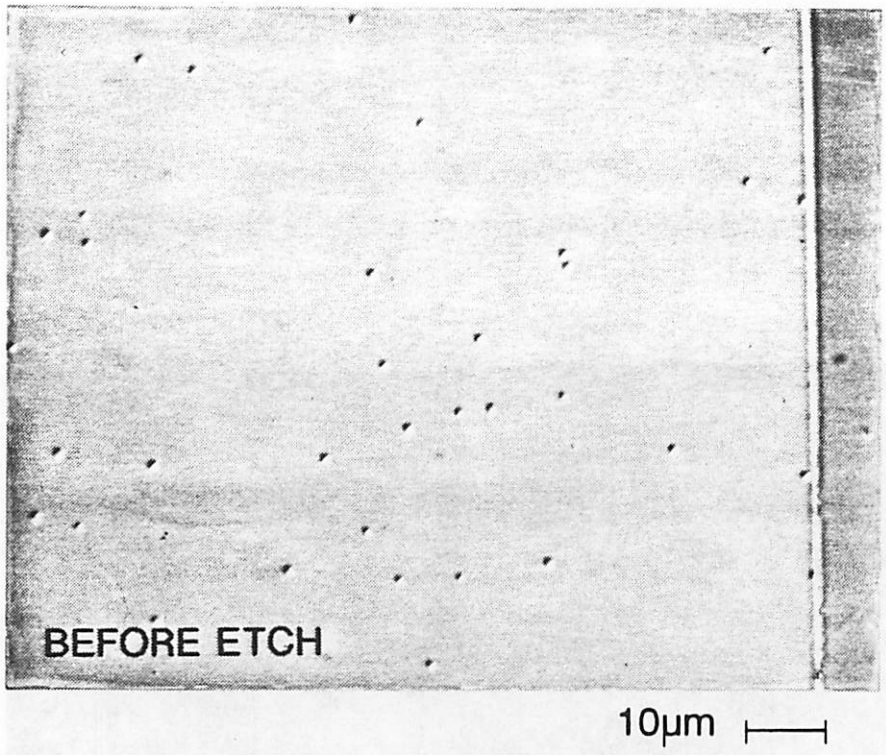


Fig. 6. Nomarski surface micrographs(1000X) comparing surface morphology of the materal of Fig. 2. (a) as-grown and (b) after a 2 minute dilute Schimmel etch which removes approximately 0.8 um Si layer, revealing the epi-substrate interface.



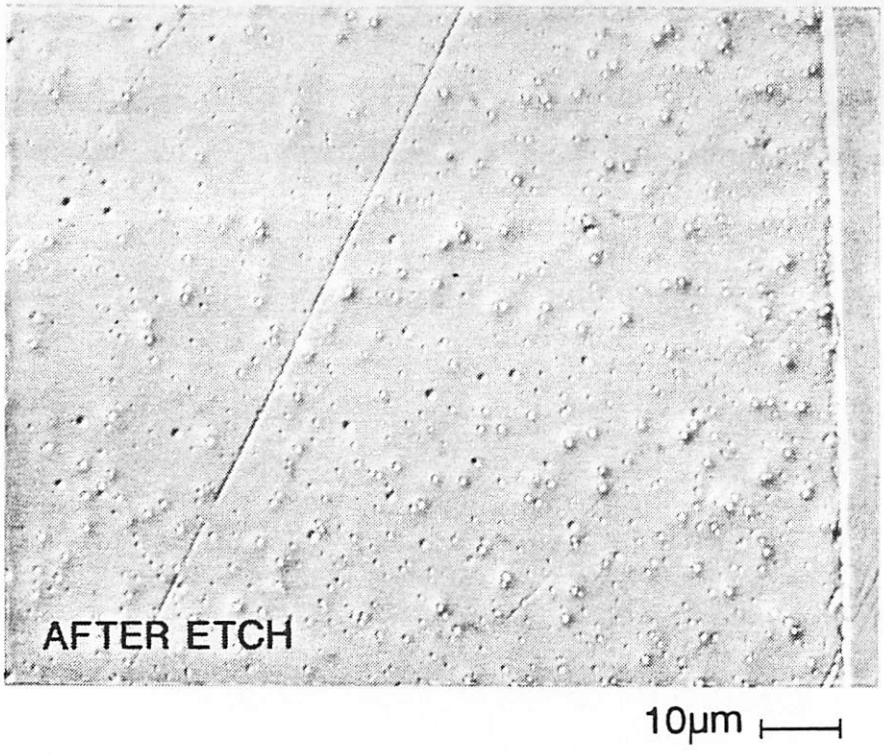


Fig. 7. Nomarski surface micrographs(1000X) for material processed as in Fig. 2, with samples taken at increasing radial position. The pit density is (a) 1.6x $10^6/cm^2$, (b) $10^7/cm^2$, (c) > $10^8/cm^2$.

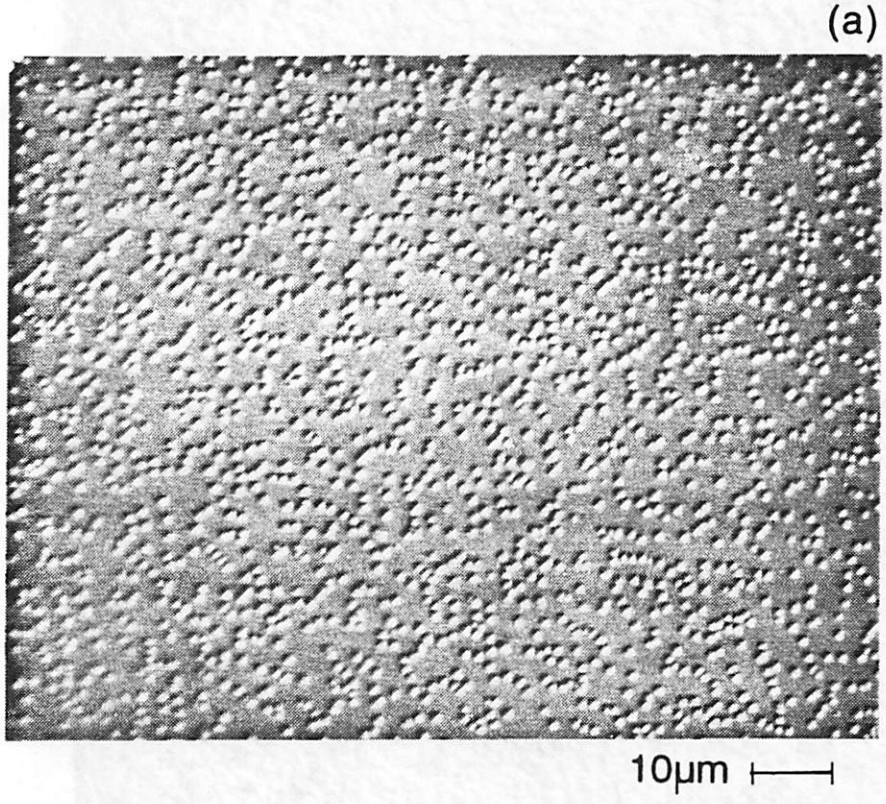


Fig. 7. (cont.)

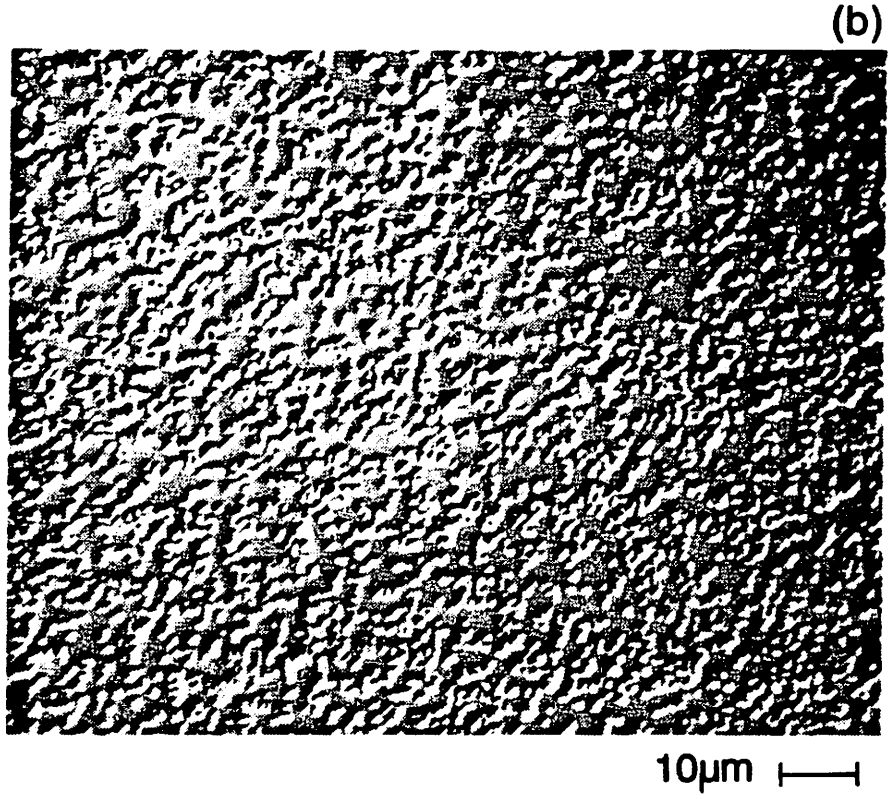


Fig. 8. An XTEM micrograph of a textured area on epitaxial film deposited at 850°C as in Fig. 2. It shows large interfacial oxide islands, voids, and dense threading dislocations in the epilayer.

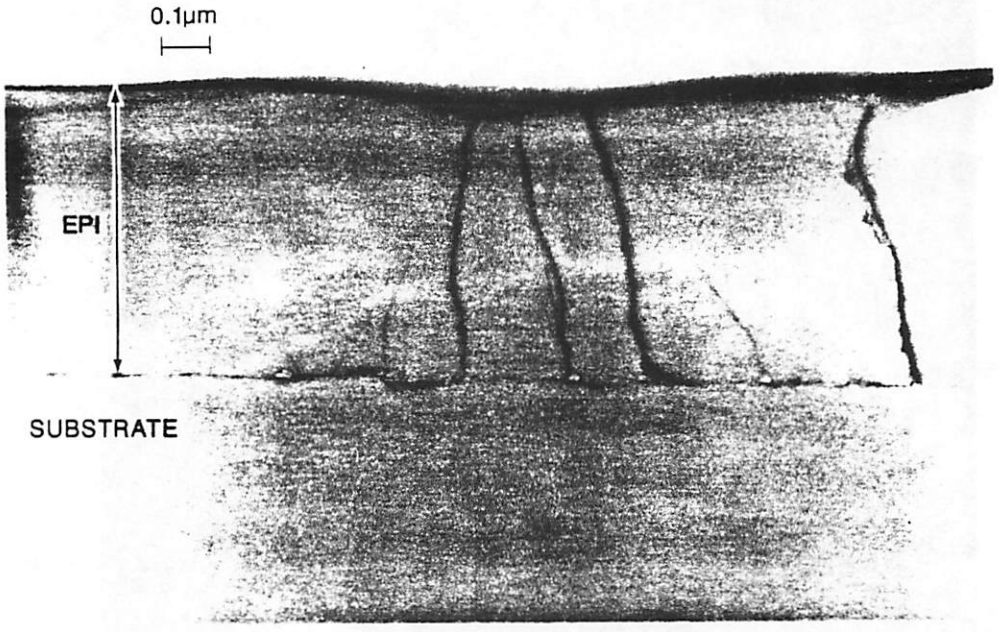


Fig. 9. The Nomarski surface micrograph(1000X) for area with pit density in the range of $10^5/cm^2$ on a epilayer deposited at 900°C.

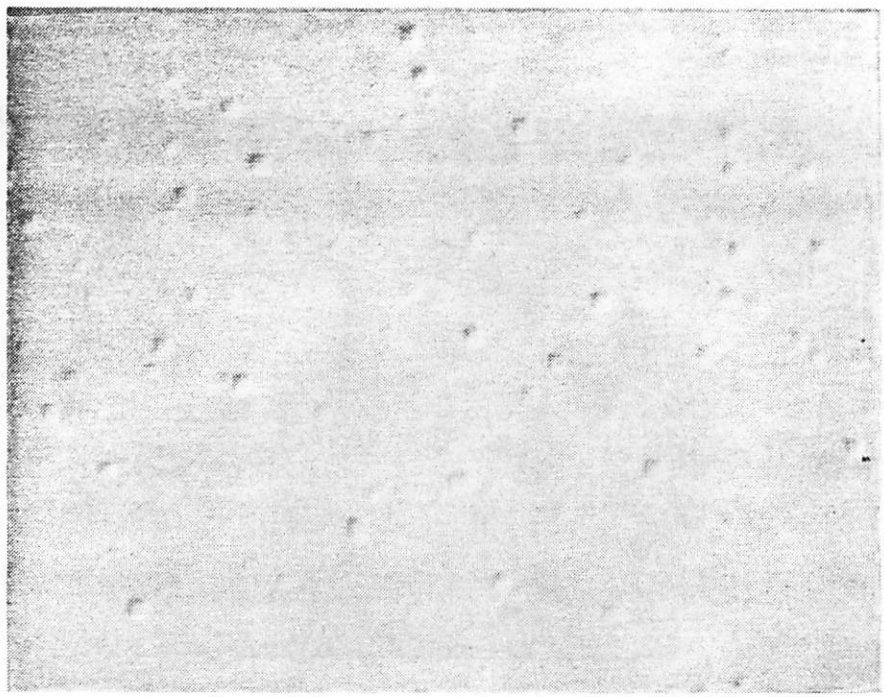


Fig. 10. A cross-sectional TEM micrograph through a concave pit on the surface of Fig.9. No oxide inclusion is found at the epi/substrate interface.

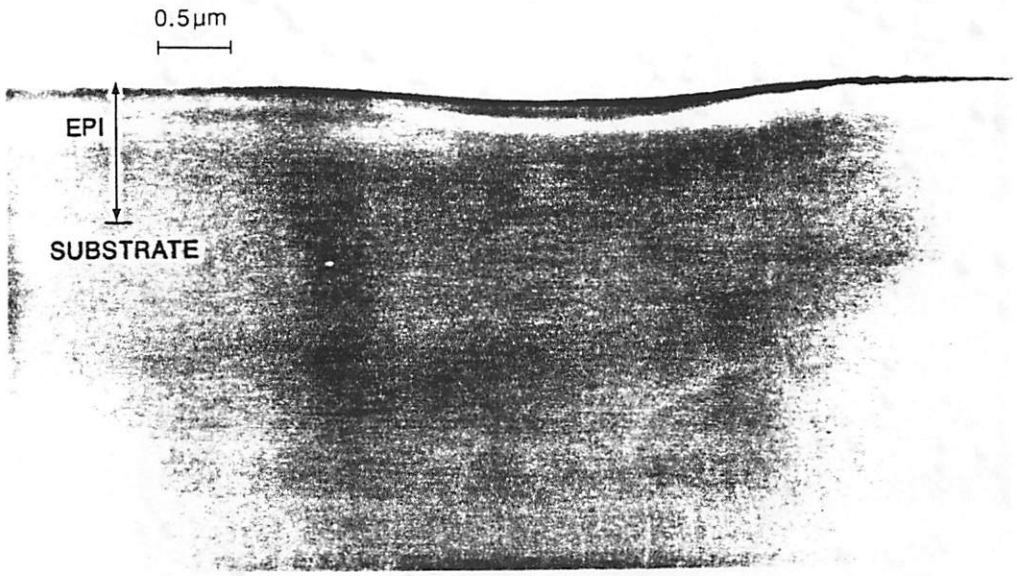


Fig. 11. The Nomarski surface micrographs(1000X) of the epilayer deposited at 900°C for 100 minutes. With increasing radius shallow pits are at a density of (a) $5x10^5/cm^2$, (b) $1.4x10^6/ cm^2$, (c) $>10^7/cm^2$.

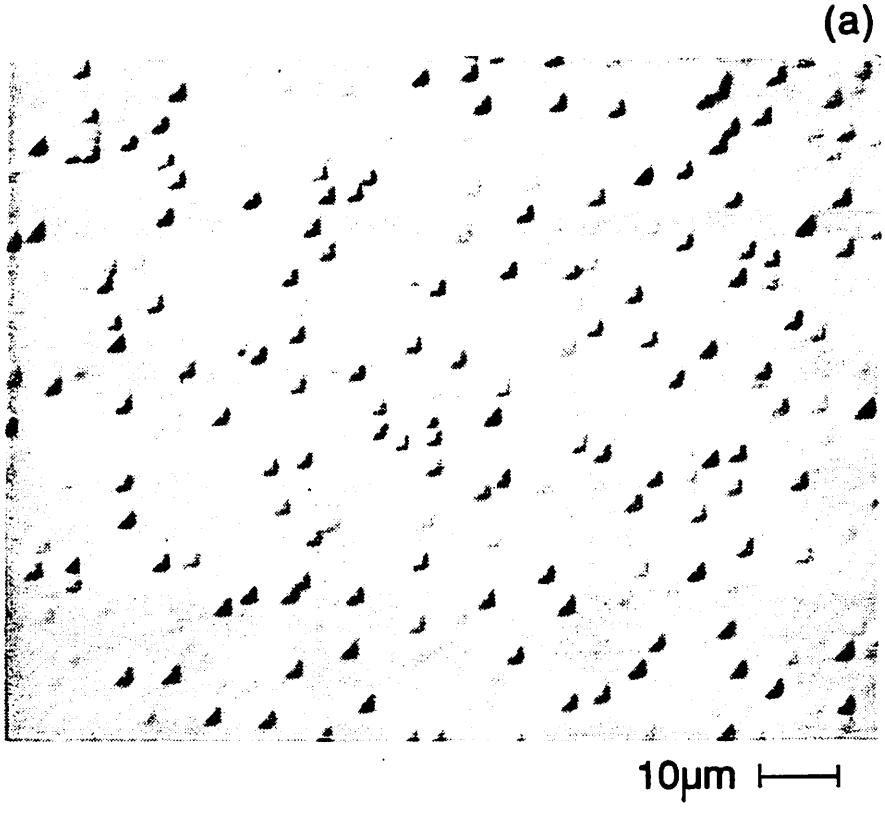


Fig. 11. (cont.)

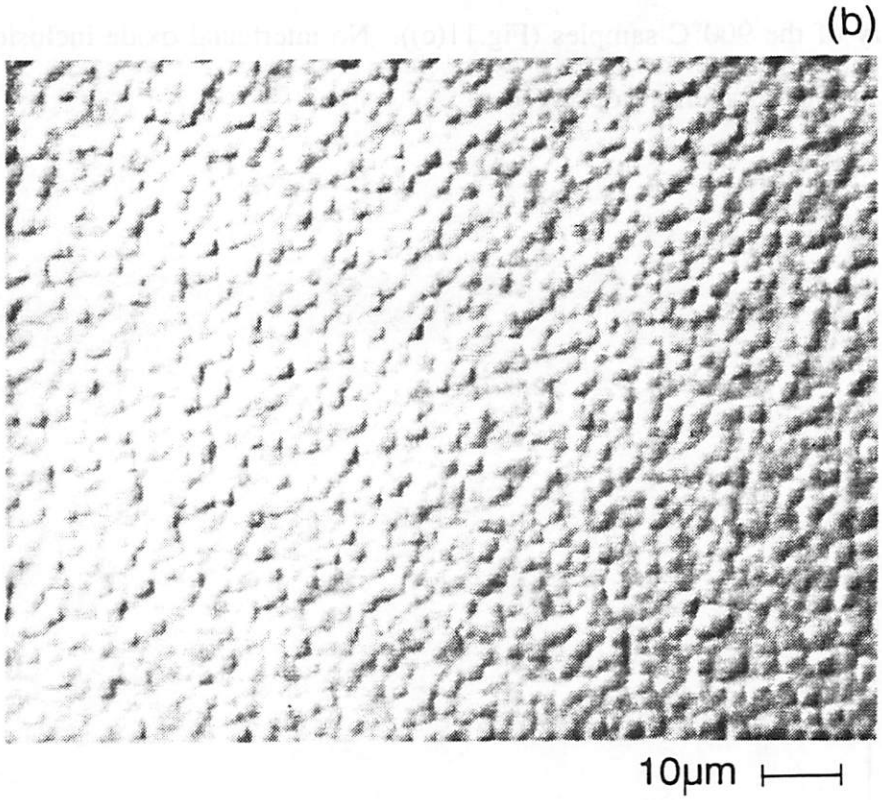


Fig. 12. An XTEM micrograph illustrating the rough surface morphology near the periphery of the 900°C samples (Fig.11(c)). No interfacial oxide inclusions or other defects in the epilayer are observed.

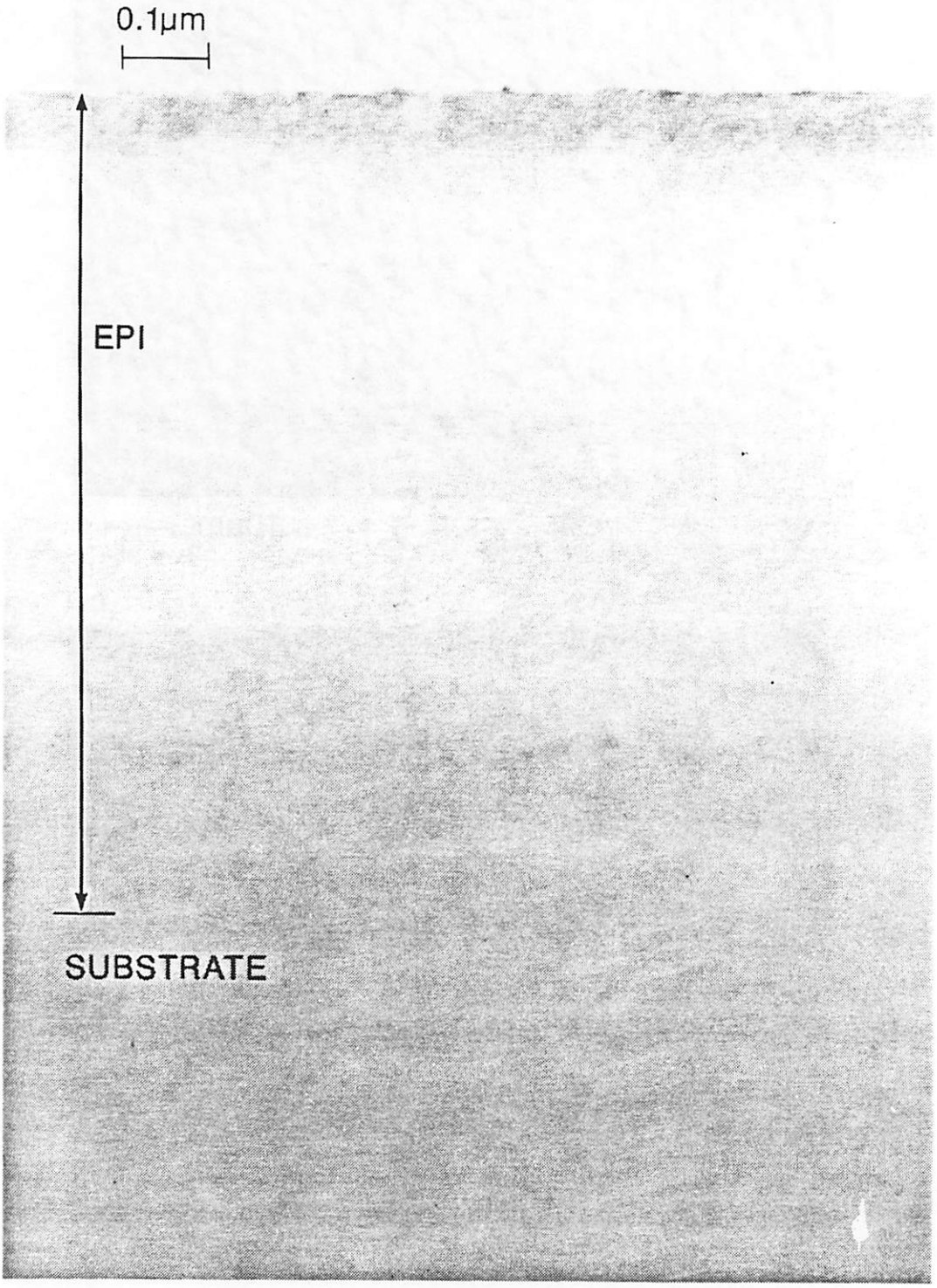


Fig. 13. Nomarski micrographs(500x) of oxygen implanted (20 Kev, 10^{14} ions/cm^2 and un-implanted areas of an epitaxial film grown at 850°C. (a) near the wafer center the epitaxial layer is defect-free, but shows a 0.04 um step between implanted and un-implanted areas. (b) Near the peripheral area of the wafer, in addition to the step, dense pits are observed on implanted areas, with specular surface on un-implanted areas.

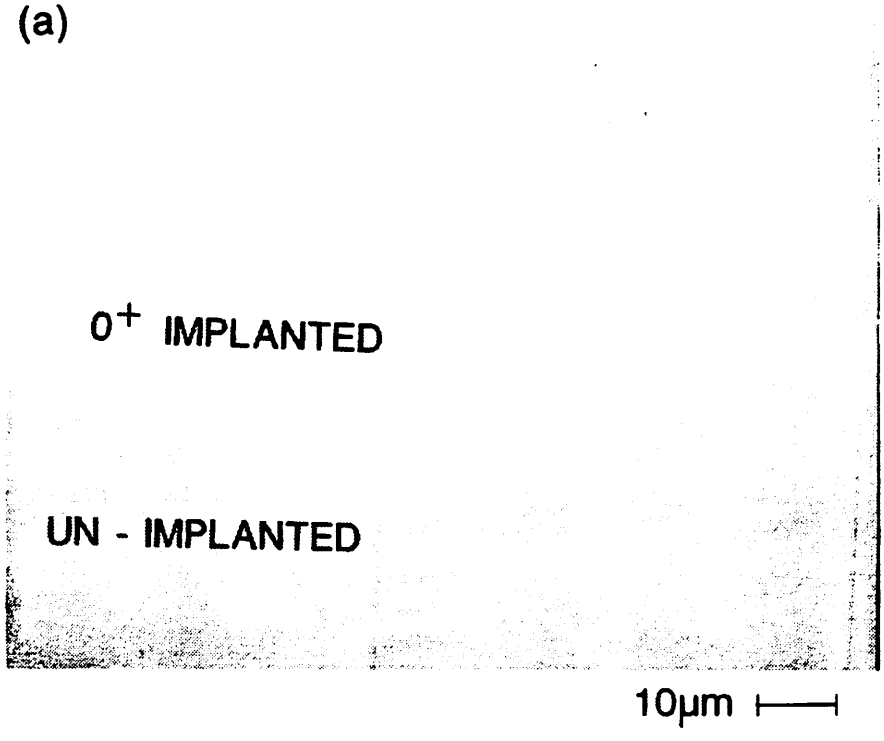


Fig. 13. (cont.)

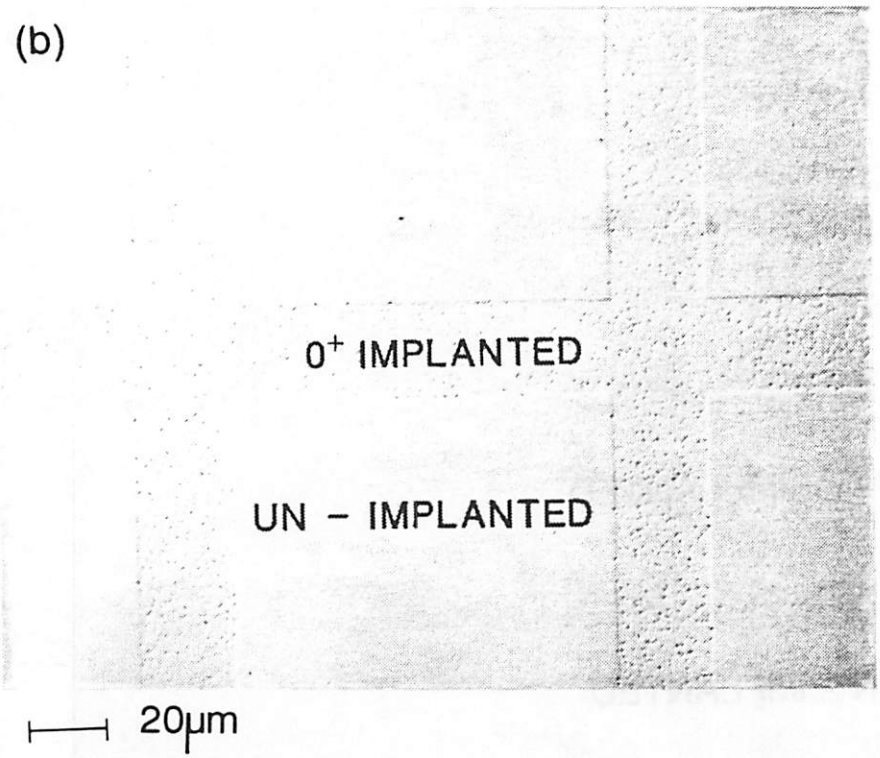
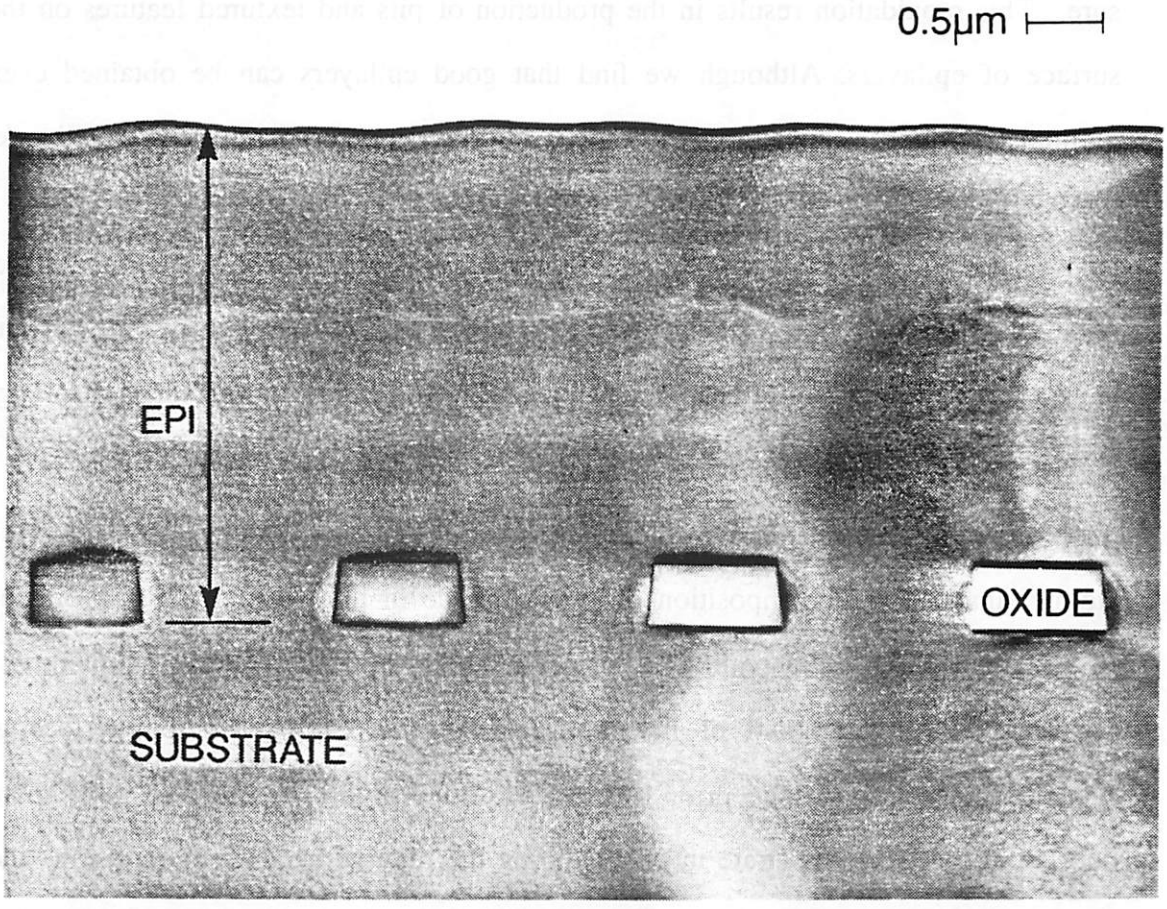


Fig. 14. The XTEM micrograph shows the high quality selectively overgrown silicon epilayer deposited on patterned silicon wafers at 850°C. The deposition duration is 10 hours. It shows the defect-free nature of the epitaxial Si film which completely covers a series of oxide lines(1 um lines and spaces).



Chapter 6

Future Studies

6.1 More Studies in Fluorine Incorporation

As stated in chapter 3, after the HF vapor treatment, the wafer surface is passivated by fluorine species resulting in Si-F bonds and hydrogen species resulting in Si-H bonds. Subsequently, water and oxygen in the air gradually replace passivating Si-F bonds to form Si-OH bonds and Si-O bonds during the air exposure. This reoxidation results in the production of pits and textured features on the surface of epilayers. Although we find that good epilayers can be obtained even with an 18 hour air exposure, a quantative description of the passivation is still unknown. Hence, X-ray photoelectron spectroscopy (XPS) can provide a quantitative analysis of the residual fluorine and hydrogen passivation after each air exposure. A study of passivation efficiency for HF vapor treated wafers stored in the inert gas (e. g., N_2) or in a vacuum chamber before the loading into the reactor is also suggested.

We introduce the fluorine incorporation model to explain how fluorine atoms enhance the decomposition of surface oxide in the thermal cycle. From the BF_2^+ and the F^+ ion implantation experiments in chapter 3, we believe that there is a minimum required amount of fluorine needed at the SiO_2/substrate interface to achieve a clean Si surface prior to the 850°C deposition. In order to keep more fluorine at the oxide/substrate interface during the thermal cycle, we propose to add fluorine gas (F_2) or nitrogen trifluoride (NF_3) in the reactor to suppress the outdiffusion of fluorine. This extra fluorine source may enhance the efficiency of surface oxide decomposition and increase the surface oxide removal at lower pre-

bake temperatures, to result in high quality epilayers at lower temperatures. We need to design a matrix experiment to determine the time to supply the fluorine related gas with a suitable flow rate in the thermal cycle. If fluorine does behave as a passivating agent, we believe this process can be widely used in the low temperature Si epitaxy and metal deposition. Also, the effect of the BF_2^+ and the F^+ ion implantation on patterned oxide areas is unknown. We should investigate this ion implantation experiment if it results in poly-Si on oxide areas.

6.2 Further Work in Plasma-Etch-Induced Effects

As noted in chapter 4, there are several unsolved issues which require further study. Without the sacrificial oxide growth, we find precipitates and dislocation loops at the epi/substrate interface. However, the detailed microstructure at the interface is unknown. The characteristics of these interfacial defects are unknown either. We suggest using high resolution TEM and electron energy loss spectroscopy to investigate them. Furthermore, studies concerning the effects of the high temperature prebakes on the formation of microtwins on (100) Si epilayers are needed. Although we show that a 5 nm thin sacrificial oxide can remove the plasma-etch-induced surface contaminants, we suggest trying a chemical oxide growth-and-etch step instead to achieve the same result.

6.3 Future Studies in Interfacial Oxide Islands

With an inadequate ex-situ and/or in-situ wafer cleaning process, we occassionally observe pits and/or textured features on the surface of epilayers. These abnormal surface features are interfacial oxide related. Based on the O^+ ion implantation, we believe that oxygen incorporation dissolved from interfacial oxide can locally suppress the Si growth rate and result in pits and textured features. We find that for 850°C grown epilayers each pit which shows low angle facets on the sur-

face is centered by an oxide island at the epi/substrate interface We suggest studying the local oxygen profile near the interfacial oxide island using electron energy loss sepctroscopy, to reveal the relationship between the oxygen profile and the epitaxial surface profile. Furthermore, both nitrogen and carbon ion implantation also result in reducing the Si growth rate. We need to study the effect of impurity incorporation on the Si growth rate. As shown in Fig. 1, the XTEM micrograph shows no defects near these overgrown interfacial oxide islands; however, we suggest using high resolution TEM technique to reveal the detailed microstructure and the lattice images around these areas. In addition, as stated in chapter 5, 900°C grown epilayers show no oxide islands at the epi/substrate interface even through pits or textured surface features are observed. The short-range profile of oxygen near these pits or textured features will have to be studied. The dissolved oxygen may form donors or deep levels below the conduction-band edge. We can use deep level transient spectroscopy (DLTS) to characterize these defect levels. Furthermore, we obtain large pits of uniform size (about 12 um) on the surface of epilayers deposited at 850°C for 16 hours. We need to use XTEM to inspect the oxide islands at the interface to see if the long duration can change their characteristics. Also, the electron energy loss spectroscopy should be employed to measure the oxygen profiles near the pit.

In the textured area, the high magnification XTEM micrograph in Fig. 2 illustrates a semi-continuous oxide multilayer at the epi/substrate interface, a high density of threading dislocation originating at the epi/substrate interface, and interfacial voids. The kinetic formtion of this interfacial oxide multilayer is unknown. We also observe some threading dislocations originating at voids. The voids could be generated by the decomposition of interfacial oxide layer during the deposition, or result from the coalesence of two misaligned growth fronts. Again, we need to use electron energy loss spectroscopy to identify the impurity distribution along

these dislocations and near voids. High resolution TEM must be employed to study the microstructure and the lattice images near these defects.

6.4 Selective Epitaxy Using N^+ Ion Implantation

We find that a high flux nitrogen ion implantation ($10^{15}/cm^2$) can form a nitride-like layer on the Si surface and inhibit the epitaxial growth. As shown in Fig. 3, the Nomarski micrograph illustrates a good selectivity of epitaxial growth between the implanted and un-impanted regions. Also, it shows no poly-Si nuclei on nitrogen implanted regions. We suggest using Auger electron spectroscopy (AES) to study the composition of nitrogen implanted layers. The effect of the thermal treatment duration and the temperature on the quality, the composition, and the selectivity of the nitride-like layer should be studied. High resolution TEM should be employed to study the interface between the epilayer and the nitride-like layer.

6.5 Substrate Orientation Effects

Selective epitaxial growth on (111) and (110) substrates needs more work. Under the same growth conditions, we can achieve high quality epilayers on (100) Si substrates at 850°C; however, we obtain faceted growth on (111) and (110) substrates. As shown in Fig. 4, the surface morphology of epilayers deposited at 850°C on (111) substrates is terraced. We observe many pyramidal features with three-fold symmetry, where the sides are concave-in, on the epilayers. Some pyramidal features show oxide debris on the bottom. We cannot avoid the formation of these surface features until we raise the deposition temperature to 1000°C. In Fig. 5 we observe specular epilayer with rough edges due to the H_2 undercutting effect at 1000°C. We also observe a large facet. The characteristics of this facet is unknown. In addition, the surface morphology of epilayers deposited on 4° off axis (111) sub-

strates is improved. Smaller surface features (pits) are still observed on 850°C and 900°C deposited epilayers. Likewise, a specular surface is observed with rough edges for 1000°C deposited epilayers. Epitaxial growth on (110) substrates also shows similar results. As illustrated in Fig.6, there are a lot of concave surface features (two-fold symmetry) on 850°C and 900°C deposited epilayers. Again, for 1000°C deposition we also obtain specular epilayers with rough edges. The origin and the characteristics of these surface features are unknown. However, it is obviously deposition temperature dependent. Based on these observation, we will have to use SIMS and XTEM to identify these surface features, then study the kinetics of the formation of these surface features on different substrates. Also, the kinetics of selective epitaxial growth on different oriented substrates at different temperatures must be investigated.

6.6 Raman Scattering Spectroscopy Measurements

Another area to be studied is the residual stress distribution at the interface between the patterned oxide and the epilayer. The thermal expansion coefficient for the oxide and the silicon is 5×10^{-7}/°K and 2.8×10^{-6}/°K, respectively. The deposition temperature is between 800°C to 1000°C. As a result, there is a residual compressive stress between the patterned oxide and the epilayer at room temperature. This residual compressive stress may cause some microstructure defects in epilayers. The residual stress is not uniform. Therefore, the effects due to the deposition temperture, the temperature ramping rate, the size of epitaxial window, the thickness of epilayers, the thickness of patterned oxide layer, the sidewall direction of patterns, the space between patterns, and the density of patterns on the residual compressive stress should be investigated. Details of stress effects can be revealed by Raman scattering spectroscopy. For example, as shown in Fig. 7, the Raman scattering spectroscopy on the side of Si epilayer indicates a 0.83 λ^{-1} shift near the edge of

the epi/oxide pattern interface. This residul compressive stress can be estimated as 2.07×10^8 N/m^2.

6.7 The Formation and the Annihilation of Facets

We obtain {110} and {111} facets along the <100> and the <110> sidewalls on (100) Si substrates, respectively. Also, we obtain {111} facets at corners of deposition windows with <100> sidewalls. These facets may not only initiate defects but also may complicate the fabrication of integrated circuits, and then demote the advantages of the selective epitaxial growth. For that reason, we have to study the facet causing mechanisms during the selective epitaxial growth of silicon, and modify the processing factors to suppress facet formation.

6.8 The Formation and the Annihilation of Microtwins

It is found in the SEG of Si that with [100] sidewall, microtwin-free epi-layer can be achieved on (100) Si substrates. With [110] sidewall; on the other hand, microtwins are observed near the edges of epilayers. It seems trivial to explain the formation of microtwins near [110] sidewalls because the {111} facets near edges can initiate microtwins. However, as illustrated in Fig. 8, we recently obtain microtwin-free epilayers near edges of [110] sidewalls. From the macros-tructural point of view, we understand that once the {111} facets form, there is a large possibility of yielding microtwins on these {111} facet planes. But, from the microstructural point of view, we do not know which factors motivate this structure change to achieve the microtwins. We therefore have to investigate the detailed kinetics of microtwins formation and microtwin-free epilayers near edges of [110] sidewalls on (100) silicon substrates. With this information, we can modify the process to suppress the formation of microtwins.

6.9 Future Work in Selective Epitaxial Overgrowth

Fig. 9 indicates a rough interface between the overgrown epilayer and the patterned oxide layer. It seems that the overgrowth of Si etches a very thin oxide layer, and which results in an unlevel oxide surface. We hypothesize that there is a weak H_2 undercutting effect at the interface. High resolution XTEM will be employed to reveal the microstructure at the overgrown epi/oxide interface and to see if microdefects are there.

Finally, the lateral growth rate of Si on patterned oxide layer will have to be studied. A higher lateral growth rate can achieve overgrown epilayers on patterned oxide earlier. The growth temperture, the pressure, the flow rate of Si source gas, and the Si/oxide ratio on substrates can significantly influence the lateral overgrowth rate of Si along each direction. All these parameters should be determined to understand the kinetics of the lateral overgrowth. Also, coalescence of two growth fronts together to form an overgrown epilayer on oxide films is of importance for silicon-on-insulator (SOI) applications. The main issue concerns the alignment of the two growth fronts to avoid seams, strain induced defects (dislocations and microtwins), and void annihilation. We need to know these detailed kinetics.

Fig. 1. The XTEM micrograph of an interfacial oxide island in which the oxide thickness is 7 nm and the dimension of this island is 1000 nm. We observe a strain-field-induced dark band above this oxide island.

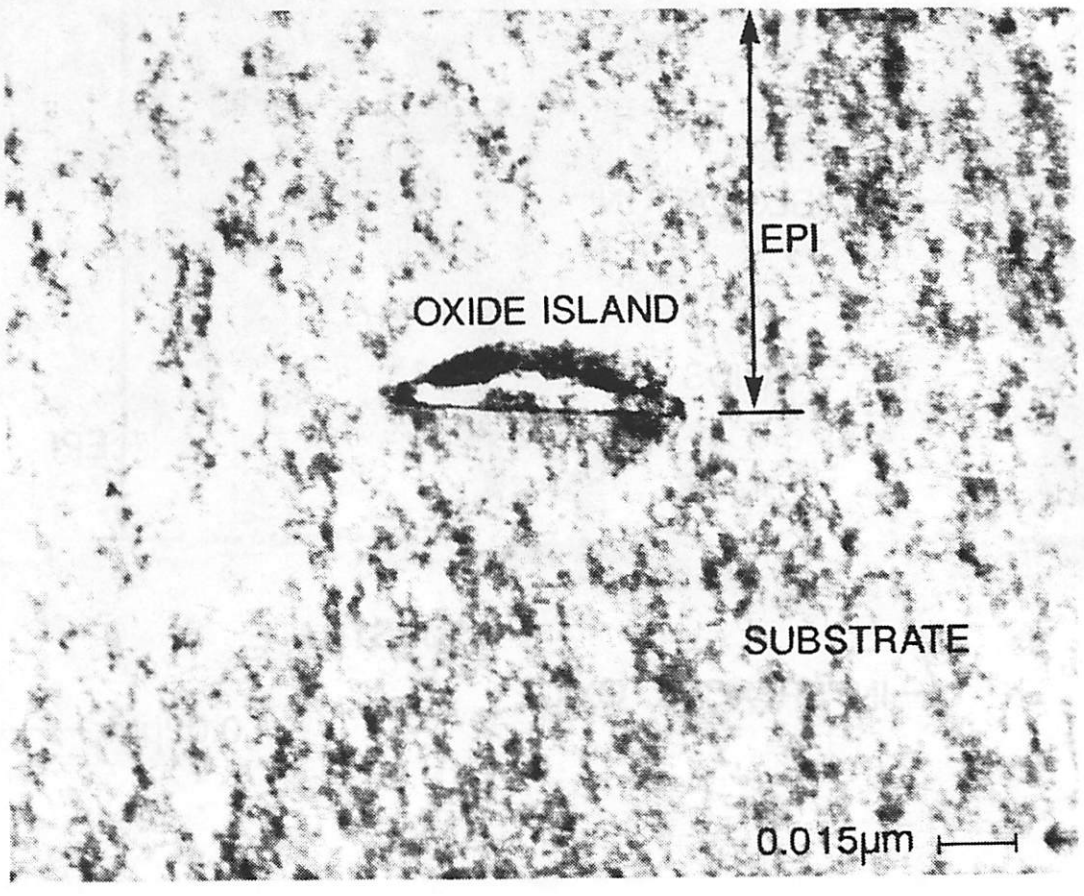


Fig. 2. the XTEM micrograph of a semi-continuous interfacial oxide layer. We observe threading dislocations in the epilayer, voids and multi thin oxide layers at the epi/substrate interface.

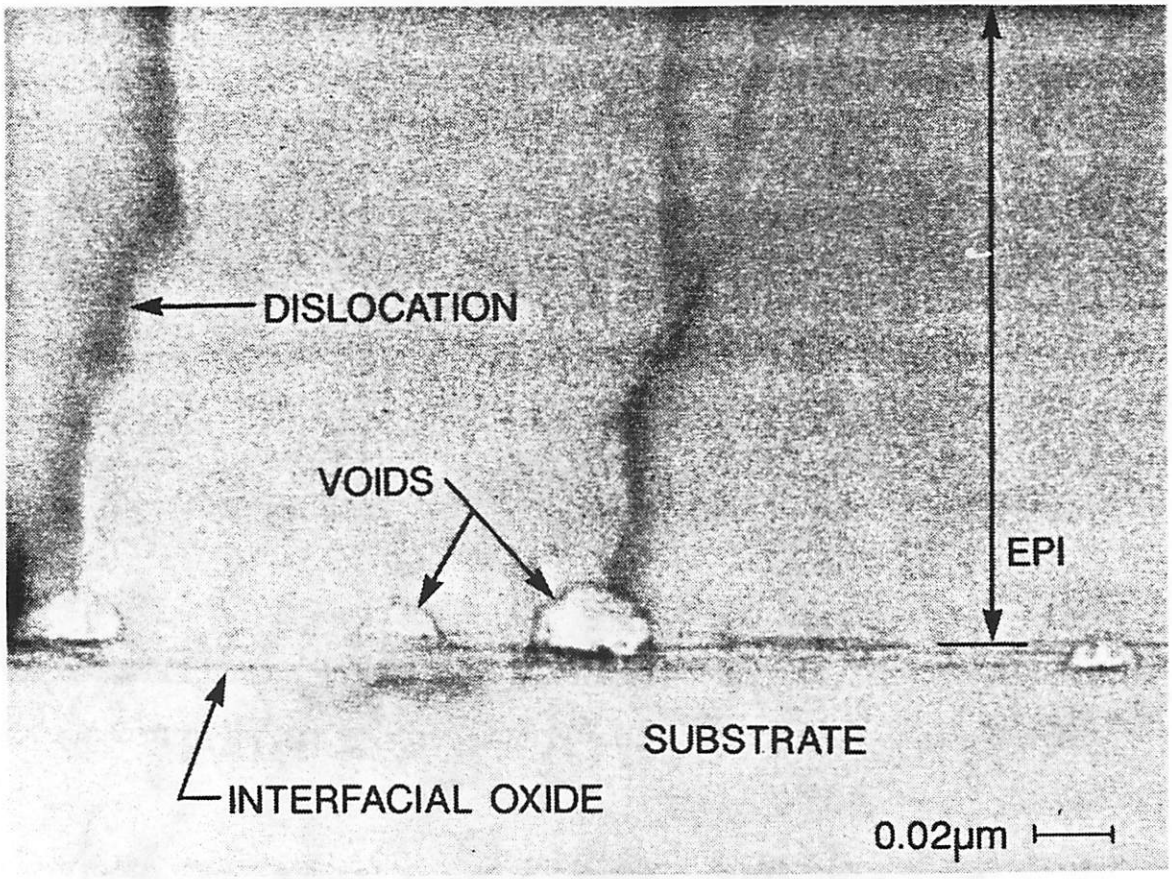


Fig. 3. The Nomarski micrograph (1000X) shows a selectively grown epilayer with a specular surface morphology and smooth edges. We observe no poly-Si nuclei on N^+ ion ($10^{15}/cm^2$) implanted areas.

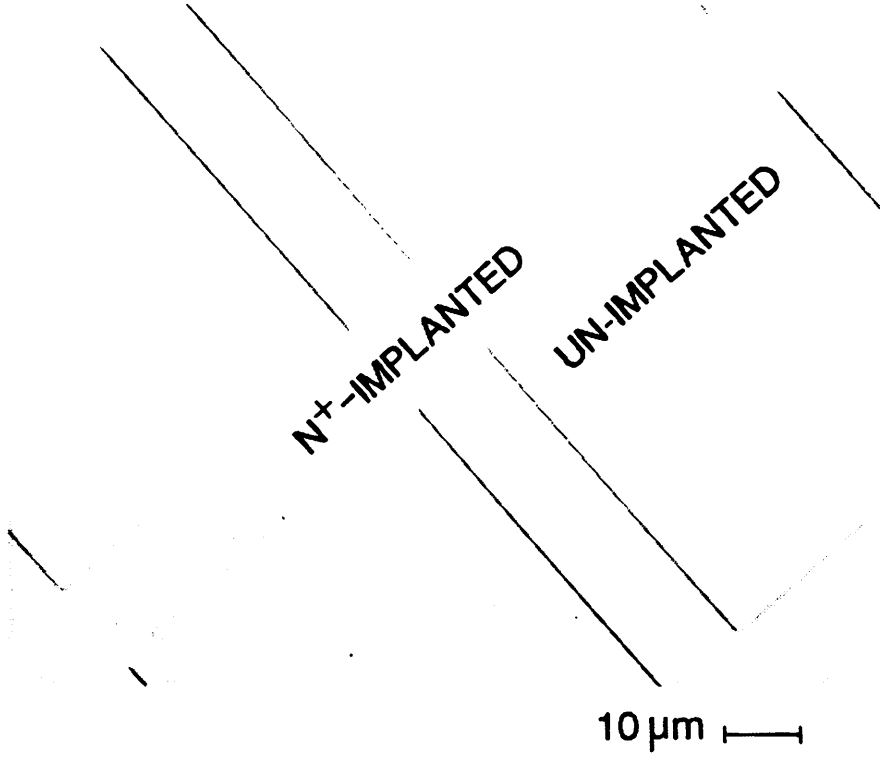


Fig. 4. The Nomarski micrograph (500X) illustrates many pyramidal features on the terraced epilayer deposited at 850°C on (111) Si substrates.

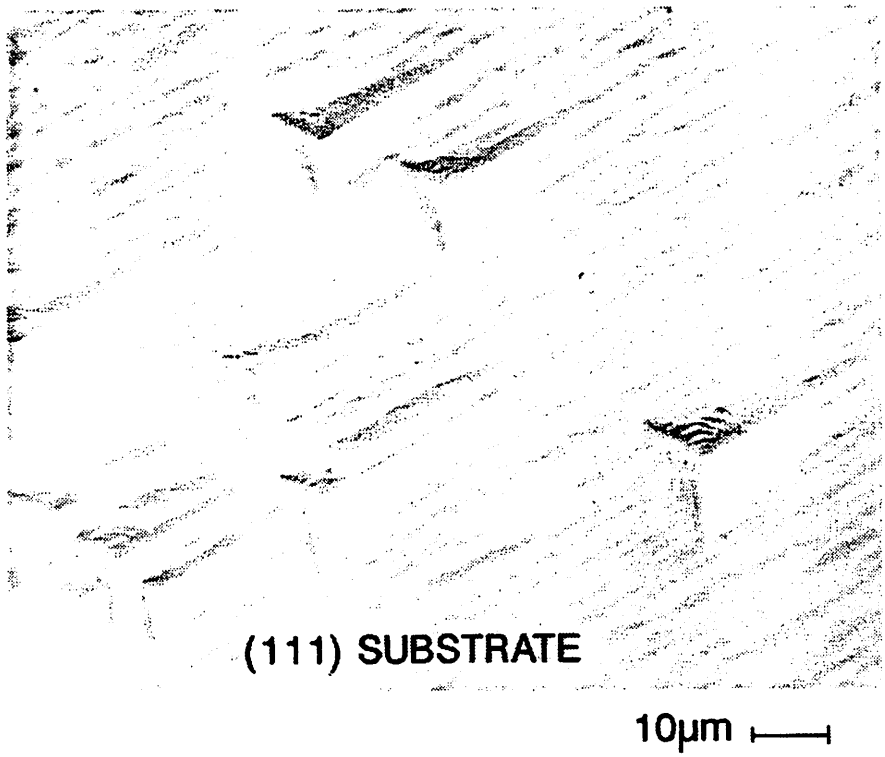


Fig. 5(a). The Nomarski micrograph (1000X) shows a specular epilayer with rough edges. This epilayer is deposited at 1000°C on (111) Si substrate. The sidewalls are along <100> directions.

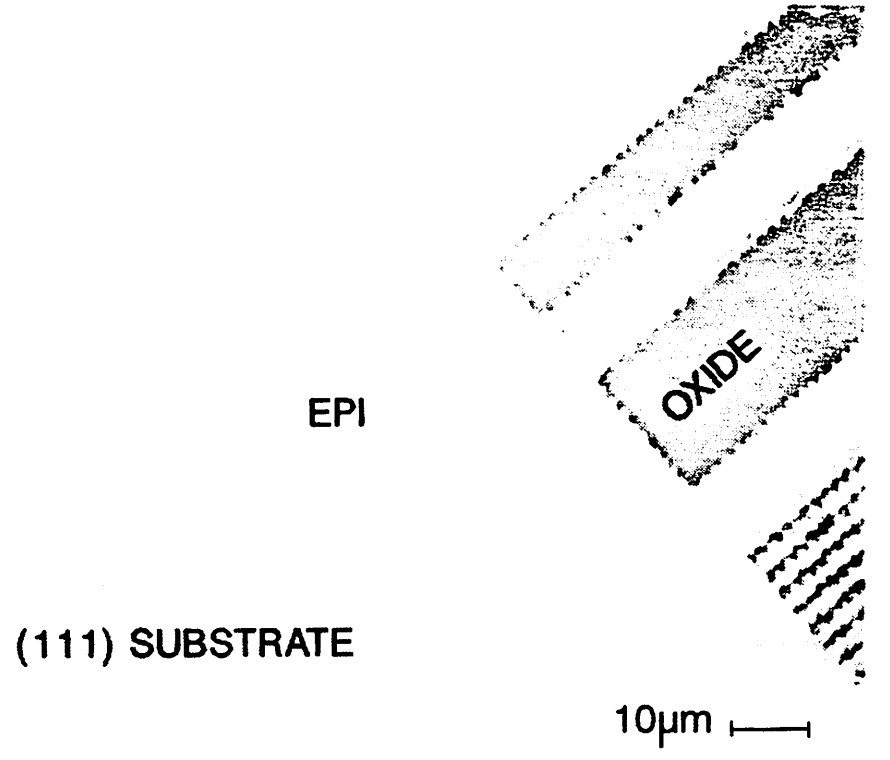


Fig. 5(b). On the same substrate, with <110> sidewalls the Nomarski micrograph show epilayers and an unknown facet.

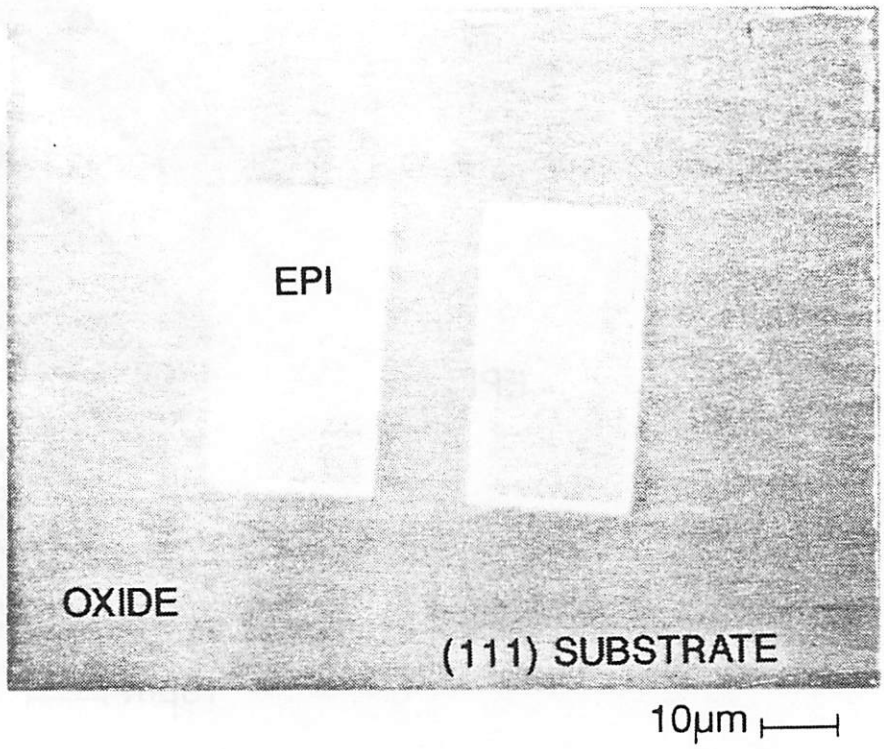
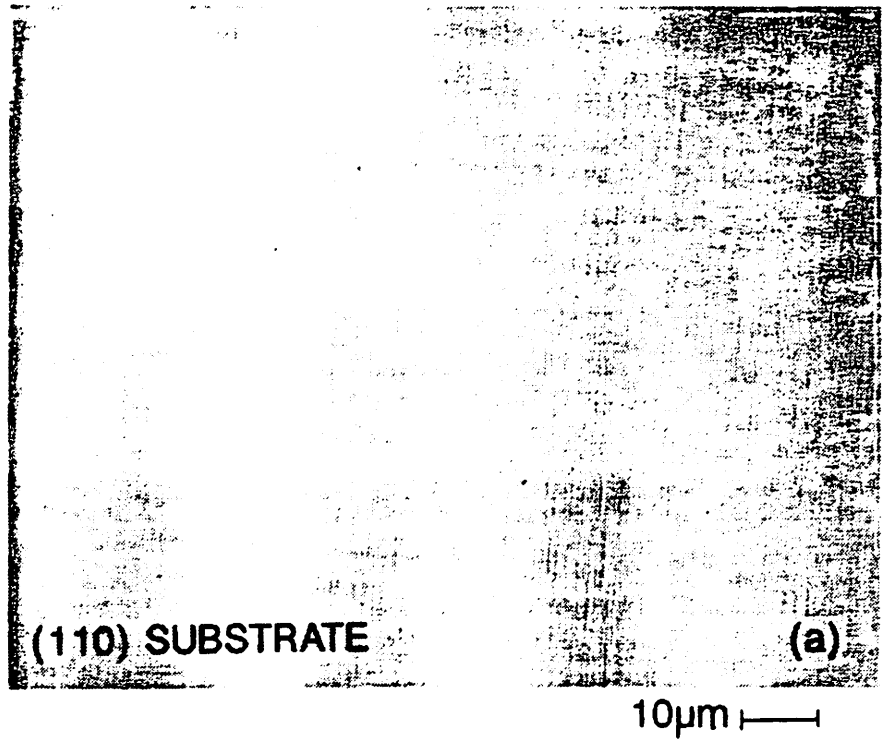


Fig. 6. Nomarski micrographs (500X) of epilayers deposited on (110) substrates. There are many two-fold surface features on epilayers. (a) Deposition temperature: 850°C. (b) Deposition temperature: 900°C.



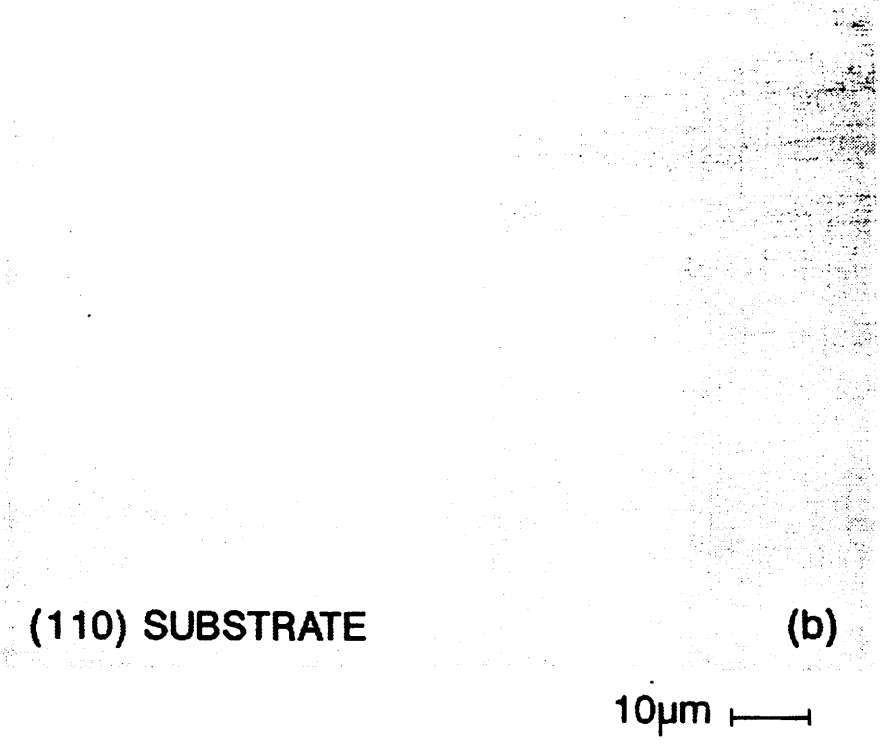


Fig. 7. The Raman scattering spectrum indicates a 0.83 λ^{-1} shift resulting from the residual compressive stress near the edge of the epi/oxide pattern interface.

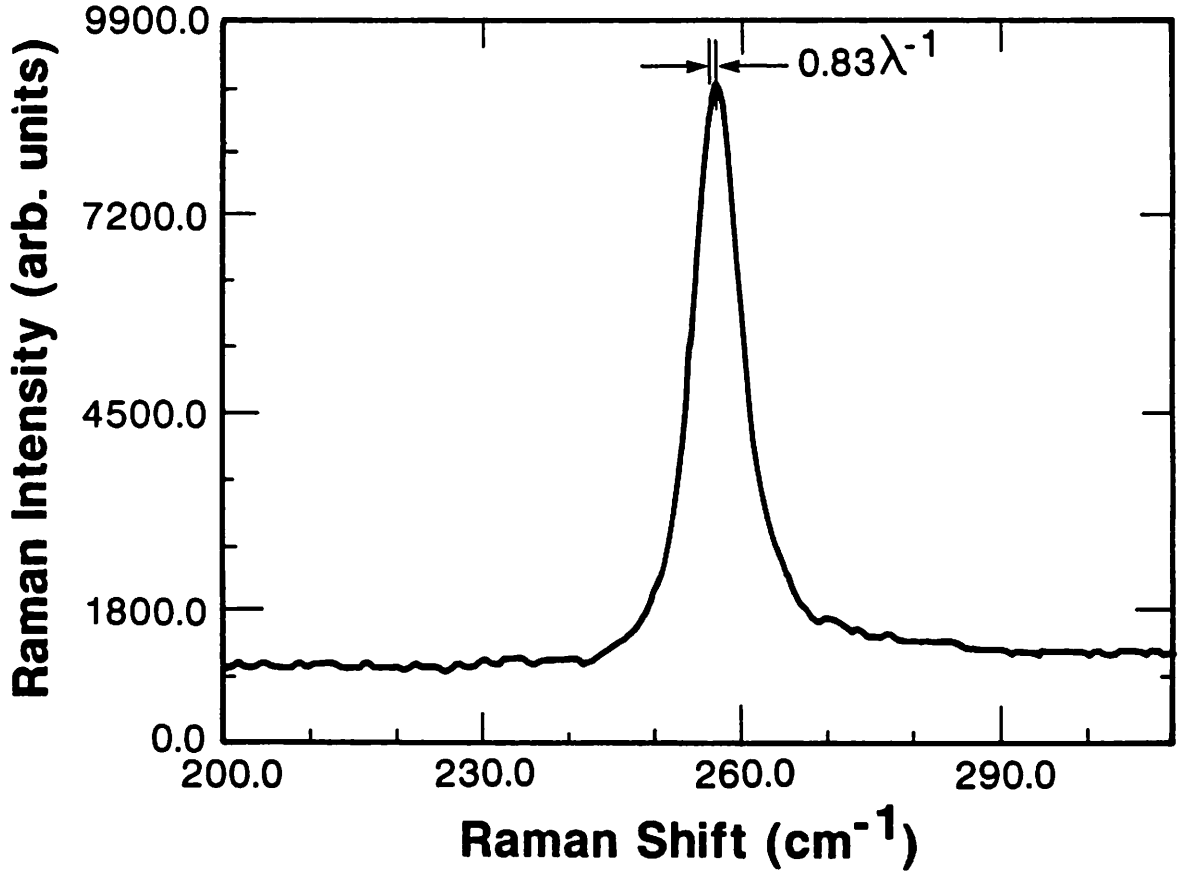


Fig. 8(a). A XTEM micrograph of the epilayer deposited at 850°C. With <110> sidewalls, it shows microtwins near the edge of epi/oxide pattern.

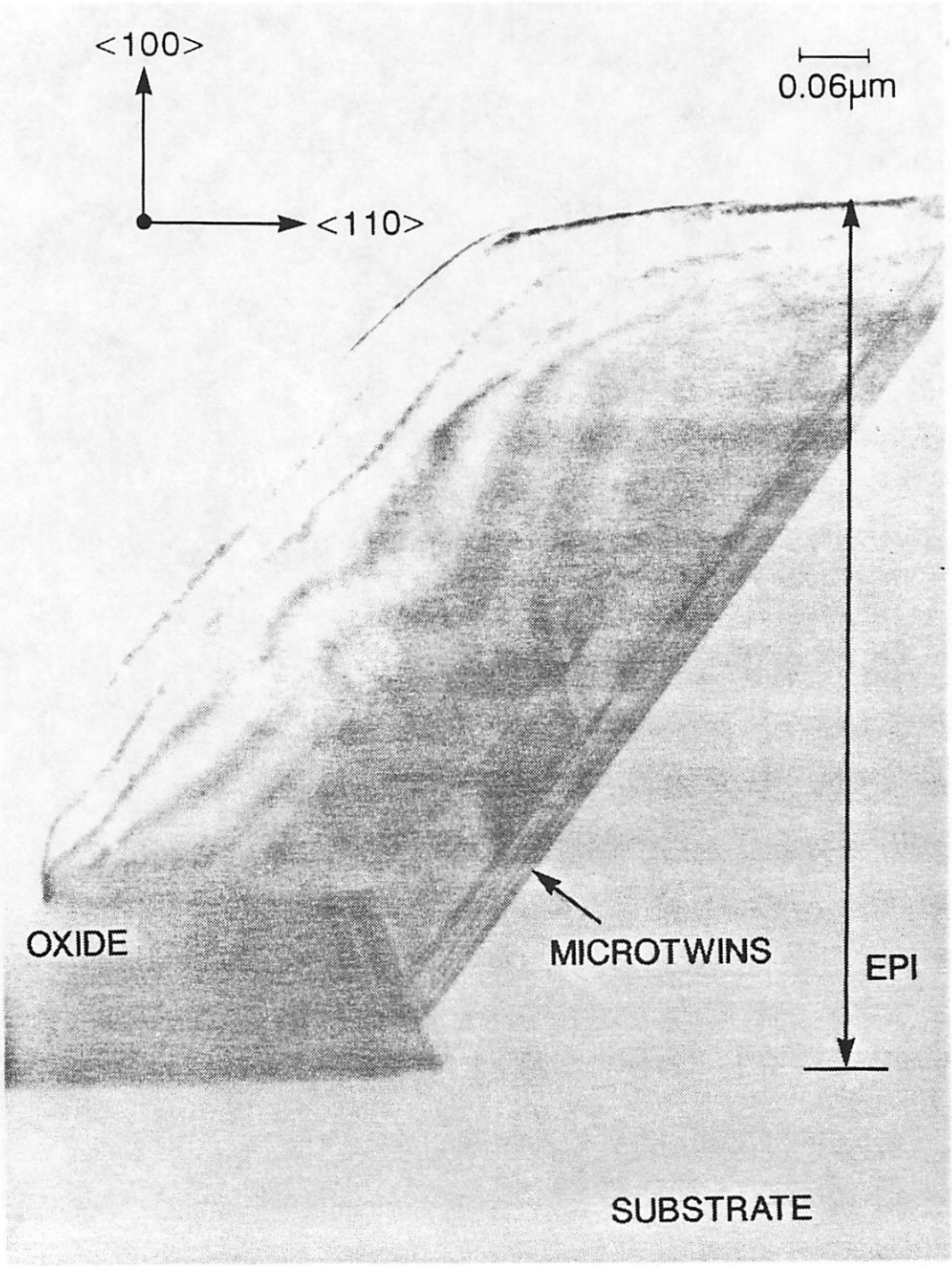


Fig. 8(b). The diffraction pattern of the specimen in Fig. 8(a) clearly indicates that twin spots occurs on {111} planes at 1/3 $n\vec{g}$ in <111> directions.

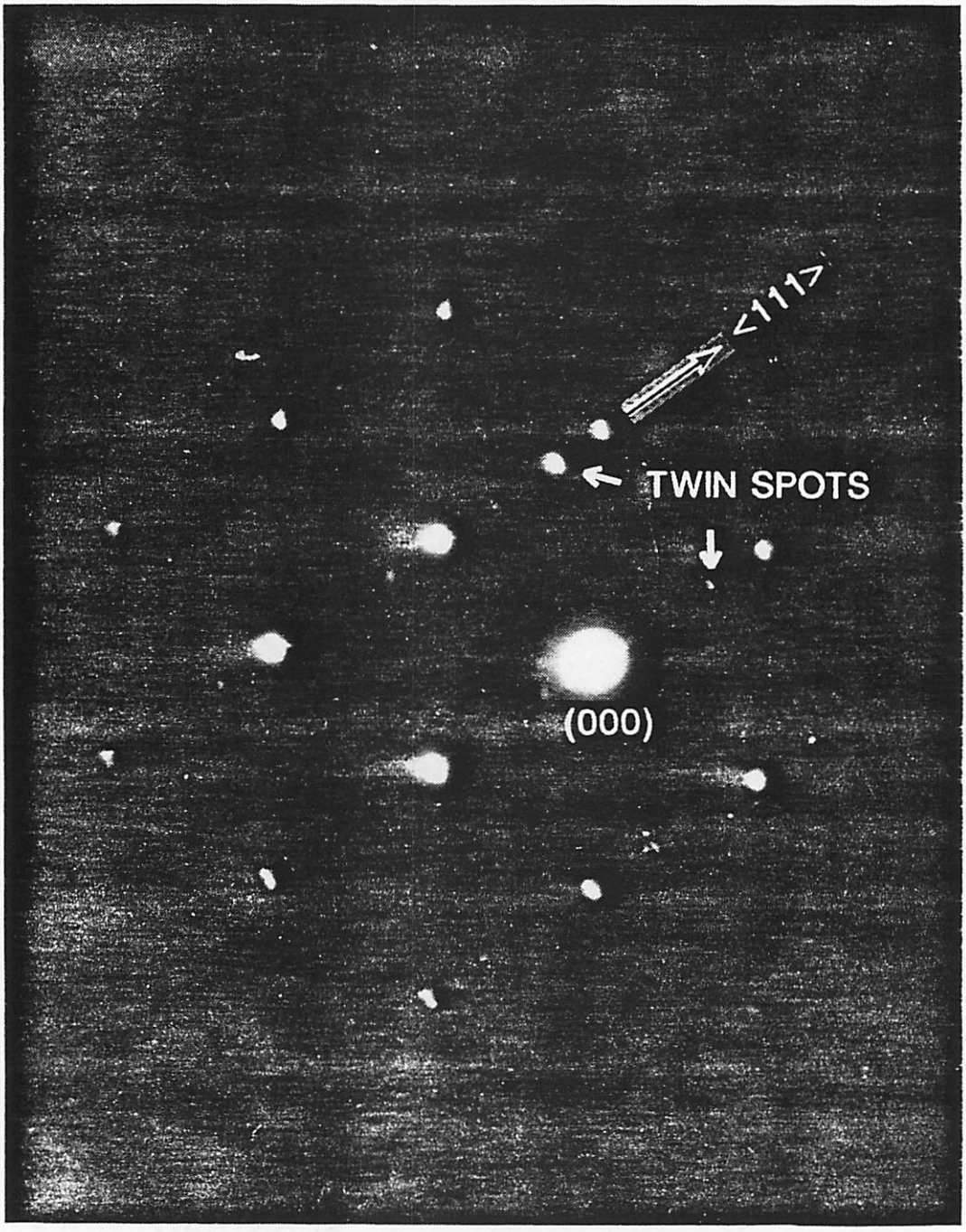


Fig. 8(c). The XTEM micrograph shows no microtwins in the epilayer deposited at 850°C with <110> sidewalls.

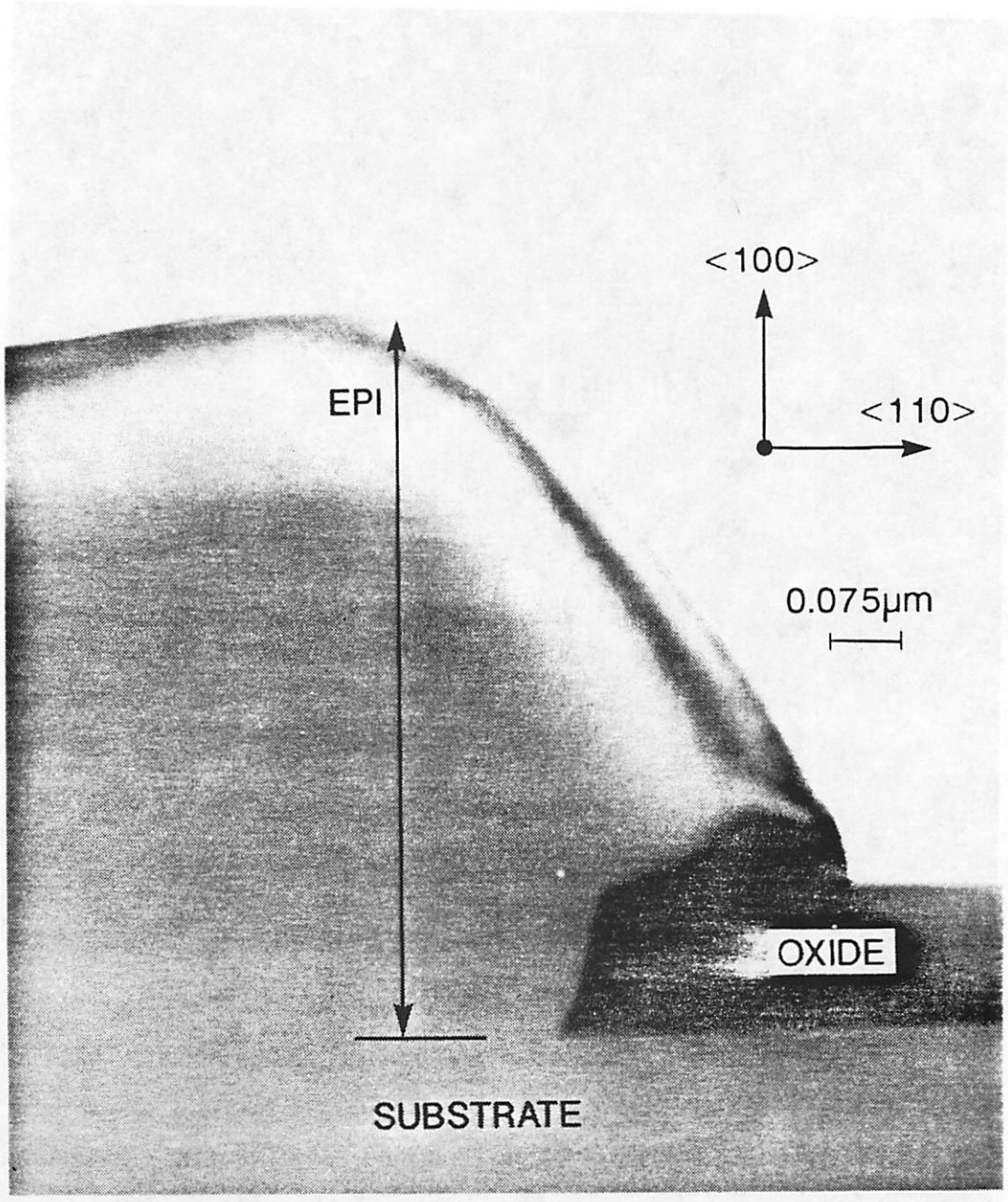


Fig. 8(d). The diffraction pattern of the specimen in Fig. 8(c) reveals no twin spots.

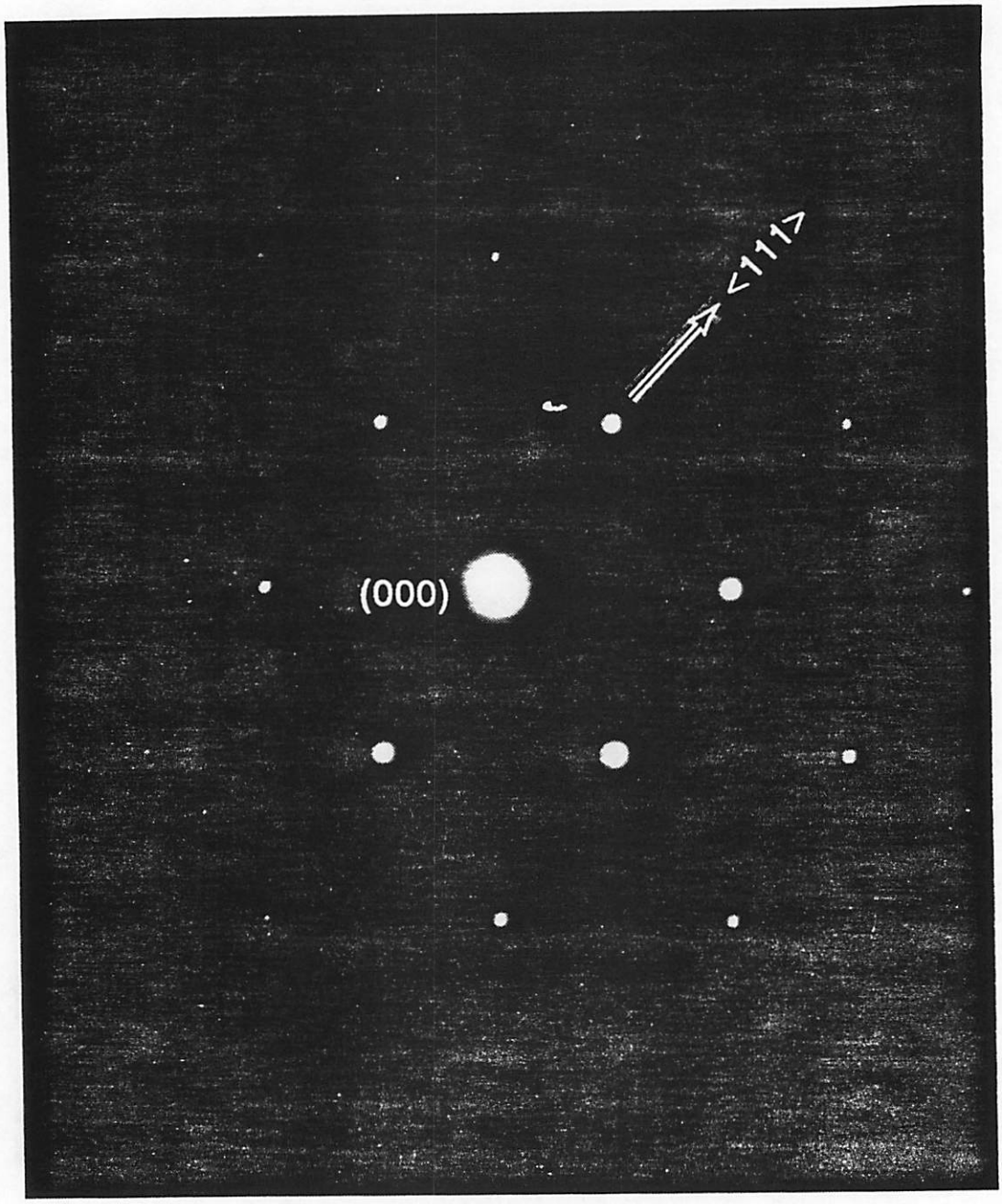
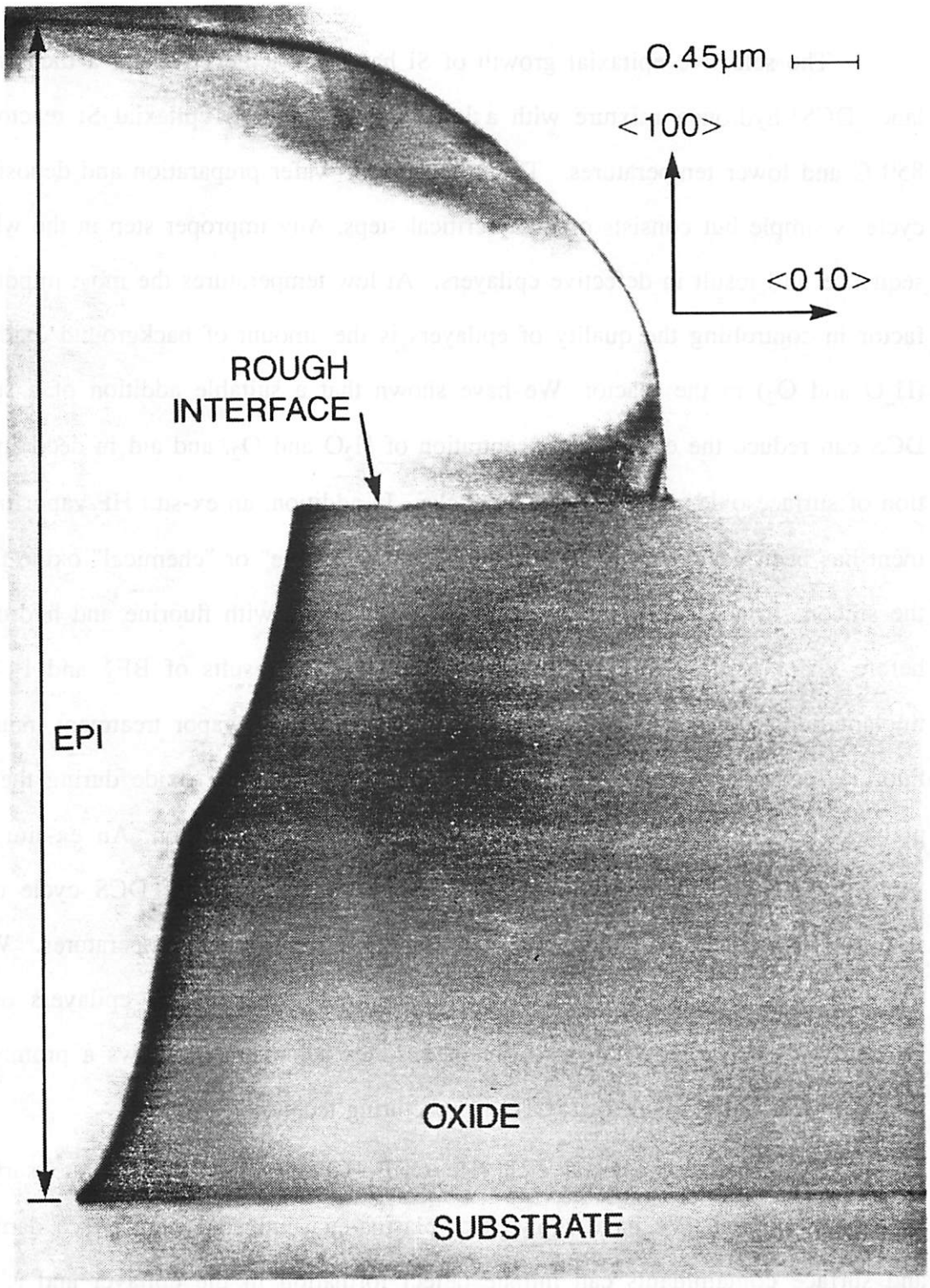


Fig. 9. A XTEM micrograph shows a partially overgrown epilayer. It illustrates a slightly rough interface between the overgrown epilayer and the patterned oxide layer.



Chapter 7

Conclusion

The selective epitaxial growth of Si has been achieved using a dichlorosilane (DCS)-hydrogen mixture with a low-pressure hot-wall epitaxial Si reactor at 850°C and lower temperatures. The procedure of wafer preparation and deposition cycle is simple but consists of many critical steps. Any improper step in the whole sequence will result in defective epilayers. At low temperatures the most important factor in controlling the quality of epilayers is the amount of background oxidants (H_2O and O_2) in the reactor. We have shown that a suitable addition of a small DCS can reduce the effective concentration of H_2O and O_2, and aid in decomposition of surface oxide during the H_2 prebake. In addition, an ex-situ HF vapor treatment has been developed to successfully remove "native" or "chemical" oxide from the silicon surface and to passivate the silicon surface with fluorine and hydrogen before wafer loading into the reactor. Based on the results of BF_2^+ and F^+ ion implantation experiments, we propose that the ex-situ HF vapor treatment induced fluorine incorporation enhances the decomposition of surface oxide during the H_2 prebake, and leads to a clean Si surface prior to the deposition. An ex-situ HF vapor treatment combined with an in-situ low concentration of DCS cycle consistently results in high quality epilayers at 850°C and lower temperatures. With the extension of deposition duration, specular and defect-free Si epilayers overgrown on oxide patterns are also obtained. This achievement shows a promising future for silicon-on-insulator (SOI) manufacturing technology.

The effects of plasma etch ($He+CHF_3+CF_4$) on the Si substrate surface have been studied. We have shown that plasma-etch-induced near-surface damage and surface contaminants can initiate defect formation in the epilayer and at the

epi/substrate interface. We found that a 5 nm 900°C grown sacrificial oxide is adequate to completely remove plasma-etch-induced surface damage and contaminants after a HF dip. Furthermore, a cycled plasma etch can avoid the thick polymer accumulation near edges of substrate/oxide patterns. With this modified plasma etch step, a thin sacrificial oxide growth, and an oxide removal step, defect-free epilayers are obtained.

Improper wafer preparation and deposition cycles can result in defective epilayers with pits and/or textured structures. We have found that these abnormal surface features are related to the oxide islands at the epi/substrate interface. With O^+ ion implantation experiments, we found that the oxygen incorporation in the Si epilayer reduces the Si growth rate. As a result, we attribute the formation of these surface features to the local depression of the Si growth rate resulting from the dissolution of interfacial oxides.