PLASMA IMMERSION ION IMPLANTATION (PIII) FOR INTEGRATED CIRCUIT MANUFACTURING; THIRD QUARTERLY PROGRESS REPORT

by

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

Third Quarterly Progress Report
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PLASMA IMMERSION ION IMPLANTATION (PIII) FOR INTEGRATED CIRCUIT MANUFACTURING

CCTP Contract #C90-071

Applied Materials Inc.

Project Managers:	N. W. Cheung, UCB M. A. Lieberman, UCB
Product Manager:	W. J. Wriggins, Applied Materials
Program Manager:	P. R. Klein, CA Office of Competitive Technology

FINANCIAL REVIEW

CompTech Program
Plasma Immersion Ion Implantation for Integrated Circuit Processing
Grant No. C90-071
Third Quarterly Report
June 18, 1991 - September 17, 1991

Participant	To Date Planned	To Date Actual	Percent Actual of Planned	This Quarter Planned	This Quarter Actual	Percent Actual of Planned	Next Quarter Planned
CompTech	104,859	155,118	1.47	37,605	50,259	1.33	35,141
Applied Materials							
Cash	42,768	61,067	1.42	12,989	18,299	1.40	27,234
In-kind	11,250	8,000	.71	3,750	4,000	1.06	3,750

The amounts include indirect costs.

PERSONNEL

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M.A. Lieberman	Project Manager	UCB
W.J. Wriggins	Product Manager	Applied Materials
P.R. Klein	Program Manager	OCT
R.A. Stewart	Postdoctoral Research	UCB
C.A. Pico	Postdoctoral Research	UCB
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M.H. Kiang	Graduate Student	UCB
C. Yu	Graduate Student	UCB
V. Vahedi	Graduate Student	UCB
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J. Benasso	Technician	UCB

Collaboration with Other Research Groups

Dr. Ian Brown	Research Scientist	Lawrence Berkeley Lab
Dr. Kin-Man Yu	Research Scientist	Lawrence Berkeley Lab
Dr. Andy Keenan	Research Manager	Prometrix Inc.

PROJECT REVIEW

I INTRODUCTION

Ion implantation is an important technique in integrated circuit fabrication. Due to the continuing trend toward smaller, faster and more densely packed circuitry, conventional ion implantation technology faces several challenges. Two major challenges are throughput, which is limited by the available ion current, and the production of very low energy ion beams for shallow implants. Other important concerns include charging, channeling, shadowing and damage.

An alternative to conventional ion implantation that may eliminate several of the above problems is *plasma immersion ion implantation* (PIII). We have successfully applied PIII to semiconductor device fabrication for a number of VLSI applications including sub–100 nm p+/n junction formation, conformal implantation for trench doping, and palladium seeding for electroless Cu plating. The PIII process is illustrated in Figs. 1 and 2, and a perspective is given in Appendix A.

Ions that are created in an electron cyclotron resonance (ECR) plasma source, diffuse into a process chamber where they are extracted directly from the process plasma in which the wafer holder is located (Fig. 1). The substrate holder is biased to a high negative voltage (either pulsed or DC) and the ions are accelerated to the wafer through a high-voltage plasma sheath (Figs. 2a, 2b). Since the ion energy is controlled by the applied voltage, very low energy implants ($\leq$ 1 keV) are possible. In addition, since PIII operates with an ECR plasma discharge, a range of pressures from 0.1–100 mTorr may be used. Thus, the angular distribution of the implanted ions can be adjusted by varying the gas pressure. This feature is very attractive for conformal doping of nonplanar surface topographies such as high-aspect-ratio trenches.

PIII can also operate in a triode (Fig. 2c) mode by introducing a sputtering target near to or within the ECR source chamber. The sputtering rate can be controlled by applying a suitable bias to the target. This technique provides the capacity of implanting any solid material into the substrate as long as the material has reasonable sputtering and ionization rates. In addition, dual ion implantations of both the source and sputtered atomic species can be achieved by varying the target and wafer holder

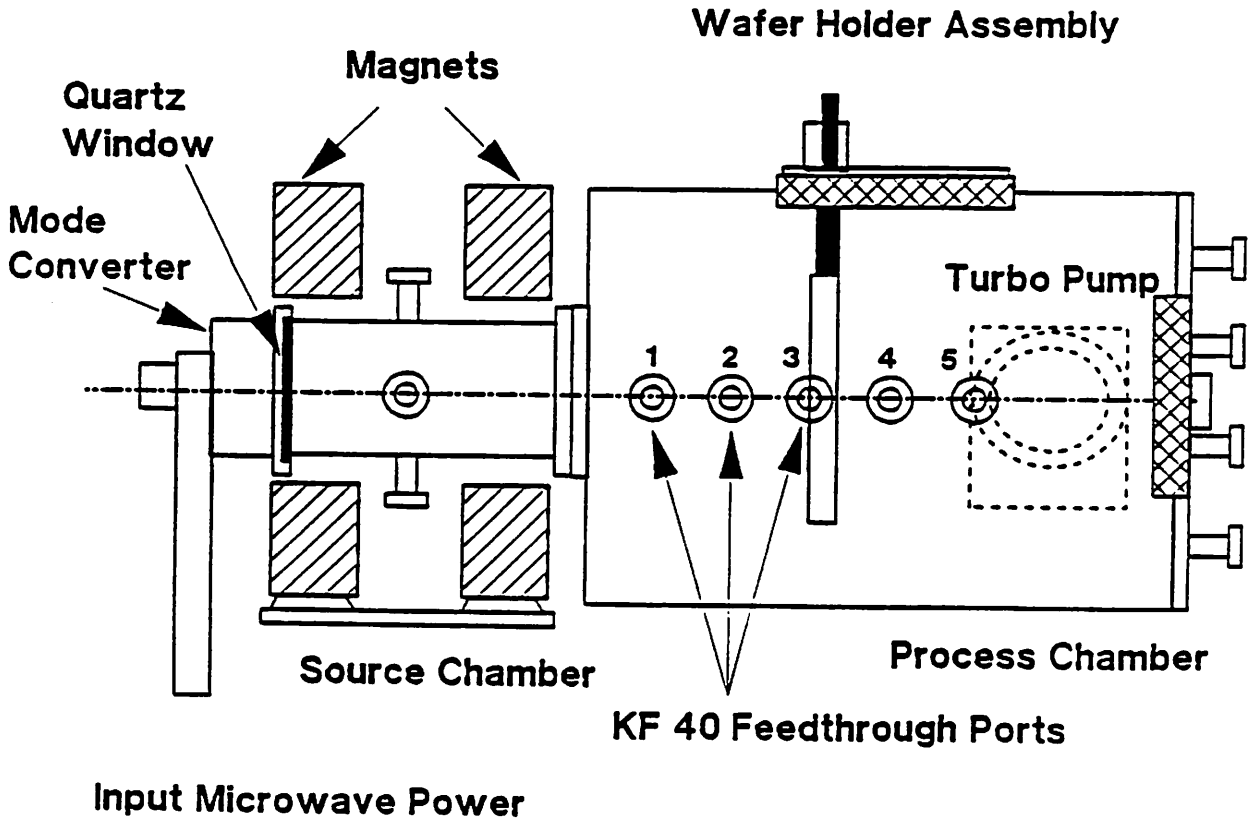
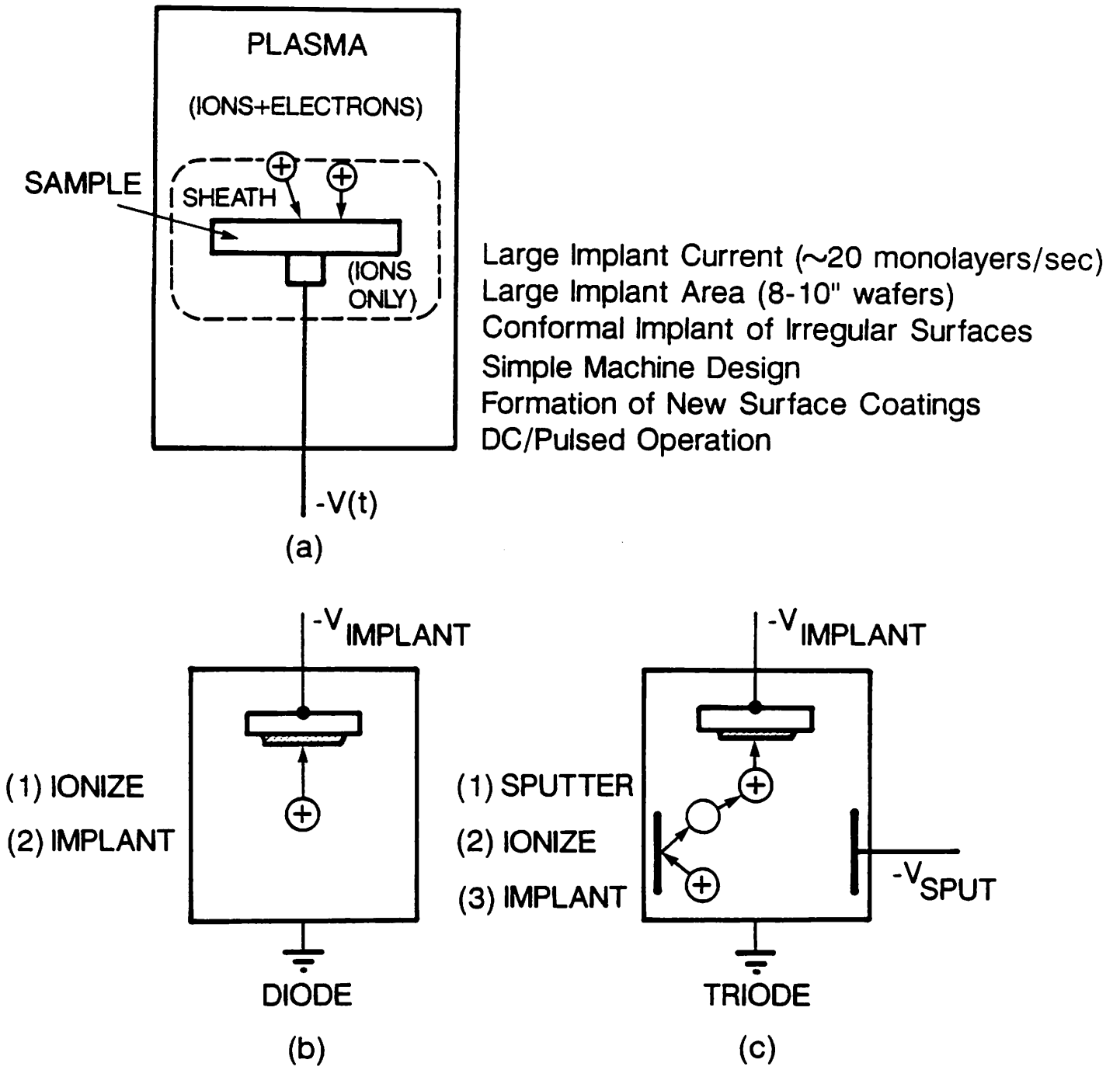


Fig. 1: Schematic side view of the PIII Reactor



Figs. 2 (a), (b), (c): Unique Features of PIII

biases.

Several features of PIII make it an attractive alternative to conventional ion implantation. With the high current capability of PIII, the throughput of present integrated circuit steps can be substantially increased. Also, the intermediate step of the ion source and all of its support equipment is completely eliminated, leading to a simple reactor design that is compatible with the cluster tool concept.

The PIII program at Berkeley in 1990-91 is supported by a $70,000 cash and $15,000 in-kind grant from Applied Materials, Inc., and a $140,000 contract from the State of California Office of Competitive Technology. The goal of the project is to transfer the PIII process under development at Berkeley to Applied Materials, Inc.

II. SUMMARY OF PROGRESS

The three critical issues for transfer of the PIII technology to Applied Materials are:

A. Process Demonstration. Demonstrate PIII processes that are more cost effective than conventional ion implantation.

B. Process Integration. Demonstrate PIII process compatibility with conventional IC processes to fabricate a complete integrated circuit.

C. Reactor Demonstration. Demonstrate a reactor that meets the required process uniformity and lack of oxide breakdown over a 200 mm wafer.

To address the first critical issue, three processes are being developed to demonstrate PIII superiority over conventional ion implantation:

(1) We have demonstrated the formation of 800 angstrom thick pn junctions with leakage currents less than 25 nA/cm^2 and low interfacial defect densities, comparable to the best commercial pn junction fabrication processes. The process consists of a 10kV SiF_4 pre-amorphization PIII implant followed by a 5kV BF_3 boron implant, followed by a one second rapid thermal anneal to activate the dopant (see Fig. 3). However, an obstacle to pn junction fabrication is condensation of BF_3 polymer, and/or substrate etching by BF_3 dissociation products, which interfere with both the implant and the measurement of implant dose. Safety considerations preclude our using di-borane (B_2H_6) or any arsenic

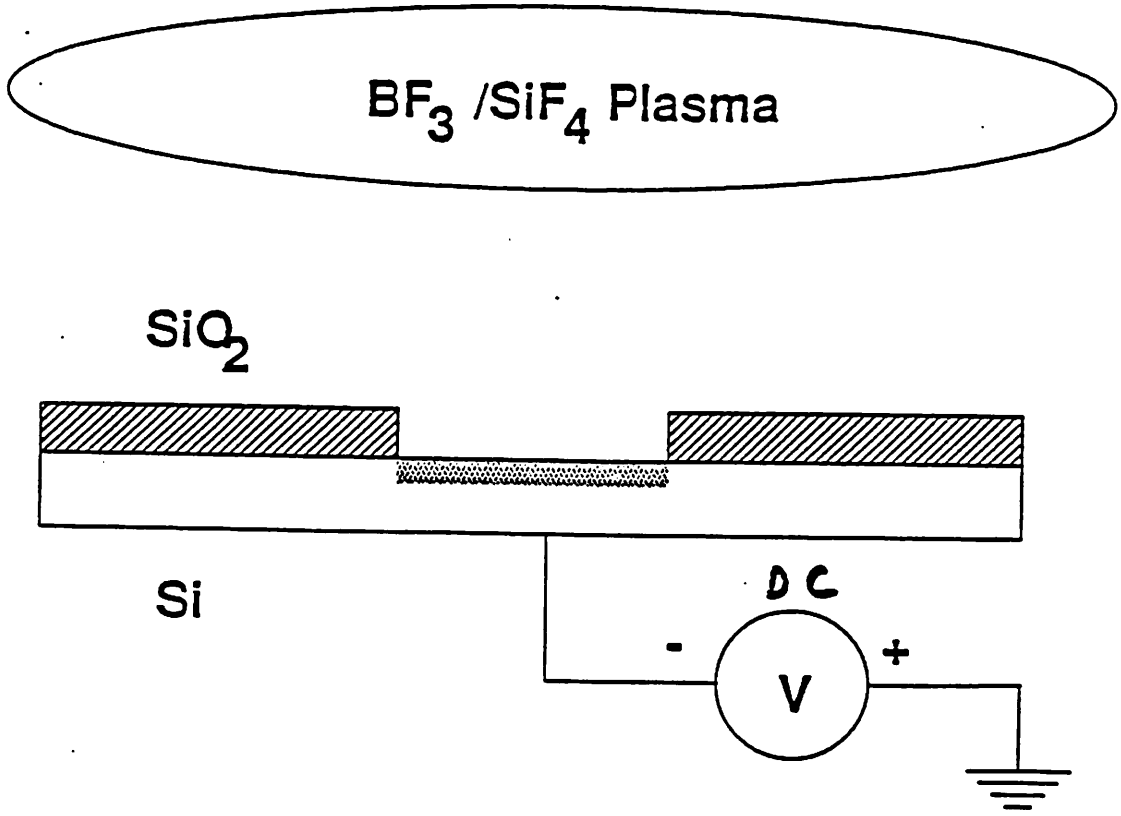


Fig. 3: PIII Shallow p^+n Junction Fabrication Process

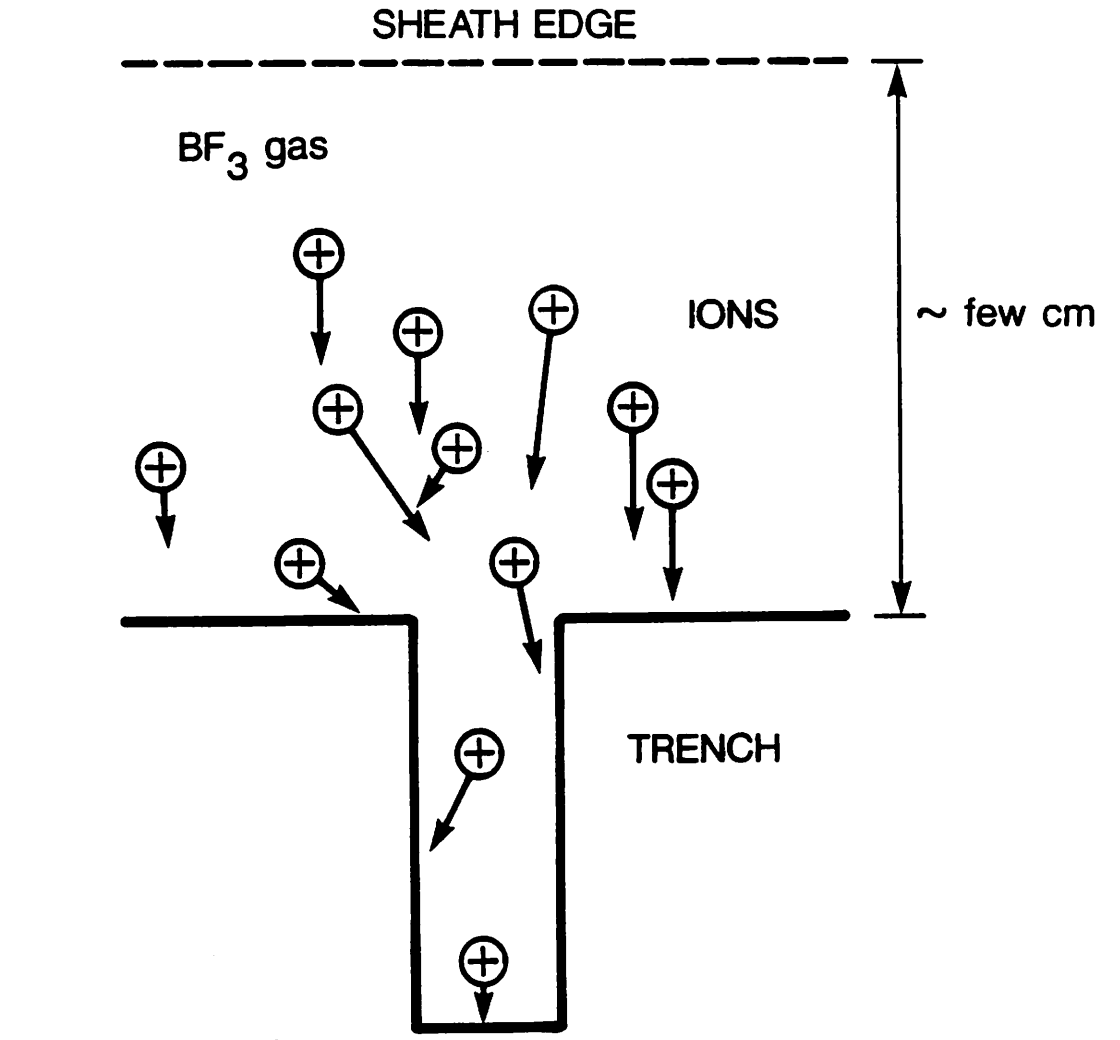
or phosphorous-containing gases in our laboratory at Berkeley. Characterization and control of BF_3 condensates and etching are described in Sec. III, and are currently one thrust of our work on pn junction formation.

(2) The second process being developed is conformal doping of trenches for trench capacitor or trench isolation. We have demonstrated conformal doping of trenches using a high-pressure (~5 mTorr) BF_3 PIII process (Fig. 4), with the doping boundary delineated by a crude staining technique (Fig. 5). As described in Sec. IV, we are refining our staining technique to delineate simultaneously a number of equiconcentration contours. We have recently obtained theoretical and computer simulation results on the angulars distribution of ions hitting the wafer. This work is described in Sec. V.

(3) The third process being developed is the formation of a metal seed layer for selective, electroless copper plating of oxide trenches. This process, which is a demonstration of the triode PIII configuration (see Fig. 2c), was described in detail in the Second Quarterly Progress Report. A brief summary of the current status is given in Sec. VI.

To address the second critical issue (Process Integration) and part of the third critical issue (Oxide Breakdown), we have developed a complete PIII processing compatibility test chip to investigate wafer charging as a cause of oxide breakdown and the use of poly-silicon as a p+ doping source. The test chip is a PMOS process including inverters and ring oscillators, in which PIII is used for all (two) p+ doping process steps. The complete chip has been designed, simulated and fabricated at Berkeley, and working devices (e.g., inverters) have been obtained. This work was described in the Second Quarterly Progress Report, and a report is given in Appendix B.

To address the remainder of the third critical issue (Process Uniformity), we are using analysis, computer simulation, and experiments to model the formation of the PIII process plasma, its injection into the process chamber, and the actual implantation process itself. We have developed a model of the implantation for pulses with finite rise- and fall-times. We have developed and are using a 2D simulation code to model the injection of the source plasma into the process chamber. We have recently extended this model, as described in Sec. VII. We have characterized experimentally the plasma uniformity using a multidipole plasma confinement system on the process chamber in argon, CF_4, and BF_3



PRESSURE	λm	
10^{-5}t	8m	
10^{-4}t	80cm	
10^{-3}t	8cm	OPERATING
10^{-2}t	8mm	PRESSURE

Fig. 4: Conformal Trench Doping

- 10 kV
- 200 mC
- 5 mT

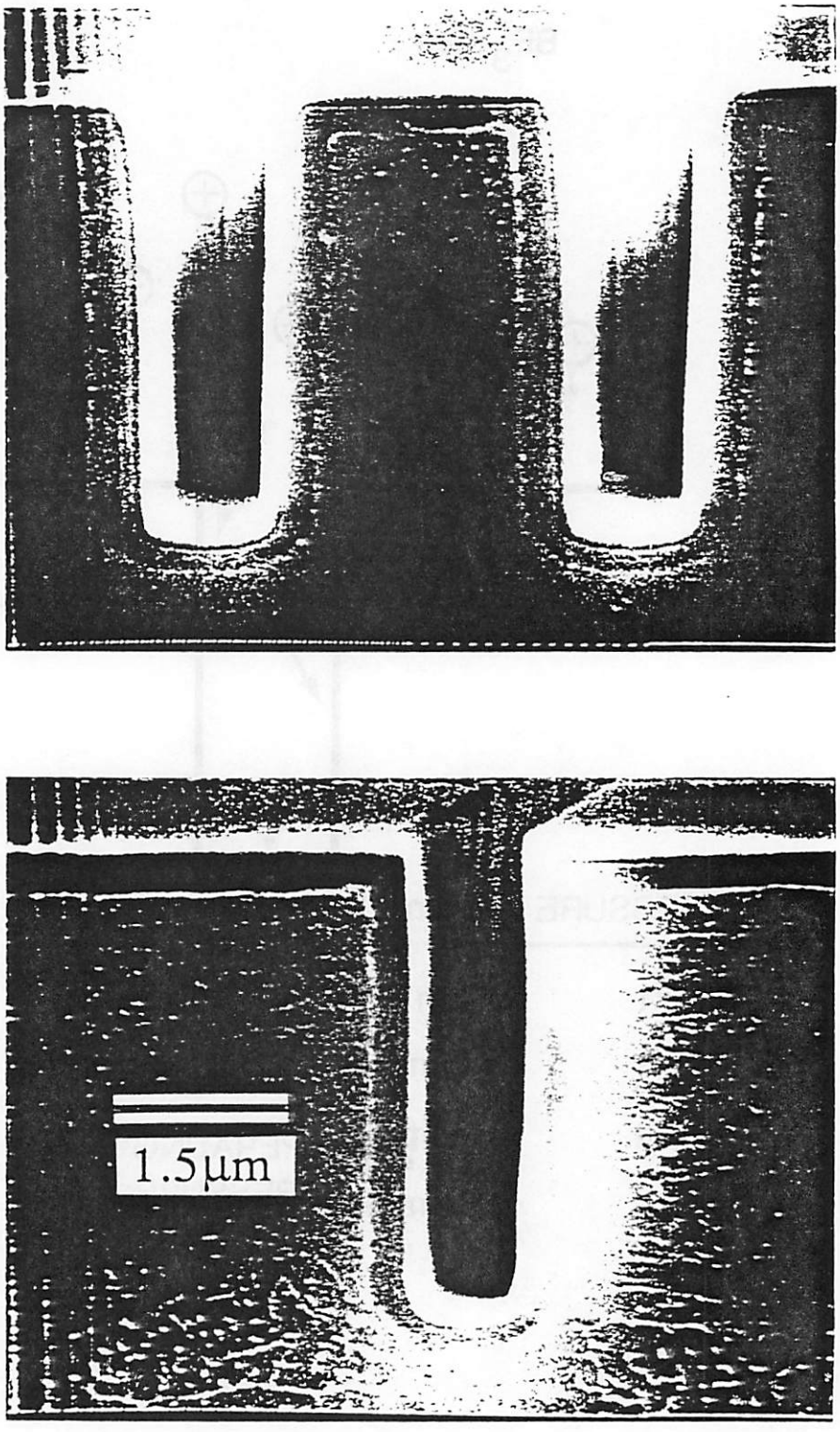


Fig. 5: PIII BF_3 Doped Trenches

gases over a range of pressures and ECR source powers. We have achieved a density uniformity over an 8" wafer of ±1%. This work was described in the Second Quarterly Progress Report.

A key test of uniformity is actual implanted dose. We have used PIII to implant 4" wafers, having an n+ doped surface layer with argon ions. We then determine the implant uniformity by measuring the increase in the resistivity of the layer due to the damage induced by the implanted argon ions. Our preliminary results show that implant uniformities of ±3% can regularly be achieved. Our major limitation to achieving even better implant uniformities appears to be the non-optimized (non-axisymmetric) design of the wafer holder (particularly, the wafer holder clips), and not any limitation arising from the PIII process itself. This work was described in the Second Quarterly Progress Report. In cooperation with G. Lecouraf and W. Wriggins at Applied Materials, we are in the middle of an implant uniformity study using BF_3 for 6" wafers. This work is described briefly in Sec. VIII.

The milestones are shown in Table 1. The Month 1 Milestone was met ahead of schedule.

The Month 3 Milestone was met ahead of schedule. A manuscript describing the excellent low leakage properties of the junctions has appeared in *Applied Physics Letters*. The results are at least as good as those achievable using any other commercial process.

The Month 5 Milestone was due on 18 May 1991 and was not met. The Month 8 milestone, which is a follow-on to the Month 5 milestone, was also not met. Hence we are behind schedule on the trench sidewall doping project.

The Month 9 milestone has been met (see Appendix B). We have designed and fabricated a PMOS test chip, and have obtained working devices.

Progress on the Month 10 milestone, due on 18 October, is described in Sec. VI. We have demonstrated planarization of copper interconnects and are studying adhesion to oxide and structural defects. We expect to meet this milestone.

The month 12 milestone deals with collisional modeling of the PIII implantation process and with the two-dimensional modeling and computer simulation of plasma and implant radial profiles. At the request of Dr. W. J. Wriggins, Product Manager from Applied, we have given the work on plasma and implant uniformity a high priority during the second and third quarters, and have achieved favorable

Table 1

Milestones

Month 1

Start characterization of 8" wafer Engineering PIII Reactor.

Month 3

Demonstrate low leakage current sub-100nm p^+n junctions with current density less than 25 nA/cm^2 at a reverse bias of -5V.

Month 5

Demonstrate trench sidewall doping uniformity to ± 50% for 7:1 aspect-ratio trenches. Junction uniformity will be measured by staining methods and spreading resistance measurements.

Month 8

Demonstrate electrical characteristics of doped trenches showing no surface state inversion and adequate oxide breakdown strengths using C-V and breakdown measurements.

Month 9

Completion of a testing integrated circuit using PIII for sub-100nm junction formation to show compatibility with conventional process flow. The testing circuit will be a ring oscillator or an inverter.

Month 10

Demonstrate planarization of Cu interconnects using PIII seeding for 2:1 aspect-ratio oxide trenches. Verify electromigration reliability and adequate adhesion to oxide, and examine microstructural defects using cross sectional scanning electron microscopy.

Month 12

Complete collisional modeling of PIII and first-order 2-D PIII model. Includes analytical model of ion energy and angular distribution along with particle-in-cell computer simulation verification, ion current versus time for realistic PIII pulse shapes, and analytical and static 2D simulation of plasma density distribution in magnetic bucket process chamber geometry and ion implant radial profiles.

Month 12

Analysis of Phase I process development progress. Fine tuning for process optimization.

results, as described in Sections III, VII, and VIII. We are now confident that we have a process with adequate uniformity, as demonstrated by both experimental measurements and modeling results.

III. INVESTIGATING DEPOSITION PROBLEMS WITH BF_3 (W. En and C. A. Pico)

In the past, PIII has had difficulties with boron depositing occasionally on wafer samples. This problem was compounded by occasional unreproducible results. In order to attain reproducibility, we have established a two step procedure to condition the chamber when we switch to a different gas. Before starting a new gas, an O_2 plasma is run for approximately one hour and then an argon plasma is run for approximately one hour. This procedure appears to remove any kind of deposited or adsorbed materials from the chamber.

To test the cleaning and to map out the deposition problem we ran a series of samples at 900 W of microwave power and 1 mTorr of BF_3. We varied the length of time exposed to the plasma for one series and for another we implanted for various amounts of time at 10 KV and 100 Hz rep. rate. When the samples were measured using an alphastep, we discovered that the samples were being etched. Several of the runs were repeated in a random fashion to check for reproducibility, and we consistently observed etching. A plot of the etch depth versus time (Fig. 6) shows that implantation does not affect the etch rate.

Apparently, at 900 W a sufficient amount of fluorine ions are generated to prevent any deposition of boron to occur and to cause etching of the silicon substrate. Previously, we have implanted at low microwave power ~ 300 W and low pressure (< 1 mtorr), to avoid deposition problems. So, now we will vary the microwave power to find the crossover point between etching and deposition. We will also explore the possibility to adding hydrogen gas to BF_3 to see if it will react with the fluorine ions, thus preventing etching.

IV. MULTIPLE EQUICONCENTRATION CONTOUR DELINEATION IN Si (C. Yu)

In 1989, Gong et al. reported the delineation of up to three equiconcentration lines by a chemical stain for the purpose of measuring dopant concentrations in Si in two dimensions. This effect was attributed to the rapid change of etch rate of the Si in the etching solution as a function of dopant concen-

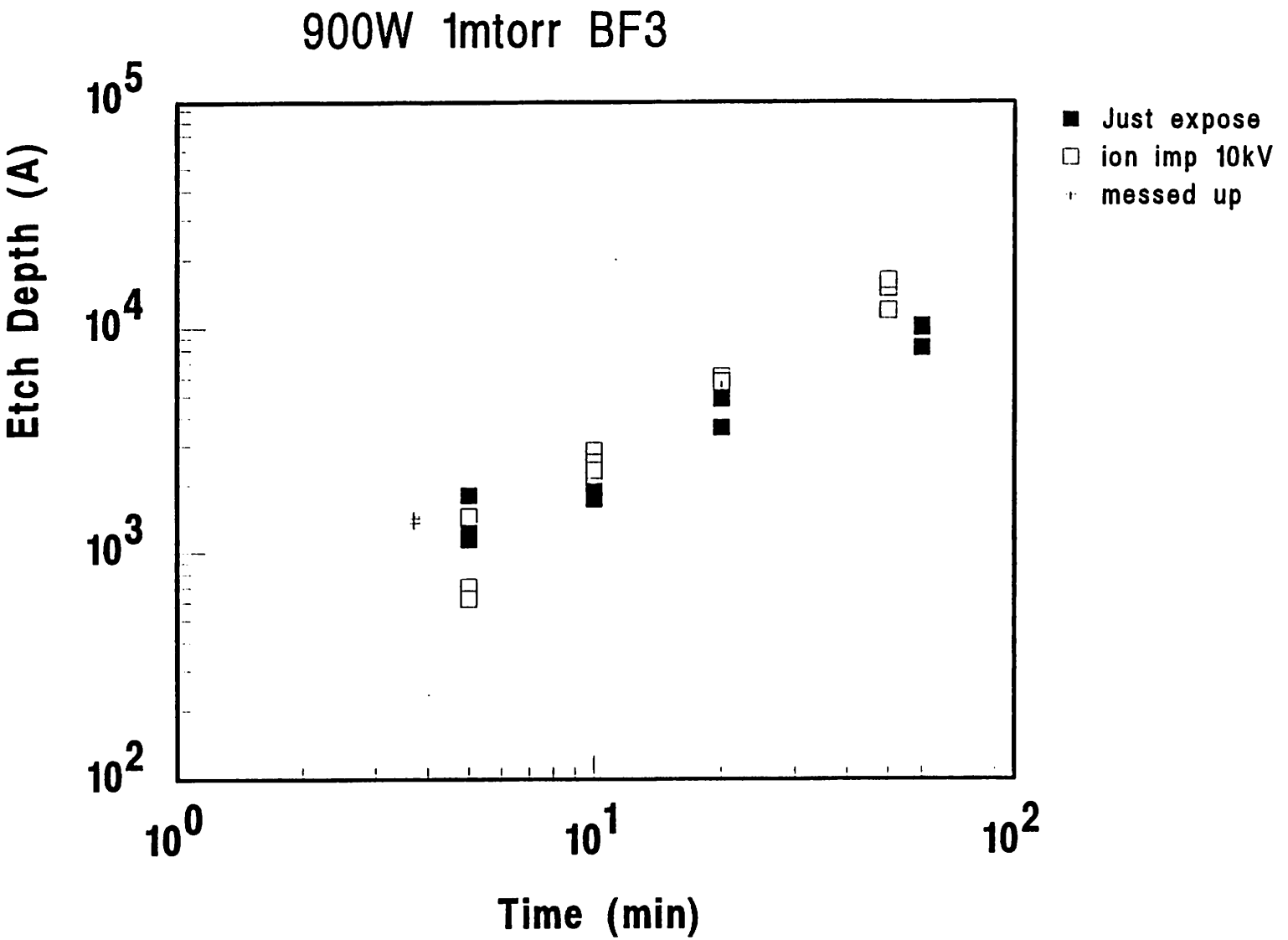


Fig. 6: Etch Depth vs. Time

tration.

Implantation of dopants into irregular surfaces results in two dimensional dopant profiles. Specifically, trench structures in Si are doped to serve as device isolation or storage capacitors in DRAM's. As of now no convenient or reliable electrical means exist to characterize these dopant distributions. A chemical multi-contour delineation would be extremely useful in this application as it would provide quick and semi-quantitative information for 2D dopant distributions. In addition, two dimensional dopant profile parameters can be extracted directly from device structures for CAD simulators.

We have been able to obtain reproducibly two equiconcentration lines in p+ Si by the staining procedure described below. Samples of <100> Si were implanted with 1.5 MeV boron at a dose of $5\times10^{14}/cm^2$ and subsequent annealed at 1060°C for 20 s. Shown in Fig. 7 is a typical SEM micrograph of a vertical cross-section of the sample after staining. The standard shown is 2.78 microns, within 5% accuracy. Two sets of contours are visible. The positions of these contours with error bars are plotted in Fig. 8 over the simulated dopant distribution generated by SUPREM using Pearson IV parameters, which are well known from literature. This calibrates the observed contours at approximately $5\times10^{17}/cm^3$ and $8\times10^{18}/cm^3$. This is different from the values of $1.5\times10^{19}/cm^3$ and $6\times10^{16}/cm^3$ reported by Gong for two reasons. First, our staining was carried out under a strong, broad band white light source instead of the UV source used by Gong. We have observed significant heating of the sample during exposure and believe that this caused the lower concentration contour to shift. Second, the delineations we observe are due to significant variations in etching rate of silicon for different dopant concentrations. Thus, the higher concentration delineation is very sharp past the peak of the profile and smeared before the peak. Also, the higher concentration contour corresponds to the peak of the dopant concentration in our sample. Thus, only one contour is observed for this concentration. We will perform this stain on other high energy, high dose samples as they become available to cross-calibrate our results.

We have also performed this stain on a diffused p+ sample prepared by surface diffusion of boron at the solid solubility limit for 50 min. at 1050 °C. However, because of the proximity of the two

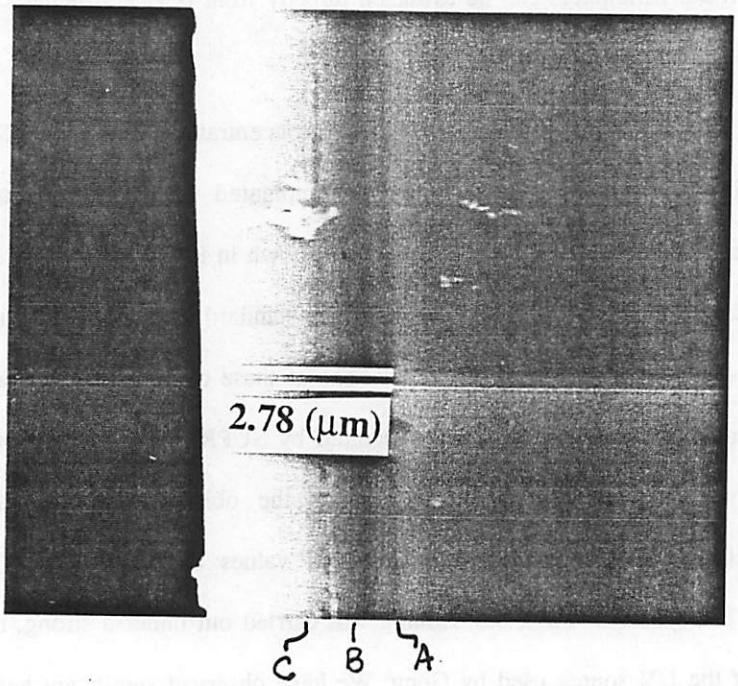


Fig. 7: Cross Sectional SEM Micrograph of 1.5 MeV B Samples with Dose $5\times 10^{14}/cm^2$ after staining

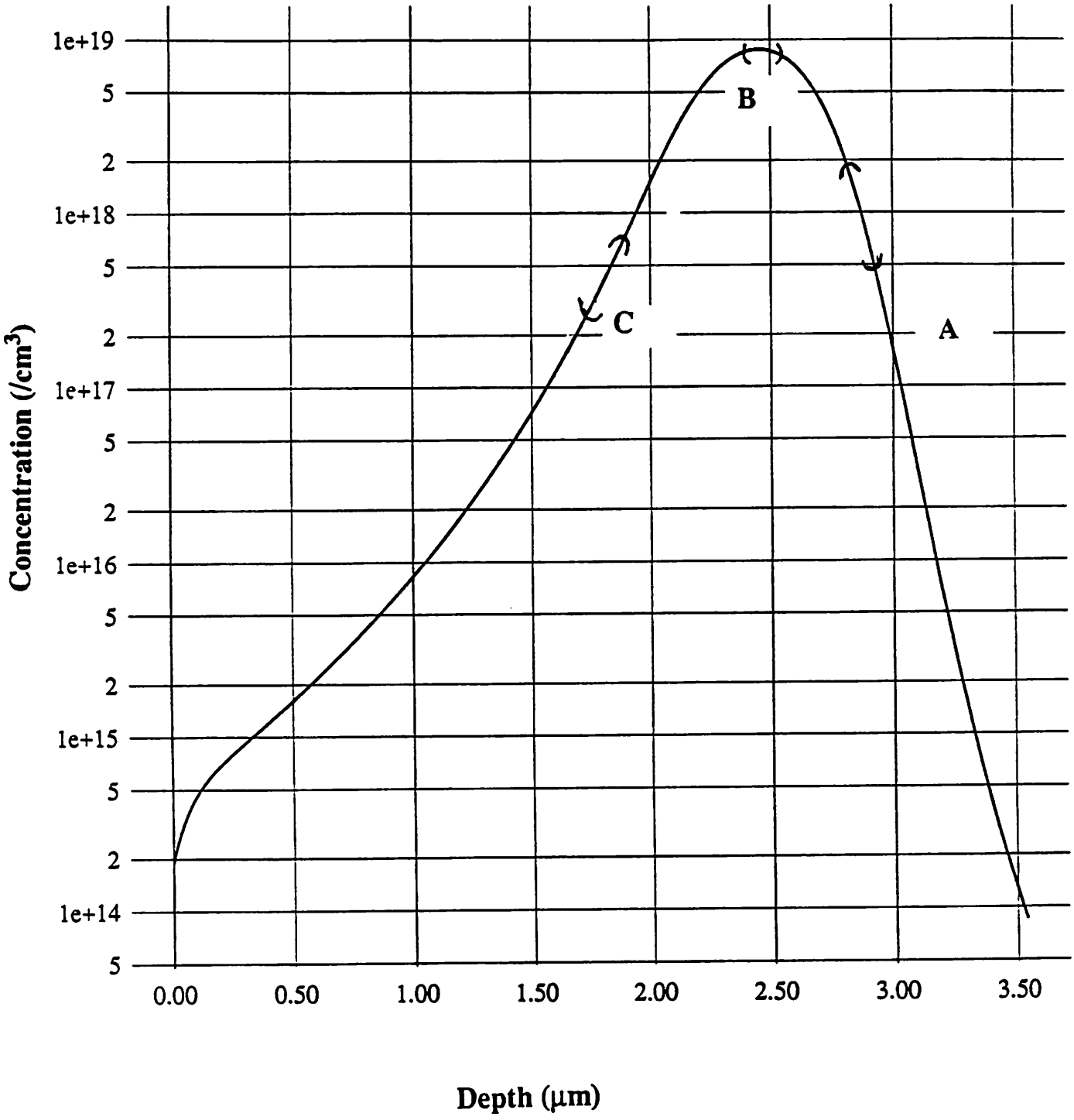


Fig. 8: Delineated Contours from Figure A Overlaid with Error Bars on SUPREM Profile for 1.5 MeV B at $5\times 10^{14}/cm^2$

expected contours, SEM analysis of a vertical cross-section will not offer enough resolution for meaningful measurements. Thus we have also performed 3° angle lapping before staining. This will yield about 20 times magnification along the depth direction. The SEM micrograph is shown in Fig. 9. We are currently pursuing an accurate simulation of this diffusion to verify the delineations.

The etching solution is prepared by mixing HF (50%):HNO3(70%):CH3COOH(100%) in a ratio of 1:3:8. We found that the most reproducible results were obtained if the cleaved samples receive a short 10s dip in dilute HF (~ 5%). Since the etching mechanism consists of the oxidization of Si and the removal of the byproduct by HF, we believe that the HF pretreatment clears any oxide that might be on the surface to be stained to facilitate the etching action of the solution. Then, the sample is exposed to a strong white light (Sun Gun) while being immersed in the solution. The distance of the lamp from the sample was approximately 6". The optimum staining time for this procedure was determined to be 8s. The sample was quenched and rinsed in DI water immediately to stop the etching action. Variations in etching time are important because SEM images are very sensitive to surface roughness. We often observe samples where the entire heavily doped region was etched out, and this appears as fissures and wide openings on SEM micrographs.

Recently we have been able to observe the stained area with an optical microscope on angle-lapped samples. Figure 10 shows an optical image of the same 1.5 MeV sample lapped at approximately 3°. Note that the optical picture is much different from the SEM one. We can actually observe bands of different colors, seen as different shades on the photo. We believe that the staining solution creates some compound of oxidized silicon which is strongly dependent on dopant concentration. Moreover, this suggests that the contours we observe in SEM are actually regions of different thickness of the compound. Thus, SEM images of the stain have been difficult to obtain since there is very little variation in the surface of the stained area. We believe that stripping off the residue will leave a contoured surface which will facilitate SEM observations of the delineations.

Also, there appears to be many more regions delineated in the optical image than the SEM image of the same sample. We are currently corrolating these delineations to the dopant profile from simulation.

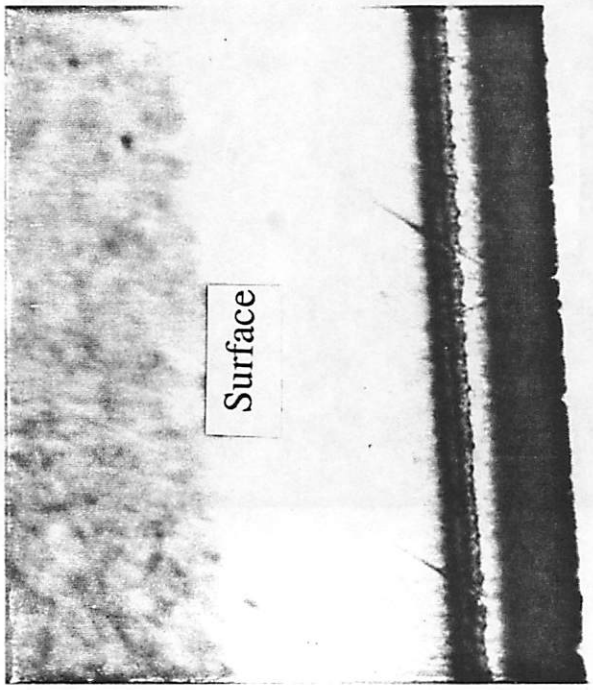


Fig. 9: SEM Micrograph of Stained 1.5 MeV Sample Lapped at 3°. Magnification = 1000 X

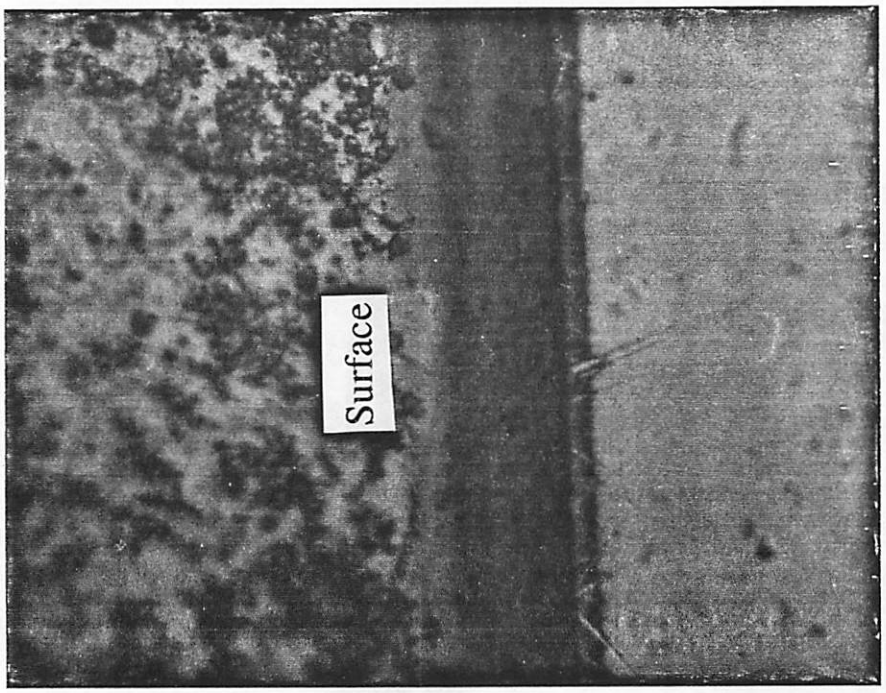


Fig. 10: Optical Photograph of Stained p+ Diffused Junction Lapped at 3°. Magnification = 1000 X

In summary, we have developed a chemical technique that can delineate so far up to two equiconcentration contours of boron implanted Si in a reproducible procedure. These contours have been calibrated to be approximately $5\times10^{17}/cm^3$ and $8\times10^{18}/cm^3$. We are in the process of cross-corrolating these contours to other different high energy and high dose implants. We have evidence that the nature of the delineation is due to the different thicknesses of residual compounds from the staining. This may pose a limitation on the visibility of the stain to SEM microscopy. Surface cleaning and etching time has also been determined to be crucial to how the delineation will appear in SEM observations. By stripping the residue, we will be able to enhance the contrast of the SEM image and make this technique more valuable as a quantative tool which can be applied to determine dopant distributions in two dimensions.

V. ANGULAR DISTRIBUTION MODELING (R. A. Stewart, V. Vahedi, and M. A. Lieberman)

One of the attractive features of PIII is the ability to obtain implants that are either very directional or very conformal simply by adjusting the gas pressure. In the low pressure limit, the ion motion through the sheath is collisionless, resulting in a directional implant. In the high pressure limit, the sheath is highly collisional, which results in ions striking the wafer surface with some angular distribution and allows for doping of topological features such as trench sidewalls.

We have begun a study of the influence of parameters such as gas pressure, gas species, wafer bias, and pulse width on the ion angular distribution function (IADF). A model has been developed that predicts the IADF in the limit of a highly collisional sheath corresponding to gas pressures greater than 10 mTorr. We consider both the ion energy distribution and angular distribution to arise from ion-neutral collisions consisting of charge-exchange collisions and elastic scattering. We assume charge-exchange is the dominant mechanism, hence we consider the angular distribution to arise mainly from ions that strike the wafer surface after undergoing only one elastic scattering collision following the last charge-exchange collision before striking the wafer. We further assume that the ion density in the sheath is uniform, corresponding to the high pressure limit.[2]

The IADF $f(\theta)$ is obtained by performing a double numerical integration over the distribution of ion speeds at the wafer surface and the distribution of initial ion positions following their last elastic

scattering event. Results are plotted in Fig. 11 for argon ions implanted at 500 volts over the pressure range of 10-100 mTorr. The ratio λ_s/λ_{cx} was taken equal to 6, where λ_s and λ_{cx} are the mean free paths for elastic and charge-exchange scattering, respectively. Currently we are comparing results from the model with the PDP1 particle-in-cell simulation results. In addition we are investigating an analytical approximation to the IADF which could aid in relating plasma parameters to process conditions required for a variety of implantation applications.

VI. METAL SEED LAYER FORMATION FOR ELECTROLESS COPPER PLATING

(M. H. Kiang)

More Rutherford backscattering (RBS) measurements have been done to study the effects on the copper film adhesion that results from different dopant distributions and PIII processing procedures (i.e., 1-step vs. 2-step). Results showed that for low-dose samples that are desirable for reducing deposition on the trench sidewalls, the 2-step process dose gives a deeper dopant distribution into the substrate, which in turn may improve the adherence between the deposited Cu film and oxide substrate.

A series of resistivity measurements of the planarized trenches has been carried out, and we obtained a copper film resistivity of around 2 μΩ–cm for 0.5 μm thick plated trenches, a reasonably good number as compared to 1.7 μΩ–cm for pure bulk copper. The temperature coefficient of the resistors (TCR) was 0.3554% °C, compared with the quoted 0.3616% °C for pure copper.

VII. PLASMA UNIFORMITY STUDIES (R. A. Stewart, B. Troyanovsky, and M. A. Lieberman)

A study is in progress to improve the plasma uniformity in the process chamber. In the Second Quarterly Progress Report, we reported on the modifications made to the process chamber, including an octupole arrangement of permanent magnets and shielding of the magnetic field generated by the ECR electromagnets. Variations of radial ion uniformity obtained from Langmuir probe measurements were presented along with predicted uniformity from a diffusion model of the ion motion in the process chamber that we developed and described in detail in the previous report.

Figure 12 shows the process chamber geometry that we have used in the model. The two-dimensional (r,z) diffusion equation

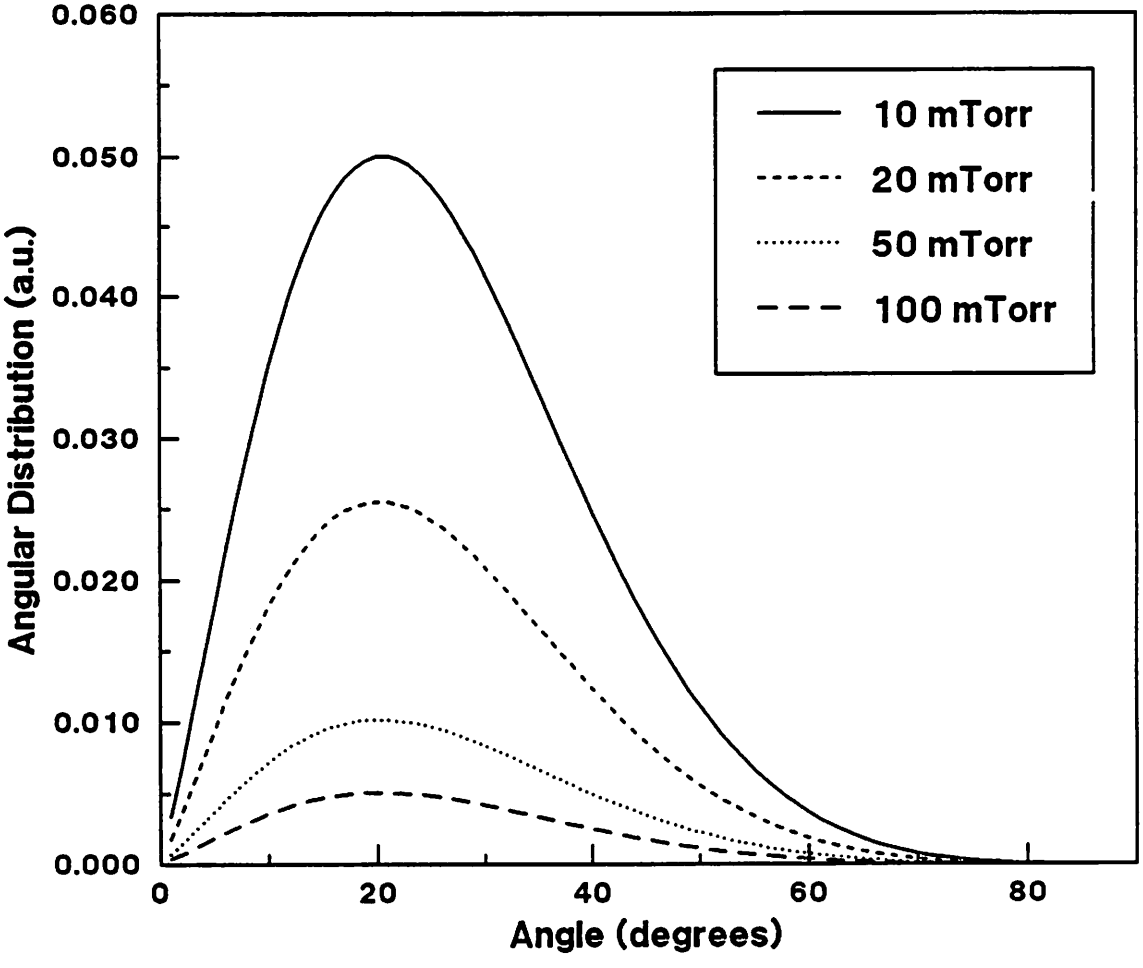


Fig. 11: Computed Angular Scattered Distribution of Scattered Ions at Various Implant Pressures for an Electrode Biased at -500 volts

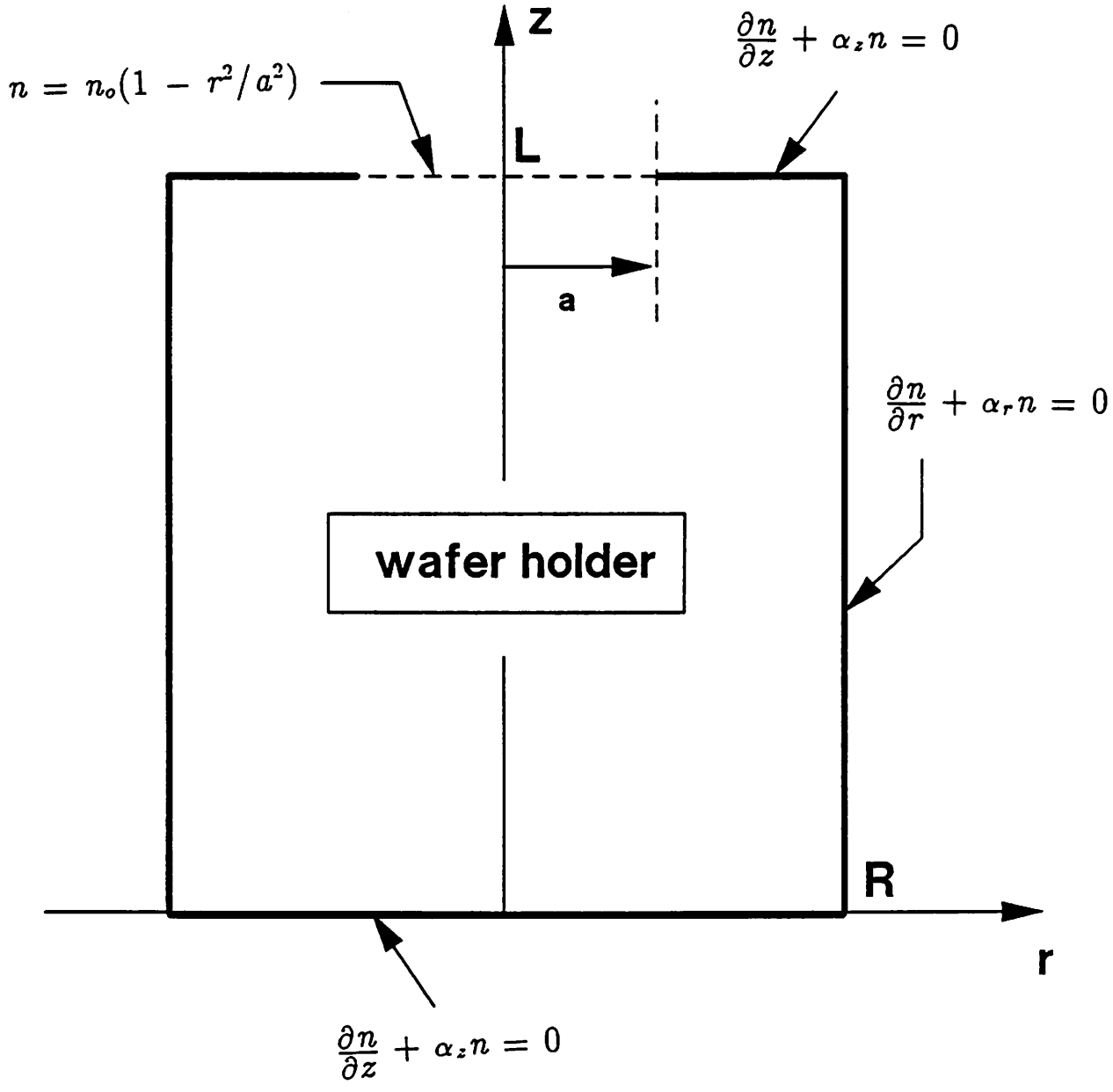


Fig. 12: Process Chamber Geometry used to Model Ion Diffusion with Magnetic Multipole Side-wall Confinement

$$\nabla^2 n + k^2 n + G = 0$$

is solved in the interior of the chamber subject to boundary conditions of the general form

$$\frac{\partial n}{\partial x} + \alpha n = 0,$$

where x = r or z and α depends on gas pressure and the effective reflection coefficient of the walls.

A number of enhancements have been made to the model to provide a more realistic description of the actual conditions in the process chamber. First, we have included an option in the computer code to specify an electrode (wafer holder) in the interior of the chamber, as indicated in Fig. 12. Second, we are studying several different models for describing the effect of the diverging magnetic field from the source region on ion diffusion. Third, we have developed a simple interface for graphing our program output with Mathematica.

Most previously published studies of the diffusion equation in a downstream ECR reactor do not consider the effect of an electrode placed in the chamber. However, as the results presented below will show, the diffusion solution may be significantly altered in this case. Our computer program allows for specification of an electrode of arbitrary shape and with general boundary conditions of the form given above. Figure 13 shows a three-dimensional plot of n(r,z) when a 28 cm diameter, 1 cm thick electrode is placed at the position z = 43 cm, centered on the z axis. The electrode was specified to be a perfectly absorbing surface for ions. The electrode clearly has a significant effect on the solution of the diffusion equation in this case.

The effect of an electrode on uniformity is illustrated in Fig. 14. The radial variation of ion density 1 cm in front of the wafer holder electrode is plotted for electrodes similar to that described above, but with radii R_{wh} varying from 10-20 cm. Note that the solution for R_{wh} = 20 cm has the usual form for the diffusion solution in an empty cylinder; this result is expected since R_{wh} = 20 cm is close to the chamber radius (21.5 cm). Hence, the solution for R_{wh} = 20 cm gives essentially the same solution as if the lower chamber end wall was at the position of the electrode. In contrast, the solutions for R_{wh} < 20 cm are dramatically different in form. In these plots, the solution changes noticeably beyond the radius of the electrode. Near the electrode, the ion density is controlled primarily by the absorbing boundary condition at the electrode surface, while beyond the electrode, the solution is controlled by

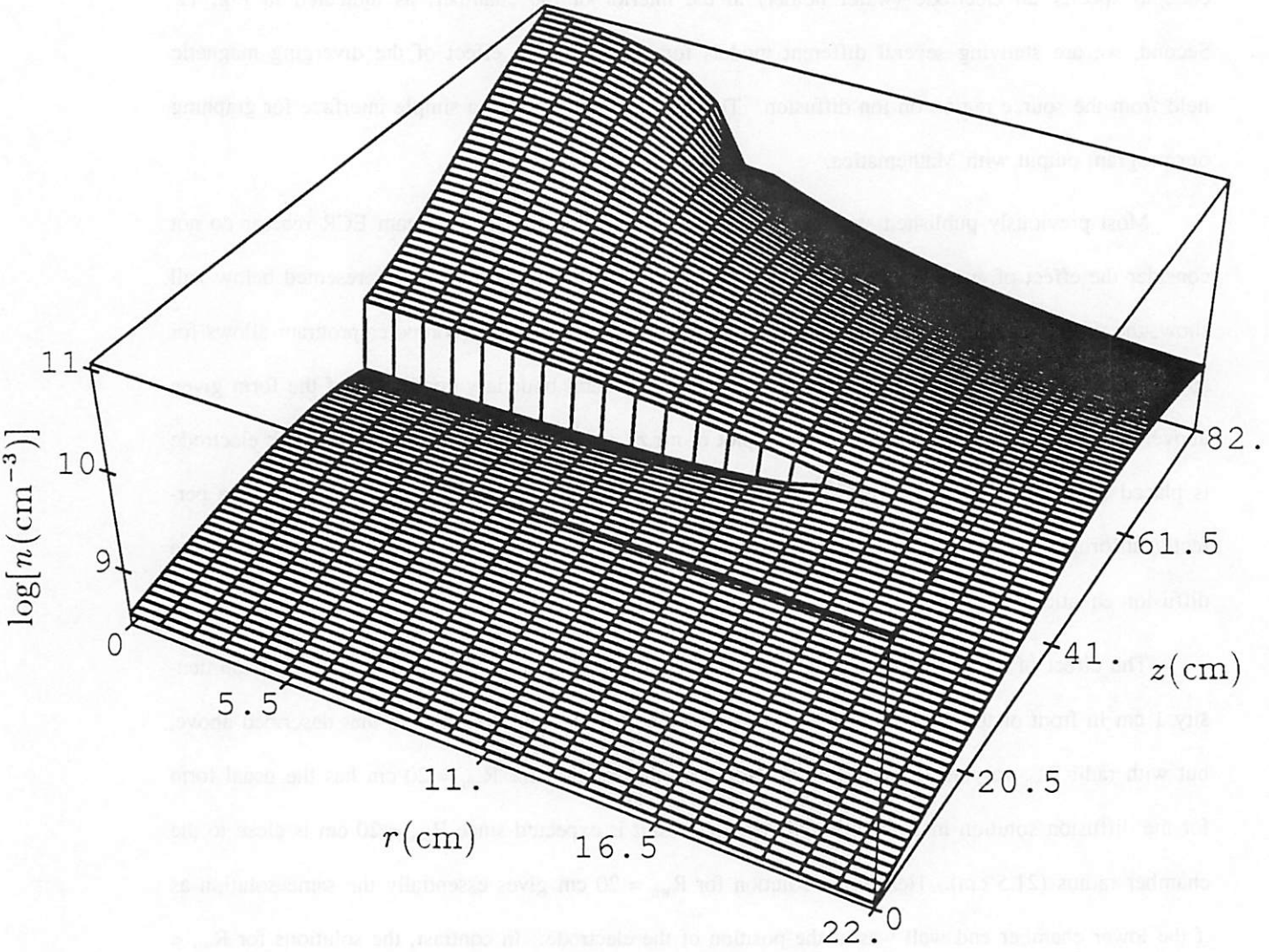


Fig. 13: Three-dimensional Plot of Computed Plasma Density in the ECR Process Chamber for an Argon Plasma at 1 mTorr. The Source End is at z = 82 cm. The Electrode is at $0 \leq R \leq 14$ cm, $42 \leq z \leq 43$ cm

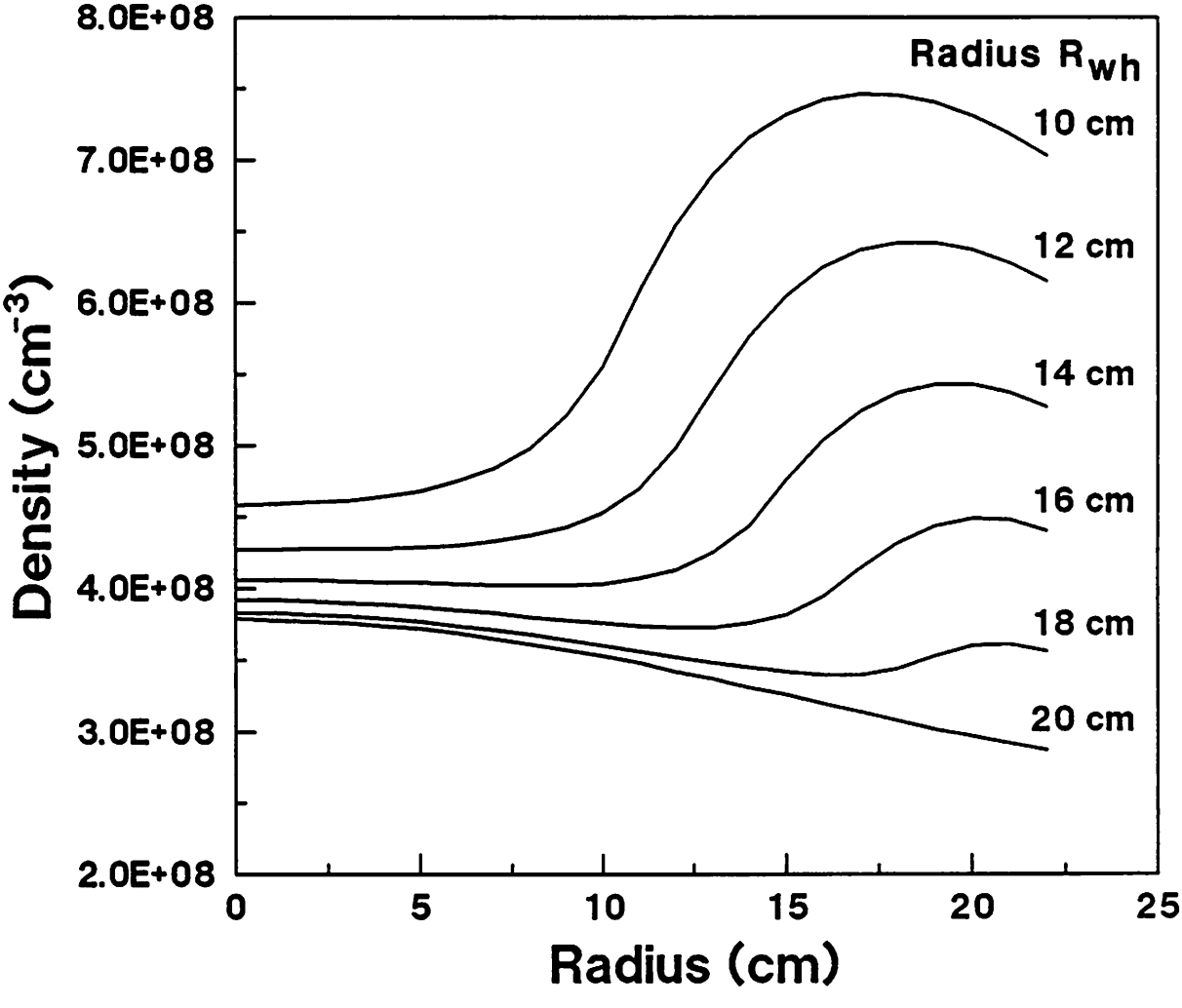


Fig. 14: Computed Radial Plasma Density Profiles in the ECR Process Chamber for an Argon Plasma at 1 mTorr with electrodes at $42 \leq z \leq 43$ cm, and with Various Wafer Holder Electrode Radii

diffusion and the ion confinement of the multipole magnets on the chamber side-walls. Note that in the region R ≈ 10–14 cm, there is an optimal electrode diameter for achieving the best (flattest) plasma uniformity near the axis of the process chamber.

The magnetic field caused by the electromagnets that typically straddle the source chamber in an ECR system may significantly alter the simple diffusion solution that is believed to exist in the field free case. In particular, for low pressure discharges, the ions will be somewhat magnetized, i.e., upon entering the process chamber, their trajectories will follow the diverging field lines. For higher pressures, the ions suffer collisions which allows for cross field diffusion. An accurate diffusion model must therefore include, (1) ambipolar diffusion to account for the unequal diffusion rates of ions and electrons, (2) cross field diffusion that is pressure dependent and weaker than diffusion along field lines, and (3) a coordinate transformation to properly describe the diffusion parallel and perpendicular to field lines in the (r,z) coordinate system. We are currently implementing all of the above enhancements into our model. An extensive study of uniformity optimization will then be performed.

VIII. IMPLANT UNIFORMITY (N. W. Cheung)

Applied Materials has started evaluating the uniformity of implanted Si wafers (6"-diameter) with PIII performed at the University of California at Berkeley (UCB). This investigation was designed to optimize BF_3 shallow implants over large-diameter wafers and to compare electrical activation of conventional BF_2 implants with plasma BF_3 implants. Applied Materials will provide UCB with 6-inch n-type Si wafers and will perform the rapid thermal annealing (RTA) in their Implant Division Processing Laboratory in Santa Clara. Applied Materials will also perform conventional BF_2 implantation with their Model-9200 commercial implanter. The AMAT technical co-ordinators are George Lecouraf and Walter Wriggins. Resistivity mapping will also be performed at Applied Materials because of their large-area mapping capability (up to 8" wafers). Both AMAT and UCB agreed to concentrate on the high-dose, low-energy BF_3 implantation conditions. The PIII conditions are listed in Table 2 and the processing conditions are listed in Table 3.

Table 2

Log Sheet of AMAT/UCB PIII BF_3 Implants

Wafer Number	Nominal Voltage	Nominal Dose
AM-1	10kV	1E16
AM-3	2kV	1E15
AM-4	2kV	1E16
AM-5	10kV	1E15
AM-7	10kV	1E15
AM-8	2.5kV	1E15
AM-9	2.5kV	1E16

Table 3

Processing Procedure for PIII Wafers

(1) Standard Clean (Done at UCB)

(a) Piranha clean 10 min

(conc. H_2SO_4, 120°C bath. Add 100 ml of H_2O_2 just before clean)

(b) Rinse in DI water for 2 min

(c) HF (25:1) dip for 1 min

(d) Rinse in DI water until resistivity is ~12 Mohm-cm.

(2) RTA at 1000°C for 30 sec in N2.

(3) Standard Clean (HF Dip at AMAT)

(4) Sheet Resistance Mapping.

The first set of wafers described in Table 2 was delivered to AMAT around mid-September. Preliminary analysis shows various non-reproducible results, but the best wafer has a 2% uniformity (not bad). This shows reproducibility problems (or conditions) but also demonstrates good uniformity can be done. The 2% sample is better than some of the typical results obtained using commercial implanters. This work is continuing.

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APPENDICES

APPENDIX A

PLASMA IMMERSION ION IMPLANTATION: A PERSPECTIVE

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ABSTRACT. Many kilovolts can be sustained in the sheath between the boundary of a high ion density plasma generated by Electron Cyclotron Resonance (ECR) and a negatively biased substrate in the plasma. Very high dose rate implantation can occur as ions are accelerated from the edge of the sheath towards the substrate. This, combined with simple reactor design, allows plasma immersion ion implantation (PIII) to be used in thin film modification applications that are not viable for conventional implanters. We have used PIII to form sub-100nm p+/n junctions and to getter impurities by backside implantation. By using a separately biased target, ionization of sputtered material can occur and plasma assisted vapor deposition can be achieved. This can also be done with concurrent ion beam mixing of the interface. These capabilities have been demonstrated in Pd seeding for selective electroless copper plating. Through collisions with neutrals in the sheath, the ions can acquire an energy and angular distribution dependent on processing conditions. This has been used to conformally dope high aspect-ratio trenches. As with any high dose implantation, wafer heating is potential problem for PIII as well as substrate sputtering during low implant energy operations. Other potential problems of PIII include pasma/substrate interactions in the forms of etching, deposition, or particulate formation on the substrate.

1. Background

Conventional ion implantation machines consist of an ion source, an accelerator to impart kinetic energy to the ions, ion optics to focus and direct the beam, and some means of ion mass selection. Recently, a novel ion implantation technique using plasma-generated ions was demonstrated by Conrad [1] and Tendys [2]. The Berkeley implementation of this technique for integrated-circuit fabrications, called plasma immersion ion implantation (PIII) [3] is shown schematically in figure 1. A plasma is generated by an electron cyclotron resonance (ECR) source powered by a 2.45 GHz microwave power supply with power adjustable from 0 to 1500 W and matching network. The processing chamber contains the wafer holder to which a negative bias supply is attached. With high ion densities (10^{10}–10^{11}/cm^3), kilovolts of negative bias can be sustained between the edge of the ion-matrix sheath and the wafer surface. Implantation is achieved as the positively charged ions in the sheath are accelerated toward the wafer.

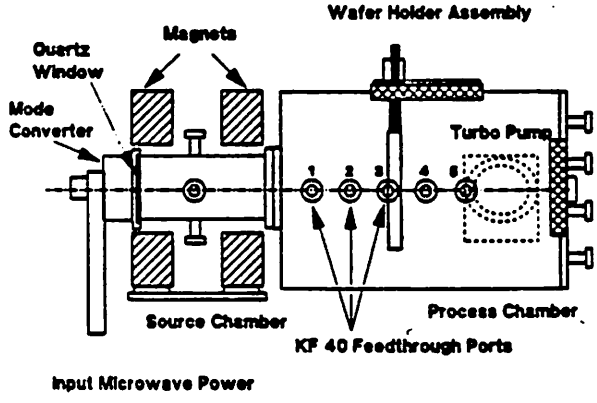

Figure 1. Schematic of Plasma Immersion Ion Implantation apparatus.

Note that in this configuration, no mass selection or ion optics is used. The implant dose rate can be quite high (10^{16}/cm^2–s) even at low energies. Also, the complexity of the implant machine is greatly reduced, as well as the machine foot-print needed. The implant area can be quite large, and

large workpieces can be accomodated without scanning the beam. The simple machine design, high throughput, and small reactor size positions PIII in the direction of cluster tools.

2. Processing Features

2.1. HIGH DOSE IMPLANTATION

The high dose rate at low energies make PIII ideal for heavy implants and material surface modification applications. Figure 2 shows the implant current density versus microwave power and DC substrate bias. We have reported sub 100nm p+/n junciton formation [4], where SiF_4 preamorphization followed by BF_3 implantation at -2kV bias was performed followed by RTA post implant dopant activation. Figure 3 shows the SIMS profile of the as-implanted B profile:

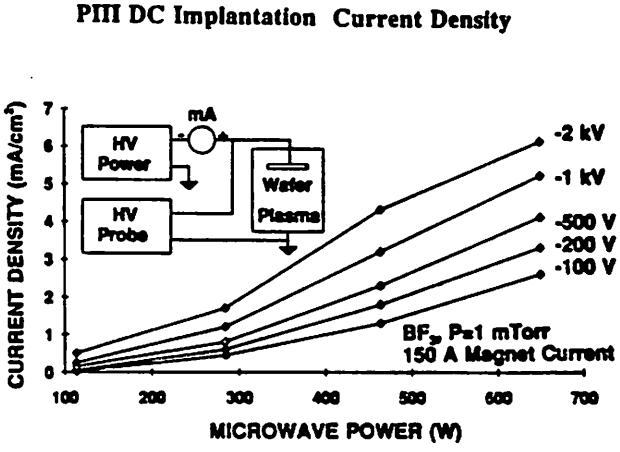

Figure 2. Implantation current density dependence on forward microwave power with BF_3 plasma in DC mode.

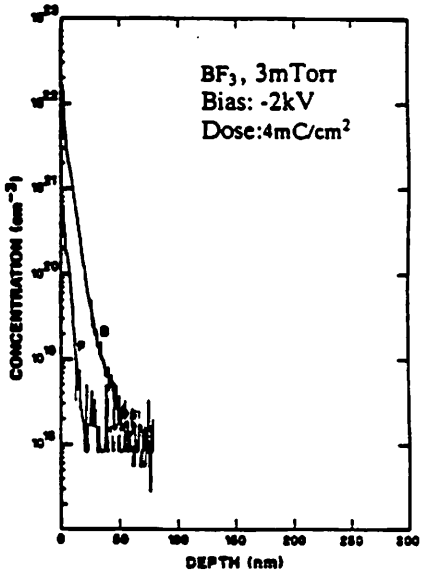

Figure 3. SIMS profiles of BF_3 PIII Si wafers with -2 kV DC bias at 3mTorr and dose of 4 mC/cm^2.

For a low substrate bias of -2kV, the B concentration peaks at the substrate surface and falls rapidly into the substrate. This profile is representative of the ion energy distribution with PIII. The diodes fabricated show excellent reverse bias leakage characteristics ($30nA/cm^2$) at -5V reverse bias.

PIII has been used in other high dose applications which have traditionally been nonviable by implantation because of throughput constraints. Thermally induced hillocks on Al films have been suppressed following high dose ($>10^{16}/cm^2$) implantation of N_2 ,O_2, and Ar using PIII [5]. We have also demonstrated the effectiveness of PIII to getter Au, Ni, and Cu by high dose backside implantation of argon with a bias of 20-40 kV [6].

2.2. ION VELOCITY AND ANGULAR DISTRIBUTION

Because the implanted ions are accelerated through an ion-matrix sheath, they will acquire a velocity and angular distribution from collisions with the neutrals in the sheath, depending on gas pressure, bias voltage, ion charge, and substrate surface topology. Several authors have reported either analytical or monte carlo simulations of the ion energy and angular distributions of the ions traveling in a glow discharge sheath. An example of such is Berkeley's PDP1 [7]. Using this simulation, it was shown that the straggle in both the energy and angular distributions increrased with increasing gas

pressure. Thus, by adjusting the gas pressure and the microwave power, the amount of straggle in the energy and angular distributions of the incident ions can be varied to suit particular applications.

2.2.1. Dose Control. While the total implanted dose control with PIII poses no difficulties, the non-monoenergetic nature of the implanted ions can be a challenge in cases where the actually "useful" dose depends on the ion energy distribution. This is the case with implantion through an intermediate layer where the ion energy distribution needs to be known in order to calculate the number of ions that penetrate the masking material. For cases where the angular spread of the ions is significant as in high gas pressure PIII operations, the angular distributions have to be determined as well. However, PIII is ideal for high-dose doping applications in which the implanted profile is not critical such as poly doping or source/drain formation where the subsequent thermal dopant redistribution actually determines the final dopant profile. For these applications, PIII acts as a predep implanter with high throughput and good dose control.

2.2.2. Conformal Doping. With the trend in Si processing technology to scale down, an emerging need is surfacing to make use of the vertical dimension of non-planar wafer topologies such as trenches as storage capacitors for DRAM cells or device isolation. Doping of these non-planar structures with conventional line-of-sight implantation often require wafer tilting and multiple implants to dope all sides. Taking advantage of the inherent angular divergence in the PIII ion beam, we have also demonstrated conformal doping of BF_3 implanted into high aspect ratio trenches [8].

2.3. PULSED AND DC OPERATION

The PIII reactor can operate either with a pulsed or DC negative substrate bias. Operation in the pulsed mode is necessary if the substrate has an insulating coating. In this case the throughput of PIII is determined by the time average dose rate it can deliver which is limited by the duty factor and the repetition rate of the pulser. For conductive substrates, the DC mode is advantageous as the throughput is not restricted by these constraints.

2.3.1. Charge Neutralization. With conventional high current implantors, there is always concern whether the thin gate dielectric in MOS devices will be able to withstand the high electric field that results as positive charge accumulates on the wafer surface. However, during pulsed mode PIII operation, the positive charge only accumulates during the "on" part of the pulse cycle as the sheath forms and positives ions accelerate and implant into the substrate, leaving positive charge on the surface. During the "off" portion of the pulse cycle, electrons are attracted to the wafer surface where they neutralize the accumulated positive charge. However, dielectric breakdown can still occur during the "on" part of the cycle. The maximum cricital charge that causes breakdown can be written simply as:

$$Q_{max}=\varepsilon_{ox}xE_{breakdown}(SiO_2)$$

For an estimated breakdown field of 5MV /cm, Q_{max} is 10^{13}q/cm^2–pulse. Thus, it is obvious that in order to minimize wafer charging, higher frequency pulses with lower duty cycle is desirable. From CV dots of Al over SiO_2 and an n substrate exposed to the same plasma conditions as that of a typical p+ PIII implant, the oxide breakdown field remains the same as the unexposed control samples at about 8 MV/cm [9]. Almost no difference is seen in CV behavior between MOS capacitors exposed to PIII implant conditions and those unexposed.

2.4. ION ASSISTED VAPOR DEPOSITION

PIII can also be operated with another negatively biased target controlled by a separate power supply, or the triode mode. The target atoms can be sputtered by the carrier gas plasma ions. From the

differential optical emission spectrum of an Ar plasma with a Pd sputtering target, both Pd+ and Pd emission peaks are observed, indicating ionization of the sputtered material in the plasma. In this way, ion assisted physical vapor be realized. If the plasma gas reacts chemically with the sputtered material, ion assisted chemical vapor deposition may also be achieved. This depostion action can occur simultaneously with the implantation of the sputtered material. This mode of PIII operation has been applied to selective electroless copper interconnect plating with Pd seeding [10]. By incorporating Pd ions which were sputtered from a negatively biased target in an Ar plasma, the Pd ions can be implanted into an SiO_2 substrate. Because of the straggle in ion energy distribution, the resulting Pd profile is a gradual transition from a metal-rich SiO_2 surface to pure SiO_2 substrate. Combined with using Si as well in the sputtering target, a Pd/Si alloy was deposited to improve adhesion.

Subsequent Ar bombardment was carried out to facilitate ion beam mixing of the Pd/SiO_2 interface, which also improves the adhesion of the sputtered Pd. Thus, PIII has been demonstrated in ion assisted physical vapor deposition as well as ion beam mixing applications. Furthermore, it is possible to have simultaneous deposition of sputtered material and ion beam mixing action by tailoring the bias waveforms to the target and the substrate.

3. PIII Concerns

3.1. CONTAMINATION

While the "plasma immersion" features of PIII offer advantages in the form of higher throughput and machine simplicity, there are several concerns with placing the substrated directly in the plasma gas. One immediate concern is that since no mass separation is used contaminants can be sputtered from the chamber walls and be deposited or implanted into the substrate. However, the excellent reverse leakage characteristics of p/n junctions fabricated by PIII suggest that at least for BF_3 implantation, implanted contaminants do not significantly affect electrical device performance. If necessary, quartz liners can be used in the reactor to prevent contamination from the reactor fixtures.

3.2. SURFACE BOUNDARY MOVEMENT

Placing the substrate inside the gas plasma may cause the gas to interact either chemically or physically with the wafer surface. We have observed polymer formation on wafers exposed to BF_3 in PIII processing. Similarly, chemical etching may also occur if the gas reacts with the substrate to form a volatile compound. With any low energy, high dose implantation, substrate surface sputtering can also occur. This effect may be complicated by the fact that for PIII implantation, especially with high gas pressures, the energy and angular The combined effects of substrate surface boundary movement on the resulting profile can be modeled by approximating the typical PIII implant (figure 2) by an exponential and convoluting it with a moving surface boundary. As expected, the effects of substrate etching/deposition is more pronounced as the product of the rate of surface variation and the implant time approaches that of the implanted range. Also, for long implant durations, the surface concentration and the implanted dose approach some asymptotic value.

3.3. WAFER HEATING AND SECONDARY ELECTRON GENERATION

The throughput capabilities of PIII may eventually be limited by a number of factors. Significant wafer heating during high current density implantation has been observed with PIII. Thus, wafer cooling mechanisms will need to be installed for very high current implantation. Also, secondary electron generation from implantation may lead to x-ray generation which have adverse effects on SiO_2 integrity. Magnetic field redirection of the secondary electrons away from the chamber walls may be

necessary.

4. Summary

PIII offers new possibilities for modifications of thin-films. Its high dose-rate capabilities and its charge neutralization features alleviate the throughput and charge accumulation problems associated with high dose implantation. Through the use of different gas mixtures or triode operation, concurrent thin-film deposition and ion-beam mixing is also possible. Furthermore, the angular distribution of the incident ions also offers novel processing features. Work is being carried out to better characterize and model the plasma and improve plasma uniformity. Plasma-surface interactions need to be studied to minimize the effects of substrate etching/deposition during implantation. Also, microcontamination in the form of particulates sputtered from somewhere inside the chamber or condensing on the wafer may eventually lead to yeild loss. This, however, is not an intrinsic problem of PIII and can be avoided by careful reactor design and judicious choice of the gases used.

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APPENDIX B

COMPLETE PMOS INTEGRATED CIRCUIT FABRICATION USING PLASMA IMMERSION ION IMPLANTATION OF BF_3

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ABSTRACT

The feasibility of plasma immersion ion implantation (PIII) for multi-implant integrated circuit fabrication is demonstration. Patterned Si wafers were immersed in a plasma containing boron trifluoride (BF_3) ions. Microsecond negative voltage (-2 kV to -30 kV) pulses were applied at a frequency of 100 Hz to 1 kHz to the wafers induced blanket B implants of up to $3X10^{15}$ atoms/cm^2. After implantation the wafers were annealed using rapid thermal annealing (RTA) at 1060°C for 20 seconds to activate the dopants and heal Si wafer damage. Subsequent processing was done to fabricate PMOS test devices in which both the Si wafer and polycrystalline Si (poly-Si) levels were doped using PIII. The functionality of several types of devices, including diodes, capacitors, and transistors, were electrically measured to determine they could withstand the high voltage PIII process.

INTRODUCTION

The drive to fabricate ultra-large-scale integration (ULSI) devices having critical dimensions of 0.25 μm requires the use of shallow (<100 nm) p-n junctions. We are developing a new doping technique called plasma immersion ion implantation (PIII) for this purpose. While several techniques exist for fabricating shallow p-n junctions, including, predeposition sources [1-5], laser assisted doping [6-8], surface layer deposition using chemical-vapor deposition (CVD) [9], and low energy [10,11] or molecular [12,13] ion beam implantation, each has some potential limitation. Wafer doping using predeposition or poly-Si sources is susceptible dopant segregation at interfaces [3,5] which are frequently nonuniform [3]. Laser assisted doping requires the use of reflective coatings, typically of Al [6,8], to reflect unwanted laser power from regions not requiring doping. Both heat stress and metal contamination in the junction are significant concerns. CVD has been shown effective in doping high aspect ratio trenches [9]. However, for p-n junction fabrication it is limited by the dopant solubility limit at the wafer surface in addition to the expected sensitivities to nonuniformities at the Si surface. Shallow p-n junction fabrication by low-energy ion beam implantation is limited by both the lack of readily available sub-10 keV implanters and wafer charging from the constant implant of positive ions and expulsion of secondary electrons. While electron flood guns are being used to counteract this charging [14,15], both electron gun control and the neutralizing of charge

during implantation is hindered by position sensitive charge differences that is expected to become more problematic with the thinner oxides required for 0.25 μm devices.

PIII promises to bypass each of these limitations. Originally developed for metallurgical applications [16,17], PIII uses short (10^{-3} to 10^{-6} sec.) pulses of negative biases (500 V to 100 kV) to implant ions that surround the sample into that sample. The implantation overcomes surface sensitivities and thermodynamic limitations. The critical charge accumulation per unit area that leads to gate oxide damage is avoided by choosing an appropriately short (<10 μsec.) pulse length that limits the implanted ions (~10^{11} ions/cm^2) per pulse. In addition, a net build up of charge is circumvented by the neutralization between pulses by electrons present in the plasma. Finally, with the possibility of high (100 kHz) repetition pulse rates, PIII will be able to achieve a high range of implantation dose rates (10^{11}-10^{16}/cm^2-s).

While PIII may bypass the drawbacks of pre-existing doping techniques, it is not without its own limitations. Obvious ones are the inability to energy or mass select the implant species from the presumably multi-fragmented plasma gas. These issues are fairly innocuous. More important is whether PIII can be used to dope integrated devices without having the high voltage implant pulses degrade sensitive materials such as thin oxides. We are currently evaluating through systematic studies the attributes and limitations of PIII. Earlier we demonstrated that shallow (≤ 100 nm) p^+-n junctions could be fabricated using PIII [18]. We also

reported that low voltage (-2.5 kV) BF_3 PIII-doped diodes had leakages less than 30 nA/cm^2 and that thin (20 nm) oxide MOS capacitors suffered no ill effects due to the PIII process [19].

In this work we have taken the next step by addressing whether PIII can actually be used to make a complete integrated circuit. In doing so, we have taken a conservative approach by using well established technologies for the non-PIII processing steps. We have fabricated individual PMOS devices and integrated circuits using a four mask-set design. We use PIII of BF_3 to dope both the wafer and poly-Si levels and test the functionality of the completed devices and circuits.

EXPERIMENTAL

The PIII system used in this work is an improved version of a previous set up [20]. In PIII the sample to be doped is placed in intimate contact with an electrically isolated Al wafer holder inside a vacuum chamber having a base pressure of $3X10^{-7}$ torr (Fig.1). A plasma containing BF_3 ions is created by an upstream electron-cyclotron-resonance (ECR) source and transported by normal gas flow through the chamber, immersing the sample. The wafer holder is negatively biasing to voltages up to 30 kV for approximately 1 microsecond. During this time, electrons are repulsed and ion accelerated to the wafer where they ballistically implant into the wafer, yielding implant doses of 10^{10}-10^{11} ions/cm^2-pulse. The holder is then returned to ground where electrons from

the plasma return to neutralize any charge built up on the wafer due to the ions. This procedure is repeated at rates up to 1000 times per second to produce the desired doping levels.

The compatibility of PIII for PMOS fabrication was demonstrated using moderately doped (~0.1 Ω-cm), n-type Si(100) wafers as starting material and a process flow as outlined in Figure 2. The doping level of the starting wafers was chosen to allow a bypass of an additional channel implant. A 500 nm field oxide was grown by steam oxidation, patterned, and chemically etched to leave the active regions exposed. A gate oxide of 65 nm was then thermally grown in a dry oxidation furnace. The thickness of the oxide was chosen in order to show sensitivity to subsequent implant damage from subsequent processing. A 350 nm layer of undoped poly-Si was then deposited using low pressure chemical vapor deposition (LPCVD). The poly-Si was then boron-doped using PIII of BF_3 at -2.5 kV with an intended total dose of $5X10^{14}/cm^2$ to $2X10^{15}/cm^2$ as described below.

The B was then activated using a 20 second rapid thermal anneal (RTA) at 1060°C in N_2. The poly-Si/gate oxide film was patterned and reactive ion etched (RIE) leaving regions at the Si wafer level exposed for subsequent doping. The exposed wafer regions were boron doped using PIII of BF_3 at -30 kV. The wafers were again annealed at 1060°C for 20 seconds using RTA to activate the B dopants. Concluding the dopant activation step, an intermediate (350 nm) oxide was deposited. Contact holes were

patterned and wet etched. Finally, a 500 nm thick film of $Al_{99wt\%}Si_{1wt\%}$ was sputter deposited, patterned, and wet etched. The finished wafers contained p^+-n diodes, capacitors, transistors, inverters, and NOR gates with the smallest critical dimension of 2 μm. The devices were electrically measured for functionality.

RESULTS AND DISCUSSION

Previously PIII had been shown effective in doping single crystal Si wafers for the fabrication of sub-100 nm p^+-n junctions [18]. This work has been extended to include two individual implants to dope both the wafer and poly-Si levels. Measurement of test structures for sheet resistance, R_s, of the B activated Si(100) regions gave values of 84 Ω/square to 225 Ω/square, depending on intended dose. Assuming that the energy imparted to boron from the BF_3 molecule during implant is defined by the ratio of the masses (i.e. 15% of the energy goes into boron), TRIMM predicts an implant depth of ~20 nm for an implant voltages of 30 kV (i.e. ~4.5 keV implant energy for boron). It follows that the junction depth is dictated by the thermodynamics of the anneal and not the implant. From previous work [18,19] this depth is ~100 nm. Using the relationship

$$1/R_s = \int \mu e D, \qquad (1)$$

where μ is the hole mobility determined by mobility curves [21], e is the electron charge, and D is the implant dose per square centimeter, the electrical dopant dose is determined to be $5X10^{14}$

to 10^{15} atoms/cm^2. In addition, the sheet resistance of the PIII B-doped poly-Si is measured to be 180 Ω/square to 320 Ω/square. While the poly-Si is not at saturation, these values demonstrate the ability to dope poly-Si using PIII.

The rectifying properties of the p-n junction fabricated by PIII at -30 kV were determined using 50 μm X 50 μm area diodes. Figure 3 shows the diode current under forward and reverse bias conditions. The turn-on voltage is determined to be approximately 0.6 V. At low voltages the forward diode current, I_{FOR}, is given as

$$I_{FOR} = I_o \exp(eV_a/nkT), \qquad (2)$$

where J_o is the pre-exponential factor, V_a is the applied forward bias, n is the ideality factor, and kT is 1/40 eV. At 0.6 V the diode current rises by a factor of ten when the bias was increased by 64 mV (Fig.4). From this the ideality factor is determined to be 1.07. Under reverse bias the reverse leakage current at -5 V was measured to be 2 pA and the reverse breakdown voltage to be -29 V. The leakage current density, equivalent to 80 nA/cm^2, is on the order of expected leakage current densities [11,12]. In comparison with previous PIII fabricated diodes using -2.5 kV implant voltages, it is approximately 3 times higher [18,19]. We attribute the difference to the either perimeter-to-area ratio of the smaller diodes or to processing variables unrelated to the PIII process. We do not expect the higher implant voltage to be a significant difference since the depth of implant from the

molecular plasma is predicted to be only ~20 nm for -30 kV implants.

Earlier we had reported [19] that thin (20 nm) oxides were not degraded from PIII processing for implant voltages up to -8 kV. As an extreme case, we sought to determine whether relatively thick (65 nm) gate oxide capacitors, in which leakage currents are much smaller in comparison to thin (20 nm) oxides, are degraded by the PIII process using a much higher voltage, 30 kV. To address this issue the properties of patterned MOS capacitors were measured after -30 kV BF_3 implants using 200 μm X 200 μm area test structures having an oxide thickness of 65 nm with p^+ poly-Si gates. The capacitance exhibited under high-frequency C-V measurements (Fig.5) was 20 pF in the accumulation mode and 10 pF in the depletion mode. This corresponds to a oxide capacitance of $5X10^{-8}$ F/cm^2 and a the n-type substrate having a doping level of ~$3X10^{16}/cm^3$. No change was seen in the effective dopant levels below the oxide as determined by the depletion width. The breakdown characteristics of the 65 nm oxides are shown in Figure 6. The gate oxide dielectric breakdown field is determined to be 8 MV/cm. This high field implies that the oxide was not damaged to first order. In addition, the breakdown characteristics of the gate oxide are asymmetric with the lowest breakdown voltage occurring in the forward bias mode as expected due to the additional depletion width capacitance in the reverse bias mode.

Another important issue is whether transistors can be

successfully fabricated using the PIII process for both p^+ source and drain regions and p^+ poly-Si gates. PMOS transistors were fabricated and tested to determine their functionality. Figure 7 shows the characteristic source-drain current, I_{DS}, as a function of source-drain voltage, V_{DS}, for increasing amounts of negative gate bias, V_G. In this case, the transistor gate width, W_{eff}, is 15 μm and the gate length, L_{eff}, is 2 μm. The source-drain current is given as

$$I_{DS} = (W_{eff}/L_{eff})\mu_{eff}C_{ox}[(V_G-V_T)V_{DS}-V_{DS}^2/2], \quad (3)$$

where μ_{eff} is the effective hole mobility, C_{ox} is the gate oxide capacitance, and V_T is the threshold voltage. At saturation I_{DS} is approximated by

$$I_{DS} = (W_{eff}/2L_{eff})\mu_{eff}C_{ox}(V_G-V_T)^2. \quad (4)$$

Figure 8 shows a plot of the square root of I_{DS} versus V_G. By finding the y-axis intercept, we determine V_{T0} to be -1.70. This V_{T0} value matches that predicted by Sze [22] for a 65 nm oxide having a p^+ poly-Si gate. The effective hole mobility in the saturation region is determined to be 310 $cm^2/V\text{-}s$. At low values of V_{DS}, the first term in Eqn.3 dominates. In this region the effective hole mobility was extracted to be 180 $cm^2/V\text{-}s$. In addition, at low V_{DS} the transconductance, g_m, is given by

$$g_m = \partial I_{DS}/\partial V_G = \mu_{eff}C_{ox}(W_{eff}/2L_{eff})V_{DS}. \quad (5)$$

The value predicted by eqn.5, 6.6 μA/V (i.e. 44 mS/mm) at V_{DS} = 0.1

V, agrees extremely well with the 6.4 μA/V measured directly at the its peak at V_G ~2.2 V (Fig.9) and is comparable to those extrapolated from the literature [12,23] on shallow junctions.

Finally, to demonstrate that PIII can be used in the processing of complete integrated circuits, two types of PMOS IC's were fabricated using PIII and tested for functionality. The two types of IC's are an inverter and a NOR gate in which both the wafer and poly-Si levels were boron doped using the PIII process. Figure 10a shows the voltage response of the inverter to the input voltage. Similarly, the voltage output of the NOR gate is plotted as a function of input voltage in Fig.10b for 0 V and -5 V applications to the secondary input. We find that both circuits produce the desired outputs, demonstrating that the PIII process can be used to fabricate complete integrated circuits.

CONCLUSION

Plasma immersion ion implantation, a process that uses microsecond pulses of voltage potential to implant ions from a plasma into materials, has been applied to the fabrication both single Si devices and integrated circuits. Both single crystal Si substrates and poly-Si films were boron doped by PIII of BF_3 and subsequently used as materials in p^+-n junction diodes and MOS transistors. The diodes exhibited near ideal performance and the capacitors showed no signs of degradation in terms of capacitance and dielectric breakdown measurements due to the PIII process

using pulse voltages of -30 kV. Transistors using both wafer and poly-Si level doping by PIII of BF_3 as the electrically active materials were shown to be functional with the expected response characteristics. Finally, complete integrated circuits were fabricated for the first time using PIII, showing that PIII can be used for complete IC fabrication.

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FIGURES

Figure 1- Schematic diagram of the plasma immersion ion implantation system.

Figure 2- Outline of process flow for device fabrication.

Figure 3- Diode current as a function of forward and reverse bias.

Figure 4- Diode current for small forward biases.

Figure 5- High frequency capacitance-voltage of the 65 nm gate oxide as a function of p^+ poly-Si gate voltage.

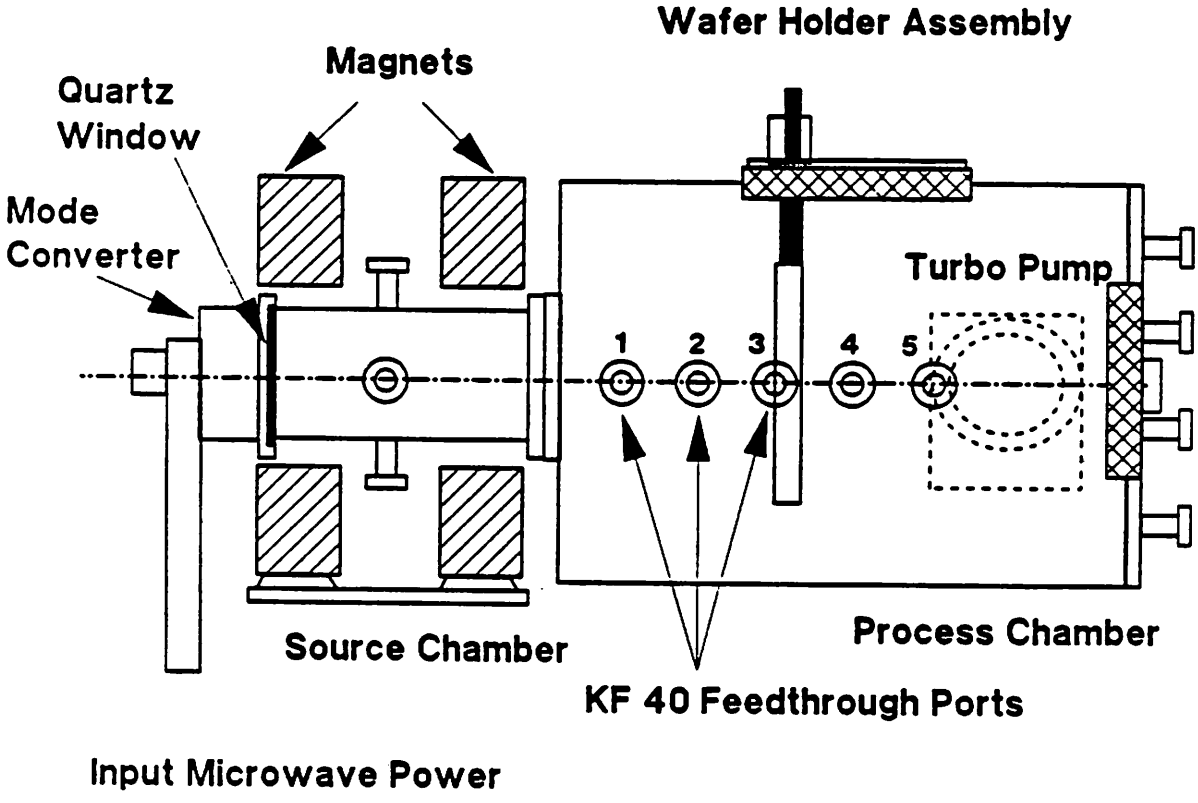
Figure 6- Gate oxide current leakage and current breakdown as a function of forward and reverse biases.

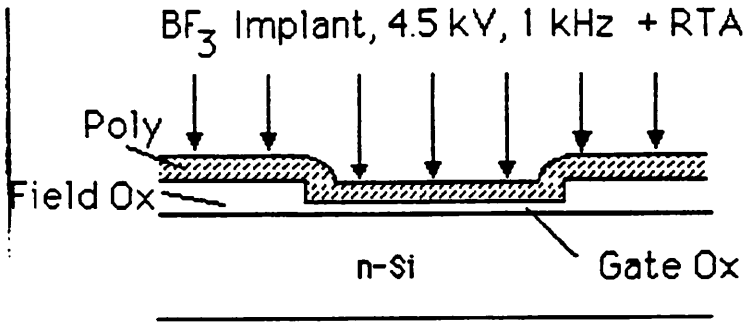
Figure 7- Transistor drain-source current as a function of applied drain-source voltage. Each curve represents gate bias increments of 0.5 V, with the top curve corresponding to a gate voltage of -5 V.

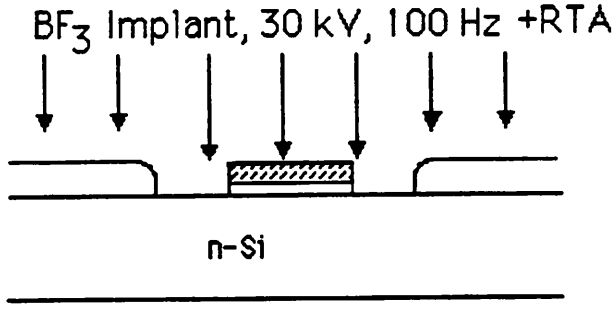
Figure 8- The square root of the transistor drain-source current as a function of gate voltage. Each curve represents substrate bias increments of 1 V, with the first curve corresponding to a gate voltage of 0 V.

Figure 9- The transistor's transconductance as a function of gate voltage. Each curve represents increased source-drain voltage increments of -0.1 V, with the top curve corresponding to a gate voltage of -0.5 V.

Figure 10- The output voltage dependence as a function of input voltage of a) an inverter and b) a NOR gate (top curve represents a -5 V input to the second input).


Wafer Holder Assembly
Magnets
Quartz
Window
Mode
Converter
Turbo Pump
1
2
3
4
5
Source Chamber
Process Chamber
KF 40 Feedthrough Ports
Input Microwave Power


BF_3 Implant, 4.5 kV, 1 kHz + RTA
Poly
Field Ox
n-Si
Gate Ox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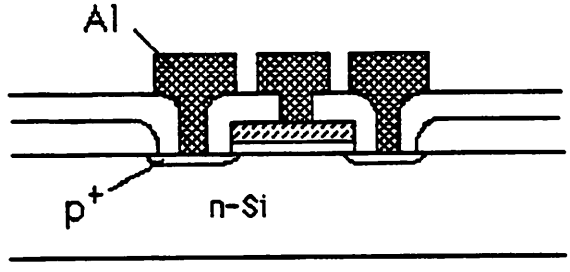
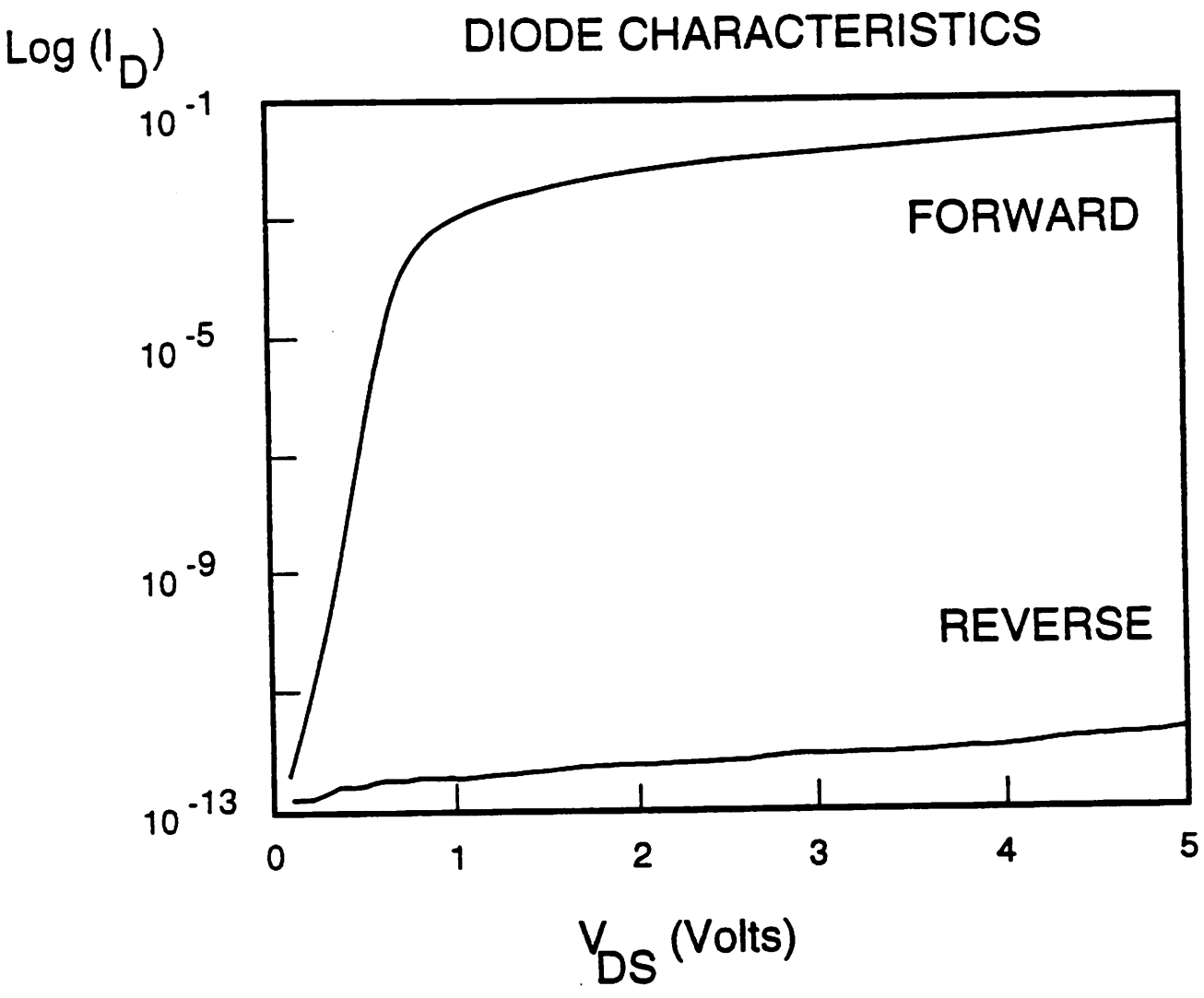
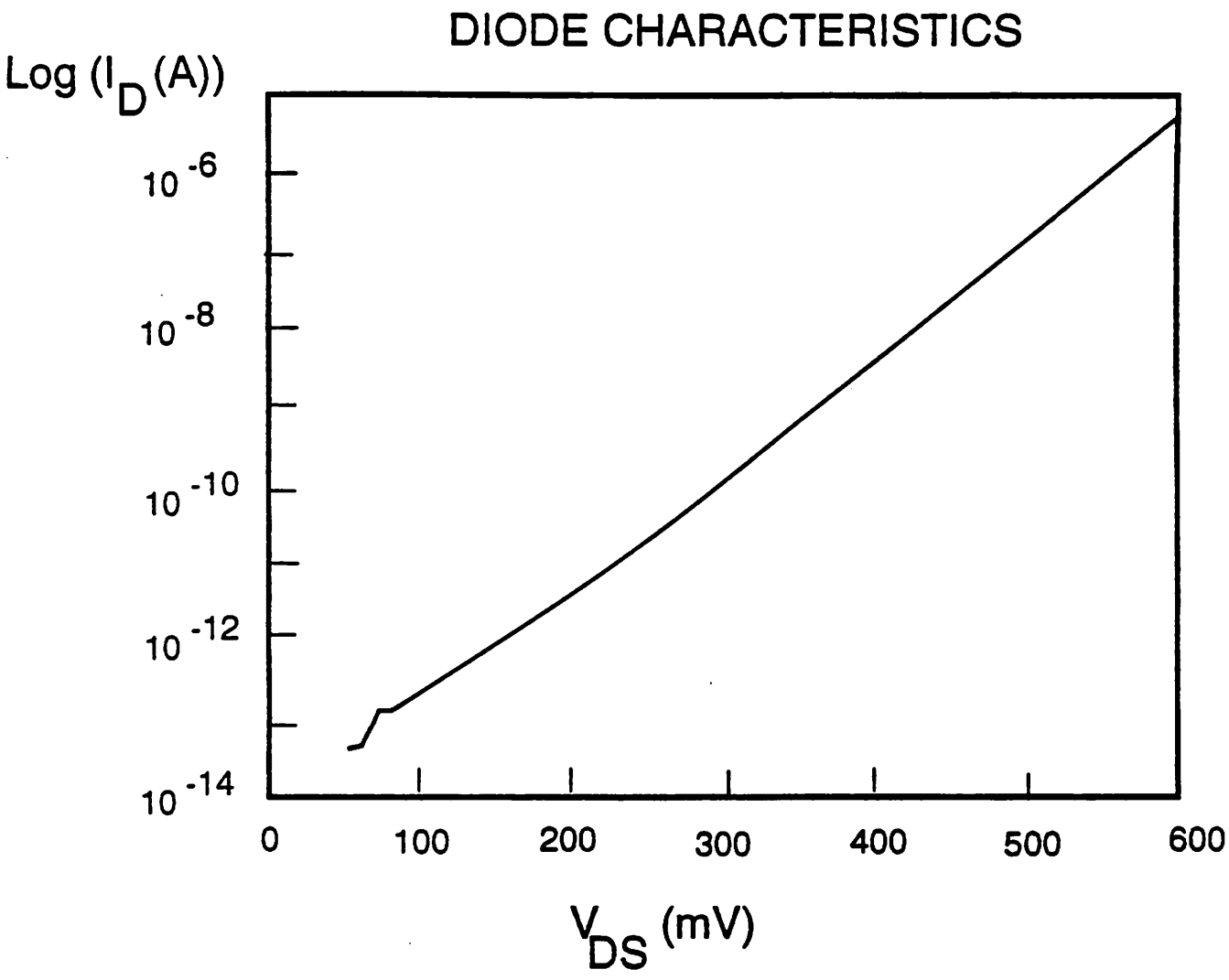
n-Si


Al
p^+
n-Si


DIODE CHARACTERISTICS
Log (I_D)
10^{-1}
10^{-5}
10^{-9}
10^{-13}
FORWARD
REVERSE
0
1
2
3
4
5
V_{DS} (Volts)


DIODE CHARACTERISTICS
Log (I_D (A))
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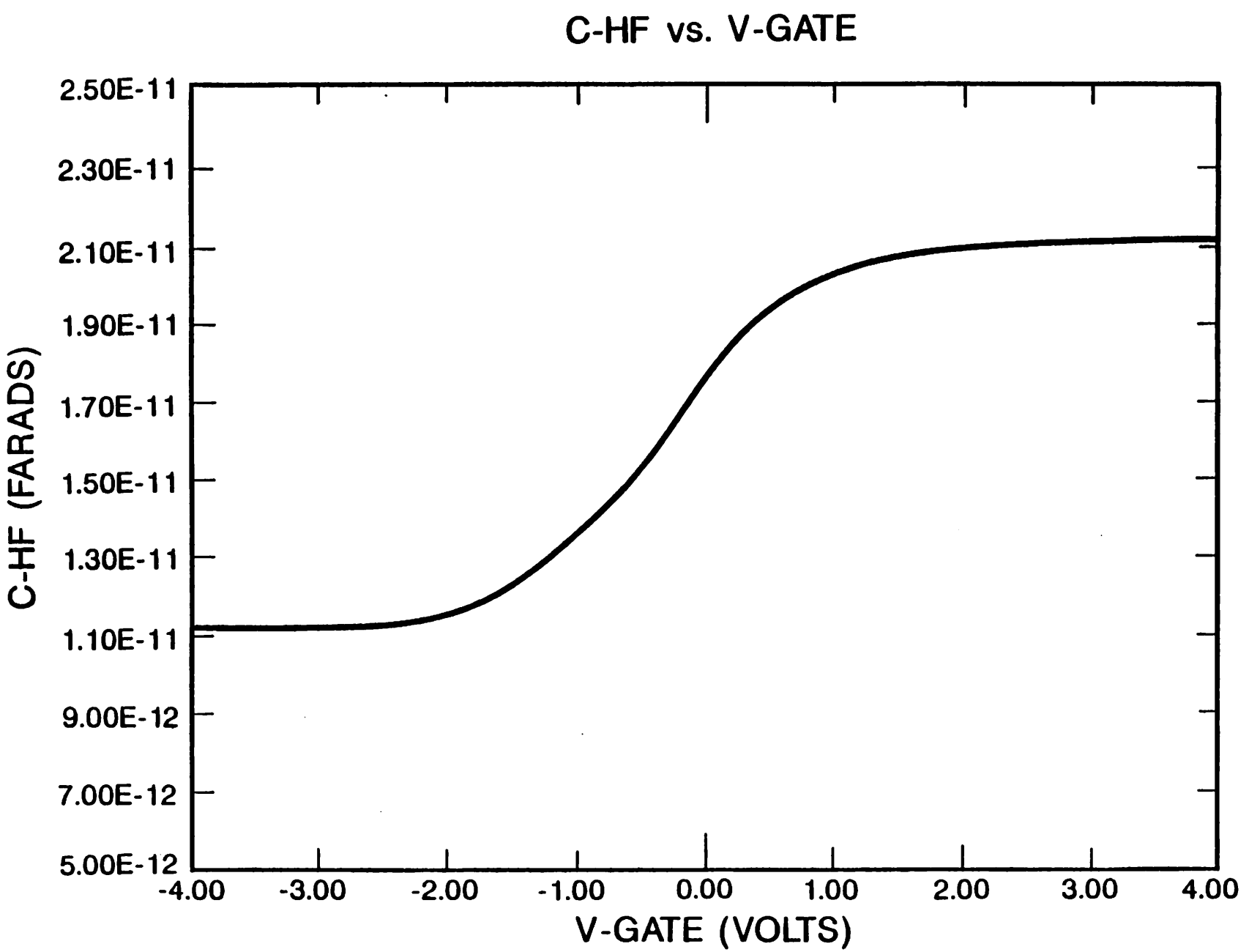
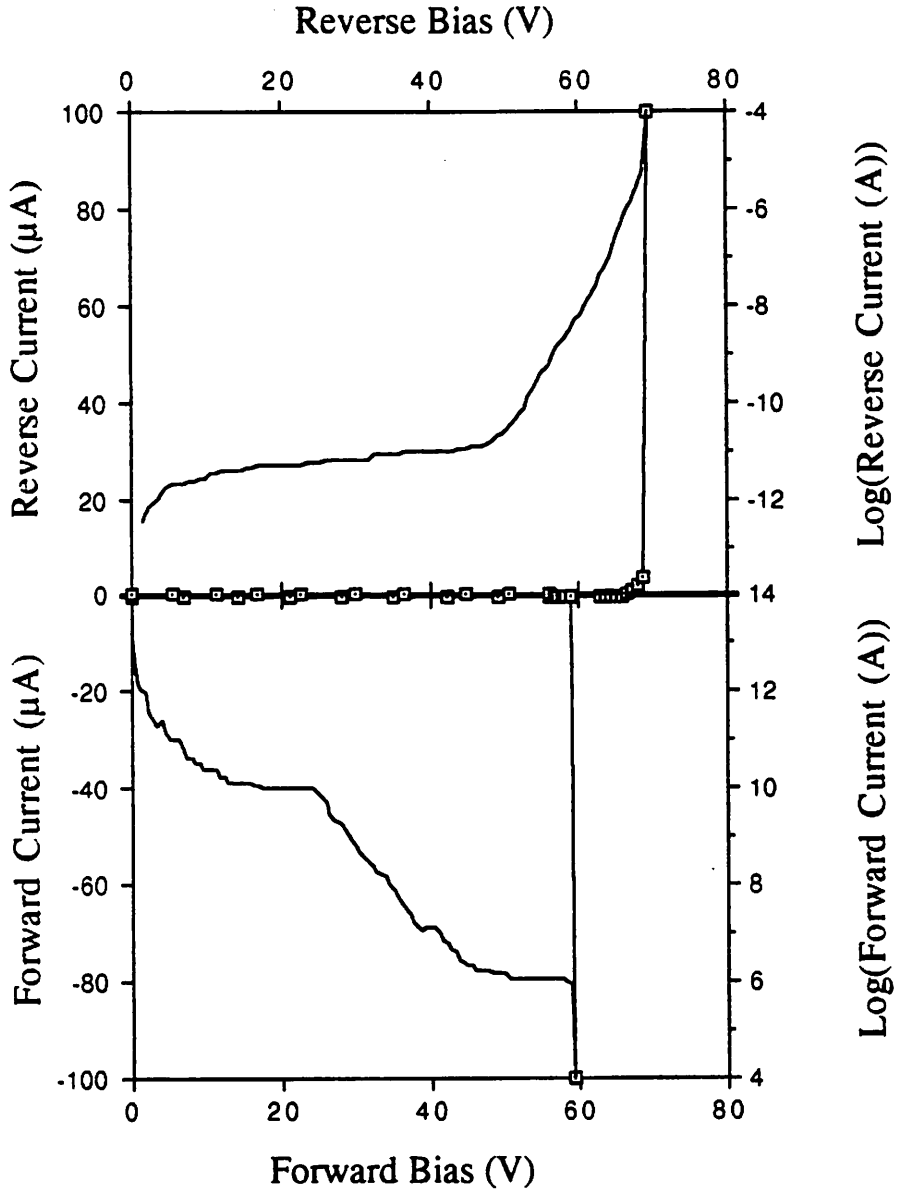
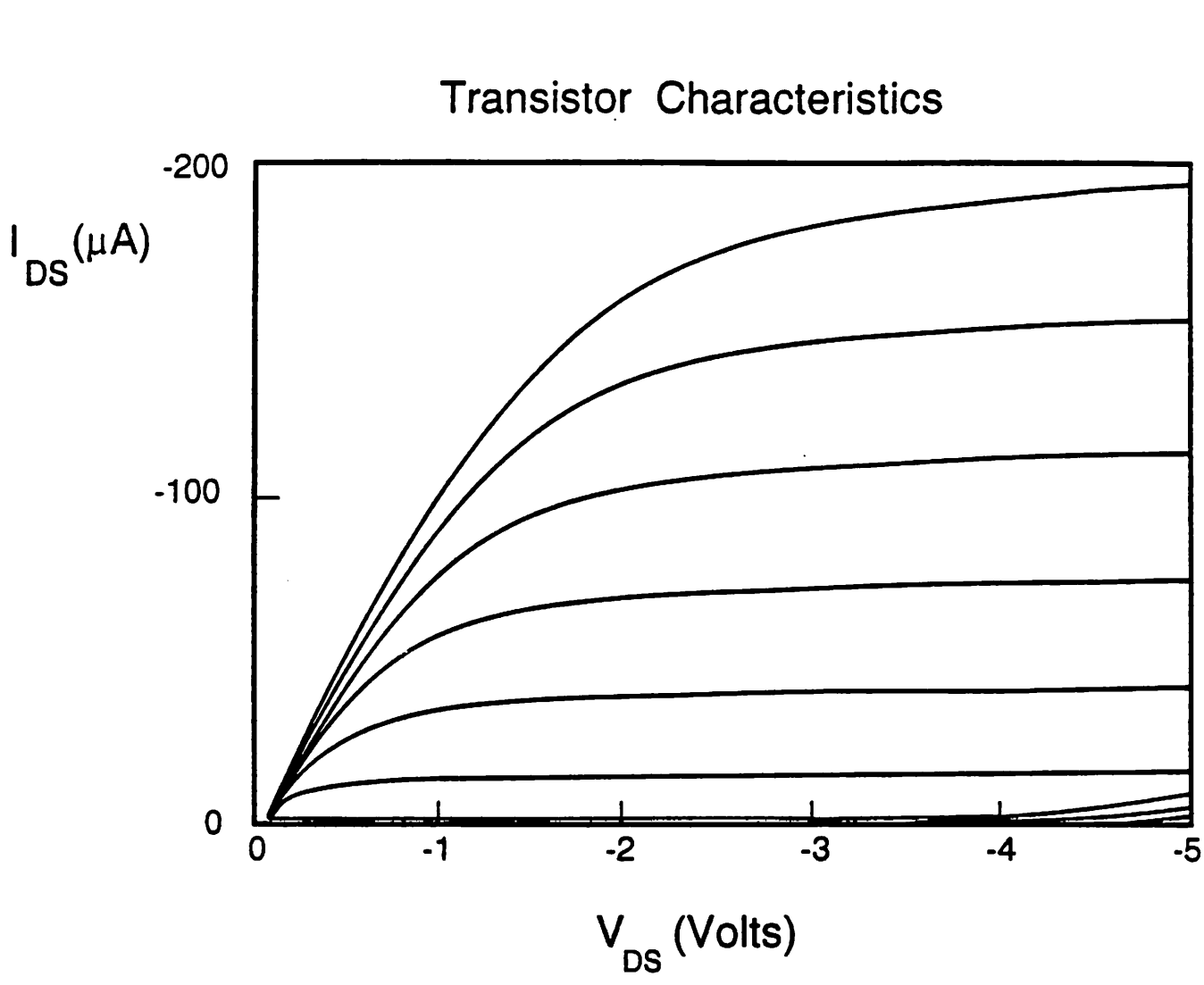
10^{-8}
10^{-10}
10^{-12}
10^{-14}
0
100
200
300
400
500
600
V_{DS} (mV)


C-HF vs. V-GATE
2.50E-11
2.30E-11
2.10E-11
1.90E-11
1.70E-11
1.50E-11
1.30E-11
1.10E-11
9.00E-12
7.00E-12
5.00E-12
C-HF (FARADS)
-4.00
-3.00
-2.00
-1.00
0.00
1.00
2.00
3.00
4.00
V-GATE (VOLTS)


Reverse Bias (V)
0
20
40
60
80
100
80
60
40
20
0
-20
-40
-60
-80
-100
Reverse Current (μA)
Forward Current (μA)
-4
-6
-8
-10
-12
14
12
10
8
6
4
Log(Reverse Current (A))
Log(Forward Current (A))
0
20
40
60
80
Forward Bias (V)


Transistor Characteristics
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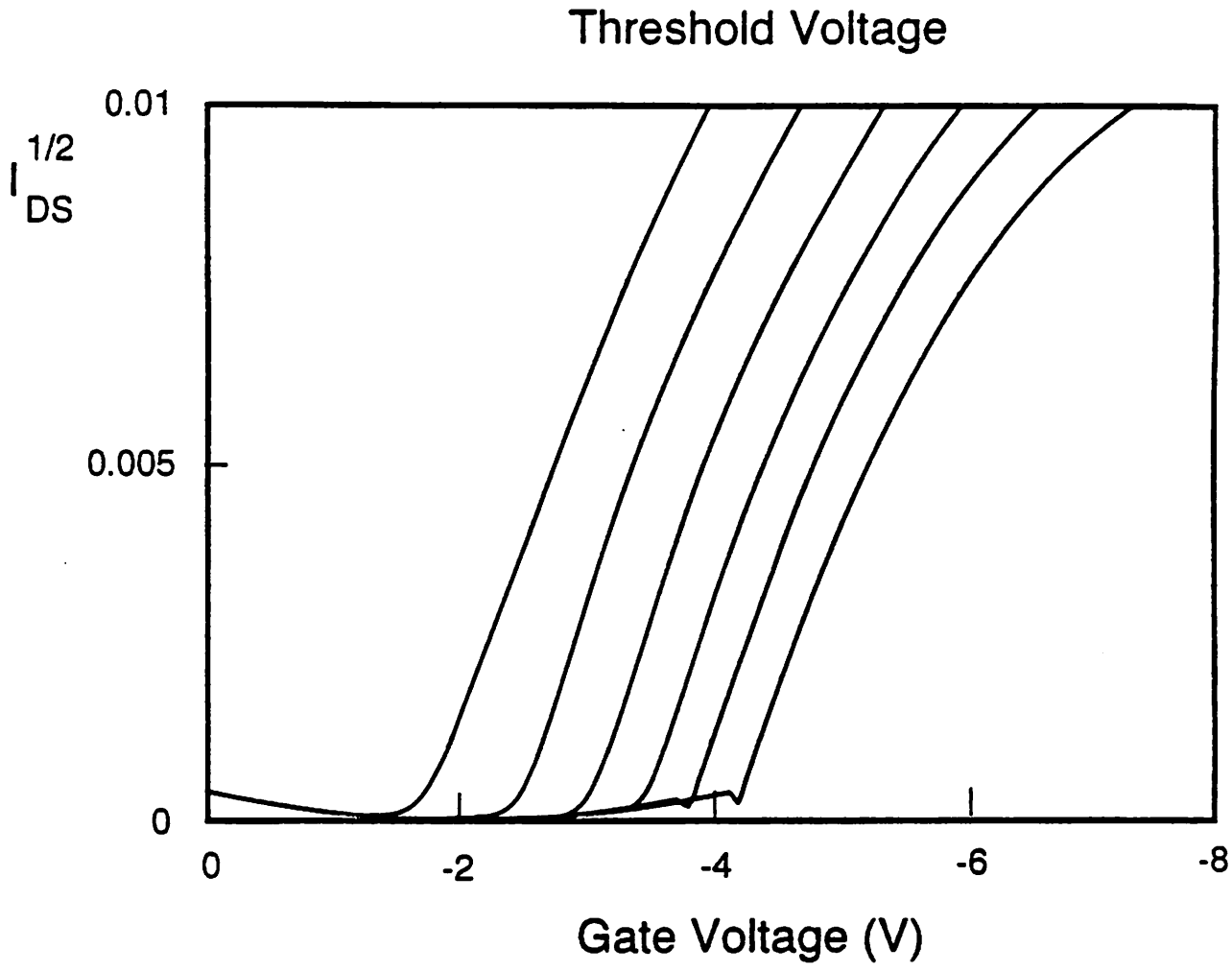
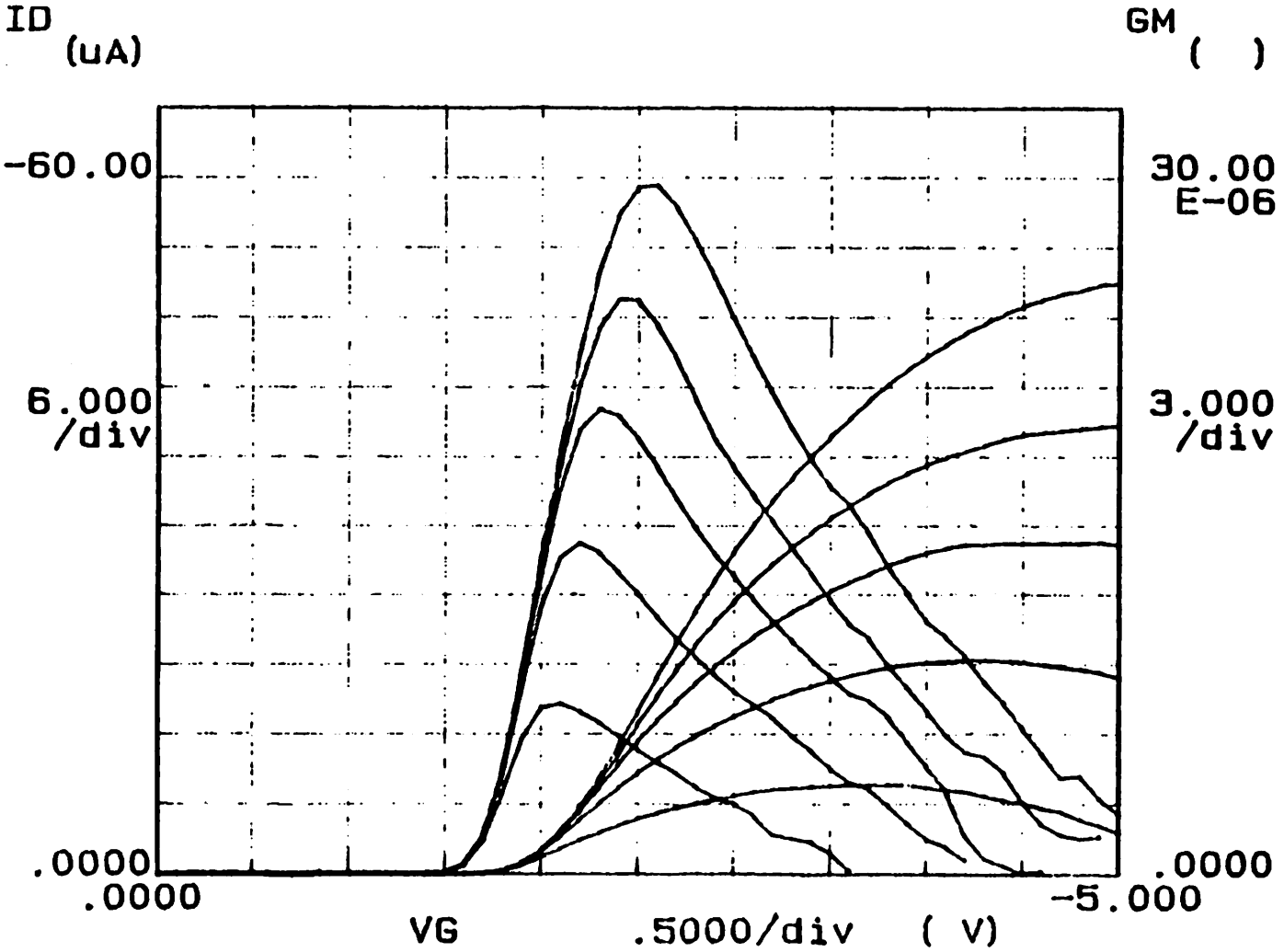
I_{DS} (μA)
-100
0
0
-1
-2
-3
-4
-5
V_{DS} (Volts)


Threshold Voltage
0.01
$I_{DS}^{1/2}$
0.005
0
0
-2
-4
-6
-8
Gate Voltage (V)

****** GRAPHICS PLOT ******

143-3 2u TRANS AFT SINTER

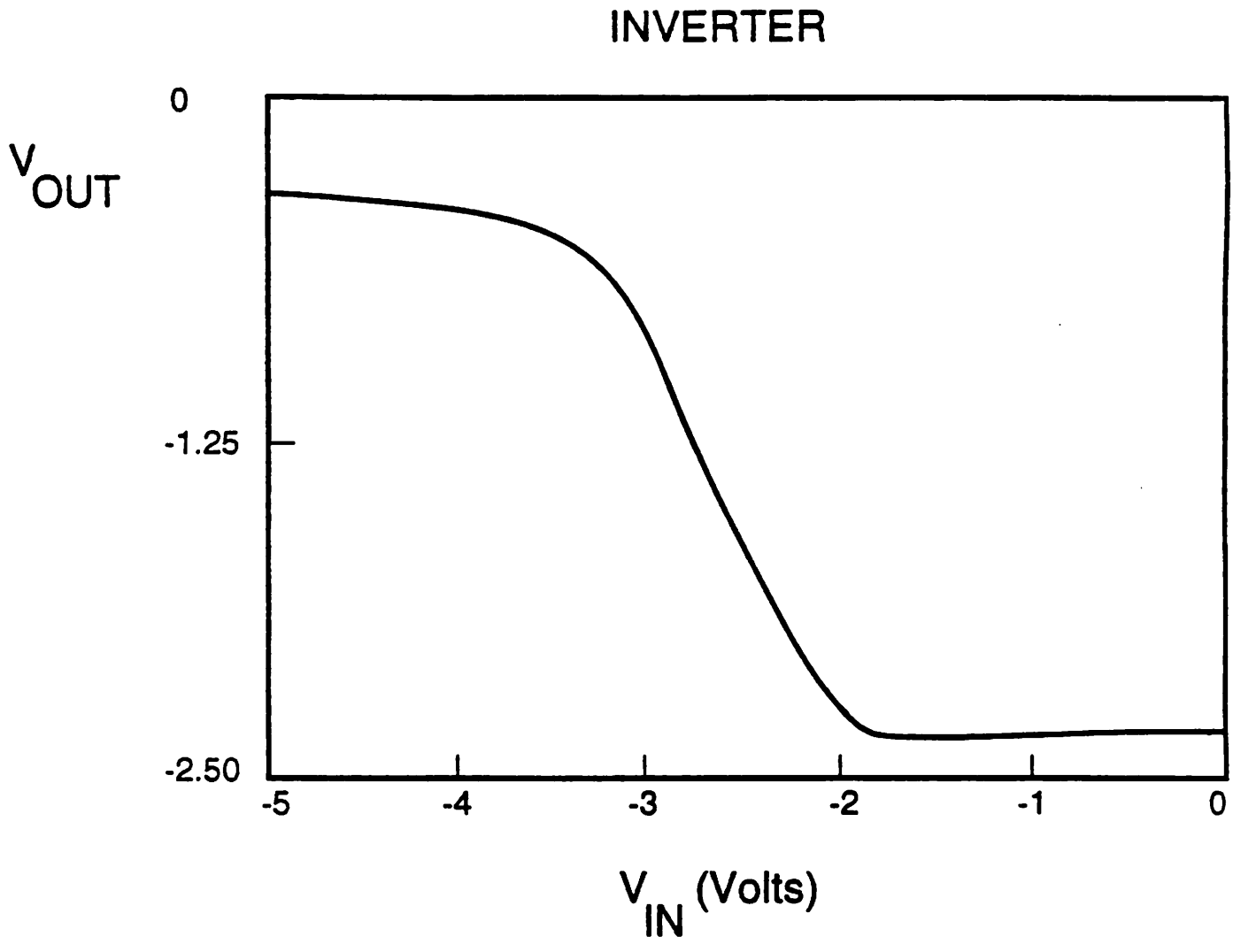


Variable1:
VG -Ch3
Linear sweep
Start .0000V
Stop -8.0000V
Step - .1000V

Variable2:
VD -Ch2
Start .0000V
Stop - .5000V
Step - .1000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V

SQRT ( ) = √ID
GM ( ) = ΔID/ΔVG


INVERTER
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V_{OUT}
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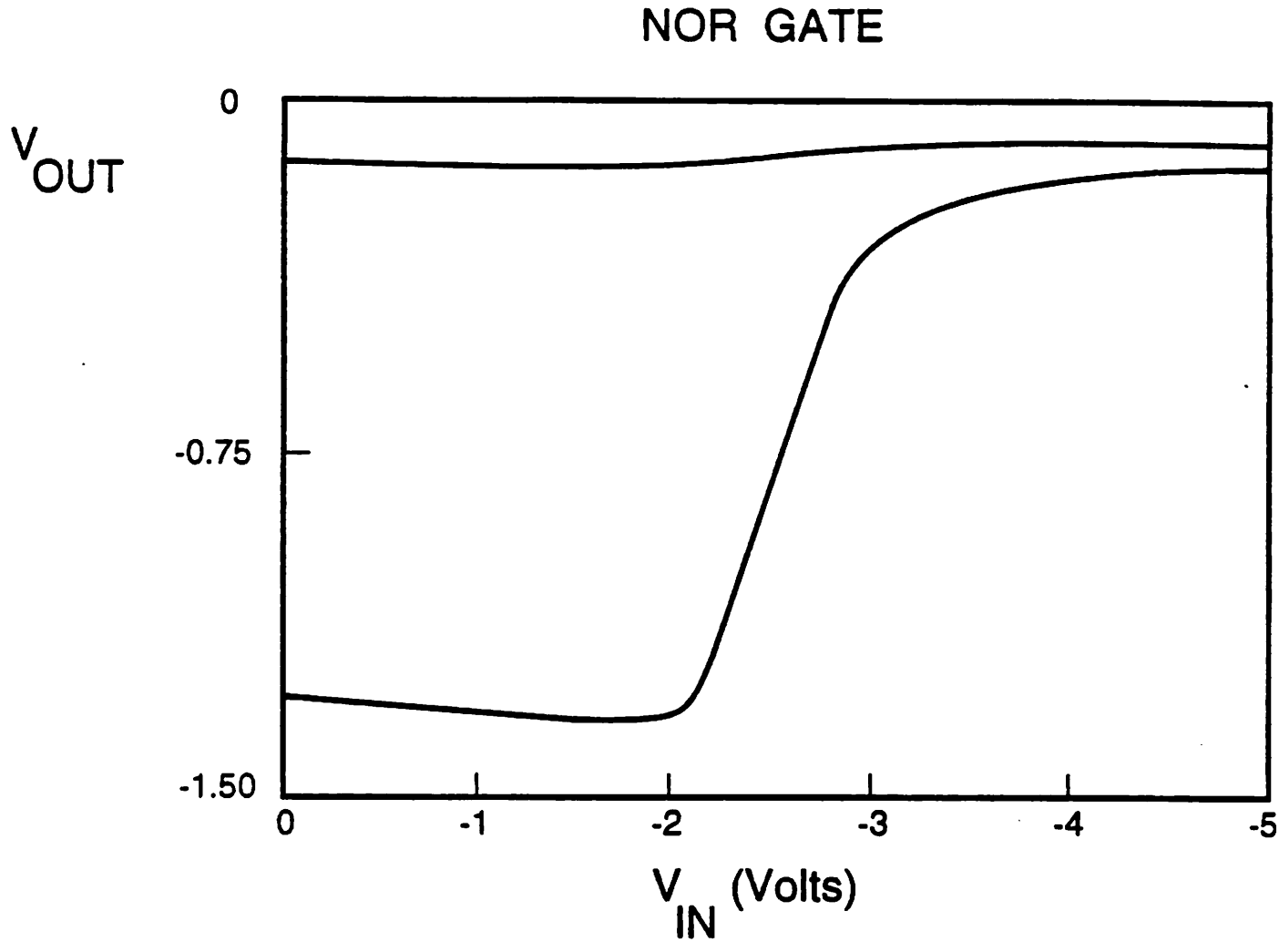
-2.50
-5
-4
-3
-2
-1
0
V_{IN} (Volts)


NOR GATE
V_{OUT}
0
-0.75
-1.50
0
-1
-2
-3
-4
-5
V_{IN} (Volts)