AN INTRODUCTION TO SEMICONDUCTOR MANUFACTURING AND MARKETS

by

Patricia K. Schank and Lawrence A. Rowe

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ELECTRONICS RESEARCH LABORATORY

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An Introduction to Semiconductor Manufacturing and Markets[1]

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Abstract

This paper summarizes the material presented in a multimedia course on integrated circuits, called IC-HIP, that we developed using Hypermedia in Picasso (HIP). IC-HIP offers an online text, image, and video introduction to semiconductor manufacturing and markets.

Introduction

IC-HIP is an introductory course on semiconductor manufacturing that we developed using Hypermedia in PICASSO (HIP), a hypermedia extension of the PICASSO graphical user interface environment (Becker & Rowe, 1990). IC-HIP integrates a variety of multimedia information about integrated circuits, such as: 1) textual descriptions of the history and evolution of IC's, the stages of IC design and manufacturing, the Berkeley Microfabrication Facility, software systems used in IC manufacturing, and the world-wide IC markets; 2) video sequences of introductory lectures (from EECS 143, "Processing and Design of Integrated Circuits") about IC fabrication steps, equipment used at the various steps, and economic issues; 3) video tours of the Berkeley Microfabrication Facility; 4) images of wafer profiles after various steps of the manufacturing process; and 5) cross-refenced instructional materials for formal specifications of each step of a simple fabrication process (e.g., process step parameters, equipment use, and wafer profiles after a particular step), specified in the Berkeley Process Flow Language (BPFL). A sample screen from IC-HIP is shown in Figure 1. This paper is a textual verion of IC-HIP.

In IC-HIP, segments of information (e.g., images, vidoe clips, textual descriptions) are stored in "nodes", and cross-references between information are implemented as links between nodes. Throughout this paper, each figure, table, and section of text below bold headings typically represents one IC-HIP node. (Node names are indicated in right-justified caps. While video nodes cannot be represented, nodes from which IC-HIP video segments can be viewed are marked with a '*' by the node name; e.g., *FAB-8.) We have implemented a number of "paths" in IC-HIP for students who prefer a more structured, guided tour of the material, and represent these paths by lists of sequential node names (see Table 1). This paper reflects path 5, the "Complete tutorial", shown in Table 1. Appendix A contains a list of all IC-HIP text, image, and video nodes, and their links.

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1. This research was supported by NSF grant MIP-9014940 and a grant from the Semiconductor Research Corporation.

Figure 1. Sample screen

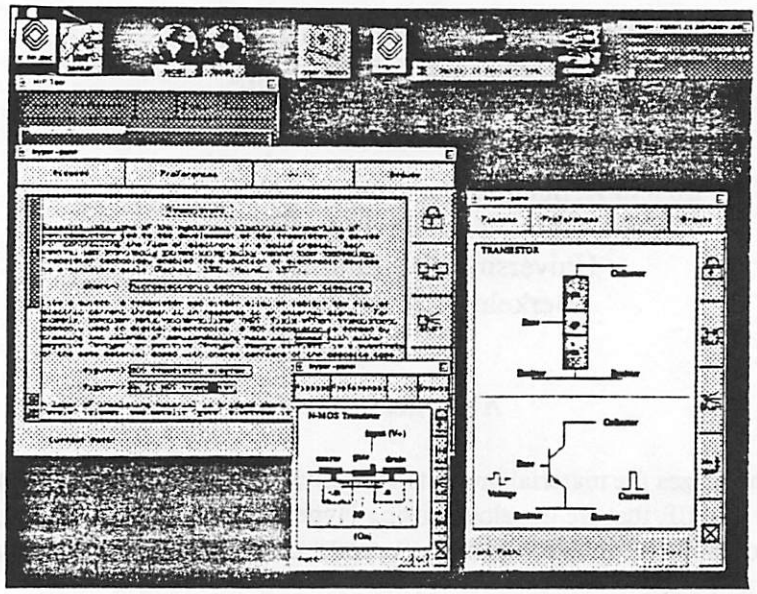


Table 1. Pre-defined paths through IC-HIP

1. Introduction to IC elements: (INTRO-0 ELEM-0 ELEM-7 ELEM-1 TRANSPIC ELEM-4 PHOSDOPE ELEM-5 ELEM-8 ELEM-6 ELEM-9 ELEM-11 ELEM-10)
2. Introduction to IC fabrication: (INTRO-0 FAB-0 CYLINDER FAB-6 FAB-1 FAB-7 FURNACE FAB-14 FAB-8 LITHSTAGES SPIN-ON FAB-9 FAB-10 PHOTOMASK FAB-11 SEM FAB-12 DOPE FAB-13 DEP FAB-2 TEST FAB-3 ASSEMBLY FAB-4 SORT FAB-5)
3. Introduction to software for IC manufacturing: (INTRO-0 CIM-0 CIM-5 CIM-1 CIM-2 CIM-3 SAMPLE CIM-4 CIM-6)
4. Iintroduction to the UCB Microlab: (INTRO-0 MICROLAB-0 MICROLAB-1 MICROLAB-2 FAB-14 FAB-5 MICROLAB-3 MICROLAB-4 CIMTOOL)
5. Introduction to IC markets: (INTRO-0 MARKETS-0 MARKETS-1 MARKETS-2 YIELD MARKETS-10 MARKETS-3 PRODGRAPH RD-GRAPH EQUIPGRAPH MARKETS-4 MARKETS-5 MARKETS-6 MARKETS-7 MARKETS-8 MARKETS-9 MARKETS-10)
6. Complete tutorial: (INTRO-0 ELEM-0 ELEM-7 ELEM-1 TRANSPIC ELEM-4 PHOSDOPE ELEM-5 ELEM-8 ELEM-6 ELEM-9 ELEM-11 ELEM-10 FAB-0 CYLINDER FAB-6 FAB-1 FAB-7 FURNACE FAB-14 FAB-8 LITHSTAGES SPIN-ON FAB-9 FAB-10 PHOTOMASK FAB-11 SEM FAB-12 DOPE FAB-13 DEP FAB-2 TEST FAB-3 ASSEMBLY FAB-4 SORT FAB-5 CIM-0 CIM-5 CIM-1 CIM-2 CIM-3 SAMPLE CIM-4 CIM-6 MICROLAB-0 MICROLAB-1 MICROLAB-2 FAB-14 FAB-5 MICROLAB-3 MICROLAB-4 CIMTOOL MARKETS-0 MARKETS-1 MARKETS-2 YIELD MARKETS-10 MARKETS-3 PRODGRAPH RD-GRAPH EQUIPGRAPH MARKETS-4 MARKETS-5 MARKETS-6 MARKETS-7 MARKETS-8 MARKETS-9 MARKETS-10)

Course Content INTRO-0

The IC-HIP course, and this paper, cover the following topics:

(1) A review of IC circuit elements and evolution

(2) IC Manufacturing, including

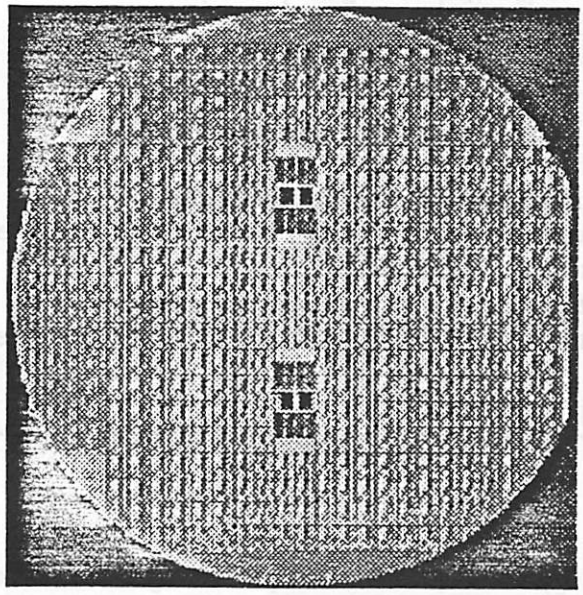
Stages of IC design and manufacturing

Software systems for IC manufacturing

The Berkeley Microfarication Laboratory

(3) World-wide IC markets

Figure 2. Silicon wafer with 470 computer chips **WAFER**



1. A Review of Microelectronic Circuit Elements ELEM-0

Electronic devices are made of active circuit elements like transistors, and passive elements like resistors and capacitors (e.g., Meindl, 1977). Before the advent of microelectronic technology, these basic functional units were manufactured separately and wired together with metallic conductors to form electronic devices (e.g., Rockett, 1991; McCanny & White, 1987; see Table 2).

Table 2. Electronic Technology Evolution Timeline **ELEM-7**

1900's: The Vacuum Tube.
1905 First electronic diode vacuum tube is built by English physicist J. Ambrose Fleming, allowing the change of alternating current into a direct one-way signal.
1906 First electronic triode vacuum tube is built by American electrical engineer Lee DeForest, allowing signals to be controlled and amplified. Technology of electronics is born.
Late 1940's, early 1950's: The Transistor.
1947 The point-contact bipolar transistor is invented by Bell Lab's Bardeen, Shockley, and Brattain.
1951 Junction field-effect transistor (JFET) is invented.
1952 Single-crystal silicon is fabricated.
1954 Oxide masking process is developed.
Late 1950s: Key IC discoveries.
1958 First silicon integrated circuit is built by Texas Instrument's Jack Kirby.
1959 Planar process to distribute transistors on silicon, with passive oxide layers to protect junctions, is developed by Fairchild Semiconductor's Noyce and Moore. A modern version of this process is used today.
1960's: Small Scale Integration (SSI), up to 20 gates per chip.
1960 Metal-Oxide-Silicon (MOS) transistor is invented.
1962 Transistor-transistor Logic (TTL) is developed.
1963 Complementary Metal Oxide Silicon (CMOS) is invented.
Late 1960's: Medium Scale Integration (MSI), 20-200 gates per chip.
1968 MOS memory circuits are introduced.
1970's: Large Scale Integration (LSI), 200-5000 gates per chip.
1970 8-bit MOS calculator chips are introduced, 7 micrometer chip geometries.
1971 16-bit Microprocessors are introduced.
1980's: Very Large Scale Integration (VLSI), over 5000 gates per chip.
1981 Very High Speed Integration (VHSIC), tens's of thousands of gates per chip, 1.5 micrometer chip geometries.
1984 0.5 micrometer chip geometries.

Circuit Elements

Microelectronic technology has not, for the most part, changed the nature of these basic functional units. Rather, it has made these electronic functions more reproducible, more reliable, and less expensive by fabricating miniaturized versions of them on a single semiconducting substrate of silicon or (less commonly) gallium arsenide. As a result, a growing number of logic circuits have been implemented using the basic circuit elements that are most easily fabricated in silicon and perform best: transistors.

Transistors *ELEM-1

Research into some of the mysterious electrical properties of semiconductors led to the development of the transistor, a device for controlling the flow of electrons in a solid crystal. Such control was previously gained using bulky vacuum tube technology. Transistor technology enabled the reduction of electronic devices to a miniature scale (Rockett, 1991; Meindl, 1977).

Like a switch, a transistor can either allow or inhibit the flow of electric current through it in response to an external signal. For example, consider metal-oxide-silicon (MOS) field effect transistors, commonly used in digital electronics. A MOS transistor is formed by creating two islands of semiconducting material, doped with either negative "N-type" or positive "P-type" charge carriers, in a substrate of the same material doped with charge carriers of the opTosite type.

Figure 3. MOS transistor diagram (symbol) **TRANSCIRCUIT**

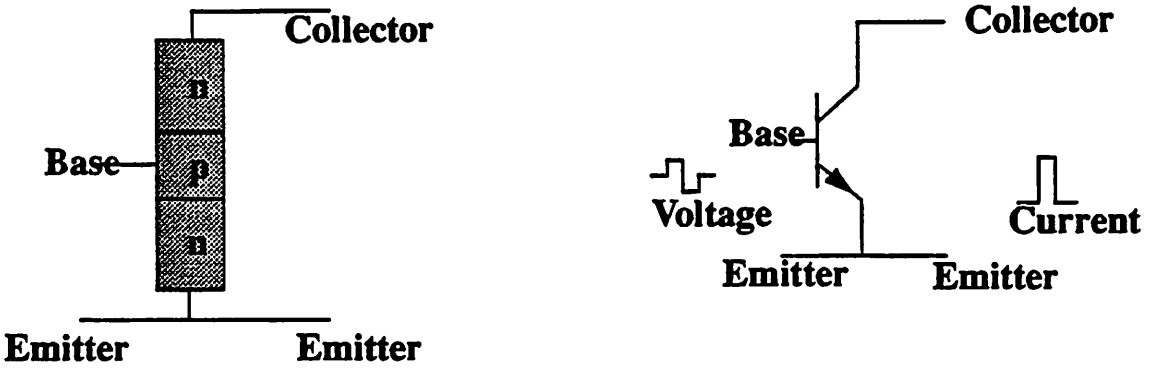
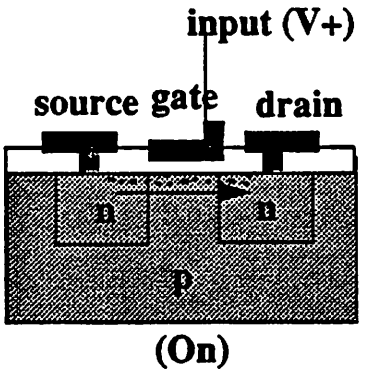


Figure 4. IC NMOS transistor (microelectronic component) **TRANSPIC**



A layer of insulating material is bridged above these "source" and "drain" islands, and metalic "gate" electrode is deposited on the insulator. By alternating the voltage applied to the gate, charge carriers from the source are either attracted toward the channel under the gate, or repelled from it. When several charge carriers are attracted toward the region under the gate, an induced channel is formed that allows charge carriers to travel all the way across the gate region and into the drain region. Another common transistor, the bipolar transistor, is formed by sandwiching a thin layer of P- or N-type semiconductor between two regions of the opposite type of semiconductor. (Bate,

1988; Meindl, 1977, 1987).

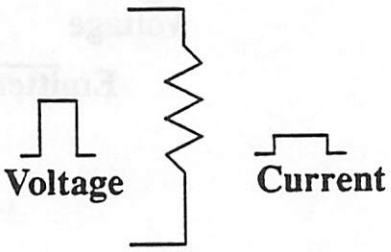
By connecting together several transistors, logic signals can be sent to the next stage of a circuit. In this way, large circuits that remember voltages (e.g., Static and Dynamic Random Access Memories, SRAMs and DRAMs), or make complex switching decisions based on memories and other inputs, are created (Hodges, 1977; Mayo, 1977).

Resistors

ELEM-2

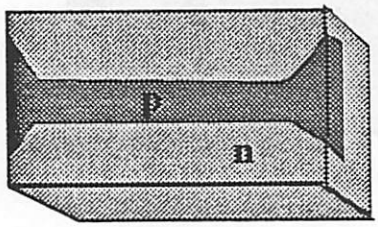
The electrical resistance of a material is a measure of how difficult it is for electric current to flow through the atomic structure of a material. A resistor is an electronic circuit element with a fixed amount of resistance to current flow. Resistors are used to create a voltage drop to meet the voltage requirements of the electrical device through which the electric current is flowing.

Figure 5. Resistor diagram (symbol) **RESISTORCIRCUIT**



A microelectronic resistor is commonly formed by creating a thin ribbon of semiconducting material, doped with either negative "N-type" or positive "P-type" charge carriers, in a region doped with charge carriers of the opposite type (Meindl, 1977).

Figure 6. An IC resistor (microelectronic component) **RESISTORPIC**

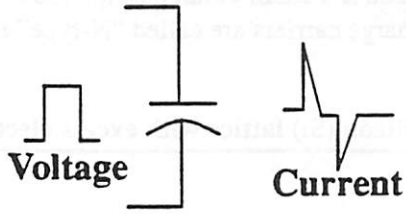


Capacitors

ELEM-3

Capacitance is a measure of the strength of the electric field surrounding a conductor. A capacitor is a passive electronic circuit element with the ability to store electrical charge. Capacitors can be used to change alternating current (AC, what comes out of electrical wall outlets) into stored direct current (DC, like in a battery). This stored electrical energy can then be used to drive the operation of electrical devices.

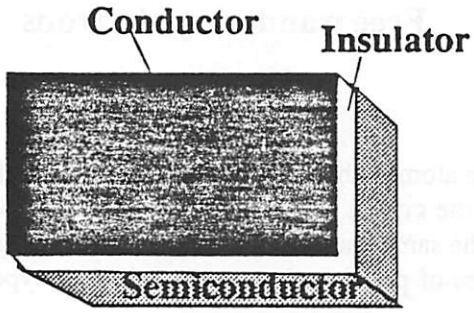
Figure 7. Capacitor diagram (symbol) **CAPCIRCUIT**



Capacitance, or stored electrical charge, is increased when large areas of conductors bearing opposite electrical charges are brought close together. Discrete capacitors are often made of metal plates separated by a thin insulating layer.

In a microelectronic circuit, a capacitor is commonly created by forming a thin layer of insulator on the surface of a doped semiconducting material, followed by a deposited layer of metal. Only very small values of capacitance can be created this way (Meindl, 1977).

Figure 8. IC capacitor (microelectronic component) **CAPPIC**



Semiconductors **ELEM-4**

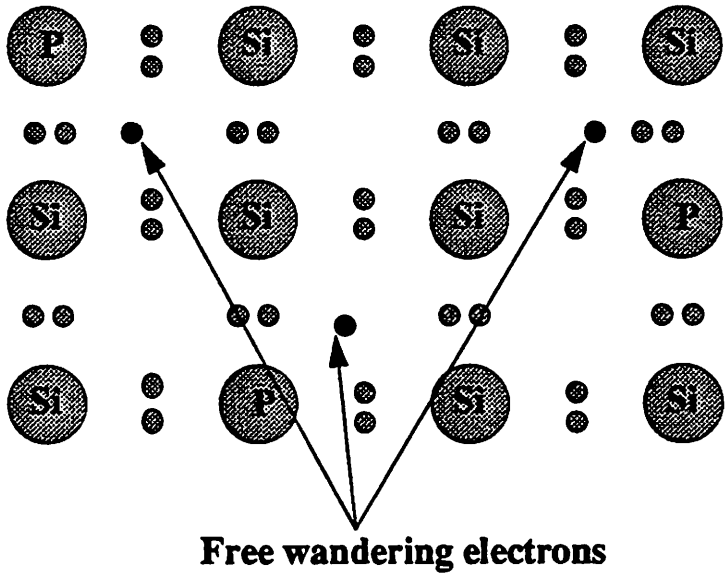
A semiconductor is a material that is neither a good conductor nor a good insulator. The semiconducting material most commonly used in IC manufacturing is silicon, although gallium arsenide is also used for some applications.

In conductors such as metal, electric current is carried by electrons free to wander about the atomic lattice of the material. In insulators, electrons normally stay tightly bound to their atoms and are not available to serve as charge carriers. In semiconductors, free carriers are not ordinarily present, but they can be generated with a modest amount of energy.

Semiconductor devices are made by introducing controlled amounts of impurity atoms into a

semiconducting crystal. This process is called doping. Silicon has 4 electrons in its valence, or outermost shell, and all of the electrons are committed to bonds between atoms. If silicon is doped with atoms such as phosphorus, which has 5 electrons in its valence, each phosphorus atom displaces a silicon atom. However, the extra electron the phosphorus atom brings with it has no place in the interatomic bonds and can be mobilized if a small voltage is applied to the crystal. Semiconductor regions with an excess of negative charge carriers are called "N-type" regions.

Figure 9. Phosphorus (P) -doped silicon (Si) lattice with excess electrons **PHOSDOPE**



If silicon is doped with boron atoms, which have only 3 electrons in their valence, electron deficiencies call "holes" are left in the crystal structure. Holes have positive electric charge and can move through the lattice much the same way that a bubble moves through a liquid medium. Semiconductor regions with an excess of positive charges are called "P-type" regions (Meindl, 1977, 1987).

The Virtues of Silicon **ELEM-5**

Several properties of silicon (Si) explain its dominance as a substrate base in the fabrication of integrated circuits. Material limits of silicon have resulted in the (less common) use of another semiconductor, gallium arsenide.

Silicon has a large bandgap, which is the difference in energy, or gap, between the valence and conduction electrons. As a result, silicon is relatively insensitive to temperature increases that can boost valence electrons into the conduction band and interfere with the precise control of the electrical properties required in a device. What's more, silicon is an abundant element that can be formed into almost perfect crystals at a relatively low cost, and silicon's native oxide, silicon dioxide (SiO2), is an excellent insulator with desirable attributes for IC's (Meindl 1977, 1987).

Gallium Arsenide ELEM-8

Gallium arsenide (GaAs) does not occur in nature. It was synthesized in the 1950's and is used as a semiconducting substrate in a few IC chips. Gallium arsenide's virtue is speed: conduction-band electrons in gallium arsenide drift faster than they do in silicon-- by some measures, about 2.5 times faster (Brodsky, 1990; Meindl, 1987).

Compared to silicon, however, gallium arsenide has some disadvantages. It is less abundant than silicon, and does not grow an excellent insulating native oxide as does silicon. And as transistors become smaller, gallium arsenide's speed advantage is offset by other material factors. A transistor can be made to switch faster by applying more power to it, but this additional power also increases heat buildup in the device. For very small devices, switching speed is limited by the capacity of the substrate to conduct heat away from the device. Since silicon has three times the thermal conductivity of gallium arsenide (that is, it can conduct heat away more quickly), small silicon devices may actually be able to switch just as fast as gallium arsenide ones, thus reducing the advantages of using gallium arsenide as a semiconducting substrate for integrated circuits.

Gallium arsenide devices are used for computing, television reception, satellite reception, and the optoelectronic transmission of data through optical-fiber networks (a technology known as photonics). Gallium arsenide light emitting diodes and lasers (used in visual-display systems and audio disk players) currently account for $1 billion in annual sales.(Brodsky, 1990).

Digital Logic Circuit Technologies ELEM-6

In microelectronics, the main cost of a component is measured by the area of silicon it occupies. It's difficult, however, to shrink passive components such as resistors, capacitors, and inductors and still maintain practical values of resistance, capacitance, and inductance. Although improvements in technology will lead to an increased selection of miniaturized passive components, simple -replacement- of passive components by active transistors (resistors, for example, can be replaced by direct substitution) has proven to be a far more effective strategy. Thus over the past two decades, research in microelectronic technology has focused on producing miniaturized high-quality transistors. This trend is reflected in the evolution of digital logic circuits toward a state where transistors are now used for almost all functions (Meindl, 1977).

The fundamental units of electronic logic are logic gates, and at the heart of every gate is at least one active circuit element. Discrete bipolar transistors and integrated circuits were first produced using bipolar technologies. MOS technologies, employing MOS transistors, were developed later than bipolar ones, and for the most part have been built only in microelectronic form. The evolution of bipolar and MOS technologies reflect advances in processing technology (Meindl, 1977; McCanny & White, 1987; see Figure 10.).

Bipolar Technologies ELEM-9

The first families of bipolar logic circuits were constructed from discrete components. In transistor-resistor logic (TRL), the number of resistors was maximized since they were the cheapest devices. In diode-transistor logic (DRL), performance was improved by substituting semiconductor diodes for many of the resistors (Meindl, 1977; McCanney & White, 1987).

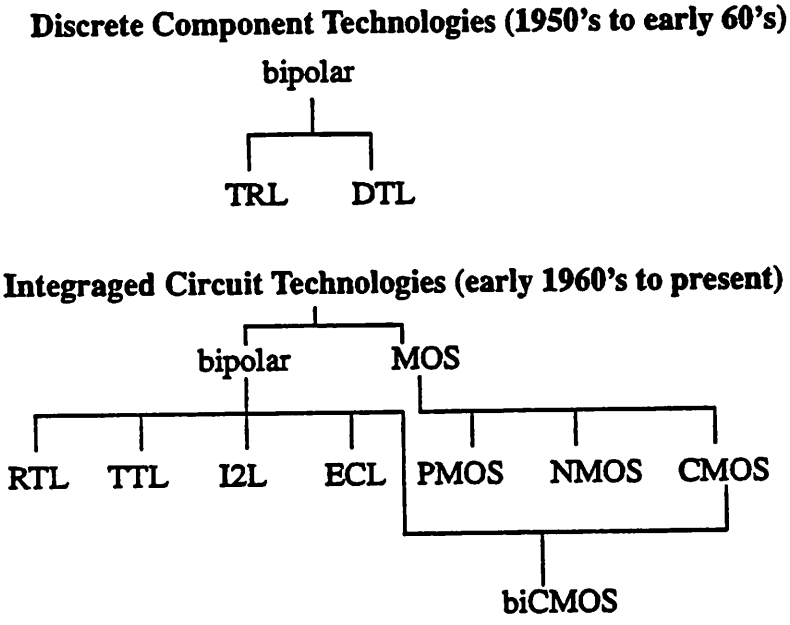
The first microelectronic technology, resistor-transistor logic (RTL), used mostly transistors and only a few resistors. Transistor-transistor logic (TTL), in which transistors are abundant and coupled directly together, remains the most popular bipolar technology today. Integrated-injection

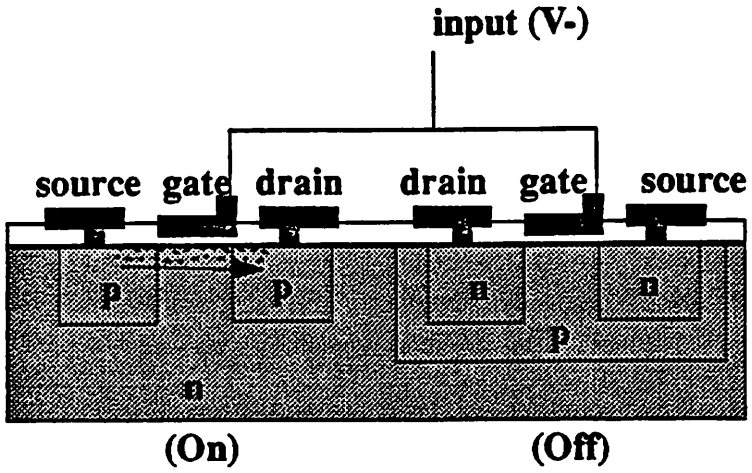
logic (I2L) technology reduces the packing densities of bipolar devices to a size approaching that of MOS devices by compressing a logic circuit made of two transistors into a single unit. Finally, emmitter-coupled logic (ECL) deviceswere developed for applications that demand extremely high speed. ECL devices consume much more power, and are used exclusively in Cray computers. (Meindl, 1977; McCanney & White, 1987; Oldham, 1991).

MOS Technologies — ELEM-10

MOS (metal oxide silicon) technologies offer a reduction in the large space and high power consumption requirements of bipolar devices. The first MOS electronic circuits employed p-channel (PMOS) devices because they were the easiest to make. As MOS technology advanced, n-channel (NMOS) devices replaced PMOS devices because they offered higher speed performance for the same density, complexity, and cost. The need for reduced power consumption led to the development of the larger but more power efficient complementary MOS (CMOS) devices (Meindl, 1977; McCanney & White, 1987; Oldham, 1991).

Figure 10. Important Technologies — ELEM-11





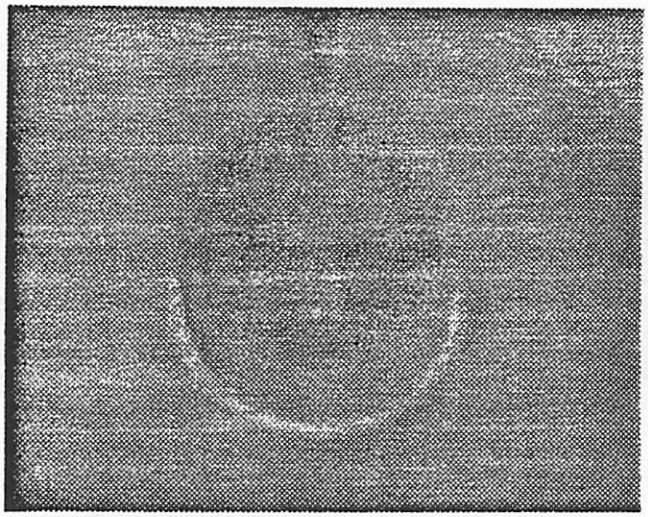
Dispite the density and power efficiency advantages of MOS technologies, high-speed bipolar technologies have continued to be developed. Recently emerging biCMOS technologies provide the best of both worlds by combining the speed advantages of modern bipolar technology with the space and power advantages of MOS technology (Oldham, 1991).

2. IC Manufacturing FAB-0

When a designer conceives of a new product, he or she specifies the functional characteristics of the device, selects many of the process steps required to manufacture it, and uses CAD tools to estimate the size and location for the hundreds and thousands of circuit elements. So that the goals of the circuit designer will be achieved, a high degree of control over the materials, process steps, and cleanliness of the production environment is essential during IC fabrication.

In IC manufacturing, 100's of copies of a microelectronic circuit are simultaneously fabricated on a thin semiconducting substrate, commonly made of silicon, called a wafer. Silicon wafers are typically produced by slicing 20-40 mil thick and 3-8 inch diameter slices from a purified silicon cylinder grown from a single-crystal seed placed within and slowly withdrawn from a vat of molten silicon.

Figure 12. Silicon cylinder growth CYLINDER



Mass production of IC's is completed in several stages, in which wafers, grouped together in lots of 20-100 wafers, are processed together and converted into the same final product. This process can be summarized in four process stages: wafer fabrication, wafer probe and sort, chip assembly, and final chip test and burn-in (e.g., Harrison, 1989; Chen, 1987; see Table 3).

Three important measures of manufacturing efficiency are yield, cycle time and fabrication cost. The costs of the last two stages, chip assembly and final testing, are often higher than wafer fabrication and testing because manufacturing costs are not shared among many die. (A die, or chip, is an individual microelectronic circuit.) Each die must be separately packaged and tested. (Oldham, 1977; Elliot, 1989; Harrison et al, 1989; Chen et al, 1987; see Table 3).

Table 3. Four Main IC Manufacturing Stages FAB-6

STAGE	LOCATION	CYCLE-TIME	YIELD
1.Wafer Fabrication	Fab plant	20-40 days	92% (good wafers)
2. Wafer Probe	Fab plant	3-5 days	25-75% (higher for mature products)
(probed wafers go on to die bank inventory)			
3. Chip Assembly	Assembly plant	3-10 days	92-98% (units out per unit started)
4. Chip test	Assembly plant	4-15 days	10-92% (low for new products)
(tested chips go on to final goods inventory)			
Overall		**30-70 days**	**30-40%**

Stage 1: Wafer Fabrication

*FAB-1

During wafer fabrication, various layers of substances are formed within the wafer, or deposite00d on the surface of it in accordance with the plan of the circuit designer. These layers are typically formed in the following way:

A thin film of oxide is formed or (less commonly) deposited on the surface of the wafer in a process called oxidation.Then, a photoengraving process called photolithography (also known as "masking" or "imaging") is used to transfer a desired pattern onto the surface of a silicon wafer. Portions of the oxide surface under the pattern are then dissolved away in a process called etching.- Finally, in a process called doping, impurities are introduced into the exposed surface to form device elements such as the source and drain of a transistor. Thin films may also be deposited on the wafer to form elements such as the polysilicon gate of a transistor.

These procedures are repeated many times until a complete circuit is is constructed. To fabricate circuits, several users of the Berkeley Microfabrication Lab formally specify these steps using the Berkeley Process Flow Language (BPFL) (see Berkeley Microfabrication Lab below).

Oxidation

FAB-7

When silicon is exposed to oxygen or water vapor at elevated temperatures (between approximately 900 and 1000 degrees celcius), the silicon reacts with the oxygen to form a continuous layer of silicon dioxide. In this process (called thermal or wet oxidation) part of the silicon substrate is consumed to form a little under 50% of the final oxide thickness.

This oxide layer can be used as a mask during dopant diffusion, as a junction passivator, as an insulating field oxide, or as a gate dielectric in MOS transistors (Maly, 1987).

Figure 13. Wafers exiting oxide furnace FURNACE

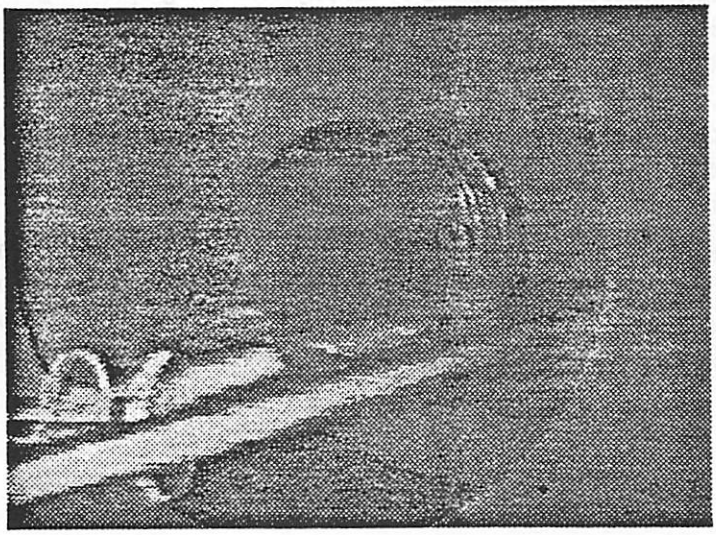


Table 4. An example Process Flow Segment **FAB-14**

START (100) p-type 10 ohm cm wafers ; start 100 wafers
CLEAN in H2(S0)4-H202 piranha etch, 2 min ; clean, rinse, dry
RINSE 1, 4 min
RINSE 2, 4 min
DRY
OXIDIZE 1 hr at 1000 C in Wet Oxygen ; oxidize
place wafers in quartz oxidation boat
insert into furnace ante-chamber
push at 1/2" per sec at 800 C in Oxygen
ramp to 1000 C (10 C/min), 20 min
turn on steam, 60 min
ramp down to 800 C in Oxygen
pull at 1/2" per sec
unload into plastic carriers

Table 5. BPFL code, Student CMOS **FAB-5**

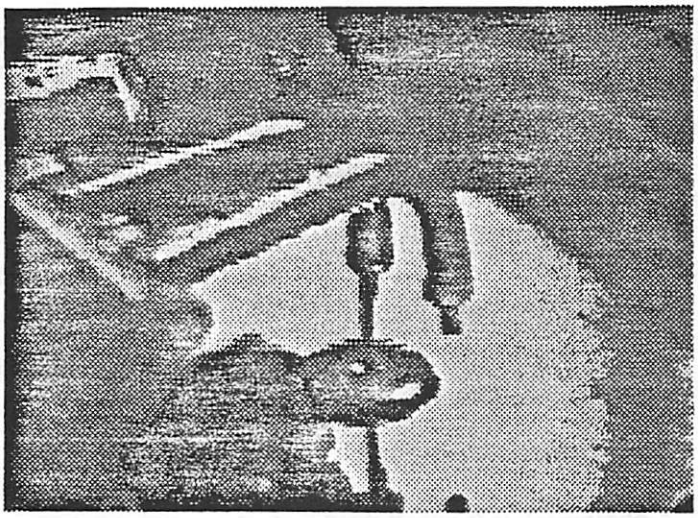
```
step START-OXIDE begin /* oxidize wafer surface */
 std-dry-oxidation(thickness: {58 nm}, temperature: {900 degC});
end;
```

Photolithography *FAB-8

The photolithographic process was inspired by the physical lithographic engraving process--or contact printing--used in printing businesses to transfer desired patterns onto surfaces. In IC manufacturing, optical photolithography, or (less commonly) electron-beam or X-ray lithography, are used to define patterns, layer by layer, on a wafer. Once a layer is defined, it can be etched into the underlying (usually oxide) surface to create elements of devices. Using optical techniques, 0.75 micrometer chip geometries are common (compared to 7 micrometer geometries in 1970), allowing thousands of gates to fit onto a single chip (e.g. Oldham, 1977, 1991; Maly, 1987

First, the entire (usually oxide-covered) surface of a wafer is covered with a thin film of photoresist, a light-sensitive polymer that changes its solubility in a developing solution when exposed to UV light. The film is spread by placing a drop of the resist on the wafer and rapidly spinning it. The wafer is then baked to dry the film and cause it to adhere more strongly to the wafer.

Figure 14. Covering a wafer with resist **SPIN-ON**



The resist-covered surface of the wafer is exposed to UV light through a photomask, in which clear and opaque areas represent the pattern to be transferred. The mask prevents the UV light from passing through the opaque regions while allowing radiation to pass through the clear regions, which changes the solubility of the underlying photoresist. The resist is then developed by washing the wafer in a solvent that removes the film wherever the mask was clear (if a "positive" photoresist is used) or opaque (if a "negative photoresist is used). Positive photoresists generally require longer exposure than negative photoresists, but they provide better photolithographic resolution. After developing, the wafer is baked to harden the remaining photoresist.

Table 6. BPFL code, Student CMOS example **FAB-5**

```
step NWELL-LITHO begin /* spin on, expose, develop resist */
 pattern(mask: 'nwell, resist-thickness: {1 um});
/* NWELL pattern */
end;
```

Electron beam and X-ray lithography *FAB-9

In X-ray lithography, X-rays instead of UV (optical) rays are used to expose the photoresist. X-ray radiation has a shorter wavelength than UV radiation, and was developed as a technique to allow for additional reduction of the minimum dimensions of circuit elements. Thus far, however, the less expensive optical lithography techniques have been perfected so that circuit elements with minimum dimensions approaching the size of those created using X-ray techniques (presently near .5 micrometer) can be produced. Thus, the overwhelming advantages of X-ray lithography have not yet been realized (Oldham, 1991).

X-ray and optical lithography are both parallel processes in which the surface (or each die) of

a photo-sensitive resist-coated wafer is exposed to radiation through a photomask. If a circuit pattern can be written directly onto a photomask, why not skip the mask step and write the circuit pattern directly on the wafer?

In electron-beam (E-beam) lithography, this is exactly what is done. Using ebeams, the circuit pattern is written directly onto an electron-sensitive resist by serially scanning an E-beam across the wafer in the desired pattern. Very high pattern resolution can be achieved using E-beams. This technique is not commonly used, however, since E-beam equipment is much more complex and expensive, available electron-sensitive resists have poor sensitivity, and (serial) E-beam exposure takes much longer than (parallel) optical and X-ray exposures. For example, parallel optical exposure of a 6 inch wafer (with .75 micrometer resolution) typically takes 60 seconds, while E-beam exposure time can take up to an order of magnitude longer at 600 seconds (Elliott, 1986, 1989).

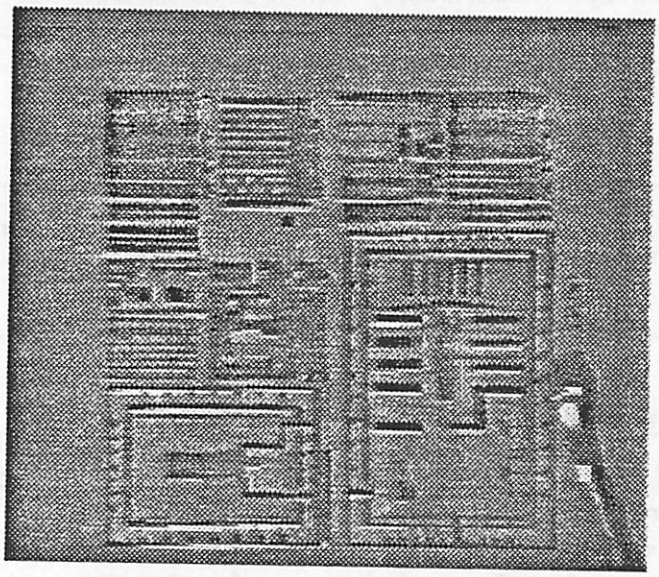
E-beam lithography is very expensive. Since economics drive technology in the IC industry, e-beam lithography is thus rarely used. (E-beams are often used to create photomasks, however, of which only a few, necessarily highly accurate, master copies are needed).

Photomasks

***FAB-10**

(Oldham, 1977, 1991). A photomask is (typically) a 5 inch glass plate that has a pattern of clear and opaque areas, repeated over its surface, that defines a single layer of a ciruit. Between 15 and 20 masks are commonly used today to describe an entire circuit.

Figure 15. A photomask **PHOTOMASK**



Photomasks are typically generated from circuit designs laid out with the aid of CAD tools. The transfer of the circuit design to the photomask is typically done by scanning a computer-controlled optical or electron beam across a photographic plate in the given (generally ten-fold enlarged) pattern for a layer of the circuit. This pattern, called a reticle, is then checked for correctness, and a

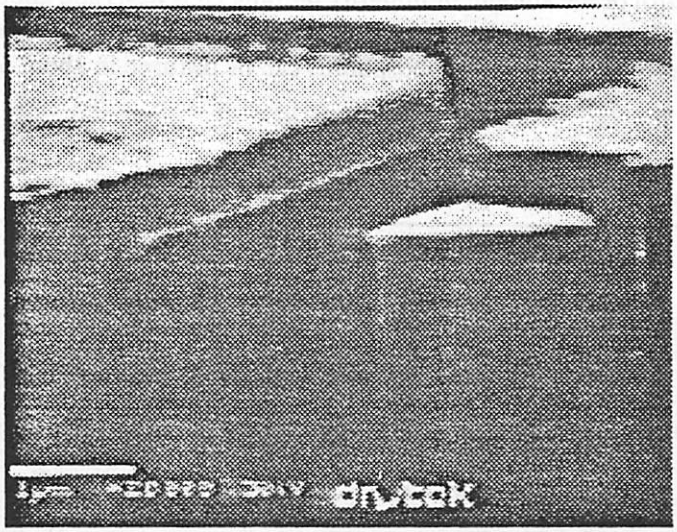
reduced version of it is reproduced and (repeatedly) projected side by side on a final mask. A series of reproduced masks, called submasters, are then created and sent to a wafer fabrication laboratory where they are often used to produce thousands of wafers per week.

Etching

FAB-11

After the photolithographic step, the material areas of the wafer unprotected by the hardened photoresist are removed in a process called etching. Etching techniques are characterized by their selectivity (what materials the etching agent attacks; for instance, an etching agent should dissolve silicon oxide but not silicon or photoresist) and degree of anisotropy (the tendency to etch in one direction only, in contrast to undesired "isotropic" etching simultaneously in all directions). Etching can be either physical or chemical, or a combination of both (Oldham, 1977, 1991; Maly, 1987).

Figure 16. Etched surface (from scanning electron microscope) **SEM**



Physical etching involves bombarding a wafer with high-energy ions that chip off materials, which is highly anisotropic but unselective.

Chemical etching is done in either a liquid (wet) or gas (dry, or plasma) environment in which chemicals are used to dissolve selected material. In wet chemical etching, the wafer is placed in a highly selective but isotropic liquid chemical that dissolves an exposed surface material such as oxide. However, such isotropic etches result in a pattern that significantly departs from the desired pattern. In dry etching, the wafer is bombarded with a highly selective gaseous chemical that dissolves certain (exposed) surface materials. Dry chemical etching combines the advantages of physical and wet chemical etching in that it is both highly anisotropic and highly selective.

Table 7. BPFL code. Student CMOS example **FAB-5**

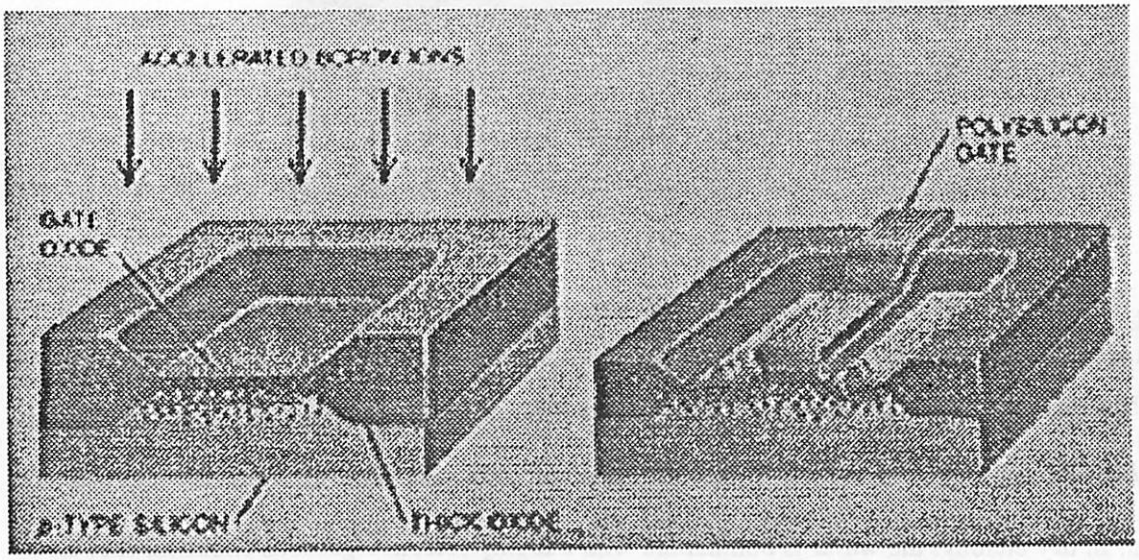
```
step NWELL-ETCH begin /* etch the exposed nitride */
 etch-nitride(overetch: {20 %}, undercut: {50 %});
end;
```

Methods of Doping **FAB-12**

To create active circuit elements such as transistors, impurities (e.g., used to create n-type and p-type transistor regions) must be selectively introduced. Two commonly used doping techniques are diffusion and (more commonly) ion implantation (Picraux & Peercy, 1985; Oldham, 1977).

In diffusion, the wafer surface is exposed to an impurity (such as boron or phosphorus) in a high ambient temperature (such as 1000 degrees) and the impurity enters the silicon wherever the photolithographic process has left it unprotected. Under this heat, the impurities diffuse slowly into the bulk of the wafer. The depth to which the impurities diffuse is determined by temperature, and the amount of time the wafer is kept at the temperature. Two heat treatments, one at a "deposit" temperature (at which the control of the amount of impurity introduced is best) and another at a (usually higher) "diffusion drive-in" temperature (at which most the impurity is diffused) are generally used. For example, a one micrometer deep layer of phosphorus can be diffused in about one hour at 1100 degrees fahrenheit.

Figure 17. Ion implanation **DOPE**



In ion implantation, impurities are introduced into unprotected ares of the wafer at room temperature by accelerating dopant ions (atoms stripped of one or more of their electrons) to a high energy so they are driven into the wafer and become embedded. The depth at which the dopant ions become embedded depends on their mass and (accelerated) energy. As the dopant ions plow into

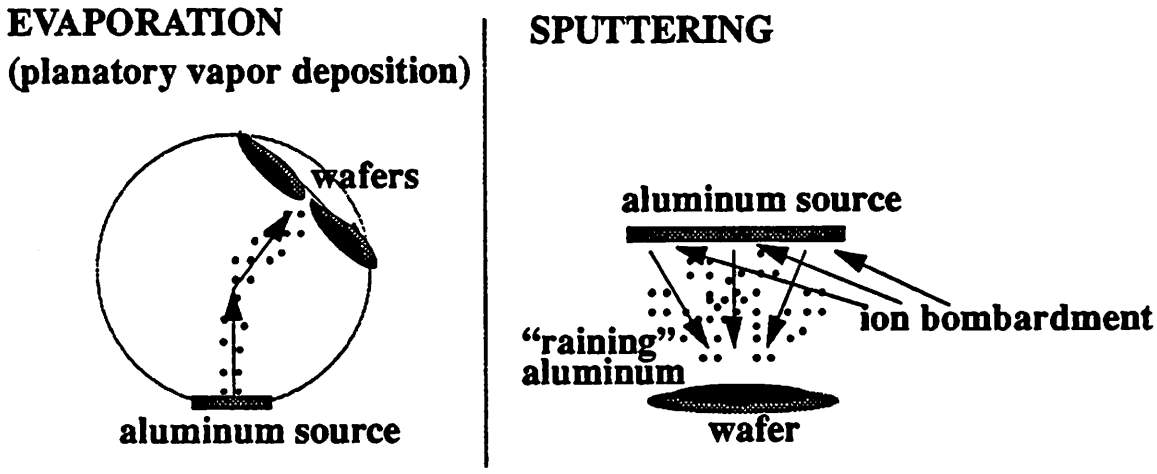
the silicon they can damage the crystal. However, some of this damage can be healed in a moderate-heat treatment process called annealing. Ion implantation allows more accurate control of dopant level, can be used to introduce impurites through an oxide layer if desired, and can be used to introduce impurities that are difficult to deposit from a high temperature vapor.

Deposition of Thin Films

FAB-13

(Oldham 1977, 1991; Maly 1987). The uppermost layers of IC's consist of deposited thin films, such as aluminum to form metal contacts between device elements. Two common methods of deposition are evaporation (otherwise known as physical vapor deposition, or PVD) and chemical vapor deposition (CVD). PVD is often used to deposit metals such as aluminum, and CVD is often used to grow oxides and polycrystalline silicon (which is then doped to act as a metal).

Figure 18. Deposition of metal **DEP**



Evaporation, the simplest method, is done by heating the material to be evaporated (usually aluminum) in a vacuum by bombarding it with high-energy electrons, and placing the wafers to be coated above the material. The wafers are usually rotated as the aluminum evaporates to ensure uniform coverage. The rising (evaporating) pure aluminum typically is deposited on the wafer to a thickness of a half to one micrometer.

In a method similar to evaporation, called sputtering, the wafers are place below the material to be deposited. The material is then bombarded with ions that scatter the atoms, which fall in a "rain" onto the wafers. Sputtering of alloys is easier than evaporation because of the different evaporation rates of different elements. Silicon-aluminum alloys are often used as a metal source because they prevent the silicon in the wafer from reacting with the deposited aluminum (which can cause spiking, or short circuits).

In chemical vapor deposition, the deposited material is a product of a chemical reaction (in a

vapor) on the surface of the wafer substrate. For example, polycrystalline silicon can be grown on the surface of a wafer by decomposing silane gas (SiH4) in the presence of the wafer.

Table 8. BPFL code, Student CMOS example **FAB-5**

```
step DEPOSIT-PSG begin /* deposit polysilicon glass */
 std-psg-deposition(thickness: {0.75 um});
end;
```

Stage 2: Wafer Probe and Sorting FAB-2

In the second stage of wafer manufacturing, each die on a fabricated wafer is tested for functionality. The dice that fail are marked with an ink spot. The wafer is then sectioned into individual die by scribing lines between the dice and breaking the wafer along these lines. The defective dice are discarded, and the remaining dice are usually sent from the fabrication facility to a die bank inventory. Die lots will be withdrawn from the inventory and assembled when they are scheduled for release.The wafer probe and sorting stage generally takes from a couple of hours up to 2 weeks to complete.

Figure 19. Testing a circuit **TEST**

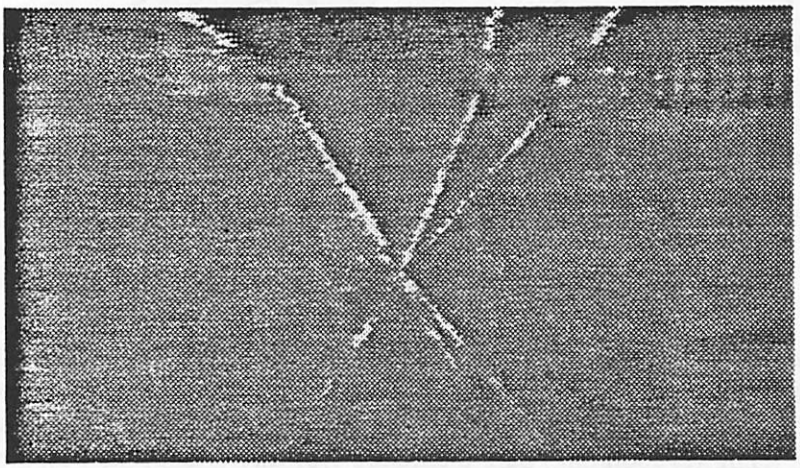
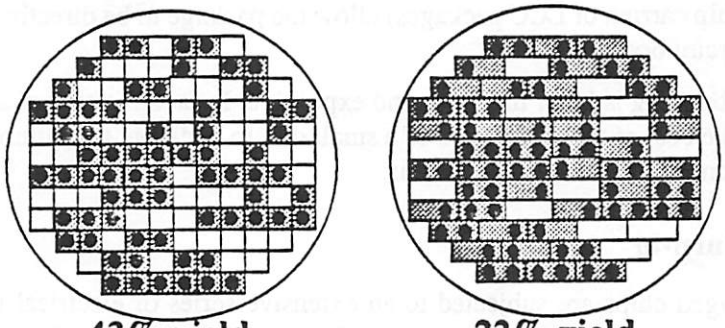


Figure 20. Effect of doubling die size on yield (dots indicate a defect) **YIELD**



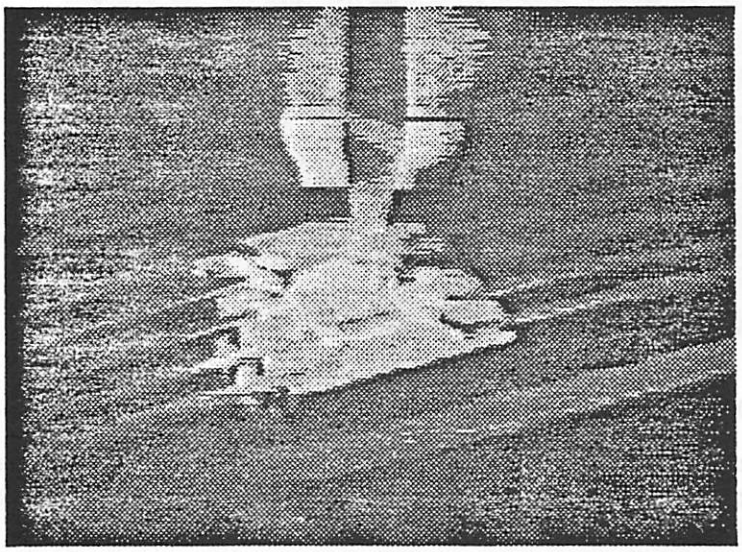
Stage 3: Chip Assembly

FAB-3

In the third stage of wafer manufacturing, die that have been fabricated and tested are assembled for product release. An inventory, called a die bank, of tested die is usually maintained at the assembly plant to smooth out variations in productivity at the wafer fabrication stage. The assembly stage typically takes a few days to several weeks to complete.

Individual integrated circuit die can be mounted in a wide variety of packages. A chip generally assembled by placing it on a (commonly lead) frame, attaching electrical leads to it at contact points (for connections to the outside world), and sealing the assembly in a (commonly plastic or ceramic) protective housing.

Figure 21. Chip assembly **ASSEMBLY**



Two common packages made for mounting into holes in printed-circuit boards are the dual-in-line (DIP) and pin-grid array (PGA) packages. The popular and cheap DIP package, commonly made of plastic, epoxy, or ceramic, accomodates between 4 and 80 leads. The (more expensive) PGA package, on the other hand, can have hundreds of pins. Recently developed "surface mount" packages (such as leadless chip carrier, or LCC packages) allow the package to be directly soldered to the surface of a printed-circuit board.

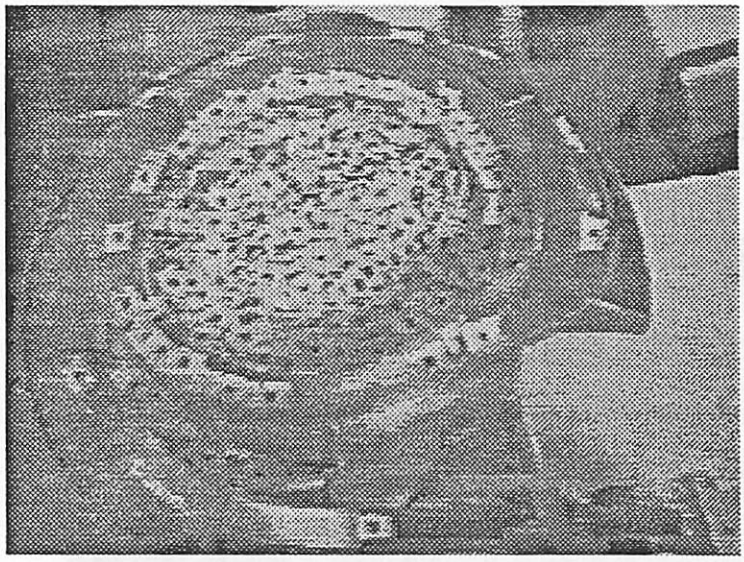
Die-mounting and wire-bonding is labor intensive and expensive. In fact, the cost of assembly and test can be many times the cost of the fabrication of a small die. In addition, the failure of wire bonds is one of the most common IC reliability problems.

Stage 4: Chip Test and Burn-in FAB-4

In this final stage, packaged chips are subjected to an extensive series of electrical tests and burn-in operations to ensure that the circuit functions correctly and will continue to do so reliably. (For example, they may be operated for several hours in a high- temperature environment).

Final testing and burn-in usually take 1 to 7 days (although burn-in can take up to 5-6 weeks) and are usually done at the assembly plant where chips are packaged (stage 3). After final test, chips are sorted into different bins based on attributes like device speed and power consumption (Harrison et al, 1989; Oldham, 1991).

Figure 22. Chip sort **DIESORT**



Software Systems for IC Manufacturing CIM-0

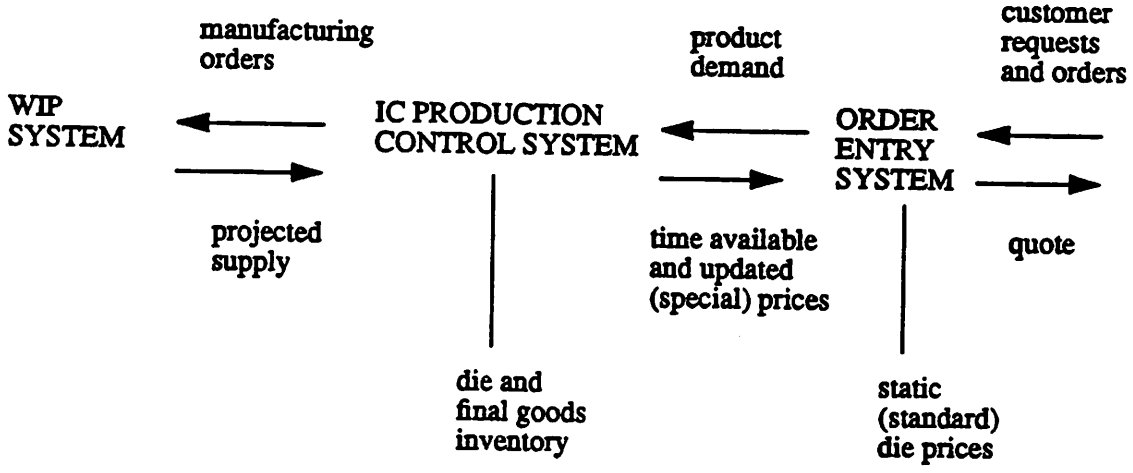
The IC manufacturing process is a complex process in which design and fabrication are currently done independently. The fabrication process alone involves hundreds of steps, resulting in turnaround times of several months. As device and process complexity increase and product lifetimes shrink, the manual steps involved become so cumbersome and labor intensive that more effec-

tive, automatic methods to collect and monitor processing data are essential.

Computer-integrated manufacturing (CIM) systems integrate many software packages, such as: computer-aided design (CAD) and computer-aided manufacturing tools (e.g., work-in-progress, or WIP, systems); process simulators, facility management systems like those used to help operate the Berkeley Microfabrication Laboratory, and production control and order entry systems. CIM emphasizes the integration of these systems, aided by a shared integrated database and a formally specified process flow representation, as the key to dramatic productivity improvements. Such improvements will allow IC manufacturers to respond quickly in todays increasingly competative environment of more complex and customized IC's with shorter life cycles (e.g., Hegarty 1991; Bray 1988; Harrison et al 1989; see Figure 23).

The objective of CIM is to automate the complex manufacturing process to improve flexibility and portability, and product quality and consistency; to permit application-specific chip development; and to minimize turnaround time, scrap and rework, development and manufacturing costs, confusion, and human error (Penfield, 1989).

Figure 23. Integrated Software Systems for IC Manufacturing **CIM-5**



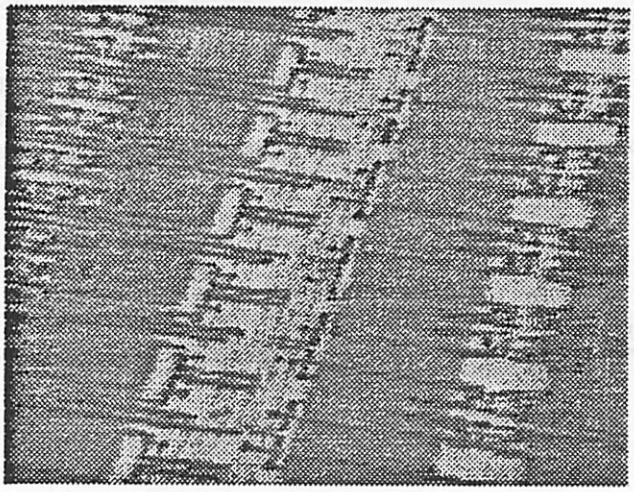
Computer-aided Design **CIM-1**

Prior to the advent of sophisticated computer-aided circuit design (CAD) systems in 1978, IC device design was often done by device experts by drawing circuit layouts completely by hand. CAD systems allow designers to simulate the operation of a circuit, and to determine the most space-conserving layout of each layer of the integrated circuit.

Simulation is less expensive and more accurate than assembling and testing breadboard circuits

made of discrete circuit elements. Simulation also allows the designer to modify a circuit by a few keystrokes and immediately observe the resulting behavior of the circuit. Circuit layout is also computer-aided, with the help of formally specified design rules which specify the physical contraints on circuit geometries imposed by physics and patterning processes (Oldham, 1977; Elliot, 1989).

Figure 24. CAD circuit layout **CAD**



Design abstractions allowed free-form layout to give way to automatic design and circuit testing, and as a result, IC process design was revolutionized. New architectures (e.g., RISC) were developed, rapid prototyping ensued, and design became accessible to a broader range of people--chemists, physicists, computer scientists--not just device experts. As function and layout abstractions revolutionized the design process in 1978, abstraction of the manufacturing process with a process flow language and computer-integrated manufacturing can revolutionize the fabrication process, allowing new structures and designs, rapid prototyping of structures, and process design by circuit engineers--not just fabrication experts--to facilitate the development of more application-specific chips (Penfield, 1989).

Shop Floor Control with Work-in-Progress (WIP) CIM-2

A process-flow is a specification of the steps needed to manufacture a product. Traditional shop floor control is usually specified in a structured document system in which a printed copy of the process-flow specification, called a traveller, accompanies a wafer lot as it moves between different fabrication equipment. Equipment operators follow the instructions on the traveller to process the wafer lot. Although computer systems are often used to store the traveller specifications they cannot interpret them, nor can they automatically collect process data during a run (e.g., Hegarty, 1991).

Run-sheet systems employ -interactive- travellers to track work- in-progress (WIP) and automate some of the equipment operations. However, they are usually limited to a small, fixed set of sequentially executed commands. WIP systems control and record the movement of wafer lots through a fabrication facility, issue instructions to people and equipment to execute steps to process

the lots, allocate resources (i.e., equipment), and maintain a log of the processing history of wafer products. Examples of commercial run-sheet systems are PROMIS, WIPSYS, and WORK-STREAM (Harrison et al 1989).

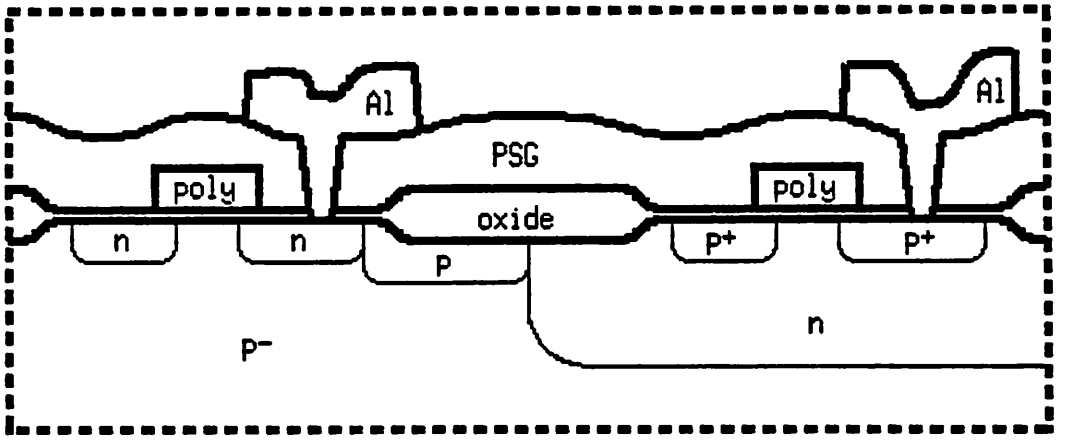
In addition to keeping track of currently active wafer lots, some WIP systems also contain up-to-date information on production lots in different stages of the manufacturing process--fabricated wafer lots stored in the die bank (prior to final assembly), lots in the assembly plant, lots firmly scheduled for future release, and tested chips in the finished goods inventory.

Input commands to WIP systems can be entered directly by fabrication engineers, received from a WIP interpreter that executes a process flow program, or from production control systems requesting projected die supplies for customer orders (Rowe et al 1990; Harrison et al 1989).

Process Simulation Systems CIM-3

(Rowe et al 1990). Process simulators are used to produce wafer profiles at different stages of the fabrication process. Producing and testing simulated profiles is less expensive than fabricating and testing the wafers themselves. Simulation allows a process engineer to easily modify the fabrication process and observe the resulting two-dimensional cross-section (or less commonly) three-dimensional sideview of the wafer, called a wafer profile, at various steps of the process.

Figure 25. A sample wafer profile **SAMPLE**



The input commands to process simulators can be entered directly by fabrication engineers or received from a simulation interpreter that executes a process flow program. Examples of process simulators are PROSE, SIMPL, and SUPREME. Factory simulators (such as BLOCS, CHIPS, and MODES) and simulators that check generated wafer profiles and process correctness (such as the Funokoshi system) can also be given commands directly or through input-generator interpreters executing process flow programs.

Order Entry and Production Control Software Systems CIM-4

Order entry systems (such as SWISS; see Harrison et al, 1989) operate on a database of booked (but not yet delivered) customer orders and quote guides to track the status of customer orders. Based on this information, order entry systems request price quotes and delivery schedules from production control systems.

Production control systems further automate the mechanics of doing business by generating delivery quotations based on product availability information from inventory and WIP systems, and by generating time-phased production requests for WIP systems once a quotation is accepted and a customer order is booked.

Shared Integrated Databases CIM-6

A key component of a CIM system is a shared database that stores all of the information about the design and manufacture of semiconductors. Such a database may contain information about the facility areas and equipment, process-flow specifications, work-in- progress (WIP), equipment status, and product inventory and orders. This information can be used by multiple CIM software applications for tasks such as equipment control, circuit design, process simulation, process specification, fault diagnosis, and operations monitoring (e.g., Hegarty, 1991).

For example, BPFL, a process-flow specification language, uses two main kinds of database entities. The first kind includes entities required to implement a BPFL program (such as process flows, wafer snapshots and lots), and the second includes entities a BPFL program might access (such as equipment and mask descriptions).

The Berkeley Microfabrication Laboratory *MICROLAB-0

The Berkeley Microfabrication Lab in Cory Hall is a complete facility to fabricate semiconductor devices and circuits.

Microelectronics research began at the Berkeley lab, the first university IC lab in the world, in 1960. The first working silicon-based circuits were produced in 1962. Expansion and renovation of the now 10,000 square feet lab was completed in 1983. The lab currently supports 160 Berkeley students, faculty, and staff from EECS (about 75% of the users) and physics, material science, chemistry, and chemical engineering (about 25% of the users). A broad range of undergraduate courses at Berkeley--in device physics, fabrication technology, circuit and systems design, and computer aided design--provides the fundamental basis for advanced research. Students are expected to carry out all fabrication steps from design to testing experimental devices, with the exception of a few highly specialized steps such as ion implantation (e.g., Dunster, 1987).

The Microlab contains over 60 different kinds of equipment, and is a test site for Berkeley's Computer Integrated Manufacturing (CIM) projects. The following software systems and languages are available to aid in the fabrication process:

1. The WAND, to reserve and control equipment, and report problems.
2. Circuit design software (e.g. KIC, MAGIC).
3. Process simulation software (e.g., SAMPLE, SUPREM, SPICE, BIPS).
4. Berkeley Process Flow Language (BPFL), used to specify the steps needed to manufacture a project. BPFL programs are evaluated by simulation and fabrication

interpreters.

5. Faults to record and diagnose equipment problems.
6. BLIMP and CIM Browser to monitor the operation of the microlab.

The WAND MICROLAB-1

The WAND is a menu-driven interface to the Berkeley Laboratory Information System (BLIS) for managing the operation of the Berkeley Microlab. Users can enable and disable lab equipment through the system, which checks user's authorization level on each piece of equipment. Using the system, users can post equipment problems and comments, which go directly to the facility technicians and management so they can be addressed quickly. Users can also inquire about and reserve pieces of equipment through the the online equipment status board (Dunster, 1987).

Berkeley Process-Flow Language (BPFL) MICROLAB-2

A process flow is a specification of the steps needed to fabricate a product. The BPFL language was developed for specifying process flows. BPFL specifys all aspects of a process, including instructions to make IC's, the structures created during fabrication, or the movement of material through a semiconducture manufacturing facility. A formal process-flow representation, provided by BPFL, is an important part of an IC computer-integrated manufacturing (CIM) system (Hegarty, 1991; Rowe et al, 1990).

A BPFL program is composed of procedural and object-oriented abstractions, data and control structures, and exception handlers. BPFL programs are evaluated by interpreters that perform tasks like work-in-progress (WIP) tracking and process simulation.

Processes for fabricating bipolar and MOS transistors can be specified in BPFL. For example, BPFL specifications are available for Student CMOS, a simple CMOS process used in EECS 143, "Processing and Design of Integrated Circuits", and CMOS-16, the baseline CMOS process used in the Berkeley Microlab.

Following is the BPFL code for the student CMOS fabrication process used in EECS 143, which contains approximately 41 steps. (Many steps are omitted.) Beside several steps are hyperlinks to figure nodes that show the wafer profile image that results after the step is completed.

Figure 26. Student CMOS VLSI layout **MASK-0**

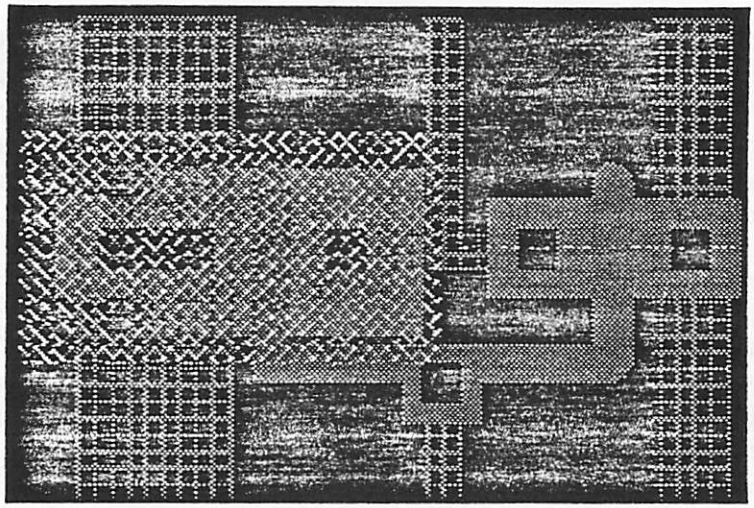
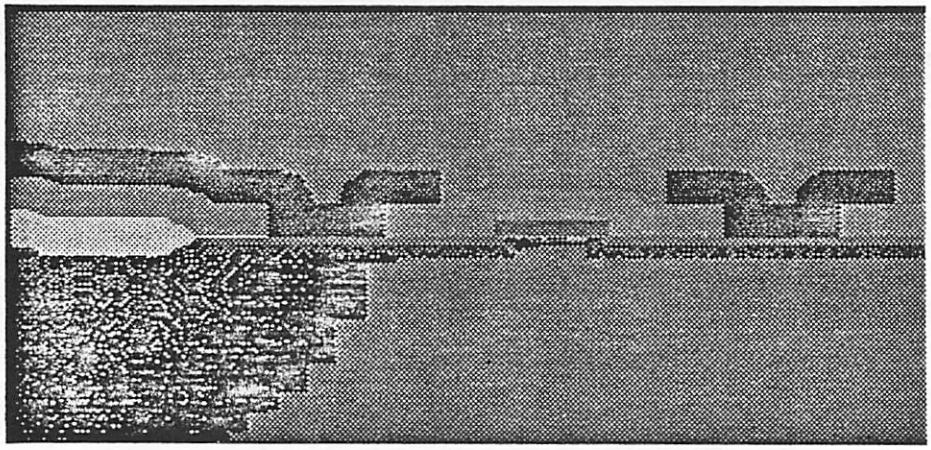


Figure 27. Student CMOS Wafer profile at the end of fabrication **DEVL-42**



```
defflow Student-CMOS (mask-set, lot-size)
begin
/* allocate wafer */
wafer-spec := bare-silion-wafer(crystal-face: 100,
       resistivity: [(18 ohm-cm) (22 ohm-cm)],
       quality: 'product, dope: 'p);
allocate-lot(size: 1, snapshot: wafer-spec, lot-name: 'test);
/* figure-> substrate-0 */

step START-OXIDE begin /* oxidize wafer surface */
       std-dry-oxidation(thickness: (58 nm), temperature: (900 degC));
end;
step INSULATOR begin /* deposit silicon nitride insulator */
       std-nitride-deposition(thickness: (80 nm));
end;
step NWELL-LITHO begin /* spin on, expose, develop resist */
       pattern(mask: 'nwell, resist-thickness: (1 um)); /* NWELL pattern */
end;
step NWELL-ETCH begin /* etch the exposed nitride */
       etch-nitride(overetch: (20 %), undercut: (50 %));
end;
 . . .
step POLY begin /* put down poly layer */
       pattern(mask: 'poly);
       etch-poly();
       strip-resist();
end; /* figure-> devl-26 */
 . . .
step RESIST-PSD begin /* strip resist left after doping polysilicon */
       strip-resist();
end;
step DEPOSIT-PSG begin /* deposit polysilicon glass */
       std-psg-deposition(thickness: (0.75 um));
end; /* figure-> depo-37 */
step CONTACT begin /* put down contacts */
       pattern(mask: 'cont, invert: true); /* figure-> expo-38 */
       etch-psg();
       strip-resist();
end; /* figure-> devl-38 */
step ETCH-OXIDE begin /* remove oxide */
       etch-oxide(thickness: (0.7 um), undercut (0 %));
end; /* figure-> etch-39 */

step DEPOSIT-PSG begin /* deposit aluminum */
       std-al-deposition(thickness: (0.8 um));
end; /* figure-> depo-40 */
step CONTACT begin /* deposit metal layer */
       pattern(mask: 'mtl); /* figure-> expo-41 */
       etch-al();
       strip-resist();
end; /* figure-> devl-42 */
end;
```

Faults MICROLAB-3

Faults combines a forms-based user interface with a facility-wide relational database to record equipment maintenance and repair events as they occur. The semantics of preventive maintenance (PM) and repair events are formalized to create clear and unambiguous maintenance reports. Storing PM and equipment failure information in an organized database has several benefits. Accumulated information is automatically indexed to aid diagnosis of failures as they occur. Equipment failure information is available to utility programs for display and statistical analysis, to produce summaries such as preventive maintenance intervals, mean time between failures, predicted downtimes, performance trends, et (Mudie, 1990).

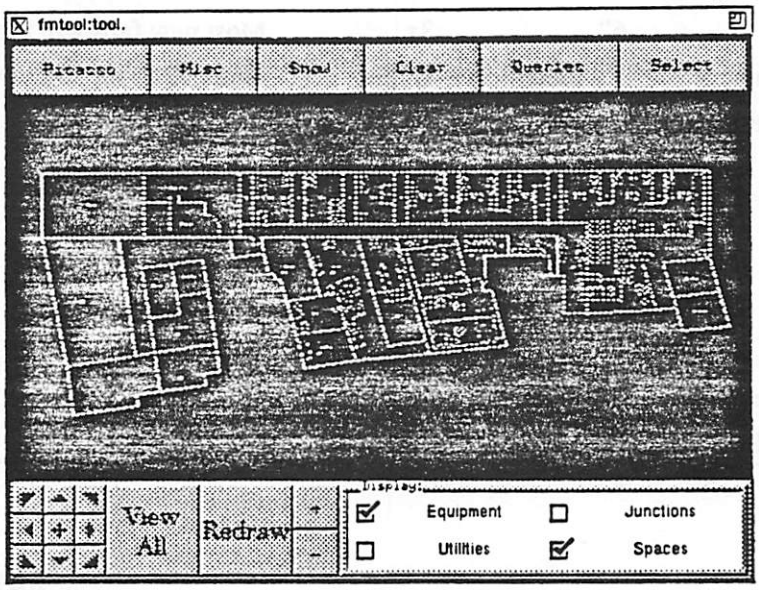
Faults iscomonly used at the Berkeley Microfabrication Facility. Lab technicians have entered knowledge of over a hundred different pieces of equipment into the database. The Faults system has provided a significant improvement in the management of preventive maintenance and equipment repair information.

Operation of the Microlab MICROLAB-4

A key component of any CIM system is a shared integrated database that stores all of the information about the design and manufacture of a product (such as semiconductors). Berkeley Microlab users have access to an online database that contains information about the Microlab facility, including equipment, utilities and work-in-progress (WIP). The BLIMP and CIM Browser systems operate on this database.

The Berkeley Laboratory Infrastructure Monitoring Program (BLIMP III) provides for real-time sensor monitoring within the Microfabrication Lab. At present, there are nineteen sensors located throughout the Microlab. These sensors monitor things such as storage tank levels; air, liquid nitrogen, and oil pressures; and air temperatures. The BLIMP software interacts with the data acquisition device, processes and displays sensor readings, saves the history of readings within a database for future examination, and performs the appropriate actions (i.e., sending out alarm notices) for the necessary conditions (i.e., temperature too high, storage tank level too low). In addition, BLIMP can also provide sensor data to external applications, including the the CIM Browser.

CIM Browser (Smith and Rowe, 1990) is an graphical interface that allows end-users to specify queries to the database.



3. The Worldwide IC Markets MARKETS-0

The evolution of IC technology illustrates the constant interaction between technology and economics, resulting in more reproducible, more reliable, and less expensive devices (Noyce, 1977). Advances in IC technology are driven mainly by economic desires for high yield and cycle time, mass fabrication at low cost, and shares in high-volume electronics markets. Competition in international markets is high (Noyce, 1977; Longfellow et. al., 1991).

In the past 30 years, chip packages have remained fairly constant in size and price (about $5 per chip), but the number of transistors per chip have increased by six orders of magnitude, doubling every year or two, to the point where today a typical chip contains 10^6 transistors. (In 1960, a "chip" was a 1/2 inch wafer containing one transistor; see Economics chart below).

The most striking characteristic that separates the IC industry from other industries is in its annual doubling of output. This rapid growth has resulted in a greater rate of price reduction (where price in the IC industry is measured per bit) than in other industries (Noyce, 1977).

Table 10. Economics Chart **MARKETS-1**

	1970	1990	CHANGE	COMMENTS
Wafer size	2"	6"	3x	Most new fabs will use 8" wafers
Feature size	7 u meters	1 u meter	1/7x	Reduces about 50% every 6 yrs.
DRAM	1 Kbit	1 Mbit	1000x	Dynamic Random Access Memory
Chip area	.1 sq. cm	1 sq. cm.	10x	Constrained by yield.
Wafer cost	$50	$500	10x	At end of fabrication
No. masks	4-7	15-25	5x	
Yield*	20%	80%	4x	
Chip cost	$2	$4	2x	
Cost/bit	0.2 cents	0.0004 cents	1/500x	Going down fast
Equip cost/wk	$160K	$160M	100x	For 1000 wafers

*reaching ceiling

Yield MARKETS-2

Yield is the percentage of good circuits (that is, individual die) that survive the manufacturing process to emerge as packaged chips.

Twenty years ago, IC chip yields were at 20%, which left enormous leverage for profit potential. In the 1980's, a large percentage of the chip market share was taken over by Japanese IC manufacturers, who concentrated on yield. As fabrication technology matured, yields increased to the point where commercial yields for simple circuits are presently at a stable 75-80% at competative IC manufacturing firms.

Yield typically decreases with increasing circuit size and integration because bigger circuits have a higher probability of having a defect (i.e., more can go wrong with them) and because fewer (large) die can fit on a single wafer (Oldham, 1991, 1977). Thus, typical commercial yields currently vary from as low as 30% to as high as 80%, depending on the complexity of the circuit, the maturity of the process, and the efficiency of the fab.

Cycle Time MARKETS-10

Cycle time is the elapsed time required to produce a chip. Overall cycle times, as well as the cycle times of each stage of the manufacturing process, are both important measures of manufacturing efficiency. Typical commercial fabs require between 30 - 70 days cycle time, depending on the complexity of the circuit.

IC manufacturing lines can be categorized by the number of wafers that are started per week (typically 5,000 to 10,000), and by the variety of products manufactured and processes used. A high volume line that produces commodity memory products (DRAM'S) might start up to 25,000 wafers per week and only use one process. A low volume line that produces a variety of products might start 1,000 to 5,000 wafers per week. A research and development (R&D) line that is used to develop new products and processes might start 500 wafers per week and use different processes for each lot.

Currently, US firms hold 36% of the world IC market share, and Japanese firms hold 52%. Since 1985, Japan has been ahead of the US in production and in research and development (R&D) investments. R&D investment is currently the most significant indicator of future performance, and the gap in R&D spending between the largest Japanese and US semiconductor suppliers is increasing. Also increasing is the gap between investment in equipment in Japan and the US (Longfellow et al, 1991).

Figure 29. World IC production by region PRODGRAPH

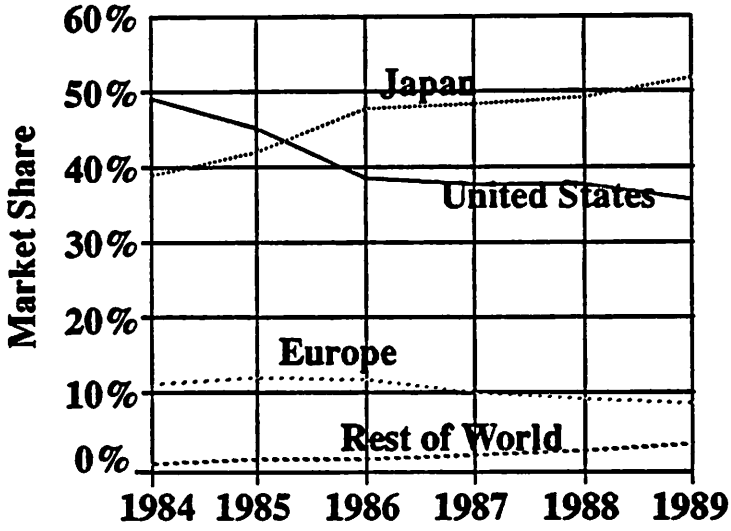


Figure 30.Semiconductor R&D spending RD-GRAPH

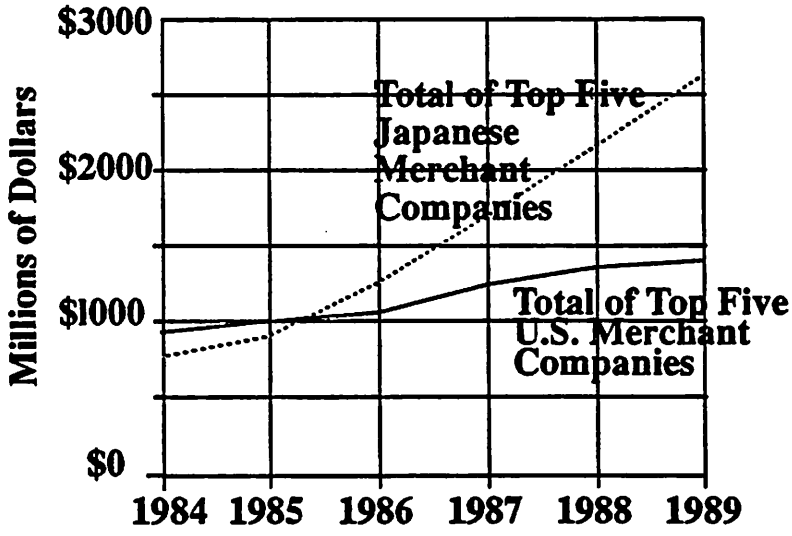
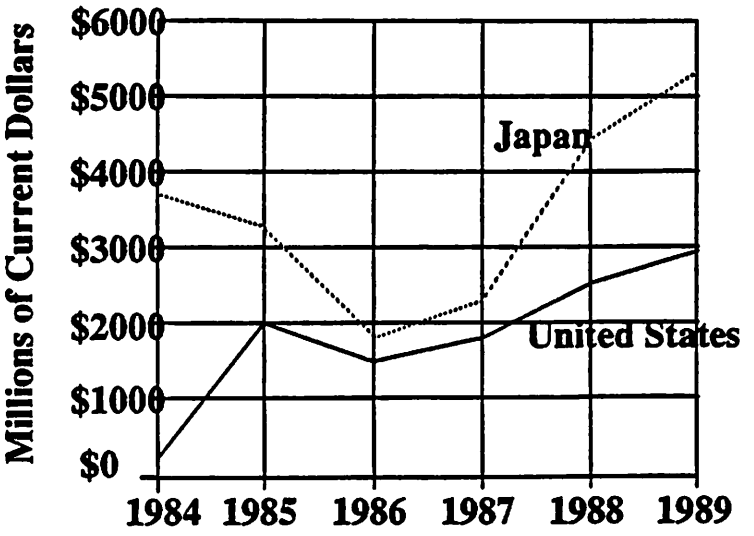


Figure 31. Semiconductor capital equipment spending **EQUIPGRAPH**



There are four key causes of the declining market share of US IC companies. First, US capital expenses, such as for facilities and workers, are higher than foreign capital expenses. Thus businesses are less willing to invest, and consequently have shorter planning horizons. Second, more final products such as display systems and disk drives are made outside of the US, and these products use fewer US components. Third, less emphasis has been placed on manufacturing (compared to innovative design) in the US, so US manufacturing quality suffers. Japanese firms have tended to focus more heavily on manufacturing and yield. Fourth, a tighter coupling between final product makers and local (and inhouse) IC manufacturers has allowed Japanese firms to have access to the latest technology. As a result, Japanese firms have a stronger influence over the direction of technology development.

In order for the US semiconductor industry to remain competative in the worldwide markets, it must increase its participation in projected critically important high-volume markets, and increase R&D funding. The role of academic research could also be strengthened, support for students and education increased, and incentives such as reduced IC manufacturing equipment depreciation schedules could be introduced.

Mass IC Production and Cost **MARKETS-4**

Today, a competative IC manufacturing facility produces 3000 wafers per week at a cost of $750M (where $500M is for equipment alone). Fabrication of the small planar features that characterize IC's requires complex equipment that changes quickly as technology advances. Thus, IC equipment becomes rapidly obsolete. Equipment costs have risen 100 times their cost 30 years ago, and equipment lifecycles are typically no more than three years in length (Moore, 91).

The uncommonly short lifespan of IC facilities and equipment, coupled with extraordinarily rapid change in technology and products, has resulted in exceptionally high costs for remaining competative with Japanese firms in the international market. The typical lifespan for a fabrication line is 5 to 10 years, of which at most 5 will be years when the line is at the leading edge.

High Volume Electronic Markets MARKETS-5

Three emerging markets show potential for high growth and strong influence in determining future technologies used in several major products. These markets are consumer electronics, broadband communications, advanced display systems, and intelligent vehicles and highway systems.

Broadband Communications MARKETS-6

Broadband Integrated Services Digital Network (ISDN) transmissions will allow a single optical fiber connection to transmit digital video signals, telephone conversations, and data simultaneously to end users. The demand for electronic and optoelectric components (such as lasers, amplifiers, and advanced high-speed IC's to implement signal processing and communications algorithms) along with equipment to digitize, code, transmit, receive, and decode data at high speed frequencies will be served by IC manufacturers. Also in demand will be a wide-range of consumer products such as cellular phones, high- definition video receivers and video recorders, plus many new products that have no equivalent today.

The expanded array of serviced available through broadband networks will reduce the time and expense of traveling to collect information, increase in the range of educational and entertainment materials available, and diminish the need for workers to be physically located together at a common workplace. Access to video services, information databases, electronic mail, and computer networks through a single seamless network will be possible. As a result, and increasing number of workers will soon have the option of exchanging work and ideas from home.

Advanced Display Systems MARKETS-7

Advanced Display Systems (ADS) require advanced sensors and displays, memories (to store images), image processors, and display drivers. Flat panel human-machine interface displays will eventually replace much of todays cathode ray tube (CRT) technology, and will do so reliably, using much less power, and in smaller packaging. The demand for ADS for computers, workstations, and televisions will challenge the US IC industry. If this challenge isn't met, lighter, fully assembled TV's, computers and workstations will be shipped from overseas (and thus will be made of fewer US produced IC components). These systems will replace US products, adversely affecting US jobs and sales (Longfellow et al, 1991).

Intelligent Vehicle and Highway Systems MARKETS-8

Intelligent Vehicle and Highway Systems (IVHS) refers to new technologies that will greatly increase highway and automobile efficiency and safety. IVHS electronics will require microprocessors, signal processors, and memories embedded in automotive controls and communications systems, as well as IC components for satellite receivers, sensors, radar-based collision-avoidance systems, and distributed highway control systems. Major IVHS projects are currently underway in Europe and Japan, and US firms are in a good position to serve the projected demand for IC components.

Consumer Electronics MARKETS-9

A wide range of consumer products, such as camcorders, high- definition video receivers and video recorders, high-definition television (HDTV), cellular phones, facsimile machines, personal computers, plus many new products that have no equivalent today, will be in high demand in the

near future. These next-generation products will require new chips. The impact on US electronics firms, and the IC manufacturers who supply them, will be great as long as US firms remain competative by contributing to the advancement of chip design, packaging, software, and manufacturing technologies.

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Appendix A: IC-HIP nodes, types, and links

Text nodes:

INTRO-0 An Introduction to Microelectronics Manufacturing and Markets
links to: WAFER ELEM-0 FAB-0 CIM-0 MICROLAB-0 MARKETS-0 REFS-0
ELEM-0 A Review of Microelectronic Circuit Elements
links to: ELEM-1 ELEM-1 ELEM-3 ELEM-4 ELEM-5 ELEM-8 ELEM-6 ELEM-7
ELEM-1 Transistors
links to: ELEM-4 ELEM-7 FAB-12 TRANSCIRCUIT TRANSPIC TRANSDEMO
ELEM-2 Resistors
links to: RESISTORCIRCUIT ELEM-4 FAB-12 RESISTORPIC
ELEM-3 Capacitors
links to: CAPCIRCUIT FAB-12 ELEM-4 CAPPIC
ELEM-4 Semiconductors
links to: ELEM-5 FAB-12 PHOSDOPE
ELEM-5 The Virtues of Silicon
links to: ELEM-8
ELEM-6 Digital Logic Circuit Technologies
links to: ELEM-7 ELEM-1 ELEM-9 ELEM-10
ELEM-7 Timeline of Electronic Technology Evolution
ELEM-8 Gallium Arsenide
links to: ELEM-4 ELEM-5
ELEM-9 Bipolar Technologies
links to: ELEM-10 ELEM-11
ELEM-10 MOS Technologies
links to: CMOS-TRANS ELEM-9 ELEM-11
ELEM-11 Summary of Important Electronic Technologies
links to: ELEM-9 ELEM-10
FAB-0 IC Manufacturing
links to: CIM-1 ELEM-4 ELEM-5 CYLINDER FAB-6 MARKETS-2 MARKETS-10 MARKETS-4
FAB-1 Stage 1: Wafer Fabrication
links to: FAB-7 FAB-8 FAB-11 FAB-12 ELEM-1 FAB-13 FAB-6 EQUIP MICROLAB-2 FAB-5
FAB-2 Stage 2: Wafer Probe and Sorting
links to: FAB-3 TEST YIELD FAB-6"
FAB-3 Stage 3: Chip Assembly
links to: FAB-6 ASSEMBLY
FAB-4 Stage 4: Chip Test and Burn-in
links to: FAB-3 CHIPSORT FAB-6
FAB-5 Student CMOS Fabrication Process
links to: MICROLAB-2 MASK-0 DEVL-42 SUBSTRATE-0 DEVL-26 DEPO-37 EXPO-38 DEVL-38 ETCH-39 DEPO-40 EXPO-41 DEVL-42
FAB-6 Four Main IC Manufacturing Stages
links to: MARKETS-10 MARKETS-2 FAB-1 FAB-2 FAB-3 FAB-4
FAB-7 Oxidation
links to: FAB-12 ELEM-1 MICROLAB-2 FAB-14 FURNACE FAB-5
FAB-8 Photolithography
links to: FAB-9 FAB-11 ELEM-7 SPIN-ON FAB-10 LITH-DEMO MICROLAB-2 FAB-5
FAB-9 Electron Beam and X-ray Lithography
links to: FAB-8 FAB-10 BEAMS
FAB-10 Photomasks
links to: PHOTOMASK CIM-1 FAB-9 BEAMS

FAB-11 Etching
links to: FAB-8 SEM MICROLAB-2 FAB-5
FAB-12 Methods of Doping (Ion Implantation)
links to: ELEM-1 FAB-8 DOPE
FAB-13 Deposition of Thin Films
links to: FAB-12 DEP MICROLAB-2 FAB-5
FAB-14 Example Process Flow Segment
CIM-0 Software Systems for IC Manufacturing
links to: CIM-1 CIM-2 CIM-3 MICROLAB-4 CIM-4 CIM-6 MICROLAB-2 CIM-5
CIM-1 Computer-aided Design
links to: FAB-8 CAD MICROLAB-2 CIM-0
CIM-2 Shop Floor Control with Work-in-Progress (WIP)
links to: FAB-0 CIM-5 FAB-4 FAB-6 MICROLAB-2 CIM-4
CIM-3 Process Simulation Systems
links to: SAMPLE MICROLAB-2
CIM-4 Order Entry and Production Control Software Systems
links to: CIM-2 CIM-5
CIM-5 Integrated Software Systems for IC Manufacturing
links to: CIM-2 CIM-4 CIM-4
CIM-6 Shared Integrated Databases
MICROLAB-0 The Berkeley Microfabrication Laboratory
links to: FAB-12 ULAB-OVERVIEW ULAB-HISTORY ULAB-EQUIP ULAB-CONTROL ULAB-ACCESS CIM-0 MICROLAB-1 CIM-1 CIM-3 MICROLAB-2 MICROLAB-3 MICROLAB-4
MICROLAB-1 The WAND
MICROLAB-2 Berkeley Process-Flow Language (BPFL)
links to: FAB-0 CIM-0 FAB-6 FAB-14 CIM-2 CIM-3 ELEM-1 FAB-5
MICROLAB-3 Faults
MICROLAB-4 Operation of the Microlab
links to: CIM-0 CIM-6 CIM-2 CIMTOOL
MARKETS-0 The Worldwide IC Markets
links to: MARKETS-2 MARKETS-10 MARKETS-4 MARKETS-5 MARKETS-3 MARKETS-1
MARKETS-1 Economics Chart
links to: MARKETS-2 MARKETS-2
MARKETS-2 Yield
links to: FAB-6 MARKETS-3 YIELD
MARKETS-3 Comparing Japanese and United States IC Industries
links to: PRODGRAPH RD-GRAPH EQUIPGRAPH MARKETS-5
MARKETS-4 Mass IC Production and Cost
links to: MARKETS-1 MARKETS-3
MARKETS-5 High Volume Electronic Markets
links to: MARKETS-9 MARKETS-6 MARKETS-7 MARKETS-8
MARKETS-6 Broadband Communications
MARKETS-7 Advanced Display Systems
MARKETS-8 Intelligent Vehicle and Highway Systems
MARKETS-9 Consumer Electronics
MARKETS-10 Cycle Time
REFS-0 References and Further Information

Image nodes:

MASK-0 Student CMOS VLSI layout
DEVL-42 Student CMOS wafer profile at the end of fabrication
SAMPLE A sample wafer profile
SUBSTRATE-0 Student CMOS wafer substrate profile
DEVL-26 Student CMOS wafer profile after putting down poly layer
DEPO-37 Student CMOS wafer profile after depositing silicon glass
DEVL-38 Student CMOS wafer profile after putting down contacts
ETCH-39 Student CMOS wafer profile after removing oxide
DEPO-40 Student CMOS wafer profile after depositing aluminum
RESISTORCIRCUIT Resistor diagram (symbol)
TRANSCIRCUIT A MOS Transistor diagram (symbol)
TRANSPIC An IC NMOS transistor (microelectric component)
RESISTORPIC An IC resistor (microelectronic component)
CAPCIRCUIT Capacitor diagram (symbol)
CAPPIC An IC capacitor (microelectronic component)
PHOSDOPE Phosphorus-doped silicon lattice with excess electrons
CMOS-TRANS A CMOS transistor
CIMTOOL CIM Browser program
PRODGRAPH World IC production by region
RD-GRAPH Semiconductor R&D spending
EQUIPGRAPH Semiconductor capical equipment spending
CAD Computer Aided Design circuit layout
CYLINDER Silicon cylinder growth
TEST Testing a circuit
ASSEMBLY Chip assembly
SORT Chip sort
FURNACE Wafers exiting oxide furnace
PHOTOMASK A photomask
SPIN-ON Covering a wafer with resist
SEM Etched surface, from a scanning electron microscope
DOPE Ion implantation
DEP Deposition of metal
WAFER Silicon wafer with 470 computer chips
YIELD Effects of doubling die size on yield

Video nodes:

ULAB-OVERVIEW Overview of the Berkeley microlab
ULAB-HISTORY History of the Berkeley microlab
ULAB-EQUIP Equipment used in the Berkeley microlab
ULAB-CONTROL Control in the Berkeley microlab
ULAB-ACCESS Access to the Berkeley microlab
TRANSDEMO Making a transistor (EECS 143 demo)
BEAMS E-beam and X-ray lithography (EECS 143 lecture)
EQUIP Equipment used in semiconductor manufacturing (EECS 143 lecture)
LITH-DEMO The photolithographic process (EECS 143 demo)