DENSE OPTICAL INTERCONNECTS FOR HIGH SPEED DIGITAL SYSTEMS

by

Chung-Sheng Li

Memorandum No. UCB/ERL M92/59

2 June 1992

DENSE OPTICAL INTERCONNECTS FOR HIGH SPEED DIGITAL SYSTEMS

by

Chung-Sheng Li

Memorandum No. UCB/ERL M92/59

2 June 1992

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

DENSE OPTICAL INTERCONNECTS FOR HIGH SPEED DIGITAL SYSTEMS

by

Chung-Sheng Li

Memorandum No. UCB/ERL M92/59

2 June 1992

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

DENSE OPTICAL INTERCONNECTS FOR HIGH SPEED DIGITAL SYSTEMS

by

Chung-Sheng Li

Abstract

Optical interconnect technology has the potential to provide larger bandwidth and better noise immunity than existing electrical interconnect technology for high-speed digital systems. Both the bandwidth and the noise immunity are limited in the electrical interconnect technology at the backplane, the board, and the multi-chip-module levels by problems such as reflections, ground-loop noise, crosstalk, frequency-dependent signal distortion, and capacitive loading effect. However, an optical interconnect system might still be limited in density and speed due to optical and electrical crosstalk either from neighboring channels or through the shared power supply. This thesis is thus focused on analyzing problems arising from using dense optical interconnects in a high-speed digital system.

Fully Differential Optical Interconnect. A fully differential optical interconnect concept is proposed and analyzed in this thesis to overcome the electrical noise problems. Furthermore, a series of fully differential driver and receiver array chips with maximum array size from 4 to 12 using advanced bipolar, BiCMOS and GaAs technology have been designed and fabricated. Extensive circuit simulations verify the new design of the driver and the receiver, which are fully functional at 2.5 and 1 Gbps, respectively, with the capability of supporting less than 200ps signal rise time. In order to address the electrical packaging issues, models of the laser transmitter array and receiver array are developed to examine the influences of system performance through thermal noise, parasitic capacitance, and coupling through the substrate and power supply. Our study shows that it is possible to drive a large number of differentially configured laser drivers and receivers (≥ 32 if the maximum allowable switching noise is 25%) at 1 Gbps in a monolithic integration environment using a common power supply. Single-ended drivers or receivers are far more sensitive to noise, and are not recommended for this application.

Interconnect Density. Crosstalk models that incorporate detailed device models for each individual optical and optoelectronical component in a system have been developed and used to evaluate the density of the optical channels in a waveguide array environment as well as in a Wavelength-Division-Multiplexed (WDM) environment. The results show that the interference between the waveguides can contribute a significant amount of crosstalk, and the effect depends on the coherence of the signals carried in the adjacent waveguides. Using a 1 dB power penalty criterion, we show that the crosstalk between adjacent waveguides must be smaller than -12 dB and -25 dB for wavelength noncoinciding and coinciding monochromatic light sources, respectively, in order to achieve a bit-error rate smaller than 10^{-15}. These crosstalk requirements limit the spacing between adjacent single-mode waveguides to $\approx$ 10 μm. Instead of transmitting different channels through different waveguides, it is also possible to transmit different channels through the same waveguide but at different wavelengths. In contrast to a waveguide-based interconnect system, channel den-

sity of a WDM-based system using OOK is limited by the transient chirp of the laser diode and the crosstalk allowed by the optical filter. The combined effect is significant for high bit-rate channels. Our results indicate that a minimum channel spacing of ≥ 30 GHz, with each channel operating at 2 Gbps, is needed with the use of commercially available DFB laser diodes and optical filters.

System Requirements. Analytical models for high-speed synchronous and self-timed interconnect systems have been developed and analyzed to derive system-level requirements (such as rise time, the maximum allowable skew, and the latency) of using optical interconnects for high speed digital systems. Optical clock distribution using single-stage architecture and multi-stage architecture with optical amplifiers has been evaluated using these models. The results show that such a multi-stage distribution network can improve the total number of fanout by several orders of magnitude when compared to that obtained from a single-stage distribution network. Experimental results are consistent with those predicted by the analytical model.

David G. Messerschmitt 11/27/91

Professor David G. Messerschmitt
Chairman, Thesis Committee

To my parents,

An-Min and Kuei-Yueh Li

ACKNOWLEDGEMENTS

I am grateful to my advisor, Prof. David G. Messerschmitt, for his generous and continuous support, encouragement and guidance throughout my graduate career. My supervisor at IBM, Dr. Harold S. Stone, who also served on my thesis committee, has been a tremendous source of guidance, support, and inspiration during the last two years. I also wish to thank Dr. Paul E. Green Jr. for his technical guidance in my WDM/WDMA work and his generosity in providing lab space during my stay in IBM, and thank Dr. Stephen S. Lavenberg for his unreserved support of my projects during my stay in IBM. Many thanks go to Drs. Karen Liu, Franklin Tong, C. Michael Olsen, Michael M. Choy, Rajiv Ramaswami, Richard Bates, and John D. Crow, who have been of great help in giving me basic understanding of optical devices and systems, and to Drs. Kai-Yap Toh, Young Hoon Kwark, Peter Lim, and Dennis Rogers, who assisted me in understanding circuit design, and to Drs. Y. Kwark, F. Tong, Randall A. Cieslak, Kumar Sivaraj, and Rajesh Pankaj for their careful reviewing of the chapters in this thesis.

I would like to thank Profs. T. K. Gustafson, Paul R. Gray, Michael Klass, for serving on my qualifying examination committee, and Profs. Joseph M. Kahn and Michael Klass for participating in my thesis committee. I would also like to thank numerous discussions with Profs. Kam Lau, Randy Katz, Jean Walrand, Richard Newton, Robert G. Meyer, and Abhiram Ranade during my graduate study.

The work reported here was supported by California MICRO and a grant from IBM. This work is performed at both U.C. Berkeley and IBM Thomas J. Watson Research Center, Yorktown Heights, New York.

The transmission line models in Chapter 2 are characterized by W. P. Smetana and A. Deutsch. Chapters 4 and 6 of this thesis were joint work with F. Tong and K. Liu, Chapter 5 was joint work with C. M. Olsen. Chapter 8 has used simulation models from K. Toh and D. Rogers. Chapter 10 came out of a collaboration with K. Toh and H. Ainspan. Chapter 11 uses a circuit designed by Y. Kwark and also came out of a collaboration with Y. Kwark and K. Wrenner. The

chip photographs in Chapter 11 were taken by K. P. Jackson, digitized by J. C. Lee, and the digitized images were processed using a halftoning program developed by G. R. Thompson.

Finally, a word of thanks to Ming-Kang Liu, Ping-San Tzeng, Bernard Shung, Alex Lee, Ming-Chang Wu, Wen-Lung Chen, Teresa H.-Y. Meng, Horng-dar Lin, Limin Hu, Shih-Fu Chang, Vijay Maddisetti, Meng-Hsiung Kiang and many others of my friends who continuously provide moral and technical support during my graduate study in Berkeley, and to Long-Sheng Fan in particular, for many inspirational days when we live in the same house. I am also grateful to Wei-Yi Li, my nephew, for his help in serving as a great communicator between me and Berkeley while I was in New York.

Contents

CHAPTER 1 INTRODUCTION 1

1.1 Motivation 1

1.1.1 Reflections 3

1.1.2 Ground-loop noise 4

1.1.3 Crosstalk among adjacent interconnects 4

1.1.4 Frequency-dependent signal distortion 5

1.2 Optical Interconnects for High-Speed Digital Systems 5

1.2.1 Potential advantages 6

1.2.2 Potential problems 7

1.3 Architecture of Dense Optical Interconnects 9

1.3.1 Interconnect media 9

1.3.2 Backplane optical interconnects 10

1.3.3 Board and multi-chip-module optical interconnects 11

1.4 Differential Optical Interconnection 13

1.5 Prior Art of Optical Interconnects 16

1.6 Contribution of This Thesis 16

1.7 Thesis Outline 17

CHAPTER 2 MODELING AND PERFORMANCE EVALUATION OF METAL INTERCONNECTS 19

2.1 Introduction 19

2.2 Multi-Chip Module Level Metal Interconnects 21

2.2.1 Modeling 21

2.2.2 Simulation Results 25

2.3 Board Level Metal Interconnects 28

2.3.1 Modeling 28

2.3.2 Simulation Results 30
2.4 Backplane Level Metal Interconnects 32
2.4.1 Modeling 32
2.4.2 Simulation Results 34
2.5 Summary 36

CHAPTER 3 STATISTICAL ANALYSIS OF TIMING RULES FOR SYNCHRONOUS INTERCONNECTS 41
3.1 Introduction 41
3.2 Sources of Timing Skew 43
3.2.1 Static skew 46
3.2.1.1 Variation of propagation length and signal group velocity 46
3.2.1.2 Device Variation 47
3.2.2 Random skew 49
3.2.2.1 Timing Jitter on the Clock Sources 49
3.2.2.2 Circuit Noise 49
3.3 Timing Rules for Synchronous Bus Systems 50
3.3.1 Conservative design 51
3.3.2 Aggressive design 56
3.4 Timing Rules for Finite State Machines 58
3.5 Throughput Improvement from Pipelined Architecture 61
3.5.1 Pipelined approach 61
3.5.2 Nonpipelined approach 64
3.6 Numerical Results 66
3.7 Summary 70

CHAPTER 4 CLOCK DISTRIBUTION USING OPTICAL AMPLIFIERS 71
4.1 Introduction 71
4.2 Architecture of Clock Distribution Networks 73

4.3 Clock Skew Analysis 74
4.3.1 Distribution skew 76
4.3.2 Receiver static skew 77
4.3.3 Receiver random skew 79
4.4 Maximum Fanout of a Single-Stage Clock Distribution Network 81
4.5 Maximum Fanout For Multistage Distribution Network 88
4.5.1 Modeling of multi-stage amplifier chain 88
4.5.2 Maximum fanout calculation 89
4.6 Experimental Results 98
4.7 Summary 103

CHAPTER 5 CROSSTALK MODELING OF DENSE SINGLE-MODE WAVEGUIDE ARRAY 109
5.1 Introduction 109
5.2 Waveguide Array Model 110
5.3 Formulation of Waveguide Crosstalk 117
5.3.1 Adjacent channel crosstalk 117
5.3.2 Total receiver noise 119
5.3.3 Calculation of optimal threshold level 120
5.4 SYSTEM PENALTY DUE TO ADJACENT CHANNEL CROSSTALK 121
5.4.1 Noncoinciding Uncorrelated Light Sources 121
5.4.2 Coinciding Uncorrelated Light Sources 124
5.4.3 Coinciding Correlated Light Sources 125
5.4.4 Discussion 127
5.5 SUMMARY 132

CHAPTER 6 DENSE WDM/WDMA SYSTEMS 143
6.1 Introduction 143
6.2 Derivation of System Penalty 145

6.3 Simulation Models 148
6.4 Simulation 155
6.5 System Optimization 173
6.6 Dense WDM/WDMA-FSK Systems 181
6.7 Conclusions 186

CHAPTER 7 DENSE TRANSMITTER ARRAYS 187
7.1 Introduction 187
7.2 Transmitter Array Modeling 188
7.2.1 Laser Modeling 188
7.2.2 Single-Ended Driver 190
7.2.3 Differential Driver 190
7.3 Switching Noise Analysis of Single-Ended Driver 191
7.4 Simulation of Differential Driver 193
7.4.1 Simulation Methodology 193
7.4.2 Simulation Results 194
7.5 Summary 196

CHAPTER 8 DENSE RECEIVER ARRAYS 201
8.1 Introduction 201
8.2 Receiver Array Model 203
8.3 Simulation Methodology 206
8.4 Single-Ended Receiver 206
8.5 Differential Receivers 213
8.6 Summary 213

CHAPTER 9 DIFFERENTIAL OPTICAL INTERCONNECTS 217
9.1 Introduction 217
9.2 Optical Interconnect Architectures 219

9.2.1 Single-Ended Interconnect 219
9.2.1.1 Disadvantages 219
9.2.1.2 Advantages 222
9.2.2 Differential Interconnect 222
9.2.2.1 Disadvantages 222
9.2.2.2 Advantages 223
9.3 Implementation of Differential Optical Interconnects 225
9.3.1 External Modulators 225
9.3.2 Time Division Multiplexing Technique 228
9.3.3 Frequency Division Multiplexing Technique 230
9.3.4 Wavelength Division Multiplexing 231
9.3.5 Polarization Division Multiplexing Technique 233
9.4 Receiver Sensitivity Analysis 234
9.4.1 Single-ended optical interconnect 234
9.4.2 Differential Optical Interconnect 239
9.5 System Degradation Due to Channel Mismatch 242
9.5.1 Threshold Offset 242
9.5.2 System Penalty 246
9.6 Mismatch Cancellation Techniques 247
9.6.1 Periodic Null Insertion 247
9.6.2 Average Computation 248
9.6.3 Decision Feedback Average Computation 248
9.7 Summary 248

CHAPTER 10 FULLY DIFFERENTIAL TRANSMITTER ARRAY 251
10.1 Introduction 251
10.2 Circuit Design 252
10.3 Physical Circuit Layout 255
10.4 Simulation Results 256

10.5 Summary 261

CHAPTER 11 FULLY DIFFERENTIAL INTEGRATED OPTICAL RECEIVER ARRAY 267

11.1 Introduction 267

11.2 Circuit Design 268

11.2.1 Preamplifier Array 268

11.2.2 Full Receiver Array 272

11.3 Receiver Sensitivity and Front-End Optimization 273

11.3.1 Receiver Sensitivity 273

11.3.2 Preamp Optimization 274

11.3.3 MSM-PD Optimization 280

11.4 Chip Photographs of the Receiver Array 284

11.4.1 Receiver Cell 284

11.4.2 Integrated Receiver Array 284

11.5 Simulation Results 284

11.6 Summary 287

CHAPTER 12 SUMMARY AND FUTURE WORK 307

12.1 Summary 307

12.2 Future Work 309

12.2.1 Multi-Mode Waveguide 309

12.2.2 Fault-Tolerant Interconnect Architecture 310

12.2.3 Impact of Optical Interconnects on Computer Architecture 310

12.2.4 Integration of Optical Interconnect with Electronic or Photonic Switching 311

Bibliography **315**

List of Illustrations

1-1. Packaging hierarchy 2

1-2. Optical backplane interconnects 11

1-3. Optical backplane interconnects 12

1-4. E/O and O/E conversion 13

1-5. E/O and O/E conversion 14

1-6. A fully differential optical interconnect architecture 15

2-1. Structure of an electrical path for an MCM interconnect 22

2-2. Circuit model of a typical multi-chip module interconnect 23

2-3. Equivalent circuit for a electrical discontinuity 24

2-4. ECL driver and receiver circuit used for simulations 25

2-5. Simulated eye pattern of an MCM interconnect 26

2-6. Simulated eye pattern of an MCM interconnect 27

2-7. Simulated eye pattern of an MCM interconnect 28

2-8. Structure of a board level interconnect 29

2-9. Equivalent circuit of a board level metal interconnect 30

2-10. Simulated eye pattern of a board level interconnect 31

2-11. Simulated eye pattern of a board level interconnect 32

2-12. Simulated eye pattern of a board level interconnect 33

2-13. Structure of a backplane interconnect 34

2-14. Equivalent circuit of a backplane level interconnect 35

2-15. Equivalent circuit of a cable connector 36

2-16. Simulated eye pattern of a backplane interconnect 37

2-17. Simulated eye pattern of a backplane interconnect 38

2-18. Simulated eye pattern of a backplane interconnect 39

3-1. Architecture of a synchronous digital system 44

3-2. Timing relationship between the data input, clock input and the data output of a latch 45

3-3. Circuitry of a typical ECL gate 48
3-4. Architecture of a synchronous bus 51
3-5. Timing relationship between the transmitter and the receiver in a synchronous bus 52
3-6. Timing relationship between the transmitter and the receiver in a synchronous bus 53
3-7. Architecture of a finite state machine 59
3-8. Architecture of a pipelined system 62
3-9. Minimum cycle time as a function of the standard deviation of the random skew . 65
3-10. Minimum cycle time as a function of the standard deviation of the random skew for conservative design scheme 66
3-11. Minimum cycle time as a function of the standard deviation of the random skew for the aggressive design scheme 67
3-12. Minimum cycle time as a function of the standard deviation of the random skew for the aggressive design scheme 68
3-13. Minimum cycle time as a function of the standard deviation of the static skew for the aggressive design scheme 69
4-1. Architecture of a single-stage optical clock distribution 74
4-2. Architecture of a multi-stage optical clock distribution 75
4-3. Circuit schematic of a typical CMOS flip-flop 80
4-4. Maximum fanout as a function of avalanche gain for various ionization factor . . . 81
4-5. Maximum fanout of a single-stage clock distribution network 82
4-6. Maximum fanout as a function of extinction ratio for various values of avalanche gain 83
4-7. Maximum fanout as a function of receiver voltage noise for various values of clock rise time 84
4-8. Maximum fanout as a function of receiver current noise for various values of clock rise time 85
4-9. Maximum fanout as a function of distribution skew for various clock rise time . . . 90
4-10. Maximum fanout is plotted against distribution skew for various values of optical filter bandwidth 91
4-11. Maximum fanout as a function of clock rise time for various optical filter bandwidths 92

4-12. Maximum fanout vs. optical filter bandwidth for various clock rise time 93
4-13. Maximum fanout as a function of avalanche gain for various values of ionization factor 94
4-14. Maximum fanout as a function of branch loss for various optical filter bandwidths 95
4-15. Maximum fanout as a function of extinction ratio of the clock signal for various values of laser output power 96
4-16. Maximum fanout vs. receiver voltage noise for various optical filter bandwidth . . . 97
4-17. Maximum fanout as a function of amplifier gain for various optical filter bandwidths 98
4-18. Schematic of the clock distribution experiment setup 99
4-19. Jitter as a function of second-stage splitting 100
4-20. Comparison of experimental and calculated constant rms jitter contour 101
4-21. Total attenuation is plotted against the first stage attenuation for various values of constant rms jitter 102
5-1. Structure of a buried-structure single-mode waveguide array 111
5-2. Power coupling between two waveguides as a function of waveguide separation . 112
5-3. Power coupling between two waveguides as a function of waveguide separation . 113
5-4. Power coupling between two waveguides as a function of waveguide separation . 114
5-5. Power coupling between five waveguides 115
5-6. Power penalty vs. frequency spacing 122
5-7. Power penalty vs. crosstalk 125
5-8. Power penalty vs. laser linewidth 126
5-9. Power penalty vs. crosstalk for various phase difference 127
5-10. Power penalty vs. phase difference 128
5-11. Threshold vs. crosstalk for various phase difference 129
5-12. Threshold vs. phase difference 130
5-13. Power penalty vs. crosstalk comparison for difference source conditions 131
5-14. Maximum allowable crosstalk vs. position of the threshold 132
6-1. Architecture of a typical N-channel WDM/WDMA backplane 144
6-2. A typical eye pattern showing the horizontal and vertical eye opening. 147

6-3. System configuration for a single channel. 149
6-4. Frequency response of a Fabry-Perot filter 153
6-5. Simulated output of instantaneous optical power of a DFB laser using bit pattern 0011110000 156
6-6. Simulated output of instantaneous chirp frequency of a DFB laser using bit pattern 0011110000 157
6-7. Simulated output of instantaneous optical power of a DFB laser using bit pattern 0000010000 158
6-8. Simulated output of instantaneous chirp frequency of a DFB laser using bit pattern 0000010000 159
6-9. Simulated output of instantaneous optical power of a DFB laser using bit pattern 0001010000 160
6-10. Simulated output of instantaneous chirp frequency of a DFB laser using bit pattern 0001010000 161
6-11. Simulated eye pattern in the absence of a FP filter 162
6-12. Simulated eye pattern in the presence of a FP filter with bandwidth = 20 GHz . . 163
6-13. Power penalty versus bit rate for various filter bandwidth 164
6-14. Eye degradation from the ideal ONE signal level as a function of bit rate 165
6-15. Eye degradation from the ideal ZERO signal level as a function of bit rate 166
6-16. Eye-closure as a function of bit rate. 167
6-17. Horizontal eye closure versus bit rate at various filter bandwidth 168
6-18. Power penalty as a function of FWHM 169
6-19. Horizontal eye-closure as a function of FWHM 170
6-20. Power penalty as a function of the skew between the interfering channels and the signal channel for N = 128 and 256 171
6-21. Power penalty versus number of stations at 1, 2, and 3 Gbps 172
6-22. Power penalty versus number of stations at filter bandwidth of 10, 20, 30 GHz . . 173
6-23. Comparison of results between with chirp and without chirp for power penalty versus number of stations 174

6-24. Power penalty versus filter bandwidth at various filter bandwidth 175
6-25. Horizontal eye-closure is plotted against the number of stations at filter bandwidth of 10, 20, and 30 GHz 176
6-26. Power penalty is plotted against linewidth enhancement factor 177
6-27. Power penalty as a function of the center frequency of the FP filter 178
6-28. Power penalty as a function of filter center frequency 179
6-29. Power penalty as a function of laser bias current 180
6-30. Power penalty as a function of filter center frequency 181
6-31. Power penalty as a function of rise time 182
6-32. Single-channel power penalty as a function of filter bandwidth 183
6-33. Multi-channel power penalty vs. channel spacing for filter bandwidth of 2 and 3 GHz 184
6-34. Power penalty vs. linewidth enhancement factor for various nonlinear-gain-suppresion ratio 185
7-1. Block diagram of a transmitter array 189
7-2. Circuit Model of a laser diode 190
7-3. Circuit diagram of a single-ended laser driver 191
7-4. Circuit diagram of a differential laser driver 192
7-5. Switching noise waveform of the laser driver 194
7-6. Switching noise waveform of the laser driver 195
7-7. Switching noise waveform of the laser driver 196
7-8. Switching noise as a function of the array size 197
7-9. Switching noise as a function of the lead inductance 198
7-10. Switching noise as a function of decoupling capacitance 199
8-1. Basic configuration of a receiver array with common power supply and ground . 204
8-2. Circuit configuration of a single-ended receiver 205
8-3. Circuit configuration of a differential receiver 206
8-4. Switching noise waveform 207
8-5. Switching noise versus photodetector capacitance 208

8-6. Switching noise versus lead inductance for a single-ended configured receiver array with N = 16 209
8-7. Switching noise generated by a single-ended configured receiver as a function of array size 210
8-8. Switching noise generated by a single-ended configured receiver as a function of array size 211
8-9. Switching noise generated by a single-ended configured receiver as a function of array size 212
8-10. Switching noise generated by a differentially configured receiver array 214
8-11. Switching noise versus signal rise time for a differential receiver array with N = 16 215
8-12. Switching noise versus lead inductance for a differentially configured preamp . . . 216
9-1. Possible structures for a single-ended optical interconnect 220
9-2. Possible structures for a differentially configured optical interconnect 223
9-3. Structure of a Mach-Zehnder modulator 226
9-4. Structure of a directional coupler modulator 227
9-5. Structure of a modulator using total internal reflection 228
9-6. Structure of a multiple quantum well modulator 229
9-7. Structure of a differential optical interconnect using TDM 230
9-8. Structure of a differential optical interconnect using FSK 231
9-9. Structure of a differential optical interconnect using WDM 232
9-10. Structure of a differential optical interconnect using polarization division multiplexing 233
9-11. Full circuit of a differential receiver using in a single-ended optical interconnect . 235
9-12. Half circuit of a differential receiver using in a single-ended optical interconnect . 236
9-13. Full circuit of a differential receiver used in a differential optical interconnect . . . 240
9-14. Half circuit of a differential receiver used in a differential optical interconnect . . . 241
9-15. Power penalty as a function of threshold error 247
9-16. Structure of decision feedback optimal threshold computation 249
10-1. Circuit diagram of a fully differential driver 254

10-2. Circuit diagram of a fully differential transmitter array 256
10-3. Physical layout of a fully differential driver 257
10-4. Physical layout of a fully differential driver array 258
10-5. Block diagram of a differential transmitter array environment 259
10-6. Simulated eye pattern of a laser driver at 1Gbps 260
10-7. Simulated eye pattern of a laser driver at 2Gbps 261
10-8. Simulation of switching noise for a driver array at 1 Gbps 262
10-9. Simulation of switching noise for a driver array at 2 Gbps 263
10-10. Switching noise vs. N for a differential driver array 264
10-11. Crosstalk vs. mutual inductance for various driver array configurations 265
10-12. Comparison of switching noise vs. N between single-ended and differential driver array 266
11-1. Circuit block diagram of a fully differential preamplifier 269
11-2. Simplified circuit diagram of the transimpedance front-end 270
11-3. Circuit block diagram of a complete receiver 271
11-4. Half circuit of the fully differential receiver 274
11-5. Equivalent circuit of a cascode configured stage 275
11-6. Noise equivalent circuit of a cascode configured stage 276
11-7. Sensitivity vs. channel width of the input MESFET 277
11-8. Sensitivity vs. channel width of the input MESFET 278
11-9. Typical Structure of a MSM photodetector 281
11-10. Total MSM capacitance as a function of the finger spacing 282
11-11. Total MSM capacitance as a function of the finger width 283
11-12. Chip photograph of a single preamplifier cell 285
11-13. Chip photograph of a full receiver cell 286
11-14. Chip photograph of a 12-receiver array 287
11-15. Chip photograph of a 6-receiver array 288
11-16. Simulated eye pattern of the receiver response 289
11-17. Simulated eye pattern of the receiver response 290

11-18. Simulated eye pattern of the receiver response 291
11-19. Simulated eye pattern of the receiver response 292
11-20. Simulated eye pattern of the receiver response 293
11-21. Low frequency response of the receiver 294
11-22. Low frequency response of the receiver 295
11-23. Simulated switching noise of a preamp array 296
11-24. Simulated switching noise of a preamp array 297

CHAPTER 1 INTRODUCTION

1.1 Motivation

As technology progresses, the demand for high performance digital systems such as high-speed switching systems for broadband integrated service data network (B-ISDN) as well as general-purpose mainframes and workstations for scientific and business applications is unrelenting. Higher performance can be achieved through exploiting concurrent architectures such as parallelization [1] and pipelining of executions [2] or through the use of more advanced and faster technologies. Eventually the more advanced technologies can be applied to the concurrent architectural approaches, achieving increasingly better performance.

Faster devices are announced frequently [3, 4]. These leading devices include

- Super-self-aligned silicon bipolar technology [5],
- GaAs MESFET technology [6],
- high electron mobility transistor (HEMT) [7],
- heterojunction bipolar transistor (HBT) [8],
- Josephson junction technology [9].

These devices routinely demonstrate a gate delay of 30ps or less, and have good prospects in LSI/VLSI applications. Even the speed of CMOS VLSI is improving through either scaling or/and cooling down to liquid nitrogen temperature [10]. Yet speed of devices is not the only criterion that determines the acceptance of a technology. When these devices are used in a complicated system such as a high performance computer, problems of parasitics, circuit design, power consumption and packaging often dominate over sheer speed. Therefore, it is insufficient to improve the performance of a system simply by choosing a faster device technology. Packaging and interconnections also have to be taken into consideration in order to optimize the overall system performance. Currently available packaging and interconnect technology at various packaging levels are [11]:

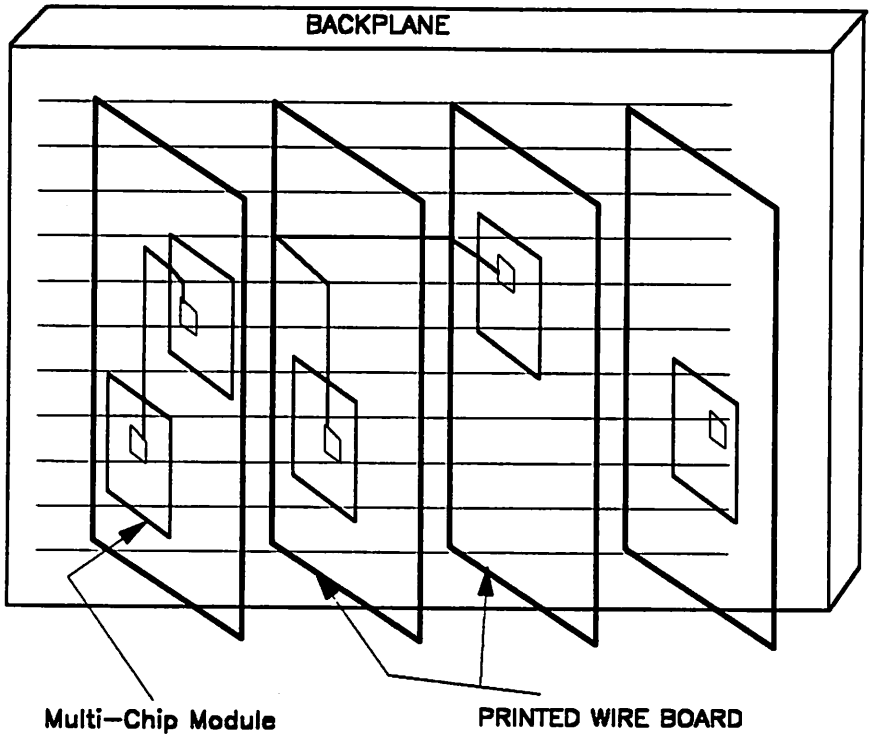

Figure 1-1. Packaging hierarchy. A typical packaging hierarchy, from bottom to top includes chips, multi-chip modules (MCM), cards, boards, and backplanes.

- Chip-to-package interconnections: These technologies include wirebonding, tape automated bonding (TAB), and flip-chip bonding using solder ball.
- Ceramic and plastic chip modules: Each module made of ceramic or plastic encapsulation contains a single chip (single chip module or SCM) or multiple chips (multichip module or MCM). The interconnections on these modules can have multiple signal layers using thin-film or thick-film processing techniques.[1]

[1] Thin-film packaging refers to packages in which the conductor and insulators are fabricated using deposition and patterning techniques similar to those used for fabricating integrated-circuit chips.

- Package-to-board interconnections: Existing technologies can be categorized as pin-through-hole (PTH), leadless chip carrier (LLCC), and surface mount technology (SMT). A through-hole on the printed circuit board is provided for each pin of a chip package in PTH. Both mechanical joint and solder joint are feasible for this technology. On the other hand, both LLCC and SMT, which are more area efficient and provide better signal quality, require solder joint between each lead of a package and the pad on a circuit board.
- Printed-circuit board: This technology has been around before 1960. The progress over the past 30 years includes the decrease in the through-hole diameter (from ~840 μm to ~350 μm), the increase in the through-hole density (from ~9 to ~ 64 /cm^2), the increase in the number of signal planes (from ~4 to ~ 50), and the decrease of the interconnect width (from ~250 μm to ~ 50 μm).

As the speed of devices increases, existing metallic interconnect technology is no longer adequate due to its performance degradation at high-frequency. Sources of performance degradation include

- Reflections,
- Ground-loop noise,
- Crosstalk among adjacent interconnects,
- Frequency dependent signal distortion.

We will now describe a few of these impairments.

1.1.1 Reflections

A high performance system requires more than one level of packaging and interconnects to accommodate complicated logic functions. A typical packaging hierarchy, as shown in Figure 1-1, includes chips, single-chip modules (SCM), multi-chip modules (MCM), cards, boards, and backplanes. However, electrical discontinuities exist between any two packaging levels. Discontinuities may be primarily inductive (such as electrical connectors) or capacitive (such as stubs in a multidrop net and 90-degree bends in a microstrip line). Depending upon the nature of the discontinuities and impedance changes, the resulting reflections may be either positive or negative.

Various methods exist to reduce the reflections resulting from impedance mismatch. For example, a termination resistor is usually placed at the receiving end of an interconnect in order to reduce the reflections. However, a perfect matching between the characteristic impedance of the interconnection and the impedance of the load is difficult to achieve because of the parasitic capacitance and inductance. If the round-trip propagation time between the source and the discontinuities is less than the rise time of the signal, these reflections can be absorbed by the interconnect driver with a net effect of an increased signal rise time. On the other hand, the waveform of the signal is severely degraded by the multiple reflections if the round-trip propagation time is longer than the rise time of the signal, resulting in a reduced noise margin or/and false switching.

1.1.2 Ground-loop noise

The ground plane of a packaging system usually cannot achieve zero resistance and inductance. Any local injection of current from the devices changes the electrical potential at that point. For a single-ended interconnection, the receiving side has to rely on the potential of the local ground plane as a reference to determine the amplitude of the incoming signals. Any disturbance of the ground plane is therefore coupled into the received signal.

One way of alleviating this problem is to transmit differential signals so that the signal can be interpreted unambiguously at the receiving end of an interconnect. However, the required interconnect density has to be doubled and thus more signal layers are necessary to accommodate the increased interconnect complexity. Some of the chips that are already pin-count-limited cannot afford this option either.

1.1.3 Crosstalk among adjacent interconnects

For a given interconnect density, crosstalk between adjacent interconnects increases as the rise time of the signal decreases. Furthermore, crosstalk of the transmission lines with a TEM or near-TEM structure,[2] such as slotted lines and microstrip lines, usually couple with switching noise and may consume the entire noise margin if they are not carefully controlled [12]. Therefore, either the interconnects have to be spaced farther apart or additional shielding lines have to be inserted

[2] TEM mode is the fundamental mode supported by a transmission line such as a coaxial cable. The transmission line structures that can support TEM mode are said to have TEM structures.

between signal lines to reduce crosstalk to an acceptable level. In both cases, the effective interconnect density is reduced.

1.1.4 Frequency-dependent signal distortion

Packaging discontinuities introduce frequency-dependent signal distortion as a result of the inductive or capacitive nature of the discontinuities. Additional signal distortion is introduced by the dispersion and the skin effect of metal interconnects.

The microstrip lines on a printed circuit board are inherently dispersive, since they are incapable of supporting a pure TEM mode [13]. The mode's effective dielectric constant is a function of frequency, causing different frequency components of the signal to travel at a different speed. This effect becomes significant when the rise time of the waveform is smaller than 100ps and the signal has to travel more than a few centimeters.

The skin effect also contributes to frequency-dependent signal distortion for metal interconnects when the thickness of the interconnects is large compared to the skin depth. Due to the skin effect, high-frequency components within the signal experience higher attenuation, yielding non-negligible waveform distortion. In order to reduce the skin effect, the thickness of the metal has to be less than the skin depth of the metal.[3] A wider transmission line is thus required to accommodate signals with higher data rate while maintaining an acceptable DC and low-frequency loss, resulting in a net reduction of the interconnect density.

1.2 Optical Interconnects for High-Speed Digital Systems

Because of the bandwidth bottleneck associated with the existing interconnect and packaging technology, optical interconnect using free-space, optical waveguides or optical fiber thus becomes a viable and attractive alternative to increase the total system throughput. In this thesis, issues associated with using optical interconnect for high-speed digital systems are investigated. In particular, we will examine the potential problems and solutions of using dense optical interconnects for high-performance digital systems. In such systems, serialization of data cannot be employed to

[3] The skin depth of copper is 2 μm at 1 GHz, and becomes 0.7 μm at 10GHz.

increase the channel density if the data rate of each channel is very high before serialization is introduced. Therefore, an interconnect technology with the capability of providing high density and high bandwidth is necessary for acceptance in digital systems.

1.2.1 Potential advantages

Dense optical interconnects have the potential of offering the following advantages:

- More sophisticated interconnection pattern. Light beams from different sources do not interfere with each other upon crossing. Very sophisticated 2-D and 3-D interconnect patterns based on planar optical waveguide and free space interconnect technologies, respectively, can thus be built from this principle, achieving a higher packaging density and shorter average signal propagation distance.
- Electrical reflection reduction. The reflections due to electrical discontinuities of a packaging system does not seriously affect the signal waveform as long as the round-trip propagation delay is less than the rise-time of the signal waveform. Therefore, multiple reflections due to impedance mismatch between different levels of packaging can be reduced or eliminated by replacing metal interconnects on higher packaging levels (such as the boards and the backplanes) with optical interconnects so that the round-trip propagation delay of any metal interconnects is shorter than the signal rise time.
- Higher bandwidth. The bandwidth of the optical interconnects is mainly limited by the interface electronics and has the potential to achieve a multi-gigabit data rate with very little signal distortion.
- Higher spatial density. The potential spatial density of either optical-waveguide or free-space interconnect technology is an order of magnitude higher than what can be achieved by the current metal interconnect technology (line spacing between two thin-film metal interconnects is ≥ 25 μm with a propagation distance less than 7 cm and increases to ≥ 100 μm for longer distance in order to avoid large crosstalk between adjacent interconnects [11]).
- Freedom from electro-magnetic interference (EMI). The propagation of light does not generate EMI to interfere with the surrounding circuit, nor can it be affected by the EMI produced

by the environment. As we will show in later chapters, optical crosstalk between adjacent optical interconnects is usually negligible.

- Breaking of ground-loops. By using optical interconnects, current is no longer transferred between the transmitters and receivers, and thus the disturbance on the ground plane is reduced. In addition, optical signals in an optical interconnect can not be disturbed by the noise of the ground plane and therefore the signal quality is improved.

1.2.2 Potential problems

On the other hand, we also have to be aware of the potential problems if optical interconnects are used to replace metal interconnects:

- Modal noise [14]. When multimode waveguides or fibers are used in conjunction with highly coherent lasers, the coherent interference of different spatial waveguide or fiber modes give rise to a speckle pattern. Fluctuations of the speckle pattern due, for example, to fluctuations in the spectrum of the optical source, can lead to modal noise if a mode-selective loss (such as a bad connector) is present in the optical link. Modal noise can cause a bit-error-rate (BER) floor which might not be tolerable in applications which require extremely low BER. Modal noise problem can be solved by either using a laser diode with large linewidth or premodulating the laser at a frequency comparable to the relaxation oscillation frequency of the laser diode [15].

- Optical reflections [16]. Index discontinuities are also unavoidable in waveguide or fiber interconnects. Reflections from the laser/waveguide interface might increase the linewidth as well as the relative intensity noise (RIN) of the laser. Other reflections due to the discontinuities along the optical path degrade the signals arriving at the receiver by reducing the eye opening and increasing the RIN.

- Optical crosstalk. Optical crosstalk can occur at the coupling between laser array and optical waveguide array, between adjacent waveguides, or between the waveguide array and the photodetector array as a result of the high packaging density required by the system. This problem will be examined in detail in Chapter 5.

- Threshold uncertainty [17]. The large number of interconnects within a digital system require all of the receivers to be set at the same threshold. In practice, this threshold cannot be individually adjusted according to the characteristics of the source. This means there is no feedback between the driver and the receiver to adjust the laser output, which deteriorates with time. Local feedback might be able to correct for this problem, but the added logic circuitry would compete for chip area with other logic circuitry. This problem will be investigated in Chapter 9.

- High density required for optoelectronic components. Each typical single-chip module (SCM) may have over 100 of signal-I/O's, while a multi-chip module (MCM) can have several hundreds to several thousands of signal-I/O's. In order to provide optical interconnect in this environment, we have to be able to fabricate equally dense optoelectronic devices such as LD/LED, PIN/APD arrays, driver arrays and receiver arrays. This problem will be addressed in Chapters 7, 8, 10 and 11.

- Propagation delay [17]. The propagation delay of light in waveguide is unlikely to reduce below the 5.0 ps/mm value currently available. This compares unfavorably with the 3.5-4.0 ps/mm for metal interconnects if suitable fabrication processes are developed to use expanded PTFE type material as an insulator in multi-chip modules and boards. This seems to be a fundamental limitation for waveguide optical interconnects. However, metal interconnects suffer additional delay at each discontinuity as well as require longer settling time due to switching noise, crosstalk, and reflections. Therefore, propagation delay alone can not be used to evaluate the performance of an interconnect technology. System implication of this problem is further exploited in Chapter 3.

- Conversion delay. Signals are useful only in their electrical forms. Therefore, electrical-to-optical (E/O) and optical-to-electrical (O/E) conversions are necessary for every interconnect, which always involve nonnegligible conversion delay. This problem will be examined further in Chapter 4 and 9 in which optical amplifiers are proposed to boost the optical signal power, thus reducing the number of gain stages as well as the O/E conversion time at the receiver.

- Sensitivity to noise during E/O and O/E conversion. Existing optical interconnect technology has more loss than metal interconnection for such distances, due to the insertion loss of the connector and scattering loss of the surface defects of a waveguide. Therefore, more amplification and a higher sensitivity to both power supply noise and electrical crosstalk are experienced by the receiver. This problem is further aggravated by the high density required by a dense optical interconnect environment. In such an environment, there could be significant electrical interference either through the shared common power supply or through the parasitic inductance and capacitance. This problem is analyzed in Chapters 7 and 8 and a solution is proposed in Chapter 9.
- Thermal interactions. Laser characteristics, such as the wavelength, threshold current and differential quantum efficiency, are strongly affected by the operating temperature. Thermal interactions between adjacent lasers in a dense laser array could thus significantly degrade the system performance. A solution to this problem is also proposed in Chapter 9.

Among all these potential problems, optical crosstalks, threshold uncertainty, electrical crosstalk and thermal interactions result from high interconnect density as required by the system and will be addressed in detail in this thesis.

1.3 Architecture of Dense Optical Interconnects

In this section, possible architectures for dense optical interconnects are investigated. The constraints for designing the architecture of an optical interconnect systems are:

- Compatibility with existing packaging technology,
- Flexibility in fitting into the architectures of digital systems,
- Fault tolerance,
- Easy engineering change and fault diagnostics.

In the following, we will first examine the available interconnect forms. Possible interconnect architectures at backplane, board, and multi-chip module level will then be investigated. Possible E/O and O/E conversion schemes will also be evaluated.

1.3.1 Interconnect media

Possible media that can be used for optical interconnects include:

- Free-space interconnect. Light travels fastest in free space. In addition, free space interconnects also offer the highest density and the most sophisticated interconnection patterns. Unfortunately, bulk optical elements such as lenses, holograms, beam splitters, etc., are usually unavoidable in free-space optical interconnects and thus make the alignment of optical beams very difficult and unstable with respect to environmental disturbances.
- Optical fiber. Optical fiber has the least loss compared with the other two media, and most of the technologies used in fabrication are already mature. Fiber ribbon cable also has the potential of providing reasonable interconnect density with regular interconnection pattern. However, fibers are incompatible with the existing packaging technology at the board or MCM level and they are not suitable for interconnects with very short distance or complicated patterns due to the possibly excessive volume occupied by the fiber cable.
- Planar optic waveguide. Passive planar optic waveguides are emerging as a viable alternative to optical fiber for very short distance interconnects. It has a higher propagation loss than optical fiber (0.01 $\sim$ 0.5 dB/cm as compared to 0.2 dB/km) but uses technologies that are compatible with existing PCB or MCM technology. Therefore, it is more suitable for short-distance dense interconnect applications. However, coupling of light into and from the waveguides is also difficult and careful alignment cannot be avoided.

1.3.2 Backplane optical interconnects

The function of a backplane is to provide a logical bus for all of boards connected to it. Free space, fibers and planar waveguides are all suitable for backplane interconnects. An optical backplane can be achieved through using of star couplers, as shown in Figure 1-2. Each board in the architecture occupies one input port and one output port from each of the star couplers so that signals input to any of the input port will be broadcast to all of the output ports. The total number of star couplers required can be greatly reduced by multiplexing several channels into a single waveguide with each channel using a different wavelength.

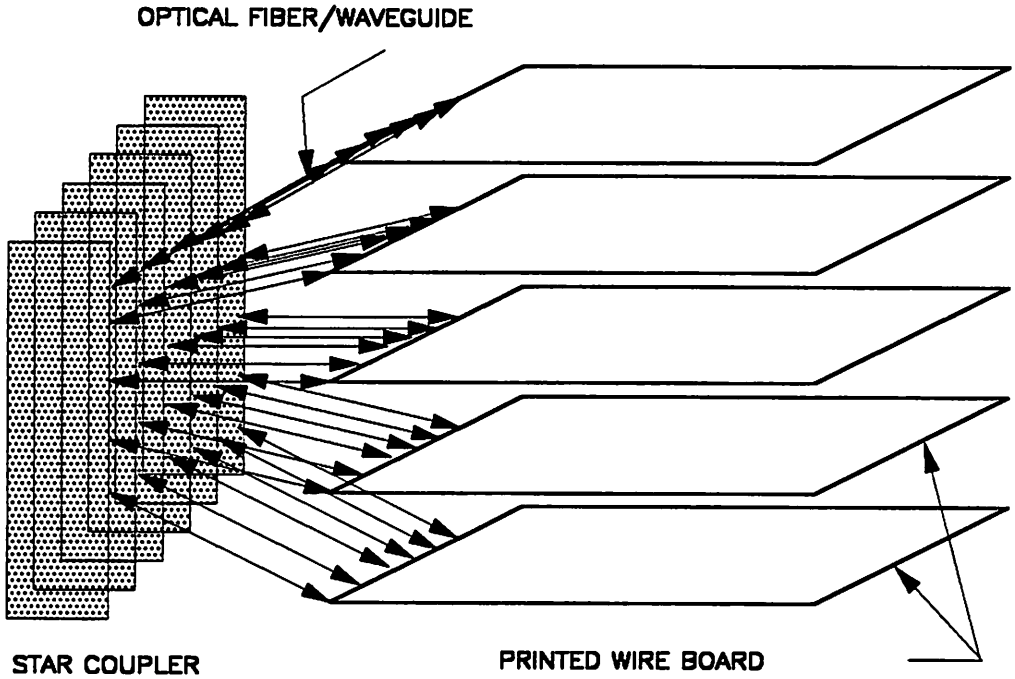

Figure 1-2. Optical backplane interconnects. Star couplers are used to combine and redistribute the data signals.

On the other hand, a topological bus can also be used to interconnect from one board to another, as shown in Figure 1-3. The bus is either folded back at the end or two independent buses are used because a unidirectional optical bus structure is usually easier to implement.

1.3.3 Board and multi-chip-module optical interconnects

Board-level optical interconnects have to provide interconnects between different SCM's or MCM's while MCM-level optical interconnects have to provide interconnects between unpackaged wire-bonded or solder-ball-bonded flipped chips. At the board level, the E/O and O/E conversion can be performed within an SCM/MCM, or through separate special-purpose E/O and O/E chips.

Similarly, the E/O and O/E conversion at the MCM level can be performed within the chip where the logical signals are generated or via separate special-purpose E/O and O/E chips on an MCM.

If the E/O and O/E conversion is performed before the package is connected to the next higher level, as shown in Figure 1-4, the electrical discontinuity can be minimized but the optical alignment is more difficult. On the other hand, more electrical discontinuity and thus more signal distortion is introduced if the E/O and O/E conversion is performed after the package is connected to the next level, as shown in Figure 1-5. However, this is acceptable for applications that require only moderate data rates.

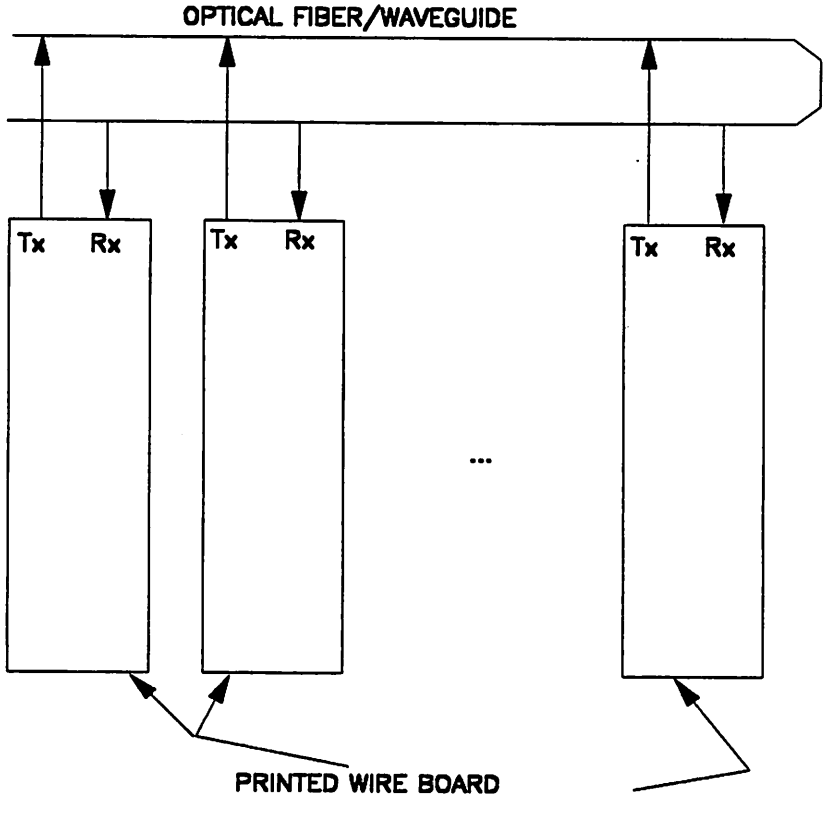

Figure 1-3. Optical backplane interconnects. A topological bus is used to provide communication path between any two boards connected to the backplane.

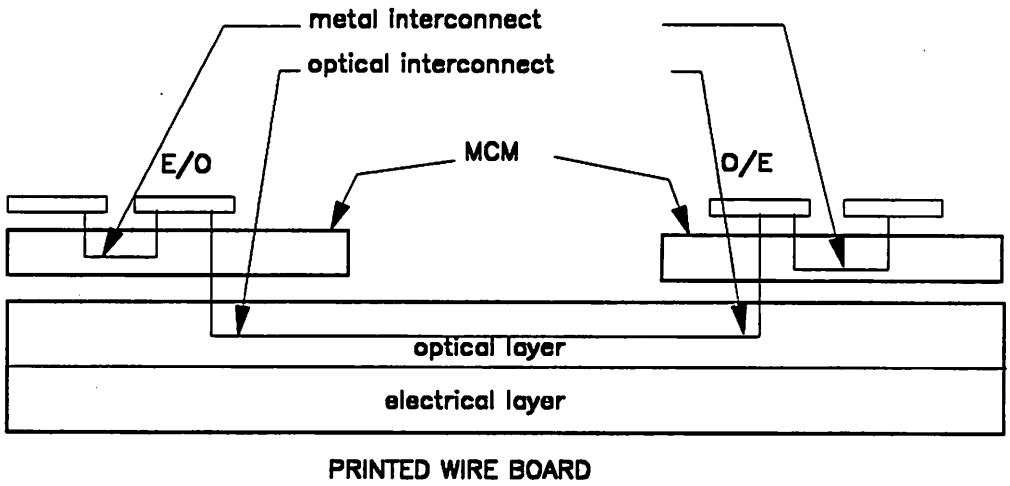

Figure 1-4. E/O and O/E conversion. Conversion is performed at the same packaging level as the electrical signal is generated.

In both cases, there already exist multiple layers of metal interconnect to provide signal lines as well as power and ground plane. Optical interconnects can be developed on top of these metal interconnect layers to allow optical signals to propagate from one chip/module to another chip/module. In some cases, more than one optical layer may be necessary in order to provide sufficient interconnect density (such as at the MCM level) just similar to its electrical counterpart.

1.4 Differential Optical Interconnection

As discussed in 1.2.2, "Potential problems" on page 7, optical interconnects for a digital system have the following potential problems:

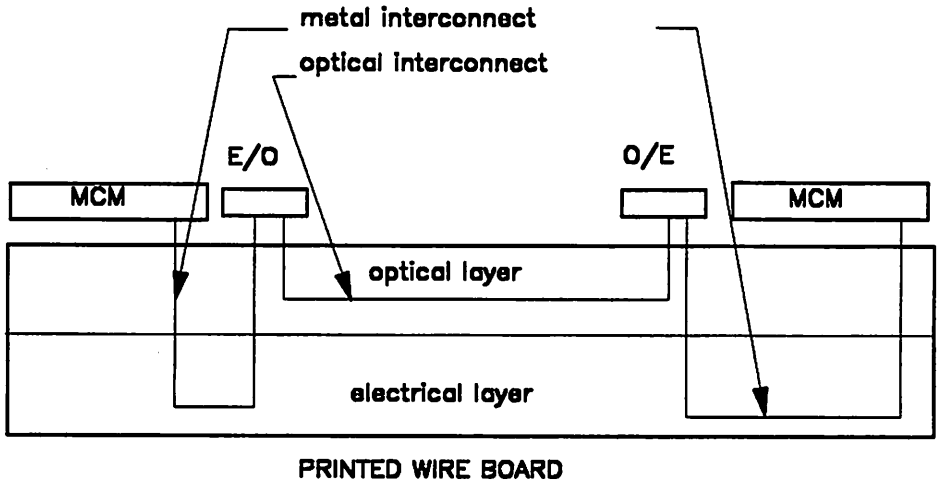

Figure 1-5. E/O and O/E conversion. Conversion is performed at the next higher packaging level.

- Threshold uncertainty,
- Latency due to serialization/deserialization, encoding/decoding,
- Sensitivity to the switching noise and power supply noise.
- Sensitivity to the thermal interactions.
- Sensitivity to the DC level of the data at the receiver.

A fully differential optical interconnect architecture, as shown in Figure 1-6, is proposed in this thesis to minimize the detrimental effects arising from these potential problems. In this architecture, complementary optical signals are generated, transmitted, and received along two independent optical channels.

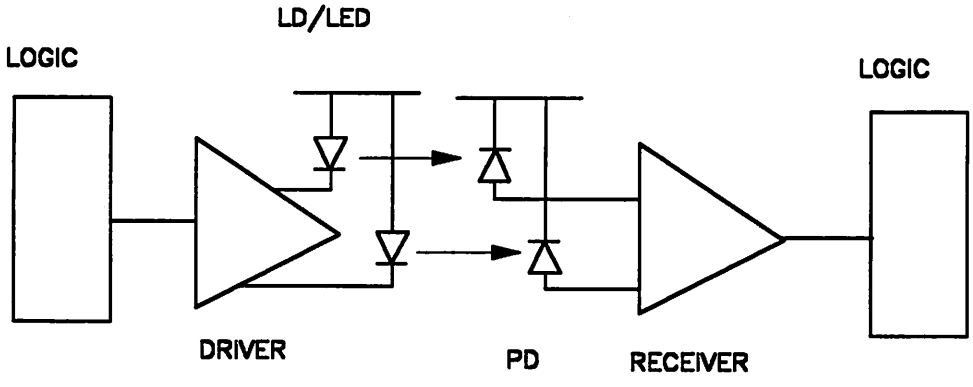

Figure 1-6. A fully differential optical interconnect architecture.

In a fully differential optical interconnect, the threshold voltage at the output of the receiver is always located at differential zero, which is halfway between two signal voltage of approximately equal amplitude but opposite sign, assuming two lasers at the differential transmitter have approximately the same average power and the attenuation along the differential path is similar. The threshold voltage is then independent of the actual power output of the lasers and the attenuation of the channel. Since the laser drivers and receivers are both fully balanced, the fluctuation of the current demands from the power supply is minimized, and thus the switching noise is reduced.[4]

[4] An offset voltage is incurred when the laser output power or the attenuation is not balanced along the differential path. We will show in Chapter 9 that a total of 40% mismatch between the lasers, the attenuation of the optical path, and the quantum efficiency of the photodetector cause a 2.2 dB power penalty.

Furthermore, the differential structure for both drivers and receivers increases the common-mode rejection and thus reduces the sensitivity to the power supply noise. Therefore, differential optical interconnect is very attractive in a dense optical environment and has been pursued in detail in this thesis (Chapters 9-11). Fully differential drivers, receivers, and receiver arrays have been designed, fabricated, and characterized to verify this concept.

1.5 Prior Art of Optical Interconnects

Using optics for interconnections between VLSI systems was first suggested in [18, 19]. Early systems are mostly based on free space interconnects with the use of holographic optical elements (HOE) and spatial light modulators (SLM) to establish interconnect patterns. More recent systems have begun to use both optical fibers and planar waveguides [20]. An interprocessor optical link has been demonstrated between processor blocks in the Thinking Machines CM-2 at 400 Mbps [21]. The feasibility of board-level optical interconnect using polymer [22, 23] and silica [24] have also been demonstrated recently. Both of these prototypes can demonstrate a bit rate higher than 300 Mbps. However, the problems associated with the high density interconnect are yet to be addressed.

1.6 Contribution of This Thesis

In this thesis, we demonstrate that high-density high-speed optical interconnects can be achieved in a synchronous digital system environment. The density of planar optical waveguides can approach 11μm pitch while the density of a wavelength-division-multiplexed (WDM) system can approach 37 GHz channel spacing for an OOK system with direct detection. We also show that a multi-stage tree-structured optical clock distribution system using optical amplifiers can achieve a very large fanout ($\geq 10^5$) for synchronous digital systems.

The electrical interference between adjacent channels and from the neighboring digital circuitry could be a serious threat to a dense optical interconnect system. A fully differential optical interconnect architecture is therefore proposed, analyzed and implemented in this thesis. We show that a very high density transmitter and receiver array ($\geq$16 channels/chip) can be achieved with minimal adjacent channel interference and switching noise ($\leq$0.2% for the receiver array).

1.7 Thesis Outline

The main theme of this thesis is to investigate potential problems and solutions arising from using dense optical interconnects in a digital system.

Since the metal interconnects cannot be avoided even in systems employing optical interconnects, we thus investigate in Chapter 2 the strength and the weakness of metal interconnects at various packaging level, and quantify when optical interconnects should be used.

The system requirements for dense optical interconnects are investigated in Chapter 3, in which a statistical timing skew model is proposed and used to analyze the timing requirements of various synchronous systems requiring parallel interconnections. We conclude that the rise time in the clocks and data signals must be as small as possible in order to maximize system performance. Therefore an optical clock distribution system using multi-stage optical amplifiers is proposed and evaluated both theoretically and experimentally in Chapter 4. The results show that a very large fanout from the clock distribution can be supported through this architecture with a proper adjustment of the system parameters.

Optical and electrical crosstalk in a dense optical interconnect system are evaluated in Chapters 5-8. In Chapter 5, the mode coupling within a parallel waveguide array is analyzed. A crosstalk model which includes the effect of nonzero linewidth of the light source is used to evaluate the crosstalk penalty. Instead of using multiple parallel waveguides, more than one channel can share the same waveguide with each channel occupying a different wavelength, resulting in a wavelength-division multiplexing (WDM) system. In Chapter 6, a dense WDM system is simulated to determine the maximum channel capacity, taking into account the chirp from the laser and imperfect optical filtering.

Chapter 7 describes the simulation results of the crosstalk and switching noise in an optical transmitter array consisting of a driver array and a laser diode array under various packaging assumptions. Simulation results of the crosstalk and switching noise in an optical receiver array consisting of photodetector array, preamp array, and postamp array are reported in Chapter 8. Both of the single-ended and differential-ended configurations for drivers and receivers are considered in Chapters 7 and 8.

A differential optical interconnect architecture that minimizes the electrical and thermal interference is proposed and analyzed in Chapter 9. A fully differential driver and receiver based on this concept are designed, simulated and fabricated. In Chapters 10 and 11, we report the design and simulation results of these fully differential driver and receiver array.

A summary of this thesis and suggestions for future work are given in Chapter 12.

CHAPTER 2 MODELING AND PERFORMANCE EVALUATION OF METAL INTERCONNECTS

2.1 Introduction

Metal interconnects have been used inside of most of the digital systems for either point-to-point or multi-drop interconnects. Even a system employing optical interconnects still cannot avoid using metal interconnects as part of its transmission paths. Therefore it is important to realize the strength and weakness of metal interconnects at various packaging levels so that optical interconnects can be used to supplement at those places where metal interconnects become the performance bottleneck.

A high speed digital system usually assumes a controlled-impedance environment, in which a constant characteristic impedance is maintained for its metal interconnects in order to minimize signal distortion and reflections. However, electrical discontinuity cannot be completely avoided even in such an environment. Several types of discontinuities usually arise in this environment:

- *Connector discontinuities.* Due to the lack of a reference (ground) plane, the characteristic impedance of connectors such as bonding wires is very difficult to control.
- *Via discontinuities.* In general, multichip modules, cards, and boards can have more than one signal plane. Vias are used for signals to pass from one signal plane to another. However, the characteristic impedance of these vias is also difficult to control due to the lack of a reference plane.
- *Signal-line bends and T-junctions.* For routing purposes, some of the signal paths on a signal plane have to be bent by 45 degrees or 90 degrees. In other cases, signal line splitting is necessary in order to provide fan-out. Both of these cases create electrical discontinuities.
- *Other line and vias (OLV) discontinuities.* Ideally, a continuous ground or power plane can provide the best shielding and isolation between signal planes. However, due to the vias which are necessary for signals to pass from one signal plane to another, the ground and power plane are usually configured as a mesh plane instead of a continuous plane. Adjacent transmission

lines and vias surrounding a signal transmission line may increase its line capacitance and inductance and modify its local characteristic impedance.

These effects, together with the dispersion, skin effect, crosstalk, and switching noise, introduce intersymbol interference as well as signal distortion and limit the bandwidth of metal interconnects.

Transmission lines for interconnects in a high-speed LSI/VLSI system have been analyzed in [25-32]. Signal dispersion and distortion in microstrip lines at the multi-chip module (MCM) and printed circuit board (PCB) levels have been analyzed and simulated, for example, in [13, 33]. A linear source and a resistive load are usually used for analysis as well as simulations while the discontinuities of a transmission path are mostly ignored. On the other hand, various types of electrical discontinuities that can be found in a transmission line have been analyzed in [34] while their implications on waveform distortion is reported in [35, 36]. Signal distortion at a system level that includes driver and receiver circuits, transmission lines, and packaging discontinuities is simulated and evaluated in [37]. However, only the discontinuity due to bonding wire at a chip boundary is considered.

In this chapter, we investigate the signal distortion due to skin effect, DC loss, and electrical discontinuities at various package boundaries.[5] Using a strategy similar to [37], we simulate eye patterns of the following systems

- From one chip to another chip located on the same multi-chip module (MCM),
- From one chip to another chip located on a different MCM, and
- From one chip to another chip located on a different board.

with various interconnect lengths and signal rise time.

From these simulations, we have found that

- For a short distance MCM interconnect ($\leq$ 3 cm for signal rise time $\geq$ 200 ps), signal propagation is insensitive to the electrical discontinuities. The bandwidth can exceed several GHz.

[5] The parameters and models for the multi-chip module used in this chapter are characterized by W. P. Smetana of IBM General Technology Division, East Fishkill, New York. The parameters of the thin-film microstrip lines are characterized by A. Deutsch of IBM T. J. Watson Research Center.

- Rise-time degradation becomes significant for longer MCM interconnect ($\geq$ 5 cm for signal rise time $\leq$ 200 ps) due to the lossy nature of thin-film transmission lines.
- Significant ringing ($\geq$ 25 %) and reflections ($\geq$ 20 %) can be observed at the board and backplane interconnect level and can limit the maximum transmission bandwidth to less than 500 MHz.

From these results, we show that it would be very difficult for optical interconnects to compete with electrical interconnects at the on-chip and short-distance multi-chip module interconnects even in the gigabit regime. It becomes more attractive to employ optical interconnects at the long-distance multi-chip module level, board level, and backplane level interconnects for a bit rate higher than 500 Mbps.

The organization of this chapter is as follows: Section 2 evaluates the signal distortion of MCM-level interconnects, while Section 3 evaluates the signal degradation of board-level interconnects. Backplane level interconnects are evaluated in Section 4. This chapter is summarized in Section 5.

2.2 Multi-Chip Module Level Metal Interconnects

2.2.1 Modeling

In a multi-chip module (MCM) environment, chips are either wire-bonded or flipped and soldered onto the multilayer substrate of an MCM. The substrate can be made of Al_2O_3 (NEC), glass ceramic (Hitachi, IBM), silicon (AT&T), polyimide, alumina or sapphire [11]. In such an environment, signals from an on-chip driver have to pass through bonding pads, bonding wires (or solder balls if the chip is flip-chip-bonded), vias (between the surface of the substrate and the signal layer), microstrip lines (on the MCM), vias (between the signal layer and the surface of the substrate), bonding wires (or solder ball), bonding pads before the signals can reach the receiver of another chip. This structure is shown in Figure 2-1. An equivalent circuit for a chip-MCM-chip interconnect is shown in Figure 2-2.

The microstrip line on a multi-chip module has been modeled by a lossy transmission line with skin effect. We assume the characteristic impedance is 50Ω, signal propagation delay is 6.45 ps/mm, and DC resistance is $0.45\Omega/mm$. The bonding pad is modeled by a capacitor (100 fF) while the

solder ball is modeled by the equivalent circuit shown in Figure 2-3 [36], with $C = 604fF$, $R = 0.1376\Omega$, $L = 4.065nH$. For flip-chip solder balls approximated by cylinders in parallel and placed orthogonally between ground planes, simple formulas for L, C and R used in Figure 2-3 can be developed [36, 38]. We can also use the same equivalent circuit shown in Figure 2-3 to model the vias between solder balls and the signal layers. The parameters used in the simulations for the vias are $R = 0.01\Omega$, $L = 0.468nH$, and $C = 139.5fF$.

This equivalent circuit for modeling the discontinuity is accurate as long as the propagation delay through the discontinuities is much smaller than the rise-time of the signal. As the rise time approaches the propagation delay through the discontinuities, more than two sections of the same

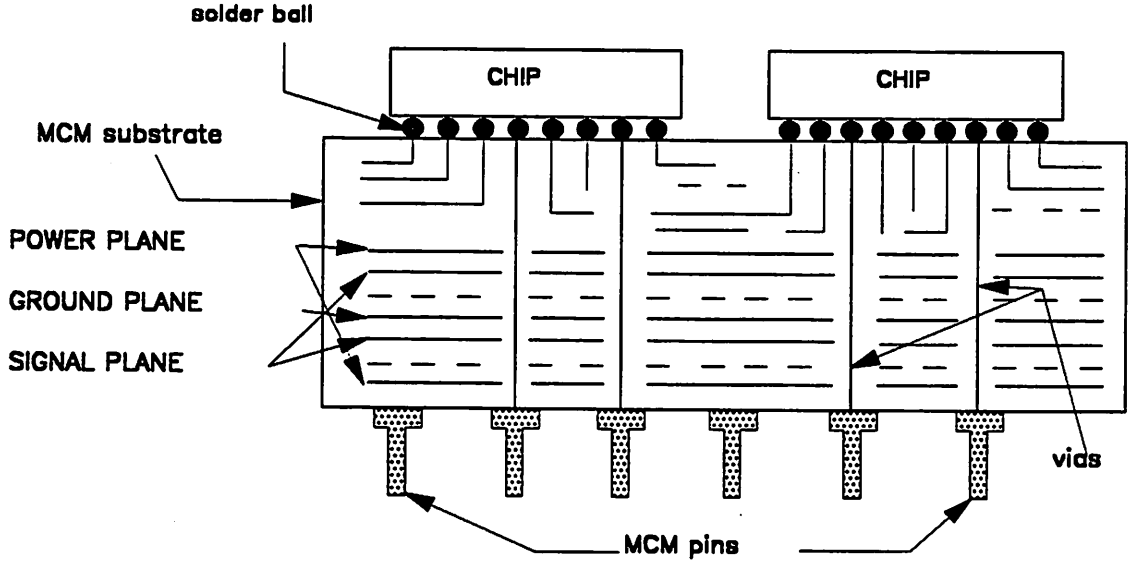

Figure 2-1. Structure of an electrical path for an MCM interconnect.

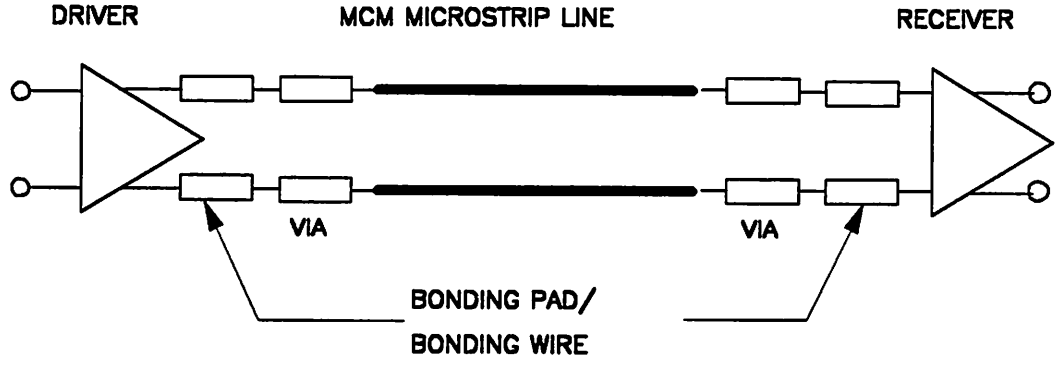

Figure 2-2. Circuit model of a typical multi-chip module interconnect. Signals from the differential driver have to go through bonding pad, bonding wire, vias from the surface to a signal layer, MCM microstrip lines, vias from the signal layer back to the surface, bonding wire, bonding pad, and to the differential receiver.

equivalent circuit can be cascaded together so that the propagation delay of each individual section is still much smaller than the signal rise time.

Fully differential metal interconnects are assumed throughout the simulations, so that ground-loop noise can be ignored. The driver and the receiver in Figure 2-2 consist of the same circuit, as shown in Figure 2-4 (which is a modification from the schematics shown in [37]). The receiver has an on-chip 50Ω termination resistor for each input. This design has been shown to have better performance than the one with off-chip termination in [37]. A single-stage voltage follower serves as a buffer for the input signals, while the output is an open-collector current-switch

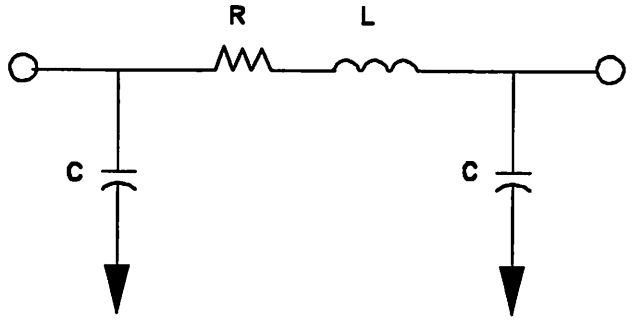

Figure 2-3. Equivalent circuit for a electrical discontinuity. This equivalent circuit is very general and can be applied to almost all sorts of discontinuities.

configuration so that the collectors at the output of the driver sink current from the receiver through the transmission line. The bipolar transistors used in these simulations have an f_T exceeding 20 GHz. Biasing of the circuit has been optimized to achieve the maximum f_T.

A 40-bit pseudo random sequence at 200 Mbps is used for the input to the driver while the complement of this sequence is applied to the complementary input of the driver. The outputs are sampled at the input point to the receiver before the waveform is reshaped. The simulated differential output voltage, which is the voltage difference between the signal channel and its complementary channel, are overlayed over a single bit period to generate the eye pattern.

An eye pattern is considered acceptable only if the eye is at least 50% opened, because most of the digital logic has been designed to tolerate at least 25% noise margin for either logical ONE or ZERO.

2.2.2 Simulation Results

Figure 2-5 shows the simulated eye pattern for a differential MCM interconnect with length 1 cm and input signal rise time 200 ps. A ringing with maximum amplitude of 10.75% can be observed (as compared to a full voltage swing). This ringing is mostly due to the resonance between the capacitance of the bonding pad and the inductance of the solder ball. Note the transitions that

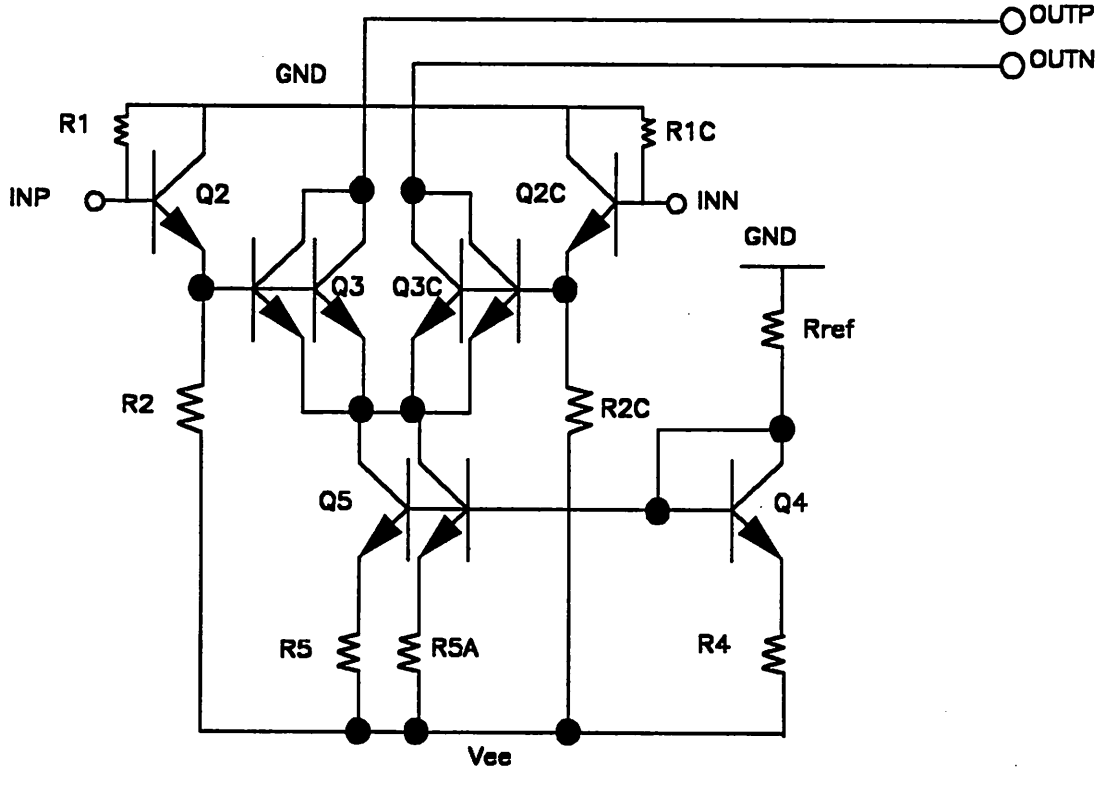

Figure 2-4. ECL driver and receiver circuit used for simulations. $R_1 = R_{1C} = R_4 = R_5 = R_{5A} = 50\Omega$, $R_2 = R_{2C} = 420\Omega$, $R_{ref} = 370\Omega$.

start at 0.3ns. The rise and fall time of the waveform is degraded to 340 ps and no jitter is observable.

Figure 2-6 shows the simulated eye pattern from the same system but the interconnect length has been increased to 5 cm. The ringing of the waveform completely disappears at this distance. On the other hand, the rise time is degraded to 1.75 ns while a jitter of ~150 ps can be observed.

The simulated eye pattern of an MCM interconnect with an interconnect length of 8 cm is shown in Figure 2-7. The waveform jitter remains essentially the same as compared to Figure 2-6 while the rise time is further degraded to 2.75 ns. Severe signal distortion can also be observed.

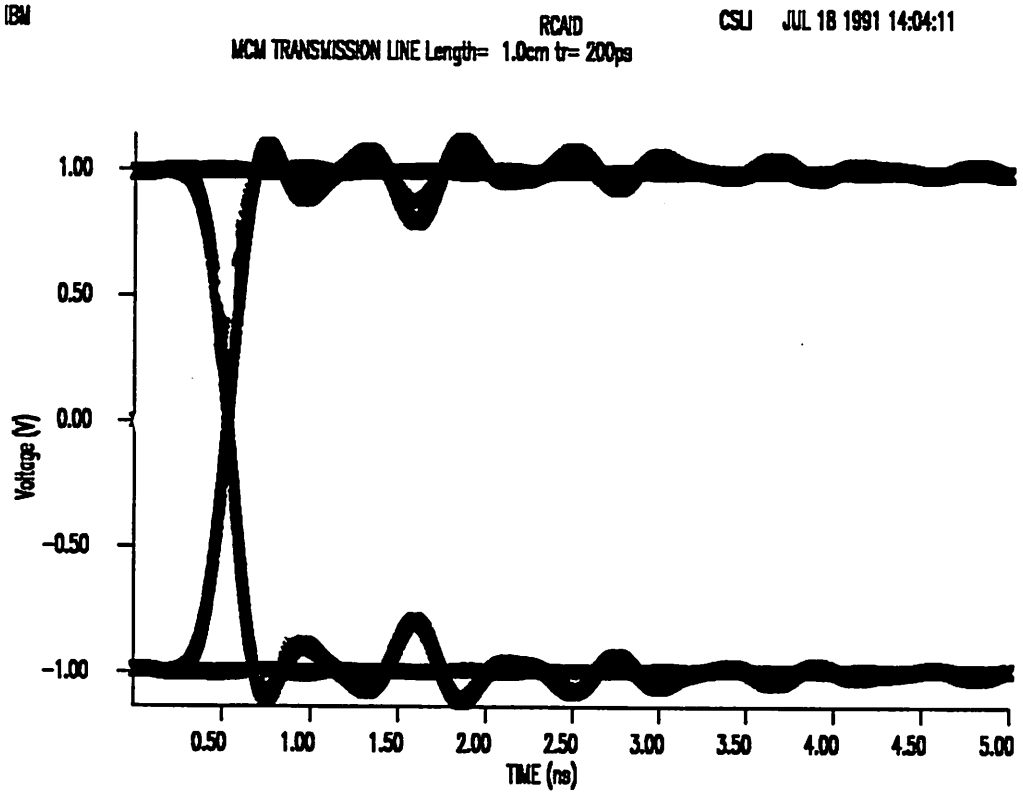

Figure 2-5. Simulated eye pattern of an MCM interconnect. Signal rise time = 200 ps, interconnect length = 1 cm.

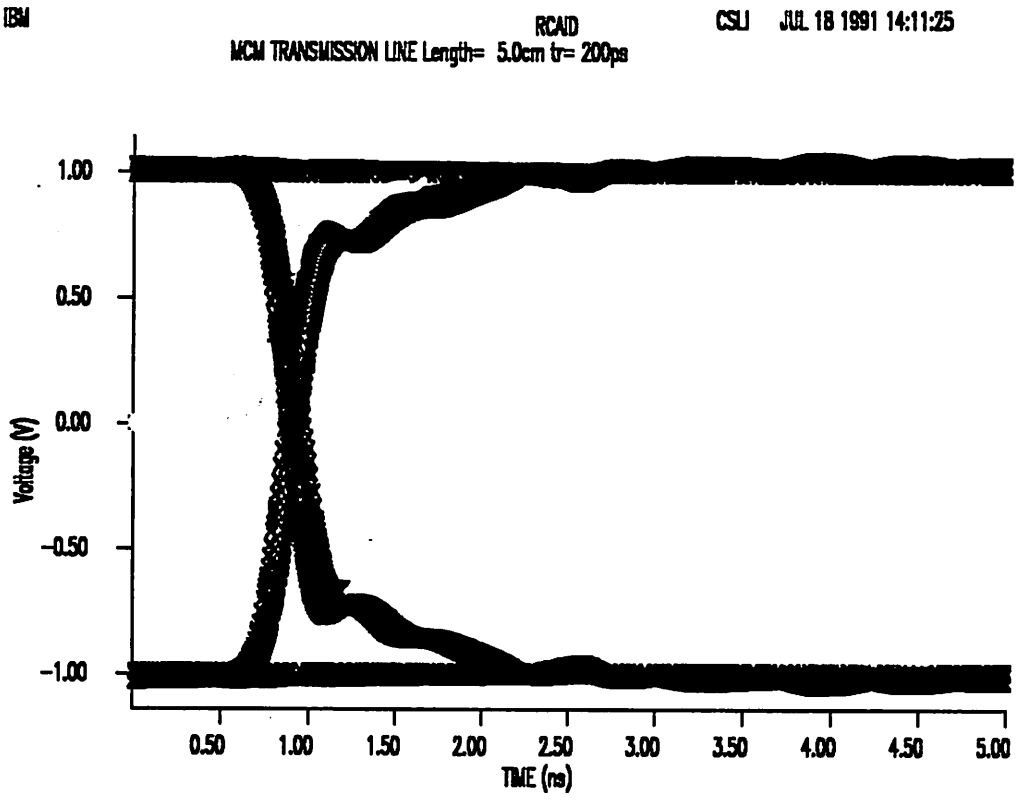

Figure 2-6. Simulated eye pattern of an MCM interconnect. Signal rise time = 200 ps, interconnect length = 5 cm.

Due to the highly lossy nature of the thin-film microstrip lines assumed for the MCM interconnects, waveform degradation (the increase in rise time) is significant for long MCM interconnects while reflections due to discontinuities are negligible. We can also extrapolate the maximum operating frequency from the eye pattern shown in these figures. Without changing the signal rise time and fall time, the increase in operating frequency merely close the eye in the horizontal direction. And thus the maximum operating frequency is obtained when the eye is no longer 50% opened. For short interconnects ($\leq$ 3 cm), the maximum operating frequency can easily reach several GHz. The maximum achievable frequency reduces to $\leq$ 500 MHz for longer interconnects ($\geq$ 5 cm).

2.3 Board Level Metal Interconnects

2.3.1 *Modeling*

The structure of a board level interconnect is shown in Figure 2-8. In a chip-MCM-board-MCM-chip environment, the signals have to travel through the MCM pin, on-board microstrip lines, and another MCM pin, in addition to all of the signal paths discussed in the previous section, before the signals can reach the other MCM. The equivalent circuit of such an interconnect is shown in Figure 2-9. Note that it is a common practice that the signal is brought down immediately to the MCM pins from the chip output to avoid additional loss due to the MCM microstrip lines. Therefore, MCM transmission line models are not included in the equiv-

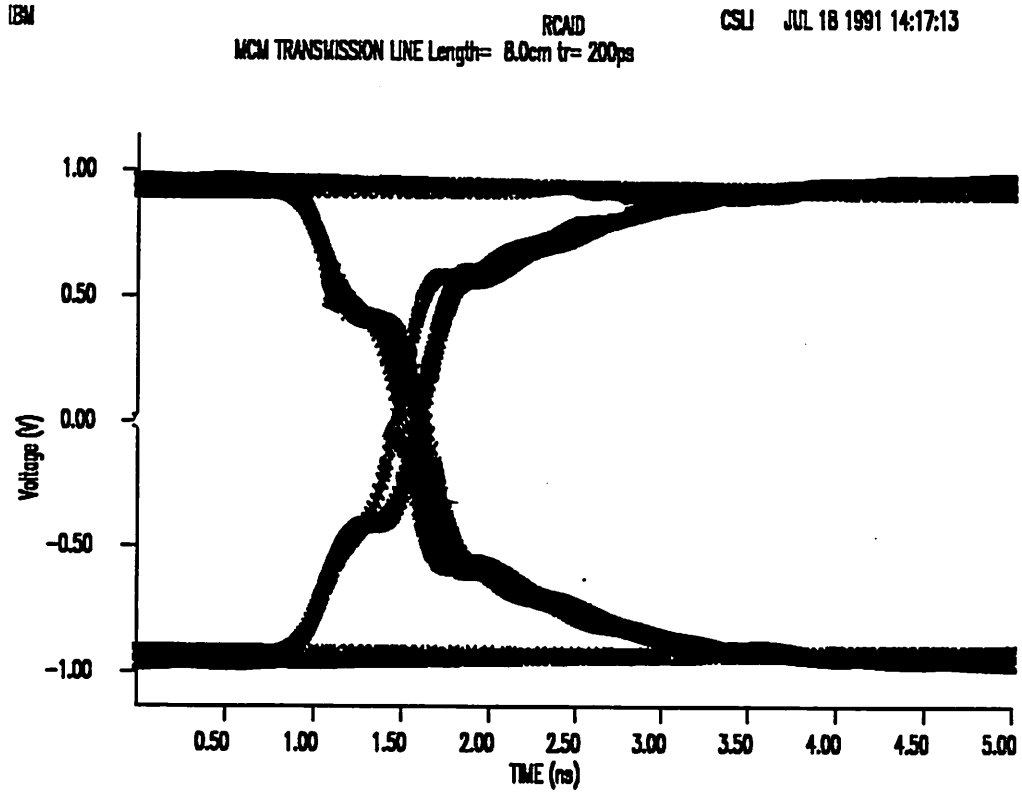

Figure 2-7. Simulated eye pattern of an MCM interconnect. Signal rise time = 200 ps, interconnect length = 8 cm.

alent circuit shown in Figure 2-9. But the length of the via that the signal has to travel before it can reach the MCM pin is twice as long as the average length that has to be traveled in an chip-MCM-chip environment. Therefore, two identical via models have been cascaded to reflect this increased propagation length. The model used for an MCM pin is identical to that shown in Figure 2-3 with $R = 0.021\Omega$, $L = 4.07nH$, and $C = 1.68pF$.

The board microstrip line is modeled by a lossy transmission line with skin effect included. The characteristic impedance is assumed to be 50Ω. The propagation delay is 6.88 ps/mm, while the DC resistance is 0.0057 Ω/mm. Note that the DC resistance of a board transmission line is much smaller than that of an MCM transmission line because the density requirement for board

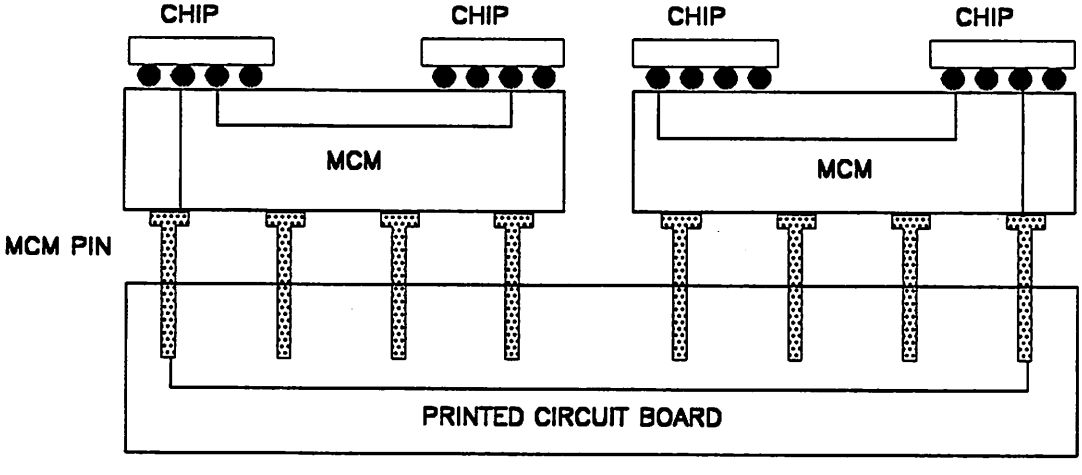

Figure 2-8. Structure of a board level interconnect.

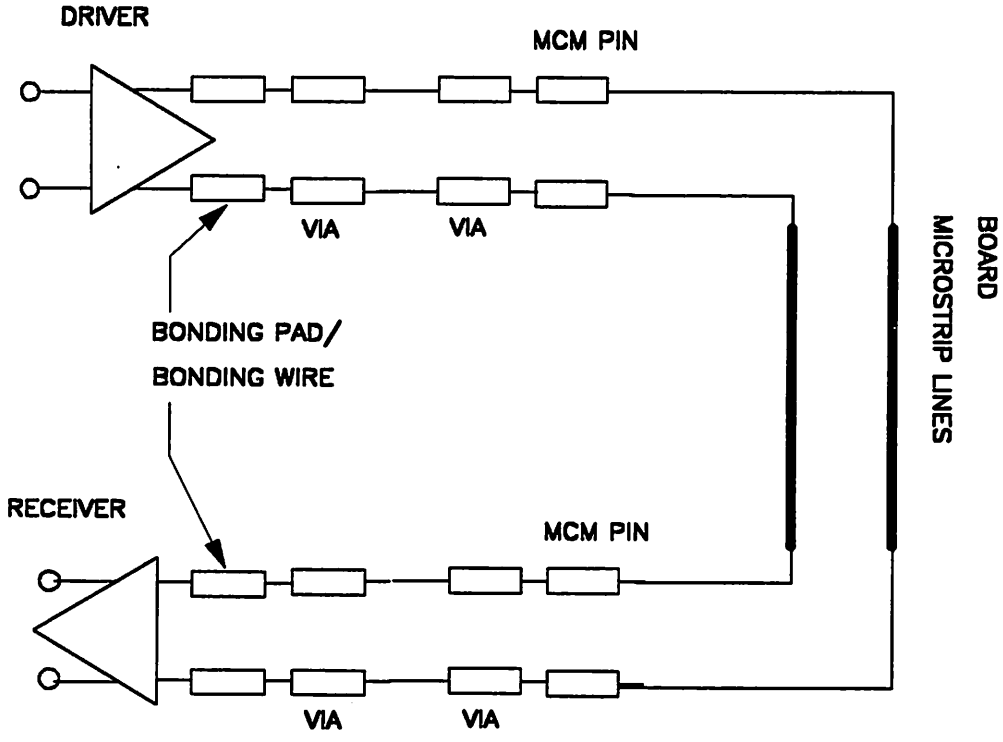

Figure 2-9. Equivalent circuit of a board level metal interconnect. The signals have to travel through MCM pins of an MCM, board microstrip lines, and MCM pins of the other MCM in addition to all of the paths discussed in Figure 2-2.

transmission lines is less stringent and therefore allows the board transmission line to be wider and thicker than an MCM transmission line. The rest of the circuits and parameters shown in Figure 2-9 are identical to those used in Figure 2-2.

2.3.2 Simulation Results

Using the same simulation methodology described in the previous section, we obtain the simulated eye pattern of a board level interconnect with length 20 cm and input signal rise time 200 ps, as shown in Figure 2-10. The rise time has been degraded to 615 ps while the relative maximum ringing is 21.39%. The increased maximum ringing in this case as compared to an MCM

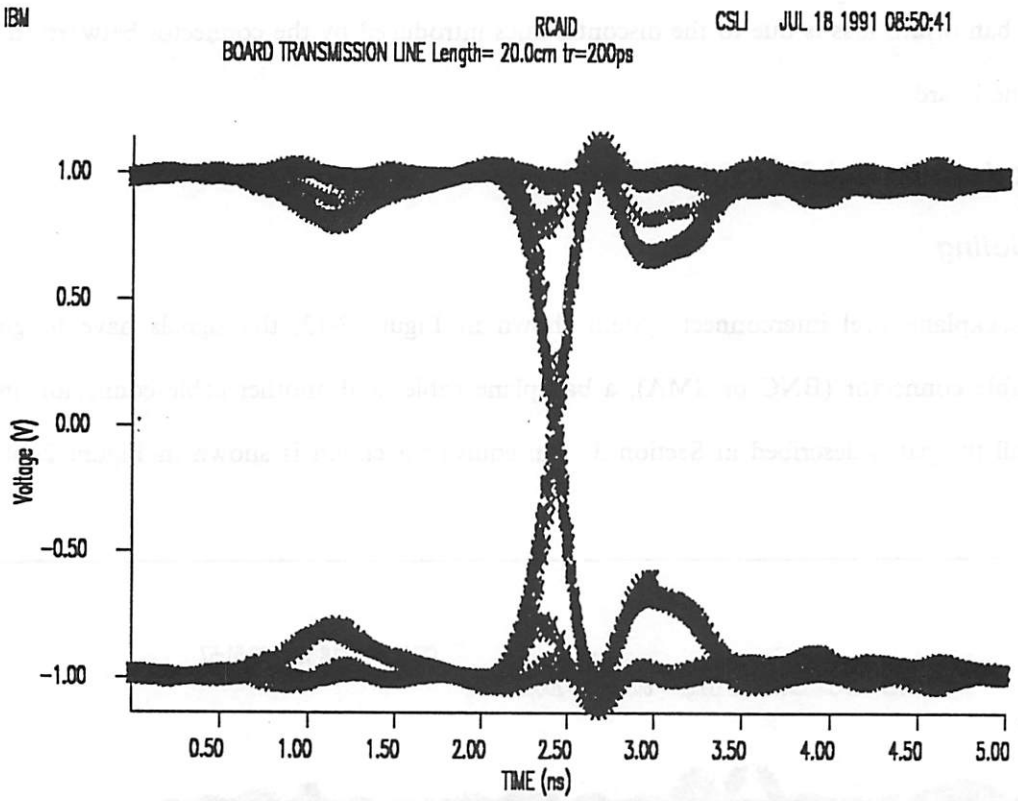

Figure 2-10. Simulated eye pattern of a board level interconnect. Interconnect length is 20 cm and signal rise time is 200 ps.

interconnect can be attributed to the increased discontinuities between the chip output and the board transmission line. Reflections can no longer be ignored at this propagation distance where a maximum reflection of 12.83% (as compared to the full voltage swing) has occurred.

Figure 2-11 and Figure 2-12 show the simulated eye patterns for board level interconnect with an interconnect length of 60 cm and 120 cm, respectively. As the length of an interconnect increases, waveform degradation due to multiple reflections becomes more serious. Maximum degradation (30%) occurs when the reflections coincide with the ringing, as shown in Figure 2-12. On the other hand, the rise time degradation remains essentially the same (615 ps).

For the board level interconnect system simulated in this section, we can extrapolate that the maximum operating frequency is $\leq$ 500 MHz for a maximum interconnect length up to 60 cm. Most of the bandwidth loss is due to the discontinuities introduced by the connector between the MCM and the board.

2.4 Backplane Level Metal Interconnects

2.4.1 Modeling

For a backplane-level interconnect system shown in Figure 2-13, the signals have to go through a cable connector (BNC or SMA), a backplane cable, and another cable connector, in addition to all the paths described in Section 3. An equivalent circuit is shown in Figure 2-14.

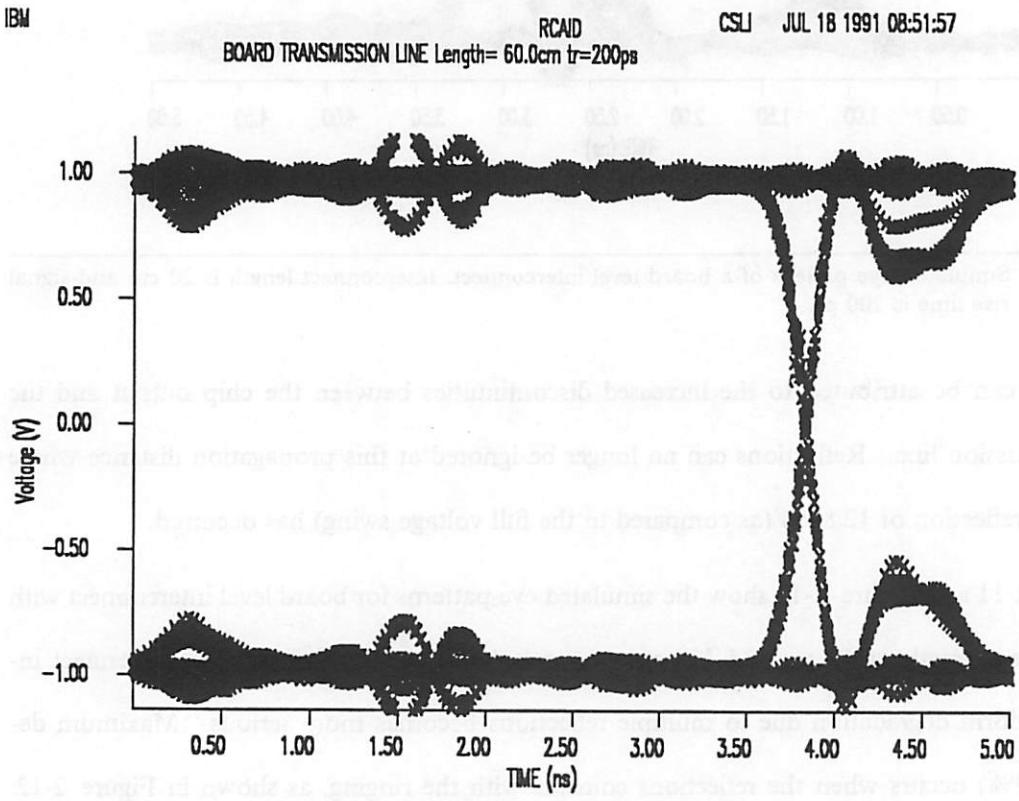

Figure 2-11. Simulated eye pattern of a board level interconnect. Interconnect length is 60 cm and signal rise time is 200 ps.

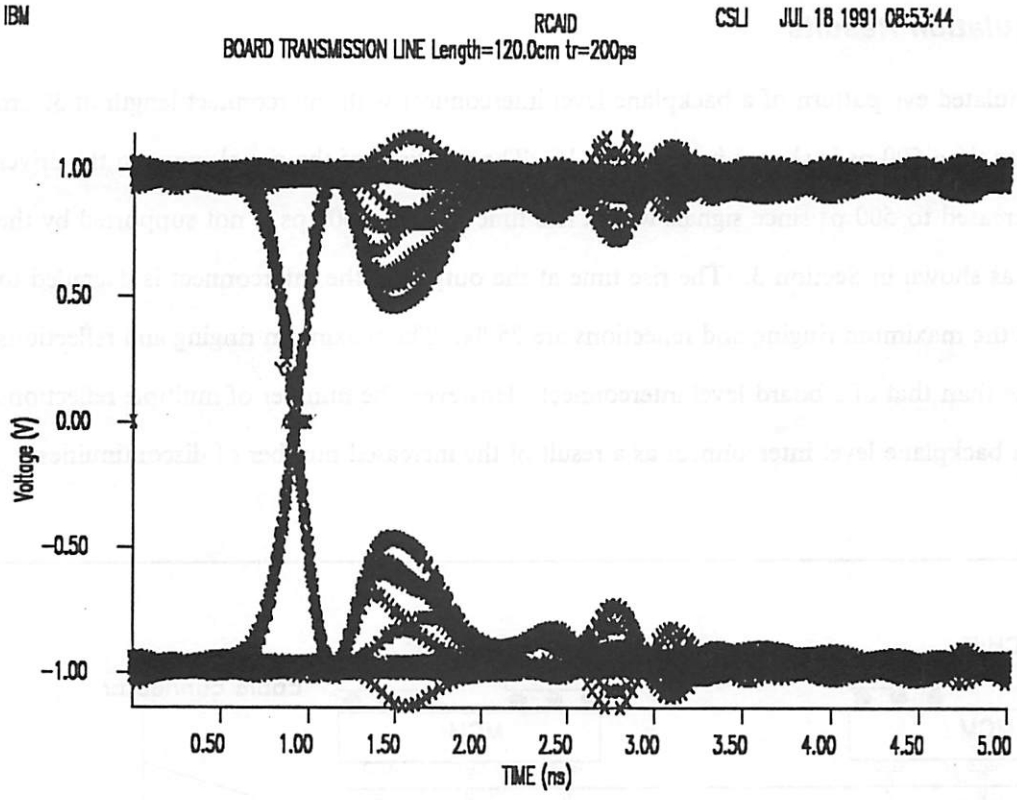

Figure 2-12. Simulated eye pattern of a board level interconnect. Interconnect length is 120 cm and signal rise time is 200 ps.

The cable connector is modeled by a series of lumped-LC circuits, whose equivalent circuit is shown in Figure 2-15.

Unlike the situation in a board level interconnect system, it is not always possible to place a cable connector close to the MCM pin, and therefore the signal has to travel through some board level interconnect before it can reach the backplane connector. A 10-cm board level interconnect is assumed between the MCM pin and the board connector in our simulations.

The coaxial cable for backplane interconnection is modeled by a lossy transmission line with skin effect included. The characteristic impedance of the cable is assumed to be 50Ω. The propagation delay is assumed to be 3.81 ps/mm, while the DC resistance is assumed to be 0.000676

Ω/mm. Note that the propagation speed of the signals in a cable is significantly faster than that in a board level or an MCM level interconnect.

2.4.2 Simulation Results

The simulated eye pattern of a backplane level interconnect with interconnect length of 30 *cm* and signal rise time 500 ps is shown in Figure 2-16. The rise time of the signal input to the driver has been increased to 500 ps since signals with a rise time less than 500 ps is not supported by the MCM pins, as shown in Section 3. The rise time at the output of the interconnect is degraded to 625 ps while the maximum ringing and reflections are 25 %. The maximum ringing and reflections are not worse than that of a board-level interconnect. However, the number of multiple reflections is more for a backplane level interconnect as a result of the increased number of discontinuities.

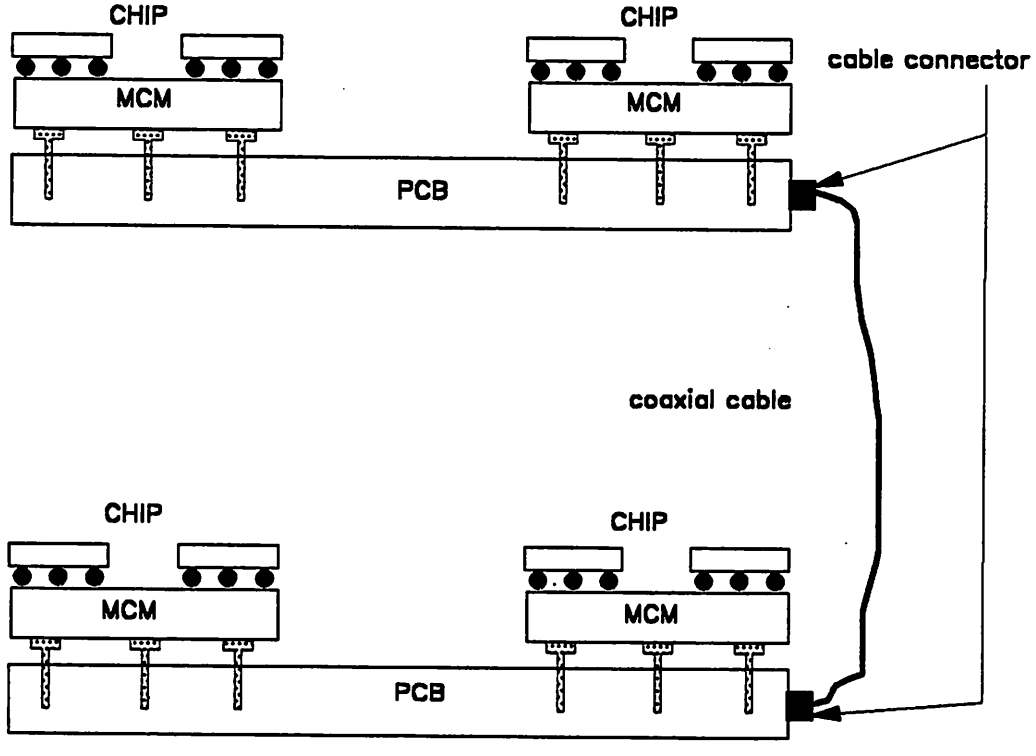

Figure 2-13. Structure of a backplane interconnect.

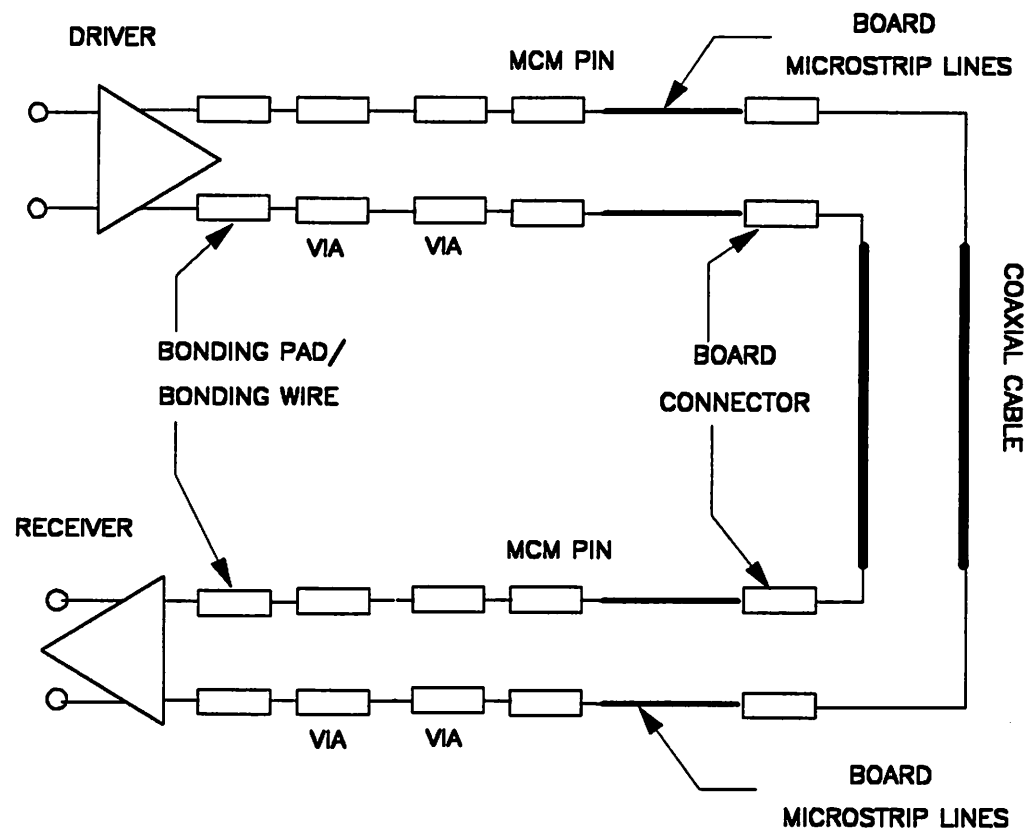

Figure 2-14. Equivalent circuit of a backplane level interconnect. The signals have to go through a cable connector, a coaxial cable, and another cable connector in addition to the circuit shown in Figure 2-9.

As the length of the backplane cable increases, the rise time of the signal begins to degrade significantly, as shown in Figure 2-17 (750 ps) and Figure 2-18 (2.5 ns). The waveform is severely distorted in Figure 2-18.

Assuming the eye has to be at least 50% opened, we can extrapolate from these figures that a backplane system as simulated in this chapter is limited to 500 MHz for a maximum backplane interconnect length $\leq$ 200 cm.

2.5 Summary

In this chapter, we evaluated the simulated eye patterns for metal interconnects at

- multi-chip module level,
- board level, and
- backplane level.

Using the parameters assumed in this paper, we can summarize the following observations:

- The bandwidth is practically unlimited for a short distance interconnect ($\leq$3 cm) at the multi-chip module level.

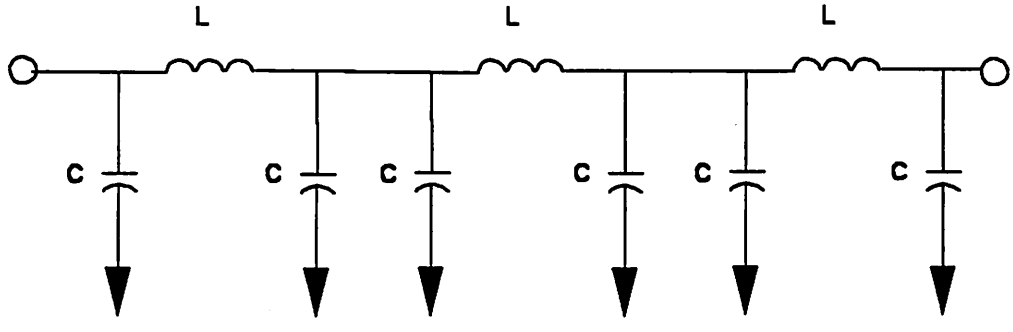

Figure 2-15. Equivalent circuit of a cable connector.

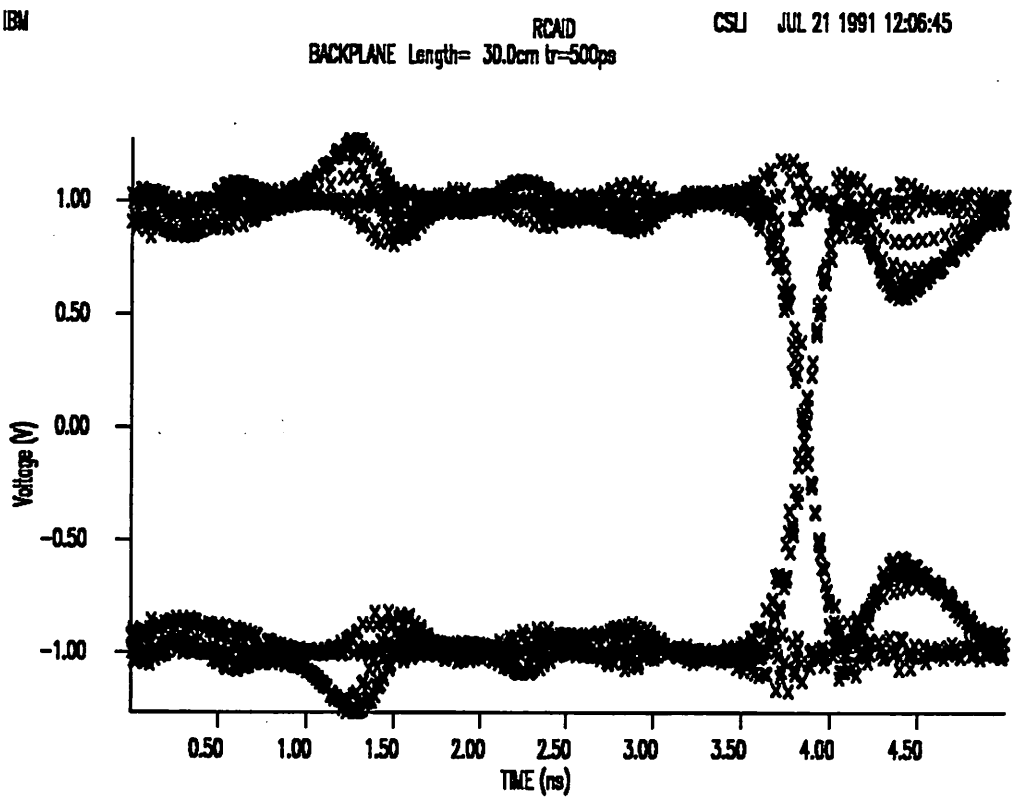

Figure 2-16. Simulated eye pattern of a backplane interconnect. Interconnect length is 30 cm, rise time is 500 ps.

- A longer (≥5 cm) interconnect at the multi-chip module using thin-film packaging technique can suffer substantial rise time degradation and the bandwidth is limited to less than 1 GHz.
- Significant waveform distortion (≥25 %) and multiple reflections can be observed at the board level or backplane level interconnects. The bandwidth is therefore limited to less than 500 MHz.

This performance is the upper bound that can be achieved by metal interconnects since we only considered the single interconnect case and excluded many other potential performance impairments that can arise in a dense interconnect environment such as the switching noise and the crosstalk.

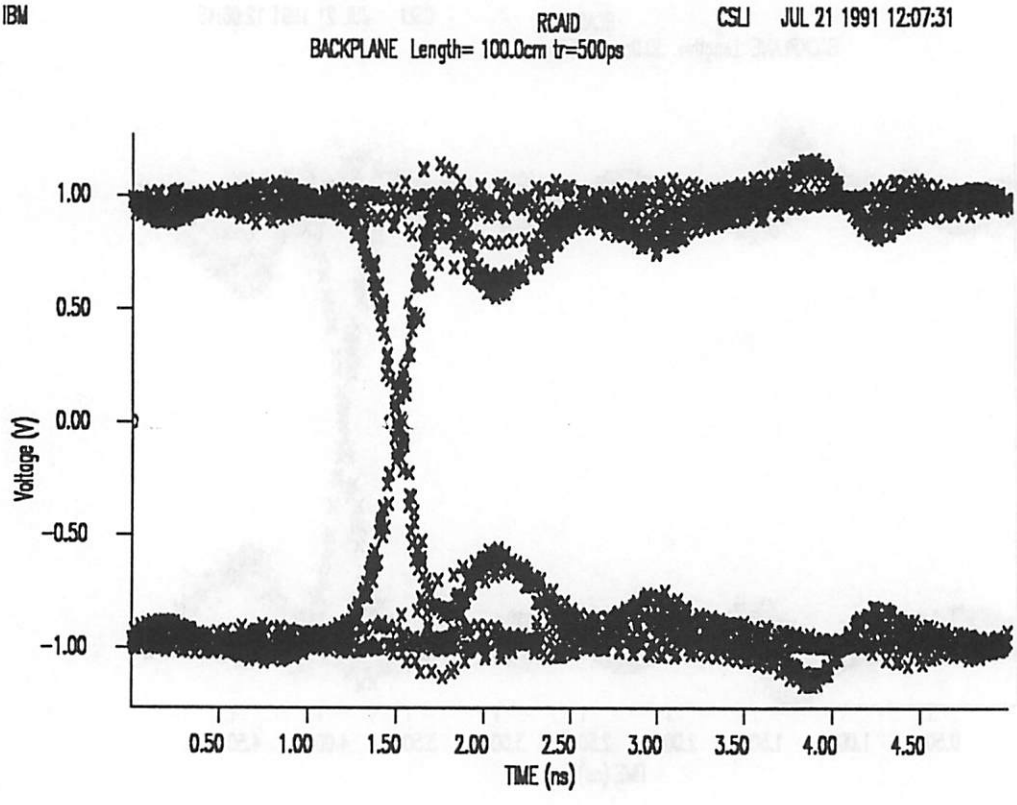

Figure 2-17. Simulated eye pattern of a backplane interconnect. Interconnect length is 100 cm, rise time is 500 ps.

It is clear from these observations that existing metal interconnects can perform very well for the short distance MCM interconnect. However, they are not able to support a gigahertz data rate at the board and backplane level due to the electrical discontinuities present in the signal transmission path. Therefore, optical interconnects technology applied at the board and the backplane level have the potential to substantially increase the system throughput. Furthermore, optical interconnect techniques can also be applied at the MCM level for interconnect at a longer distance to eliminate the possible rise time degradations. Optical interconnect at the board and backplane levels will therefore be the subjects in subsequent chapters.

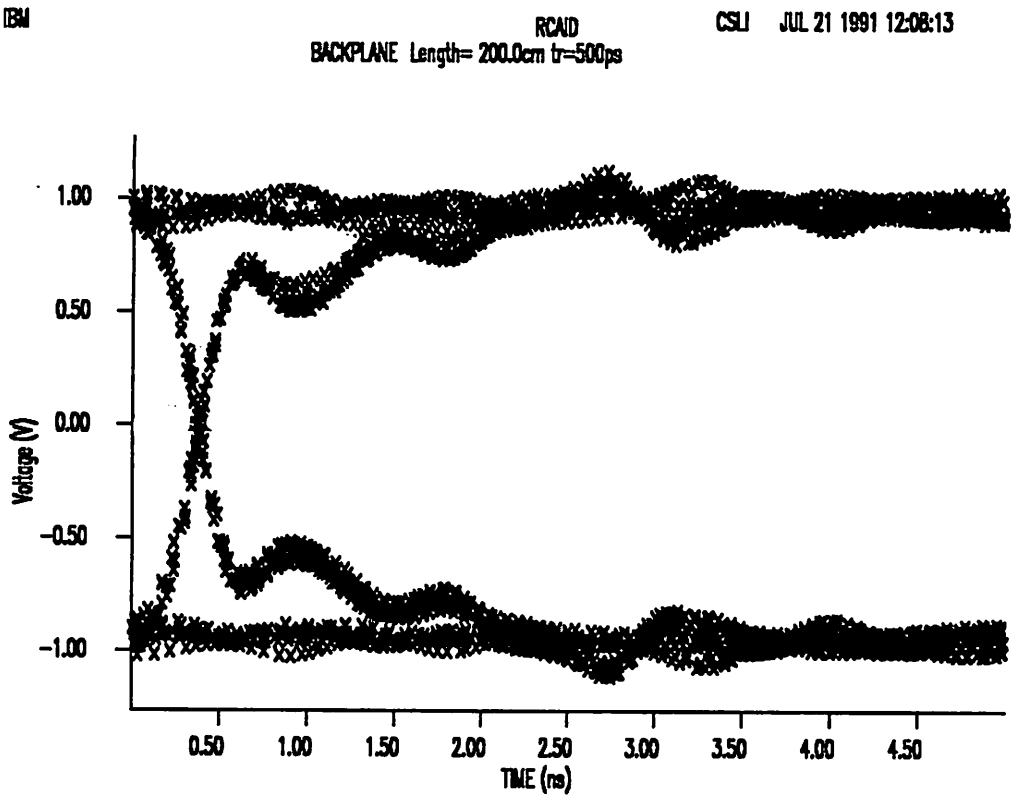

Figure 2-18. Simulated eye pattern of a backplane interconnect. Interconnect length is 200 cm, rise time is 500 ps.

CHAPTER 3 STATISTICAL ANALYSIS OF TIMING RULES FOR SYNCHRONOUS INTERCONNECTS

3.1 Introduction

Synchronous interconnects are commonly used at the backplane and board level in a digital system. Parallel data channels are sampled by a clock signal transmitted on a separate channel. The maximum system throughput of synchronous interconnects is usually limited by the timing skew among the parallel channels. Timing skew can be categorized into static skew and random skew. Static skew is usually caused by device variations while random skew is usually caused by circuit noise. Deterministic timing skew models for synchronous circuits have previously been studied in [39-41], but only the worst-case timing skews are accounted for by these models. On the other hand, statistical skew models for the clock distribution subsystem have been investigated in [42-44], but the connections between these models and the system performance are yet to be established.

In this chapter, timing rules which take statistical variations of timing skew into consideration are proposed and their impact on high-speed synchronous system design are evaluated. In particular, this model has the capability of predicting the *yield*[6] of a system if the statistics of the system parameters are given. For a given device technology in which the parameters of device fabrication is known, the yield of the subsystem can be calculated from the model proposed in this chapter.

Using this model, we derive the relationship between the maximum system throughput and the timing skew (both static and random) for the following synchronous system configurations:

- Synchronous bus
- Finite state machine
- Feedforward pipelined systems

Two timing schemes are evaluated: (1) *Conservative timing scheme.* The transmitter cannot initiate the next cycle until the receiver has received the data. (2) *Aggressive timing scheme.* The transmitter

[6] *Yield* of a system is defined as the percentage of fabricated systems that meet the timing specifications.

initiates the next cycle as soon as the current data has been sent out. Apparently, the cycle time of a system using the conservative timing scheme is limited by the propagation delay of the interconnects. However, this timing scheme has been widely used in synchronous system design because of the simplicity in its timing verification. In many existing system implementations, the transmitter waits at least a round-trip propagation delay before it sends out the next bit in order to allow the reflections and crosstalk to die out. In contrast, the aggressive timing scheme does not wait for the arrival of the current bit at the receiver before it sends out the next bit and thus tries to pipeline the transmission process in order to alleviate the propagation delay bottleneck.

In addition to the evaluation of these two timing schemes, we also evaluate the impact on the performance improvement of a pipelined system vs. a nonpipelined system when statistical variations of the timing skew are considered.

These evaluations show that the impact from an increase in random skew in the aggressive timing scheme are more dramatic than the conservative timing scheme. For a given static skew (20 ps) and propagation delay (1000 ps),

- The absolute maximum propagation delay of an interconnect limits the maximum system throughput in the conservative timing scheme. An increase of the standard deviation of the random skew or static skew from 1 ps to 10 ps increases the cycle time from 1020 ps to 1200 ps.
- The random skew limits the system throughput in the aggressive timing scheme. An increase of the random skew standard deviation from 1 ps to 10 ps increases the cycle time from 50 ps to 200 ps.

These results show that the cycle time of a digital system design using the conventional (conservative) timing scheme is limited by its physical propagation delay and an interconnect technology with higher bandwidth does not help too much. On the other hand, much smaller cycle time can be achieved by using the aggressive timing scheme and the existing metal interconnect technology becomes the bottleneck for further improvement of the system performance due to the bandwidth limitation and performance impairments of the existing metal interconnect technology. Optical interconnect technology thus becomes very attractive for system designs using the aggressive timing

scheme because it can offer much higher bandwidth and better performance. These results are also used in designing a dense synchronous optical interconnect system in which the subsystem requirements (such as the maximum allowable static timing skew in an optical receiver array or maximum allowable random skew in an optical clock distribution system) need to be derived from the system requirements (such as the system cycle time).

The organization of this chapter is as follows: In Section 2, sources of both static and random timing skew are identified. Based on this statistical timing skew model, Section 3-5 evaluates the timing rules for various synchronous system configurations and derives the system throughput. Numerical results of these timing models are discussed in Section 6. This chapter is summarized in Section 7.

3.2 Sources of Timing Skew

The basic architecture of the synchronous systems examined in this chapter is shown in Figure 3-1. It consists of a transmitter latch, a combinatorial subsystem, and a receiver latch. For simplicity, we only consider the case in which a single-phase clock is distributed throughout the system, and the clock signals are assumed to arrive at all of the outputs of a clock distribution subsystem with similar propagation delay with possible static and random variations due to fabrication and circuit noise. The results obtained here, nevertheless, can be easily extended to a system with multi-phase clocks.

Various delay components are defined in the following: The propagation delay t_p of an interconnection segment is defined as the time interval between the 50% data input edge and the 50% data output edge. The propagation delay t_{pdl} of a latch is defined as the time interval between the 50% clock input edge and the 50% data output edge. The data edge of a latch has to arrive before the clock edge by an interval greater than t_{setup} and should remain stable for a duration greater than t_{hold} after the clock edge. The timing relationship between the data input, clock input and data output of a latch is shown in Figure 3-2. Individual t_{setup} or t_{hold} might be zero or negative, but the width of $t_{setup} + t_{hold}$ window must be zero or positive. To ensure that the latch operates correctly, the data input must remain stable during this window, or the latch might enter into a metastable

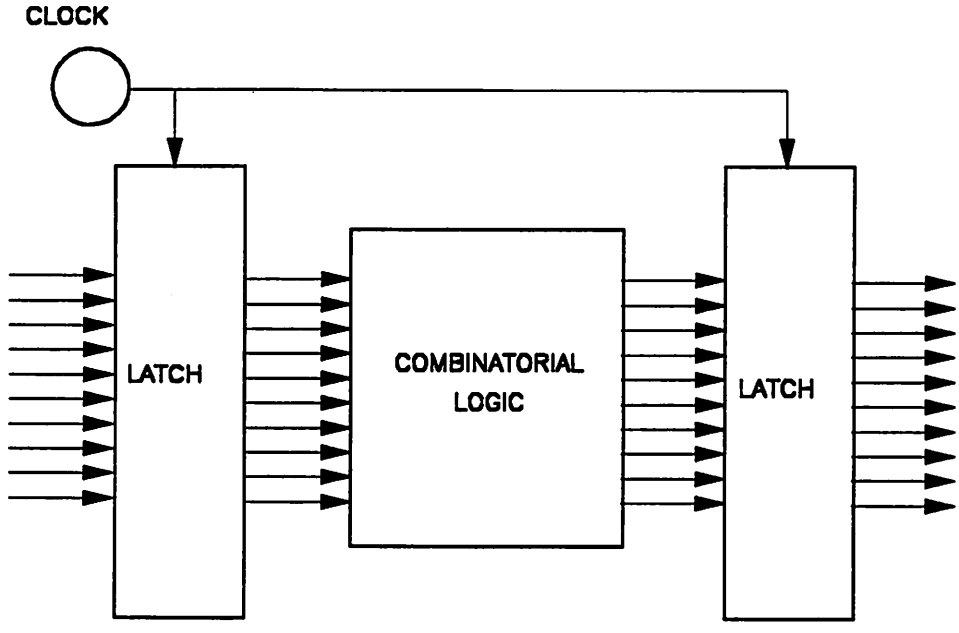

Figure 3-1. Architecture of a synchronous digital system.

state in which its behavior becomes unpredictable [44]. The propagation delay t_{pdc} through a single-input, single-output combinatorial system (such as an inverter) is defined as the time interval between the 50% data input edge and the 50% data output edge. However, the propagation delay of a combinatorial circuit is usually pattern-dependent, and thus has different values for t_{PHL} and t_{PLH}, where t_{PHL} is the propagation delay when the input makes a high-to-low transition while t_{PLH} is the propagation delay when the input makes a low-to-high transition. In these cases we assume $t_{pdcM} = \max\{t_{PHL}, t_{PLH}\}$ and $t_{pdcm} = \min\{t_{PHL}, t_{PLH}\}$. For a multiple-input single-output combinatorial system (such as an AND or XOR gate), the minimum propagation delay t_{pdcm} and the maximum propagation delay t_{pdcM} are defined as the signal propagation delay of the shortest and longest

path, respectively, from any inputs to the output. With these definitions, the data transitions at the output of a combinatorial system can only occur between t_{pdcm} and t_{pdcM}. Similarly, the minimum and maximum propagation delay of a multiple-input multiple-output combinatorial system (such as an ALU or a barrel shifter) are defined as $t_{pdcm} = \min\{t_{pdcm,j}; j = 1, \ldots, N\}$ and $t_{pdcM} = \max\{t_{pdcM,j}; j = 1, \ldots, N\}$, respectively, where $t_{pdcm,j}$ and $t_{pdcM,j}$ represent the corresponding minimum and maximum propagation delay of the j^{th} output.

For such a synchronous system, timing skew is caused by the variations in propagation delay through the clock distribution subsystem, the latch, the interconnections, and the combinatorial

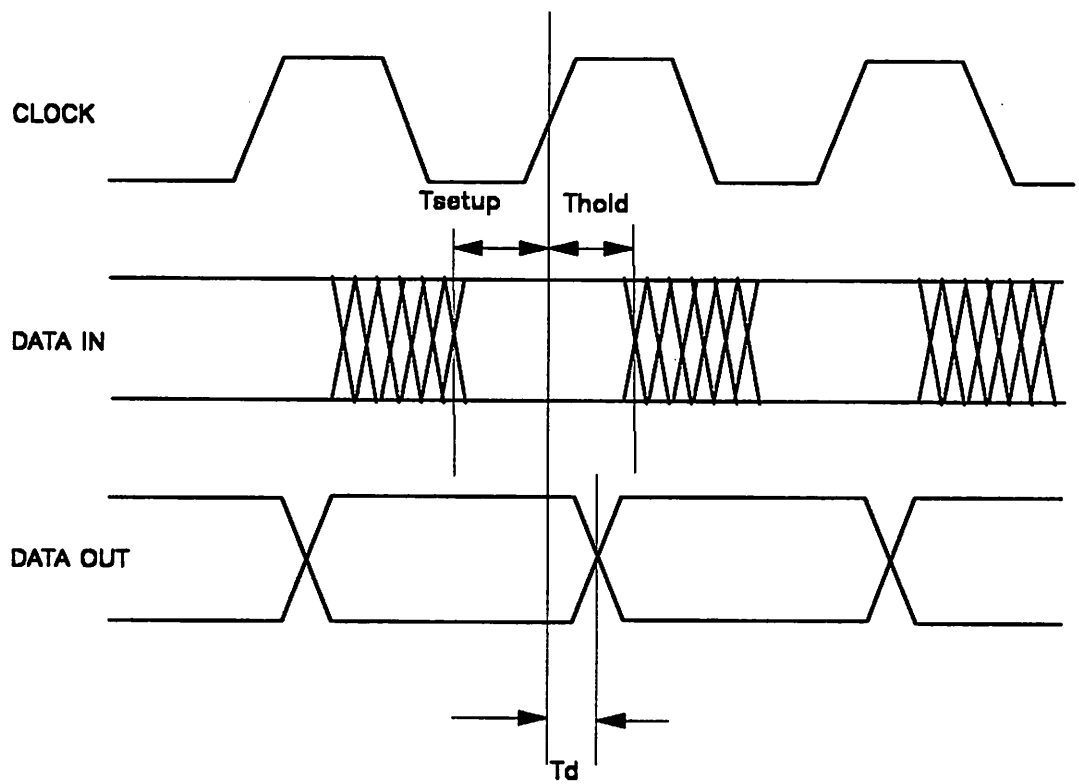

Figure 3-2. Timing relationship between the data input, clock input and the data output of a latch.

logic. Each of these skew components can be further divided into a static and a random component. In the following, we will examine the statistics of these skew components.

3.2.1 Static skew

3.2.1.1 Variation of propagation length and signal group velocity

The variation of propagation length and signal group velocity is usually caused by the following reasons:

- Lithography error caused by the diffraction limited light beam induces variation in propagation delay for interconnects on an IC chip, a multichip module or a printed circuit board.
- Local and global variations during the processing steps in fabricating IC chips and printed circuit boards introduce variations of dielectric constant in the material and causes group velocity variations.

Assuming the nominal signal propagation length from the transmitter to the receiver is l, the nominal signal velocity is v_s, the total propagation delay is $t_p = \frac{l}{v_s}$, the deviation of the propagation delay of the j^{th} interconnect from its nominal value within a synchronous system, as a first-order approximation, equals

$$\Delta\tau_{p,j} = t_p\left(\frac{\Delta l_j}{l} - \frac{\Delta v_{s,j}}{v_s}\right) \tag{3.1}$$

where Δl_j and $\Delta v_{s,j}$ are the propagation length and signal velocity deviation, respectively, from their nominal values. The random variables Δl_j and $\Delta v_{s,j}$ due to process and fabrication variation are assumed to be independent of each other and over all j. The means of Δl_j and $\Delta v_{s,j}$ are both zero while the variances are $\sigma^2_{\Delta l}$ and $\sigma^2_{\Delta v_s}$, respectively. The incurred timing skew $\Delta\tau_{p,j}$ due to variation of propagation delay thus has mean zero and variance

$$\sigma_p^2 = t_{pd}^2\left(\frac{\sigma^2_{\Delta l}}{l^2} + \frac{\sigma^2_{\Delta v_s}}{v_s^2}\right) \tag{3.2}$$

3.2.1.2 Device Variation

Figure 3-3 illustrates a typical ECL gate. Both of the local and global variations in fabrication of such a logic gate cause variations in propagation delay. Local variation in device parameters causes a mismatch between the emitter-coupled pair, resulting a variation in the threshold voltage and thus the switching time. Global variations in device parameters, on the other hand, cause variations in various parasitic *RC*-time constants and resulting variations in the total propagation delay.

The threshold voltage for discriminating an input logic ONE from an input logic ZERO of the j^{th} latch is $V_{TJ} = V_{RJ} + \Delta V_{BEJ}$, where $\Delta V_{BEJ} = V_{BE1J} - V_{BE2J}$ is the mismatch of the base-emitter voltage between transistors Q1 and Q2. The deviation of the threshold voltage from its nominal value ΔV_{TJ} thus equals $\Delta V_{RJ} + \Delta V_{BEJ}$ with mean zero and variance

$$\sigma^2_{\Delta V_T} = \sigma^2_{\Delta V_R} + \sigma^2_{\Delta V_{BE}} + 2\rho_{\Delta V_R \Delta V_{BE}} \sigma_{\Delta V_R} \sigma_{\Delta V_{BE}} \tag{3.3}$$

where $\rho_{\Delta V_R \Delta V_{BE}}$ is the correlation coefficient between ΔV_R and ΔV_{BE}. ΔV_R and ΔV_{BE} are assumed to depend on the same set of device parameters such as dopant concentrations. For a waveform with rise time t_r and full voltage swing $\Delta V = V_{ONE} - V_{ZERO}$, the switching instant is

$$\tau_t = t_r \frac{V_T}{\Delta V} \tag{3.4}$$

The variance of timing skew due to local variation (or threshold uncertainty) therefore equals

$$\sigma^2_{\Delta \tau_{D,lcl}} = t_r^2 \frac{\sigma^2_{\Delta V_T}}{(\Delta V)^2} \tag{3.5}$$

Note that a shorter rise time reduces the sensitivity of the timing skew to the threshold uncertainty.

Global variation in device parameters also causes variation in propagation delay. For a given output voltage swing ΔV, it has been shown in [45] that there exists a linear relationship between the delay and various transistor parameters for a standard ECL or CML gate:

$$\tau_D = K_0\tau_F + \sum_{i=1}^{I}\sum_{j=1}^{J} K_{ij}R_iC_j \tag{3.6}$$

where τ_F is the forward transit time of the electron in a silicon bipolar transistor, R_i's represent the load resistance and various transistor parasitic resistance such as the base resistance, the emitter

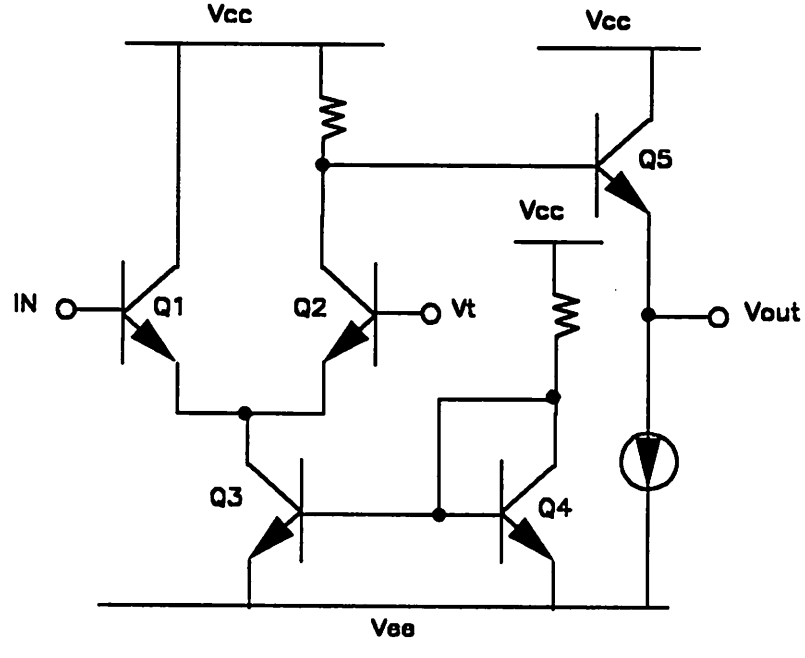

Figure 3-3. Circuitry of a typical ECL gate.

resistance, and the collector resistance. C_j represents various transistor parasitic capacitance such as the collector junction capacitance, the emitter junction capacitance, and the collector-to-substrate capacitance. K_{ij} is the contribution from each parasitic R_iC_j to the total delay. K_{ij} can be determined from circuit simulation, as shown in [46]. Each of these parameters varies from process to process as well as within the same process. The timing skew variance $\sigma^2_{\Delta\tau_{gbl}}$ due to global variation thus equals

$$\begin{aligned}\sigma^2_{\Delta\tau_{D_gbl}} = {} & K_0^2\tau_F^2\frac{\sigma^2_{\Delta\tau_F}}{\tau_F^2} + \sum_{i=1}^{I}\sum_{j=1}^{J}K_{ij}^2R_i^2C_j^2\left(\frac{\sigma^2_{\Delta R_i}}{R_i^2} + \frac{\sigma^2_{\Delta C_j}}{C_j^2}\right) \\ & + 2K_0\tau_F\sum_{i=1}^{I}\sum_{j=1}^{J}K_{ij}R_iC_j\left(\rho_{\Delta\tau_F\Delta R_i}\frac{\sigma_{\Delta\tau_F}\sigma_{\Delta R_i}}{\tau_F R_i} + \rho_{\Delta\tau_F\Delta C_j}\frac{\sigma_{\Delta\tau_F}\sigma_{\Delta C_j}}{\tau_F C_j}\right) \\ & + 2\sum_{i=1}^{I}\sum_{j=1}^{J}\sum_{k=1}^{I}\sum_{l=1}^{J}K_{ij}K_{kl}R_iR_kC_jC_l\left(\frac{\rho_{\Delta R_i\Delta R_k}\sigma_{\Delta R_i}\sigma_{\Delta R_k}}{R_iR_k} + \frac{\rho_{\Delta C_j\Delta C_l}\sigma_{\Delta C_j}\sigma_{\Delta C_l}}{C_jC_l} + \right. \\ & \left. \frac{\rho_{\Delta R_i\Delta C_l}\sigma_{\Delta R_i}\sigma_{\Delta C_l}}{R_iC_l} + \frac{\rho_{\Delta R_k\Delta C_j}\sigma_{\Delta R_k}\sigma_{\Delta C_j}}{R_kC_j}\right)\end{aligned} \tag{3.7}$$

It is clear from this equation that a positive correlation between various device parameters increases the variance of the gate delay, while a negative correlation decreases the gate delay.

3.2.2 Random skew

3.2.2.1 Timing Jitter on the Clock Sources

For a system in which the transmitters and the receivers react to different edges of the same clock sources, jitter generated at the clock source due to noise or temperature drift of the clock source introduces additional timing uncertainties. For such a system, the variance of the timing skew introduced is equal to the variance of the clock jitter, σ^2_{jitter}.

3.2.2.2 Circuit Noise

Noise on the clock or data waveform affects the switching time in the same way as the shift of the logic threshold. The shift in the switching time of a gate is linearly proportional to the noise amplitude in the input waveform, and is also related to the total voltage swing and rise time of the

signal. It is shown in [42, 43] that the timing skew due to the noise on the clock or data waveform is

$$\sigma_{noise}^2 = \frac{t_{rc}^2}{\Delta V^2}\sigma_N^2 \tag{3.8}$$

where σ_N^2 is the variance of noise on the clock or data waveform at the switching instant. Again, a shorter rise time here can reduce the noise sensitivity of the switching instant.

3.3 Timing Rules for Synchronous Bus Systems

Figure 3-4 shows a typical synchronous bus structure that consists of at least one bus master and one or more bus slaves.[7] In this configuration, there is no combinatorial circuitry between the bus drivers and the bus receivers. The clock arrives at the bus drivers with a static skew $\tau_{clk,tx,s}$ and a random skew $\tau_{clk,tx,r}$. Data from the bus drivers are gated onto the bus with a propagation delay $\tau_{pdl,s}$ and a random skew $\tau_{pdl,r}$, while the propagation of data from the bus drivers to the receivers introduces a delay τ_{pd}. The receiver samples the data when the rising edge of the clock crosses the decision threshold. The received clock has a static skew $\tau_{clk,rx,s}$ and a random skew $\tau_{clk,rx,r}$. The sampling time uncertainty due to device variation and noise at the receiver introduces a static skew $\tau_{D,rx,s}$ and a random skew $\tau_{D,rx,r}$. Therefore, the static component of the propagation delay from the source to the destination of the j^{th} channel is:

$$\tau_{static} = \tau_{clk,tx,s} + \tau_{pdl,s} + \tau_{pd} + \tau_{clk,rx,s} + \tau_{D,rx,s} \tag{3.9}$$

The random component of the relative skew is:

$$\tau_{random} = \tau_{clk,tx,r} + \tau_{pdl,r} + \tau_{clk,rx,r} + \tau_{D,rx,r} + \tau_{jitter} \tag{3.10}$$

[7] A bus master is defined as a subsystem that can initiate bus transactions (either read or write), while a bus slave cannot.

with mean zero and variance

$$\sigma^2_{random} = \sigma^2_{clk,tx,r} + \sigma^2_{pdl,r} + \sigma^2_{clk,rx,r} + \sigma^2_{D,rx,r} + \sigma^2_{jitter} \tag{3.11}$$

since the random components of the skew are assumed independent of each other.

In the following, we evaluate the system throughput based on the conservative and aggressive timing scheme.

3.3.1 Conservative design

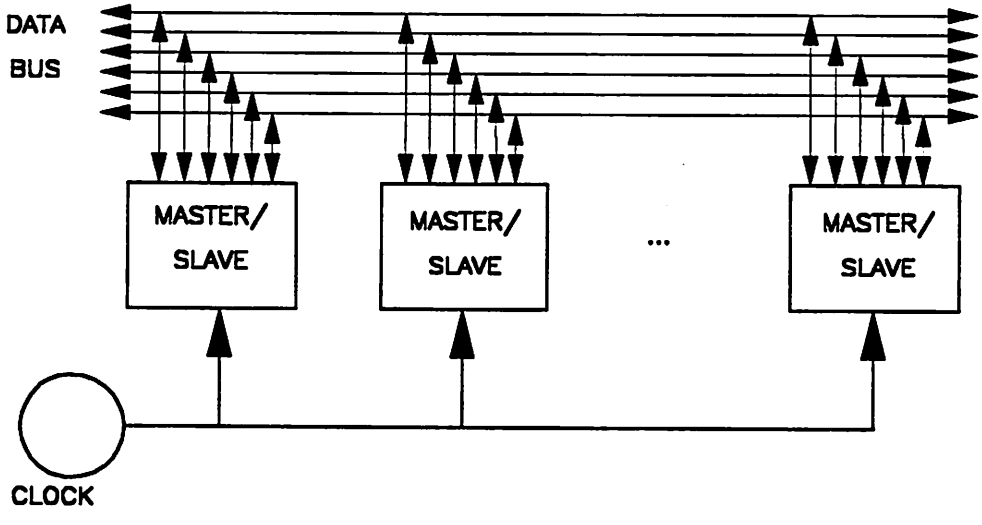

Figure 3-4. Architecture of a synchronous bus.

In this design methodology, the receiver uses the next clock edge relative to the edge used by the transmitter. In order to ensure correct operation of a system, data released from transmitter latches during a clock transition should arrive at the receiver latches

- before the setup-hold window of the next clock edge,
- after the setup-hold window of the current clock edge.

The first requirement is to ensure data arrives in time, while the second requirement is to ensure previously arrived data remains stable until after the setup-hold window. This timing relationship between the transmitters and the receivers is illustrated in Figure 3-5. We thus require the following timing relationship:

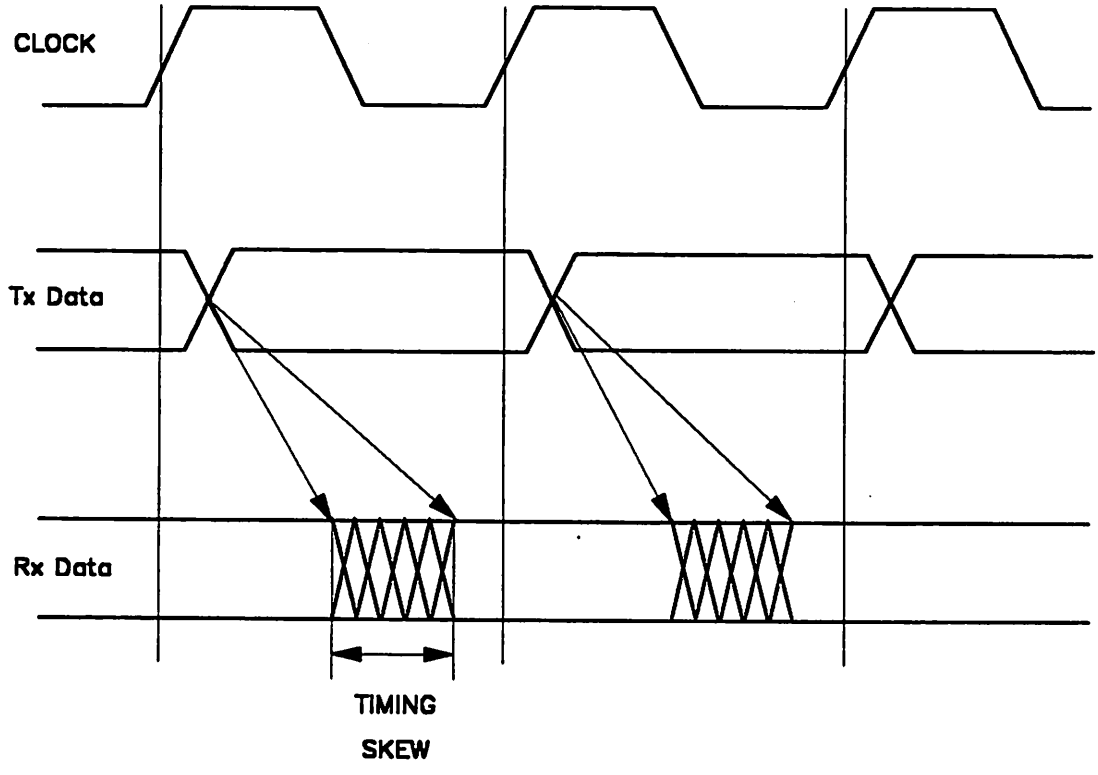

Figure 3-5. Timing relationship between the transmitter and the receiver in a synchronous bus. A conservative scheme is assumed here.

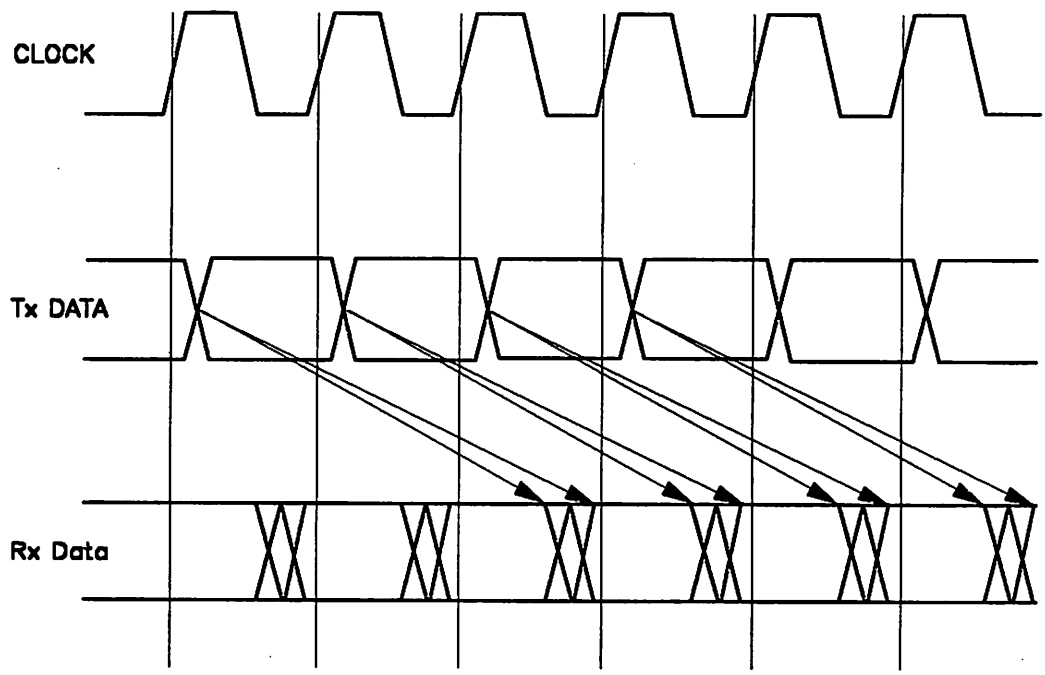

Figure 3-6. Timing relationship between the transmitter and the receiver in a synchronous bus. An aggressive scheme is assumed here.

$$\begin{aligned} &T - t_{setup} \geq \tau_{static,j} + \tau_{random,j} \\ &\tau_{static,j} + \tau_{random,j} \geq t_{hold} \\ &j = 1, ..., N \end{aligned} \tag{3.12}$$

where T is the cycle time of the bus, $\tau_{static,j}$ and $\tau_{random,j}$ are the static and random skew of the j^{th} channel, respectively, and N is the width of the bus. In order to achieve a failure rate less than P_e for a given system consisting of N parallel interconnects, the following inequality has to be satisfied:

$$\prod_{j=1}^{N} \text{Prob}[T - t_{setup} - \tau_{static,j} \geq \tau_{random} \geq t_{hold} - \tau_{static,j}] \geq 1 - P_e \tag{3.13}$$

for a given set of $\{\tau_{static,1}, \ldots, \tau_{static,N}\}$.

We assume $\sigma^2_{static} \gg \sigma^2_{random}$, the failure modes of a system are therefore determined by the extreme values of $\tau_{static,i}$ and Eq.(3.12) can be approximated by

$$\begin{aligned} &T - t_{setup} \geq \tau_{static,I} + \tau_{random,I} \\ &\tau_{static,J} + \tau_{random,J} \geq T + t_{hold} \\ &I \neq J \end{aligned} \tag{3.14}$$

In order to have an error rate less than P_e for a given system, we need

$$\text{Prob}[T - t_{setup} - \tau_{\max} \geq \tau_{random}]\text{Prob}[\tau_{random} \geq t_{hold} - \tau_{\min}] \geq 1 - P_e \tag{3.15}$$

since $\tau_{random,I}$ and $\tau_{random,J}$ are independent and have the same probability distribution. Note that only the first term in Eq.(3.14) depends on the speed of the bus. Therefore, if $\text{Prob}[\tau_{random} \geq t_{hold} - \tau_{\min}] < 1 - P_e$, there does not exist a value of T which satisfies Eq.(3.15) since $\text{Prob}[T - t_{setup} - \tau_{\max} \geq \tau_{random}]$ is always less than 1. In the following discussion, we will only consider the timing rules of a system *given* $\text{Prob}[\tau_{random} \geq t_{hold} - \tau_{\min}] \geq 1 - P_e$. If the probability density function of τ_{random} is $r(\tau)$, Eq.(3.15) reduces to

$$\int_{-\infty}^{T - t_{setup} - \tau_{\max}} r(\tau)d\tau \int_{t_{hold} - \tau_{\min}}^{\infty} r(\tau)d\tau > 1 - P_e \tag{3.16}$$

The minimum cycle time $T_{\min}$ (or the maximum speed) that can be achieved by a bus system is the solution to Eq.(3.16):

$$T_{\min} = t_{setup} + \tau_{\max} + R^{-1}\left(\frac{1-P_e}{1-R(t_{hold}-\tau_{\min})}\right) \tag{3.17}$$

where $R(.)$ is the cumulative distribution function of τ_{random}. The distribution $R(.)$ is a strictly monotonic function so that its inverse $R^{-1}(.)$ exists.

Assuming the probability density function and the cumulative distribution function of $T_{\min}$ is $h_T(t)$ and $H_T(t)$, respectively, the *yield* of the bus systems for a given distribution of the static skew is Prob$[T_{\min} \le t_{\min}]$ and equals $H_T(t_{\min})$. *Yield* of such a bus system is defined as the percentage of the systems fabricated that meet the minimum system cycle time specification $t_{\min}$. The probability density function $h_T(t)$ can be derived from (3.17), given the joint probability density function of $\tau_{\max}$ and $\tau_{\min}$ is known. The mean value of the cycle time μ_T over an ensemble of bus systems is:

$$\mu_T = \int\int \left\{ t_{setup} + \tau_{\max} + R^{-1}\left(\frac{1-P_e}{1-R(t_{hold}-\tau_{\min})}\right)\right\} f(\tau_{\max}, \tau_{\min}) d\tau_{\min} d\tau_{\max} \tag{3.18}$$

while the variance is

$$\sigma_T^2 = \int\int \left\{ t_{setup} + \tau_{\max} + R^{-1}\left(\frac{1-P_e}{1-R(t_{hold}-\tau_{\min})}\right)\right\}^2 f(\tau_{\max}, \tau_{\min}) d\tau_{\min} d\tau_{\max} - \mu_T^2 \tag{3.19}$$

where $f(\tau_{\max}, \tau_{\min})$ is the joint probability density function of $\tau_{\max}$ and $\tau_{\min}$. For an N-channel system with each channel having independent and identical statistics, the probability density function for $\tau_{\min}$, $\tau_{\max}$, which are *order statistics* of the $\tau_{static,i}$'s, are [47]:

$$\begin{aligned} f_1(\tau_{\min}) &= N(1-G(\tau_{\min}))^{N-1} g(\tau_{\min}) \\ f_N(\tau_{\max}) &= N G^{N-1}(\tau_{\max}) g(\tau_{\max}) \end{aligned} \tag{3.20}$$

The joint probability density function for τ_{max} and τ_{min} equals [47]:

$$f(\tau_{min}, \tau_{max}) = N(N-1)[G(\tau_{max}) - G(\tau_{min})]^{N-2} g(\tau_{max}) g(\tau_{min}) \tag{3.21}$$

where τ_{max} and τ_{min} are the maximum and minimum propagation delay, respectively, while $G(.)$ and $g(.)$ are the cumulative distribution function and probability density function, respectively, of the random variable τ_{static}.

If there is no random skew, T_{min} is solely determined by $\tau_{max} + t_{setup}$ and the probability density function of T_{min} is a shifted verion of the probability density function of τ_{max}. The variance of T_{min} is identical to the variance of τ_{max}. When the random skew is taken into consideration, both of the mean and the variance of T_{min} are increased, as it is evident from Eq.(3.18) and Eq.(3.19).

If the random skew of a channel is Gaussian distributed with mean zero and σ^2_{random}, Eq.(3.16) reduces to

$$\left(1 - \frac{1}{2}\,\mathrm{erfc}\left(\frac{|T - t_{setup} - \tau_{max}|}{\sqrt{2}\,\sigma_{random}}\right)\right)\left(1 - \frac{1}{2}\,\mathrm{erfc}\left(\frac{|t_{hold} - \tau_{min}|}{\sqrt{2}\,\sigma_{random}}\right)\right) \geq 1 - P_e \tag{3.22}$$

where erfc(x) is the complementary error function.

Zero rise time has been assumed for the analysis so far. In order to account for the finite rise time, all of the t_{hold} and t_{setup} can be substituted by $t_{hold} + 1/2t_r$ and $t_{setup} + 1/2t_r$ respectively.

3.3.2 Aggressive design

As shown in the previous subsection, the absolute signal propagation delay severely limits the speed of a bus. In this subsection, we will evaluate a propagation delay independent design methodology which can reduce or eliminate the impact from this constraint.

In this scheme, we assume the bus master is responsible to activate a *data_valid* signal on one of the bus channels so that the receiver can begin latching the incoming data on every clock edge

once this signal is detected.[8] The bus transactions will be continued until the *data_valid* signal is no longer active. The bus receiver is assumed to use the M^{th} clock edge relative to the edge used by the bus driver. The timing relationship between the transmitted data and the received data in this scheme is shown in Figure 3-6. In order to ensure that this bus system operates correctly, it is necessary to have the arriving data edge of any channel earlier than the setup-hold window of the M^{th} clock edge, but later than the setup-hold window of the $(M-1)^{th}$ clock edge, both of which are relative to the clock edge used for transmitting the data. Similar to the procedures used in deriving Eq.(3.12), we require

$$\begin{aligned} &MT - t_{setup} \geq \tau_{static,I} + \tau_{random,I} \\ &\tau_{static,I} + \tau_{random,I} \geq (M-1)T + t_{hold} \\ &i = 1, ..., N; \quad M \geq 1 \end{aligned} \tag{3.23}$$

Note that M decreases as T increases. This scheme reduces to the conservative scheme described earlier when M equals 1.

Again, we assume $\sigma^2_{static} \gg \sigma^2_{random}$, the failure modes of a system are therefore determined by the extreme values of $\tau_{static,I}$ and Eq.(3.23) can be approximated by

$$\begin{aligned} &MT - t_{setup} \geq \tau_{\max} + \tau_{random,I} \\ &\tau_{\min} + \tau_{random,J} \geq (M-1)T + t_{hold} \\ &I \neq J; \quad M \geq 1 \end{aligned} \tag{3.24}$$

In order to have an error rate less than P_e for a given system, we need

$$\text{Prob}[MT - t_{setup} - \tau_{\max} \geq \tau_{random}]\text{Prob}[\tau_{random} \geq t_{hold} - \tau_{\min} + (M-1)T] \geq 1 - P_e \tag{3.25}$$

Assuming the probability density function of τ_{random} is $r(\tau)$, we thus have

---

[8] The *data_valid* signal may not be necessary if the receiver can decode the address from the bus data and determine whether it is the destination for the incoming bus data.

$$\int_{-\infty}^{MT - t_{setup} - \tau_{\max}} r(\tau)d\tau \int_{t_{hold} - \tau_{\min} + (M-1)T}^{\infty} r(\tau)d\tau > 1 - P_e \tag{3.26}$$

This inequality can be solved recursively:

$$MT_{\min} = t_{setup} + \tau_{\max} + R^{-1}\left(\frac{1 - P_e}{1 - R(t_{hold} - \tau_{\min} + (M-1)T_{\min})} \right) \tag{3.27}$$

If the skew of a channel relative to its nominal value is Gaussian distributed with mean zero and σ^2_{random}, Eq.(3.26) reduces to

$$\left(1 - \frac{1}{2}\operatorname{erfc}\left(\frac{|MT_{\min} - t_{setup} - \tau_{\max}|}{\sqrt{2}\,\sigma_{random}}\right)\right)\left(1 - \frac{1}{2}\operatorname{erfc}\left(\frac{|t_{hold} - \tau_{\min} + (M-1)T_{\min}|}{\sqrt{2}\,\sigma_{skew}}\right)\right) \geq 1 - P_e \tag{3.28}$$

In our analysis, reflections and crosstalk in data transmission have been ignored. There are situations such as

- The static timing skew is close to the propagation delay,
- Each cycle has to allow additional *signal settling time* so that the reflections and crosstalk can die out.

where using the largest attainable M in the aggressive timing scheme becomes infeasible. However, the maximum throughput obtained from using the maximum allowable M can still serve as an upper bound of the real system throughput.

3.4 Timing Rules for Finite State Machines

A typical finite-state machine, shown in Figure 3-7, consists of a state register and a combinatorial subsystem. Upon receiving a clock edge, the register releases the data into a multiple-input multiple-output combinatorial subsystem, and the output from the combinatorial subsystem is

sampled upon receiving of the next clock edge. The clock arrives at the state register with a static skew $\tau_{clk,tx,s}$ and a random skew $\tau_{clk,tx,r}$. Data from the state register are gated into the combinatorial subsystem with a propagation delay $t_{pdl,s}$ and a random skew $\tau_{pdl,r}$. The propagation of the data from the inputs to the j^{th} output of the combinatorial subsystem has a minimum propagation delay $\tau_{pdcm,j}$ and a maximum propagation delay $\tau_{pdcM,j}$. The associated random skew is $\tau_{pd,r}$. The state register samples the data when the rising edge of the clock crosses the decision threshold. The receiver clock has a static skew $\tau_{clk,rx,s}$ and a random skew $\tau_{clk,rx,r}$. The sampling time uncertainty introduces a static skew $\tau_{D,rx,s}$ and a random skew $\tau_{D,rx,r}$. Therefore, the maximum propagation delay of of the j^{th} channel is:

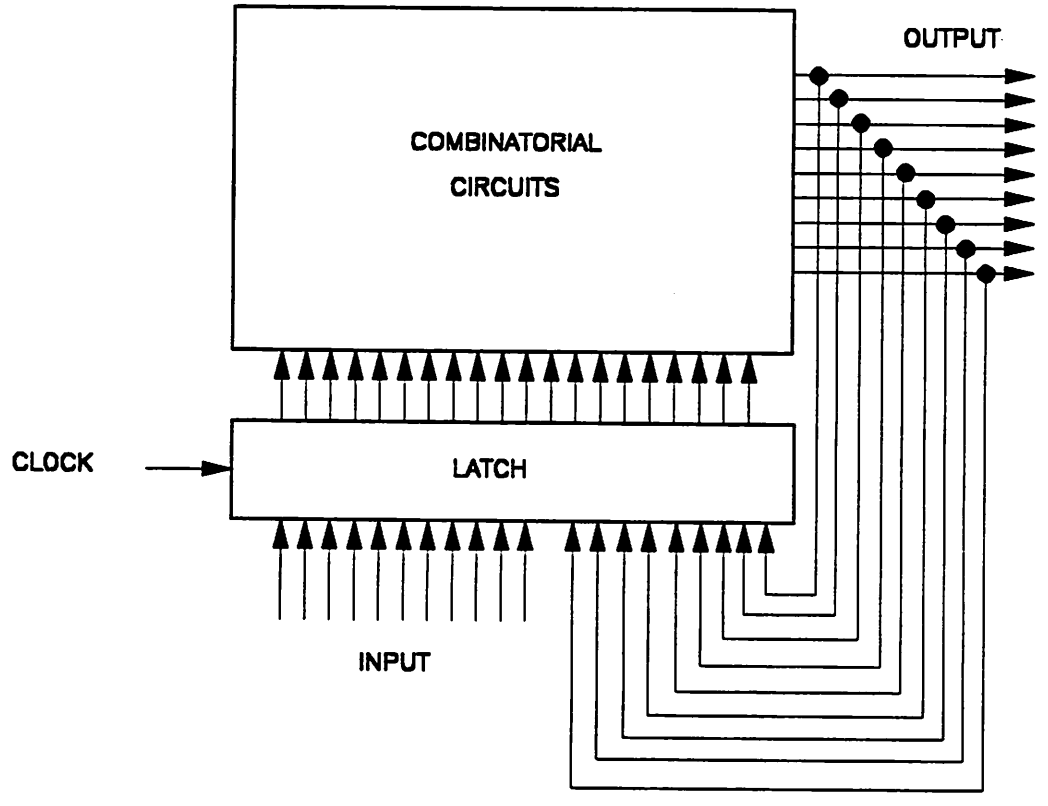

Figure 3-7. Architecture of a finite state machine.

$$\tau_{staticMj} = \tau_{clk,tx,s} + \tau_{pdl,s} + \tau_{pdMj} + \tau_{clk,rx,s} + \tau_{D,rx,s} \tag{3.29}$$

and the minimum propagation delay is

$$\tau_{staticmj} = \tau_{clk,tx,s} + \tau_{pdl,s} + \tau_{pdmj} + \tau_{clk,rx,s} + \tau_{D,rx,s} \tag{3.30}$$

while the random component of the skew is:

$$\tau_{random} = \tau_{clk,tx,r} + \tau_{pdl,r} + \tau_{pd,r} + \tau_{clk,rx,r} + \tau_{jitter} \tag{3.31}$$

with mean zero and variance

$$\sigma^2_{random} = \sigma^2_{clk,tx,r} + \sigma^2_{pdl,r} + \sigma^2_{pd,r} + \sigma^2_{clk,rx,r} + \sigma^2_{jitter} \tag{3.32}$$

For the finite state machine, it is not feasible to use an aggressive design methodology due to the feedback from the combinatorial outputs to the state register. In order to ensure correct operation of this finite state machine, we require

$$\begin{aligned} &T - t_{setup} \geq \tau_{staticMj} + \tau_{random} \\ &\tau_{staticmj} + \tau_{random} \geq t_{hold} \\ &j = 1, ..., N \end{aligned} \tag{3.33}$$

Similar to the conservative design in the synchronous bus case, if we assume $\sigma^2_{static} \gg \sigma^2_{random}$, Eq.(3.33) can be simplified to

$$\begin{aligned} &T - t_{setup} \geq \tau_{staticM} + \tau_{random} \\ &\tau_{staticm} + \tau_{random} \geq t_{hold} \end{aligned} \tag{3.34}$$

where $\tau_{staticM} = \max\{\tau_{staticM,j}\ j = 1,..,N\}$, and $\tau_{staticm} = \min\{\tau_{staticm,j}\ j = 1,..,N\}$. In order to achieve a failure rate less than P_e, we require

$$\text{Prob}[T - t_{setup} \geq \tau_{staticM} + \tau_{random}]\text{Prob}[\tau_{random} \geq t_{hold} - \tau_{staticm}] \geq 1 - P_e \tag{3.35}$$

The minimum cycle time for the finite state machine can be obtained by using a similar technique to that which leads to Eq.(3.17):

$$T_{\min} = t_{setup} + \tau_{staticM} + R^{-1}\left(\frac{1 - P_e}{1 - R(t_{hold} - \tau_{staticm})}\right) \tag{3.36}$$

3.5 Throughput Improvement from Pipelined Architecture

Pipelining of a combinatorial system, which is achieved by inserting latches in the middle of a system, has been a standard technique to shorten the cycle time and increase the system throughput. In this section, we investigate the throughput improvement of a feedforward system with a pipeline structure as compared to that of the same system without pipelining. Only the conservative approach is evaluated here, but the results obtained can be extended to the aggressive approach.

3.5.1 Pipelined approach

For simplicity, we assume a combinatorial subsystem which has similar delay characteristics among channels (such as in an ALU). This combinatorial subsystem is partitioned into L stages with each stage having approximately equal amount of delay and a latch is inserted between successive two stages, as shown in Figure 3-8. Using a similar definition for the delay and skew components as used in previous sections, the static skew component of the j^{th} channel of the i^{th} stage in a pipelined structure is:

$$\tau_{static} = \tau_{clk,tx,s} + \tau_{pdl,s} + \tau_{pdc,s} + \tau_{clk,rx,s} + \tau_{D,rx,s} \tag{3.37}$$

while the random component of the relative skew is:

$$\tau_{random} = \tau_{clk,tx,r} + \tau_{pdc,r} + \tau_{clk,rx,r} + \tau_{D,rx,r} + \tau_{jitter} \tag{3.38}$$

with mean zero and variance

$$\sigma^2_{random} = \sigma^2_{clk,tx,r} + \sigma^2_{pdc,r} + \sigma^2_{clk,rx,r} + \sigma^2_{D,rx,r} + \sigma^2_{jitter} \tag{3.39}$$

In a conservative design, the data is maintained stable throughout the whole period, we thus require

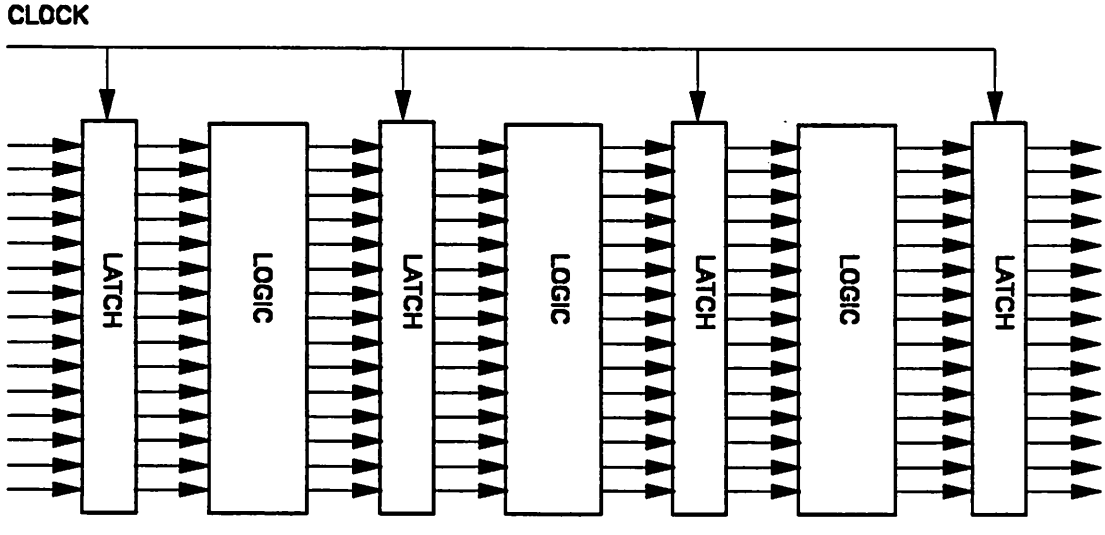

Figure 3-8. Architecture of a pipelined system.

$$
\begin{aligned}
&T - t_{setup} \geq \tau_{static,ij} + \tau_{random} \\
&\tau_{static,ij} + \tau_{random} \geq t_{hold} \\
&i = 1,...,N \; j = 1,...,L
\end{aligned}
\tag{3.40}
$$

where i represents the i^{th} channel while j represents the j^{th} stage in the pipelined structure. In order to achieve a failure rate less than P_e, we thus have

$$
\prod_{i=1}^{N} \prod_{j=1}^{L} \text{Prob}[T - t_{setup} - t_{static,ij} \geq \tau_{random} \geq t_{hold} - t_{static,ij}] \geq 1 - P_e \tag{3.41}
$$

Similar to Section 3, the failure modes will be determined by the extreme values of $\tau_{static,ij}$ if we assume $\sigma^2_{static} \gg \sigma^2_{random}$. Eq.(3.41) can therefore be approximated by

$$
\begin{aligned}
&T - t_{setup} \geq \tau_{\max} + \tau_{random,pq} \\
&\tau_{static,rs} + \tau_{random} \geq t_{hold} \\
&pq \neq rs
\end{aligned}
\tag{3.42}
$$

where

$$
\begin{aligned}
&\tau_{\max} = \tau_{static,pq} = \max \{\tau_{static,ij} \;\; i = 1,..,N \; j = 1,..,L\} \\
&\tau_{\min} = \tau_{static,rs} = \min \{\tau_{static,ij} \;\; i = 1,..,N \; j = 1,..,L\}
\end{aligned}
\tag{3.43}
$$

In order to achieve a failure rate less than P_e, we thus require

$$
\text{Prob}[T - t_{setup} - \tau_{\max} \geq \tau_{random}]\text{Prob}[\tau_{random} \geq t_{hold} - \tau_{\min}] \geq 1 - P_e \tag{3.44}
$$

If the probability density function of τ_{random} is $r(\tau)$, Eq.(3.44) reduces to

$$\int_{-\infty}^{T - t_{setup} - \tau_{max}} r(\tau)d\tau \int_{t_{hold} - \tau_{min}}^{\infty} r(\tau)d\tau > 1 - P_e \tag{3.45}$$

The minimum cycle time T_{min} that can be achieved by a pipelined system is the solution to Eq.(3.45):

$$T_{min,pipe} = t_{setup} + \tau_{max,pipe} + R^{-1}\left(\frac{1 - P_e}{1 - R(t_{hold} - \tau_{min,pipe})}\right) \tag{3.46}$$

Both the mean and the variance of the maximum operating speed over an *ensemble* of pipelined systems can be found by following similar procedures to those leading to Eq. (3.18) and Eq. (3.19) in Section 3.

3.5.2 Nonpipelined approach

For a nonpipelined feedforward architecture, the static skew component of of the j^{th} channel is:

$$\tau_{static,j} = \tau_{clk,tx,s} + \tau_{pdl,s} + \sum_{l=1}^{N} \tau_{static,jl} + \tau_{clk,rx,s} + \tau_{D,rx,s} \tag{3.47}$$

The random component of the relative skew is:

$$\tau_{random} = \tau_{clk,tx,r} + \tau_{pdl,r} + \sum_{l=1}^{N} \tau_{pdc,r,l} + \tau_{clk,rx,s} + \tau_{jitter} \tag{3.48}$$

with mean zero and variance

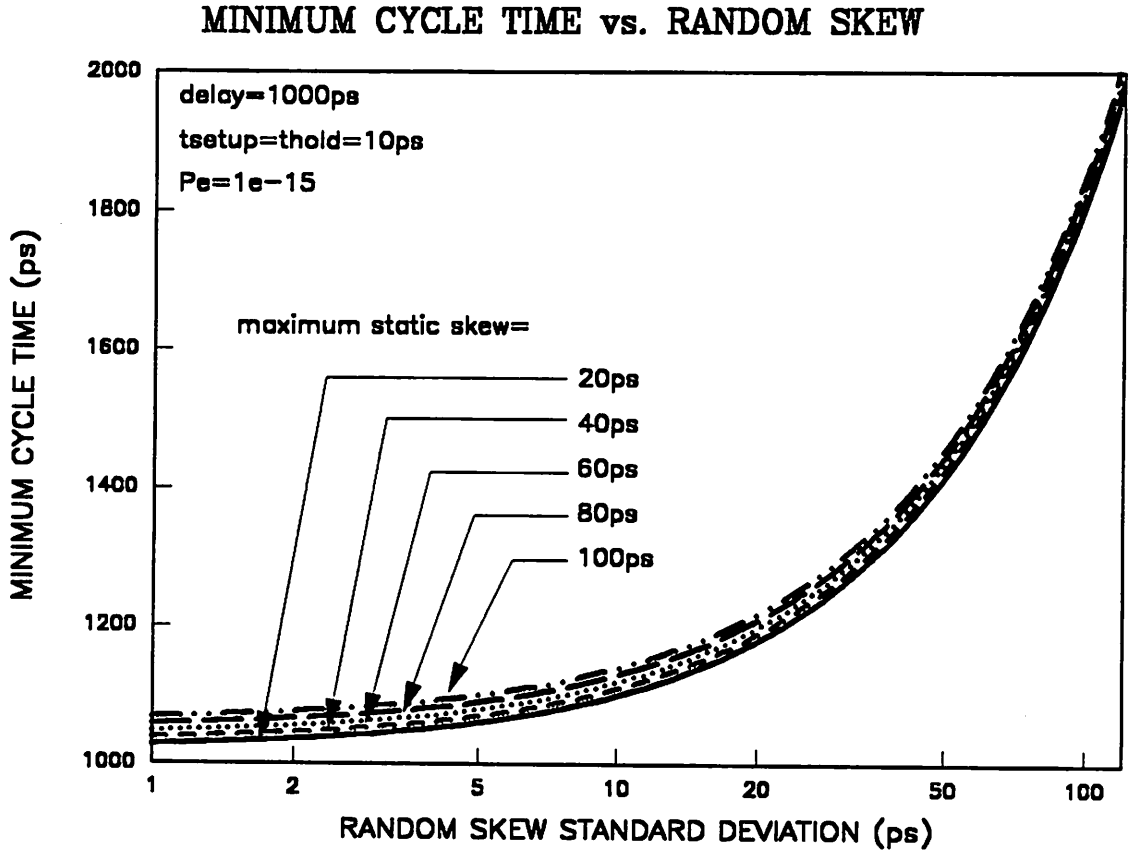

Figure 3-9. Minimum cycle time as a function of the standard deviation of the random skew. Nominal propagation delay is 1000 ps. The maximum static skew is varied from 20 ps to 100 ps, which correspond to τ_{max} from 1010 ps to 1050 ps while τ_{min} from 950 ps to 990 ps. Both of the t_{setup} and the t_{hold} are assumed to be 10 ps. The error rate is assume to be 10^{-15}.

$$\sigma^2_{random} = \sigma^2_{clk,tx} + \sigma^2_{pdl,r} + N\sigma^2_{pdc,r} + N(N-1)\rho_r\sigma^2_{pdc,r} + \sigma^2_{clk,rx,r} + \sigma^2_{jitter} \tag{3.49}$$

where ρ_r is the correlation coefficient between the random skew of different stages. T_{min} for the nonpipelined architecture thus equals:

$$T_{min,nonpipe} = t_{setup} + \tau_{max,nonpipe} + R^{-1}\left(\frac{1-P_e}{1-R(t_{hold}-\tau_{min,nonpipe})}\right) \tag{3.50}$$

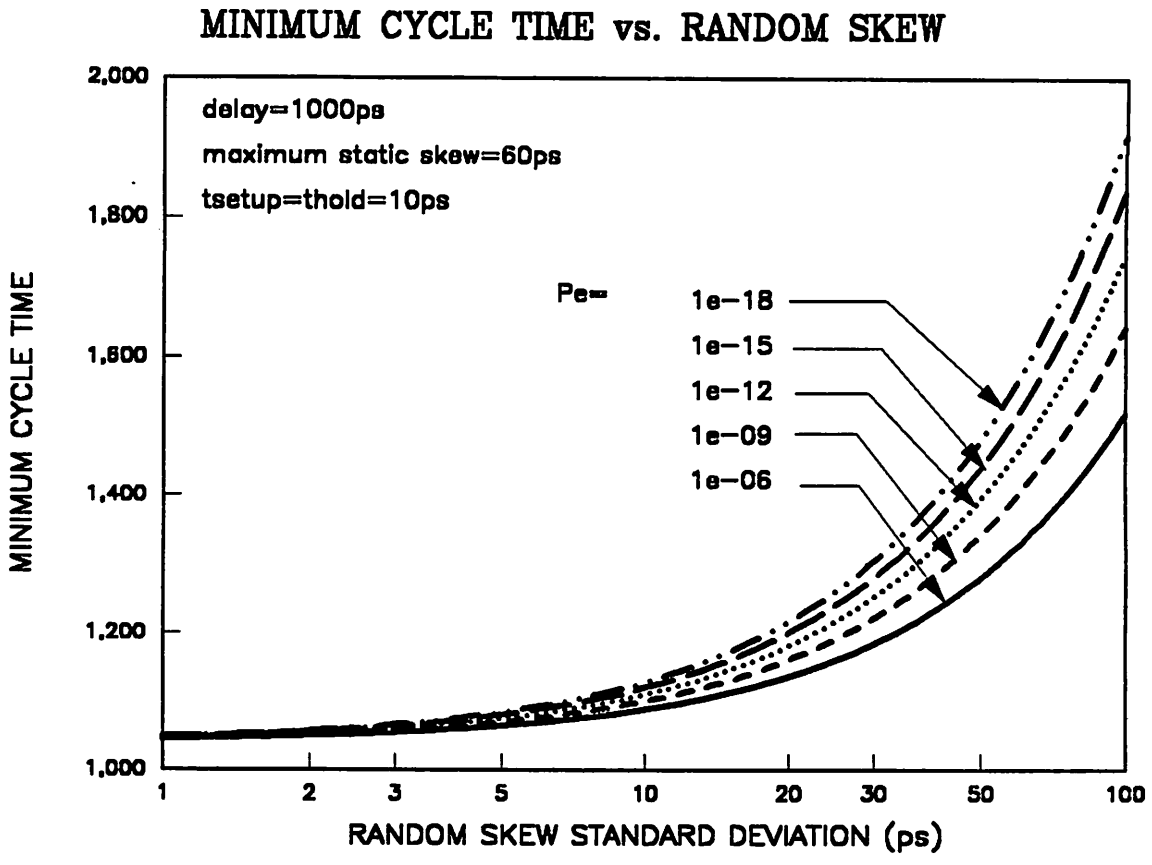

Figure 3-10. Minimum cycle time as a function of the standard deviation of the random skew for conservative design scheme. The system error rate is varied from 10^{-6} to 10^{-18}. Nominal propagation delay is 1000 ps. The maximum static skew is 60 ps, which correspond to that τ_{max} equals 1030 ps and τ_{min} equals 970 ps. Both of the t_{setup} and the t_{hold} are assumed to be 10 ps.

The throughput improvement can be found by evaluating $T_{min\_nonpipe}/T_{min\_pipe}$.

3.6 Numerical Results

In this section, we evaluate the minimum cycle time for both conservative and aggressive schemes. Since the expressions for the minimum cycle time are similar for all of the synchronous buses, finite state machines, and pipelined systems, the numerical results discussed in this section are therefore applicable to all of these cases.

Figure 3-9 and Figure 3-10 show the minimum cycle time as a function of σ_{random} for the conservative design scheme. For small random skew ($\sigma_{random} \ll$ 100 ps), the minimum cycle time is limited by $\tau_{max} + \tau_{setup}$. The minimum cycle time increases from 1020 ps to 1200 ps as the standard deviation of the random skew increases from 1 ps to 10 ps. When the random skew exceeds 100 ps, it is not possible to achieve the required system performance ($P_e = 10^{-15}$) even with large cycle time, due to the fact that the timing rule $\tau_{random} \geq \tau_{hold} - \tau_{min}$ can no longer be enforced. Furthermore, increased static skew also increases the minimum cycle time as a result of increased

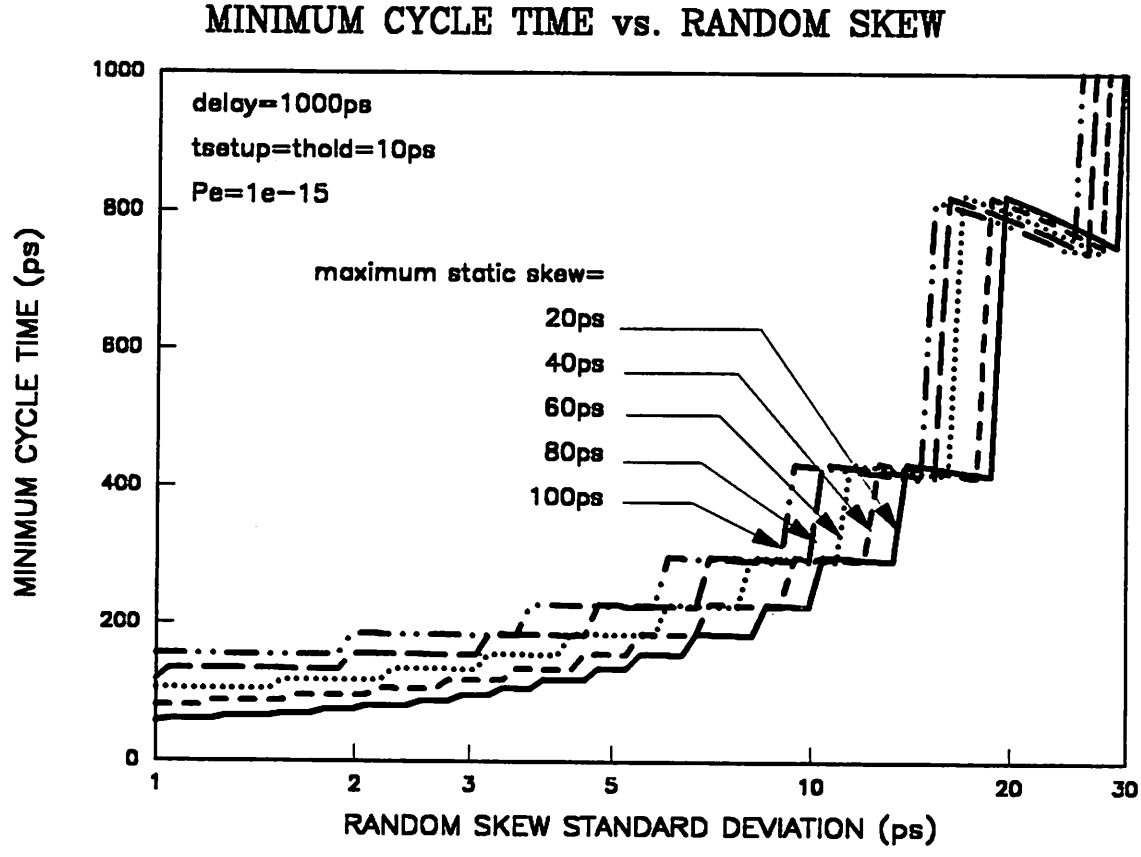

Figure 3-11. Minimum cycle time as a function of the standard deviation of the random skew for the aggressive design scheme. The system error rate is 10^{-15}. Nominal propagation delay is 1000 ps. The static skew is varied from 20 ps to 100ps, which correspond to τ_{max} from 1010 to 1050 and τ_{min} from 950 ps to 990 ps. Both of the t_{setup} and the t_{hold} are assumed to be 10 ps.

$\tau_{max} + t_{setup}$. More stringent requirement on P_e increases the minimum cycle time, which is evident from Figure 3-10.

Figure 3-11, Figure 3-12, and Figure 3-13 show the minimum cycle time for the aggressive timing scheme. In Figure 3-11 and Figure 3-12, the minimum cycle time is plotted as a function of the σ_{random} for various values of static skew and P_e, respectively. A similar global trend between the minimum cycle time and σ_{random} as compared to the conservative scheme can be observed here, except that the minimum cycle time here is limited by the difference between τ_{max} and τ_{min}. The minimum cycle time increases from 50 ps to 200 ps as the standard deviation of the random skew

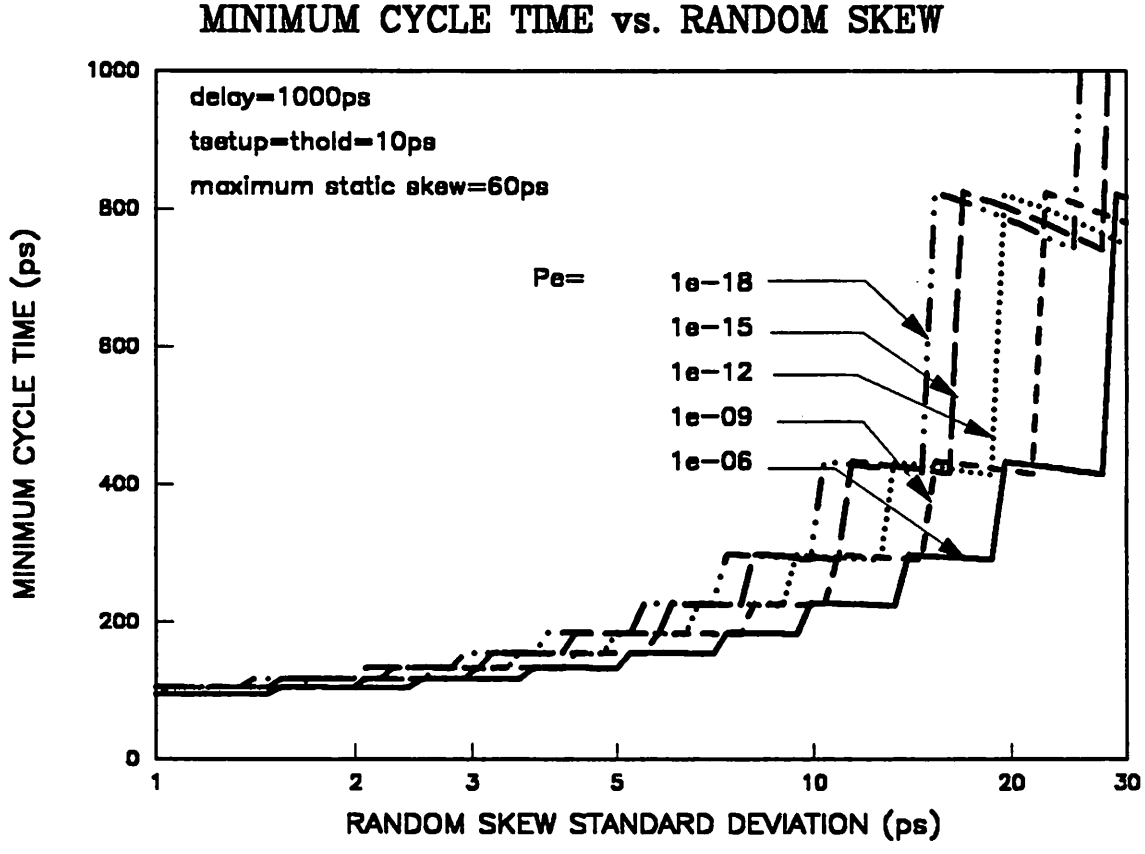

Figure 3-12. Minimum cycle time as a function of the standard deviation of the random skew for the aggressive design scheme. The system error rate is varied from 10^{-6} to 10^{-18}. Nominal propagation delay is 1000 ps. The static skew is kept at 60 ps, which correspond to τ_{max} equals 1030 ps and τ_{min} equals 970 ps. Both of the t_{setup} and the t_{hold} are assumed to be 10 ps.

increases from 1 ps to 10 ps. The zigzag shape of the curve is due to the effect of integer values of M in the timing rule. As random skew increases, T_{min} remains essentially constant until M has to be decreased. At this time, there is a big step increase in T_{min}. Similar effects can be observed in Figure 3-13 for the relationship between the minimum cycle time and the static skew. For a given random skew standard deviation of 10 ps, the minimum cycle time increases from 200 ps to 400 ps as the static skew ($(\tau_{max} - \tau_{min})/2$) increases from 20 ps to 100 ps.

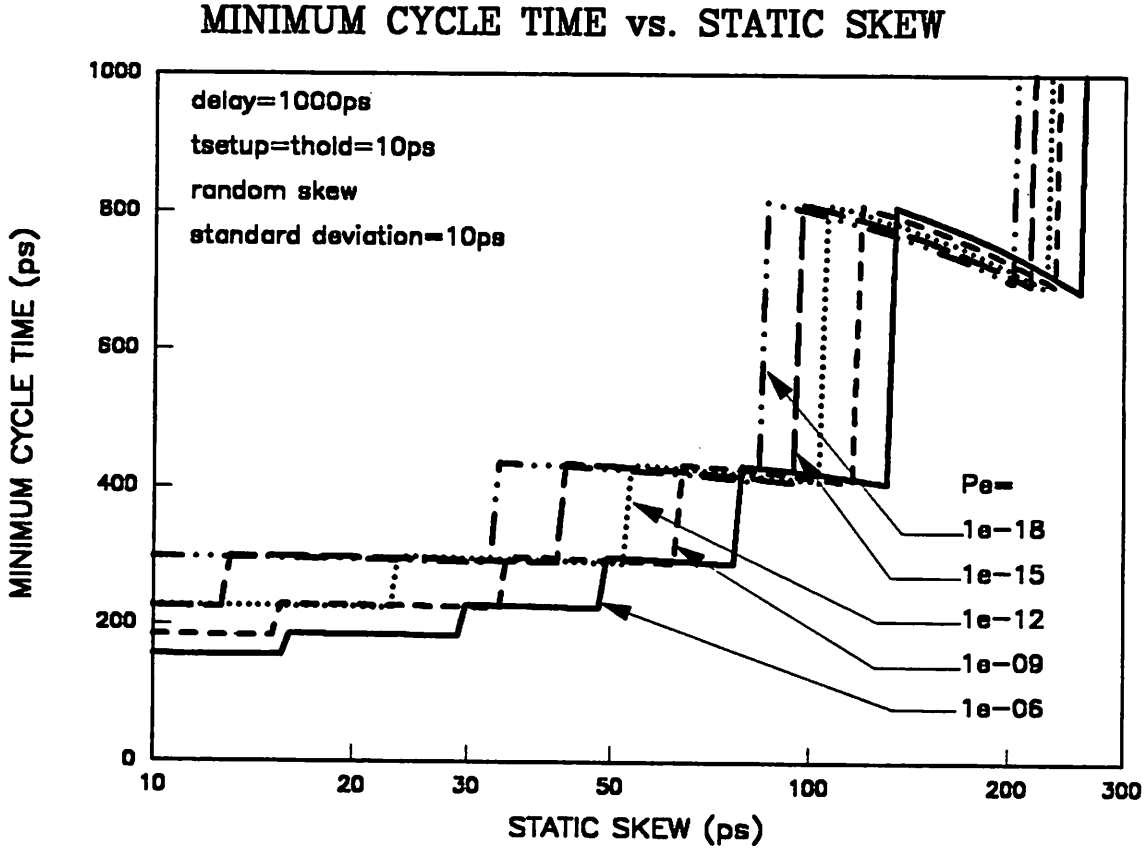

Figure 3-13. Minimum cycle time as a function of the standard deviation of the static skew for the aggressive design scheme. The system error rate is varied from 10^{-6} to 10^{-18}. Nominal propagation delay is 1000 ps. The static skew is kept at 60 ps, which corresponds to τ_{max} equals 1030 ps and τ_{min} equals 970 ps. Both of the t_{setup} and the t_{hold} are assumed to be 10 ps. The standard deviation of the random skew is assumed to be 10 ps.

3.7 Summary

A probabilistic timing skew model which accounts for both static and random timing skew is proposed in this chapter. Based on this model, the timing rules are derived for synchronous buses, finite state machines, and pipelined systems. Both the conservative and aggressive timing rules are analyzed. In the conservative timing rule, the system performance is limited by the absolute propagation delay as well as the random timing skew. On the other hand, an aggressive timing rule can yield a higher system performance but is limited by both of the static skew and random skew.

From this timing skew model, we have shown that the rise time of the clock as well as the data is critical in determining the performance of synchronous interconnections. Smaller rise time is desirable in minimizing the random timing skew due to the noise on the clock waveforms as well as the static skew due to the threshold uncertainty caused by device variations.

We have also shown that a digital system design using the conservative timing scheme is limited by its physical propagation delay and an interconnect technology capable of providing higher bandwidth does not help too much. On the other hand, the aggressive timing scheme can achieve a much smaller system cycle time and the existing interconnect technology becomes a serious bottleneck. Optical interconnect technology thus becomes very attractive for system designs using the aggressive timing scheme because its potential to offer much higher bandwidth and better performance.

CHAPTER 4 CLOCK DISTRIBUTION USING OPTICAL AMPLIFIERS

4.1 Introduction

Optimization of the performance of a high-speed synchronous digital system requires a tight control of the timing skew among system-level clock distribution network [48, 49].[9] It has been suggested in [42, 43] that optical clock distribution can be used to reduce the timing skew in a system-level clock distribution network. In a dense synchronous optical interconnect, optical clock distribution is essential for optimizing the system throughput, since clock distribution usually requires the highest bandwidth in a system. Compared with traditional electrical clock distribution, optical clock distribution has the potential of offering the following advantages:

- Higher bandwidth: The speed of an optical clock distribution network is only limited by the laser drivers and the optical receivers and is thus able to support clock waveforms with much smaller rise time.
- Lower distribution skew: The control of the refractive index in the optical fiber or optical waveguide is usually tighter as compared to that of the dielectric constant of the electrical transmission lines. The signals thus experience less variation in propagation delay among different branches in a clock distribution network [42, 43],
- Free from the capacitive loading effect: The fanout of an optical clock distribution network is determined by the minimum received power required by the optical receiver. In contrast, fanout of an electrical clock distribution network is determined by the driving capability of the line driver at the clock generator. A larger capacitive load thus requires a larger line driver, and increases the rise time.[10]

---

[9] A substantial portion of this chapter is from C.-S. Li, F. Tong, K. Liu, and D. G. Messerschmitt, "Fanout Analysis of Multi-Stage Optical Clock Distribution Using Optical Amplifiers," *Proc. GLOBECOM'91*, Phoenix, Dec. 1991. (c) 1991 IEEE. Reprinted with permission.

[10] In practical implementations, electrical clock distribution is usually implemented as a buffer chain [50] so that the clock driver need not to drive a big capacitive load directly. However, this architecture is limited by the timing skew introduced by the device tolerance among different buffers.

- Freedom from crosstalk: Electrical shielding from interfering sources becomes more difficult as the system operates at a higher speed, while optical clock distribution is immune to these electrical interferences.
- Freedom from the ground-loop problems: Optical clock distribution is immune to the unequal ground potential between different parts of a system as well as the electrical disturbance on the ground plane [51].[11]

Previously, optical clock distribution has been studied under the assumption that there is only a single-stage splitting of the clock waveform [42, 43, 52]. In this chapter, we investigate the maximum allowable number of fanout for a given skew budget when the optical amplifiers are introduced in the distribution. Our results are based on the semiconductor optical amplifiers (SOA) [53], but the analysis can be extended to incorporate Erbium-doped fiber amplifiers (EDFA) as well [54].

The results reported in this chapter are:

- An analytical skew model for a clock distribution network is developed and is applicable to both single-stage and multi-stage optical clock distribution.
- With the use of optical amplifiers, the fanout of a clock distribution network can increase many fold while maintaining the same clock skew.
- The maximum fanout of a clock distribution network is found to be very sensitive to the distribution skew introduced at each stage. The multi-stage architecture is no longer favorable when the distribution skew at each stage exceeds a few tenths of the total skew budget.
- In contrast to a single-stage architecture, the maximum fanout of a multi-stage architecture using optical amplifiers is not improved by using APD's.
- An optimal rise time of the clock waveform exists for both single- and multi-stage clock distribution.

[11] Ground loop problems can be avoided in the electrical domain if the clock signals are sent through fully differential lines.

The organization of this chapter is as follows: Section 2 describes the architecture for the single-stage and the multi-stage optical clock distribution network. The timing skew model for optical clock distribution is established in Section 3. Section 4 and Section 5 present the fanout analysis for the single-stage and the multi-stage optical clock distribution network, respectively. Section 6 present the experimental results based on a two-stage clock distribution network using an Erbium-doped optical amplifier. This chapter is summarized in Section 7.

4.2 Architecture of Clock Distribution Networks

The basic single-stage optical clock distribution network is shown in Figure 4-1. The clock distribution is achieved by equally splitting the output power from the laser into d branches. The clock signal is recovered from the optical receiver located at the end of each branch.

In order to increase the fanout as compared to that of a single-stage distribution, optical amplifiers can be used to boost the clock signal. The resulting architecture is shown in Figure 4-2, which is a tree with depth N, with each level allowing a different degree of fanout d_j. An optical amplifier is located at each nonleaf branch. Using this architecture, the total number of optical amplifiers required is $\sum_{i=0}^{N-1}\prod_{j=0}^{i} d_j$ while the total number of leaves is $\prod_{j=0}^{N} d_j$. We assume clock signals can only be recovered from the optical receivers located at the leaves of the distribution tree and tapping from nonleaf nodes is not allowed. In such a distribution tree, any clock signal arriving at the optical receiver has to travel through N stages of optical amplifiers.

One additional advantage of using a multi-stage clock distribution network with optical amplifiers is that the optical power in the system is always within eye-safety margin, as opposed to that of the single-stage distribution in which a high-power laser is required to achieve similar fanout.

4.3 Clock Skew Analysis

In a system-level electrical clock distribution network, the dominant skew components are:

- Mismatch of the propagation delay along different transmission lines, due to the mismatch of the terminating resistance as well as the line inductance and capacitance of the transmission lines.

- Discontinuities at the package boundary, such as those between the backplane and the board, as well as those between the board and the multi- or single-chip module.
- Variation of gate delay among clock buffers, due to the variation in the processing of the semiconductors.

In contrast, the dominant skew components in an optical clock distribution network are the distribution skew, the receiver static skew, and the receiver random skew.

Assuming the clock distribution architectures defined in the previous section are used, the timing skew at any receiver of such a network is defined as the deviation of the time instant from

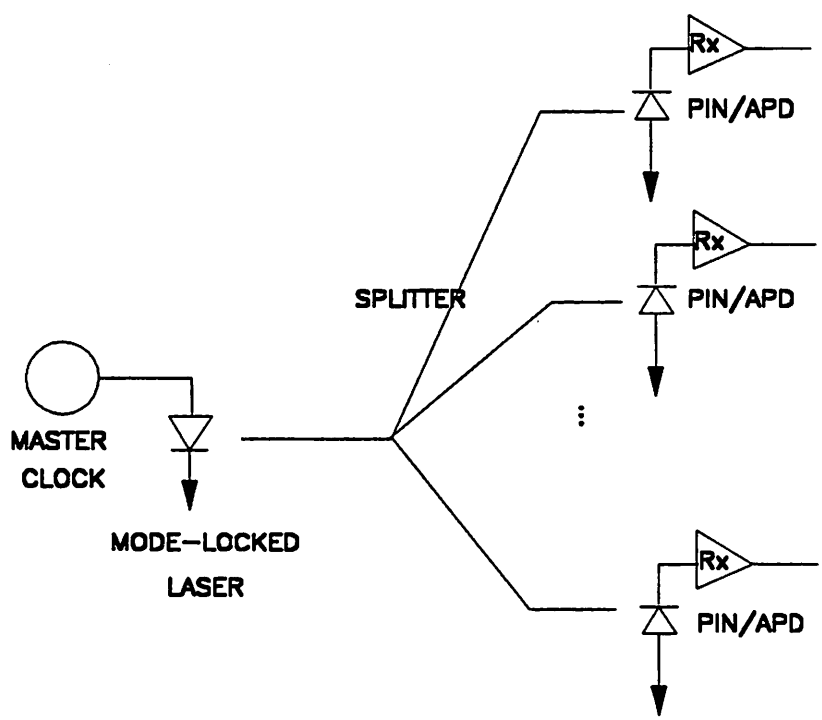

Figure 4-1. Architecture of a single-stage optical clock distribution.

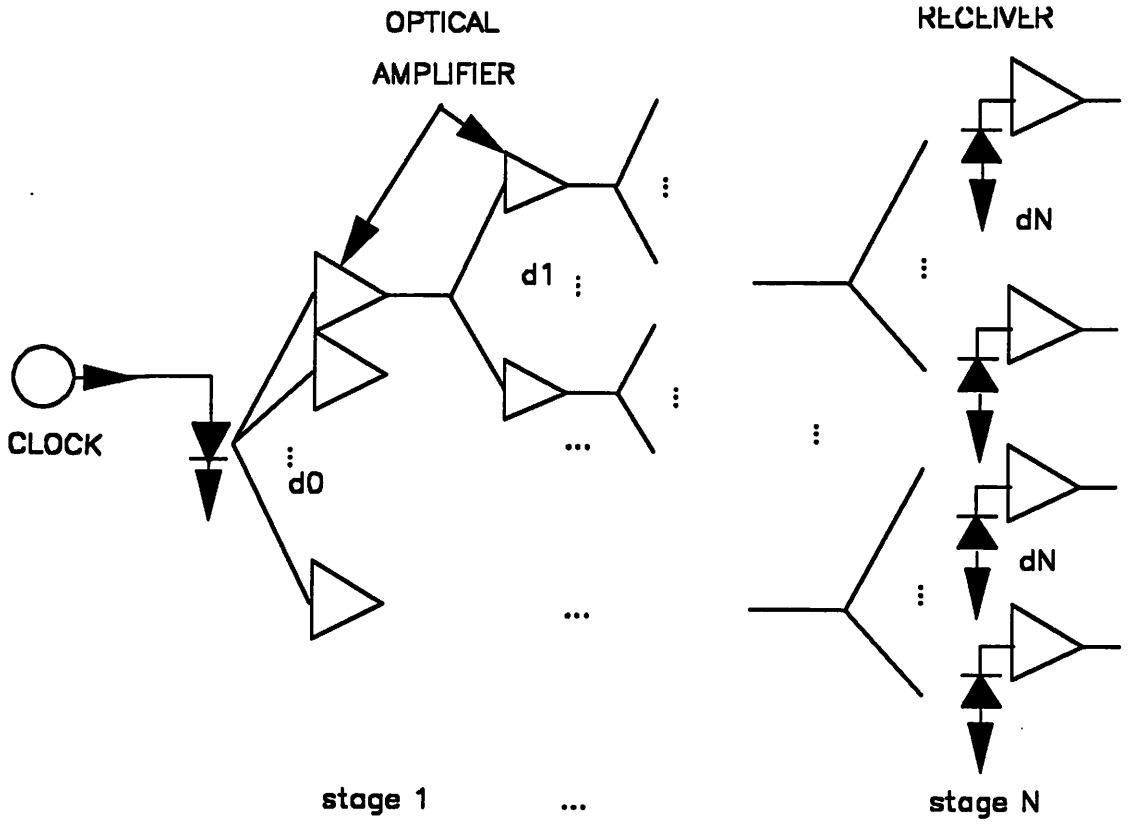

Figure 4-2. Architecture of a multi-stage optical clock distribution.

its nominal value at which the received clock signal triggers the latch operation. The total timing skew of an optical clock distribution network consists of three components:[12]

$$\tau_{skew} = \Delta\tau_{dist} + \Delta\tau_{rx,s} + \Delta\tau_{rx,r} \tag{4.1}$$

[12] The jitter generated by the clock source also contributes to the system timing skew if the receiver logic is using a different clock edge than the one used by the transmitter logic. However, this skew component is not contributed by the clock distribution network and is thus not considered in the present treatment.

where $\Delta\tau_{dist}$, $\Delta\tau_{rx,s}$, $\Delta\tau_{rx,r}$ are the random variables representing the distribution skew, the receiver static skew, and the receiver random skew, respectively. The variance of the total skew is thus given by

$$\sigma^2_{\tau_{skew}} = \sigma^2_{\Delta\tau_{dist}} + \sigma^2_{\Delta\tau_{rx,s}} + \sigma^2_{\Delta\tau_{rx,r}} \tag{4.2}$$

since we can safely assume that all these three random variables are independent of each other.

4.3.1 Distribution skew

Variation in propagation length and refractive index due to tolerance in the fabrication of the optical fiber or waveguides introduces distribution skew. The total propagation time through a segment of a distribution network is $\tau = ln/c$ where l and n are the nominal length and the nominal refractive index of a fiber/waveguide segment, respectively, while c is the speed of light. The timing skew due to the variation in propagation length and refractive index among different branches of a distribution network is thus given by $\Delta\tau/\tau = \Delta l/l + \Delta n/n$. When the clock signals have to propagate more than one segment of a distribution network, the total distribution skew then becomes

$$\Delta\tau_{dist} = \sum_{j=1}^{N} \tau_j \left(\frac{\Delta l_j}{l_j} + \frac{\Delta n_j}{n_j}\right) \tag{4.3}$$

where l_j, n_j, and τ_j represents correspondingly the nominal length, the nominal refractive index, and the nominal delay, while Δl_j, Δn_j, and $\Delta\tau_{dist}$ are the random variables representing variations of these parameters in the jth segment. The random deviations of all of the parameters from their nominal values are prefixed with Δ for the rest of this chapter. Assuming all of the Δl_j's and Δn_j's are mutually independent, the variance of the distribution skew equals

$$\sigma^2_{\Delta\tau_{dist}} = \sum_{j=1}^{N} \tau_j^2 \left(\frac{\sigma^2_{\Delta l_j}}{l_j^2} + \frac{\sigma^2_{\Delta n_j}}{n_j^2}\right) \tag{4.4}$$

where $\sigma^2_{\Delta l_j}$ and $\sigma^2_{\Delta n_j}$ are the corresponding variances for Δl_j and Δn_j. This is the case when the fiber or waveguide segments are fabricated independently. Furthermore, if the Δl_j's and Δn_j's are independent and have identical statistics, Eq.(4.4) reduces to

$$\sigma^2_{\Delta\tau_{dist}} = N\tau^2\left(\frac{\sigma^2_{\Delta l}}{l^2} + \frac{\sigma^2_{\Delta n}}{n^2}\right) \tag{4.5}$$

From this equation, we can observe that the variance of the total distribution skew is proportional to the number of stages in the network. As revealed in later sections, the maximum achievable fanout in a multi-stage distribution network could be significantly reduced due to this skew component.

4.3.2 Receiver static skew

Using the same definition of propagation delay in digital circuitry, the delay through an optical receiver can be defined as the interval between the 50% of the input transition point and the 50% of the output transition point. Based on [46, 55], we can derive the delay equation for an optical receiver, whose circuit design is independent of the number of stages in an optical clock distribution network. The delay is given by

$$\tau_{rx,s} = K_0\tau_F + \sum_{i=1}^{I}\sum_{j=1}^{J} K_{ij}R_iC_j \tag{4.6}$$

where R_i and C_j are various parasitic resistors and capacitors in a transistor, respectively, τ_F is the forward transit time of a transistor, and K_{ij} is the weighting factor of each R_iC_j. The parameters K_{ij} can be determined from circuit simulation of an optical receiver. Note that there is no power dependency in this formula because the receiver is assumed to have an output-limiting stage [56] such that the output of the receiver will be clamped at a constant voltage swing as long as the input power is within the dynamic range of the receiver. If the received power is below the dynamic

range, either the gain of the amplifier has to be increased (e.g. through the increase of the feedback resistance) or additional gain stages are needed. Both will increase the delay of the receiver.

For a particular receiver within an ensemble of receivers using the same fabrication process, the deviation in delay from its nominal value can be derived from Eq.(4.6):

$$\Delta\tau_{rx,s} = K_0\tau_F\frac{\Delta\tau_F}{\tau_F} + \sum_{i=1}^{I}\sum_{j=1}^{J}K_{ij}R_iC_j(\frac{\Delta R_i}{R_i} + \frac{\Delta C_j}{C_j}) \tag{4.7}$$

and the variance of the total receiver static skew is

$$\begin{aligned}\sigma^2_{\Delta\tau_{rx,s}} = {} & K_0^2\tau_F^2\frac{\sigma^2_{\Delta\tau_F}}{\tau_F^2} + \sum_{i=1}^{I}\sum_{j=1}^{J}K_{ij}^2R_i^2C_j^2(\frac{\sigma^2_{\Delta R_i}}{R_i^2} + \frac{\sigma^2_{\Delta C_j}}{C_j^2}) \\ & + K_0\tau_F\sum_{i=1}^{I}\sum_{j=1}^{J}K_{ij}R_iC_j(\rho_{\Delta\tau_F\Delta R_i}\frac{\sigma_{\Delta\tau_F}\sigma_{\Delta R_i}}{\tau_F R_i} + \rho_{\Delta\tau_F\Delta C_j}\frac{\sigma_{\Delta\tau_F}\sigma_{\Delta C_j}}{\tau_F C_j}) \\ & + \sum_{i=1}^{I}\sum_{j=1}^{J}\sum_{k=1}^{I}\sum_{l=1}^{J}K_{ij}K_{kl}R_iR_kC_jC_l(\frac{\rho_{\Delta R_i\Delta R_k}\sigma_{\Delta R_i}\sigma_{\Delta R_k}}{R_iR_k} + \frac{\rho_{\Delta C_j\Delta C_l}\sigma_{\Delta C_j}\sigma_{\Delta C_l}}{C_jC_l} + \\ & \frac{\rho_{\Delta R_i\Delta C_l}\sigma_{\Delta R_i}\sigma_{\Delta C_l}}{R_iC_l} + \frac{\rho_{\Delta R_k\Delta C_j}\sigma_{\Delta R_k}\sigma_{\Delta C_j}}{R_kC_j})\end{aligned} \tag{4.8}$$

where ρ_{XY} is the correlation coefficient between the random variables X and Y. The cross-correlations among $\Delta\tau_F$, ΔR_i and ΔC_j are caused by the variation in the same set of parameters in semiconductor processing such as the dopant concentration.

Since the receiver static skew is independent of the number of stages in an optical clock distribution network, the receiver static skew will be treated as a constant for the rest of this chapter.

4.3.3 Receiver random skew

In order to determine the receiver random skew, the sampling process of the data signal in a flip-flop has to be considered. Here we assume the output of the receiver is connected to a CMOS flip-flop, whose operation relies on the activation and coupling of a sample module and two re-

generation loops, as shown in Figure 4-3 [57]. The downward transition of the inverted clock signals close the CMOS transmission gate in the sample module while the delayed non-inverted clock signals open the transmission gate in the regenerative loop 1. After this transmission gate is opened, the flip-flop becomes autonomous and the voltage retained at the instant when this transmission gate is opened is regenerated by the regeneration loops to either a logical ONE or a logical ZERO. Therefore the effective sampling time is determined by the instant that the clock signal amplitude reaches the threshold of the transmission gate. When the signal-to-noise ratio of the clock signal is high, the clock signal is unlikely to cross the threshold more than once and the sampling instant is uniquely determined by this threshold crossing instant. On the other hand, it

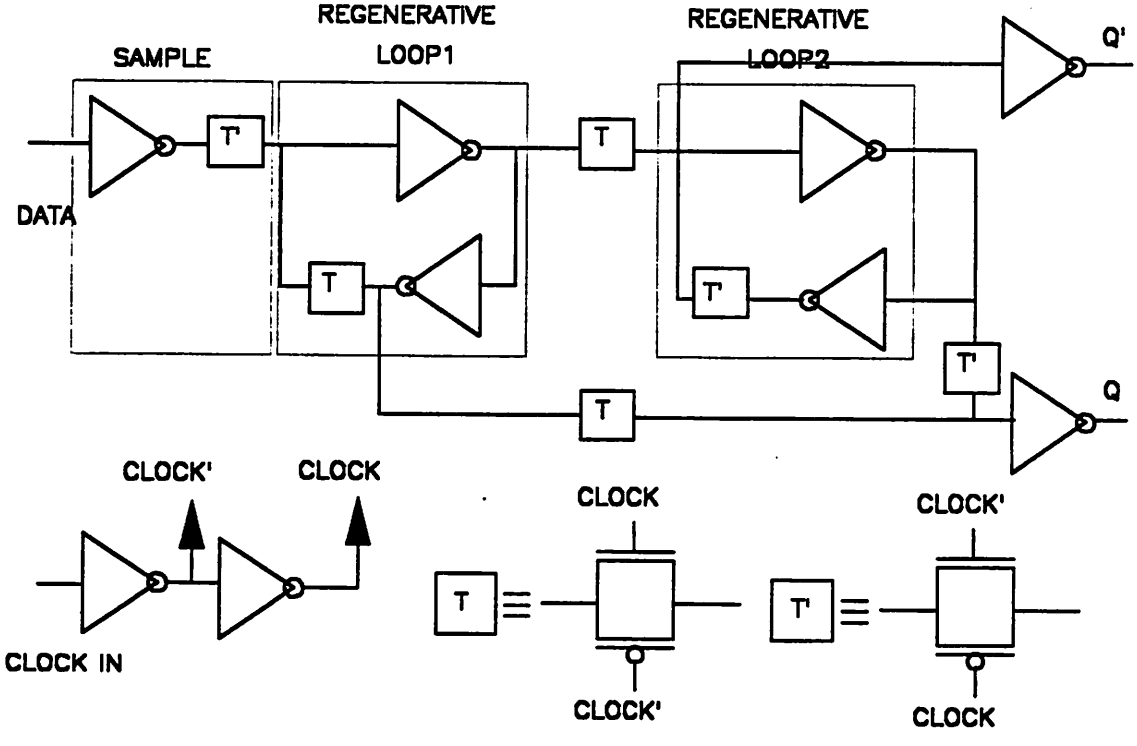

Figure 4-3. Circuit schematic of a typical CMOS flip-flop.

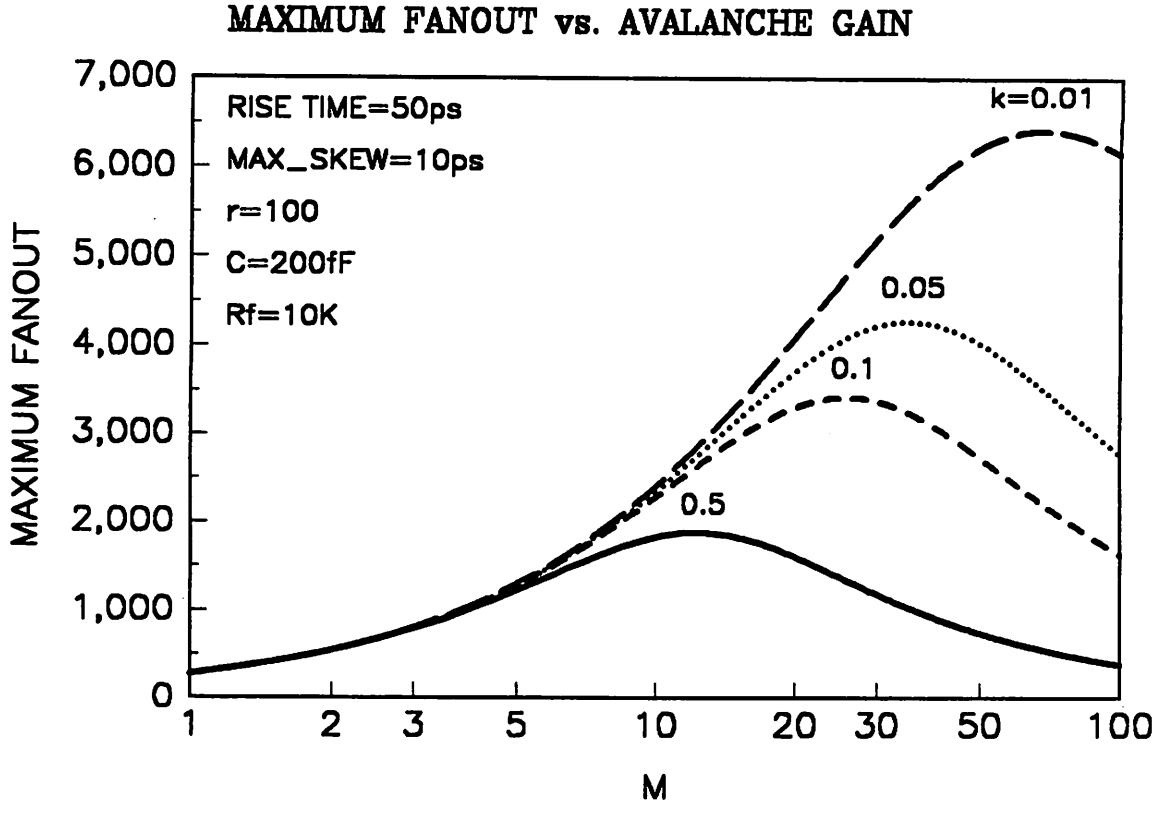

Figure 4-4. Maximum fanout as a function of avalanche gain for various ionization factor.

is probable that there is more than one threshold crossing instant if the signal-to-noise ratio of the clock signal is low. The effective sampling instant of the data will then depend on the details of the interactions between the sampling module and the regeneration loops. In the CMOS flip-flop structure shown in Figure 4-3 [57], each positive threshold crossing causes a new sampling of the input data and thus only the last threshold crossing within a clock cycle determines the effective data sampling instant.[13]

[13] The sampling process could become more complicated if the sample module of a flip-flop displays hysteresis behavior in the sampling process in which two thresholds are involved. In this case, the effective sampling instant would be the last upward transition through the higher threshold within a clock cycle given that there is a downward transition through the lower threshold previously.

Here we assume an idealistic latch model and a high signal-to-noise ratio such that the sampling instants are solely determined by a single threshold crossing instant. The standard deviation of the random timing skew of the optical clock signal will then be determined by the noise at that particular instant. It has been shown in [42, 43] that this deviation is

$$\frac{\sigma_{\Delta\tau_{rx,r}}}{T_b} = \frac{t_r/T_b}{\sqrt{SNR}} \tag{4.9}$$

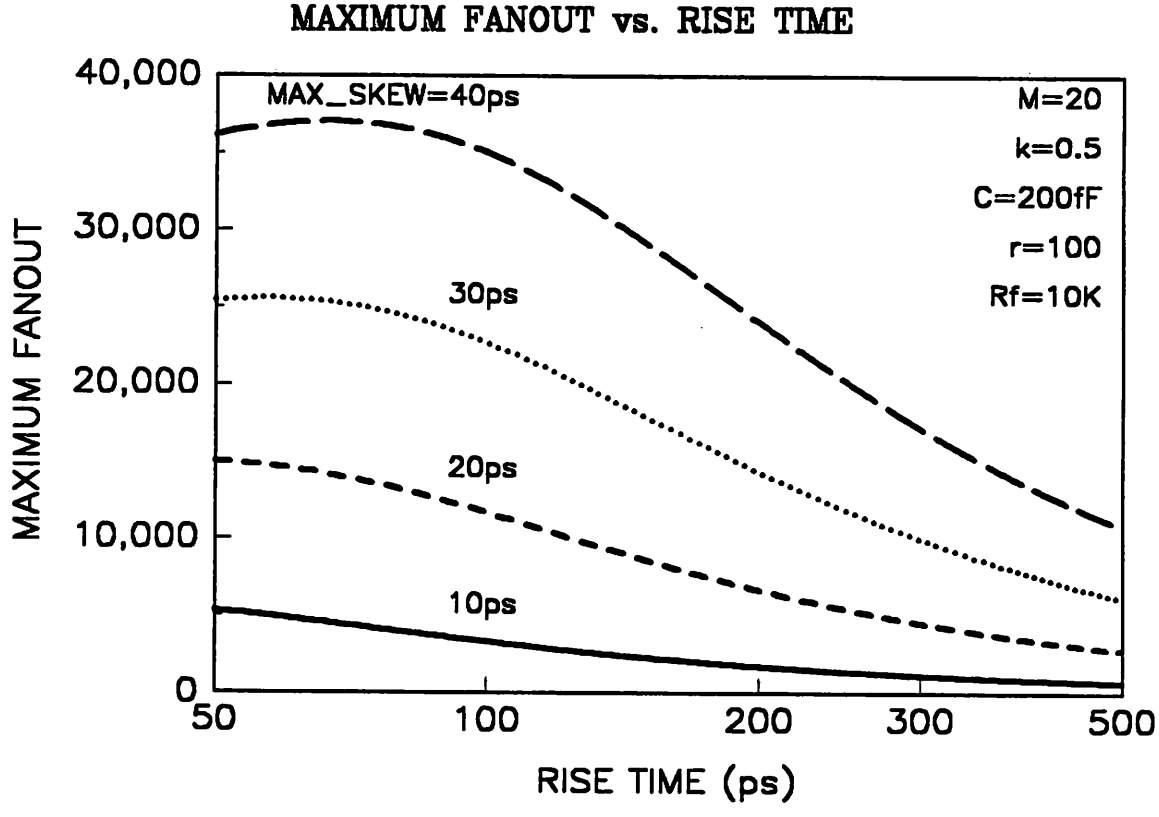

Figure 4-5. Maximum fanout of a single-stage clock distribution network. Maximum fanout as a function of the clock rise time for various receiver random skew budget.

where T_b is the clock interval, SNR is defined as the signal-to-noise ratio of the clock signal at the sampling point, and t_r is the 10% to 90% rise time of the clock waveform. This rise time is related to the electrical bandwidth by $B_e = b_f/t_r$ where b_f is a waveshape dependent factor with values between 0.1 and 1. Equation (4.9) can then be rewritten as

$$\sigma_{\Delta\tau_{rx,f}} = \frac{b_f}{B_e\sqrt{SNR}} \tag{4.10}$$

4.4 Maximum Fanout of a Single-Stage Clock Distribution Network

In this section, we examine the maximum fanout of a single-stage clock distribution system as set by the maximum allowable clock skew budget. If the output power from the laser is P_{LD}, the average optical power arriving at the receiver is thus given by $P_{rx} = P_{LD}L/d$ where L is the loss of each branch in addition to the splitting such as the fiber or waveguide connector loss, d of the distribution network. Assuming a transimpedance receiver is used, it is shown in Appendix A that the signal-to-noise ratio of the clock signal for a single-stage clock distribution system at the sampling instant is given by

$$\sqrt{SNR} = 2M\eta e\frac{P_{rx}}{h\nu}\frac{r-1}{r+1}\frac{R_F}{\sqrt{N_T}} \tag{4.11}$$

where M is the avalanche gain, e is the electron charge, η is the quantum efficiency of the photodetector, h is the Planck's constant, ν is the optical frequency, r is the extinction ratio of the optical clock signal defined as the ratio between the power of signal ONE and that of the signal ZERO, R_F is the feedback resistance used in the receiver, and $\sqrt{N_T}$ is the total noise voltage. The parameter $\sigma^2_{\Delta\tau_{rx,f}}$ can be considered independently of the other skew sources since there is only one stage of fanout and both of the $\sigma^2_{\Delta\tau_{dist}}$ and the $\sigma^2_{\Delta\tau_{rx,s}}$ are constant. For a given maximum allowable timing skew tolerance $\sigma_{skew,max}$, the minimum required received optical power is

$$P_{rx,min} = \frac{b_f}{B_e \sigma_{\Delta\tau_{rx,r,max}}} \frac{\sqrt{N_T}}{R_F} \frac{r+1}{r-1} \frac{h\nu}{2M\eta e} \tag{4.12}$$

where $\sigma^2_{\Delta\tau_{rx,r,max}} = \sigma^2_{\tau_{skew,max}} - \sigma^2_{\Delta\tau_{dist}} - \sigma^2_{\Delta\tau_{rx,s}}$. The maximum fanout which can be supported by a single-stage clock distribution network thus equals

$$d_{\max} = \frac{P_{LD} L}{P_{rx,min}} \tag{4.13}$$

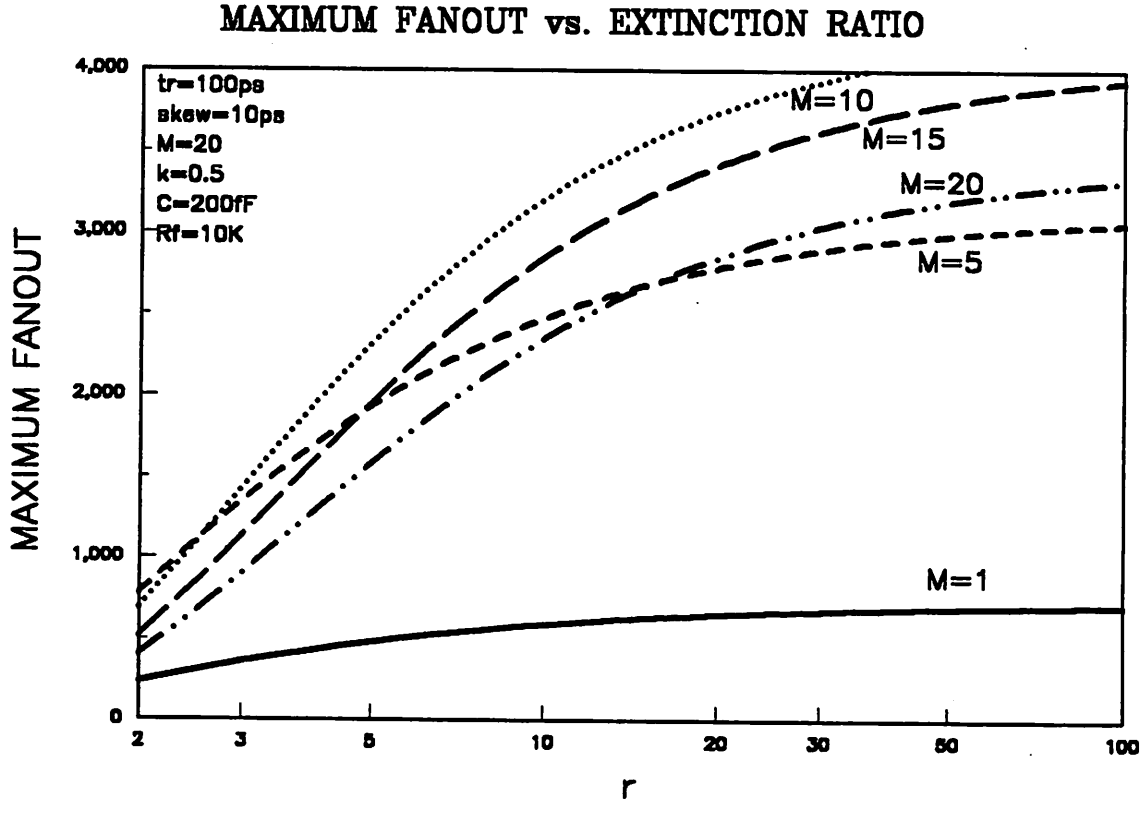

Figure 4-6. Maximum fanout as a function of extinction ratio for various values of avalanche gain.

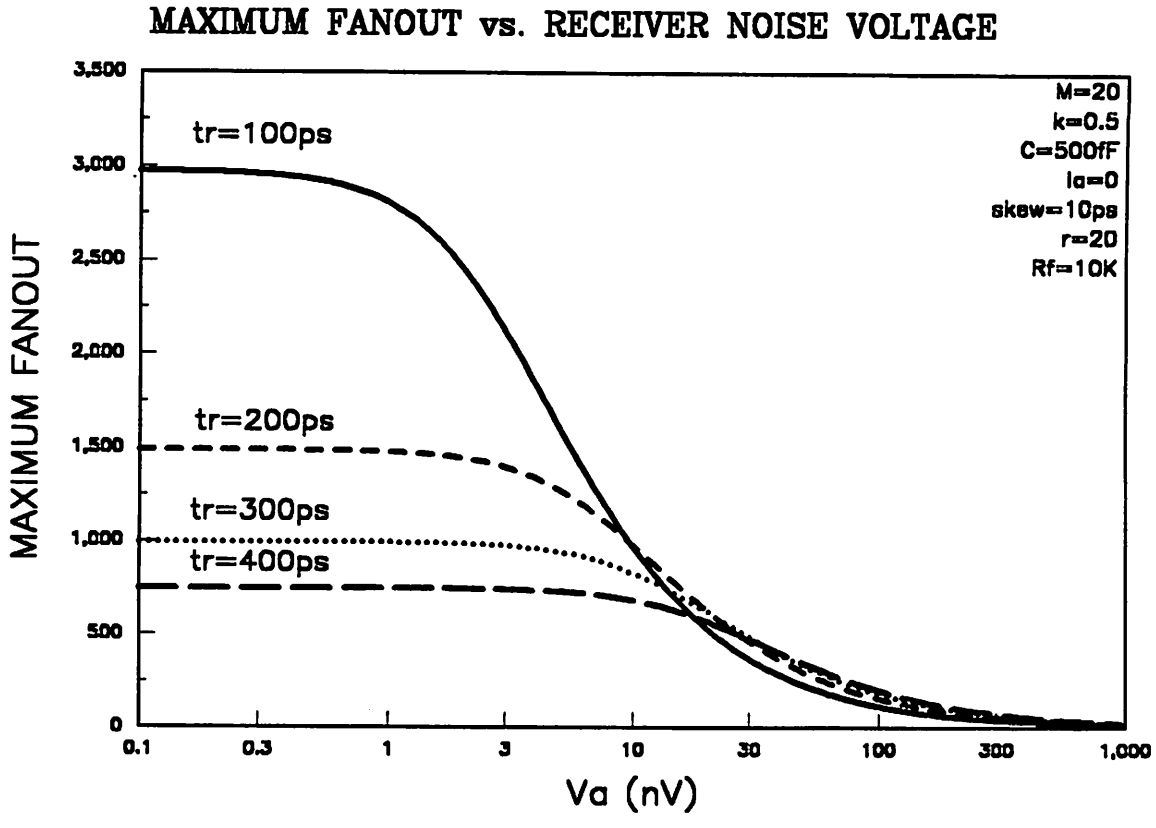

Figure 4-7. Maximum fanout as a function of receiver voltage noise for various values of clock rise time.

The required received power can be obtained by substituting Eq.(4.25) into Eq.(4.12), yielding the following quadratic equation:

$$AP_{rx,min}^2 + BP_{rx,min} + D = 0 \tag{4.14}$$

where

$$A = B_e \frac{\sigma^2_{\Delta\tau_{rx,r,max}}}{b_f^2} \left(\frac{r-1}{r+1}\right)^2 \left(\frac{2M\eta e}{h\nu}\right)^2 \tag{4.15}$$

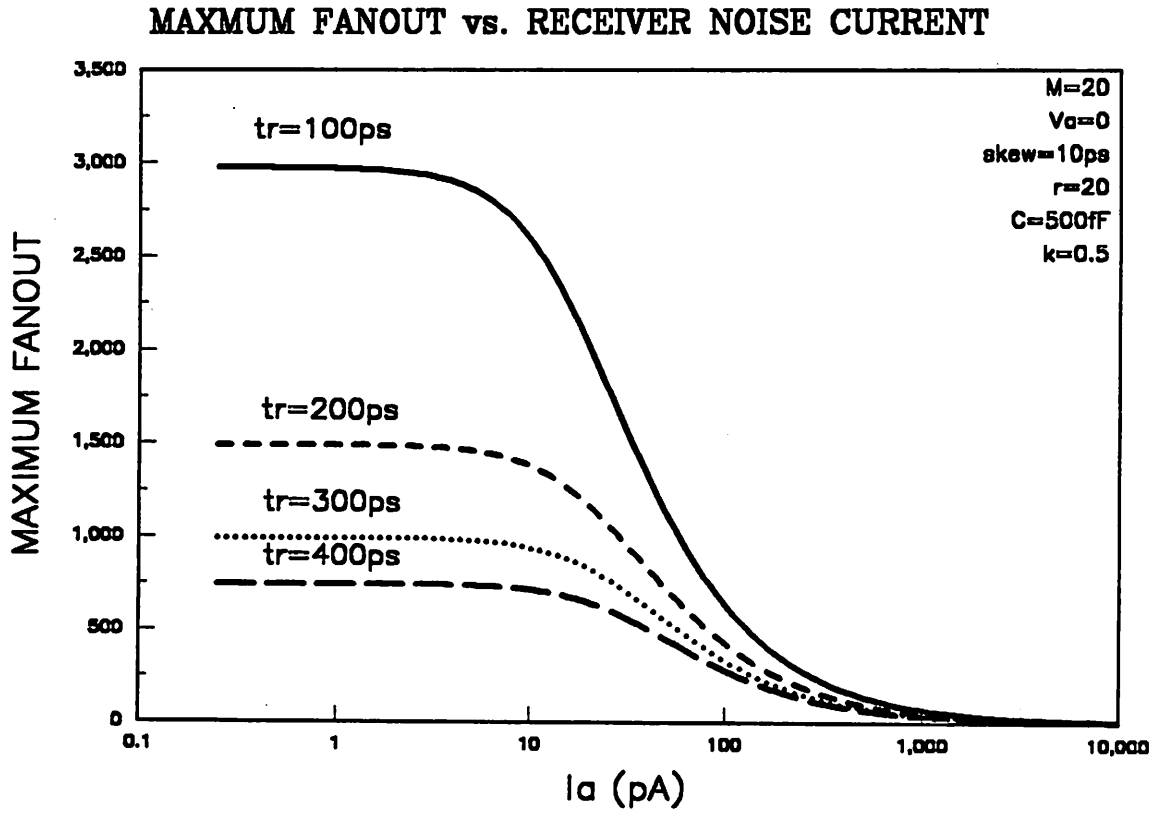

Figure 4-8. Maximum fanout as a function of receiver current noise for various values of clock rise time.

$$B = \frac{2e^2M^2F}{h\nu} \tag{4.16}$$

$$D = ((\frac{1}{R_F} + \frac{1}{R})^2 + \frac{4}{3}\pi^2B_e^2C^2)V_A^2 + 4kT(\frac{1}{R_F} + \frac{1}{R}) + I_A^2 \tag{4.17}$$

In these expressions, R and C are the receiver input resistance and capacitance, including the loading capacitance added by the photodetector. The parameters V_A^2 and I_A^2 are the receiver noise voltage spectral density and receiver noise current spectral density (see Table I).

The dynamic range requirement for this distribution architecture is moderate compared to a multi-stage distribution architecture. The only factor that could contribute to the received power variation is the variation of the branch loss L. The dynamic range requirement for the receiver thus equals $P_{LD}\Delta L/d_{max}$ in order to accommodate the possible received power variations among different branches, where ΔL is the maximum mismatch of the branch loss among different branches in a distribution network. In practice, the total mismatch of the connector loss and the fiber/waveguide loss is expected to be less than 5 dB, which results in a very moderate dynamic range requirement.

Figure 4-5 shows the maximum fanout as a function of the clock rise time for various values of receiver random skew budget, using an avalanche photodiode with gain $M = 20$ as the detector. Depending on the allowable random skew budget, the maximum fanout could reach as many as several tens of thousands. As indicated in this figure, there clearly exists an optimal clock rise time that maximizes the fanout. This can be understood as follows. From Eq.(4.12) and Eq.(4.13), the maximum fanout is inversely proportional to $P_{rx,min}$, and is therefore proportional to $B_e/\sqrt{N_T}$. From Eq.(4.25), the total noise N_T is proportional to $aB_e^3 + bB_e$, where a represents the contribution from the receiver voltage noise and b represents the contribution from other noise sources. The solution to the equation $\partial(B_e/\sqrt{N_T})/\partial B_e = 0$ gives the optimal electrical bandwidth $\sqrt{b/a}$, which in turn yields the optimal rise time $b/\sqrt{b/a}$. In other words, a decrease in clock rise time (or an increase in electrical bandwidth) allows more receiver voltage noise and reduces the benefits from reducing the noise sensitivity. Varying the avalanche gain M, the maximum fanout is plotted in Figure 4-4 for various ionization factor γ. As expected, smaller γ gives larger maximum fanout. Although an increase in the avalanche gain increases the signal power, there is also a simultaneous increase in the excess noise generated by the avalanche photodiode, and eventually reduces the maximum fanout for a given skew budget. The maximum fanout is also plotted as a function of the extinction ratio of the clock signal in Figure 4-6 for various values of M assuming γ is fixed at 0.5. The effect on the fanout from increased extinction ratio diminishes as the extinction ratio increases above 10. Figure 4-7 and Figure 4-8 show the influence of the maximum fanout by the noise voltage and noise current in the receiver. There is an apparent threshold behavior in the noise voltage and current, limiting V_a to be less than 10 $nV/\sqrt{Hz}$ and I_a to be less than 50 $pA/\sqrt{Hz}$. The results obtained show that a fanout of several thousand can be supported in a single-stage

optical clock distribution network when combined with an avalanche photodiode in the receiver, assuming a maximum random skew budget of $\simeq$ 20 ps.

M	avalanche gain of an APD	1 ~ 100
η	quantum efficiency of PIN/APD	1.0
F	excess noise factor of an APD	
γ	ionization factor of an APD	0.01 ~ 0.5
ν	optical frequency	1.935×10^{14}Hz (1.55 μm)
T	temperature	300 °K
r	extinction ratio	2 ~ 100
R_F	feedback resistance	10KΩ
R	receiver input resistance	40KΩ
C	receiver input capacitance	0.2 pF
V_A	amplifier noise voltage	$2nV/\sqrt{Hz}$
I_A	amplifier noise current	$2pA/\sqrt{Hz}$
t_r	rise time of the clock	50 ~ 500 ps
B_o	optical bandwidth	10 ~ 3000 Å
B_e	electrical bandwidth	0.78 ~ 7.8 GHz
b_f	wave shape factor	0.39
P_{sat}	internal amplifier saturation power	8.5 dBm
N_{sp}	spontaneous emission factor	1.4(SOA), 2.5(EDFA)
G_o	small signal amplifier gain	20dB
$\eta_{in(out)}$	input (output) coupling efficiency	0.31(0.27)

TABLE I. A SUMMARY OF THE IMPORTANT PARAMETERS AND THEIR VALUES USED IN THE CALCULATIONS.

4.5 Maximum Fanout For Multistage Distribution Network

Although the number of stages can be increased with the use of optical amplifiers in a multi-stage architecture, there will be an increase in the noise and in the distribution skew. In particular, the accumulated noise power may saturate the optical amplifier even in the absence of the clock signals. It is therefore important to estimate the accumulated amplifier noise in such an architecture employing a long chain of amplifiers.

4.5.1 Modeling of multi-stage amplifier chain

For a given input optical power $P_{amp,in}$ to the amplifier with gain G, the output optical power $P_{amp,out}$ is $GP_{amp,in}$. The amplifier gain, however, can be influenced by the input optical power through the following implicit function [58]:

$$P_{amp,in} = \frac{P_{sat}}{G - 1} \ln \frac{G_o}{G} \tag{4.18}$$

where P_{sat} is the internal saturation power and G_o is the small signal gain of the amplifier. The internal saturation power can directly be related to the output saturation power by $P_{sat,out} = P_{sat} \ln 2/(1 - \frac{2}{G_o})$, at which the amplifier gain G is decreased by 3 dB from G_o.

By tracing a signal path from root to any leaf in the clock distribution network shown in Figure 4-2, the signal power at the input of the receiver after N stages of amplification and $N + 1$ stages of splitting is

$$P_{rx} = P_{LD} \frac{L_0}{d_0} \prod_{i=0}^{N} \frac{\eta_{in} G_i \eta_{out} L_i}{d_i} \tag{4.19}$$

while the accumulated spontaneous emission power generated by the optical amplifier chain is

$$P_{sp} = \sum_{i=1}^{N} \frac{P_{sp,i}}{G_i \eta_{in}} \prod_{j=i}^{N} \frac{L_j \eta_{in} G_j \eta_{out}}{d_j} \tag{4.20}$$

The parameter $P_{sp,i}$ is the spontaneous emission generated at the ith optical amplifier, L_j is the loss of the jth distribution stage in addition to the splitting d_j, and N is the distribution depth or the number of levels of the clock distribution network. From [59], the spontaneous emission power generated at the output of an optical amplifier is equal to

$$P_{sp} = (G - 1) N_{sp} B_o h\nu \tag{4.21}$$

where N_{sp} is the spontaneous emission factor of the optical amplifier, and B_o is the optical bandwidth. Equation (4.21) can thus be expressed as

$$P_{sp} = N_{sp} B_o h\nu \sum_{i=1}^{N} (1 - \frac{1}{G_i}) \frac{1}{\eta_{in}} \prod_{j=i}^{N} \frac{L_j \eta_{in} G_j \eta_{out}}{d_j} \tag{4.22}$$

In general, each of the G_j and the d_j could be optimized individually to maximize the splitting.

The dynamic range required by a receiver in multi-stage distribution is larger than that of the single-stage distribution, and can be derived from Eq.(4.19):

$$\frac{\Delta P_{rx}}{P_{rx}} = \frac{\Delta L_0}{L_0} + \sum_{i=0}^{N} (\frac{\Delta \eta_{in}}{\eta_{in}} + \frac{\Delta G_i}{G_i} + \frac{\Delta \eta_{out}}{\eta_{out}} + \frac{\Delta L_i}{L_i}) \tag{4.23}$$

The received power variation should not exceed the dynamic range of the receiver, which has a typical value of 20 dB [56].

4.5.2 Maximum fanout calculation

The nonlinearity in amplifier gain requires a numerical method to obtain the maximum fanout for the the multi-stage distribution. An algorithm for searching the architecture that optimizes the fanout is described as follows:

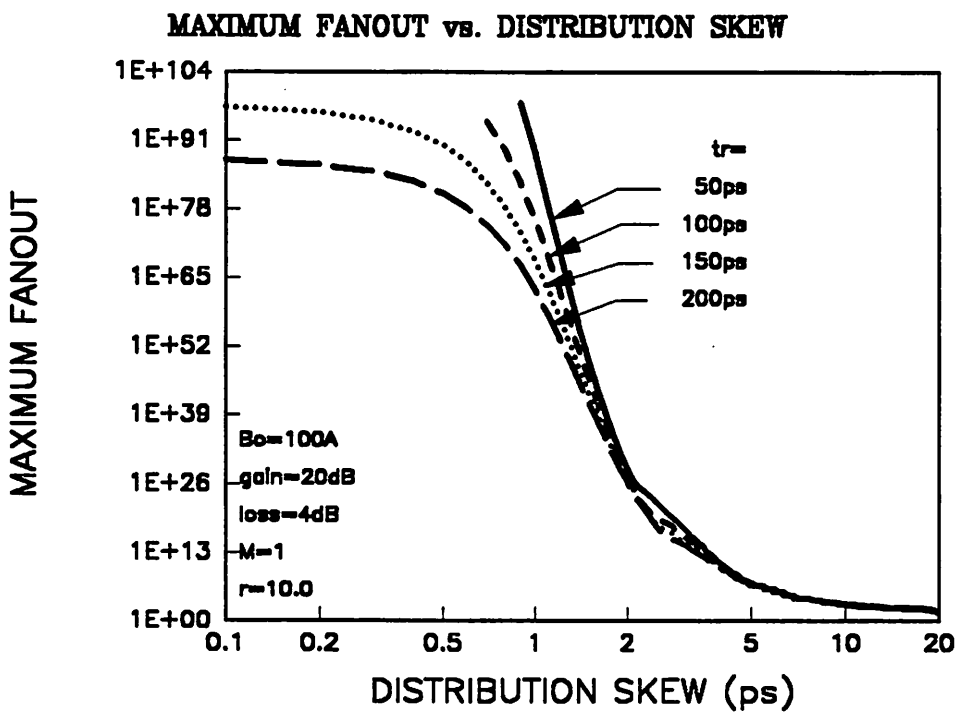

Figure 4-9. Maximum fanout as a function of distribution skew for various clock rise time.

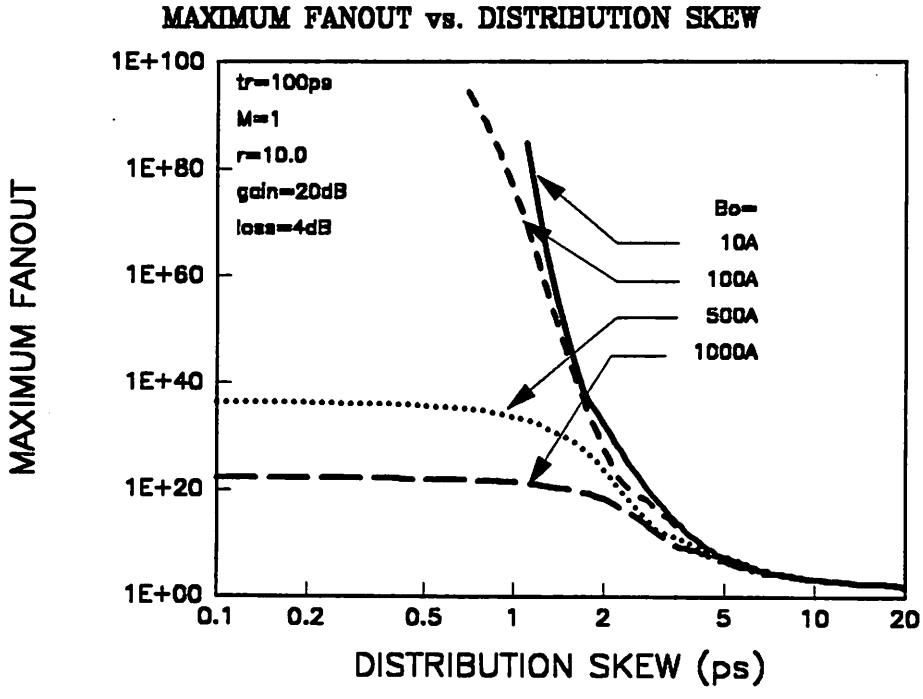

Figure 4-10. Maximum fanout is plotted against distribution skew for various values of optical filter bandwidth.

ALGORITHM A. MAXIMUM FANOUT CALCULATION:

(1) $N := 0$, $d_0 := 1$, *look_ahead*: $= 0$,

(2) Calculate $FANOUT_N := \prod_{j=0}^{N} d_j$ allowed by $\sigma_{skew,max}$.

(3) if $FANOUT_N > FANOUT_{N-1}$, *look_ahead*: $= 0$, $FANOUT_{max} = FANOUT_N$, else *look_ahead*: $=$ *look_ahead* $+ 1$,

(4) if *look_ahead* $>$ *look_ahead_max*, exit.

(5) $N := N + 1$, $FANOUT_{N-1} := FANOUT_N$, go to (2).

Due to the nonconvexity of the solution space $(d_0, d_1, ..., d_N)$, a parameter *look_ahead* is provided in steps (3) and (4) of the algorithm to search the neighborhood of the possible optimal N. By adjusting the parameter *look_ahead_max*, it is possible to define the diameter of the searching area surrounding the optimal N. With *look_ahead_max* = 0, the algorithm exits at the moment when an increase in N no longer improves the maximum fanout. In this chapter, the parameter *look_ahead_max* has been set to 150. An unconstrained search of the optimal $(d_0, d_1, ..., d_N)$ is not feasible due to the excessively large number of degrees of freedom. Consequently, we consider only the special case in which the splitting at each stage is identical.

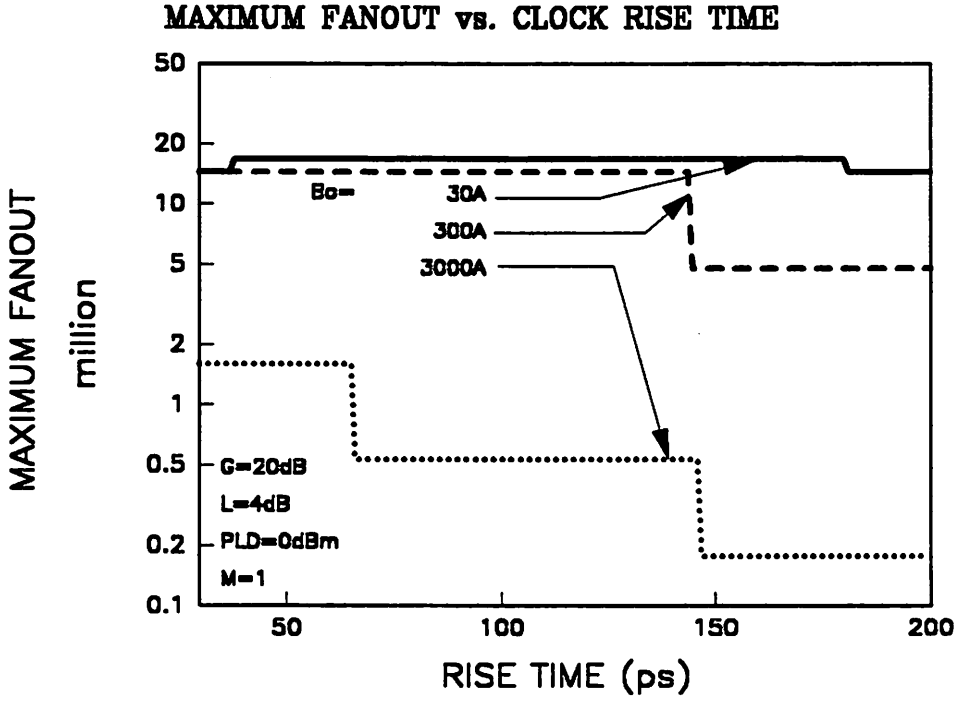

Figure 4-11. Maximum fanout as a function of clock rise time for various optical filter bandwidths.

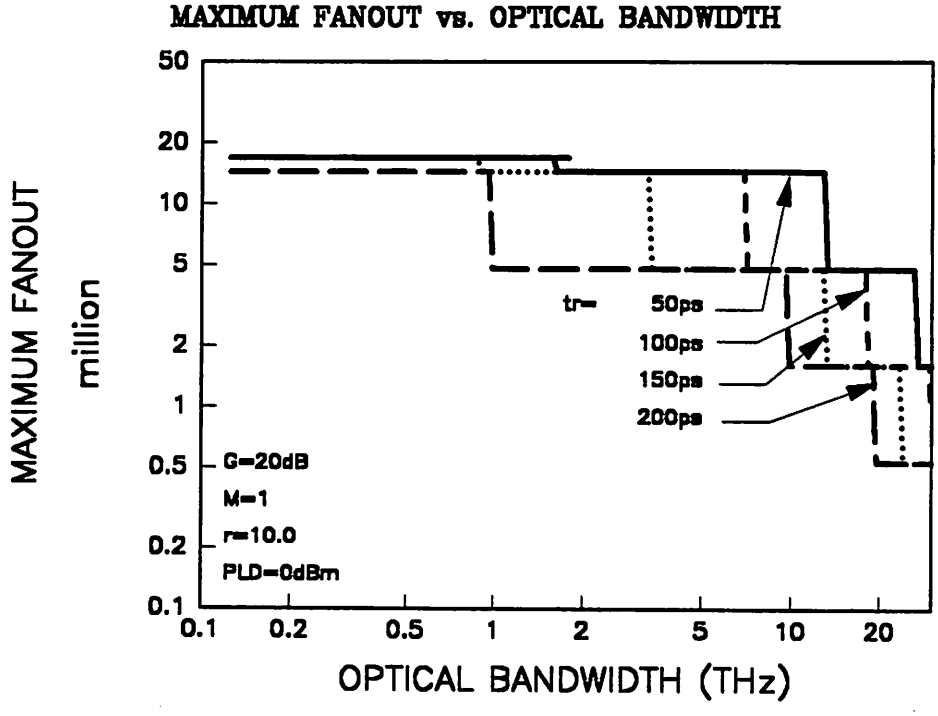

Figure 4-12. Maximum fanout vs. optical filter bandwidth for various clock rise time.

In this case, both the splitting and amplifier gain are maintained constant throughout the whole distribution network. That is, we assume

$$\begin{aligned} d_0 &= d_1 = \ldots = d_N = d \\ G_{o,1} &= G_{o,2} = \ldots = G_{o,N} = G_o \end{aligned} \tag{4.24}$$

Using the signal-to-noise ratio calculation formula developed in Appendix B, it becomes straightforward to calculate $d_{max,N}$ in step (2) of Algorithm A:

ALGORITHM B. MAXIMUM SPLITTING/STAGE CALCULATION

(1) $d = 2$,

(2) calculate the skew incurred by $(d_0, d_1, ..., d_N) = (d, d, ..., d)$

(3) if skew $\geq \sigma_{skew,max}$, $d = d - 1$, exit.

(4) $d = d + 1$, go to (2).

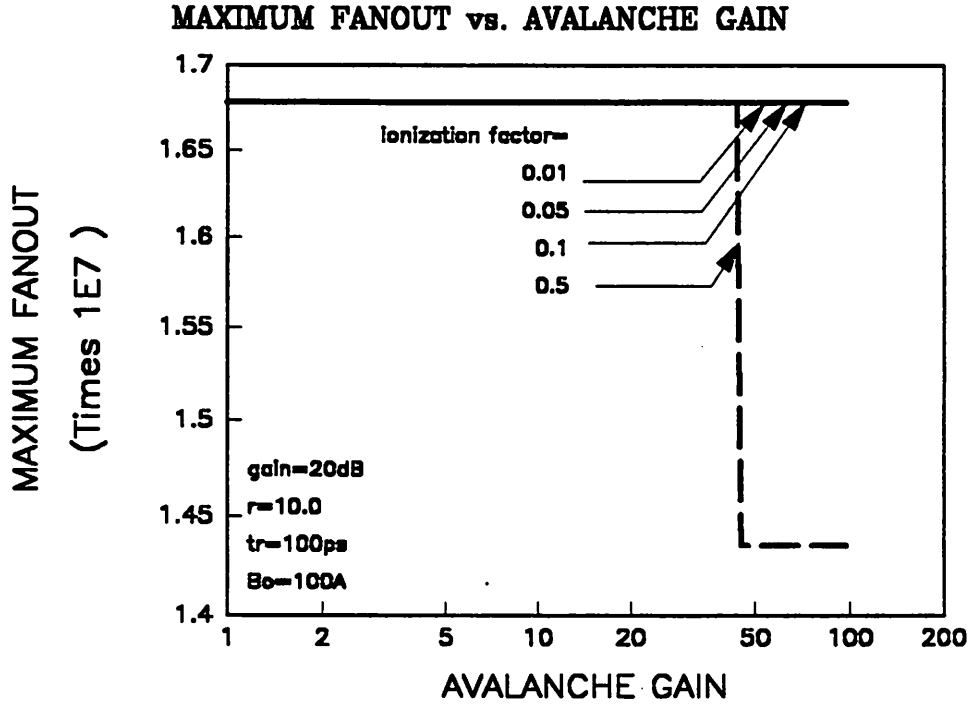

Figure 4-13. Maximum fanout as a function of avalanche gain for various values of ionization factor.

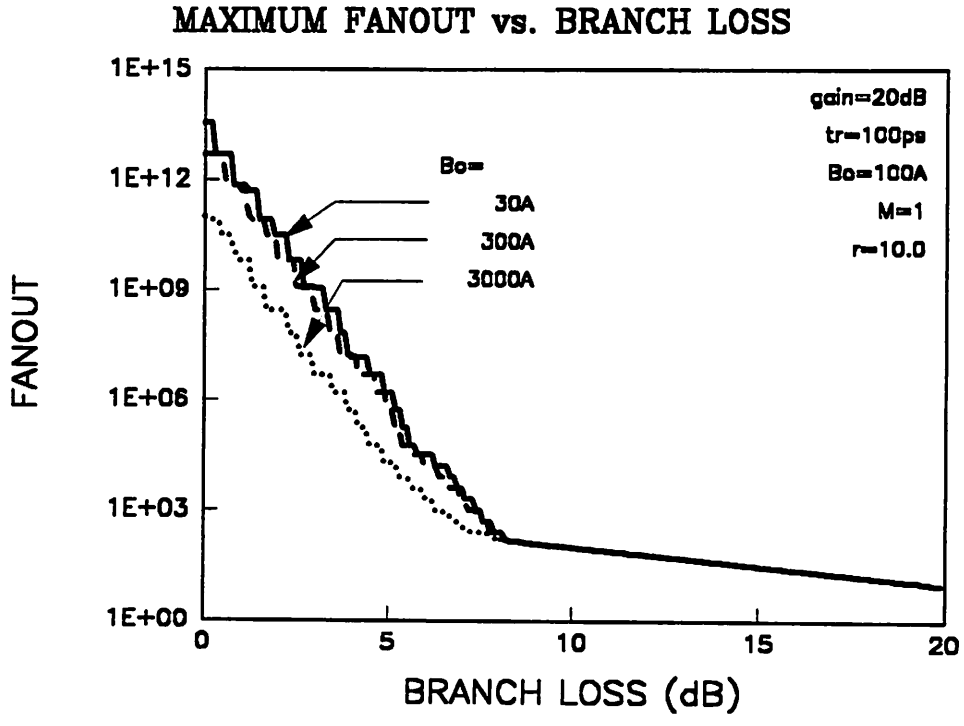

Figure 4-14. Maximum fanout as a function of branch loss for various optical filter bandwidths.

Because of equal splitting at each stage, the solution is a staircase function as the fanout in each stage is increased. Although this architecture is suboptimal, it has the advantage of having a homogeneous structure which in principle has less implementation cost.

In a multi-stage clock distribution network, the distribution skew can no longer be treated independent of the receiver random skew, as in the single-stage case. The effect of the distribution skew on the maximum fanout is displayed in Figure 4-9 for various values of rise time and in Figure 4-10 for various values of optical filter bandwidths. In either Figure 4-9 or Figure 4-10, there is a steep decrease in the maximum fanout as the distribution skew increases from 0.5 ps to 5 ps. Figure 4-11 shows the maximum fanout as a function of the clock rise time for various optical filter bandwidths. For a larger optical filter bandwidth, the maximum fanout decreases faster

as the rise time increases, since more optical amplifier noise is allowed to accumulate at each stage. Similar to the single-stage case, there exists an optimal rise time $b_f/\sqrt{b/a}$ that maximizes the fanout. Note that the parameter b includes an additional noise contribution from the amplifier. An increase in the optical filter bandwidth allows more amplifier noise and a decrease in the optimal rise time is expected. Figure 4-12 shows the sensitivity of the maximum fanout to the optical filter bandwidth for various values of clock rise time. The maximum fanout sharply decreases at an optical bandwidth between 1 and 20 THz. It is therefore important to include an optical filter after each amplifier stage to reduce the spontaneous noise passed to subsequent stages. Figure 4-13 shows the maximum fanout as a function of avalanche photodiode gain. In contrast to the single-stage

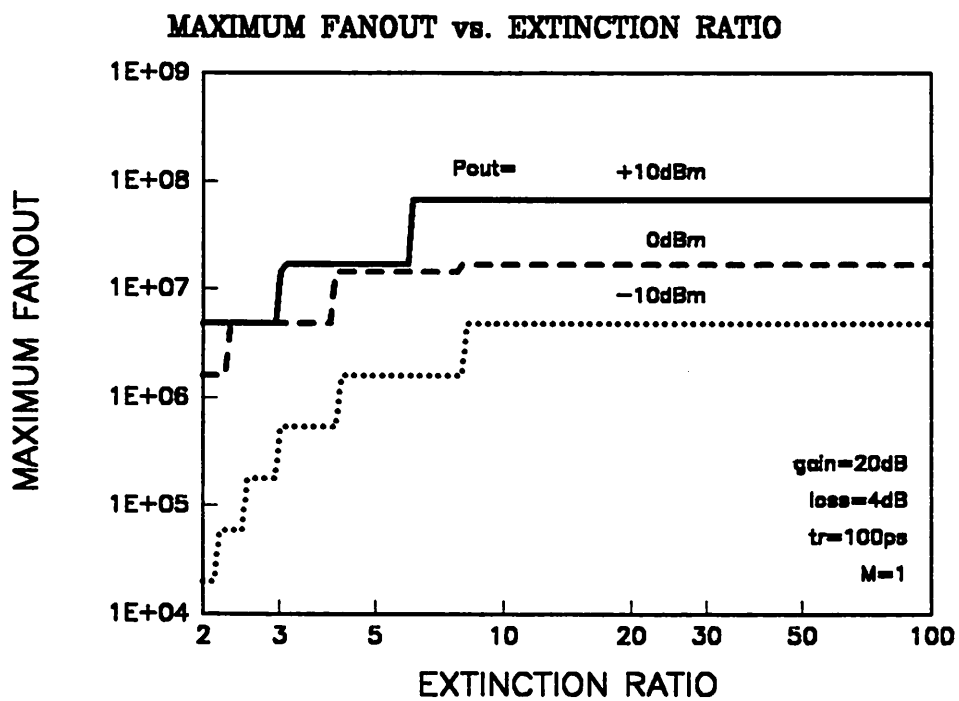

Figure 4-15. Maximum fanout as a function of extinction ratio of the clock signal for various values of laser output power.

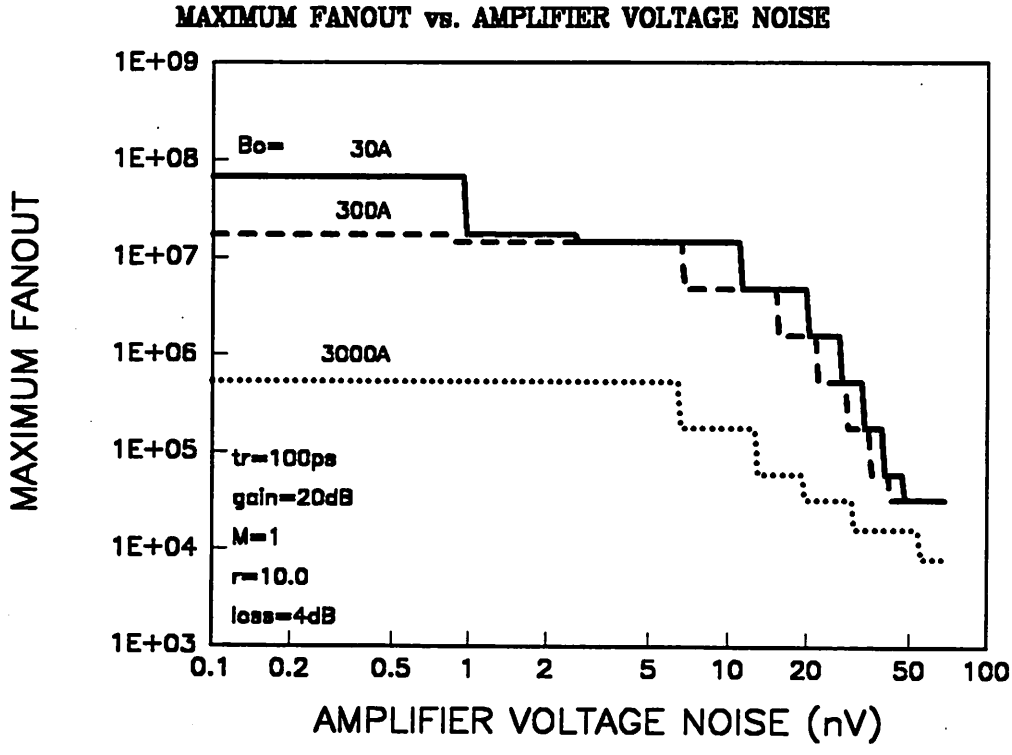

Figure 4-16. Maximum fanout vs. receiver voltage noise for various optical filter bandwidth.

case, the avalanche gain at various values of ionization factor does not improve the maximum fanout due to the simultaneous amplification of the signal and the optical amplifier noise. The fanout decreases monotonically as M increases for large γ due to the excess noise generation associated with the avalanche process (see Eq.(4.23)). The influence of the optical amplifier gain on the maximum fanout is plotted in Figure 4-17 for different values of B_o. A minimum of 15 dB gain is necessary in order to overcome the loss incurred by the splitting and the coupling loss. In Figure 4-14, the maximum fanout is plotted against the excess loss in each distribution stage, L. In increasing L, the maximum fanout decreases monotonically until L reaches $\simeq$ 8 dB, in which case the single-stage architecture is more preferable. The maximum fanout is plotted against the

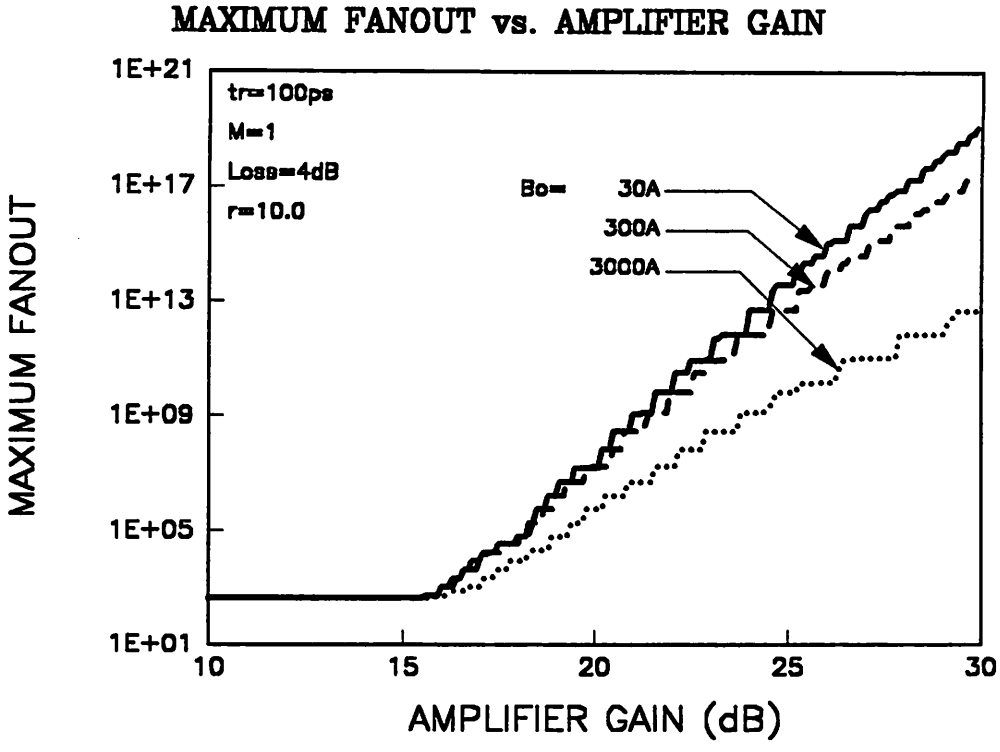

Figure 4-17. Maximum fanout as a function of amplifier gain for various optical filter bandwidths.

extinction ratio in Figure 4-15. As the extinction ratio of the clock signal improves beyond $\simeq$ 10, there is no increase in the maximum fanout. Similar to the single-stage case, the maximum fanout is evaluated as a function of amplifier voltage noise in the receiver in Figure 4-16. The value of V_a is limited to $\simeq 2\ nV/\sqrt{Hz}$ in order to avoid a steep decrease in the fanout.

4.6 Experimental Results

A system experiment is performed to verify the validity of the random skew calculation in a multi-stage clock distribution system using optical amplifiers. In this experiment, an optical amplifier is placed between two stages of splitting, as shown in Figure 4-18, in order to emulate a

two-stage optical clock distribution network. An N −stage clock distribution with equal splitting at each stage can be emulated by a ring consisting of an attenuator, an optical amplifier and a photonic switch. The clock signals at the output of the emulated distribution system are obtained by switching the ring into a closed loop in order for the clock signals to circulate the loop and switch the loop open at the end of the N^{th} circulation. However, a two-stage clock distribution experiment is sufficient to verify the relationship between the random skew and the number of splitting at each stage.

Experimental measurements are made on the root-mean-square (rms) values of the timing jitter at the output of the optical receiver. This is equivalent to measuring the variance of the receiver

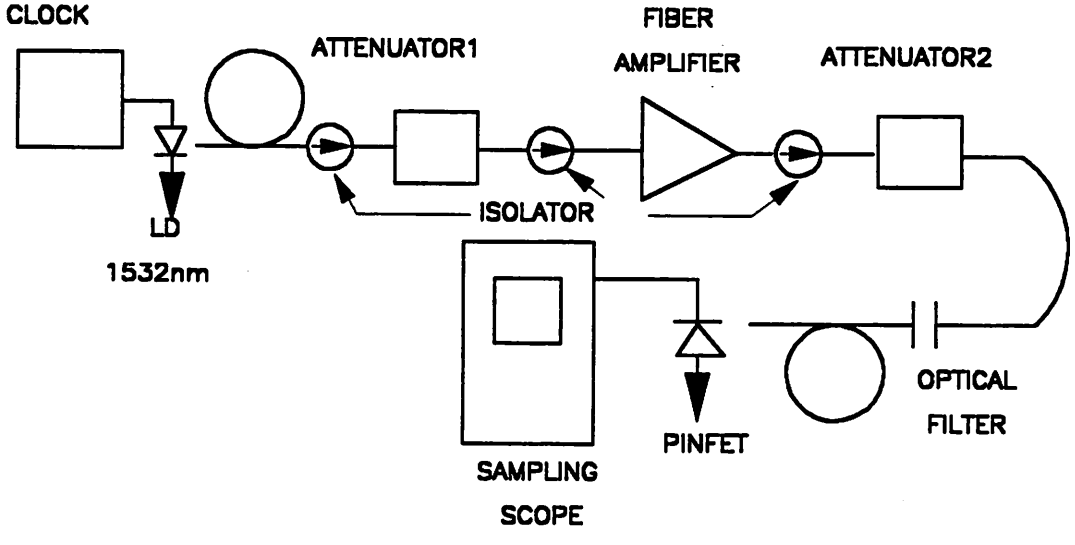

Figure 4-18. Schematic of the clock distribution experiment setup.

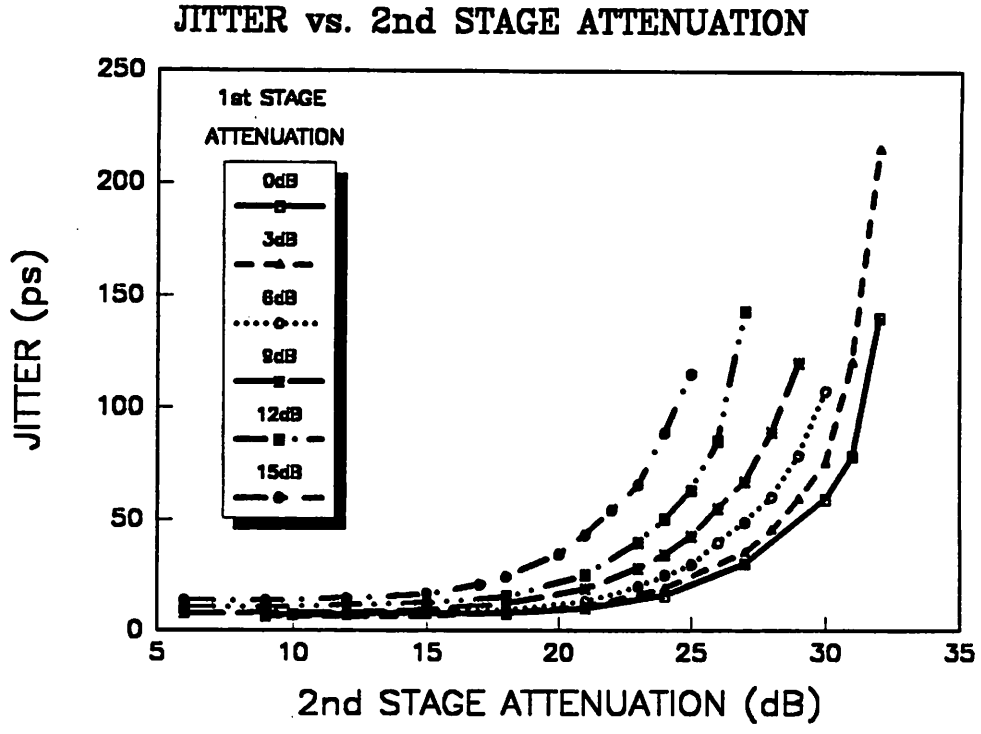

Figure 4-19. Jitter as a function of second-stage splitting. Root-Mean-Square values of jitter are measured as a function of the second-stage splitting for various values of first-stage splitting.

random skew among N receivers, assuming the input noise process is either stationary or cyclostationary.

The clock signal generated by a word generator is used to modulate a distributed feedback laser diode emitting at 1532 nm. The resulting extinction ratio of the optical clock signal is kept at 10 throughout the experiment. The 10%–90% rise time of the clock signal is 550 ps. The optical amplifier is a commercial Er-doped fiber amplifier (BT&D Model EFA 3000) with pump current set at 350 mA. The amplifier gain for various values of average input power is measured to range from 10 dB to 23 dB, corresponding to the power into the optical amplifier from −7.9 dBm to −32.9 dBm, respectively. Variable optical attenuators are used to emulate the splitting loss at each

stage and are placed before and after the optical amplifier. The RMS value of the clock timing jitter is then measured as a function of the amount of attenuation in the two splitting stages. Polarization-independent isolators, each with 30 dB isolation, are used to reduce the optical reflection back to the laser transmitter and the amplifier. A 6 dB improvement in splitting was obtained by introducing an isolator between the laser and the receiver. An optical filter with a passband of 3.5 nm is placed immediately before the receiver in order to reduce the spontaneous noise generated by the amplifier. The loss from the output of the amplifier to the input of the receiver due to fixed losses of the attenuator, the isolator, and the filter is estimated to be 4.5 dB.

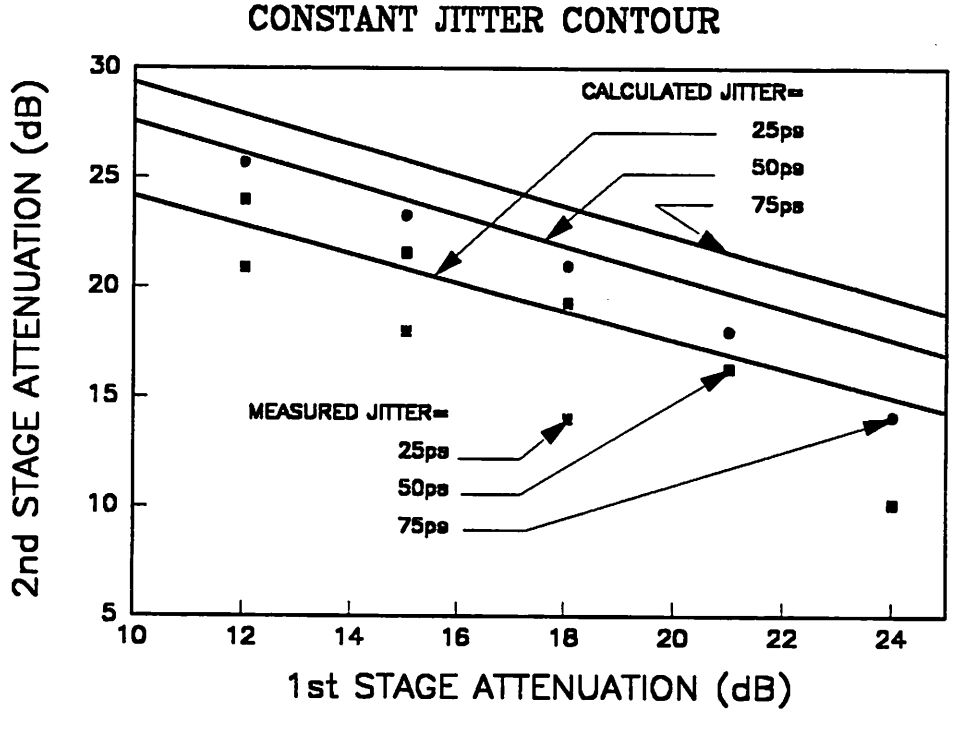

Figure 4-20. Comparison of experimental and calculated constant rms jitter contour.

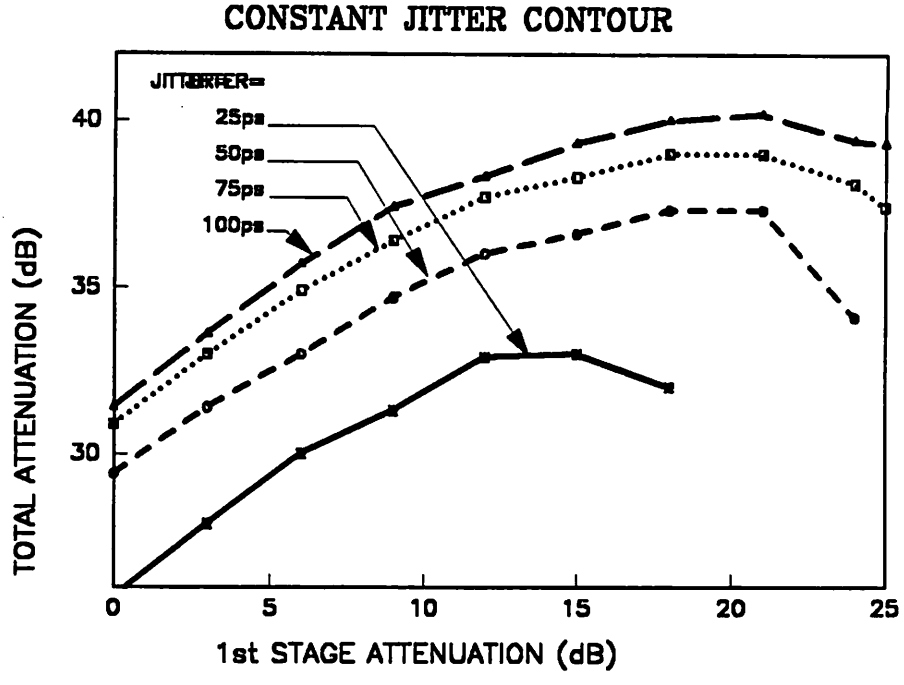

Figure 4-21. Total attenuation is plotted against the first stage attenuation for various values of constant rms jitter.

The receiver is a pin-FET receiver which is designed for 2.4 Gbps NRZ data. The nominal sensitivity of the receiver is −29 dBm.

A typical data set is plotted in Figure 4-19, showing the measured rms values of the timing jitter as a function of the splitting loss in the second stage d_1 for various values of the splitting loss in the first stage d_0. Splitting loss has been defined as 10 log d. The data show two distinct regimes: a thermal-noise-dominated regime at high attenuation and an amplifier-noise-dominated regime at low attenuation. The major component of the amplifier noise that causes the jitter floor is the signal-spontaneous beat noise, since a significant amount of the spontaneous-spontaneous beat noise has already been removed by the optical filter. For the same reason, an increase in d_0 raises

the jitter floor in the amplifier-noise-dominated regime. At high second stage attenuation, the receiver thermal noise becomes dominant and the jitter increases rapidly with attenuation.

The calculated constant-jitter contours are overlayed in Figure 4-20 with the measured data. A good match between the experimental data and the calculated data indicates the validity of the skew model for $N = 1$. The total splitting loss (i.e., $10 \log d_0 + 10 \log d_1$) is plotted against the first stage splitting d_0 in Figure 4-21. The maximum total splitting is found to be 33 dB, equivalent to a splitting of $\simeq 2000$, for a constant rms timing jitter of 25 ps at $10 \log d_0 = 12$ dB. If a larger jitter budget is allowed, the optimum splitting favors more d_0 than d_1.

4.7 Summary

An analytical skew model for optical clock distribution has been developed in this chapter. Using this model, we evaluated, compared, and set out the design parameters for the maximum fanout of the single-stage as well as a suboptimal multi-stage clock distribution network for a given skew budget. We found that a multi-stage clock distribution network using optical amplifiers can result in several orders of magnitude more fanout than single-stage distribution, assuming a reasonable distribution skew can be maintained. We also observed that:

- The fanout is extremely sensitive to the distribution skew in a multi-stage distribution network.
- Single-stage splitting using an APD as photodetector is more desirable than using a PIN, while multi-stage splitting favors a PIN.
- An optimal clock rise time exists for both single-stage and multi-stage splitting.
- An optimal avalanche gain exists for single-stage splitting.

Appendix A. SNR Calculation for Single-Stage Clock Distribution

In this appendix, we are going to evaluate possible noise sources in an single-stage optical clock distribution system. We assume a transimpedance configured receiver [60] is used in this derivation. For a single-stage clock distribution network, the total noise at the output of the receiver is given by [60]:

$$N_T = \left[\left((1 + \frac{R_F}{R})^2 + \frac{4}{3}\pi^2 B_e^2 C^2 R_F^2 \right) V_A^2 + R_F^2 \left(\frac{4kT}{R} + I_A^2 + 2eM^2 F i_s \right) + 4kTR_F \right] B_e \quad (4.25)$$

where B_e is the electrical bandwidth, V_A and I_A are the equivalent input noise voltage and current of the receiver amplifier, M and F are the avalanche gain and excess noise factor of an APD, respectively. F is a function of M and the ionization factor γ of the avalanche photodetector. When the multiplication is initiated by electrons, it has been shown in [61]:

$$F = M\left[1 - (1 - \gamma)\left(1 - \frac{1}{M}\right)^2\right] \quad (4.26)$$

Both M and F in Eq.(4.25) are equal to one for a PIN photodetector. The clock signal levels, i_s for ONE and ZERO are

$$i_{s,ONE} = M\eta e P_{rx} \frac{2r}{h\nu(r + 1)} \quad (4.27)$$

$$i_{s,ZERO} = M\eta e P_{rx} \frac{2}{h\nu(r + 1)} \quad (4.28)$$

The signal level at the sampling instant, assuming the data is sampled at 50% point of the clock, is thus given by

$$i_{s,sample} = \frac{M\eta e P_{rx}}{h\nu} \quad (4.29)$$

The signal-to-noise ratio at the sampling instant thus equals:

$$\sqrt{SNR} = \frac{(i_{s,ONE} - i_{s,ZERO})R_F}{\sqrt{N_T}} \tag{4.30}$$

Substituting eq. (4.27) and (4.28) into (4.30), we have

$$\sqrt{SNR} = 2M\eta e \frac{P_{rx}}{h\nu} \frac{r-1}{r+1} \frac{R_F}{\sqrt{N_T}} \tag{4.31}$$

Appendix B. SNR Calculation for Multi-stage Clock Distribution

The signal-to-noise ratio for a multi-stage clock distribution system is evaluated in this appendix. The total equivalent noise current introduced by N stages of in-line optical amplifiers is [53]:

$$i_{\text{amp}}^2 = i_{shot}^2 + i_{s\text{-}sp}^2 + i_{sp\text{-}sp}^2 \tag{4.32}$$

where the *shot noise*, i_{shot}, contributed by the signal as well as the spontaneous emission of the amplifier, is given by

$$i_{shot}^2 = 2eM^2F(i_s + i_{sp}) \tag{4.33}$$

the *signal-spontaneous beat noise*, $i_{s\text{-}sp}$, is given by

$$i_{s\text{-}sp}^2 = 4M^2 i_s i_{sp} \frac{1}{B_o} \tag{4.34}$$

and the *spontaneous-spontaneous beat noise*, $i_{sp\text{-}sp}$, is given by

$$i_{sp\text{-}sp}^2 = M^2 i_{sp}^2 \frac{2B_o - B_e}{B_o^2} \tag{4.35}$$

The photo current equivalent of the spontaneous emission power is:

$$i_{sp} = N_{sp} e B_o \sum_{l=1}^{N} (1 - \frac{1}{G_l}) \frac{1}{\eta_{in}} \prod_{j=l}^{N} \frac{L_j \eta_{in} G_j \eta_{out}}{d_j} \tag{4.36}$$

where N_{sp} is the spontaneous emission factor, G_j is the gain of the optical amplifier, η_{in} and η_{out} are the input and output efficiency of the optical amplifier, respectively.

The received signal current after the square-law photodetector is

$$i_s = i_{LD} \frac{L_0}{d_0} \prod_{l=1}^{N} \frac{\eta_{in} G_l \eta_{out} L_l}{d_l} \tag{4.37}$$

where the photo current equivalent clock signal levels for the ONE and the ZERO at the laser output are

$$i_{LD,ONE} = e\eta P_{LD} \frac{2r}{h\nu(r + 1)} \tag{4.38}$$

$$i_{LD,ZERO} = e\eta P_{LD} \frac{2}{h\nu(r + 1)} \tag{4.39}$$

The clock signal levels at the sampling point, assuming the data is sampled at 50% point of the clock, is thus given by

$$i_{LD,sample} = \frac{e\eta P_{LD}}{h\nu} \tag{4.40}$$

With the use of a transimpedance configured receiver, the total noise power at the output of the receiver is

$$N_T = \left[\left((1 + \frac{R_F}{R})^2 + \frac{4}{3}\pi^2 B_e^2 C^2 R_F^2 \right) V_A^2 + R_F^2 \left(\frac{4kT}{R} + I_A^2 + i_{amp}^2 \right) + 4kTR_F \right] B_e \tag{4.41}$$

The signal-to-noise ratio at the sampling instant is thus given by:

$$\sqrt{SNR} = \frac{M(i_{LD,ONE} - i_{LD,ZERO}) \frac{L_0}{d_0} \prod_{i=1}^{N} \frac{\eta_{in} G_i \eta_{out} L_i}{d_i} R_F}{\sqrt{N_T}} \tag{4.42}$$

By substituting Eq.(4.38) and (4.39) into (4.42), the signal-to-noise ratio can be rewritten as:

$$\sqrt{SNR} = \frac{2M \frac{e\eta P_{LD}}{h\nu} \frac{r-1}{r+1} \frac{L_0}{d_0} \prod_{i=1}^{N} \frac{\eta_{in} G_i \eta_{out} L_i}{d_i} R_F}{\sqrt{N_T}} \tag{4.43}$$

CHAPTER 5 CROSSTALK MODELING OF DENSE SINGLE-MODE WAVEGUIDE ARRAY

5.1 Introduction

Optical interconnects have the potential to provide higher bandwidth and higher density than metal interconnects.[14] It has been shown that passive waveguides based on silicon nitride [62] and polymers [63, 64] are attractive for very short distance interconnections, such as those between chips on a multi-chip module or on a printed-circuit-board, or as backplane interconnections. Although suffering more loss than fiber, waveguides have the potential of providing much closer spacing and planar crossover geometries and can integrate modulators, optical amplifiers and receivers on the same substrate as well [65]. The density of a waveguide array is limited mainly by the coupling-induced crosstalk between adjacent waveguides. In order to achieve the maximum density allowed by the required bit-error-rate (BER), it is necessary to determine the power coupling among waveguides in an array structure and thus the incurred system penalty.

Waveguide coupling has been intensively studied previously [66-72], but its relation to the system requirements has yet been established. In this chapter, we start with the analysis of waveguide coupling in a dense waveguide environment. A crosstalk model that relates the system requirements to the coupling between waveguides is then developed. Specifically, the following light-source scenarios are considered:

- *Noncoinciding uncorrelated light sources.* This is the most general case in which each channel has a separate laser source.
- *Coinciding uncorrelated light sources.* This situation could arise when the lasers are injection locked to a weak reference laser line.
- *Coinciding correlated light sources.* This case arises when the channels share the same laser source.

[14] A substantial portion of this chapter is adapted from C.-S. Li, C. M. Olsen, and D. G. Messerschmitt, "Analysis of Crosstalk Penalty in Dense Optical Chip Interconnects Using Single-Mode Waveguides," *IEEE Journal of Lightwave Technology*. (c) IEEE. Reprinted with permission.

In each case the power penalty at a bit-error-rate (BER) of 10^{-15} and the optimal threshold for minimizing the BER are computed. In addition, the effect of a nonoptimized decision threshold is considered.

It will be shown that for a 1-dB power penalty criterion, less than −25dB crosstalk can be tolerated in the worst case where the channel light sources are coinciding and correlated and the adjacent light sources are 180° out of phase with that of the center channel. For a nonoptimized decision threshold, the allowable crosstalk is reduced to −32 dB. In the other extreme, where either the channel wavelength spacing or the linewidth is much larger than the receiver bandwidth, a crosstalk level of as high as −12dB can be tolerated. If the light sources are uncorrelated but emitting at the same wavelength or the wavelength spacing is smaller than the receiver bandwidth, the laser phase noise contributes to the intensity noise due to the beating among the channel signals. The contributed intensity noise is largest when the laser linewidth is smaller than the receiver bandwidth.

Using typical waveguide parameters and −30dB as the criteria for maximum acceptable crosstalk, we can thus determine the minimum waveguide separation should be greater than 8 μm for a waveguide with width 3 μm and length up to 50 cm.

This chapter is organized as follows: Section 2 derives the mode coupling mechanism for a single-mode waveguide array. Simulations are then performed to demonstrate the mode coupling for various system configurations. Section 3 describes the general formulation of crosstalk between adjacent waveguides and derives the total receiver noise as well as the optimal decision threshold. In Section 4, the crosstalk induced intensity noise is derived for various relationships among the channel light sources. A summary is given in Section 5.

5.2 Waveguide Array Model

Figure 5-1 shows the geometry of an array of N buried waveguides, each with length ℓ, width w, and separation d from its neighbor. The refractive index of the waveguide and the substrate are n_1 and n_0, respectively. The waveguide width determines the spatial profile of the electric and magnetic field and the waveguide separation determines the overlap between the evanescent field of one waveguide and the confined field of the adjacent waveguide. In a multimode waveguide, the

power distribution among different excited waveguide modes depends on the exact launching conditions. We thus limit our crosstalk analysis to the single-mode waveguide array.

Neglecting the radiating modes, the coupled-wave equation for N-coplanar single-mode buried waveguides can be expressed as [68, 73]:

$$\frac{da_m}{dz} = -j\sum_{n=1}^{N} C_{m,n}e^{-j\Delta k_{m,n}z}a_n \qquad (5.1)$$
$$m = 1, \ldots, N; \quad n = 1, \ldots, N$$

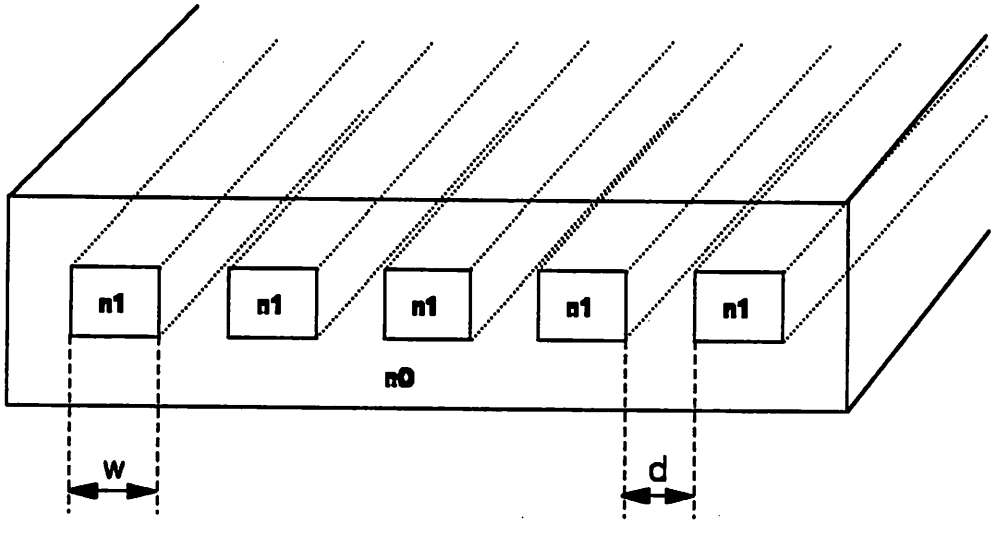

Figure 5-1. Structure of a buried-structure single-mode waveguide array. In this structure, the waveguide width is w and the waveguide separation is d. The optical index for the waveguide is n_1 while for the substrate is n_0.

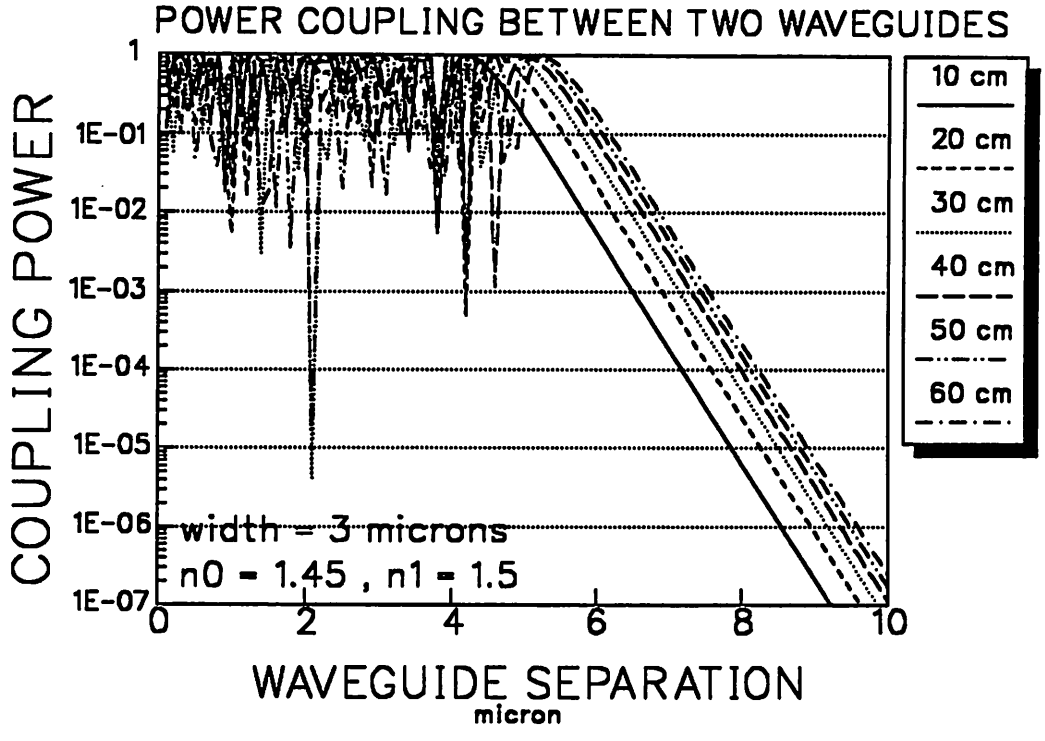

Figure 5-2. Power coupling between two waveguides as a function of waveguide separation. The waveguide lengths are ℓ =10, 20, 30, 40, 50, and 60 cm while w is fixed at 3 μm. $n_0 = 1.45$ and $n_1 = 1.5$.

where a_j is the coefficient of the normalized guided mode of the j^{th} waveguide and $\Delta k_{m,n} = k_{zm} - k_{zn}$ is the mismatch of the propagation constant between the m^{th} and the n^{th} waveguides along the propagation axis z. Assuming $\mathbf{e}_j(x,y)$ and $\mathbf{h}_j(x,y)$ represent the respective transversal electric and magnetic field distribution of the unperturbed guided mode of the j^{th} waveguide, the total electric and magnetic field of the waveguide array can be expressed as:

$$\mathbf{E}(x,y,z) = \sum_{m=1}^{N} a_m(z)\mathbf{e}_m(x,y)e^{-jk_{zm}z}$$
$$\mathbf{H}(x,y,z) = \sum_{m=1}^{N} a_m(z)\mathbf{h}_m(x,y)e^{-jk_{zm}z} \tag{5.2}$$

The coupling coefficient $C_{m,n}$ between the guided modes of the m^{th} and the n^{th} waveguides is

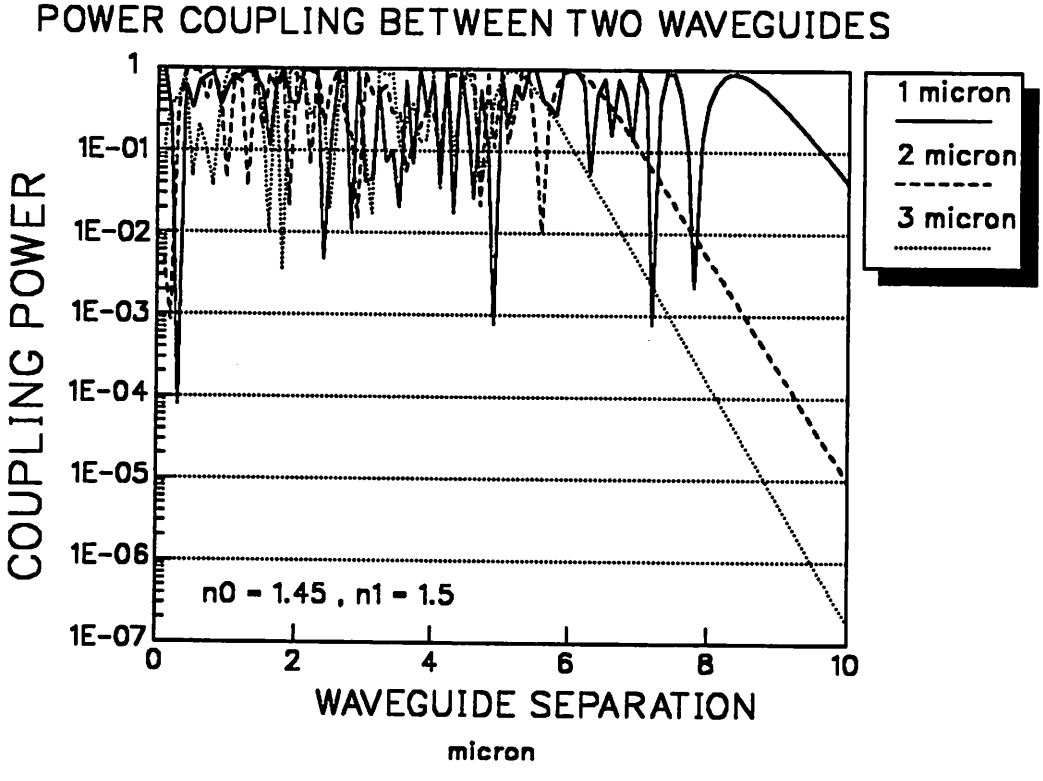

Figure 5-3. Power coupling between two waveguides as a function of waveguide separation. The waveguide widths are $w = 1$, 2, and 3 μm while $n_0 = 1.45$ and $n_1 = 1.5$.

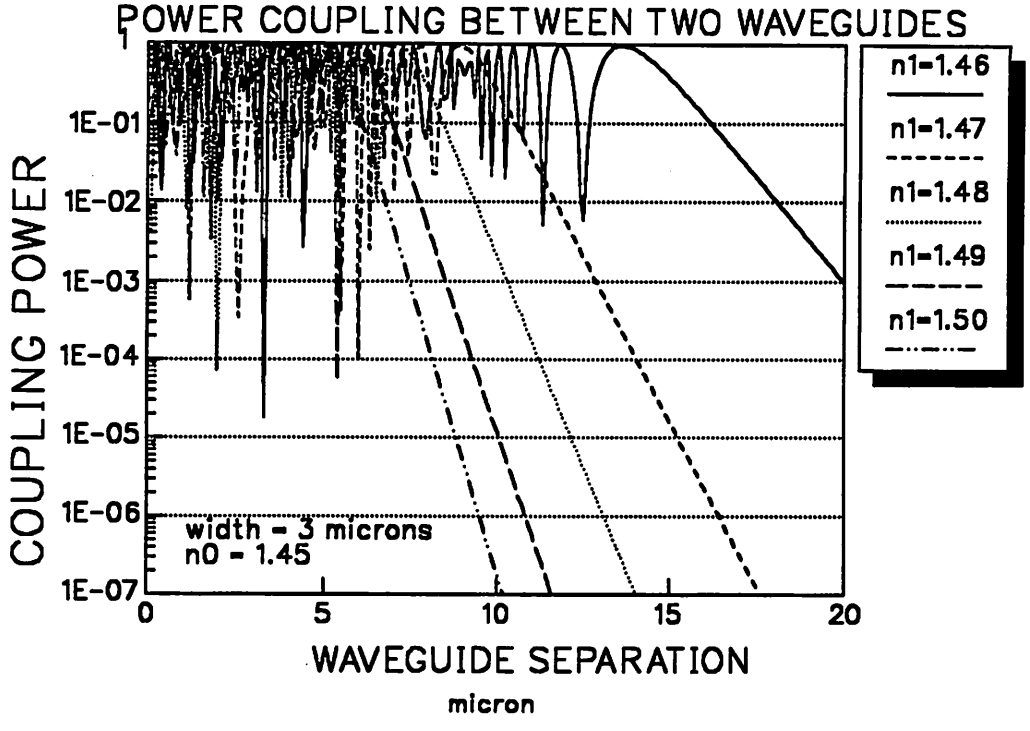

Figure 5-4. Power coupling between two waveguides as a function of waveguide separation. for $n_1 = 1.46$, 1.47, 1.48, 1.49 and 1.50; $n_0 = 1.45$ and $w = 3$ μm.

$$C_{m,n} = \frac{\omega}{2} \int\int_{S_m} (\varepsilon_1 - \varepsilon_0) \mathbf{e}_m \cdot \mathbf{e}_n^* \, dS \tag{5.3}$$

where ω is the optical frequency (set at $\lambda = 1.55$ μm), ε_1 and ε_0 are the corresponding dielectric constant for the waveguide and the substrate. Note that the variables d and w are embedded in the overlap integral of the electric field of the adjacent waveguides. In these expressions, the variations in the refractive index of the same waveguide and among different waveguides are ignored. Due to the symmetric and homogeneous geometry (no self-coupling) assumed for the waveguide array

[74], we have $C_{m,n} = C_{n,m}$, $C_{m,m} = 0$, and $k_{zm} = k_{zn}$. In addition, we also assume weak coupling between adjacent waveguides so that the coupling between nonadjacent waveguides is negligible, i.e., $C_{m,n} = 0$ for $|m - n| \geq 2$. With these simplifications, Eq.(5.1) reduces to

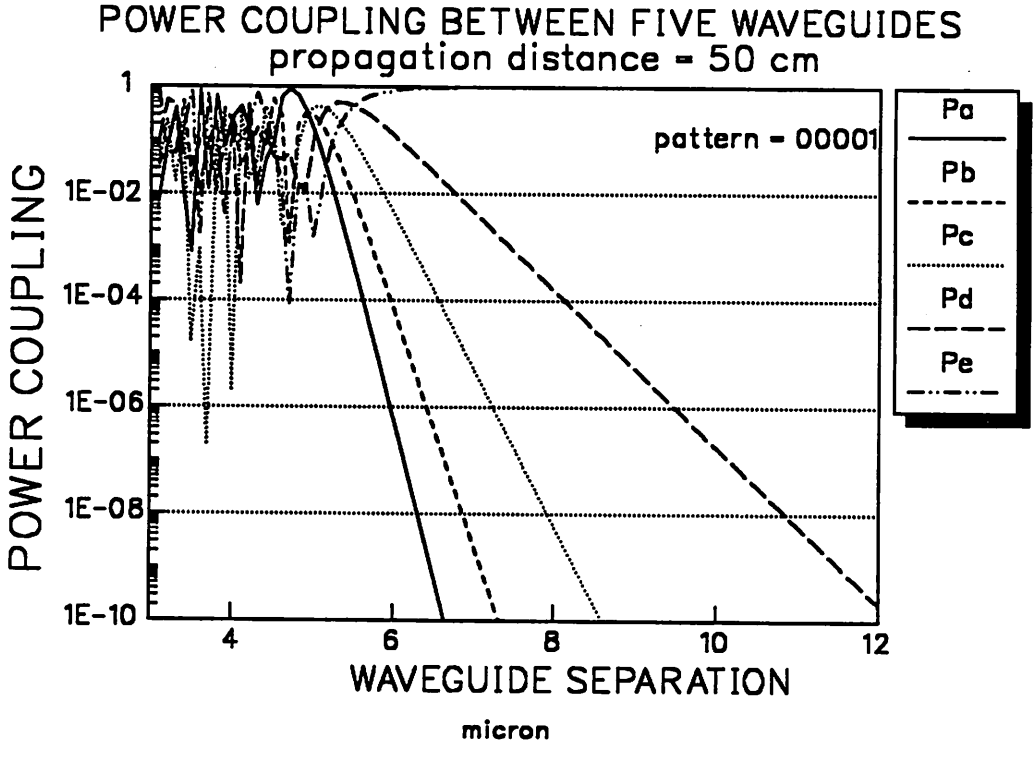

Figure 5-5. Power coupling between five waveguides. A spatial bit pattern of 00001 is launched into the waveguide array.

$$\frac{da_1}{dz} = -jC_{1,2}a_2$$

$$\frac{da_m}{dz} = -jC_{m,m-1}a_{m-1} - jC_{m,m+1}a_{m+1} \qquad (5.4)$$
$$m = 2,3,4, \ldots, N-1$$

$$\frac{da_N}{dz} = -jC_{N,N-1}a_{N-1}$$

For $N = 2$, Eq.(5.4) can be solved analytically and a closed-form solution can be obtained [74, 75]. Figure 5-2 shows the coupling power as a function of d for various values of ℓ at $w = 3\mu$m, $n_0 = 1.45$ and $\Delta n/n_0 = 0.344$. There exists a strong and oscillatory coupling behavior between the two waveguides until d reaches a critical separation, $d_c \simeq 5\mu$m, after which the coupling power reduces monotonically with the increase of d. The coupling length, $L_c(d)$, defined as the ℓ at which a first total transfer of optical power from one waveguide to its neighbor is occurred, increases as d increases. Note that total power transfer occurs at $\ell = (2p-1)L_c$ while zero power transfer occurs at $\ell = 2pL_c$, where p is any positive integer. Suppose d is reduced from infinity to zero, the first total power transfer happens at $d = d_c$, which is the solution of $L_c(d) = \ell$. The subsequent total power transfer occurs at values of d that satisfy $(2p-1)L_c(d) = \ell$ and lead to oscillatory behavior for $d \in (0, d_c]$. When $d > d_c$, which leads to $L_c(d) > \ell$, the amount of power coupled monotonically decreases with the increase in d. Likewise, longer ℓ requires larger d_c in order to achieve $L_c(d_c) = \ell$, as shown in the figure. The coupling power as a function of d for various values of w is shown in Figure 5-3. For small w, the guided mode is less confined and more field coupling between waveguides is allowed, resulting in an increase in d_c and a decrease in L_c. Similarly, a decrease in Δn reduces the field confinement, thus resulting in an increase in d_c, as shown in Figure 5-4.

For $N > 2$, Eq.(5.4) can be solved numerically using Runge-Kutta method [76]. Detail simulations have been performed for $N = 3$ and 5 at $w = 3\mu$m, $\ell = 50$ cm, and $\Delta n/n_0 = 0.344$. As shown in Figure 5-5, the coupling power behavior depends on the spatial bit patterns sent into the waveguides. For spatial bit pattern 00001, the coupling at the waveguide adjacent to the signal

channel is similar to that in $N = 2$. The coupling is weaker at channels farther away from the signal channel, yielding a steeper slope in power coupling versus d for $d > d_c$.

In order to utilize single-mode waveguides as parallel interconnections, the separation between any two waveguides has to exceed $\simeq 6\mu$m for $\Delta n/n_o = 0.344$, $w = 3\mu$m, and $\ell = 50$ cm. This separation is several times smaller than that can be achieved by the thin-film metal approach ($d = 25 \sim 250$ μm [11]), showing the significant density improvement in optical approach. However, the optical alignment between the transmitter and waveguide could be difficult and an integrated approach in fabrication, such as having the transmitters, waveguide array, and receivers be fabricated on the same wafer, is thus preferred.

5.3 Formulation of Waveguide Crosstalk

We consider an interconnect system with N identical single-mode waveguides with uniform separation, as shown in Figure 5-1. We assume synchronous transmission and a data rate much smaller than the laser relaxation oscillation frequency.

5.3.1 Adjacent channel crosstalk

If the optical signal from the laser diode has an extinction ratio, r, then the optical power levels P_{on} and P_{off} for the logical signal ONE and ZERO, respectively, are

$$P_{on} = \frac{2r}{r+1} P_{av}$$
$$P_{off} = \frac{2}{r+1} P_{av} \tag{5.5}$$

where P_{av} is the average laser output power. A nonreturn-to-zero (NRZ) modulation format has been assumed. Considering only the coupling from adjacent waveguides, the output electric field from the j^{th} waveguide is

$$E_j(t) = \sqrt{1-2B^2}\sqrt{1-A^2}\sqrt{2P_j}\cos(\omega_j t + \Phi_j(t) + \Theta_j) \tag{5.6}$$

when there is no light input to the adjacent waveguides. In this expression, B^2 is the total power coupled from a waveguide into the adjacent waveguide, A^2 is the losses incurred by the waveguides (i.e. scattering and absorption), P_j can be either P_{on} or P_{off}, ω_j is the angular laser frequency, $\Phi_j(t)$ is the laser phase noise process, and Θ_j is the initial phase of the laser. The electric field coupled into the adjacent waveguides (i.e. channel $j-1$ and $j+1$) is

$$E_{xtalk}(t) = B\sqrt{1-A^2}\,\sqrt{2P_j}\,\cos(\omega_j t + \Phi_j(t) + \Theta_j) \tag{5.7}$$

Considering only the crosstalk from adjacent channels and ignoring the losses, the output electric field of the j^{th} waveguide in the presence of crosstalk from channels $j-1$ and $j+1$ is

$$\begin{aligned} E_{bcond}(t) = &\sqrt{1-2B^2}\,\sqrt{2P_j}\,\cos(\omega_j t + \Phi_j(t) + \Theta_j) \\ &+ B\sqrt{2P_{j-1}}\,\cos(\omega_{j-1} t + \Phi_{j-1}(t) + \Theta_{j-1}) \\ &+ B\sqrt{2P_{j+1}}\,\cos(\omega_{j+1} t + \Phi_{j+1}(t) + \Theta_{j+1}) \end{aligned} \tag{5.8}$$

where $bcond = b_{j-1}b_jb_{j+1}$ is the bit pattern sent into the waveguides $j-1, j, j+1$. From Eq.(5.8), the output intensity of channel j is

$$\begin{aligned} P_{bcond}(t) = &(1-2B^2)P_j + B^2(P_{j-1} + P_{j+1}) \\ &+ 2B\sqrt{1-2B^2}\,(\gamma_{jj-1}(t)\sqrt{P_jP_{j-1}} + \gamma_{jj+1}(t)\sqrt{P_jP_{j+1}}) \\ &+ 2B^2\gamma_{j-1j+1}(t)\sqrt{P_{j-1}P_{j+1}} \end{aligned} \tag{5.9}$$

where terms at twice the optical frequency have been ignored. $\gamma_{m,n}(t)$ is defined as:

$$\gamma_{m,n}(t) = \cos((\omega_{m,n})t + \Phi_{m,n}(t) + \Theta_{m,n}) \tag{5.10}$$

where $\omega_{m,n} = \omega_m - \omega_n$, $\Phi_{m,n}(t) = \Phi_m(t) - \Phi_n(t)$, and $\Theta_{m,n} = \Theta_m - \Theta_n$. In these expressions, $m \in \{j, j-1\}$, $n \in \{j, j+1\}$ and $m \neq n$.

5.3.2 *Total receiver noise*

The optical signal is assumed to be received by a photodetector with quantum efficiency η and avalanche gain M, and is amplified by a transimpedance preamplifier with feedback resistance, R_f. The voltage of the output signal, V, from the j^{th} preamplifier for a given bit pattern, *bcond*, sent into the waveguides $j-1, j, j+1$ thus equals

$$V_{bcond} = \frac{\eta M e}{h\nu} E[P_{bcond}] R_F \tag{5.11}$$

where

$$E[P_{bcond}] = (1 - 2B^2)\, P_j + B^2 (P_{j-1} + P_{j+1}) \tag{5.12}$$

is the expectation of Eq.(5.9), e is the electron charge, ν is the optical frequency and h is the Planck's constant. The total noise power V_N^2 from the j^{th} receiver, assuming the receiver has a bandwidth BW, equals [60]:

$$\begin{aligned} V_{N_{bcond}}^2 = & \left[(V_A^*)^2 \left((1 + \frac{R_F}{R})^2 + \frac{4\pi^2}{3} BW^2 C^2 R_F^2 \right) + R_F^2 \left(\frac{4kT}{R} + (I_A^*)^2 \right) + 4kTR_F \right] BW \\ & + R_F^2 \int_{-BW}^{BW} S_{bcond}^I(f)\, df \end{aligned} \tag{5.13}$$

where R and C are the preamplifier input resistance and capacitance, respectively, k is Boltzmann's constant, and T is the temperature. $S_{bcond}^I(f)$ is the noise spectral density of the photodetector output current which can be derived (See Appendix A.) using a similar strategy to that of [58]:

$$S_{bcond}^I(f) = \left(\frac{\eta M^2 F e^2}{h\nu} E[P_{bcond}] + \left(\frac{\eta M e}{h\nu} \right)^2 S_{bcond}^P(f) \right) \tag{5.14}$$

where $S^{r}_{bcond}(f)$ is the optical intensity noise spectral density and F is the avalanche photodiode excess noise factor. F is usually related to both the avalanche gain M and the ionization factor of the APD [61]. In Eq.(5.14), the first term is the signal-induced detector shot-noise while the second term is contributed by the signal-intensity noise. The subscript, *bcond*, in equations (5.11)-(5.14) has been used to emphasize the impact of the parallel bit pattern on the total noise. Table 1 summarizes the definition as well as the values for various parameters used in this chapter. In the next section we shall calculate the optical intensity noise in the j^{th} channel in the presence of the crosstalk from adjacent channels.

R_F	feedback resistance	10 kΩ
R	receiver input resistance	40 kΩ
C	receiver input capacitance	0.2 pF
V_A^*	amplifier noise voltage	2 nV/$\sqrt{Hz}$
I_A^*	amplifier input noise current	2 pA/$\sqrt{Hz}$
M	avalanche gain	1
λ	wavelength	1550 nm
T	temperature	300 K
η	photodetector quantum efficiency	1.0
BW	electrical bandwidth	500MHz
r	extinction ratio	20.0

TABLE I. A SUMMARY OF THE DEFINITION AND VALUES OF THE PARAMETERS USED IN THE CALCULATIONS.

5.3.3 Calculation of optimal threshold level

The probability of detecting an error in channel j in the presence of crosstalk from adjacent channels $j-1$ and $j+1$ is

$$P_e = \frac{1}{8}\sum_{i=0}^{1}\sum_{k=0}^{1}\left(P[b_j^r = 1 \,|\, (b_{j-1}, b_j, b_{j+1}) = (i,0,k)] + P[b_j^r = 0 \,|\, (b_{j-1}, b_j, b_{j+1}) = (i,1,k)]\right) \quad (5.15)$$

assuming equal probability of 1's and 0's in all the channels. In Eq.(5.15) b_j^i is the regenerated bit value in the j^{th} receiver. If the optimal threshold is x, Eq.(5.15) reduces to

$$P_e = \frac{1}{16}\sum_{i=0}^{1}\sum_{k=0}^{1}\left(\text{erfc}\left(\frac{x - V_{i0k}}{\sqrt{2}\,V_{N_{i0k}}}\right) + \text{erfc}\left(\frac{V_{i1k} - x}{\sqrt{2}\,V_{N_{i1k}}}\right)\right) \tag{5.16}$$

where V_{i0k} and V_{i1k} are the expected output voltage when logical ZERO and ONE, respectively, are sent. The optimal threshold is the value that minimizes the bit-error rate. Therefore the optimal threshold for signal detection in the presence of interfering channels is the solution to

$$\sum_{i=0}^{1}\sum_{k=0}^{1}\left(\frac{1}{V_{N_{i0k}}}e^{-\frac{(x - V_{i0k})^2}{2V_{N_{i0k}}^2}} - \frac{1}{V_{N_{i1k}}}e^{-\frac{(V_{i1k} - x)^2}{2V_{N_{i1k}}^2}}\right) = 0 \tag{5.17}$$

which is obtained by setting $\partial P_e/\partial x$ to zero.

In the following we will investigate the impact of phase-to-intensity noise conversion on the system performance (i.e. Eq.(5.16)) of the j^{th} channel.

5.4 SYSTEM PENALTY DUE TO ADJACENT CHANNEL CROSSTALK

In this section, the system penalty caused by adjacent channel crosstalk will be derived for the following light-source scenarios:

- noncoinciding uncorrelated light sources,
- coinciding uncorrelated light sources, and
- coinciding correlated light sources.

5.4.1 *Noncoinciding Uncorrelated Light Sources*

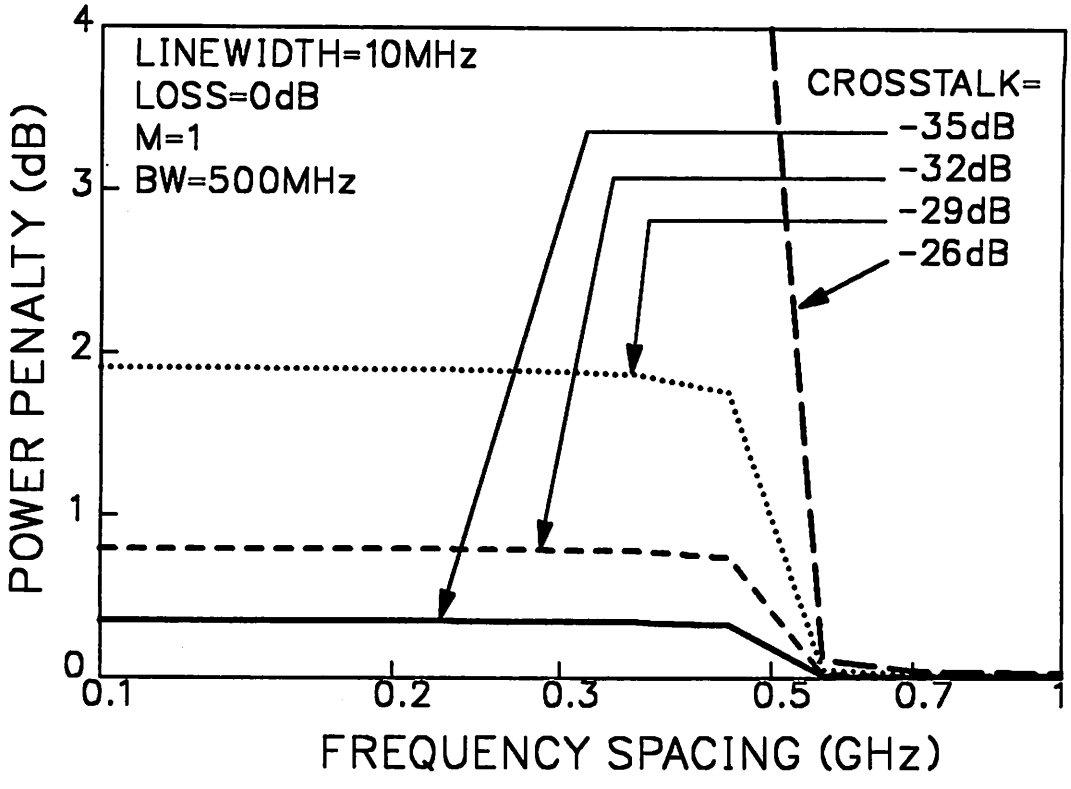

Figure 5-6. Power penalty vs. frequency spacing. The crosstalk levels vary from −35dB to −26dB. The electrical bandwidth of the receiver is assumed to be 500 MHz.

Each channel in this case is operated with an independent laser source. In order to calculate the BER in Eq.(5.16), we need to calculate the expectation of Eq.(5.9) and the optical noise spectral density, S^{P}_{bcond}, in Eq.(5.14). The expectation of the light intensity is given in Eq.(5.12) and the power spectral density of the light intensity in the j^{th} channel can be calculated to (see Appendix B)

$$S^{P}_{bcond}(f) = \frac{\Delta\nu}{2\pi}\left(\frac{c^2_{j,j-1}}{(\Delta\nu)^2 + (f-\Delta f_{j,j-1})^2} + \frac{c^2_{j,j+1}}{(\Delta\nu)^2 + (f-\Delta f_{j,j+1})^2} + \frac{c^2_{j-1,j+1}}{(\Delta\nu)^2 + (f-\Delta f_{j-1,j+1})^2}\right) \tag{5.18}$$

where $\Delta\nu$ is the laser linewidth and $\Delta f_{m,n} = f_m - f_n$. $c_{j,j-1}$, $c_{j,j+1}$, and $c_{j-1,j+1}$ are given as

$$\begin{aligned} c_{j,j-1} &= 2B\sqrt{1-2B^2}\,\sqrt{P_j P_{j-1}} \\ c_{j,j+1} &= 2B\sqrt{1-2B^2}\,\sqrt{P_j P_{j+1}} \\ c_{j-1,j+1} &= 2B^2\sqrt{P_{j-1}P_{j+1}} \end{aligned} \tag{5.19}$$

The total noise power due to phase-to-intensity noise conversion is

$$\begin{aligned} N_{bcond} = \frac{1}{2\pi}\Big[& c^2_{j,j-1}\left(\tan^{-1}\frac{BW-\Delta f_{j,j-1}}{\Delta\nu} + \tan^{-1}\frac{BW+\Delta f_{j,j-1}}{\Delta\nu}\right) \\ & + c^2_{j,j+1}\left(\tan^{-1}\frac{BW-\Delta f_{j,j+1}}{\Delta\nu} + \tan^{-1}\frac{BW+\Delta f_{j,j+1}}{\Delta\nu}\right) \\ & + c^2_{j-1,j+1}\left(\tan^{-1}\frac{BW-\Delta f_{j-1,j+1}}{\Delta\nu} + \tan^{-1}\frac{BW+\Delta f_{j-1,j+1}}{\Delta\nu}\right) \end{aligned} \tag{5.20}$$

Using the derivations of Section 3, we calculated the power penalty at BER = 10^{-15} as a function of the channel frequency spacing for a laser linewidth of 10MHz. A uniform channel spacing is assumed here (i.e. $|\Delta f_{j,j-1}| = |\Delta f_{j,j+1}|$ and $|\Delta f_{j-1,j+1}| = 2|\Delta f_{j,j-1}|$). The result is illustrated in Figure 5-6 for crosstalk levels ranging from −35dB to −26dB. The power penalty is at its maximum when the channel frequency spacing is zero. The intensity noise seen by the receiver (i.e. N_{bcond}) approaches zero when the channel frequency spacing becomes much larger than the receiver bandwidth and the laser linewidth. This behavior is evident from Eq.(5.18) in which we can observe that the frequency spacing $\Delta f_{m,n}$ has the effect of shifting the intensity noise spectral density by an amount $\Delta f_{m,n}$. Therefore, zero frequency spacing gives the maximum overlap between the noise spectral density and the receiver passband. As the frequency spacing increases, the overlap

between the down-converted intensity noise spectral density and the receiver passband monotonically decreases and asymptotically approaches zero as the frequency spacing goes to infinity. In this case, the only effect from the crosstalk is a bit-pattern-dependent DC-eye-closing (due to the first two terms in Eq.(5.9)) which gives rise to the smallest system degradation for a given crosstalk level. The maximum allowable crosstalk level is calculated to be −12dB for a 1dB power penalty criterion in this case.

5.4.2 Coinciding Uncorrelated Light Sources

If the light sources, for example, are locked to a weak external absorption line, the lasers will have coinciding mean wavelengths but still be individually uncorrelated with regard to the phase noise process. Another scenario is the situation in which the channels are sharing the same source but the difference of propagation delay between adjacent channels exceeds the laser coherence time. In either case, the laser phase noise will contribute to the intensity noise of the signal due to the frequency beating among the channel signals. The total noise power in the receiver bandwidth, BW, due to phase-to-intensity noise conversion can be derived from Eq.(5.20) by setting $\Delta f_{m,n}$ equal to zero:

$$N_{bcond} = \frac{1}{\pi}(c_{j,j-1}^2 + c_{j,j+1}^2 + c_{j-1,j+1}^2)\tan^{-1}\frac{BW}{\Delta\nu} \tag{5.21}$$

It is clear from Eq.(5.21) that the maximum optical intensity noise level is reached when $\Delta\nu \ll BW$ (i.e. all the down-converted phase-to-intensity noise falls within the receiver bandwidth). The minimum noise level appears in cases where $\Delta\nu \gg BW$ (i.e. only a small fraction of the down-converted phase-to-intensity noise falls within the receiver bandwidth). As $BW/\Delta\nu$ approaches zero, the total intensity noise power also approaches zero.

Figure 5-7 shows the power penalty versus crosstalk level for various values of the laser linewidth and Figure 5-8 shows the power penalty as a function of linewidth for various crosstalk levels. As expected, the power penalty increases as either the crosstalk level increases or the laser linewidth decreases. The maximum allowable crosstalk is about −17dB for a laser linewidth of 10

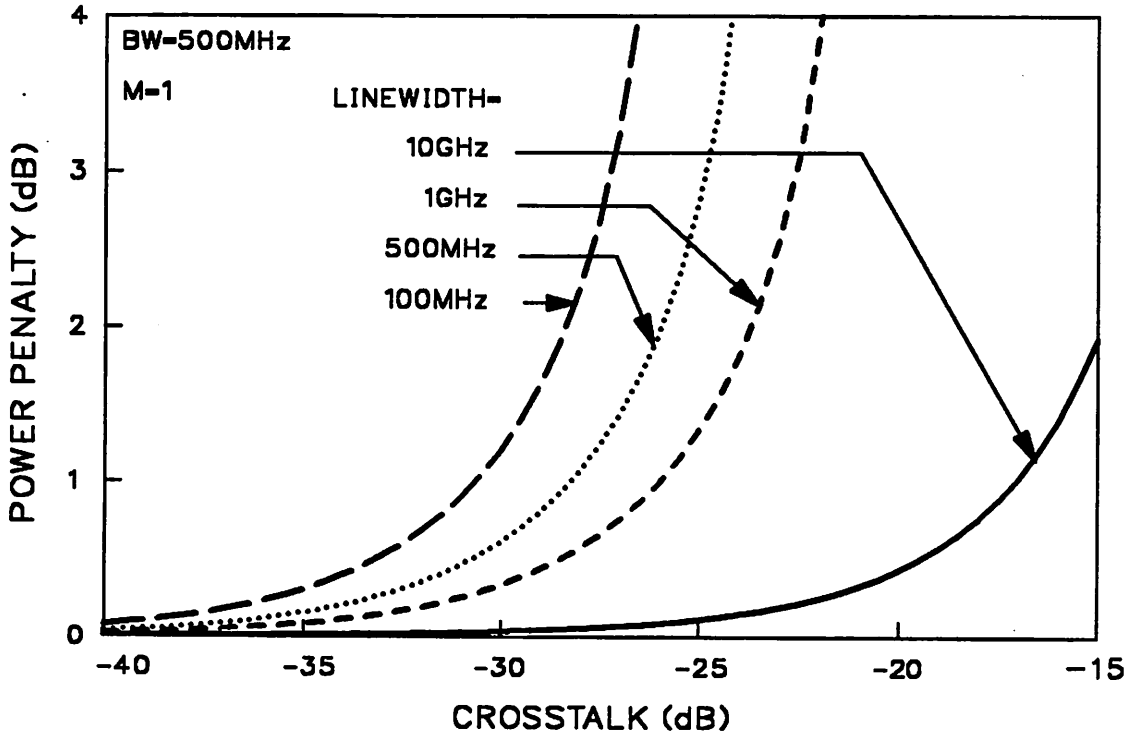

Figure 5-7. Power penalty vs. crosstalk. The laser linewidth varies from 100 MHz to 10 GHz.

GHz. On the other hand, the allowable crosstalk is reduced to −31dB when the laser linewidth is 100MHz. Note that even though the linewidth or the channel frequency spacing goes to infinity, the crosstalk still has an impact on the eye opening due to the first two terms in Eq.(5.9).

5.4.3 Coinciding Correlated Light Sources

If the light sources have identical wavelength and constant phase relationship (e.g. an array of external modulators modulating the light from a shared laser source), the phase terms in Eq.(5.9) will be deterministic and time-invariant except for the possible dependency on a random initial phase.

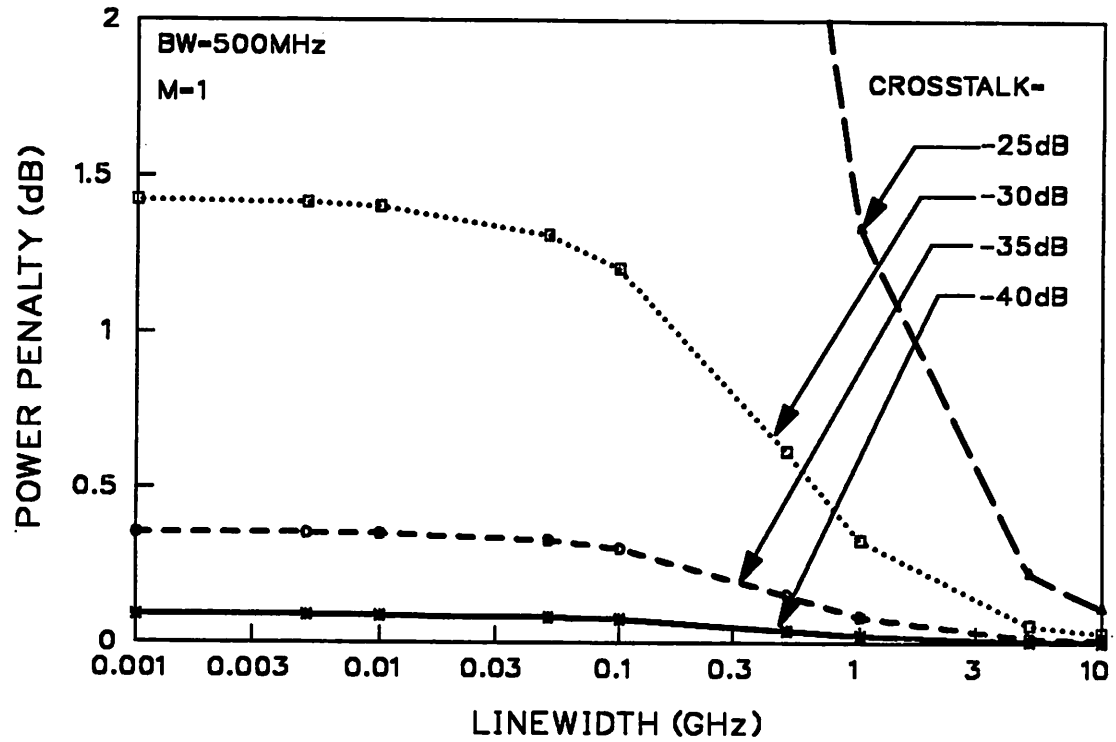

Figure 5-8. Power penalty vs. laser linewidth. The crosstalk levels vary from −40dB to −25dB. The electrical bandwidth of the receiver is assumed to be 500 MHz.

Figure 5-9 shows the power penalty as a function of the crosstalk level for various phase difference values between the adjacent waveguides and the center waveguide. In the worst case when the phase of both adjacent waveguides are 180° out of phase with the center waveguide, only −25dB crosstalk can be tolerated. In the best case (i.e. $\Theta_{j,j\pm1} \in [60°, 90°]$), the maximum allowable crosstalk level is −11dB. Figure 5-10 shows the impact on the power penalty for nonidentical phase differences (i.e. $\Theta_{j,j-1} \neq \Theta_{j,j+1}$). As shown in this figure, the power penalty for −20dB of crosstalk is not significantly dependent on the phase difference as long as $\Theta_{j,j\pm1} \in [-90°, 90°]$. Figure 5-11 shows that the normalized optimum threshold is significantly affected (≥20% in the worst case) as the amount of crosstalk exceeds −20dB. On the other hand, the optimal threshold

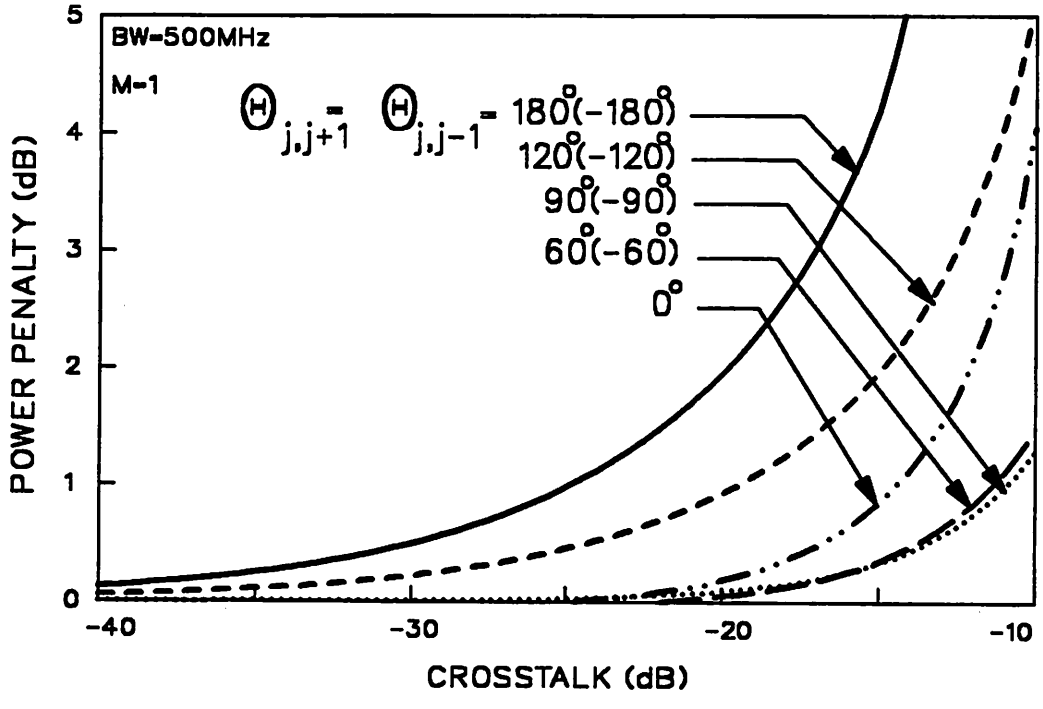

Figure 5-9. Power penalty vs. crosstalk for various phase difference. $\Theta_{m,n}$ is defined as $\Theta_m - \Theta_n$.

is also affected by the phase difference between adjacent channels, as shown in Figure 5-12. The normalized optimal threshold reaches a maximum when the source used by adjacent waveguides are 90° out of phase (i.e. $\Theta_{m,n} = 90°$) and reaches a minimum when the source used by adjacent waveguides are 180° out of phase (i.e. $\Theta_{m,n} = 180°$).

5.4.4 Discussion

The system degradation for various source conditions is summarized in Figure 5-13. As shown in this figure, the power penalty for the wavelength-coinciding weakly coherent light sources exceed that of the wavelength-coinciding strongly coherent source, e.g. for a laser linewidth of 500

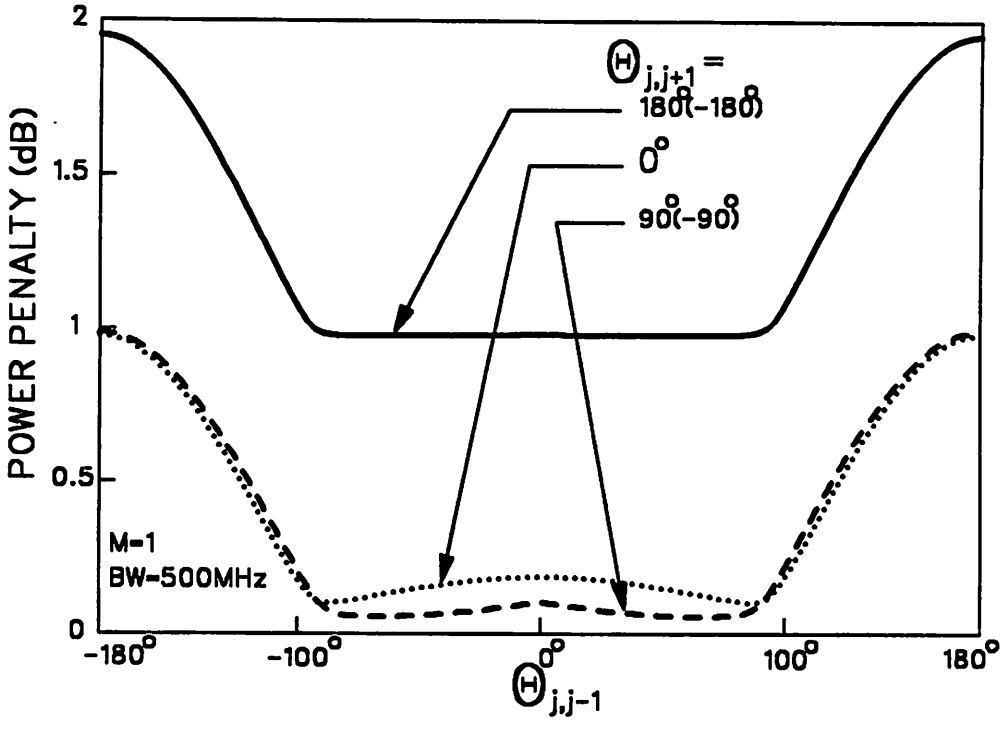

Figure 5-10. Power penalty vs. phase difference. The crosstalk level is assumed to be −20dB.

MHz and a crosstalk level higher than −25dB. One may wonder why wavelength-noncoinciding or wavelength-coinciding weakly coherent sources (the cases discussed in Section 4.1 and 4.2) impose stronger demands on the crosstalk level than wavelength-coinciding strongly coherent source (the case discussed in Section 4.3) under some circumstances. Intuitively, wavelength-coinciding strongly coherent light sources should give rise to the largest and constant closing of the eye (e.g. for 180° phase difference). Due to the random nature of the phase-to-intensity noise conversion in the case of using weakly coherent light sources, the same amount of eye closing may only be observed temporarily since the phase difference, $\Phi_{m,n}$, changes randomly in time between 0 and 2π. Therefore, the *average* power penalty for a system using weakly coherent light sources could

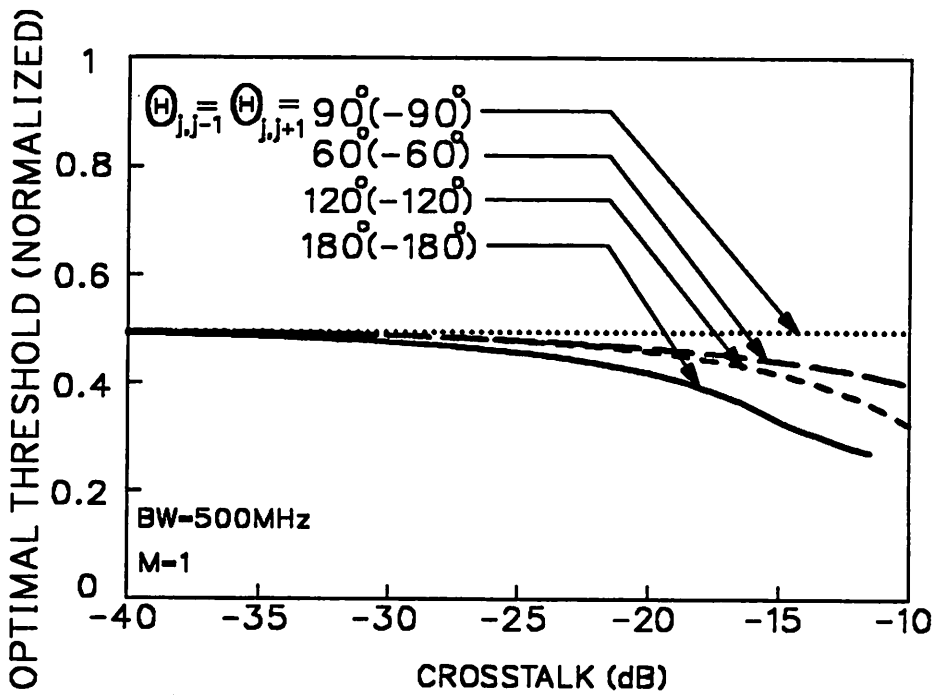

Figure 5-11. Threshold vs. crosstalk for various phase difference. The crosstalk level is assumed to be −20dB.

only be better than that obtained from the worst case of using wavelength-coinciding strongly coherent light sources. The explanation is simply that we have assumed the probability distribution function of the phase-to-intensity noise is Gaussian in computing the bit-error rate (Eq.(5.16)). The bit-error rate calculations based on this assumption usually overestimates the power penalty as compared to that from using the actual probability distribution function [16] since there obviously is an upper and lower bound on the eye closure imposed by the crosstalk. Therefore, in general the maximum allowable crosstalk level for the cases discussed in Section 3.1 and 3.2 will always be higher than the case where $\Delta v \gg BW$ or $\Delta f_{m,n} \gg BW$ and lower than the case where $\Delta f_{m,n} = 0$ and $\Delta\Theta_{m,n} = 180°$, as indicated by the hatched area on Figure 5-13.

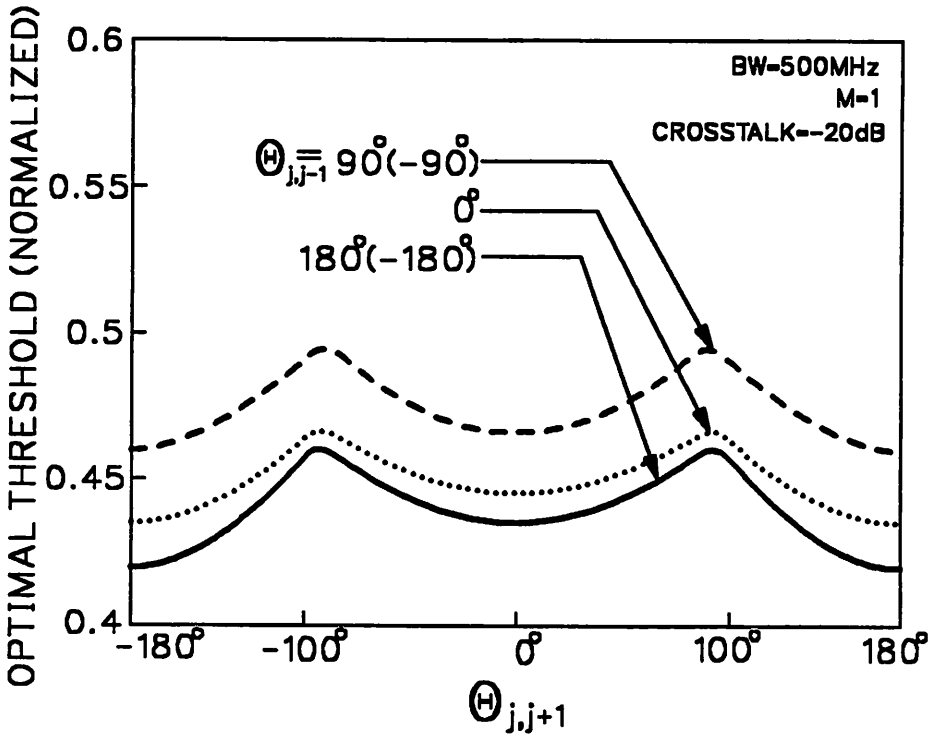

Figure 5-12. Threshold vs. phase difference. The crosstalk level is assumed to be −20dB.

In Section 4.3, we have shown that the optimal decision threshold is modified by the crosstalk from adjacent channels. However, the decision threshold in a practical optical receiver is usually derived from an automatic gain control mechanism and is set at the average of the incoming light signals. Therefore, a substantial power penalty is induced if the optimal decision threshold is different from the average value of the incoming light signals. Furthermore, an additional power penalty is introduced when the decision threshold is offset from the average value of the light signals due to the device mismatch in a receiver. Both of these factors affect the maximum allowable crosstalk, as shown in Figure 5-14. In Figure 5-14, a criterion of 1-dB power penalty at BER $= 10^{-15}$ has been used to obtain the maximum allowable crosstalk as a function of the decision

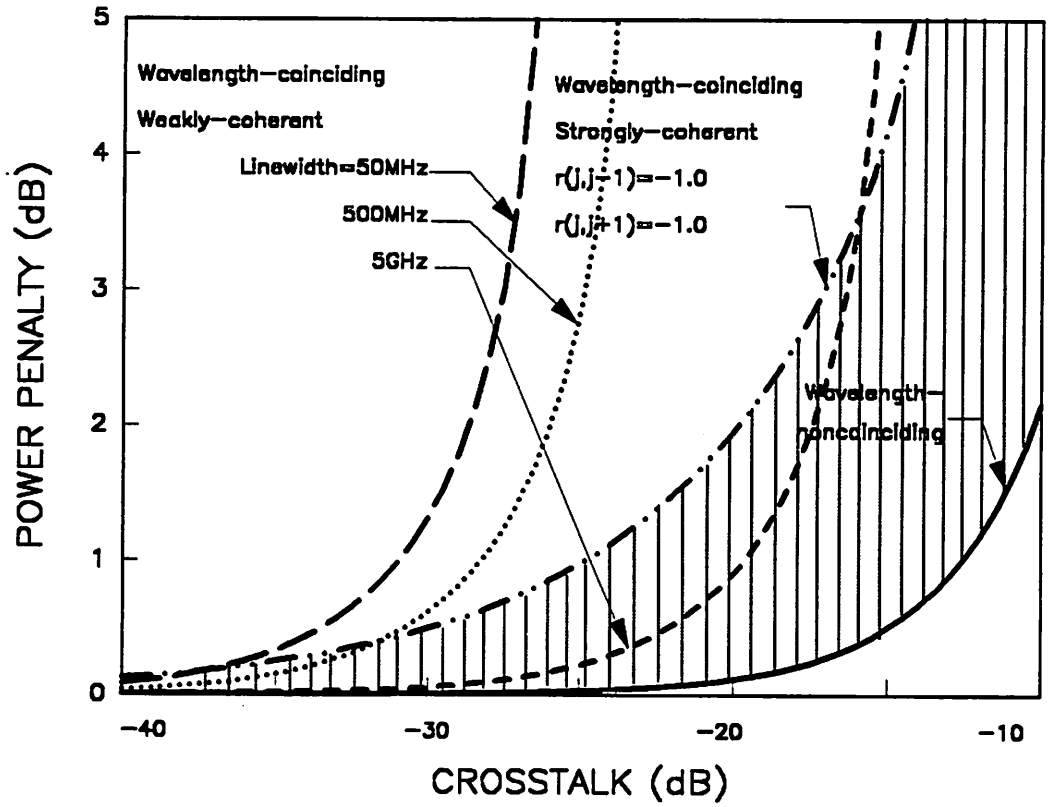

Figure 5-13. Power penalty vs. crosstalk comparison for difference source conditions. $r(j,j-1)$ and $r(j,j+1)$ are defined as $\cos(\Theta_j - \Theta_{j-1})$ and $\cos(\Theta_j - \Theta_{j+1})$, respectively.

threshold. This figure shows that the maximum allowable crosstalk is very sensitive to the decision threshold. Assuming that the sampling level will not be optimized and that it will be set to 50% with ± 5% accuracy, it is seen from the figure that the crosstalk level should not exceed −32 dB (obtained at the 55% sampling level). Assuming the threshold uncertainty is even worse, say ± 10%, the maximum allowable crosstalk level reduces to −54 dB! Therefore, we further conclude that the uncertainty on the decision threshold should be smaller that ± 5% in order to obtain realistic requirements to the crosstalk level. The asymmetric nature of the curve in Figure 5-14 is due to the larger shot noise level in the logical ONE.

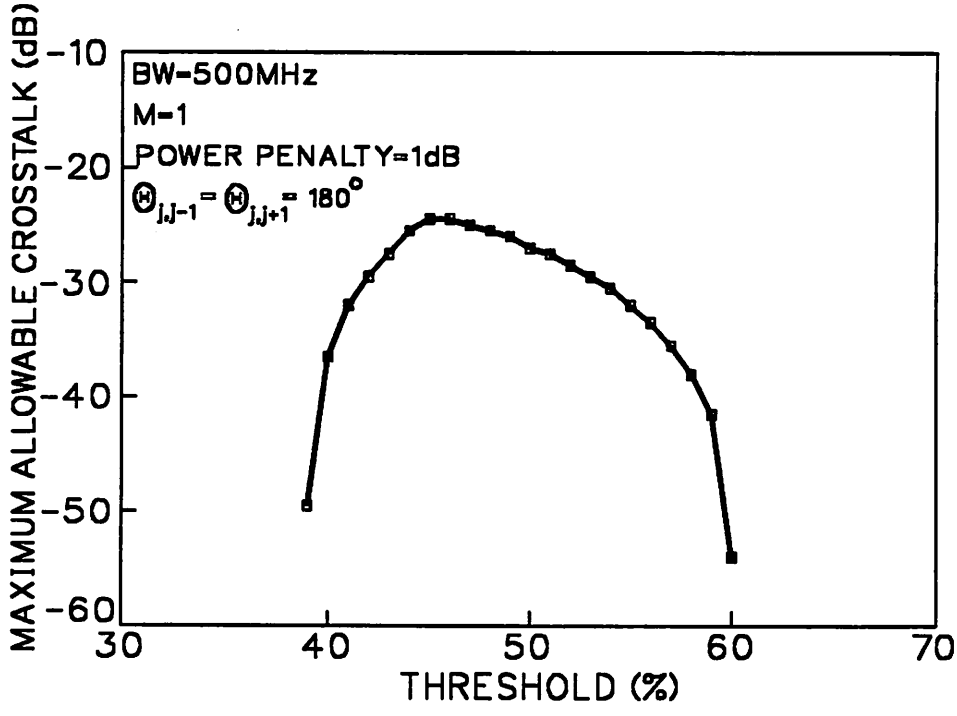

Figure 5-14. Maximum allowable crosstalk vs. position of the threshold. A 1-dB power penalty criterion at 10^{-15} is assumed.

5.5 SUMMARY

In this chapter, we have derived a crosstalk model to determine the crosstalk-induced system penalty caused by coupling between adjacent channels in a dense single-mode waveguide array environment. Three different light-source scenarios are considered:

(1) Wavelength-noncoinciding uncorrelated,

(2) Wavelength-coinciding uncorrelated and

(3) Wavelength-coinciding correlated light sources.

In case (3) where the channels share the same laser source, the system penalty only depends on the phase difference between adjacent waveguides. Only −25dB of crosstalk can be tolerated in the

worst case when both of the adjacent waveguides are 180° out of phase with the center waveguide. In the other extreme where the channel frequencies are widely spaced (i.e. the channel frequency spacing is much larger than the receiver bandwidth), a crosstalk of −12dB can be tolerated. If the light sources are emitting at the same wavelength but are uncorrelated, the laser phase noise contributes to the intensity noise due to the beating among the channel signals. The contributed intensity noise is largest for laser linewidths smaller than the receiver bandwidth. In the best case where the linewidth is significantly larger than the receiver bandwidth, a maximum crosstalk of about −12dB is acceptable. In the worst case where all the down-converted phase-to-intensity noise falls within the receiver bandwidth, we can not accurately predict the maximum allowable crosstalk level with the assumption that the phase-to-intensity noise follows a Gaussian distribution. However, the maximum allowable crosstalk level will be lower-bounded by −25dB.

In optical chip interconnects it is unlikely that the decision threshold will be optimized. For a sampling level at 50% of the average signal swing we found that the requirement to the maximum allowable crosstalk level reduces to −32 dB assuming a ± 5% uncertainty on the sampling level.

Using −30 dB as the maximum allowable crosstalk, we can determine the minimum waveguide spacing to be larger than 8 μm from Figure 5-3, assuming the waveguide width is 3 μm and length is 50 μm. The density of the single mode waveguide therefore approaches 900/cm, which is significantly larger than thin-film microstrip lines.

Finally, our derivation does not take into account the effect of laser wavelength chirping. The system penalty would be smaller than predicted by the present model if this effect is included.

APPENDIX A. DERIVATION OF EQUATION (5.17)

Following the derivation in [58], we divide the time axis into small intervals Δt with the k^{th} interval being $[(k-1/2)\Delta t,(k+1/2)\Delta t]$. Let the random variable N_k denote the number of arrivals in the k^{th} interval, the current can then be expressed as

$$I_f(t) = \lim_{\Delta t \to 0} e \sum_{k=-\infty}^{\infty} G_k N_k h(t - k\Delta t) \tag{5.22}$$

Since the intervals are nonoverlapping, the $\{N_k\}$ are independent Poisson random variables with rate parameter $\lambda(k\Delta t)\Delta t$, and $\{G_k\}$ are also independent random variables with mean M and variance M^2F. Similar to the derivation in [16], the conditional mean and autocorrelation of $I(t)$ can now be determined under the limit $\Delta t \to 0$:

$$E[I_f(t)\,|\,P(.)] = \frac{\eta M e}{h\nu}\int_{-\infty}^{\infty} P(\tau)h(t-\tau)d\tau \tag{5.23}$$

$$\begin{aligned} E[I(t_1)I(t_2)\,|\,P(.)] = {} & \frac{\eta M^2 F e^2}{h\nu}\int_{-\infty}^{\infty} P(\tau)h(t_1-\tau)h(t_2-\tau)d\tau \\ & + \left(\frac{\eta M e}{h\nu}\right)^2 \int_{-\infty}^{\infty} P(\tau)h(t_1-\tau)d\tau \int_{-\infty}^{\infty} P(\tau)h(t_2-\tau)d\tau \end{aligned} \tag{5.24}$$

and we thus have

$$\begin{aligned} E[I_f(t)] &= E[E[I_f(t)\,|\,P(.)]] \\ &= \frac{\eta M e}{h\nu}\int_{-\infty}^{\infty} m_P h(t-\tau)d\tau \\ &= \frac{\eta M e}{h\nu} m_P \int_{-\infty}^{\infty} h(t-\tau)d\tau \\ &= \frac{\eta M e}{h\nu} m_P H(0) \end{aligned} \tag{5.25}$$

where $H(\omega)$ is the receiver transfer function.

$$\begin{aligned} E[I_f(t_1)I_f(t_2)] &= E[I_f(t_1)I_f(t_2)\,|\,P(.)] \\ &= \frac{\eta M^2 F e^2}{h\nu}\int_{-\infty}^{\infty} m_P h(t_1-\tau)h(t_2-\tau)d\tau \\ &\quad + \left(\frac{\eta M e}{h\nu}\right)^2 \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} R_p(u,v)h(t_1-u)h(t_2-v)dudv \end{aligned} \tag{5.26}$$

where m_P and $R_p(u,v)$ are the mean and autocorrelation of the light intensity. The autocovariance of $I_j(t)$ therefore equals:

$$\begin{aligned} L_I(t_1, t_2) &= E[I_j(t_1)I_j(t_2)] - E[I_j(t_1)]E[I_j(t_2)] \\ &= \frac{\eta M^2 Fe^2}{h\nu} m_P \int_{-\infty}^{\infty} h(t_1 - \tau)h(t_2 - \tau)d\tau \\ &+ \left(\frac{\eta Me}{h\nu}\right)^2 \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} L_p(u, v)h(t_1 - u)h(t_2 - v)dudv \end{aligned} \tag{5.27}$$

The spectrum thus equals the Fourier transform of Eq.(5.27):

$$S_I(f) = \left(\frac{\eta M^2 Fe^2}{h\nu} m_P + \left(\frac{\eta Me}{h\nu}\right)^2 S_p(f) \right) |H(f)|^2 \tag{5.28}$$

APPENDIX B: DERIVATION OF EQUATION (5.20)

In this appendix, we will derive the autocovariance and the power spectral density of the light intensity for the most general case of noncoinciding uncorrelated light sources presented in Section 5.3.1. The special cases presented in Section 5.3.2 can be derived from the expressions in this appendix.

The autocovariance, $L_P(\tau)$, is defined as

$$\begin{aligned} L_P(\tau) &= E[(P_{bcond}(t+\tau) - E[P_{bcond}(t+\tau)])\,(P_{bcond}(t) - E[P_{bcond}(t)])] \\ &= \sum_{(m,n)} c_{m,n}^2 E[\cos((\omega_m - \omega_n)(t+\tau) + \Phi_m(t+\tau) - \Phi_n(t+\tau) + \Theta_m - \Theta_n) \cdot \\ &\qquad \cos((\omega_m - \omega_n)t + \Phi_m(t) - \Phi_n(t) + \Theta_m - \Theta_n)] \\ &+ \sum_{(m,n)}\sum_{(p,q)} c_{m,n}c_{p,q} E[\cos((\omega_m - \omega_n)(t+\tau) + \Phi_m(t+\tau) - \Phi_n(t+\tau) + \Theta_m - \Theta_n) \cdot \\ &\qquad \cos((\omega_p - \omega_q)t + \Phi_p(t) - \Phi_q(t) + \Theta_p - \Theta_q)] \end{aligned} \tag{5.29}$$

where $m,p \in \{j, j-1\}$; $n,q \in \{j, j+1\}$; and $m \neq p$, $n \neq q$. Since the phase noise processes from sources m and n are independent, the first term in (5.29) can be expanded to

$$
\begin{aligned}
& c_{m,n}^2 E[\cos((\omega_m-\omega_n)(t+\tau)+\Phi_m(t+\tau)-\Phi_n(t+\tau)+\Theta_m-\Theta_n) \\
& \qquad \cos((\omega_m-\omega_n)t+\Phi_m(t)-\Phi_n(t)+\Theta_m-\Theta_n)] \\
= \; & c_{m,n}^2 E[\{\cos(\omega_m(t+\tau)+\Phi_m(t+\tau)+\Theta_m)\cos(\omega_n(t+\tau)+\Phi_n(t+\tau)+\Theta_n) \\
& \qquad +\sin(\omega_m(t+\tau)+\Phi_m(t+\tau)+\Theta_m)\sin(\omega_n(t+\tau)+\Phi_n(t+\tau)+\Theta_n)\} \\
& \qquad \{\cos(\omega_m t+\Phi_m(t)+\Theta_m)\cos(\omega_n t+\Phi_n(t)+\Theta_n) \\
& \qquad +\sin(\omega_m t+\Phi_m(t)+\Theta_m)\sin(\omega_n t+\Phi_n(t)+\Theta_n)\}] \\
= \; & c_{m,n}^2 (E[\cos(\omega_m(t+\tau)+\Phi_m(t+\tau)+\Theta_m)\cos(\omega_m t+\Phi_m(t)+\Theta_m)] \\
& \qquad E[\cos(\omega_n(t+\tau)+\Phi_n(t+\tau)+\Theta_n)\cos(\omega_n t+\Phi_n(t)+\Theta_n)] \\
& + \; E[\sin(\omega_m(t+\tau)+\Phi_m(t+\tau)+\Theta_m)\cos(\omega_m t+\Phi_m(t)+\Theta_m)] \\
& \qquad E[\sin(\omega_n(t+\tau)+\Phi_n(t+\tau)+\Theta_n)\cos(\omega_n t+\Phi_n(t)+\Theta_n)] \\
& + \; E[\cos(\omega_m(t+\tau)+\Phi_m(t+\tau)+\Theta_m)\sin(\omega_m t+\Phi_m(t)+\Theta_m)] \\
& \qquad E[\cos(\omega_n(t+\tau)+\Phi_n(t+\tau)+\Theta_n)\sin(\omega_n t+\Phi_n(t)+\Theta_n)] \\
& + \; E[\sin(\omega_m(t+\tau)+\Phi_m(t+\tau)+\Theta_m)\sin(\omega_m t+\Phi_m(t)+\Theta_m)] \\
& \qquad E[\sin(\omega_n(t+\tau)+\Phi_n(t+\tau)+\Theta_n)\sin(\omega_n t+\Phi_n(t)+\Theta_n)])
\end{aligned}
\tag{5.30}
$$

In the first term of Eq.(5.30),

$$
\begin{aligned}
& E[\cos(\omega_m(t+\tau)+\Phi_m(t+\tau)+\Theta_m)\cos(\omega_m t+\Phi_m(t)+\Theta_m)] \\
= \; & \frac{1}{2}(E[\cos(\omega_m(t+\tau)+\omega_m t+\Phi_m(t+\tau)+\Phi_m(t)+2\Theta_m)] \\
& + E[\cos(\omega_m(t+\tau)-\omega_m t+\Phi_m(t+\tau)-\Phi_m(t))])
\end{aligned}
\tag{5.31}
$$

Since Θ_m is uniformly distributed over $[0,2\pi]$ and independent of $\Phi(t)$, it can be shown that $E[\cos(\omega_m(t+\tau)+\omega_m t+\Phi_m(t+\tau)+\Phi_m(t)+2\Theta_m)]$ equals zero. Since $\Phi(t)=\int_0^t \dot{\Phi}(\tau)d\tau$, it has been shown in [16] that $\Phi(\tau)=\Phi(t+\tau)-\Phi(t)$ is a Gaussian random variable with mean zero and variance $2\pi\Delta\nu|\tau|$. The expectation of $\cos(\Phi(\tau))$is

$$
E[\cos(\Phi(\tau))] = \frac{1}{2}E[e^{j\Phi(\tau)}+e^{-j\Phi(\tau)}] = e^{-\pi\Delta\nu|\tau|}
\tag{5.32}
$$

while the expectation of $\sin(\Phi(\tau))$ is

$$E[\sin(\Phi(\tau))] = \frac{1}{2j} E[e^{j\Phi(\tau)} - e^{-j\Phi(\tau)}] = 0 \tag{5.33}$$

Equation (5.31) thus equals $1/2\cos(\omega_m\tau)e^{-\pi\Delta\nu|\tau|}$, and it follows that the first term in (5.30) equals $1/4\cos(\omega_m\tau)\cos(\omega_n\tau)e^{-2\pi\Delta\nu|\tau|}$. Similar to (5.31), we can show that the fourth term in (5.30) equals $1/4\cos(\omega_m\tau)\cos(\omega_n\tau)e^{-2\pi\Delta\nu|\nu|}$ while the second and the third terms are both equal to $1/4\sin(\omega_m\tau)\sin(\omega_n\tau)e^{-2\pi\Delta\nu|\nu|}$. The first term in (5.29) thus equals $1/2c_{m,n}^2\cos(\Delta\omega_{m,n}\tau)e^{-2\pi\Delta\nu|\tau|}$ where $\Delta\omega_{m,n} = \omega_m - \omega_n$.

If m,n,p,q are substituted by $j,j-1,j,j+1$, respectively, the second term in (5.29) can be expanded into

$$\begin{aligned}
& c_{j,j-1}c_{j,j+1}E[\cos((\omega_j - \omega_{j-1})(t+\tau) + \Phi_j(t+\tau) - \Phi_{j-1}(t+\tau) + \Theta_j - \Theta_{j-1}) \\
&\qquad \cos((\omega_j - \omega_{j+1})t + \Phi_j(t) - \Phi_{j+1}(t) - \Theta_j - \Theta_{j+1})] \\
&= c_{j,j-1}c_{j,j+1}E[\{\cos(\omega_j(t+\tau) + \Phi_j(t+\tau) + \Theta_j)\cos(\omega_{j-1}(t+\tau) + \Phi_{j-1}(t+\tau) + \Theta_{j-1}) \\
&\qquad + \sin(\omega_j(t+\tau) + \Phi_j(t+\tau) + \Theta_j)\sin(\omega_{j-1}(t+\tau) + \Phi_{j-1}(t+\tau) + \Theta_{j-1})\} \\
&\qquad \{\cos(\omega_j t + \Phi_j(t) + \Theta_j)\cos(\omega_{j+1}t + \Phi_{j+1}(t) + \Theta_{j+1}) \\
&\qquad + \sin(\omega_j t + \Phi_j(t) + \Theta_j)\sin(\omega_{j+1}t + \Phi_{j+1}(t) + \Theta_{j+1})\}] \\
&= c_{j,j-1}c_{j,j+1}\{E[\cos(\omega_j(t+\tau) + \Phi_j(t+\tau) + \Theta_j)\cos(\omega_j t + \Phi_j(t) + \Theta_j)] \\
&\qquad E[\cos(\omega_{j-1}(t+\tau) + \Phi_{j-1}(t+\tau) + \Theta_{j-1})]E[\cos(\omega_{j+1}(t) + \Phi_{j+1}(t) + \Theta_{j+1})] \\
&\qquad + E[\sin(\omega_j(t+\tau) + \Phi_j(t+\tau) + \Theta_j)\cos(\omega_j t + \Phi_j(t) + \Theta_j)] \\
&\qquad E[\sin(\omega_{j-1}(t+\tau) + \Phi_{j-1}(t+\tau) + \Theta_{j-1})]E[\cos(\omega_{j+1}t + \Phi_{j+1}(t) + \Theta_{j+1})] \\
&\qquad + E[\cos(\omega_j(t+\tau) + \Phi_j(t+\tau) + \Theta_j)\sin(\omega_j t + \Phi_j(t) + \Theta_j)] \\
&\qquad E[\cos(\omega_{j-1}(t+\tau) + \Phi_{j-1}(t+\tau) + \Theta_{j-1})]E[\sin(\omega_{j+1}t + \Phi_{j+1}(t) + \Theta_{j+1})] \\
&\qquad + E[\sin(\omega_j(t+\tau) + \Phi_j(t+\tau) + \Theta_j)\sin(\omega_j t + \Phi_j(t) + \Theta_j)] \\
&\qquad E[\sin(\omega_{j-1}(t+\tau) + \Phi_{j-1}(t+\tau) + \Theta_{j-1})]E[\sin(\omega_{j-1}t + \Phi_{j-1}(t) + \Theta_{j-1})]\}
\end{aligned} \tag{5.34}$$

which is zero. Similarly, we can also show that other substitutions in the second term of (5.29) will yield the same result.

The autocovariance $L_p(\tau)$ thus equals

$$L_p(\tau) = \frac{1}{2}(c_{jj-1}^2 \cos(\Delta\omega_{jj-1}\tau) + c_{jj+1}^2 \cos(\Delta\omega_{jj+1}\tau) + c_{j-1j+1}^2 \cos(\Delta\omega_{j-1j+1}\tau))e^{-2\pi\Delta v|\tau|} \tag{5.35}$$

From (5.35) we can determine the double-sided power spectral density:

$$S_{bcond}^P(f) = \frac{\Delta v}{\pi}\left(\frac{c_{jj-1}^2}{(\Delta v)^2 + (f-\Delta f_{jj-1})^2} + \frac{c_{jj+1}^2}{(\Delta v)^2 + (f-\Delta f_{jj+1})^2} + \frac{c_{j-1j+1}^2}{(\Delta v)^2 + (f-\Delta f_{j-1j+1})^2}\right) \tag{5.36}$$

where $\Delta f_{m,n} = \Delta\omega_{m,n}/2\pi$.

APPENDIX C. DERIVATION OF EQUATION (5.24)

It is straightforward to show from definition that the mean of eq. (5.12) is zero. Since Θ and $\Phi(t)$ are independent, the mean of the crosstalk process can be reduced to

$$\begin{aligned}
&E[P_{b_j|b_{j-1}b_{j+1}}(t) - E[P_{b_j|b_{j-1}b_{j+1}}(t)]] \\
&= c_{jj-1}\{E[\cos(\Phi_j(t) - \Phi_{j-1}(t))]E[\cos(\Theta_j - \Theta_{j-1})] \\
&\quad - E[\sin(\Phi_j(t) - \Phi_{j-1}(t))]E[\sin(\Theta_j - \Theta_{j-1})]\} \\
&+ c_{jj+1}\{E[\cos(\Phi_j(t) - \Phi_{j+1}(t))]E[\cos(\Theta_j - \Theta_{j+1})] \\
&\quad - E[\sin(\Phi_j(t) - \Phi_{j+1}(t))]E[\sin(\Theta_j - \Theta_{j+1})]\} \\
&+ c_{j-1j+1}\{E[\cos(\Phi_{j-1}(t) - \Phi_{j+1}(t))]E[\cos(\Theta_{j-1} - \Theta_{j+1})] \\
&\quad - E[\sin(\Phi_{j-1}(t) - \Phi_{j+1}(t))]E[\sin(\Theta_{j-1} - \Theta_{j+1})]\}
\end{aligned} \tag{5.37}$$

Furthermore, since Θ_m and Θ_n are independent, we have

$$E[\cos(\Theta_m - \Theta_n)] = E[\cos\Theta_m]E[\cos\Theta_n] + E[\sin\Theta_m]E[\sin\Theta_n] \tag{5.38}$$

$$E[\sin(\Theta_m - \Theta_n)] = E[\sin\Theta_m]E[\cos\Theta_n] - E[\cos\Theta_m]E[\sin\Theta_n] \tag{5.39}$$

Θ_m and Θ_n are uniformly distributed in $[0, 2\pi]$, $E[\cos\Theta_m]$, $E[\cos\Theta_n]$, $E[\sin\Theta_m]$, and $E[\sin\Theta_n]$ are thus all equal to zero. We can thus conclude that both (5.38) and (5.39) equal zero. It follows that (5.37) also equals zero.

The autocovariance $L_p(\tau)$ is

$$\begin{aligned} L_p(\tau) &= E[\{P_{b_j|b_{j-1}b_{j+1}}(t+\tau) - E[P_{b_j|b_{j-1}b_{j+1}}(t+\tau)]\}\{P_{b_j|b_{j-1}b_{j+1}}(t) - E[P_{b_j|b_{j-1}b_{j+1}}(t)]\}] \\ &= \sum_{(m,n)} c_{m,n}^2 E[\cos(\Phi_m(t+\tau) - \Phi_n(t+\tau) + \Theta_m - \Theta_n) \\ &\qquad \cos(\Phi_m(t) - \Phi_n(t) + \Theta_m - \Theta_n)] \\ &+ \sum_{(m,n)}\sum_{(p,q)} c_{m,n}c_{p,q} E[\cos(\Phi_m(t+\tau) - \Phi_n(t+\tau) + \Theta_m - \Theta_n) \\ &\qquad \cos(\Phi_p(t) - \Phi_q(t) + \Theta_p - \Theta_q)] \end{aligned} \tag{5.40}$$

The first term in (5.40) can be simplified to

$$\begin{aligned} & c_{m,n}^2 E[\cos(\Phi_m(t+\tau) - \Phi_n(t+\tau) + \Theta_m - \Theta_n)\cos(\Phi_m(t) - \Phi_n(t) + \Theta_m - \Theta_n)] \\ &= c_{m,n}^2 E[\{\cos(\Phi_m(t+\tau) + \Theta_m)\cos(\Phi_n(t+\tau) + \Theta_n) + \sin(\Phi_m(t+\tau) + \Theta_m)\sin(\Phi_n(t+\tau) + \Theta_n)\} \\ &\qquad \{\cos(\Phi_m(t) + \Theta_m)\cos(\Phi_n(t) + \Theta_n) + \sin(\Phi_m(t) + \Theta_m)\sin(\Phi_n(t) + \Theta_n)\}] \\ &= c_{m,n}^2\{E[\cos(\Phi_m(t+\tau) + \Theta_m)\cos(\Phi_m(t) + \Theta_m)]E[\cos(\Phi_n(t+\tau) + \Theta_n)\cos(\Phi_n(t) + \Theta_n)] \\ &\quad + E[\sin(\Phi_m(t+\tau) + \Theta_m)\cos(\Phi_m(t) + \Theta_m)]E[\sin(\Phi_n(t+\tau) + \Theta_n)\cos(\Phi_n(t) + \Theta_n)] \\ &\quad + E[\cos(\Phi_m(t+\tau) + \Theta_m)\sin(\Phi_m(t) + \Theta_m)]E[\cos(\Phi_n(t+\tau) + \Theta_n)\sin(\Phi_n(t) + \Theta_n)] \\ &\quad + E[\sin(\Phi_m(t+\tau) + \Theta_m)\sin(\Phi_m(t) + \Theta_m)]E[\sin(\Phi_n(t+\tau) + \Theta_n)\sin(\Phi_n(t) + \Theta_n)]\} \end{aligned} \tag{5.41}$$

In the first term of (5.37),

$$\begin{aligned} & E[\cos(\Phi_m(t+\tau) + \Theta_m)\cos(\Phi_m(t) + \Theta_m)] \\ &= \frac{1}{2}\{E[\cos(\Phi_m(t+\tau) - \Phi_m(t) + 2\Theta_m)] + E[\cos(\Phi_m(t+\tau) - \Phi_m(t))]\} \end{aligned} \tag{5.42}$$

Since Θ_m is uniformly distributed over $[0,2\pi]$ and independent of $\Phi(t)$, it can be shown that $E[\cos(\Phi_m(t+\tau)-\Phi_m(t)+2\Theta_m)]$ equals zero. Since $\Phi(t) = \int_0^t \dot{\Phi}(\tau)d\tau$, it has been shown in [58] that $\Phi(\tau) = \Phi(t+\tau) - \Phi(t)$ is a Gaussian random variable with mean zero and variance $2\pi\Delta\nu|\tau|$. The expectation of $\cos(\Phi(\tau))$is

$$\begin{aligned} E[\cos(\Phi(\tau))] &= \frac{1}{2}E[e^{j\Phi(\tau)} + e^{-j\Phi(\tau)}] \\ &= e^{-\pi\Delta\nu|\tau|} \end{aligned} \tag{5.43}$$

while the expectation of $\sin(\Phi(\tau))$ is

$$\begin{aligned} E[\sin(\Phi(\tau))] &= \frac{1}{2j}E[e^{j\Phi(\tau)} - e^{-j\Phi(\tau)}] \\ &= 0 \end{aligned} \tag{5.44}$$

Equation (5.42) thus equals $1/2e^{-\pi\Delta\nu|\tau|}$, and it follows that the first term in Eq.(5.41) equals $1/4e^{-2\pi\Delta\nu|\tau|}$. Using similar technique as used for (5.42), we can show that both of the second and the third term in (5.41) are zero, and the fourth term is $1/4e^{-2\pi\Delta\nu|\tau|}$. (5.41), or the first term in (5.40), thus equals $1/2c_{m,n}^2e^{-2\pi\Delta\nu|\tau|}$. If m,n,p,q are substituted by $j,j-1,j,j+1$, respectively, the second term in (5.40) can be expanded into

$$
\begin{aligned}
& c_{j,j-1}c_{j,j+1}E[\cos(\Phi_j(t+\tau)-\Phi_{j-1}(t+\tau)+\Theta_j-\Theta_{j-1}) \\
& \qquad \cos(\Phi_j(t)-\Phi_{j+1}(t)-\Theta_j-\Theta_{j+1})] \\
= \; & c_{j,j-1}c_{j,j+1}E[\{\cos(\Phi_j(t+\tau)+\Theta_j)\cos(\Phi_{j-1}(t+\tau)+\Theta_{j-1}) \\
& \qquad + \sin(\Phi_j(t+\tau)+\Theta_j)\sin(\Phi_{j-1}(t+\tau)+\Theta_{j-1})\} \\
& \qquad \{\cos(\Phi_j(t)+\Theta_j)\cos(\Phi_{j+1}(t)+\Theta_{j+1}) \\
& \qquad + \sin(\Phi_j(t)+\Theta_j)\sin(\Phi_{j+1}(t)+\Theta_{j+1})\}] \\
= \; & c_{j,j-1}c_{j,j+1}\{E[\cos(\Phi_j(t+\tau)+\Theta_j)\cos(\Phi_j(t)+\Theta_j)] \\
& \qquad E[\cos(\Phi_{j-1}(t+\tau)+\Theta_{j-1})]E[\cos(\Phi_{j+1}(t)+\Theta_{j+1})] \\
& \quad + E[\sin(\Phi_j(t+\tau)+\Theta_j)\cos(\Phi_j(t)+\Theta_j)] \\
& \qquad E[\sin(\Phi_{j-1}(t+\tau)+\Theta_{j-1})]E[\cos(\Phi_{j+1}(t)+\Theta_{j+1})] \\
& \quad + E[\cos(\Phi_j(t+\tau)+\Theta_j)\sin(\Phi_j(t)+\Theta_j)] \\
& \qquad E[\cos(\Phi_{j-1}(t+\tau)+\Theta_{j-1})]E[\sin(\Phi_{j+1}(t)+\Theta_{j+1})] \\
& \quad + E[\sin(\Phi_j(t+\tau)+\Theta_j)\sin(\Phi_j(t)+\Theta_j)] \\
& \qquad E[\sin(\Phi_{j-1}(t+\tau)+\Theta_{j-1})]E[\sin(\Phi_{j-1}(t)+\Theta_{j-1})]\}
\end{aligned}
\tag{5.45}
$$

which is zero. Similarly, we can also show other substitutions in the second term of (5.40) will yield the same result. Therefore, the autocovariance $L_p(\tau)$ is

$$
L_p(\tau) = \frac{1}{2}(c_{j,j-1}^2 + c_{j,j+1}^2 + c_{j-1,j+1}^2)e^{-2\pi\Delta\nu|\tau|} \tag{5.46}
$$

CHAPTER 6 DENSE WDM/WDMA SYSTEMS

6.1 Introduction

In Chapter 5, we have evaluated the maximum density of a dense waveguide array for optical interconnects at the MCM, board, and backplane levels. For this chapter, instead of exploiting density in space, we exploit density in wavelength. The wiring density of an optical backplane system can be relaxed by multiplexing more than one wavelength into the same fiber/waveguide. The wavelength-division multiplexed (WDM) systems or the wavelength-division multiple access (WDMA) systems using on-off modulation or frequency shift keying and direct detection have recently been shown to be a practical system solution for utilizing the vast bandwidth offered by the optical fibers/waveguide [77].[15] A typical N-channel WDM/WDMA backplane consists of a fixed wavelength single-mode semiconductor laser diode such as the distributed feedback (DFB) laser as the transmitter, an optical amplifier, and an optical filter such as the tunable Fabry-Perot (FP) filter at the receiver end, as shown in Figure 6-1. Optical amplifiers such as Er^{3+} doped fiber amplifier [78] whose large bandwidth (~30 nm) and high gain (~30 dB) further suggest that such a backplane with large fanout can be implemented.

Direct on-off modulation of the single-mode laser diode introduces significant frequency excursion or chirp during the transients of the on and off levels [79]. The frequency chirping is the result of the nonlinear interaction between photons and carriers. The sudden increase in current density disturbs the system from equilibrium, generating a train of relaxation oscillations on the carrier density and the optical refractive index of the laser medium. The laser emission wavelength will shift correspondingly. Strong damping prevents these oscillations from continuing for more than a few periods. Frequency chirp typically ranges from 0.2-0.8 nm, based upon experimental observation [79].

---

[15] A significant portion of this chapter is adapted from C.-S. Li, F. Tong, K. Liu, and D. G. Messerschmitt, "Channel Capacity Optimization of Chirp Limited Dense WDM/WDMA Systems Using OOK Modulation and Optical Filters," *IEEE Journal of Lightwave Technology*. (c) IEEE. Reprinted with permission.

When passing through an optical filter, the chirped signal may suffer degradation when the filter bandwidth is comparable to or smaller than the chirp width. The imperfect optical filter response also allows crosstalk from adjacent channels. The combined chirp and crosstalk effects thus limit the ultimate channel capacity of a direct modulation dense WDM/WDMA system. It is therefore important to determine the maximum number of channels of such a system, and the optimal operating conditions for the lasers and the optical filters. In this chapter, we choose a set of typical laser parameters and, assuming this laser, we concentrate on systems which operate at speed faster than 1 Gbps and use a Fabry-Perot filter as the optical filter.

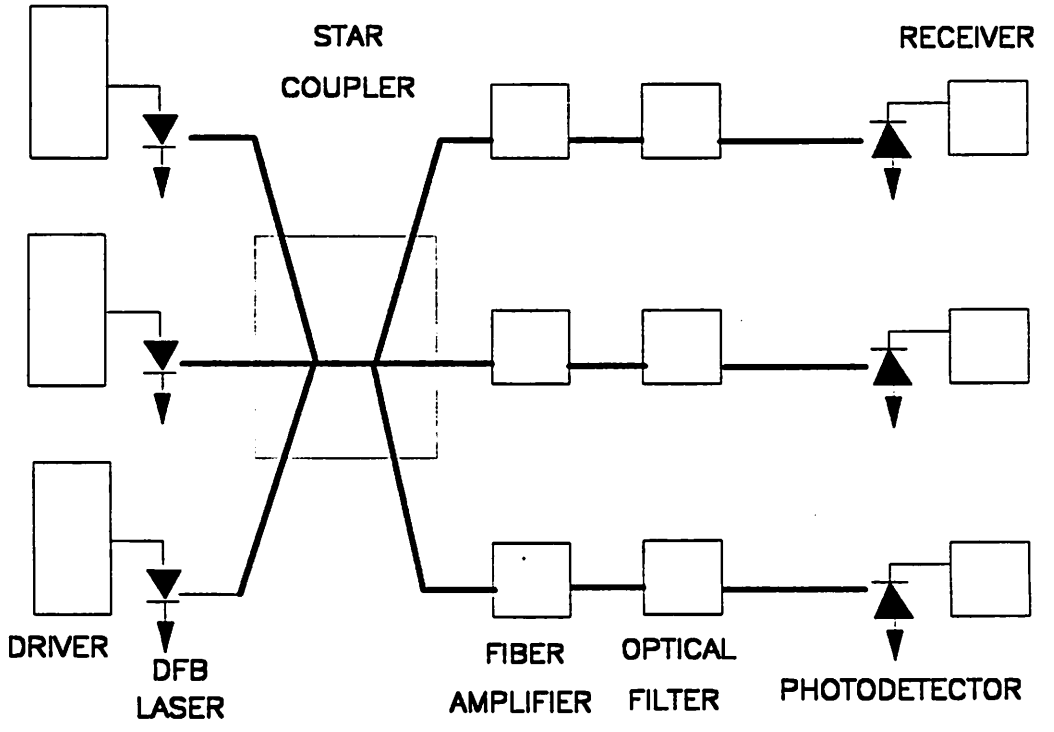

Figure 6-1. Architecture of a typical N-channel WDM/WDMA backplane. In this structure, single-mode lasers are used as transmitters and fixed-tuned or tunable Fabry-Perot filters are used as wavelength selective elements.

Both analytical approaches [79, 80] and simulation approaches [81-83] have been pursued to evaluate the laser chirp effect, but these focused only on the penalty induced by fiber dispersion for long-haul communication systems. Chirp-induced penalty through FP filters has not yet been analyzed. Crosstalk in FP filters has been analyzed in [84], but the chirp effect was largely ignored in this calculation.

There are several results in this chapter:

- A simulation model for a dense WDM/WDMA system has been developed.
- Over 100 stations can be accommodated with each station operating at 2 Gbps.
- At bit rates larger than 1 Gbps, a power penalty of greater than 1 dB is induced when the filter bandwidth is comparable to or less than the chirp width.
- For a multiple channel system, there exists an optimal optical filter bandwidth which minimizes the combined crosstalk and chirp penalty.
- There are optimal operating conditions for the laser and the filter such that the induced penalty is minimized.

The organization of this chapter is as follows: Section 2 describes and justifies the the eye-degradation criterion for obtaining the system penalty. Section 3 describes the system simulation model. Simulation results are presented in Section 4 and system optimization results are presented in Section 5. Simulation results of a WDM system using FSK scheme is discussed in Section 6. Conclusions are given in Section 7.

6.2 Derivation of System Penalty

Two types of interference are introduced by the system under consideration: *intra-channel interference* and *inter-channel interference*. The intra-channel interference (or inter-symbol interference) occurs when the chirp bandwidth is comparable to or larger than the optical filter bandwidth, thus causing the loss of a fraction of optical power in the transmitted bit stream. The inter-channel interference is caused by the chirp, which substantially increases the bandwidth of the signals of the

adjacent channels, as well as the response of the optical filter, which allows crosstalk from adjacent channels.

In general, it is difficult to determine the power penalty for a given system. There exist a variety of error bounds and approximation techniques to estimate the effect of intersymbol interference, such as the truncated-pulse-approximation [82, 85, 86], worst-case bound [87], Chernoff bound [88], worst possible distribution bound [89], series-expansion bound [85], or moment-space bound [90]. However, these approaches usually rely on a prior knowledge of the distribution of bit patterns, and most of them assume that each bit has equal probability of being a ONE or ZERO. In computer communications, especially in computer bus communications when coding or scrambling is not generally assumed, these assumptions do not hold. One approach that does not require these assumptions uses the eye closure criterion [91], which we shall adopt throughout this study.

The eye pattern is generated by superimposing the simulated outputs from all of the possible M-bit sequences [81], In order to observe the pattern dependency of the frequency chirp, M has to be larger than the channel memory to account for all possible intersymbol interference. For the operating conditions simulated in this chapter, the channel memory has been determined to be less than three bits. Considering the intersymbol interference generated from the previous two bits and the following bit, we superimpose all possible patterns from a 8-bit sequence and examine the eye opening of the fourth bit.

A typical eye pattern for a nonreturn-to-zero (NRZ) coded waveform is shown in Figure 6-2. Both of the vertical and horizontal eye degradation are evaluated in this chapter. The vertical eye degradation is defined as

$$ED_V = \frac{ED_1 + ED_0}{S_1 - S_0} \tag{6.1}$$

where S_1 and S_0 are the steady state signal levels for logical ONE and ZERO, respectively, and ED_1 and ED_0 are the respective signal level deviation compared with the steady state levels. The

fully opened horizontal eye equals the bit interval, T. The horizontal eye degradation can thus be expressed as

$$ED_H = \frac{T - EO_H}{T} \tag{6.2}$$

where EO_H is the horizontal eye opening.

The power penalty of the NRZ waveform can be derived from the vertical eye degradation:

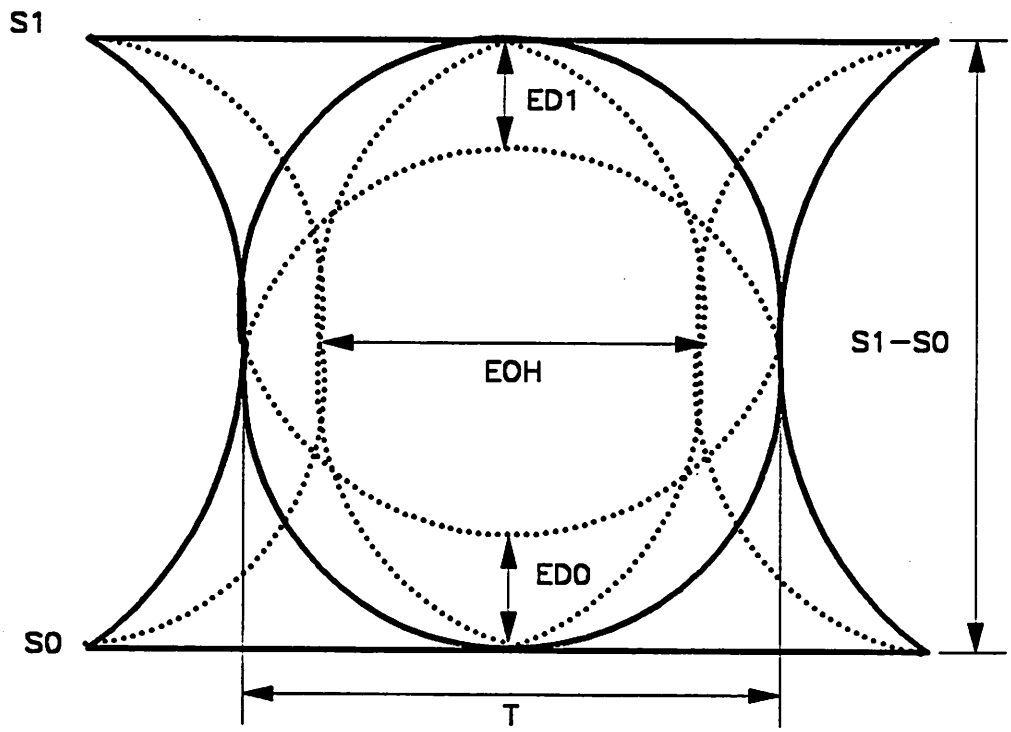

Figure 6-2. A typical eye pattern showing the horizontal and vertical eye opening.. S_1 and S_0 are the signal level for ONE and ZERO, respectively; ED_1 and ED_0 are the degradation of the eye opening from ideal signal levels; and EO_H is the horizontal eye opening and T is the bit period.

$$P_{penalty}(dB) = 10\log_{10}ED_V \tag{6.3}$$

This power penalty is a measure of the additional power in dB required to achieve the ideal eye opening.[16] The horizontal eye degradation gives rise to the waveform jitter. Waveform jitter affects the receiver timing recovery, increases the variance of receiver sampling instants, and introduces timing error to the receiver. Its effects can also be translated into system penalty. However, the exact calculation of the system penalty due to timing jitter [92] depends on the type of the timing recovery circuitry used in the receiver and is not pursued here.

6.3 Simulation Models

The system simulated in this chapter is shown in Figure 6-3, and consists of, in order, a laser driver, a single-mode DFB laser, a single-mode fiber of length up to 200 *cm*, a Fabry-Perot optical filter, and a lightwave receiver. The values of the parameters used in the simulation are summarized in Table 1. The model of each component is provided as below:

(1) *Laser Driver*

The NRZ current pulse shape, $I_p(t)$, generated from the laser driver depends on the previous and the current bit. This is given by

$$I_p(t) = \begin{cases} I_{bias} + I_m(1 - {}_{th}e^{-\frac{2.2t}{\tau_r}}) & \text{if current bit} = 1, \text{previous bit} = 0 \\ I_{bias} + I_m e^{-\frac{2.2t}{\tau_r}} & \text{if current bit} = 0, \text{previous bit} = 1 \\ I_{bias} & \text{if current bit} = 0, \text{previous bit} = 0 \\ I_{bias} + I_m & \text{if current bit} = 1, \text{previous bit} = 1 \end{cases} \tag{6.4}$$

where I_{bias} is the bias current, I_m is the modulation current, and τ_r is the 10% to 90% rise time and fall time of the modulation current. This rise time τ_r is related to the time constant of the laser

[16] In order to relate this expression to the bit-error-rate, the eye opening has to be properly weighted according to the distribution of the bit patterns. For bit patterns with equal distribution, the average eye opening can be used to calculate the bit-error-rate.

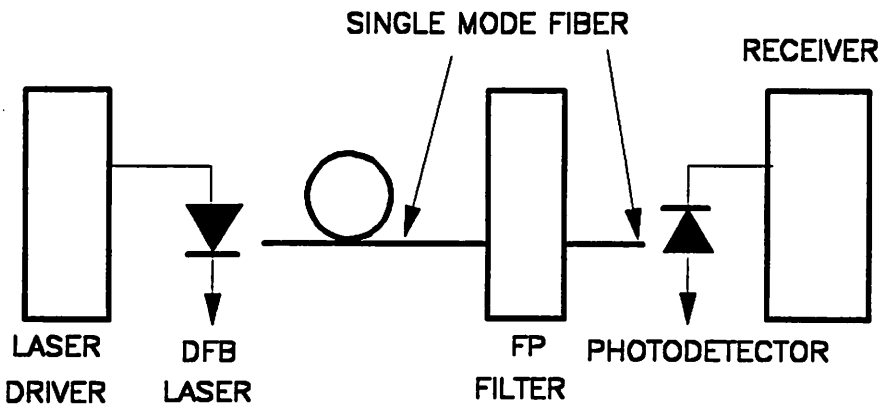

Figure 6-3. System configuration for a single channel.. If crosstalk is considered, N single mode laser emitting at N different wavelengths are used in the simulation.

parasitics given by $\tau_r = 2.2RC$, where R and C are the corresponding laser parasitic resistance and capacitance.

(2) *Single-Mode DFB Laser*

• The dynamics of a single-mode semiconductor diode laser can be modelled by the laser rate equations [93], which describe the interactions between the photon density $p(t)$, carrier density $n(t)$, and the phase of the electric field $\phi(t)$:

$$\frac{dp(t)}{dt} = \Gamma G(t)(n(t) - n_0)p(t) - \frac{p(t)}{\tau_p} + \frac{\beta\Gamma n(t)}{\tau_n} \tag{6.5}$$

$$\frac{dn(t)}{dt} = \frac{I_p(t)}{qV_a} - G(t)(n(t) - n_0)p(t) - \frac{n(t)}{\tau_n} \tag{6.6}$$

$$\frac{d\phi(t)}{dt} = \frac{\alpha}{2}\left(\Gamma v_g a_0(n(t) - n_0) - \frac{1}{\tau_p}\right) \tag{6.7}$$

In these equations, Γ is the mode confinement factor, n_0 is the carrier density at transparency, τ_p is the photon lifetime, β is the fraction of spontaneous emission coupled into the lasing mode, τ_n is the carrier recombination lifetime, q is the electron charge, V_a is the active layer volume, v_g is the group velocity, a_0 is the gain coefficient, α is the linewidth enhancement factor. The parameter $G(t)$ is the saturable gain coefficient defined by

$$G(t) = \frac{v_g a_0}{1 + \varepsilon p(t)} \tag{6.8}$$

where ε is the gain compression factor. This semiclassical treatment does not distinguish between the particle and wave nature of light. Thus the photon density and the electric field of the optical wave are used interchangeably [82]. By numerically integrating Eq.(6.5-6.7) using injected current from Eq.(6.4), we obtain the optical power emitted per facet $P(t)$ and the instantaneous chirp frequency $\Delta\nu(t)$:

$$P(t) = \frac{p(t)}{2}\frac{V_a \eta_0 h\nu}{\Gamma\tau_p} \tag{6.9}$$

and

$$\Delta\nu(t) = \frac{1}{2\pi}\frac{d\phi(t)}{dt} \tag{6.10}$$

where η_0 is the differential quantum efficiency of the laser performance. It can be shown that by substituting Eq.(6.5) and (6.7) into Eq.(6.10), the frequency chirp $\Delta\nu(t)$ can be simplified to [94, 95]

$$\Delta\nu(t) = \frac{\alpha}{4\pi}\left\{\frac{1}{p(t)}\frac{dp(t)}{dt} + [\frac{\varepsilon}{\tau_p} - \frac{\beta\Gamma n(t)}{\tau_n p(t)}]\right\} \tag{6.11}$$

The first term in this expression is the *transient* chirp, while the second term is the *adiabatic* chirp [81]. Due to its derivative nature, the transient chirp occurs when the laser is turned on or off. Adiabatic chirp occurs as a result of spontaneous emission and gain suppression and causes frequency offset between the steady state on and off levels during modulation. Note that α and ε have a strong effect on the frequency chirp. Devices with lower value of α, such as multiple-quantum-well lasers, exhibit smaller chirp [96].

(3) *Single-Mode Fiber*

The electric field at the output end of the fiber in the frequency domain is given by

$$S_{fiber}(f) = H_{fiber}(f)S_s(f) \tag{6.12}$$

where

$$H_{fiber}(f) = e^{j\frac{\pi\lambda^2 D\ell f^2}{c}} \tag{6.13}$$

[97] and

$$S_s(f) = \int_{t=-\infty}^{\infty} \sqrt{P(t)}\, e^{j\phi(t)} e^{-j2\pi ft} dt \tag{6.14}$$

The coefficient D is the fiber dispersion parameter, ℓ is the fiber length, λ is the optical wavelength, and c is the velocity of light.

(4) *Fabry-Perot Filter*

Likewise, the electric field at the output side of the FP filter in the frequency domain is given by

$$S_{FP}(f) = H_{FP}(f)S_{fiber}(f) \tag{6.15}$$

where H_{FP} is the frequency domain transfer function [98], given by

$$H_{FP}(f) = \frac{T}{1 - Re^{j2\pi\frac{(f-f_c)}{FSR}}} \tag{6.16}$$

where T and R are the power transmission coefficient and the power reflection coefficient of the filter, respectively. The parameter f_c is the center frequency of the filter. The parameter FSR is the *free spectral range* at which the transmission peaks are repeated and can be defined as $FSR = c/2\mu L$, where L is the FP cavity length and μ is the refractive index of the FP cavity. The 3 dB transmission bandwidth FWHM (*full width at half maximum*) of the FP filter is related to FSR and F:

$$FWHM = \frac{FSR}{F} \tag{6.17}$$

where the *finesse* F of the FP filter is defined as

$$F = \frac{\pi\sqrt{R}}{1-R} \tag{6.18}$$

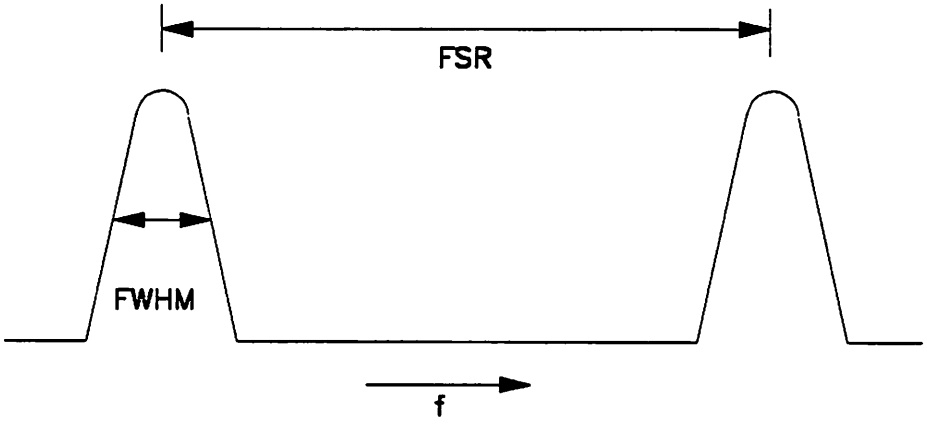

Figure 6-4. Frequency response of a Fabry-Perot filter.

These parameters are represented in Figure 6-4. Note that models describing the single-mode fiber and the FP filter are both linear with respect to the electric field. The results are thus independent of the placement order of the fiber and the FP filter.

(5) *Lightwave Receiver*

The lightwave receiver is modeled by a photodetector followed by a linear pulse-shaping filter. The photo-current from the photodetector is related to the incident optical power $P_{FP}(t)$ by

$$i(t) = \frac{\eta\lambda}{hc} P_{FP}(t) + \lambda_0 \tag{6.19}$$

where η is the quantum efficiency of the photodetector and λ_0 is the dark current. $P_{FP}(t)$ can be calculated from $S_{FP}(f)$:

$$P_{FP}(t) = s_{FP}(t)s^*_{FP}(t) \tag{6.20}$$

where $s_{FP}(t)$ is the inverse Fourier transform of $S_{FP}(f)$. The photocurrent $i(t)$ is convolved with a receiver filter with Gaussian-shaped frequency response

$$H_R(f) = e^{-\pi(\frac{f}{2f_R})^2} \tag{6.21}$$

where $f_R = 0.75/T$, and T is the bit period. This particular filter bandwidth is chosen in an attempt to minimize the receiver noise while maximizing the eye opening.

(6) *Crosstalk Model*

Previous system models only consider the degradation of a single channel in the presence of laser chirp and a FP filter. Here, we consider the signal degradation in the presence of crosstalk channels. Crosstalk from adjacent channels has been of primary concern for a dense WDM or WDMA system. We consider a WDM or WDMA system consisting of N channels equally spaced Δf apart. In order to estimate the worst-case interference pattern, all of the $N - 1$ stations are assumed to be transmitting the same interfering patterns synchronously. The total interfering spectrum, $S_{int}(f)$ becomes

$$S_{int}(f) = \sum_{i=1}^{N-1} S_i(f - i\Delta f)e^{-j2\pi f t_d} \tag{6.22}$$

where $S_i(f - i\Delta f)$ is the spectrum of the i^{th} channel and t_d is the phase difference between the interfering channels and the signal channel. The total transmission including the signal $S_S(f)$ through the FP filter is

$$S_{total}(f) = H_{FP}(f)[S_s(f) + S_{int}(f)] \tag{6.23}$$

The same eye-closure criterion can be applied to obtain the performance of a multiple channel system as was used in the single channel case.

Notation	Definition	Value
Γ	mode confinement factor	0.4
n_0	electron density at transparency	$10^{18} cm^{-3}$
τ_p	photon lifetime	3 ps
τ_n	electron lifetime	1 ns
β	spontaneous emission factor	3×10^{-5}
q	electron charge	1.6×10^{-19} C
V_a	Active volume	$1.5 \times 10^{-10} cm^3$
α	linewidth enhancement factor	5
v_g	group velocity	$8.5 \times 10^9 cm/s$
a_0	gain coefficient	$2.5 \times 10^{-16} cm^2$
η_0	total quantum efficiency	0.4
ε	gain suppression factor	$10^{-17} cm^3$
η	photodetector quantum efficiency	0.8
λ_0	dark current	6.25×10^{10}/ sec
D	fiber dispersion constant	$-17 ps/km/nm$

TABLE 1. DEFINITION AND VALUE OF THE PARAMETERS USED IN THIS CHAPTER.

6.4 Simulation

Of all the parameters describing the system, the parameters that can be varied experimentally have been limited to a few, namely,

- the laser bias current, I_{bias},
- the modulation current, I_m,

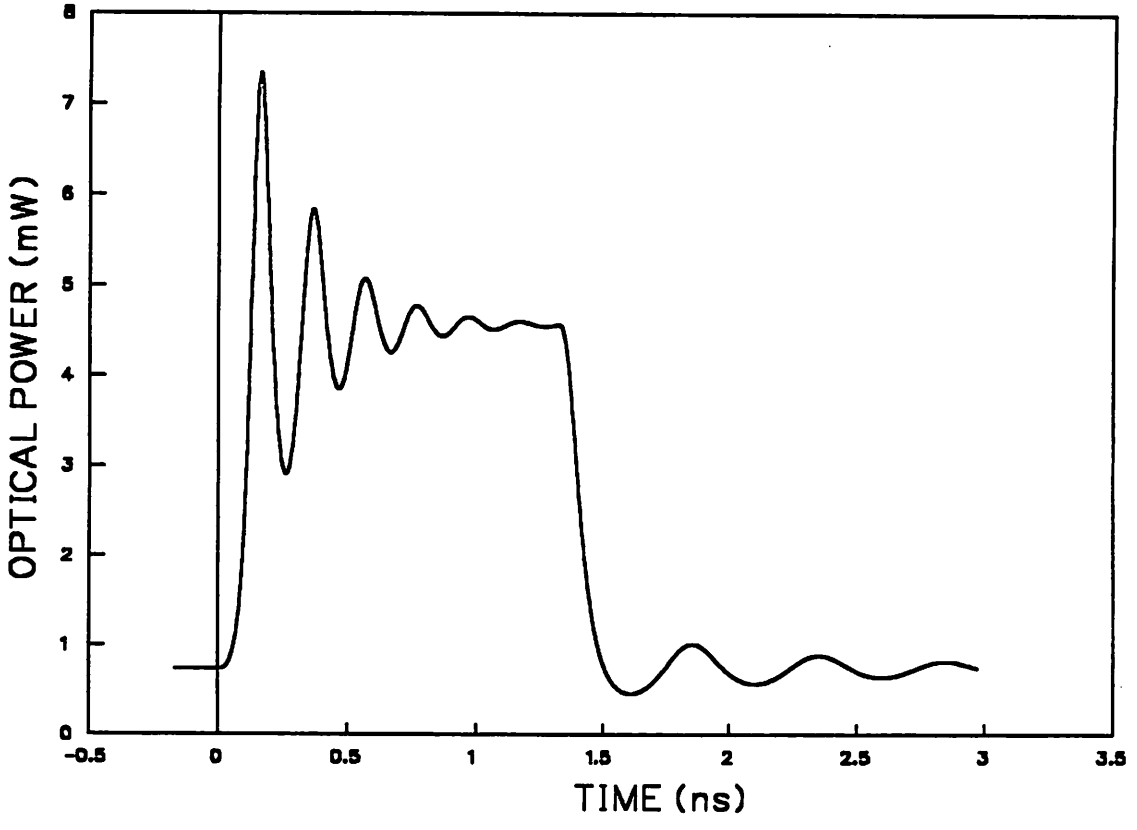

Figure 6-5. Simulated output of instantaneous optical power of a DFB laser using bit pattern 0011110000. The operating parameters are: bit rate $B = 3Gbps$, normalized bias current $I_b/I_{th} = 1.16$, rise time of the drive current $t_r = 1/2T$, and extinction ratio $r = 0.16$.

- the rise time of the driving current, t_r,
- the bit rate, B, or the bit period, $1/T$,
- the position of the center frequency, f_c,
- the 3dB bandwidth of the FP filter, *FWHM*.

In order to match the optical amplifier bandwidth, the FSR is fixed at 3.7 THz, corresponding to 30 nm at 1.55 μm. In changing the filter bandwidth, the finesse is also changed correspondingly to preserve the total FSR. The center frequency of the FP filter has been fixed at half way between the steady state ONE bit and ZERO bit. The relatively short length in our model ($\ell < 200$ cm)

causes insignificant dispersion. To maintain the same optical power reaching the FP filter, the total driving current to the laser during the ONE bit is maintained at

$$I_T = I_{bias} + I_m = 1.85 I_{th} \tag{6.24}$$

Note that the bias current here is used for the driving current of a ZERO bit and is larger than the lasing threshold, which has been simulated to be 33.5 mA. The bias current normalized to the threshold current I_{th} ranges from 1.0 to 1.2. The ratio

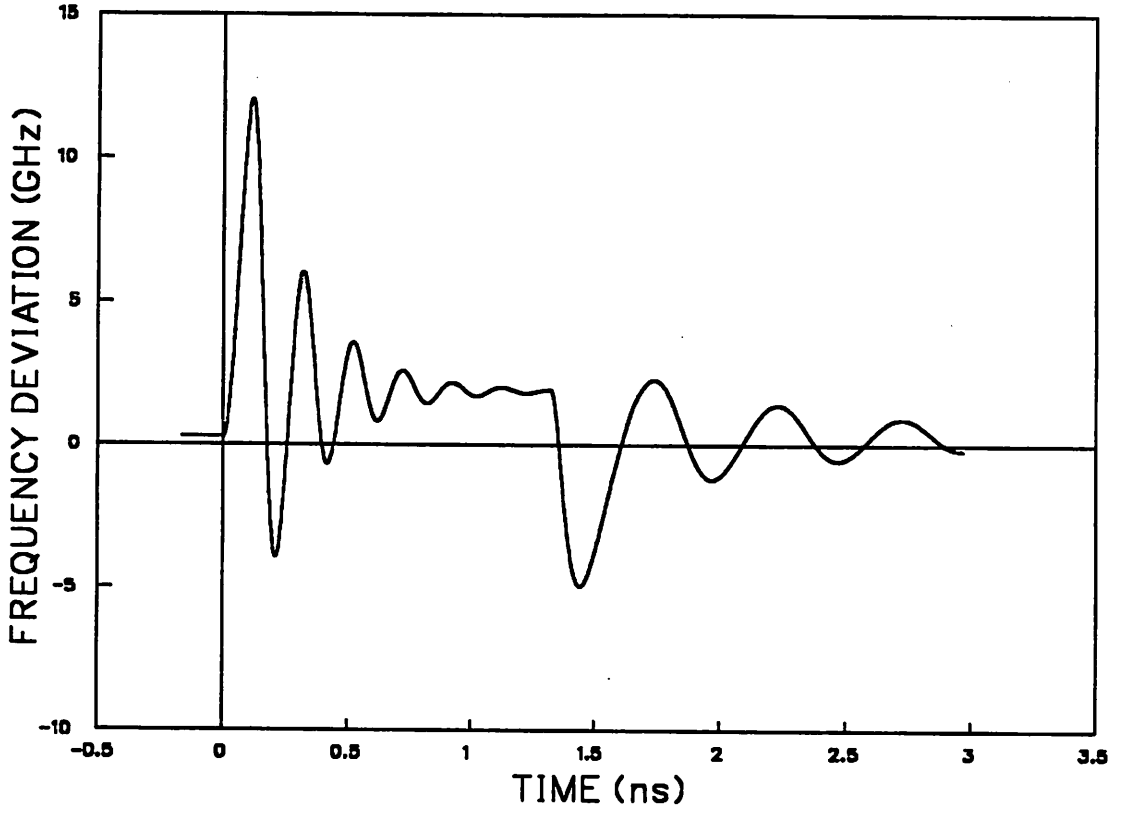

Figure 6-6. Simulated output of instantaneous chirp frequency of a DFB laser using bit pattern 0011110000.

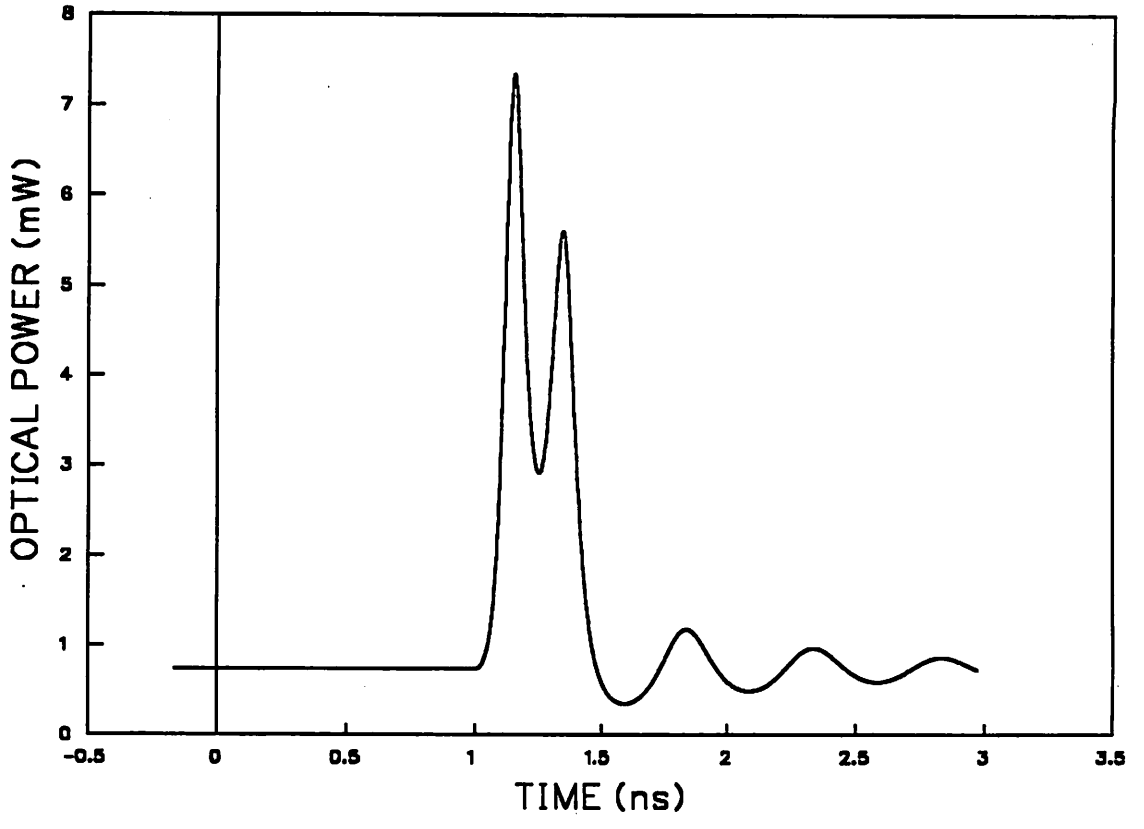

Figure 6-7. Simulated output of instantaneous optical power of a DFB laser using bit pattern 0000010000. The operating conditions are same as in Figure 6-5.

$$r = \frac{S_0}{S_1} \tag{6.25}$$

is defined to be the *extinction ratio* of the signal and ranges from 0.02 to 0.16 in our simulations. The rise time of the laser driving current can be related to the bit period by

$$t_r = xT = \frac{x}{B_r} \qquad x < 1 \tag{6.26}$$

A fourth-order Runge-Kutta method is used to integrate the laser rate equations. Figure 6-5, Figure 6-6, Figure 6-7, Figure 6-8, Figure 6-9 and Figure 6-10 show the instantaneous optical power and emission frequency of the laser for bit pattern 0011110000, 0000010000, and 0001010000 at 3 Gbps. These figures demonstrate that the relaxation oscillation and frequency excursion are pattern dependent. As shown in Figure 6-5 and Figure 6-6, the laser is modulated by a pattern 0011110000. The relaxation oscillation frequency is found to be 5 GHz for the ONE bit and 2 GHz for the ZERO bit. We designate frequency chirp offset of 0 GHz corresponding to laser emission frequency at threshold. In Figure 6-6, the corresponding transient chirp spans from −5 GHz to 12 GHz during the the first cycle of oscillation. The adiabatic chirp is found to be less than 2 GHz.

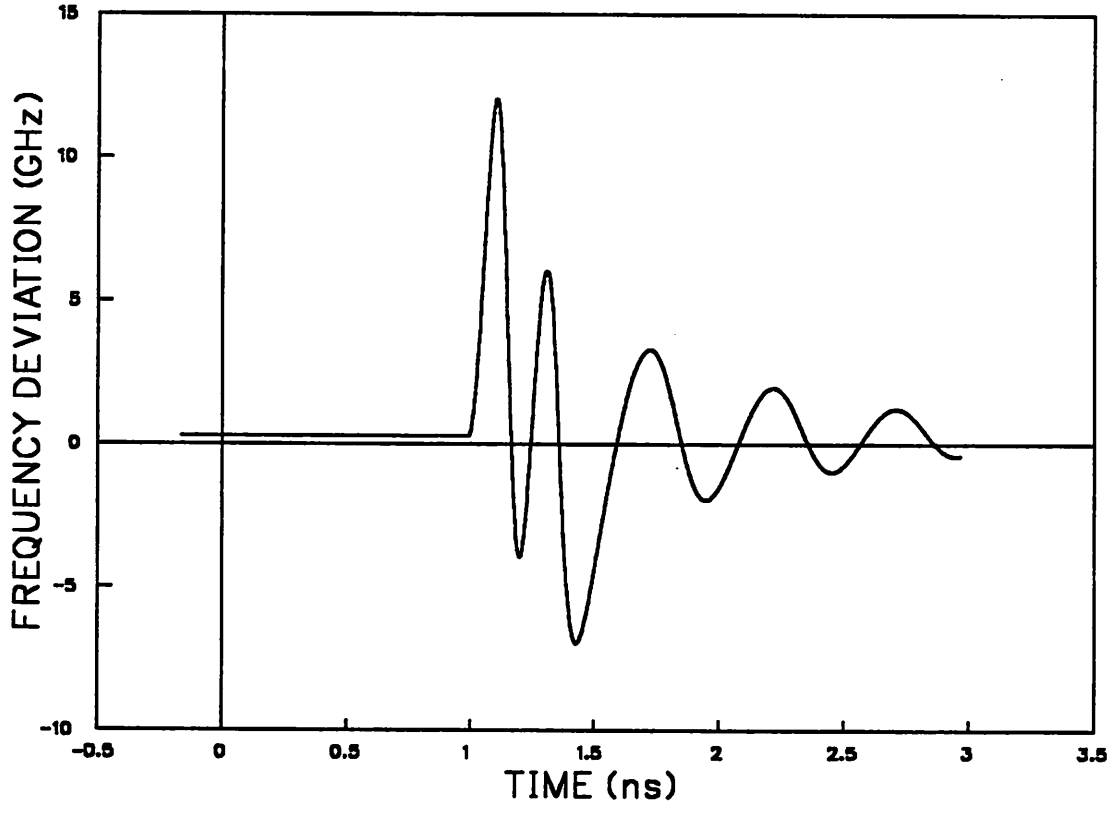

Figure 6-8. Simulated output of instantaneous chirp frequency of a DFB laser using bit pattern 0000010000.

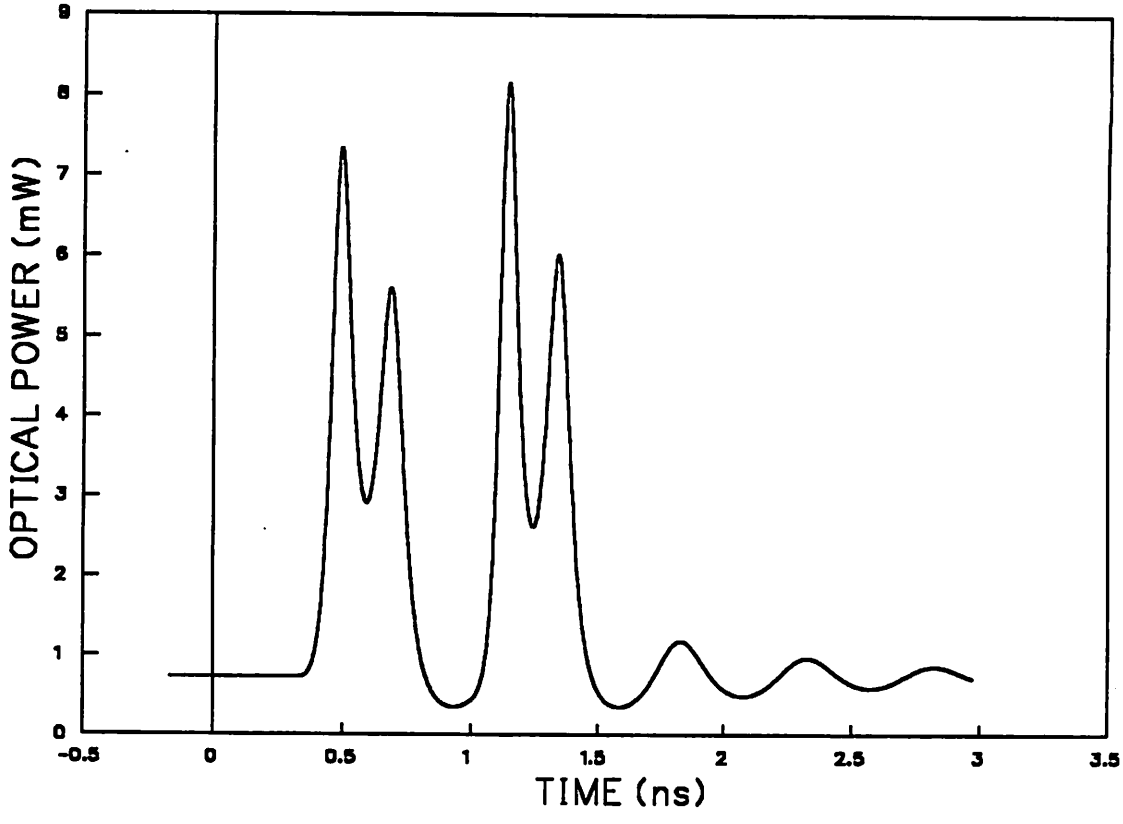

Figure 6-9. Simulated output of instantaneous optical power of a DFB laser using bit pattern 0001010000. The operating conditions are same as Figure 6-5.

These values are close to those obtained from experiments [85]. Figure 6-7 and Figure 6-8 show the case in which the laser is modulated by a bit sequence 0000010000. The number of relaxation oscillations are limited to 2 cycles by the duration of the ONE bit, which is 330 ps. The height of the optical pulses and the frequency excursion are similar to those generated by the sequence 0011110000. However, as the bit pattern changes to 0001010000, as shown in Figure 6-9 and Figure 6-10, there are increases in peak optical power and maximum frequency excursion in the second ONE bit of the pattern. The maximum frequency excursion during the first relaxation oscillation of the second ONE bit is 20% more than the first relaxation oscillation in the first ONE

bit. The corresponding peak power also increases by 11%. This increase in chirp is due to undershooting in the carrier density during the preceding ZERO.

Figure 6-11 and Figure 6-12 show the eye patterns from a single channel system operated at 3 Gbps. Careful observation of these eye patterns reveals that different bit patterns are responsible for the closing of the upper trace and the lower trace of the eye. As shown in the figures, pattern 0010100000 is responsible for closing the upper trace of the eye while pattern 0010010000 is responsible for closing the lower trace of the eye. The effect of introducing an FP filter is illustrated in Figure 6-11. By comparing Figure 6-11 and Figure 6-12, one can observe immediately that the

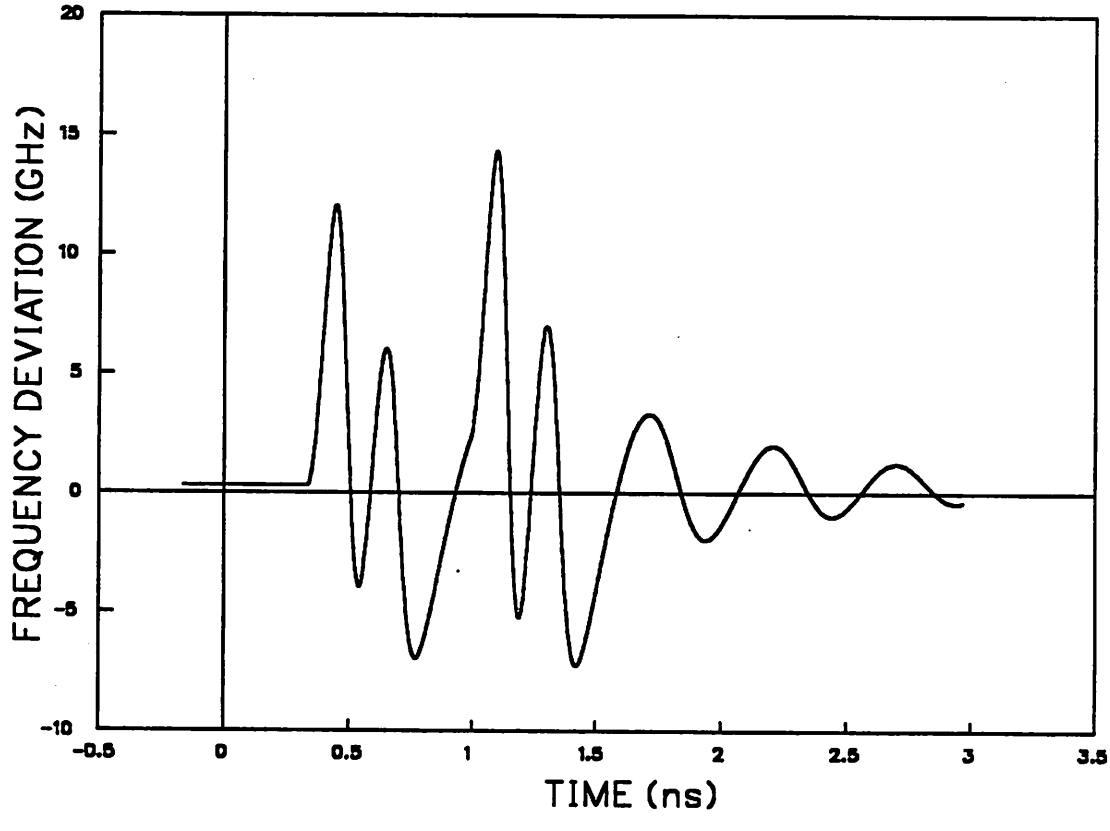

Figure 6-10. Simulated output of instantaneous chirp frequency of a DFB laser using bit pattern 0001010000.

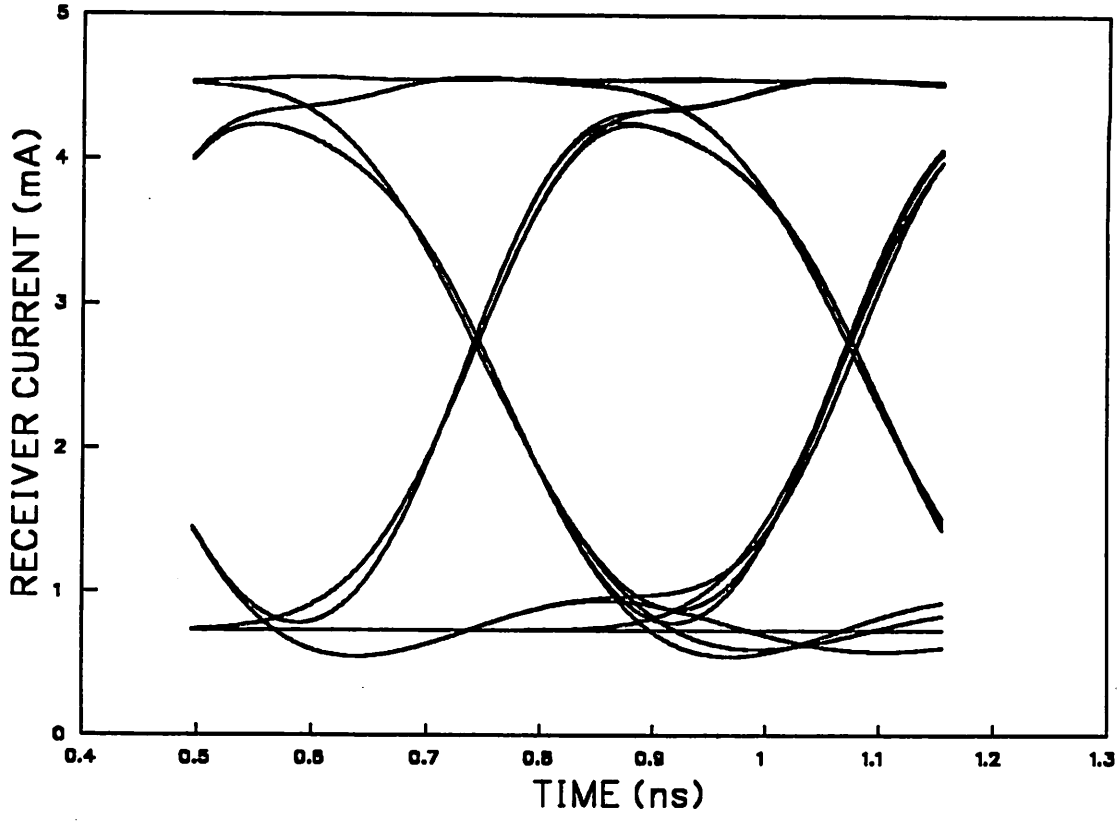

Figure 6-11. Simulated eye pattern in the absence of a FP filter. The system parameters are $B = 3.33Gbps$, $I_{bias}/I_{th} = 1.16$, and $t_r = 0.5T$.

eye pattern degrades significantly after an FP filter of 20 GHz bandwidth with center frequency at 0 GHz is introduced, as not all of the optical power falls on the receiver.

(1) *Single Channel System*

Using the criterion given in Eq. (6.3), we show in Figure 6-13 the power penalty as a function of bit rate for various FP filter bandwidths. In these simulations, the normalized bias current and the extinction ratio are set at 1.12 and 0.16 respectively for all bit rates. The rise time of the laser driving current equals one half the bit period. Simulation data in the absence of the FP filter are also presented for comparison. Without the FP filter, the power penalty is minimized at 5 Gbps, corresponding to the relaxation oscillation frequency of the ONE bit. The large response at laser

relaxation oscillation frequency increases the eye-opening, thus causes a dip in the power penalty characteristics. For the bit rate larger than the relaxation oscillation frequency, the penalty increases sharply from 1 dB to 4 dB over 1 Gbps range of increment.

For an FP filter bandwidth larger than that of the chirp, there is little degradation in the eye opening. As the filter bandwidth approaches the chirp bandwidth, there is a substantial increase in power penalty. At FWHM equal to 4 GHz, which is much smaller than the chirp bandwidth, the additional power penalty reaches as much as 7 dB at 4 Gbps. One can observe that for the filter bandwidth considered, the increase in power penalty always occurs at a bit rate higher than 1 Gbps,

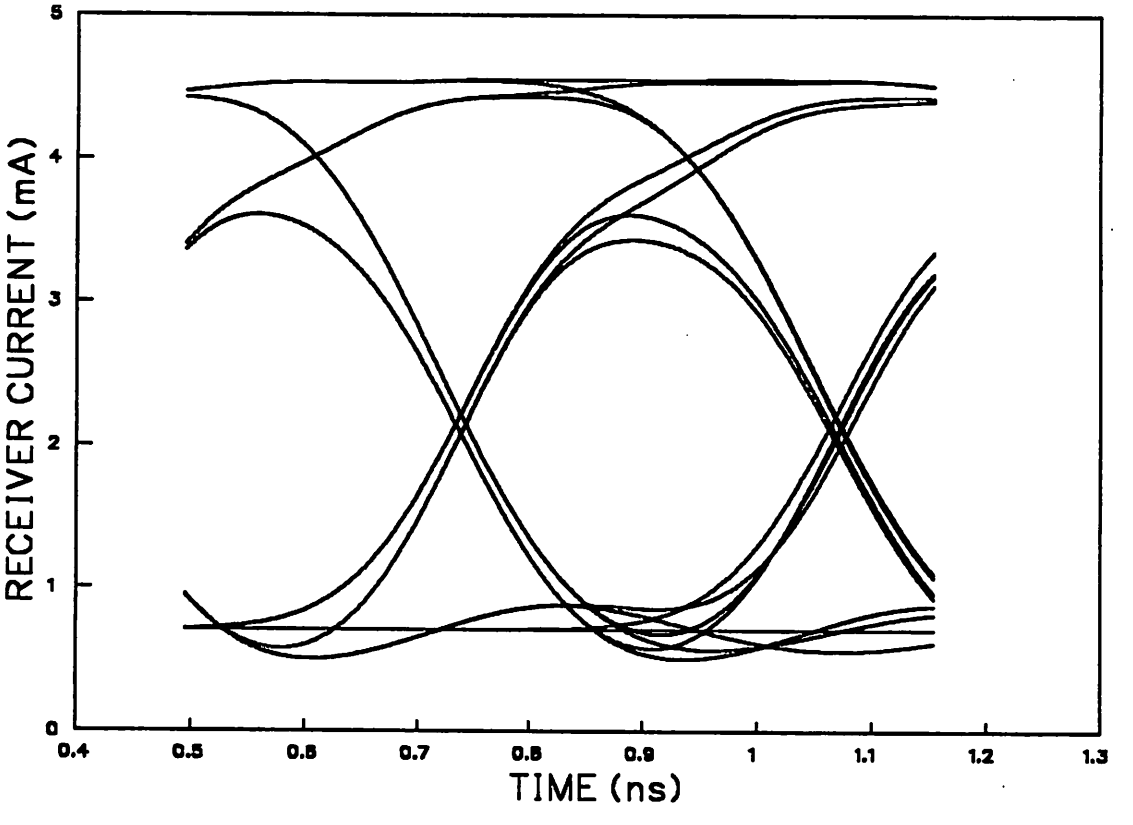

Figure 6-12. Simulated eye pattern in the presence of a FP filter with bandwidth = 20 GHz. The system parameters are the same as in Figure 6-11.

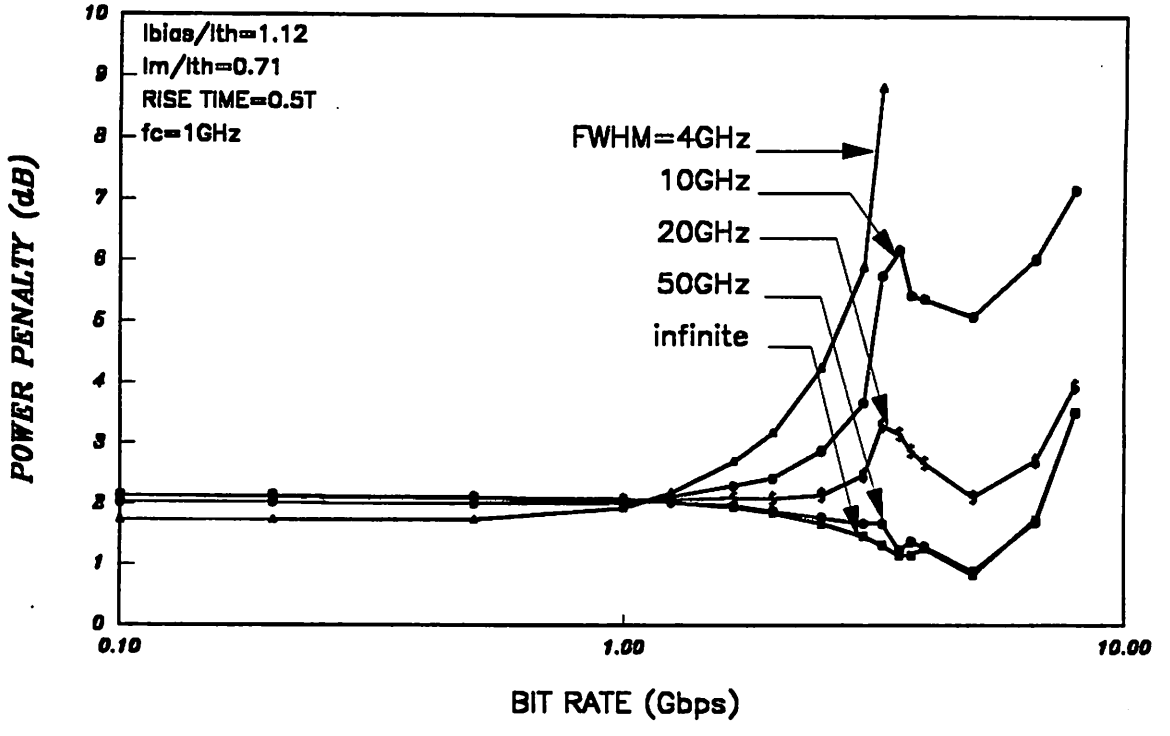

Figure 6-13. Power penalty versus bit rate for various filter bandwidth.

and remains fairly constant at bit rate less than 1 Gbps. The results indicate that a dense WDMA system using FP filters may operate up to 1 Gbps before chirp becomes a dominant limitation.

Examination of these curves in Figure 6-13 also reveals that the power penalty is smaller for filters with a small bandwidth than for those with a large bandwidth at bit rates less than 1 Gbps. This effect is further demonstrated in Figure 6-14 and Figure 6-15, in which degradation of the ONE bit and the ZERO bit are analyzed separately. As shown in these two figures, the degradation of the ONE bit increases monotonically with the decrease of the filter bandwidth while the degradation of the ZERO bit decreases monotonically with the decrease of the filter bandwidth. The improvement of the level ZERO is more than the degradation of the level ONE, and thus accounts for the overall decrease of power penalty at lower bit rate. Furthermore, we can observe that there

is a dip of eye degradation for the ONE bit at 5 Gbps while there is a peak of eye degradation for the ZERO bit at 2 Gbps. The former effect arises from the relaxation oscillation frequency of the ONE bit and the latter from the relaxation oscillation frequency of the ZERO bit.

For a filter bandwidth of 10 GHz, as shown in Figure 6-16, the degradation of ZERO decreases while the degradation of ONE increases with the increase of bit rate. These two effects cancel out each other at low bit rate, and the overall power penalty thus remains essentially constant. At a higher bit rate, the degradation of ONE begins to dominate, and the overall power penalty degrades sharply.

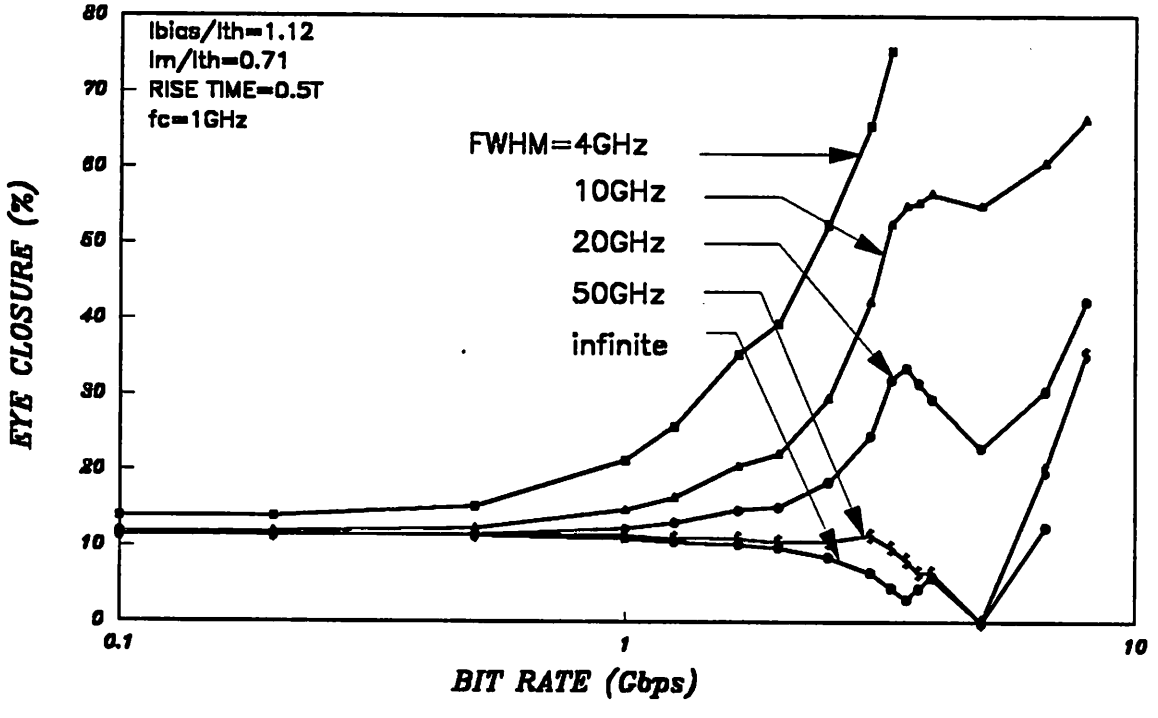

Figure 6-14. Eye degradation from the ideal ONE signal level as a function of bit rate.

The horizontal eye-opening is also measured and the waveform jitter is extracted as a function of bit rate at various FP filter bandwidths, as shown in Figure 6-17. There is a substantial increase of horizontal eye closure, as defined by Eq.(6.2), at a bit rate larger than 3 Gbps. A narrower filter bandwidth gives rise to sharper increase in horizontal eye-closure. This degradation can be as dramatic as 70% at 3 Gbps for filter bandwidth equals 4 GHz.

Figure 6-18 plots the power penalty as a function of filter bandwidth at a fixed bit rate of 2 Gbps for various biasing levels. The normalized bias current is set at 1.12, 1.06 and 1.00 and the rise time is set at one half of the bit rate. As shown in this figure, the power penalty maintains a fairly constant value for filter bandwidth larger than 30 GHz. The increase in power penalty occurs at filter bandwidth close to one half of the maximum chirp width. In reducing the biasing current,

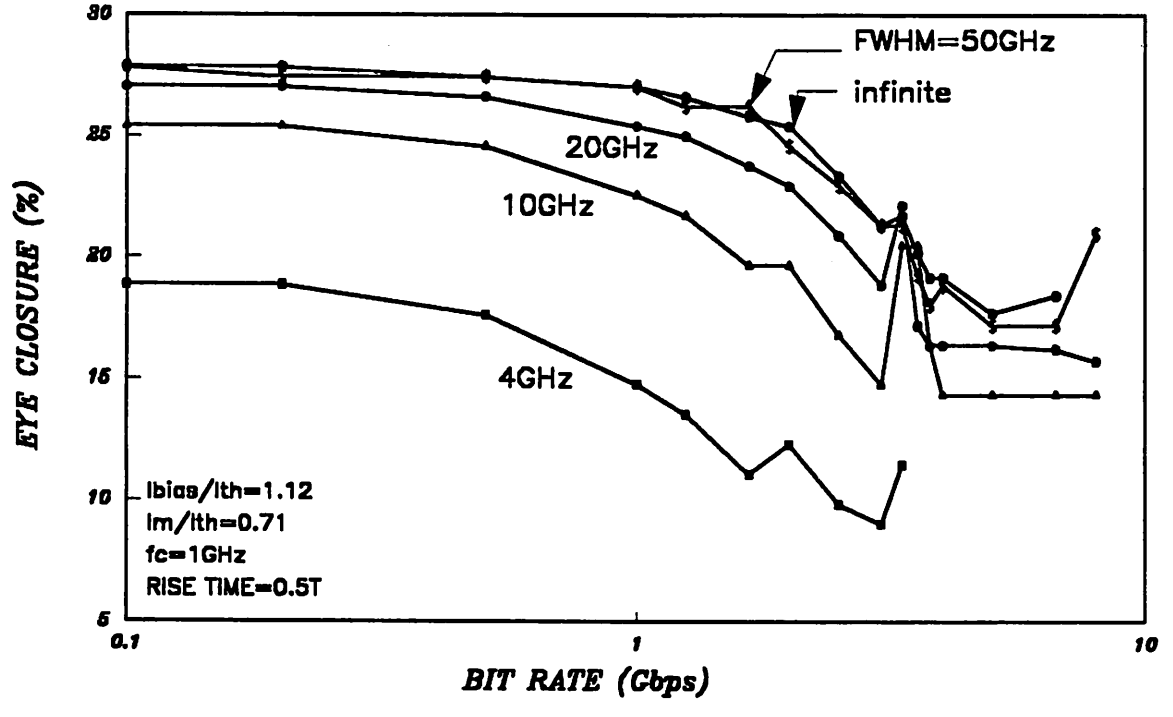

Figure 6-15. Eye degradation from the ideal ZERO signal level as a function of bit rate.

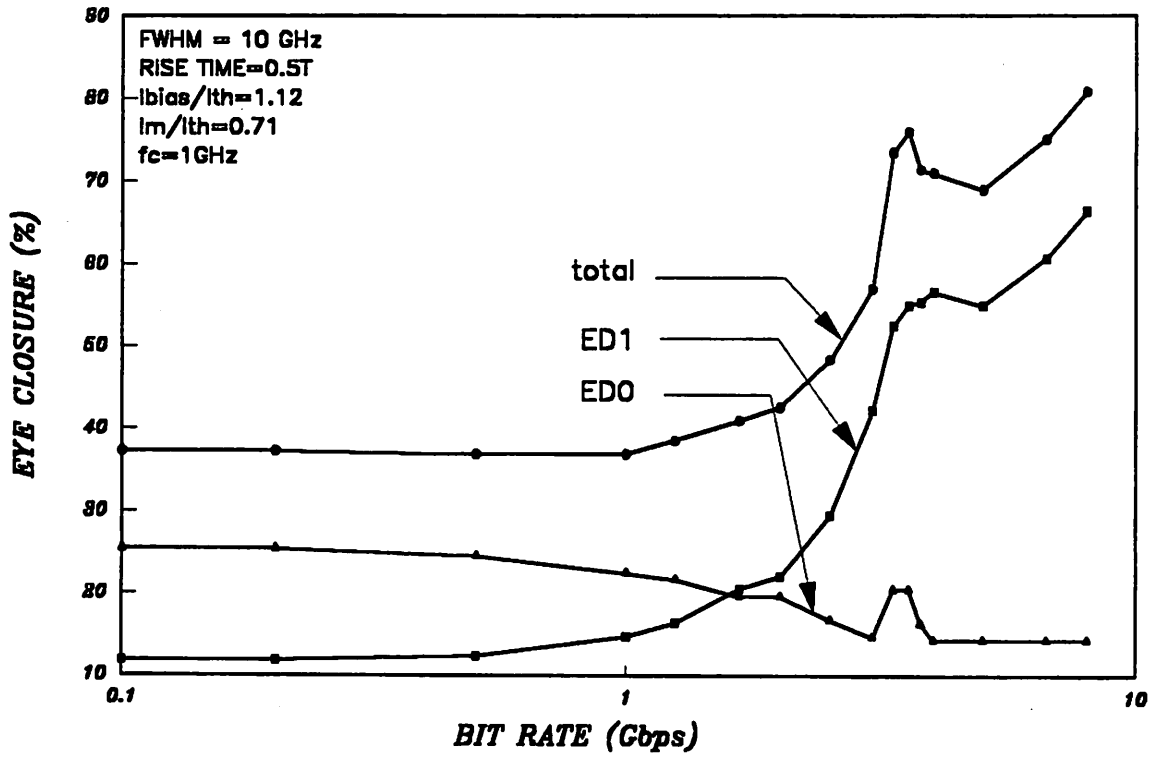

Figure 6-16. Eye-closure as a function of bit rate.. $FWHM = 10$ GHz. The peaks at $3GHz$ and at $5GHz$ are the relaxation oscillation frequencies at the applied currents for the ZERO and ONE bit, respectively. The total eye degradation is also displayed.

the extinction ratio decreases and a lower power penalty results. Horizontal eye closure of the same set of data displays a similar trend in Figure 6-18. A considerable increase in eye closure occurs for filter bandwidth larger than 20 GHz. Note that these curves (for normalized bias current equals 1.0, 1.06, and 1.12) are the reverse of those of the power penalty. This can be attributed to the fact that smaller biasing current introduces stronger initial relaxation oscillations and degrades the horizontal eye-closure.

(2) *Multi-channel System*

The presence of interfering channels degrades the eye opening and increases the system penalty and waveform jitter, so we must include not only the intra-channel effects of the preceding sub-

section, but also the inter-channel effects. Figure 6-20 shows the power penalty as a function of the time skew between the interfering channels and the signal channel for a system with 128 channels and 256 channels using a fixed-bandwidth FP filter of 12 GHz. The penalty is periodic and is maximized within each bit period when the interfering channels synchronize with the signal channel. Synchronization between the interfering channels and the signal channel will thus be used to obtain the worst case system performance for the rest of this section. Figure 6-21 shows the power penalty as a function of number of stations operating at 1, 2, and 3 Gbps using a fixed filter bandwidth. As discussed in the previous section, the stations are distributed across the entire free spectral range of the FP filter with equal channel spacing. The constant penalty for a small number of stations is mainly contributed by the intra-channel chirp effects, as just analyzed (Figure 6-19

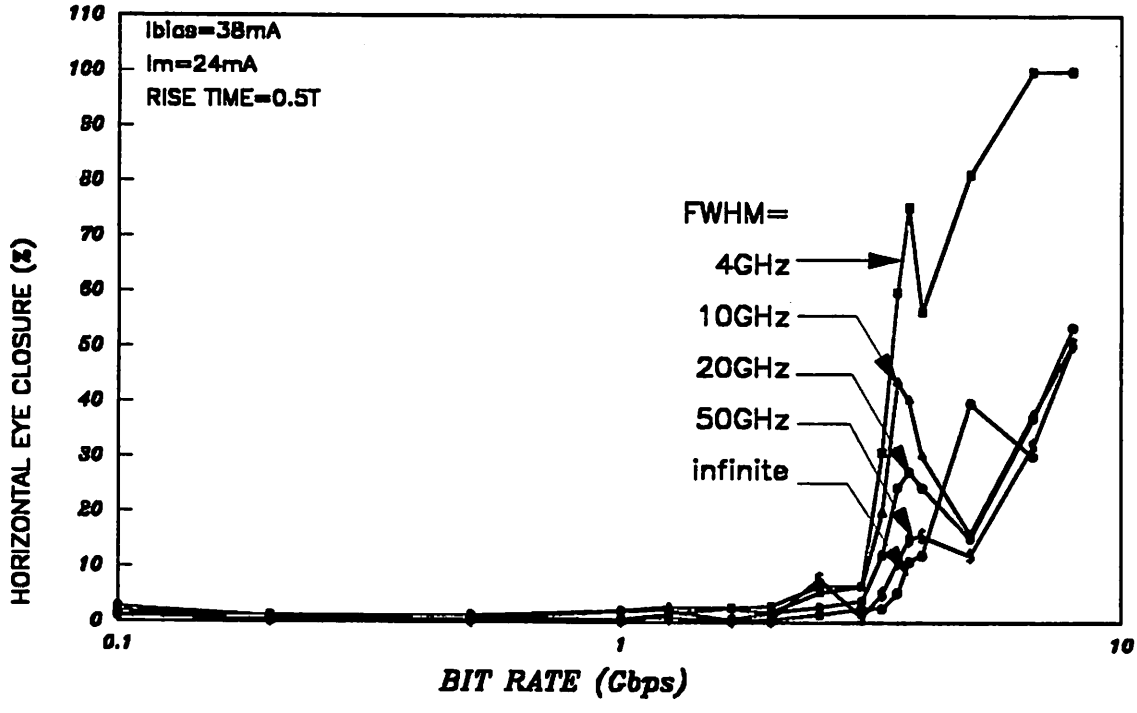

Figure 6-17. Horizontal eye closure versus bit rate at various filter bandwidth.

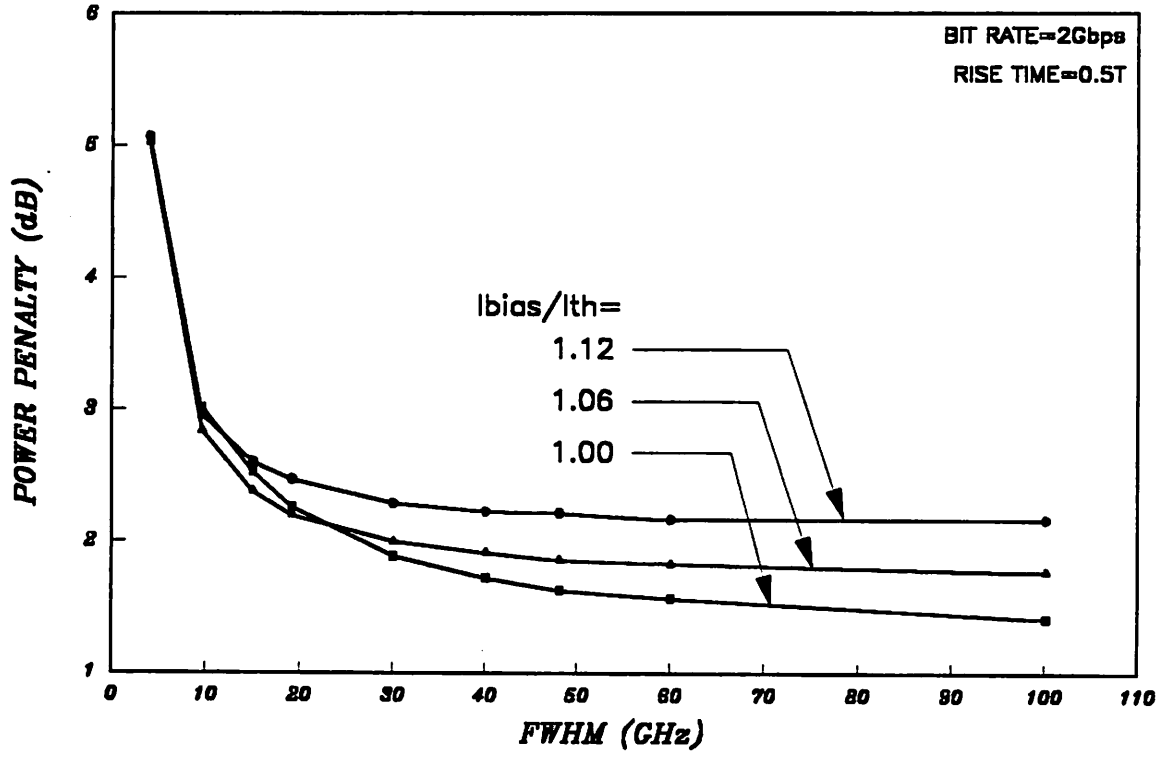

Figure 6-18. Power penalty as a function of FWHM. I_{bias}/I_{th}= 1.12, 1.06, and 1.00.

and Figure 6-18); the crosstalk is insignificant in this case. The performances curves of the 1 and 2 Gbps cases are similar, though the 2 Gbps suffers a larger penalty resulting from the chirping of the signal channel alone. The 3 Gbps case displays a even larger intra-channel chirp penalty, a 3.5dB increase as compared with the 1 Gbps case. As the number of stations increases, the cross-talk penalty from adjacent channels begin to dominate. All three curves show a substantial increase in total system penalty as N exceeds 100, indicating that a system with capacity of no more than 100-130 stations can be achieved before the chirp effect reaches unacceptable levels.

Figure 6-22, Figure 6-23, Figure 6-24 and Figure 6-25 illustrate the filter-bandwidth dependency of the system penalty. Figure 6-22 displays the power penalty versus the number of stations for filter bandwidth of 10, 20, and 30 GHz. All stations are transmitting at 2 Gbps. For a small

number of stations, smaller filter bandwidths have more intra-channel signal distortion. This trend is completely reversed for large number of stations because the crosstalk from adjacent channels becomes the dominant source of signal interference and smaller bandwidths allow less crosstalk. These results are further compared in Figure 6-23, with those reported in [84] in which only the steady-state crosstalk effect is considered, and frequency chirping from any station is ignored. The power penalty as calculated without chirp and with chirp are consistent for small number of stations. The constant offset for small number of stations is due to the nonzero extinction ratio and finite signal rise time for laser modulation and chirp penalty induced by the FP filter. The system penalty from chirp rises sharply for large number of stations as compared to the nonchirp results. This can be attributed to the nonzero chirp width occupied by the interfering channels.

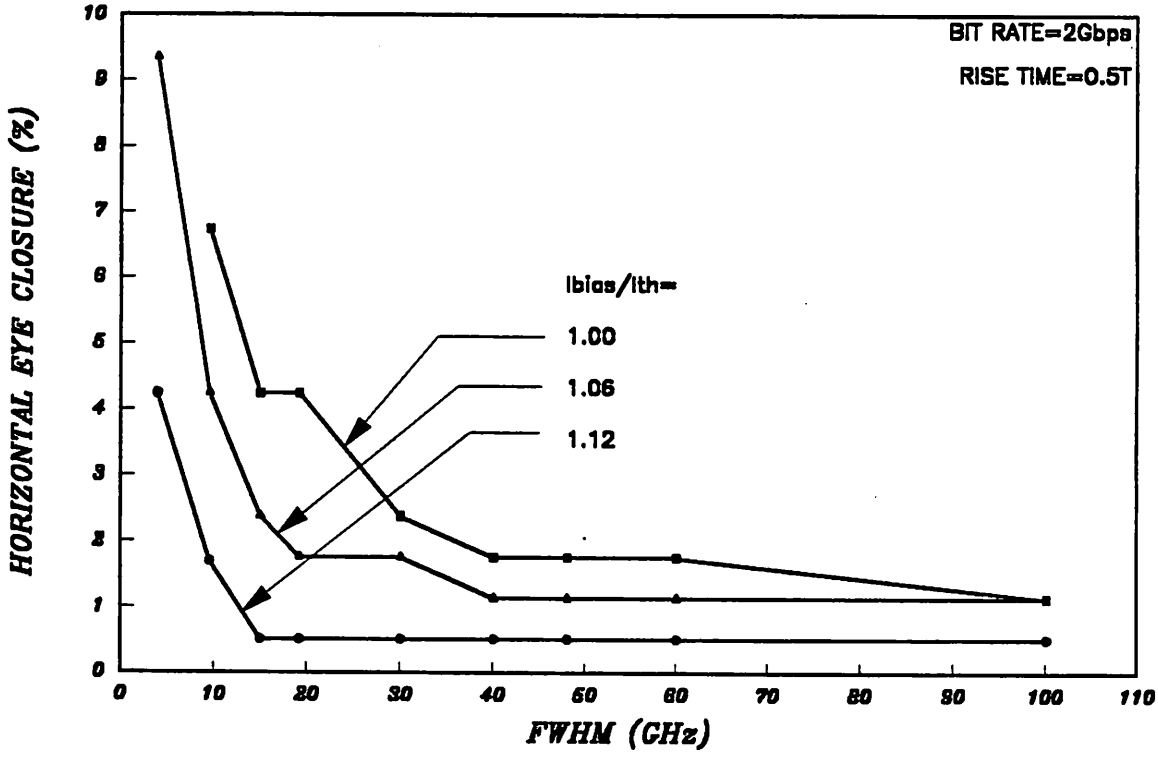

Figure 6-19. Horizontal eye-closure as a function of FWHM.

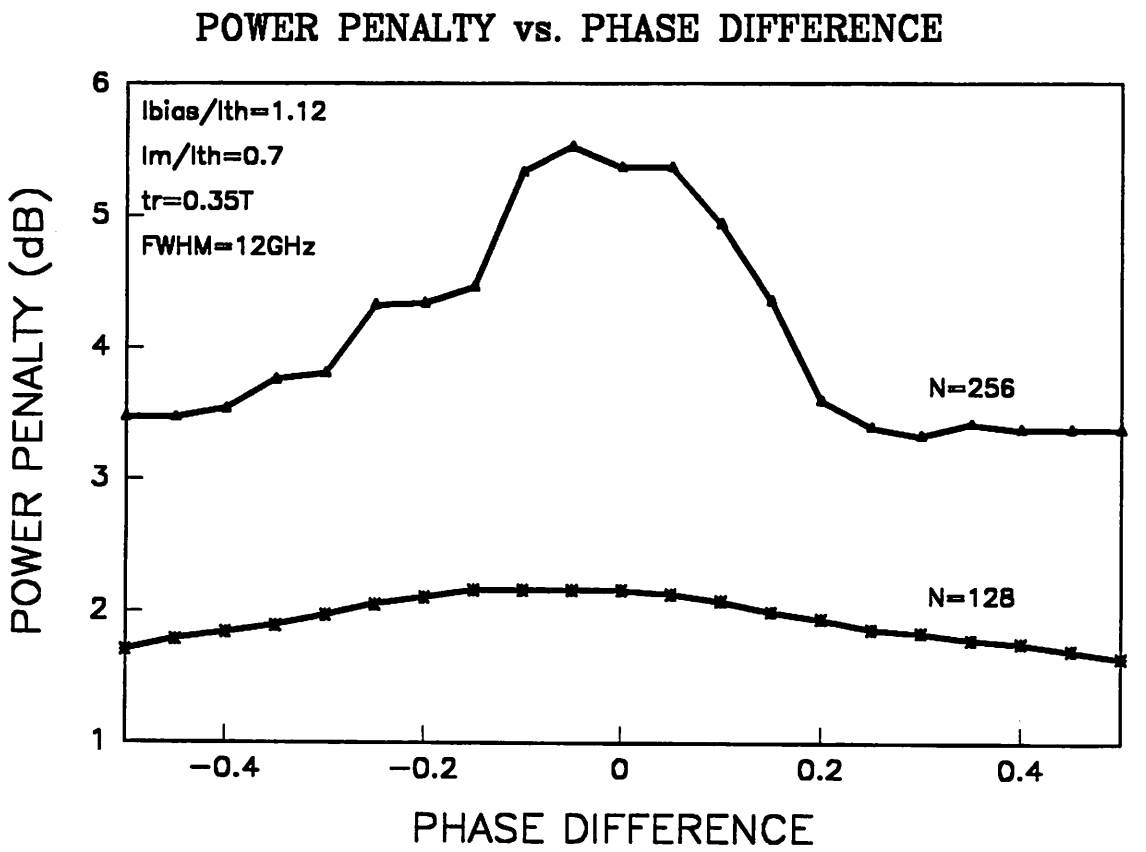

Figure 6-20. Power penalty as a function of the skew between the interfering channels and the signal channel for N = 128 and 256. Skew has been normalized with respect to T, and is periodic outside of (− 0.5,0.5).

As the interfering channels are brought spectrally closer to the signal channel, their finite spectral widths generate larger crosstalk as compared with those obtained from the theory, which assumes zero spectral width for each individual channel.

Because a larger filter bandwidth allows more crosstalk while a narrower bandwidth induces a larger chirp penalty, there exists an optimal filter bandwidth for a given number of stations, at which a minimum system penalty is achieved. Figure 6-24 displays such an optimum for 32, 64, and 128 stations operating at 2 Gbps. As shown in this figure, the optimal filter bandwidth becomes nar-

rower as the number of stations increases. For a system with 128 stations with each station transmitting at 2 Gbps, the optimal bandwidth occurs at 10 GHz.

The horizontal eye closure experienced by the system in the presence of interfering channels is displayed in Figure 6-25. The eye closure increases monotonically as the number of stations in a system increases. The horizontal eye closes completely as the number of stations reaches 256 for a filter bandwidth larger than 20 GHz.

The laser parameters, such as the gain suppression and the linewidth enhancement factor, affect the system performance. The power penalty is shown in Figure 6-26 as a function of the linewidth enhancement factor for various values of gain suppression. As the linewidth enhancement factor increases, a larger power penalty is incurred as a result of larger transient chirp. On the other hand,

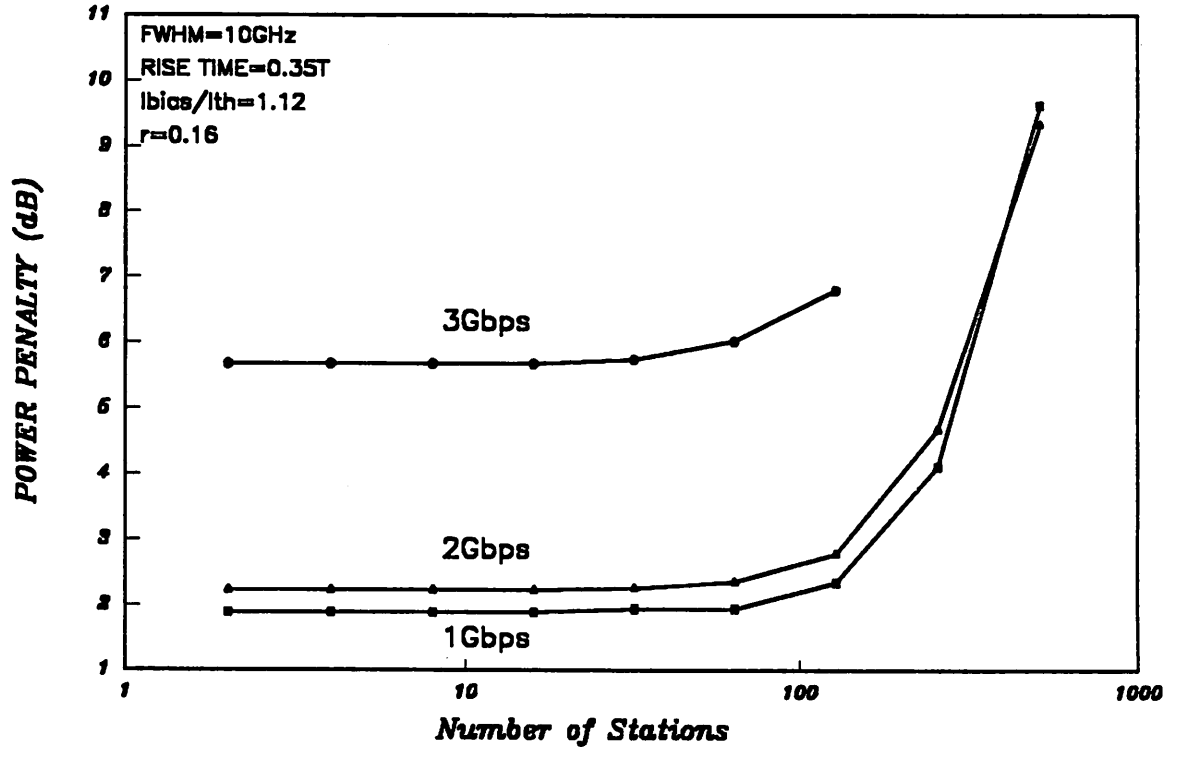

Figure 6-21. Power penalty versus number of stations at 1, 2, and 3 Gbps.

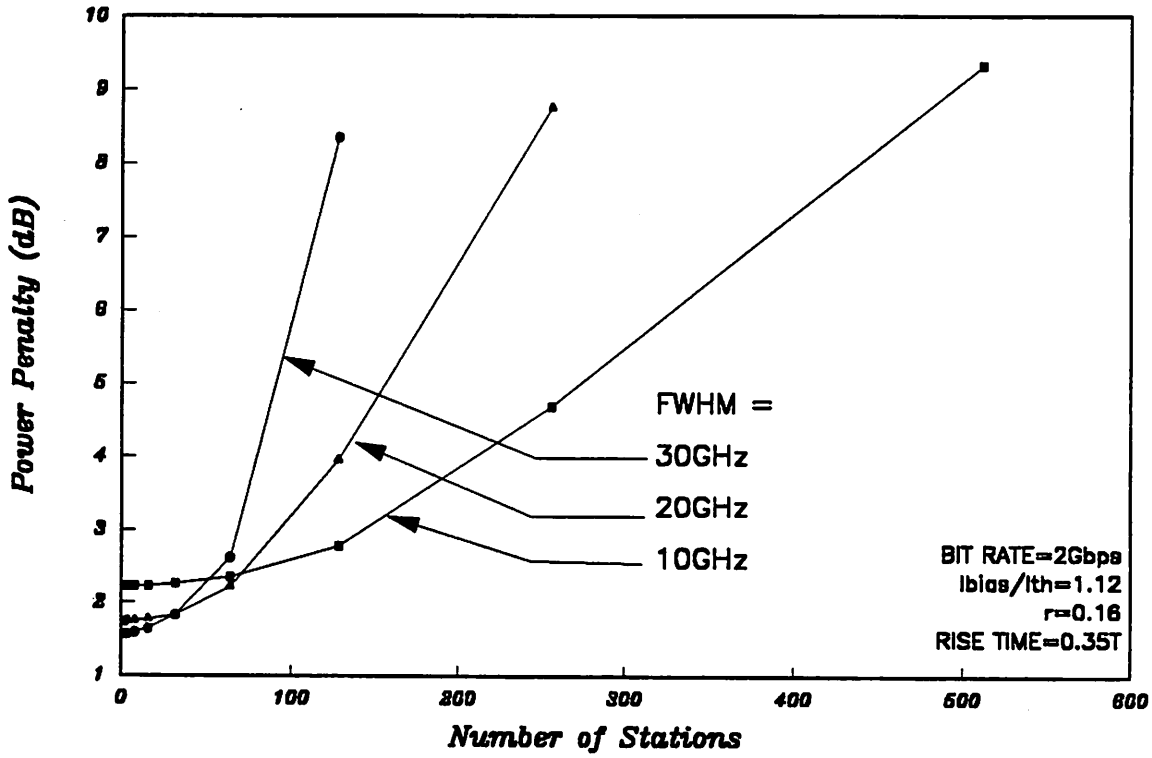

Figure 6-22. Power penalty versus number of stations at filter bandwidth of 10, 20, 30 GHz.

larger gain suppression increases the adiabatic chirp while decreasing the transient chirp, resulting in a decrease of the power penalty.

Frequency chirping and crosstalk, rather than waveform jitter, are the dominant factors in determining the channel capacity. These results, 100-130 channels at 2 Gbps, are the largest channel capacity one could achieve as limited by the frequency chirping and crosstalk. Considerable improvement in the transmission rate will be made in device development such as quantum well lasers with low chirp [96], or waveform shaping on the driving current of the laser diode [97].

6.5 System Optimization

The optimization of each individual channel in a dense WDMA system is essential for achieving maximum system capacity. In this section, we evaluate the various optimal operating conditions of the laser and the FP filter and the sensitivity of the system performance to these conditions for a single channel in a WDMA environment. It is assumed that each channel runs at 2 Gbps and that the finesse of the FP filter is 312. The parameters that are allowed to vary are

- FP filter center frequency, f_c,
- laser bias current, I_{bias},
- laser rise time, t_r.

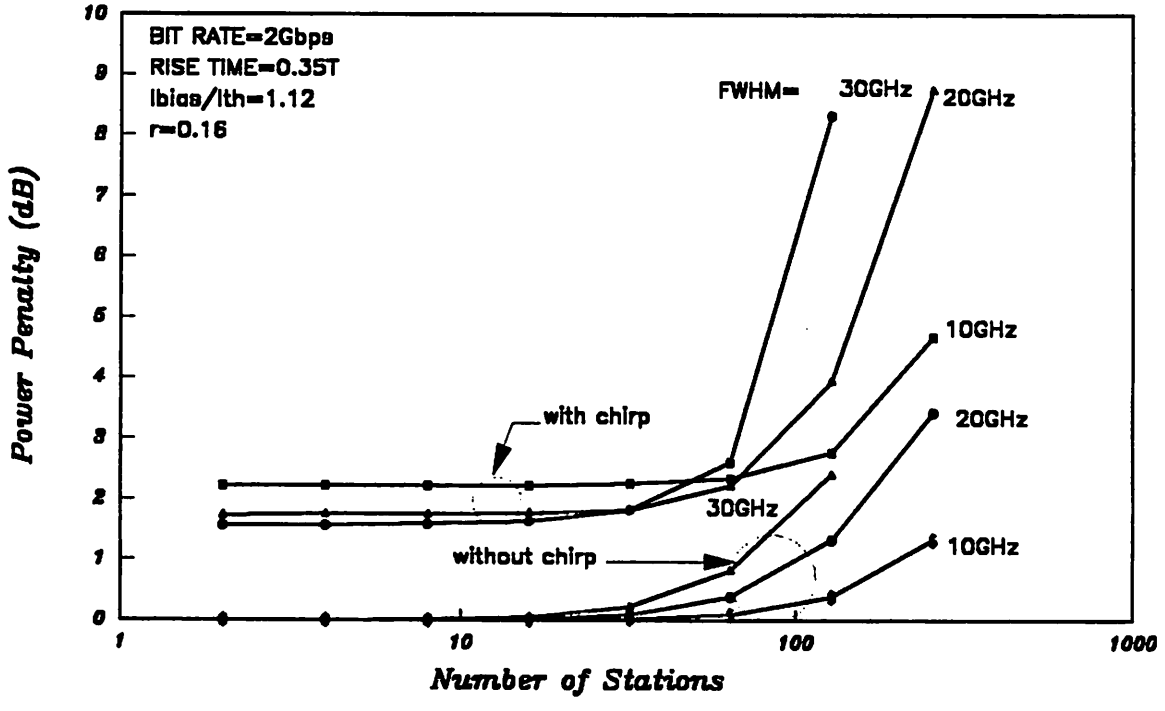

Figure 6-23. Comparison of results between with chirp and without chirp for power penalty versus number of stations. Filter bandwidth is set at 20 and 30 GHz.

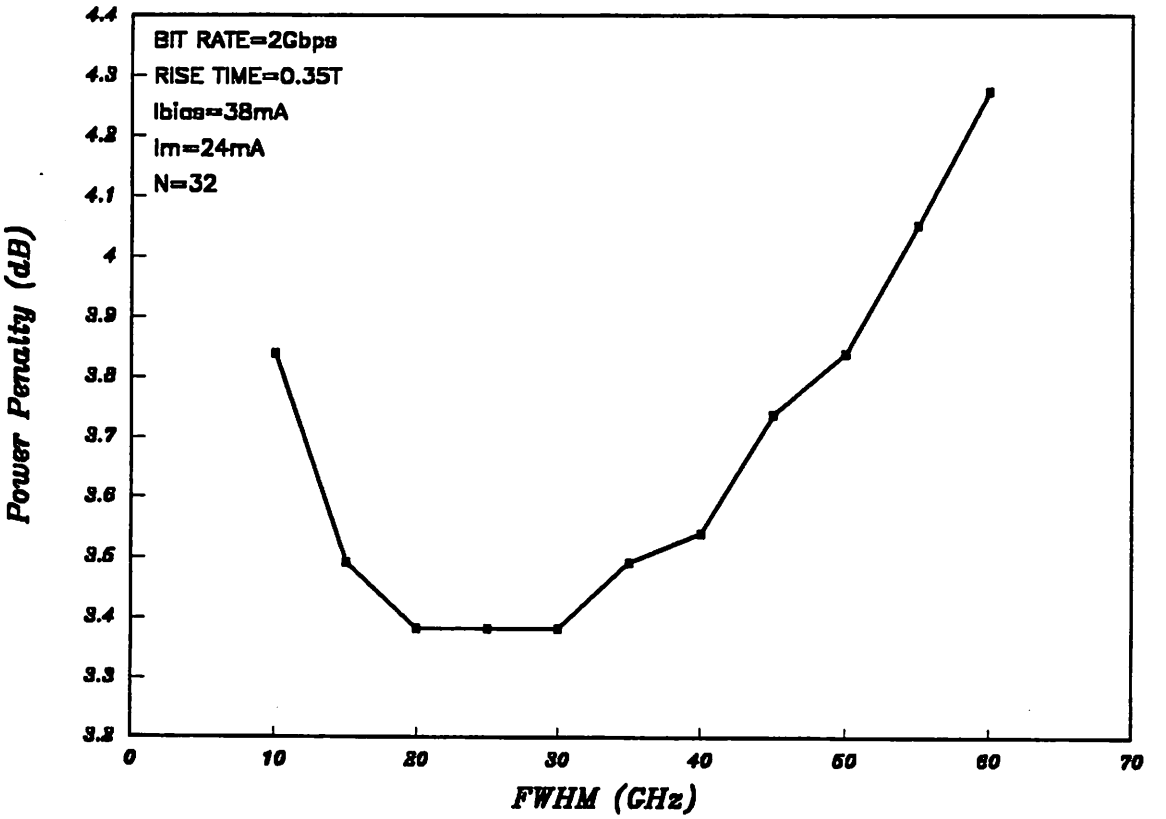

Figure 6-24. Power penalty versus filter bandwidth at various filter bandwidth.

Figures Figure 6-27, Figure 6-28, Figure 6-29 and Figure 6-30 display the sensitivity of the system penalty to the position of the center frequency of the FP filter. The center frequency is of significance since the laser emission frequency of the steady state ONE bit differs from the steady state ZERO bit by 2 GHz due to the adiabatic chirp. Only the optical power of the ONE bit contributes to the signal detection. If transient chirp is neglected, the FP filter should be centered at the steady-state frequency of the ONE bit so that most of the power of a ONE bit can pass un-attenuated while most of the power of a ZERO bit is blocked. Thus, a combination of on-off-keying and frequency-shift-keying demodulated by the FP filter can be achieved. This leads to a net reduction in system penalty when the FP filter is introduced. The results would be similar for conditions where transient chirp is either reduced by the laser bias level, or where the duration of

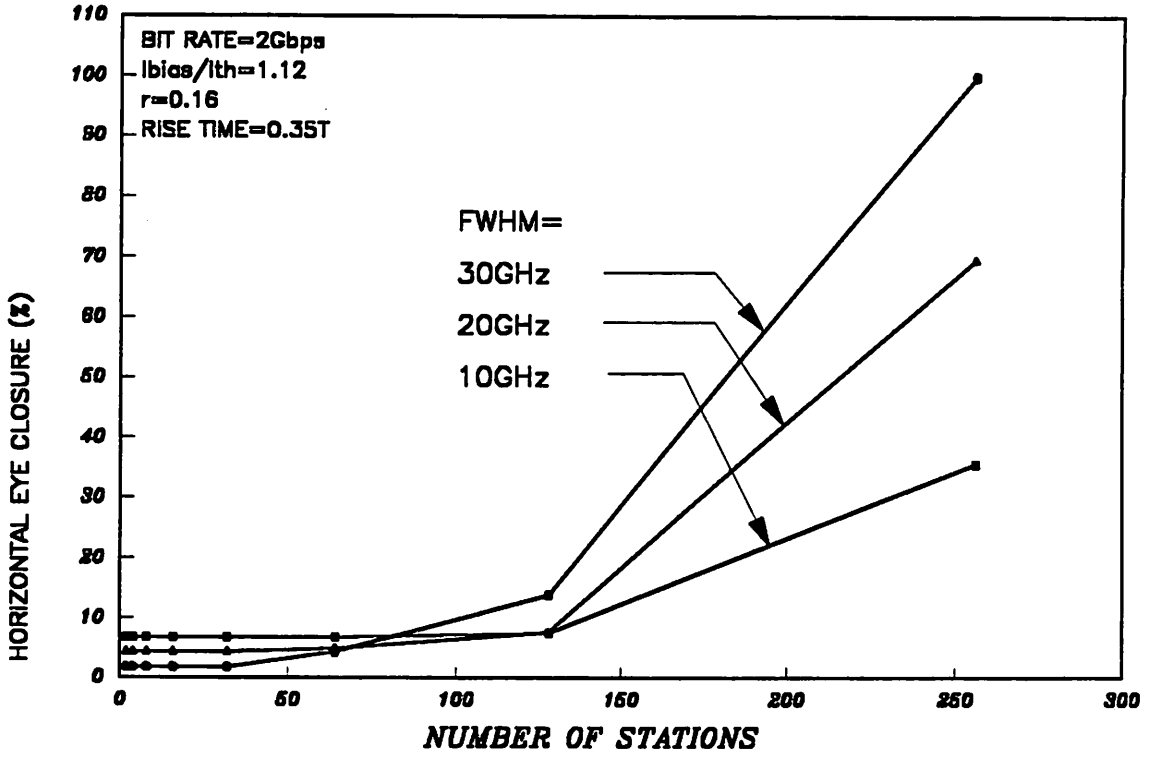

Figure 6-25. Horizontal eye-closure is plotted against the number of stations at filter bandwidth of 10, 20, and 30 GHz.

the chirp is small compared to the bit period. However, under conditions where the transient chirp is large, the optical power of a ONE bit is spread across the entire chirp spectral width while the power of a ZERO bit is still concentrated around the steady state frequency of the ZERO bit. In this case there is little power at the steady state frequency of the ONE bit even during the ONE bit, and the optimal center frequency is shifted toward the steady-state frequency of the ZERO bit.

Figure 6-27 shows the power penalty as a function of the center frequency for FP filter bandwidth equal to 10 GHz, 20 GHz, and 50 GHz. As shown in this figure, the optimal center frequency occurs at the steady-state frequency of the ZERO bit rather than the slightly higher steady state frequency of the ONE bit. Narrower bandwidths suffer larger system penalty. For a

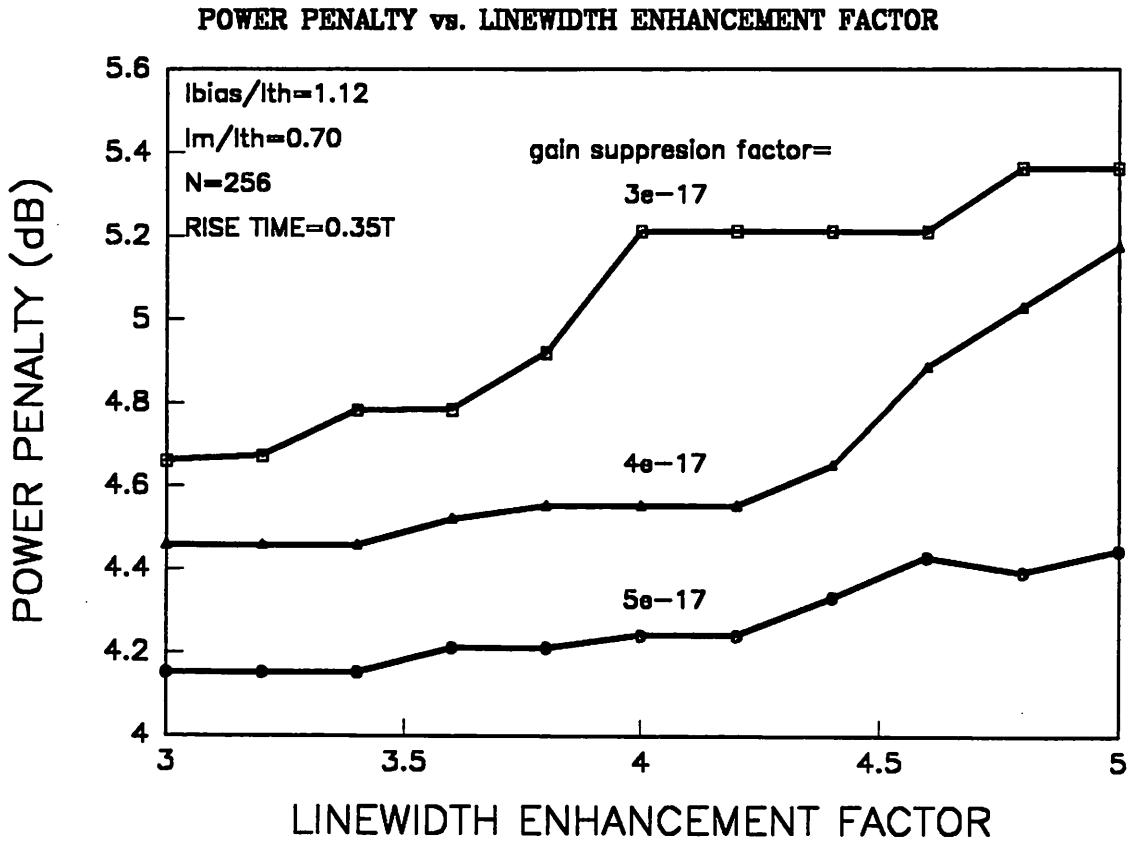

Figure 6-26. Power penalty is plotted against linewidth enhancement factor. Gain suppression = 3×10^{-17}, 4×10^{-17} and 5×10^{-17}.

filter bandwidth equal to 10 GHz, the system quickly degrades as the center frequency shifts towards the negative side. There is a relatively small increment in power penalty on the positive frequency side compared to the negative side, since most of the signal power is distributed over the positive frequency range covered by the chirp. When the filter bandwidth is comparable to or larger than the chirp width, as is the case when FWHM is equal to 20 GHz, the FSK demodulation effect is less significant and the asymmetric power penalty is no longer appreciable. For even larger filter bandwidths, as in the case when FWHM equals 50 GHz, the power penalty is relatively insensitive to the position of the center frequency.

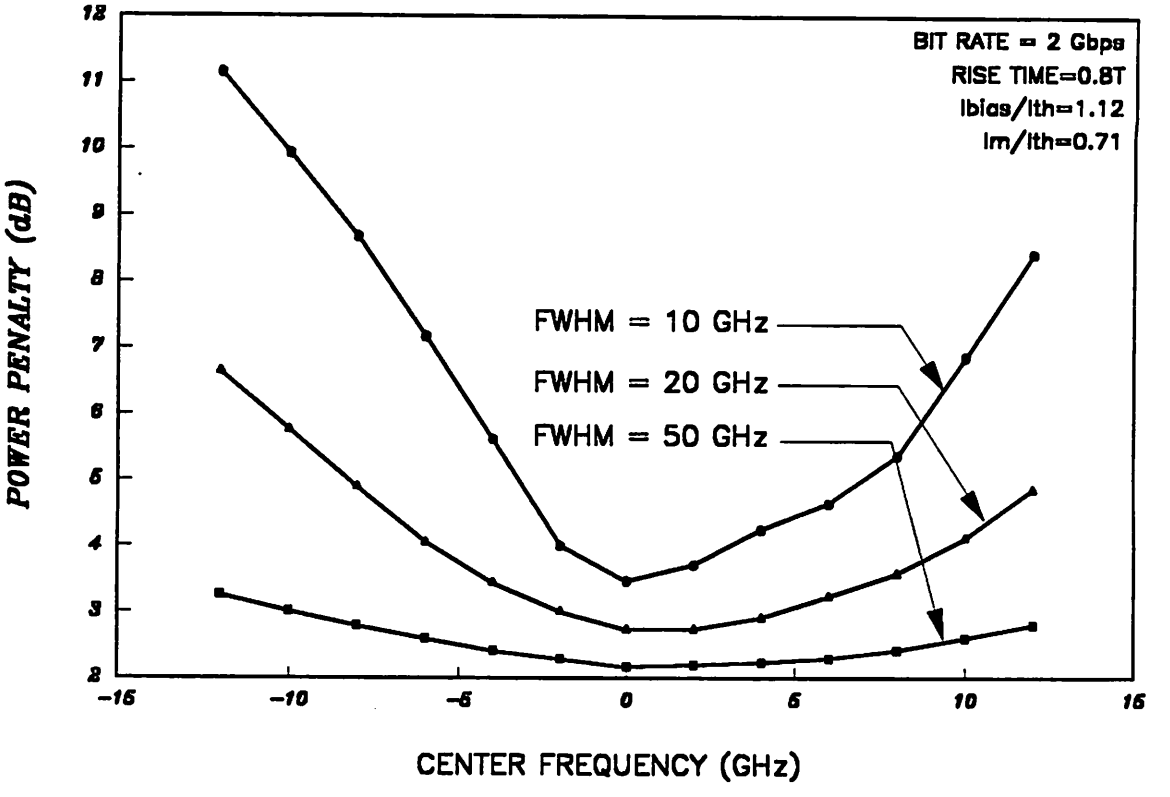

Figure 6-27. Power penalty as a function of the center frequency of the FP filter.

The position of the center frequency of a FP filter is also affected by the laser bias current. An increase in bias current decreases the amount of chirp, and shifts the optimal center frequency of the FP filter towards the steady state frequency of the ONE bit. For a given bit rate and FP filter bandwidth, Figure 6-28 displays the power penalty as a function of filter center frequency for normalized bias currents of 1.0, 1.06, and 1.12. Curves corresponding to normalized current equals 1.06 and 1.12 have their optimal frequencies at around the steady state frequency of the ONE bit. The corresponding power penalty is also reduced by 0.5 dB compared with normalized bias current of 1.0.

Increase of the laser bias current reduces the chirp but also increases the extinction ratio. An optimal condition in power penalty therefore exists. By maintaining the center frequency at 1 GHz

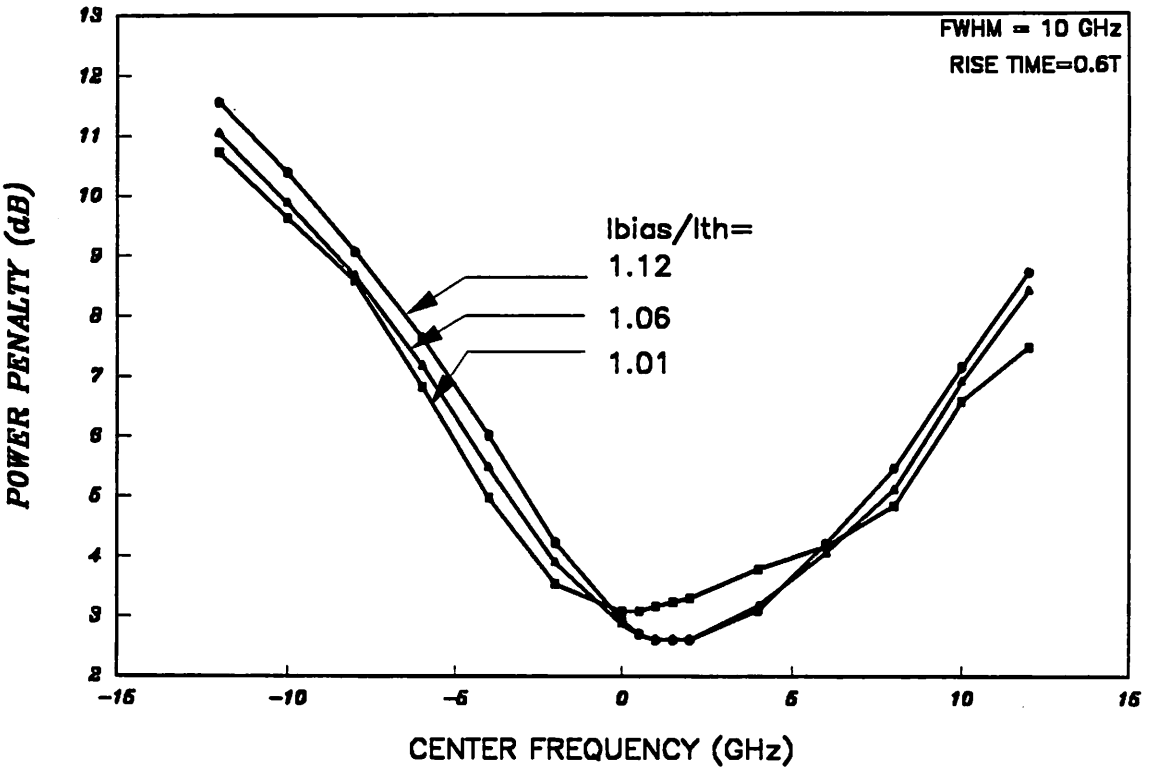

Figure 6-28. Power penalty as a function of filter center frequency. $I_{bias}/I_{th} = 1.00$, 1.06, and 1.12.

and the bandwidth of the FP filter at 10 GHz, we investigate the power penalty as a function of bias current. As shown in Figure 6-29, the system penalty exhibits an optimum at normalized bias current equal 1.05. By removing the FP filter, the eye degrades only due to the increase of extinction ratio, and the system exhibits a monotonic increase in penalty with the increase of bias current. The penalty due to chirp alone can thus be obtained by subtracting the extinction penalty from the total penalty. The monotonic decrease in penalty with the increase of bias current is consistent with the results from previous studies on chirp-induced dispersion penalty [82].

The optimal center frequency of the FP filter is also sensitive to the rise time and the fall time of the laser driving current. Figure 6-30 show the power penalty as a function of center frequency for rise time equal to 1/5, 2/5, 3/5 and 4/5 of the bit period. The laser is biased at threshold in order

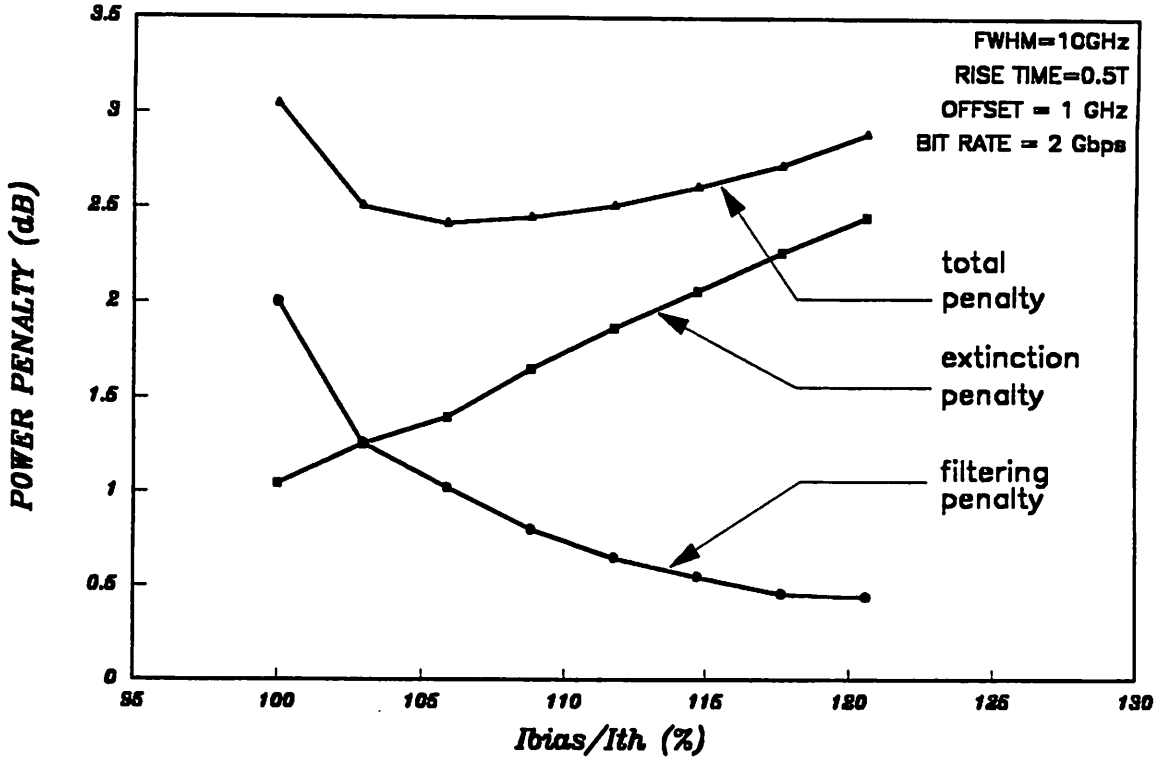

Figure 6-29. Power penalty as a function of laser bias current. The laser threshold current has been normalized with respect to its threshold current, i.e., I_{bias}/I_{th}.

to generate the largest chirp width. The general behavior of the power penalty is similar to that obtained in Figure 6-27 and Figure 6-28, displaying an asymmetric behavior. A shorter rise time causes larger chirp and the system suffers a larger penalty. The optimal center frequency shifts towards the negative side for a sharper rise time, and the power penalty is also less sensitive to the position of the center frequency. This is because a sharper rise time results in an increase of chirp width, especially as the power of the ONE bit spreads across the entire chirp width.

It has been shown in [99] and Eq.(6.26) that the amount of laser chirp can be reduced by increasing the rise time. However, increasing the rise time also reduces the vertical eye opening, since the signal level for a ONE bit requires longer time to reach its maximum value. The combination

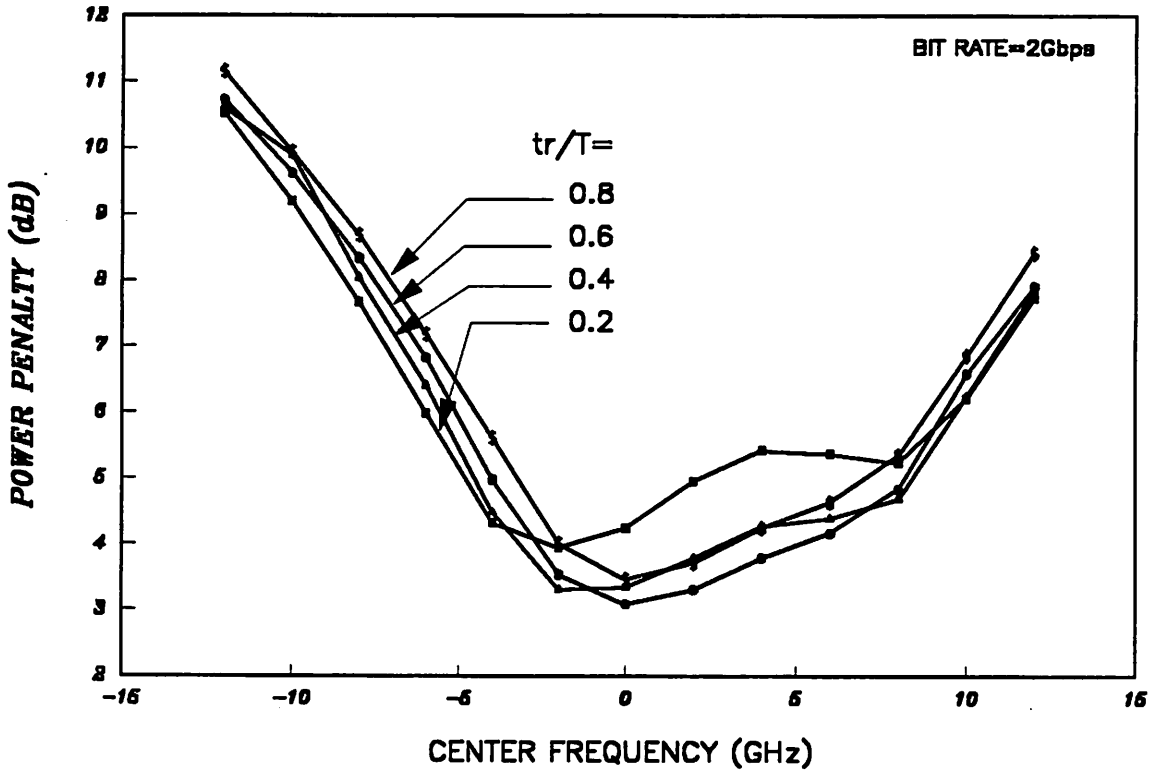

Figure 6-30. Power penalty as a function of filter center frequency.

of these effects produces an optimal rise-time for the power penalty. Figure 6-31 shows the power penalty as a function of rise time. The optimal rise time for the conditions chosen is found to be 150 ps, which spans one third of a bit period. Less than 0.5 dB change in power penalty is observed over the rise time range from 0 to 300 ps. When the FP filter is removed, system degradation is entirely due to slower rise time, and thus exhibits a monotonic increase in power penalty. The penalty due to the chirp effect alone can thus be extracted by subtracting the rise time penalty from the total penalty.

6.6 Dense WDM/WDMA-FSK Systems

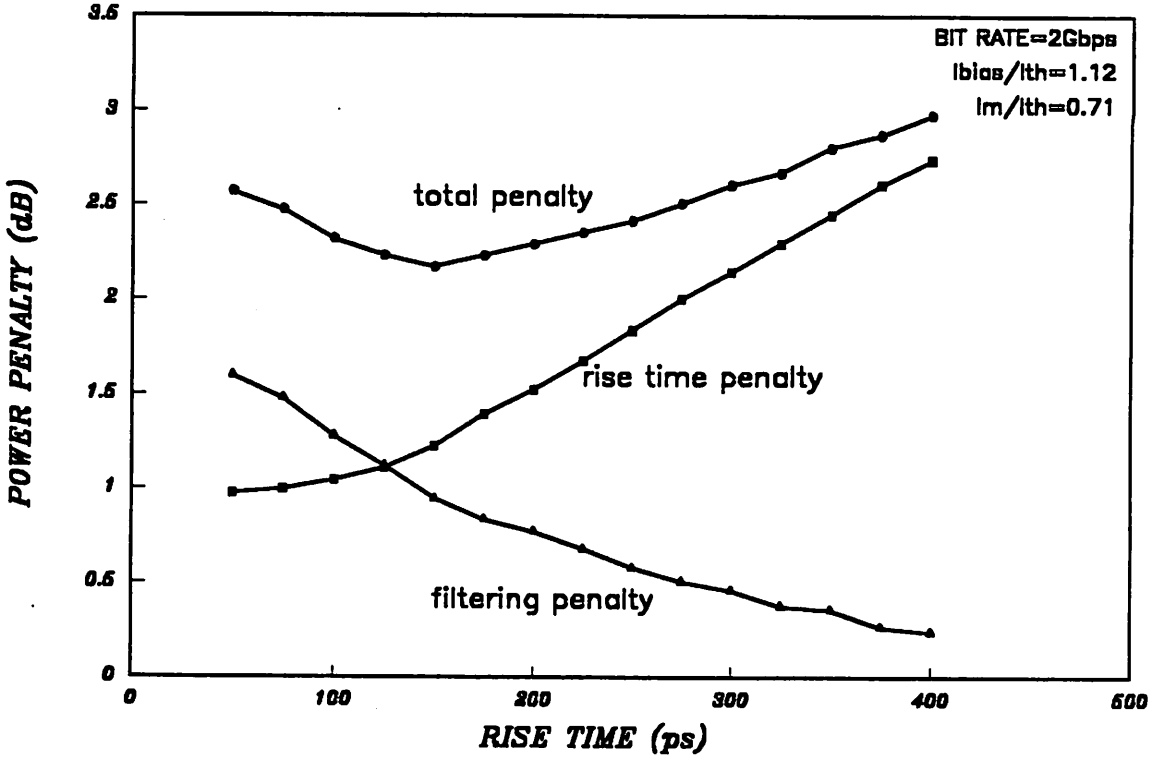

Figure 6-31. Power penalty as a function of rise time.

In addition to be modulated by OOK, lasers in a WDM/WDMA system can also be modulated by frequency-shift-keying (FSK). FSK usually induces significantly less chirp and thus introduces less performance degradation. However, the filter FWHM requirement of using FSK is more stringent than that of using OOK, because of the need to select one tone out of the two tones transmitted for each channel. A convenient way to select one out of N FSK channels and demodulate it simultaneously is to pass the received optical signal through a fixed-tuned or tunable Fabry-Perot optical filter, selecting one out of $2N$ tones while rejecting all the others [100-103]. For a given channel spacing, the selected signal in this scheme may suffer degradation when the optical filter bandwidth is close to or smaller than the modulation width of an FSK channel. On the other hand, larger filter bandwidth allows more leakage from the adjacent tone of the same

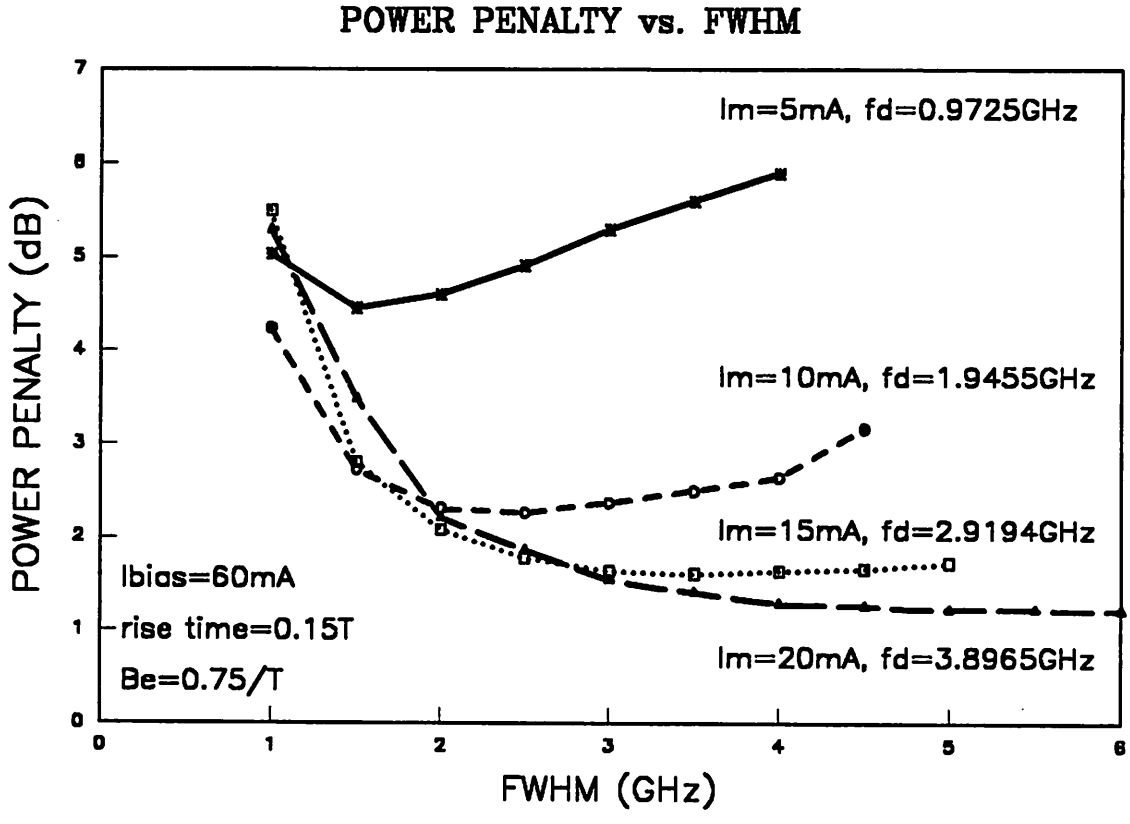

Figure 6-32. Single-channel power penalty as a function of filter bandwidth. Tone spacing f_d of 0.9, 1.9, 2.9, and 3.9 GHz. The laser is biased with I_{bias} at 60 mA (current level for the ONE bit) with lasing threshold at 34 mA, while $I_{bias} - I_m$ is the current for the ZERO bit. The parameters T is the bit interval and B_e is the receiver bandwidth.

channel as well as from neighboring channels. The combined effects thus yield an optimal filter bandwidth. Furthermore, reducing the tone spacing within the same channel or channel spacing between neighboring channels increases crosstalk. To achieve a certain system performance, there thus exists a minimum channel spacing and tone spacing.

Computer simulations for a FSK system using a two-section DFB laser at low data rates [102] and a single-section single-mode laser at high data rates [104] have been reported, but only a single channel is considered. In this section, we report simulated system performance of an N –channel dense WDM/WDMA-FSK system using single-section single-mode lasers with each

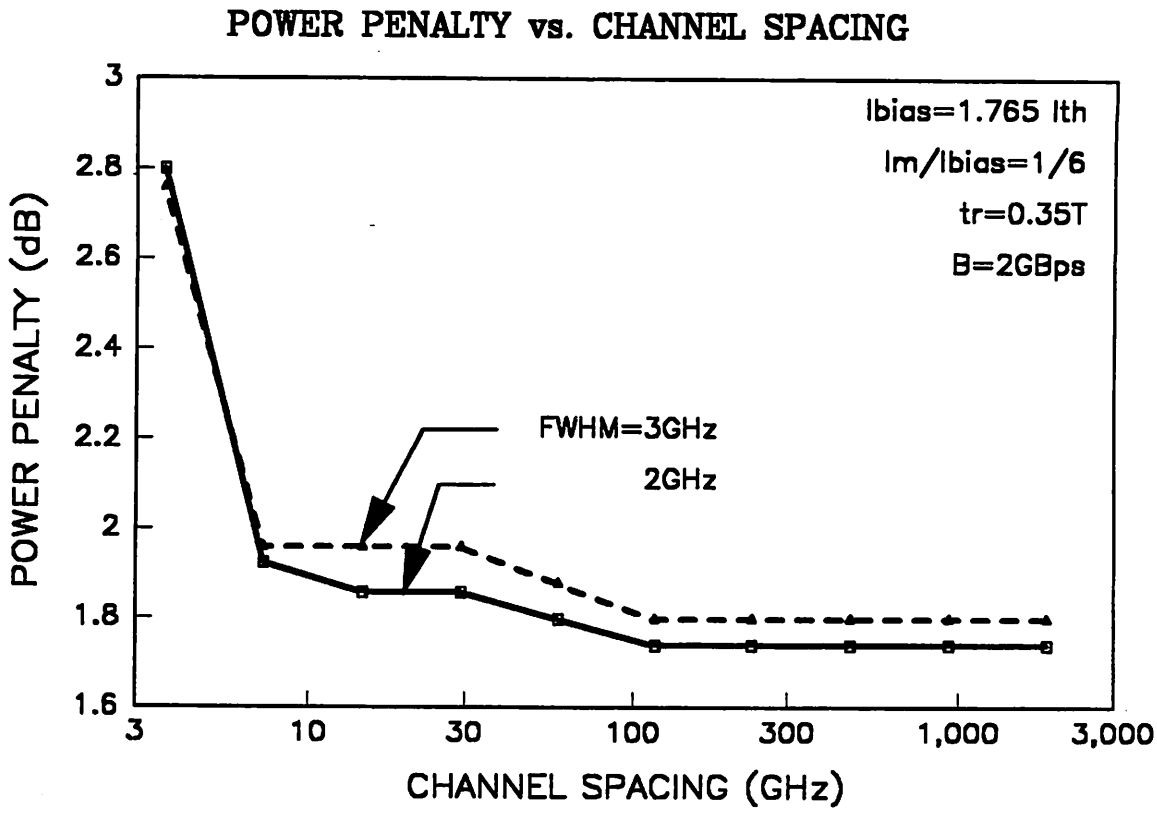

Figure 6-33. Multi-channel power penalty vs. channel spacing for filter bandwidth of 2 and 3 GHz.

channel transmitting at 2 Gbps. A single-section single-mode laser model, rather than multi-section laser model, is used because of its superior FM response in the gigabit regime [103, 104]. The simulation models for the single-mode laser, the optical fiber, the Fabry-Perot filter, and the receiver as well as their parameters are similar to those used in the previous sections. For an N –channel system with the optical filter centered at the center frequency of the ONE-tone of the signal channel, simulated power spectra reveal that the worst-case crosstalk occurs when all channels, including the signal channel, are transmitting ZEROs. A superposition of all possible variations of an 8-bit sequence is used to generate the eye pattern. The system penalty and waveform jitter can then be calculated from the corresponding vertical and horizontal eye opening.

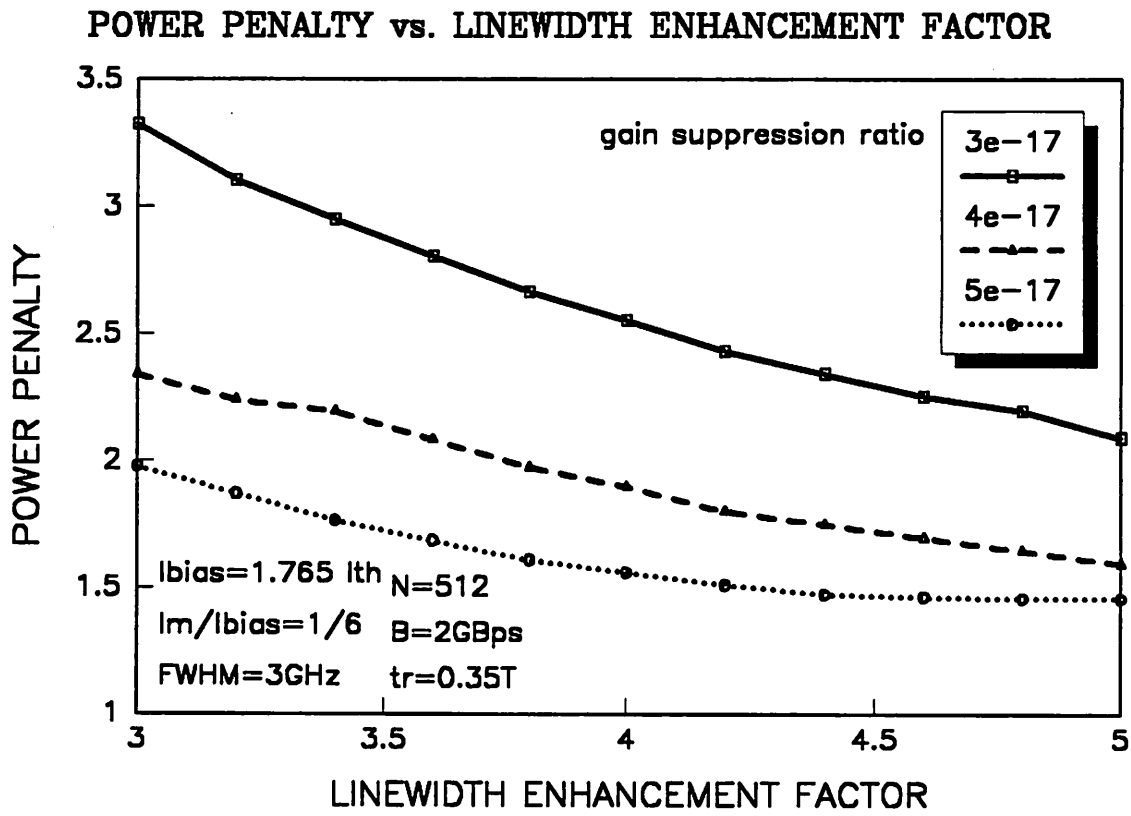

Figure 6-34. Power penalty vs. linewidth enhancement factor for various nonlinear-gain-suppresion ratio. The number of channels is fixed at 512.

For a single-channel FSK system operating at 2Gbps, Figure 6-32 shows the calculated power penalty as a function of filter bandwidth for various tone spacings. The power penalty is found to be insensitive to the laser bias current from 1.5 to 3 times its threshold current. An optimal filter bandwidth exists as a result of compromising between the penalty caused by the leakage from the adjacent tones at large filter bandwidth and the penalty induced by signal distortion at narrow filter bandwidth, which is consistent with the results from a theoretical model reported in [101]. For an N−channel FSK system, the calculated power penalty is plotted against the channel spacing in Figure 6-33 for filter bandwidth of 2 and 3 GHz. Both cases exhibit strong increases in power penalty as the channel spacing decreases below 7 GHz. This result is further verified by the simu-

lated power spectra, in which there is an increase in the spectral density level between adjacent channels when the channel spacing is reduced below 7 GHz. Assuming an available optical bandwidth of 30 nm, as enforced by the available fiber amplifier bandwidth at 1.55 μm, the maximum number of FSK channels could then reach $\simeq$500. The laser parameters that influence laser FM response, such as the linewidth enhancement factor and the nonlinear gain suppression ratio, also affects system performance, as shown in Figure 6-34. As shown in this figure, either an increase in the linewidth enhancement factor or gain suppression ratio reduces power penalty due to the large laser FM response.

6.7 Conclusions

A simulation model has been developed to assess the overall performance of a WDM/WDMA system for dense optical interconnect applications. For the laser assumed, several results have been concluded from this work: (1) In the absence of crosstalk from adjacent channels, the chirp penalty is important for bit rates larger than 1 Gbps. The waveform jitter introduced by the FP filter does not affect the system for bit rates lower than 3Gbps. Narrower FP filter bandwidth improves the system performance for lower bit rates. (2) If crosstalk from adjacent channels is considered, over 100 stations with each station operating at 2 Gbps can be accommodated by a system with total optical bandwidth 3.7 THz (30nm). (3) There exists an optimal FP filter bandwidth of 10 GHz, at which the combined chirp and crosstalk effects are minimized for a system with 128 stations. (4) The system penalty can be minimized by selecting an optimal combination of the bias current and the rise time of the laser and the center frequency of the FP filter. (5) In the FSK case, the minimum channel spacing is found to be $\simeq$7GHz for 1 dB additional system penalty. Optimal tone spacing and optical filter bandwidth can also been determined from simulations.

CHAPTER 7 DENSE TRANSMITTER ARRAYS

7.1 Introduction

In a dense optical interconnect, electrical interactions among elements in a transmitter or receiver array due to high density requirement might limit the system performance, and will be the subject of this and the next chapter.

A transmitter array usually consists of a driver array and a laser diode array (or LED array). These two components might be monolithically or hybrid integrated on the same substrate. Among possible interactions in a dense transmitter array are

- Electrical crosstalk between laser diodes due to the sharing of a common substrate,
- Electrical crosstalk due to parasitic capacitance and mutual inductance between adjacent channels,
- Switching noise due the sharing of a common power supply and ground.

These interactions increase with the increase of channel density, modulation speed, and modulation current of the transmitter.

Crosstalk among laser array elements has been a subject of continuous interest. Fabrication and characterization of one dimensional individually addressable laser or LED array has been reported in [105-108]. Recently, two-dimensional vertical cavity surface emitting laser (VCSEL) diode arrays or surface emitting LED arrays have received a lot of attention and have emerged as a very promising light source for two-dimensional optical interconnects. The performance of these LED's and laser diodes is reported in [109-113] but the crosstalk data has yet to be established. Most of the laser or LED driver circuits were published in the late 70's and early 80's [114-120]. Recent laser driver circuit designs usually include monitoring circuits which calculate the peak and average of the laser output power in order to maintain a constant extinction ratio. Based on these designs, a driver array can be built by replicating the same design N times. Both monolithic integration [121] and hybrid integration [122, 123] of the driver array with the laser array have been exploited. Crosstalk in these works is usually determined through experiments or simulations, but

a systematic study of the crosstalk due to switching noise is yet to be addressed. However, this issue is important for choosing a suitable driver architecture to minimize overall interference.

In this chapter, both analysis and simulation are used to determine the system penalty due to switching noise. Important results reported in this chapter are:

- A circuit model is developed for the transmitter array,
- A simulation methodology that determines the worst case interference is developed,
- Switching noise is the dominant source for crosstalk. A differentially configured driver array has large switching noise ($\geq$50% for a size of 16) due to the unbalanced load presented to the driver.
- A large power supply decoupling capacitor ($\gg$100nF) is necessary to suppress the switching noise.

The organization of this chapter is as follows: Section 2 derives the equivalent circuit of a single-ended and differential driver array hybrid integrated with a laser array. The analytical results on the single-ended driver array are presented in Section 3 while Section 4 presents simulation results of a differential driver array hybrid integrated with a laser diode array. This chapter is summarized in Section 5.

7.2 Transmitter Array Modeling

A transmitter array is shown in Figure 7-1. It consists of a driver array and a laser diode array hybrid integrated on the same substrate. The equivalent circuit of this transmitter array also include parasitic coupling between bonding wires as well as power supply and ground inductance. The substrate of the laser array is die bonded to the package, which usually includes a thermoelectric cooler to stabilize the temperature of the laser diodes.

7.2.1 Laser Modeling

The laser diodes are assumed to have channeled substrate buried heterostructure (CSBH) [108]. The active areas are grown by liquid phase epitaxy (LPE), metal-organic chemical vapor deposition (MOCVD), or metal beam epitaxy (MBE) on the etched channels. Each laser is modeled by its series resistance R_s, an ideal diode, and a capacitor C_d which is in parallel with the resistor

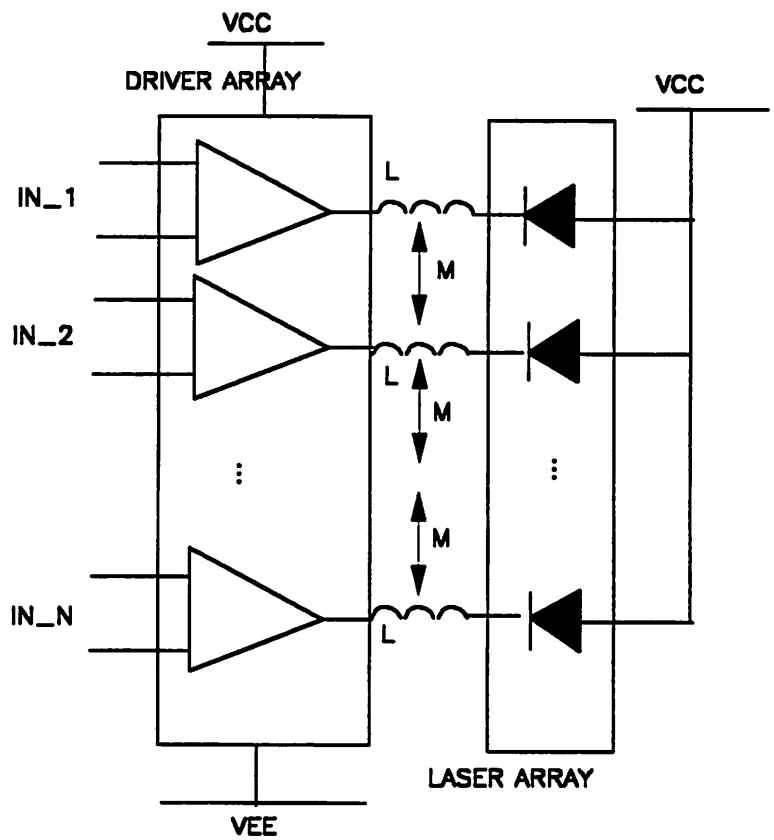

Figure 7-1. Block diagram of a transmitter array.

and the diode, as shown in Figure 7-2 [124]. Good electrical isolation between laser elements can be obtained by using a deep trench from the surface to the semi-insulating layer [108]. The laser diode array is assumed to share a common resistive substrate. We neglect the substrate coupling between adjacent laser diodes by assuming the substrate resistance between adjacent laser diodes is much larger than the resistance between active layers.

7.2.2 Single-Ended Driver

The single-ended transmitter consisting of a single-ended driver and a laser diode is shown in Figure 7-3. The driver circuit includes a bias control transistor Q1 and a modulation transistor Q2.

7.2.3 Differential Driver

The equivalent circuit of a differential differential driver is shown in Figure 7-4. In the driver circuit shown in this figure, transistors Q1 and Q2 provide the input buffering, Q3 and Q4 are emitter coupled and provide the current drive to the laser through the collector of Q4. Transistors Q5 and Q6 compose a current mirror which provide the modulation current control, while Q8 and Q9 compose another current mirror which provide the bias current control.

The bipolar transistors used in the simulations in this chapter have been assumed to have an f_T larger than 20 GHz, which is quite typical for an advanced self-aligned silicon bipolar process.

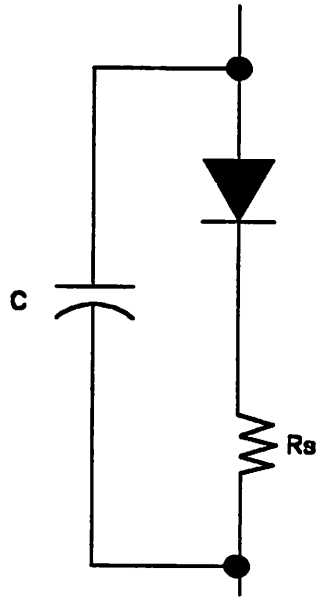

Figure 7-2. Circuit Model of a laser diode.

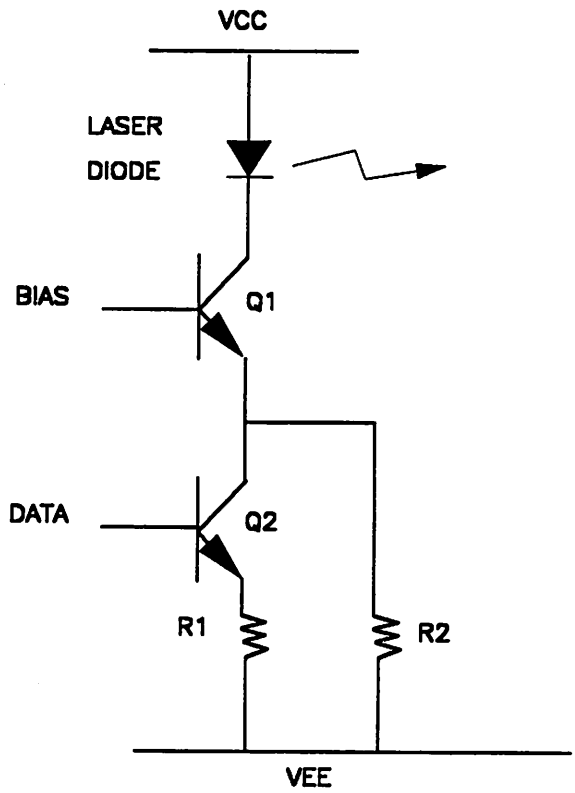

Figure 7-3. Circuit diagram of a single-ended laser driver.

7.3 Switching Noise Analysis of Single-Ended Driver

The driver circuit shown in Figure 7-3 is very vulnerable to power supply and ground disturbances as demonstrated from the following analysis.

The current demand from the power supply V_{CC} and the current injection into the power supply V_{EE} changes from I_{bias} to $I_{bias} + I_{mod}$ over a period of time t_r when the data input switches from logical ZERO to logical ONE. For a current transient of di/dt, V_{CC} decreases by Ldi/dt while V_{EE} increases by Ldi/dt where L is the inductance of the bonding wire of the power supply. Assuming the voltage reference to the bias control V_{bias} remains constant, the total bias current is reduced since

$$I_{bias} = \frac{V_{bias} - V_{BE} - V_{EE}}{R_{bias}} \tag{7.1}$$

and the modulation current is also reduced since

$$I_{\text{mod}} = \frac{V_{data} - V_{BE} - V_{EE}}{R_{\text{mod}}} \tag{7.2}$$

Assuming channel 1 in the array has a constant input of logical ONE while all the other channels switch from logical ZERO to logical ONE, the total current flowing through the laser diode of

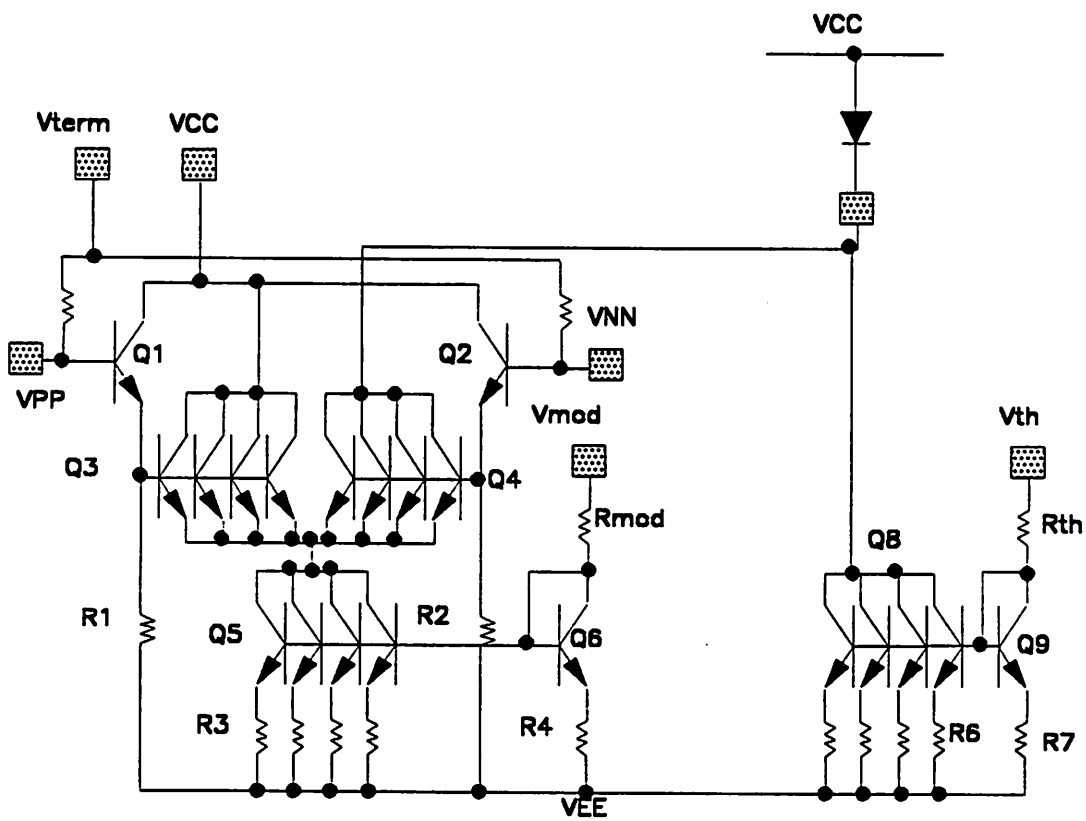

Figure 7-4. Circuit diagram of a differential laser driver.

channel 1 is reduced due to the decrease of both modulation and bias current. The fractional reduction of the current flowing through the laser diode equals

$$\frac{\Delta I}{I_{\text{mod}}} = NL\frac{1}{t_r}\left(\frac{1}{R_{bias}} + \frac{1}{R_{\text{mod}}}\right) \tag{7.3}$$

if there are a total of $N + 1$ drivers. In this expression, t_r is the rise time of the signal and L is the inductance of the bonding wire. Assuming N is 16, L is 0.5nH, t_r is 200ps, R_{bias} and R_{mod} are both equal to 100Ω, the fractional switching noise is 80%!

In this expression, the switching noise is linearly proportional to the number of channels as well as the bonding wire inductance, and inversely proportional to the rise time of the signal. There is no power supply noise cancellation mechanism, so all the disturbances on the power supply will be reflected on the output laser driver current.

7.4 Simulation of Differential Driver

7.4.1 Simulation Methodology

A worst-case simulation methodology has been used to obtain the maximum switching noise under various packaging conditions. In this model, the worst-case scenario is obtained by transmitting a pseudo-random sequence synchronously into receivers 1,2,...,N,$N + 2$,...,$2N + 1$, so that a total of $2N$ out of $2N + 1$ drivers switch simultaneously in the same direction while the input to driver N remains silent. This scenario incurs the maximum current excursion from the power supply as well as introduces a maximum adjacent channel coupling. The output optical power of channel N is then observed and the maximum power spike is compared with the full output swing of an active channel.

Sending identical data patterns to all channels as well as switching synchronously are both essential in obtaining the worst case scenario since

- The switching noise is generated from Ldi/dt where L is the bonding wire inductance of the power supply,

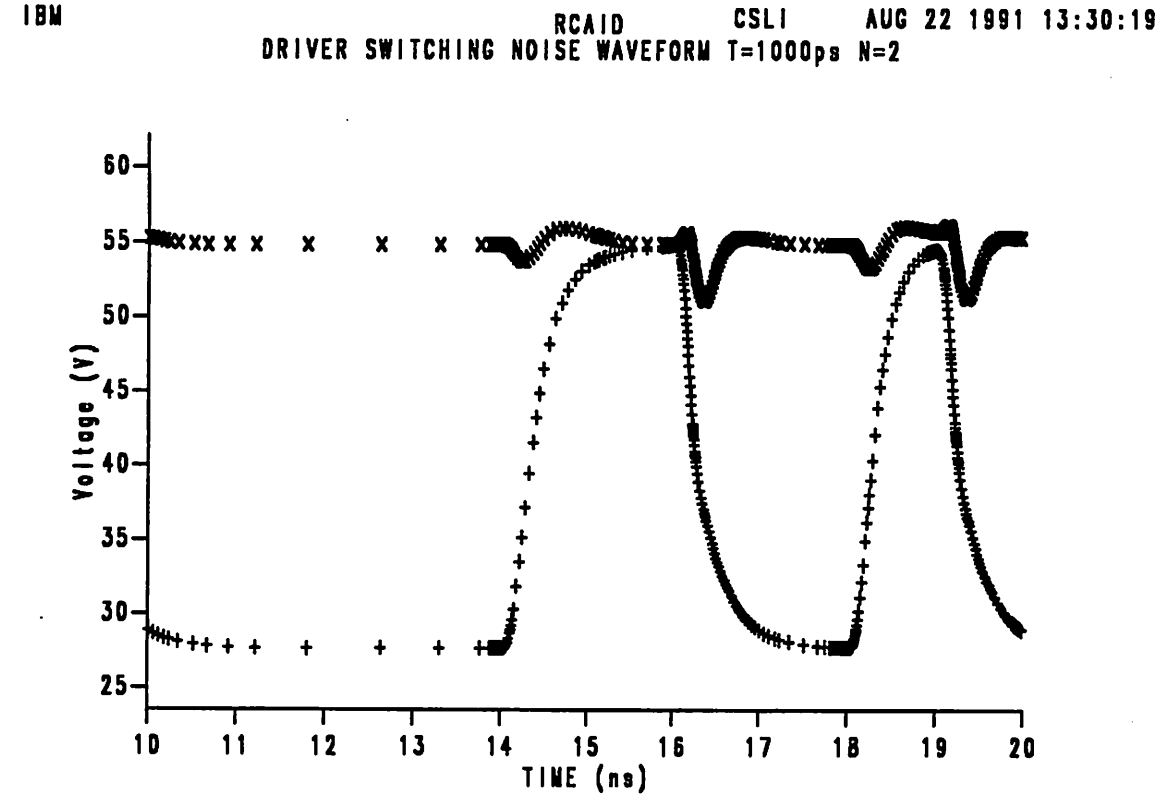

Figure 7-5. Switching noise waveform of the laser driver. N = 2, T = 1000 ps, and t_r = 200 ps.

- Adjacent channel crosstalk is generated from Cdv/dt and Mdi/dt where C and M are the coupling capacitance and mutual inductance between adjacent bonding wires.

and an exact temporal alignment of the transition period of all the active channels yields the maximum interference (with all of the transitions going in the same direction).

7.4.2 Simulation Results

The simulated waveform shown in Figure 7-5 assumes a driver array in which each driver has the same circuit as shown in Figure 7-4 with $N = 2$ and $L_{VCC} = L_{VEE} = 1.5$ nH. The switching noise increases with size of the array, as clearly indicated in Figure 7-6 for $N = 8$ and Figure 7-7 for $N = 16$.

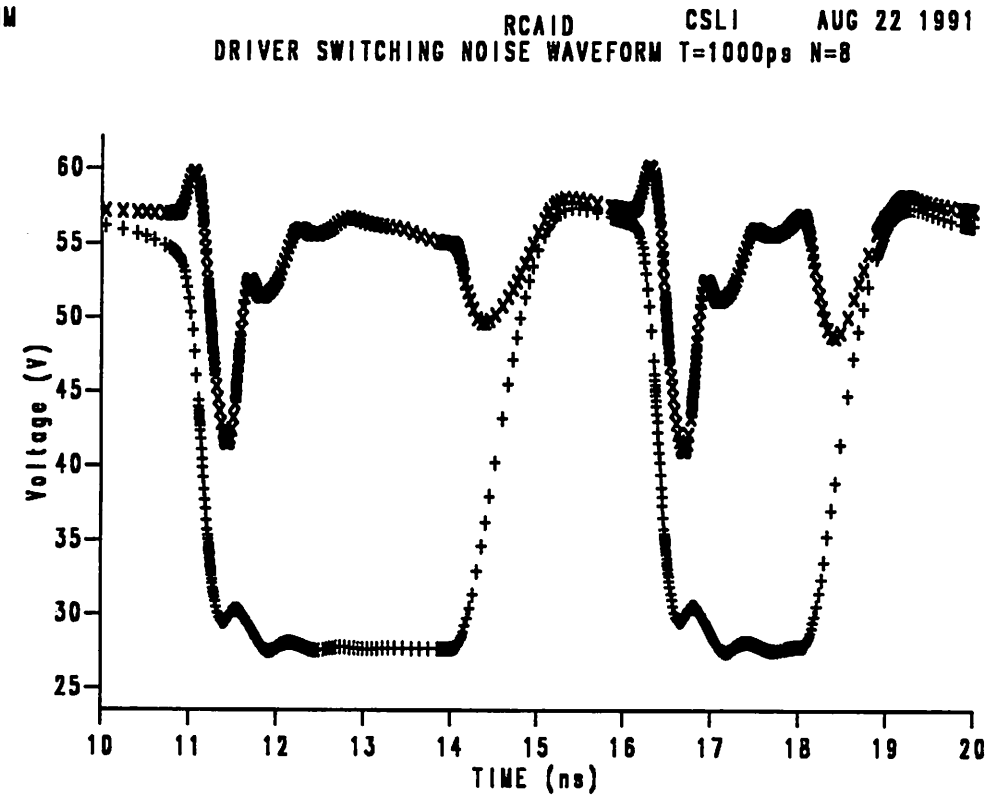

Figure 7-6. Switching noise waveform of the laser driver. N = 8, T = 1000 ps, and t_r = 200 ps.

Figure 7-8 shows the switching noise as a function of the number of channels for various values of bonding wire inductance. As indicated in this figure, the switching noise increases linearly with the number of channels. Figure 7-9 shows that the switching noise is also linearly proportional to the bonding wire inductance. Figure 7-10 shows that power decoupling cannot suppress the switching noise for $C_{decouple} \leq 100nF$. It has also been determined that balancing the driver load with a resistor that matches the resistance of the laser diode does not help too much.

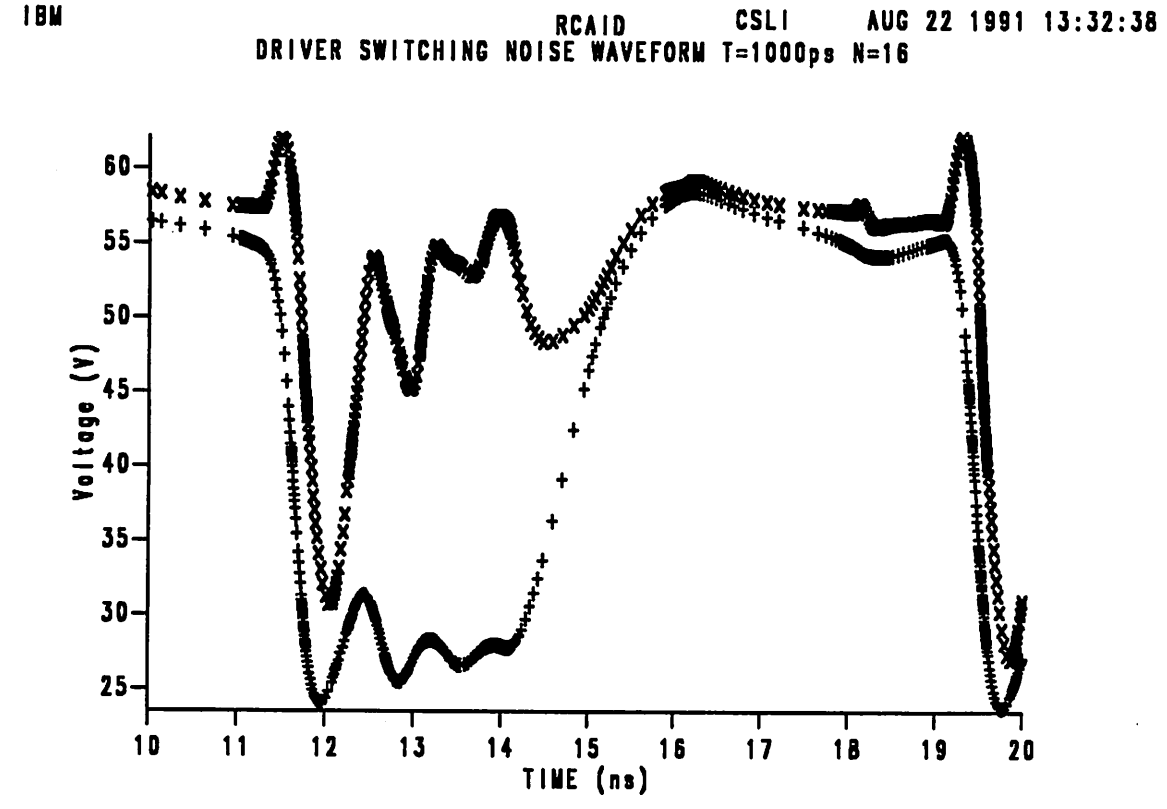

Figure 7-7. Switching noise waveform of the laser driver. N = 16, T = 1000 ps, and t_r = 200ps.

7.5 Summary

In summary, we found that the switching noise is a significant interference source in a transmitter array. A differential driver array can provide less waveform distortion and smaller switching noise compared to those that can be achieved by the single-ended configuration. Furthermore, we show that the switching noise in both single-ended and differential driver array is linearly proportional to the size of the array and the lead inductance of the power supply. The switching noise of a large driver array ($N \geq 8$) is very significant ($\geq 25\%$), indicating that a very large power decoupling capacitor ($\gg 100$nF) is necessary.

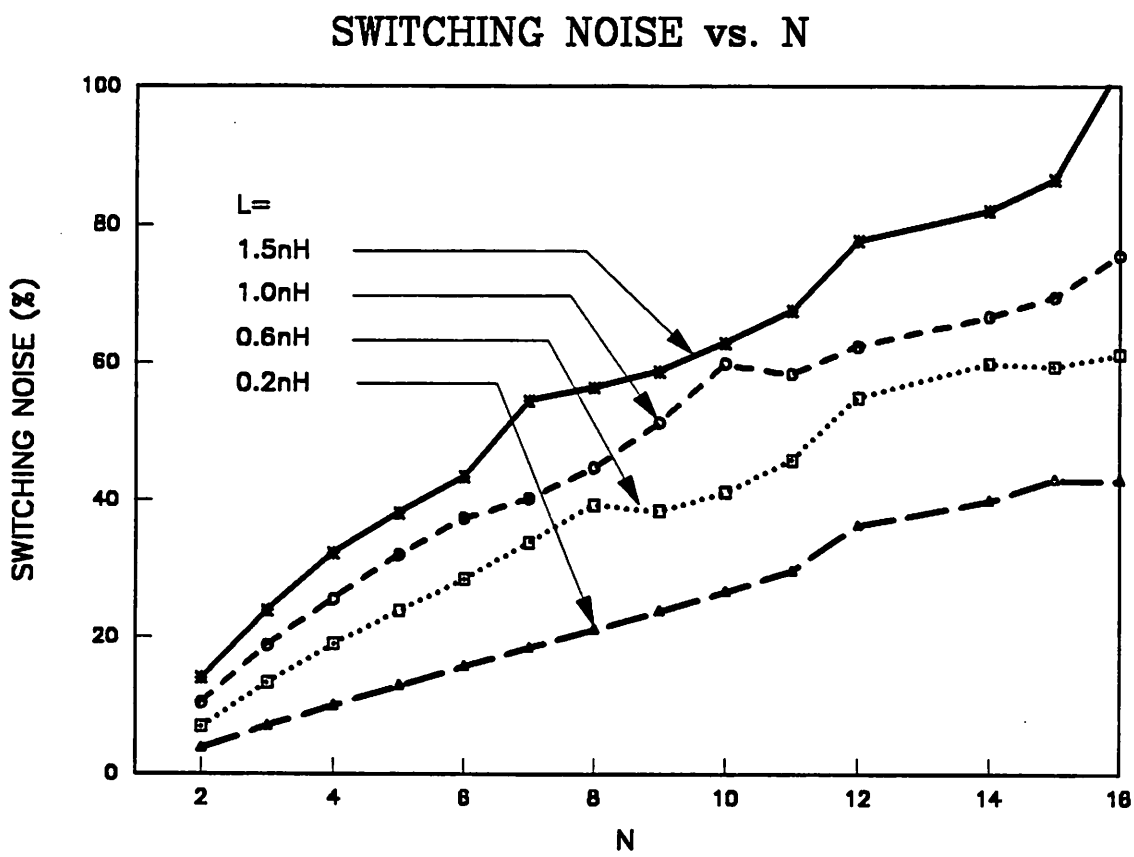

Figure 7-8. Switching noise as a function of the array size. Bit rate = 1 Gbps.

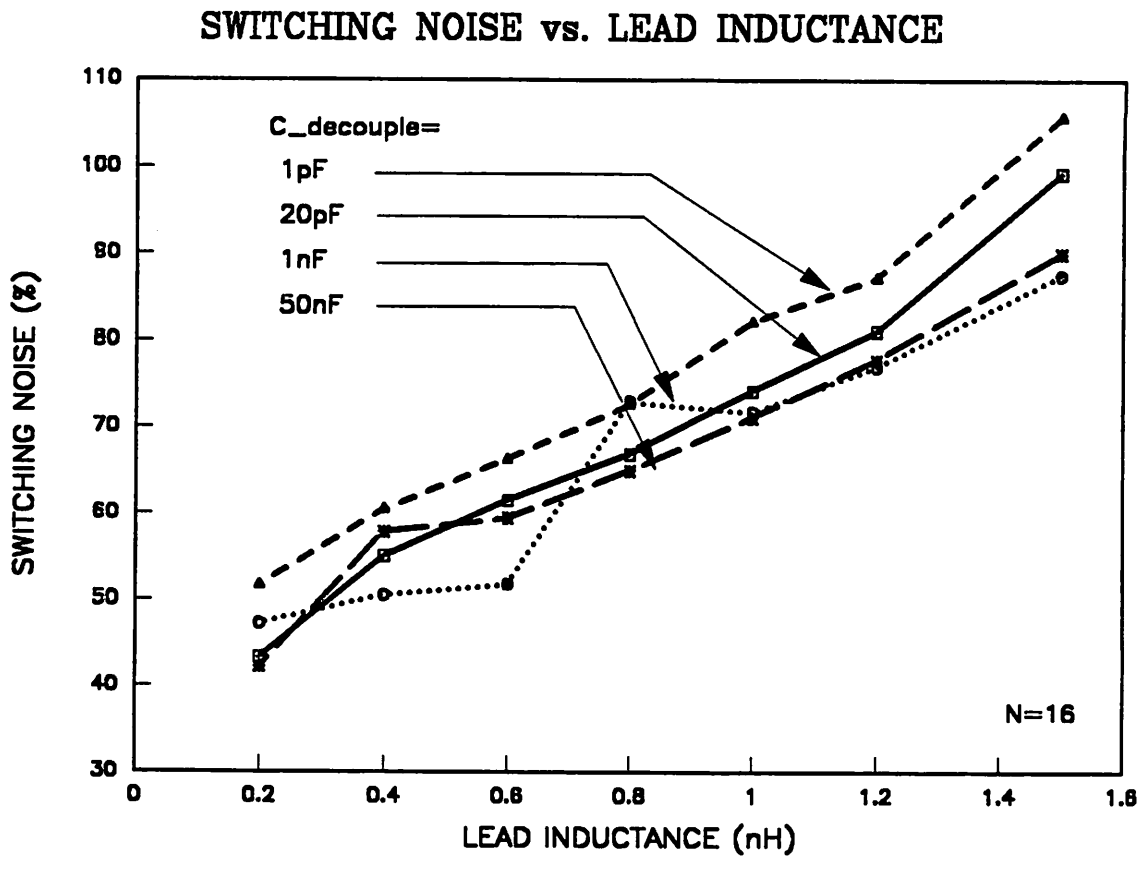

Figure 7-9. Switching noise as a function of the lead inductance. $N = 16$ and bit rate = 1 Gbps.

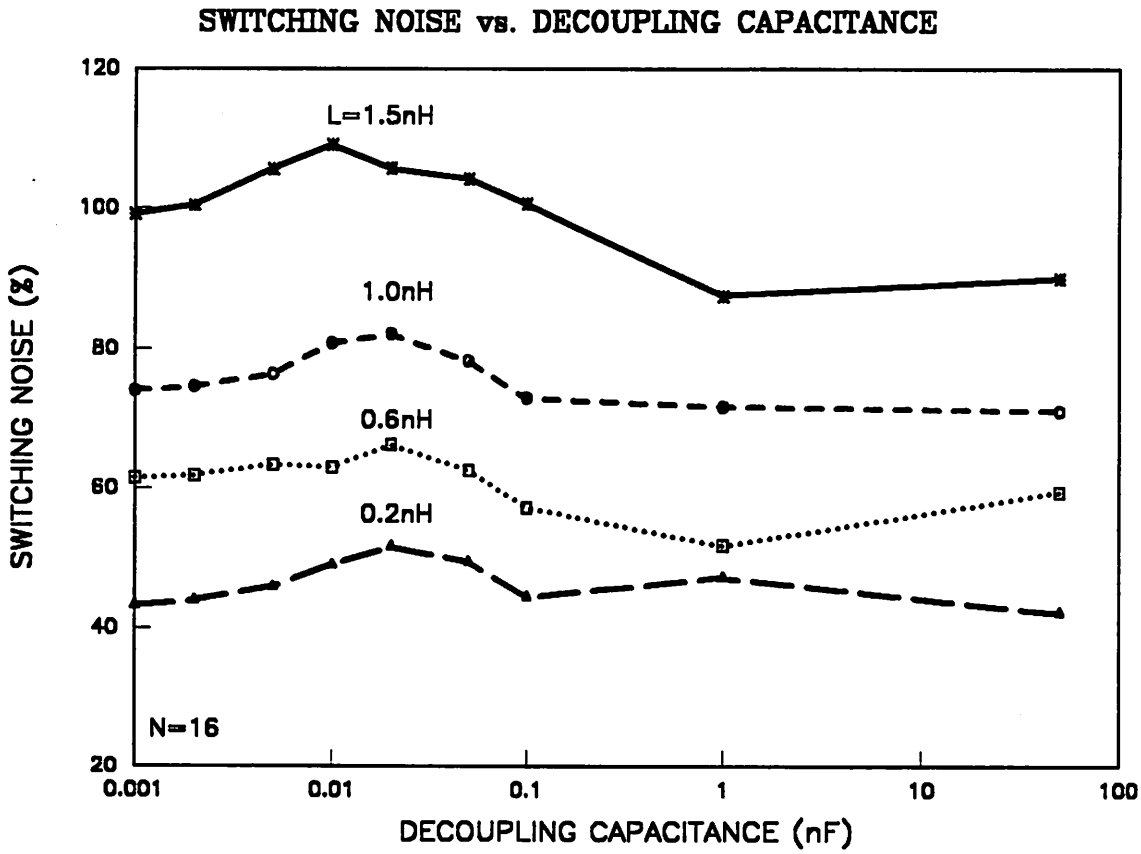

Figure 7-10. Switching noise as a function of decoupling capacitance. $N=16$ and bit rate = 1 Gbps.

CHAPTER 8 DENSE RECEIVER ARRAYS

8.1 Introduction

Electrical interference in a receiver array for dense optical interconnects is investigated in this chapter. Maximizing the receiver sensitivity is usually the primary objective in conventional receiver design for long-haul optical communication systems using on-off keying and a direct detection scheme with a propagation distance longer than a few hundred meters. For such systems, minimizing the receiver thermal noise, or equivalently maximizing the receiver sensitivity, is sufficient to optimize such performance parameters as the repeater spacing or the diameter of a network. On the other hand, thermal noise, as well as coupling noise generated by the interactions among elements in a receiver array, can limit the system performance of a dense optical interconnect system. Possible interactions among elements in a receiver array include:

- Electrical crosstalk among photodetectors due to the sharing of a common substrate,
- Electrical crosstalk due to parasitic capacitance and inductance between adjacent bonding wires,
- Switching noise due to finite bonding wire inductance of the shared power supply and ground distribution, and
- Power supply noise due to external disturbances on the power supply from other digital circuits.

All these interactions increase with the component density, the modulation speed, and the input signal level of a receiver. Optical receiver design for such an environment thus requires minimizing the combined thermal noise and coupling noise in order to optimize the overall system performance.

Both hybrid integration and monolithic integration technology can be used to package a photodetector array with an amplifier array. Hybrid integration allows separate optimization of the processing technology for the photodetectors and the amplifiers. This technology usually gives better device performance, at the expense of greater adjacent channel crosstalk and signal distortion

introduced by the bonding wires. The photodetector array in a hybrid receiver array usually has a p-i-n structure and is made of Si, GaAs or InGaAs/InP, depending on the wavelength of the light signals [122, 125]. The amplifier array is made of Si bipolar [126] or GaAs MESFET. In a monolithic integration environment, both the photodetector array and the receiver array are integrated on the same semiconductor substrate. A planar process for the photodetectors is usually preferable for easier monolithic integration with other electronic circuits.[17] Metal-semiconductor-metal (MSM) with its planar structure has thus far emerged as the most popular structure for the photodetector array [127-142].

Previously, there have been a number of receiver array designs using either hybrid integration [122, 126] or monolithic integration [123, 143-147] technology. Up to 6 and 8 channels/chip have been achieved thus far with monolithic [123] and hybrid technology [126], respectively. These receiver array designs are optimized for telecommunication applications in which sensitivity and bandwidth are the primary concern. Whether these designs can be scaled to a higher density and used in a noisy optical interconnect environment is yet to be addressed.

Electrical crosstalk between photodetectors in a p-i-n array has been previously examined in [125, 148]. It was concluded in [148] that the common substrate of a p-i-n array introduces negligible DC crosstalk. A majority of the crosstalk came from the parasitic coupling between the bonding wires connecting between photodetectors and receivers. This type of crosstalk, however, is not present in a monolithic integration environment. For this reason, the monolithic integration environment has been assumed in this chapter, and the dominant source for coupling noise is due to switching noise.

A simulation approach is used in this chapter to determine the packaging and architecture requirements to achieve a high-density optical receiver array in a monolithic integration environment. The packaging requirements include maximum allowable bonding wire inductance of the power

[17] A p-i-n structure usually has a vertical structure which requires growing of a thick epitaxial layer in order to accommodate the intrinsic region of the p-i-n structure. The thickness of the intrinsic region is at least 2 μm in GaAs and 10μm in silicon for efficient absorption of the light signals at λ=0.8μm. This process is usually incompatible with the processing steps used for electronic circuits that usually only require a thin epitaxial layer ($\leq$2μm).

supply and minimum required decoupling capacitance.[18] Possible receiver architectures evaluated are single-ended and differential receiver structures. The results show that it is possible to drive a large size ($\geq$ 32) receiver array synchronously at 1 Gbps using a differentially configured receiver structure with minimal interactions through the power supply. In contrast, a single-ended receiver array introduces much larger switching noise ($\geq$25% of the total voltage swing, or -12 dB) and thus makes a large array size difficult to achieve. We also show that a large bypass capacitance ($\sim$100 nF) is required for suppressing the switching noise in a receiver array with single-ended structure while a much smaller bypass capacitance ($\sim$1 nF) is necessary for a differentially configured receiver array.

The organization of this chapter is as follows: Section 2 describes the receiver circuit model used for the simulations. Section 3 defines the simulation methodology. Sections 4 and 5 present switching noise simulation results for a single-ended and a differential receiver array, respectively. This chapter is summarized in Section 6.

8.2 Receiver Array Model

In this section, we develop the equivalent circuits for both single-ended and differential receiver array. These models include the bonding wire inductance of the power supply in order to predict the switching noise introduced by the sharing of a common power supply.

The basic configuration for a receiver array is shown in Figure 8-1. All of the receivers in this array have identical structure and device parameters. They share the same power supply and ground through an on-chip power and ground distribution network.

The receiver model used for the single-ended configured receiver array is shown in Figure 8-2 [149].[19] Each receiver in this array consists of a shunt-series feedback preamplifier stage, a single-ended to balanced conversion stage, and an output driver stage. The photodetector in this receiver is DC-coupled to the input of the pre-amplifier. The circuit model used for the differential receiver

[18] A bypass (decoupling) capacitor is usually provided between the external power and ground to damp the ringing in the power supply voltage during a switching operation.

[19] The receiver simulation model is provided by K. Toh of T. J. Watson Research Center.

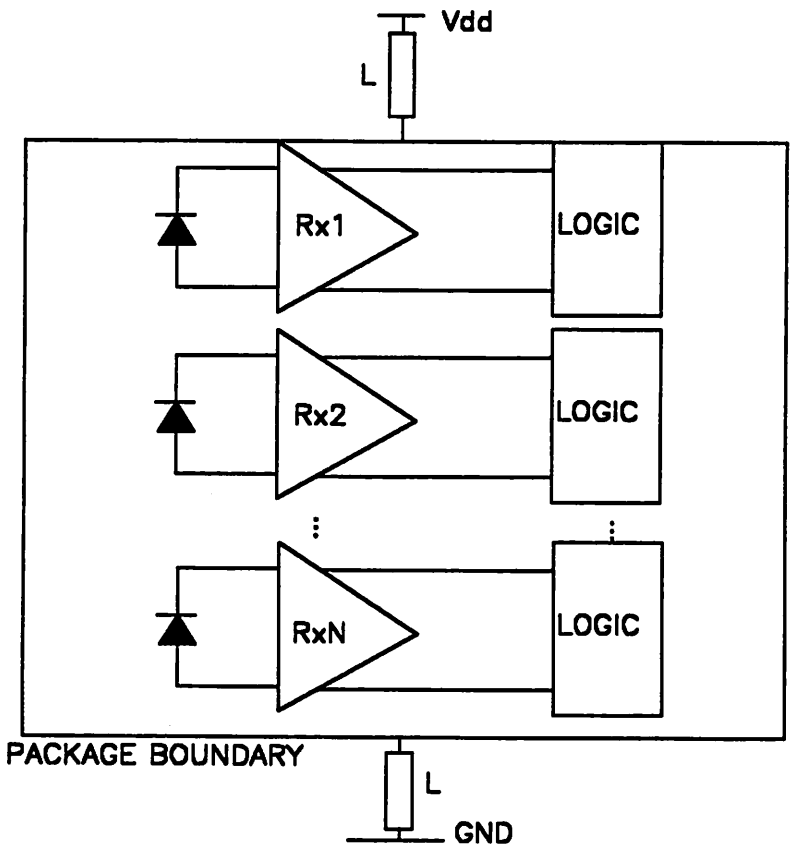

Figure 8-1. Basic configuration of a receiver array with common power supply and ground.

is shown in Figure 8-3 [150].[20] The MSM-photodetector in this case is AC-coupled into the front-end of the pre-amplifier.[21] The biasing networks of the photodetectors are not shown in Figure 8-2 and Figure 8-3. In both cases, each photodetector is modeled by an ideal current source in parallel with a capacitor representing the capacitance of the photodetector.

For the simulations performed in this chapter, the power supply inductance varied from 0.05 nH to 2 nH. The photodetector capacitance of the receiver varied from 100fF to 2pF. The bit rate

[20] The receiver model is provided by D. Rogers of IBM T. J. Watson Research Center.

[21] Since an MSM-photodetector usually requires a large bias voltage across its terminals (≥2 V), it is not possible to tie the terminals of an MSM-photodetector directly into the inputs of a differential receiver which is very sensitive to input offset voltage. Therefore, AC-coupling is necessary for an MSM photodetector to be used in conjunction with a receiver with differential front end.

varied from 100 Mbps to 1 Gbps, while the rise time and fall time of the signal varied from 6/100 to 8/10 of a bit interval. A silicon bipolar technology is assumed for the single-ended receiver while the GaAs E/D MESFET (enhancement/depletion metal semiconductor field effect transistor) technology is assumed for the differential receiver. Each receiver was loaded with an RC filter to emulate the post-amplifier and the decision circuitry.

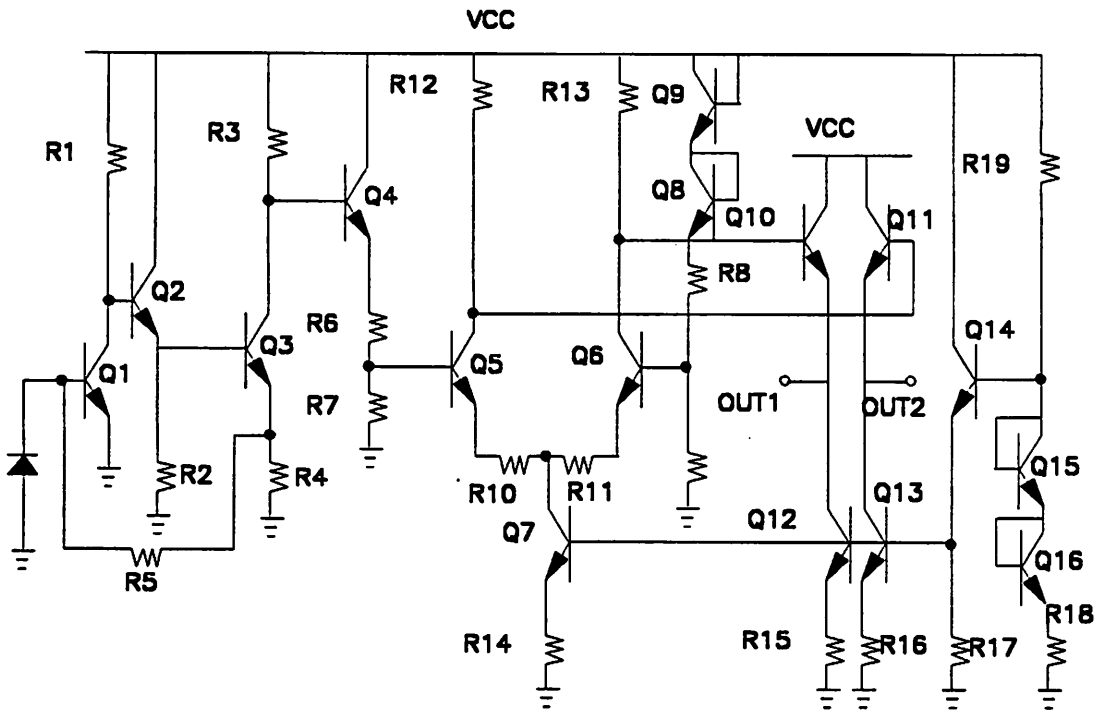

Figure 8-2. Circuit configuration of a single-ended receiver. This circuit is from [149].

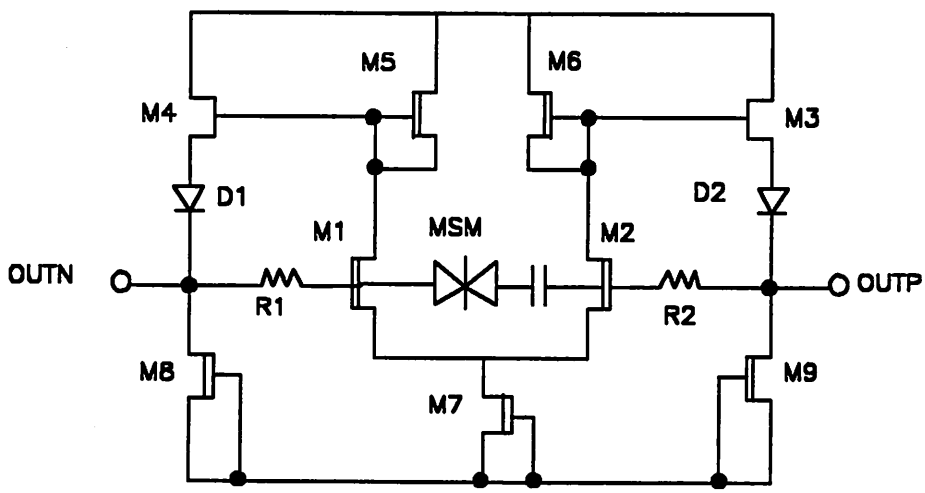

Figure 8-3. Circuit configuration of a differential receiver. This circuit is from [150].

8.3 Simulation Methodology

Similar to the simulation strategy used for simulating the electrical interference in a dense transmitter array, we simulate the situation in which $N-1$ receivers of an N-receiver array switch from ONE to ZERO or from ZERO to ONE simultaneously. The results obtained from this methodology give an upper bound on the switching noise.

N in the simulations varied from 2 to 32. The output of the quiet channel and one of the active channels were observed.

8.4 Single-Ended Receiver

For a single-ended configured transimpedance receiver array with each receiver using the same configuration shown in Figure 8-2, a significant switching noise exists at a bit rate greater than 100 Mbps if a bypass capacitor between the power-supply pad and the ground pad is not provided. Figure 8-4 shows the simulated output waveform from the channel with quiescent input when the other 15 channels switch synchronously. This waveform is overlayed with the simulated waveform from the channel with an active input, showing a maximum of 10% and 20% of switching noise

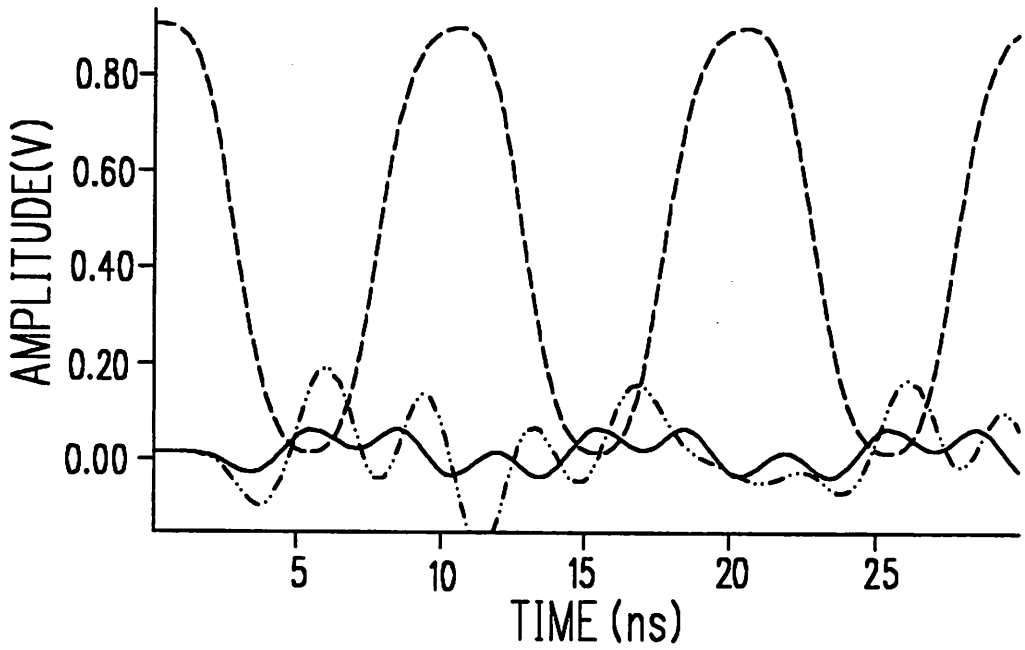

Figure 8-4. Switching noise waveform. This waveform is the output from a single-ended configured receiver with quiescent input and simultaneous switching of the other 15 receivers for an effective lead inductance of 0.5 nH and 1.2 nH. The output of a switching receiver is also shown for comparison. Bit rate and rise time of the signal is 100 Mbps and 2 ns, respectively. The photodetector capacitance, C_d, and the package capacitance, C_p, are both equal to 0.5 pF. No bypass capacitance is provided in this case.

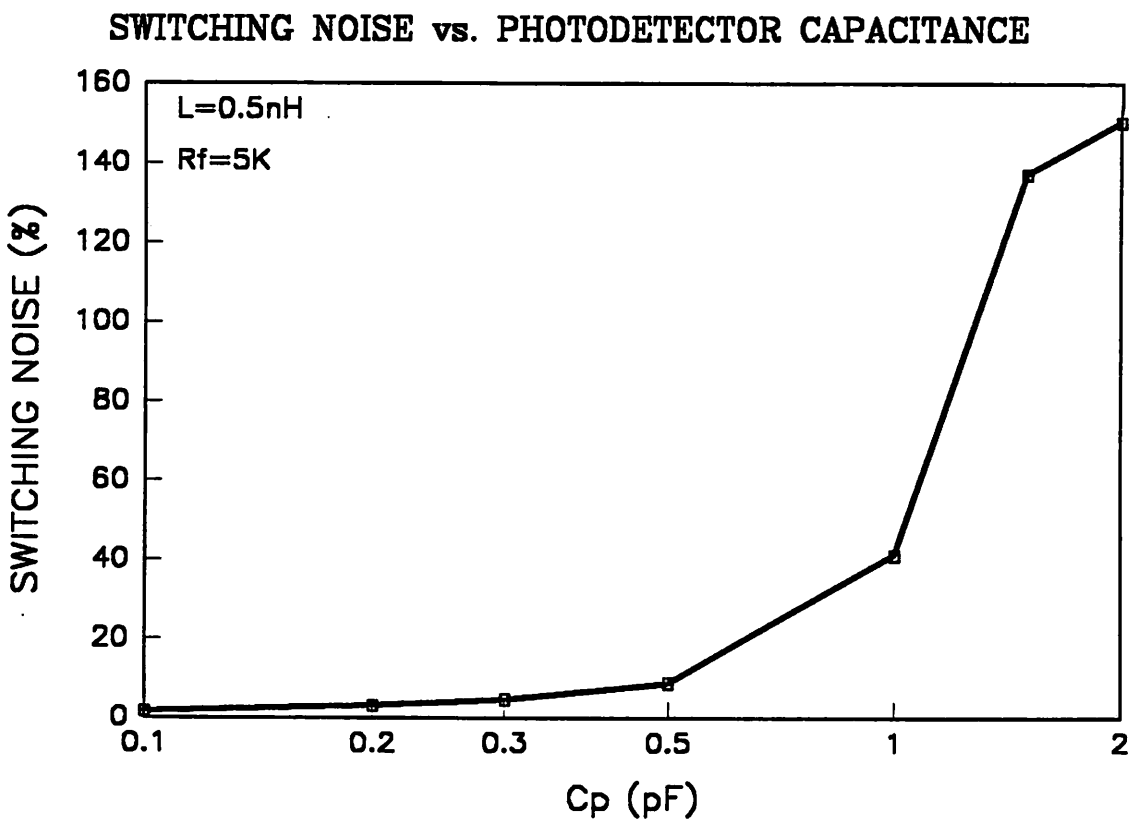

Figure 8-5. Switching noise versus photodetector capacitance. Lead inductance is assume to be 0.5 nH, while feedback resistance is 5KΩ.

is reached when the corresponding effective bonding-wire inductance of the power supply is 0.2 nH and 0.5 nH, respectively.

As the photodetector capacitance increases, the coupling between the power supply and the input of the pre-amplifier increases and the amount of switching noise increases accordingly, as shown in Figure 8-5. Figure 8-6 shows a small bypass capacitor (0.5 nF ~ 2 nF) helps to reduce the switching noise, but a large bypass capacitor (≫ 2 nF) is necessary to eliminate the switching noise completely. However, a large bypass capacitor is very difficult to incorporate into an integrated circuit due to its excessive area requirement,[22] indicating that more power supply and ground

[22] On a GaAs chip, each picofarad of capacitance requires an area of 92μm×92μm.

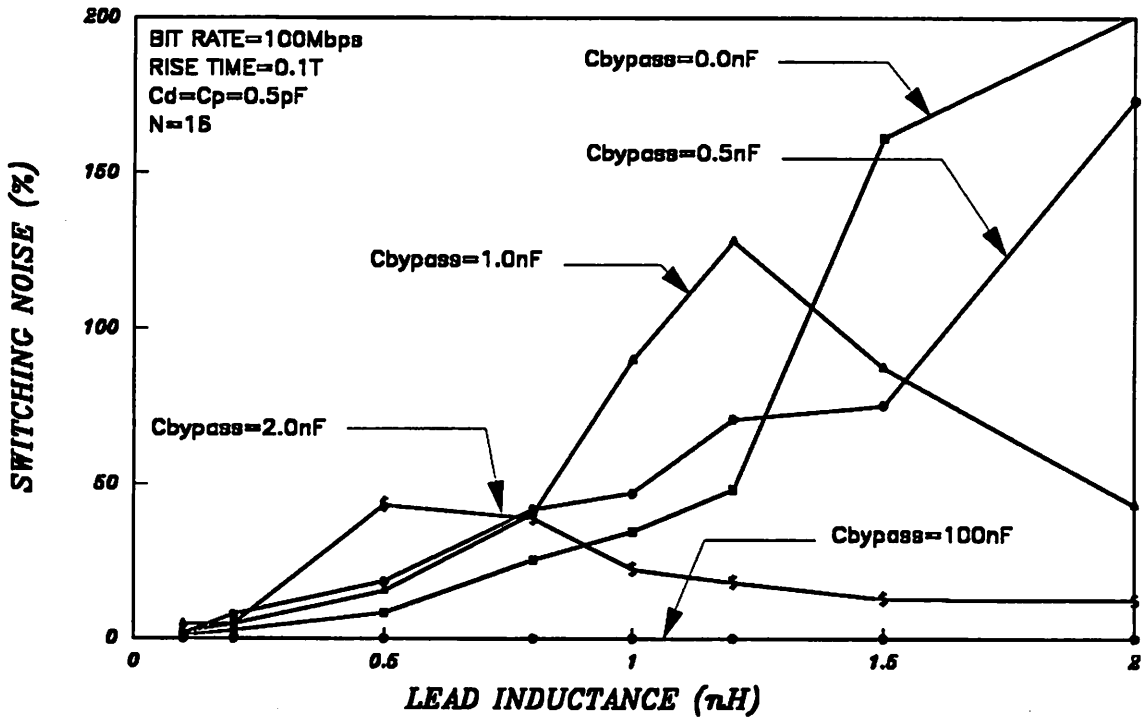

Figure 8-6. Switching noise versus lead inductance for a single-ended configured receiver array with N = 16. Bit rate and rise time of the optical signal are 100 Mbps and 1 ns, respectively. Other operating conditions are similar to those of Figure 8-4.

pads are required to reduce the effective power supply and ground lead inductance. Furthermore, we can observe from Figure 8-6 that the value of the lead inductance where a maximum switching noise occurs decreases with increasing bypass capacitance. By fixing the value of the lead inductance (e.g. 1 nH), the switching noise increases at first as the bypass capacitance increases from zero to 1 nF before the switching noise drops as the bypass capacitance increases above 2 nF. This suggests a small bypass capacitance ($\leq$2 nF) for a single-ended receiver does not suppress the switching noise. The shift of the lead inductance value where a maximum switching noise occurs is due to the shift of the LC-resonant condition formed between the bypass capacitance and the lead inductance.

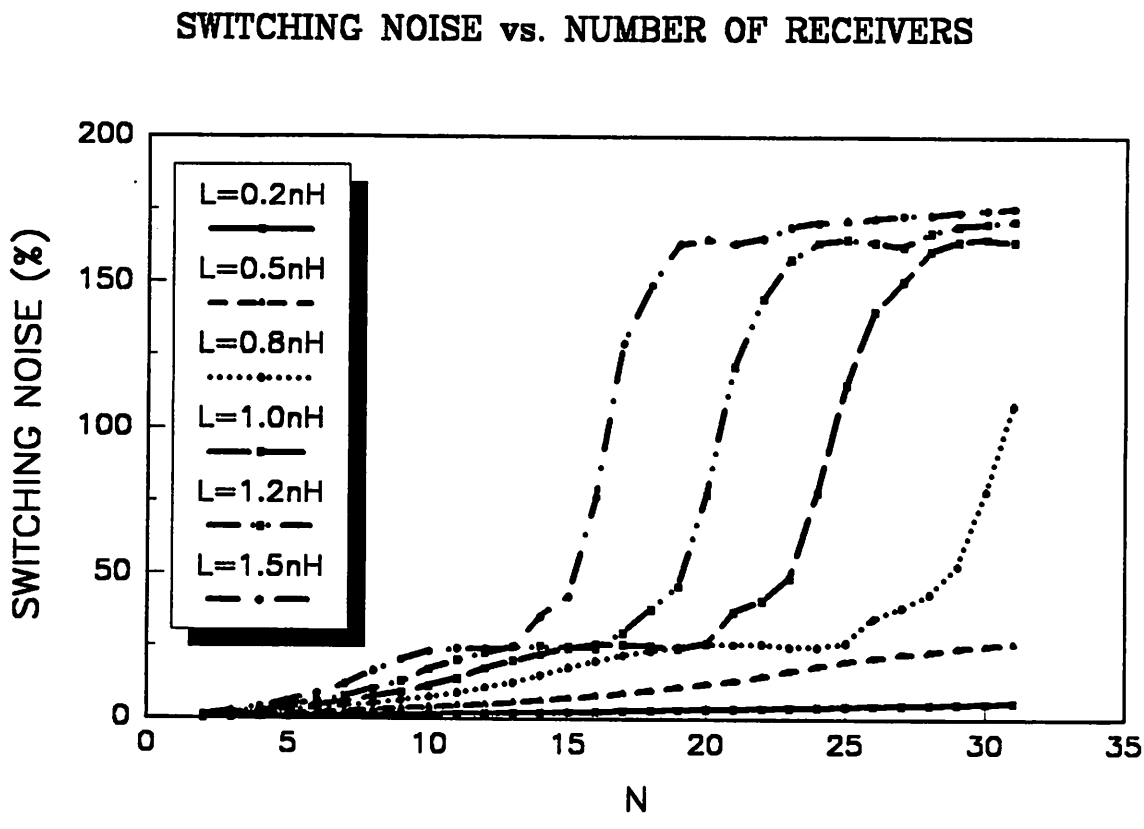

Figure 8-7. Switching noise generated by a single-ended configured receiver as a function of array size. Bit rate is 100 Mbps, rise time is 1 ns, and no bypass capacitor is provided.

Figure 8-7, Figure 8-8, and Figure 8-9 show the relationship between the amount of switching noise as a function of the number of receivers for various values of bypass capacitance. The switching noise has a nonlinear dependency on the number of receivers when no bypass capacitance is provided. Assuming the lead inductance equals 1.5 nH, the amount of maximum switching noise first increases linearly with N until $N = 10$, after which the switching noise remain essentially constant at 25% between $N = 10$ and $N = 13$. The switching noise rises sharply from 25% to 150% as N increases from 13 to 18. The amount of switching noise levels off to 175% at N equals 18 since the preamplifier saturates at this point. As the lead inductance decreases, the switching noise levels off at a larger value of N. The slope of the increase in switching noise as a function of N

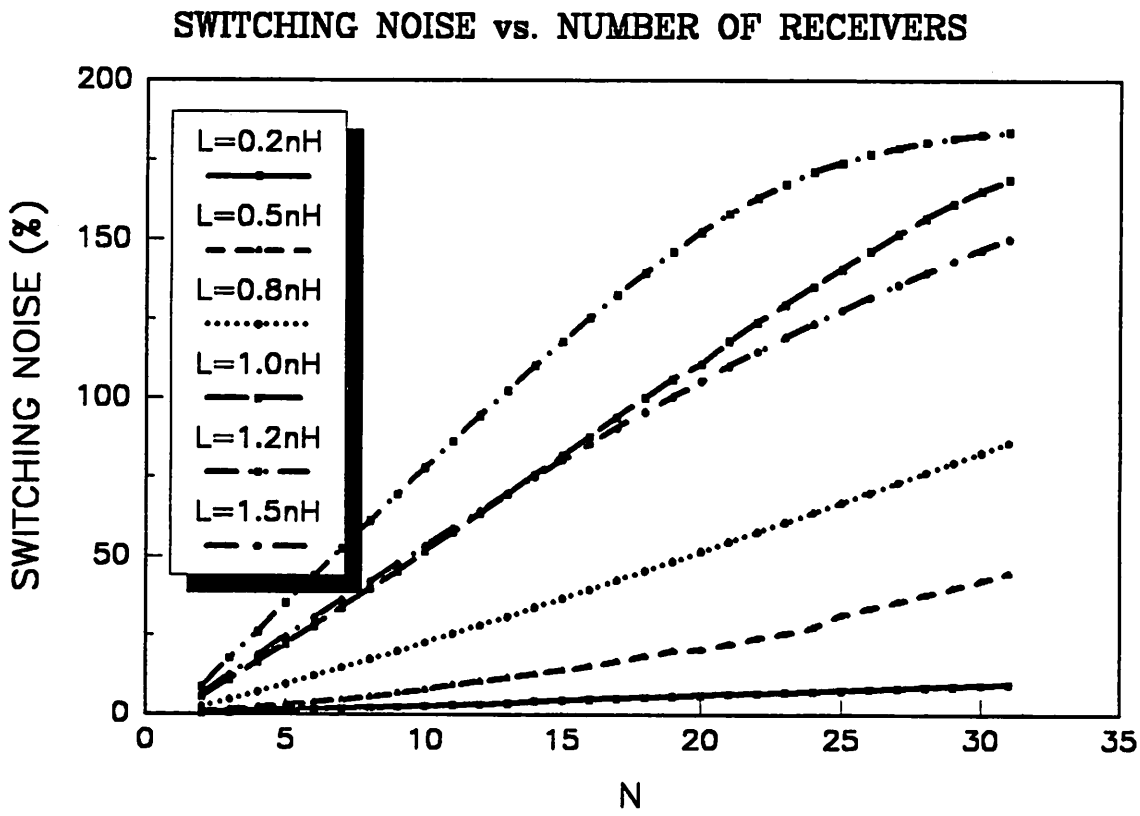

Figure 8-8. Switching noise generated by a single-ended configured receiver as a function of array size. All the simulation condition is similar to Figure 8-7 except a bypass capacitor of 1 nF is provided between power and ground.

decreases as the lead inductance decreases. In contrast, the slope of the increases in switching noise becomes much less dependent on the lead inductance as the first level off point is passed.

The mechanism for this phenomenon can be understood as follows: There is limited power supply noise cancellation capability in this receiver due to the common-mode rejection in the single-ended to balance conversion stage. Note that the input voltage to Q6 in Figure 8-2 is derived from both power and ground:

$$V_{B6} = \frac{R_9 V_{CC}(t) + R_8 GND(t)}{R_8 + R_9} - 2(1 + \frac{R_8}{R_8 + R_9})V_{BE} \qquad (8.1)$$

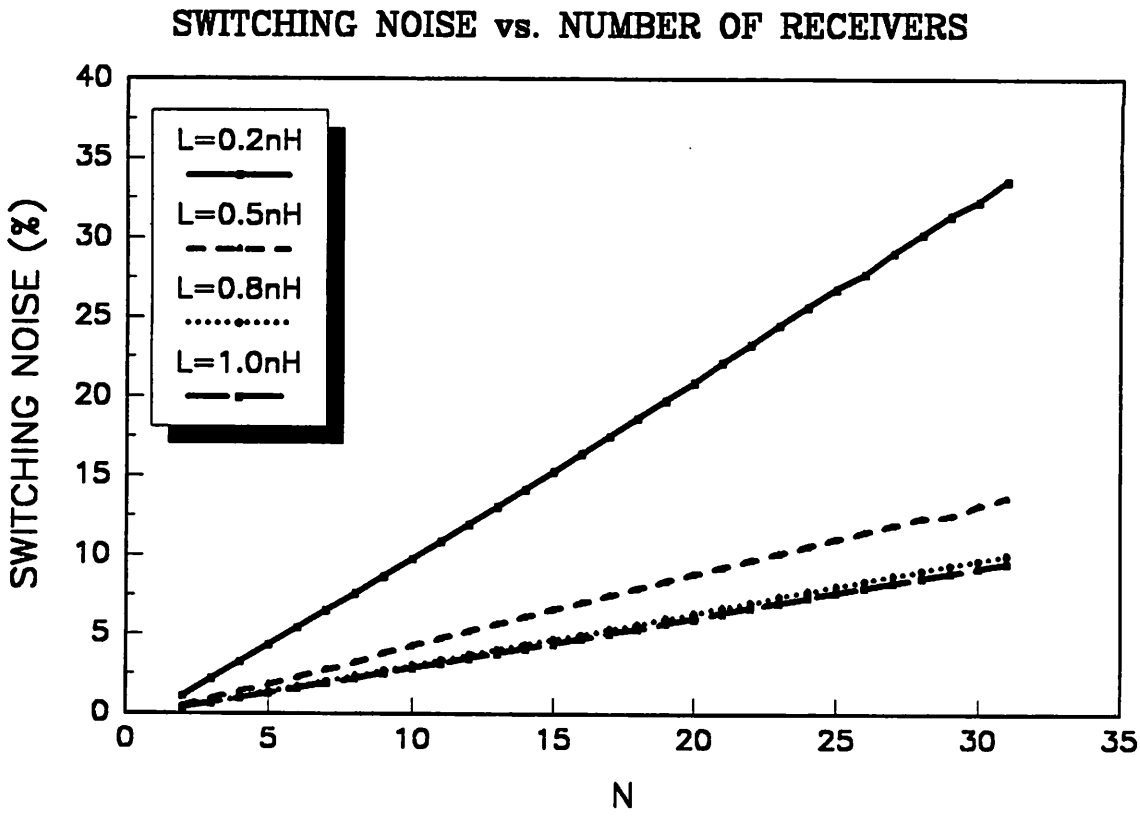

Figure 8-9. Switching noise generated by a single-ended configured receiver as a function of array size. All the simulation condition is similar to Figure 8-7 except a bypass capacitor of 2 nF is provided between power and ground.

The values for R_8 and R_9 chosen in the circuit simulation are 150Ω and 1450Ω, respectively; the voltage V_{B6} thus reflect less ground voltage change than the power supply voltage change. Coupling of ground and power supply disturbance into the circuit are through independent electrical paths. The phase difference between the power supply and ground disturbance thus critically affects the effectiveness of this common-mode rejection capability. This single-ended to balance conversion stage becomes a positive feedback stage as the power disturbance becomes large, resulting in the oscillation of the receiver. From Figure 8-7, we conclude that a maximum receiver array size of 20 is allowed for a lead inductance $\leq$1 nH, assuming the maximum allowable switching noise is 25%(−12 dB).

As the bypass capacitance increases from zero, the dependence of switching noise on N becomes linear, as shown in Figure 8-8 and Figure 8-9. This is because the bypass capacitance introduces coupling between the power and ground and thus provide a linkage between the disturbance on the power supply and ground. The voltage of the reference input for single-ended-to-balanced conversion stage (V_{B6}) therefore has the capability of tracking the power supply and ground disturbance more accurately.

8.5 Differential Receivers

Figure 8-10 shows the switching noise waveform generated from a receiver array of size 4 with each receiver using a differential configuration shown in Figure 8-3. The switching noise is suppressed by the common-mode rejection of the differential input-stage at the sacrifice of higher thermal noise ($\leq$3 dB) because of the differential front-end. The amount of switching noise only slightly increases as the rise time decreases, as shown in Figure 8-11. The switching noise as a function of lead inductance for various bypass capacitance is shown in Figure 8-12. The maximum switching noise for 2 nH lead inductance is less than 12%($-$18.4 dB) at 1 Gbps for a receiver array of size 16 even without a bypass capacitor. In contrast to the case of the single-ended receiver, even a small amount of bypass capacitance is effective in eliminating the switching noise. For a bypass capacitance equal to 1.0 nF, the maximum switching noise is less than 0.05% for almost any practical range of lead inductance value.

8.6 Summary

In this chapter, simulation has been used to determined the maximum switching noise for both single-ended and differential receiver configurations under various packaging conditions. The switching noise can be the dominant noise source in a receiver array. It is possible to drive a large number ($\sim$32) differentially configured receivers at 1 Gbps in a monolithic integration environment using the criterion of $-$12 dB maximum allowable crosstalk with a single power supply. It is more difficult to obtain similar performance from a single-ended configuration without the help of a large bypass capacitor ($\geq$100nF).

We also show that there exists a trade-off between minimizing the thermal noise and minimizing the switching noise in a receiver array design. A differentially configured receiver has 3 dB

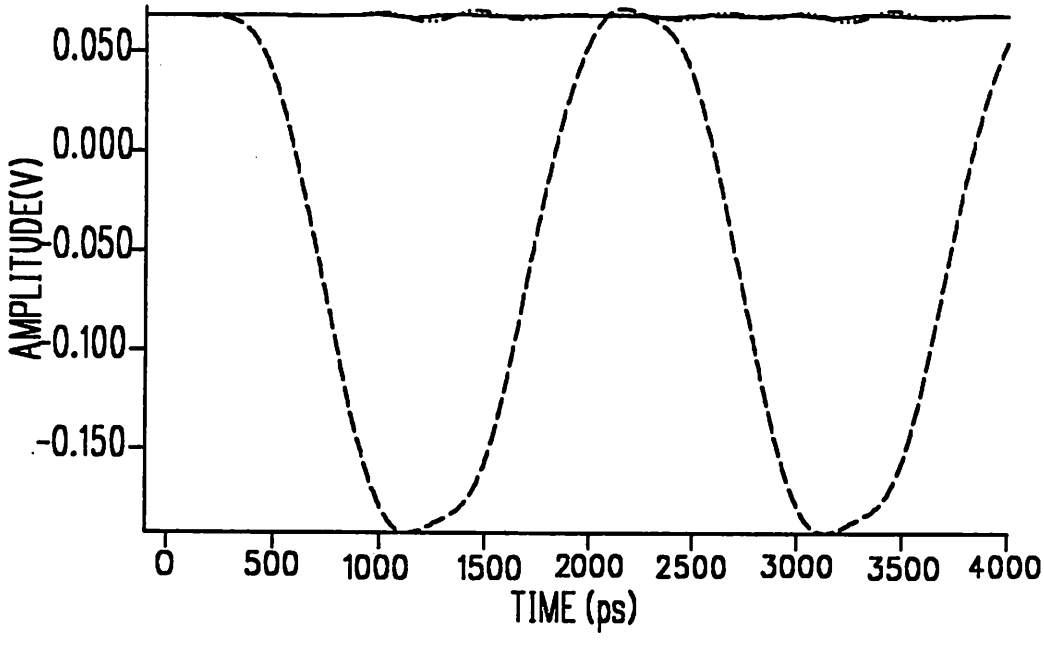

Figure 8-10. Switching noise generated by a differentially configured receiver array. The array size is 4, and the lead inductance varied from 0.05 nH to 2 nH. Each receiver is operating at 1 Gbps with rise time 100ps. No bypass capacitor is provided in this simulation.

more thermal noise due to its double sided front-end but performs much better in switching noise rejection. A differentially configured receiver structure is thus more favorable for a large size receiver array design.

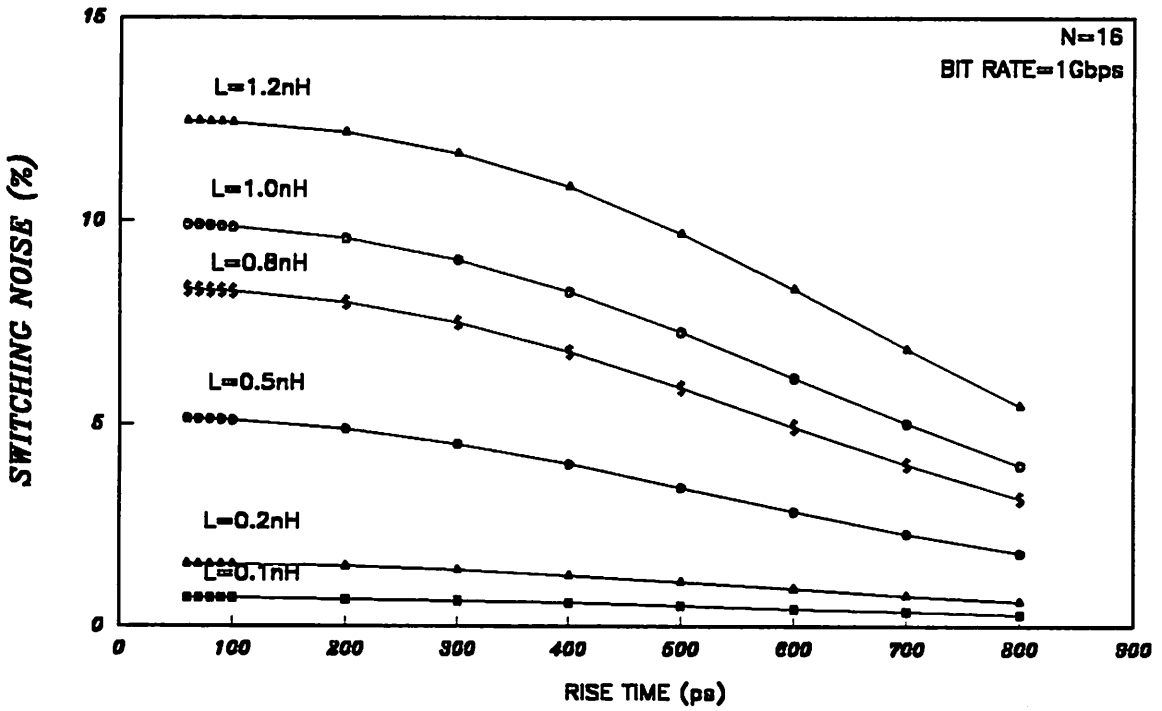

Figure 8-11. Switching noise versus signal rise time for a differential receiver array with N = 16. Bit rate is 1 Gbps, no bypass capacitor is provided in this case.

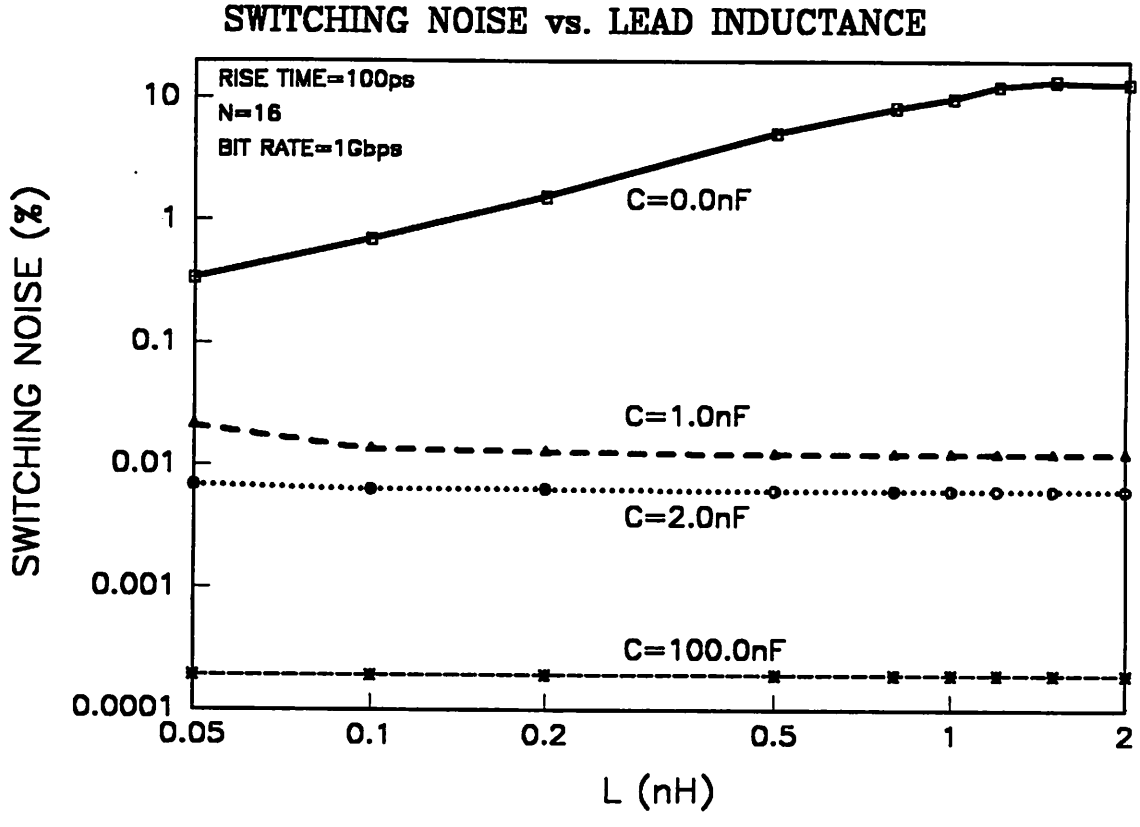

Figure 8-12. Switching noise versus lead inductance for a differentially configured preamp. Rise time of the optical signal is 100 ps, size of the receiver array is 16, and bit rate is 1 Gbps.

CHAPTER 9 DIFFERENTIAL OPTICAL INTERCONNECTS

9.1 Introduction

As shown in earlier chapters, optical interconnects at the backplane and the board levels can provide much larger bandwidth, higher density, superior immunity to ground-loop noise and reflection noise than metal interconnects. However, electro-optical components such as the laser driver and optical receiver used by an optical interconnect system usually have to operate in a noisy environment. In this environment, switching noise generated by the nearby digital circuits or adjacent optical interconnects might be coupled into the electrical path of an optical interconnect, either through power distribution or through parasitic capacitive and inductive coupling among neighboring interconnects.

In Chapters 7 and 8, we have shown that a fully differential structure can minimize the interference between adjacent channels and maximize the immunity to external power and/or ground disturbances in a transmitter or receiver array. By generalizing this concept, the interconnect system can have a fully differential structure in which both data and its complement are simultaneously transmitted. Some potential advantages of such an interconnect structure include:

- The optimal threshold at the output of the receiver does not depend upon the absolute value of the signal levels.
- Complicated AGC circuits at the receiver side might be simplified or even eliminated.
- This structure allows photodetectors to be DC-coupled into a receiver with a differential front-end and therefore does not require scrambling or encoding of the transmitted data stream.
- Due to its balanced operation throughout the interconnect, this architecture is less vulnerable to common-mode noise generated from the power supply, ground, switching, and parasitic coupling than those interconnect structures considered in earlier chapters.

All these advantages can be achieved without having to add substantial complexity to the existing electrical circuits.

The fully differential optical interconnect concept was first applied in free space optical interconnect using S-SEED's (symmetric self-electro-optic devices) [151] due to the poor contrast ratio of the SEED device [152-155]. But the generalization of this concept to optical interconnects using other electro-optic devices and a comprehensive system analysis of this architecture has yet to be developed.

In this chapter, several candidate structures for differential optical interconnects are investigated. The most straightforward implementation of a differential optical interconnect uses two laser diodes, two spatially-separate interconnects (waveguides or fibers) and two photodetectors. In more sophisticated implementations, differential channels can be combined in the

- frequency domain (FSK),
- wavelength domain (WDM),
- time domain (Manchester encoded), and
- polarization domain,

resulting in interconnect architectures which have the same number of waveguides (or fibers) as in the single-ended interconnect structures.

Based on these structures, the signal-to-noise ratio (SNR) and the system penalty due to channel mismatch are analyzed and the results are compared to those of a single-ended interconnect with similar driver and receiver structures. From this analysis, we show that

- The SNR of differential optical interconnects is similar to that of single-ended structures.
- System penalty due to mismatch is negligible if there exists a slight channel mismatch ($\leq$10%). However, a large power penalty ($\geq$2dB) is introduced as the mismatch between differential channels becomes significant ($\geq$40%).

Since channel mismatch can limit the system performance, several channel mismatch cancellation techniques are described later in this chapter.

The organization of this chapter is as follows: Section 2 compares the relative merits of different optical interconnect structures that can be used in a dense optical interconnect environment. Section 3 examines feasible implementation techniques of differential optical interconnects. Section

4 analyzes and compares the noise performance of single-ended and differential optical interconnect systems. System performance degradation due to channel mismatch is studied in Section 5. Various mismatch cancellation techniques are described in Section 6. This chapter is summarized in Section 7.

9.2 Optical Interconnect Architectures

In this section, we examine possible interconnect structures that can be used for an optical interconnect. The merits and drawbacks of each structure are then evaluated qualitatively.

9.2.1 Single-Ended Interconnect

There are four possible structures for a single-ended interconnect, as summarized in Figure 9-1 Possible driver structures for a single-ended interconnect can be either single-ended or differential, as discussed in Chapter 7. When a differential current switch is used to drive a laser, the unused branch of the current switch is usually tied to the power supply.

Similarly, both single-ended and differential front-end structures can be used for the receiver, as discussed in Chapter 8. When a differential front-end is used, the photodetector is usually AC-coupled with the receiver because the photodetector and the front-end of the receiver have different biasing requirements.[23] A loss of low-frequency spectral component from the data stream is unavoidable for an AC-coupled front-end because a large AC-coupling capacitor is difficult to integrate in an LSI or VLSI system. This dictates that the data has to be encoded or scrambled in order to eliminate the DC and low frequency spectral components.

9.2.1.1 Disadvantages

First we consider the combination of a differential driver with a single LD/LED device, as shown in Figure 9-1(b) and (d). Differential configuration are usually used to reduce the switching noise in a laser driver. These configurations are not desirable because:

- Switching noise is large in structure (b) due to the use of a single-ended configured receiver array.

[23] In theory, it is possible to differentially coupled a detector to a differential preamplifier without a capacitor, but it most likely will suffer from large offset voltage or a degradation in sensitivity.

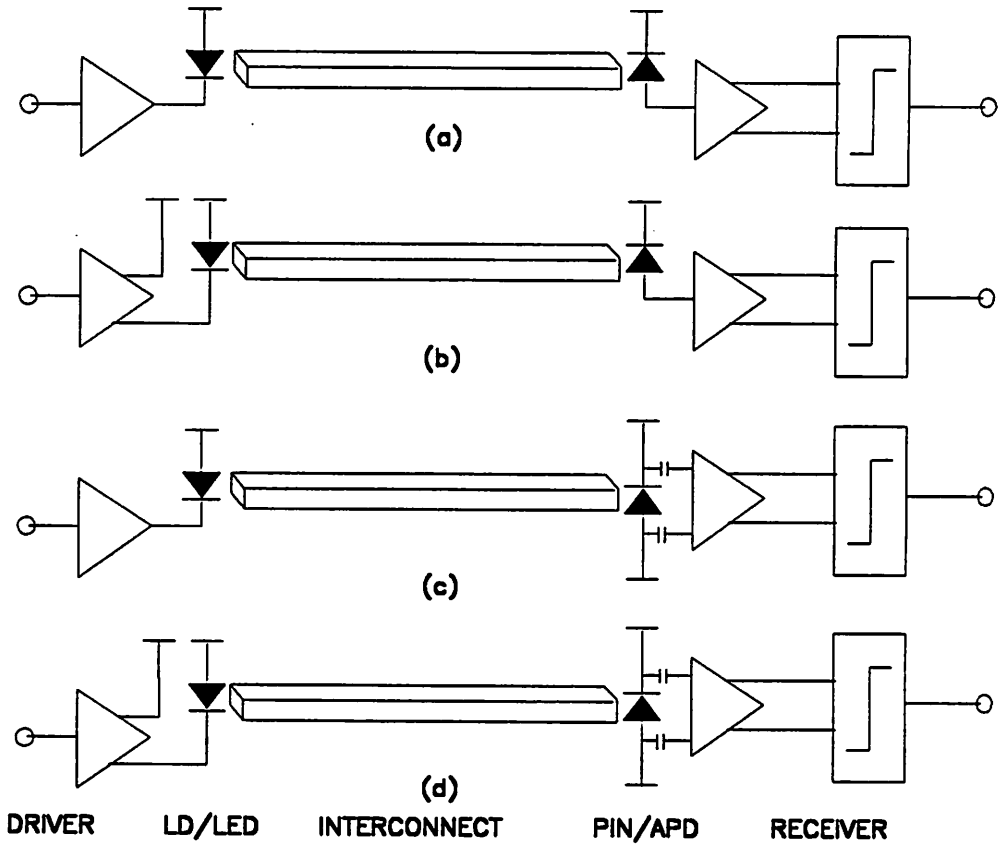

Figure 9-1. Possible structures for a single-ended optical interconnect. (a) Single-ended driver, single-ended receiver. (b) Differential driver, single-ended receiver. (c) Single-ended driver, differential receiver. (d) Differential driver, differential receiver.

- Line coding is required in structure (d) because the photodetector is AC-coupled to the preamplifier.
- Matching the load of the driver arms with appropriate passive and/or active devices for these configurations is difficult due to the low resistance (~5Ω) and high capacitance (~5 pF) of an LD/LED device. If the LD/LED's are not monolithically integrated with the drivers, the lead inductance of the bonding wire between the LD/LED's and the drivers introduces additional imbalance and waveform distortion for high-speed operations.
- Slight imbalance at the load of a differential laser driver could induce a nonnegligible amount of switching noise, as shown in Chapter 7.

It is also possible to have the laser driver drive two laser diodes with one of the laser diode unconnected. The purpose of having this laser diode is to serve as a dummy load for the laser driver to reduce the switching noise of the driver array.

Now let us consider the combination of a single PIN/APD with a differential receiver, as shown in Figure 9-1(c) and (d). These combinations are not satisfactory because:

- DC-coupling is difficult to achieve. This is due to the following conflicting requirements when DC-coupling a photodiode to the front-end of a differential receiver: On one hand, it is necessary to maintain a sufficient bias for a photodetector to maximize its quantum efficiency. On the other hand, it is necessary to minimize the input offset voltage to the front-end of the differential receiver.
- An AC-coupling design requires a large chip area.[24] In principle, two AC coupling capacitors can be used to couple the terminals of a photodetector to the front-end of the receiver. However, this configuration usually requires an excessive area in order to achieve a low cut-off frequency, which is determined by the impedance of the detector bias network and the coupling capacitance. Alternatively, it is possible to AC-couple one terminal of the photodetector and DC-couple the other one. But this configuration requires a level restoration circuitry to cancel the possible DC level shifting at the other terminal due to different light input levels.
- AGC or limiting receiver design is required [56]. Incoherent detection of light does not allow transmitting antipodal signals since only the optical power of the signal is detected. The detection of this type of signal is thus sensitive to the absolute value of the threshold. However, the optical power usually arrives at the receiver with a wide dynamic range because of the possible large variation in propagation loss, coupling loss, and the need to provide fan-out. Additional tolerance has to be provided to allow device variations and device aging. Therefore either an automatic gain control mechanism or a limiting amplifier stage is necessary to maintain a constant logic swing. However, using AGC circuitry requires a DC-balanced data stream

[24] The required area of an AC-coupling capacitor depends on the cutoff frequency of the data spectrum. Lower cutoff frequency requires larger AC-coupling capacitor. Line coding of the data stream usually can help to increase the cutoff frequency and reduce the area required by the AC-coupling capacitor.

while using a limiting amplifier results in an unequal noise power for logical ONE's and ZERO's.

Both the requirements for AC-coupling (for easier receiver design) and AGC (to enhance the dynamic range) necessitate line coding techniques such as Manchester [156] or 8B/10B code [157] to maintain a DC-balanced data stream. However, encoding/decoding implies a reduction in the effective bandwidth available to the data and an increase in latency. Furthermore, bit timing has to be recovered for each interconnect and the timing recovery circuitry at the receiver might occupy a large chip area and thus limit the interconnect density. Therefore, the usefulness of this type of optical interconnect is only restricted to delay-insensitive applications.

The interconnect structure in Figure 9-1(a) is not suitable for a dense optical interconnect because of the large switching noise incurred as described in Chapter 7 and 8.

9.2.1.2 Advantages

The single-ended configuration requires the least number of optical and opto-electronical components at the expense of additional complexity in the electronic components. If the interconnect is not in a critical path of a digital system and can afford encoding/decoding delay, single-ended interconnect has the potential of offering the highest interconnect density for asynchronous channels, only limited by the switching noise incurred at the photodetectors.

9.2.2 *Differential Interconnect*

There are two possible structures for a differentially configured optical interconnect, as summarized in Figure 9-2. The driver for this type of interconnect has to be differentially configured, while the receiver can be either single-ended or differentially configured. The photodetectors can be either AC- or DC-coupled to the receiver.

9.2.2.1 Disadvantages

The number of optical and opto-electronical components such as the waveguides, photodetectors, laser diodes, and, depending on the modulator structure, some types of modulators are doubled in this configuration. This has an adverse impact on interconnect density and system reliability. Furthermore, mismatch of the parameters along a differential link such as the threshold

current and differential quantum efficiency of the laser diodes, the attenuation of the interconnects, and the quantum efficiency of the photodetectors can introduce additional system penalty.

9.2.2.2 Advantages

In contrast to the single-ended interconnect configurations, a fully differential optical interconnect architecture enjoys the following advantages:

- Self-thresholding. As discussed previously, incoherent detection of light does not allow transmitting of antipodal signals since only the power of the light signal is detected. In addition, a constant logic swing has to be maintained at the output of a receiver so that the digital logic can have a constant decision threshold, which is usually achieved by using an automatic gain

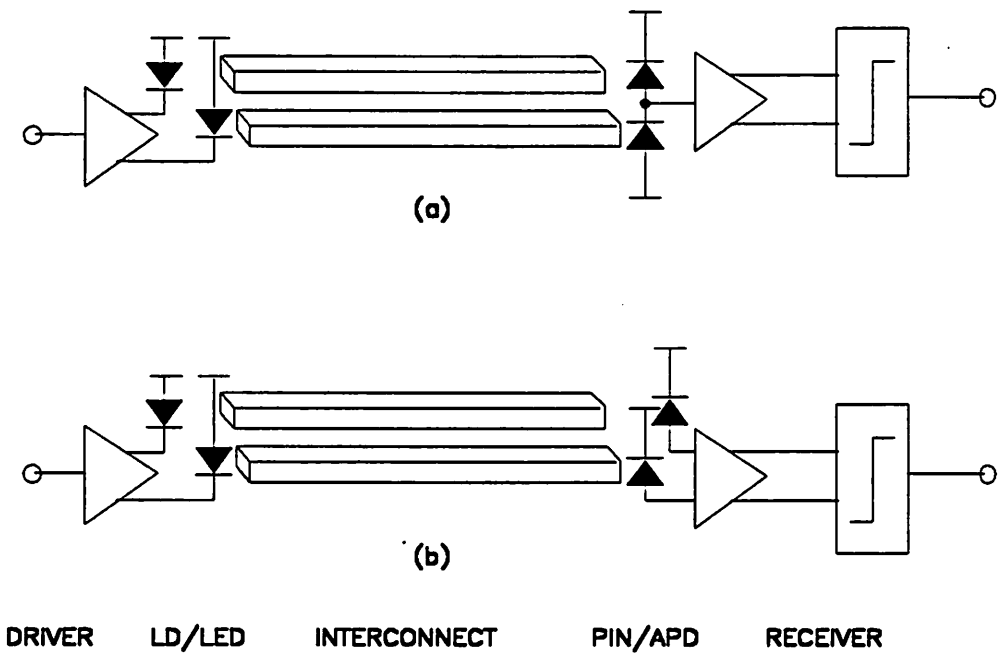

Figure 9-2. Possible structures for a differentially configured optical interconnect. (a) Single-ended receiver. (b) Differential receiver.

control circuitry. Since both the noninverted and inverted signals are always present in a differential optical interconnect, the determination of a logical ONE vs. a logical ZERO can be achieved by simply subtracting the signals coming out of the inverting channel from the signals coming out of the noninverting channel, and using differential zero as the threshold to distinguish between ONE's and ZERO's. This is important because the light output from the LD/LED, the propagation loss, the number of fan-out as well as the light coupling can vary from one interconnect to another and give rise to a wide dynamic range of the light signals at the receiver. In addition, the absolute value of the light output may degrade over time as well as due to variations in temperature. Therefore, it is very difficult to maintain satisfactory system performance of an interconnect system that derives the optimal decision threshold from the incoming signals without using complicated bias compensation at the driver and an AGC mechanism at the receiver.[25]

- Less vulnerable to common-mode noise. Differential amplification is always less vulnerable to common-mode noise. Therefore, the proposed differential optical interconnect is less sensitive to the power supply and ground noise of the transmitter, in which the noise is incorporated as common-mode signals. In addition, the transmitter and the receiver structures are more balanced than those in a single-ended interconnect and is therefore less vulnerable to distortion, waveform jitter, and switching noise.
- Allows easy DC-coupling to the front-end of a differential receiver. Both DC- and AC-coupling are straightforward for this configuration.
- Allows DC-unbalanced data streams, and thus eliminates the requirements for encoding/decoding. This could be extremely important whenever the interconnect has to be used in a critical path that does not allow encoding/decoding delay.

---

[25] The comparison between differential optical interconnects and single-ended optical interconnects is similar to that between FSK and OOK in classical communications. It has been well-known in communication theory [156] that given the same symbol distance and hence noise immunity, the symbol constellation of phase-shift keying (PSK) requires 3dB less in signal power than that required by frequency-shift keying (FSK) or on-off keying (OOK) due to the antipodal symbol constellation of PSK. In terms of the required energy per bit to achieve the same bit-error-rate, the performance of FSK is exactly the same as OOK. In practice, however, a constant decision threshold can be maintained in an FSK environment while the optimum threshold depends on the absolute amplitude of the light intensity in an OOK environment.

9.3 Implementation of Differential Optical Interconnects

The differential optical interconnect structure discussed in the last section assumes a straight-forward implementation in which two laser diodes, two waveguides, and two photodetectors for each channel are used. In this section, other techniques that can be used to implement a differential optical interconnect system are discussed and evaluated. These techniques have the potential of reducing the number of laser diodes or/and the number of waveguides.

9.3.1 External Modulators

Instead of using two lasers for each channel, it is possible to use just one laser and one external modulator (or two external modulators if the quantum well modulator is used) to generate the differential optical signals. The number of light sources can be further reduced by having several channels sharing the same *optical power supply*. The number of waveguides or photodetectors are not affected in this approach.

External modulators such as a Mach-Zehnder type interferometer, directional coupler, or total internal reflection (TIR) modulator [158-160] on $LiNbO_3$, $GaAs$, or InP substrates can be used for generating differential light output from a single light source. Most of these devices are based on the electro-optic effect, in which the refractive index of the material ($LiNbO_3$ or $GaAs$) and therefore the *effective* propagation path length changes when a voltage is applied. The refractive index change can also be induced by carrier injection or depletion in semiconductor materials (Si, $GaAs$ or InP). For a Mach-Zehnder type interferometer as shown in Figure 9-3, the input wave splits into equal components after the input 3dB coupler. If no phase shift is introduced by the electrode, the input power is completely coupled into the other waveguide after the output 3dB coupler. On the other hand, the power will be completely coupled back to the input waveguide if a π phase shift is introduced to the optical signals by the electrode. A directional coupler, as shown in Figure 9-4, operates by a similar principle. Two identical strip waveguides are brought into proximity over a length of L. In Chapter 5, we showed that optical power couples between two single-mode waveguides in an oscillatory fashion. Therefore, it is possible to design a coupler such that the power coming from the input waveguide will be coupled into the other waveguide completely without having to apply voltage to the electrode. On the other hand, the power will stay in the

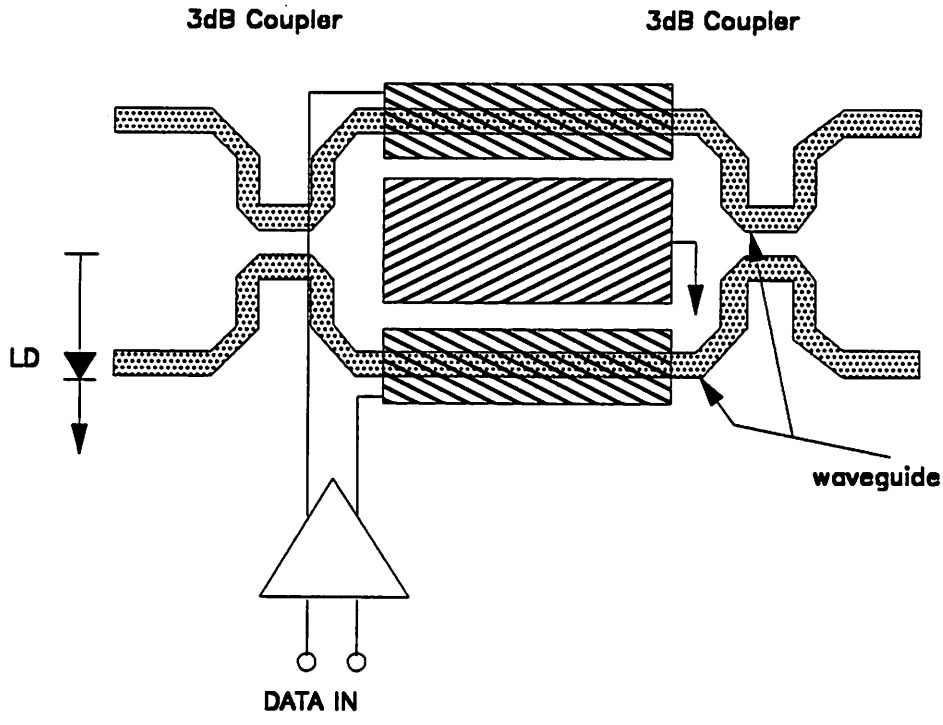

Figure 9-3. Structure of a Mach-Zehnder modulator.

same waveguide if a voltage is applied. For a modulator using total internal reflection as shown in Figure 9-5, the electro-optically induced index change [158] or carrier-induced index change [161] will cause the light incident in the top left waveguide to be reflected to the top right. The light will remain in the incident waveguide and come out at the bottom right waveguide if no voltage is applied. Modulators using the electro-optic or carrier-depletion effect to induce refractive index change have the potential to achieve multi-gigabit data rate, while modulators using carrier injection are somewhat slower because of the longer carrier lifetime.

Alternatively, the differential optical signals can be generated by using quantum well modulators [152-155] as shown in Figure 9-6. Light signals are absorbed by a quantum well

modulator when the wavelength of the light signals is within the absorption edge of such a device. The absorption edge of the modulator is shifted when a voltage is applied to this device. The modulation of the light signals can therefore be achieved by choosing the signal wavelength close to the absorption edge of the modulator and applying the voltage that corresponds to the modulation data across the device to achieve the modulation. In order to generate differential signals, two such devices are connected in series and driven by the modulation voltage simultaneously. The other terminals of these two modulators are connected to V_{dd} and V_{ss}. For a given modulation voltage (which could be either V_{dd} or V_{ss}), it will turn on the absorption of one of the modulator

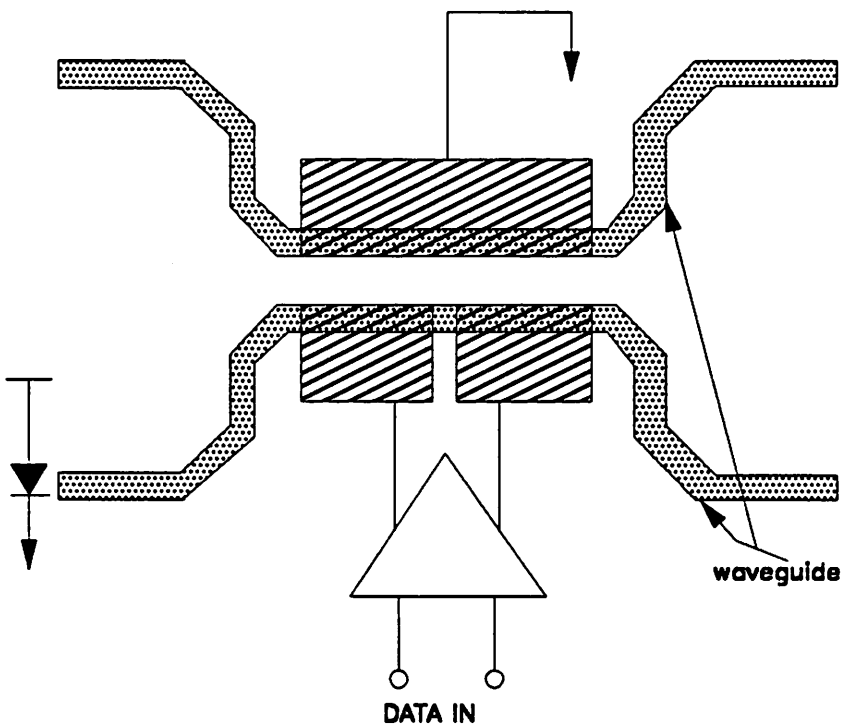

Figure 9-4. Structure of a directional coupler modulator.

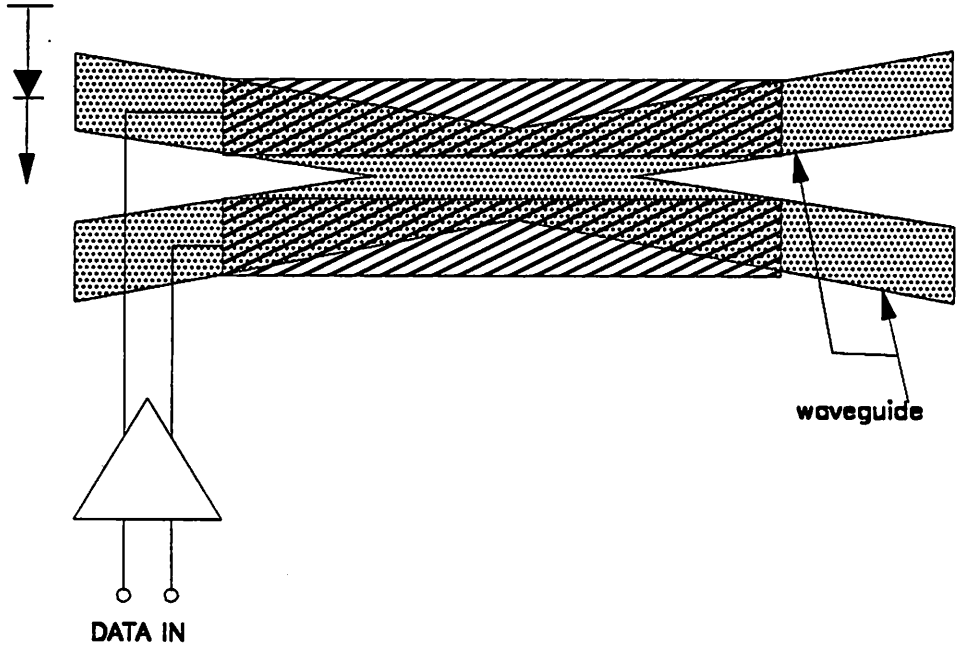

Figure 9-5. Structure of a modulator using total internal reflection.

and turn off the absorption of the other one. The input light will thus be reflected if the absorption is off and will be absorbed if the absorption is on, resulting in differential light signals.

9.3.2 *Time Division Multiplexing Technique*

It is possible to transmit both noninverted and inverted data over the same channel by using time division multiplexing to reduce the total number of interconnects. Each bit interval in a time division multiplexed system is divided into two *minibits* so that the noninverted bit is transmitted in the first minibit while the inverted bit is transmitted in the second minibit. Therefore a bit sequence 10 is transmitted for each logical ONE while a bit sequence 01 is transmitted for each logical ZERO. This is the same as Manchester encoding.

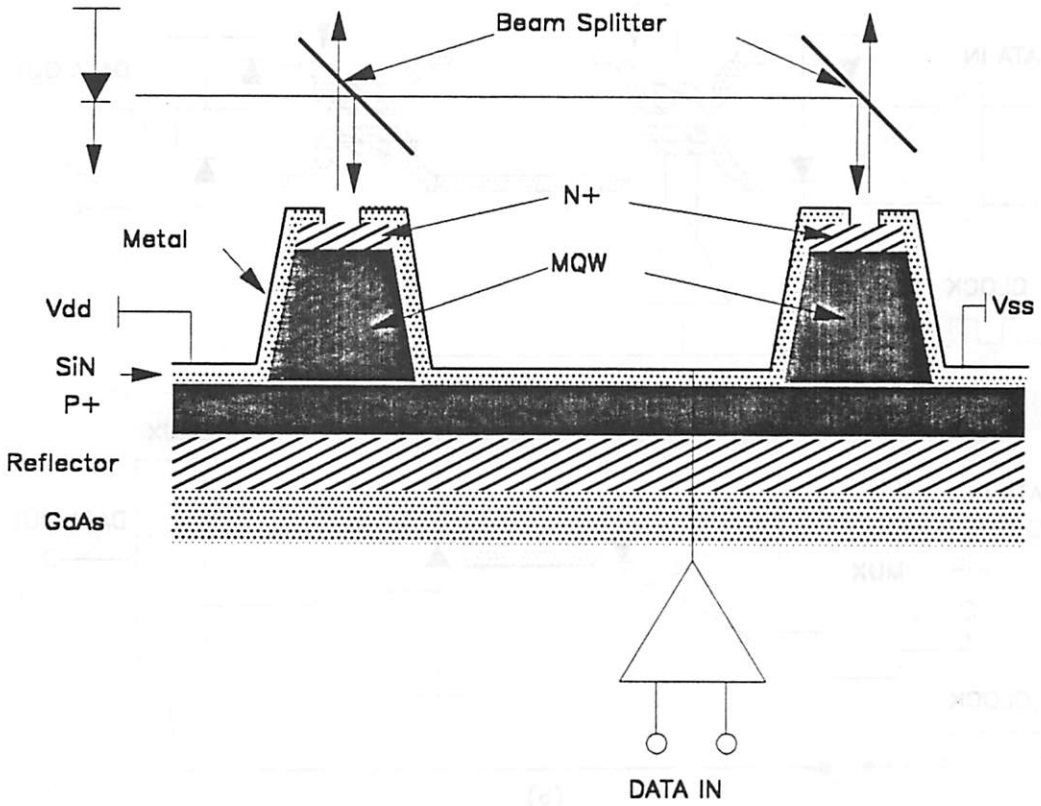

Figure 9-6. Structure of a multiple quantum well modulator.

An optical interconnect system using a time division multiplexing technique to transmit complementary data is shown in Figure 9-7. This time division multiplexing operation can occur in the optical domain or in the electrical domain. When time division multiplexing is achieved in the optical domain, as shown in Figure 9-7(a), a directional coupler driven by the channel clock is used to control the multiplexing and demultiplexing operation. In this system, the demultiplexed output signals have the return-to-zero (RZ) format. On the other hand, the data can be multiplexed and demultiplexed in the electronic domain, as shown in (b) of Figure 9-7. But multiplexing and demultiplexing in the electronic domain requires the driver and receiver to operate twice as fast as multiplexing and demultiplexing in the optical domain.

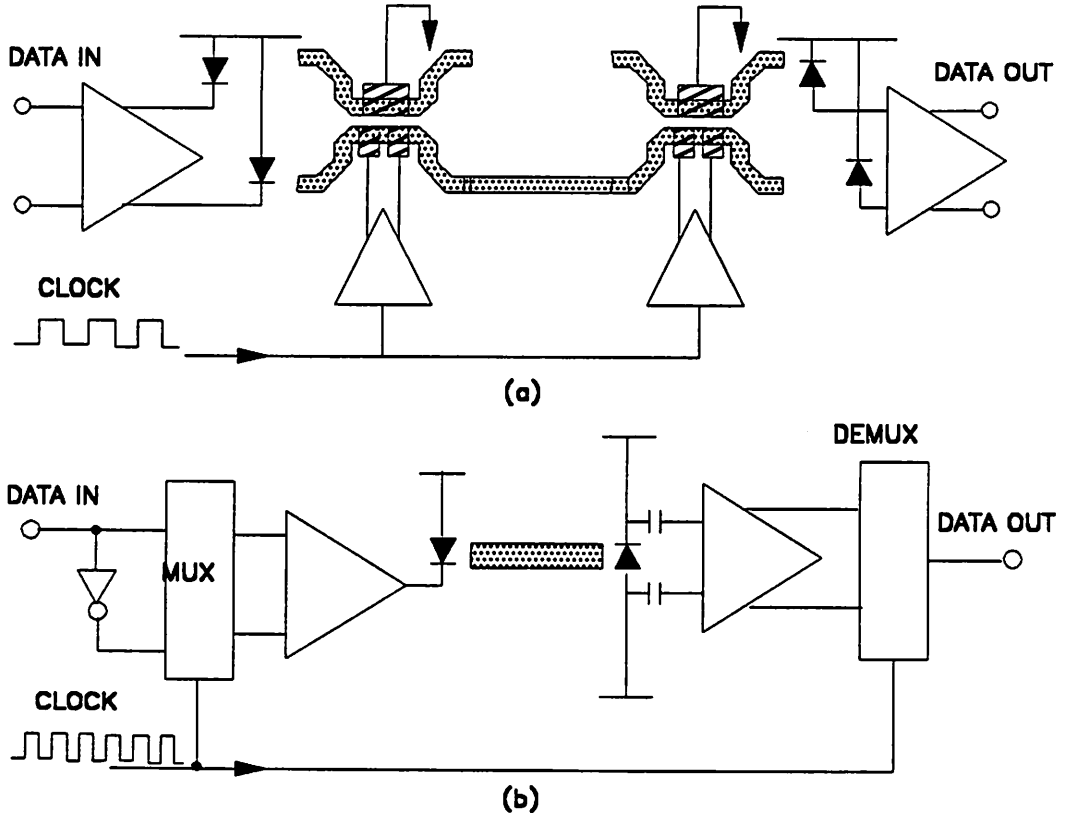

Figure 9-7. Structure of a differential optical interconnect using TDM. (a) Differential channels are multiplexed in the optical domain. (b) Differential channels are multiplexed in the electrical domain.

9.3.3 *Frequency Division Multiplexing Technique*

The laser's emission frequency (wavelength) is modified at different levels of current injection due to *adiabatic chirp* as discussed in Chapter 6. An optical interconnect system using FSK modulation, as shown in Figure 9-8, can be implemented by biasing the laser well above lasing threshold and modulating the laser with a small current. At the receiver side, the light is split into two filters via a splitter (or a grating demultiplexer) with one filter positioning at the center frequency of ONE while the other one positioning at the center frequency of ZERO. The output light signals from the filter is sent to a differential receiver. This structure uses the same total number of waveguides and lasers as that of a single-ended optical interconnect at the expense of requiring a more complicated receiver structure (requiring two filters and single-mode lasers).

9.3.4 *Wavelength Division Multiplexing*

The number of interconnecting fibers or waveguides can also be reduced by using wavelength-division multiplexing (WDM). Differential signals are sent at different wavelengths through the same waveguide or fiber, as shown in Figure 9-9. For single-wavelength LD/LEDs and PIN/APDs, fiber or waveguide combiners and splitters can be used to multiplex and demultiplex optical signals. A moderate wavelength selectivity is required since only two wavelengths need to coexist within the same interconnect. There has been a successful demonstration [162] of a monolithically integrated detector chip which includes a Bragg grating wavelength demultiplexer and PIN photodetectors. It is also possible to fabricate dual-wavelength devices so that two wavelengths can be coupled in and out of the fiber and waveguide without having to use waveguide

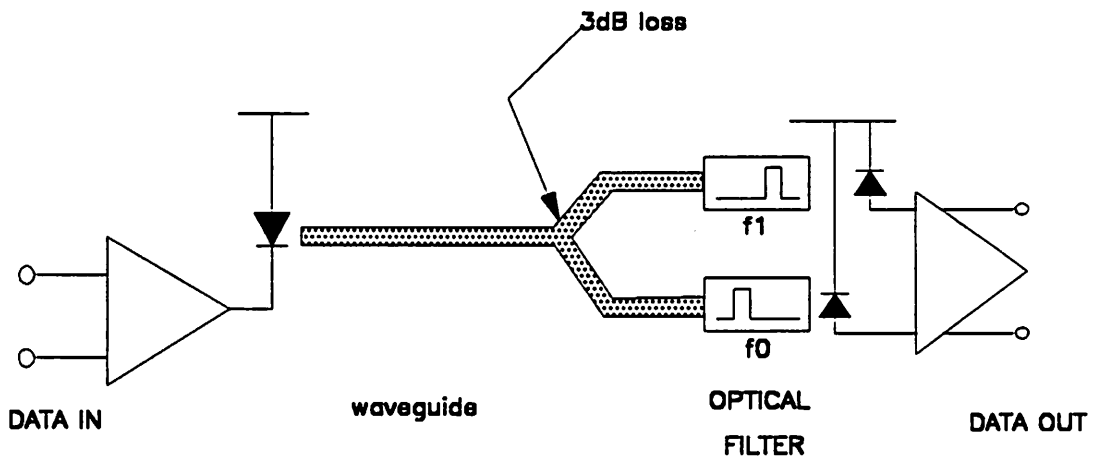

Figure 9-8. Structure of a differential optical interconnect using FSK.

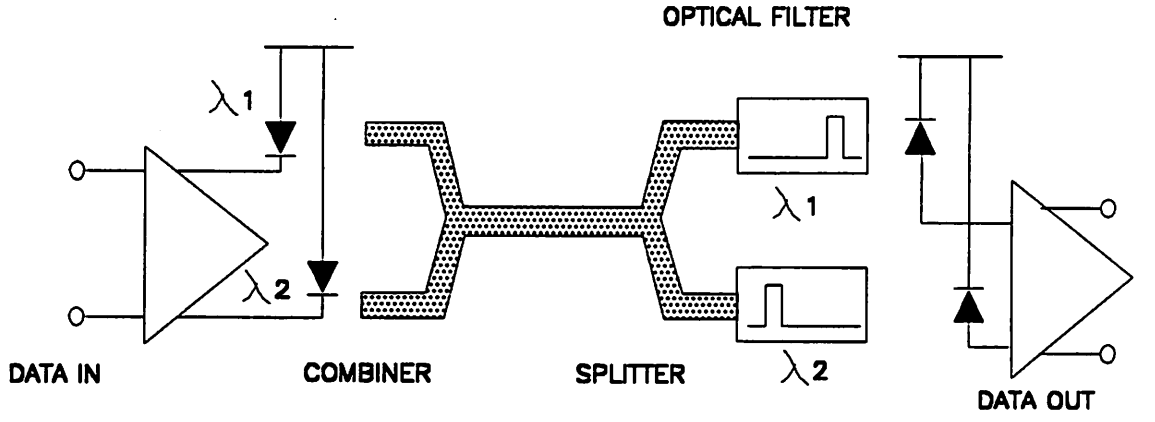

Figure 9-9. Structure of a differential optical interconnect using WDM.

combiners/splitters. There already exist dual-wavelength LEDs, LD's [163-166], as well as dual-wavelength PINs [167, 168] that can serve this purpose.

If the wavelengths used by the differential signals are too close, it might be difficult to fabricate fused PIN's that can distinguish two wavelengths. A small overlap in the responsivity vs. wavelength of a fused dual-wavelength PIN is not necessarily harmful since common-mode response can be suppressed by the differential receiver.

9.3.5 *Polarization Division Multiplexing Technique*

The differential optical signals can also be multiplexed in the same waveguide/fiber by using different polarizations (TE and TM). A system using this technique is shown in Figure 9-10. A

polarization modulator [158] is used at the source to modulate the incoming single-polarization light (TE or TM) so that the polarization state of the light is toggled (TE→TM/TM→TE) when the modulating voltage is in the ON state. At the receiving end of the interconnect, there is a polarization splitter so that TE signals come out from the bottom waveguide while TM signals come out from the top waveguide. The outputs from the polarization splitter are then applied to a differential receiver. This architecture requires a polarization maintaining waveguide or fiber and usually needs large modulation voltage.

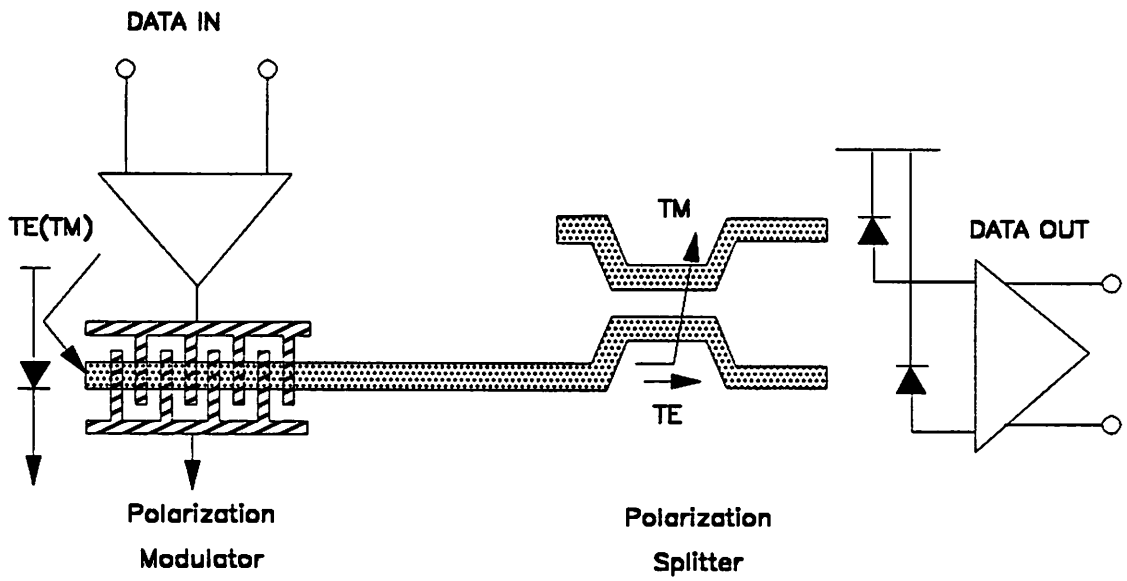

Figure 9-10. Structure of a differential optical interconnect using polarization division multiplexing.

9.4 Receiver Sensitivity Analysis

In this section, we analyze the SNR of a differential optical interconnect with the architecture shown in Figure 9-2. These results are then compared with those of a single-ended interconnect with both driver and receiver differentially configured (Figure 9-1(d)). In the following analysis, we assumed the optical power of ONE's and ZERO's are, respectively,

$$P_1 = \frac{2r}{1+r} P_{av}$$
$$P_0 = \frac{2}{1+r} P_{av} \tag{9.1}$$

where r is the extinction ratio of the optical signal and is defined as P_1/P_0, while P_{av} is the average optical power of the signal.

9.4.1 Single-ended optical interconnect

We assume a transimpedance amplifier [169] is used throughout this section. A schematic diagram which shows a single-ended configuration with an AC-coupled differential receiver is shown in Figure 9-11. Its half circuit is shown in Figure 9-12. Similar to the analysis in [169], we can determine the receiver output signal and noise voltage V_{out} and V_N, respectively. Assuming a DC-balanced state has been reached, the coupling capacitor shifts the differential current swing from $\left(2\frac{\eta MeP_0}{h\nu}, 2\frac{\eta MeP_1}{h\nu}\right)$ to $\left(\frac{\eta Me}{h\nu}(P_0 - P_1), \frac{\eta Me}{h\nu}(P_1 - P_0)\right)$, where M is the avalanche photodiode gain (equal to unity for PIN diode), η is the quantum efficiency of the photodetector, h is the Planck's constant, ν is the optical frequency of the light signals, and e is the electron charge.[26] We first define

$$C = C_d + C_i$$
$$\frac{1}{R} = \frac{1}{R_b} + \frac{1}{R_i} \tag{9.2}$$

[26] The factor 2 in the expression is due to the same amount of photocurrent flowing into one of the input terminals of a differential preamplifier flows out of the other input terminal, resulting in the total differential to be twice as large as the photocurrent generated at the photodetector.

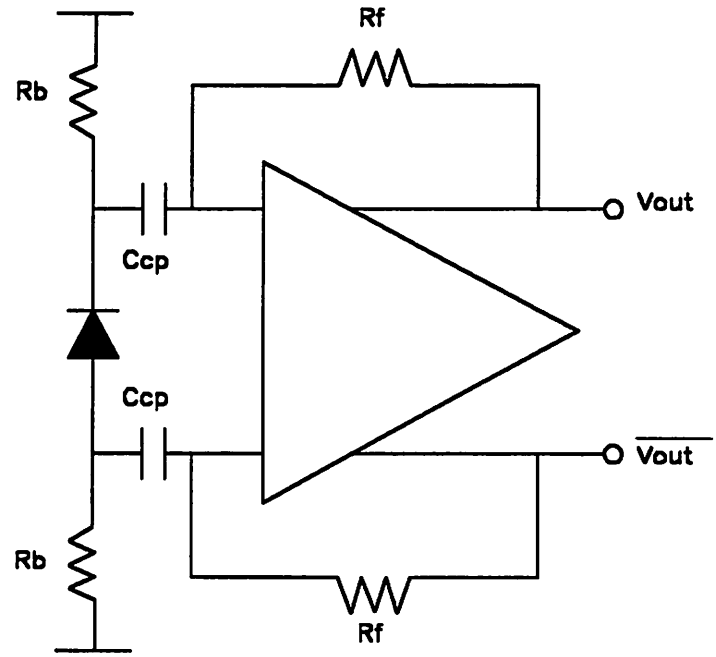

Figure 9-11. Full circuit of a differential receiver using in a single-ended optical interconnect.

where C_d and C_i are the detector and receiver input capacitance, respectively, while R_b and R_i are the corresponding biasing and receiver input resistance. We further define $1/Z = 1/R + j\omega C$, or equivalently $Z = R/(1 + j\omega RC)$. Using the half circuit shown in Figure 9-12, we can find that

$$\frac{v_{in}}{Z} + \frac{v_{in} - v_{out}}{R_f} = MI \tag{9.3}$$

where v_{in} is the input voltage to the amplifier denoted by $-A$, where A is the amplifier voltage gain. Since $v_{out} = -Av_{in}$, we can thus conclude

$$v_{out} = -\frac{MI}{\frac{1}{R_F} + \frac{1}{AR_F} + \frac{1}{AZ}} \quad . \tag{9.4}$$

For $A \gg 1$, the above equation reduces to $v_{out} = -MIR_F$. In other words, the output voltage is

$$V_{\{1,0\}} = \pm 2M \frac{\eta e}{h\nu} \frac{r-1}{r+1} P_{av} R_F \tag{9.5}$$

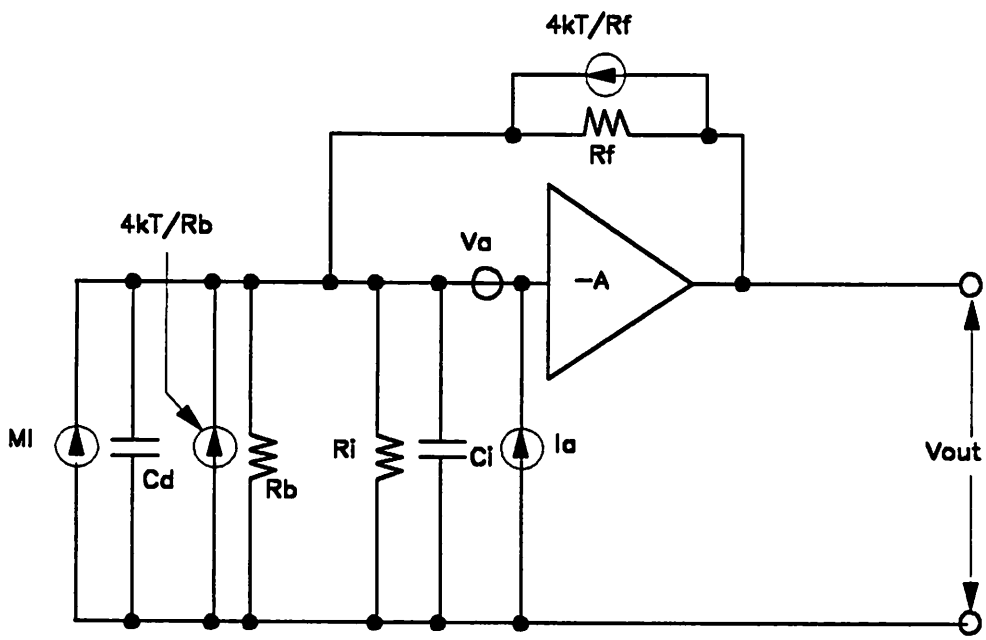

Figure 9-12. Half circuit of a differential receiver using in a single-ended optical interconnect.

where the sign in this equation depends on the data transmitted. Positive and negative signs correspond to logical ONE and ZERO, respectively.

There are a total of five noise sources: (1) Shot noise ($2eM^2FI$) where F is the excess noise factor of the avalanche diode, (2) Thermal noise contributed by the biasing resistor ($4kT/R_b$), (3) Thermal noise contributed by the feedback resistor ($4kT/R_F$), (4) Amplifier voltage noise (V_A^2), (5) Amplifier current noise (I_A^2).

To evaluate the contribution by the shot noise, amplifier current noise, and the feedback resistor noise, we can follow the same procedures as those in evaluating the output signal voltage. The output voltage noise spectral density due to these three sources is thus $(2eM^2FI + 4kT/R_b + I_A^2)R_F^2$. In order to find the noise contributed by the amplifier voltage noise, we equate the current at the input node of the feedback resistor,

$$\frac{V_A}{Z} = \frac{v_{out} - V_A}{R_F} \tag{9.6}$$

assuming a *virtual short circuit* condition at the input to the amplifier.[27] Therefore,

$$\begin{aligned} v_{out,V} &= (1 + \frac{R_F}{Z})V_A \\ &= [(1 + \frac{R_F}{R}) + j2\pi f R_F C]V_A \end{aligned} \tag{9.7}$$

and the spectral density equals

$$v_{out,V}^2 = [(1 + \frac{R_F}{R})^2 + 4\pi^2 f^2 R_F^2 C^2]V_A^2 \quad . \tag{9.8}$$

---

[27] A virtual short circuit condition usually exists when the input impedance of an amplifier is infinite. Under this situation, input current to the amplifier is almost zero and the voltage difference between two input terminals is therefore identical to zero.

In order to find the contribution of the thermal noise of the feedback resistance to the output noise, we equate the current flowing into the input node to the amplifier:

$$\frac{v_{in}}{Z}+\frac{v_{in}-v_{out,R}}{R_F}=I_R \quad . \tag{9.9}$$

Since $v_{in}=-v_{out,R}/A$, the above equation reduces to

$$v_{out,R}=\frac{I_R}{\frac{1}{R_F}+\frac{1}{A}(\frac{1}{R_F}+\frac{1}{Z})} \quad . \tag{9.10}$$

Assuming $A \gg 1$, the output noise spectral density due to feedback resistor thus equals

$$\begin{aligned} v_{out,R}^2 &= \frac{4kT}{R_F} R_F^{\,2} \\ &= 4kTR_F \end{aligned} \quad . \tag{9.11}$$

By summing each individual noise component, the total noise spectral density is

$$V_N^2(f)=[(1+\frac{R_F}{R})^2+4\pi^2 f^2 R_F^2 C^2]V_A^2+4kTR_F+(2eM^2FI+\frac{4kT}{R_b}+I_A^2)R_F^2 \tag{9.12}$$

and the total noise power can be obtained by integrating the above equation over the interval $f \in [0, B]$, assuming frequency independent contributions from I_A^2 and V_A^2:

$$V_N^2=\left\{[(1+\frac{R_F}{R})^2+\frac{4\pi^2}{3}B^2R_F^2C^2]V_A^2+4kTR_F+(2eM^2FI+\frac{4kT}{R_b}+I_A^2)R_F^2\right\}B \tag{9.13}$$

where B is the noise equivalent bandwidth of the receiver. Except for shot noise, the noise sources of the two half circuits are independently generated and can be added incoherently. The shot noise sources to both half circuits are identical and correlated so the total shot noise power is four times rather than twice the shot noise power in a half circuit. The total noise power of this configuration thus equals

$$\begin{aligned} V_{\{N,1\}}^2 &= 2\left[\overline{V_A^2}((1+\frac{R_F}{R^2})^2 + \frac{4\pi^2}{3}B^2C^2R_F^2) + R_F^2(4eM^2FI_1 + \frac{4kT}{R_b} + \overline{I_A^2}) + 4kTR_F\right]B, \\ V_{\{N,0\}}^2 &= 2\left[\overline{V_A^2}((1+\frac{R_F}{R^2})^2 + \frac{4\pi^2}{3}B^2C^2R_F^2) + R_F^2(4eM^2FI_0 + \frac{4kT}{R_b} + \overline{I_A^2}) + 4kTR_F\right]B \end{aligned} \tag{9.14}$$

where

$$\begin{aligned} I_1 &= \frac{\eta Me}{h\nu}P_1, \\ I_0 &= \frac{\eta Me}{h\nu}P_0. \end{aligned} \tag{9.15}$$

Note that the noise power is different for logical signal ONE and ZERO due to different shot noise contribution for logical ONE's and ZERO's. The above analysis ignores the noise contribution from the postamplifier stages. This analysis has ignored noise contributions from the postamplifier gain stages. However, if the transimpedance of the preamplifier is sufficiently large, the equivalent output noise sources due to subsequent gain stages would be negligible and the results obtained here can still serve as a first-order approximation of this receiver configuration.

9.4.2 Differential Optical Interconnect

A schematic diagram of a differential interconnect using a DC-coupled differential receiver is shown in Figure 9-13. Its half circuit is shown in Figure 9-14. Using a similar strategy described in the previous subsection, we can determine the receiver output signal and noise voltage. The equivalent input signal current equals the difference between the current carried by each channel. The output voltage of the signal thus equals

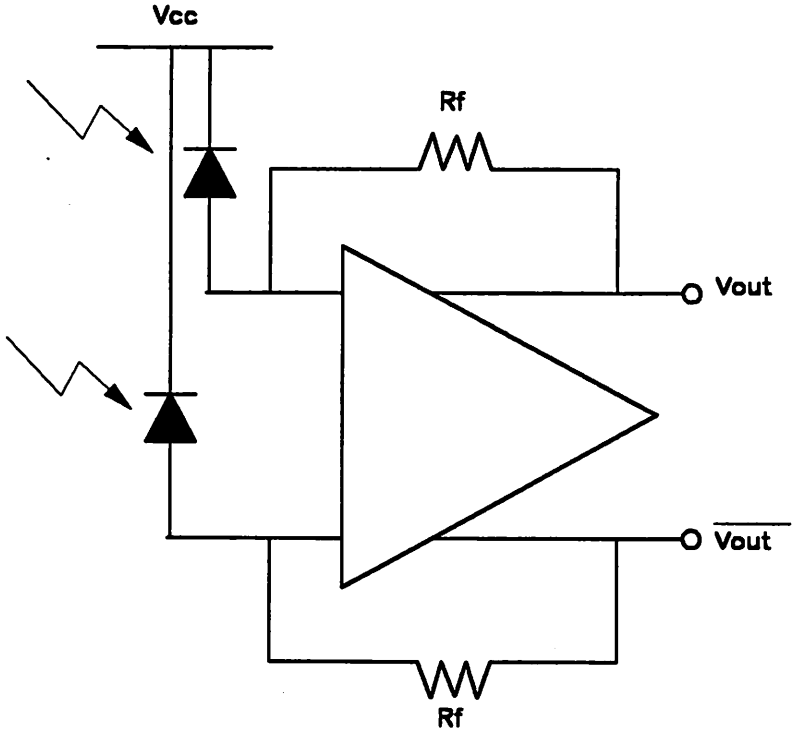

Figure 9-13. Full circuit of a differential receiver used in a differential optical interconnect.

$$V_1 = M\frac{\eta e(P_1 - P_0)}{h\nu} R_F \ ,$$
$$V_0 = M\frac{\eta e(P_0 - P_1)}{h\nu} R_F \ , \tag{9.16}$$

or equivalently,

$$V_{\{1,0\}} = \pm 2M\frac{\eta e}{h\nu}\frac{r-1}{r+1} P_{av} R_F \ , \tag{9.17}$$

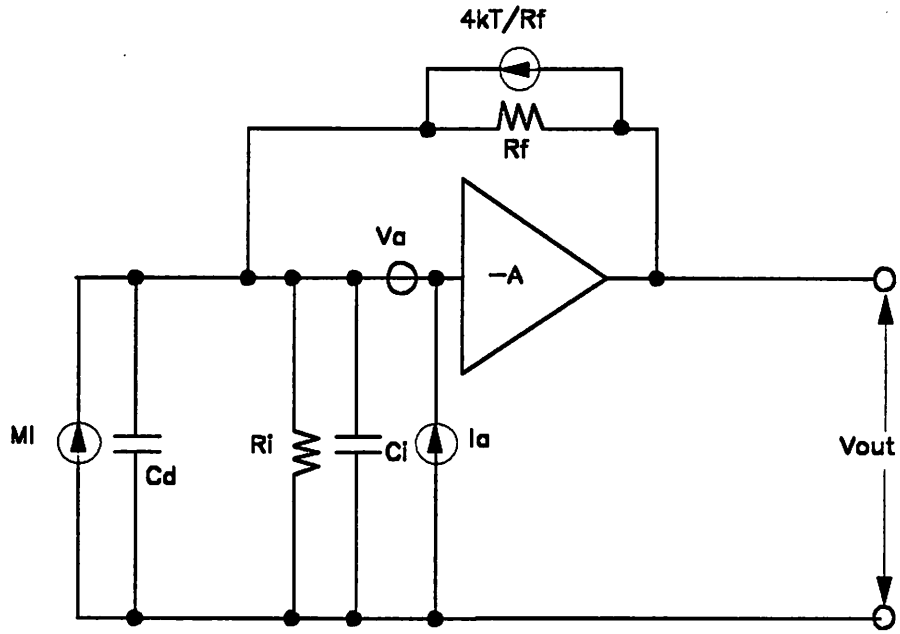

Figure 9-14. Half circuit of a differential receiver used in a differential optical interconnect.

where the plus and minus sign corresponds to receiving a logical ONE and ZERO, respectively. The total noise power of this configuration is

$$V^2_{\{N,1\}\{N,0\}} = 2\left[\overline{V_A^2}\left((1+\frac{R_F}{R_l^2})^2 + \frac{4\pi^2}{3}B^2C^2R_F^2\right) + R_F^2(2eM^2FI + \overline{I_A^2}) + 4kTR_F\right]B \qquad (9.18)$$

where $I = \eta eP_{av}/h\nu$. Note that the noise component contributed by the biasing resistor R_b is no longer present and the total noise power for logical ONE's and ZERO's are the same and inter-

mediate between those of the ZERO's and ONE's for the single-ended interconnect case analyzed in the previous subsection.[28]

From above derivations, we conclude that a fully differential optical interconnect system receives the same signal power as compared to a single-ended interconnect system, assuming $A \gg 1$. However, the shot noise for the receiver in a single-ended interconnect system is two times as compared to that in a fully differential interconnect system when transmitting a logical ONE. For thermal noise dominated operations, a fully differential optical interconnect therefore performs slightly better than a single-ended optical interconnect with similar driver and receiver structure.

9.5 System Degradation Due to Channel Mismatch

In practice, the differential gain of LD/LED's, the attenuation through the fibers/waveguides, the responsivity of the photodetector can be different between differential channels. Furthermore, process related offset voltages in the circuitry of the laser driver, preamplifier, and postamplifier introduce additional imbalance between differential channels. In the worst case, the imbalance between differential channels can drive the preamplifier or postamplifier into clamping and the channel will fail. Even if the outright failure does not occur, the waveform at the output of the receiver might be severely distorted as clamping is approached and thus degrade the system performance. However, it is likely that the offset voltage problem can be reduced significantly in the future as technologies such as silicon bipolar or GaAs on silicon become more mature. In this section, the effect of parameter mismatch on the system performance is analyzed.[29]

9.5.1 Threshold Offset

---

[28] The total shot noise is constant in this configuration. At any given time, one photodetector is receiving a ONE and the other photodetector is receiving a ZERO, the total shot noise $2eI_1 + 2eI_0$ is therefore constant.

[29] In addition to the DC mismatches discussed here, there are several AC mismatch sources which could occur in a differential optical interconnect and degrade the channel performance. These mismatch sources include mechanical vibration, thermal gradient of the laser, and the laser coherence time. The first one is not likely to be a serious problem for a differential optical interconnect since this type of noise can be cancelled at the receiver due to its large common-mode component. Small thermal gradient exists between adjacent lasers when the transmitted data is not DC-balanced. However, the thermal gradient of a laser array is much reduced when it is operated in a differential mode because of the spatially balanced nature of a differential optical interconnect array. Modal noise due to the mismatch of laser coherence in a differential optical interconnect will be twice as much as in a single-ended interconnect when lasers with large coherence time are used with multi-mode waveguides. However, this problem can be overcome by using self-pulsating lasers or by premodulating the lasers at a frequency comparable to their relaxation oscillation frequency.

The input signals to the positive and the negative terminals of the receiver, respectively, are

$$\begin{aligned} i_{in,+} &= R_+ A_+ \eta_{diff,+} I_+ \\ i_{in,-} &= R_- A_- \eta_{diff,-} I_- \end{aligned} \tag{9.19}$$

where R is the responsivity of the PIN/APD, A is the attenuation either due to propagation or due to fan-out, and η_{diff} is the differential quantum efficiency[30] of an LD/LED. I_+ and I_- are the output currents of the laser driver. Defining

$$\begin{aligned} R &= \frac{R_+ + R_-}{2} \\ \Delta R &= R_+ - R_- \end{aligned} \tag{9.20}$$

$$\begin{aligned} A &= \frac{A_+ + A_-}{2} \\ \Delta A &= A_+ - A_- \end{aligned} \tag{9.21}$$

$$\begin{aligned} \eta_{diff} &= \frac{\eta_{diff,+} + \eta_{diff,-}}{2} \\ \Delta \eta_{diff} &= \eta_{diff,+} - \eta_{diff,-} \cdot \end{aligned} \tag{9.22}$$

Therefore,

[30] Unfortunately, the symbols used here conflict with the symbols used earlier in this chapter. But we keep these symbols in order to be consistent with the conventions used in the literature. The meaning of this symbols will be clarified if they are not clear from the context.

$$
\begin{aligned}
i_{in,+} &= (R + \frac{\Delta R}{2})(A + \frac{\Delta A}{2})(\eta_{diff} + \frac{\Delta \eta_{diff}}{2})I_+ \\
&= RA\eta_{diff}(1 + \frac{\Delta R}{2R})(1 + \frac{\Delta A}{2A})(1 + \frac{\Delta \eta_{diff}}{2\eta_{diff}})I_+ \\
i_{in,-} &= (R - \frac{\Delta R}{2})(A - \frac{\Delta A}{2})(\eta_{diff} - \frac{\Delta \eta_{diff}}{2})I_- \\
&= RA\eta_{diff}(1 - \frac{\Delta R}{2R})(1 - \frac{\Delta A}{2A})(1 - \frac{\Delta \eta_{diff}}{2\eta_{diff}})I_- \ .
\end{aligned}
\tag{9.23}
$$

Assuming the mismatches are small, the above equation can be approximated by

$$
\begin{aligned}
i_{in,+} &= RA\eta_{diff}(1 + \frac{\Delta R}{2R} + \frac{\Delta A}{2A} + \frac{\Delta \eta_{diff}}{2\eta_{diff}})I_+ \\
i_{in,-} &= RA\eta_{diff}(1 - \frac{\Delta R}{2R} - \frac{\Delta A}{2A} - \frac{\Delta \eta_{diff}}{2\eta_{diff}})I_-
\end{aligned}
\tag{9.24}
$$

Defining a parameter *total channel mismatch*

$$
\Delta M = \frac{\Delta R}{R} + \frac{\Delta A}{A} + \frac{\Delta \eta_{diff}}{\eta_{diff}} \tag{9.25}
$$

as well as the differential mode and the common-mode of the LD/LED driver current

$$
\begin{aligned}
I &= \frac{I_+ + I_-}{2} \\
\Delta I &= I_+ - I_- \ .
\end{aligned}
\tag{9.26}
$$

The differential-mode of the input current to the receiver amplifier then equals

$$
\begin{aligned}
i_{diff} &= i_{in,+} - i_{in,-} \\
&= RA\eta_{diff}\Delta I + RA\eta_{diff}\Delta M I
\end{aligned}
\tag{9.27}
$$

and the common-mode of the input current to the receiver amplifier is

$$\begin{aligned} i_{common} &= \frac{i_{in,+} + i_{in,-}}{2} \\ &= RA\eta_{diff}I + \frac{1}{2}RA\eta_{diff}M\Delta I \quad . \end{aligned} \tag{9.28}$$

Assuming there is no mismatch within the receiver, the differential output is therefore equal to

$$\begin{aligned} v_{out,diff} &= R_{dm}(RA\eta_{diff}\Delta I + RA\eta_{diff}\Delta MI) \\ &= R_{dm}RA\eta_{diff}\Delta I + R_{dm}RA\eta_{diff}\Delta MI \end{aligned} \tag{9.29}$$

where R_{dm} is the transimpedance of the receiver.

Since I is a constant, the total voltage swing of the received signal is

$$\Delta V_{out,diff} = R_{dm}RA\eta_{diff}\Delta I \tag{9.30}$$

and a DC offset from the threshold at zero by an amount

$$TH_{offset} = R_{dm}RA\eta_{diff}\Delta MI \quad . \tag{9.31}$$

or

$$\frac{TH_{offset}}{\Delta V_{out,diff}} = \Delta M \frac{I}{\Delta I} \tag{9.32}$$

If the laser has a zero threshold, then $\Delta I = 2I$ and the fractional threshold change is equal to one half of the total channel mismatch. As the threshold (I_0) of the laser increases, the fractional

threshold change increases for the same amount of total channel mismatch. The fractional threshold change equals the total channel mismatch when $I_1 = 3I_0$.

From this analysis, we can argue that a low-threshold laser is desirable in a fully differential optical interconnect to minimize the threshold offset due to channel mismatch. Furthermore, *at least* one half of the total channel mismatch will be reflected in the threshold offset even if lasers with zero threshold current are used.

Since it is not possible to adjust the threshold of the circuit individually, this offset either has to be compensated by circuit techniques or be absorbed by the noise tolerance of the logic.

9.5.2 System Penalty

Assuming the probability of transmitting ONE's and ZERO's are equally likely, the error probability of a differential optical interconnect system is

$$P_e = \frac{1}{4}\,\mathrm{erfc}\left(\frac{V_1 - V_{th}}{\sqrt{2}\,\sigma_{N,1}}\right) + \frac{1}{4}\,\mathrm{erfc}\left(\frac{V_{th} - V_0}{\sqrt{2}\,\sigma_{N,0}}\right) \tag{9.33}$$

where V_{th} is the threshold voltage and V_1, V_0, $\sigma_{N,1}$, and $\sigma_{N,0}$ have been derived in the previous section. The optimal threshold $V_{th,opt}$ is the solution to $\partial P_e / \partial V_{th} = 0$.

When the actual threshold is not the optimal threshold, more optical power is required to maintain the same bit-error-rate and thus incurs power penalty. With the threshold error defined as $(V_{th} - V_{th,opt})/\Delta V_{out,diff}$, the power penalty as a function of threshold error is plotted in Figure 9-15. From this figure, we can see that a 20% threshold error incurs 2.2dB power penalty. If the laser is operated with infinite extinction ratio (i.e. $\Delta I = 2I$), a total channel mismatch of 40% can be tolerated, assuming a 2.2dB power penalty criterion. Note that this analysis assumes the interconnect is operated in its linear region, thus these results are no longer applicable if any of the components are driven into saturation or clamping and become nonlinear.

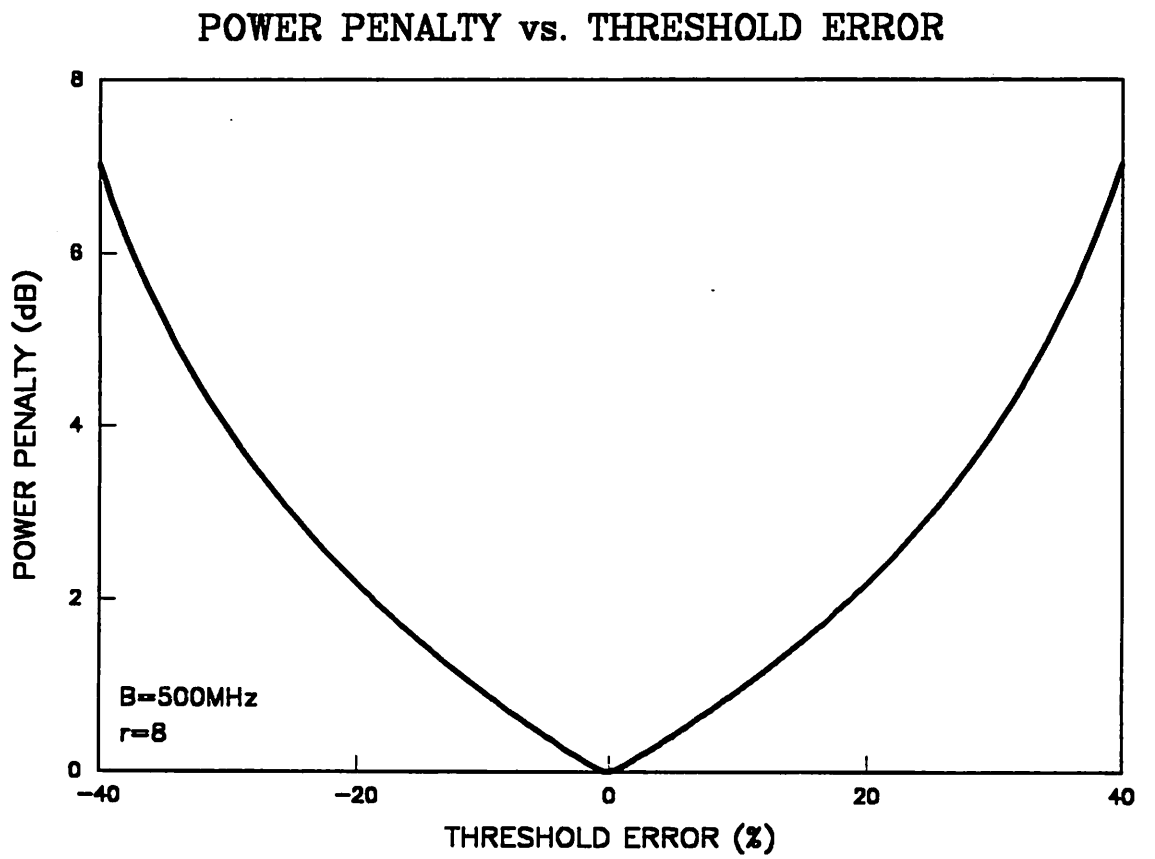

Figure 9-15. Power penalty as a function of threshold error. Extinction ratio r is 8 and electrical bandwidth of the receiver B is 500MHz.

9.6 Mismatch Cancellation Techniques

As we have shown in the previous section, the mismatch between differential channels causes an offset of the optimum decision threshold and degrades the system performance. Some mismatch cancellation is therefore necessary when a system requires high sensitivity and cannot tolerate any sensitivity loss due to channel mismatch. In this section, several channel mismatch cancellation techniques are proposed and evaluated. Some of these mismatch cancellation techniques are similar to an AGC system and require either a DC-balanced data stream or a special transmission protocol.

9.6.1 Periodic Null Insertion

The actual threshold at the output of a differential receiver can be obtained by periodically

- Turning on both of the laser diodes of a differential channel,
- Sampling the output voltage of the receiver,
- Storing the result in a capacitor.

A special synchronization circuitry between the transmitter and the receiver is required in this case in order to coordinate the threshold sampling process. The threshold sampling frequency of this scheme is determined by the time constant of the capacitor, which is usually on the order of KHz. The bandwidth loss due to threshold sampling is therefore insignificant for gigabit data rate. This technique has been used for offset cancellation in some operational amplifiers based on switched capacitor principles.

9.6.2 *Average Computation*

Alternatively, the average of the differential output signals can be continuously sampled and stored. However, this technique will be effective only if the data stream is DC balanced. This circuitry will be functionally equivalent to an AGC circuit used in most of the single-ended optical interconnect.

9.6.3 *Decision Feedback Average Computation*

The drawback of the previous technique is the requirement of a DC-balanced data stream in order to calculate the average of the threshold. This problem can be overcome by a decision feedback mechanism, as shown in Figure 9-16 [170]. In this decision feedback mechanism, the output differential voltage are routed to two separate capacitors depending on the output logic values. The voltage difference are then computed by a differential amplifier to generate the optimal threshold.

9.7 Summary

In this chapter, we presented and analyzed a differential optical interconnect architecture. This interconnect technique provides a symmetric channel for transmitting optical signals. It relaxes the system and circuit constraints posed by the traditional interconnect architecture, namely, the dependency of the absolute magnitude of decision threshold and the vulnerability to the power supply and the ground noise.

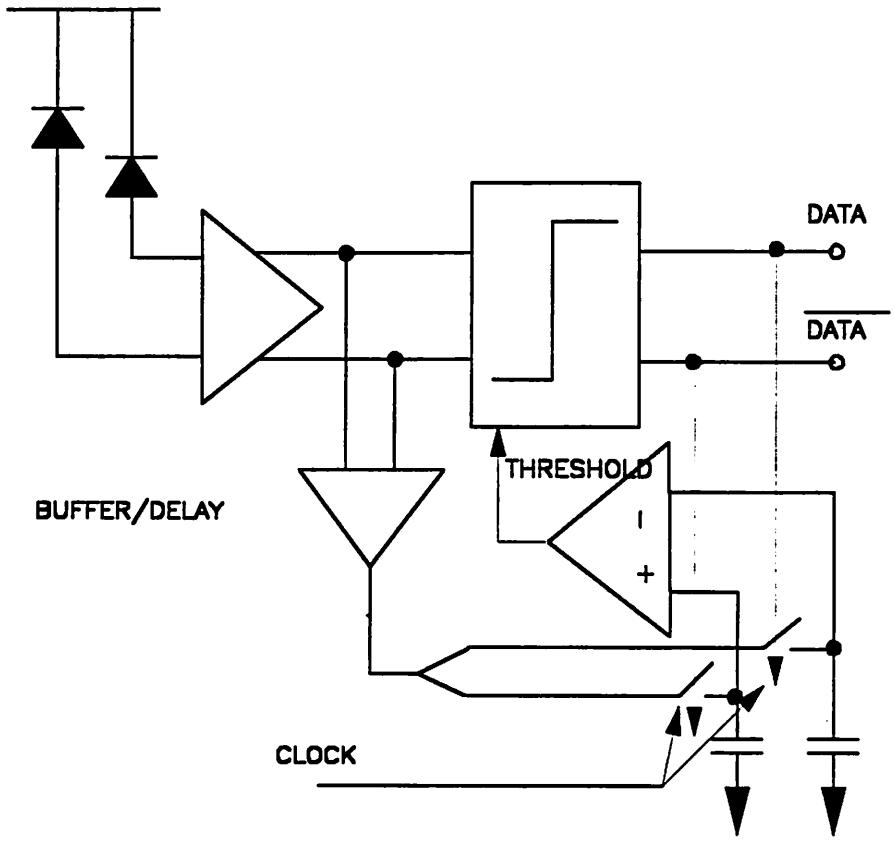

Figure 9-16. Structure of decision feedback optimal threshold computation.

There are various ways of implementing a differential optical interconnect without increasing the interconnect density. We have investigated combining differential channels in the time division, in the frequency division, in the wavelength division and in the polarization division. All of these techniques are realizable using today's technology. It also has interesting implications for possible future device structures suitable for this application.

We have shown in this chapter that the signal-to-noise performance of a differential optical interconnect is almost the same as a single-ended optical interconnect using differentially configured

laser drivers and receivers. Differential optical interconnect is slightly better due to the omission of the biasing resistors which reduces the thermal noise of the front-end.[31]

Though this architecture is less vulnerable to many types of noise, it is sensitive to channel mismatch. The mismatch between channels causes the cross-coupling among the common-mode and differential-mode signals of the previous stage and thus changes the optimum decision threshold. We showed that a total channel mismatch of 40% will cause a 20% of threshold offset, and a 2.2 dB power penalty. This is usually tolerable in most of the applications. When high sensitivity is required in some applications, it becomes necessary to use circuit techniques to reduce the system penalty created by this channel mismatch.

[31] In practice, thermal noise performance is not an essential criterion for deciding between single-ended or differential optical interconnect structure since these short distance interconnects are usually not operated in their sensitivity region.

CHAPTER 10 FULLY DIFFERENTIAL TRANSMITTER ARRAY

10.1 Introduction

A fully differential transmitter is one of the key components in a differential optical interconnect system. A fully differential transmitter consists of an electronic driver together with lasers and/or external modulators. It takes either single-ended or differential electrical signals and converts them into complementary light signals. In Chapter 9, a number of fully differential transmitter structures were examined. Among these configurations, driving two lasers with an electronic driver is most straightforward and will be further considered in this chapter. The principles for the laser driver design described in this chapter are, nevertheless, also applicable to the driver design for an external modulator.

There exists a fundamental difference between a laser and an external modulator[32] in terms of their external characteristics. A laser, usually modeled as a capacitor in parallel with a series resistor and an ideal diode, is a current device and presents very low input impedance ($\leq 5\Omega$) to the driver. On the other hand, a modulator, either modeled as a lumped capacitor (for low bandwidth applications) or as a traveling wave device (for high-bandwidth applications), is a voltage device and presents a very high input impedance ($\geq 1M\Omega$) to a driver. However, termination is usually required if the modulator is driven through a transmission line to prevent reflections. This could result in a large driver current (100 mA for a modulation voltage of 5V across a 50Ω termination resistor). Therefore, a driver capable of handling large driving current is necessary for driving either a laser diode or a traveling-wave type modulator.

Previously, there have been intensive studies on the laser driver design for single-ended fiber optical systems [114-116, 118-120]. In these designs, the driver usually consists of a waveshaping circuitry for reducing the laser chirp, a differential current switch, a biasing circuit, and a monitor circuit for detecting the peak and average of the feedback signals from a built-in photodiode in the transmitter to adjust the biasing current and the modulation current. The circuit structure of the

[32] The external modulators discusses here can be either a Mach-Zehnder modulator or a directional coupler, either on a *GaAs* or a $LiNbO_3$ substrate.

driver for a differential optical interconnect is similar to that for a single-ended optical interconnect, except a separate biasing circuit is necessary to bias the additional laser diode in a differential transmitter.

Due to the large modulation current required by some types of lasers ($I_{mod} > 20$ mA) or traveling-wave type modulator, significant switching noise is introduced in an array environment due to the sharing of a common power supply and ground. In this chapter, we show that a fully differential transmitter design has very little switching noise ($\leq$5% or -26 dB) in a dense array environment due to its balanced circuit configuration. Other features of this differential transmitter design include:

- Fully functional (verified by simulations) up to 2.5 Gbps,
- The maximum modulation current and bias current are both 40 mA.[33]
- On-chip 50Ω termination,
- Drive sink type laser array in which the laser array shares a common p-type substrate.

We also present a circuit design for driving source-type laser array in which the laser array shares a common n-type substrate.

The organization of this chapter is as follows: Section 2 describes the circuit design issues for the differential driver while the physical layout of a single differential driver is presented in Section 3. Simulation results are discussed in Section 4. This chapter is summarized in Section 5.

10.2 Circuit Design

The important parameters in designing a laser driver include

- The extinction ratio r which is defined as the ratio between P_{on} and P_{off},
- The bias current I_{bias},
- The modulation current.

[33] If the driver is used to drive a traveling wave modulator, this driving capability can be translated into a modulation voltage of 2V and a bias voltage of 2V.

Biasing the laser below threshold results in a substantial turn-on delay (~100ps) and turn-on jitter (~30ps) as well as strong relaxation oscillations. On the other hand, biasing the laser above threshold reduces the extinction ratio and the receiver sensitivity. Therefore, it is usually desirable to bias the laser slightly above its threshold to optimize the system performance.

The important parameters in designing a modulator driver are

- The modulation voltage, and/or
- The bias voltage which is necessary for some type of modulator.

The modulation voltage for a modulator using either electro-optic effect or carrier-induced index change is usually determined by the device. In the Mach-Zehnder modulator case, the modulation voltage is determined by the the voltage difference between the electrodes required to induce a π phase shift of the optical signals. If the modulation of the device is based on carrier-induced index change effect, a bias voltage is necessary to deplete the carriers.

The device characteristics of a laser diode, such as the differential quantum efficiency, η_{diff}, and the threshold current, I_{th}, changes from one laser to another and varies with the temperature. In a single laser driver design, separate control circuits for the modulation current and the threshold current are usually provided in order to maintain a constant extinction ratio. The control circuit is often combined with a monitor circuit which consists of a photodetector, a peak detection circuit and an average detection circuit for calculating the differential quantum efficiency as well as the threshold current. Very sophisticated circuits have been designed so that the driver can adapt to a wide variety of working environment and a wide range of parameters [120]. However, it is not possible to have separate monitoring and adaptation circuits for each channel in an array environment due to the packaging density requirements. Fortunately, the characteristics of individual elements in a laser array are usually close [108] so that there is no need for individual adjustment. Furthermore, the receiver has been built to accept a wide range of signals so that the stabilization of the light signal output at the transmitter is not critical.

A fully differential circuit for driving a sink type laser array is shown in Figure 10-1. This design contains separate external control circuits for adjusting the biasing current and the modu-

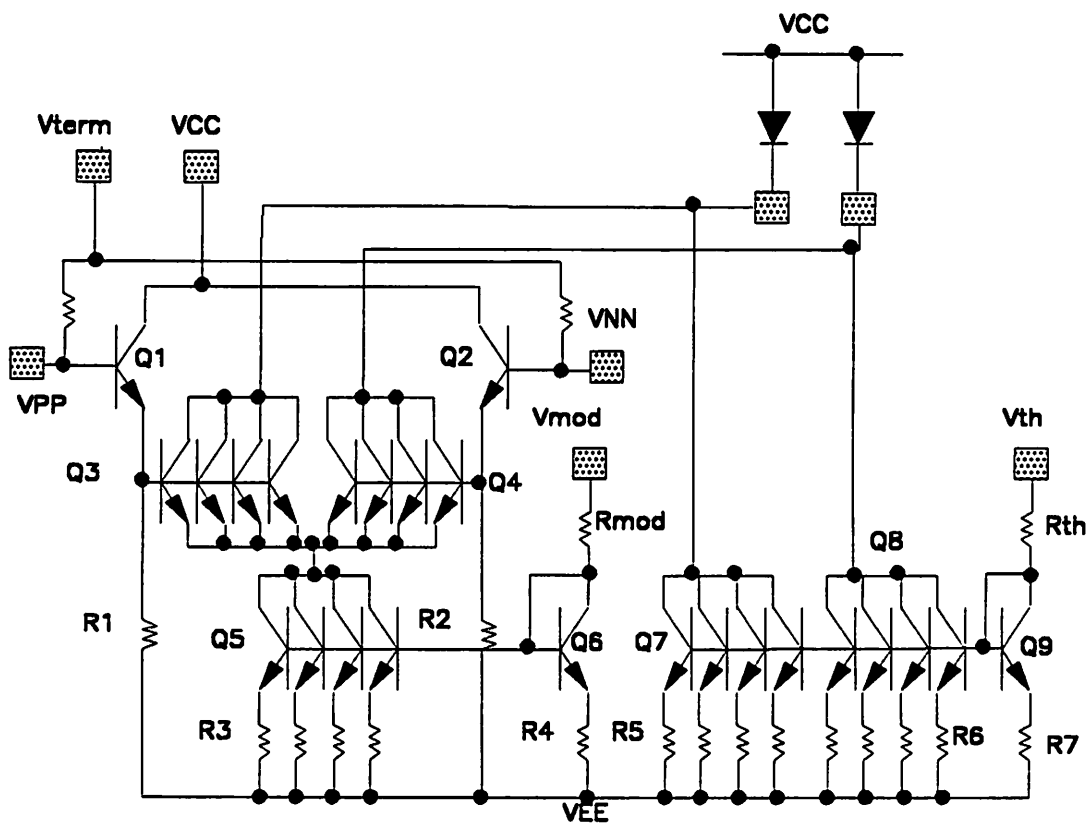

Figure 10-1. Circuit diagram of a fully differential driver. This circuit is for sink type laser array in which the *p*-type substrate is served as the common ground.

lation current. The adjustment mechanism is common to every driver in an array. In this circuit, the bias current is

$$I_{bias} = 4\frac{V_{th} - V_{BE}}{R_{th} + R_7} \tag{10.1}$$

for both differential channels. Similarly, the modulation current is

$$I_{\text{mod}} = 4\frac{V_{\text{mod}} - V_{BE}}{R_{\text{mod}} + R_4} \quad . \tag{10.2}$$

The factor four in Eq.(10.1) and Eq.(10.2) is due to the sizing of the current mirror.

The major difference of this laser driver from the one that is used for single-ended application is the additional biasing circuitry necessary to provide biasing current for the second laser. These two biasing circuits share the same current mirror and cannot be individually adjusted.

An input buffer is provided in order to interface with the 50Ω transmission lines. The outputs from the emitter followers drive an open-collector configured differential current switch. The collectors of the differential current switch can then be wire-bonded to the laser diode array.

The driver circuit for a source type laser array is shown in Figure 10-2. The basic design philosophy is similar to that shown in Figure 10-1 except the biasing current mirror has been designed to provide the *total* current for the laser diode rather than the threshold current. When one branch of the current switch is turned on, it will sink current *away* from the total current supplied by the PNP transistors and reduce the amount of current supplied to the laser diode. The performance of a PNP transistor is usually poorer in a bipolar process in comparison with an NPN transistor because these processes can only have lateral PNP transistors. This is not a problem for this particular design since the PNP transistors are not involved in high speed switching.

Alternatively, the PNP transistors can be replaced by PMOS's available in a BiCMOS process. The PMOS can usually provide much higher driving capability and thus reduce the total area requirement of the driver.

10.3 Physical Circuit Layout

The physical layout of the driver circuit shown in Figure 10-1 is shown in Figure 10-3. The size of the chip including the bonding pad for the laser diodes is 1100 μm×800 μm. Both the nominal biasing current and the nominal modulation current are 30 mA when V_{th} and V_{mod} are tied to V_{cc}. This driver has been designed to sustain up to 40 mA of modulation and biasing current. The total power consumption (including the power consumed at the laser diodes) is ~600 mW. The excessive power consumed by this transmitter design is because of the high biasing and modulation current usually required for high-speed modulation. The power consumption by the transmitter can be significantly reduced if a low-threshold multiple-quantum-well (MQW) laser with sub-miliamp threshold current is used.

The physical layout of a driver array based on the circuit from Figure 10-2 for driving source type laser diode arrays is shown in Figure 10-4. The features of this driver array are very similar to the one for driving sink type laser diode arrays.

10.4 Simulation Results

(1) Single Transmitter

The simulated eye pattern of laser output from a single laser driver described in Section 2 is shown in Figure 10-6 and Figure 10-7 for 1 Gbps and 2 Gbps operation, respectively. A small

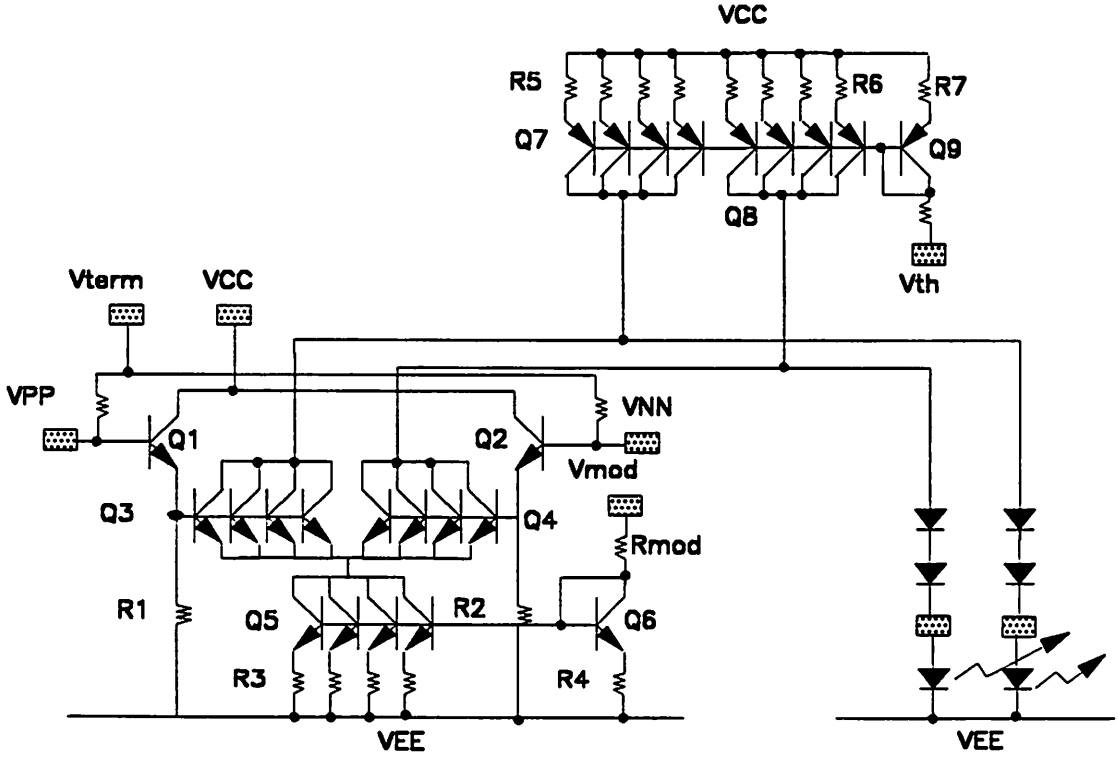

Figure 10-2. Circuit diagram of a fully differential transmitter array. This circuit is for source type laser array in which the *n*-type substrate is served as the common ground.

ringing exist in both cases due to the bonding wire inductance. At 2 Gbps, a significant waveform jitter (~80ps) can be observed.

(2) Transmitter Array

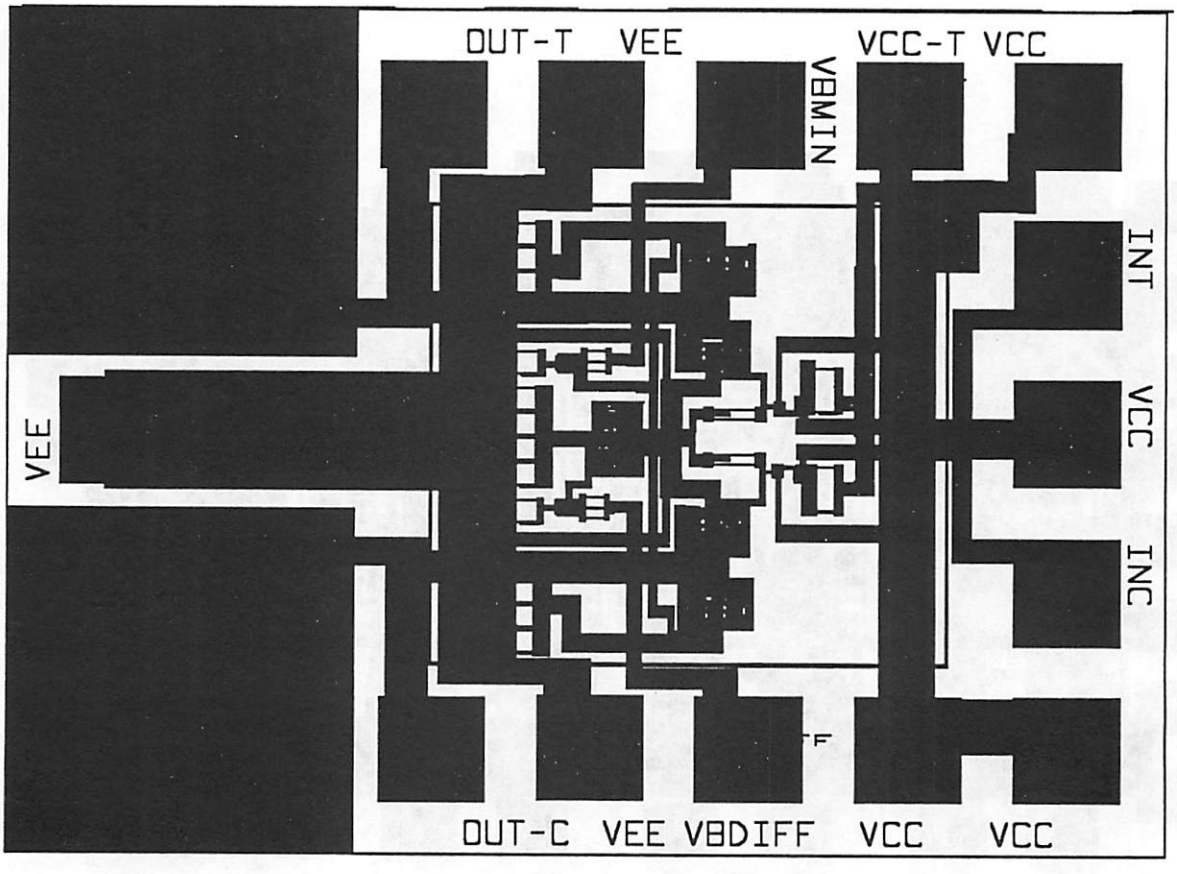

Figure 10-3. Physical layout of a fully differential driver. This corresponds to the circuit shown in Figure 10-1.

The hybrid integrated transmitter array system assumed for the simulation is shown in Figure 10-5 in which a bipolar driver array is wire-bonded to a laser diode array. The bonding wires between the driver array and laser diode array introduce crosstalk and waveform distortion for the signals and have been accounted for in the simulations. A worst-case methodology which as-

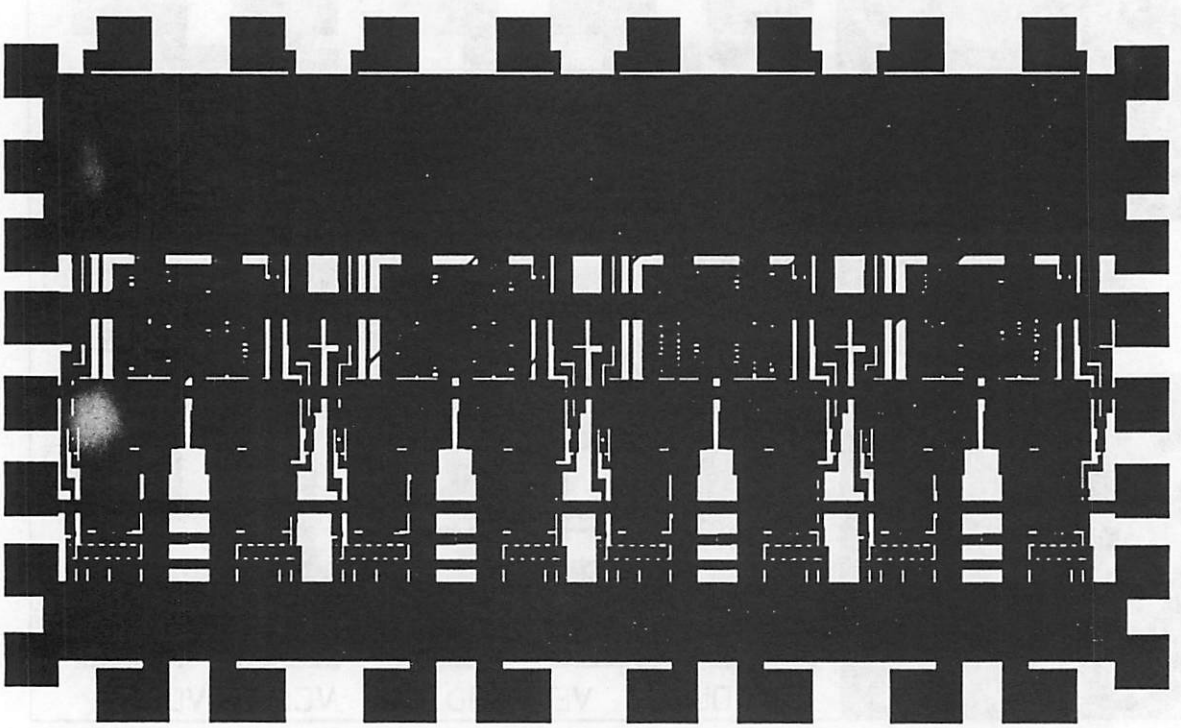

Figure 10-4. Physical layout of a fully differential driver array. Each cell in this array corresponds to the circuit shown in Figure 10-2.

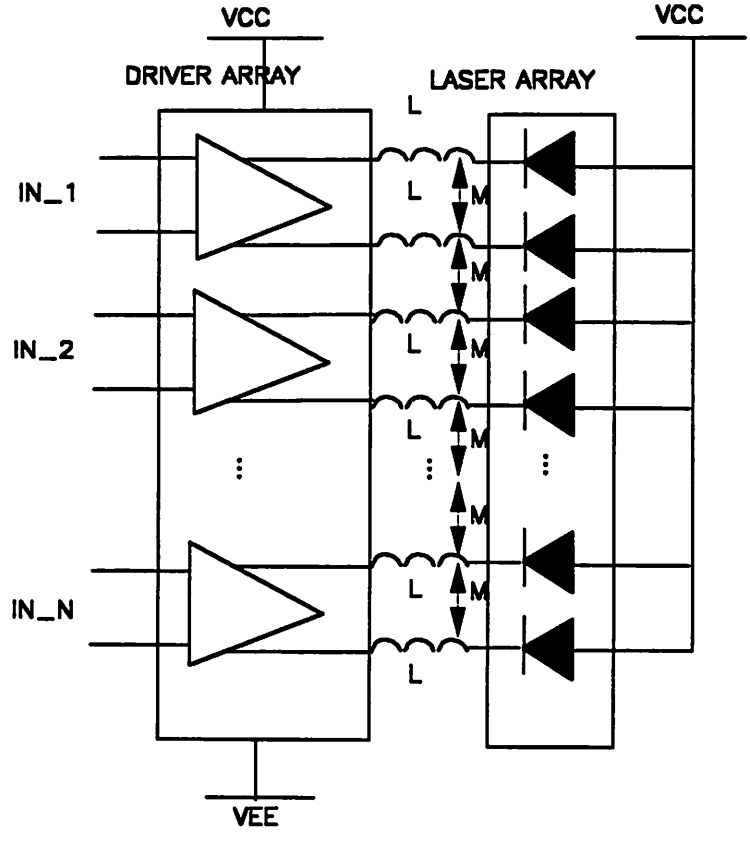

Figure 10-5. Block diagram of a differential transmitter array environment.

sumes all except one channel switch simultaneously in the same direction is used here to obtain the maximum switching noise.

The simulated switching noise waveform for an array of size 16 consisting of identical design is shown in Figure 10-8 and Figure 10-9 for 1 Gbps and 2 Gbps operation, respectively. The maximum switching noise for both cases are $\leq$5%(or $-$26 dB). The eye pattern of the active channels, however, suffers a significant eye degradation at 2Gbps.

Switching noise vs. array size is shown in Figure 10-10. The maximum switching noise is less than 5% even for an array size of 16. This is significantly less than those reported in Chapter 7 in which a similar driver circuit is used to drive a single-ended configuration. The crosstalk is plotted as a function of mutual inductance in Figure 10-11 for both single-ended and differential driver

array. The ratio between mutual inductance and the bonding wire inductance in this figure varies from 0.01 to 0.20. Apparently, the dominant effect of crosstalk comes from switching noise (as illustrated between $N = 3$ and $N = 9$) rather than mutual inductance, which rises less than 1% as the mutual inductance varies from 0.01 to 0.2. Switching noise vs. the size of the array for both single-ended and differentially configured driver array using BiCMOS technology to drive a common n-substrate laser diode array is compared in Figure 10-12. The crosstalk is significantly less in the differential case as compared to the single-ended case. This result is consistent with the case in which a common p-substrate laser diode array is driven by a bipolar driver array even though the basic circuit technologies for these two laser driver array are different.

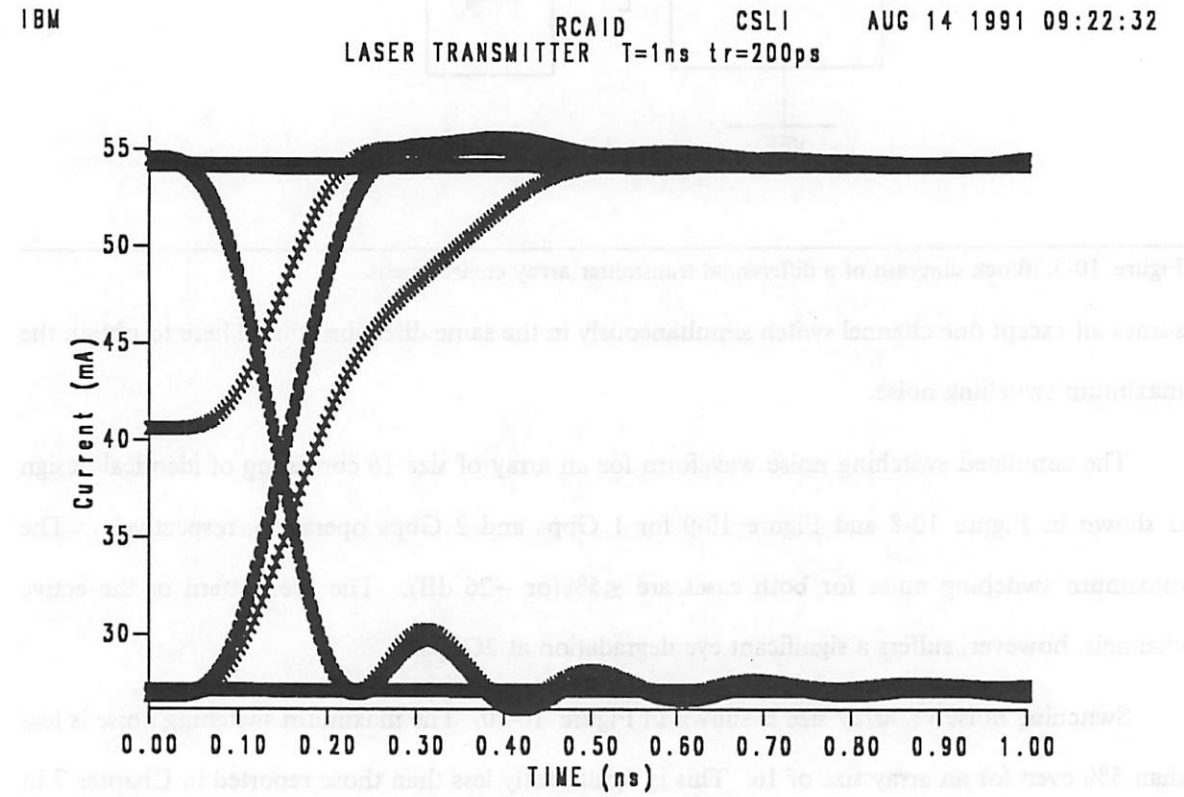

Figure 10-6. Simulated eye pattern of a laser driver at 1Gbps. The rise time of the input signal is 200ps.

10.5 Summary

In this chapter, we describe the design and simulation results of a laser driver which can be operated up to 2.5 Gbps with a maximum switching noise less than 5% (or −26 dB). This design also verifies that a fully differential configuration can reduce the maximum switching noise at the transmitter side compared with a single-ended optical interconnect with a similar driver structure.

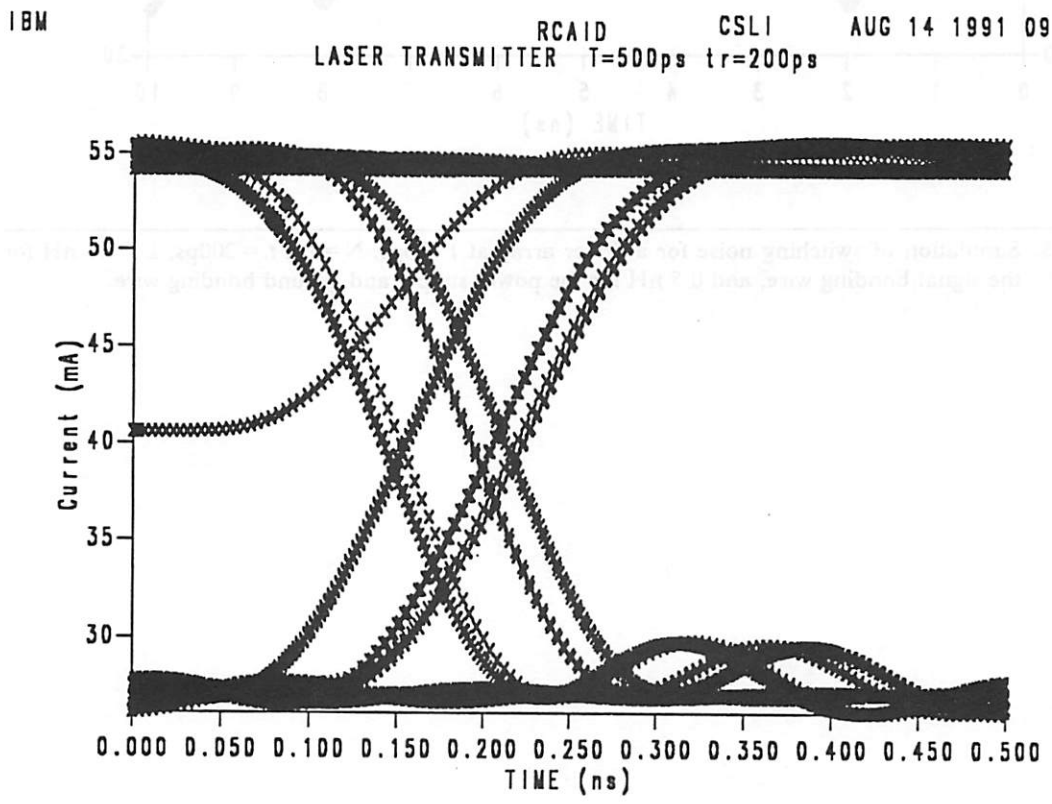

Figure 10-7. Simulated eye pattern of a laser driver at 2Gbps. The rise time of the input signal is 200ps.

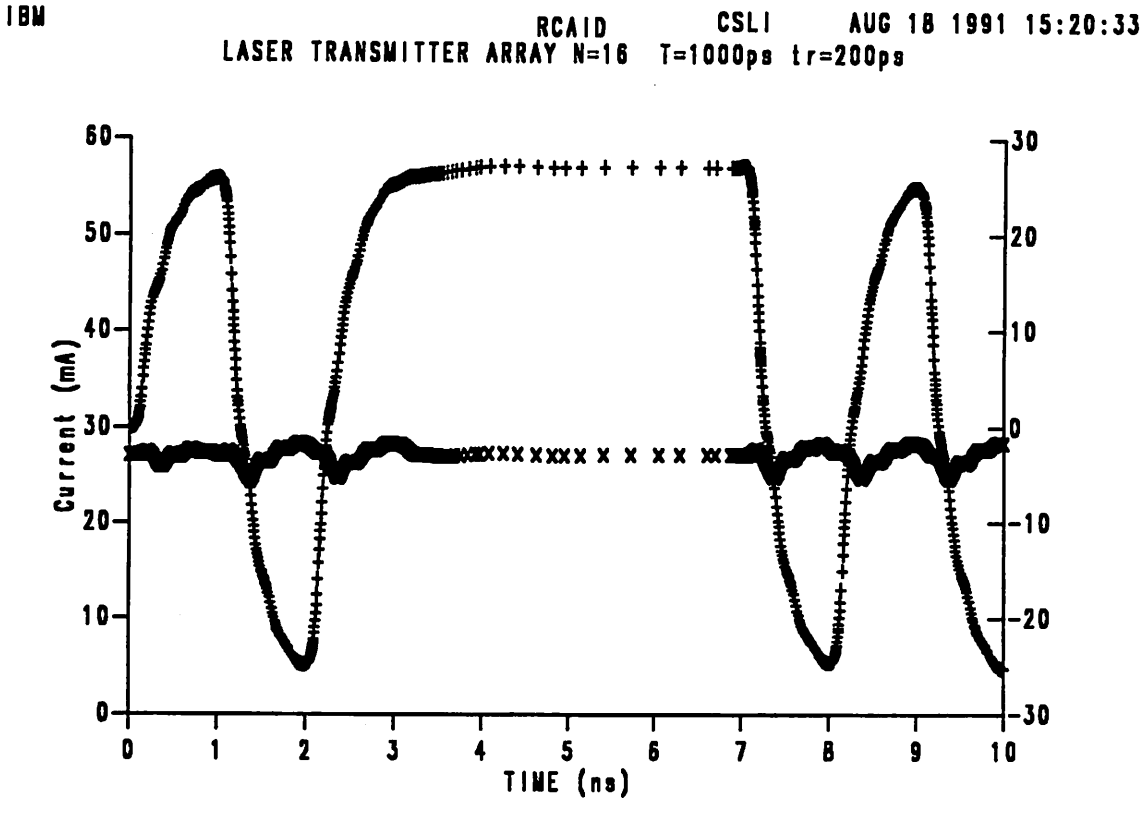

Figure 10-8. Simulation of switching noise for a driver array at 1 Gbps. N = 16, t_r = 200ps, L = 1.5 nH for the signal bonding wire, and 0.5 nH for the power supply and ground bonding wire.

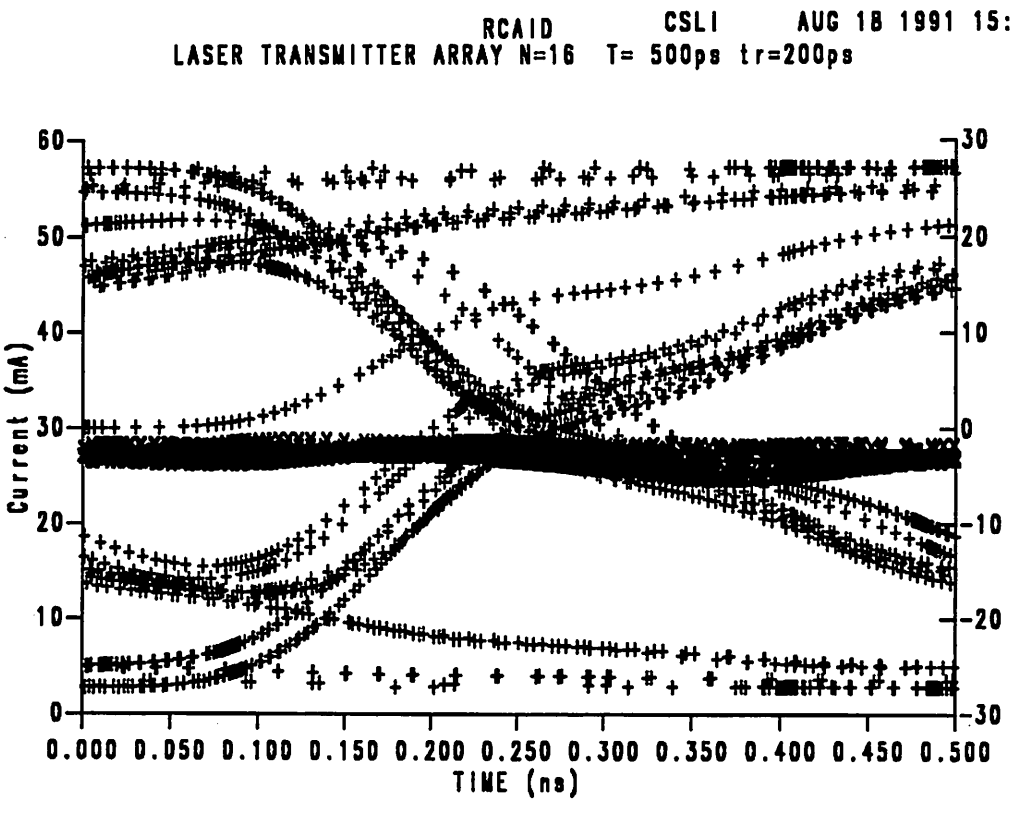

Figure 10-9. Simulation of switching noise for a driver array at 2 Gbps. N = 16, t_r = 200 ps, L = 1.5 nH for the signal bonding wire, and 0.5 nH for the power supply and ground bonding wire.

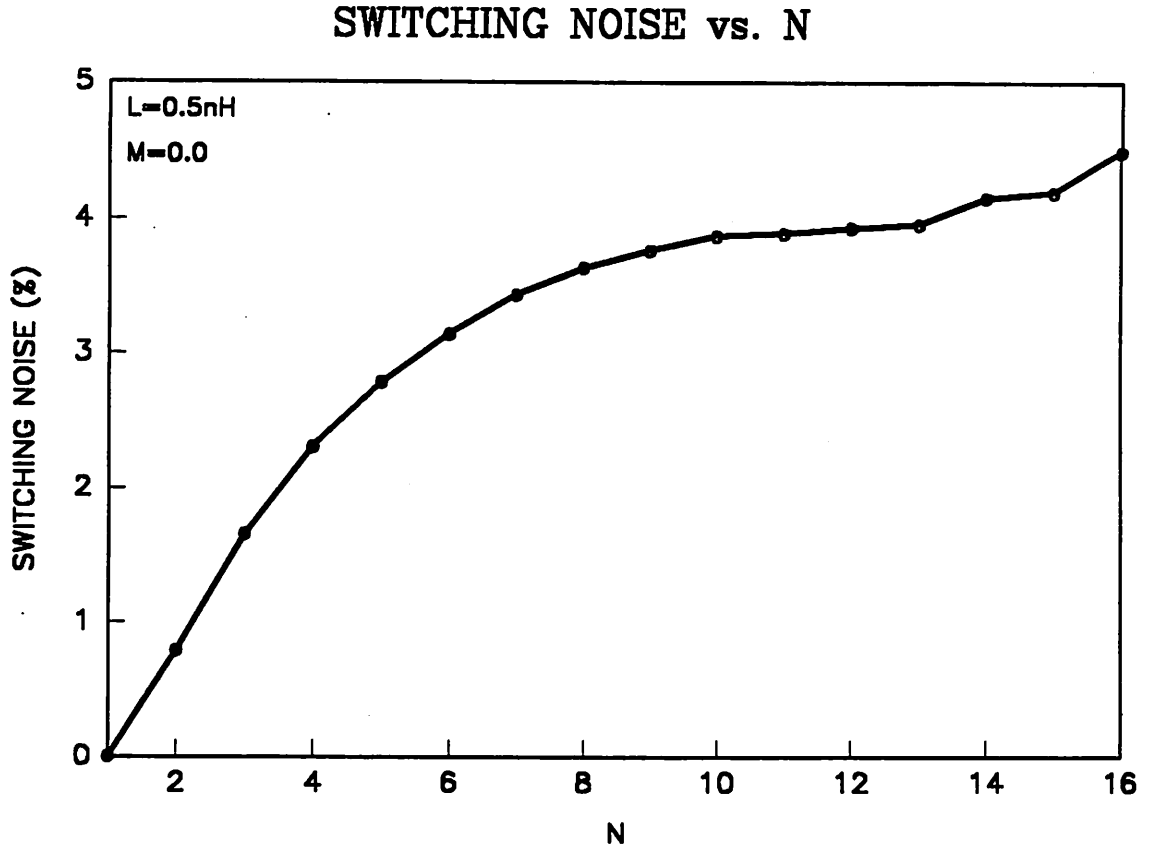

Figure 10-10. Switching noise vs. N for a differential driver array. A common p —substrate laser diode array is assumed.

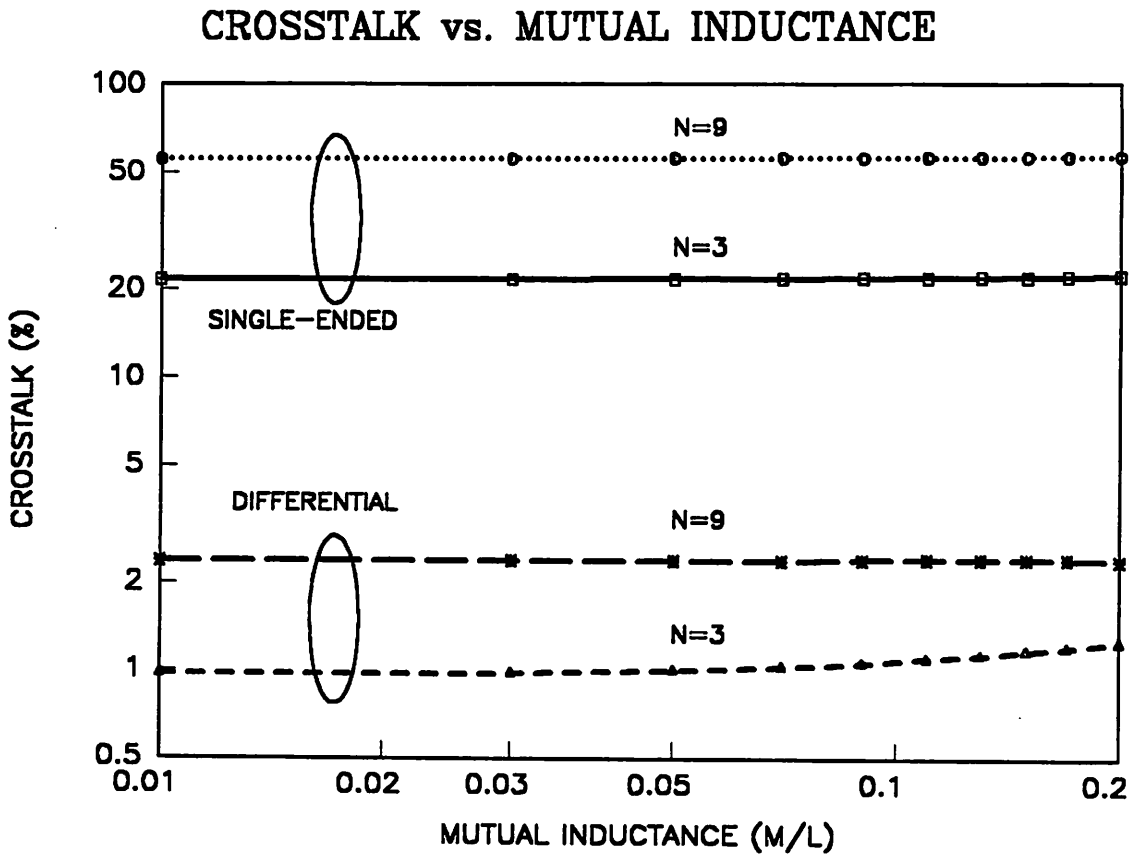

Figure 10-11. Crosstalk vs. mutual inductance for various driver array configurations. Mutual inductance is measured with respect to the bonding wire inductance, i.e., M/L. L is assume to be $0.5nH$ while power decoupling capacitance is assumed to be $10nF$ in all cases.

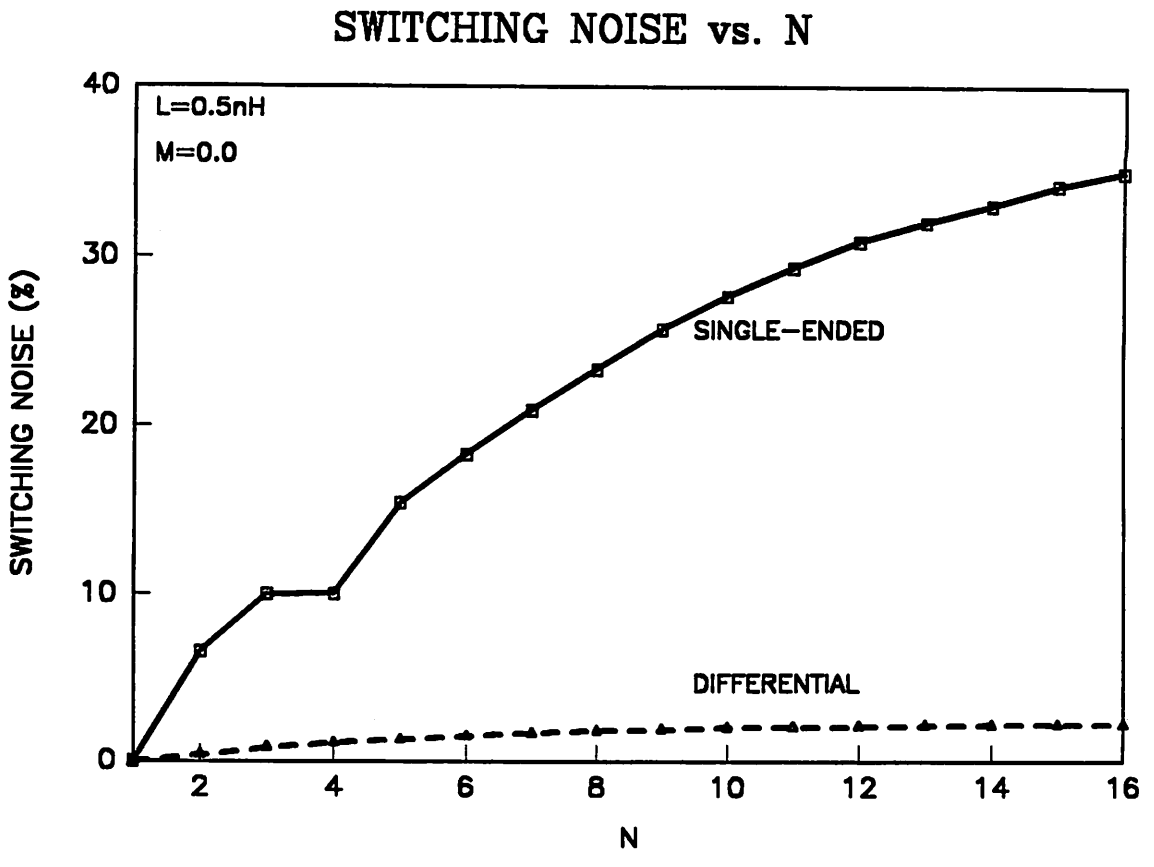

Figure 10-12. Comparison of switching noise vs. N between single-ended and differential driver array. A common *n* –substrate laser diode array is assumed.

CHAPTER 11 FULLY DIFFERENTIAL INTEGRATED OPTICAL RECEIVER ARRAY

11.1 Introduction

A fully differential optical interconnect system using a differentially configured laser driver and receiver, as proposed in Chapter 9, has the potential to offer the following advantages:

- Packaging constraints such as power supply decoupling are relaxed,
- Power supply and ground noise generated by surrounding electronic circuits is suppressed,
- Ideally, the threshold at the output of the receiver does not depend on the signal level, providing that channel mismatch is not serious, and thus avoids having to use a sophisticated automatic gain control mechanism to maintain a constant threshold.

In Chapter 10, we described how to implement a fully differential driver using bipolar or BiCMOS technology. In this chapter, an OEIC (optoelectronic integrated circuit) approach[34] has been used to design, simulate and fabricate a receiver array.[35]

According to the simulations, the features of this receiver array design include:

- The photodetector array and the amplifier array are monolithically integrated on the same GaAs substrate with 400 μm channel spacing,
- Each Metal-Semiconductor-Metal photodetector (MSM-PD) has a diameter of 80 μm. Its responsivity is between 0.25 and 0.35 A/W at 0.85 μm and its capacitance is less than 200 fF,
- The receiver has a nominal bandwidth 800 MHz with 4KΩ transimpedance,
- The receiver sensitivity is -23 dBm at a bit error rate of 10^{-15},
- The power consumption of each preamp and postamp is 78 mW and 170 mW, respectively,

[34] OEIC technology allows both of the photodetectors and receivers to be monolithically integrated on the same GaAs substrate.

[35] The receiver design for this array is based on an earlier design for a single-ended optical interconnect system by Y. Kwark of IBM T. J. Watson Research Center.

- The switching noise is almost negligible even with 0 dBm input light signals ($\leq$0.2%, or ≤ -40 dB)
- The waveform jitter and signal distortion are negligible.

The organization of this chapter is as follows: Section 2 discusses the preamp and the overall receiver circuit design. Section 3 describes the sensitivity calculation and the preamp optimization. The chip photographs of a single receiver cell and the receiver array are shown in Section 4, while the simulation results are presented in Section 5. This chapter is summarized in Section 6.

11.2 Circuit Design

11.2.1 Preamplifier Array

The block diagram of an integrated transimpedance preamplifier is shown in Figure 11-1. The MSM-PD's are DC-coupled to the front-end of the preamplifier. Biasing of each MSM-PD is determined by the voltage difference between the power supply of the MSM-PD and the input node of the preamp. In this design, a separate power supply is provided for the MSM-PD array so that the adjustment of the bias voltage for the MSM-PD is independent of the receiver power supply. Usually, a larger bias is preferable for an MSM-PD in order to achieve a higher quantum efficiency. Furthermore, a separate power supply for the MSM-PD's prevents the switching noise of the amplifier stage from coupling into the receiver stage.

The preamplifier, as shown in Figure 11-2, consists of a cascode input stage followed by a source follower output stage. The input and output are connected through the feedback resistor which determines the transimpedance of this receiver. The bandwidth of this preamplifier circuit is limited by either the input or an internal RC time constant. The input time constant is determined by the feedback resistance and the total input capacitance, consisting of the detector and amplifier input capacitance, while the internal RC time constant is determined by the load resistance R_L and the gate capacitance of the source followers M_5 and M_6. Since the input capacitance (including the photodetector capacitance) is usually several times larger than the gate capacitance, and the feedback resistance is also several times larger than the load resistance, the bandwidth in this case is solely determined by the input stage, the location of the secondary pole is, however, determined by stability requirements. The input resistance is dominated by the resistive Miller effect:

DIFFERENTIAL PREAMPLIFIER

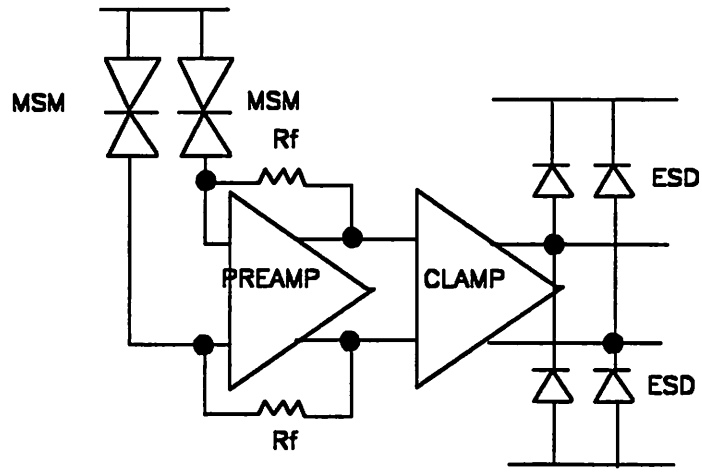

Figure 11-1. Circuit block diagram of a fully differential preamplifier.

$$R_i = \frac{R_f}{1 + a_V} \tag{11.1}$$

where R_f is the feedback resistance and a_V is the voltage gain from input to output. Assuming the transconductance of a GaAs MESFET is g_m while the voltage gain, a_V, of this circuit equals $g_m R_L$, the input resistance can then be computed,

$$R_i = \frac{R_f}{1 + g_m R_L} \tag{11.2}$$

The input capacitance is

$$C_i = C_d + C_g \tag{11.3}$$

where C_d and C_g are the photodetector capacitance and gate capacitance, respectively. The −3-dB bandwidth of the transimpedance amplifier thus approximately equals

$$f_{-3dB} = \frac{1 + g_m R_L}{2\pi R_f (C_d + C_g)} \tag{11.4}$$

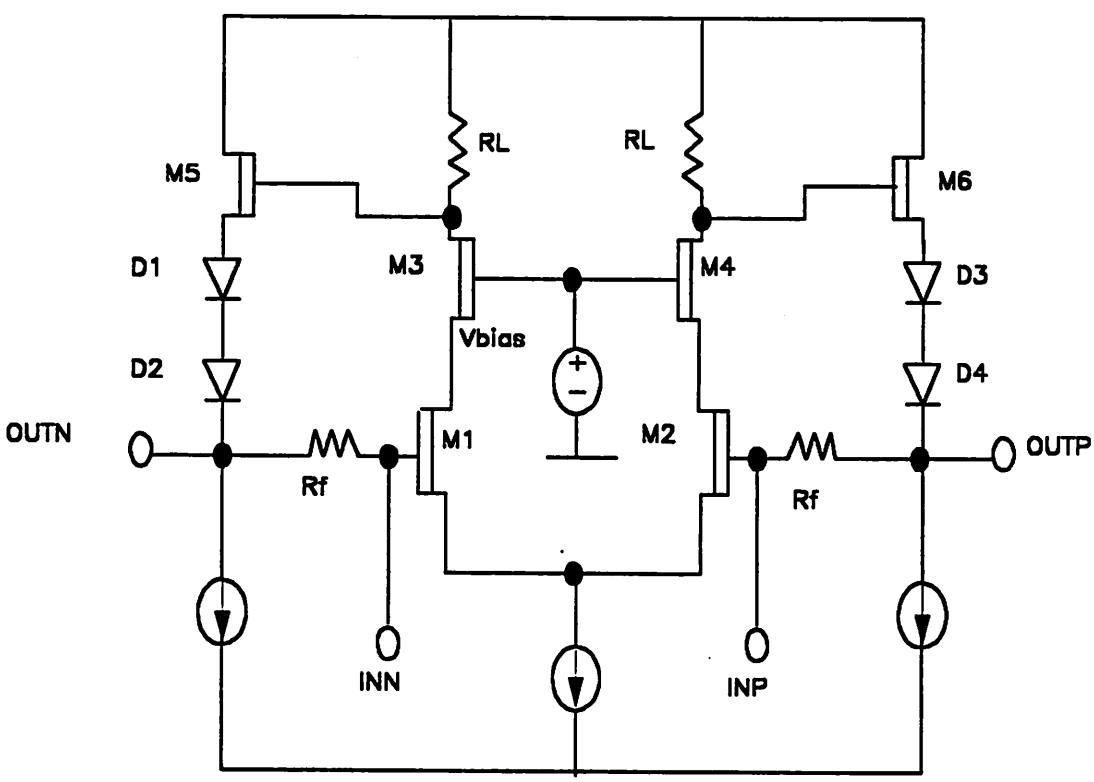

Figure 11-2. Simplified circuit diagram of the transimpedance front-end.

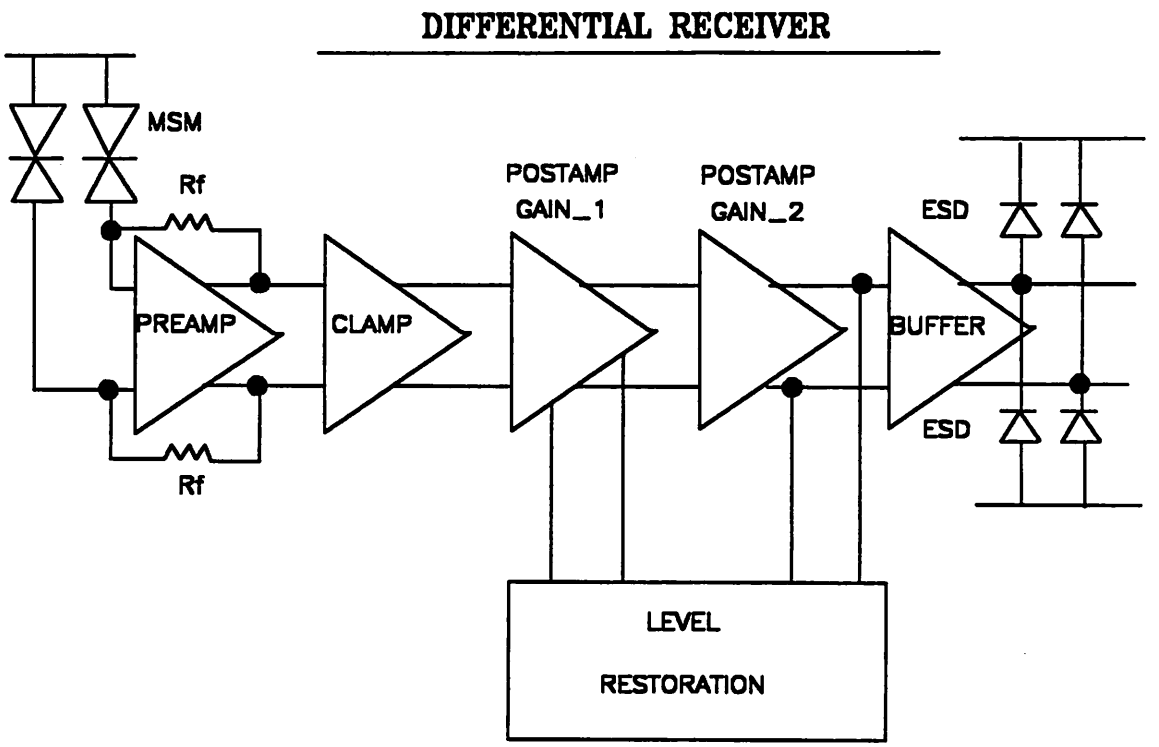

Figure 11-3. Circuit block diagram of a complete receiver.

Assuming C_d is 200fF, C_g of the input MESFET is 100 fF, g_m of the input MESFET is 5 mS, R_L is 2KΩ, R_f is 4KΩ, the −3-dB bandwidth thus equals 1.46 GHz. From this equation, we can also observe that the bandwidth is inversely proportional to the feedback resistance and proportional to the voltage gain. Therefore, there are several alternatives to improve the bandwidth of the preamp stage, but each of them has its own limitation:

- Decrease the feedback resistance. This will usually decrease the phase margin of the circuit and might affect the stability of the circuit. Furthermore, this also increases the thermal noise contributed by R_f and reduces the receiver sensitivity.

- Increase the load resistance. This will increase the dominance of the *RC*-constant determined by the load resistance and the gate capacitance of the source follower. Eventually, the bandwidth and stability will be determined by this *RC* time constant rather than the *RC* time constant of the input stage.
- Increase the size of the MESFET at the input stage to increase g_m. But this will also lead to the increase of the gate capacitance, resulting in an increase in the RC time constant of the input stage.[36]

In order to provide a wider dynamic range for the receiver, the preamplifier is followed by a clamp stage so that the output from the preamp stage does not saturate the postamp even at high input signal level. The output of the clamp stage has been designed with an maximum differential output of 200 mV driving into a 50Ω load.[37] The outputs of the clamp stage are protected with ESD diodes.

11.2.2 Full Receiver Array

A full receiver array, which includes both preamp and postamp, can be built using the circuit shown in Figure 11-3. In addition to the transimpedance preamplifier and the clamp stages described in the previous subsection, there are two gain stages, a level restoration stage, and an output buffer stage.

The circuit of a gain stage is similar to that of the transimpedance front-end except there is no feedback resistor between the input and the output. The input voltage is first amplified by a cascode stage followed by a source follower to serve as the buffer to the next stage. In this case, the bandwidth is usually limited by the *RC*-time constant determined by the load resistance and the gate capacitance of the source follower. Assuming a gate capacitance of 50 fF and load resistance of 2 KΩ, the −3-dB bandwidth is 1.59 GHz. The design principle for a gain stage is to make sure it has a similar bandwidth as compared to the preamplifier. The bandwidth is reduced when two identical gain stages are cascaded due to the faster roll-off rate of the combined frequency response.

---

[36] As it will become apparent in later discussions, the gain bandwidth product of a receiver is also set by the maximum allowable power supply voltage and the technology, namely, the f_T of a device.

[37] This means the load is 50 Ω single-ended each side and 100 Ω differential.

The level restoration circuitry has a lowpass filter to determine the DC component of the output of the postamp so that the offset voltage incurred by the possible device mismatch within the postamp can be compensated. This is necessary due to the presence of very large device mismatch in currently available GaAs processes. The DC response of the receiver, however, is somewhat degraded due to the presence of an averaging capacitor in the lowpass filter.

The output buffer consists of several source follower cascaded in series to provide sufficient driving capability into a 50Ω load.

11.3 Receiver Sensitivity and Front-End Optimization

11.3.1 Receiver Sensitivity

It has been shown in Chapter 9 that the error probability of a fully differential transimpedance preamplifier is

$$P_e = \frac{1}{2} erfc\left(\frac{V_{\{1,0\}}}{\sqrt{2}\,\sigma_{N,\{1,0\}}}\right) \tag{11.5}$$

because of the symmetric symbol constellation (i.e. $|V_1| = |V_0|$) and equal noise power (i.e. $\sigma_{N,1} = \sigma_{N,0}$). In order to achieve a bit-error-rate less than 10^{-15}, it is necessary to have

$$K = \frac{V_{\{1,0\}}}{\sigma_{N,\{1,0\}}} \geq 7.94 \tag{11.6}$$

The minimum required average optical power to achieve a bit-error-rate of 10^{-15} thus equals

$$P_{av,min} = 7.94\sigma_{N,\{1,0\}} \frac{h\nu}{\eta e R_f} \tag{11.7}$$

In the ideal case when noise is dominated by the thermal noise (Johnson noise) contributed by the feedback resistor R_f, we have

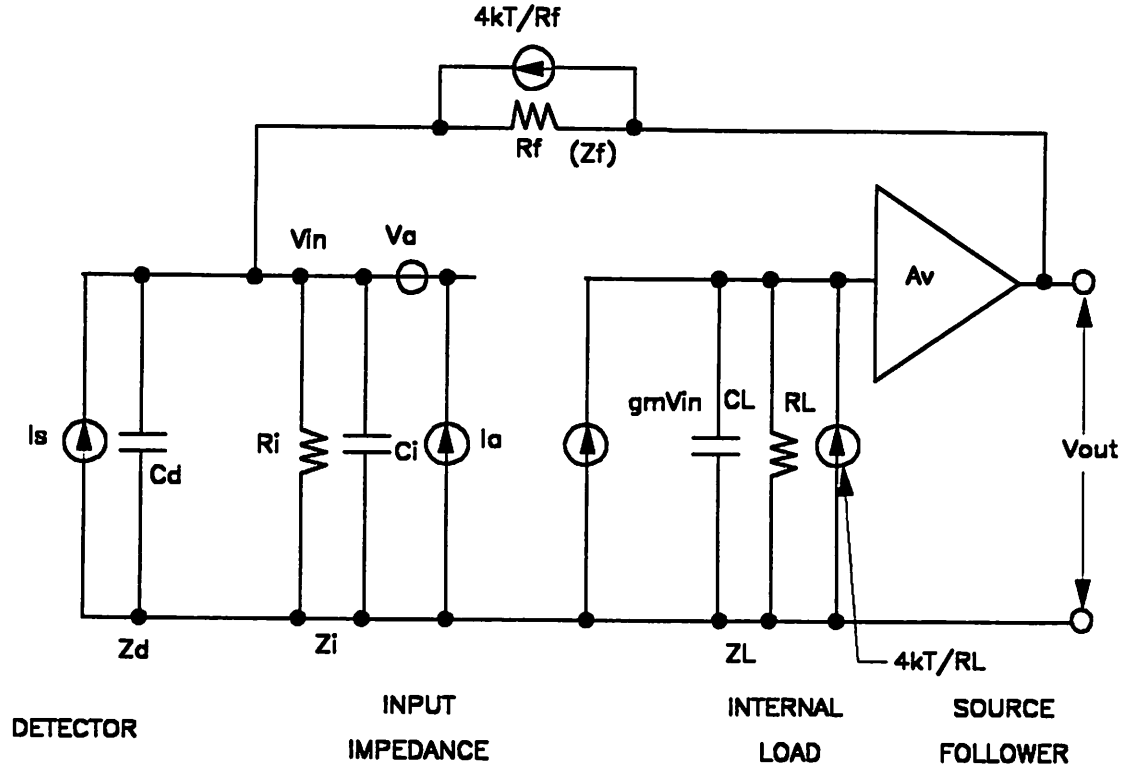

Figure 11-4. Half circuit of the fully differential receiver.

$$\sigma_{N,\{1,0\}} = \sqrt{8kTR_fB_e} \tag{11.8}$$

Assuming R_f is 4KΩ, B_e is 800 MHz, and the responsivity $\eta e/h\nu$ is 0.25A/W, the sensitivity achievable with this receiver configuration is −26 dBm. If other noise contributions are equal to the thermal noise of the feedback resistor, the theoretical achievable sensitivity becomes −23 dBm.

11.3.2 Preamp Optimization

A crude estimate of the receiver sensitivity was presented in the previous subsection. In this section, the full noise expression of the preamplifier is derived in order to perform front-end optimization. The half circuit of the preamplifier shown in Figure 11-2 is drawn in Figure 11-4. In

this half circuit, the MSM-PD is represented by an ideal current source in parallel with a capacitor C_d. The input impedance to the preamplifier is represented by Z_i, the feedback impedance is represented by Z_f, and the load resistance of the cascode stage and the input impedance of the source follower stage are lumped into Z_L. The source follower is represented as a voltage amplifier with amplification A_V.

As shown in Appendix A, the transconductance of a cascode stage G_m can be approximated by the transconductance g_m of the first MESFET in the cascode configuration while the output resistance can be ignored. Not shown in Figure 11-4 are

- input equivalent noise voltage i_e and noise current v_e of the cascode stage,

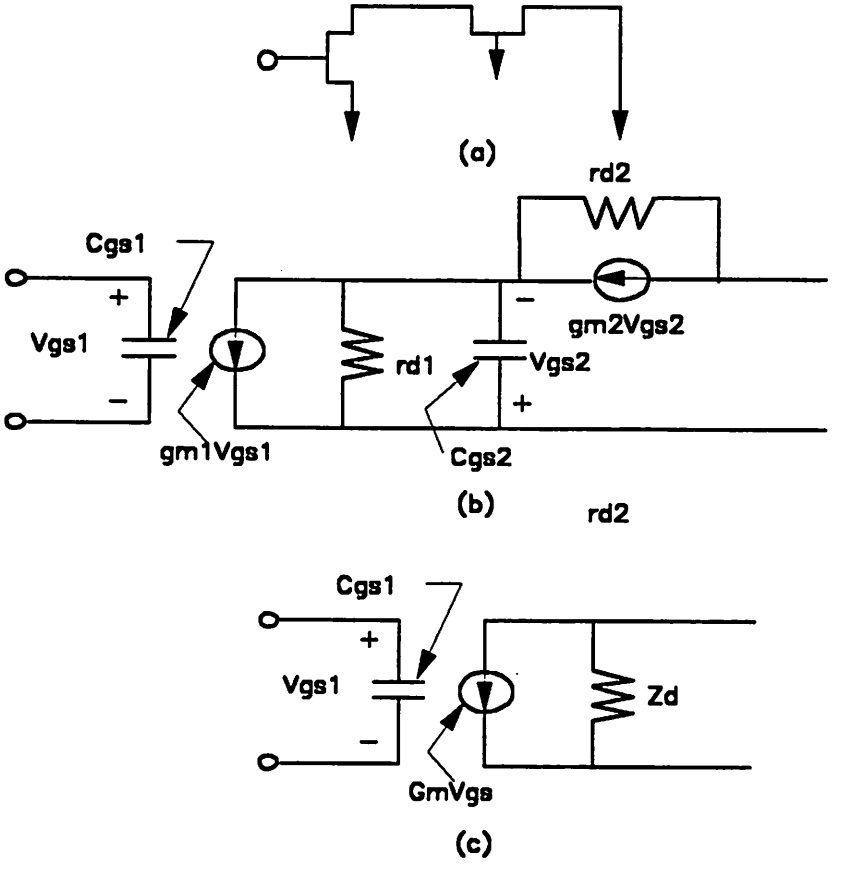

Figure 11-5. Equivalent circuit of a cascode configured stage.

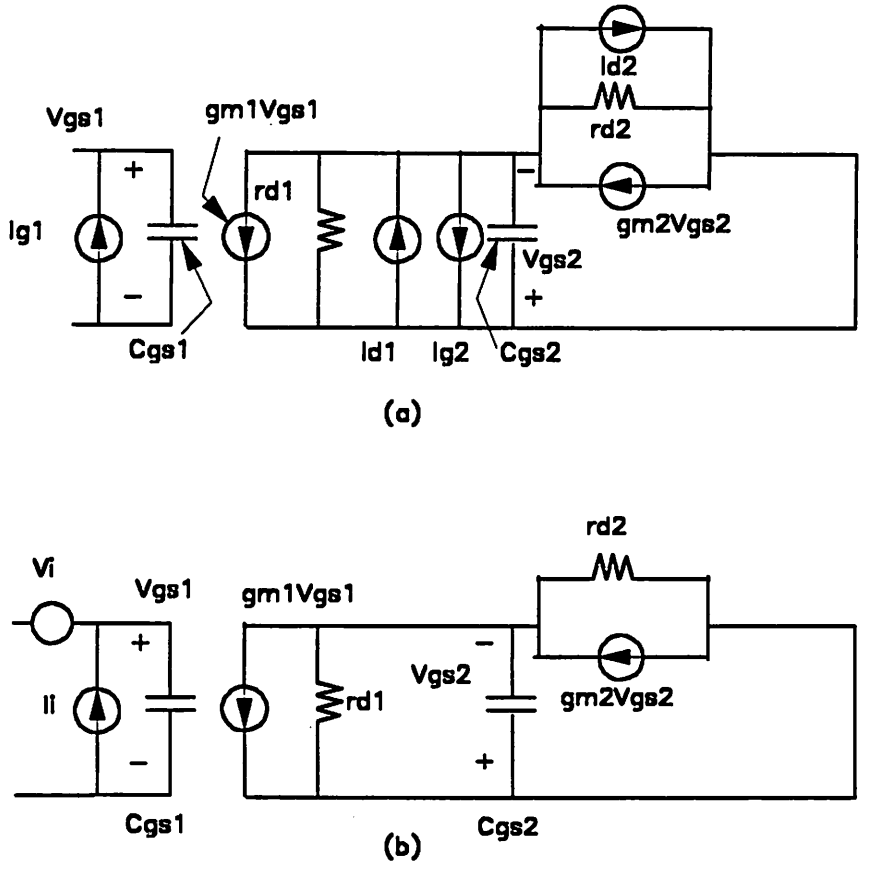

Figure 11-6. Noise equivalent circuit of a cascode configured stage.

- input equivalent noise voltage i_{sf} and noise current v_{sf} of the source follower stage,
- noise current of the feedback resistor i_f, and
- shot noise $2eI$.

We first compute the output signal. Summing the current flowing into the input node of the cascode stage, we have

$$I_s = \frac{v_{in}}{Z_i'} + \frac{v_{in} - v_{out}}{Z_f} \tag{11.9}$$

where the total input impedance Z_i' is

$$\frac{1}{Z_i'} = \frac{1}{Z_i} + \frac{1}{Z_d} \tag{11.10}$$

and has taken into account of the input impedance of the preamplifier Z_i and the impedance of the detector Z_d. In addition, the relationship between input and output voltage is $v_{out} = A_V g_m v_{in} Z_L$. We can thus solve for v_{in} in terms of v_{out} and substitute into Eq.(11.9):

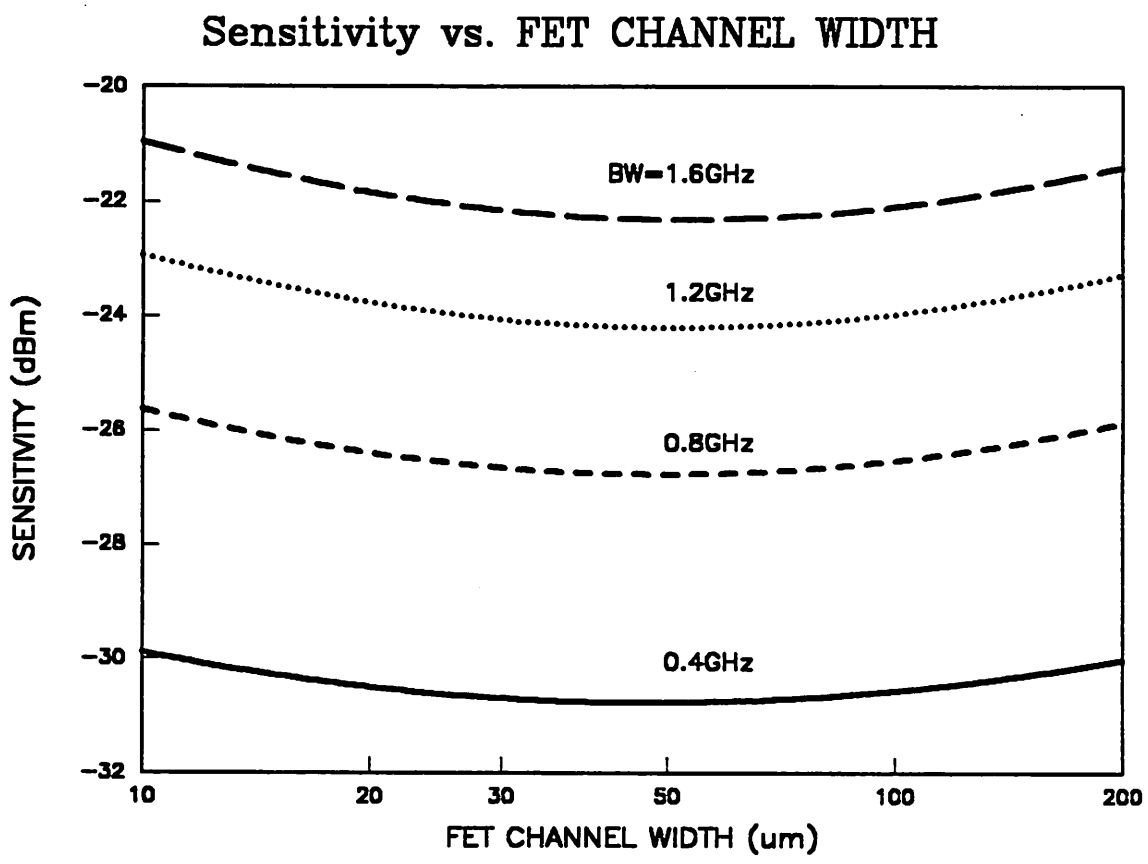

Figure 11-7. Sensitivity vs. channel width of the input MESFET. The receiver bandwidth is varied from 400 MHz to 1.6 GHz.

$$I_s = \frac{v_{out}}{A_V g_m Z_L}\left(\frac{1}{Z_i'} + \frac{1}{Z_f}\right) - \frac{v_{out}}{Z_f} \tag{11.11}$$

Therefore,the output voltage is

$$V_{out,s} = \frac{1}{\frac{1}{A_V g_m Z_L}\left(\frac{1}{Z_i'} + \frac{1}{Z_f}\right) - \frac{1}{Z_f}} I_s \tag{11.12}$$

Assuming $A_V g_m Z_L \gg 1$, this expression can be approximated by $V_{out,s} = -Z_f I_s$.

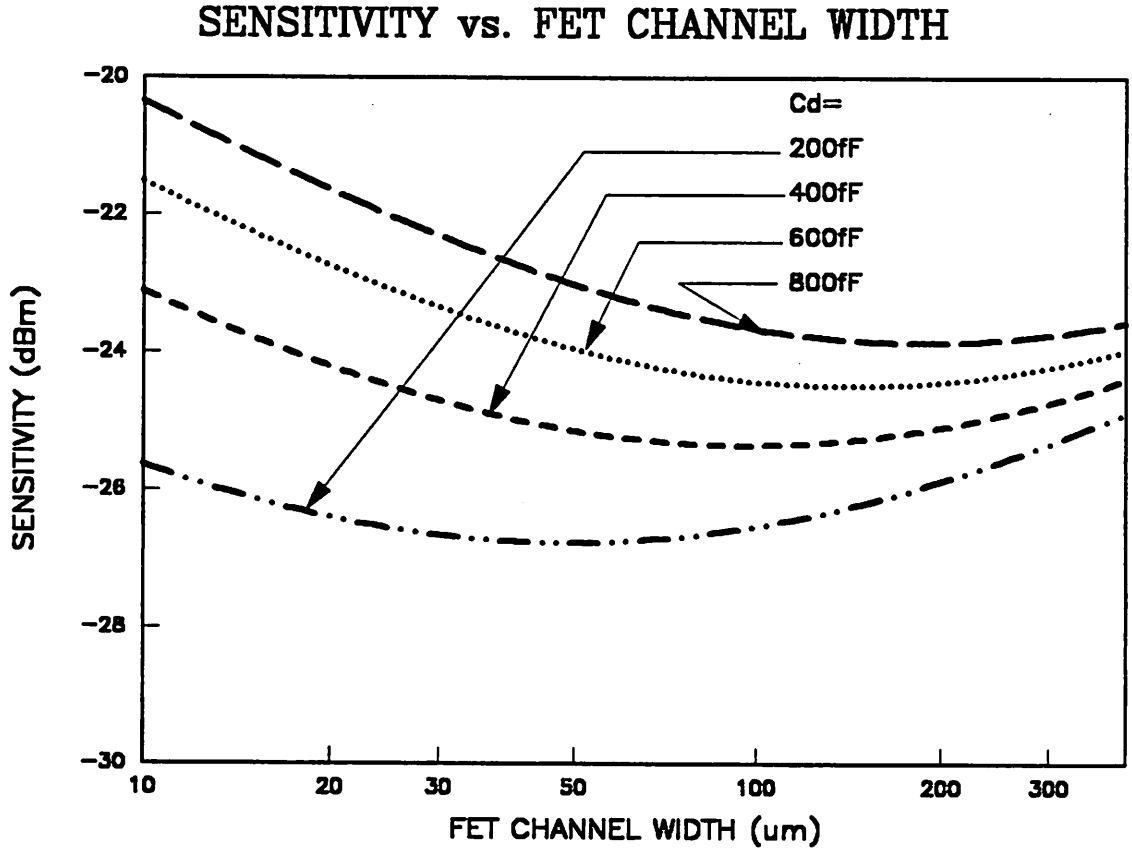

Figure 11-8. Sensitivity vs. channel width of the input MESFET. The receiver bandwidth is fixed at 800 MHz while the capacitance of the MSM-PD varied from 200 fF to 800 fF.

Using the equivalent input noise voltage and noise current of the cascode stage derived in Appendix B, it is shown in Appendix C that the total noise voltage equals

$$\begin{aligned} V_{out,N}^2 = & (1+\frac{4}{3}\pi^2 B^2 R_f^2 (C_d^2 + C_{gs1}^2))B4kT\Gamma \frac{1}{g_{m1}} + (\ln B + 2\pi^2 B^2 R_f^2 (C_d^2 + C_{gs1}^2))4kT\Gamma \frac{f_N}{g_{m1}} \\ & + (2eI + \frac{4kT}{R_f})R_f^2 B + \frac{1}{g_{m1}^2}(\frac{4\pi^2 B C_{gs5}^2}{3g_{m5}} 4kT\Gamma + \frac{16\pi^4 B^3 R_f^2 (C_{gs1}+C_d)^2 C_{gs5}^2}{5g_{m5}} 4kT\Gamma \\ & + \frac{2\pi^2 C_{gs5}^2}{g_{m5}^2} 4kT\Gamma f_N + \frac{4\pi^4 B^2 R_f^2 (C_{gs1}+C_d)^2 C_{gs5}^2}{g_{m5}^2} 4kT\Gamma f_N)B^2 \\ & + \frac{1}{g_{m1}^2}(1+\frac{4}{3}\pi^2 B^2 R_f^2 (C_{gs1}+C_d)^2)B\frac{4kT}{R_L} + 4kT\Gamma \frac{1}{g_{m5}}(B + f_N \ln B) \end{aligned} \tag{11.13}$$

where f_N is the noise corner frequency[38] of the flicker noise (or 1/f noise) while Γ is a factor that depends on the type of FET and may theoretically have numerical values between 1/3 and 2/3. The value 2/3 has been used throughout the calculations in this chapter.

Assuming a GaAs process with $C_{gs0} + C_{gd0} = 1.6fF/\mu m$, $g_{m0} = 150\mu S/\mu m$, the f_T of the intrinsic MESFET[39] thus equals ~15GHz. The parameters C_{gs0}, C_{gd0}, and g_{m0} are the gate-source parasitic capacitance, the gate-drain parasitic capacitance, and the transconductance, respectively. The available voltage gain is then limited to $f_T/1.5B$ where B is the amplifier bandwidth.[40] From the above noise expression, it can be shown that maximizing R_f also maximizes the sensitivity of the receiver, subjecting to the constraint imposed by Eq.(11.4). Using this noise expression, the sensitivity is plotted as a function of the channel width of the MESFET used at the front-end in Figure 11-7 for various bandwidth requirements. The gate capacitance and the transconductance of the front-end are assumed to be $C_g = W(C_{gs0} + C_{gd0})$ and $g_m = Wg_{m0}$, respectively, where W is the width of the channel. The noise corner frequency is assumed to be 10MHz. It is clear from this figure that an optimal channel width which maximizes the sensitivity exists. At 400 MHz band-

[38] The noise corner frequency is defined as the frequency where the total noise power spectral density is 3dB larger than the asymptotical noise power as the frequency approaches infinity.

[39] The f_T of the intrinsic MESFET equals $g_m/2\pi(C_{gd0} + C_{gs0})$.

[40] We require the amplifier bandwidth to be at least 1.5 times larger than the bandwidth determined by the input capacitance and the feedback resistance.

width, the optimal front-end channel width is 48 μm with a minimum achievable sensitivity of -30 dBm. The optimal channel width increases to 49.3 μm and 52.3 μm while the minimum achievable sensitivity degrades to -26 dBm and -22 dBm for a receiver bandwidth of 800 MHz and 1600 MHz, respectively. Note that the minimum sensitivity varies insignificantly over a wide range of channel width. On the other hand, the optimal channel width is very sensitive to the detector capacitance, as shown in Figure 11-8. The optimal channel width for a receiver bandwidth of 800 MHz increases from 49.3 μm to 97.37 μm when the capacitance of the detector is doubled from 200 fF to 400 fF.

11.3.3 MSM-PD Optimization

Figure 11-9 shows a typical MSM structure with finger width W, finger spacing L, and total photosensitive area A. An electrical field is established between adjacent fingers when a bias is applied across the electrode, as shown in Figure 11-9. Each electron-hole pair generated by the incoming photon is separated by this E-field and absorbed by the electrodes. Therefore, one speed limitation of such a device is determined by the transit time that an electron or a hole takes to travel to the electrode. From this aspect, a smaller finger spacing is more favorable to reduce the transit time. On the other hand, a smaller finger spacing increases the detector capacitance and thus the RC time constant of the front-end of the preamp. It has been reported in [139] that the rise time of the photo signal response is limited by the transit time while the fall time is limited by the RC time constant determined by the capacitance of the detector and the resistance of the external circuit. Therefore an optimal finger spacing exists which minimizes the fall time while allows a reasonable rise time.

It has been shown in [129, 140] that the total capacitance of this structure is

$$C = C_0 \frac{\text{photosensitive area}}{\text{finger period}} \tag{11.14}$$

where C_0 is given by

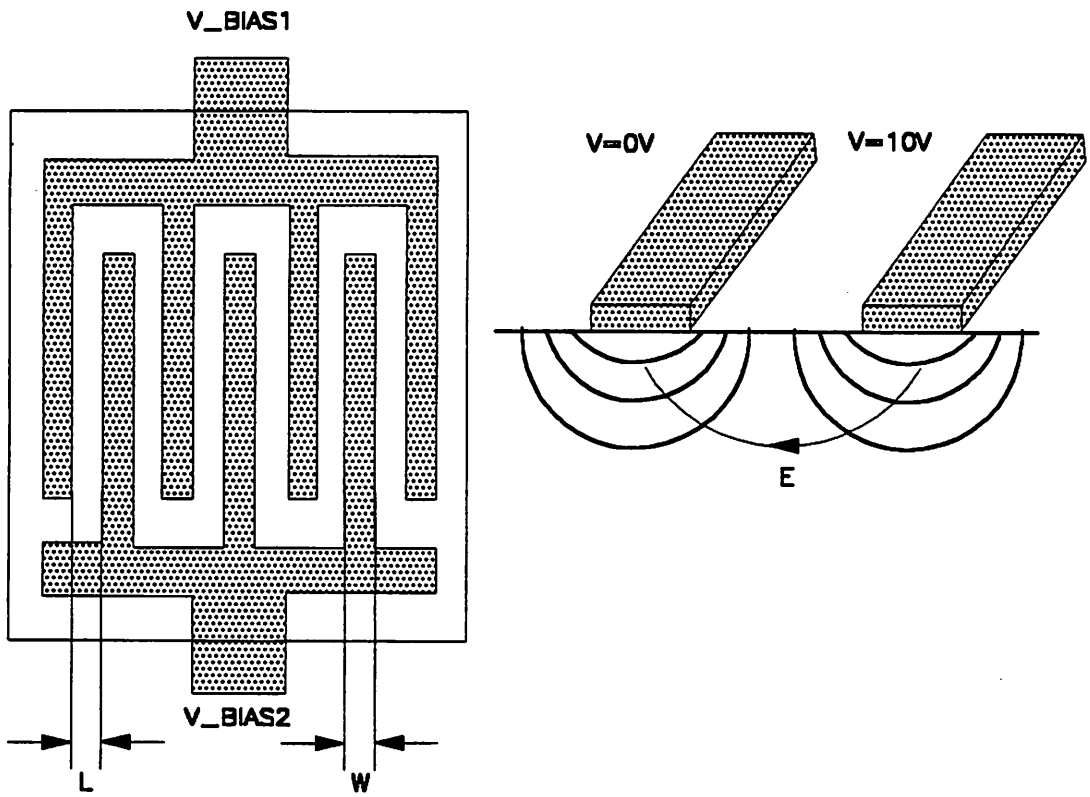

Figure 11-9. Typical Structure of a MSM photodetector.

$$C_0 = \varepsilon_0(1 + \varepsilon_r)\frac{K(k)}{K(k')} \tag{11.15}$$

In this expression, ε_0 and ε_r are the dielectric constant of vacuum and the relative dielectric constant of semiconductor, respectively, and $K(k)$ is the complete elliptic integral of the first kind, defined as

$$K(k) \equiv \int_0^{\frac{\pi}{2}} \frac{d\phi}{\sqrt{1 - k^2 \sin^2\phi}} \tag{11.16}$$

where

$$k = \tan^2 \frac{\pi}{4} \frac{\text{finger width}}{\text{finger period}} \tag{11.17}$$

and $k' = \sqrt{1 - k^2}$. Using these expressions, Figure 11-10 shows the capacitance as a function of the finger spacing for various values of finger width. The capacitance decreases monotonically with the increase of the finger spacing for a given finger width. In contrast, Figure 11-11 shows the total capacitance as a function of the finger width for various values of finger spacing. A maximum capacitance exists for each given finger spacing. The existence of such a maximum is due to the

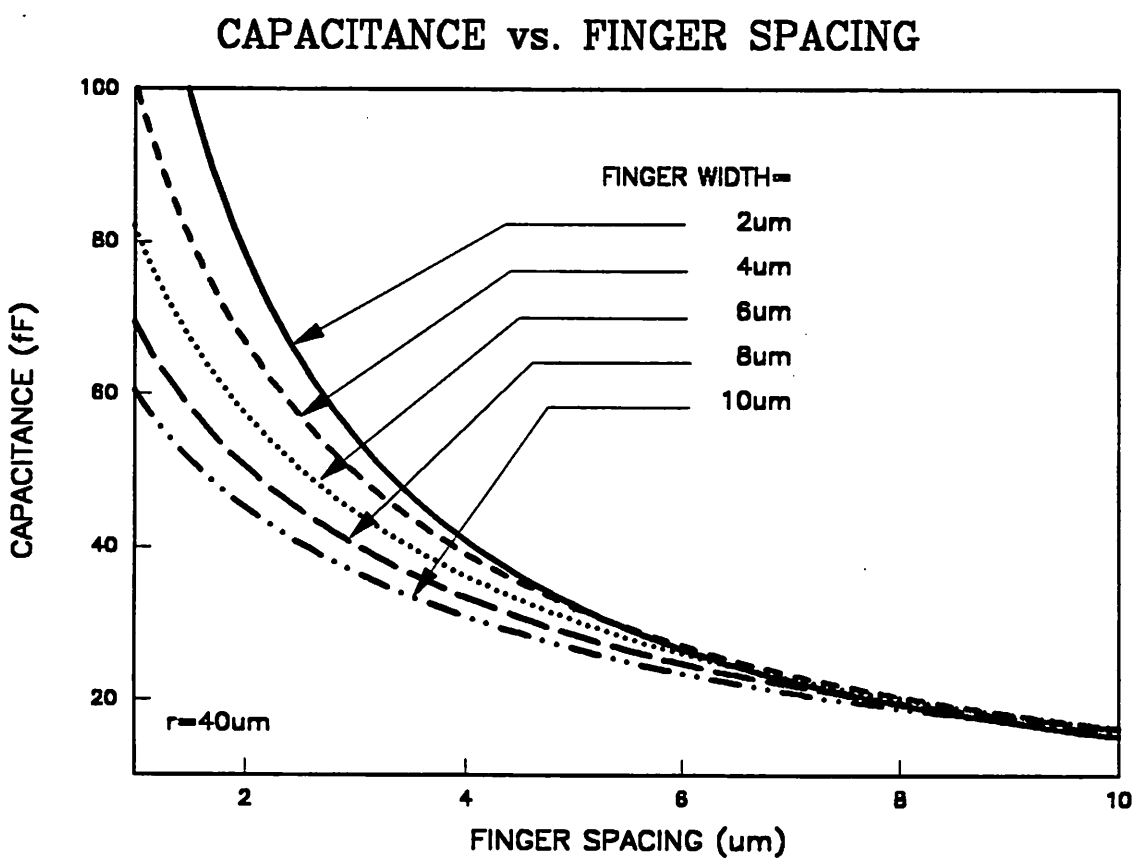

Figure 11-10. Total MSM capacitance as a function of the finger spacing. Total MSM photosensitive area has a radius of 80 μm.

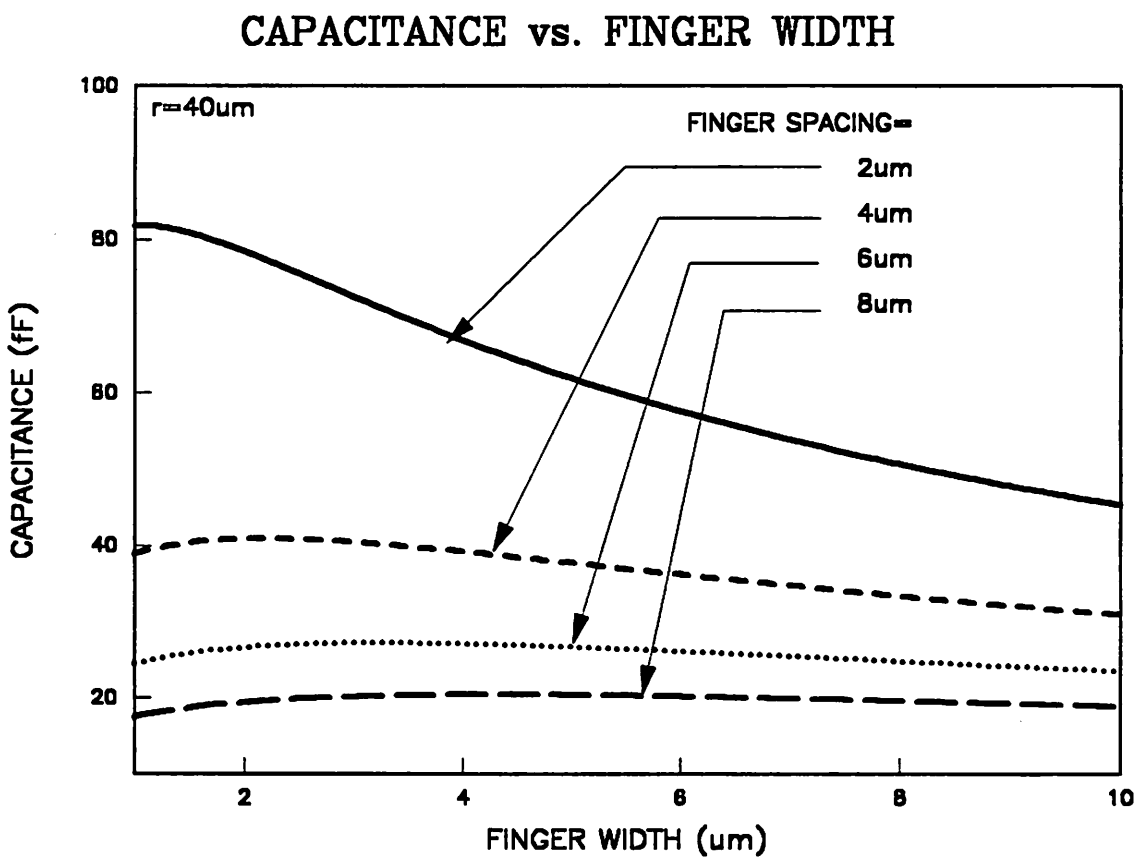

Figure 11-11. Total MSM capacitance as a function of the finger width. Total MSM photosensitive area has a radius 80 μm.

behavior of the elliptical integral $K(k)$, which monotonically increases with the increase of W. However, the number of fingers decreases as the finger width increases and thus the total capacitance is dominated by the reduction of the total number of fingers as the finger width is larger than a few microns.[41] This analysis, however, does not account for the passivation of the detector surface which is commonly adopted to reduce the surface states and to improve the detector frequency response.

[41] The responsivity decreases as the finger width increases while maintaining a constant finger spacing, since the total effective photon reception area is decreased.

Assuming the photosensitive area has a radius of 40 μm, a finger spacing of 2 μm, and a finger width of 2 μm, the total capacitance will be less than 100 fF.[42]

11.4 Chip Photographs of the Receiver Array

11.4.1 Receiver Cell

The chip photograph of a differential preamp cell is shown in Figure 11-12. From right to left, the preamp cell consists of two photodetectors, a transimpedance amplifier, a clamp stage, and two output bonding pads. The power and ground distribution has already take into the array geometry into consideration. The channel width is limited by the bonding pads and is 400μ while the channel height is 1422 μm.

The chip photograph of a full receiver is shown in Figure 11-13. Starting from the bottom, the first three stages of the full receiver are the same as the preamp. The fourth stage to the eighth stage are the first gain stage, the level restoration stage, the low-pass filtering stage, the second gain stage, and an output buffer stage, respectively. The channel width is still 400 μm while the height has increased to 3053 μm.

In both cases, a fully differential analog output is provided.

11.4.2 Integrated Receiver Array

The chip photograph of a 12-preamp array with each preamp based on the design in Figure 11-12 is shown in Figure 11-14. The preamp cell has been flipped for every other channel in order to match the power and ground distribution. The power and ground pads for the preamp are located at both ends while separate power pads are provided for the MSM photodetector. The size of the chip is 1422 μm×5000 μm and the total power consumption is 936 mW (simulation).

The chip photograph of a 6-receiver array with each receiver based on the design in Figure 11-13 is shown in Figure 11-15. More power and ground pads are provided for the receiver. The size of the chip is 3053 μm×2600 μm and the total power consumption is 1.49W (simulation).

11.5 Simulation Results

[42] A more exact simulation of this photodetector structure which include other parasitic capacitance run by Y. Kwark of IBM Watson Research indicates the total capacitance is ~200 fF.

The simulation eye pattern of the preamplifier and full amplifier using a 40-bit pseudo random sequence is shown in Figure 11-16 for 0 dBm, Figure 11-17 for −12 dBm, and Figure 11-18 for −24 dBm. The upper traces of these figures show the differential output from the second gain stage of the postamplifier while the lower traces show the output of the whole receiver. No noticeable edge jitter or waveform distortion can be observed from these eye patterns. The waveforms at various extinction ratios are shown in Figure 11-19 for $r = 5$, and Figure 11-20 for $r = 2$. As the extinction ratio decreases, the waveform becomes more distorted. But the waveform is still intelligible even at $r = 2$. The low frequency response of the receiver is shown in Figure 11-21 for 0 dBm input. The low frequency response is obtained by sending a long stream of logical ONE (40 bits) and observe the output to investigate the degradation. From Figure 11-21, the low frequency response does not have a noticeable droop during the simulation period. The switching noise of the preamplifier array for the case where $N = 8$ and input light level at 0 dBm is shown in Figure 11-23 for a extinction ratio of 8 and in Figure 11-24 for a extinction ratio of 2. The maximum switching noise is obtained by using the worst case model as described in Chapter 8. At 0 dBm light input and assuming perfect balance, the switching noise is less than 0.2% (or −40 dB).

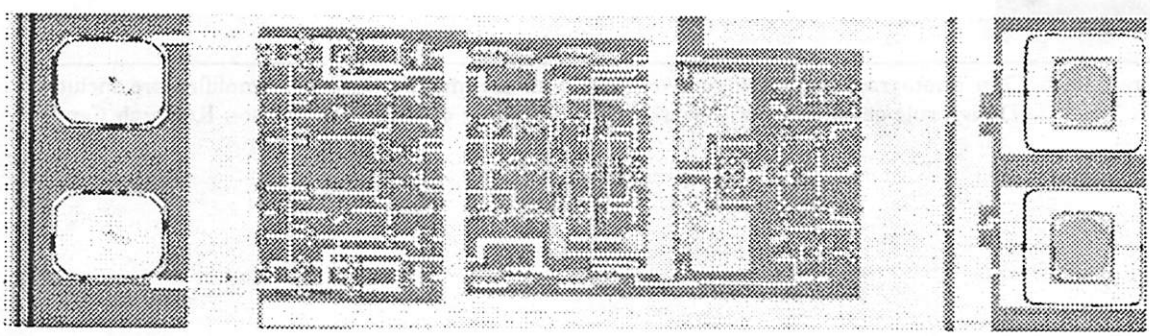

Figure 11-12. Chip photograph of a single preamplifier cell. (Design rule checked by Y. Kwark and K. Wrenner of IBM T. J. Watson Research Center.)

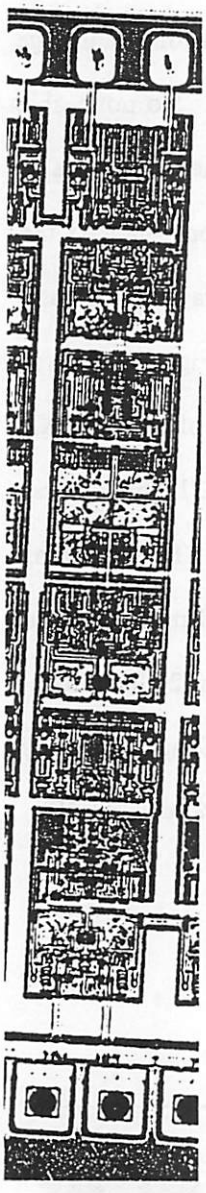

Figure 11-13. Chip photograph of a full receiver cell. Both preamplifier and postamplifier are included. (Design rule checked by Y. Kwark and K. Wrenner of IBM T. J. Watson Research Center.)

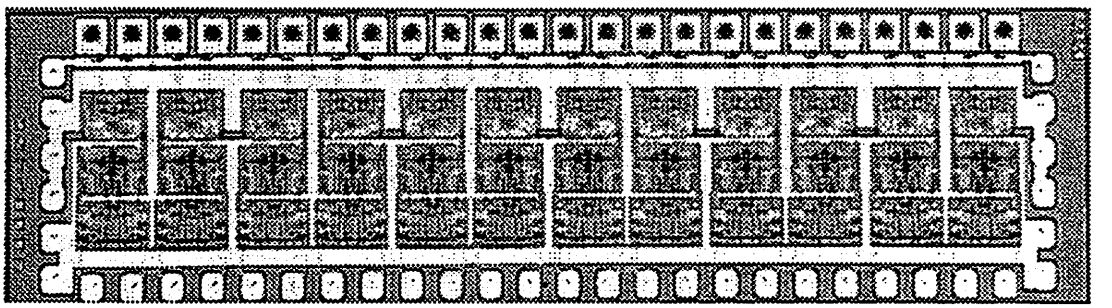

Figure 11-14. Chip photograph of a 12-receiver array. Each receiver has the same circuit as shown in Figure 11-1. (Design rule checked by Y. Kwark and K. Wrenner of IBM T. J. Watson Research Center.)

11.6 Summary

In this chapter, we have described the design and simulation of a monolithically integrated differential receiver using GaAs technology. An Metal-Semiconductor-Metal (MSM) structure is used for the photodetector so that the fabrication process for the photodetector is compatible with the GaAs E/D (Enhancement/Depletion) MESFET technology. Because of the monolithic integration of the photodetector and the receiver, the capacitance of each photodetector and the adjacent channel crosstalk have been greatly reduced. The remaining source of possible inter-channel interference came from the switching noise due to the sharing of the same power supply and ground. As a result of the use of a fully differential structure, we have shown from simulation that the maximum switching noise of the receiver array when all of the receivers are switched simultaneously is less than 0.2% (or less than −40 dB) at 0 dBm light input under ideal conditions.

This receiver is designed for a nominal speed 800 MHz with a sensitivity down to ≤ -23 dBm. The receiver is very insensitive to the extinction ratio of the light input, and can function well even when the extinction ratio is reduced to 2. Furthermore, it has been determined from simulation results that the power consumption is 78 mW for the preamplifier and 170 mW for the postamplifier.

In our simulations, we also verify that the low frequency components of the incoming data stream can pass the receiver without any distortion. We also demonstrate the waveform jitter and

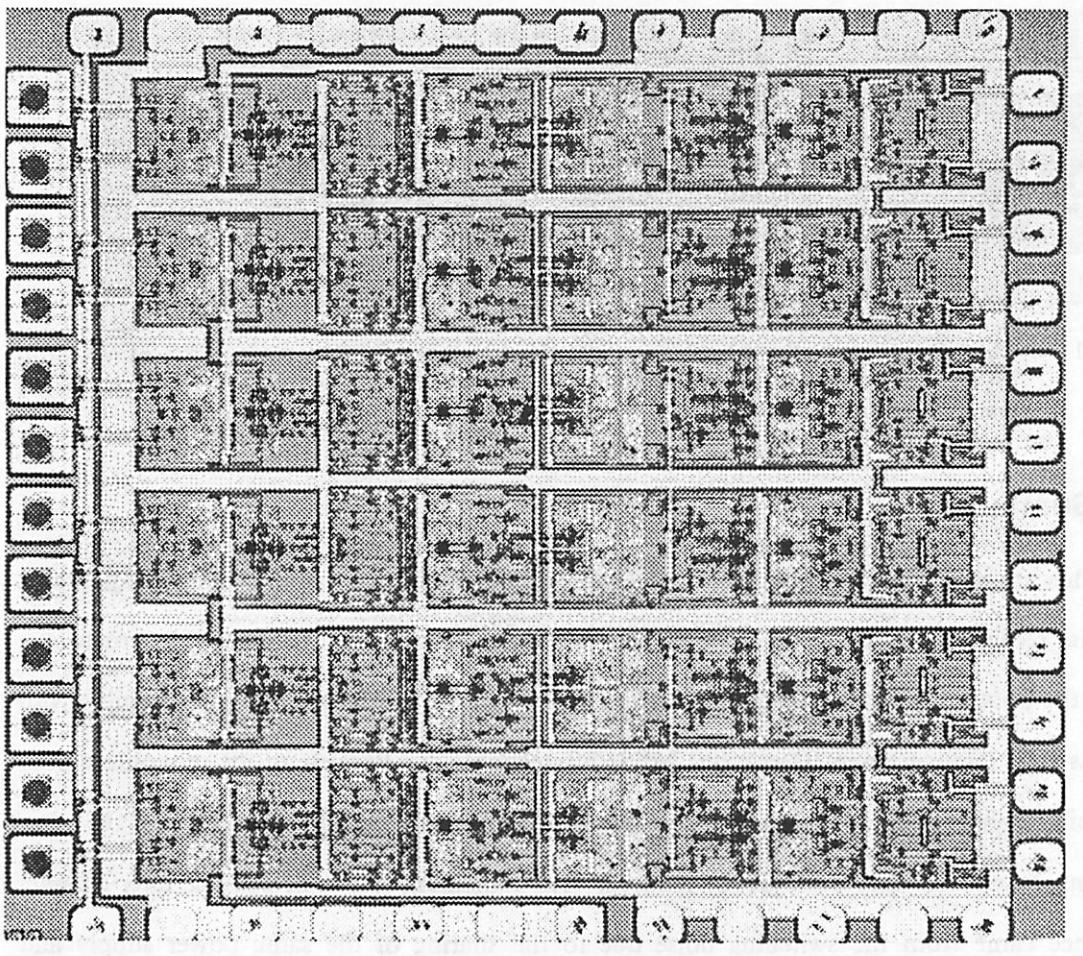

Figure 11-15. Chip photograph of a 6-receiver array. Each receiver has the same circuit as shown in Figure 11-3. (Design rule checked by Y. Kwark and K. Wrenner of IBM T. J. Watson Research Center.)

distortion has been reduced compared with the same receiver structure using a single-ended optical interconnect.

Appendix A. Derivation of Equivalent Circuit For Cascode Configured MESFET

A cascode configured MESFET pair has been shown of Figure 11-5(a), and its equivalent is shown in (b) of the same figure. In this appendix, we compute the equivalent transconductance G_m and output impedance R_d of the whole cascode circuit.

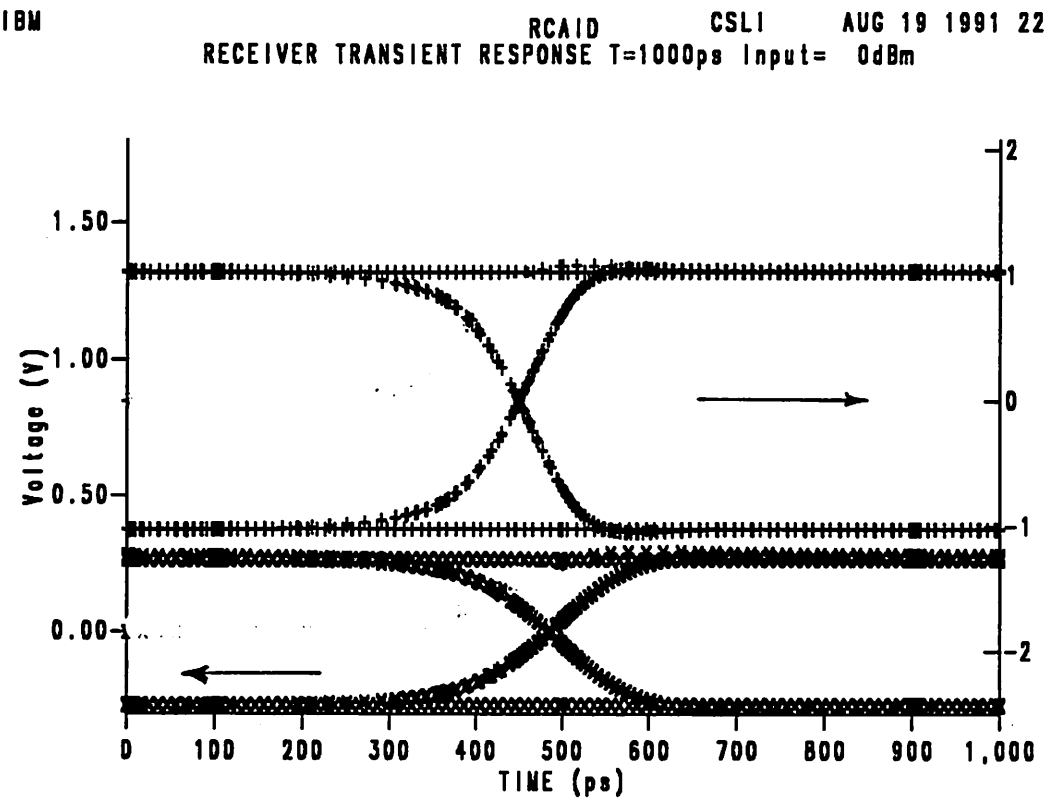

Figure 11-16. Simulated eye pattern of the receiver response. Extinction ratio = 8, T = 1000ps, t_r = 200ps, input light level = 0 dBm. The upper trace uses the Y-axis on the right hand side while the lower trace uses the Y-axis on the left hand side.

In order to compute G_m, we short the output of both Figure 11-5(b) and (c) and equate the output currents. Summing the current at the source node of the second MESFET, we have

$$g_{m1}v_{gs1} = \frac{v_{g2}}{r_{d1}} + j\omega C_{gs2}v_{gs2} + g_{m2}v_{gs2} + \frac{v_{gs2}}{r_{d2}} \tag{11.18}$$

We can thus find the relationship between v_{gs2} and v_{gs1}

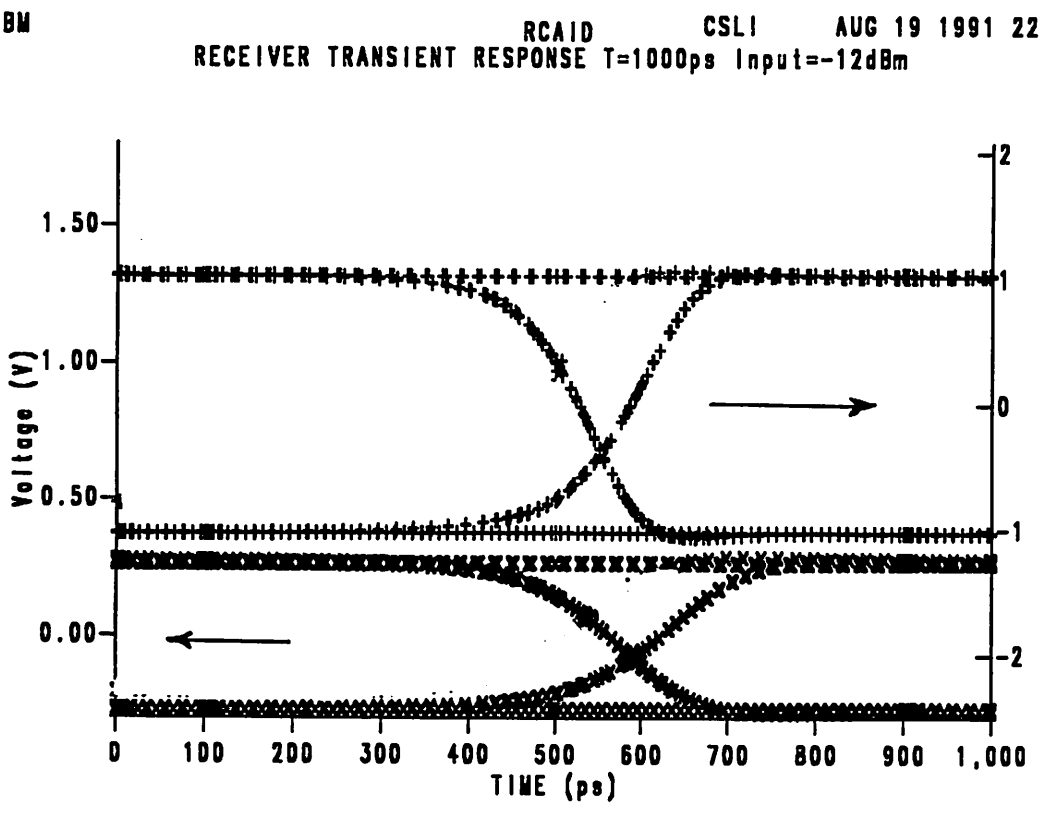

Figure 11-17. Simulated eye pattern of the receiver response. Extinction ratio = 8, T = 1000ps, t_r = 200ps, input light level = −12 dBm. The upper trace uses the Y-axis on the right hand side while the lower trace uses the Y-axis on the left hand side.

$$v_{gs2} = \frac{g_{m1} v_{gs1}}{\frac{1}{r_{d1}} + \frac{1}{r_{d2}} + j\omega C_{gs2} + g_{m2}} \tag{11.19}$$

The output current thus equals

$$i_o = (g_{m2} + \frac{1}{r_{d2}}) v_{gs2}$$

$$= \frac{(g_{m2} + \frac{1}{r_{d2}}) g_{m1} v_{gs1}}{\frac{1}{r_{d1}} + \frac{1}{r_{d2}} + j\omega C_{gs2} + g_{m2}} \tag{11.20}$$

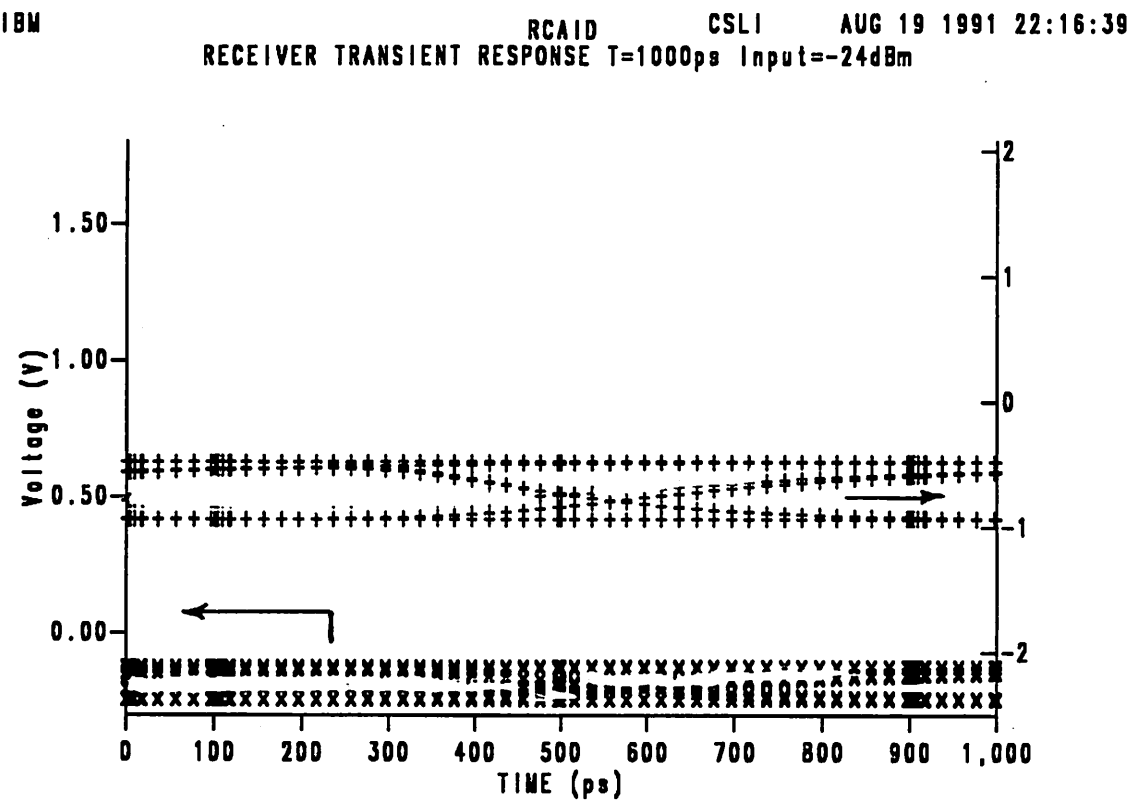

Figure 11-18. Simulated eye pattern of the receiver response. Extinction ratio = 8, T = 1000ps, t_r = 200ps, input light level = −24 dBm. The upper trace uses the Y-axis on the right hand side while the lower trace uses the Y-axis on the left hand side.

Since $i_o = G_m v_{gs1}$, G_m thus equals

$$G_m = \frac{(g_{m2} + \frac{1}{r_{d2}})g_{m1}}{\frac{1}{r_{d1}} + \frac{1}{r_{d2}}\frac{1}{j\omega C_{gs2}} + g_{m2}} = \frac{g_{m1}}{1 + \frac{\frac{1}{r_{d1}} + j\omega C_{gs2}}{g_{m2} + \frac{1}{r_{d2}}}} \tag{11.21}$$

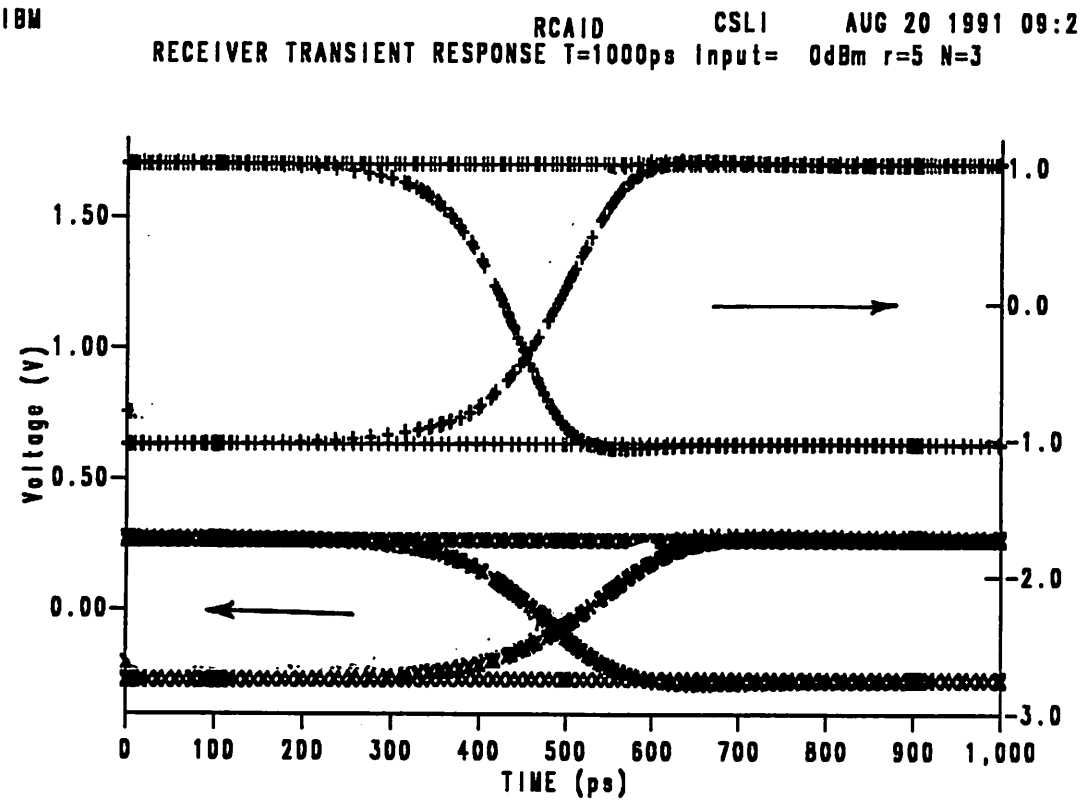

Figure 11-19. Simulated eye pattern of the receiver response. Extinction ratio = 5, T = 1000ps, t_r = 200ps, input light level = 0 dBm. The upper trace uses the Y-axis on the right hand side while the lower trace uses the Y-axis on the left hand side.

Since $g_{m2} \gg 1/r_{d2}$, $1/r_{d1} \ll 1$, and ωC_{gs2} is relatively small over the frequency range we consider ($f \leq 1$ GHz), $G_m = g_{m1}$ in most practical cases.

The output impedance of this cascode configured pair is obtained by applying a voltage source v_x at the output, shorting the input, and measuring the input current i_x from the applied source. By inspection,

$$i_x = \frac{v_x + v_{gs2}}{r_{d2}} + g_{m2} v_{gs2} \tag{11.22}$$

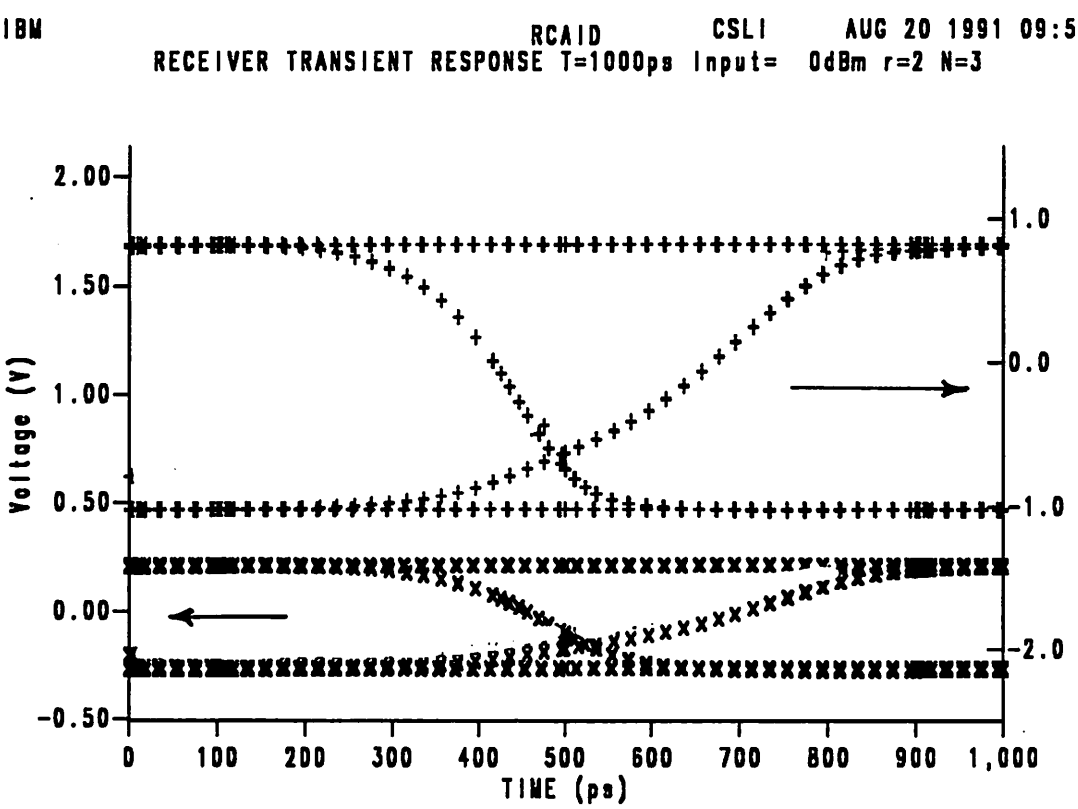

Figure 11-20. Simulated eye pattern of the receiver response. Extinction ratio = 2, T = 1000ps, t_r = 200ps, input light level = 0 dBm. The upper trace uses the Y-axis on the right hand side while the lower trace uses the Y-axis on the left hand side.

and

$$\frac{v_{gs2}}{r_{d1}} + j\omega C v_{gs2} + g_{m2} v_{gs2} + \frac{v_x + v_{gs2}}{r_{d2}} = 0 \tag{11.23}$$

From the second equation, we can solved for v_{gs2} in terms of v_x:

$$v_{gs2} = -\frac{\frac{1}{r_{d2}}}{j\omega C_{gs2} + \frac{1}{r_{d1}} + g_{m2} + \frac{1}{r_{d2}}} v_x \tag{11.24}$$

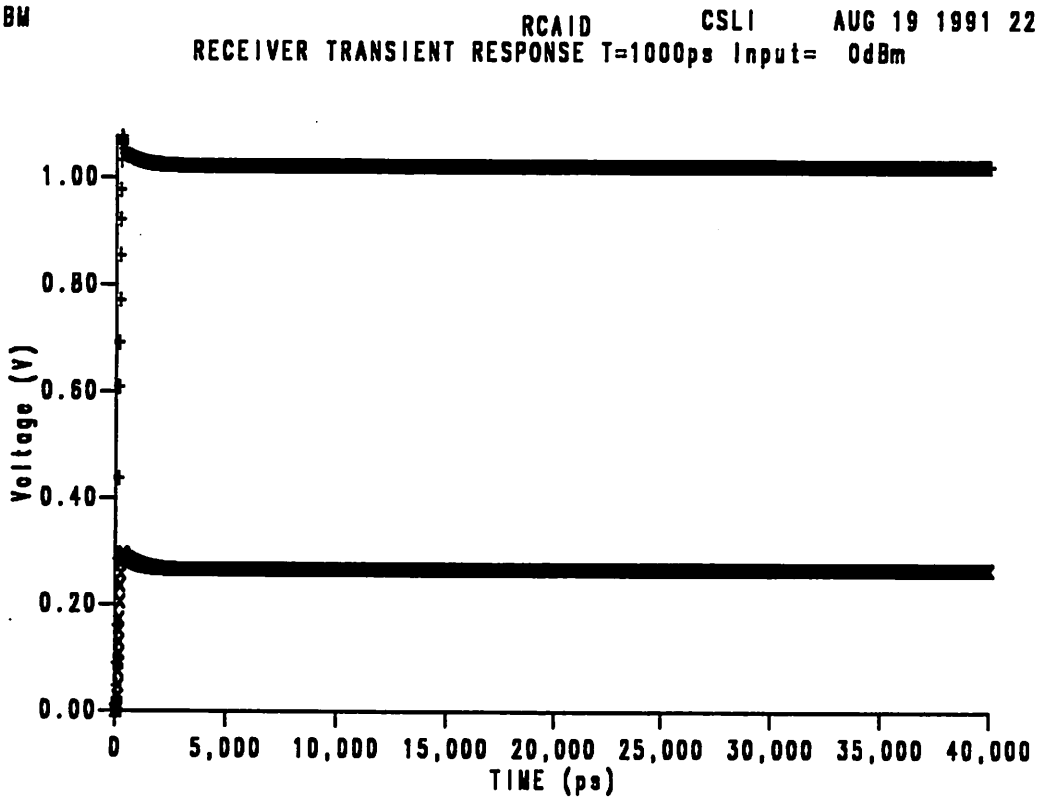

Figure 11-21. Low frequency response of the receiver. Extinction ratio = 8, T = 1000ps, t_r = 200ps, input light level = 0 dBm.

This can be substituted into the first equation, yields

$$\frac{i_x}{v_x} = \frac{1}{r_{d2}} - \frac{1}{r_{d2}} \frac{\frac{1}{r_{d2}} + g_{m2}}{j\omega C_{gs2} + \frac{1}{r_{d1}} + g_{m2} + \frac{1}{r_{d2}}}$$

$$= \frac{1}{r_{d2}} - \frac{\frac{1}{r_{d2}}}{1 + \frac{j\omega C_{gs2} + \frac{1}{r_{d1}}}{g_{m2} + \frac{1}{r_{d2}}}} \qquad (11.25)$$

The output impedance thus equals

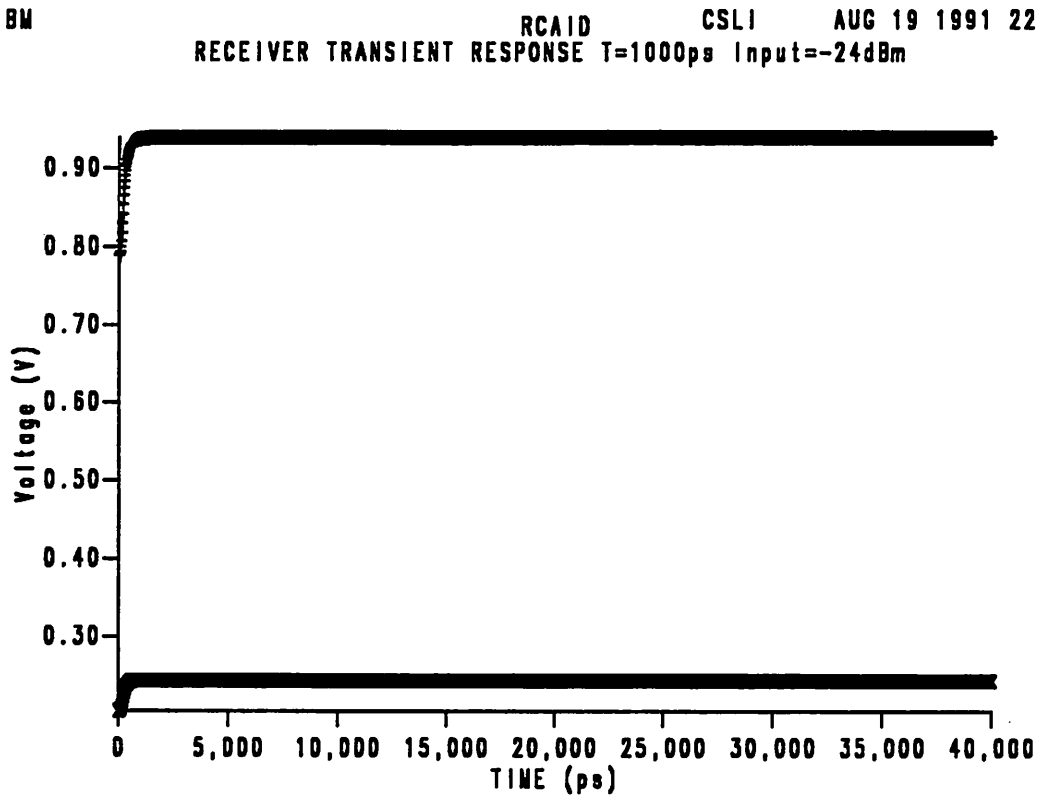

Figure 11-22. Low frequency response of the receiver. Extinction ratio = 8, T = 1000ps, t_r = 200ps, input light level = −24 dBm.

$$Z_d = r_{d2}\left(1 + \frac{g_{m2} + \frac{1}{r_{d2}}}{j\omega C_{gs2} + \frac{1}{r_{d1}}}\right) \tag{11.26}$$

Since $g_{m2} \gg 1/r_{d2}$, and $j\omega C_{gs2}$ could be ignored in the frequency range we are interested, the above equation can be approximated by

$$Z_d \simeq r_{d2}(1 + g_{m2} r_{d1}) \tag{11.27}$$

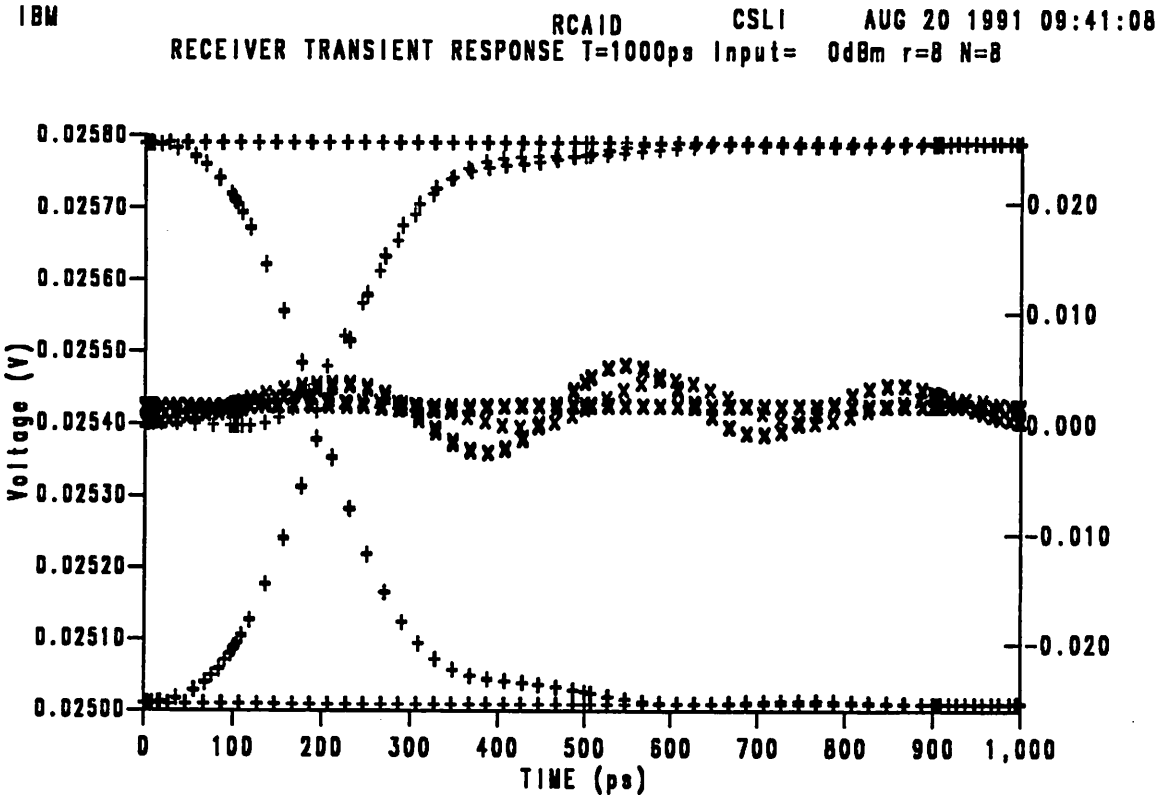

Figure 11-23. Simulated switching noise of a preamp array. Extinction ratio = 8, T = 1000ps, t_r = 200ps, N = 8, input light level = 0 dBm. The center trace, which corresponds to the switching noise of the quiet channel, uses the Y-axis on the left hand side, while the outer trace, which corresponds to the output of an active channel, uses the Y-axis on the right hand side.

Therefore, the output impedance of a cascoded MESFET pair has been *amplified* by $g_{m2}r_{d1}$ as compared to a single common source MESFET amplifier.

Appendix B. Derivation of Equivalent Input Noise for Cascode Configured MESFET

In this appendix, we derive the equivalent input noise voltage and noise current for a cascode configured MESFET pair shown in Figure 11-6. The input noise voltage and current can be found by short circuit and open circuit the input of of Figure 11-6(a) and (b) and equate the output current.

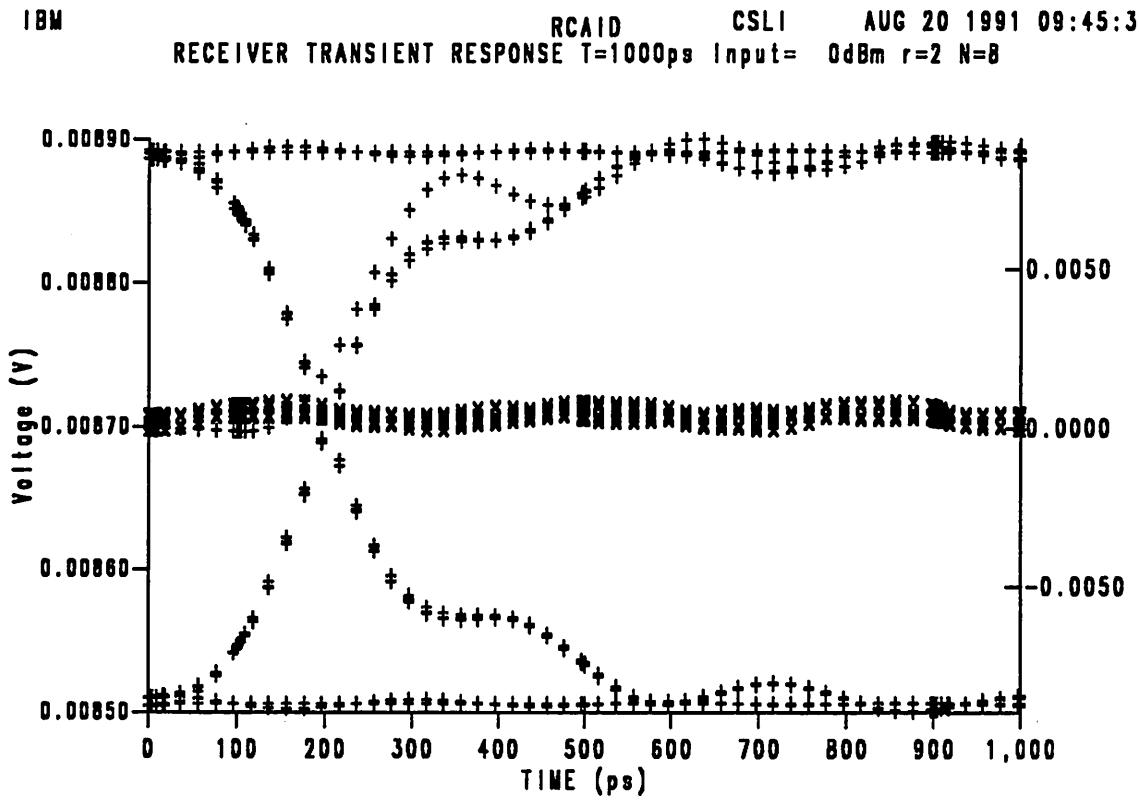

Figure 11-24. Simulated switching noise of a preamp array. Extinction ratio = 2, T = 1000ps, t_r = 200ps, N = 8, input light level = 0 dBm. The center trace, which corresponds to the switching noise of the quiet channel, uses the Y-axis on the left hand side, while the outer trace, which corresponds to the output of an active channel, uses the Y-axis on the right hand side.

We first short circuit the input of both of Figure 11-6(a) and (b), and sum the current flowing into the source node of the second MESFET:

$$-i_{g2} + i_{d1} + \frac{v_{gs2}}{r_{d1}} + j\omega C_{gs2} v_{gs2} + g_{m2} v_{gs2} + \frac{v_{gs2}}{r_{d2}} - i_{d2} = 0 \tag{11.28}$$

We can thus solve v_{gs2} in terms of other parameters:

$$v_{gs2} = \frac{i_{d2} + i_{g2} - i_{d1}}{j\omega C_{gs2} + \frac{1}{r_{d1}} + g_{m2} + \frac{1}{r_{d2}}} \tag{11.29}$$

the output current of (a) is

$$\begin{aligned} i_o &= (g_{m2} + \frac{1}{r_{d2}})v_{gs2} - i_{d2} \\ &= \frac{i_{d2} + i_{g2} - i_{d1}}{1 + \frac{j\omega C_{gs2} + \frac{1}{r_{d1}}}{g_{m2} + \frac{1}{r_{d2}}}} - i_{d2} \\ &= \frac{i_{g2} - i_{d1} - \frac{j\omega C_{gs2} + \frac{1}{r_{d1}}}{g_{m2} + \frac{1}{r_d}} i_{d2}}{1 + \frac{j\omega C_{gs2} + \frac{1}{r_{d1}}}{g_{m2} + \frac{1}{r_{d2}}}} \end{aligned} \tag{11.30}$$

Using the expression of G_m derived in Appendix A., the output current in Figure 11-6(b): is

$$i_o = \frac{g_{m1}}{1 + \frac{\frac{1}{r_{d1}} + j\omega C_{gs2}}{g_{m2} + \frac{1}{r_{d2}}}} v_i \tag{11.31}$$

Equating these two expressions, we can therefore find the equivalent noise voltage v_i

$$v_i = \frac{1}{g_{m1}} (i_{g2} - i_{d1} - \frac{j\omega C_{gs2} + \frac{1}{r_{d1}}}{g_{m2} + \frac{1}{r_{d2}}} i_{d2}) \tag{11.32}$$

The noise spectral density of v_i is

$$v_i^2 = \frac{1}{g_{m1}^2}\left(i_{g2}^2 + i_{d1}^2 + \frac{\omega^2 C_{gs2}^2 + \frac{1}{r_{d1}^2}}{\left(g_{m2} + \frac{1}{r_{d2}}\right)^2} i_{d2}^2\right) \tag{11.33}$$

If we ignore the gate leakage current and assume $g_{m2} \gg \frac{1}{r_{d2}}$, the above expression can be simplified:

$$v_i^2 = \frac{1}{g_{m1}^2}\left[i_{d1}^2 + \left(\frac{\omega^2 C_{gs2}^2}{g_{m2}^2} + \frac{1}{g_{m2}^2 r_{d1}^2}\right) i_{d2}^2\right] \tag{11.34}$$

Since $g_{m2}/\omega C_{gs2}$ can be recognized as the current gain of the second MESFET, the equivalent noise voltage is therefore dominated by i_{d1} at low frequency as i_{d2} is divided by the current gain when it is referred back before the input stage.

Now we open the input circuit, and sum the current flowing into the source node of the second MESFET:

$$-g_{m1}\frac{i_{g1}}{j\omega C_{gs1}} - i_{g2} + i_{d1} + \frac{v_{gs2}}{r_{d1}} + j\omega C_{gs2} v_{gs2} + g_{m2} v_{gs2} + \frac{v_{gs2}}{r_{d2}} - i_{d2} = 0 \tag{11.35}$$

We can thus solve v_{gs2} in terms of other parameters:

$$v_{gs2} = \frac{g_{m1}\frac{i_{g1}}{j\omega C_{gs1}} i_{d2} + i_{g2} - i_{d1}}{j\omega C_{gs2} + \frac{1}{r_{d1}} + g_{m2} + \frac{1}{r_{d2}}} \tag{11.36}$$

the output current of (a) is

$$
\begin{aligned}
i_o &= (g_{m2} + \frac{1}{r_{d2}})v_{gs2} - i_{d2} \\
&= \frac{g_{m1}\dfrac{i_{g1}}{j\omega C_{gs1}} + i_{d2} + i_{g2} - i_{d1}}{1 + \dfrac{j\omega C_{gs2} + \dfrac{1}{r_{d1}}}{g_{m2} + \dfrac{1}{r_{d2}}}} - i_{d2} \\
&= \frac{g_{m1}\dfrac{i_{g1}}{j\omega C_{gs1}} + i_{g2} - i_{d1} - \dfrac{j\omega C_{gs2} + \dfrac{1}{r_{d1}}}{g_{m2} + \dfrac{1}{r_d}} i_{d2}}{1 + \dfrac{j\omega C_{gs2} + \dfrac{1}{r_{d1}}}{g_{m2} + \dfrac{1}{r_{d2}}}}
\end{aligned}
\tag{11.37}
$$

Using the expression of G_m derived in Appendix A., the output current in (b) of Figure 11-6 is

$$
i_o = \frac{\dfrac{g_{m1}}{\dfrac{1}{r_{d1}} + j\omega C_{gs2}}}{1 + \dfrac{j\omega C_{gs2} + \dfrac{1}{r_{d1}}}{g_{m2} + \dfrac{1}{r_{d2}}}} \frac{i_i}{j\omega C_{gs1}} \tag{11.38}
$$

Equating these two expressions, we can therefore find the equivalent noise voltage v_i

$$
i_i = \frac{j\omega C_{gs1}}{g_{m1}} \left(g_{m1} \frac{i_{g1}}{j\omega C_{gs1}} + i_{g2} - i_{d1} - \frac{j\omega C_{gs2} + \dfrac{1}{r_{d1}}}{g_{m2} + \dfrac{1}{r_{d2}}} i_{d2} \right) \tag{11.39}
$$

If we ignore the gate leakage current of the both MESFET's, the equivalent input noise current spectral density thus equals

$$
i_i^2 = \frac{\omega^2 C_{gs1}^2}{g_{m1}^2} \left(i_{d1}^2 + \left(\frac{\omega^2 C_{gs2}}{g_{m2}^2} + \frac{1}{g_{m2}^2 r_{d1}^2} \right) i_{d2}^2 \right) \tag{11.40}
$$

Therefore, the noise current i_{d1} is attenuated by the current gain of the MESFET once while i_{d2} is attenuated by the current gain twice when they are referred to the input.

From the above derivation, we show that the noise coming from the second stage is relatively small compared with the first stage. As a first order approximation, we will ignore the noise component coming from the second stage in the rest of this appendix and the main discussion in Section 3.

In a GaAs MESFET, two major sources contributed to i_d: (1) Thermal noise due to the resistive nature of the channel $4kT\Gamma g_m$, (2) Flicker noise (or $1/f$ noise) $4kT\Gamma g_m f_N/f$ where Γ is a factor which depends on the type of the MESFET while f_N is the noise corner frequency of the flicker noise. The equivalent input noise voltage and current spectral density therefore equals

$$v_i^2 = 4kT\Gamma \frac{1}{g_m}(1 + \frac{f_N}{f}) \tag{11.41}$$

$$i_i^2 = \frac{4\pi^2 f^2 C_{gs1}^2}{g_{m1}^2}(4kT\Gamma g_m(1 + \frac{f_N}{f})) \tag{11.42}$$

Appendix C. Noise Calculation of the Preamplifier

Note that the input equivalent noise voltage and current of the cascode stage are i_c and v_c, respectively, the input equivalent noise voltage and current of the source follower stage are i_{sf} and v_{sf}, respectively, the noise current of the feedback resistor is i_f, and the shot noise is I.

In order to calculate the contribution of the output noise voltage due to v_c, we short circuit all the other voltage noise and open circuit all the current source. Since

$$\frac{v_a + v_{in}}{Z_d} + \frac{v_{in}}{Z_i} = \frac{v_{out} - v_c - v_{in}}{Z_f} \tag{11.43}$$

and $v_{out} = A_V g_m v_{in} Z_L$, the output noise voltage due to v_c thus equals

$$v_{out,vc} = \frac{\frac{1}{Z_d} + \frac{1}{Z_f}}{\frac{1}{Z_f} - \frac{1}{g_m Z_L A_V}\left(\frac{1}{Z_d} + \frac{1}{Z_i} + \frac{1}{Z_f}\right)} v_c \qquad (11.44)$$
$$\simeq \left(1 + \frac{Z_f}{Z_d}\right) v_c$$

assuming $g_m Z_L A_V \gg 1$. We then calculate the contribution due to i_c. Summing the current flowing into the input node of the cascode stage, we have

$$i_c = \frac{v_{in}}{Z_i'} + \frac{v_{in} - v_{out}}{Z_f} \qquad (11.45)$$

where

$$\frac{1}{Z_i'} = \frac{1}{Z_i} + \frac{1}{Z_d} \qquad (11.46)$$

In addition, the relationship between input and output voltage is $v_{out} = A_V g_m v_{in} Z_L$. We can thus solve for v_{in} in terms of v_{out} and substitute into the previous equation:

$$i_c = \frac{v_{out}}{A_V g_m Z_L}\left(\frac{1}{Z_i'} + \frac{1}{Z_f}\right) - \frac{v_{out}}{Z_f} \qquad (11.47)$$

Therefore,the output noise voltage contributed by i_c is

$$v_{out,ic} = \frac{1}{\frac{1}{A_V g_m Z_L}\left(\frac{1}{Z_i'} + \frac{1}{Z_f}\right) - \frac{1}{Z_f}} i_c \qquad (11.48)$$

Assuming $A_V g_m Z_L \gg 1$, this expression can be approximated by $v_{out,ic} = -Z_f i_c$. Similarly, the noise voltage due to I and i_f are, respectively:

$$v_{out,I} = \frac{1}{\frac{1}{A_V g_m Z_L}\left(\frac{1}{Z_i'} + \frac{1}{Z_f}\right) - \frac{1}{Z_f}} I \simeq -Z_f I \tag{11.49}$$

and

$$v_{out,f} = \frac{1}{\frac{1}{A_V g_m Z_L}\left(\frac{1}{Z_i'} + \frac{1}{Z_f}\right) - \frac{1}{Z_f}} i_f \simeq -Z_f i_f \tag{11.50}$$

The output noise voltage contributed by the noise current of the source follower can be found by solving

$$\frac{v_{out} - v_{in}}{Z_f} = \frac{v_{in}}{Z_i'} \tag{11.51}$$

Therefore,

$$v_{in} = \frac{1}{Z_f\left(\frac{1}{Z_i'} + \frac{1}{Z_f}\right)} v_{out} \tag{11.52}$$

On the other hand,

$$v_{out} = A_V(g_m v_{in} + i_{sf}) Z_L \tag{11.53}$$

The output noise voltage contributed by i_{sf} thus equals

$$v_{out,isf} = \frac{A_V Z_L}{1 - \frac{A_V g_m Z_L}{Z_f(\frac{1}{Z_i'} + \frac{1}{Z_f})}} i_{sf} \tag{11.54}$$

Assuming $A_V g_m/(1 + Z_f/Z_i') \gg 1$, the above expression can be approximated by

$$v_{out,isf} = \frac{1}{g_m}(1 + \frac{Z_f}{Z_i'}) i_{sf} \tag{11.55}$$

Similarly, we can find the noise voltage contributed by v_{sf} is

$$v_{out,vsf} = \frac{A_V}{1 - \frac{A_V g_m}{Z_f(\frac{1}{Z_i'} + \frac{1}{Z_f})}} v_{sf} \tag{11.56}$$

Since $A_V g_m/(1 + Z_f/Z_i') \ll 1$ in this case, we can approximate the above expression with $v_{out,vsf} = A_V v_{sf}$. This is usually not surprising because of the circuit has a source follower configuration.

The total noise voltage thus equals

$$v_{out,N} = (1 + \frac{Z_f}{Z_d}) v_c - (i_c + I + i_f) Z_f + \frac{1}{g_m}(1 + \frac{Z_f}{Z_i'}) i_{sf} + v_{sf} \tag{11.57}$$

Using $Z_f = R_f$, $Z_d = 1/j\omega C_d$, $Z_i' = 1/j\omega C_i$, the total noise spectral density is

$$v_{out,N}^2 = (1 + \omega^2 R_f^2 C_d^2) v_c^2 + (i_c^2 + 2eI + i_f^2) R_f^2 + \frac{1}{g_{m1}^2}(1 + \omega^2 R_f^2 C_i^2) i_{sf}^2 + v_{sf}^2 \tag{11.58}$$

Substituting the equivalent input noise voltage and current derived in Appendix B to the previous equation, the total noise spectral density can therefore be computed:

$$\begin{aligned} v_{out,N}^2 &= (1+4\pi^2 f^2 R_f^2 C_d^2)4kT\Gamma\frac{1}{g_{m1}}(1+\frac{f_N}{f}) \\ &+ (\frac{4\pi^2 f^2 C_{gs1}^2}{g_{m1}^2}4kT\Gamma g_{m1}(1+\frac{f_N}{f})+2eI+\frac{4kT}{R_f})R_f^2 \\ &+ \frac{1}{g_{m1}^2}(1+4\pi^2 f^2 R_f^2 C_i^2)(\frac{4\pi^2 f^2 C_{gs5}^2}{g_{m5}^2}4kT\Gamma g_{m5}(1+\frac{f_N}{f})+\frac{4kT}{R_L})+4kT\Gamma\frac{1}{g_{m5}}(1+\frac{f_N}{f}) \end{aligned} \tag{11.59}$$

where g_{m1} and g_{m5} are the transconductance of M1 and M5, respectively, I_{D1} and I_{D5} are the drain current of M1 and M5, respectively, $C_i = C_d + C_{gs1}$, C_{gs1} and C_{gs5} are the gate capacitance of M1 and M5, respectively. Assuming a bandwidth of B, the total noise voltage variance thus equals

$$\begin{aligned} V_{out,N}^2 &= (1+\frac{4}{3}\pi^2 B^2 R_f^2(C_d^2+C_{gs1}^2))B4kT\Gamma\frac{1}{g_{m1}}+(\ln B+2\pi^2 B^2 R_f^2(C_d^2+C_{gs1}^2))\frac{4kT\Gamma f_N}{g_{m1}} \\ &+ (2eI+\frac{4kT}{R_f})R_f^2 B+\frac{1}{g_{m1}^2}(\frac{4\pi^2 BC_{gs5}^2}{3g_{m5}}4kT\Gamma+\frac{16\pi^4 B^3 R_f^2(C_{gs1}+C_d)^2 C_{gs5}^2}{5g_{m5}}4kT\Gamma \\ &+ \frac{2\pi^2 C_{gs5}^2}{g_{m5}^2}4kT\Gamma f_N+\frac{4\pi^4 B^2 R_f^2(C_{gs1}+C_d)^2 C_{gs5}^2}{g_{m5}^2}4kT\Gamma f_N)B^2 \\ &+ \frac{1}{g_{m1}^2}(1+\frac{4}{3}\pi^2 B^2 R_f^2(C_{gs1}+C_d)^2)B\frac{4kT}{R_L}+4kT\Gamma\frac{1}{g_{m5}}(B+f_N\ln B) \end{aligned} \tag{11.60}$$

CHAPTER 12 SUMMARY AND FUTURE WORK

12.1 Summary

We demonstrated in this thesis that using a dense optical interconnect system in a high performance digital system can increase the packaging density and interconnect bandwidth as compared to an existing metal interconnect system. However, using dense optical interconnect in a noisy digital system can introduce crosstalk in both the optical and electrical domains. This thesis has focused on analyzing and solving these problems.

The major results obtained in this thesis are:

- Electrical interference is the dominant noise source in a dense optical interconnect system and limits the high-speed system performance. This interference includes adjacent-channel crosstalk through the parasitic coupling capacitance and inductance contributed by the packaging, as well as through the sharing of a common power supply. A simulation approach has been used to determine the performance degradation due to these interference sources for various transmitter and receiver structures. A fully differential structure is essential for both laser driver and receiver in order to minimize switching noise, and a large driver and receiver array ($\geq$16) can be realized using this differential structure.
- Using a 1-dB power penalty criterion at a bit-error rate of 10^{-15}, the maximum allowable optical crosstalk in a dense single-mode waveguide system cannot exceed -12 dB if the frequency spacing between adjacent waveguide sources or the laser linewidth is much larger than the receiver bandwidth. When the waveguides share the same light source, the maximum allowable crosstalk cannot exceed -30 dB. If -30 dB is the maximum allowable crosstalk, the minimum center-to-center spacing between single-mode waveguides is $\sim$ 11 μm.
- Instead of increasing density in the spatial domain, it is possible to multiplex more than one channel into the same fiber/waveguide by using wavelength division multiplexing (WDM). In this case, the leakage of the optical filter and the chirp of the laser limit the minimum channel spacing that can be achieved. Assuming typical laser and receiver parameters, we show that a

WDM system using OOK and Fabry-Perot filter can achieve 37 GHz channel spacing with each channel transmitting at 2 Gbps.

- Clock distribution is a critical issue for a high-performance digital systems. Large-fanout optical clock distribution can be achieved with a multi-stage tree structure using semiconductor or erbium-doped fiber optical amplifiers. A low skew ($\leq$20 ps) and large fanout ($\geq 10^5$) clock distribution system can be achieved with this multi-stage structure. We have demonstrated a two-stage low-skew distribution system experimentally with an erbium-doped fiber amplifier.
- Using a statistical timing model, we examined the timing requirements of two approaches for designing a synchronous interconnect system: (1) A conservative approach in which the data is not transmitted until the previously transmitted data is received. (2) An aggressive pipelined approach in which the data is transmitted as fast as the interconnect allows. We show that the interconnect delay and the random skew dominate the interconnect cycle time in the conservative approach, while the random timing skew dominates the interconnect cycle time in the aggressive approach. For an interconnect system with 1000 ps propagation delay, the system cycle time increases by 20% and by a factor of three, respectively, for conservative and aggressive approaches as the standard deviation of the random skew increases from 1 ps to 10 ps.

Based on this analysis, a fully differential optical interconnect structure is proposed, analyzed and prototyped in this thesis. A fully differential optical interconnect has the following advantages:

- The latency of the receiver is minimized because this interconnect structure does not require encoding/decoding and serialization/deserialization of the data stream.
- The receiver structure can be simplified because the decision threshold at the output of an interconnect does not depend on the absolute value of the incoming signal. Furthermore, this interconnect architecture is not sensitive to the DC content of the incoming data stream.
- It is less vulnerable to power and ground noise due to the use of a differential structure for both drivers and receivers.

However, this interconnect structure might suffer performance degradation when there is a mismatch between differential channels. It has been determined that a 40% total channel mismatch would result in a 2.2 dB power penalty.

A fully differential driver using an advanced silicon bipolar process and a monolithically integrated receiver array using a GaAs process have also been designed and implemented to verify this fully differential optical interconnect concept. Simulation results indicate that this driver and receiver array are fully functional at a data rate over 1 Gbps with minimal switching noise.

12.2 Future Work

There are a few potential extensions of the work reported in this thesis. These extentions can be categorized into three areas:

- using multi-mode waveguides for dense optical interconnects,
- fault-tolerant interconnect architecture,
- impact of optical interconnects on computer architecture,
- integration of optical interconnects with photonic or electronic switching.

12.2.1 Multi-Mode Waveguide

The analysis of the crosstalk power penalty in Chapter 5 was based on the assumption that single-mode waveguides are used. However, multi-mode waveguides are still widely used for very short distance interconnect due to their simplicity in packaging and their tolerance to alignment error.[43] Therefore, an investigation of the mode coupling between multi-mode waveguides would be of practical interest. This analysis is very complicated because the actual coupling depends on the launching condition from the light source into the waveguides. However, an upper bound of power coupling between waveguides can be obtained by assuming all of the optical power is coupled into the mode which has the largest evanescent field outside of the waveguide.

---

[43] Accuracy of light coupling for a single-mode waveguide has to be within a micron while this accuracy can be relaxed to about 50% to 80% of the diameter of a multi-mode waveguide, depending on the numerical aperture of the waveguide.

Using multi-mode fiber or waveguide also introduces the modal noise problem as described in Chapter 1. Modal noise can be eliminated using a wide-linewidth or small-coherence-length light source, such as:

- Light emitting diode. This is the least expensive light source. But its modulation speed is limited and therefore not suitable for high-speed operation.
- Superluminicent diode. It usually has a similar structure as a laser diode with antireflection coating on both facets to prevent it from lasing. It usually provides much higher power but its cost is comparable to a laser diode.
- Self-pulsating laser. It has already been widely used in commercial electronics, such as CD players, but the modulation speed is limited due to the presence of a self-pulsating frequency.
- Premodulation. In contrast to a self-pulsating laser, which relies on the modification of the laser structure to introduce the self-pulsating phenomenon, the linewidth of the laser can be broadened with premodulation [15]. The premodulation circuitry can be integrated with the laser driver and a very compact packaging of a transmitter array can be achieved.

12.2.2 Fault-Tolerant Interconnect Architecture

Some of the current optoelectronic components such as laser diodes used for an optical interconnect system still have reliability problems. These problems are further aggravated in a dense optical interconnect system because the failure of any single component will bring down the whole system. A fault-tolerant system should therefore be able to survive any single component failure inside the interconnect system. Redundancy can be introduced by using error correcting codes on the data stream across parallel data channels or by replicating crucial components of an interconnect. It may also be possible to achieve this goal through innovative circuit design.

12.2.3 Impact of Optical Interconnects on Computer Architecture

This thesis focused on the point-to-point optical interconnect system for applications at the multi-chip module level, the printed circuit board level, and the backplane level. The basic assumption is to have a direct replacement of each existing metal interconnect that becomes a performance bottleneck with an optical interconnect, so that the computer architecture is not affected.

However, the fact that optical interconnects can offer smaller latency and larger bandwidth also has the potential of impacting the existing computer architecture design.

Most of the existing computer architecture designs introduce a prohibitive penalty for inter-processor communication due to the low bandwidth serial link between processors. This situation exists for a mesh-connected multiprocessor, N-cube, systolic array, and wavefront array [2, 171, 172]. Parallel optical interconnects can significantly increase the bandwidth available between processors and would change the fundamental assumptions for designing future parallel algorithms.

12.2.4 Integration of Optical Interconnect with Electronic or Photonic Switching

As VLSI technology and the RISC computer architecture become mature for central processing units (CPU's), it is apparent that high-speed high-capacity switching is essential for achieving higher performance in general-purpose multi-processor architecture. Switching functions can be integrated with a dense optical interconnect system by either using an electronic switch or a photonic switch. In the first case, the mature electronic circuit or packet switching technology would be combined with the optical interconnect technology described in this thesis to provide a very high bandwidth switching function. In the second case, space division or wavelength division switching can be combined with the optical interconnect technology to provide even higher bandwidth between input and output ports.

Bibliography

[1] K. Hwang and F. A. Briggs, *Chapter 7: Multiprocessor Architecture and Programming, Computer Architecture and Parallel Processing*, McGraw-Hill, NY, 1984.

[2] H. S. Stone, *Chapter 3: Pipeline Design Techniques, High-Performance Computer Architecture*, Addison-Wesley, NY, 1987.

[3] P. T. Greiling, "High-Speed Digital IC Performance Outlook," *IEEE Transactions on Microwave Theory and Techniques*, vol. 35, no. 3, pp. 245-259, March 1987.

[4] P. M. Solomon, "A Comparison of Semiconductor Devices for High-Speed Logic," *Proceeding of the IEEE*, vol. 70, no. 5, pp. 489-509, May 1982.

[5] M. Kokado, M. Yoshida, N. Miyoshi, K. Suzuki, M. Takaoka, N. Tsuzuki, and H. Harada, "A 54000-gate ECL Array with Substrate Power Supply," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1271-1274, Oct. 1989.

[6] M. Ino, M. Togashi, S. Horiguchi, M. Hirayama, and H. Kataoka, "30ps 7.5GHz GaAs MESFET Macrocell Array," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1265-1270, Oct. 1989.

[7] M. Abe, T. Mimura, N. Kobayashi, M. Suzuki, M. Kosugi, M. Nakayama, K. Odani, and I. Hanyu, "Recent Advances in Ultrahigh-Speed HEMT LSI Technology," *IEEE Transactions on Electron Devices*, vol. 36, no. 10, pp. 2021-2031, Oct. 1989.

[8] P. M. Asbeck, M. F. Chang, J. A. Higgins, N. H. Sheng, G. J. Sullivan, and K. Wang, "GaAlAs/GaAs Heterojunction Bipolar Transistors: Issues and Prospects for Application," *IEEE Transactions on Electron Devices*, vol. 36, no. 10, pp. 2032-2042, Oct. 1989.

[9] Y. Hatano, S. Yano, H. Mori, H. Yamada, M. Hirano, and U. Kawabe, "A 4-bit Josephson Data Processor Chip," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1312-1316, Oct. 1989.

[10] D. M. Carlson, D. C. Sullivan, R. E. Bach, and D. R. Resnick, "The ETA10 Liquid-Nitrogen-Cooled Supercomputer System," *IEEE Transactions of Electron Devices*, vol. 36, no. 8, pp. 1404-1413, Aug. 1989.

[11] R. R. Tummala, R. W. Keyes, W. Grobman, and S. Kapur, "Thin Film Packaging," *Microelectronics Packaging Handbook*, Van Nostrand Reinhold, New York, 1989.

[12] G. A. Katopis, "Delta-I Noise Specification for a High-Performance Computing Machine," *Proceedings of the IEEE*, vol. 73, no. 9, pp. 1405-1415, Sept. 1985.

[13] R. L. Veghte and C. A. Balanis, "Dispersion of Transient Signals in Microstrip Transmission Lines," *IEEE Transactions on Microwave Theory and Technique*, vol. 34, no. 12, pp. 1427-1436, Dec. 1986.

[14] R. E. Epworth, "The Phenomenon of Modal Noise in Analog and Digital Optical Fiber Systems," *Proc. of 4th ECOC in Genova,*, pp. 492-501, 1978.

[15] R. W. Huegli and C. M. Olsen, "Elimination of Modal Noise Bit-Error-Rate Floors by Strong Stimulation of the On-Level Relaxation Oscillations," *IBM Research Report RC 16675*, IBM T. J. Watson Research Center, March 1991.

[16] J. Gimlett and N. K. Cheung, "Effects of Phase-to-Intensity Noise Conversion by Multiple Reflections on Gigabit-per-Second DFB Laser Transmission Systems," *IEEE Journal of Lightwave Technology*, vol. 7, no. 6, pp. 888-895,, 1989.

[17] G. Arjavalingam and B. Rubin, "Electrical Considerations for Interconnections Inside a Computer," *Proc. SPIE*, vol. 991, pp. 12-21, 1988.

[18] J. W. Goodman, F. I. Leonberger, S. Kung, and R. A. Athale, "Optical Interconnections for VLSI Systems," *Proceedings of the IEEE*, vol. 72, pp. 850-866., 1984.

[19] R. K. Kostuk, J. W. Goodman, and L. Hesselink, "Optical Imaging Applied to Microeletronic Chip-to-Chip Interconnections," *Applied Optics*, vol. 24, pp. 2851-2858, 1985.

[20] L. D. Hutcheson, P. Haugen, and A. Husain, "Optical Interconnects Replace Hardwire," *IEEE Spectrum*, pp. 30-35, March 1987.

[21] B. O. Kahle and E. C. Parish, "Optical Interconnects for Interprocessor Communications in the Connection Machine," *Proc. ICCD*, pp. 58-61, 1989.

[22] D. H. Hartman, G. R. Lalk, and T. C. Banwell, "Board Level High Speed Photonic Interconnections: Recent Technology Developments," *Proc. SPIE*, vol. 994, pp. 57-64, 1988.

[23] D. H. Hartman, G. R. Lalk, J. W. Howse, and R. R. Krchnavek, "Radiant Cured Polymer Optical Waveguides on Printed Circuit Boards for Photonic Interconnection Use," *Applied Optics*, vol. 28, no. 1, pp. 40-47, Jan. 1989.

[24] Y. Yamada, T. Miya, M. Kobayashi, S. Sumida, and T. Miyashita, "Optical Interconnections Using Silica-Based Waveguide on Si substrate," *Proc. SPIE*, vol. 991, pp. 4-11, 1988.

[25] S. K. Ho and S. K. Mullick, "Analysis of Transmission Lines on Integrated-Circuit Chips," *IEEE Journal of Solid-State Circuits*, vol. 2, no. 4, pp. 201-208, Dec. 1967.

[26] H. Guckel, P. A. Brennan, and I. Palocz, "A Parallel-Plate Waveguide Approach to Microminiaturized, Planar Transmission Lines for Integrated Circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 15, no. 8, pp. 468-477, August 1967.

[27] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of Microstrip Line on Si-," *IEEE Transactions on Microwave Theory and Techniques*, vol. 19, no. 11, pp. 869-881, November 1971.

[28] H. Hasegawa and S. Seki, "Analysis of Interconnection Delay on Very High-Speed LSI/VLSI Chips Using an MIS Microstrip Line Model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 32, no. 12, Dec. 1984.

[29] S. Seki and H. Hasegawa, "Analysis of Crosstalk in Very High-Speed LSI/VLSI's Using a Coupled Multiconductor MIS Microstrip Line Model," *IEEE Transactions of Microwave Theory and Techniques*, vol. 32, no. 12, pp. 1715-1720, Dec 1984.

[30] E. G. Farr, C. H. Chan, and R. Mittra, "A Frequency-Dependent Coupled-Mode Analysis of Multiconductor Microstrip Lines with Application to VLSI Interconnection Problems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 34, no. 2, pp. 307-310, Feb 1986.

[31] R. A. Lawton and W. T. Anderson, "Two-Layer Dielectric Microstrip Line Structure: on Si and GaAs on Si: Modeling and Measurement," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 4, pp. 785-789, April 1988.

[32] K. W. Goossen and R. B. Hammond, "Modeling of Picosecond Pulse Propagation in Microstrip Interconnections on Integrated Circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 3, pp. 469-478, March 1989.

[33] J. F. Whitaker, T. B. Norris, G. Mourou, and T. Y. Hsiang, "Pulse Dispersion and Shaping in Microstrip Lines," *IEEE Transactions on Microwave Theory and Techniques*, vol. 35, no. 1, pp. 41-47, Jan 1987.

[34] K. C. Gupta, R. Garg, and I. J. Bahl, *Microstrip Discontinuities, in Microstrip Lines and Slotlines*, Dedham, Massachusetts: Artech House, pp. 140-148, 1979.

[35] C. J. Stanchan and B. M. Macdonald, "Electrical Characterization of Packages for High-Speed Integrated Circuits," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 8, no. 4, pp. 468-473, December 1985.

[36] H. A. Beha and N. Raver, "Electrical Characteristics of a Superconducting High-Speed Computer Package," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 8, no. 3, pp. 374-385, Sept. 1985.

[37] J. Hauenschild and H. Rein, "Influence of Transmission-Line Interconnections Between Gigabit-per-Second IC's on Time Jitter and Instabilities," *Journal of Solid-State Circuit*, vol. 25, no. 3, pp. 763-766, June 1990.

[38] A. J. Rainal, "Computing Inductive Noise of Chip Package," *Bell System Technical Journal*, vol. 63, no. 1, Jan. 1984.

[39] A. F. Champernowne, L. B. Bushard, J. T. Rusterholz, and J. R. Schomburg, "Latch-to-Latch Timing Rules," *IEEE Trans. on Computers*, vol. 39, no. 6, pp. 798-808, June 1990.

[40] D. G. Messerschmitt, "Synchronization in Digital System Design," *IEEE Trans. on Selected Areas in Comm.*, vol. 8, no. 8, pp. 1404-1419, Oct. 1990.

[41] J. P. Fishburn, "Clock Skew Optimization," *IEEE Trans. on Computers*, vol. 39, no. 7, pp. 945-951, July 1990.

[42] R. L. Khalil, "Clock Skew Analysis for Si and GaAs Receivers in Optical Clock Distribution Systems," *Proc. SPIE*, vol. 1178 Optical Interconnects in the Computer Environment, pp. 171-176, 1989.

[43] R. L. Khalil, L. R. McAdams, and J. W. Goodman, "Optical Clock Distribution for High Speed Computers," *Proc. SPIE*, vol. 991, pp. 32-41, 1988.

[44] S. D. Kugelmass and K. Steiglitz, "An Upper Bound on Expected Clock Skew in Synchronous Systems," *IEEE Transactions on Computers*, vol. 39, no. 6, pp. 798-808, June 1990.

[45] E. G. Chor, A. Brunnschweiler, and P. Ashburn, "A Propagation-Delay Expression and its Application to the Optimization of Polysilicon Emitter ECL processes," *IEEE Journal of Solid-State Circuits*, vol. 23, pp. 251-259, 1988.

[46] W. Fang, "Accurate Analytical Delay Expressions for ECL and CML Circuits and Their Applications to Optimizing High-Speed Bipolar Circuits," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 2, pp. 572-583, April 1990.

[47] R. V. Hogg and A. T. Craig, *Introduction to Mathematical Statistics (4th e.d.)*, New York: Macmillan, 1978.

[48] A. L. Fisher and H. T. Kung, "Synchronizing large VLSI processor arrays," *IEEE Trans. on Computers*, vol. 34, pp. 734-740,, August 1985.

[49] E. E. Davidson and M. Technology, "Electrical Design of a High Speed Computer Packaging System," *IEEE Transactions on Components Hybrids, and*, vol. 6, no. 3, pp. 272-282, Sept. 1983.

[50] H. B. Bakoglu, "Chapter 8: Clocking of High-Speed Systems, in," *Circuits, Interconnections, and Packaging for VLSI*, Addison-Wesley, Reading Massachusetts, 1990.

[51] C. M. Li, "Optimal Design of High-Speed Synchronous Interconnections: A Comparison of Optical and Electrical Approaches," *Research Report, RC 14898*, IBM T. J. Watson Research Center, Sept. 1989.

[52] D. H. Hartman, P. J. Delfyett, and S. Z. Ahmed, "Optical Clock Distribution Using a Mode-Locked Semiconductor Laser Diode System," *Proc. OFC'91 Technical Digest*, p. 210, Feb 1991.

[53] N. A. Olsson, "Lightwave Systems with Optical Amplifiers," *IEEE Journal of Lightwave Technology*, vol. 7, no. 7, pp. 1071-1082, 1989.

[54] M. L. Dakss and W. J. Miniscalco, "Fundamental Limits on Amplifier Performance at 1.3," *Photonic Technology Letters*, vol. 2, no. 9, pp. 647-649, Sept. 1990.

[55] R. Muller, *Chapter 7: Bipolar Transistors: Limitations and Models, in, Device Electronics for Integrated Circuits*, Wiley, New York, 1986.

[56] R. Reimann and H. Rein, "Bipolar High-Gain Limiting Amplifier IC for Optical Fiber Receivers Operating up to 4 Gbit/s," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 4, pp. 504-511, Aug. 1987.

[57] L. Kleeman, "The Jitter Model for Metastability and Its Applications to Redundant Synchronizers," *IEEE Transactions on Computers*, vol. 39, no. 7, pp. 930-942, July 1990.

[58] R. Ramaswami and P. Humblet, "Amplifier Induced Crosstalk in Multichannel Optical Networks," *IEEE Journal of Lightwave Technology*, vol. 8, no. 12, pp. 1882-1896,, Dec. 1990.

[59] T. Saitoh, "Pulse Energy Gain Saturation in Subpico- and Picosecond Pulse Amplification by a Traveling-Wave Semiconductor Laser Amplifier," *Photonics Technology Letters*, vol. 1, no. 10, pp. 297-299, Oct. 1989.

[60] J. Gowar, *Chapter 14: The Receiver Amplifier, Optical Communication Systems*, Prentice-Hall: NJ, 1984.

[61] J. Gowar, *Chapter 13: Avalanche Photodetectors, Optical Communication Systems*, Prentice-Hall, 1984.

[62] S. Stutius and W. Streifer, "Silicon nitride films on silicon for optical waveguides," *Applied Optics*, vol. 6, no. 12, pp. 3218-3222, 1977.

[63] B. L. Booth, "Low Loss Channel Waveguides in Polymers," *IEEE Journal of Lightwave Technology*, vol. 7, no. 10, pp. 1445-1453, Oct. 1989.

[64] J. M. Trewhella, "Polymeric Optical Waveguides," *Proc. SPIE*, vol. 1177, pp. 379-386, 1989.

[65] M. Dagenais, R. Leheny, H. Temkin, and P. Bhattacharya, "Application and Challenges of OEIC Technology: A Report on the 1989 Hilton Head Workshop,," *IEEE Journal of Lightwave Technology*, vol. 8, no. 6, pp. 846-862, 1990.

[66] W. K. Burns, "Normal Mode Analysis of Waveguide Devices. Part I: Theory," *IEEE Journal of Lightwave Technology*, vol. 6, no. 6, pp. 1051-1057, 1988.

[67] W. K. Burns, "Normal Mode Analysis of Waveguide Devices. Part II Output and Crosstalk," *Journal of Lightwave Technology*, vol. 6, no. 6, pp. 1058-1068, 1988.

[68] N. Dagli and C. G. Fonstad, "Universal Design Curves for Rib Waveguides," *IEEE Journal of Lightwave Technology*, vol. 6, no. 6., pp. 1136-1145, 1988.

[69] A. Hardy and W. Streifer, "Couple Mode Theory of Parallel Waveguides," *IEEE Journal of Lightwave Technology*, vol. 3, no. 5, pp. 1135-1146, 1985.

[70] A. Hardy and W. Streifer, "Coupled Modes of Multiwaveguides Systems and Phased Arrays," *IEEE Journal of Lightwave Technology*, vol. 4, no. 1, pp. 90-99, 1986.

[84] P. A. Humblet and W. M. Hamdy, "Crosstalk Analysis and Filter Optimization for Single- and Double-Cavity Fabry-Perot Filters," *IEEE Journal of Selective Area in Communications*, vol. 8, no. 6, Aug. 1990.

[85] G. L. Carlolaro, "Error Probability in Digital Fiber Optical Communication," *IEEE Transactions on Information Theory*, vol. 24, pp. 213-221, March 1978.

[86] B. E. Saleh and M. I. Irshid, "Coherence and Intersymbol Interference in Digital Fiber Optic Communication Systems," *IEEE Journal of Quantum Electronics*, vol. 18,, no. 6, pp. 944-951., 1982.

[87] S. D. Personik, "Receiver Design for Digital Fiber Optic Communication Systems," *Bell System Technical Journal*, vol. 52, pp. 843-886, July-Aug 1973.

[88] S. Oshita, "Chernoff Bound of Optical System with Intersymbol Interference," *Proceeding International Conference on Communication*, vol. 1, pp. Boston, MA., June 10-14 1979.

[89] J. W. Matthews, "Sharp Error Bounds for Intersymbol Interference," *IEEE Transaction on Information Theory*, vol. 19, pp. 440-447, July 1973.

[90] K. Yao and R. M. Tobin, "Moment Space Upper and Lower Error Bounds for Digital Systems with Intersymbol Interference," *IEEE Transactions on Information Theory*, vol. 22, pp. 65-74, Jan. 1976.

[91] P. P. Bohn and S. K. Das, "Return Loss Requirements for Optical Duplex Transmission," *IEEE Journal of Lightwave Technology*, vol. 5, no. 2, pp. 243-254, Feb. 1987.

[92] P. R. Trischitta and E. L. Varima, *Chapter 4: The Effect of Jitter on Transmission Quality, Jitter*, Artech House, Norwood, MA, 1988.

[93] D. Welford, "A Rate Equation analysis for the frequency chirp to modulated power ratio of a semiconductor diode laser," *IEEE Journal of Quantum Electronics*, vol. 21, no. 11, pp. 1749-1751, Nov. 1985.

[94] T. L. Koch and R. A. Linke, "Effect of nonlinear gain reduction on semiconductor laser wavelength chirping," *Applied Physics Letters*, vol. 48, no. 10, pp. 613-615, March 1986.

[95] T. L. Koch and J. E. Bowers, "Nature of wavelength chirping in directly modulated semiconductor lasers," *Electronic Letters*, vol. 20, no. 25/26, pp. 1038-1040, Dec. 6 1984.

[96] Y. Sasai, J. Ohya, and M. Ogura, "Spectral Linewidth and Resonant Frequency Characteristics of InGaAsP/InP Multiquantum Well Lasers," *IEEE Journal of Quantum Electronics*, vol. 25, no. 4, April 1989.

[97] B. Wedding, "Reduction of bit error rate in high speed optical transmission systems due to optimized eletrical drive pulse shaping," *Proc. European Conf. Commun.*, pp. 187-190, Brighton, U.K., Sept. 11-15 1988.

[98] G. Forsythe, M. Malcolm, C. Moler, and J. M. Vaughan, *Computer Methods for Mathematical Computations Chapter 3: The Plane Fabry-Perot Interferometer, The Fabry-Perot Interferometer*, Adam Hilger, Philadephia, 1989.

[99] T. M. Shen and P. Agrawal, "Pulse-Shape Effects on Frequency Chirping in Single-Frequency Semiconductor Lasers Under Current Modulation," *IEEE Journal of Lightwave Technology*, vol. 4, no. 5, pp. 497-503, May 1986.

[100] A. E. Willner, I. P. Kaminow, M. Kuznetsov, J. Stone, and L. W. Stulz, "1.2 Gb/s Closely-Spaced FDMA-FSK Direct-Detection Star Network," *IEEE Photonics Technology Letters*, vol. 2, no. 3, pp. 223-226, March 1990.

[101] A. E. Willner, "Simplified Model of an FSK-to-ASK Direct-Detection System Using a Fabry-Perot Demodulator," *IEEE Photonics Technology Letters*, vol. 2, no. 5, pp. 363-366, May 1990.

[102] D. Marcuse, "Computer Simulation of FSK Laser Spectra and of FSK-to-ASK Conversion," *IEEE Journal of Lightwave Technology*, vol. 8, no. 7, pp. 1110-1122, July 1990.

[103] A. R. Chraplyvy, R. W. Tkach, A. H. Gnauck, B. L. Kasper, and R. M. Derosier, "8 Gbit/s FSK Modulation of DFB Lasers with Optical Demodulator," *Electronic Letters*, vol. 25, no. 5, pp. 319-321, March 1989.

[104] R. S. Vodhanel, A. F. Elrefaie, R. E. Wagner, M. Z. Iqbal, J. L. Gimlett, and S. Tsuji, "Ten-to-Twenty Gigabit-per-Second Modulation Performance of 1.5-μm Distributed Feedback Lasers for Frequency-Shift-Keying System," *IEEE Journal of Lightwave Technology*, vol. 7, no. 10,, pp. 1454-1460, October 1989.

[105] J. P. Ziel, R. A. Logan, and R. M. Mikulyak, "A Closely Spaced (50 μm) Array of 16 Individually Addressable Buried Heterostructure GaAs Lasers," *Applied Physics Letters*, no. 41, p. 9, 1982.

[106] P. P. Deimel, J. Cheng, S. R. Forrest, S. J. Walker, R. Hu, R. Huntington, R. C. Miller, J. R. Potopowicz, D. D. Roccassecca, and C. W. Seabury, "Electrical and Optical Integration of a Monolithic 1 x 12 array of InGaAsP/InP ($\lambda = 1.3\mu$m) Light Emitting Diodes," *Journal of Lightwave Technology*, vol. 3, 1985.

[107] D. Botez, J. C. Connolly, D. B. Gilbert, M. G. Harvey, and M. Ettenberg, "High-Power Individually Addressable Monolithic Array of Constricted Double Heterojunction Large-Optical-Cavity Lasers," *Applied Physics Letters*, no. 41, 1982.

[108] L. A. Koszi, B. P. Segner, H. Temkin, W. C. Dautremont-Smith, and D. T. Huo, "1.5 μm InP/GaInAsP Linear Laser Array with Twelve Individually Addressable Elements," *Electronic Letters*, vol. 24, no. 4, pp. 217-219, 1988.

[109] L. A. Koszi, H. Temkin, B. H. Chin, S. G. Napholtz, and B. P. Segner, "Fabrication and Performance of an InP/InGaAsP monolithic 12 x 12 element matrixed LED array," *Electronic Letters*, no. 23, pp. 284-286, 1987.

[110] D. L. McDaniel Jr., J. G. McInerney, M. Y. Raja, C. F. Schaus, and S. R. Brueck, "Vertical Cavity Surface-Emitting Semiconductor Laser with CW Injection Laser Pumping," *IEEE Photonic Technology Letters*, vol. 2, no. 3, March 1990.

[111] R. S. Geels, S. W. Corzine, J. W. Scott, D. B. Young, and L. A. Coldren, "Low Threshold Planarized Vertical-Cavity Surface Emitting Lasers," *IEEE Photonic Technology Letters*, vol. 2, no. 4, April 1990.

[112] Y. H. Lee, B. Tell, K. Brown-Goebeler, J. L. Jewell, C. A. Burrus, and J. M. Hove, "Characteristics of Top-Surface-Emitting GaAs Quantum-Well Lasers," *IEEE Photonic Technology Letters*, vol. 2, no. 9, Sept. 1990.

[113] J. L. Jewell, Y. H. Lee, A. Scherer, S. L. McCall, N. A. Olsson, J. P. Harbison, and L. T. Florez, "Surface-Emitting Microlasers for Photonic Switching and Interchip Connections," *Optical Engineering*, vol. 29, no. 3, March 1990.

[114] M. Uhle, "The Influence of Source Impedance on the Electrooptical Switching Behavior of LED's," *IEEE Transactions on Electron Devices*, vol. 23, pp. 438-441, 1976.

[115] R. Olshnasky and D. Fye, "Reduction of Dynamic Linewidth in Single-Frequency Semiconductor Lasers," *Electronic Letters*, no. 20, pp. 928-929, 1984.

[116] L. Bickers and L. D. Westbrook, "Reduction of Laser Chirp in 1.5 μm DFB Lasers by modulation pulse shaping," *Electronic Letters*, no. 21, pp. 103-104, 1985.

[117] M. A. Karr, F. S. Chen, and P. W. Shumate, "Output Power Stability of GaAlAs Laser transmitter Using an Optical Tap for Feedback Control," *Applied Optics*, no. 18, pp. 1262-1265, 1979.

[118] P. W. Shumate, F. S. Chen, and P. W. Dorman, "GaAlAs Laser Transmitter for Lighwave Transmission Systems," *Bell System Technical Journal*, vol. 57, pp. 1823-1836, 1978.

[119] D. W. Smith and M. R. Matthews, "Laser Transmitter Design for Optical Fiber Systems," *IEEE Journal of Selective Area Comminications*, pp. 515-523, 1983.

[120] R. G. Schwatz and B. A. Wooley, "Stabilized Biasing of Semiconductor Lasers," *Bell System Technical Journal*, vol. 62, pp. 1923-1936, 1983.

[121] O. Wada, H. Nobuhara, T. Sanada, M. Kuno, M. Makiuchi, T. Fujii, and T. Sakurai, "Optoelectronic Integrated Four Channel Transmitter Array Incorporating AlGaAs/GaAs Quantum Well Lasers," *IEEE Journal of Lightwave Technology*, vol. 7, no. 1, pp. 186-197, Jan. 1989.

[122] K. Kaede, T. Uji, T. Nagahori, T. Suzaki, T. Torikai, J. Hayashi, I. Watanabe, M. Itoh, H. Honmou, and M. Shikada, "12-Channel Parallel Optical-Fiber Transmission Using a Low-Drive Current 1.3-μm LED Array and a p-i-n PD Array," *IEEE Journal of Lightwave Technology*, pp. 883-888, June 1990.

[123] N. Yamanaka, M. Sasaki, S. Kikuchi, T. Takada, and M. Idda, "A Gigabit-Rate Five-Highway GaAs OE-LSI Chipset for High-Speed Optical Interconnections Between Modules or VLSI's," *IEEE Journal of Lightwave Technology*, vol. 9, no. 5, June 1991.

[124] K. P. Jackson, C. Harder, P. Buchmann, and K. Datwyler, "High-Speed Characterization of a Monolithically Integrated GaAs-AlGaAs Quantum-Well Laser-Detector," *IEEE Photonic Technology Letters*, vol. 2, no. 11, Nov. 1990.

[125] M. G. Brown, D. R. Hu, D. R. Kaplan, Y. Ota, C. W. Seabury, M. A. Washington, E. E. Becker, J. G. Johnson, M. Koza, and J. R. Potopowicz, "Monolithically Integrated 1 x 12 Array of Planar InGaAs/InP Photodiodes," *IEEE Journal of Lightwave Technology*, vol. 4, no. 3, pp. 283-287, March 1986.

[126] J. Wieland and H. Melchior, "Optical Receivers in ECL for 1GHz Parallel Links," *SPIE Proceedings of International Symposium on Advances in Interconnection and Packaging*, vol. 1389, pp. 659-664, 1990.

[127] L. Figueroa and C. W. Slayman, "A Novel Heterostructure Interdigital Photodetector (HIP) with Picosecond Optical Response," *IEEE Electron Device Letters*, vol. 2, no. 8, pp. 208-210, Aug. 1981.

[128] W. Roth, H. Schumacher, J. Kluge, H. J. Geelen, and H. Beneking, "The DSI Diode - A Fast Large-Area Optoelectronic Detector," *IEEE Transactions on Electron Devices*, no. 6, pp. 1034-1036, June 1985.

[129] M. Ito and O. Wada, "Low Dark Current GaAs Metal-Semiconductor-Metal (MSM) Photodiodes Using WSIx Contacts," *IEEE Journal of Quantum Electronics*, vol. 22, no. 7, pp. 1073-1077, July 1986.

[130] W. C. Koscielniak, R. M. Kolbas, and M. A. Littlejohn, "Performance of a Near-Infrared GaAs Metal-Semiconductor-Metal (MSM) Photodetector with Islands," *IEEE Electron Device Letters*, vol. 9, no. 9, pp. 485-487, 1988.

[131] B. J. Van Zeghbroeck, W. Patrick, J. Halbout, and P. Vettiger, "105 GHz Bandwidth Metal-Semiconductor-Metal Photodiodes," *IEEE Electron Device Letters*, vol. 9, no. 10, pp. 527-529, Oct. 1988.

[132] H. Schumacher, H. P. Leblanc, J. Soole, and R. Bhat, "An Investigation of the Optoelectronic Response of GaAs/InGaAs MSM Photodetectors," *IEEE Electron Device Letters*, vol. 9, no. 11, pp. 607-609, Nov. 1988.

[133] O. Wada, H. Hamaguchi, L. L. Beller, and C. Y. Boisrobert, "Noise Characteristics of GaAs Metal-Semiconductor-Metal Photodiodes," *Electronic Letters*, vol. 24, no. 25, pp. 1574-1575, Dec. 1988.

[134] T. Kikuchi, H. Ohno, and H. Hasegawa, "Metal-Semiconductor-Metal Photodiodes Using a Lattice Mismatched Schottky Assist Layer," *Electronic Letters*, vol. 24, no. 19, pp. 1208-1210, 1988.

[135] D. L. Rogers, J. M. Woodal, G. D. Pettit, and D. McInturff, "High-Speed 1.3 μm GaInAs Detectors Fabricated on GaAs," *IEEE Electronic Device Letters*, vol. 9, no. 10, pp. 515-517, Oct. 1988.

[136] W. Hong, G. Chang, and R. Bhat, "High Performance," *IEEE Transaction on Electron Device*, vol. 36, no. 4, pp. 659-662, April 1989.

[137] L. Yang, A. S. Sudbo, R. A. Logan, T. Tanbun-Ek, and W. T. Tsang, "High Performance of Fe:InP/InGaAs Metal/Semiconductor/Metal Photodetectors Grown by Metalorganic Vapor Phase Epitaxy," *IEEE Photonics Technology Letters*, vol. 2, no. 1, pp. 56-58, Jan 1990.

[138] L. Yang, A. S. Sudbo, W. T. Tsang, P. A. Garbinski, and R. M. Camarda, "Monolithically Integrated InGaAs/InP MSM-FET Photoreceiver Prepared by Chemical Beam Epitaxy," *IEEE Photonic Technology Letters*, vol. 2, no. 1, pp. 59-62, 1990.

[139] K. Nakajima, T. Iida, K. Sugimoto, H. Kan, and Y. Mizushima, "Properties and Design Theory of Ultrafast GaAs Metal-Semiconductor-Metal Photodetector with Symmetrical Schottky Contacts," *IEEE Transactions on Electron Devices*, vol. 37, no. 1, pp. 31-35, Jan. 1990.

[140] J. B. Soole and H. Schumacher, "Transit-Time Limited Frequency Response of InGaAs MSM Photodetectors," *IEEE Transactions on Electron Devices*, vol. 37, no. 11, pp. 2285-2291, Nov. 1990.

[141] D. Kuhl, F. Hieronymi, E. H. Bottcher, and D. Bimberg, "High-Speed Metal-Semiconductor-Metal Photodetectors on InP/Fe," *IEEE Photonic Technology Letters*, vol. 2, no. 8, pp. 574-576, Aug. 1990.

[142] E. Sano, "A Device Model for Metal-Semiconductor-Metal Photodetectors and its Applications to Optoelectronic Integrated Circuit Simulation," *IEEE Transactions on Electron Device*, vol. 37, no. 9, pp. 1964-1968, Sept. 1990.

[143] W. Hong, G. Chang, R. Bhat, H. Lee, C. Nguyen, and J. R. Hayes, "High-Functionality Waveguide/MSM/HEMT Integrated Receiver Prepared by One-Step OMCVD Grown on Patterned InP Substrates," *Proc. OFC'91*, p. 5, Feb. 1991.

[144] J. D. Crow, "Optical Interconnects for High-Performance Data Processing Systems," *Proc. IOOC'89*, 1989.

[71] H. A. Haus, W. P. Huang, S. Kawakami, and N. A. Whitaker, "Coupled Mode Theory of Optical Waveguides," *IEEE Journal of Lightwave Technology*, vol. 5, no. 1, pp. 16-23, 1987.

[72] S. Kawakami and H. A. Haus, "Continuum Analog of Coupled Multiple Waveguides," *IEEE Journal of Lightwave Technology*, vol. 4, no. 2, pp. 160-168, 1986.

[73] C.-S. Li, "Optimal design of high-speed parallel interconnections: a comparison of optical and electrical approach,," *Research Report, RC14898*, IBM Research Division, T. J. Watson Research Center, Sept. 1989.

[74] D. L. Lee, *Electromagnetic Principles of Integrated Optics*, New York: John Wiley & Sons, 1986.

[75] A. Yariv, *Chapter 13: Propagation, Modulation, and Oscillation in Optical Dielectric Waveguides, Optical Electronics*, Holt, Rinehart and Winston, New York, 1985.

[76] R. L. Burden and J. D. Fairs, *Numerical Analysis*, Boston, MA: Prindle, Weber & Schmidt Publishers, 1985.

[77] N. R. Dono, P. E. Green Jr., K. Liu, R. Ramaswami, and F. Tong, "A Wavelength Division Multiple Access Network for Computer Communication," *IEEE Journal of Selected Area in Communications*, vol. 8, no. 6, pp. 983-994, Aug. 1990.

[78] E. Desurvire, C. R. Giles, J. L. Zyskind, J. R. Simpson, P. C. Becker, and N. A. Olsson, "Recent Advances in Erbium-doped Fiber Amplifiers at 1.5," *Proc. Optical Fiber Communication Conference*, pp. San Francisco, CA., 1990.

[79] R. A. Linke, "Modulation induced Transient Chirping in Single Frequency Lasers," *IEEE Journal of Quantum Electronics*, vol. 21,, no. 6, pp. 593-597, June 1985.

[80] S. Yamamoto, M. Kuwazuru, H. Wakabayashi, and Y. Iwamoto, "Analysis of Chirp Power Penalty in 1.55- High-Speed Optical Fiber Transmission Systems," *IEEE Journal of Lightwave Technology*, vol. 5, no. 10, pp. 1518-1524, October 1987.

[81] P. J. Corvini and T. L. Koch, "Computer Simulation of High-Bit-Rate Optical Fiber Transmission Using Single-Frequency Lasers," *IEEE Journal of Lightwave Technology*, vol. 5, no. 11, pp. 1591-1595, November 1987.

[82] J. C. Cartledge and G. S. Burley, "The Effect of Laser Chirping on Lightwave System Performance," *IEEE Journal of Lightwave Technology*, vol. 7, no. 3, pp. 568-573, March 1989.

[83] J. C. Cartledge and M. Z. Iqbal, "The Effect of Chirping-induced Pulse Shaping on the Performance of 11 Gbit/s Lightwave Systems," *IEEE Photonic Technology Letters*, vol. 1, no. 10, pp. 346-348, October 1989.

[145] J. D. Crow, C. J. Anderson, S. Bermon, A. Callegari, J. F. Ewen, J. D. Feder, J. H. Greiner, E. P. Harris, P. D. Hoh, H. J. Hovel, J. H. Magerlein, T. E. Mckoy, A. T. Pomerence, D. L. Rogers, G. J. Scott, M. Thomas, G. W. Mulve, "A GaAs MESFET IC for Optical Multi-processor Network," *IEEE Transaction on Electron Devices*, vol. 36, p. 263, 1989.

[146] N. Yamanaka and T. Takada, "A 1.5 Gbit/s GaAs Four-Channel Selector LSI with Monolithically Integrated Newly Structured GaAs Ohmic Contact MSM Photodetector and Laser Driver," *IEEE Photonic Technology Letters*, vol. 1, no. 10, pp. 310-312, 1989.

[147] M. Makiuchi, H. Hamaguchi, T. Kumai, M. Ito, O. Wada, and T. Sakurai, "A Monolithic Four-Channel Photoreceiver Integrated on GaAs Substrate Using Metal-Semiconductor-Metal Photodiodes and FET's," *IEEE Electronic Device Letters*, vol. 6, no. 12, pp. 634-635, 1985.

[148] D. R. Kaplan and S. R. Forrest, "Electrical Crosstalk in p-i-n Arrays, Part I: Theory," *IEEE Journal of Lightwave Technology*, vol. 4, no. 10, pp. 1460-1469, Oct. 1986.

[149] R. G. Meyer and R. A. Blauschild, "A Wide-Band Low-Noise Monolithic Transimpedance Amplifier," *IEEE J. Solid-State Circuits*, vol. 21, no. 4, pp. 530-533, Aug. 1986.

[150] D. Rogers, "Monolithic Integration of a 3-GHz Detector/Preamplifier Using a Refractory-Gate, Ion-Implanted MESFET Process," *IEEE Electron Device Letters*, vol. 7, no. 11, pp. 600-602, Nov. 1986.

[151] A. Dickinson and M. E. Prise, "An Integrated Free Space Optical Bus," *Proc. ICCD*, pp. 62-65, 1989.

[152] D. A. Miller, D. S. Chemla, T. C. Damen, A. C. Gossard, W. Wiegmann, T. H. Wood, and C. A. Burrus, "Novel Hybrid Optically Bistable Switch: The Quantum Well Self-Electro-Optic Effect Devices," *Applied Physics Letters*, July 1984.

[153] D. A. Miller, D. S. Chemla, T. C. Damen, T. H. Wood, C. A. Burrus Jr., A. C. Gossard, and W. Wiegmann, "The Quantum Well Self-Electrooptic Effect Device: Optoelectronic Bistability and Oscillation and Self-Linearized Modulation," *IEEE Journal of Quantum Electronics*, Sept. 1985.

[154] D. A. Miller, J. E. Henry, A. C. Gossard, and J. H. English, "Integrated Quantum Well Self-Electro-Optic Device: 2x2 array of Optically Bistable Switches," *Applied Physics Letters*, Sept. 1986.

[155] A. L. Lentine, H. S. Hinton, D. A. Miller, J. E. Henry, J. E. Cunningham, and L. M. Chirovsky, "Symmetric Self-Electro-Optic Device: Optical Set-Reset Latch," *Applied Physics Letters*, April 1988.

[156] E. A. Lee and D. G. Messerschmitt, *Digital Communication, Digital Communication*, Kluwar Academic Publishers, Boston, 1988.

[157] A. Widmer and P. Franaszek, "A dc-balanced partitioned-block, 8B/10B transmission code," *IBM Journal of Research and Development*, Sept. 1983.

[158] R. C. Alferness, "Waveguide Electro-optic Modulators," *IEEE Transactions on Microwave Theory and Techniques*, Aug. 1982.

[159] E. Voges and A. Neyer, "Integrated-Optic Devices on for Optical Communication," *IEEEJournal of Lightwave Technology*, Sept. 1987.

[160] H. Kogelnik and R. V. Schmidt, "Switched Directional Coupler with Alternating," *IEEE Journal of Quantum Electronics*, July 1976.

[161] K. Ishida, H. Nakamura, H. Matsumura, T. Kadoi, and H. Inoue, "InGaAsP/InP Optical Switches Using Carrier Induced Refractive Index Change," *Applied Physics Letters*, vol. 50, no. 3, pp. 141-142, 1987.

[162] G. Winzer, W. Doldissen, C. Cremer, F. Fiedler, G. Heise, R. Kaiser, R. Marz, H. F. Mahlein, L. Morl, H. J. Nolting, W. Rehbein, M. Schienle, G. Schulte-Roth, G. Unterborsch, H. Unzeitig, and U. Wolff, "Monolithically Integrated Detector Chip for a Two-Channel Unidirectional WDM Link at 1.5 μm," *IEEE Journal on Selected Areas in Communications*, vol. 8, no. 6, Aug. 1990.

[163] T. P. Lee, C. A. Burrus, and A. G. Dentai, "Dual Wavelength Surface Emitting InGaAsP LEDs," *Electronic Letters*, vol. 16, p. 845, 1980.

[164] J. C. Campbell, A. G. Dentai, T. P. Lee, and C. A. Burrus, "Improved Two-Wavelength Demultiplexing InGaAsP Photodetector," *IEEE Journal of Quantum Electronics*, vol. 16, p. 601, 1980.

[165] K. Ogawa, T. P. Lee, C. A. Burrus, J. C. Campbell, and A. G. Dentai, "Wavelength Division Multiplexing Experiment Employing Dual-wavelength LEDs and photodetectors," *Electronic Letters*, vol. 17, p. 857, 1981.

[166] A. K. Chin, B. H. Chin, I. Camlibel, C. L. Zipfel, and G. Minneci, "Practical Dual-Wavelength Light-Emitting Double Diode," *Journal of Applied Physics*, vol. 57, p. 5519, 1981.

[167] J. C. Campbell, C. A. Burrus, J. A. Copeland, and A. G. Dentai, "Wavelength-discriminating Photodetector for Lightwave System," *Electronic Letters*, vol. 19, pp. 672-674, 1983.

[168] T. H. Wood, C. A. Burrus, A. H. Gnauck, J. M. Wiesenfeld, D. A. Miller, and D. S. Chemla, "Wavelength-Selective Voltage-Tunable Photodetector Made from Multiple Quantum Wells," *Applied Physics Letters*, vol. 47, pp. 190-192, 1985.

[169] J. Gowar, *Chapter 14: The Receiver Amplifier, Optical Communication System*, Englewood Cliffs, NJ, 1984.

[170] C.-S. Li and H. S. Stone, "Decision Feedback Automatic Threshold Computation," *IBM Technical Disclosure Bulletin*, 1991.

[171] K. Hwang and D. Degroot, *Parallel Processing for Supercomputers and Artificial Intelligence*, McGraw-Hill, New York, 1989.

[172] S. Y. Kung, *VLSI Array Processors*, Prentice-Hall, Englewood Cliffs, NJ., 1988.