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A METHOD FOR ESTIMATING OVERLAP CAPACITANCE IN MOSFET DEVICES BY DC CURRENT MEASUREMENT

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Abstract

The performance of modern IC devices is often determined by, among other factors, the value of the parasitic gate to source/drain overlap capacitance. It is therefore desirable to determine the overlap capacitance in order to have a better model of the device, so that one can bin the ICs during production based upon speed and performance. In high volume production, measurement results of early runs can be used to improve the process. Since capacitance measurements are tedious and time consuming, they are not practical to perform during production. On the other hand, DC current measurements are performed as routine electrical tests. The objective of this paper is to introduce a technique that infers the gate-to-drain/source overlap capacitance of submicron devices by simple DC measurements. The inference is based on the asymmetry of the device, typically caused by angled ion implantation. For certain values of t_{ox}, implantation angle, dopant concentration, and drive-in time, a linear model can be built experimentally to determine the gate-to-drain overlap capacitance (C_{gd}) and gate-to-source overlap capacitance (C_{gs}) based strictly on DC measurements; the DC measurements would be the measurements of the two saturation currents of the device interchanging its source and drain. In an IC production facility, a model can be built from experimental data obtained from early runs. Then routine DC measurements will determine the C_{gs} and C_{gd} throughout production.

Acknowledgments

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Chapter 1

Introduction

The exact control of the gate transition delay has always been a challenge for CMOS technology. One important factor in the CMOS transition speed is the gate-to-source/drain overlap capacitance. Unfortunately, direct measurement of the overlap capacitance is too expensive and time consuming to be done during production. Also it may not be very accurate, since the fringing field capacitance between gate and source/drain is included in every measurement of the overlap capacitance whether there is an actual overlap of gate on source/drain or not. Further, the typical 7-degree implantation that is done to prevent channeling in silicon causes asymmetric overlap capacitance, which in turn results in different saturation current of the device, depending on whether the side of the weaker overlap is used as source or drain (Fig. 1). This phenomena becomes more pronounced as the channel length is reduced.

This work suggests an inexpensive method for estimating the overlap capacitance by using I-V measurement of the device. This method is based on the correlation between the current asymmetry and overlap asymmetry of gate on source and drain; current asymmetry refers to the difference between the two saturation currents when source and drain are interchanged. Initial capacitance measurements on test patterns are required to establish the relationship between the current asymmetry and overlap asymmetry of gate on source and drain. Once this relationship is characterized, I-V measurements on both sides, i.e. source and drain, can be performed to obtain an accurate estimate of the overlap capacitance.

This method can be used in fabrication lines to estimate the overlap extension of the gate on source and drain. The result in turn can be used to control process factors such as drive-in time.

This method is easy, inexpensive, non-destructive, and practical. The accuracy of the method will be addressed and discussed.

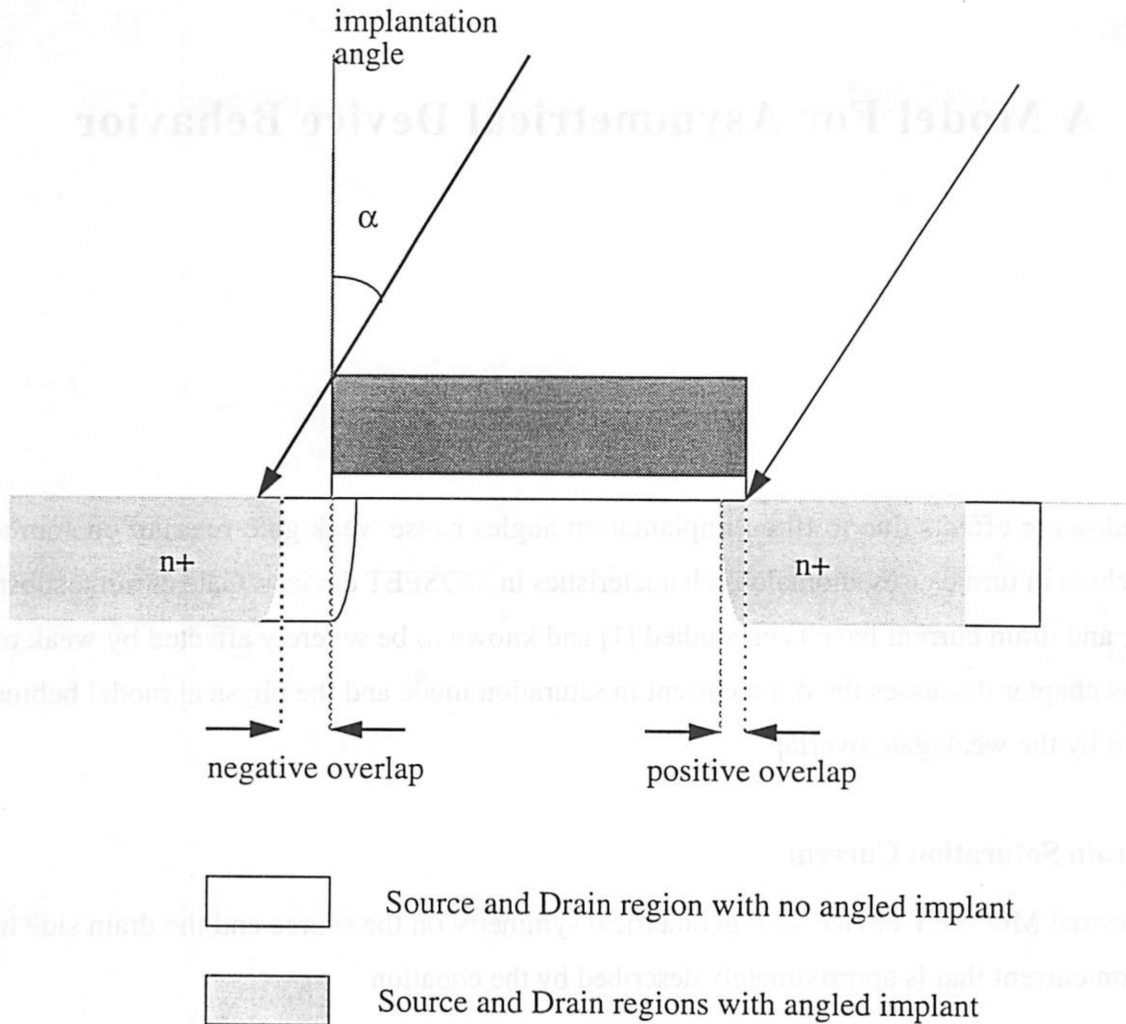


Figure 1 Asymmetrical overlap caused by slanted implantation angle

The rest of this report contains the device theory of asymmetrical MOSFETs, detailed description of the experiment and an analysis of the extracted model suggesting the measurement method for overlap capacitance. Chapter two analyzes asymmetrical MOSFETs in comparison with normal devices from a physical point of view for both cases of drain weak overlap and source weak overlap and asymmetrical LDD MOSFETs. The details of the experiment, including test pattern design, fabrication, measurement set up, procedure, and data extraction are provided in chapter three. The results and conclusion are presented in chapters four and five, respectively. A summary of measurements is appended.

Chapter 2

A Model For Asymmetrical Device Behavior

Shadowing effects due to tilted implantation angles cause weak gate-overlap on source or drain, which in turn causes anomalous characteristics in MOSFET devices. Gate current, substrate current, and drain current have been studied [1] and known to be severely affected by weak overlap. This chapter discusses the drain current in saturation mode and the physical model behind its variation by the weak gate overlap.

2.1 Drain Saturation Current

A normal MOSFET device with geometrical symmetry on the source and the drain side has a saturation current that is approximately described by the equation

$$Id = \frac{1}{2}\mu Cox\frac{W}{L}(Vg - Vt)^2$$

neglecting the channel modulation and other second order effects. In order to see how the implantation shadowing effect makes an asymmetrical device behave differently from a symmetrical device in terms of the current in saturation mode, let us first review the assumptions in deriving the above equation. It will be seen that some of these assumptions do not hold for asymmetrical devices.

In a distributed analysis of the MOSFET behavior [2] an incremental voltage drop along the channel is assumed as a function of the channel current. By integration of the mobile charge in the

channel from source to drain, a current-voltage relationship is obtained for MOSFET devices. This relationship holds until the depletion region at the drain widens to the point that pinches off the channel. In this analysis, a gradual channel approximation is assumed to be valid from source to drain. This approximation assumes that the channel and depletion layer widths vary slowly from source to drain so that the depletion region is influenced only by fields in the vertical dimension and not by fields extending from drain to source, because the electric field in the direction of current flow is much weaker than the field in the direction perpendicular to the silicon surface. In other words, there are simplifying assumptions in the one dimensional analysis which all will not be discussed here (for detail see reference [2]). One assumption ignores the doping variation in the regions between the active channel and the heavily doped source and drain contacts. More important in this case is the assumption that the vertical field (perpendicular to silicon surface, i.e. x-direction in Fig 3.a) is uniform along the channel from source to drain.

For a symmetrical device with sufficient gate overlap on source and drain, the simplifying assumptions would be true. In the case of weak overlap, however, there is no gate-control over parts of the channel. Over these regions, the perpendicular field is very weak and the gradual channel approximation is not valid any more. For a MOSFET to have a continuous inversion layer from source to drain, it requires a much stronger field in the direction of current flow under the weak overlap region in comparison with the rest of the channel.

A schematic depiction of the electric field in the direction of current flow in the weak overlap case is shown in Fig. 2. It shows that the peak channel fields in the weak gate overlap region, either for a gate bias point just above the threshold (shown with dashed line, A), or a gate bias point near the power supply value (shown with continuous line, B), are lower than those of a normal device. Both configurations behave more or less like a normal MOSFET device except for the extra voltage drop in the weak overlap regions which results in lower peaks for the channel field in comparison with a symmetrical device; this in effect invalidates the gradual channel approximation[1].

As a result, the current characteristics for weak gate overlap devices are not the same as for normal MOSFET devices. The quantitative and qualitative differences depend on whether the weak overlap is on the source or on the drain side. Furthermore, it will be shown that drain weak overlap has a negligible effect on the drain saturation current and can be overcome by a slightly higher drain voltage which translates to increasing the electric field in the direction of current

flow. On the other hand, source weak overlap has a stronger effect on the drain saturation current and it can only be compensated by a field perpendicular to the current flow direction, as it will be explained in the following sections; this translates to a higher than normal gate voltage to maintain the same drain saturation current.

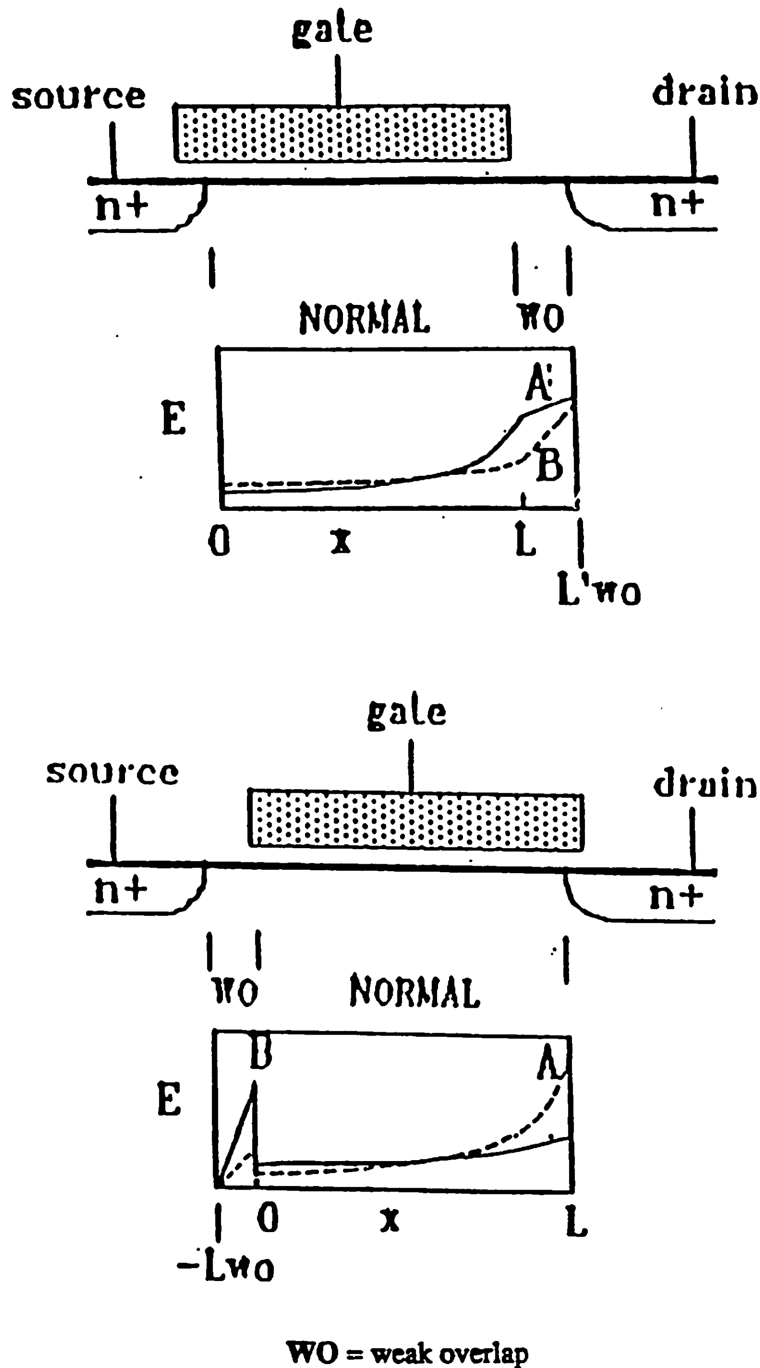


Figure 2 Qualitative channel filed profiles for asymmetrical MOSFETs [1]

2.2 Drain Weak Overlap MOSFET

As our measurements will be concentrated on the saturation current at the beginning of the pinch-off zone, channel length modulation is not a concern in this discussion. Even though any further increase in the drain voltage would increase the space charge region (region C, Fig.3b) and modulate the length of the channel, this has the same effect on both symmetrical and asymmetri-

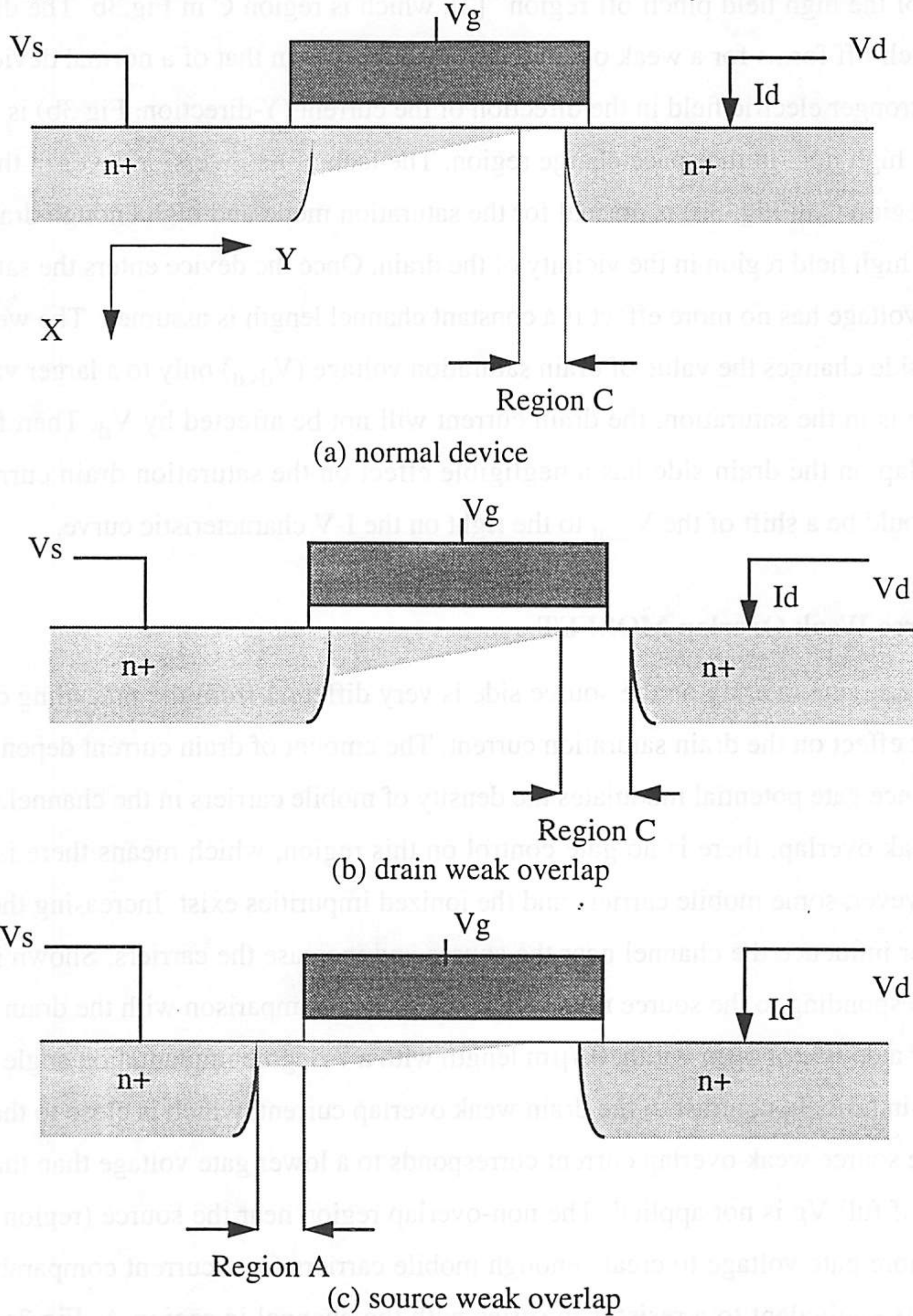


Figure 3 (a) normal, (b) drain weak overlap, and (c) source weak overlap MOSFETs at saturation.

cal devices. Based on this realization, this discussion is limited to the saturation current without further discussing channel length modulation.

The gradual channel approximation predicts the maximum current at the drain saturation voltage when $V_d = V_g - V_t$. The drain current is determined by the "rate at which electrons arrive at the edge of the high field pinch-off region" [2], which is region C in Fig.3b. The drain voltage at which pinch-off forms for a weak overlap drain is higher than that of a normal device. The reason is that a stronger electric field in the direction of the current (Y-direction, Fig 3b) is needed to create a very high field in the space charge region. The lack of an inversion layer in the non-overlap region, (region C in Fig. 3b) is normal for the saturation mode and high enough drain voltage can create the high field region in the vicinity of the drain. Once the device enters the saturation mode, the drain voltage has no more effect if a constant channel length is assumed. The weak overlap on the drain side changes the value of drain saturation voltage (V_{dsat}) only to a larger value, and once the device is in the saturation, the drain current will not be affected by V_d. Therefore, the weak gate overlap on the drain side has a negligible effect on the saturation drain current. The only change would be a shift of the V_{dsat} to the right on the I-V characteristic curve.

2.3 Source Weak Overlap MOSFET

The weak gate overlap on the source side is very different from the preceding case and has a significant effect on the drain saturation current. The amount of drain current depends on the gate voltage, since gate potential modulates the density of mobile carriers in the channel. In the case of source weak overlap, there is no gate control on this region, which means there is no inversion layer. However, some mobile carriers and the ionized impurities exist. Increasing the gate voltage will further influence the channel near the source and increase the carriers. Shown in Fig.4 is the curve corresponding to the source non-overlap current in comparison with the drain weak overlap current for a device of 5μm width, 0.7μm length with a 7-degree implantation angle and 120 minutes drive-in time. In contrast to the drain weak overlap current, which is close to that of a normal device, the source weak overlap current corresponds to a lower gate voltage than that of a normal device, as if full Vg is not applied. The non-overlap region near the source (region A in Fig. 3c) requires more gate voltage to create enough mobile carriers for a current comparable to the normal. This is equivalent to a resistor in series with the channel in region A, Fig 3c, between the source and the channel. For the saturation region of the device, a resistor of high value can be

used to model the weak gate overlap region, where the only charges are the carriers and the ionized impurities, and is not as conductive as the rest of the channel. It should be mentioned that for

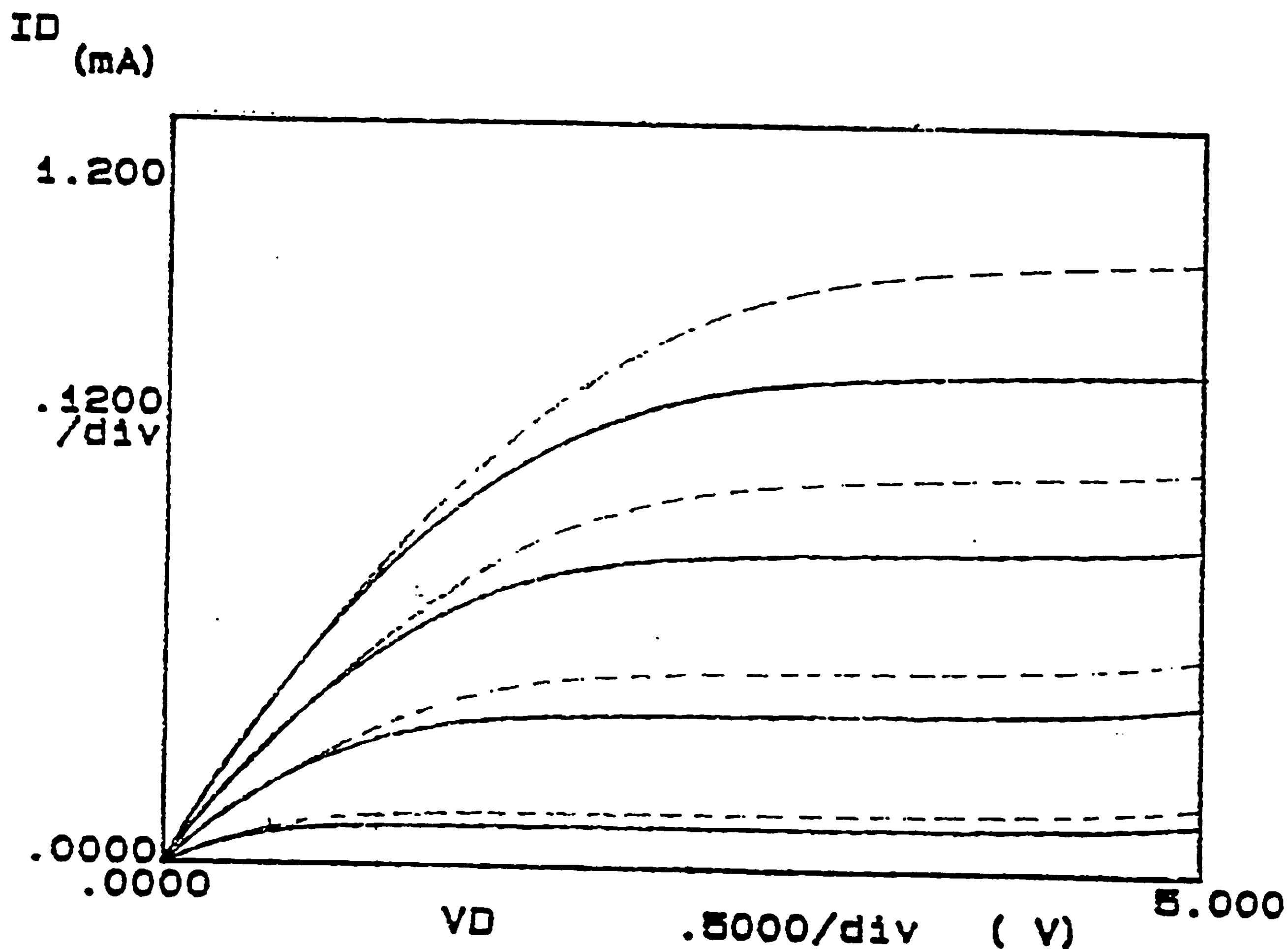


Figure 4 Source weak overlap saturation current (constant line) versus drain weak overlap saturation current (dashed line)

low drain bias in a lumped analysis[2] the drain current is related to the total charge in the channel. Hence, the current for low drain bias is not significantly different for the case of source weak overlap.

The saturation current when the weak overlap side is used as source (called the "source saturation current" in this paper) is severely degraded by the source weak overlap region and it requires

higher gate voltage to increase the current to the normal level (Fig 4). Higher gate voltage, however, will raise reliability issues due to the possibility of hot electron injection into the gate [3].

2.4 LDD MOSFET With Weak Gate Overlap

LDD devices with weak overlap region over n- could be similarly analyzed and modeled. For modelling purposes, it would be convenient to approximate the n- region as a resistor in series with the source and drain. The resistors will have a voltage drop across them. In the case of weak gate overlap, there will be resistors of unequal ohmic values on source and drain. Adding the resistors to the model will describe the anomalous I-V characteristic in the saturation region for asymmetrical LDD MOSFETs. This analysis is outside the scope of this work.

Chapter 3

Overlap Capacitance Estimation Method

As the geometry of the asymmetrical device suggests, there must be a relationship between the saturation current asymmetry and the overlap asymmetry. Consequently, there must be a dependence between current asymmetry and overall overlap capacitance. Fig.5a and Fig. 5b show

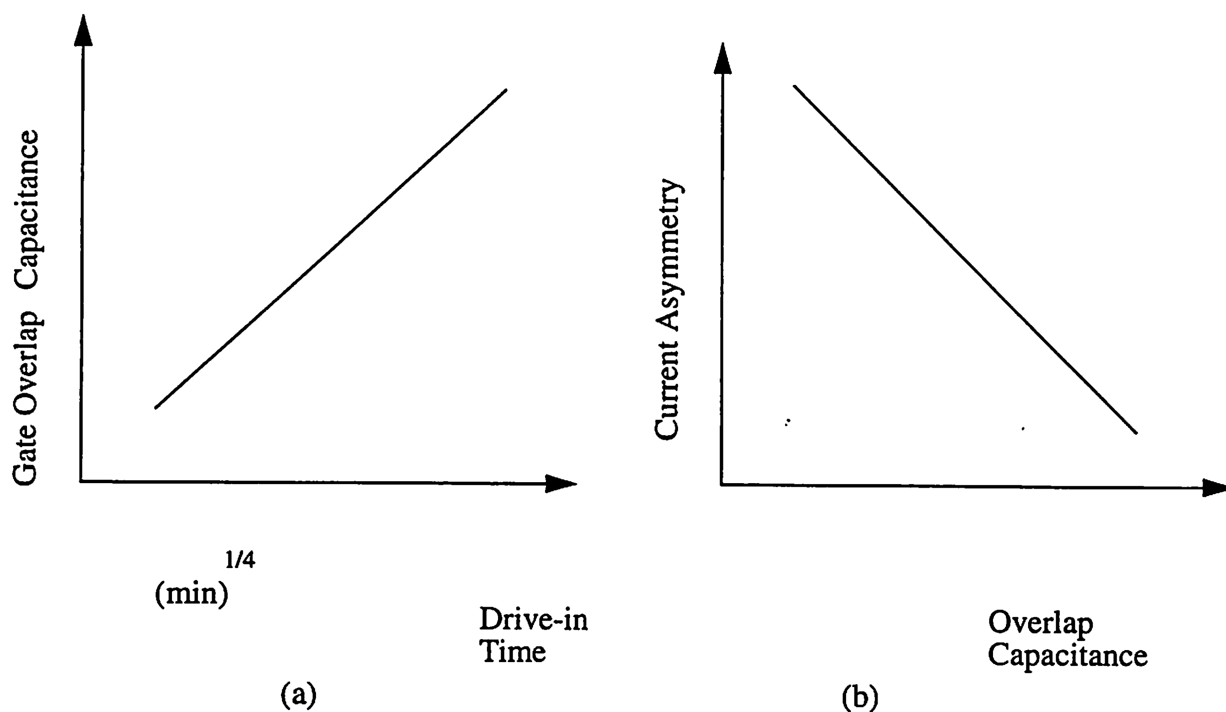


Figure 5 Dependency trend of (a) gate overlap capacitance and (b) current asymmetry versus drive-in time

the trend of variation of saturation current and overlap asymmetry with increasing drive-in time. Fig. 5a shows that as drive-in time increases, the overlap increases. Similarly, the saturation current asymmetry is increasing for the increasing overlap capacitance as depicted in Fig.5b. The purpose of this study is to find an accurate estimate of the gate overlap capacitance on source and drain via a simple method of current measurement by exploiting the relationship shown in Fig. 5b. By measuring both the difference between two saturation currents and difference between overlap on two sides of the devices on test pattern, an approximate linear relationship can be set between the saturation current and the gate overlap such that I-V measurements can reveal the difference between gate overlap on two sides.

In this experiment, the saturation current of both sides of the device were measured by applying DC voltage on gate and drain, and by grounding the source. The gate overlap on source and drain was measured by high frequency capacitance measurement as will be discussed later; the C_{gd} and C_{gs} will reveal the amount of gate overlap.

The following sections will discuss the effects of different drive-in times on the saturation current and overlap asymmetry as well as the details of the measurements. Also, the test pattern, measurement repeatability, fabrication, and the importance of the channel length in this experiment will be addressed.

3.1 The Test Pattern Design

Initially, experimental measurements are done to realize the sources of parasitic capacitance and account for them in order to obtain meaningful and repeatable data. One important component of the parasitic capacitance is the internal capacitance of the device due to the layout. The layout position of the device pads also determines the position of the probes which may contribute to the parasitic capacitance.

As it will be explained later, to estimate the overlap capacitance per unit width, the overlap capacitance of devices with the same length but different widths are compared against each other. In this experiment, devices with similar layout are compared (Fig. 6). More specifically, of the U.C.Berkeley NMOS12 series of wafers, devices of 5μm width were compared to devices of 100μm, and devices of 10μm width were compared to devices of 200μm width. This comparison

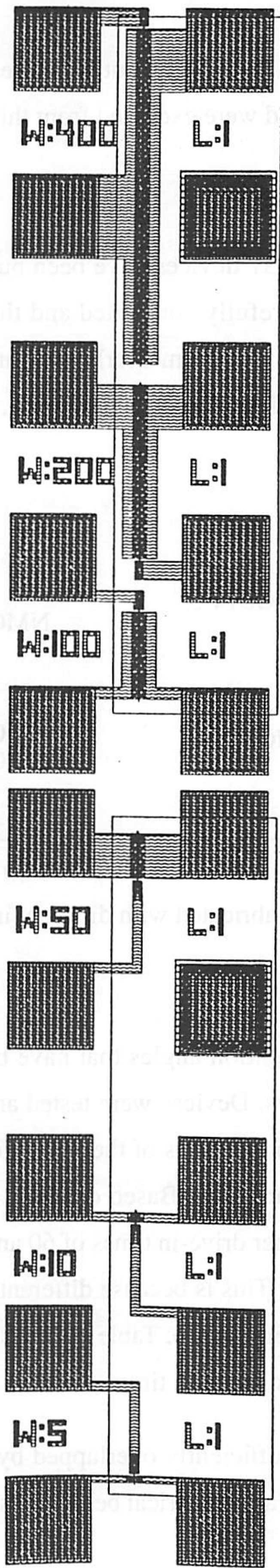


Figure 6

was feasible because of the similar layout structures. Devices of 50μm and 400μm width had different layout structures and were excluded from this comparison.

3.2 Fabrication of Test Wafers

Asymmetrical MOSFET devices have been built using ion implantation tilted at a 7-degree angle. This angle was carefully controlled and the wafers were oriented so that the measured devices were subjected to maximum overlap asymmetry. Wafers with a zero degree implantation angle were also processed and used for reference. Fig. 7 shows the wafer numbers of different

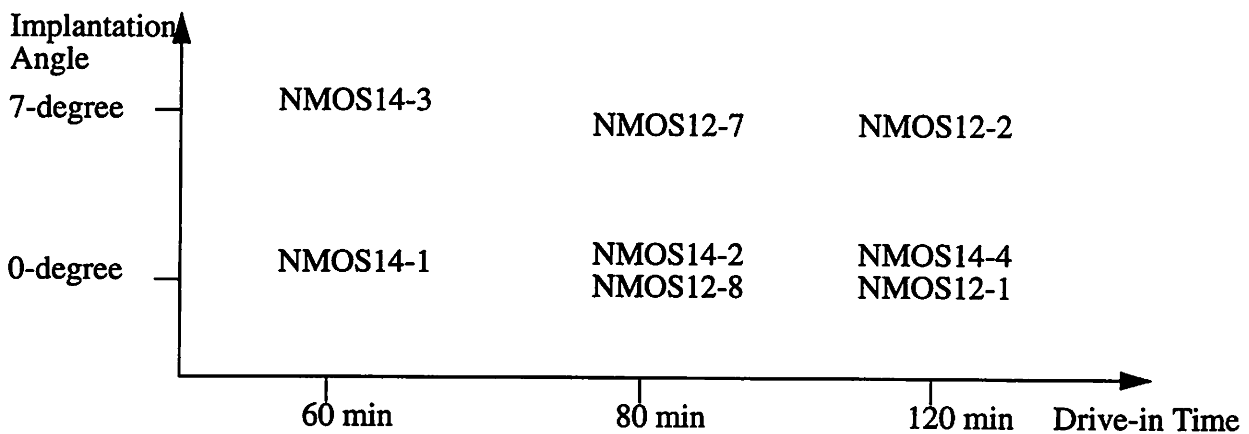


Figure 7 wafers fabricated with different implantation angles and drive-in times

drive-in times and implantation angles that have been processed. The first run of wafers had a drive-in time of 80 minutes. Devices were tested and measurements showed considerable difference between the saturation currents of the two sides of the device and also between the overlap capacitances on source and drain. Based on these results, two other series of wafers were processed with lower and higher drive-in times of 60 and 120 minutes in order to obtain different levels of overlap capacitance. This is because different drive-in times will result in different degrees of asymmetry as depicted in Fig. 5b. Table 1 shows a summary of the processed wafers of different implantation angles and drive-in times.

When both sides are sufficiently overlapped by the gate in a MOSFET device, even though with different amounts, no asymmetrical behavior is observed in saturation current characteristics.

This overlap asymmetry would make different overlap capacitance on source and drain. In this case, a difference in transition speeds between the two sides, if any, would be due to different capacitances on two sides and not different currents; the saturation current will not be asymmetric because of the lack of weak overlap region.

Table 1: Summary of processed wafers

WAFER	IMPLANT ANGLE	DRIVE IN TIME
NMOS14-1	0	60 MIN
NMOS14-2	0	80 MIN
NMOS14-3	7	60 MIN
NMOS14-4	0	120 MIN
NMOS12-1	0	120 MIN
NMOS12-2	7	120 MIN
NMOS12-7	7	80 MIN
NMOS12-8	0	80 MIN

3.3 Measurement Set Up

The Electroglass 2001X was initially considered for both capacitance and I-V measurements in this experiment. It can be connected to HP equipment for I-V measurement and capacitance measurements and its X-Y stage can automatically step and probe the desired dies on the wafer. For an accurate measurement of capacitance, the parasitic capacitance can be reduced by using coaxial probes and cables. However, it was found to be impractical to do capacitance measurement by the Electroglass within the accuracy required by this experiment. The problem with an automatic prober is that the probes should be set to have firm contact with the wafers to assure a good contact with the pads. The coaxial probes are very sensitive and brittle and also very expensive. Setting them for a hard press on the wafer may break them. If not set hard, there may not be a good contact between the probes and wafer; the measurement would not be accurate nor reliable. The lengthy coaxial cables also caused problems. These problems made the manual probing with HP equipment the better choice for measuring the overlap capacitance in order to calibrate the test pattern. The HP impedance measurement equipment 4275A used with a shielded manual probe station, was found to be more accurate for the measurement of our test patterns. The drain

saturation current was also measured manually by HP8189A for more control over the accuracy of the data in this experiment.Having established the relationship between I-V characteristics and overlap capacitance on asymmetric devices, the Electroglass 2001X can be used for statistical I-V measurements and estimating the overlap capacitance

In this experiment, the saturation current of both sides of the device were measured by applying DC voltage on gate and drain and grounding the source. The gate overlap on source and drain was obtained by high frequency capacitance measurement as will be discussed later; the C_{gd} and C_{gs} will reveal the length of the gate overlap. Drain saturation current in cases of weak overlap drain and weak overlap source were measured as well as the overlap capacitance on source and drain during the same experiment in order to eliminate any inaccuracy in data due to measurement set-up. Also, the measurements on each set of data were replicated twice to insure the repeatability of the experiment and reliability of the data.

3.4 Procedure

The drain saturation current was measured by an HP8189A semiconductor parameter analyzer. The devices were biased with V_g=5V, V_d=4V, V_s=0V, and V_b=0V. The capacitance measurement was done using an HP4275A prober. Coaxial cables and coaxial probes were used and the probe station was shielded during the experiment to minimize the disturbances to the capacitance measurement. The HP4275A was connected to an HP computer that would read 10 consecutive measurements and take the average. The set up is shown on Fig. 8 and further explained in [1]. A gate voltage of -2 volts was applied to prevent the formation of an inversion layer during overlap capacitance measurements. The source and substrate were grounded to shunt the capacitance between gate and those nodes during the measurement of gate-drain overlap capacitance. A small signal of 50 mV amplitude and 1MHz frequency was applied.

Relatively short channel transistors with drawn lengths of 0.5µm and 0.7µm were used for this experiment. The reason for choosing short channel devices is based on the discussion in the previous section; for a long channel transistor the voltage drop along the channel will obscure the voltage drop under the weak overlap region. As a result, the asymmetry in long channel transistors, i.e. length of 2µm or more, would not be as pronounced. This was confirmed by measuring the drain saturation current on both sides in asymmetrical devices with a drawn channel length of 2µm and up to 10µm. No asymmetry was observed in the saturation current. Therefore, the con-

clusion of the experiment is based on the measurements of devices with channel lengths of 0.5μm and 0.7μm. The dependency of the asymmetry with the channel length will be addressed in the following sections.

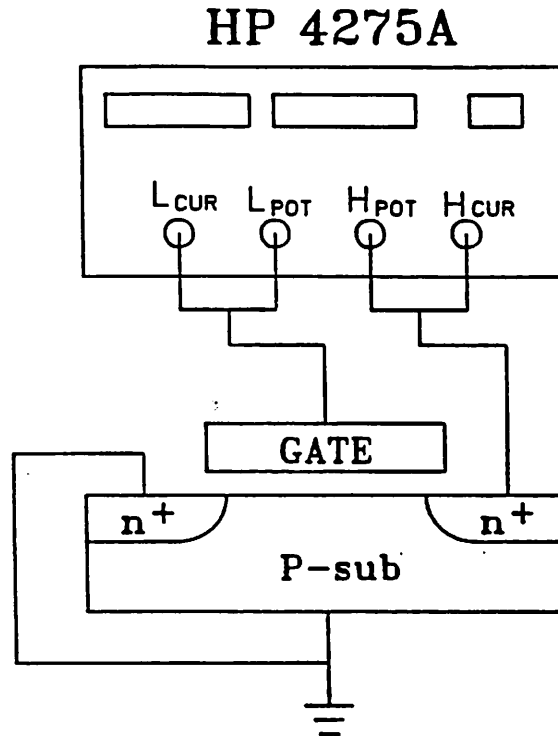


Figure 8 Set up to measure the gate-to-drain/source overlap capacitance [1]

3.5 Data Collection

Devices with drawn lengths of 0.5μm and 0.7μm and widths of 5μm, 10μm, 100μm, and 200μm were tested and their saturation currents of both source weak overlap and drain weak overlap as well as their overlap capacitance on each side were measured. In order to have an accurate estimate of the overlap capacitance, as mentioned in [1], Cgd is measured for devices with different channel width, but the same channel length. If the Cgd is plotted versus width, the slope of this linear plot (Fig. 9) would be the overlap capacitance per unit width expressed as fF/μm. The intercept at width of zero is the parasitic capacitance due to the wiring. The fringing field capacitance between the sides of the gate and the source/drain is almost of the same value for both sides even in an asymmetrical device. In this experiment, it has been concluded that the fringing field capacitance is insignificant.

The same procedure was used for C_{gs}, with the same set-up and during the same experiment time, to eliminate the noise due to the set-up. [1] explains how the actual amount of overlap can

be derived and it will be briefly explained here: for a short drive-in time when the edge of the depletion region in the drain diffusion has no overlap with the gate, its overlap capacitance is mainly the fringing field capacitance which is about the same value for both sides. The actual overlap length, Xov, can be derived as:

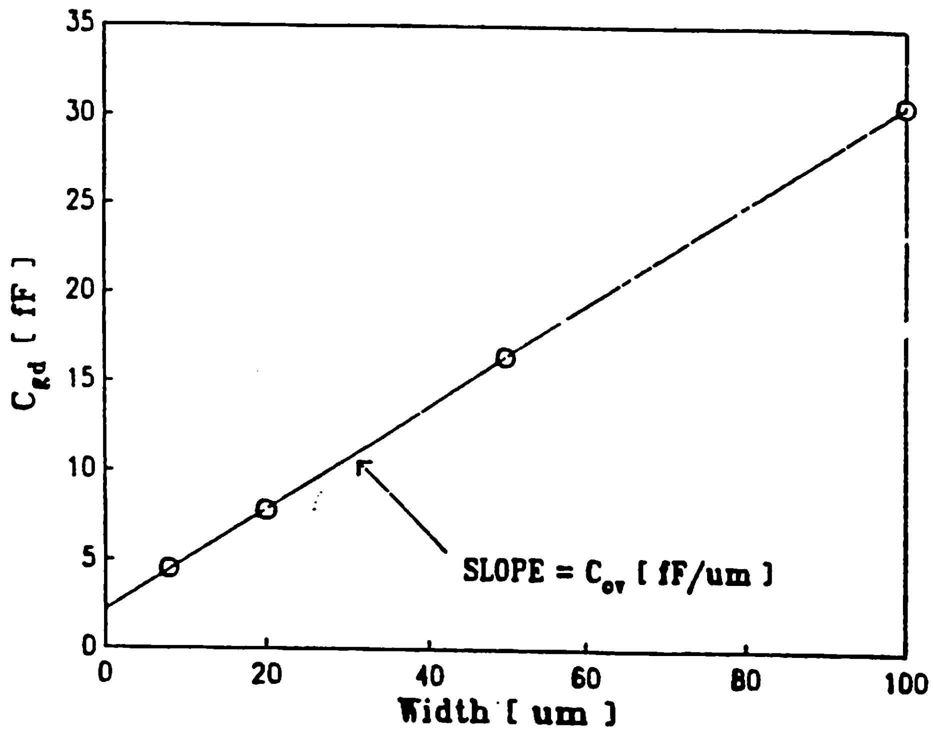


Figure 9 Plot of the gate-to-drain/source capacitance versus channel width. The overlap capacitance Cov in fF/μm can be extracted from the slope. The intercept at W=0 is the parasitic capacitance due to the wiring.

$$X_{ov}=(C_{ov}-C_{ff})/C_{ox}$$

C_{ov} and C_{ff} are in the unit of fF/μm and C_{ox} in the unit of fF/μm. The resolution of this non-destructive method is believed to be about 10Å[1].

Chapter 4

Results

The objective of establishing an empirical model between the overlap capacitance and the saturation currents is met. This model can predict the gate to source/drain overlap capacitance by direct DC measurements, eliminating the need for tedious capacitance measurement. A curve fitting software is used to build the model upon the measured data. The model is reliable; the plot of the actual average C_{ov} versus the predicted value by the model is as of x = y with a R-square of 0.9 or better and all the terms of the model are statistically significant at the 5% level or better. Such an empirical model can be built in an IC production facility by measuring overlap capacitances and saturation currents on early wafers. Having built the model, then only DC measurements are required to determine Cgs and Cgd for the rest of the wafers throughout the production. As mentioned before, the model is valid for a certain process with a specific set of values for tox, implantation angle, dopant concentration, and drive-in time. If any of the device process parameters changes, either a new model should be built or a correction factor for the changed parameter be included. This correction factor can be obtained by studying the dependency of the model on the parameter. The dependency of the model on different parameters will be discussed.

Ion implantation angle, that causes the device asymmetry, is the parameter that the empirical model has the strongest dependency on and will be discussed more. However, the model presented here, is for the specific 7-degree ion implantation angle. Accurately measured data of overlap capacitance on two sides of devices as well as the two saturation currents when source and drain are interchanged are analyzed by a software to build a statistical regression model. The actual capacitance value are then examined versus the model predicted values. The results, as mentioned, are statistically significant. To have a better understanding of the graphical figures, the

employed terms are explained here. Using the drain and source saturation currents, Id and Is respectively, AvgI, in mA, is defined as (Id + Is)/2 and DiffI as (Id-Is)/AvgI. The regression models are linear, with first degree dependency on DiffI and AvgI for each wafer. For a number of wafers, a similar model is built that also incorporates the effect of drive-in time.

Fig. 10.a shows the model predicted versus the actual average overlap capacitance or AvgC, in fF/μm. The linear model is as follows, including the 95% confidence intervals of each coefficient.

AvgC = -.085519 DiffI + 0.0077138 AvgI - 0.074141

±0.03238 ±0.00270 ±0.03238

As seen in the Summary of Fit table, this is a model with a root mean square error less that 2%. Figures 10.b and 10.c illustrate the dependency of AvgC on DiffI and AvgI, respectively.

Fig. 11.a is a plot of the model predicted versus the actual difference between drain and source overlap capacitance (DiffC). This linear model is:

DiffC = -0.487916 DiffI - 0.232017

±0.0550 ±0.03262

Including the AvgI in the model slightly improves it, but the more important factor is DiffI. The dependance on AvgI is very small:

DiffC = -0.454586 DiffI + 0.0049178 AvgI - 0.405482

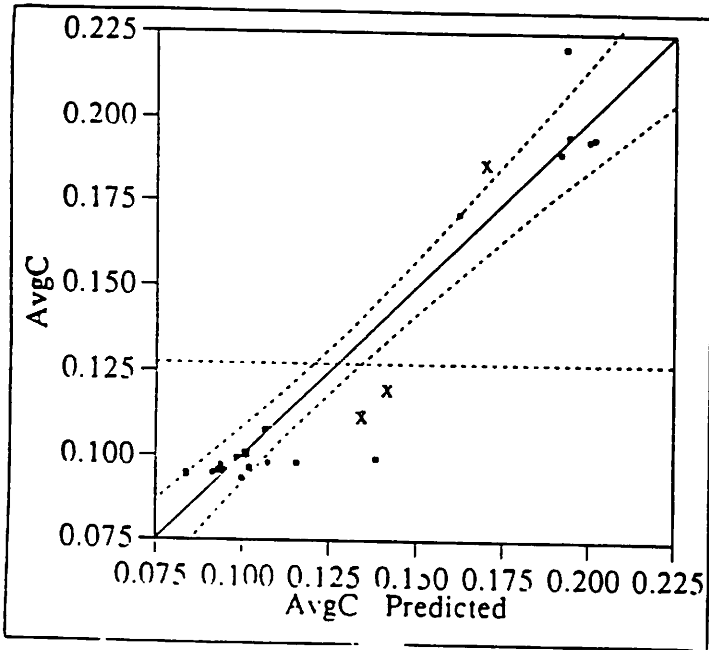
±0.08666 ±0.00988 ±0.34998

Fig. 12.a is a depiction of the dependency of DiffC on the implantation angle, DiffI, and Drive-in time. The model for DiffC in this case is:

DiffC = -0.002381 Drive-in time - 0.447106 DiffI - 0.080971 Angle + 0.5695119

±0.00108 ±0.08686 ±0.00604 ±0.11394

For the asymmetrical capacitance overlap, other dependencies have been observed, too.There exist a strong dependency on the transistor size. As it was discussed before, the asymmetry is



x = points excluded as statistical outlyiers

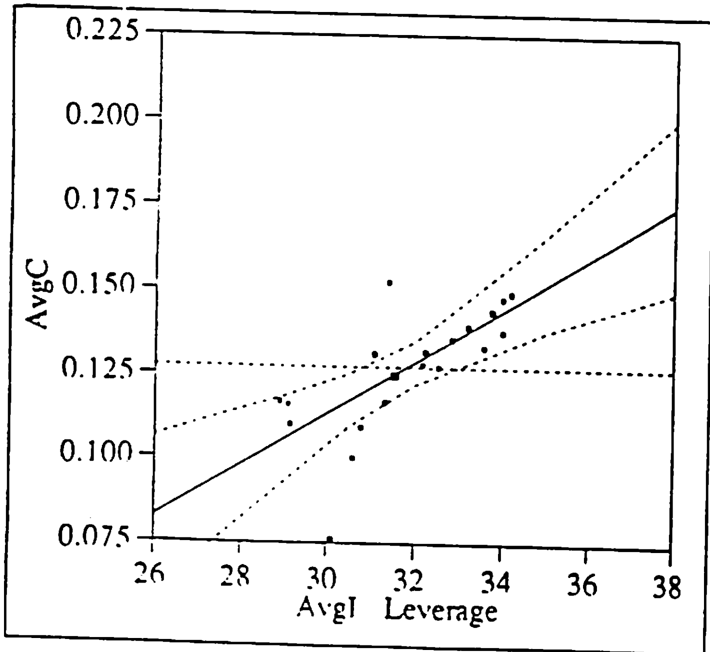
(a)

Parameter Estimates

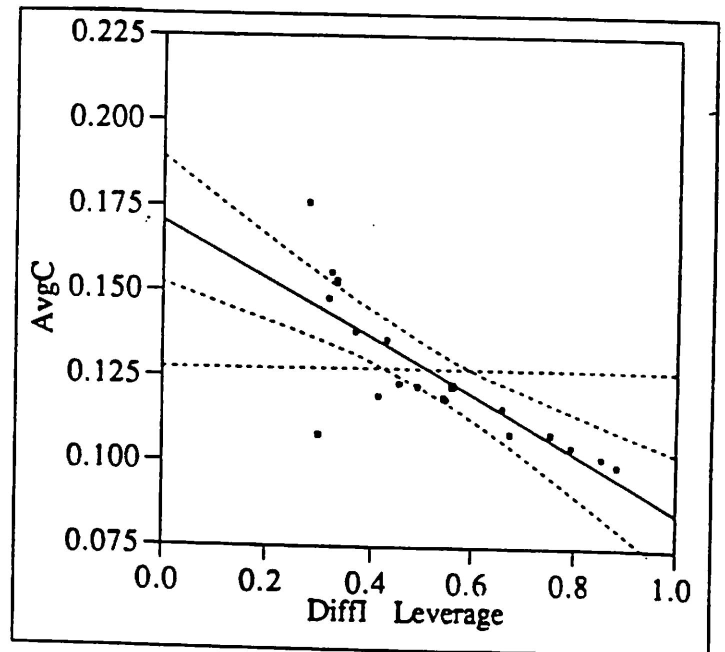
Term	Estimate	Std Error	t Ratio	Prob>|t|
Intercept	-0.074141	0.06541	-1.13	0.2727
AvgI	0.0077138	0.00185	4.18	0.0006
DiffI	-0.085519	0.01619	-5.28	0.0001

Summary of Fit

Rsquare	0.920613
Root Mean Square Error	0.013758
Mean of Response	0.127394
Observations (or Sum Wgts)	20

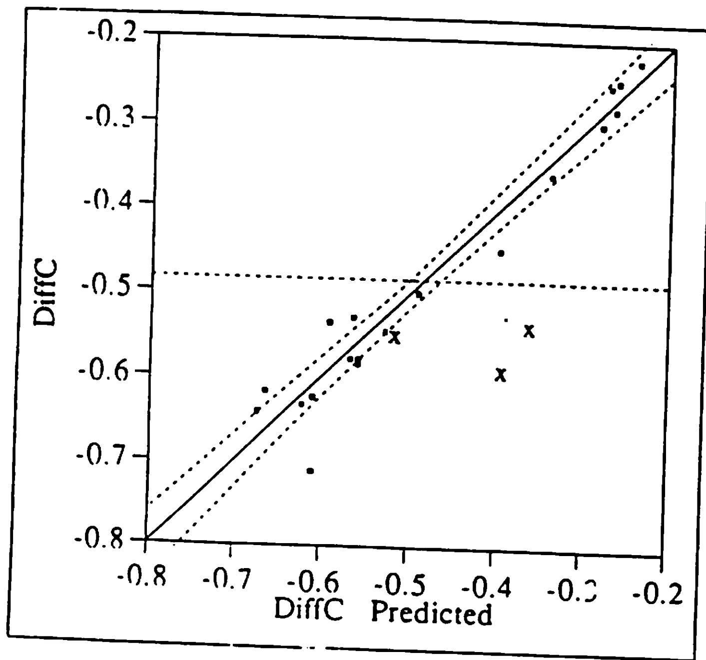


(b)



(c)

Figure 10 Model predicting AvgC as a function of AvgI and DiffI



x = points excluded as statistical outlyiers

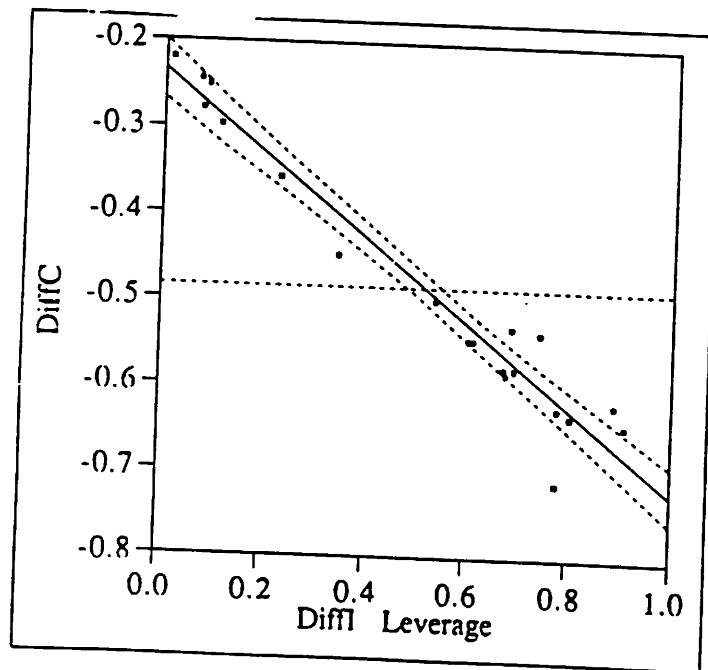
(a)

Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Intercept	-0.232017	0.01631	-14.23	0.0000
DiffI	-0.487916	0.0275	-17.74	0.0000

Summary of Fit

Rsquare	0.945927
Root Mean Square Error	0.036798
Mean of Response	-0.48183
Observations (or Sum Wgts)	20



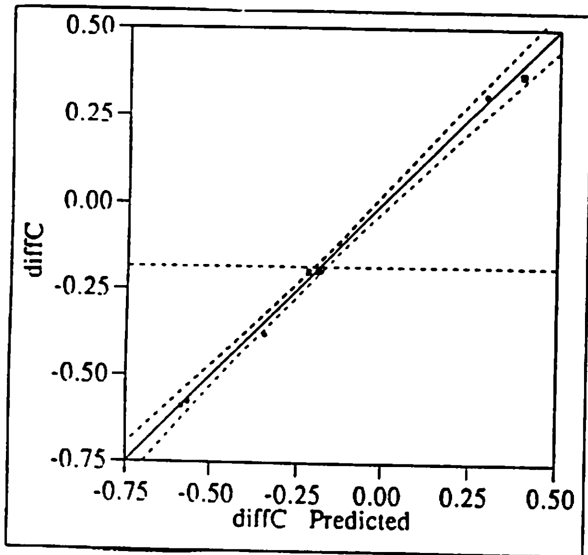
(b)

Figure 11 Model predicting DiffC as a function of DiffI

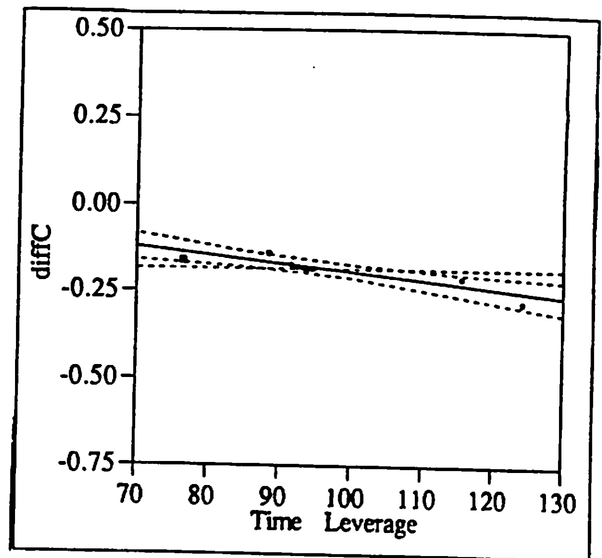
more pronounced for shorter channel lengths. Different die positions on the wafers, center and the middle of each of the four sides, have been examined. It is observed that there also exists a dependency on the die position on the wafer, both on X and Y positions. This is caused by the slight change of the implantation angle on the two opposite edges of the wafer. The implantation angle varies by two degrees between the two opposite edges in X direction. This shows how sensitive the asymmetrical characteristics are with respect to the implantation angle (Fig. 13).

4.1 Conclusion

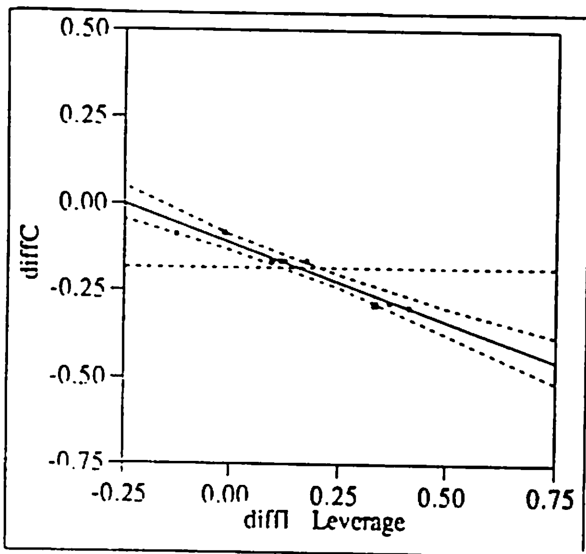
The method to estimate the overlap capacitance of MOSFET devices presented in this paper can be utilized in a fabrication process to enhance the device modeling. Since the speed of a device relatively depends on the gate to source/drain capacitance, this method can be employed to estimate the overlap capacitance of the MOSFET devices and improve the process of device binning based on speed performance [4]. Also, this method allows for a constant control of the overlap capacitance during wafer processing, and such readings can be used as feedback to control the process parameters in order to optimize the extent of the gate to source/drain overlap. Further study could be warranted using the standard plots of overlap capacitance versus saturation currents and substrate current [1] for a specific set of device process parameters.



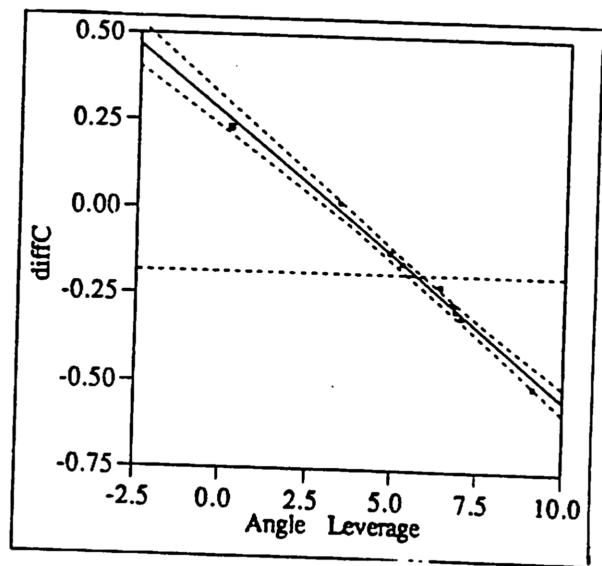
(a)



(b)

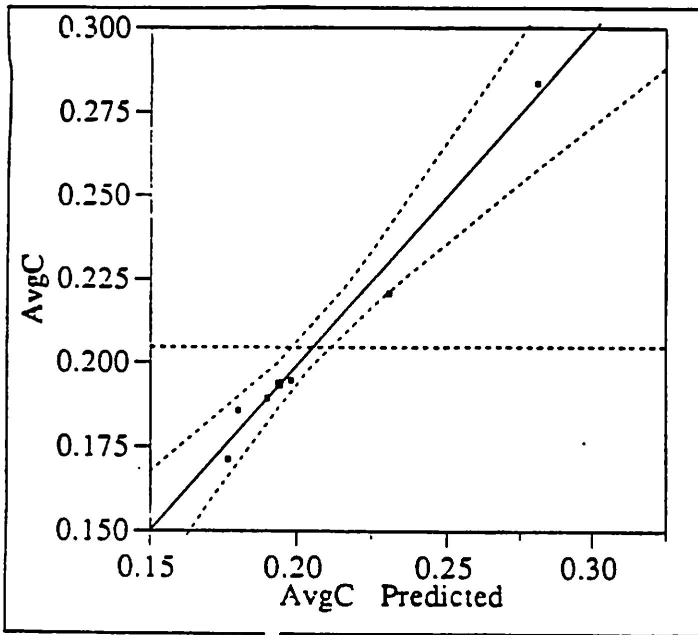


(c)



(d)

Figure 12 Model predicting DiffC as a function of DiffI and ion implantation angle



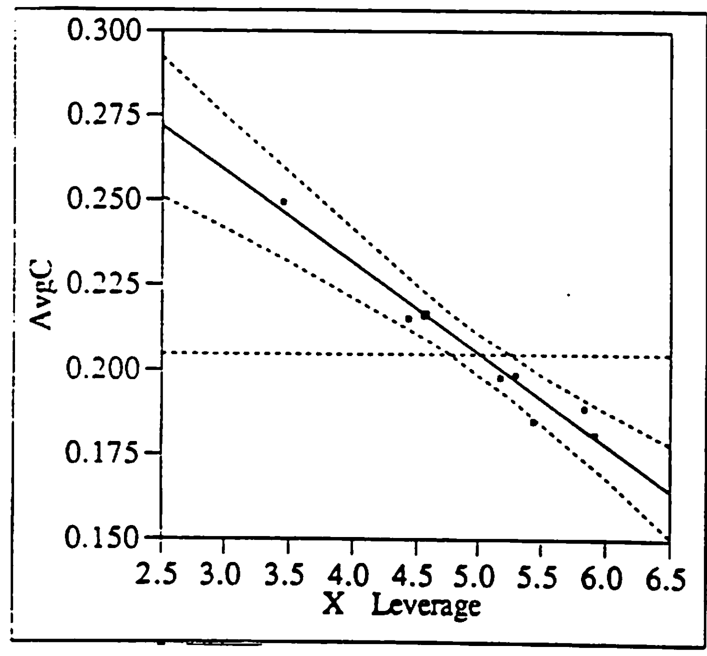
Parameter Estimates

Term	Estimate	Std Error	t Ratio	Prob>|t|
Intercept	0.9245507	0.08071	11.45	0.0003
X	-0.026834	0.00284	-9.44	0.0007
diffI	-0.63928	0.04442	-14.39	0.0001
AvgI	-0.015085	0.00206	-7.32	0.0019

Summary of Fit

Rsquare	0.982105
Root Mean Square Error	0.006157
Mean of Response	0.205081
Observations (or Sum Wgts)	8

(a)



(b)

Figure 13 Model predicting AvgC as a function of X position of the die on the wafer

References

[1] Tung-Yi P. Chan," Hot Electron Effects In VLSI MOSFET's",U.C. Berkeley, August 1986

[2] Richard S.Muller & Theodore I. Kamins, "Device Electronics For Integrated Circuits", John Wiley & Sons, New York 1987

[3] Shyh Wang," Fundamentals of Semiconductor Theory And Device Physics", Prentice Hall, 1989

[4] E. Boskin, G. Korsh & C. Spanos, "Ic Performance Prediction From Electrical Test Measurements", International Semiconductor Sciences Symposium, San Francisco, CA, June 1992

Appendix

Rows	AvgI	DiffI	Cgd	Cgs	AvgC	DiffC	DriveIn
x 1	34.685	0.02104656	0.28178947	0.28663158	0.28421053	-0.017037	80
2	36.725	0.10810075	0.16621053	0.22289474	0.19455263	-0.2913567	80
3	33.025	0.22316427	0.14184211	0.20236842	0.17210526	-0.351682	80
4	36.525	0.07255305	0.16842105	0.222	0.19521053	-0.2744675	80
5	35.695	0.08488584	0.17157895	0.21993158	0.19575526	-0.2470055	80
6	34.745	0.01525399	0.19763158	0.24584211	0.22173684	-0.2174223	80
7	35.185	0.06792667	0.16723684	0.21322632	0.19023158	-0.2417552	80
x 8	33.23	0.12879928	0.18065789	0.19302632	0.18684211	-0.0661972	80
9	31.2	0.80192308	0.06881579	0.13197368	0.10039474	-0.6290957	120
10	28.475	0.6071993	0.07171053	0.12473684	0.09822368	-0.5398526	120
11	31	0.73806452	0.07131579	0.12302632	0.09717105	-0.5321598	120
12	31.985	0.77317493	0.07039474	0.14723684	0.10881579	-0.7061669	120
13	30.17	0.59728207	0.07197368	0.12552632	0.09875	-0.5423051	120
14	30.435	0.53063907	0.07434211	0.12342105	0.09888158	-0.4963407	120
x 15	30.63	0.32190663	0.08105263	0.14763158	0.11434211	-0.5822785	120
16	30.325	0.68821105	0.07197368	0.12986842	0.10092105	-0.5736636	120
17	27.845	0.66834261	0.06842105	0.12368421	0.09605263	-0.5753425	120
18	31.505	0.90684018	0.06526316	0.12618421	0.09572368	-0.6364261	120
19	31.43	0.88641425	0.06723684	0.12657895	0.09690789	-0.6123557	120
x 20	30.845	0.26292754	0.08815789	0.15276316	0.12046053	-0.536319	120
21	30.455	0.77327204	0.06671053	0.12671053	0.09671053	-0.6204082	120
22	27.95	0.67191413	0.06776316	0.12302632	0.09539474	-0.5793103	120
23	30.11	0.68482232	0.06934211	0.11868421	0.09401316	-0.5248425	120
24	31.275	0.33988809	0.07802632	0.12263158	0.10032895	-0.4445902	120

x = points excluded as statistical outlyiers

SUMMARY OF MEASUREMENTS

::::::::::::::
waferL4_0_120
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NMOS14-4 IMPLANTATION ANGLE=0 DEGREE DRIVE-IN TIME=120 MIN

X	Y	W	L	Id	Is	Cgd/10	Cgd/200	Cgs/10	Cgs/200
3	3	100	0.5	52.60	53.67	18.44	52.32	22.04	61.18
3	4	100	0.5	49.82	48.62				
3	5	100	0.5	47.98	49.43				
3	6	100	0.5	43.98	44.67				
4	3	100	0.5	48.95	51.15				
4	4	100	0.5	49.01	50.58	18.92	54.84	21.94	64.74
4	5	100	0.5	47.22	49.92				
4	6	100	0.5	44.35	45.20				
5	3	100	0.5	46.42	48.75				
5	4	100	0.5	46.46	50.38				
5	5	100	0.5	47.05	49.18	18.46	53.1	22.24	61.72
5	6	100	0.5	41.18	45.08				
6	3	100	0.5	46.42	49.16				
6	4	100	0.5	46.58	49.63				
6	5	100	0.5	40.79	44.90				
6	6	100	0.5	40.25	45.01	18.64	52.34	22.02	60

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waferL5_7_120
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NMOS14-5 IMPLANTATION ANGLE=7 DEGREE DRIVE-IN TIME=120 MIN

X	Y	W	L	Id	Is	Cgd/10	Cgd/200	Cgs/10	Cgs/200
3	3	100	0.5	44.62	49.11	19.1	58.26	22.28	63.56
3	4	100	0.5	46.71	47.85				
3	5	100	0.5	41.79	45.36				
3	6	100	0.5	38.68	42.01				
4	3	100	0.5	42.83	46.19				
4	4	100	0.5	47.02	49.82	19.5	56.42	21.68	56.76
4	5	100	0.5	43.43	46.00				
4	6	100	0.5	37.97	41.14				
5	3	100	0.5	41.29	44.78				
5	4	100	0.5	43.67	46.16				
5	5	100	0.5	40.81	46.26	18.8	58.22	21.98	59.34
5	6	100	0.5	37.36	42.15				
6	3	100	0.5	37.06	44.66				
6	4	100	0.5	43.20	45.33				
6	5	100	0.5	37.75	44.81				
6	6	100	0.5	38.21	44.04	19.2	55.92	22.7	56

::::::::::::::
waferN1_0_120
::::::::::::::

NMOS12-1 IMPLANTATION ANGLE=0 DEGREE DRIVE-IN TIME=120 MIN

X	Y	W	L	Id	Is	Cgd/10	Cgd/200	Cgs/10	Cgs/200
3	3	50	0.5	16.06	16.71				
3	4	50	0.5	17.07	16.67				
3	5	50	0.5	16.80	16.63				
3	6	50	0.5	17.12	16.73				
4	3	50	0.5	17.17	16.97				
4	4	50	0.5	16.70	16.85	16	43.92	24.8	44.66
4	5	50	0.5	17.21	16.99				
4	6	50	0.5	16.57	16.60				
5	3	50	0.5	16.63	17.18				
5	4	50	0.5	15.85	16.35				
5	5	50	0.5	17.15	17.18	17.1	46.08	20.68	41.92
5	6	50	0.5	16.57	17.06				
6	3	50	0.5	17.03	17.46				
6	4	50	0.5	16.83	17.47				
6	5	50	0.5	16.15	17.17				
6	6	50	0.5	16.86	17.16	18.6	45.58	19.78	39.8

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waferN2_7_120
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NMOS12-2 IMPLANTATION ANGLE=7 DEGREE DRIVE-IN TIME=120 MIN

X	Y	W	L	Id	Is	Cgd/10	Cgd/200	Cgs/10	Cgs/200
3	3	100	0.5	43.71	18.69	4.100	17.175	13.775	38.850
3	4	100	0.5	37.12	19.83	4.050	17.675	13.325	37.025
3	5	100	0.5	42.44	19.56	4.425	17.975	13.525	36.900
3	6	100	0.5	44.35	19.62	4.300	17.675	13.350	41.325
4	3	100	0.5	39.18	21.16	4.525	18.200	13.950	37.800
4	4	100	0.5	38.51	22.36	4.450	18.575	14.425	37.875
4	5	100	0.5	35.56	25.70	4.450	19.850	13.525	41.575
4	6	100	0.5	40.76	19.89	4.275	17.950	13.525	38.200
5	3	100	0.5	37.15	18.54	4.325	17.325	13.575	37.075
5	4	100	0.5	45.79	17.22	4.350	16.750	13.575	37.550
5	5	100	0.5	45.36	17.50	4.175	16.950	13.850	37.900
5	6	100	0.5	34.90	26.79	4.250	21.000	12.850	41.875
6	3	100	0.5	42.23	18.68	4.250	16.925	12.500	36.575
6	4	100	0.5	37.34	18.56	4.325	17.200	13.150	36.525
6	5	100	0.5	40.42	19.80	4.375	17.550	13.300	35.850
6	6	100	0.5	36.59	25.96	4.425	19.250	14.150	37.450
3	3	50	0.5	22.32	9.666	17.08	32.14	19.94	55.96
3	4	50	0.5	21.49	9.903				
3	5	50	0.5	20.75	8.915				
3	6	50	0.5	22.31	8.090				
4	3	50	0.5	20.43	10.84				
4	4	50	0.5	19.50	11.21	15.98	35.06	21.58	55.04
4	5	50	0.5	18.95	13.49				
4	6	50	0.5	19.99	8.954				
5	3	50	0.5	21.21	9.681				
5	4	50	0.5	22.98	8.900				
5	5	50	0.5	22.92	8.695	16.74	33.4	21.28	54.04
5	6	50	0.5	18.63	12.80				
6	3	50	0.5	21.12	9.438				
6	4	50	0.5	21.47	9.433				
6	5	50	0.5	20.22	10.01				
6	6	50	0.5	19.05	13.26	16.98	38.7	20.92	51.26

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waferN3_0_120
::::::::::::::

NMOS12-3 IMPLANTATION ANGLE=0 DEGREE DRIVE-IN TIME=120 MIN

X	Y	Cgd/10	Cgd/200	Cgs/10	Cgs/200
3	3	17.88	50.76	21.44	55.7
4	4	17.9	51.96	21.76	53.42
5	5	18.06	51.28	21.36	51.78
6	6	18.28	47.76	21.48	51.62

::::::::::::::
waferN4_7_120
::::::::::::::

NMOS12-4 IMPLANTATION ANGLE=7 DEGREE DRIVE-IN TIME=120 MIN

X	Y	W	L	Id	Is	Cgd/10	Cgd/200	Cgs/10	Cgs/200
3	3	100	0.5	33.49	33.40	5.480	43.780	7.780	54.680
3	4	100	0.5	35.58	35.84				
3	5	100	0.5	38.05	36.97	6.810	39.200	10.880	51.400
3	6	100	0.5	38.60	37.08				
4	3	100	0.5	38.41	35.24				
4	4	100	0.5	33.55	32.35	7.350	31.137	10.650	45.060
4	5	100	0.5	40.64	32.42				
4	6	100	0.5	39.11	34.10	6.425	32.150	12.380	44.300
5	3	100	0.5	38.61	31.14	6.975	29.712	12.287	45.175
5	4	100	0.5	39.94	31.83				
5	5	100	0.5	39.47	31.04	6.760	28.250	11.225	44.380
5	6	100	0.5	39.43	33.57				
6	3	100	0.5	37.76	30.43				
6	4	100	0.5	38.73	29.92	5.880	27.180	11.825	43.813
6	5	100	0.5	38.88	31.23				
6	6	100	0.5	39.27	28.74	5.575	26.600	11.462	42.775
3	3					16.58	45.76	21.4	68.7
4	4					17.02	40.08	21.82	55.3
5	5					17.68	36.52	21.32	54.64
6	6					17.18	32.88	21.08	53.42

::::::::::::::
waferN7_7_80
::::::::::::::

NMOS12-7 IMPLANTATION ANGLE=7 DEGREE DRIVE-IN TIME=80 MIN

X	Y	W	L	Id	Is	Cgd/10	Cgd/200	Cgs/10	Cgs/200
4	2	100	0.5	35.05	34.32	6.800	60.340	13.150	67.610
4	3	100	0.5	33.35	32.88				
4	4	100	0.5	38.71	34.74	6.290	37.870	12.510	54.860
4	5	100	0.5	38.02	34.88				
4	6	100	0.5	36.71	29.34	6.225	33.175	12.510	50.960
4	8	100	0.5			6.450	44.187	12.587	61.800
5	2	100	0.5	35.71	34.98				
5	3	100	0.5	37.85	35.20	6.625	38.625	12.660	54.840
5	4	100	0.5	37.83	36.12				
5	5	100	0.5	37.21	34.18	6.275	38.875	12.325	54.112
5	6	100	0.5	35.52	31.73				
5	7	100	0.5			6.188	39.788	12.350	53.725
6	2	100	0.5	35.01	34.48	6.750	44.300	12.940	59.650
6	3	100	0.5	36.72	34.35				
6	4	100	0.5	36.38	33.99	6.425	38.200	12.550	53.063
6	5	100	0.5	36.30	33.51				
6	6	100	0.5	35.37	31.09	6.250	40.575	12.013	48.688
6	8	100	0.5			6.313	37.563	12.163	53.175
7	3	100	0.5			6.900	38.175	11.725	50.088
7	5	100	0.5			6.163	35.250	12.088	48.025
7	7	100	0.5			6.088	35.938	11.663	49.138
8	4	100	0.5			6.825	37.450	11.800	49.888
8	6	100	0.5			6.088	32.013	11.288	45.800
4	2	10	0.5	2.802	2.843				
4	2	200	0.5	69.72	69.48				
4	2	10	0.7	2.418	2.444				
4	2	200	0.7	59.56	59.89				
4	4	10	0.5	3.129	3.190				
4	4	200	0.5	69.58	78.11				
4	4	10	0.7	2.679	2.709				
4	4	200	0.7	63.72	65.16				
4	6	10	0.5	3.145	3.020				
4	6	200	0.5	56.45	73.91				
4	6	10	0.7	2.635	2.634				
4	6	200	0.7	63.12	57.57				
4	8	10	0.5	2.887	2.962				
4	8	200	0.5	67.27	69.74				
4	8	10	0.7	2.563	2.598				
4	8	200	0.7	58.48	58.94				
5	3	10	0.5	3.074	3.024				
5	3	200	0.5	77.62	71.15				
5	3	10	0.7	2.608	2.591				
5	3	200	0.7	62.56	63.47				
5	5	10	0.5	3.107	3.016				
5	5	200	0.5	74.68	69.64				
5	5	10	0.7	2.662	2.632				
5	5	200	0.7	62.07	62.30				
5	7	10	0.5	2.861	2.967				
5	7	200	0.5	68.29	71.79				
5	7	10	0.7	2.544	2.598				
5	7	200	0.7	60.30	60.60				
6	4	10	0.5	2.993	2.980				
6	4	200	0.5	73.35	67.62				
6	4	10	0.7	2.489	2.539				
6	4	200	0.7	60.94	62.20				
6	6	10	0.5	4.256	3.887				
6	6	200	0.5	70.64	61.98				
6	6	10	0.7	2.271	2.564				
6	6	200	0.7	58.32	59.74				
6	8	10	0.5	3.079	2.997				
6	8	200	0.5	66.33	60.59				
6	8	10	0.7	2.750	2.704				
6	8	200	0.7	56.72	56.26				
7	3	10	0.5	2.938	2.929				
7	3	200	0.5	67.12	64.79				
7	3	10	0.7	2.559	2.547				
7	3	200	0.7	57.74	59.88				
7	5	10	0.5	3.079	3.002				
7	5	200	0.5	70.21	61.91				
7	5	10	0.7	2.548	2.603				
7	5	200	0.7	59.16	59.21				
7	7	10	0.5	3.024	2.936				
7	7	200	0.5	60.81	59.85				
7	7	10	0.7	2.662	2.616				
7	7	200	0.7	56.91	54.27				
8	4	10	0.5	2.718	2.935				
8	4	200	0.5	59.77	60.37				
8	4	10	0.7	2.646	2.638				
8	4	200	0.7	55.01	55.41				
8	6	10	0.5	3.072	2.794				
8	6	200	0.5	65.94	49.08				

8	6	10	0.7	2.703	2.533				
8	6	200	0.7	55.74	42.19				
4	4					16.54	47.34	21.48	56.64
5	5					16.22	47.42	22.08	53.24
6	6					16.16	43.94	22.04	49.2

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waferN8_0_80
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NMOS14-4 IMPLANTATION ANGLE=0 DEGREE DRIVE-IN TIME=120 MIN

X	Y	W	L	Id	Is	Cgd/10	Cgd/200	Cgs/10	Cgs/200
3	3	100	0.5	32.31	32.33	16.84	65.02	21.96	59.88
3	4	100	0.5	35.62	35.65				
3	5	100	0.5	38.95	39.17				
3	6	100	0.5	38.32	38.34				
4	3	100	0.5	31.98	31.23				
4	4	100	0.5	37.23	38.54	16.9	61.6	21.94	51.0
4	5	100	0.5	38.51	38.76				
4	6	100	0.5	37.24	38.41				
5	3	100	0.5	36.49	36.85				
5	4	100	0.5	37.61	38.48				
5	5	100	0.5	37.64	38.44	16.82	58.12	21.72	47.3
5	6	100	0.5	33.57	38.44				
6	3	100	0.5	34.89	36.98				
6	4	100	0.5	35.35	37.69				
6	5	100	0.5	35.41	38.56				
6	6	100	0.5	34.47	37.53	17.08	51.24	21.5	44.88