SUPERCONDUCTING FLASH-TYPE ANALOG-TO-DIGITAL CONVERTERS WITH MULTI-GIGAHERTZ PERFORMANCE

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Memorandum No. UCB/ERL M94/61

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Abstract

Superconducting Flash-Type Analog-To-Digital Converters With Multi-Gigahertz Performance

by

Howard Cam Luong

Doctor of Philosophy in Electrical Engineering and Computer Science
University of California at Berkeley
Professor Theodore Van Duzer, Chair

This dissertation presents the design, fabrication, and testing of a fully parallel analog-to-digital converter in Josephson technology that can operate at multi-gigahertz clock and input frequencies with a total power consumption less than 1mW. Compared to the best analog-to-digital converters available in semiconductor technology, this converter performs at least one order of magnitude better in terms of both speed and power consumption.

One-junction SQUIDs (Superconducting Quantum Interference Devices) are used to introduce very sharp, narrow pulses to the comparators to achieve a very small aperture time for the converter. With a junction critical current density of 1 kA/cm^2, an aperture time as small as 4 ps can be achieved, which makes it feasible to implement a high-performance ADC with 10 GHz clock frequency, 5 GHz input bandwidth, and 4-bit resolution. A completely new ultra-fast logic family, capable of operating at frequencies up to 12.5 GHz, has also been designed based on the comparator building block and has been used to implement the thermometer-to-binary encoder required for the flash ADC.

The comparators and the logic gates have been fully tested, and their correct operations have been verified experimentally at clock frequencies up to 3 GHz, which is limited by our existing test equipment. A three-bit quantizer and a three-bit thermometer-to-binary encoder have been successfully demonstrated. However, due to the process variations in junction critical currents, circuits with larger sizes and more complexity, including a four-bit quantizer, a three-bit ADC, a four-bit ADC, and a pseudo-random bit sequence generator, were only partially functional. All design and testing issues at multi-gigahertz frequencies are discussed and possible approaches are proposed.

Finally, as an outline for potential future research, the last part of the dissertation discusses our work on another fully parallel ADC originally designed by Petersen and our preliminary study on the feasibility of implementing an ADC with higher resolution using a multi-step subranging architecture.

T. Van Duzer

Chairman of committee

To my parents and my siblings

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Chapter 1

INTRODUCTION

1.1 Background and Motivation

Within last ten years or so, the digital world has been advanced continuously and rapidly to an extent that people have started wondering whether the whole world will turn purely digital and whether there will be a place for analog circuit designers in the future. Whether this becomes true or not, it is unquestionable that most of the real signals we are dealing with are analog, and thus there is always a need to build high-performance circuits to interface between analog and digital worlds. To keep up with the fast and steady improvement of technologies and circuit performance in the two worlds, not only in speeds and levels of complexity but also in power consumption, it is clearly indispensable to conceive interfacing circuits with higher and higher performance. This project is to design, fabricate, and test a superconducting analog-to-digital converter that can work up to multi-gigahertz clock frequencies and input bandwidths and at the same time consume only few milliwatts. Compared to the best semiconductor analog-to-digital converters available, this converter performs at least one order of magnitude better in terms of speed and few orders of magnitude less in terms of active power consumption.

1.2 Thesis Organization

This thesis is organized into ten chapters. This chapter introduces the background and the motivation of the project and describes the organization of the thesis. Chapter 2 gives a brief review of existing and widely used architectures for analog-to-digital converters, including their basic designs and their advantages and disadvantages compared to other architectures. Among those available for semiconductor technology are serial-type, successive approximation, flash-type, multi-step subranging, and pipelined architectures. Chapter 3 discusses in full detail why superconducting technology has been chosen for our project over semiconductor technologies, which undoubtedly are much better developed and more mature. Fundamentals of Josephson junctions that are closely related to the specific designs of our converter prototype will be described. For comparison and for completeness, periodic-threshold designs of a flash-type analog-to-digital converter, which is quite unique and available only to optical and superconducting devices, will be presented.

In Chapter 4, we will focus our discussion on the design and fabrication of a prototype for a fully parallel superconducting analog-to-digital converter, in particular the comparators for the quantizer and the logic gates for the thermometer-to-binary encoder. The complete converter's performance and functionalities, both at low speeds and high speeds, are verified and reported in Chapter 5. In Chapter 6, we will describe how the new logic family presented in Chapter 4 has been modified to increase the speed up to 12.5 GHz. We will also present the fabrication and experimental results for a pseudo-random bit sequence generator (PRBSG) we designed to test the logic gates at their highest

possible speeds without strict requirement of synchronous high-speed input and clock signals.

Chapter 7 addresses all issues that need to be considered and treated appropriately in designing and testing circuits at mutli-gigahertz operating frequencies, including problems with crosstalk, clock distribution, and testing at high speeds and at low temperatures. Problems and solutions that are applicable not only to our particular superconducting design but also to semiconductor high-speed circuits will be mentioned in great detail.

Chapter 8 reviews another design of a fully parallel analog-to-digital converter using bridge-type current-latched comparators and reports our progress. In Chapter 9, we study the feasibility of implementing a multi-step subranging analog-to-digital converter in superconducting technology to achieve high resolution without imposing too much restriction on process variations or sacrificing too much hardware. Possible implementations of required components, mainly digital-to-analog converters (DACs), sample-and-hold circuits, subtractors, and amplifiers, will be proposed together with preliminary simulation results.

In Appendix A, we present in detail how SQUID threshold curves can be calculated. Application of the Lagrange multiplier method to derive the threshold curve for a superconducting loop will be illustrated. Appendix B describes how performance of an ADC is evaluated at very high speeds. C programs used for automatic layout generation and for data acquisition and analysis are included in Appendix C. Finally, Appendix D presents our design and test setup to demagnetize the shield before each test.

Chapter 2

OVERVIEW OF ADC ARCHITECTURES

In general, analog-to-digital converters (ADCs) are characterized and evaluated by their bit resolution (accuracy) and their sampling rate (conversion speed). Depending on the application, the required converters can have resolution ranging from four to sixteen bits and conversion rate ranging from few hundred samples per second to several hundred mega-samples per second. As examples, applications in telephony and instrumentation require converters with very high resolution and accuracy but with sampling rates in the audio range. On the other hand, video interfaces and radar applications require converters with very high speed performance but with low bit resolution.

As an alternative to the sampling rate, an ADC can be characterized by its maximum input bandwidth. Maximum input bandwidth can be interpreted as a frequency at which signal attenuation and phase shift become significantly large. Ideally, an ADC should be able to achieve a maximum input frequency at the Nyquist rate, which is half of the clock frequency. However, in practice, due to limitations of circuit components and design at high speed, most of existing ADCs have maximum input bandwidths being far below their Nyquist rate.

Assuming that the frequency response of an ADC is dominated by a single pole, the attenuation factor A(f) as a function of frequency is given by:

Assuming that the frequency response of an ADC is dominated by a single pole, the attenuation factor A(f) as a function of frequency is given by:

$$A(f) = \frac{A_0}{\sqrt{1 + (f/f_C)^2}} \tag{1.1}$$

where A_0 is the dc gain and f_c is the maximum input bandwidth. The phase shift $\theta(f)$ is:

$$\theta(f) = \arctan\left(\frac{f}{f_C}\right) \tag{1.2}$$

and the time shift error Δt (f) is:

$$\Delta t(f) = \frac{\theta(f)}{360°}\frac{1}{f} = \frac{1}{360f}\arctan\left(\frac{f}{f_C}\right) \tag{1.3}$$

Overall, given a perfect sinusoidal input signal $V_{in}(t) = \sin\omega t$, the output $V_{out}(t)$ of an ADC with a maximum input bandwidth limited to f_c becomes:

$$V_{out}(t) = \frac{A_0}{\sqrt{1 + (f/f_C)^2}}\sin\left[\omega t + \arctan\frac{f}{f_C}\right] \tag{1.4}$$

As an example, to maintain a peak accuracy of 8 bits, that is A(f) < 0.4%, it is necessary from Eq. (1.1) that the maximum input bandwidth f_c should be at least 10 times larger than the operating frequency f.

According to their performance, analog-to-digital converters can be divided into three different categories: high resolution and low speed, low resolution and high speed, or relatively high resolution and relatively high speed. As far as architectures are concerned, they can be classified according to how the analog signals are sampled and quantized to

achieve the digital outputs. Figure 2.1 shows a comparison of performance of available architectures, namely the bit resolution and the speed in terms of number of clock cycles per conversion.

At one extreme, serial converters have ultra high resolution but require 2^N clock cycles per conversion. At the other extreme, flash-type ADCs take only one clock cycle per conversion but have limited resolution. Compromising between these two extremes are converters with multi-step architectures, including successive approximation, which requires N clock cycles, and subranging or pipelined, which requires anywhere between 1 and N cycles, depending on the specific implementation.

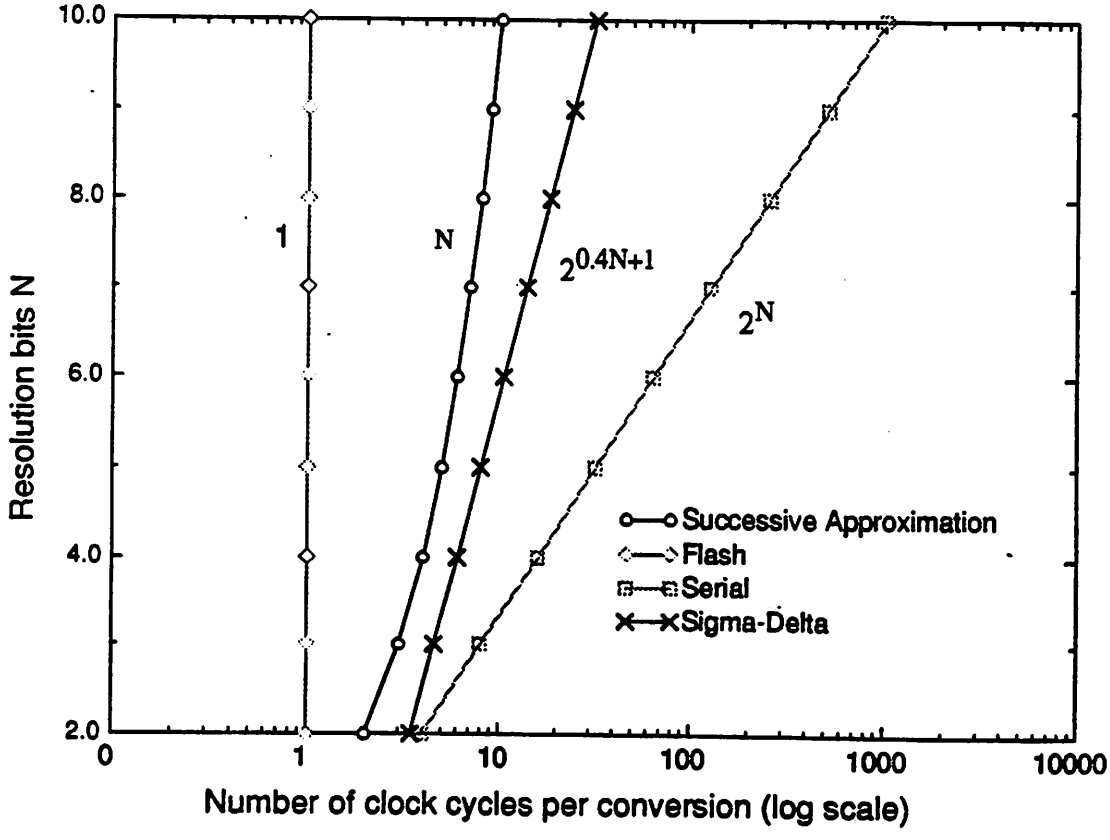


Fig. 2.1 Bit resolution vs. speed of various ADC architectures (from [1]).

The rest of this chapter will give brief overview of each architecture, emphasizing basic implementation and fundamental advantages and disadvantages.

2.1 Serial-Type (Integrating) Analog-To-Digital Converter

High-resolution and low-speed analog-to-digital conversion can be achieved by the integrating or serial-type architecture, in which the analog input signal is compared to all possible digital representations of the output codes *one at a time* [2] [3]. Figure 2.2 shows the simplest implementation of the architecture, in which the input signal is compared to a slowly ramping signal. At the beginning of each conversion, the START

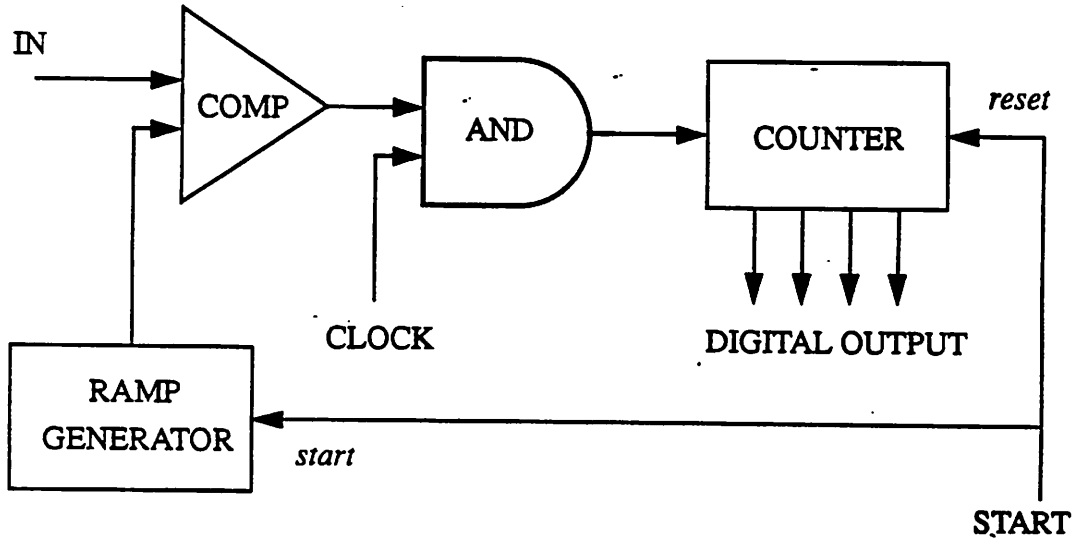


Fig. 2.2 Architecture for integrating (serial-type) analog-to-digital converter

signal resets the counter and triggers the ramping generator. As long as the generator output is smaller than the input signal, the output of the comparator is high, the clock is fed through the AND gate, the counter is enabled and the output is counted up. Once the

ramping signal equals or exceeds the input signal, the output of the comparator goes low, which deactivates both the counter and the ramping generator. The output of the counter is the total number of clock cycles required for the ramping signal to reach the input signal and thus reflects the digital representation of the input signal. The exact magnitude of the input can be calculated from the slew rate of the ramp generator, the cycle time, and the number of cycles required for the conversion.

The advantage of this architecture is that it is very simple and requires the least hardware. Since the operation depends on the ramping signal, the converter is inherently monotonic. It requires an implementation of a very linear ramping generator, and as far as the conversion speed is concerned, it takes 2^N clock cycles for each conversion and is therefore too slow to be practical in most applications.

2.2 Parallel (Flash) Analog-To-Digital Converter

The fastest conversion rate can be achieved by using the flash-type converter, in which the analog signal is compared to all digital output codes *simultaneously*, as opposed to *one at a time* as in a serial ADC [2] [3]. As shown in Fig. 2.3, a converter with N-bit resolution consists of 2^N-1 comparators to sample the analog input and a binary encoder to convert the thermometer outputs of the comparators into the corresponding binary format. Typically, a resistor string is used to provide 2^N-1 linearly graded reference levels to the comparators. The output of each comparator will be high if the input is larger than its reference, and as a result, a thermometer-coded output is achieved.

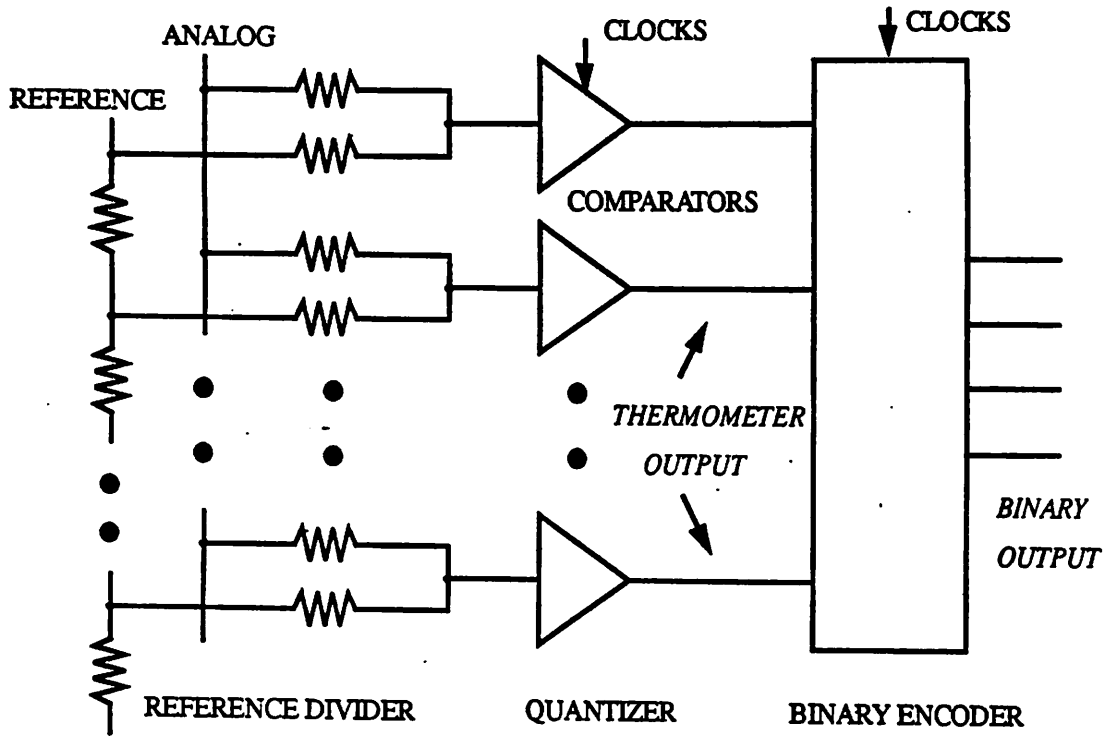


Fig. 2.3 Fully parallel (flash) analog-to-digital converter

This architecture yields the highest conversion rate, which was mainly the motivation for this work and will be described in full detail in subsequent chapters. However, the converter is relatively complex, and since the number of comparators is exponentially dependent on the resolution bits, it requires very large area, hardware, and power consumption. Another problem with this type of converter is its low resolution due to the large number of comparators, the offsets of the comparators, and the accuracy of the reference ladder network.

2.3 Successive-Approximation Analog-To-Digital Converter

By comparing the input to the output codes in a *binary-search* algorithm, successive approximation architecture can compromise between the speed and the resolution to achieve faster conversion rate than the serial type and higher resolution than the flash type [2] [3]. Figure 2.4 shows the simplified block diagram of the converter.

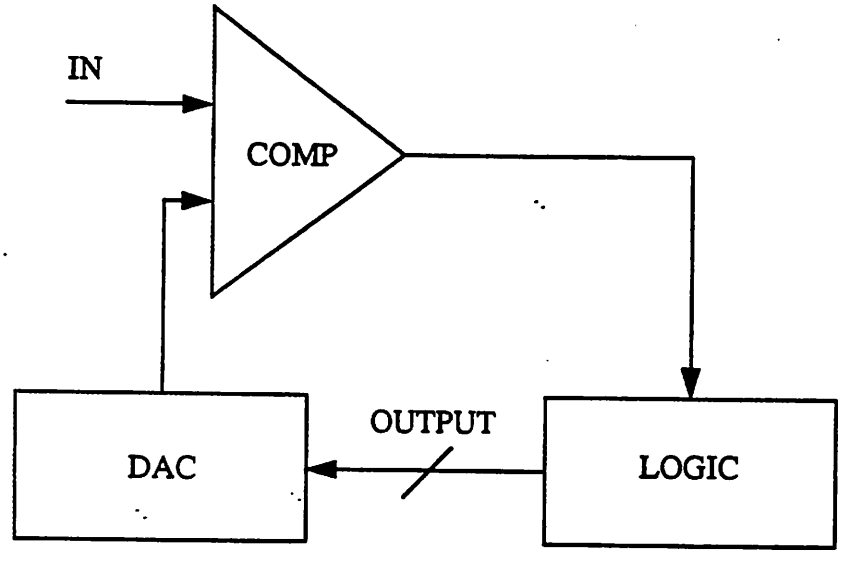


Fig. 2.4 Architecture for successive-approximation analog-to-digital converter

The function of the logic block is to select, in a binary-search format, appropriate digital codes for the DAC input, which are also the output of the whole ADC. At the start of a conversion, the logic block selects an input to the DAC such that half of the full-scale reference signal is applied to the comparator and compared to the analog input signal. If this signal is smaller than the input signal, the first digital output is high and the next higher level will be selected. Otherwise, the first digital output is low, and the output of the

DAC will be decreased to the next lower level. By successively increasing or decreasing the DAC output in a binary-search format, *one bit is achieved after one comparison*, and an N-bit resolution is achieved after N clock cycles.

Illustrated in Fig. 2.5 is an example of how a three-bit converter operates. The analog input is chosen to be approximately 11/16 of V_{ref}. In the first cycle, $V_{ref}/2$ is asserted at the DAC output. Since it is smaller than the input, the digital output D_0 is set to 1, and the DAC output is increased to 3/4 V_{ref}. Because this signal is larger than the input, the next digital bit D_1 is set to 0, and the DAC output is decreased to 5/8 V_{ref}. The comparator detects that the DAC output is now smaller than the input and sets D_2 to 1.

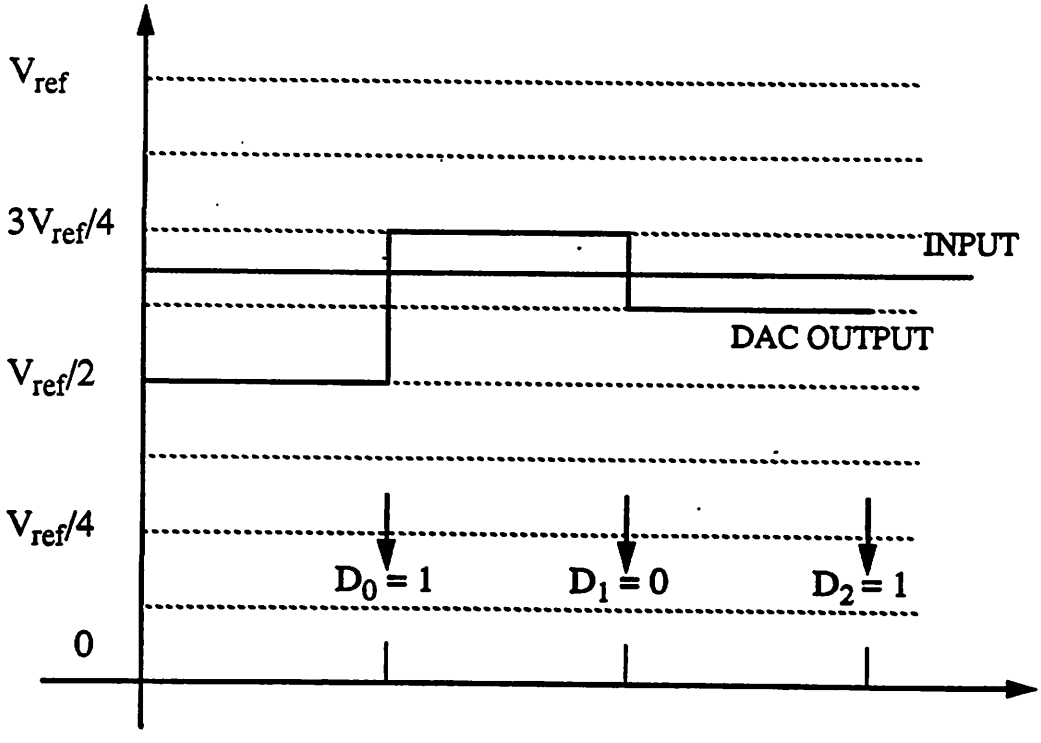


Fig. 2.5 Example of a three-bit successive approximation.

This architecture is relatively simple and requires very little hardware. The number of clock cycles per conversion is N. The main problem is that a very linear and accurate digital-to-analog converter is necessary.

2.4 Multi-Step Subranging Analog-To-Digital Converter

To alleviate the complexity and to increase the resolution of a flash-type ADC without sacrificing too much speed, multi-step subranging architecture can be used [3] [4].

Figure 2.6 shows the implementation of the converter. Basically, this subranging architecture is a combination of the flash and the successive approximation that breaks an

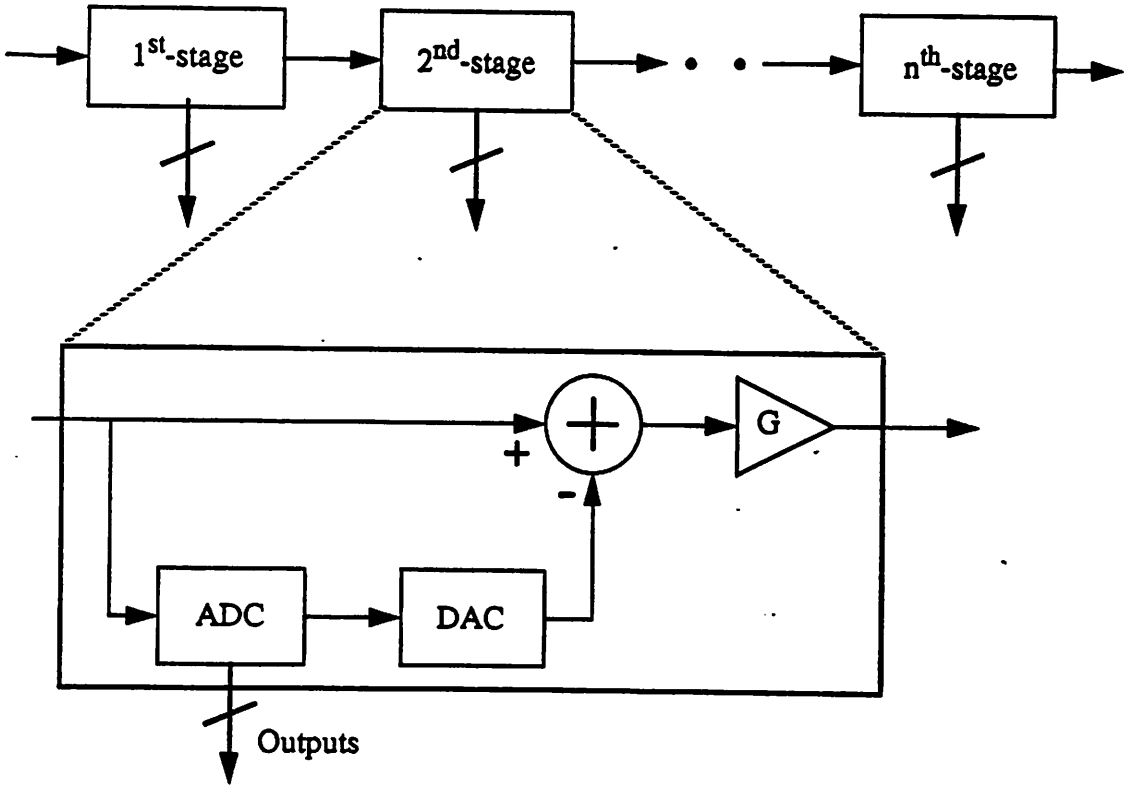


Fig. 2.6 Multi-step subranging ADC architecture

N-bit conversion into M sub-conversions of N/M bits each. The converter consists of several cascaded stages, each of which includes a low-resolution analog-to-digital converter to achieve a coarse estimation of the input, an accurate digital-to-analog converter (DAC) to convert the output of the ADC into an analog version of the estimation, a subtractor to get the residue (the difference between the actual input and its estimation), and a gain block to amplify and to restore the residue to an appropriate level for further estimation by the next stage.

As an illustration, Fig. 2.7 shows the operation of a 6-bit subranging converter that has three cascaded stages, each of which consists of a two-bit ADC, a two-bit DAC, and an amplifier with a gain of 4. The input is chosen to be approximately 77/128 V_{ref}. In the first stage, the two-bit ADC quantizes this input into $D_0D_1 = 10$, which is decoded by the DAC as 1/2 V_{ref}, and as a result, the residue becomes 13/128 V_{ref}. This residue is amplified by 4, becomes 13/32 V_{ref} and is passed to the second stage. Similarly, the second stage yields outputs D_2D_3 equal to 01 and a residue of 5/32 V_{ref}, and the third stage receives an input of 5/8 V_{ref} and results in outputs $D_4D_5 = 10$. All together, the digital output of the converter is 100110, which corresponds to 38/64 V_{ref}, and the overall error is 1/128 V_{ref}, which is equivalent to an accuracy of 1/2 LSB for 6-bit resolution.

Compared to the flash-type ADC with the same bit resolution, this architecture requires a much smaller number of comparators and thus consumes much less hardware and power. The ADCs can have low bit resolution, but all other components, including the DACs, gain amplifiers, and subtracters, need to be highly accurate. In particular, the amplifiers can limit the overall speed and resolution of the converter.

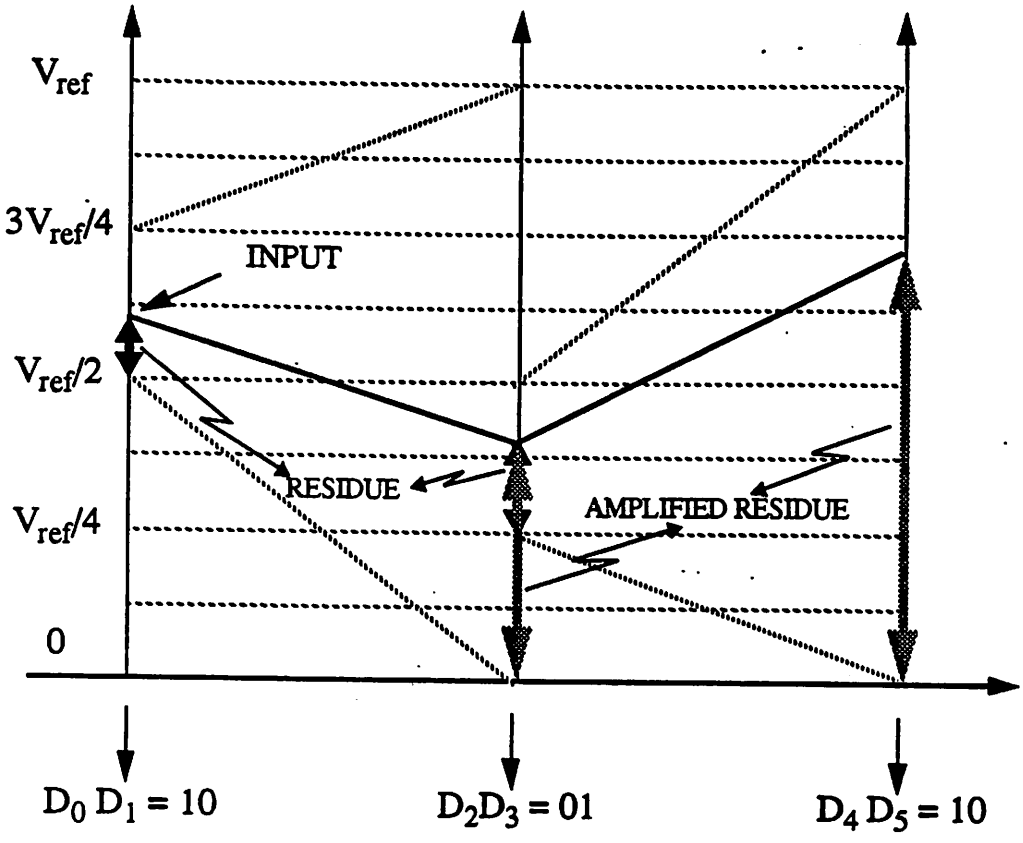


Fig. 2.7 Illustration of how a three-stage subranging ADC works

Feasibility of implementing a multi-step subranging ADC in a superconducting technology will be presented in Chapter 9. Problems in realizing all required components will be addressed, and possible solutions will be proposed.

2.5 Pipelined Analog-To-Digital Converter

The throughput of a multi-step subranging architecture can be further increased by pipelining the stages. Pipelined architecture is closely related to multi-step subranging except that sample-and-hold (S/H) circuits are added between stages [3] [5] as shown in

Fig. 2.8. With S/H, each stage can work on its input simultaneously and independently from each other. At any instant, while one stage processes the current input sample, the next stage works on the amplified residue of the previous input sample.

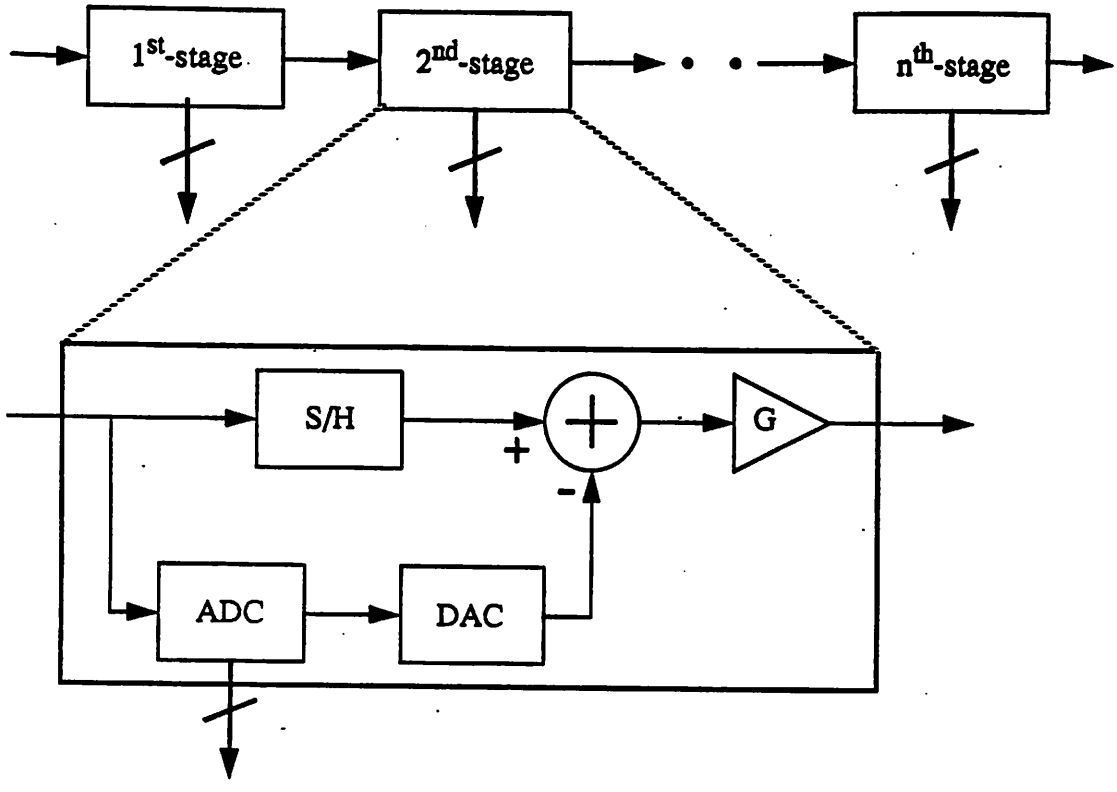


Fig. 2.8 Pipelined analog-to-digital converter architecture

Concurrent operation of the stages on many input samples results in a high throughput rate and a conversion speed independent of the number of cascading stages. In addition, like the subranging-type, this architecture requires fewer comparators, smaller area, and lower power consumption. The main disadvantage of the architecture is a limited speed due to a need of very high-performance amplifiers and sample-and-hold circuits.

Chapter 3

JOSEPHSON FLASH-TYPE ANALOG-TO-DIGITAL CONVERTERS

3.1 Motivation

Superconducting technology is very attractive for its ultra-high speed and low power. The switching time of a gate is few picoseconds, and the maximum voltage signal level is limited to the junction gap voltage, which is only around 2.6 mV. However, the technology is not as well developed as semiconductor counterparts, and the circuits need to be cooled down to very low temperature to work correctly. For example, niobium technology does not work until it is refrigerated below its critical temperature, which is 9.2 K. For these reasons, it is very hard for superconducting circuits to compete with semiconductor counterparts unless the circuit performance is at least an order of magnitude better. The belief that superconducting flash-type converters can operate at a conversion rate their counterparts in semiconductor can *never* reach has motivated much research in the field and in the architecture.

For comparison purposes, listed in Table 3.1 are ADCs that have been reported with the best performance. The first column lists the institution that performed the work, the date when the work was done, and the technology that was used. The second column

lists the reported effective bit resolution of the converter, including the effect of noise and distortion of the converter itself. The third, fourth, and fifth list the reported sampling frequency, the maximum measured input frequency, and the power consumption, respectively.

Table 3.1 Comparison of performance of the best analog-to-digital converter

Institution, Date (Technology)	Resolution (bits)	Sampling frequency (GHz)	Input frequency (GHz)	Power (W)
Fraunhofer, '92 (1 μm-GaAs)	4.4	1.00	0.500	4.30
Ruhr Univ., '87 (8 GHz-BJT)	3.5	1.00	0.500	2.40
NTT LSI, '88 (25.7 GHz-BJT)	4.7	1.00	0.500	2.00
Philips, '92 [6] (13 Ghz-BJT)	7.8	0.65	0.150	0.85
UCLA, '93 [7] (4 GHz-BJT)	9.5	0.10	0.050	0.80
Matshushita,'93 [8] (0.8 μm-CMOS)	10.0	0.02	0.002	0.03
NEC, '93 [9] (0.8 μm-BiCMOS)	8.0	0.10	0.050	0.95
This work, (Josephson)	4	10.00	5.000	0.005

Most of the semiconductor ADCs reported in our comparison have high resolution but low speed performance. In particular, those using a CMOS technology have resolution

as high as eight to ten bits and conversion rate as low as 20 MHz. Converters implemented with a bipolar technology can yield higher conversion speed but lower resolution. Those converters with advanced processes in GaAs and BJT can operate at one gigahertz clock frequencies, but their power consumption levels are several watts, which is disadvantageously large! For our superconducting work, the converter is expected to achieve a resolution of 4 bits, a maximum input bandwidth of 5 GHz, a clock frequency of 10 GHz, and at the same time to consume a power of only few milliwatts. Note that the powers listed in the table are the active power and that the power required for refrigeration is not included. Also, although much work has been done on superconducting comparators potentially used in ADCs, there has been no complete superconducting ADC ever reported. For this reason, no other superconducting ADC is included in the comparison

In order to compare the performance of converters with different applications and thus different ranges of resolutions and speeds, the aperture time τ_{ap}, defined as the time window in which a sinusoidal input signal applied to the converter can slew at most 1 LSB, has been used. For a sinusoidal input signal of the form $S_{in} = S_0 \sin(2\pi f_B t)$, the maximum slew rate MSR is $2\pi f_B S_0$ and is also equal to

$$MSR = 2\pi f_B S_0 = \frac{dS_{in}}{dt} = \frac{1LSB}{\tau_{ap}} \tag{3.1}$$

Therefore, the minimum time necessary for the input to slew 1 LSB can be derived to be:

$$\tau_{ap} = \frac{1LSB}{2\pi f_B S_0} = \frac{2S_0}{2\pi f_B S_0 2^n} = \frac{1}{\pi f_B 2^n} \tag{3.2}$$

where n is the bit resolution and f_B is the maximum input bandwidth. Qualitatively, the aperture time can be interpreted as a measurement of how well a converter can sample its input signal. The smaller the aperture time, the more precisely the converter samples the input, and the higher the performance the converter achieves.

In practice, power consumption of a converter can be and is actually sacrificed in many architectures to trade off for speed. To include the power consumption in the comparison of performance, the figure of merit FOM of a converter, defined as the product of the power consumption of the converter and its aperture time, has been widely used. With the aperture time given in Eq. (3.2), the figure of merit FOM can be simply calculated as

$$FOM = P\tau = \frac{P}{\pi f_B 2^n} \tag{3.3}$$

where P is the converter's active power consumption.

The corresponding aperture times and figures of merit of the converters mentioned in Table 3.1 are calculated and listed in the first two columns of Table 3.2. For clarification, performance of all semiconductor ADCs are normalized against that of the superconducting converter and listed in the last two columns, from which it can be seen that the potential performance (FOM) of superconducting ADCs is at least a few orders of magnitude better than its semiconductor counterparts.

Table 3.2 Aperture time and figure of merit of the converters listed in Table 3.1

Institution, Date (Technology)	Aperture (ps)	FOM (pJ)	Normalized Aperture	Normalized FOM
Fraunhofer, '92 (1μm-GaAs)	30.2	129.0	7.6	6,500
Ruhr Univ., '87 (8GHz-BJT)	56.3	135.0	14.1	6,800
NTT LSI, '88 (25.7GHz-BJT)	24.5	49.0	6.2	2,500
Philips, '92 (13Ghz-BJT)	9.5	7.6	2.4	380
UCLA, '93 (4GHz-BJT)	8.8	7.0	2.2	350
Matshushita,'93 (0.8μm-CMOS)	155	4.7	39.1	230
NEC, '93 (0.8μm-BiCMOS)	24.9	23.6	6.3	1,200
This work, (Josephson)	4	0.02	1	1

3.2 Fundamentals of Josephson Junctions

There are many different types of Josephson junctions, including the sandwich, the coplanar, and the point-contact types. However, the most popular and well-developed structure is the sandwich type. As shown in Fig. 3.1,a sandwich-type Josephson junction consists of two superconducting layers separated by a very thin insulating barrier. Today,

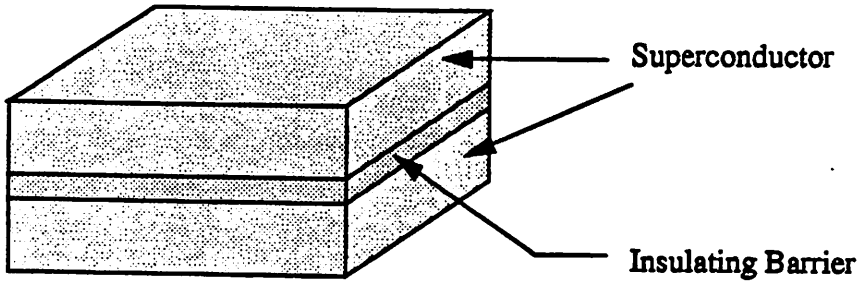


Fig. 3.1 Configuration of a sandwich-type Josephson junction.

in a typical Josephson process, the superconducting layers are Nb, and the insulting layer is 2.5 - 5.0 nm of Al_2O_3.

At low enough temperatures and with a thin enough insulating barrier, the wave functions of the two superconducting layers interact with each other. The so-called Cooper pairs can tunnel through the barrier even without any voltage drop across the junction. As a result, it is possible to have a current flowing through a Josephson junction without a voltage developed across it. This unique feature of the Josephson junction distinguishes it from all other devices and will be used extensively in designing interesting circuits.

Assuming that the wave function of each superconducting layer can be expressed in terms of the pair density n_s and the phase θ as

$$\psi = n_s^{1/2} e^{i\theta} \tag{3.4}$$

the Josephson relations can be derived to be as follows [10]

$$I = I_c \sin\phi \tag{3.5}$$

and

$$\frac{\partial \phi}{\partial t} = \frac{2e}{h} 2\pi V = \frac{2\pi}{\Phi_0} V \tag{3.6}$$

where ϕ is the phase difference of the two wave functions, defined as $\phi = \theta_1 - \theta_2$, I is the current through the junction, I_c is the maximum zero-voltage current through the junction (normally referred to as the junction critical current), h is Planck's constant, Φ_0 is the flux quantum (2.07×10^{-15} Wb), and V is the voltage drop across the junction.

3.2.1 Circuit Model and IV Characteristic Curve

Figure 3.2 shows the schematic symbol of a Josephson junction together with its circuit model. The sinusoidal component represents the current contributed by the Cooper

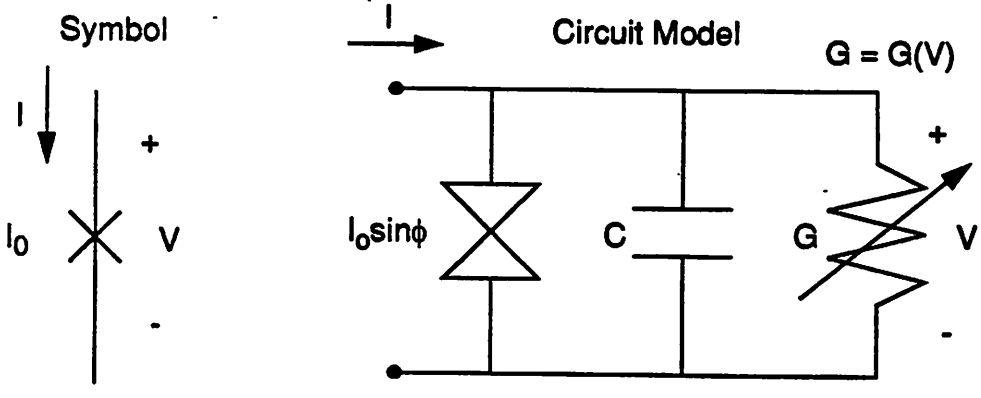


Fig. 3.2 Schematic symbol and circuit model for a Josephson junction.

pairs as described in Eq. (3.5), the capacitor represents the displacement current due to the parallel structure of the junction, and the voltage-dependent conductance represents both

the leakage current through insulator and the quasi-particle current resulting from the fact that the voltage and the absolute temperature are not zero.

It is clear from Eqs. (3.5) and (3.6) that if the voltage of a junction is not zero, the derivative term $d\phi/dt$ is not zero. As a consequence, the phase difference ϕ is changing with time, and the current I through the junction is also changing with time. This results in an oscillation of the Josephson junction in its voltage state.

The static IV curve of a Josephson junction can be obtained by applying Kirchoff's current law to the circuit model in Fig. 3.2 as follows:

$$I = I_c \sin\phi + G(V)\,V + C\frac{dV}{dt} \tag{3.7}$$

Figure 3.3 shows an IV characteristic curve of a typical Josephson junction. If the current flowing through the junction is smaller than the critical current of the junction I_o, no voltage is developed across the junction, and the junction is in its superconducting state. As soon as the current exceeds the critical current, the junction switches in a few picoseconds to the voltage state with a voltage of approximately 2.6 mV (for niobium) being developed across the junction. It is important to emphasize that the ultra-short switching time and the ultra-low high voltage level of the junction enable Josephson circuits to achieve very high performance in terms of speed and power consumption.

A junction shunted with a resistive load can be either hysteretic or nonhysteretic; the behavior in the two cases is strikingly different. A very useful and important parameter β_c, so called McCumber parameter, is widely used to define the degree of hysteresis. The parameter is defined as

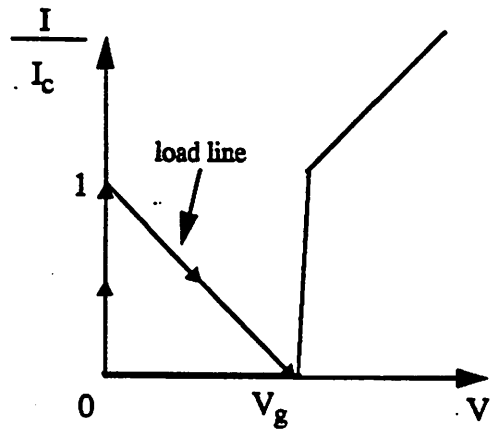


Fig. 3.3 IV characteristic curve of a typical Josephson junction.

$$\beta_c = \frac{2\pi I_c C R^2}{\Phi_0} = \omega_p^2 R^2 C^2 \tag{3.8}$$

where C is the junction capacitance, R is the equivalent impedance load, and ω_p is the plasma oscillation frequency, given by:

$$\omega_p^2 = \frac{2\pi I_c}{\Phi_0 C} \tag{3.9}$$

If β_c is less than 1, the junction is nonhysteretic, and the IV curve is single-valued; that is, for every value of current I, there exists a unique corresponding value of voltage V. If β_c is larger than 1, the junction is hysteretic, and the IV curve is more complex. As an illustration, Fig. 3.4 shows a IV curve for $\beta_c = 4$, where I_{min} denotes the maximum current required to reset the junction from the voltage state to the superconducting state. For

current I smaller than I_{min}, the IV relation is single-valued. However, for current I such that $I_{min} \leq I \leq I_0$, there are two possible operating voltages for each given current value.

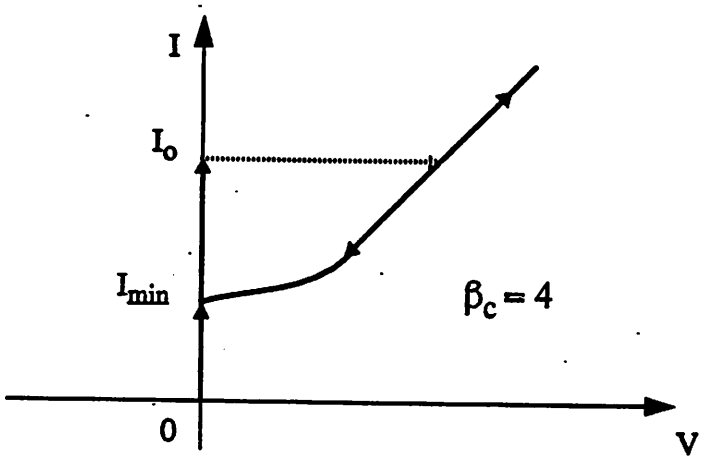


Fig. 3.4 Illustration of a hysteretic IV curve of a junction with $\beta_c = 4$ (from [11]).

3.2.2 Junction Switching Characteristic

Shown in Fig. 3.5 is a typical transient response of a Josephson junction. The top trace is the supply current and the bottom trace is the voltage developed across the junction.

As the supply current increases from zero to a level above the junction critical current, the junction switches to the voltage state. As the supply current drops back to below the resetting current, the junction returns to its superconducting state with decaying "plasma oscillation". As indicated in the figure, parameters of most interest include the turn-on time, the rise time, the fall time, and the plasma oscillation delay time.

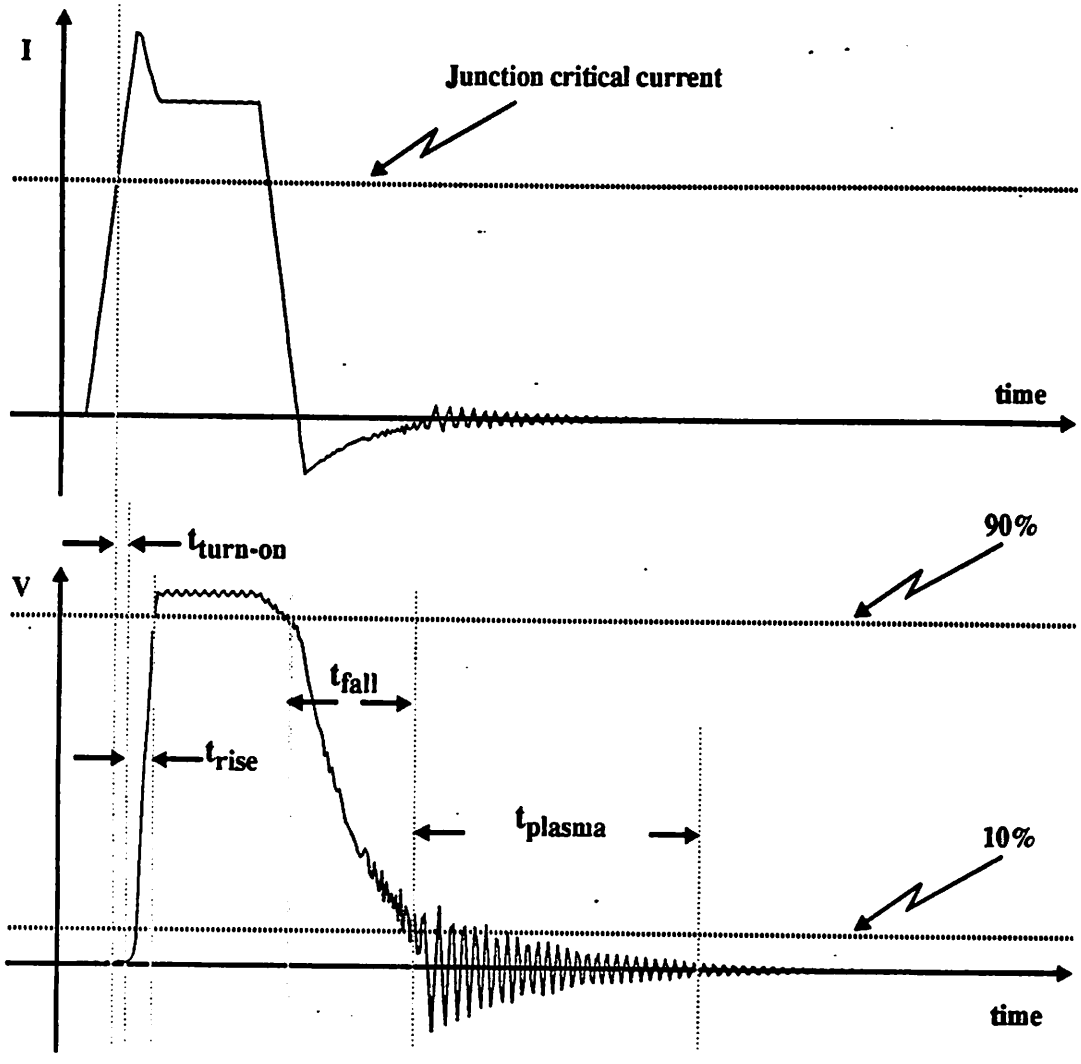


Fig. 3.5 Supply current (top) and voltage (bottom) across a Josephson junction.

3.2.2.1 Junction Turn-On Time

The turn-on switching time of a junction, by definition, is the time it takes for the voltage of the junction to begin to rise after the critical current of the junction is exceeded. This corresponds to the time it takes for the phase of the junction to change from $\pi/2$ to π.

According to Harris [12] and McDonald et al. [13], the turn-on time can be approximated as follows:

$$t_{turn-on} = \omega_p^{-1} \left\{ \frac{1 + 2\left[\frac{\pi}{2} - \arcsin\left(\frac{I_{bias}}{I_0}\right)\right]}{\frac{(I_{gate} - I_{bias})}{I_{gate}}} \right\}^{0.5} \tag{3.10}$$

where ω_p is the plasma oscillation frequency described in Eq. (3.9), I_{bias}, I_0, and I_{gate} are the critical current, the initial bias current before switching, and the final bias current right after switching, respectively. For $I_{bias} << I_{gate}$ and $I_{bias} << I_0$, the turn-on time can be further simplified as:

$$t_{turn-on} = \omega_p^{-1} \left(\frac{1 + \pi}{1}\right)^{0.5} \tag{3.11}$$

3.2.2.2 Junction Rise Time

The rise time is the time it takes for the junction voltage to increase to 90% of its final value, which has been found from simulation to be approximately 2.3 time constants RC, where C is the junction capacitance and R is the equivalent load [14].

3.2.2.3 Junction Fall Time

Analogous to the rise time, the fall time measures how long it takes for the voltage of a junction to drop from 90% to 10% of its high level. The fall time depends on the RC time constant of the junction and the current applied to reset the junction. The lower the

applied current during resetting, the shorter the fall time is. In practice, it can be approximated as somewhere between RC and 4RC [14].

3.2.2.4 Junction Plasma Oscillation Decay Time

As can be seen on Fig. 3.5, during the reset, the voltage across the junction decreases exponentially with a time constant RC, where R is the equivalent loading resistance and C is the junction capacitance. Superimposed on this exponentially decaying signal is another component due to the junction's oscillation which occurs at the plasma frequency ω_p. The time it takes for this plasma oscillation to decay to an acceptable level is referred to as the plasma oscillation decay time and is the most dominant and limiting factor of a junction's switching time. In most cases, this decay time can be estimated to be around 6 to 7 time constants RC [14].

3.2.2.5 Junction Punchthrough

In the so-called voltage-state logic applications of Josephson junctions, the junction supply current is turned off to reset the junction to the zero-voltage state. It is desired that the junction stays in the zero-voltage state even if the supply current is subsequently raised to a value close to, but less than, the junction critical current I_c. When the supply current falls below a value $|I_{min}|$ the junction will fall into the so-called plasma oscillations. If the magnitude of the supply current is raised too quickly and too close to $|I_c|$, the junction may again switch to the voltage state. This phenomenon is called punchthrough and occurs because the time allowed for resetting is not long enough. It has been found that the probability P for this type of punchthrough to occur is of the form [15] [16]:

$$P = e^{-\omega_p t_{reset}} \tag{3.12}$$

where t_{reset} is the time for resetting during which the bias is kept below I_{min}.

3.2.3 One-Junction SQUID

If an inductance is connected in parallel to a junction, one of the most useful devices for superconducting circuits, known as a one-junction SQUID (Superconducting Quantum Interference Device), is obtained. Shown in Fig. 3.6 are both the circuit implementation and the periodic dc transfer curve for a typical one-junction SQUID. Appendix A.1 shows how the transfer curve can be calculated.

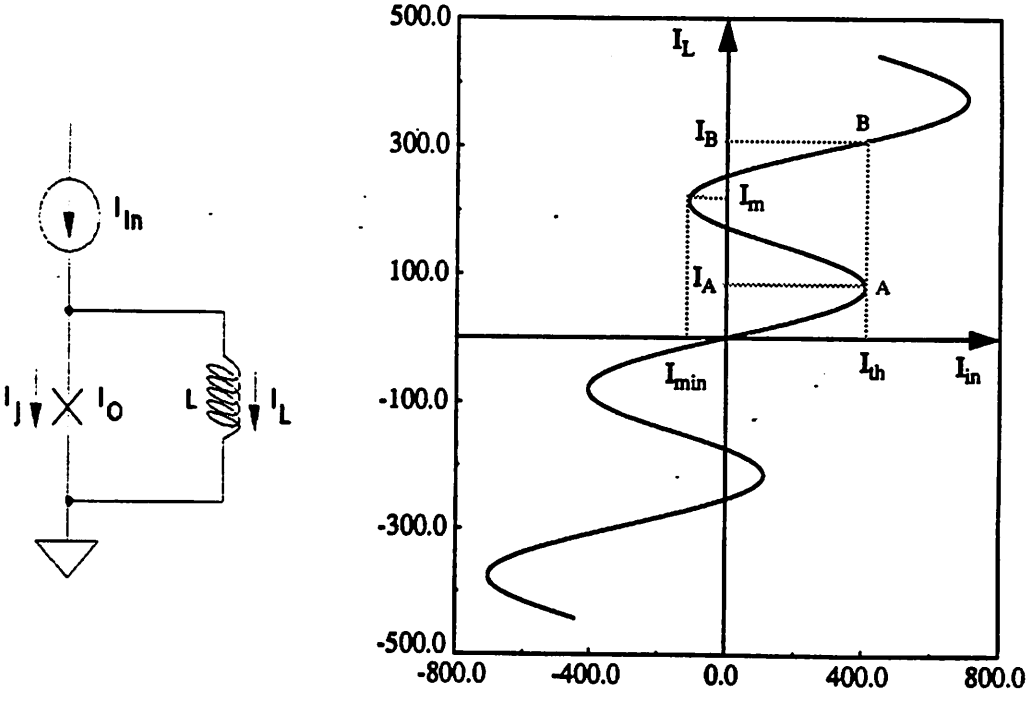


Fig. 3.6 Schematic and dc transfer curve of a one-junction SQUID.

In the figure, the horizontal axis is the input current I_{in}, and the vertical axis is the current through the inductor I_L. For an input current less than the threshold current I_{th}, the flux in the superconducting loop (formed by the junction and the inductor) is less than $\Phi_0/2$, the SQUID is considered to be the in zero-flux-quantum state, and a very small current I_A is flowing through the inductor, as indicated by point A. However, as soon as the input current exceeds the threshold current I_{th}, one flux quantum enters the loop and a much larger current I_B flows through the inductor (operating point B).

The value of the threshold input current of the SQUID I_{th} shown in the dc curve where the SQUID switches from zero-flux-quantum state to one-flux-quantum state can be obtained by differentiating Eq. (A.4) in Appendix A.1 and setting dI_{in}/dt to zero to solve for the maximum point. This would give:

$$I_{th} = I_c \left\{ \sin\left[\arccos\frac{-1}{\beta_L}\right] + \frac{\arccos(-1/\beta_L)}{\beta_L} \right\} \tag{3.13}$$

where I_c is the junction critical current and

$$\beta_L = \frac{2\pi L I_L}{\Phi_0} \tag{3.14}$$

Other useful parameters shown on the curve are the low output current I_A, the high output current I_B, the minimum input current to reset the SQUID I_{min}, and the output current I_m at the resetting point, which can be derived to be as follows, respectively [14]:

$$I_A = I_C \frac{\arccos(-1/\beta_L)}{\beta_L} \tag{3.15}$$

$$I_B = I_m + \frac{I_A}{I_{th}}(I_{th} - I_{min}) \tag{3.16}$$

$$I_{min} = I_C \frac{2\pi}{\beta_L} - I_{th} \tag{3.17}$$

$$I_m = I_C \frac{2\pi - \arccos(-1/\beta_L)}{\beta_L} \tag{3.18}$$

It will be shown later that such a device can be used to implement very sensitive comparators by applying a current signal at the input and sensing the output current through the inductor. Analysis and operation of one-junction SQUID will be discussed more extensively and in more detail then.

3.2.4 Two-Junction SQUID

Another useful, probably the most important, circuit configuration in superconducting technology is a two-junction SQUID [14] [17]. As shown in Fig. 3.7, a two-junction SQUID consists of two Josephson junctions connected to each other through two inductors L_1 and L_2, which in turn are magnetically coupled to the two inductors in the control line with mutual inductance M_1 and M_2. The SQUID is biased by the current I_g and its critical current is modulated by the control current I_{con}.

The periodic threshold characteristic curve of the SQUID is plotted in the same figure. The curves show the boundary between the region of the superconducting state (inside the lobes) and the region of the voltage state (outside the lobes). If the operating point of the SQUID lies inside a lobe when the gate bias I_g is raised, it is in superconducting state and the output voltage is zero. On the other hand, if the operating

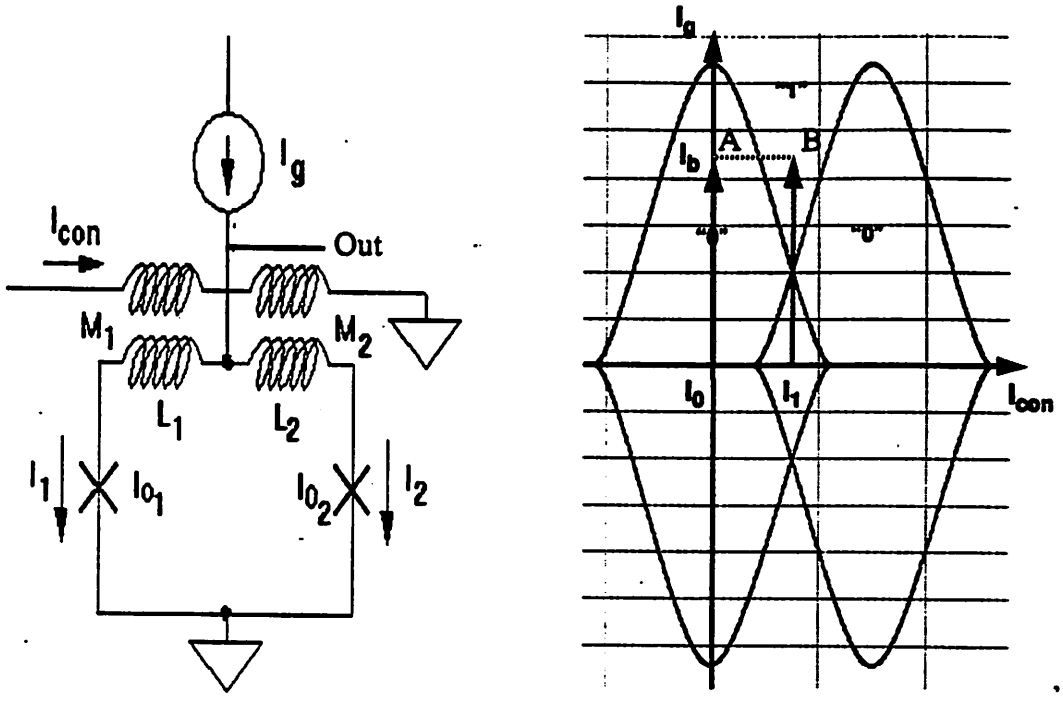


Fig. 3.7 Circuit schematic and threshold curves of a two-junction SQUID.

point falls outside a lobe, it is in the voltage state, and the output is high. As a result, for a given bias I_b, the output of the SQUID is low or high depending on whether the control current I_{con} is low or high (corresponding to whether the operating point is A or B in the figure), respectively. In the analog-to-digital converter to be discussed in subsequent chapters, this characteristic of a two-junction SQUID is going to be used to implement a device that reads out and determines whether the current through an inductive control line is high or low. Calculation of the threshold curve of a two-junction SQUID is shown in Appendix A.2 and A.3, and detailed analysis can be found in [18].

3.3 Periodic-Threshold Flash Analog-To-Digital Converters

There are two different architectures for superconducting flash-type ADCs. The first is the periodic-threshold type, which takes advantages of the periodicity of SQUID threshold characteristic curves to implement an N-bit ADC with only N comparators. The second type is fully parallel architecture, which can potentially achieve faster conversion rate than the periodic-threshold type [19] but requires 2^N-1 comparators for N-bit resolution. Fully parallel architecture is the main topic of this thesis and will be described in full detail in subsequent chapters. For completeness, various designs and implementations of periodic-threshold ADCs together with their advantages and disadvantages will be described in the rest of the chapter.

Figure 3.8 shows the architecture implementation for a four-bit periodic-threshold converter. Two- or three-junction SQUIDs are used as comparators and a resistive divider is used to divide the analog current appropriately. Only N comparators are required to implement an N-bit ADC, and the outputs of the comparators are in Gray code. Depending on applications, a Gray-to-binary encoder may or may not be needed. Note that for the Gray-coded numbers, as the output is changed from one level to the next, only one of the output bits changes. This is advantageous since an error in the threshold position can cause at most an output error of 1 LSB.

As mentioned earlier in the chapter, the threshold curves of two-junction SQUIDs are periodic. This periodicity of SQUIDs, which is determined by the junction critical current and the loop inductance, can be used to implement comparators with multiple threshold levels, as shown in Fig. 3.9. The periodic threshold curve of a SQUID is shown

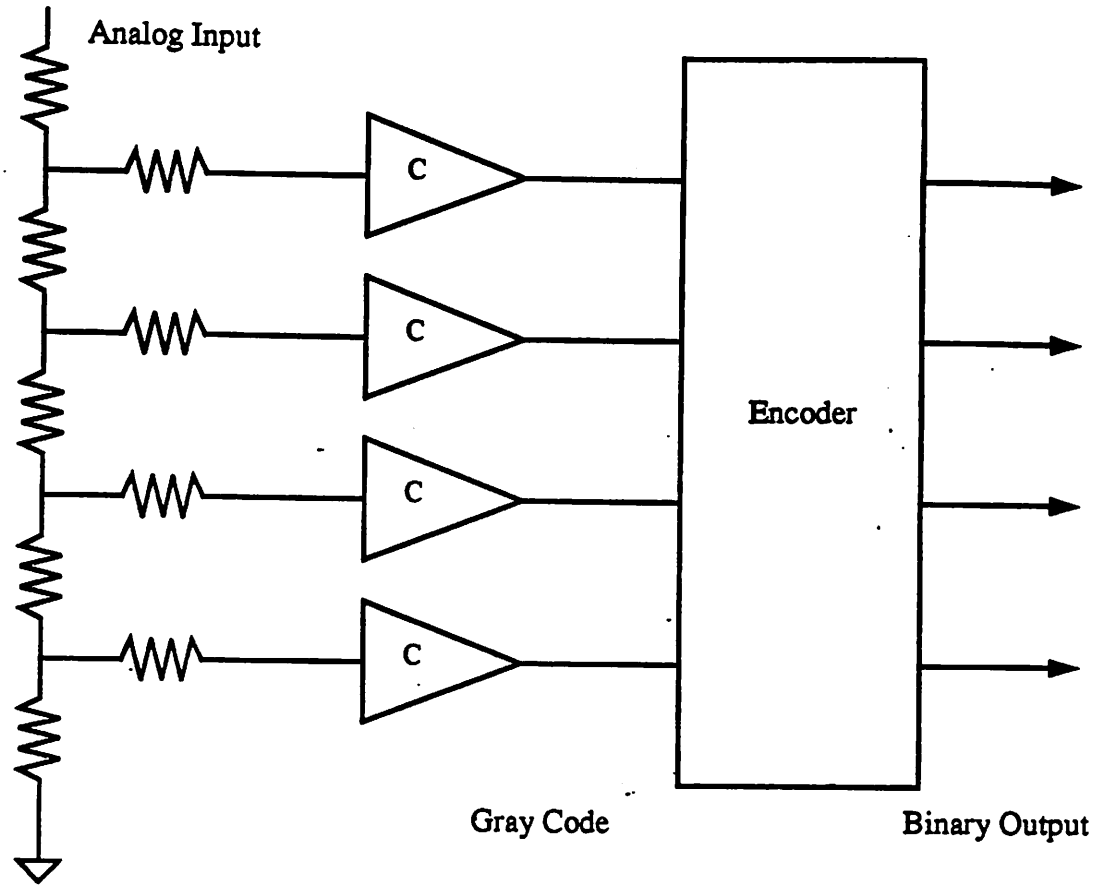


Fig. 3.8 Architecture implementation for a four-bit periodic-threshold ADC

again on the top for reference, and the second graph is the output voltage level of the SQUID as a function of the control current I_A. The input is used as the control for the SQUID and the gate current I_g is used as the bias. As described earlier, whether the SQUID is in superconducting or voltage state and whether the output is zero or one depend on whether the operating point, determined by the control current I_A and the bias current I_g, lies inside or outside a threshold lobe, respectively. As a result, if the SQUID is biased correctly, shown as I_{th} in the figure, the dependence of the output on the control input is exactly what required for a comparator with multiple threshold levels.As an

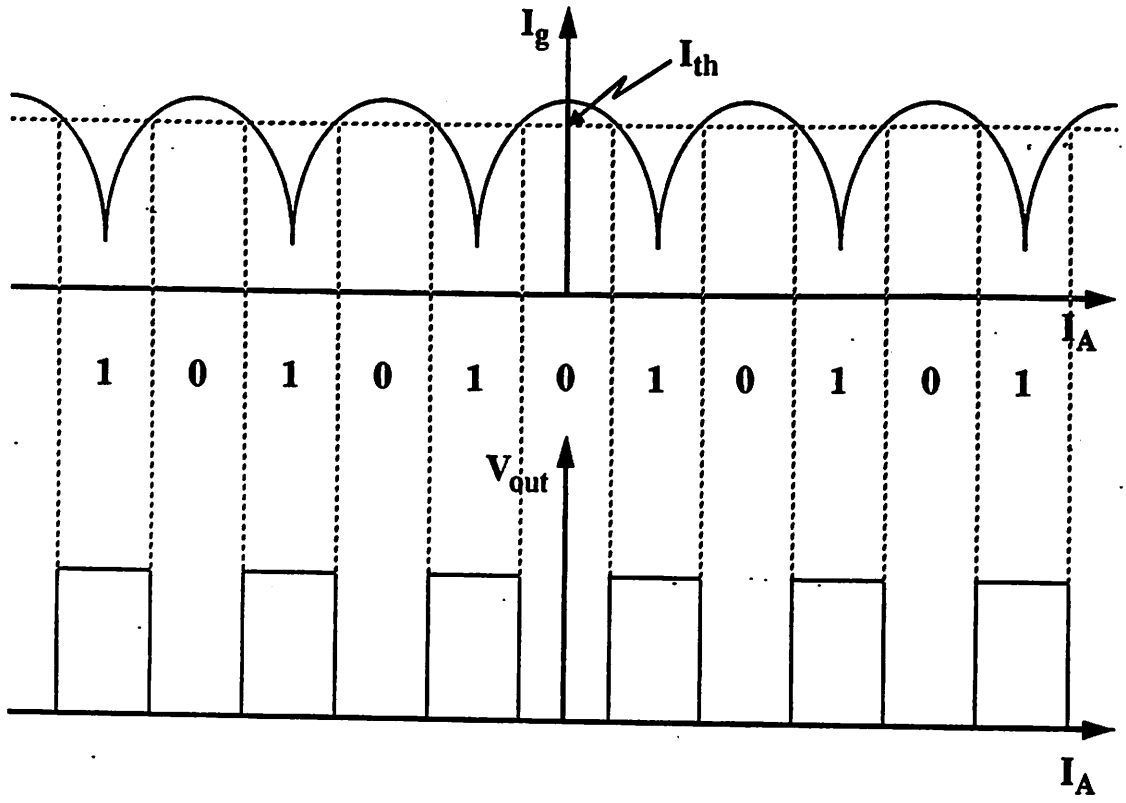


Fig. 3.9 Use of SQUID's periodic threshold curve to implement a comparator.

example, Fig. 3.10 shows the threshold curves of comparators for a 4-bit periodic-threshold ADC. The bit patterns of any bit can be generated by expanding the bit patterns of the next less significant bit by a factor of 2. This, in practice, can be done either by successively dividing the input current using a resistive divider or reducing the coupling to the SQUID comparators by a factor of 2.

3.3.1 Designs Using Two Or Three-Junction SQUIDs

Periodic threshold characteristic curves of two- or three-junction SQUIDs have been used extensively to design comparators with multiple threshold levels for bit-parallel

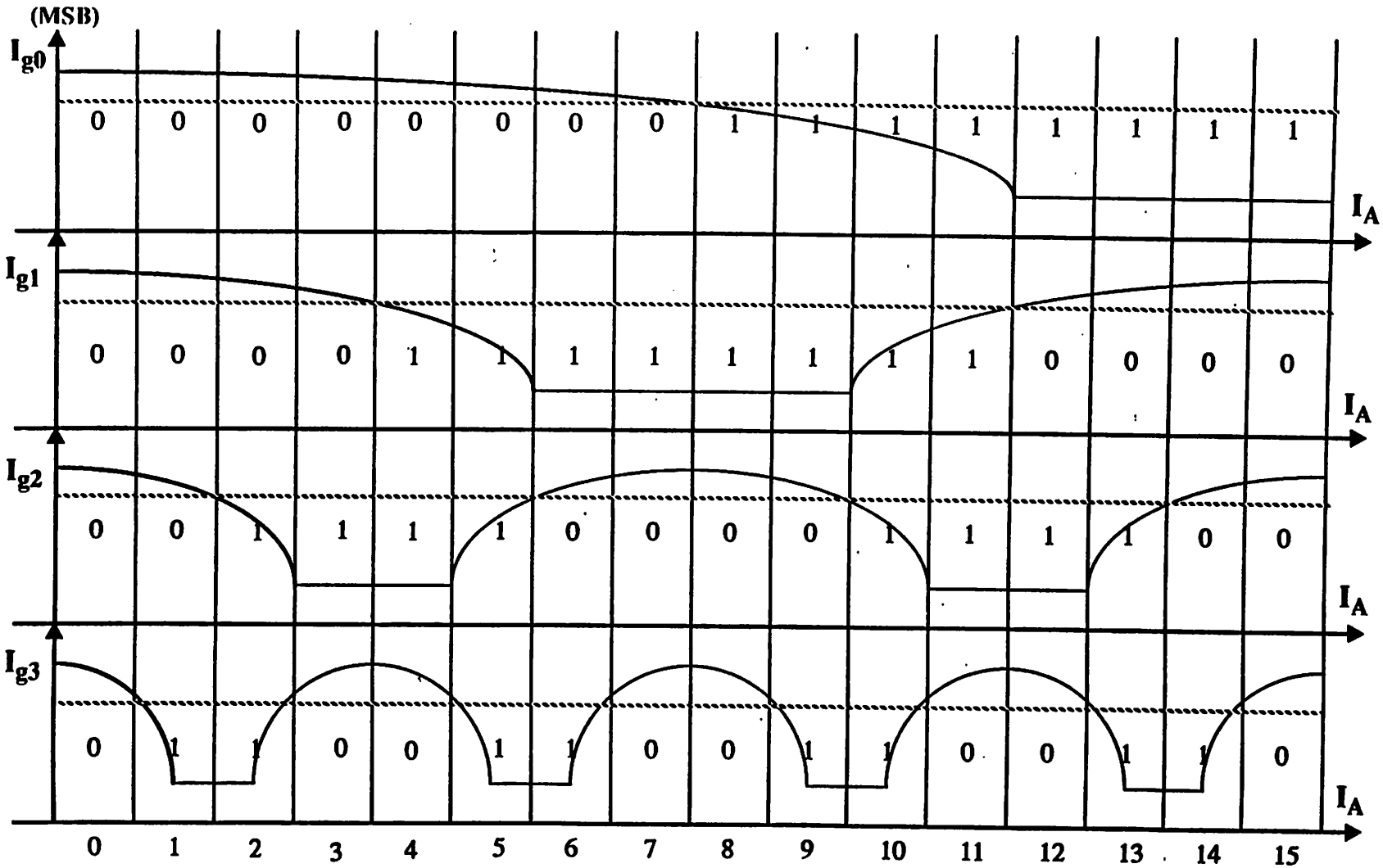


Fig. 3.10 Threshold curves of comparators for a four-bit periodic-threshold ADC.

analog-to-digital converters [20], [21], and [22]. The mutual coupling of the input signal to the N comparator SQUIDS was designed in the ratio 1,2,4,..., 2^N by varying the length of the control line. Alternatively, the desired threshold levels for the comparators as described in Fig. 3.10 can be obtained if a resistive divider network is used to divide the input current by a factor of two between successive SQUIDs

In order to achieve small aperture time and to reduce the circuit sensitivity to the process variation, in particular the variation of the junction critical current density, edge-triggered two- and three-junction SQUIDs have been used in designing comparators for periodic-threshold ADCs.

Since the operation of edge-triggering circuits relies on the rising edge of the bias current and on the relative critical currents of the SQUIDs, the absolute values of the process parameters are not critical [23]. As long as they are tracking well to each other, the circuit will function correctly. In practice, the fast rising edge for the bias current is generated by clock-shaping junctions, which will be discussed further in later chapters. Dhong et al. designed, simulated and tested at low speeds a four-bit ADC using four such edge-triggered comparators [24]. Later on, Petersen was able to demonstrate the operation of the ADC at 1 GHz clock frequency with resolution of three and four bits at 499 MHz and 280 MHz input bandwidth, respectively [25].

Another edge-triggered ADC that was very similar to Dhong's but with much simpler comparators was designed by Hamilton et al. [26]. This design, referred to as Current Latching Analog Microcomparator (CLAM), uses a series stack of two 2-junction SQUIDs to implement each of the comparators and operates in a way similar to the

self-gating AND comparator designed by Dhong. A track-and-hold circuit also was added at the front end of the ADC to increase the maximum bandwidth. The design was simulated successfully for a six-bit version at 300 MHz and for a four-bit version at 1 GHz input bandwidth. Experimentally, the circuits were demonstrated up to 100 MHz input bandwidth and 100 ps conversion time.

3.3.2 Designs Using Quasi-One-Junction SQUIDs

Simulations and experiments have shown that even though ADCs using two- or three- junction SQUIDs can be operated at very high conversion rate, they have very limited maximum input bandwidth. The main reasons include dynamic distortion of the SQUID threshold curve at high frequencies due to the hysteresis in the vortex-to-vortex transition in the SQUIDs [27]. These problems can be reduced by using nonhysteretic one-junction SQUIDs.

As can be seen from Fig. 3.11, for a one-junction SQUID, the current flowing through the junction itself I_J is a periodic function of the analog input current I_{ana}. It is single-valued as long as the parameter β_L is less than 1, where β_L is defined as

$$\beta_L = \frac{2\pi L I_0}{\Phi_0} \qquad (3.19)$$

L is the SQUID inductance and I_0 is the critical current of the junction.

As shown in Fig. 3.12, a one-junction SQUID can be combined with another junction in series with the loop to form a quasi-one-junction SQUID (QOS), which can be used to implement a comparator that potentially has higher input bandwidth than two- or

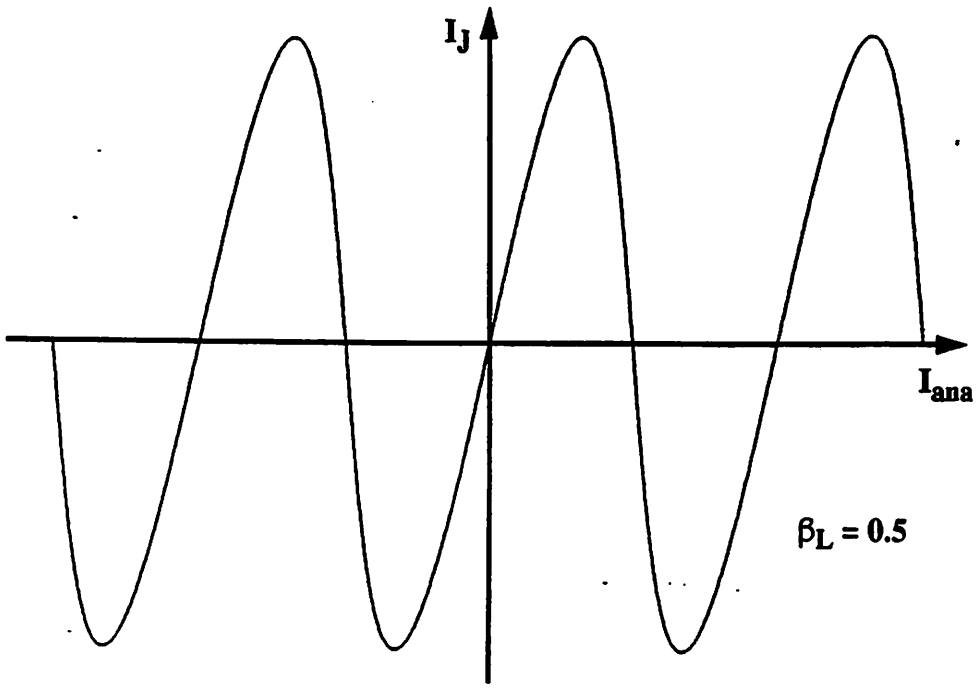


Fig. 3.11 Periodicity of the junction current of a one-junction SQUID.

three-junction SQUIDs. It has been found that the whole quasi-one-junction SQUID behaves similarly to the conventional one-junction SQUID provided that the additional junction J_S has much larger critical current than that of the original junction [28]. Figure 3.13 shows an ADC comparator based on the quasi-one-junction SQUID formed by J_0, J_S, and L_1. The junction J_S is the sampler, and J_0, with a smaller critical current, shapes the dc transfer curve. Junction J_1 and the inductor L_2 form a hysteretic one-junction SQUID (with $\beta_L > 1$), which functions as a pulse generator. R is used to convert the voltage pulses developed across the pulse generator into current pulses for the comparator, and I_{ref} is necessary to set appropriate bias for the sampler. When a pulse reaches the sampler, if the current I_J through junction J_0 is positive, the sampling junction J_S switches to the voltage

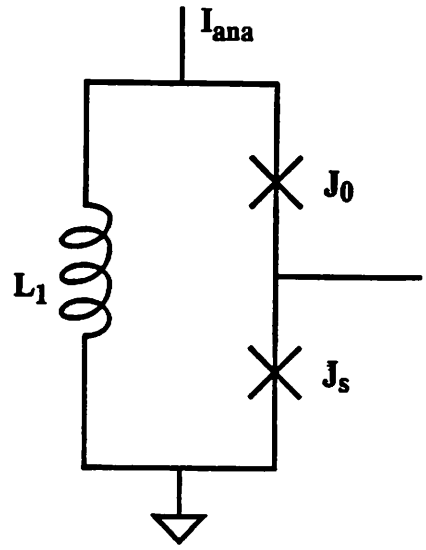


Fig. 3.12 Quasi-one-junction SQUID.

state, and a high output is detected. On the other hand, if the current I_J is negative, J_S does not switch, and the output remains low.

Ko et al. [28], first conceived and simulated a four-bit ADC using quasi-one-junction SQUIDs as comparators at sampling rate greater than 20 GHz and with an input bandwidth exceeding 10 GHz. Soon after that, Ko himself extended the design for a six-bit version and was able to simulate with 5-bit resolution at sampling rate faster than 20 GHz with an input signal of 5 GHz [29]. However, he only demonstrated the circuit operation at low speeds (few MHz). Later, Bradley et al. followed up, designed, and tested a four-bit version both at low and high speeds (up to 10 GHz bandwidth) [30] [31]. They also demonstrated the feasibility of an ADC with a dynamic range of 6 to 8 bits and an aperture time of approximately 2.5 ps. Finally, extending the design to 6-bit and 8-bit versions, they were able to perform beat-frequency tests at 1 GHz clock frequency

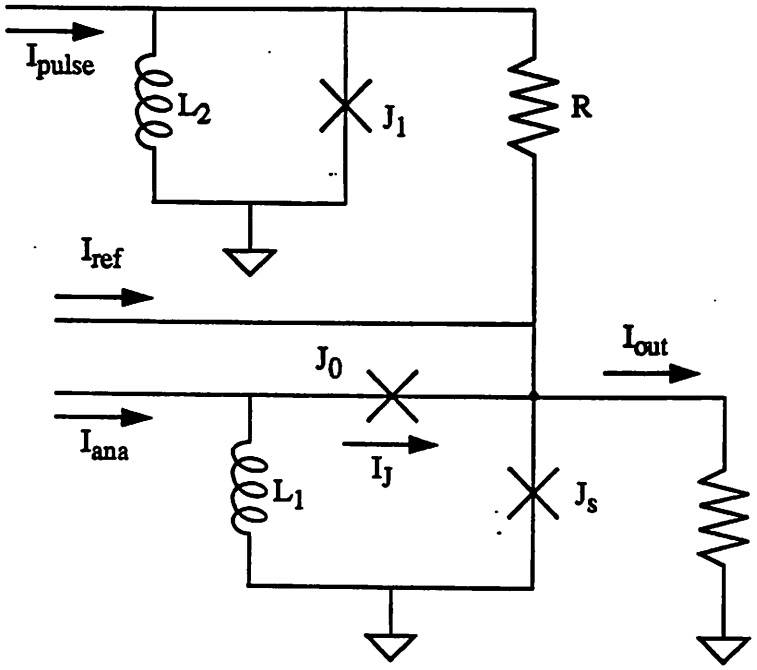


Fig. 3.13 Circuit diagram of comparator using quasi-one-junction SQUID.

and demonstrate the correct operation of the ADCs with 2, 3.7, and 4.6 effective resolution bits at 10 GHz, 7 GHz, and 2 GHz input bandwidth, respectively [32].

Chapter 4

DESIGN OF FULLY PARALLEL JOSEPHSON ADC

As discussed in the previous chapter, the periodic threshold characteristics of SQUIDs have made it possible to design successfully N-bit flash-type analog-to-digital converters with only N multiple-threshold-level comparators. The main advantage of converters of this type is that they require only N comparators to achieve an N-bit resolution. Having fewer comparators in turn makes it much easier to match all the delays in the signal and clock paths to each component. Finally, with a Gray-coded output, since only one of the output bits changes as the output changes from one level to the next, an error in threshold position can only cause at most an error of 1 LSB, and therefore, perfect alignment of the threshold levels of the comparator is not essential.

However, these ADCs have limited maximum input bandwidth, which in most of the cases is considerably smaller than the desired Nyquist rate, half of the sampling frequency. The limitation is due to the fact that SQUIDs with multiple threshold levels inherently cannot track fast signals because SQUIDs' dynamic threshold curves becomes more and more distorted as the operating frequency is increased. It has been found that threshold curves of SQUIDs are functions of the frequency of the control current and that

the shift in threshold and hysteresis of SQUIDs at high frequency is the main limiting factor for operation at very high speeds [27].

To improve the bandwidth, possibly up to the Nyquist frequencies, several converters have been implemented using conventional fully parallel architecture, in which 2^N-1 *single-threshold-level comparators* are required [33] [34]. Although this architecture would require much hardware and better process control than the other, each comparator has only one single threshold level. As a consequence, all the problems with *multiple-threshold-level comparators* that limit the speed of periodic-threshold ADCs are completely eliminated, and the conversion rate would possibly be much higher. Since our goal is to develop an ADC with *highest possible speed* but with only *low resolution*, the fully parallel architecture has become the main topic for our project and for this thesis.

4.1 Fully Parallel ADC Architecture

As reference, Fig. 2.3 in Chapter 2 is repeated in Fig. 4.1 to show the fully parallel architecture and the multiple-phase clock scheme we use for our analog-to-digital converter design. Basically, it is composed of three main blocks. The first block is the quantizer which consists of 2^N-1 comparators with linearly graded threshold levels to sample the analog signal and to assign it to one of the possible digital output levels. Since the output of the quantizer is thermometer-coded, a second block, called thermometer-to-binary encoder and realized by pipelining logic gates, is needed to convert the output into a much simpler and more useful binary representation. Finally, a reference divider network is required to set up appropriate reference levels for the comparators. This chapter will describe the design of a prototype of such an ADC using superconducting

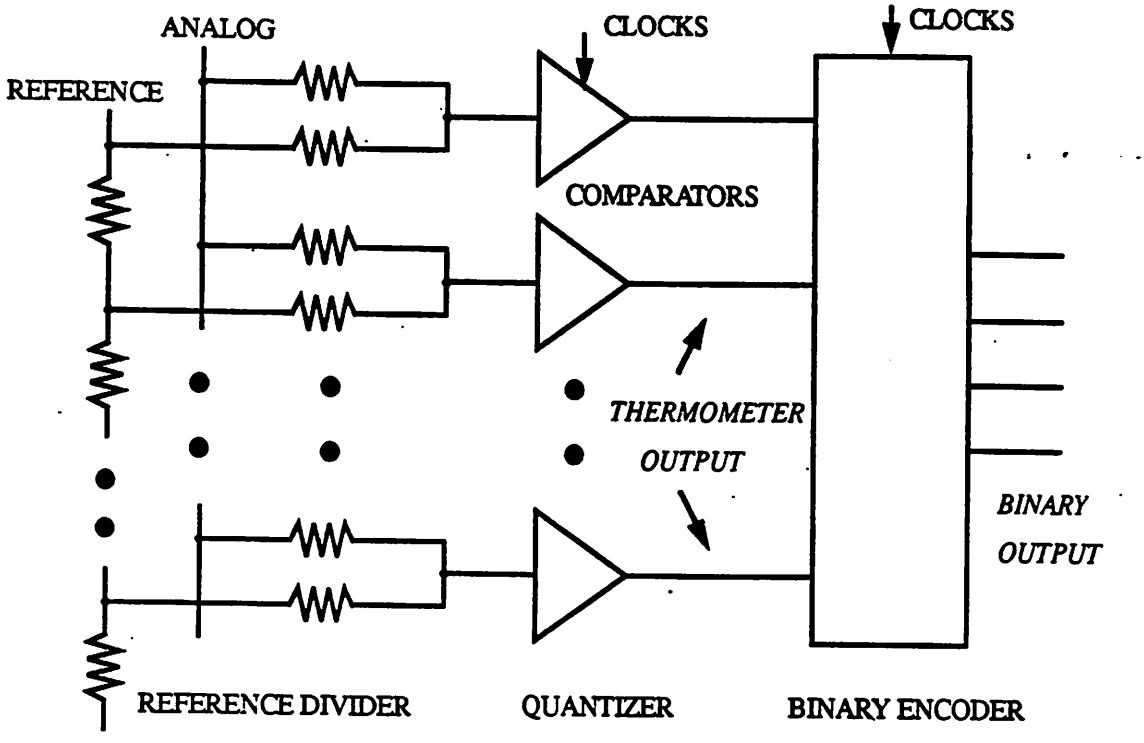


Fig. 4.1 Fully parallel (flash) analog-to-digital converter.

(niobium) technology. More specifically, the chapter will describe how the comparators are designed for the quantizer, how the logic gates are designed for the binary encoder, and finally how these individual blocks are put together to achieve complete analog-to-digital converters with very high performance.

4.2 Comparator Design

Figure 4.2 shows a simplified schematic of the comparator used in the prototype analog-to-digital converter. This comparator was originally designed by Emerson Fang [34] and has been modified extensively to optimize circuit performance and margins.

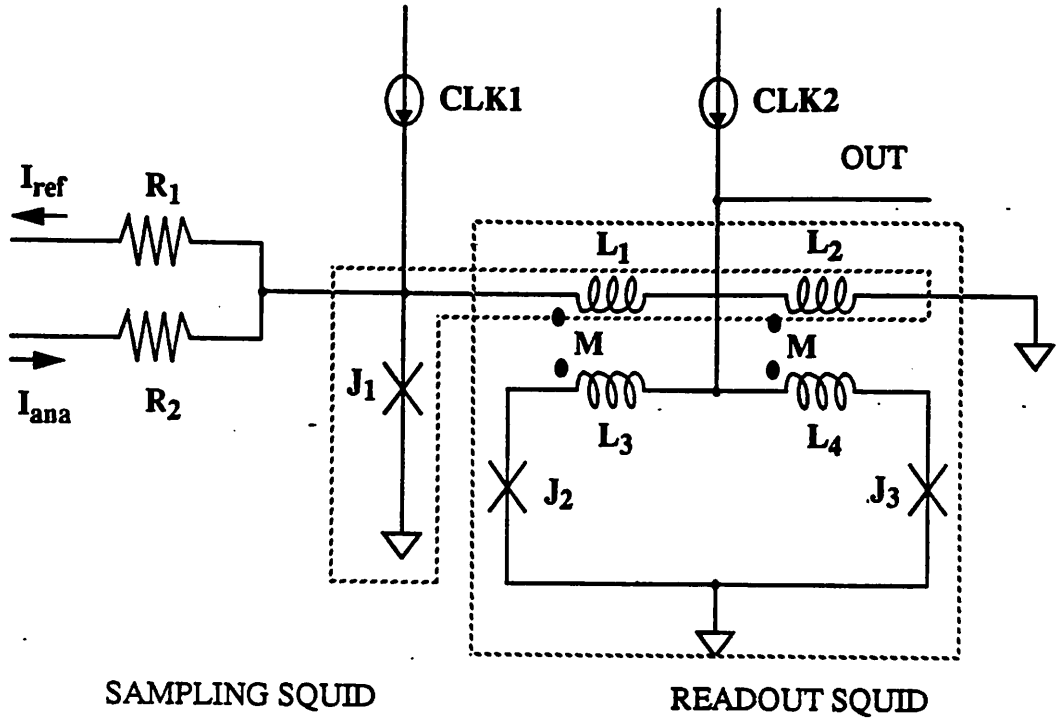


Fig. 4.2 Simplified schematic of the current-latched comparator.

Basically, it consists of a hysteretic one-junction sampling SQUID (J_1, L_1, L_2) whose output current is used as the control current for a hysteretic two-junction readout SQUID (J_2, J_3, L_3, L_4). After the one-junction SQUID samples the input signal, the two-junction SQUID reads out and determines whether the output current through the L_1 and L_2 is high or low. In addition to reading out the output current of the sampling SQUID, the two-junction SQUID also functions as an effective isolation device between the input and the output of the comparator. Any transient noise fed back from the output through SQUID inductors L_3 and L_4 would be coupled back to the control line L_1 and L_2 in opposite directions and thus would be annihilated.

Figure 4.3 illustrates graphically how the comparator works. The dc transfer curve of the one-junction SQUID and the threshold characteristic curve of the two-junction SQUID are put side by side with the vertical axes having the same scale to illustrate the fact that the output current from the one-junction SQUID I_L is used as the control current I_{con} for the two-junction SQUID. If the net input current I_{in} (which is defined as the sum

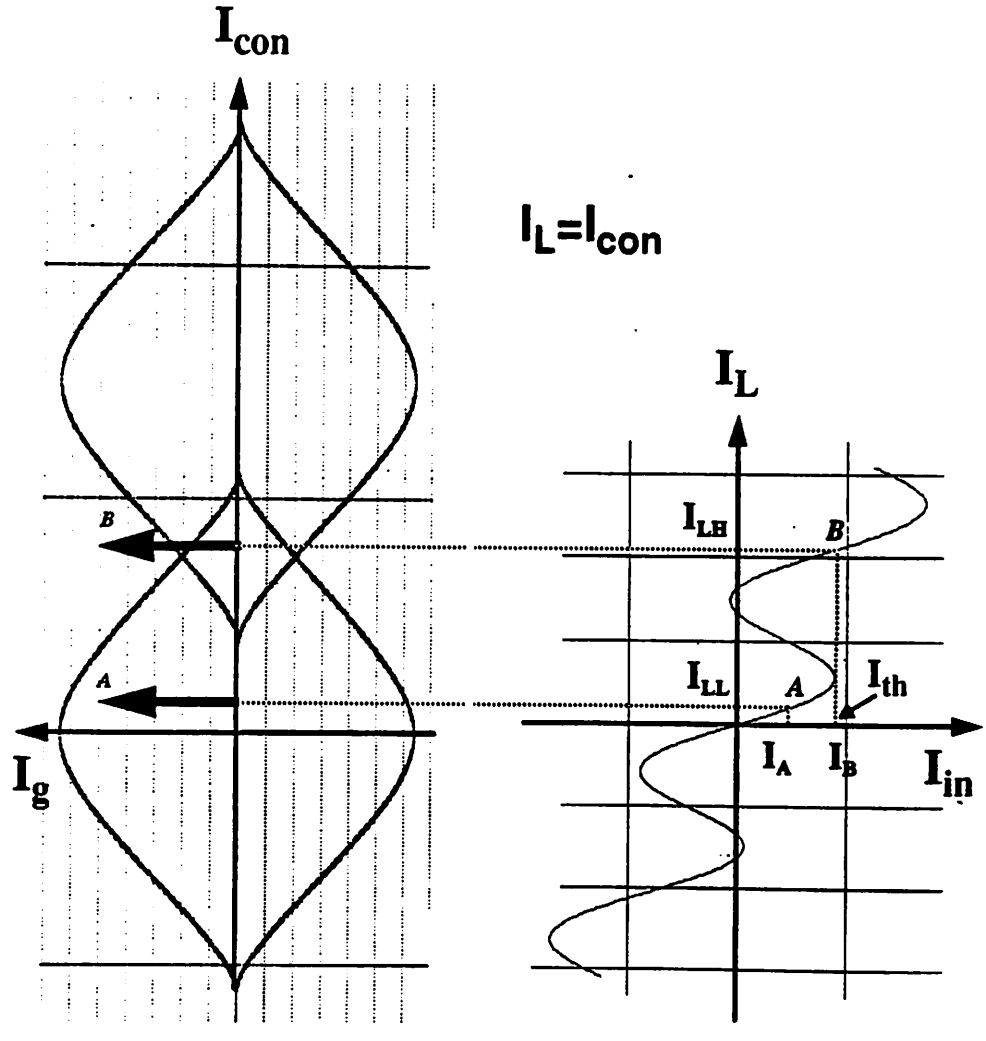


Fig. 4.3 Graphical illustration of how the current-latched comparator works.

$I_{ref} + I_{ana}$ + CLK1 in Fig. 4.2) is smaller than the threshold of the SQUID I_{th}, as indicated by point A, there is a small current $I_{LL} = I_{con}$ flowing through the control line, which keeps the operating point of the two-junction SQUID inside a threshold lobe and results in a low output voltage. On the other hand, if the net input current I_{in} exceeds the threshold current I_{th}, I_{con} becomes high enough to push the operating point of the readout SQUID outside of the threshold lobe (point B). As a result, the readout SQUID switches to the voltage state, and a high output is detected. The circuit thus indeed functions correctly as a sensitive comparator.

A complete circuit diagram for the comparator is shown in Fig. 4.4.The threshold level of the comparator is set by the combination of the bias current I_{bias}, the critical

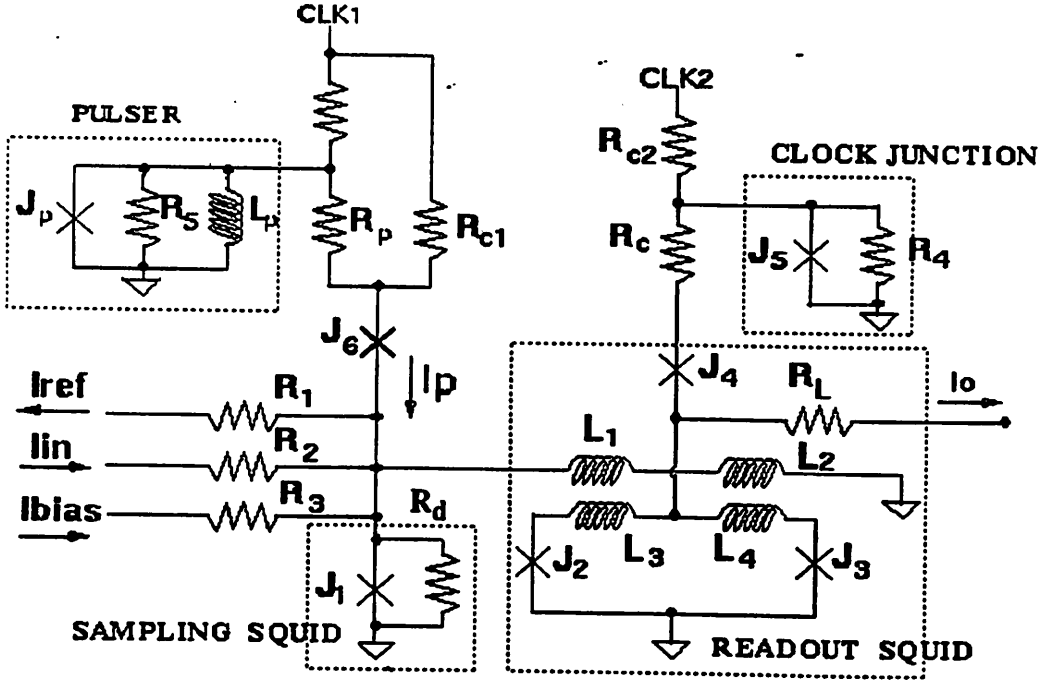


Fig. 4.4 Complete schematic diagram of the current-latch comparator.

current of junction J_1, the inductance $L_1 + L_2$, and the first -phase clock CLK1. Depending on whether the net input current is less or greater than this threshold level, either a small or large current flows through the inductors L_1 and L_2. In addition to the sampling SQUID and the readout SQUID, several other subcircuits have been added to improve the circuit performance and circuit margins.

A pulser, realized with another one-junction SQUID (J_p, L_p, R_5), is connected to the input of the comparator to minimize the aperture time and thus maximize the input bandwidth.The pulser generates and superimposes a very sharp and narrow pulse on the input of the comparator, which ensures a more accurate sampling time and a smaller aperture time. Figure 4.5 shows the circuit implementation and simulation result for a pulser, where given a slow rising sinusoidal input signal, the output is a very narrow pulse.

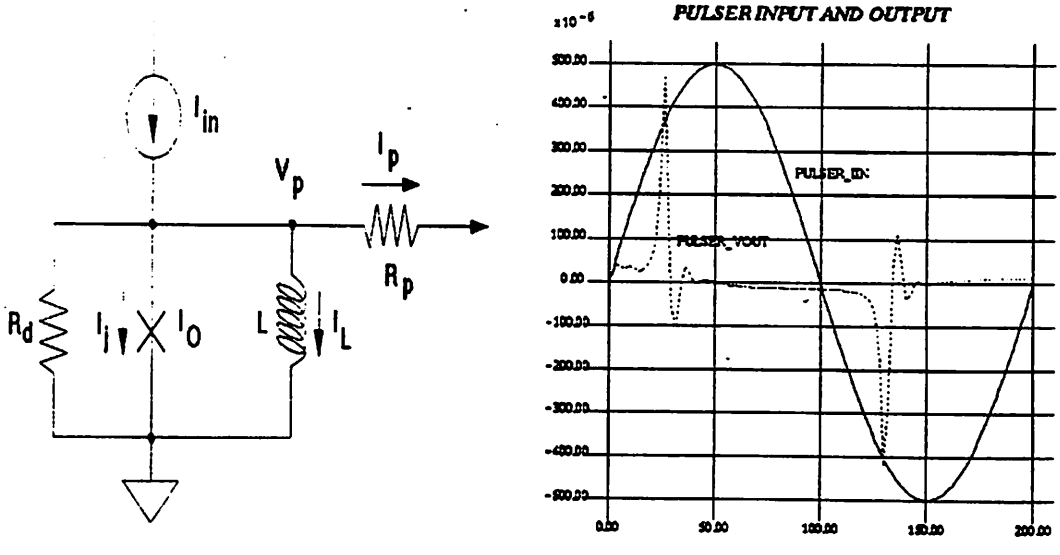


Fig. 4.5 One-junction SQUID as a pulser for a minimum aperture time.

Simulations have shown that with a critical current density of 1 kA/cm^2, a pulse as narrow as 4 ps can be achieved, which translates into, according to Eq. 3.2 in Chapter 3, a maximum input bandwidth of 5 GHz for a four-bit ADC.

It is of great interest to be able to estimate the width and the magnitude of the output pulse of a pulser. Assuming that the base width t_{base} of the pulse equals the rise time t_{rise} of the one-junction SQUID from 10% to 90% and that the pulse width t_{pw} is defined to be half of the base width t_{base}, we get:

$$t_{pw} = 0.5t_{base} = 0.5t_{rise} \tag{3.20}$$

The rise time t_{rise} can be found by modeling the one-junction SQUID as an equivalent RLC network and using the formula given by Kuo [35]

$$t_{rise} = \frac{1 - 0.4167\zeta + 2.917\zeta^2}{\omega_n} \qquad 0 < \zeta < 1 \tag{3.21}$$

where ω_n is the oscillation frequency and ζ is the damping constant defined as

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{3.22}$$

$$\zeta = \frac{1}{2R}\sqrt{\frac{L}{C}} \tag{3.23}$$

Consequently, for ζ close to 1, as the damping resistor R increases, ζ decreases, and the pulse width is decreased. Similarly, if the SQUID inductance L increases, the pulse width increases because ω_n decreases and ζ increases. If the junction capacitance increases, both ω_n and ζ decreases, and the pulse width may either decrease or increase

depending on how much ω_n and ζ change. In most practical designs, however, the damping resistor is chosen for critical damping, ie. $\zeta = 1$, and as a result, the pulse width increases with the capacitance. In practice, due to the limit of the minimum inductor that can be fabricated, narrower pulses and smaller aperture times can be achieved only with higher critical current density and smaller junction capacitance.

The amplitude V_{peak} of the output pulse can be calculated by observing that the total phase change across the junction $\Delta\phi$ when the SQUID loop switches from zero-flux-quantum to one-flux-quantum stage is:

$$\Delta\phi = \frac{2\pi\Delta I_L}{\Phi_0} = \frac{2\pi}{\Phi_0}\int V_L dt \tag{3.24}$$

where ΔI_L is the change in the inductance current and V_L is the voltage across the inductor. It follows that the peak voltage V_{peak} can be approximated as:

$$V_{peak} = \frac{\Phi_0}{2\pi}\frac{\Delta\phi}{t_{pw}} = \frac{L\Delta I_L}{t_{pw}} \tag{3.25}$$

with t_{pw} being the pulse width given in Eq. (3.20) above.

It is necessary to keep the total equivalent impedance at the input of the comparator as large as possible to minimize the thermal noise and to maximize the comparator's dynamic range. For a given process where the inductor of the one-junction SQUID and the junction capacitance cannot be changed, the damping resistor R_d is fixed, and all we can do to maximize the equivalent impedance is to maximize the resistor R_p that connects the pulser to the input. However, the resistor cannot be too large, or there

would not be enough current to clock and to switch the one-junction SQUID. One solution is to superimpose on the pulser output another source of current. The resistor R_{c1} is connected directly to the sinusoidal clock CLK1 to provide such a modulating signal to the comparator input. This contributes more current to the input and therefore reduces the amplitude required for the current from the pulser. The less current required from the pulser, the larger the resistor R_p can be, and the larger the dynamic range can be achieved.

The simple comparator design shown in Fig. 4.2 suffers from small margins, especially in critical current of the junctions. The main reason is that the threshold level and the operation of the comparator are directly dependent on the critical currents of all the junctions J_1, J_2, and J_3, and the amplitudes of CLK1 and CLK2.

Edge-triggering junctions J_4 and J_6 are included to minimize the circuit sensitivity to changes in critical current density. The critical currents of junctions J_2, J_3, and J_4 are designed in such a way that the two-junction SQUID switches and thus a high output current I_o is achieved *if and only if* there exists a large current in the control line L_1 and L_2 *on the rising edge* of the second-phase clock CLK2. If the control current is small, junction J_4 would switch, thus diverting the bias current from the two-junction SQUID and preventing it from switching. Since the operation only depends on the relative critical currents of the junctions (as opposed to their absolute values), the circuit is more robust in terms of the process variation. Similarly, junction J_6 provides an edge-triggering function to reduce the circuit sensitivity to the variation in the one-junction SQUID's parameters.

To make the circuit less sensitive to variation in clock amplitudes, the clock-shaping junction J_5 is used in Fig. 4.4. As shown in Fig. 4.6, the output generated by

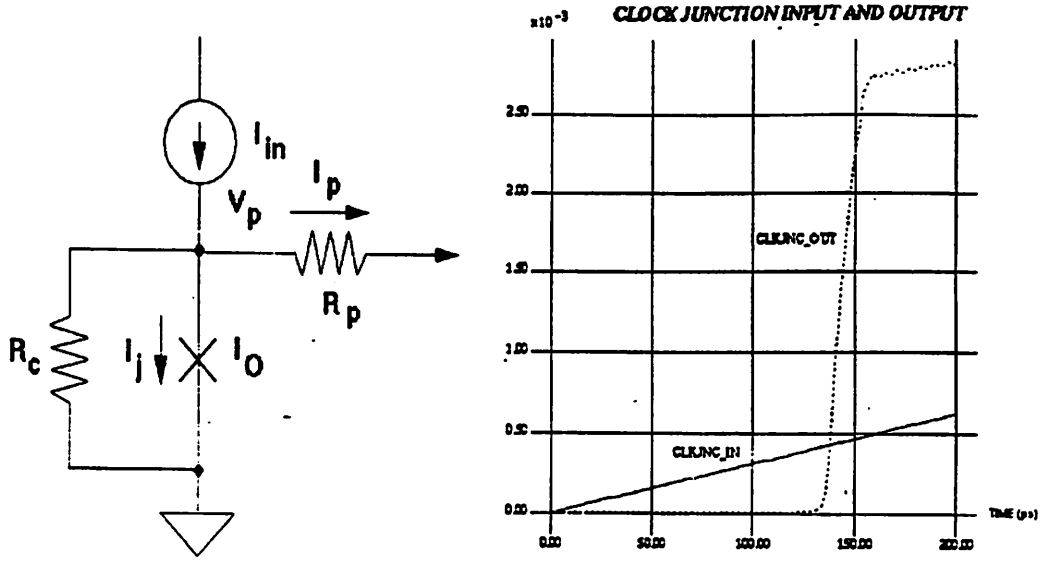


Fig. 4.6 Clock-shaping junction to obtain a clock with very sharp rising edge.

the clock-shaping junction J_5 has a constant amplitude due to the junction gap voltage and a very sharp rising edge due to the fast switching of the junction. Consequently, the actual clock fed into the circuit is relatively constant and independent of the variation of the external clock.

Table 4.1 lists the design parameters for the current-latched comparator. For comparison, the original and modified parameters are listed in the second and third columns, respectively. With the modifications and the new set of design parameters, the circuit margins in critical current density have been increased from $\pm 5\%$ to $\pm 37\%$.

Table 4.1 Original and modified design parameters for the comparator

Parameter	Original	Modified
$I_c(J_1)$	337 μA	367 μA
$I_c(J_2)$	150 μA	163 μA
$I_c(J_3)$	150 μA	163 μA
$I_c(J_4)$	225 μA	245 μA
$I_c(J_5)$	N/A	870 μA
$I_c(J_6)$	N/A	414 μA
$I_c(J_p)$	337 μA	367 μA
R_L	10 Ω	12.5 Ω
R_c	6 Ω	6 Ω
R_p	5 Ω	5 Ω
L_1	3 pH	3 pH
L_2	3 pH	3 pH
L_3	1.5 pH	1.5 pH
L_4	1.5 pH	1.5 pH
L_p	6 pH	6 pH

4.3 Logic Gates

Logic gates needed to realize the binary encoder can be conveniently realized from the comparator configuration described above. As can be seen from Fig. 4.7, a two-input AND gate can be designed by simply replacing the reference current I_{ref} with a second input and setting the bias current I_{bias} so that the gate's threshold level is larger than either input but smaller than their sum. Similarly, a two-input OR gate is achieved if the bias is adjusted so that the threshold level is smaller than either input. Once AND and OR gates are implemented, inverting gates, such as inverter, NAND, and NOR, can be readily

AND:

$I_{th} > I_A$

$I_{th} > I_B$

$I_{th} < I_A + I_B$

OR:

$I_{th} < I_A$

$I_{th} < I_B$

INVERTING GATES:

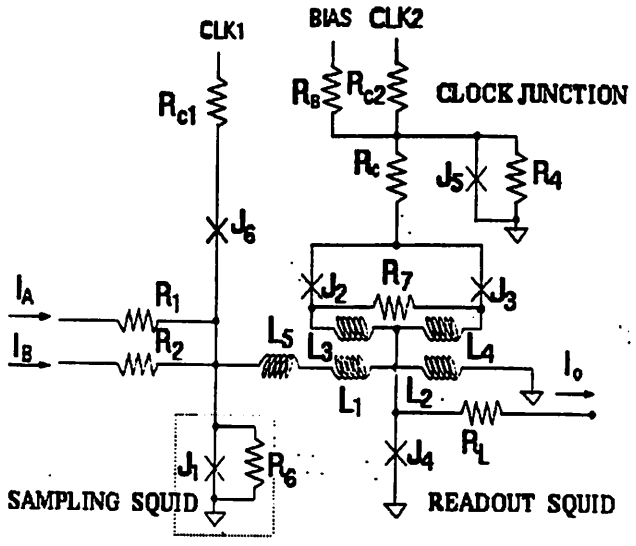


Fig. 4.7 Implementation of logic gates from the comparator building block.

obtained by switching the positions of the single junction J_4 and the two-junction SQUID. Now, for a low input, the single junction J_4 switches and gives a high output for a low input; and for a high input, the two-junction SQUID switches, prevents junction J_4 from switching, and thus yields a low output voltage.

Although another reliable logic family, Modified Variable Threshold Logic (MVTL), has been reported [36], we chose our own logic design not only because we can save a lot of time on design and simulations by using the same design for the comparators but also because our gates have potential to operate at higher speeds. Chapter 6 will describe in detail how we have modified these logic gates to optimize the speed and to make them function correctly at clock frequencies as high as 12.5 GHz.

4.4 Thermometer-To-Binary Encoder

The function of a thermometer-to-binary encoder, also referred to as an 2^N:N priority encoder, is to determine the position of the highest comparator that produces a high output and then to assign the associated output code. For semiconductor flash-type analog-to-digital converters, a typical encoder is realized by using a ROM (read-only memory) or PLA (programmable logic array) configuration. Figure 4.8 exemplifies a simple implementation of a three-bit encoder. Three-input NAND gates are used to

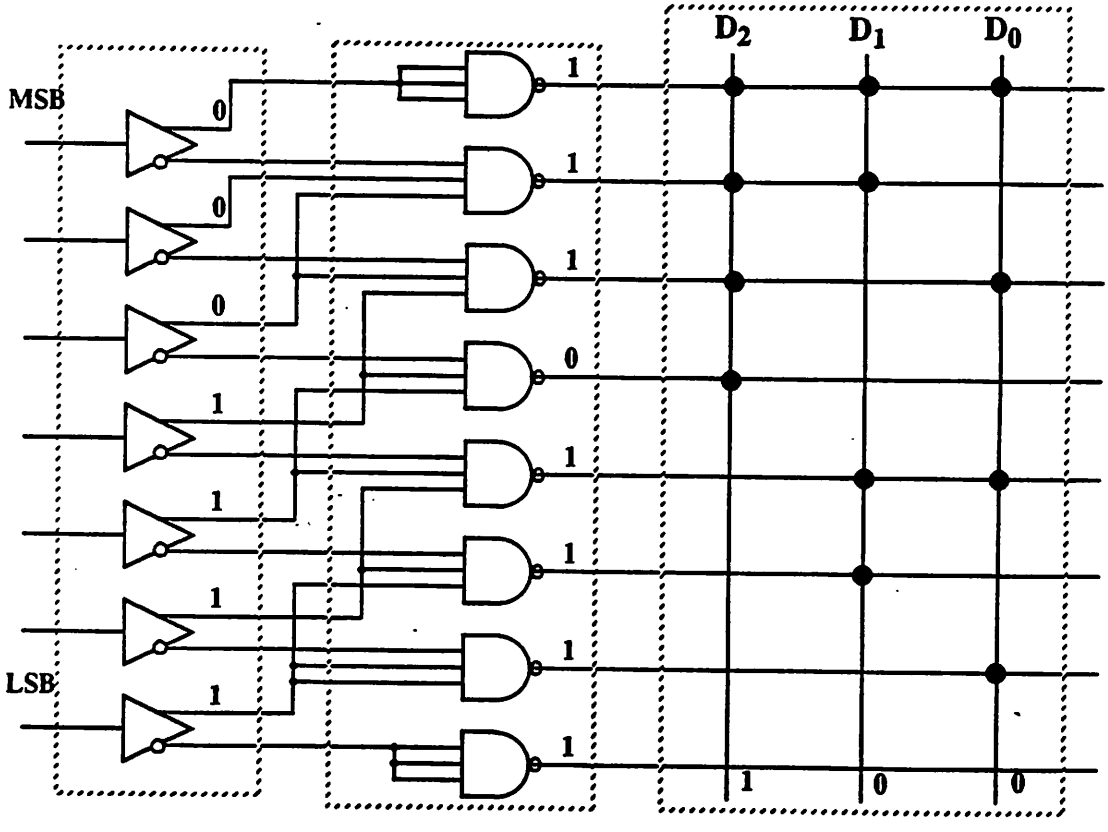


Fig. 4.8 Typical implementation of MOS thermometer-to-binary encoder.

determine the boundary between the 1's and 0's of the thermometer code, and an array of multiple-input OR gates is used to associate each output of the NAND gates to an appropriate output code. In the example, the input is chosen to be somewhere between the fourth and fifth quantization level, which results in the fifth NAND gate being the only one with a low output and a code of 100 being detected at the output of the OR array.

Although ROMs have been implemented in superconducting technology [37] [38] [39], we decided to use standard logic gates to implement a thermometer-to-binary encoder. Figure 4.9 shows the Boolean logic functions for the output bits of a four-bit encoder and how seven-input and fifteen-input XOR gates can be realized with three- and four-input XOR gates to simplify the design. In the figure, Q_n's are the inputs to the encoder, D_n's are the outputs, $\oplus$ denotes an XOR logic function and + denotes an OR.

$$D_3 = Q_7 \text{ (MSB)}$$

$$D_2 = Q_{11} \oplus Q_7 \oplus Q_3$$

$$\begin{aligned} D_1 &= Q_{13} \oplus Q_{11} \oplus \ldots \oplus Q_3 \oplus Q_1 \\ &= (Q_{13} \oplus Q_{11} \oplus Q_9) \oplus (Q_7 \oplus Q_5 \oplus Q_3 \oplus Q_1) \end{aligned}$$

$$\begin{aligned} D_0 &= Q_{14} \oplus Q_{13} \oplus \ldots \oplus Q_2 \oplus Q_1 \\ &= (Q_{14} \oplus \ldots \oplus Q_{12}) \oplus (Q_{11} \oplus \ldots \oplus Q_8) \oplus (Q_7 \oplus \ldots \oplus Q_4) \oplus (Q_3 \oplus \ldots \oplus Q_0) \\ &= (Q_{14} \oplus \ldots \oplus Q_{12}) + (Q_{11} \oplus \ldots \oplus Q_8) + (Q_7 \oplus \ldots \oplus Q_4) + (Q_3 \oplus \ldots \oplus Q_0) \end{aligned}$$

Fig. 4.9 Boolean logic functions for the output bits of a four-bit binary encoder.

The most straightforward implementation is to use basic gates (NAND or NOR) to realize two- or three-input XOR gates, and then to use these gates to build up XOR gates with higher number of inputs. However, this approach is highly undesirable due to the huge gate count and area required. For example, it would require a total of twelve two-input NAND gates to implement a three-input XOR gate!

For this particular case, we have taken advantage of the fact that the inputs to the binary encoder (which are the outputs of the quantizer) are in thermometer code to conceive quasi-three-input and quasi-four-input XOR gates. As can be seen from Figs. 4.10a and 4.10b, these quasi-XOR gates have the same logic function as their counterpart conventional gates but can be implemented with only three two-input NAND gates. Using

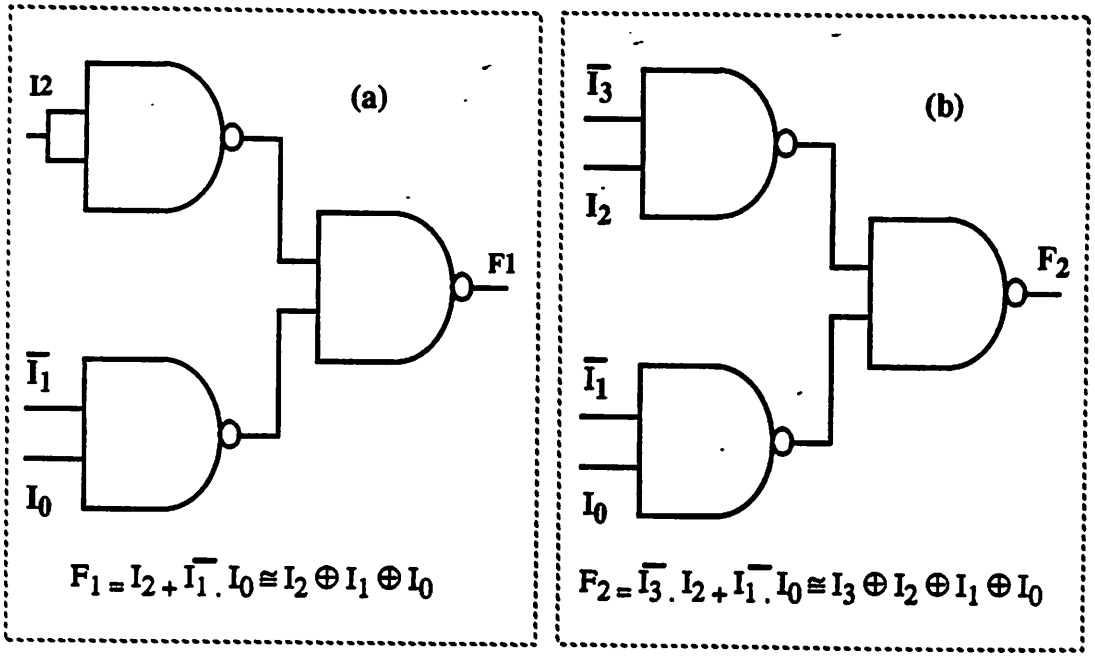


Fig. 4.10 Implementation of (a) quasi-three-input XOR and (b) quasi-four-input XOR.

these quasi-XOR gates simplifies the design complexity and significantly reduces the junction count and chip area. It is important to emphasize that these gates are "quasi" because *they function correctly as XOR gates if and only if the inputs are thermometer-coded.*

As a reference, Table 4.2, the truth table for the LSB bit, shows how the whole function F_1 (a fifteen-input XOR) can be broken down to many simpler functions, P_1, P_2, P_3, and P_4, each of which can be simply implemented with one of quasi-XOR gates. Included in the table are the definitions for the logic functions F's and P's.

The design of the quasi-three-input and quasi-four-input XOR gates using a minimum number of NAND or NOR gates described above can be easily generalized for an XOR gate with *any* number of inputs. More specifically, as long as the inputs are in thermometer code, an n-input XOR gate can be shown to be equivalent to the following, where Q_0 is the least significant and Q_n is the most significant signal level.

$$F = \overline{Q_{n-1}} * Q_{n-2} + \overline{Q_{n-3}} * Q_{n-4} + \bullet\bullet\bullet + \overline{Q_1} * Q_0, \text{ for n even}$$

$$F = Q_{n-1} + \overline{Q_{n-2}} * Q_{n-3} + \overline{Q_{n-4}} * Q_{n-5} + \bullet\bullet\bullet + \overline{Q_1} * Q_0, \text{ for n odd}$$

4.5 Complete Analog-To-Digital Converters

A complete three-bit converter and its extension to a four-bit version have been designed and fabricated both at U. C. Berkeley and Hypres, Inc. Their block diagrams are shown in Figs. 4.11 and 4.12, respectively.

Table 4.2 Truth table for the LSB bit of a 4-bit thermometer-to-binary encoder

Q_{15}	Q_{14}	Q_{13}	Q_{12}	Q_{11}	Q_{10}	Q_9	Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	F_1	P_4	P_3	P_2	P_1	F_2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	0	1
0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	1	0	1
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1

$$F_1 = Q_{15} \oplus Q_{14} \oplus Q_{13} \oplus \cdots \oplus Q_2 \oplus Q_1$$

$$F_2 = P_4 + P_3 + P_2 + P_1$$

$$P_4 = Q_{15} + \overline{Q_{14}} * Q_{13}$$

$$P_3 = \overline{Q_{12}} * Q_{11} + \overline{Q_{10}} * Q_9$$

$$P_2 = \overline{Q_8} * Q_7 + \overline{Q_6} * Q_5$$

$$P_1 = \overline{Q_4} * Q_3 + \overline{Q_2} * Q_1$$

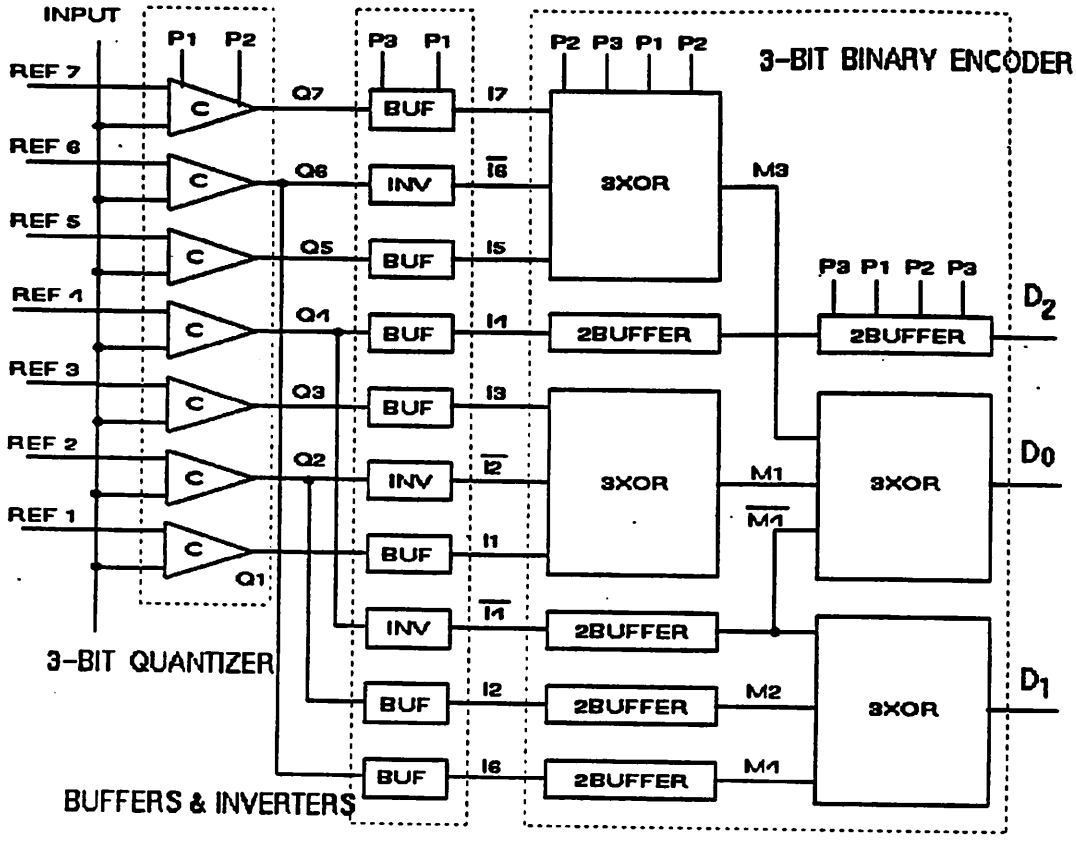


Fig. 4.11 Block diagram of a complete three-bit analog-to-digital converter.

Starting from the left are the quantizer, the buffer-and-inverter, and the thermometer-to-binary encoder. A buffer-and-inverter stage is necessary to provide complementary signals and to keep all signals in an appropriate pipeline stream. Building blocks include comparators, basic logic gates, single-stage buffer, two-stage buffers, quasi-three-input and quasi-four-input XOR gates.

Figures 4.13 and 4.14 show respectively the layouts of the two complete converters for testing at high speeds, mapping exactly one-to-one all the blocks shown in Figs. 4.11 and 4.12. Although an automatic layout tool is not available for the technology,

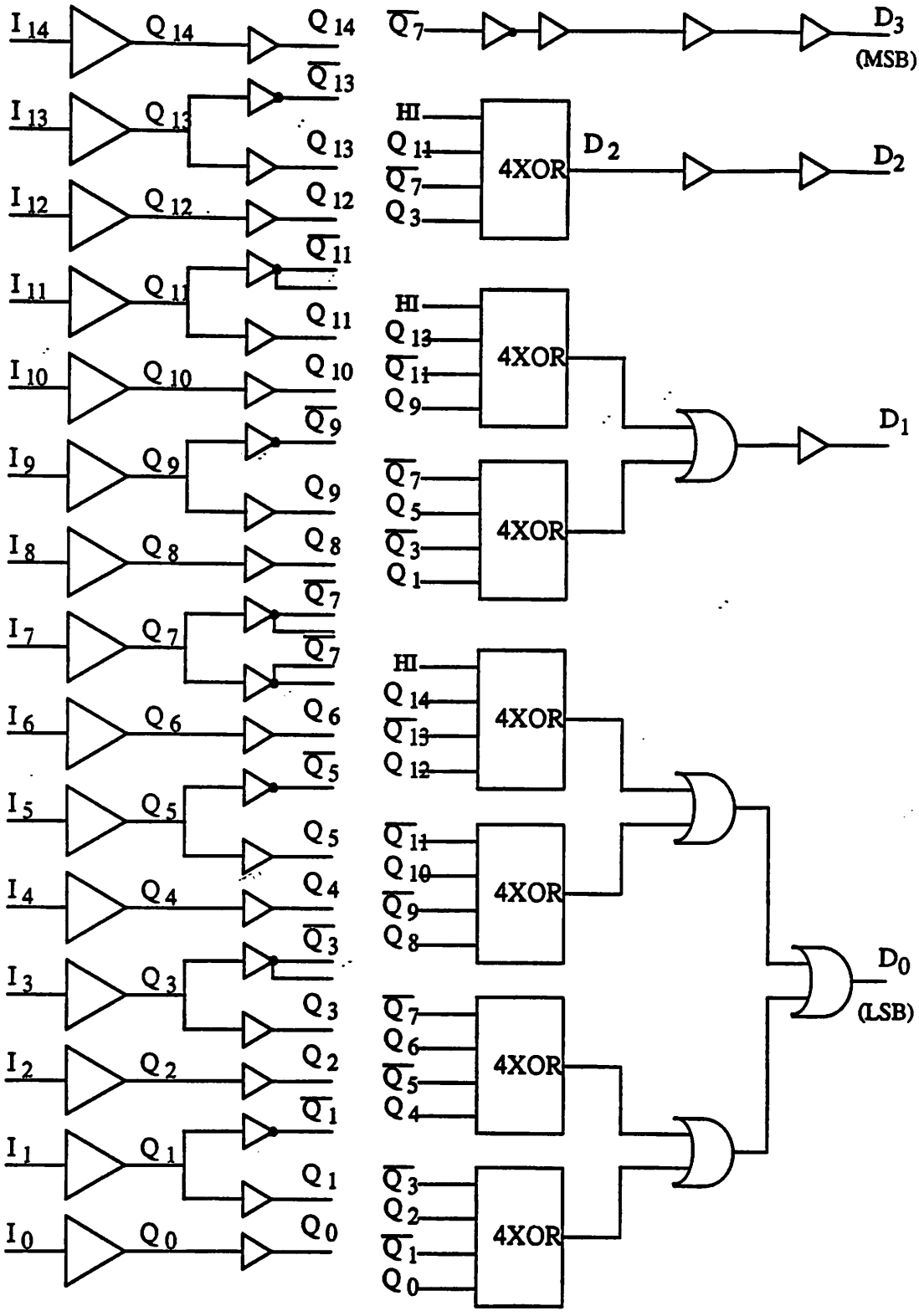


Fig. 4.12 Block diagram of a complete 4-bit fully parallel analog-to-digital converter.

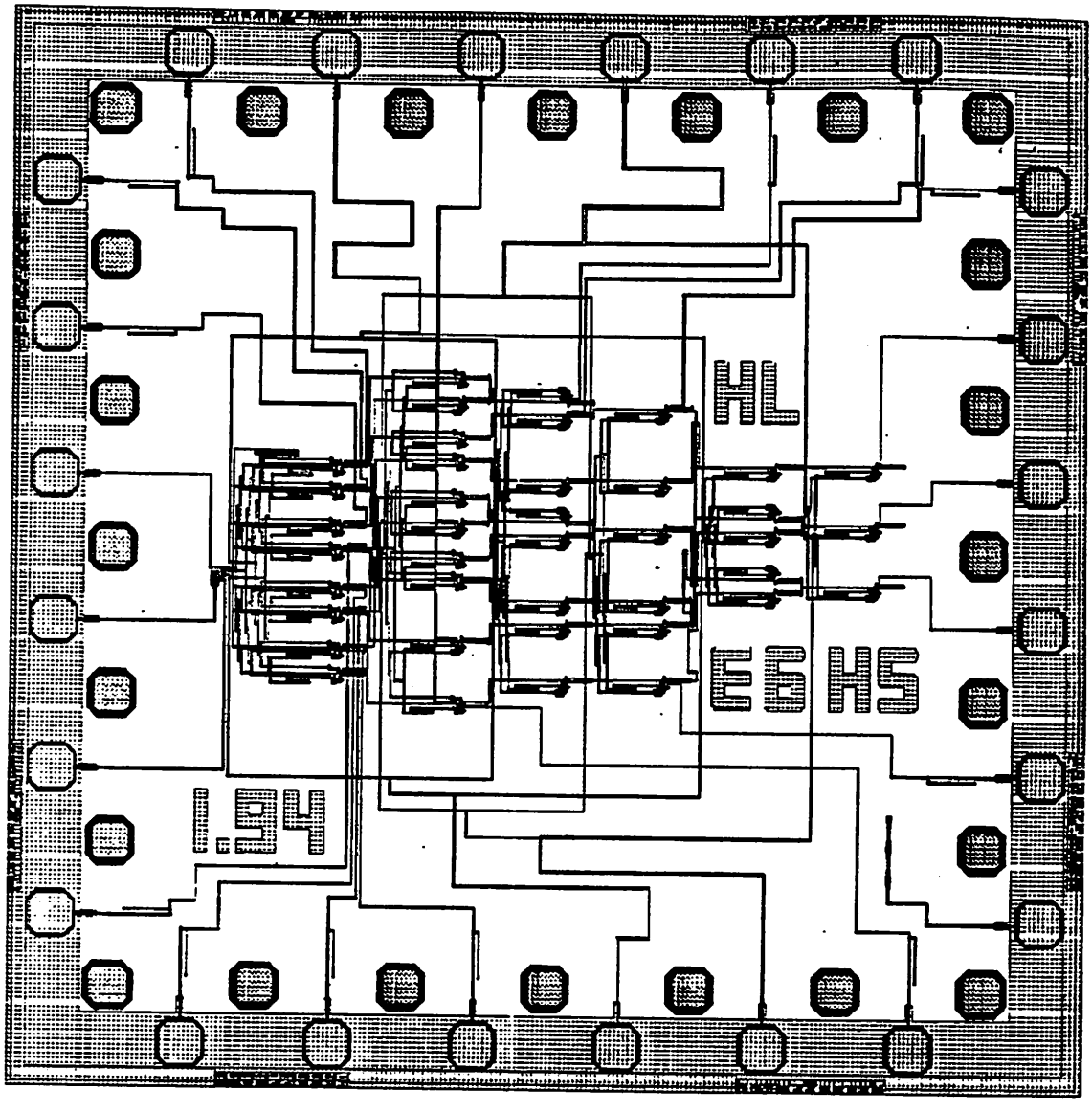


Fig. 4.13 Chip layout of the 3-bit analog-to-digital converter for high-speed testing.

we have written C programs and used them extensively to automatically generate all the subcells, including junctions, resistors, and various contacts (see Appendices C.1, C.2, and C.3 for the actual programs). Simple as they are, the programs has saved us a lot of time

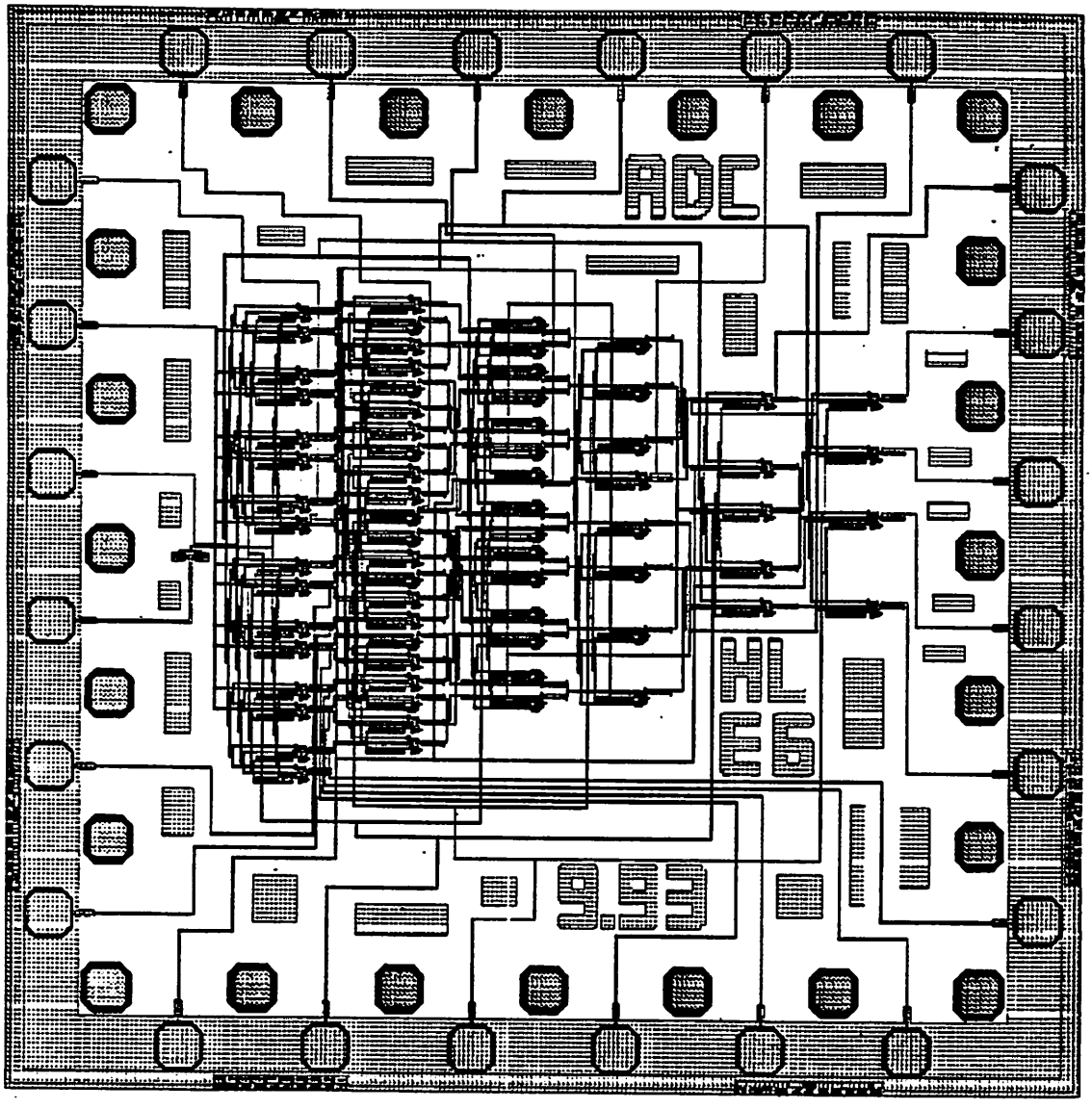


Fig. 4.14 Chip layout of the 4-bit analog-to-digital converter for high-speed testing.

and tedious effort in laying out the circuits, but most importantly, they have helped minimizing the chance of making layout errors.

To maintain symmetry in the quantizers, 2^N comparators have been laid out although only 2^N- 1 of them are required. The extra one at the bottom can be used for testing purposes or simply left unused. The three-bit converter requires a total of 320

Josephson junctions, out of which 56 are for the quantizer, 60 for buffers and inverters, and the rest is for the binary encoder. The four-bit version requires a total of 730 junctions, out of which 128 are for the quantizer, 176 for buffers and inverters, and the rest for the binary encoder.

Since the converters are to be tested at multi-gigahertz frequencies, all high-speed issues need to be considered carefully not only in design and layout but also in testing phases. For example, it is really important that all the input and output lines are designed and laid out in such a way that they have matching impedances and terminations and that all the input and clock signals are skewed from one another as little as possible. Chapter 7 will discuss in full detail all these issues together with our solutions.

4.6 Summary

This chapter described our design and fabrication of complete three-bit and four-bit analog-to-digital converters with multi-gigahertz clock and input frequencies. Fully parallel architecture has been used, rather than the periodic-threshold, because we want to achieve an ADC with highest possible conversion speed. High-performance comparators have been realized with one-junction SQUID as a sampler and a two-junction SQUID as a readout device. A small aperture time has been obtained by using another one-junction SQUID as a pulser at the input of each comparator. A new logic family, based on the same comparator configuration, was developed to implement the thermometer-to-binary encoder. In doing so, quasi-three-input and quasi-four-input XOR gates have been conceived and used to simplified the chip design and area. To the best of

our knowledge, these are the first complete ADCs ever reported in superconducting technology that include a thermometer-to-binary encoder to achieve binary output.

Chapter 5

PERFORMANCE OF FULLY PARALLEL JOSEPHSON ADC

5.1 Low -Speed Performance

Test structures have been laid out to measure the device parameters. Shown in Fig. 5.1 is the measured threshold curve for the readout two-junction SQUID used in the comparators and the logic gates. The measured parameters for the critical current, the

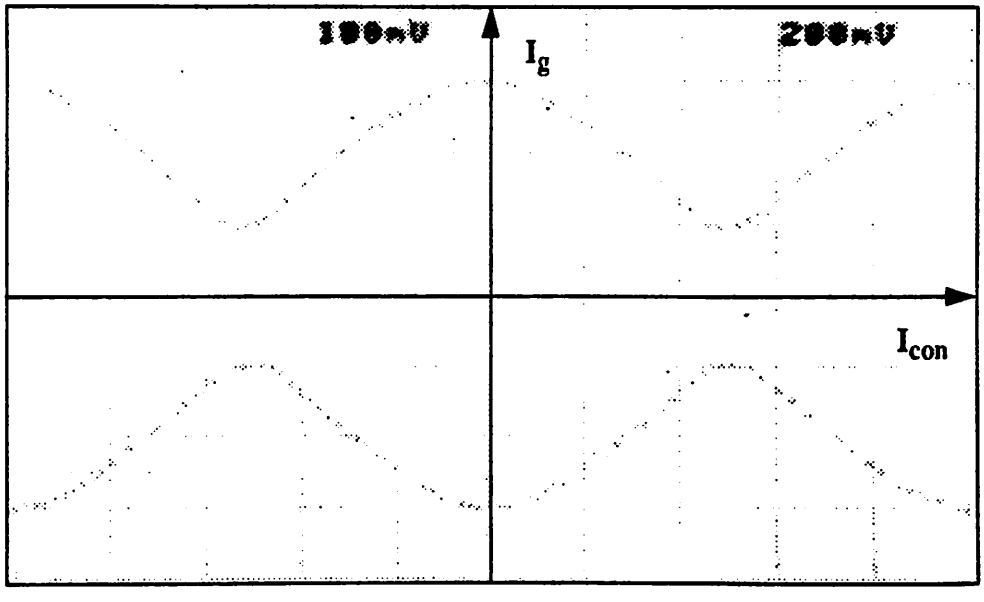


Fig. 5.1 Measured threshold curve for the readout two-junction SQUID.

optimal control current, and the modulation are 300 μA, 500 μA, and 66% compared to the designed values of 320 μA, 450 μA, and 66%, respectively.

The actual circuit and the measured threshold curve for the readout SQUID with the inclusion of a single edge-triggering junction in series are shown in Fig. 5.2. As expected, the threshold curve is clipped due to the smaller critical current of the single junction compared to that of the two-junction SQUID.

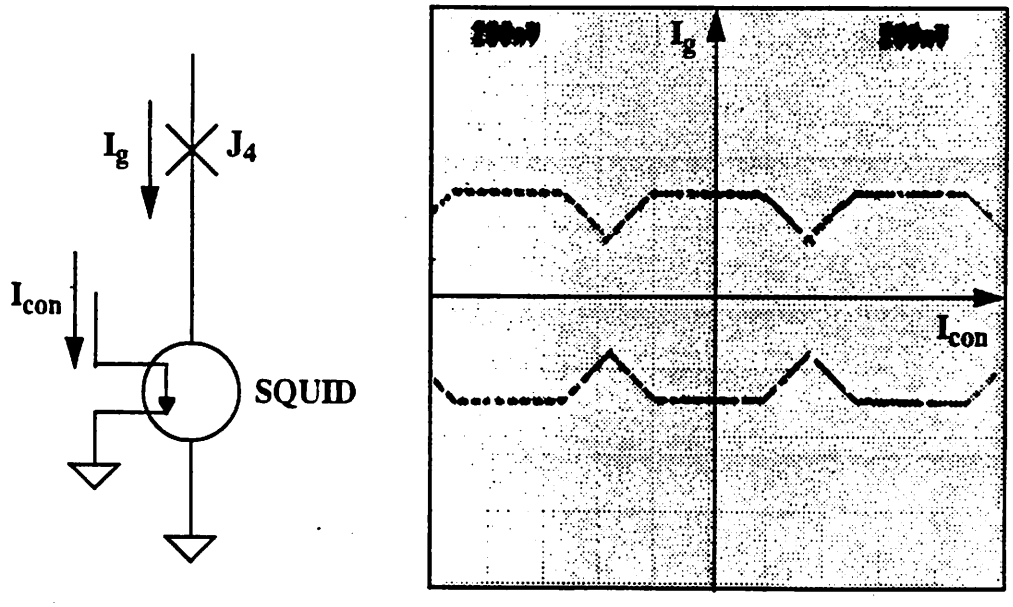


Fig. 5.2 Measured threshold curve for the readout SQUID with the edge-triggering junction.

Functionality of the comparator circuit described in Fig. 4.4, both as a comparator and as a logic gate, has been successfully demonstrated. All single-stage logic gates, including inverters, AND, OR, NAND, and NOR, work with low-speed bias margins of ± 30% and ± 50% for the first clock and the second clock, respectively. More complicated logic gates that require a cascade of many such simple gates, such as NAND driving an

inverter, two-stage buffers, three-input quasi-XOR gates, etc., have also been tested and shown to function correctly. The low-speed bias margins achieved for these cascaded gates are reduced to ± 20% for the first clock and to ± 30% for the second clock.

As an example, shown in Fig. 5.3 is the test result of a three-input quasi-XOR gate described in Fig. 4.10 in Chapter 4, which comprises two NAND gates driving another NAND gate with inputs being thermometer-coded. The first three traces are the three-phase clocks; the next three traces are the thermometer-coded inputs starting from the least significant level; and the last trace is the output of the whole quasi-XOR gate. Since the gate pipelines two consecutive stages, the gate latency is one full clock cycle, which means that the output for any input combination is not valid until one clock cycle later.

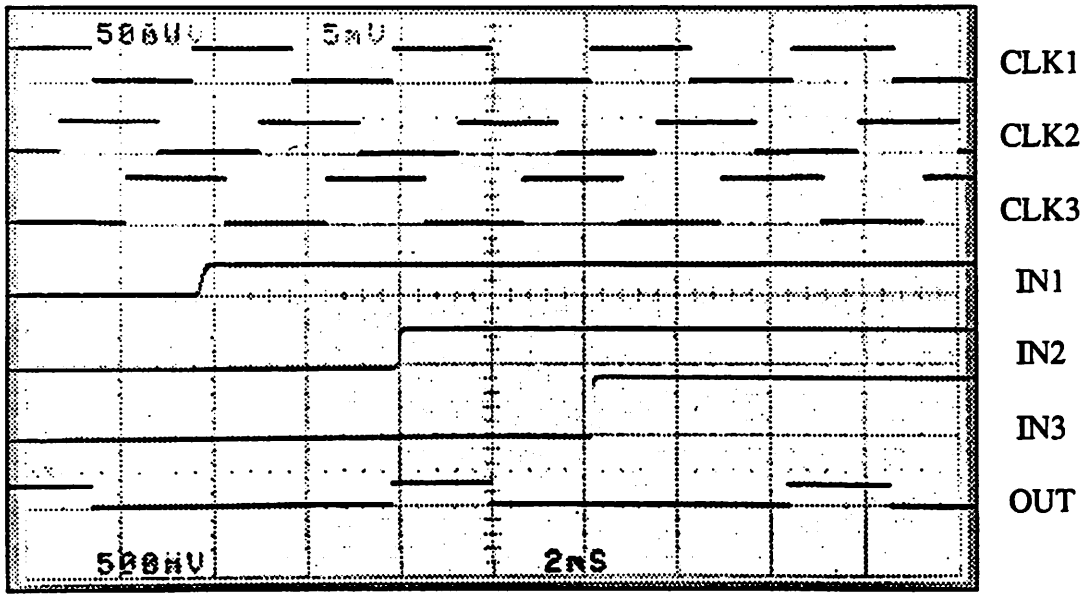


Fig. 5.3 Testing results for the three-input quasi-XOR gate shown in Fig. 4.10.

5.1.1 Two-Bit Quantizer and Two-Bit Binary Encoder

We have also performed functionality tests on a two-bit quantizer and a two-bit encoder separately [40]. The experimental results are shown on Figs. 5.4 and 5.5,

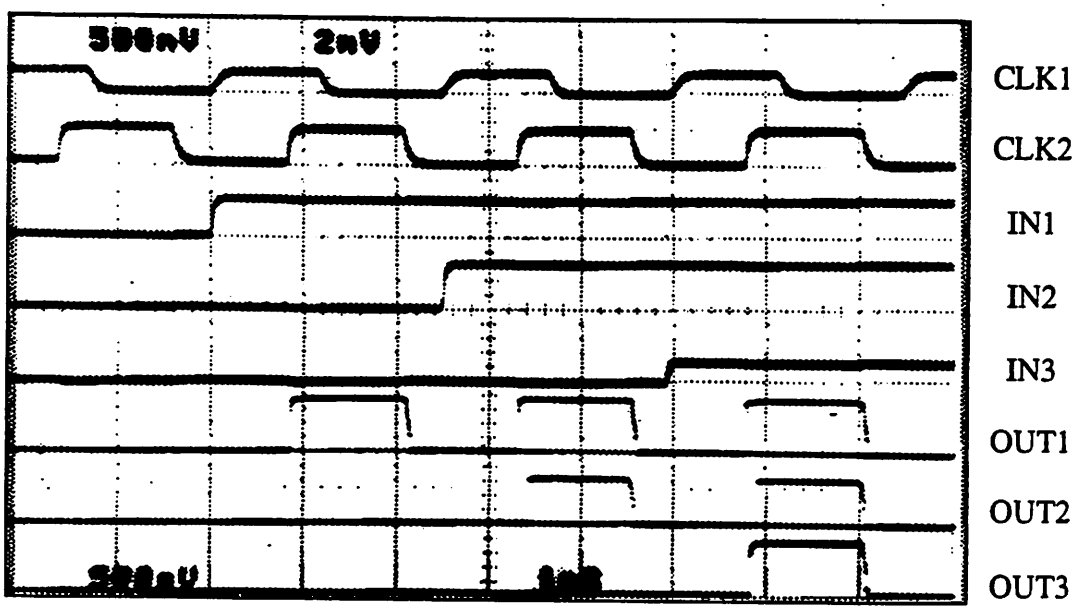


Fig. 5.4 Test results verifying the correct function of a two-bit quantizer.

respectively. In Fig. 5.4, the first two traces are the two out-of-phase clocks; the next three traces are three different analog inputs that are superimposed on each other and divided evenly among the three comparators in the quantizer. With the threshold levels of the three comparators set 100 μA apart, this choice of inputs covers all the possibilities. As expected, the outputs of the quantizer, the last three traces in the figure, are in the correct thermometer code.

Figure 5.5 shows the low speed test results for a two-bit thermometer-to-binary encoder. The first three traces are the three-phase clocks. The next three traces are the inputs to the encoder, which are in thermometer code and correspond exactly to the outputs obtained for the quantizer in Fig. 5.4. The outputs of the encoder shown in the last two traces indicate the correct operation of the binary encoder.

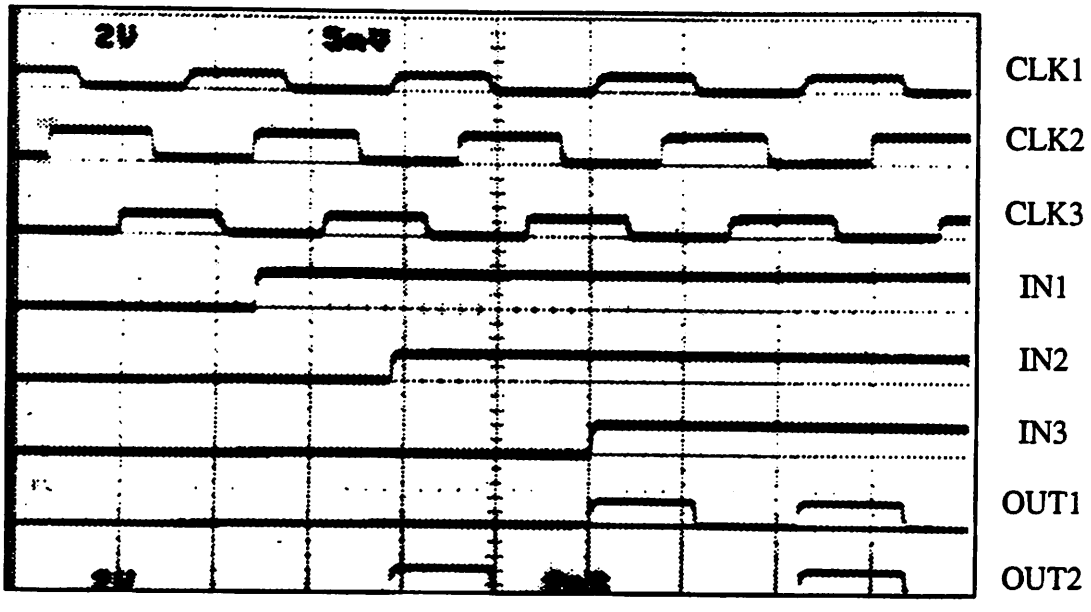


Fig. 5.5 Measurement of a two-bit thermometer-to-binary encoder.

5.1.2 Three-Bit Quantizer and Three-Bit Binary Encoder

More importantly, we have succeeded in verifying the correct operation of a three-bit quantizer and a three-bit binary encoder [40]. Test results for a three-bit quantizer are shown in Fig. 5.6, where the top trace is a ramping input and the rest are the outputs of the seven comparators, starting from the highest level on the top. The input signal is

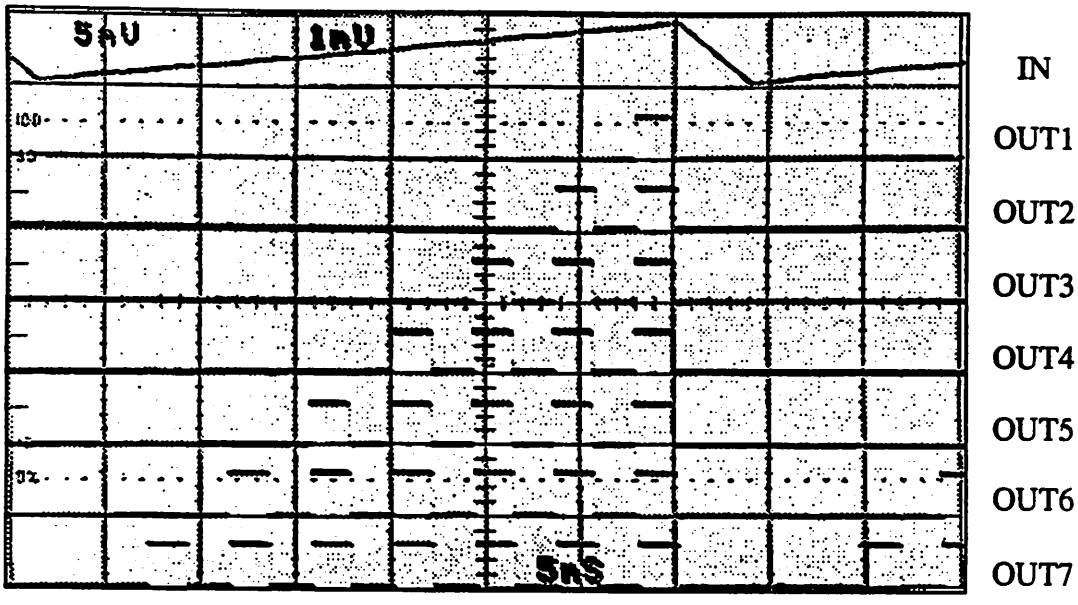


Fig. 5.6 Experimental results verifying the correct operation of a three-bit quantizer.

ramping from 0 to 2.1 mA, distributing 300 μA to each comparator. The comparators are biased 40 μA apart and clocked at 250 Hz.

Figures 5.7 and 5.8 show the outputs of the encoder corresponding to all possible combinations of the inputs. In each of the figures, the first three traces are the three-phase clock signals. For reference purposes, the truth table of a three-bit thermometer-to-binary encoder is included in Table 5.1. The outputs in Fig. 5.7 are obtained with the four inputs with highest levels being low and the other three inputs being shown as the middle three traces, which corresponds to the first four pattern combinations in Table 5.1. On the other hand, the outputs in Fig. 5.8 are obtained with the four inputs with lowest level being high and the other three inputs being shown as the middle three traces, corresponding to the last four pattern combinations in Table 5.1. All the outputs are correct and are delayed, as

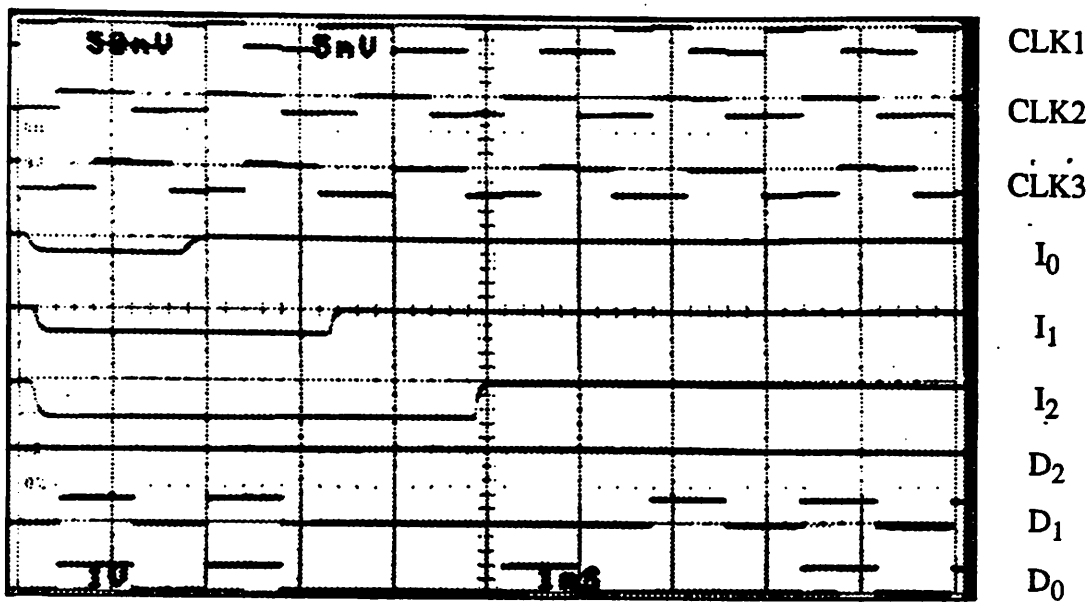


Fig. 5.7 Measurement of three-bit thermometer-to-binary encoder for the *first* four patterns shown in Table 5.1. The three middle traces are the three inputs with *least* significant level. *All other inputs are low.*

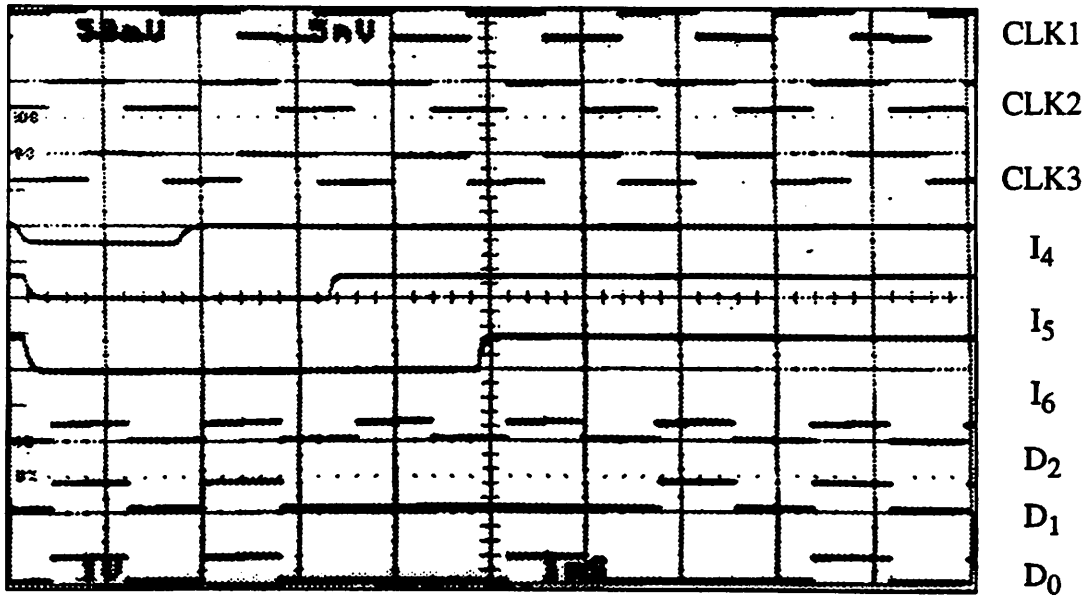


Fig. 5.8 Measurement of 3-bit thermometer-to-binary encoder for the *last* four patterns shown in Table 5.1. The three middle traces are the three inputs with *most* significant level. *All other inputs are high.*

Table 5.1 Truth table for a three-bit thermometer-to-binary encoder.

Thermometer Input							Expected Output		
Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

expected, $3^1/3$ clock cycles due to the pipelined latency of the entire encoder; the encoder is fully functional.

5.1.3 Four-Bit Quantizer

The design of the three-bit quantizer has been extended to a four-bit version, the layout of which is shown in Fig. 5.9. On the same chip, a second four-bit quantizer identical to the first has been laid out and connected for a redundant scheme. As designed, the dynamic range of each comparator is approximately 300 μA, and therefore, for a four-bit ADC, each quantization step (1 LSB) is 18.75 μA. The main problem is that this quantization step is only 6% of the critical current of the junction used in the one-junction

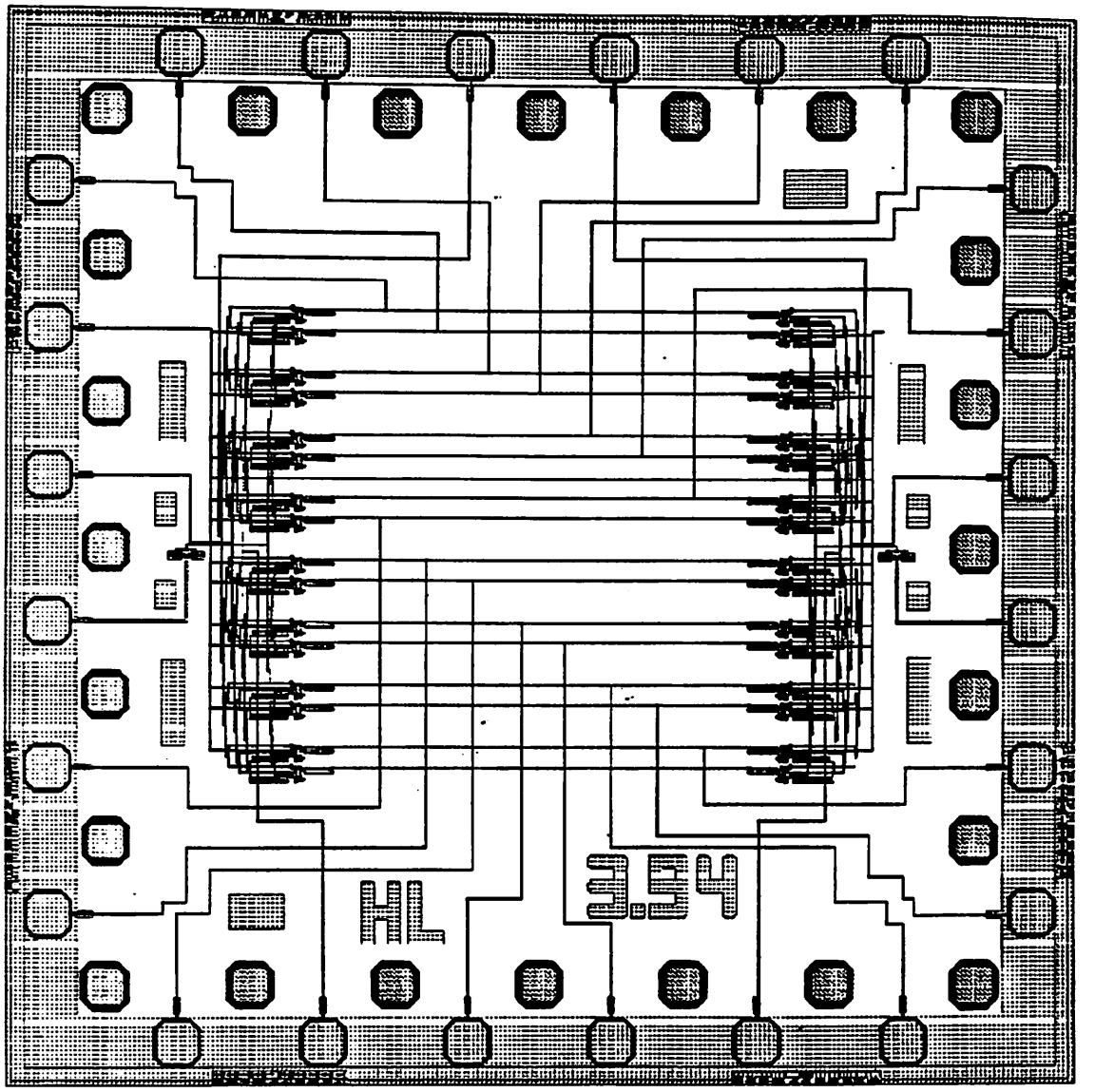


Fig. 5.9 Chip layout of two four-bit quantizers connected for a redundant scheme.

sampling SQUID, whereas the typical spread in the junction critical current in existing Hypres process has been found to be as large as 15%. If the process variations in resistor and inductors are also taken into account, it is most likely that each comparator offset would exceed this quantization step and that the quantizer would not work appropriately.

To measure the spread in the threshold level of each of the fifteen comparators used in a four-bit quantizer, the first two clocks and the input signal are applied to all the comparators at the same time. Under this test condition, all the comparators are expected to have the same circuit margins not only because they are designed to be identical but also because the clocks and the input are distributed equally to each of them. However, due to the spread of the process parameters, the measured margins vary so much that the overall circuit does not work. Figures 5.10, 5.11, and 5.12 give the bar charts showing the measured operating ranges of the input and the clocks for each of the fifteen comparators. Each vertical bar indicates the range of the operation for each comparator whose number is indicated on the horizontal axes.

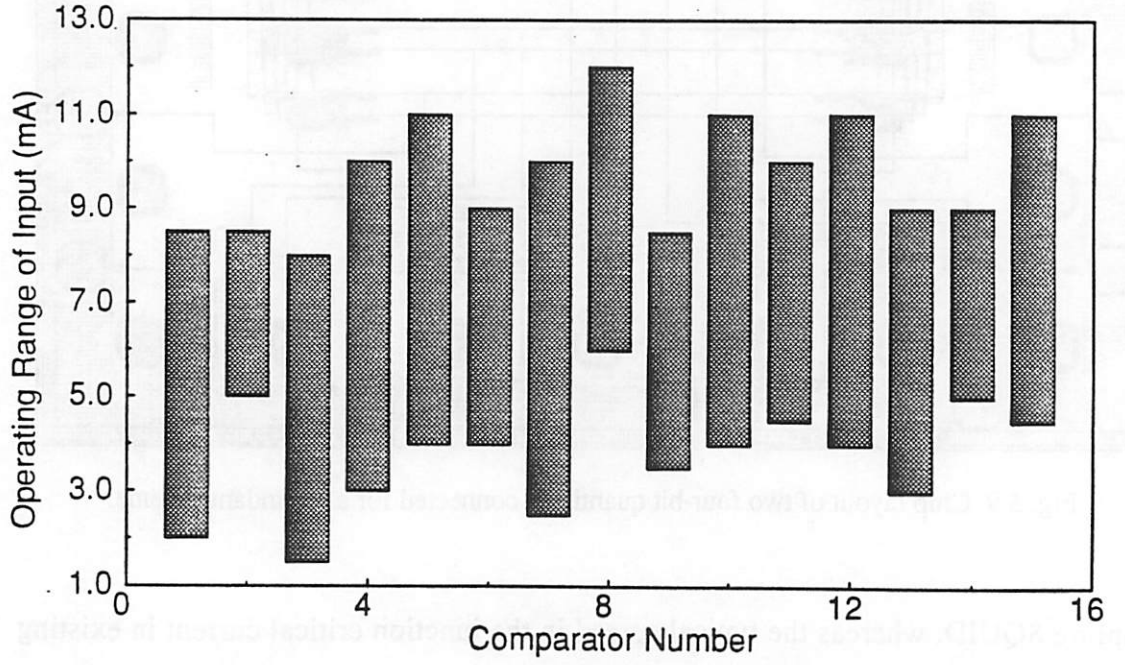


Fig. 5.10 Measured operating ranges of input for each comparator in a four-bit quantizer.

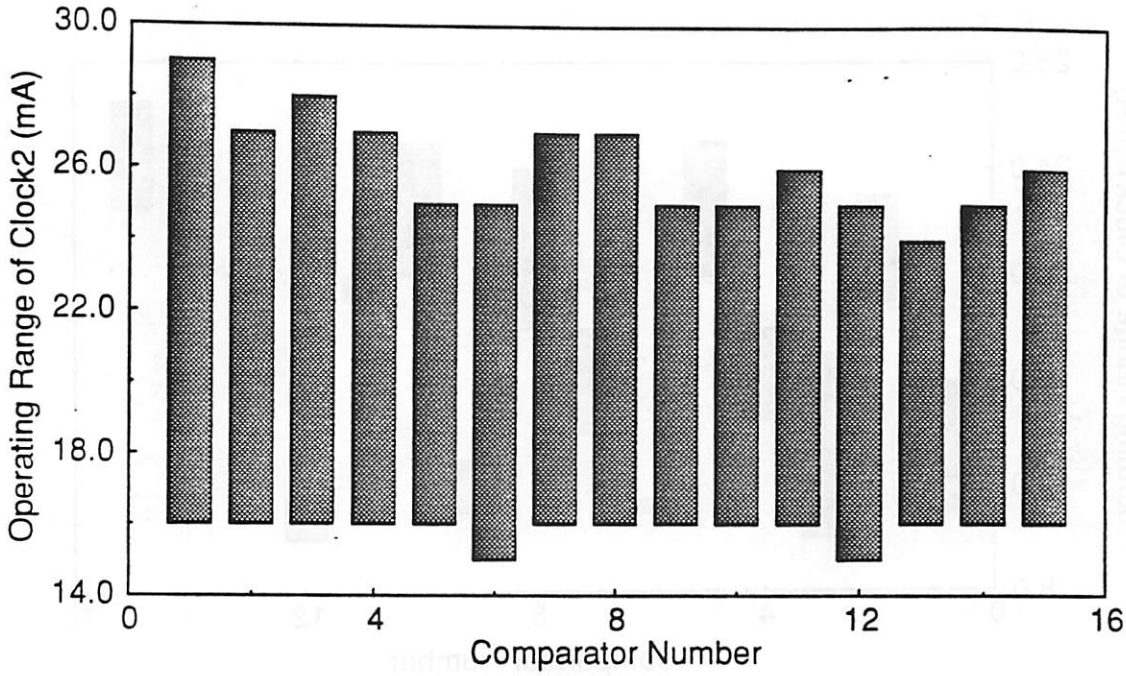


Fig. 5.11 Measured operating ranges of Clock 2 for each comparator in a four-bit quantizer.

For the second clock (Fig. 5.11), the operation regions are very wide and almost identical for all the comparators. However, for the input (Fig. 5.10) and the first clock (Fig. 5.12), the operation range varies a lot from one comparator to another. In particular, for the first clock, the comparators do not even have a common overlapping region for the entire circuit to work. Many chips from the same run have been tested, and similar results have been observed for all of them. Although the variations follow the same pattern, they are very random from chip to chip. Since the same results were obtained before and after we heated and cooled off the test chip (by pulling the probe out of the dewar and putting it back again and again), the possibility of flux trapping can be ruled out. Difference in operating regions must then be due to a wide spread in junction critical currents, and difference in the widths of operating regions (the heights of the bars) are due to the fact

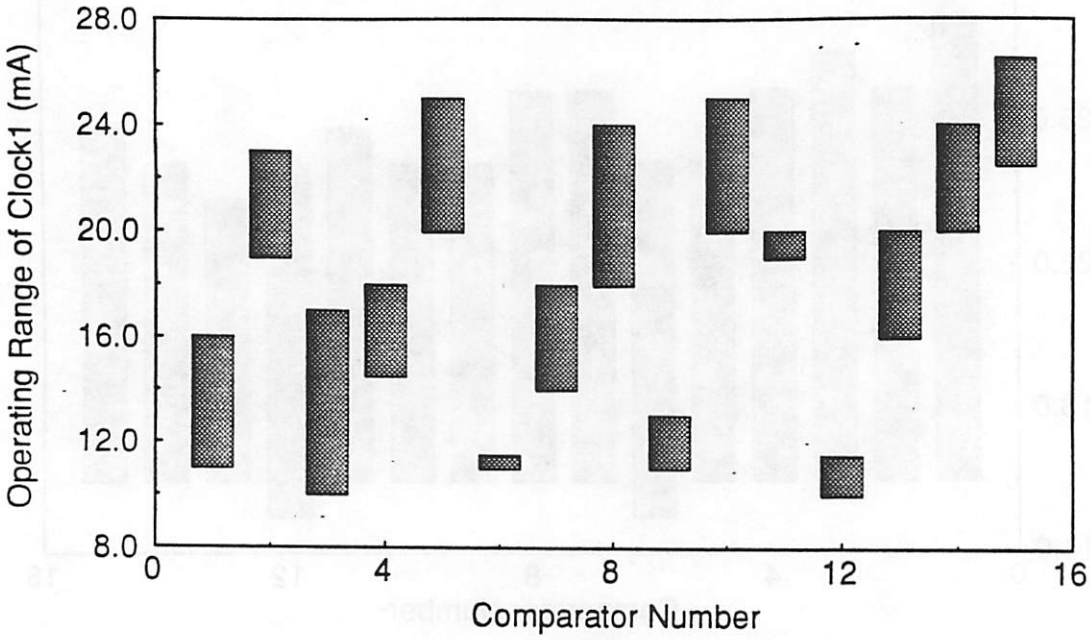


Fig. 5.12 Measured operating ranges of Clock 1 for each comparator in a four-bit quantizer.

that the critical currents of the edge-triggering junction J_6 and the one-junction sampling SQUID deviate from their nominal values in opposite directions. If these two critical currents come closer to each other, the operating regions get narrower. In the worst case, the operation margins become so small that the circuit almost fails to work at all, as can be seen in Fig. 5.12 for comparators #6 and #11.

The striking difference between operation margins for Clock 1 and Clock2 can be well explained as follows. It has been found that Josephson junctions that are laid out right on or very close to ground contacts have bad IV characteristics and bad uniformity in critical current due to stress problems [41]. Although there are no concrete experimental data available, circuit designers at Hypres has always tried to avoid such a problem either by using the same metal layer for junction's base electrode as a ground plane or by

following implicitly a design rule of 10 μm minimum spacing between junctions and ground contacts [42]. Unfortunately, neither of these was done in our designs. Figure 5.13 shows the actual layouts of one-junction sampling SQUID and two-junction readout SQUID for the comparators and the logic gates. For one-junction sampling SQUIDs, the ground contacts are only 1 μm away from the junctions to minimize the chip area, whereas for two-junction readout SQUIDs, the ground contacts are 7.5 μm away simply because of the presence of the damping resistors. As a result, it is reasonable to expect that the uniformity in junction critical current of one-junction SQUIDs is much worse than that of two-junction SQUID. This is confirmed by observing the bar graphs for the input shown in

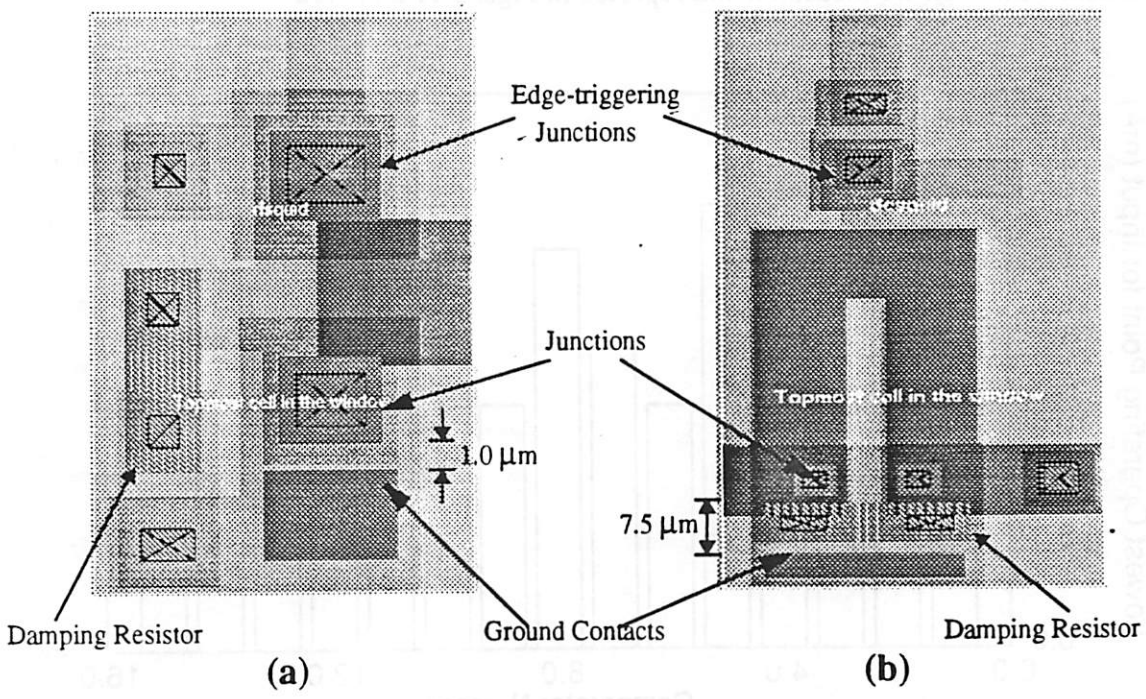


Fig. 5.13 Layouts of (a) one-junction SQUID and (b) two-junction SQUID showing the spacing between the junctions and the ground contacts.

Fig. 5.10. Because the input is applied directly to the one-junction SQUID, the lowest point of each of bar graphs corresponds to the threshold of the SQUID, which is determined by the junction critical current and the loop inductance. As reference, these operating points are plotted in Fig. 5.14, from which it can be seen that the spread in threshold level of these SQUIDs, mainly due to the spread in junction critical current, is as large as 50%.

Since one-junction sampling SQUIDs and two-junction readout SQUIDs are powered by the first and second clocks, respectively, it follows that the comparators have bad operating margins in the first clock and good margins in the second clock, which is consistent with what we measured and reported in Figs. 5.11 and 5.12.

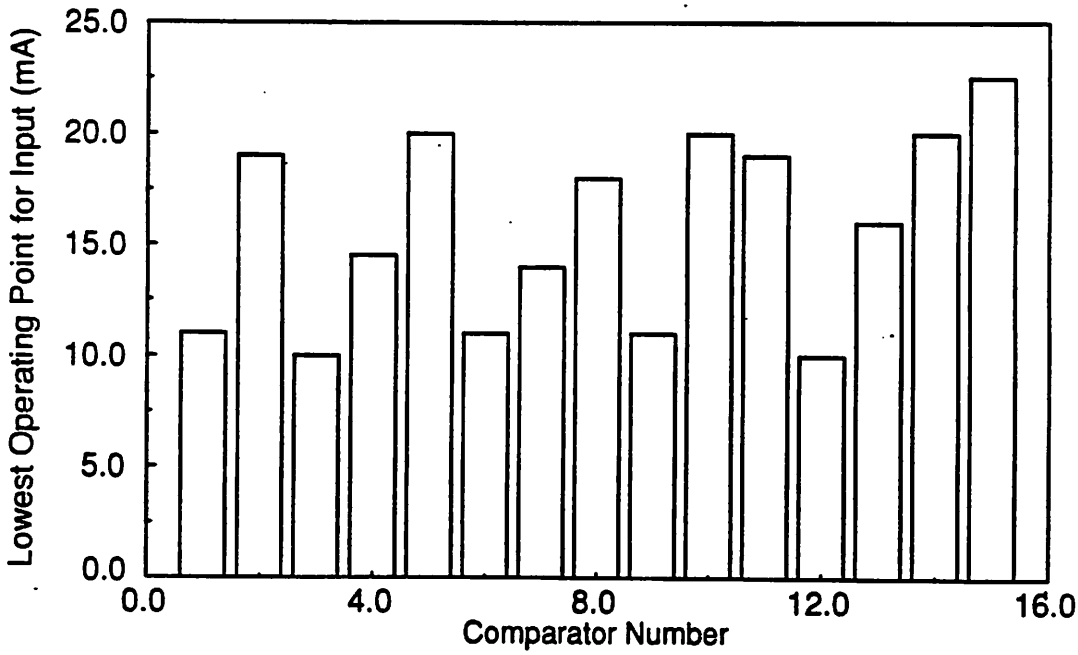


Fig. 5.14 Measured lowest operating point for the input for each comparator in a four-bit quantizer.

If the reference level can be adjusted individually for each comparator, small parameter variation and comparator offset can be compensated and the circuit can be made to work. However, due to the limited number of I/O pins, we have no choice but to use a single external reference signal and an on-chip divider network to provide reference signals to all the comparators. A feasible solution to such a large spread, small quantization step, and limited number of I/0 pin is to use a self-calibration scheme that automatically detects and adjusts the input bias to null out the offset. Such a scheme has been proposed by Fang [14] and has been implemented by Kishore et al. [43].

To increase the chance of getting fifteen comparators to work, we have employed a redundant scheme using two identical four-bit quantizers on the same chip, as shown in Fig. 5.9. Clocks, input, and reference signal are applied separately to each of the two quantizers, but their outputs are wire-ORed to each other, pair by pair. This way, we can individually test each of the quantizers and can replace any comparator in one quantizer by its counterpart in the other. By testing and selecting those comparators with better margins, a four-bit quantizer with an optimal margin can be achieved.

Such a redundant scheme has been fully tested, and its advantages are as expected. Measurement of operating regions of the first clock for the redundant quantizer is shown in Fig. 5.15. Although in this redundant quantizer, two comparators, numbers 7 and 11, do not work at all, there exist several other comparators that work better than their counterparts in the main quantizer. By selecting the best comparators in the two quantizers, that is, by combining Figs. 5.12 and 5.15, a much better overall margin is

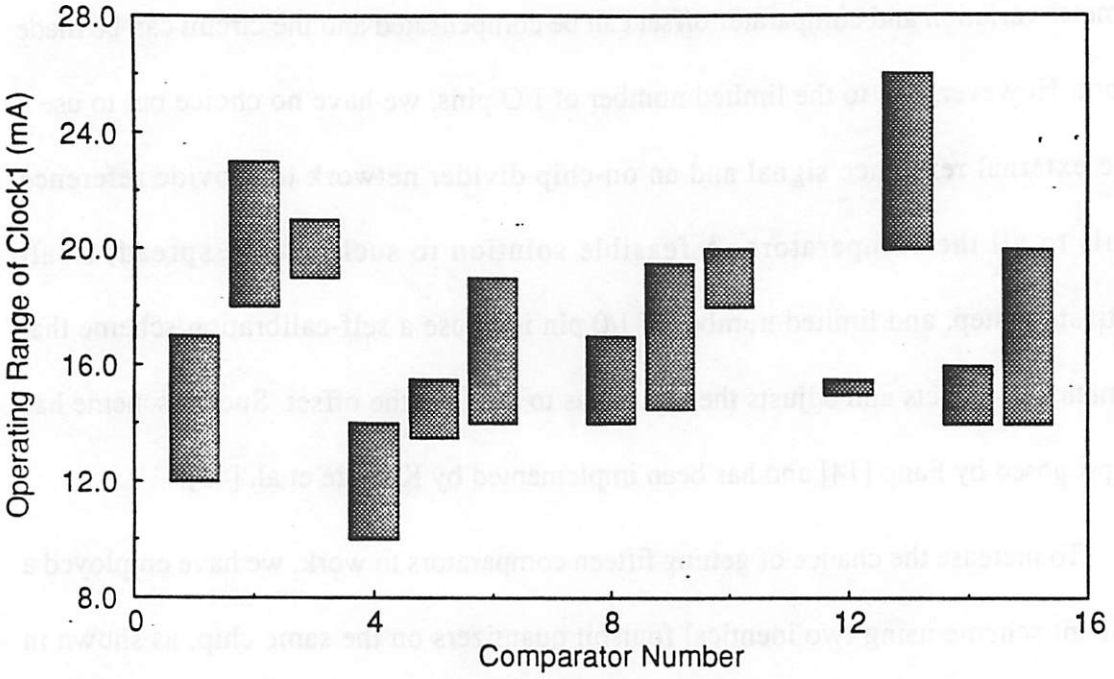


Fig. 5.15 Measured operating ranges of Clock 1 for the redundant four-bit quantizer.

achieved, as can be seen in Fig. 5.16. Unfortunately, this is still not good enough for the whole quantizer to work!

5.1.4 Three-Bit Analog-To-Digital Converter

Although we have successfully tested a three-bit quantizer and a three-bit binary encoder separately, the combination of the two for a complete three-bit ADC does not work. The same test that was done and described earlier for the four-bit quantizer is done for the three-bit quantizer of the ADC. The operating ranges of the clocks and the input for each of the seven comparators are plotted in Figs. 5.17, 5.18, and 5.19. As in the case for the four-bit quantizer, most comparators have very wide margins. In fact, the operating margins for the second clock shown in Fig. 5.18 are perfectly uniform. However, the

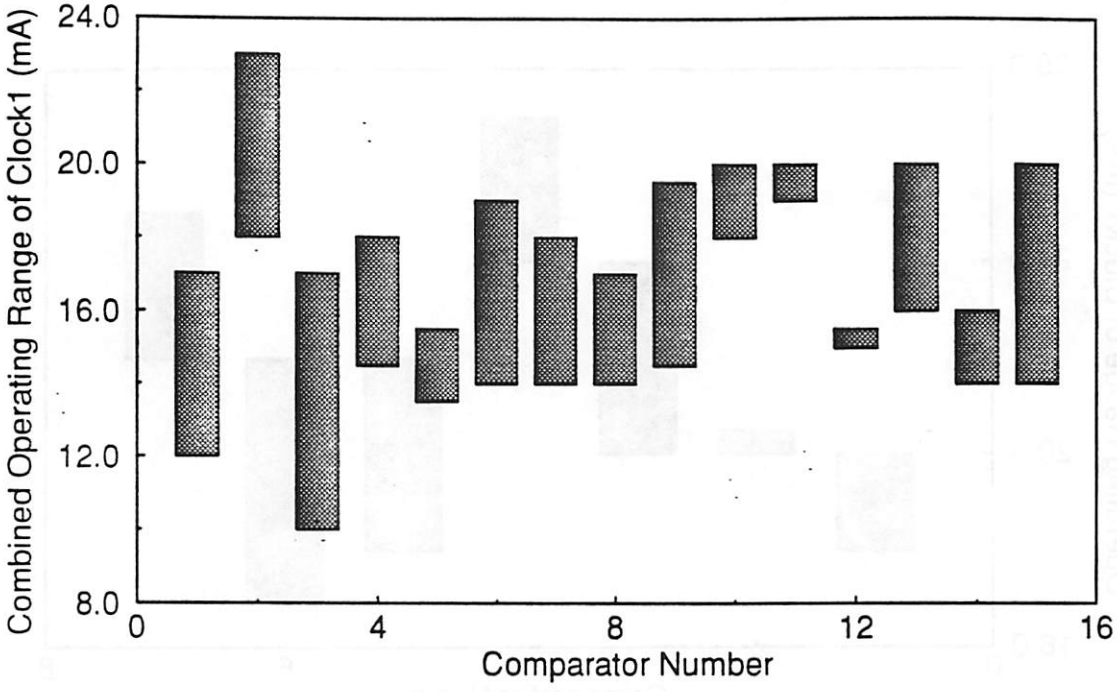


Fig. 5.16 Operating ranges of Clock 1 for the best fifteen comparators selected from the two four-bit quantizers.

operating regions for the first clock do not have enough overlapping for the quantizer to function correctly.

We have attempted to bypass the quantizer and test the three-bit binary encoder by feeding thermometer inputs directly to the output lines of the quantizer. The test was performed for two different chips. The input pattern and the measured outputs of the two chips are shown in Figs. 5.21, 5.20, and 5.22, respectively. Note that the outputs are delayed two and half clock cycles due to the pipelined latency. Included in Fig. 5.22 are also the first clock (the top trace) and two inputs Q_1 and Q_2 (the second and third traces). For both reference and clarity, the truth table of a three-bit thermometer-to-binary encoder shown in Table 5.1 is repeated in Table 5.2 together with the measured outputs.

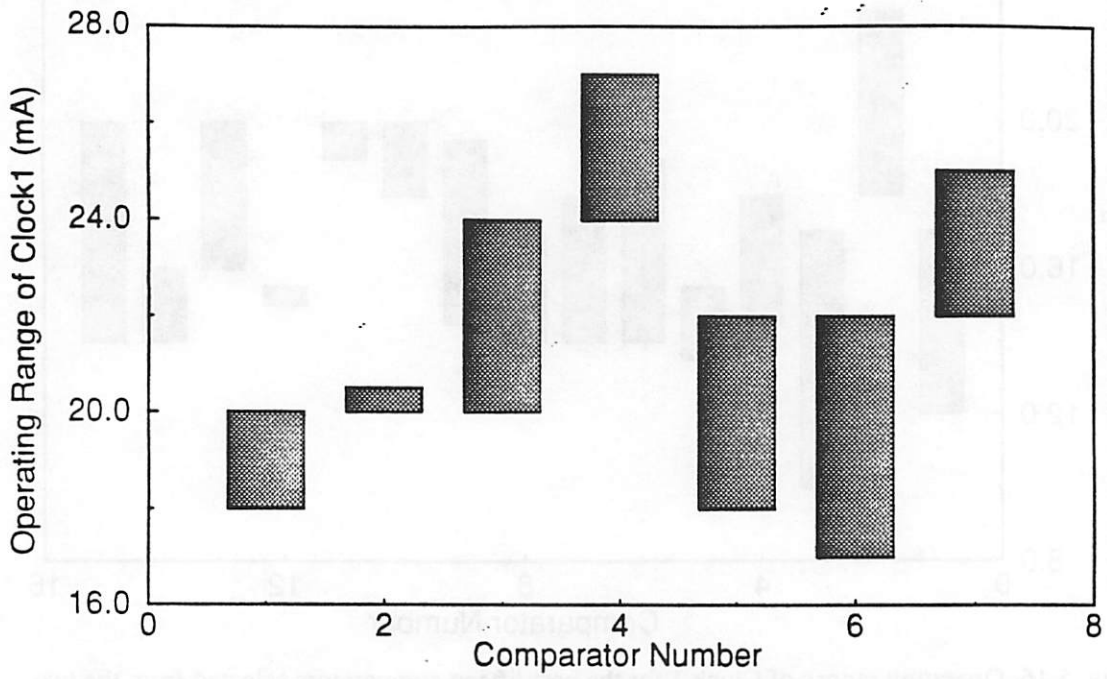


Fig. 5.17 Operating ranges of Clock 1 for the seven comparators in the three-bit ADC.

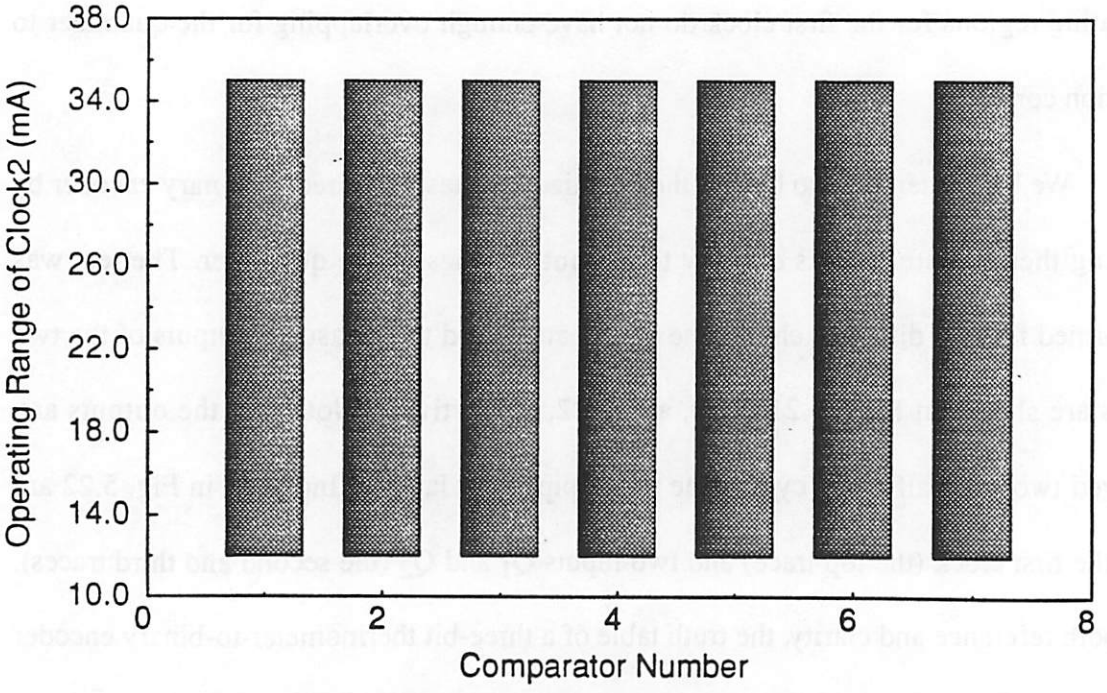


Fig. 5.18 Operating ranges of Clock 2 for the seven comparators in the three-bit ADC.

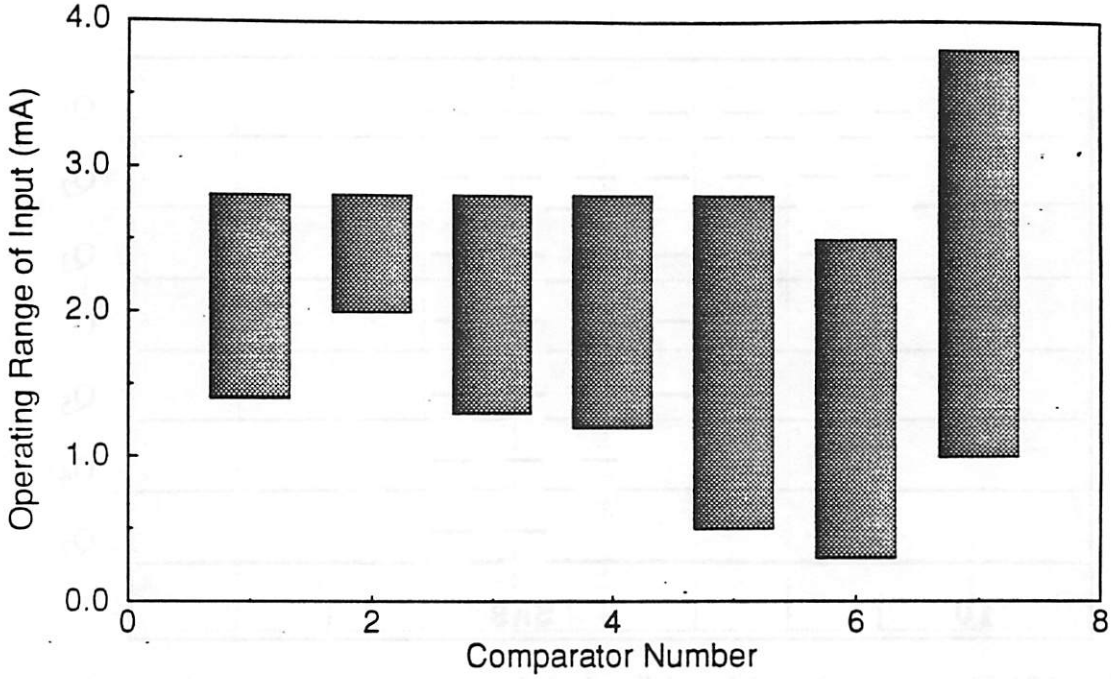


Fig. 5.19 Operating ranges of the input for the seven comparators in the three-bit ADC.

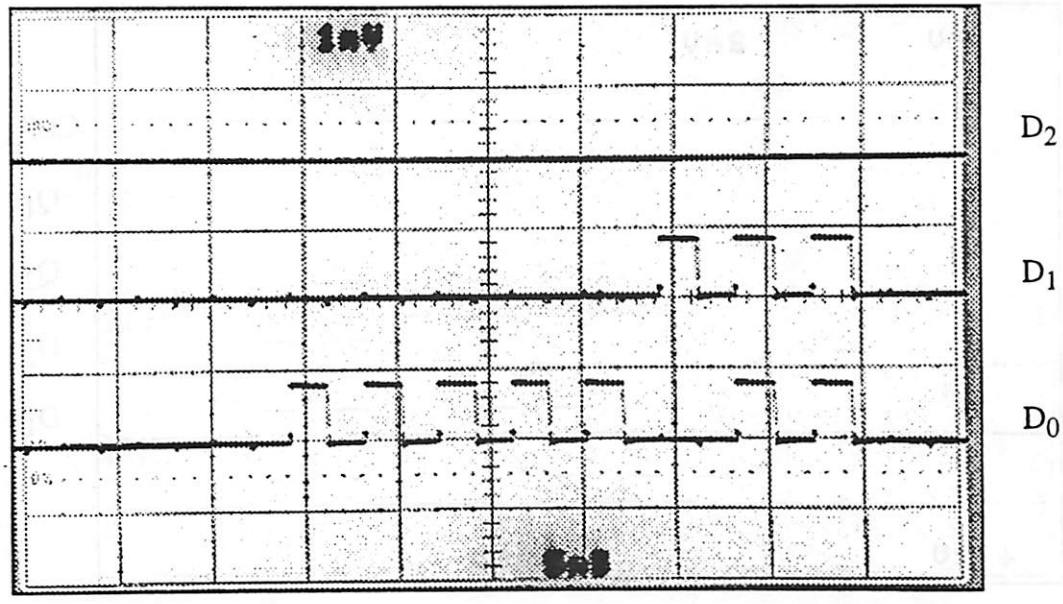


Fig. 5.20 Measured outputs of the ADC (Chip #1) with thermometer input shown in Fig. 5.21 being injected directly to the quantizer outputs.

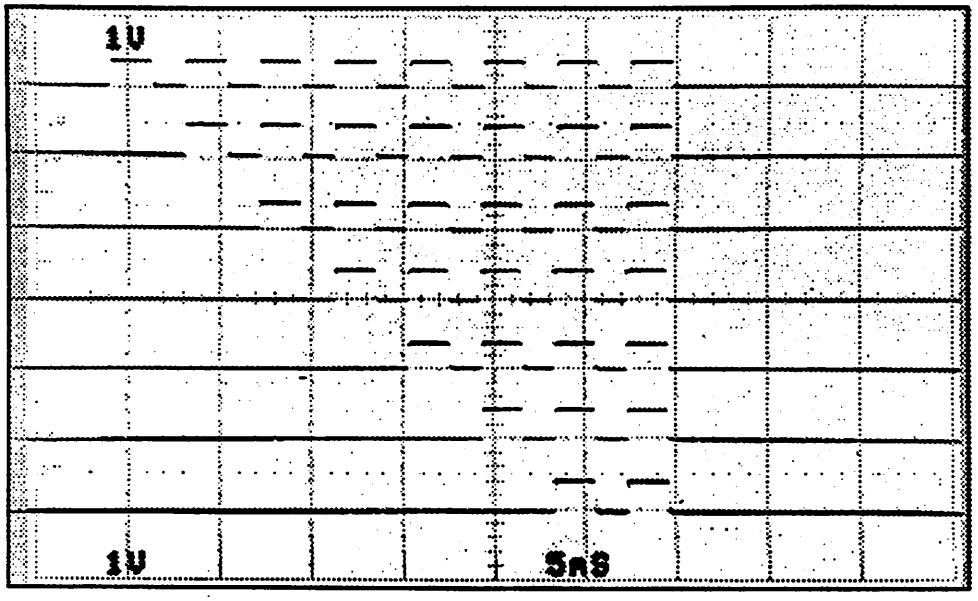


Fig. 5.21 Thermometer input injected directly to the quantizer outputs to test the encoder.

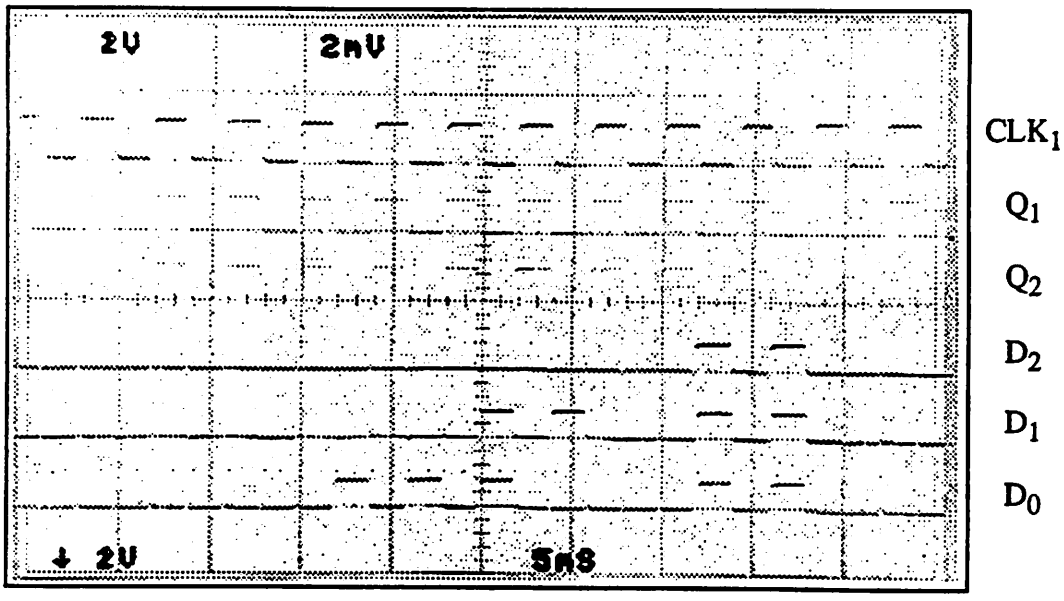


Fig. 5.22 Measured outputs of the ADC (Chip #2) with thermometer input shown in Fig. 5.21 being injected directly to the quantizer outputs.

Table 5.2 Truth table for a three-bit binary encoder together with the measured outputs.

Thermometer Input							Expected Output			Measured Output					
										Chip #1			Chip #2		
Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	D_2	D_1	D_0	D_2	D_1	D_0	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0	0	0	1	0	0	1
0	0	0	0	1	1	1	0	1	1	0	0	1	0	1	1
0	0	0	1	1	1	1	1	0	0	0	0	1	0	1	0
0	0	1	1	1	1	1	1	0	1	0	0	1	0	0	0
0	1	1	1	1	1	1	1	1	0	0	1	0	1	1	1
1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1

Obviously, the encoders for the two chips do not function correctly. For the encoder #1, the output D_2 never switches. Referring to the block diagram of the ADC in Fig. 4.11, all that we can deduce from this result is that at least one of the five buffers connected from the quantizer output Q_4 to D_2 does not work. When Q_2 changes from zero to one (from the second entry to the third in the table), D_1 and D_0 do not change their states as they are supposed to. It could be the result of malfunctionality of any of the gates connected in the path, including the buffer and the inverter connected to Q_2, the two-stage buffer, and the three bottom XOR gates. Since there is no one-to-one mapping of the

inputs to the outputs and since the inputs must be restricted to a thermometer code, we cannot figure out exactly on which gates the malfunctionality occurs.

As can be seen from the table, the output patterns obtained for the two encoders are different from each other. This fact enables us to rule out the possibility of layout errors. Judging from the measurement for the four-bit quantizer, it is reasonable to expect that the same problem described earlier for the comparators is also encountered for the logic gates and the encoder, that is, the spread in threshold level of one-junction SQUIDs is so large that there does not exist a common operating regions for all the gates to work.

Measurement of a series array of Josephson junctions of various sizes on the same run supports the fact that the spread in the junction critical currents is beyond the specification. Figure 5.20 shows the scope photograph of the measured IV curve of the array, and Table 5.3 summarizes the measurement for each junction in the array. As

Table 5.3 Measurement of the spread in the junction critical currents of a series array.

Junction Size (μm x μm)	Target I_c (μA)	Measurement of critical currents			
		Minimum I_c (μA)	Maximum I_c (μA)	I_c Spread (%)	Average ΔI_c (%)
4.0 x 4.0	160	80	120	50.0	-37.5
5.2 x 5.2	270	200	235	17.5	-19.6
5.2 x 6.5	338	250	270	8.0	-23.0
5.5 x 7.0	385	270	300	9.0	-26.0

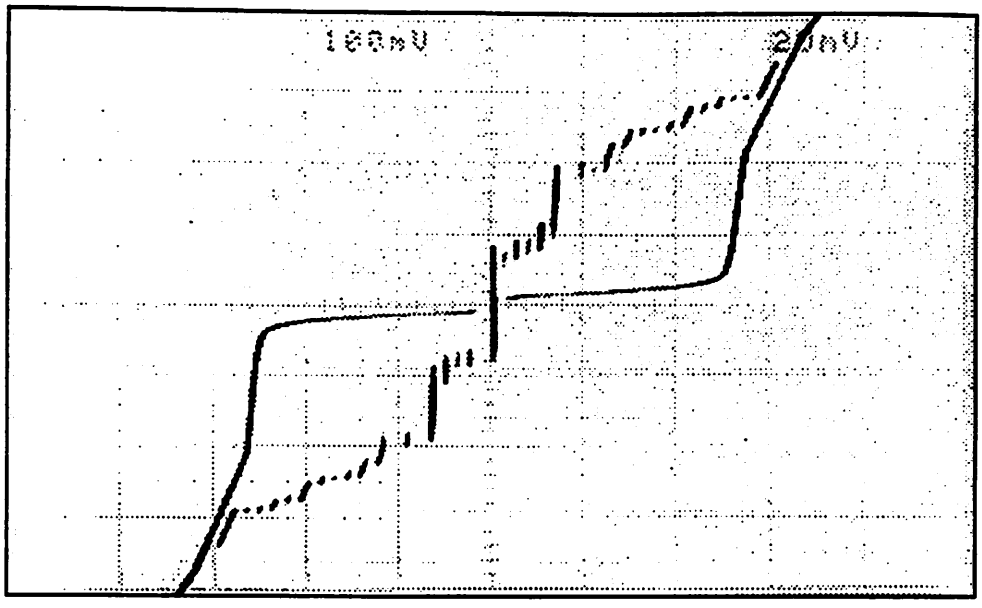


Fig. 5.23 Measured IV curve of a series array of Josephson junctions listed in Table 5.3.

expected, the variation in critical currents is worse for smaller junctions. For 4 μm x 4 μm, the average ΔI_c, defined as the percentage difference between the averaged measurement and the target value, is measured to be -37.5%. More critically, the spread measured between the minimum and the maximum critical current is as large as 50%, which justifies our margin measurement for the quantizers.

5.1.5 Four-Bit Analog-To-Digital Converter

We have also fabricated a complete four-bit ADC. However, experimentally we cannot get all fifteen comparators to switch simultaneously. Worse yet, for few chips, some comparators do not switch at all no matter how much the clocks are raised. We tried to apply a current directly to these two-junction SQUIDs through the output lines but still could not get them to switch to the voltage state. Inspection of the chips under a

microscope does not reveal anything suspicious. Since the comparators that do not work are random from chip to chip, the possibility of layout error can be ruled out. Flux trapping was not the problem because we heated the chip and cooled it down many times but, yet, the same results were obtained. For those comparators that could never be switched, it was likely that one of the junctions got shorted due to fabrication defects, possibly insulator pin holes, and prevented the entire comparator from switching at all. For those comparators that switched, the spread in junction critical current was probably so large that there existed no common operating window for all the comparators to work. As mentioned earlier, because our designs are based on edge-triggering circuits, they can tolerate large variation in absolute value of critical current density but are particularly sensitive to the spread.

5.2 High-Speed Signal Reconstruction

Extensive simulations with JSIM [44] have been carried out to verify the correct operation of the ADCs at their Nyquist input bandwidth and to fully exercise the ADCs at high clock frequencies [45] [46]. Both complete three-bit and four-bit ADCs were simulated with 2 GHz clocks and 980 MHz input sinusoidal signals. The binary outputs were reconstructed, down-sampled by two, and fitted with the best sine curves. Appendices C.4 and C.5 show the C programs we wrote for signal reconstruction and for best sinusoidal curve fitting. As can be observed from Figs. 5.24 and 5.25, the reconstructed signals and the fitted sinusoidal curves are closely matched. As expected, the frequency of the fitted signals were found to be 20 MHz, which is the beat frequency between the down-sampled clock (1 GHz) and the input signal (980 MHz). No missing

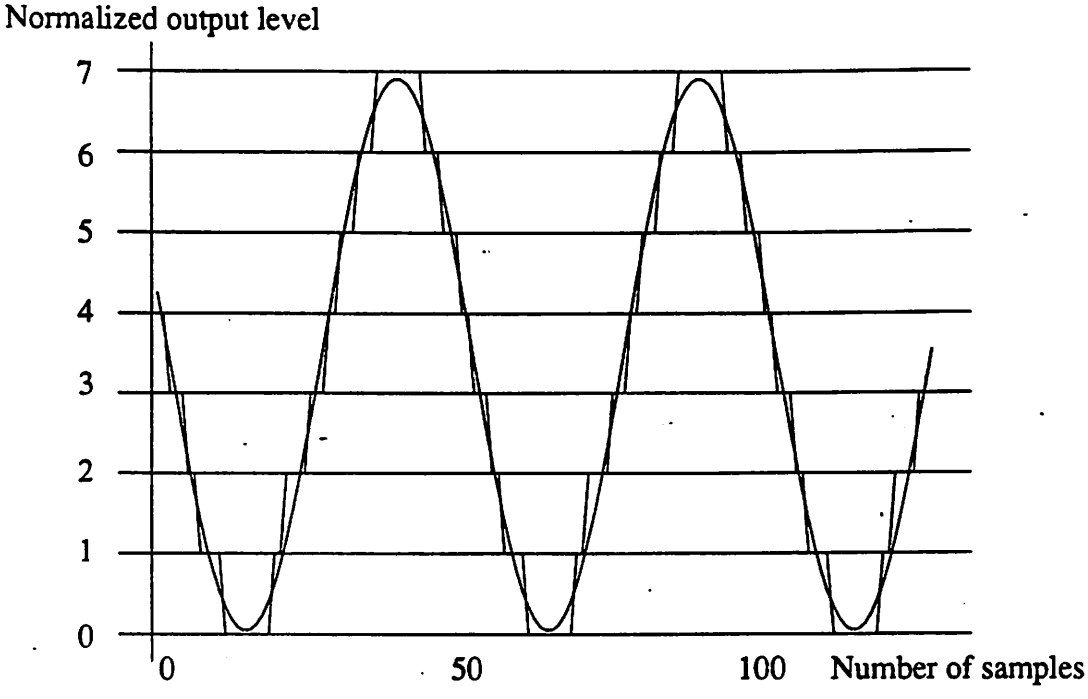


Fig. 5.24 Reconstructed and fitted signals for 3-bit ADC, f_{clk} = 2 GHz, f_{in} = 980 MHz.

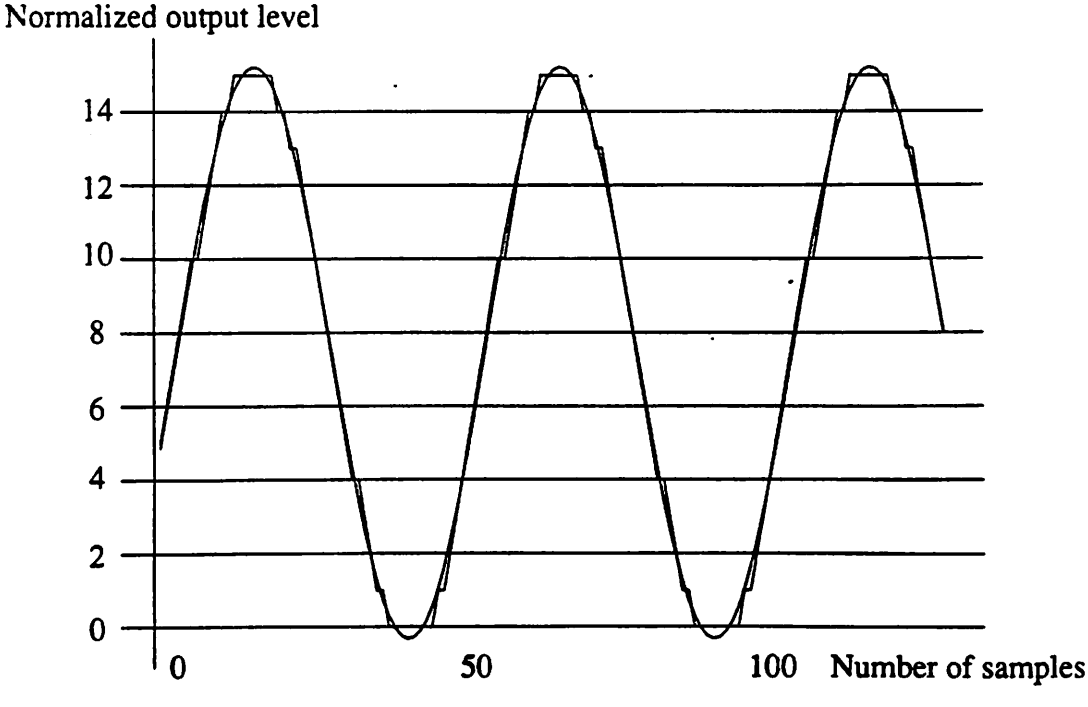


Fig. 5.25 Reconstructed and fitted signals for 4-bit ADC, f_{clk} = 2 GHz, f_{in} = 980 MHz.

code was observed; and both integral nonlinearity (INL) and differential nonlinearity (DNL) were below 0.5 LSB.

5.3 High-Speed Tests on Comparators

Test results performed at high speeds have been reported in [45] [46]. Figure 5.26 shows the experimental results for a single comparator with 2 GHz clocks and 1 GHz input. The first two traces are the two out-of-phase clocks; the third trace is the input; and the bottom trace is the output of the comparator after passing through an inverting amplifier. As expected, the output is high when the input is high and becomes low when the input is low.

The functionality of the comparator was verified experimentally up to 3 GHz, which was the maximum clock frequencies that our HP microwave amplifiers could

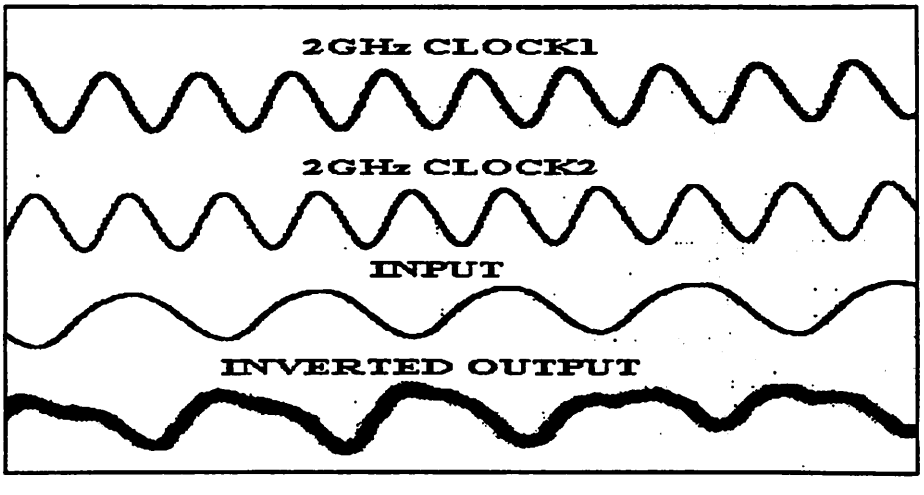


Fig. 5.26 Comparator's output tested with 2 GHz clocks and 1 GHz input.

operate at that time. The problem was that there was no input source that could be synchronized with the clock signals from an HP signal generator other than the 100 MHz signal available from the back of the same piece of equipment. As a result, we were restricted to test with 100 MHz input signals at 3 GHz clock frequencies, the result of which is shown in Fig. 5.27. A series of many 1s and 0s may not be a very interesting testing pattern but should be sufficient to demonstrate the operation of the comparator at 3 GHz.

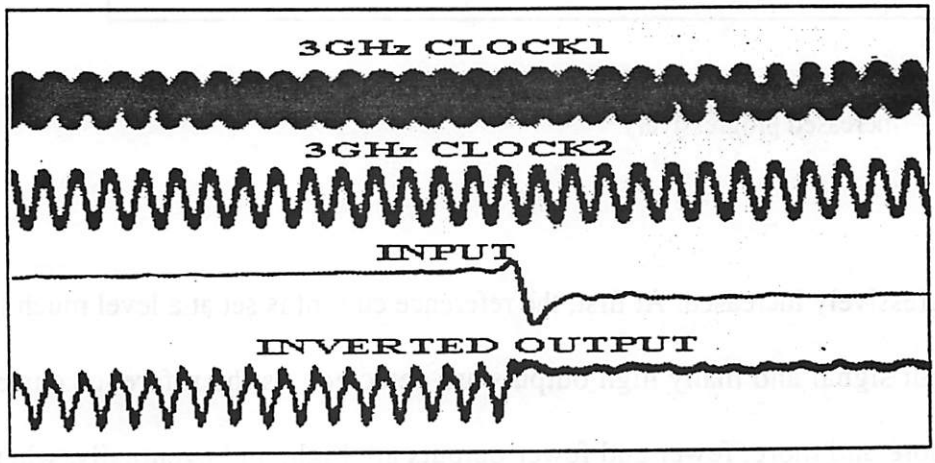


Fig. 5.27 Comparator's output tested with 3 GHz clocks and 100 MHz input.

The functionality of the comparator is further demonstrated in Fig. 5.28, where the comparator output is observed to switch properly as the applied reference current is varied. For clarity, the first-phase clock is not shown. The top trace is a 2 GHz second-phase clock; the second trace is a 100 MHz sinusoidal input; and the next six traces are the inverted outputs of the comparator as the reference current applied to the

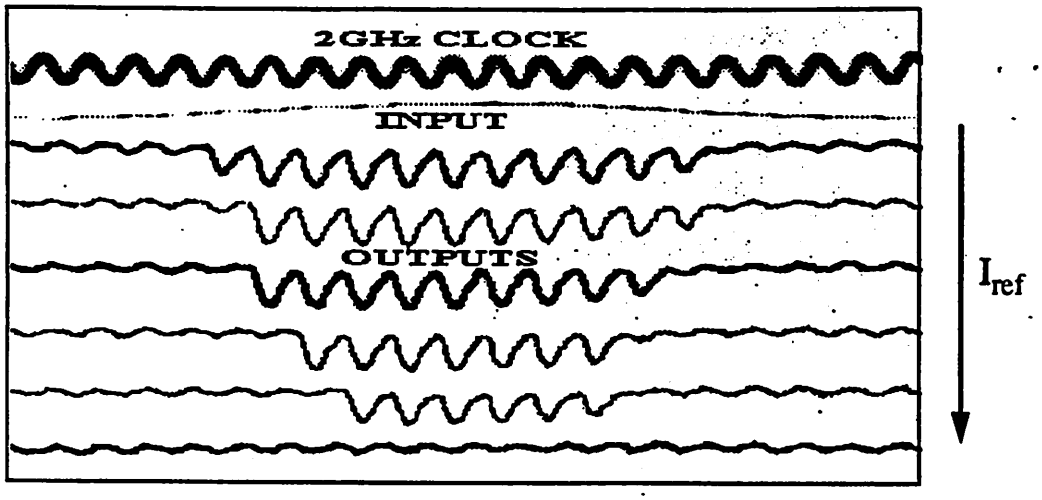


Fig. 5.28 Comparator's outputs tested at 2 GHz clocks and 1 GHz input as I_{ref} is increased progressively.

input is progressively increased. At first, the reference current is set at a level much lower than the input signal and many high outputs are detected. As the reference current is increased more and more, fewer and fewer outputs are high, and eventually, when the reference current is larger than the input amplitude, the comparator never switches, and all outputs are low.

Simulations have indicated that the speed of the comparator is mainly limited by the junction capacitance. A three-bit quantizer with seven comparators has been simulated successfully at clock frequencies as high as 16 GHz for an advanced superconducting technology with a critical current density of 5 kA/cm^2 and minimum junction area of 2 μm^2. The simulation results are shown in Fig. 5.29, of which the top trace is the ramping input and the rest are the outputs of the comparators starting from the second trace for the

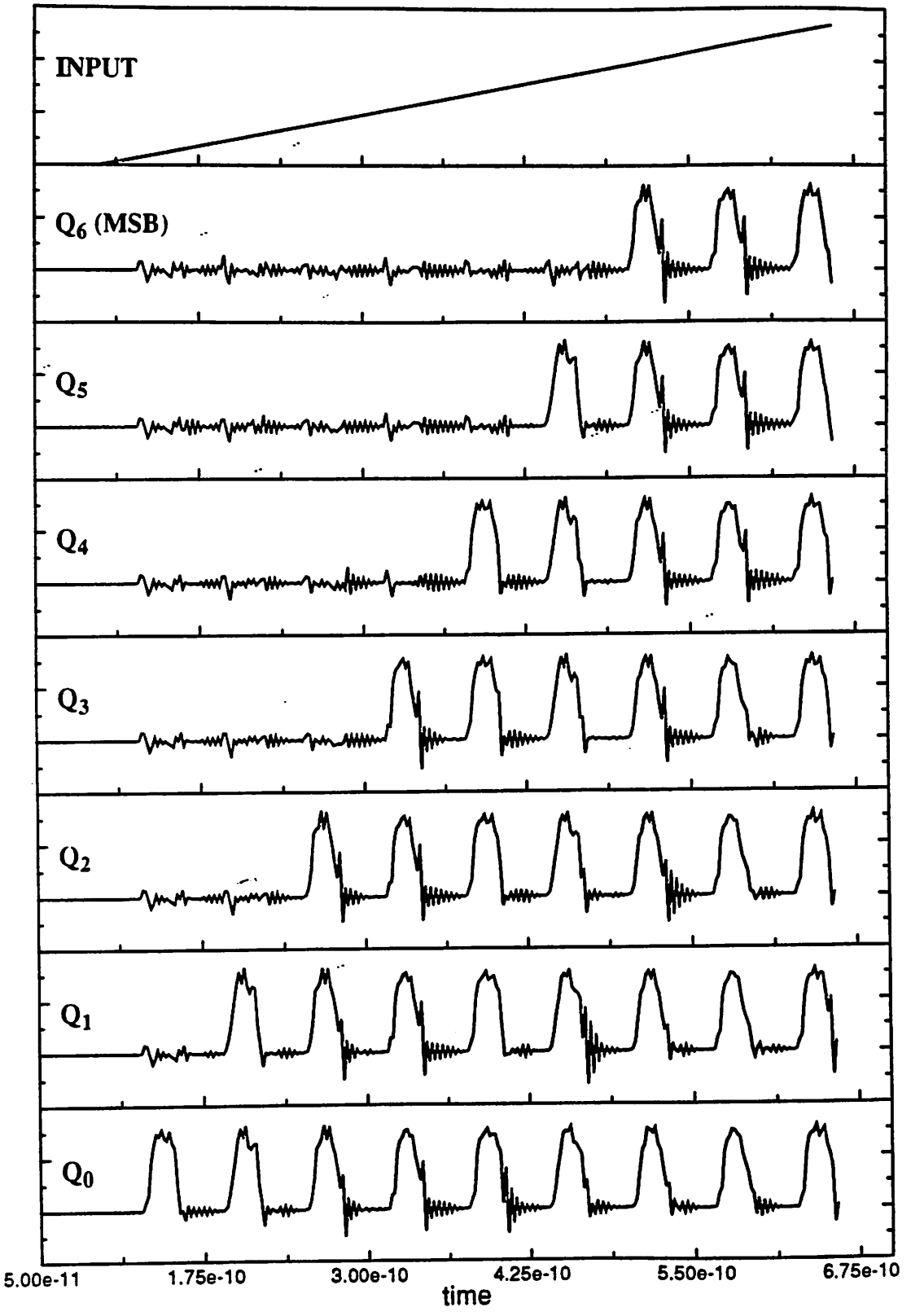


Fig. 5.29 Simulation results of a three-bit quantizer at 16 GHz clock frequency.

highest level Q6. At the beginning, the input is zero, and all the outputs are low. As the input is ramped up, the comparator for the lowest level switches first, then the second, the third, and so on. As expected, one after another, all comparators switch in a domino fashion and remain high after switching.

5.4 High-Speed Tests on Logic Gates

The operation of the logic family used to implement the thermometer-to-binary encoder has also been experimentally verified at multi-gigahertz clock frequencies [45] [46]. Again, due to the limitation of test equipment, we were able to test the logic gates only up to 3 GHz. In Fig. 5.30 are the test results for a two-stage buffer, a cascade of two OR gates. The top three traces are three 120°- out-of-phase 3 GHz clocks; the fourth trace

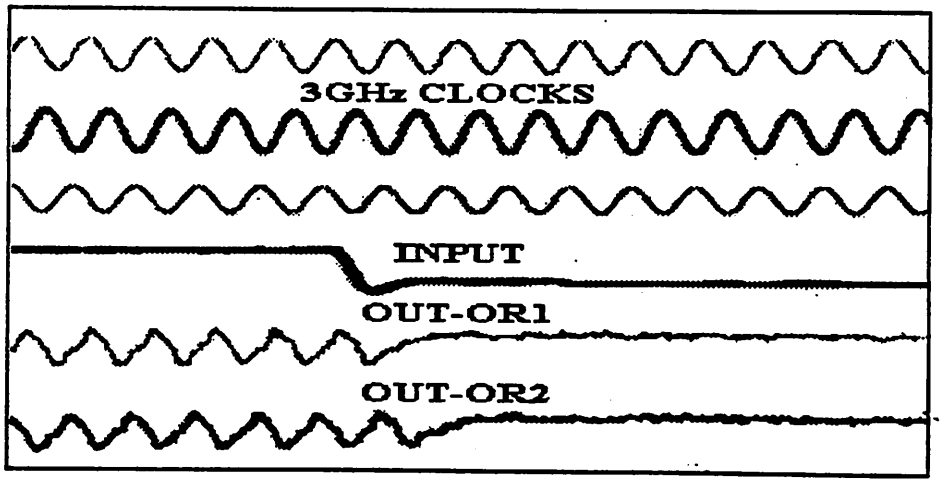


Fig. 5.30 Test result for a two-stage buffer at 3 GHz clock and 100 MHz input.

is a 100 MHz input; and the last two traces are the inverted outputs of the first and second OR gates, respectively.

5.5 High-Speed Test Setup

Figure 5.31 shows the simplified block diagram of the test setup we have used for data acquisition at multi-gigahertz clock and input signals. The HP synthesized signal generator provides sinusoidal clock signals up to 18.6 GHz. To obtain multi-phase clocks, the output from the generator is split into four identical signals using power splitters. Typically, three of these split signals are used as the clocks and the fourth one is used to trigger measurement equipment. The bias-T's provide dc bias for each of the clock signals, and the phase shifters are used to achieve appropriate phase shifts. For example, a relative phase shift of 120 degrees is required for each of the three clocks in a three-phase clock scheme. Lengths of all connections for the three-phase power are carefully matched so that the 120-degree relationship is maintained at the on-chip circuits.

Another signal generator is used to provide the input signal for the circuit under test. In order to display the signals on a sampling scope, it is critical that the input signal is phase-locked to the clocks. There are two possible ways to achieve these synchronous signals without an external phase-lock loop. The first and also the simplest is to use the built-in 100 MHz signal available from the back of the clock signal generator. The other is to use another appropriate signal generator that has triggering or phase-lock capability compatible with the clock signal generator. The first method is much simpler. However, the frequency of the input is so small that the jitter becomes excessive and the time required to run testing is unreasonably large, especially for testing with clock signals in

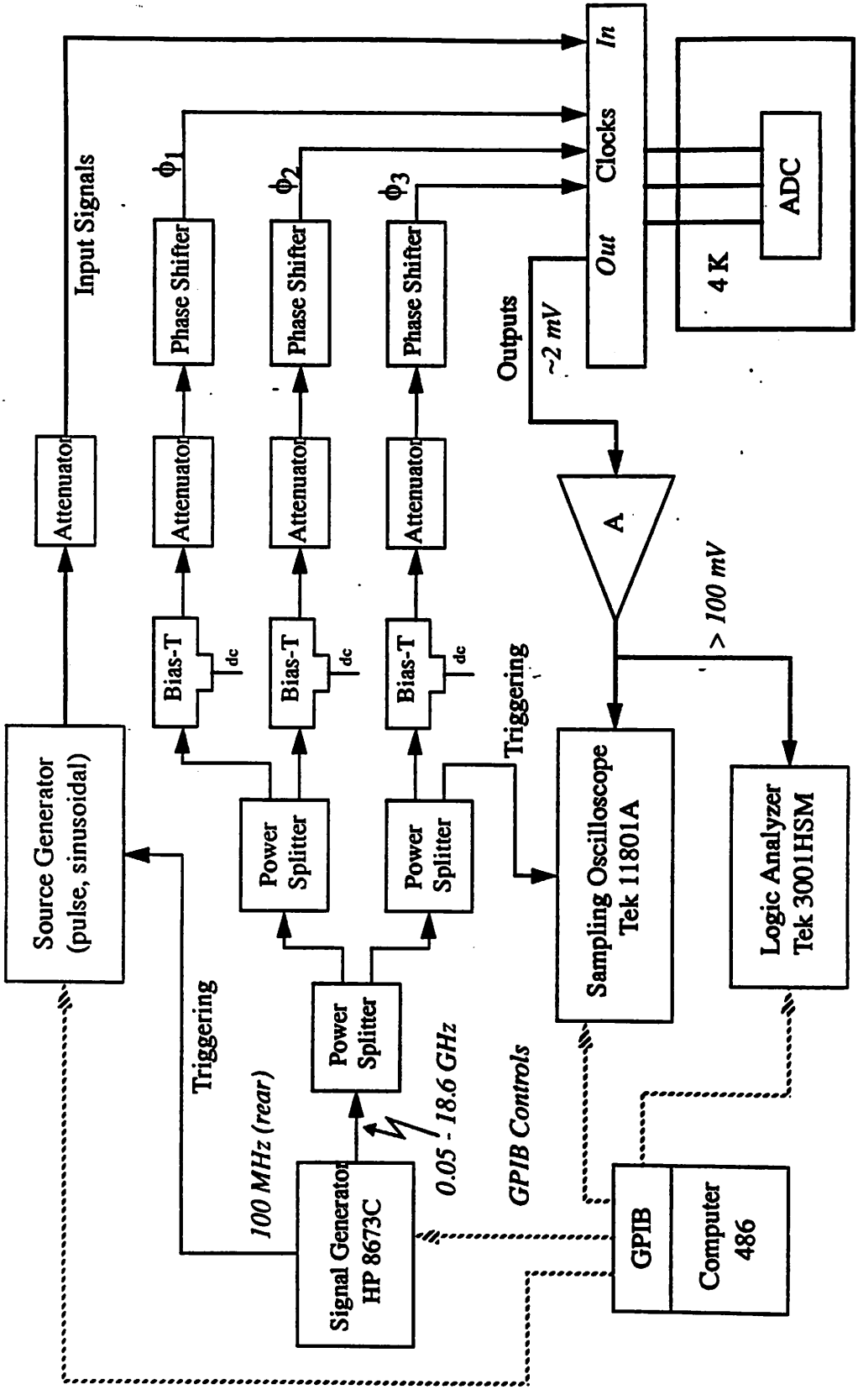


Fig. 5.31 Test setup for data acquisition at multi-gigahertz signals.

the 10 GHz range. The second method is much more attractive but is also much harder to implement; even if it were feasible, it would definitely cost more. Shown in Fig. 5.32 is our test setup to achieve synchronized input and clock signals.

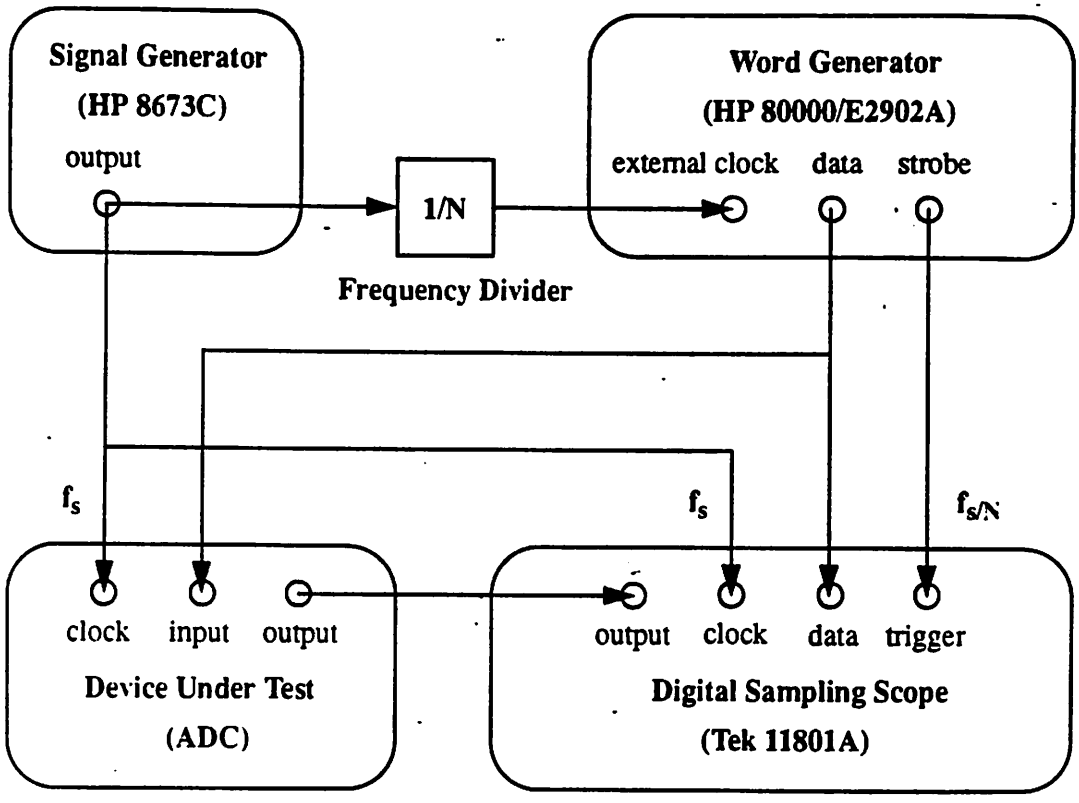


Fig. 5.32 Test setup to obtain synchronous high-speed clock and input signals.

The next challenge in the test setup is how to bring the output signals to the room temperature equipment. The fast switching and small signal level of the output would require an ultra-high-performance amplifier, with very low noise, high gain, and high bandwidth. Many testing techniques are available to avoid such an amplifier.

One way is to use a latch at each of the outputs of the converter and to clock these latches at a much slower rate than the clocks of the converters. Shown in Fig. 5.33 is the

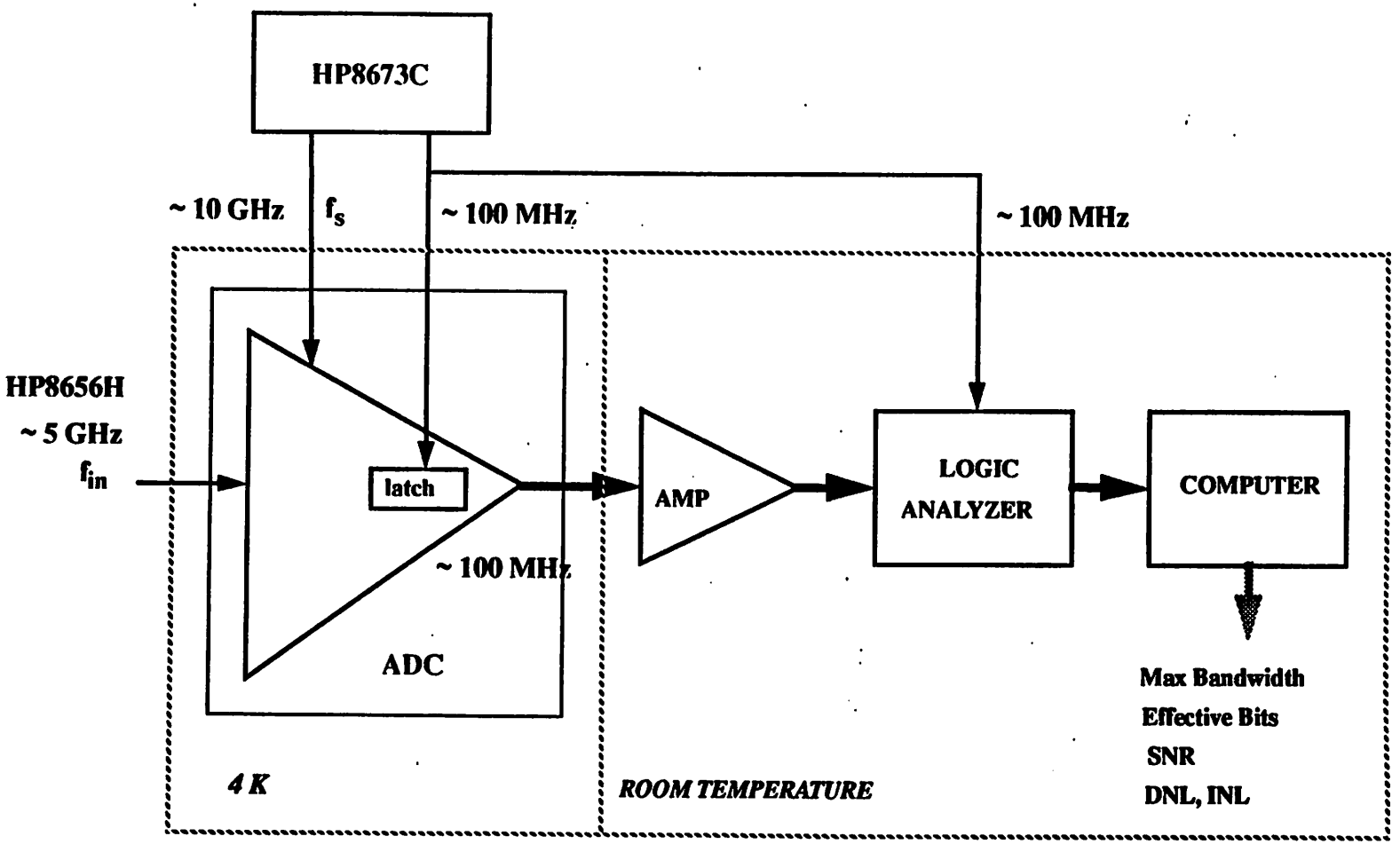


Fig. 5.33 Test setup with latches that are clocked at much slower rate than the converter itself.

test setup in which the outputs of the converter are connected to latches. For a purpose of illustration, the clock frequencies for the converter and the latches are 10 GHz and 100 MHz, respectively. Effectively, the function of the latches is to pick up and pass through one out of 100 samples. As long as the output is repetitive, which is the case for sinusoidal input signals, the output of the latches is an accurate and slow representation of the real output. Latches can be simply implemented with the same comparator configuration used in the converter but clocked at slower rate. However, it is critical to synchronize the clocks for the converter and the latches, in particular when the ratio of the two frequencies is too high. The best way to achieve this is to use a fast signal as a main clock and at the same time to use a fast frequency divider (or frequency scaler) to divide that main clock down to slower clocks.

An envelope or beat-frequency test can be performed to measure the maximum bandwidth and clock frequencies of an ADC, as shown in Fig. 5.34. Normally, according to the Nyquist theorem, the signal bandwidth should be at most half the frequency of the clock signals to avoid aliasing. However, for this testing purpose, we intentionally violate the law and use aliasing to our advantage. The ADC is clocked at a fixed frequency, and the input signal frequency is chosen to be a multiple of the clock frequency plus a small frequency offset. The input and clock signals will beat each other and result in a sinusoidal output at the offset frequency, which is much smaller than the clock frequency.

The main advantage of this test setup is that the clock signals can be fixed and that the input frequency can be continuously increased until the maximum input bandwidth is achieved while the output signal is always the same. The ADC thus can be fully exercised

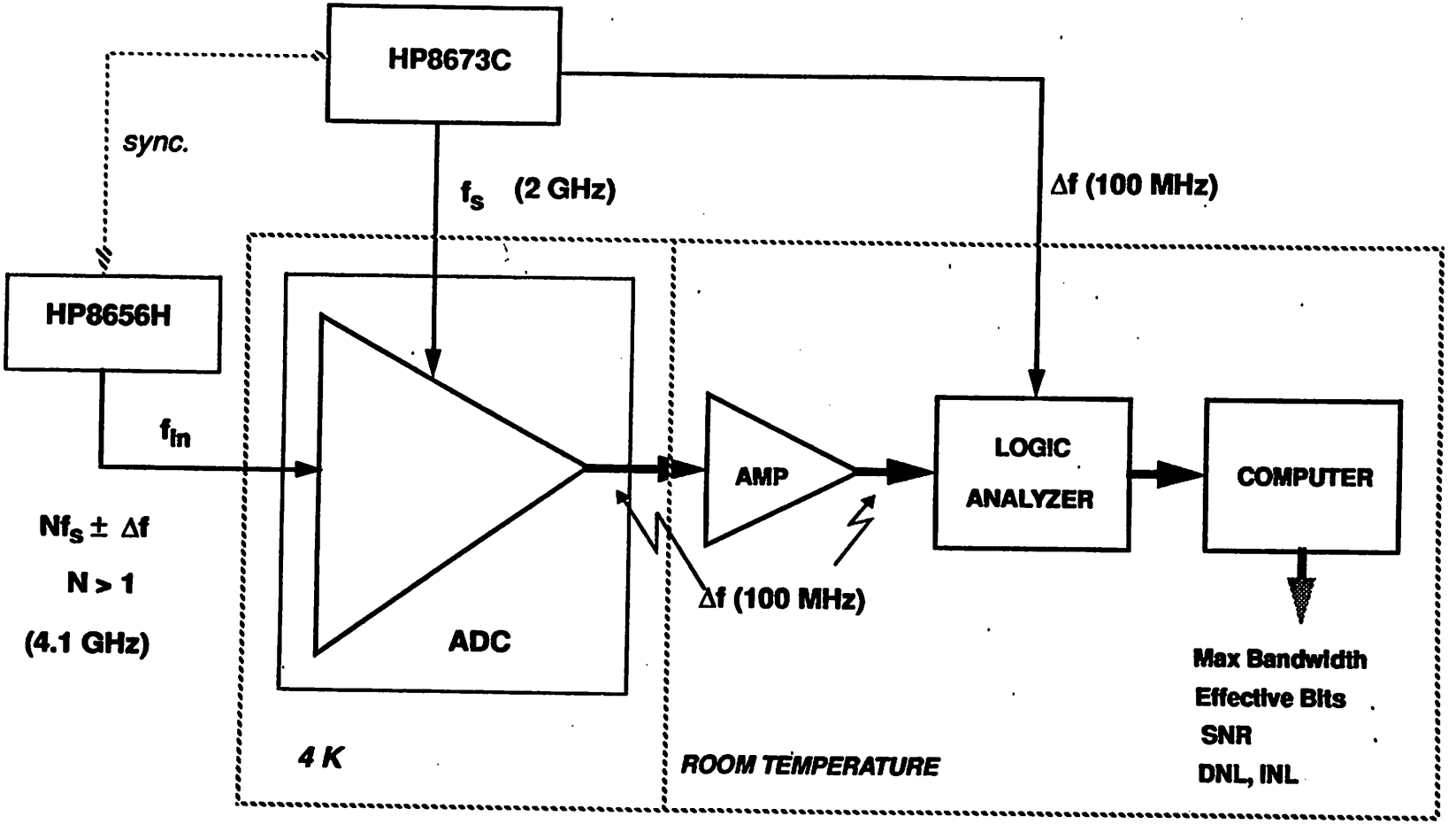


Fig. 5.34 Beat-frequency (sub-sampling) test setup, in which the input frequency is much higher than the clock frequency. The output is the beat frequency of the two.

and tested without a requirement of complicated testing setup and equipment. This test, however, does not reveal any problems associated with clocking at full speeds.

To cover all possible codes and all possible failures, it is desirable to have one or more samples for each possible output code. For M samples per possible code, it is necessary that:

$$\frac{dS_{in}}{dt} = \pi (\Delta f) S_{ref} = \frac{S_{ref}/2}{M2^N} f_S \tag{5.1}$$

where S_{in} is the input signal, S_{ref} is the reference signal, N is the bit resolution and f_s is the clock frequency. It follows that the maximum beat frequency is:

$$\Delta f = \frac{f_S}{M2\pi 2^N} \tag{5.2}$$

5.6 Evaluation of High-Speed ADC Performance

There are many different ways to evaluate the performance of an ADC once their outputs have been acquired. However, the ADCs did not fully work, and the data were not available for evaluation. Appendix B shows how we would have evaluated the ADC performance if the ADCs had worked and the output data had been collected.

5.7 Summary

This chapter presented the experimental results we have obtained for the analog-to-digital converters designed and described in Chapter 4. At low speeds, we have demonstrated the functionalities of many circuits of various levels of complexity. The

largest circuits we have tested successfully included a three-bit quantizer and a three-bit thermometer-to-binary encoder. These are the largest circuits, in terms of size and complexity, that have ever been fabricated and verified to work in our Berkeley laboratory. Larger circuits, including complete three-bit and four-bit ADCs, have also been tested but failed to function. We have been able to show that, due to the wide spread of the junction critical currents, there existed no common operating region for all the gates in these large circuits to work. In particular, the junctions in one-junction sampling SQUIDs have been found to vary a lot from each other because the ground contacts were placed not far enough from the junctions. A redundant scheme has been implemented and tested for four-bit quantizers to improve the chance of getting all fifteen comparators to work simultaneously, and its advantages have been shown to be as expected. Finally, the comparators and the logic gates have been successfully demonstrated at clock frequencies up to 3 GHz, which was limited by our existing test equipment but also was the highest speed ever demonstrated in our laboratory.

Chapter 6

ULTRA-FAST JOSEPHSON LOGIC FAMILY

6.1 Speed Limitation of Latching Logic Gates

It is of much interest to be able to estimate the speed limitation for latching logic gates. Let us consider the simple circuit shown in Fig. 6.1, where I_{sup} is the supply current, R is the equivalent loading resistance, and C is the junction capacitance. At first, a current

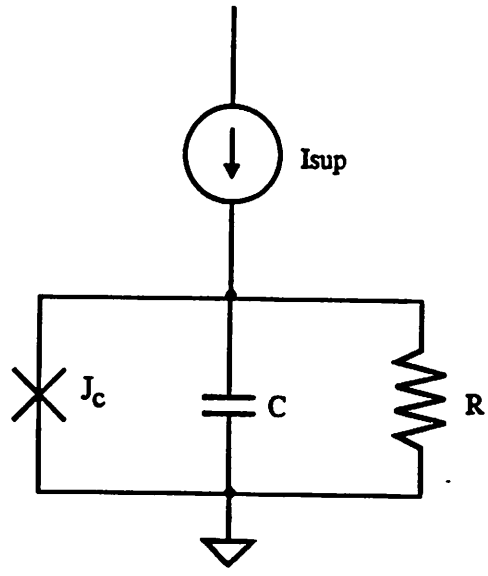


Fig. 6.1 Simple Josephson circuit for resetting calculation.

larger than the junction critical current is applied to switch the junction to the voltage state, and then, the supply current is removed to reset the junction back to the superconducting state. As discussed in previous chapters, during the reset, the voltage across the junction decreases exponentially with a time constant RC. On top of this exponentially decaying signal, there is another component due to the junction's plasma frequency ω_p oscillation, as can be seen from Fig. 3.5 in Chapter 3.

From the figure, after the supply current is removed, the plasma oscillation starts taking place when the voltage across the junction drops below the junction gap voltage by approximately a factor of e^{-2} in two RC time constants. Therefore, it is reasonable to approximate the peak of the plasma oscillation to be $V_p = V_g e^{-2}$ and to assume that the plasma oscillation V_{osc} is of the form

$$V_{osc}(t) = V_p e^{-t/RC} \sin(\omega_p t) = V_g e^{-(t/RC+2)} \sin(\omega_p t) \qquad (6.1)$$

It follows that the plasma oscillation current I_{osc} in the Josephson element can be approximated by

$$I_{osc}(t) = C\frac{dV_{osc}(t)}{dt} + \frac{V_{osc}(t)}{R} = C\omega_p V_p e^{-t/RC} \cos(\omega_p t) \qquad (6.2)$$

For simplification, we make further assumptions that the resetting time is half of the clock period T and that the amplitude of plasma oscillation current in the Josephson element at the end of resetting period should be less than 5% of the critical current I_c, where 5% is arbitrarily chosen. The peak current I_{peak} at the end of resetting period will be given by

$$I_{peak}(T/2) = C\omega_p V_p e^{-T/2RC} \leq 0.05 I_c \tag{6.3}$$

As a result, the minimum time allowed for sufficient plasma oscillation decay is

$$T_{p,min} = -2RC\ln\left[\frac{0.05 I_c}{C\omega_p V_p}\right] = -2RC\ln\left[\frac{0.37\Phi_0}{2\pi V_g}\omega_p\right] \tag{6.4}$$

To get some idea what this result implies, let us substitute some typical parameters. For I_c = 0.2 mA, J_c = 1 kA/cm^2, C_0 = 0.04 pF/μm^2, R = 10 Ω, V_g = 2.6 mV, $\omega_p = 0.87 \times 10^{12}$ rad/s, Eq. (6.4) gives the minimum plasma oscillation decay time $T_{p,min} \approx$ 6.4 RC = 51 ps, which is consistent with simulation results discussed in Section 3.2.2. From the analysis in Section 3.2.2, the turn-on time is $2\omega_p^{-1}$ =1.15 x 2 = 2.3 ps, the rise time is 2.3 RC = 19.1 ps, the fall time is 2 RC = 16.0 ps, and the plasma oscillation decay time is approximately 6.5 RC = 52.0 ps. It follows that the minimum period is 88 ps and the maximum frequency is 11 GHz.

If a critical current density J_c of 5 kA/cm^2 were used and a junction size of 2 μm x 2 μm were available, the RC time constant would be reduced from 8 ps to 1.6 ps; the minimum plasma oscillation decay time, according to Eq. (6.4), would be 10.2 ps, and the minimum clock period would become approximately 20 ps, corresponding to a maximum clock frequency of 50 GHz.

6.2 New Ultra-Fast Logic Family

As described in Chapter 4, a complete logic family has been designed by reconfiguring the comparator building block. However, such a design was not optimal, and

the maximum speed achieved for the logic gates was only about 5 GHz, which is far less than what would be predicted by Eq. (6.4) above. It was mainly because the design specification and the nature of operation of a comparator and a logic gate are not the same. For example, a good comparator would need to have a very small aperture time and to be very sensitive to the input, neither of which is critical to logic gates. Therefore, we have modified the logic family to optimize its performance. The next sections will describe how the logic gates have been modified and illustrate the design of all circuit parameters.

6.2.1 Modification of Logic Gates for Optimal Speed

Figure 6.2 shows the complete circuit schematic for new logic gate with all the modifications. First of all, whenever possible, the junction critical currents are kept as small as the technology allows (as long as they are above the minimum value required for noise) while the critical current density J_c is kept unchanged. The main idea here is to minimize the junction capacitance and the supply to improve both the speed and the power consumption of the converter. It is important to emphasize that merely increasing the current density J_c without reducing either the minimum junction size (due to the limitation of lithography) or the loading resistor would not help speed up the circuit and would only increase the power consumption.

As trade-off for speed by minimizing the junction critical current, the signal-to-noise ratio gets smaller, the current available at the output becomes less, and the process variations, in particular to the spread in junction critical current, become larger. The inductance of the one-junction SQUID loop can be increased to keep its β_L the same. In doing so, the damping resistor of the SQUID can be much larger, thermal noise gets

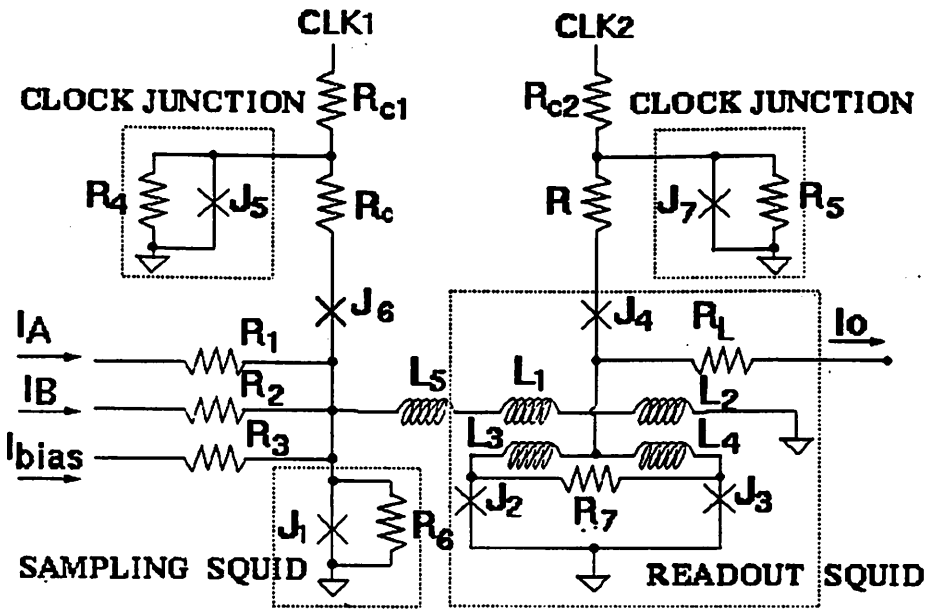


Fig. 6.2 Schematic diagram for the new ultra-fast logic gate.

smaller, and the signal-to-noise ratio would remain unchanged. The speed may not be improved in this case, but the power consumption would definitely be reduced.

Secondly, since a logic gate does not require a short aperture time and thus does not need a pulser at the input, the pulser circuit at the input is replaced by a clock-shaping junction J_5. This replacement not only simplifies the design and decreases the gate area but also helps increase the circuit margins.

Finally, simulations have shown that the pipelined logic gates stop working at very high frequency because the overlapping between adjacent clocks gets smaller as the clock frequency increases. As a result, by the time the clock for any stage is asserted, a high

output from the previous stage may have already fallen to such a low level that it is read in as a low signal. To provide more overlapping between adjacent clocks and therefore to achieve better margins at high frequencies, a four-phase clock scheme, wherein the clocks are 90 degrees out of phase from each other has been used in place of the original three-phase scheme.

Simulations have verified that, with all the circuit modifications mentioned above, the new logic gates can function correctly at a clock frequency up to 12.5 GHz, which matches closely to the result predicted from Eq. (6.4). For illustration, shown in Fig. 6.3 are the simulation results for a three-NAND gates, two driving another. The circuit was chosen to include typical loading and fanout, and all the outputs are delayed one full clock cycle relatively to their inputs due to the pipelining latency.

6.2.2 Step-By-Step Design of Circuit Parameters

The following is a step-by-step procedure to design the circuit parameters for the new logic gates using a process with a critical current density J_c of 1 kA/cm^2, a junction capacitance per unit area C_0 of 38 fF/μm^2, and a reliable minimum junction size of 3.2 x 3.2 μm^2.

The one-junction sampling SQUID shown in Fig. 6.2 can be designed by first assuming the junction critical current of I_{c1} = 250 μA which corresponds to a junction capacitance C = 0.95 pF. To achieve a β_L of 2π, the total SQUID effective inductance L_{eff} should be:

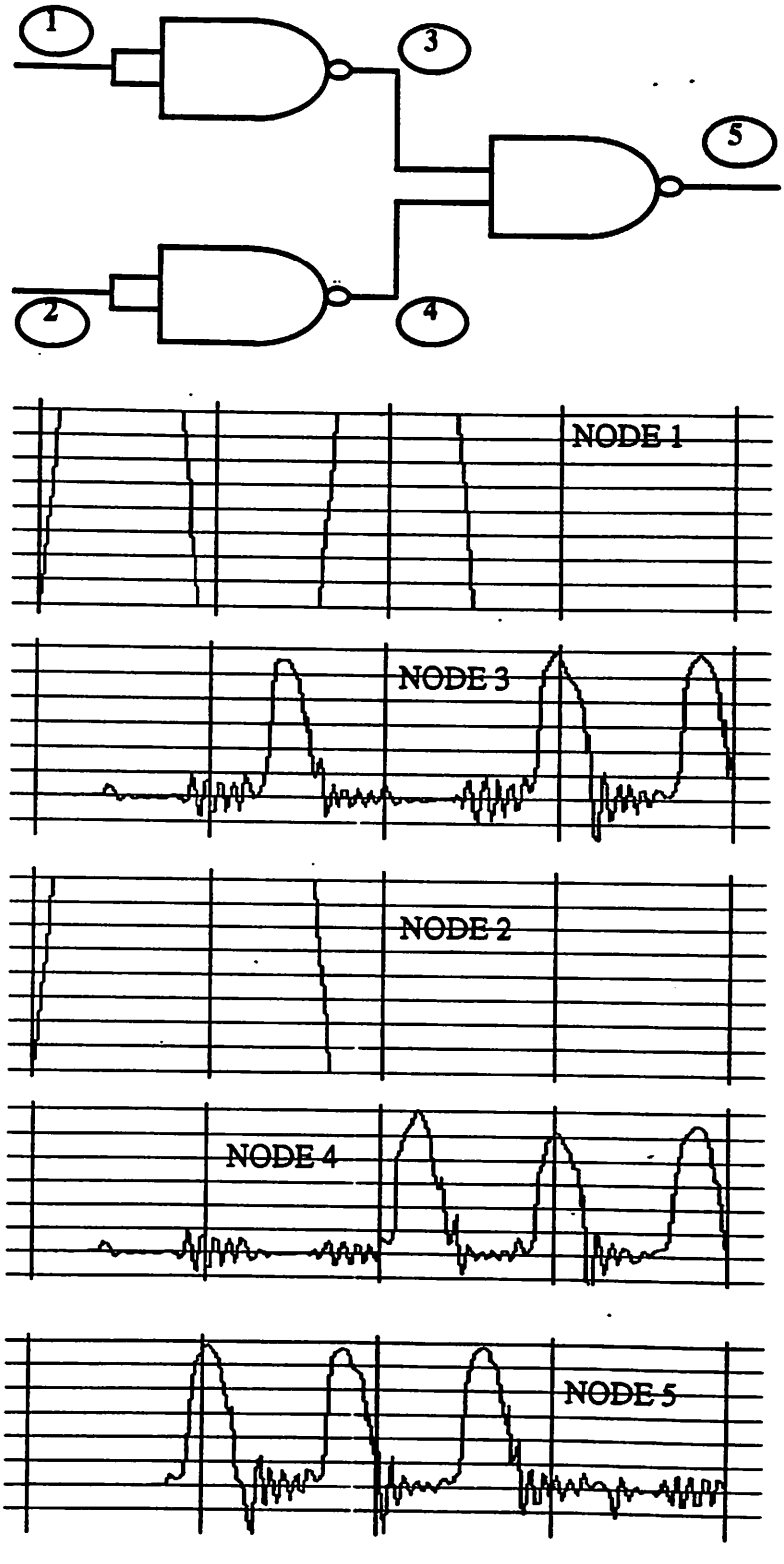


Fig. 6.3 Simulated circuit and result for new logic gates at 12.5 GHz clock.

$$L_{eff} = \frac{\Phi_0}{2\pi I_c}\beta_L = \frac{\Phi_0}{I_c} = 8.28\text{pH} \tag{6.5}$$

and the damping resistor R_6 needs to be:

$$R_6 = \frac{1}{2}\sqrt{\frac{L}{C}} = 1.48 \tag{6.6}$$

Using Eqs. (3.13)-(3.18), the threshold current I_{th} of the one-junction SQUID is found to be 316 μA, at which the output current through the inductor I_B is 265 μA.

Since the output current of the readout SQUID is limited to approximately 130 μA, the high input signal can be assumed to be ΔI = 130/2 = 65 μA. Consequently, for the best margin, the edge-triggering junction J_6 should be designed to have a critical current of

$$I_{c6} = I_{th} - \frac{\Delta I}{2} = 283\,\mu\text{A} \tag{6.7}$$

For a overdrive factor of 2.5, $I_{clk1} = 2.5 \times I_{c6} = 700$ μA, and the bias resistor R_c should be 3.5 Ω. It may be necessary to feed the clock junction J_5 with both ac and dc sources to minimize the problem with punchthrough. Also, the power consumption can be reduced further by choosing a smaller clock-overdrive factor.

With a minimum reliable junction size of 3.2 x 3.2 μm^2, the critical current of the two-junction SQUID is 205 μA, and each junction capacitance is 0.39 pH. From above, the two-junction SQUID will be driven by a control current of 265 μA from the one-junction SQUID. As a result, the period of the threshold curve p must be 265 x 2 = 530 μA, and the mutual inductance M must be:

$$M = \frac{\Phi_0}{p} = 3.9\text{pH} \tag{6.8}$$

For our particular design, the ratio L/M was found experimentally to be 1.16. It follows that the loop inductance $L_3 = L_4 = 1.16 \times M = 4.53$ pH, which corresponds to an β_L of 1.4, a depth of modulation DOM of 71.5%, and the minimum voltage-state gate current $I_{gmin} = 2 \times I_c \times (1\text{-DOM}) = 58\ \mu A$. For an optimal design, the critical current of the single edge-triggering junction I_{c4} is chosen to be:

$$I_{c4} = \frac{2I_c + I_{gmin}}{2} = 132\mu A \tag{6.9}$$

Since the small inductance L_J of each junction is given by:

$$L_J = \frac{\Phi_0}{2\pi I_c \cos\phi} = 3.3\text{pH} \tag{6.10}$$

the SQUID damping resistor R_7 should be:

$$R_7 = \frac{1}{4}\sqrt{\frac{L + L_J}{C}} = 1.11\Omega \tag{6.11}$$

Similarly to the clock junction for the sampling SQUID, an overdrive factor of 2.5 is chosen, and the clock current I_{clk2} for the two-junction SQUID should be $2.5 \times I_{c4} = 330\ \mu A$. Including the dc offset to reduce the punchthrough probability, the input to the clock junction J_7 should be $165 + 330 \sin \omega t$. The bias resistor R would become 6 Ω.

The inductance of the control line L_1 and L_2 can be calculated by noticing that the effective inductance L_{eff} for the one-junction sampling SQUID is composed of two

components. The first is the parasitic wiring inductance L_5, which is approximately 1 pH, and the second is the effective inductance $L_{s,eff}$ of the control line of the two-junction SQUID with loading, which is given by:

$$L_{s,eff} = L_1 - \frac{M^2}{L_3 + 2L_J} \tag{6.12}$$

It follows that:

$$L_1 = L_2 = L_{s,eff} + \frac{M^2}{L_3 + 2L_J} = L_{eff} - L_p + \frac{M^2}{L_3 + 2L_J} = 8.64\text{pH} \tag{6.13}$$

6.2.3 Optimization of Circuit Parameters

The complete design of most circuit parameters for the comparator and the logic gates can be found from Fang's thesis [14]. The parameters have been designed and optimized by extensive simulations with JSIM. In choosing the parameters, there are some conditions that need to be observed and satisfied for the circuit to work properly. Fang described how to choose the parameters for the junction critical currents and the inductors but not the constraints that should be considered in the design of many critical resistors.

As an example, here we will explain how the bias resistor R_c and the loading resistor R_L were chosen. To optimize these resistor values, we consider the case when the two-junction readout SQUID is in the voltage state. The equivalent circuit for the readout stage is shown in Fig. 6.4. As long as the SQUID switches but stays in the subgap region, the current through the SQUID will be negligibly small. Therefore, the bias current I_{clk} through the bias resistor R_c can be found to be:

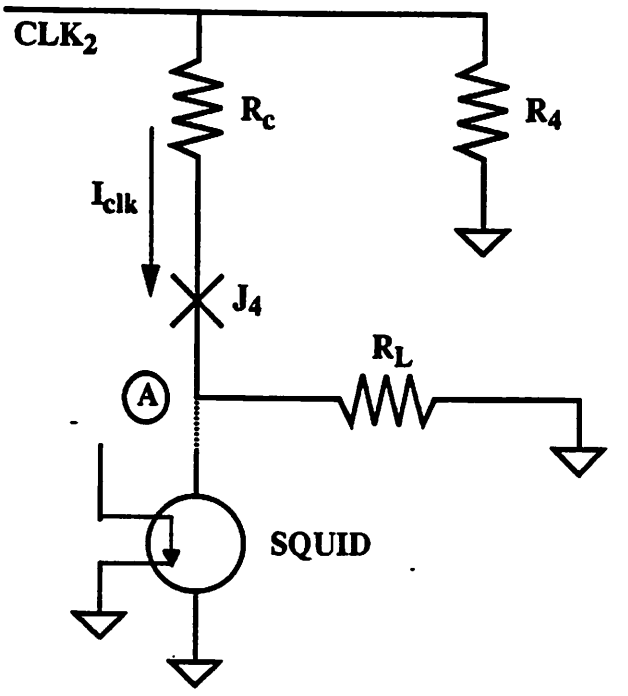


Fig. 6.4 Equivalent circuit of the logic gate when the readout SQUID switches.

$$I_{clk} = \frac{V_g}{R_c + R_L} < I_{c4} \tag{6.14}$$

This clock current needs to be smaller than the critical current of the junction J_4, or else the junction J_4 would also switch and the output current would drop significantly. Another consideration in designing the gate is that the output voltage at node A, given by

$$V_A = \frac{V_g R_L}{R_c + R_L} \tag{6.15}$$

should be smaller than the junction gap voltage to ensure that very little quasiparticle current flows through the SQUID so that substantial current is available at the output to drive the next stage.

The circuit margins can be improved by redesigning the edge-triggering junction J_4. Ideally, the critical current of J_4, I_{c4}, should be chosen to be half-way between the maximum critical current $I_{g,max}$ and the minimum critical current $I_{g,min}$ of the two-junction SQUID, as indicated in Fig. 6.5. As normally would be done, the maximum

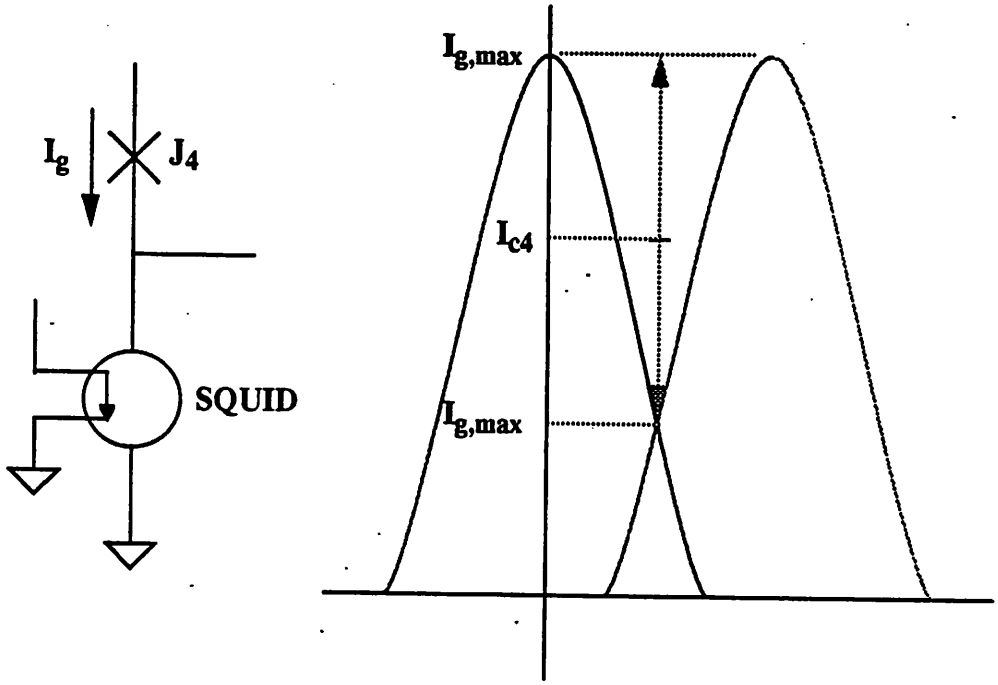


Fig. 6.5 Edge-triggering circuit and the ideal choice for critical current of the junction J_4.

critical current $I_{g,max}$ is the sum of the critical currents of the two SQUID junctions. However, this is no longer valid for high-speed clock signals. The reason is that as the clock current I_g is increased, there is a small voltage developed across the SQUID, which inevitably results in a current flowing through the junction capacitor and any other parasitic capacitance connected to the SQUID output. Effectively, this parasitic current adds to the SQUID's total critical current and increases the maximum critical current

$I_{g,max}$. The effect would be less prominent if the total capacitance and the slew rate of the clock signal are reduced. Nevertheless, it is more desirable is to increase the critical current of the junction J_4 to compensate for the parasitic current. For the same reason, inverting logic gates can achieve the best margins if the critical current of the single junction J_4 is designed to be smaller than the typical 50% value to account for the extra current that flows through the junction and parasitic wiring capacitance. It follows that the designs for a noninverting gate and its inverting version should be somewhat different, mainly in the critical current of the single junction J_4.

6.3 Testing The Ultra-Fast Logic Family

Conventionally, logic gates are tested by applying input signals with different patterns to the gates and clocking the gates at higher and higher frequencies until the gates fail to work. However, this method doesn't work well at very high frequencies, mainly because the clock and the input signals need to be phase locked to each other and synchronizing two signals in the frequency range of 10 GHz is quite challenging, if not impossible. To be able to test the logic gates at their highest possible speeds without the problem of synchronization, we have used the logic gates to build pseudo-random bit sequence generator.

6.3.1 Overview of Pseudo-Random Bit Sequence Generator

As shown in Fig. 6.6, an m-bit pseudo-random bit sequence generator (PSBSG) consists of an m-bit shift register and a feedback network to generate a sequence that looks random but is actually deterministic. Typically, the feedback network is an exclusive-OR

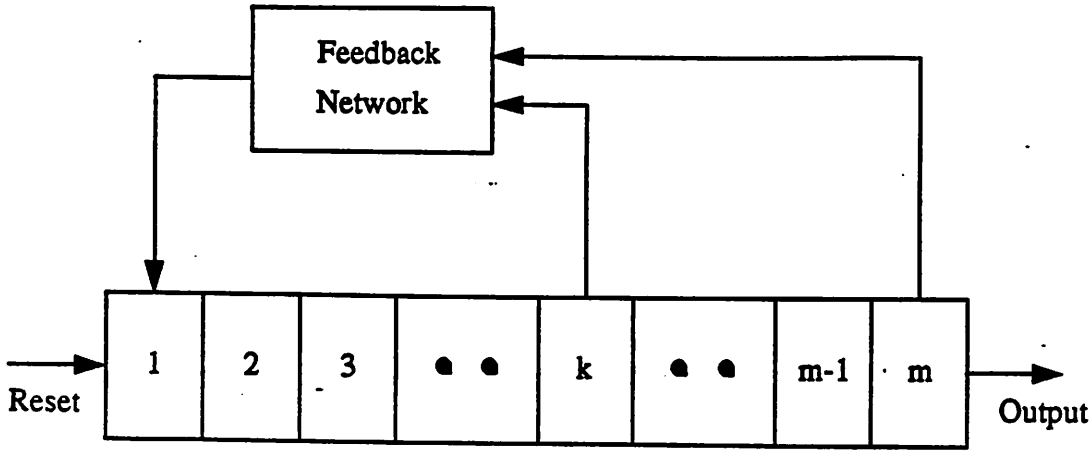


Fig. 6.6 Block diagram for a pseudo-random bit sequence generator.

gate with its inputs being two or more outputs of the shift register stages and its output being fed back to the input of the first stage. In this particular diagram, the inputs of the feedback network are taken from the output of the PRBSG and the k^{th} stage. The actual output sequence depends on the configuration of the feedback network and the initial state of the shift register. The outputs that are used as the inputs of the XOR feedback gate can be arbitrarily chosen. However, for a given number of stages of the shift register m, there are only few ways to connect the feedback configuration to achieve a sequence with maximum length 2^m -1, the so-called maximum-length linear sequence. Unlike any other nonmaximum-length generator in which the output sequence depends on the initial state of the shift register, a maximum-length sequence generator always generates the same output sequence. Only the phase of the output changes with the initial conditions.

Feedback connections required to achieve a maximum-length linear sequence using an m-bit shift register for m being any integer from 1 to 22 are tabulated in [47] and [48]. For reference, Table 6.1 shows the feedback connections for the first 10 values of m.

Table 6.1 Feedback connections to achieve an m-bit maximum-length linear sequence.

m	Feedback Function
1	a_1
2	$a_1 \oplus a_2$
3	$a_2 \oplus a_3$
4	$a_3 \oplus a_4$
5	$a_3 \oplus a_5$
6	$a_5 \oplus a_6$
7	$a_6 \oplus a_7$
8	$a_2 \oplus a_3 \oplus a_4 \oplus a_8$
9	$a_5 \oplus a_9$
10	$a_7 \oplus a_{10}$

6.3.2 Design of a Pseudo-Random Bit Sequence Generator

A pseudo-random bit sequence generator (PRBSG) has been built using the ultra-fast logic gates described above. Two of such PRBSGs are then connected to an XOR gate for bit-error rate (BER) measurement. Typically, a reset signal is connected at

the input of each PRBSG to ensure that the two PRBSGs have the same initial conditions and thus have exactly the same output sequence. However, if the two reset signals are generated separately off-chip, it is possible that they are skewed from each other. If the skew is large enough, the measurement at the output of the XOR gate for bit-error rate will become meaningless. Apparently, the problem is more severe for very high speed clocks, in which case a very small skew of the reset signals can result in two sequences completely out of phase.

One obvious solution is to generate only one reset signal on-chip and split it into two balanced signals for the reset signals. As an alternative, it is possible to delay one reset signal with respect to the other until the two output sequences appear to be the same. Even if there is no delay for the two reset signals, their slew rates can be so different that a fast enough clock will sample them at different levels. It would also help then to make sure that the reset signals have the amplitude and the rise time small enough that, in the presence of different slew rates and fast clocks, the resulting skew would not affect the output sequence. In our particular design, an inverter is inserted in the forward path of each PRBSG to ensure not only a self-triggering function but also a nonzero output sequence. This design, as described below, provides two identical initial conditions without the need of resetting and therefore results in two identical output sequences for bit-error-rate measurement.

The block diagram of the pseudo-random bit sequence generator (PRBSG) for a three-phase clock scheme is shown in Fig. 6.7. The number on each gate denotes its associated clock phases. The two-input XOR gates were implemented directly using two

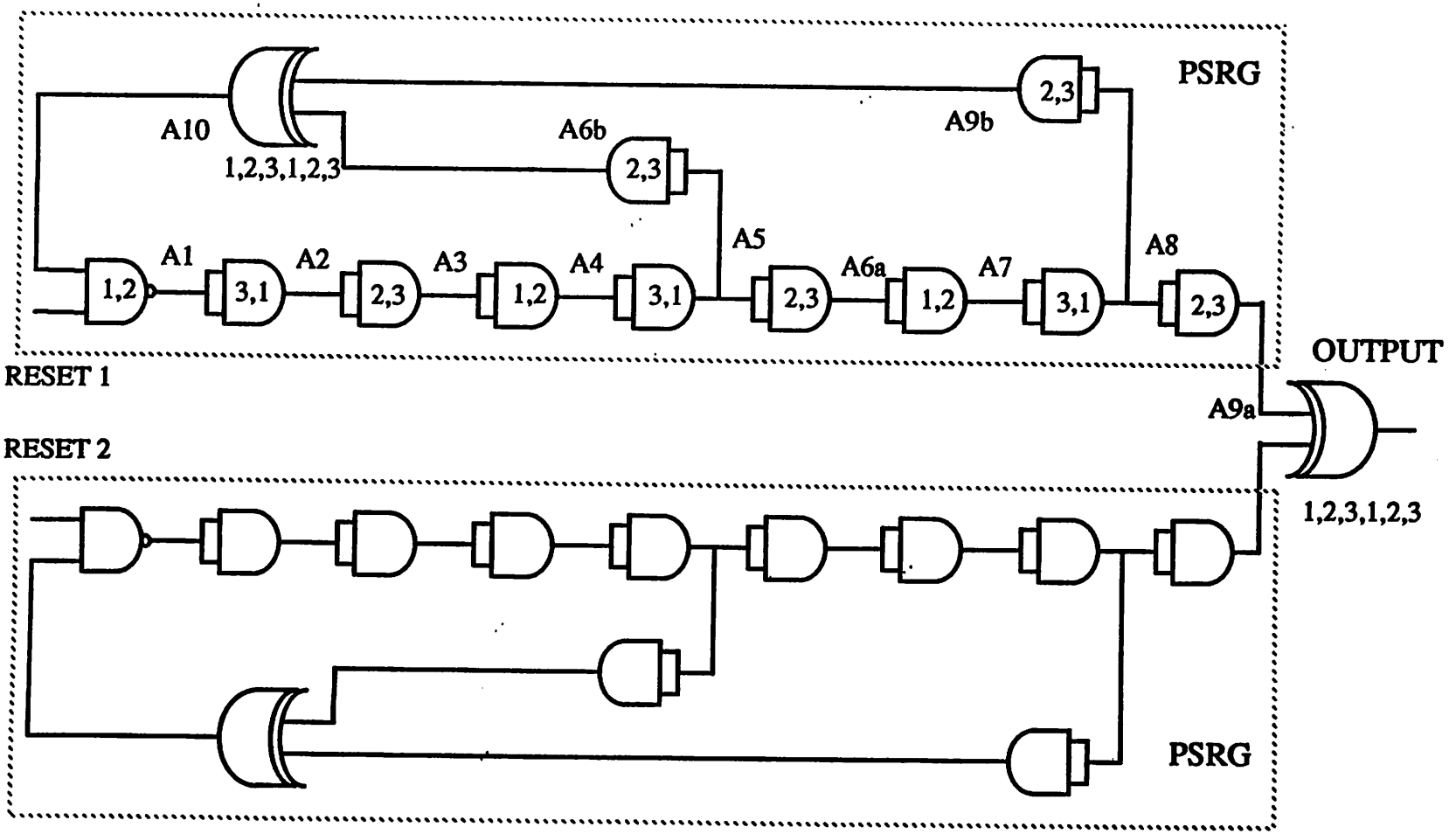


Fig. 6.7 Block diagram of the pseudo-random bit-sequence generator with *three-phase clocks*. Shown also is a second PRBSG and an XOR gate used to verify the correct operation of the PRBSG.

buffers, two inverters and three NAND gates. Due to the latching nature of superconducting circuits, all the gates in the two PRBSGs will be reset into their superconducting states and all output nodes should be zero right before the clocks are asserted. As soon as the second phase clock goes high, the outputs of the first stages of each PRBSG should become high whereas all other outputs remain in zero stage. As a result, the same initial conditions is guaranteed for both PRBSGs. Table 6.2 shows the output patterns for all stages of the PRBSG, where a transition takes place *every two clock phases*. The feedback connections are made from the outputs A_6 and A_9, and the output A_{10} is fed back to the input of the very first gate. Note that, as exemplified by the first entry from the top and the third entry from the bottom of the table, the PRBSG can never get stuck in all-zero state with the presence of an inverter in the loop. Simulation results for the output sequence A_9 shown in Fig. 6.8 verifies the correct operation of the PRBSG at a clock frequency of 10 GHz.

Although a two-input XOR gate can be implemented using a two-junction SQUID with two control lines and applying the two inputs in opposite directions, such a design has been found to be very sensitive to the input timing. To ensure that the entire circuit operation is not limited by such a problem, we choose to use conventional method and build up the two-input XOR gates from basic buffers, inverters, and NAND gates. This design choice, however, as denoted in the block diagram in Fig. 6.7, results in an XOR gate with a latency of two full clock cycles, which is three times of that required for a single stage in the forward loop. As a consequence, the feedback connections shown in Table 6.1 to achieve a maximum-length sequence are no longer applicable, and the output

Table 6.2 The output patterns for all stages in the PRBSG shown in Fig. 6.6.

A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0
1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	0	0	0
1	1	1	1	1	1	1	1	0	0
1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	1	1	1	1	0
1	1	0	0	0	1	1	1	1	0
1	1	1	0	0	0	1	1	1	0
1	1	1	1	0	0	0	1	1	0
1	1	1	1	1	0	0	0	1	0
1	1	1	1	1	1	0	0	0	1
0	1	1	1	1	1	1	0	0	1
0	0	1	1	1	1	1	1	0	1
0	0	0	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	1
0	0	0	0	0	1	1	1	1	1

A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}
0	0	0	0	0	0	1	1	1	0
1	0	0	0	0	0	0	1	1	0
1	1	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	1
0	1	1	1	0	0	0	0	0	1
0	0	1	1	1	0	0	0	0	1
0	0	0	1	1	1	0	0	0	0
1	0	0	0	1	1	1	0	0	0
1	1	0	0	0	1	1	1	0	0
1	1	1	0	0	0	1	1	1	1
0	1	1	1	0	0	0	1	1	1
0	0	1	1	1	0	0	0	1	1
0	0	0	1	1	1	0	0	0	1
0	0	0	0	1	1	1	0	0	1
0	0	0	0	0	1	1	1	0	1
0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0

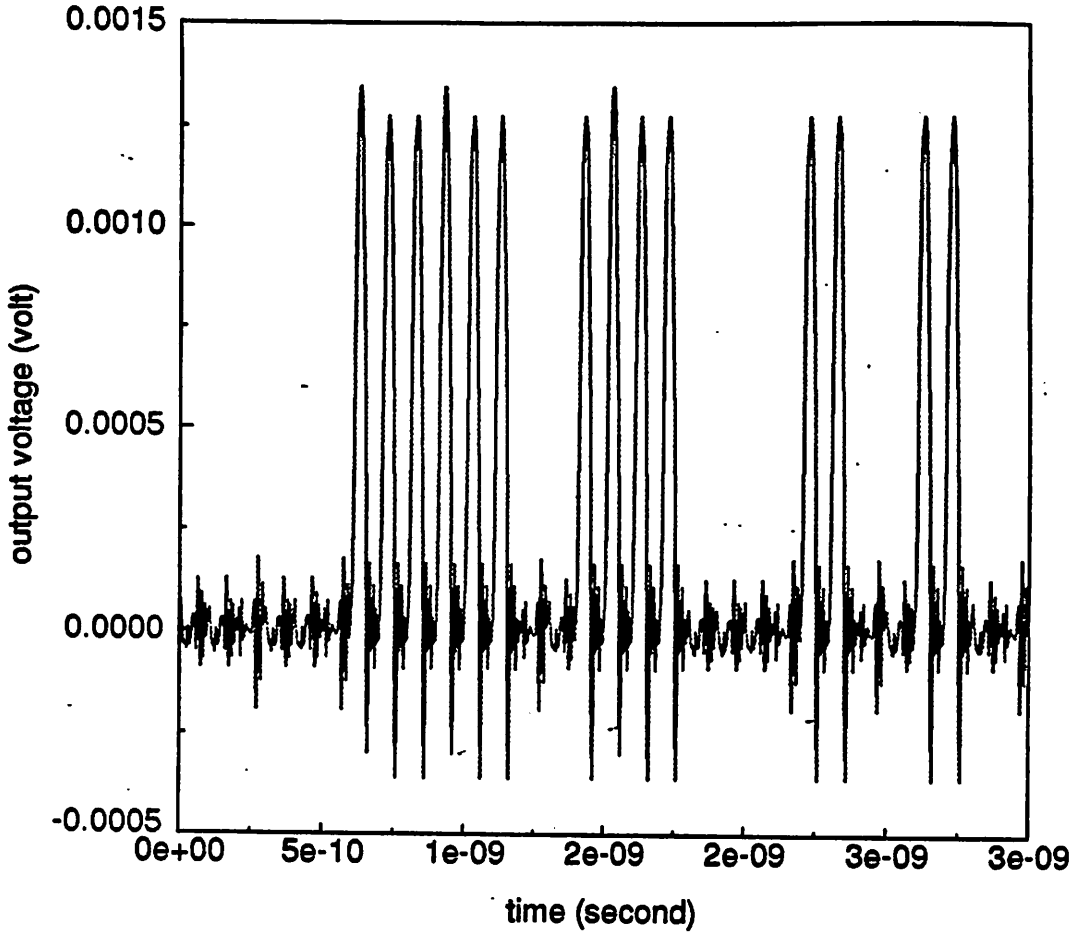


Fig. 6.8 Simulation result of the PRBSG at 10 GHz clock frequency showing one repeated output sequence.

sequence of the PRBSG does not have a maximum length. For the same reason, the PRBSG needs to be redesigned for a four-phase clock scheme, the block diagram of which is shown in Fig. 6.9 for comparison. A gate is removed from the first forward loop, and another gate is added in the second forward loop to keep all the signals aligned appropriately.

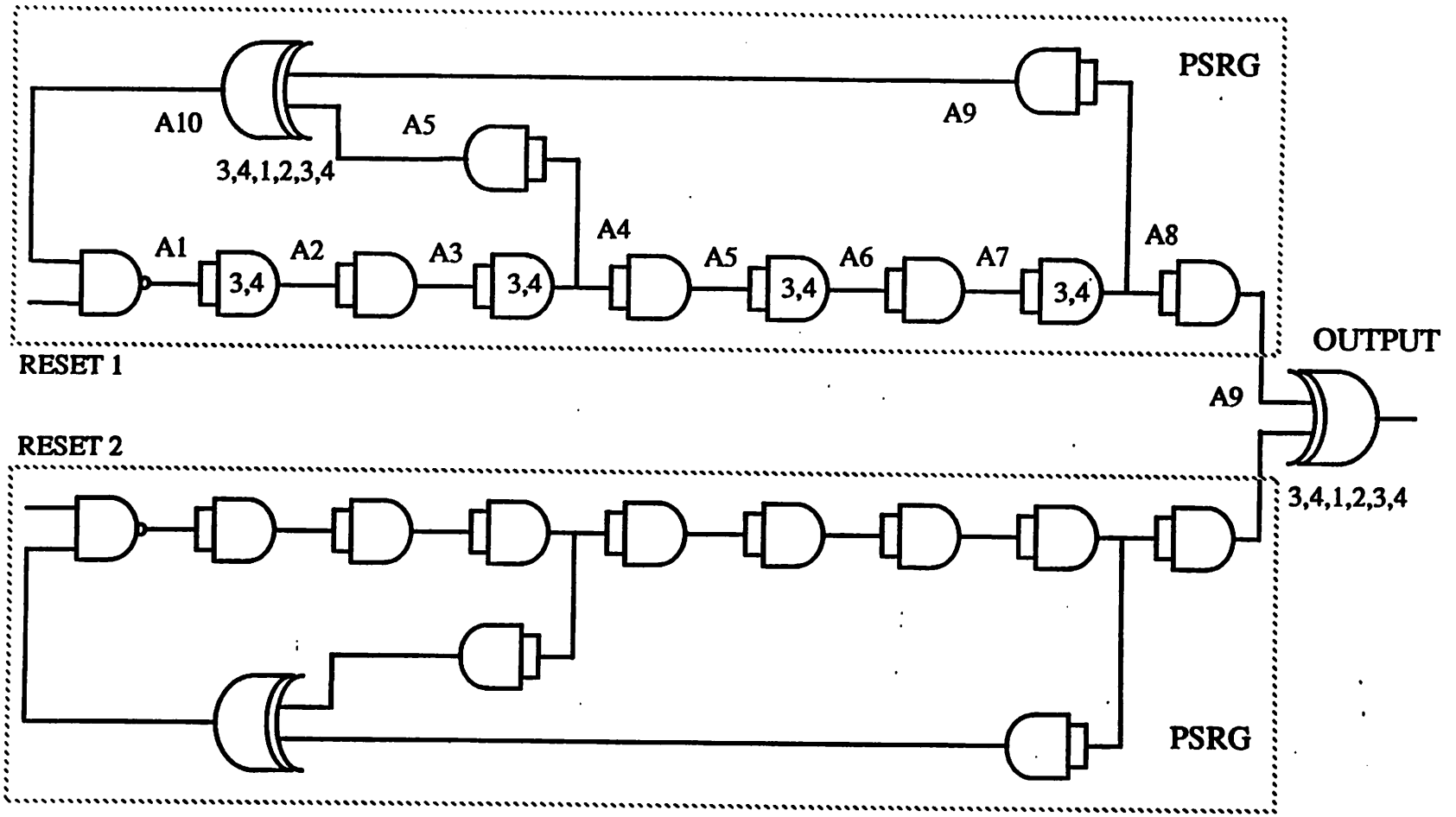


Fig. 6.9 Block diagram of the pseudo-random bit-sequence generator with *a four-phase clock scheme*. Shown also is a second PRBSG and an XOR gate used to verify the correct operation of the PRBSG.

The chip layout of the entire bit sequence generator for a four-phase clock scheme is shown in Fig. 6.10. Each of the two PRBSGs requires 18 gates (126 junctions and 144 resistors), and the whole circuit, including the XOR gate for bit-error-rate measurement, requires a total of 43 gates (301 junctions and 344 resistors). Although, as described

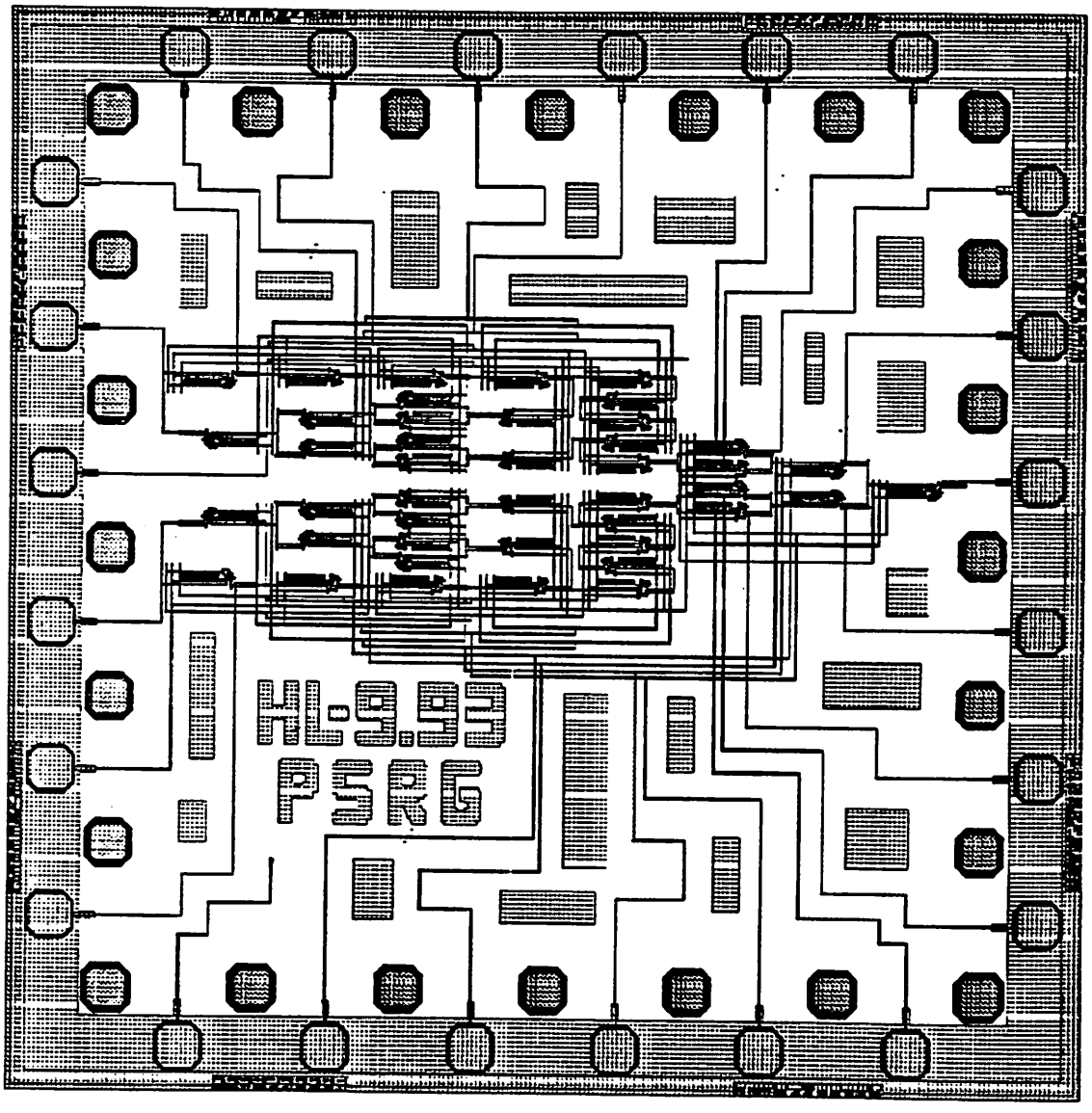


Fig. 6.10 Chip layout of two pseudo-random bit-sequence generators and an XOR gate as shown in Fig. 6.6.

earlier, a resetting signal is not necessary for our design, it is included for each of the two PRBSGs to provide not only testing points but also the flexibility in testing and obtaining different initial conditions for different output sequences.

6.3.3 Testing of a Pseudo-Random Bit Sequence Generator

We have tested the PRBSG and have been able to demonstrate the correct operations of some gates in the forward loops and the XOR gates. Unfortunately, the whole circuit does not seem to fully function. Due to the limited number of I/O pins, there are only very few monitoring points, and we cannot access most of the internal points and thus could not figure out which part of the circuit does not work right. The circuits are fabricated on the same run with the four-bit quantizers and the ADCs described in Sections 5.1.3-5.1.5, it is most likely that this circuit has the same problem with the critical currents varying too much from one junction to another. Since the design of logic gates is based on that of the comparators, we can expect that these logic gates suffer from the same problem that was discussed in full detail in Chapter 5 for the comparators. In the design of the PRBSG, it is critical that *all the gates work* with more or less the same margins. Because of the feedback, tighter margins are imposed on the individual gates. If an error occurs in any gate, it will propagate throughout all other gates. In our case, the entire circuit fails to function because malfunctionality occurs to one of the gates (either in the forward path or feedback loop) or, more likely, because the spread in critical current is too severe that there exists *no common operating regions for all the gates.*

6.4 Summary

This chapter discussed our design of an ultra-fast logic family. Optimal speed can be achieved for the gates not only by minimizing junction capacitance and by replacing the pulser used in the comparator with a clock junction but also by employing a four-phase clock scheme to provide more overlapping between adjacent clock phases. Simulations have shown that, with these modifications, the new logic gates were capable of operating at clock frequencies up to 12.5 GHz. To be able to test these logic gates at their highest possible speeds without a need of synchronizing high-speed clock and input signals, pseudo-random bit sequence generators have been designed, fabricated, and tested. In our design, an inverter was placed in the forward path to ensure that self-triggering function would be obtained and the generator could never get stuck in the all-zero state. Two identical sequence generators were connected to an XOR gate for bit-error-rate measurement. However, for the same problem described in Chapter 5, which was large process variation in junction critical current, all the gates failed to work simultaneously, and this prevented the whole PSBSG from fully functioning.

Chapter 7

HIGH-SPEED DESIGN AND TESTING ISSUES

As the frequency of interest is increased up to 10 GHz, the signal wavelength is reduced to approximately 15 mm, and the lengths of signal paths in the circuits are no longer negligibly small. As a result, distributed models for circuit elements should be used (as opposed to conventional lumped models), most signal lines should be considered as transmission lines, and transmission line theory needs to be applied in designing and laying out the circuits. More importantly, for our superconducting circuits, the high signal level is only a few millivolts, and the switching of Josephson junctions is extremely fast. Every source of noise or parasitic, which could normally be neglected at lower frequencies or in other technologies with much higher signal level, becomes significant and can cause the circuits to malfunction unless treated carefully. This chapter will address the critical factors in designing and testing the converters with multi-gigahertz input bandwidth and clock signals. Specifically, detailed discussion will be given on how we have designed circuits to minimize crosstalk, how we have distributed clock signals to minimize clock skew, and finally how we have set up equipment and what issues we have considered to ensure success in testing at high speeds.

7.1 Cross-Talk

Problems with crosstalk that are present in any fast switching circuit become much more severe and require much more attention in superconducting circuits, for which the switching time is in order of picoseconds and the high voltage level is only few millivolts. Any unwanted signal appearing on a line can generally be considered as crosstalk. Among the main factors that can cause crosstalk are signal reflection due to impedance mismatch, supply variation due to switching of some junctions, mutual inductive or capacitive coupling due to close spacing between any two conductors, and nonzero ground signal level due to inductive ground connections and fast switching.

7.1.1 Signal Reflection Due To Impedance Mismatch

In presence of a discontinuity of characteristic impedances of any two transmission lines, there will be a reflection of signal back to the source which, in general, will superimpose to the transmitted signal and inevitably reduce the circuit margins, and in the worst case prevent the circuit from working. The amounts of reflection and transmission depend on the reflection coefficient ρ, defined as the ratio of the reflected signal to the incident signal, and the transmission coefficient τ, defined as the ratio of the total signal delivered to the second transmission line to the incident signal. For an impedance mismatch between two transmission lines with characteristic impedances of Z_{01} and Z_{02}, the reflection coefficient ρ and the transmission coefficient τ are given by [49]

$$\rho = \frac{Z_{02}-Z_{01}}{Z_{02}+Z_{01}} \tag{7.1}$$

$$\tau = \frac{2Z_{02}}{Z_{02}+Z_{01}} \tag{7.2}$$

More specific and relevant to our circuit is the case shown in Fig. 7.1, where an external source with an internal impedance R_0 is connected to an on-chip circuit through a coaxial cable with a characteristic impedance Z_0. The on-chip circuit consists of a bias

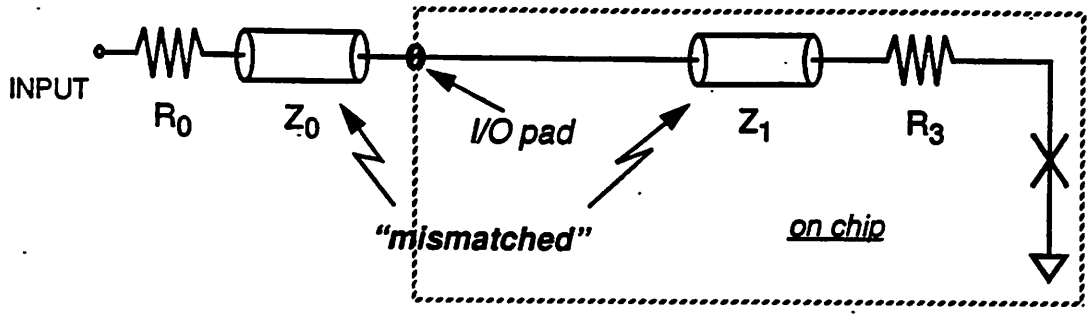


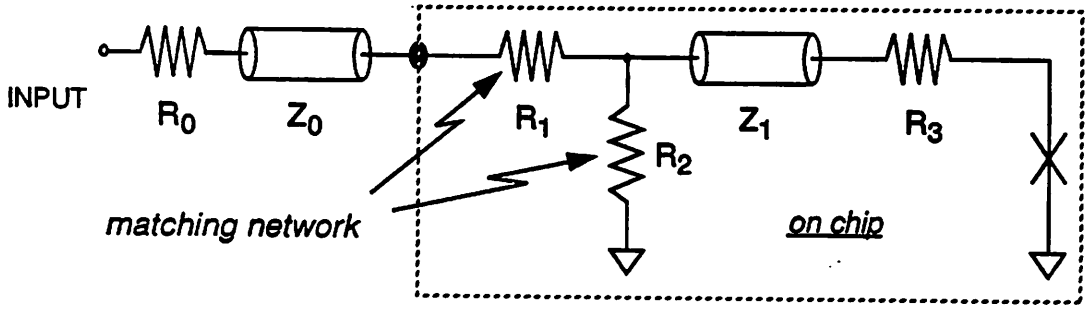
Fig. 7.1 A typical superconducting circuit with an impedance mismatch

resistor R_3 connecting an active device with an I/O pad through a transmission line with characteristic impedance of Z_1. Typically, high-speed signal sources have source impedance R_0 of 50 Ω, external coaxial cables have Z_0 of 50 Ω, on-chip bias resistors R_3 are anywhere from 5 to 20 Ω, and the junctions's impedances are virtually zero before switching. However, on-chip transmission lines, due to limitation of lithography and the required minimum line width, have characteristic impedance Z_1 much less than 50 Ω. This results in a large mismatch of the impedance between the external coaxial cable and the on-chip transmission line and inevitably causes a large reflection of the signal. Unless the

source impedance R_0 matches well with Z_0, the signal would keep bouncing back and forth, which could degrade the circuit performance, especially for nonsinusoidal signals.

The problem with the signal reflection due to impedance mismatch can be largely eliminated by simply inserting a resistive matching network R_1 and R_2 between the two transmission lines as shown in Fig. 7.1. The conditions for matching in both directions and the resulting analytical formulas for R_1 and R_2 are included in the same figure.

It is important to notice that matching does not come free. Since additional signal power is lost through the matching network, it is not always favorable to include the



$$R_1 + (R_2 // Z_1) = Z_0 = R_0$$

$$R_2 // (R_1 + Z_0) = Z_1 = R_3$$

$$R_2 = \left(\frac{Z_0}{Z_0 - Z_1}\right)^{1/2} Z_1$$

$$R_1 = [Z_0 (Z_0 - Z_1)]^{1/2}$$

Fig. 7.2 Circuit in Fig. 7.1 with addition of a resistive network for perfect matching.

network. For external input signals, whose supply power can be increased to compensate for the loss, and for critical circuits that are very sensitive to signal reflection, it may be justifiable to sacrifice the power. However, it may be better to do without a matching network for output signals that are relatively robust to the reflection or that have too small amplitude to afford any additional loss.

We have attempted to replace the on-chip transmission line by a very long resistor connecting all the way from the I/O pad to the circuits. However, this approach introduces few more new problems, including the speed degradation due to the large capacitance of the resistor and the excessive power loss and chip area due to the resistor itself. To solve the problem with the big capacitance, we removed the ground plane underneath the resistor while making sure that the L/R time constant of the resistor is small enough not to affect the original speed. Analysis for coplanar waveguides using conformal transformation was used to calculate characteristic impedance and inductance of such a long resistive structure over a ground hole [50], [51]. This seems to work, but the problems with excessive power consumption and chip area remain. In particular, for signals that need to carry a lot of current, this solution proves to be impractical because the long resistor also has to be wide enough to ensure that it does not overheat and that its power consumption does not exceed the maximum power density allowed for superconducting circuits.

In the future, impedance matching can be improved and achieved without sacrificing additional power loss by replacing the resistive matching network with a superconductive impedance transformer, which can be implemented using an inductive

transformer or an LC band-pass filter. An inductive transformer [52] can achieve moderately wide bandwidth but cannot be used in gigahertz applications because its maximum cutoff frequency is limited to approximately 300 MHz due to the parasitic capacitance between the primary and secondary transformer elements. On the contrary, an LC band-pass filter has narrow bandwidth but can be designed to operate at any given clock frequency within a range of few gigahertz. Such an impedance transformer was proposed and demonstrated successfully at 2.0 GHz at NEC and referred to as superconducting filter-type powering devices (SFPD) [53] [54]. Shown in Fig. 7.1 is an implementation of a three-stage SFPD, where each stage is a pair of inductors and capacitors. A correct set of values for inductors and capacitors needs to be selected and optimized using computer simulations for any given load and operating frequency. It has been found that the more stages the SFPD employs, the broader bandwidth it can achieve, but that three stages is sufficient in most cases.

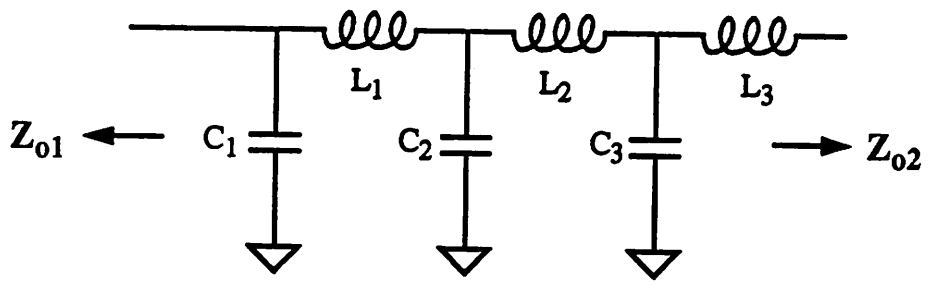


Fig. 7.3 Schematic of a 3-stage superconductive filter-type powering device (SFPD).

7.1.2 Supply Variation Due To Junction Switching

Another common source of crosstalk is likely to be found in large circuits in which many circuits share the same power line and bias of each circuit depends on the switching of the other. Figure 7.4 shows a typical situation where such crosstalk may occur. Clearly,

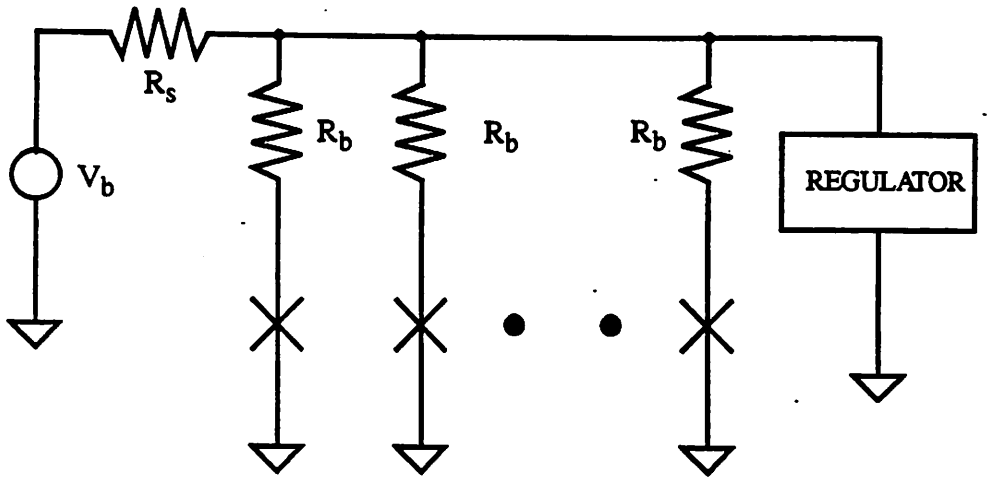


Fig. 7.4 Problem and solution for crosstalk due to junction switching.

without a regulator connected, as any junction switches to the voltage state, its bias current will be diverted to the other branches. The worst case happens when the majority of the junctions switches to the voltage state and only one or few junctions are to remain in the superconducting state. In this case, the total bias current diverted from those switched junctions will be large enough to switch those few that are not supposed to switch and thus will give wrong results.

A straightforward solution we have tried to minimize this type of crosstalk is to increase the bias resistors R_b to improve isolation and to reduce crosstalk among circuit stages. This approach normally requires many large resistors and thus consumes too much power and chip area, but it is simplest and most likely to work.

We have also tried to connect an on-chip regulator to the circuit as shown in the same figure to achieve a voltage source that is independent of the junction switching. A resistive regulator is simply a single resistor to ground whose value is much smaller than the equivalent resistive load of all the circuits. This resistor converts the total input bias current into a voltage source with relatively fixed amplitude and thus helps eliminate the crosstalk. We have found this technique to be more effective than increasing the bias resistors. However, it consumes much more power and chip area because the regulator resistor has to be very wide to be able to sustain high current without overheating.

Alternatively, Josephson junctions with appropriate loading and bias can also be used in place of a very small resistor to provide a fixed voltage source. Either a very large junction or many small junctions in parallel is required for each regulator to provide enough current, but both of these inevitably reduce the circuit yield and take up too much chip area. Worse yet, in most applications, more than a gap voltage and thus a stack of more than one junction may be needed for each regulator. The use of stacks of junctions introduces a new problem because not all the junctions in the stack may switch at the same time due to the process variation of the circuit current. Feedback can be provided by connecting two stacks of junctions in parallel to ensure simultaneous switching of all the

junctions in a stack, but again it would increase the junction count, consume more chip area, and lower the yield.

7.1.3 Mutual Inductive and Capacitive Coupling

As the signal frequencies are increased and as the spacing between signal lines gets smaller, the mutual inductive and capacitive coupling becomes larger, and unwanted signal induced on one signal line in the presence of a signal on the other lines may become significant. Figure 7.5 shows a simple model of mutual inductive and capacitive coupling between two signal lines, M and C_{mu}, respectively, where R_{eq} denotes the total equivalent

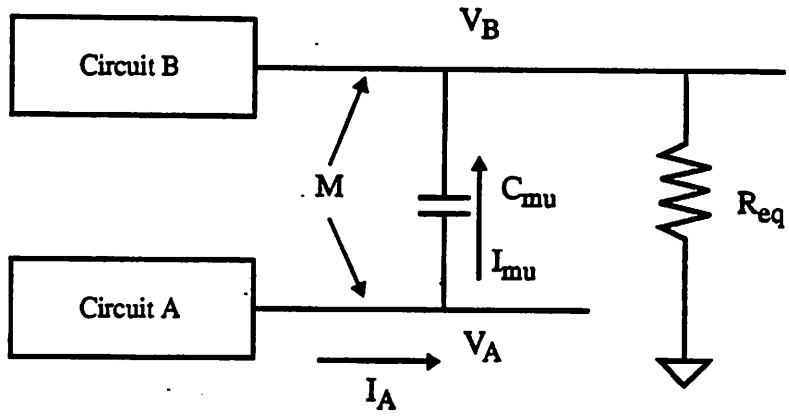


Fig. 7.5 Simple model of crosstalk due to mutual inductive and capacitive coupling.

resistive load of circuit B. If there is any large change in current or voltage on one circuit line, say A, there will be a corresponding change in voltage or current induced on circuit line B.

The crosstalk can be reduced not only by minimizing the mutual inductance and capacitance but also by optimizing the equivalent load and by avoiding switching circuits faster than necessary. Both mutual inductive and capacitive coupling can be reduced by keeping the two signal lines as far as possible from each other. It also helps to avoid having signal lines running parallel to each other for too long, especially for those lines carrying signals with large amplitude or high frequency components. Interleaving ground lines among high-speed signal lines has proved to be very effective in reducing the coupling and crosstalk. The equivalent load on each signal line can also be designed to minimize the crosstalk. If the mutual capacitance C_{mu} dominates, the mutual current I_{mu} is more important, and a smaller R_{eq} is preferred because it results in a smaller voltage noise. If the mutual inductance M dominates, as usually the case for superconducting circuits, coupling voltage V_{mu} is more important, and a large loading resistance R_{eq} should be used to minimize the current noise. Finally, it may be helpful sometimes to purposely decrease the circuit rise time to help minimize the crosstalk, as long as doing so does not affect the overall circuit delay too much.

7.1.4 Ground Noise (Ground Bounce)

As in any fast switching circuits, one of the main sources of noise in our circuits is the ground noise or ground bounce. As indicated in Fig. 7.6, the problem is due to the parasitic inductance of the ground line. Upon any switching, the total current following through the parasitic inductance L_p to the ground will change. If the total current change is fast and large enough, considerable unwanted voltage signal will be developed on the ground line and can interfere with the circuit operation.

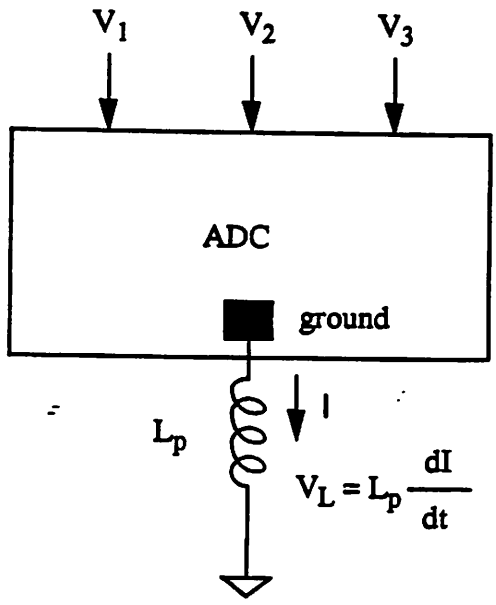


Fig. 7.6 Illustration of how high inductive ground line causes ground bounce.

There are many ways to minimize the ground noise. The parasitic ground inductance L_p can be reduced by using wider and lower-inductance internal ground planes and putting multiple and separate ground wires on smaller packages. Tape-automated bonding (TAB) and flip-chip are among the techniques available that can provide very low parasitic ground inductance. Dedicated and isolated pins may also be necessary for each of the lines that carry high-speed and large-amplitude signals, such as clock lines and output drivers pins.

All techniques mentioned above can only reduce the parasitic ground inductance to reduce the ground noise. To eliminate the power supply ground bounce, we have employed a multiple-phase clock scheme in our designs as shown in Fig. 7.6, where the

three clocks, V_1, V_2, and V_3, are 120 degrees out of phase relative to each other. Mathematically,

$$V_1 = A\sin(\omega t + \theta) \tag{7.3}$$

$$V_2 = A\sin(\omega t + \theta + 120°) \tag{7.4}$$

$$V_3 = A\sin(\omega t + \theta + 240°) \tag{7.5}$$

As long as the clocks have the same equivalent loading R,

$$I(t) = \frac{V_1(t) + V_2(t) + V_3(t)}{R} = 0 \tag{7.6}$$

In other words, the total current flowing into the ground is exactly zero. and therefore no voltage is developed across the parasitic ground inductance L_p. Even when the clocks are dc offset, the total current will remain constant at all time, dI/dt will still be zero, and no voltage noise will be induced; the ground will have no power supply bounce. It is important to notice that although the loads are designed to be the same for all the clock phases, they may vary and be rendered different due to junction switching, in which case Eq. (7.6) becomes invalid and the entire clock scheme is not as effective.

7.2 Clock Distribution

Since the converters are designed to work at gigahertz frequencies, it is difficult to avoid skew among the clocks and between the clock and signal lines. A tree distribution scheme has been used to minimize the skew among the clocks in our designs. A section of such a clock scheme is shown in Fig. 7.7 for illustration. Basically, the clock signal from

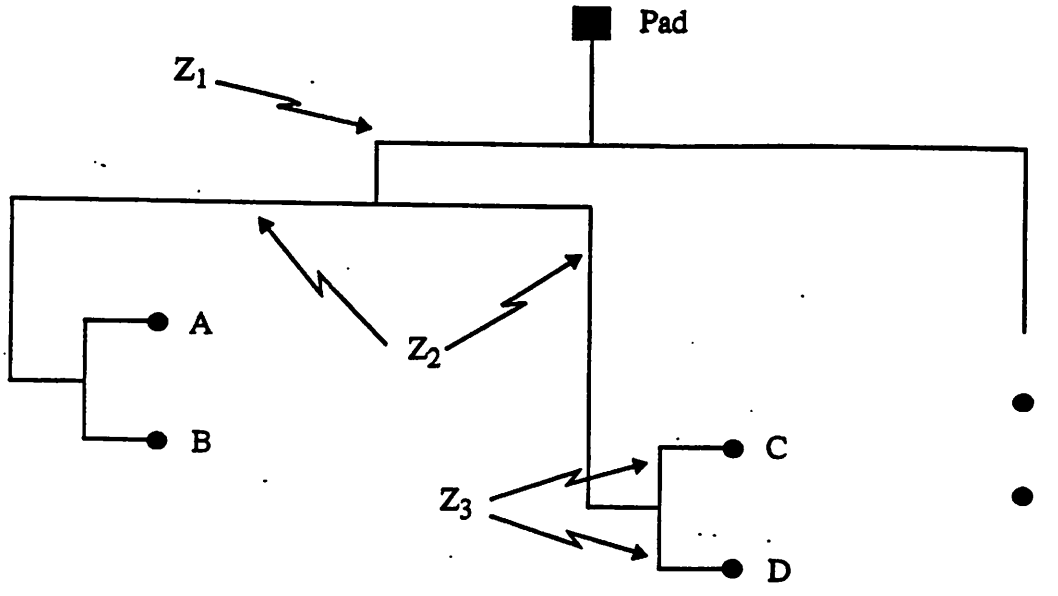


Fig. 7.7 A section of an H-tree clock distribution scheme to minimize skew.

an I/O pad is divided and distributed to the circuit nodes A, B, C, and D, in a H-tree configuration so that the traveling distances from the pad to all the circuit nodes are exactly the same.

In addition to minimizing clock skew, it is also critical to match impedance at every node to avoid reflection. In practice, this matching can be done by increasing the characteristic impedance of every branch in such a way that both equivalent impedance looking into and from each node are the same. In the example shown in Fig. 7.7, it is important to keep $Z_3 = 2Z_2 = 4Z_1$. The characteristic impedance of a microstrip transmission line can be increased by decreasing the line width. However, due to the minimum line width limitation of the process, there is a maximum impedance that can be

realized for a given metal layer, in which case one of the matching networks described earlier in Section 7.1.1 may need to be considered for impedance matching. Alternatively, a nonuniform transmission line tapers, as described in [55], can be used to ensure impedance matching at every node.

7.3 Testing Issues

There are many problems and issues in designing and fabricating superconducting analog-to-digital converters for multi-gigahertz frequencies. However, it is even much more difficult and more challenging to test these converters.

7.3.1 High-Speed Probe

Since the circuit under test (CUT) needs to be cooled down below its critical temperature to work properly, it is necessary to mount the CUT on a probe and to dip the whole probe into a four-feet-high dewar of liquid helium. The challenge then is not only to bring the high-speed signals and clocks from the room temperature electronics through long cables into the dewar but also to bring the high-speed output signals, whose amplitude is as small as two millivolts, from the CUT inside the dewar back out to the room temperature equipment.

We use a probe from American Cryoprobe that has a bandwidth exceeding 10 GHz [19] [56]. Basically, it consists of two parts. The first, the so-called cold head, is a holder on which the CUT is mounted and which is dipped into liquid helium. This head must fit into the existing liquid helium dewar, which has 1.5 inch neck opening, and needs to fit into two concentric high-permeability double magnetic shields, the inner and outer

diameters of which are 1.00 and 1.25 inches, respectively. The rest comprises 24 coaxial cables accessing the chip I/O pins from room temperature. Since twisted-pairs cables suffer from excessive crosstalk at high frequencies, semi-rigid coaxial cable (Uniform Tubes Micro-Coax) were used. This choice provides optimal performance in terms of compactness, frequency response, and electromagnetic shielding properties. A large surrounding stainless steel tube protects the sensitive cables from being damaged during testing and handling.

7.3.2 Flux Trapping

It is well-known that Josephson circuits are very sensitive to external magnetic field. Flux can be easily trapped in a superconducting SQUID loop, in which case the critical current of the SQUID would be reduced. Since this flux trapping is spatially random, it can cause random variations in critical currents and thus cause the circuits to malfunction. The probability of having flux trapping increases with the circuit size. In fact, flux trapping has been found to be *the most critical and likely* problem that prevents Josephson circuits from working correctly.

Extensive care must be taken to minimize the chance of trapping flux. As far as circuit designs are concerned, it is desirable to minimize the size of any superconducting loop in the circuit. Ground holes, normally referred to as moats, can be placed around Josephson circuits to minimize the chance of trapping flux. The idea is that these moats will provide more favorable places for flux to enter and thus can be used to prevent flux from trapping in Josephson circuits [57].

It is not only important to use double high-permeability magnetic shields, but it is also critical to demagnetize the shields before each use. Magnetic shielding will be discussed in the next section, and the design of the degausser to demagnetize the shields will be described in Appendix D. It has been found to be very effective to put the chip inside an RF shielded holder and to RF filter all the signal lines before they go into the chip. However, due to the low cutoff frequency required for the filter, the technique only works at low frequencies.

Once flux is trapped, it can be untrapped by heating up the chip and slowly cooling it down. This has been done by putting a resistor on the copper block on the probe that makes contact to the chip from the back and driving a large current through the resistor. However, since the heat is not directly applied onto the chip, this method is not very effective. We have proposed to use an on-chip resistor to apply heat and to rid of the flux trapped more effectively. Such on-chip resistors have been designed around the chip periphery right next to the pads and have been found experimentally to be effective. This choice of location leads to the center of the chip cooling first and flux should be swept to the edges during cool-down. Disadvantageously, this solution requires a dedication of two I/O pins from the chip to connect the resistor to external supply sources, which is highly undesirable for our existing I/O-limited probe. Practically and effectively, we have warmed up and cooled down the chip by lifting the probe out of the helium dewar.

7.3.3 Magnetic Shielding

In principle, only magnetic fields that are perpendicular to a superconducting loop can cause circulating currents in the loop [58]. There is therefore no need to reduce the

magnetic fields that are parallel to the chips. Magnetic shields with high permeability can be used to attenuate the magnetic fields perpendicular to the chips. Since our chips are mounted perpendicularly to the shield axis, only the field perpendicular to the chips and parallel to the shield axis is of our concern. For an open-ended cylindrical shield, the shielding factor S_t for magnetic field parallel to its axis is given by [59]

$$S_t = \mu \frac{d}{D} \tag{7.7}$$

where μ is the permeability, d is the wall thickness, and D is the diameter of the cylinder.

The shielding factor is increased significantly if more than one shield is used. For two-cylindrical shields (double-shield), the combined shielding factor S_T becomes [59]

$$S_T = S_{t1} + S_{t2} + S_{t1} S_{t2} \left(1 - \frac{A_2}{A_1}\right) \tag{7.8}$$

where S_{t1}, S_{t2}, A_1, A_2 are the shielding factors and the cross-sectional area of the outer shield and the inner shield, respectively. As an example, for Cryoperm-10 two-layer magnetic shield (Vacuumschmelze, Germany), with the individual shielding factors S_{t1} = 2240, S_{t2} = 2592, the inner diameter d_2 = 33 mm, the outer diameter d_1 = 37 mm, and the permeability μ = 70,000, the combined shielding factor is S_T = 807,000 [58].

It is important to notice that the magnetic fields are attenuated by a factor of approximately 1000 per diameter distance from the open end of the shields. As a result, the penetration of the field at the open end is normally negligible.

Fujimaki et al. reported [36] that the magnetic field tolerance is around 4×10^{-7} Wb/m^2 with the use of moats, which requires a shielding factor of at least 70, assuming

the earth magnetic field is $3x10^{-5}$ Wb/m^2. For a double magnetic shield with relative permeability of 5000, the shielding factors were measured to be close to the values predicted by Eq. (7.8), which were about 2500 in the direction parallel to the shield axis and about 100 in the direction perpendicular to the axis. These factors are much smaller than the values reported above for Cryoperm-10 only because the relative permeability is a factor of 14 smaller.

7.4 Summary

This chapter addressed what we have done not only in designing but also in fabricating and testing our circuits to ensure operations at multi-gigahertz clock and input frequencies. We have used resistive matching network to avoid signal reflection from impedance mismatch. Supply variation due to junction switching has been minimized by increasing the bias resistors. We have employed a multiple-phase clock scheme to eliminate the power supply ground bounce and a symmetric clock distribution to minimize clock skew. In laying out the circuits, high-speed signal lines were kept as far from each other as possible to reduce any mutual coupling, and ground holes have been used to prevent circuits from trapping flux. In testing, we have paid ultra care in preventing flux trapping by using double magnetic shields and by degaussing the shields before each use. We have found that the simplest and most effective way to get rid of trapped flux was to warm up and cool down the chip by lifting the probe out of the helium dewar.

Chapter 8

BRIDGE-TYPE JOSEPHSON ADC

In addition to the design of a flash-type analog-to-digital converter described in previous chapters, we have also followed up on another converter design proposed by Dave Petersen [19] for the same architecture. Designing the converter for Berkeley's previous lead alloy process, Petersen was able to demonstrate at high speeds the correct operation of all the subcircuits, including the comparator, the limiter, and the encoder [19]. However, the complete converter did not work due not only to bad dielectric layers which result in a significantly large number of pin holes but also to the large mismatch in critical current and low quality of junctions. We have redesigned the converter using Berkeley's existing niobium process. This chapter will briefly review his design, summarize his testing results, and report our progress on the project.

8.1 Architecture

This converter design is based on the same fully parallel architecture shown in Fig. 4.1 and described in Chapter 4. Specifically, it consists of a quantizer which is composed of 2^N-1 bridge-type comparators to sample the analog input signal, a thermometer-to-binary encoder realized with multiple-input XOR gates to convert the

quantizer's output into a binary format, and a resistive divider network to provide appropriate reference levels for the comparators.

8.2 Design Of Bridge-Type Comparators

8.2.1 Bridge-Type Comparator

Figure 8.1 shows the circuit schematic for the bridge-type comparator. The comparator employs an edge-triggered bridge, formed by a pair of junctions J_1, J_2, and a pair of resistors R_1, R_2, to sample the net input current I_{net}, which denotes the difference between the analog input and the reference current. The inductor L_1 is used to sense the comparator output current and to pass it to the thermometer-to-binary encoder. A clock-shaping junction is included to provide a fast rising clock signal I_{clk}. If the net input current I_{net} is positive on the rising edge of the clock current I_{clk}, the critical current of junction J_1 is exceeded before that of junction J_2. Consequently, J_1 switches to the voltage state before junction J_2, a gap voltage is developed across R_1, and a large counter-clockwise current flows through the inductor L_1 through R_1 to ground. Switching of J_1 to the voltage state immediately nulls out the clock current I_{clk} and prevents J_2 from switching. On the other hand, if the net input current I_{net} is negative when the clock I_{clk} is asserted, junction J_2 will switch to the voltage state and a clockwise current exists in the loop formed by R_2, L_1, and junction J_1. By detecting the direction of the current in the inductor L_1, the analog input can be determined to be larger or smaller than the reference current.

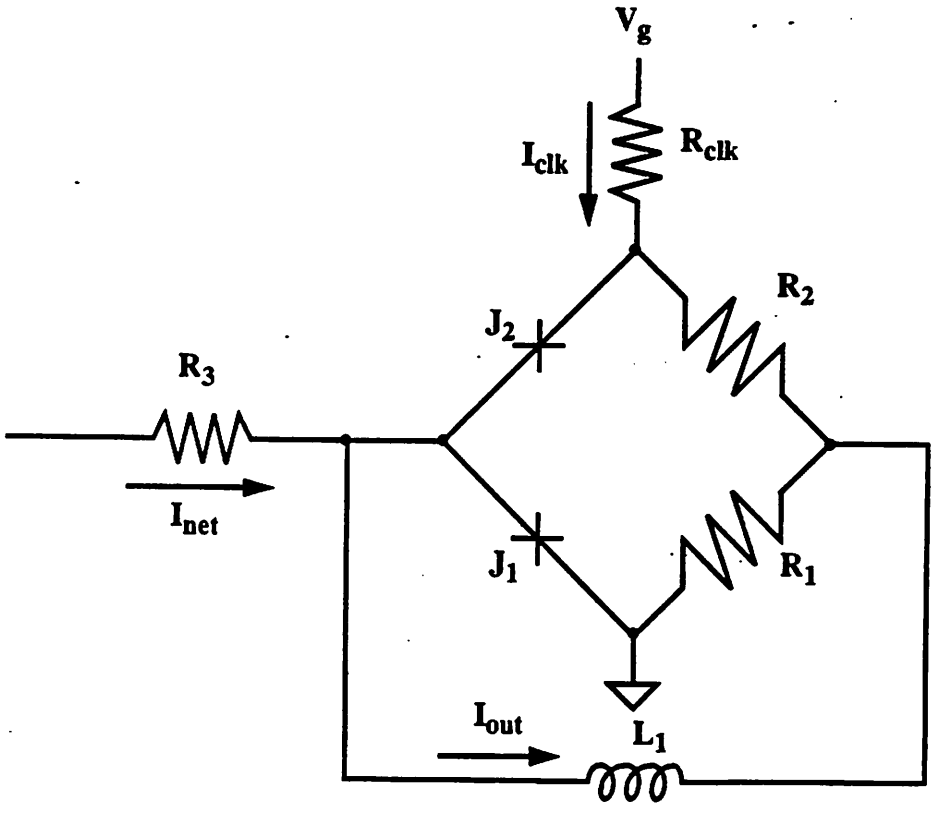


Fig. 8.1 Circuit schematic for the current-latched bridge-type comparator.

For optimal circuit margins and operating speed, J_1 and J_2 are designed to have the same critical current, and the clock current is two to three times larger than this critical current. Due to the edge-triggering nature of the design, the circuit is very robust to variation in the critical current density. As long as the changes in critical current of the two junctions J_1 and J_2 track each other well, the comparator will function as expected.

8.2.2 Design Of Limiter Circuits

The dynamic range, by definition, is the ratio between the maximum input and the minimum input that can be applied without malfunction of the comparator. The problem

with this comparator design is that this dynamic range is very small. The maximum input is set by the junction critical current because if the input amplitude exceeds this current value, one of the two junctions will switch even before the clock is applied, and the comparator will function incorrectly. The minimum input is set by the comparator's input offset due to mismatch in critical current of the two junctions. Typically, the mismatch in critical current of any two junctions can be as large as 15% of their absolute values. This results in a dynamic range of approximately seven, which falls short of even three bits. To increase the dynamic range of the input, a limiter is placed in front of each comparator.

Ideally, a limiter is a device that allows inputs with amplitude within a certain signal range to pass by without any attenuation but clips all inputs with higher amplitude so that the output never exceeds an acceptable level. The quasi-particle characteristic curve of an ideal Josephson junction turns out to be a useful choice for this purpose. In its subgap region, the junction has a very high impedance and thus sinks very little current from the input. However, in the normal region, the impedance of the junction is so low that it will sink extra current to ground and thus limits the output current. It is a soft limiter in that the voltage can rise along the R_n line of the characteristic. Figure 8.2 shows how a limiter can be implemented with a Josephson junction.

The main problem with using a Josephson junction to implement a limiter is that there exists a superconducting current in the junction. If nothing is done about it, all the current will be shunted away from the input through the junction to ground, even for input signals with acceptable amplitude. One of the solutions for this problem is to suppress the critical current of the junction to a negligible level by coupling magnetic flux laterally

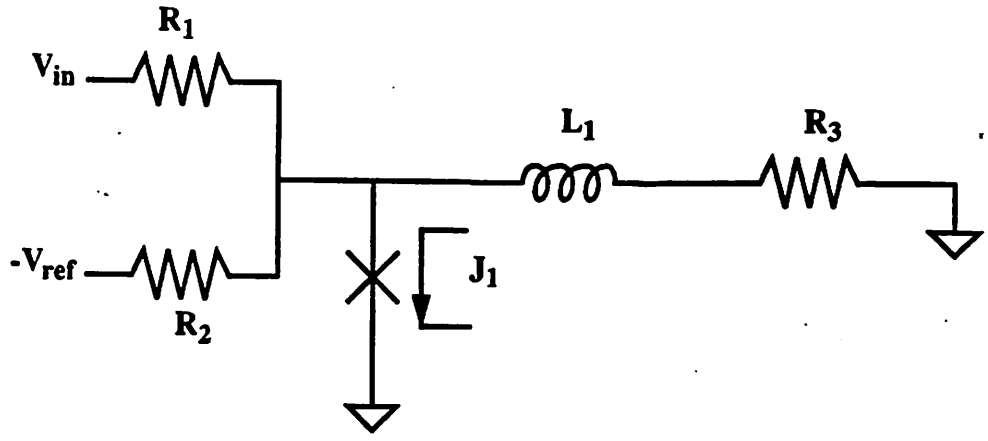


Fig. 8.2 Circuit schematic for the limiter using a Josephson junction.

across the junction. Magnetic flux can be coupled to a junction by driving a large current through a third metal wire on the top of the junction. For the Hypres process or any other process that supports more than two metal layers, a third metal layer can be conveniently used for this purpose. However, for Berkeley's process, because only two metal layers have been available, it has been necessary to extend the counterelectrode into a loop away from the junction area and to run a current through a separate line underneath using the other metal layer to couple flux into the loop and the junction. Figure 8.3 shows an example of such a layout.

8.2.3 Design Of Sine-Shaped Junctions For Limiters

Shaped Josephson junctions have been used to obtain better suppression characteristic in the presence of a magnetic field. A junction can be considered small if the ratio of its length L to its Josephson penetration depth λ_j is less than 2, where [60]

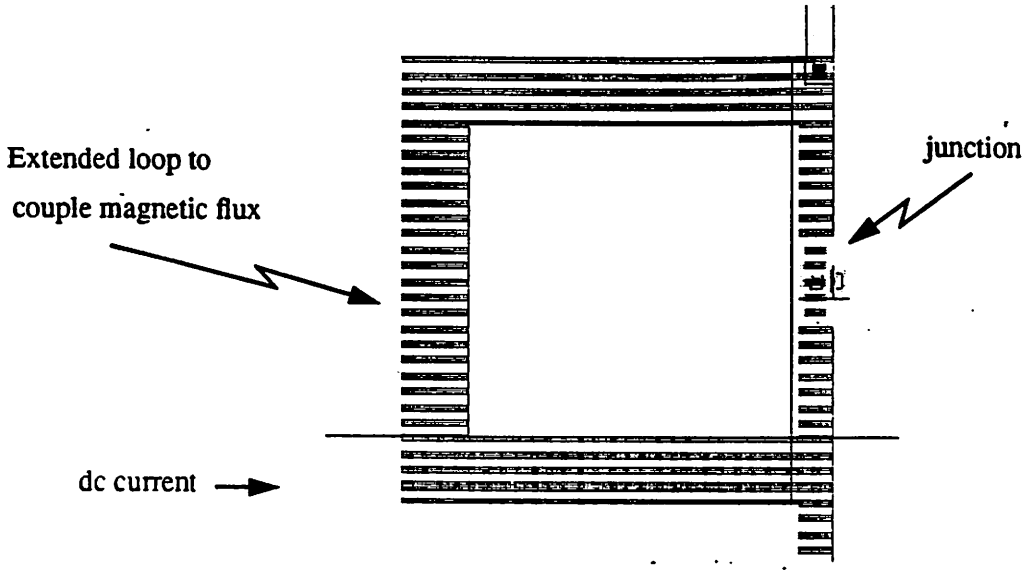


Fig. 8.3 Layout of a Josephson junction as a limiter with a loop to couple magnetic flux.

$$\lambda_j^2 = \frac{\Phi_0}{2\pi} \frac{1}{J_c \mu (2\lambda + d)} = \frac{2.6\times10^{-10}}{J_c (2\lambda + d)} \tag{8.1}$$

J_c is the junction critical current density, λ is the penetration depth, and d is the thickness of the insulating barrier. Typically, for Berkeley process, $J_c = 1$ kA/cm^2, $\lambda = 60$ nm, $d = 13$ nm, $\lambda_j = 17.4$ μm.

For small junctions, the control current I_{con} required to suppress the critical current I_c to the first minimum of the Fraunhofer diffraction pattern is given by [61]

$$I_{con} = \frac{2\pi I_c}{(L/\lambda_j)^2} \tag{8.2}$$

For long junctions, where $L/\lambda_j > 3$, the self-field of the junction current becomes important, and the junction characteristic depends strongly not only on the critical current density J_c but also on the junction geometry [61] [62]. Simulations have shown that minimum side lobes can be obtained for sinusoidal-shaped junctions [63].

It is important to emphasize that for very long junctions where the length L and the width W are much larger than the Josephson penetration depth λ_j, there is very little current in the center of the junction [62]. Most of the junction current is distributed over an outer ring with a thickness of λ_j, as indicated in Fig. 8.4. As a result, only the ring area A

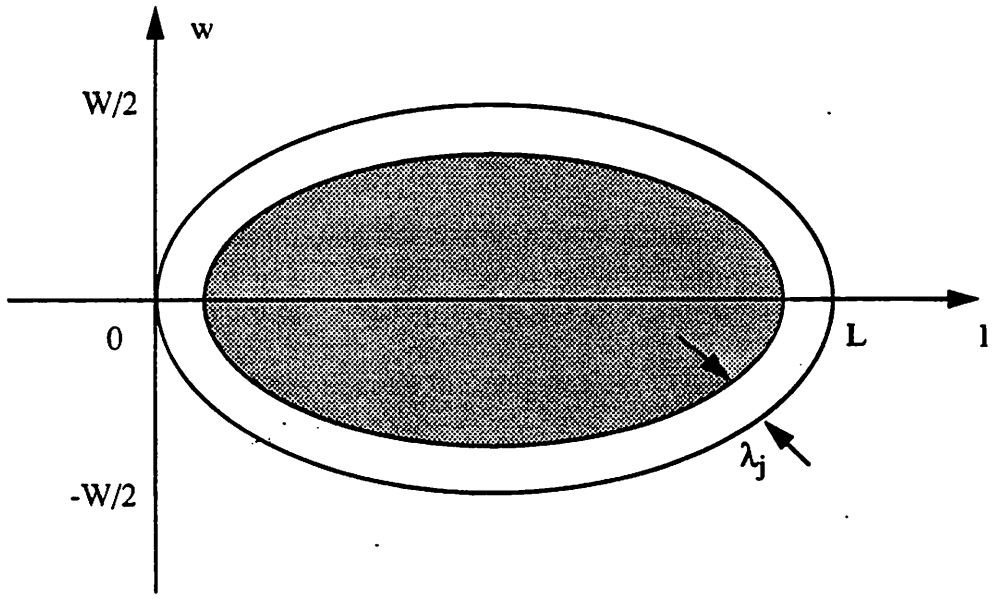


Fig. 8.4 A sinusoidal-shaped Josephson junction with large L/λ_j.

should be taken into account in calculating the junction critical current. Since the total area of a sinusoidal junction with a length L and a width of W is

$$A = 2\int_0^L \frac{W}{2} \sin\left(\frac{\pi l}{L}\right) dl = \frac{2}{\pi} WL \tag{8.3}$$

the area of the ring is given by

$$A = \frac{2}{\pi}(L + W - 2\lambda_j)\lambda_j \tag{8.4}$$

If the critical current density J_c can be approximated to be uniform on the ring, the junction critical current I_c becomes

$$I_c = A \cdot J_c = \frac{4}{\pi}(L + W - 2\lambda_j)\lambda_j J_c \tag{8.5}$$

8.2.4 Design And Layout Of The Comparator With A Limiter

Figure 8.5 shows the combination of a comparator and a limiter. The inductor L_2 is included to create a second-order RLC circuit to increase the input bandwidth of the limiter. The corresponding layout of the complete circuit is shown in Fig. 8.6.

8.3 Design Of The Thermometer-To-Binary Encoder

The logic implementation of a three-bit thermometer-to-binary encoder is shown in Fig. 8.7 By applying the inputs in opposite directions, two-junction SQUIDs can be used to implement multiple-input exclusive-OR gates for the encoder. Figures 8.8 and 8.9 show the circuit schematics and the layouts of a two-input XOR gate and a four-input XOR gate, respectively. An eight-input XOR gate is implemented in exactly the same way. Notice that the inputs are applied alternately in opposite directions and that an even number of inputs is required for a symmetrical and optimal design.

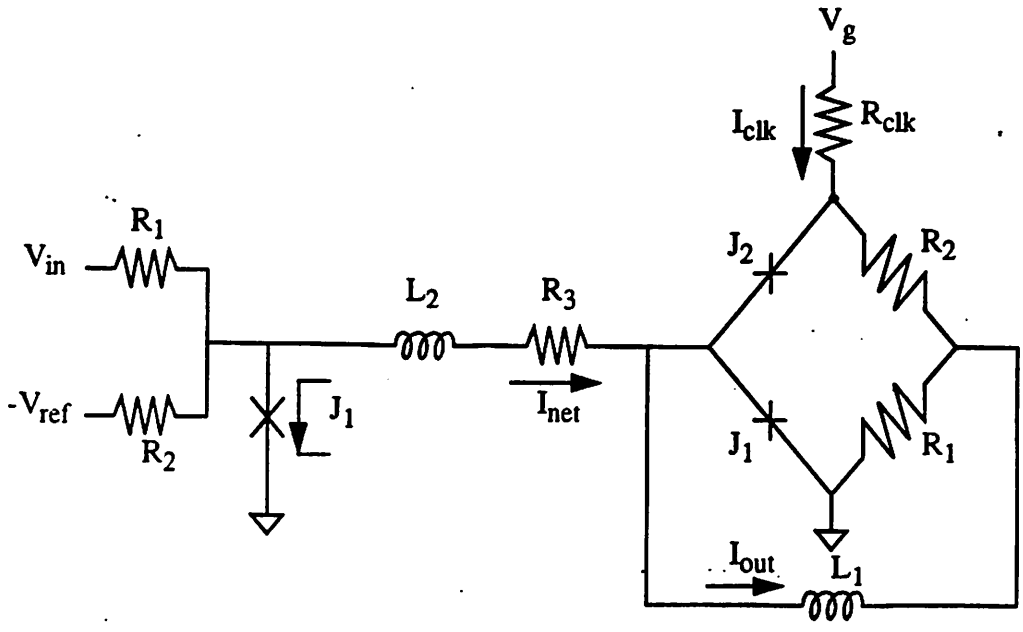


Fig. 8.5 Complete circuit schematic for the comparator preceded by a limiter.

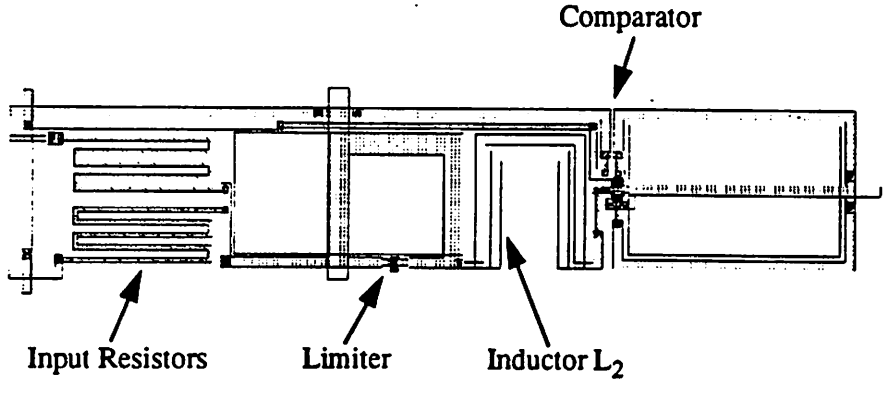


Fig. 8.6 Layout of the complete comparator including the limiter and the input resistors.

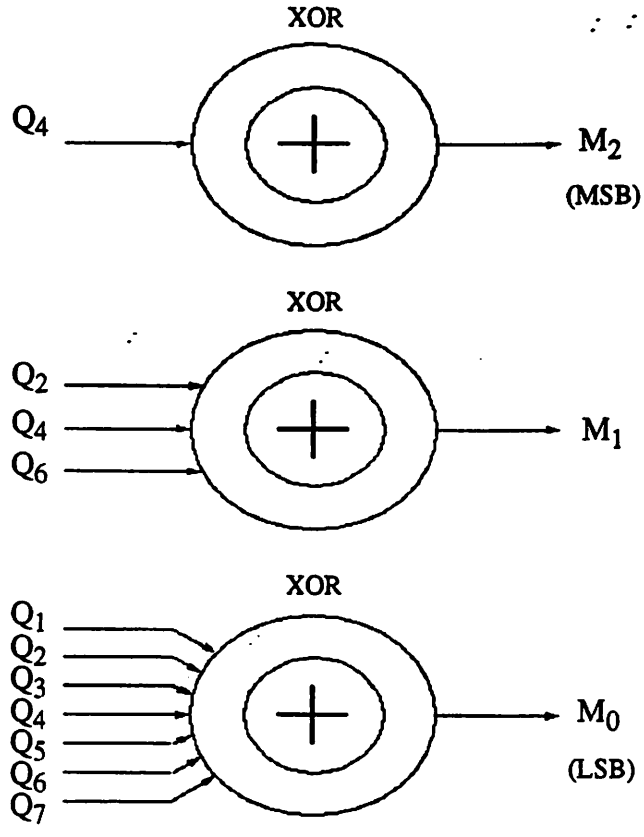


Fig. 8.7 Logic implementation of the 3-bit binary encoder using XOR gates.

To reduce the current required from the outputs of the comparators and to optimize the operating margins of the two-junction SQUIDs, it is desirable to offset the initial operating point of the SQUIDs with a dc current applied to one of the inputs.

It is important in this design that the total equivalent inductive loads for all outputs of the comparators, which are also inputs to the encoder, need to be kept the same so that an equal output current is achieved for all the comparators. It proved to be difficult and tedious to match the inductance of all the output lines, mainly because they are distributed

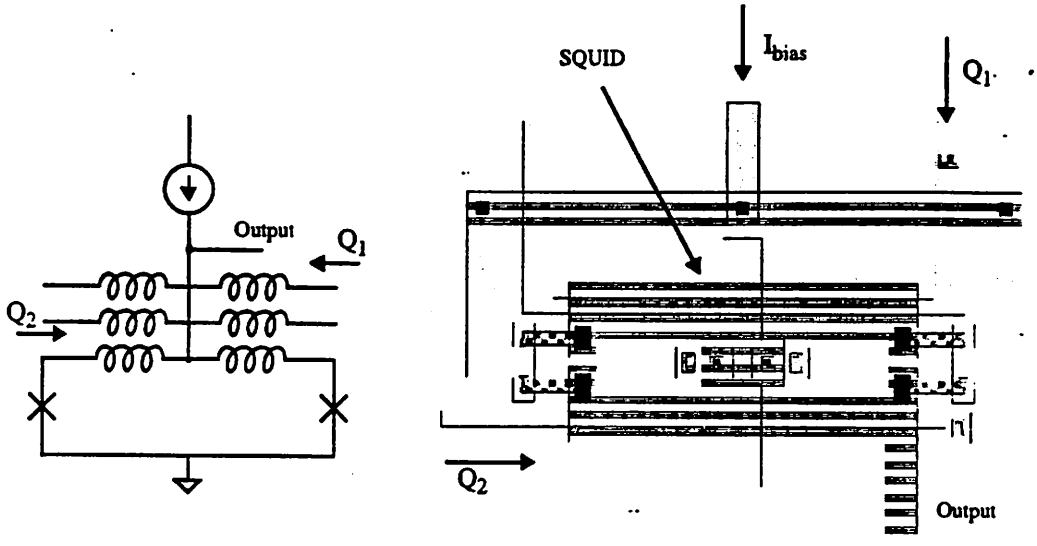


Fig. 8.8 Schematic and layout of a two-input XOR gate used as a two-bit encoder

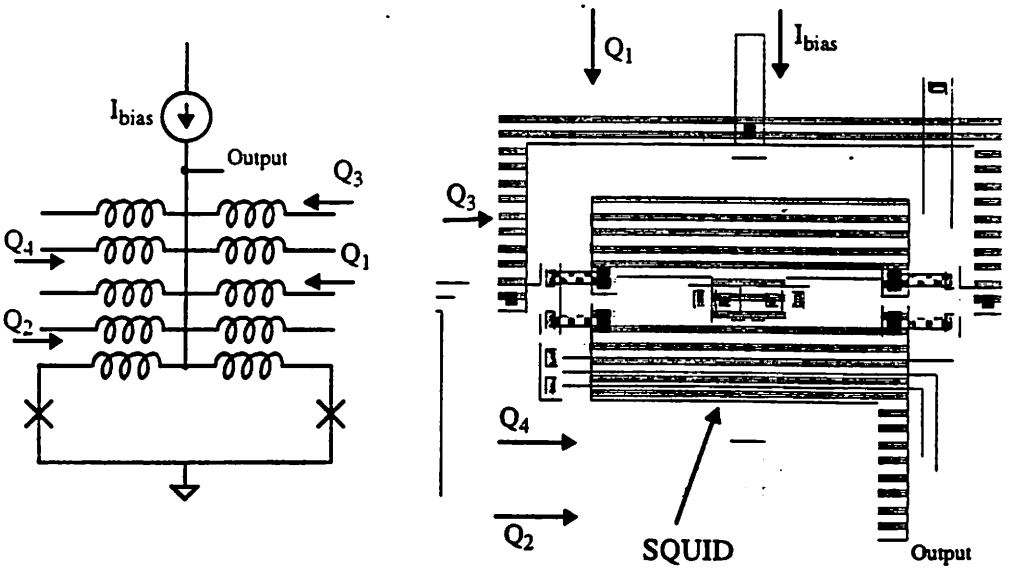


Fig. 8.9 Schematic and layout of a four-input XOR gate used as a four-bit encoder

with different loads. It is therefore necessary to have few iterations, which include layout, fabrication, measurement, and modification, before the desired matching can be achieved.

Inductance L of a microstrip transmission line can be estimated using the simple formula given by Van Duzer and Turner [64]

$$L = \frac{\mu_0 d \kappa}{w}\left(1 + \frac{\lambda_1}{d}\coth\frac{b_1}{\lambda_1} + \frac{\lambda_2}{d}\coth\frac{b_2}{\lambda_2}\right) \tag{8.6}$$

where μ_0 is the permeability of free space, d is the distance between the two superconductors, w is the width of the transmission line, κ is the fringing-field factor, b_1, λ_1, b_2, and λ_1 are the thicknesses and penetration depths of the two superconductors, respectively.

A more accurate formula for inductance calculation has been proposed by Chang using conformal mapping [65] [66] [67]

$$L = \frac{\mu_0 d}{wK(w, d, b_1)}\left(1 + \frac{\lambda_1}{d}\coth\frac{b_1}{\lambda_1} + \frac{\lambda_2}{d}\coth\frac{b_2}{\lambda_2} + \frac{\lambda_1}{d}\frac{2\sqrt{p}}{r_b}\operatorname{csch}\frac{b_1}{\lambda_1}\right) \tag{8.7}$$

where K, p, and r_b are functions of the width w, the thickness b_1, and the distance d between the superconductors. This formula also includes the effect of current redistribution due to the finite width of the microstrip line, in addition to the kinetic inductance, penetration depth, and the fringing effects and thus gives more accurate estimation.

In our design, coplanar rather than microstrip inductors are used to obtain larger inductance per unit length and thus minimize the chip area. The ratios of the widths of the

line and the hole underneath are varied according to the following formula for optimal design [50] [51] [68]

$$L = \frac{1}{4}\mu_0 \frac{K[(1-k^2)^{1/2}]}{K(k)} \tag{8.8}$$

where k is the ratio between the width of the superconducting line and the width of the hole and the function K(k) is given by

$$K(k) = \int_0^{\pi/2} \frac{d\phi}{(1-k^2\sin^2\phi)^{1/2}} \tag{8.9}$$

It is useful to approximate the function K(k) to obtain an analytic expression for the inductance L(k) as a function of the width ratio k as follows [51]

$$L(k) = \frac{1}{4}\mu_0 \frac{\ln\left[2\dfrac{1+\sqrt{(1-k^2)^{1/2}}}{1-\sqrt{(1-k^2)^{1/2}}}\right]}{\pi} \quad \text{for} \quad 0<k<\frac{1}{\sqrt{2}} \tag{8.10}$$

and

$$L(k) = \frac{1}{4}\mu_0 \frac{\pi}{\ln\left[2\dfrac{1+\sqrt{k}}{1-\sqrt{k}}\right]} \quad \text{for} \quad \frac{1}{\sqrt{2}}<k<1 \tag{8.11}$$

8.4 Design And Performance Of The Complete Converter

Table 8.1 summarizes Petersen's test results on the comparator fabricated in the earlier lead-alloy IC process.

Table 8.1 Summary of Petersen's test results on the bridge-type comparator.

Resolution		
Experimental:	3 bits @ 4.8 GHz	
Expected:	4 bits @ 2.4 GHz	
Dynamic range		
Without limiter:		
	Dynamic range:	± 200 μA
	Input offset current:	34 μA
	Resolution limit (1LSB):	8 μA
With limiter:		
	Dynamic range:	± 1040 μA
	Input offset current:	25 μA
	Resolution limit (1LSB):	16 μA

In the present work, design adjustments for the niobium process were made on Petersen's ADC, and a complete three-bit ADC has been fabricated and tested at low speeds. Figure 8.10 shows the layout of the complete three-bit ADC for the Berkeley process. To prevent any possible clock skew, only one clock junction is used to generate

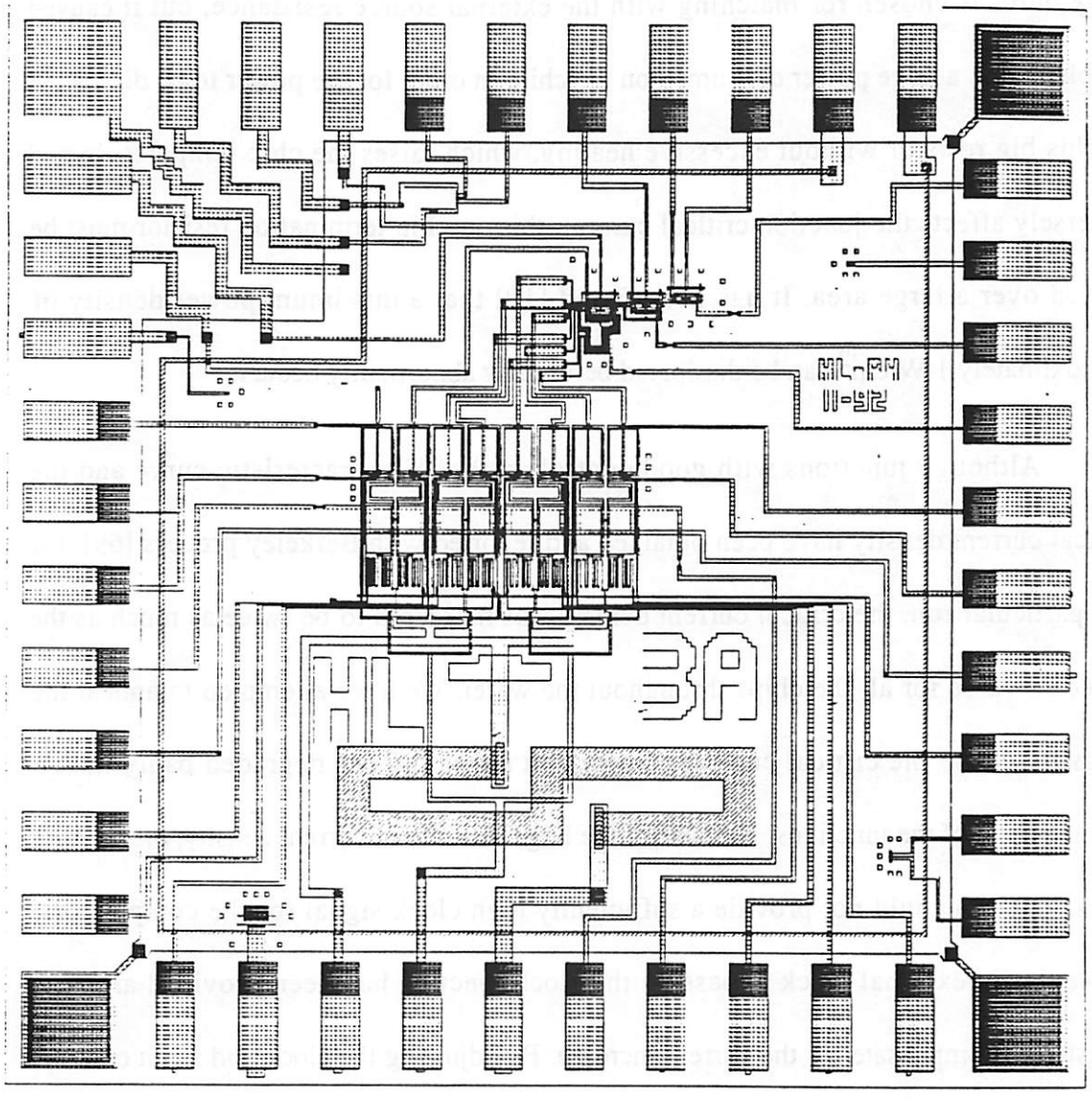


Fig. 8.10 Chip layout of the three-bit bridge-type analog-to-digital converter.

one clock signal for all seven comparators. Each comparator requires only a clock current of 300 μA, and the total clock current needs to be only 2.4 mA. However, to ensure that sufficient voltage and current are provided to the comparators, the clock junction is designed to have a critical current of around 6 mA, which is a factor of 2.5 overdrive.

A 50-Ω on-chip resistor is used to connect the clock junction to the external clock. Fifty ohms is chosen for matching with the external source resistance, but it caused problem with a large power consumed on the chip. In order for the power to be dissipated on this big resistor without excessive heating, which raises the chip temperature and adversely affects the junction critical current, this on-chip termination resistor must be spread over a large area. It has been found [19] that a maximum power density of approximately 1 W/cm^2 can be dissipated before any abnormality occurs.

Although junctions with good control on the IV characteristic curve and the critical current density have been obtained and reported with Berkeley process [69], for this particular run, the critical current density was measured to be twice as much as the expected value for all the chips throughout the wafer. We have attempted to anneal the chips to reduce the critical current density, but annealing has degraded badly the IV characteristic of the junctions. Because of the large increase in current density, the on-chip clock junction could not provide a sufficiently high clock signal for the comparators. However, an external clock bypassing the clock junction had been provided and was adjusted to compensate for the current increase. By adjusting the clock and input currents externally, the functionality of the limiters and comparators could still be successfully demonstrated.

Experimentally, it has been found that a junction's critical current can be suppressed to as small as 5 μA from a value of 400 μA if a dc suppressing current of approximately 70 mA is applied. Figure 8.11 shows typical measured IV curves of a rectangular junction. To the left is an IV curve obtained without the suppressing current

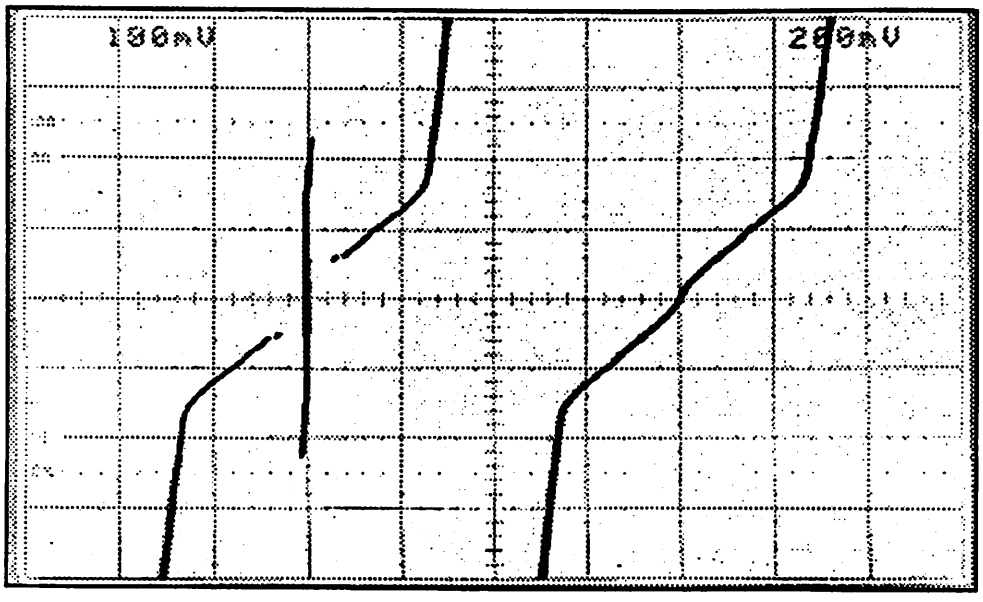


Fig. 8.11 Measured IV curve for the limiter junction without and with suppressing current.

applied, and to the right is an IV curve obtained with a dc current of 67 mA applied to the control line to couple magnetic flux into the junction for suppression. The dc suppression current required is rather large but not unreasonable considering Petersen's result, which requires a dc current of 20 mA to suppress a junction with a critical current of 170 μA.

Figure 8.12 shows the measured dc transfer curve for the limiter. The horizontal axis is the input current, and the vertical axis is the output current. As expected, the output current is leveled out when the input current is large enough. As can also be observed from the figure, the slope of the dc transfer curves is slightly less than unity. This is the result of a small fraction of the input current flowing through the limiter due to a nonideal subgap resistance of the junction. As a confirmation, the IV curve of the junction was measured,

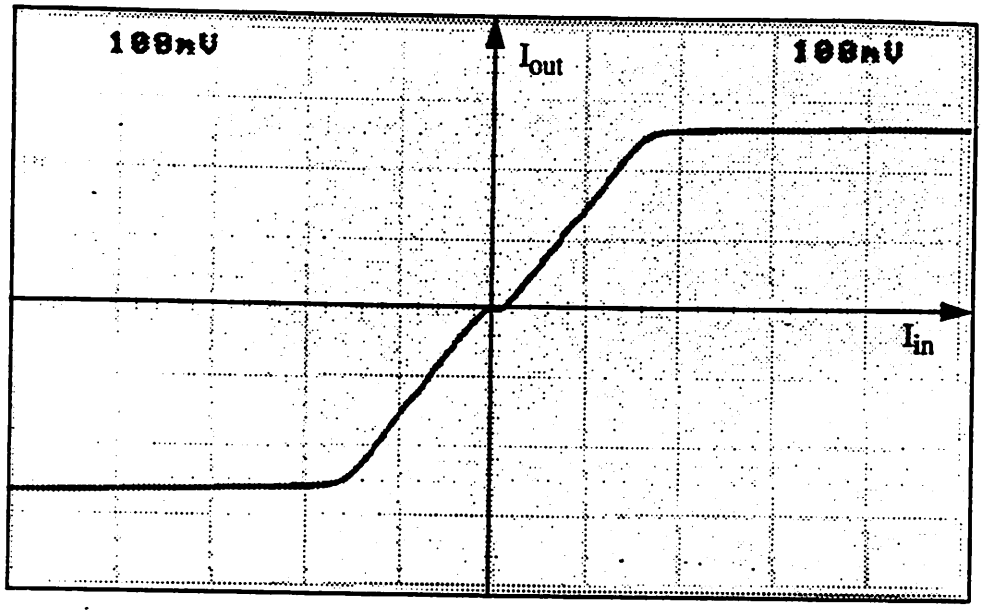


Fig. 8.12 Measured dc transfer curve for the limiter with suppression current applied.

and the V_m of the junction was found to be less than 10 mV, as opposed to the expected value of 30 to 40 mV for a good junction.

The notch ("deadband") that exists for input current around zero is zoomed in at a much smaller scale in Fig. 8.13. This is due to the nonzero residue critical current in the limiter junction as the suppressing current is applied.

Figure 8.14 shows the measured output of the complete bridge-type comparator preceded by a limiter. From the top, the traces are the clock, the input current, and the output current, respectively. Referring to the circuit schematic in Fig. 8.5, the output current through the inductor L_1 cannot be measured directly. As a result, we obtain the output current by measuring and subtracting the voltages across R_1 and R_2. Since R_1 and

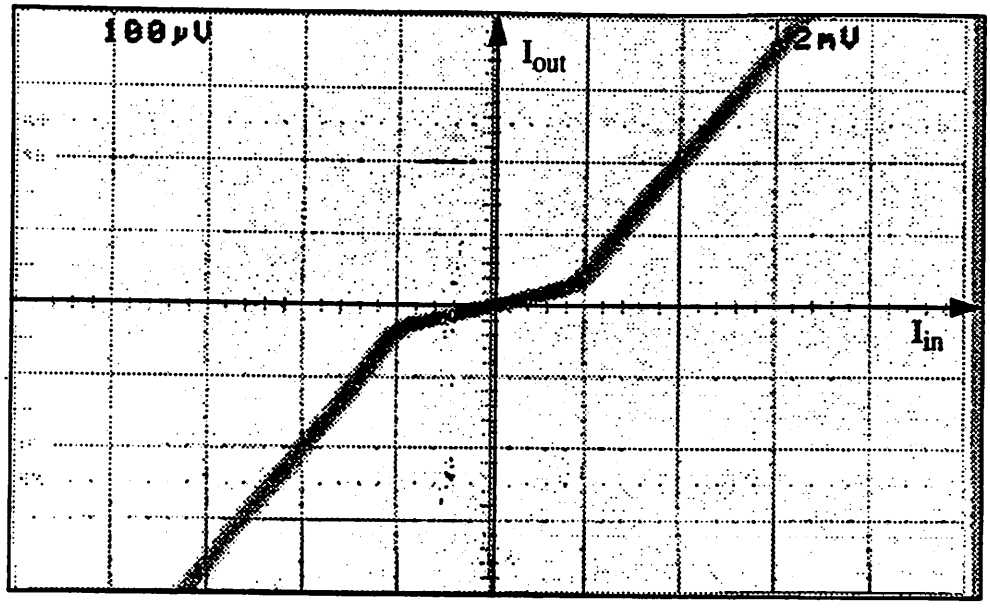


Fig. 8.13 Blown-up version of the "deadband" region around zero input current for Fig. 8.12.

R_2 have the same value, the ratio of the voltage difference and the resistance gives the actual output current flowing through the inductor.

Despite the fact that the current density is too large, the functionalities of the limiter and the comparator have been verified by adjusting the external clock accordingly. However, it was not the case for the encoders, whose operations rely on the limited internal clocking and output signals from the comparators. Another run for the same circuit with some minor design modifications has been scheduled. Hopefully, a current density close to the expected value will be achieved this time, the whole ADC will be fully tested, and more useful results will be obtained.

To improve the chance of getting the right critical current density for circuits to work, we have been in the process of developing a new Berkeley process, in which the

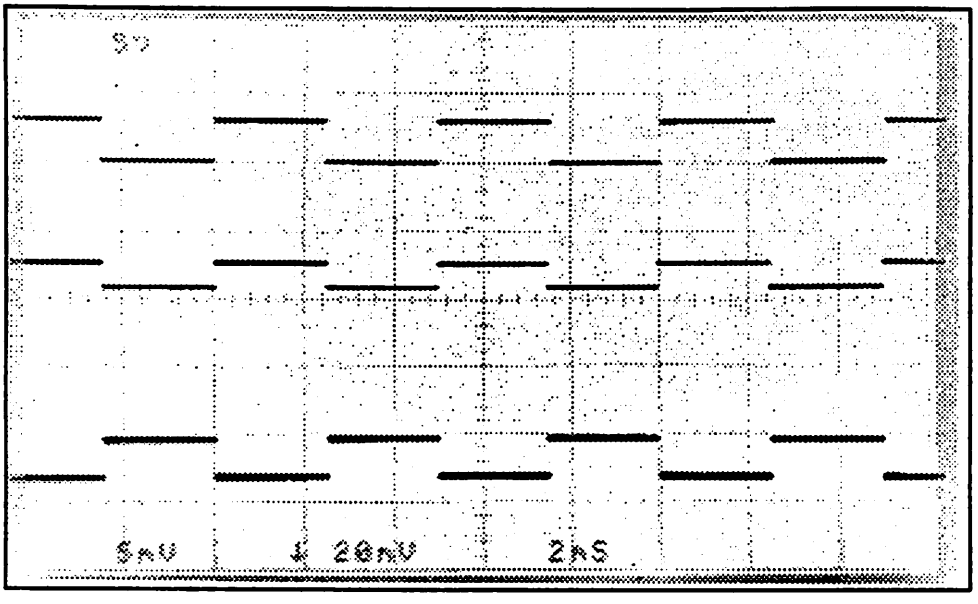


Fig. 8.14 Measured outputs of the complete bridge-type comparator.

junction trilayer is deposited and the critical current density is measured directly from the wafer before any other process is done. Knowing exactly the current density, circuit designers can adjust their design and bias the mask for the junction definition to achieve desired circuit currents.

8.5 Summary

This chapter reported the progress of our work on designing, fabricating, and testing of another fully parallel ADC, the bridge-type originally designed by Petersen. A complete three-bit ADC has been designed and fabricated. The quantizer was implemented with bridge-type comparators preceded with limiters to increase the overall dynamic range. To achieve almost ideal limiters, sinusoidal-shape junctions have been

considered, and a dc current has been used to couple magnetic flux in the limiter junction to suppress its critical current. The thermometer-to-binary encoder was realized by using multiple-input XOR gates, which were simply built out of two-junction SQUIDs. Although correct operations of comparators and limiters have been fully verified, the whole converter failed to work due to a lack of good process control, especially in critical current density. New runs and new process have been in progress to improve the chance of getting the whole circuit to work.

Chapter 9

PROPOSAL OF MULTI-STEP SUBRANGING ADC

As described in previous chapters, analog-to-digital converters implemented with the flash-type architecture can achieve very high speed. However, the main problem is the limited resolution due to the component mismatch and the number of comparators required. To increase the resolution of the converter without sacrificing too much hardware, multi-step subranging architecture has been considered. In this chapter, we will discuss the feasibility of implementing a subranging analog-to-digital converter in superconducting technology. Problems will be addressed, possible solutions will be proposed, and our preliminary design and simulation results will be presented.

9.1 Subranging Architecture

A multi-step subranging converter consists of multiple stages, each of which is a low-resolution flash-type ADC. The outputs of each ADC stage are fed into a binary encoder to obtain the corresponding significant bits and also into the input of a digital-to-analog converter (DAC) to achieve a coarse estimate of the analog input but a precise presentation of the measured bits. This estimate is subtracted from the original

input held by a sample-and-hold, and the difference is amplified and passed to the next ADC stage for a finer estimate.

For reference, the architecture for a multi-step subranging analog-to-digital converter briefly described in Chapter 2 is shown again in Fig. 9.1. Schematically, each stage needs a high-speed low-resolution ADC to achieve coarse estimation of the input signal, a low-bit high-accuracy digital-to-analog converter (DAC) to convert the digital coarse estimation to its corresponding analog signal, an accurate subtractor to obtain the residue between this analog estimation and the original input, and finally a gain stage to

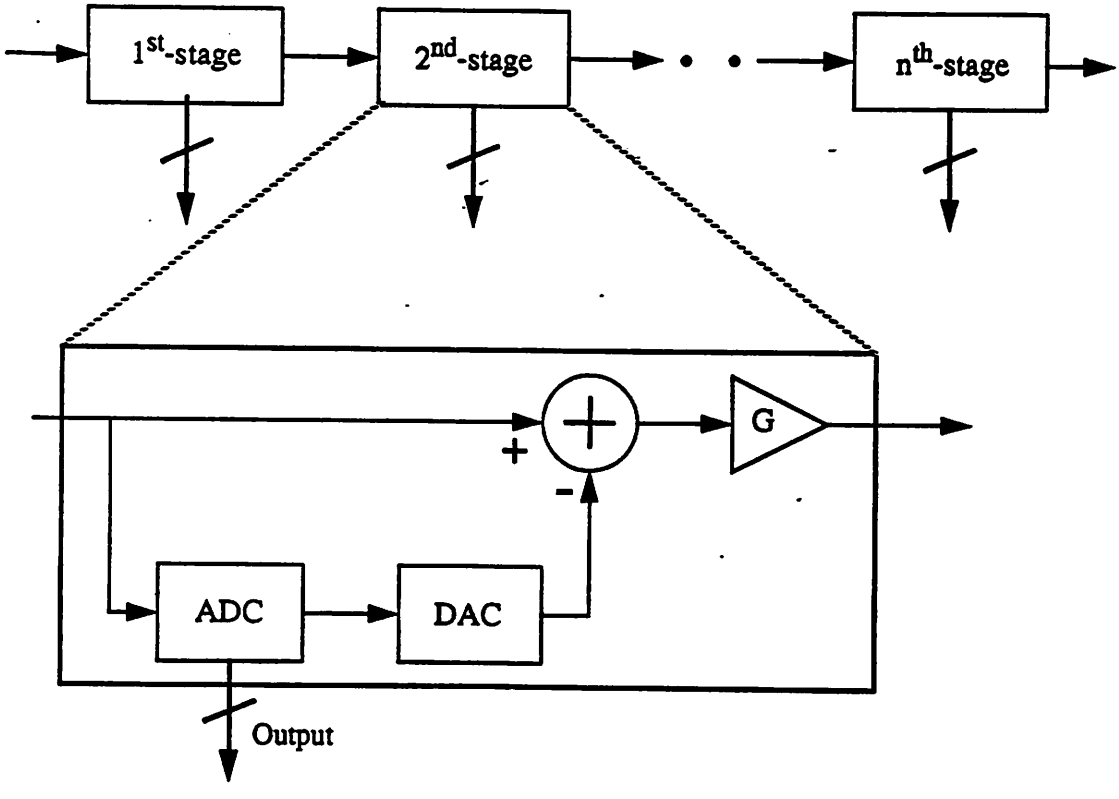


Fig. 9.1 Multi-step subranging ADC architecture.

boost up the residue to an appropriate level for finer estimation in subsequent stages. In addition, for the whole architecture to work correctly with maximum input bandwidth, it is indispensable to hold the input constant during the conversion using a sample-and-hold circuit in front of the first stage.

Figure 9.2 illustrates an example of how a six-bit three-step subranging analog-to-digital converter works, in which each of the cascading stages utilizes a two-bit ADC. The first stage compares the original input to the reference to obtain the two most significant output bits D_0D_1 and amplifies its residue for the second stage; the second stage does a

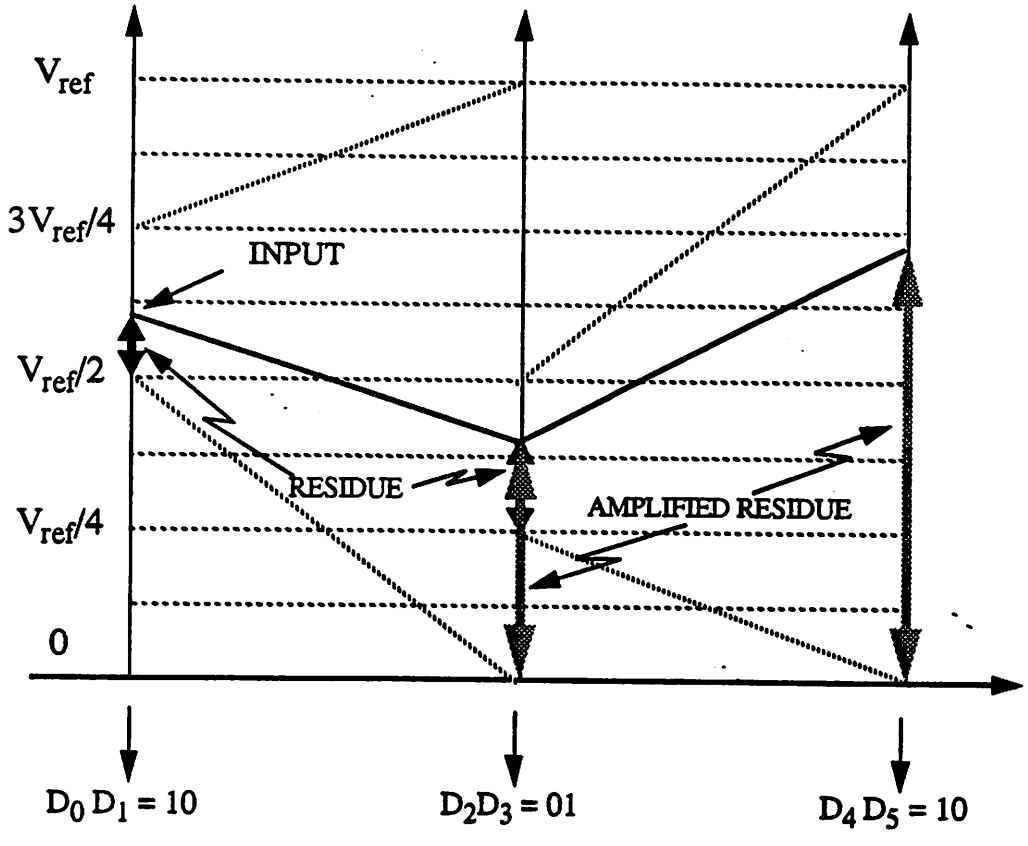


Fig. 9.2 Illustration of how a three-stage subranging ADC works.

finer estimation on this amplified residue to get two next lower significant output bits D_2D_3 and passes its residue to the third stage, which performs the final conversion and gives the two least significant output bits D_4D_5. In this example, the ADC requires a total of only nine comparators (three comparators for each of the three two-bit ADCs), which is very favorable compared to a total number of sixty-three comparators required for a fully parallel ADC with the same resolution.

This chapter will describe how different components can be designed in superconducting technology. Since parallel ADCs are ideal for the high-speed low-resolution ADCs and were fully described in previous chapters, we will focus our discussion on designs of digital-to-analog converters (DAC), sample-and-hold circuits, subtractors, and gain amplifiers.

9.2 Digital-To-Analog Converter (DAC)

The function of a digital-to-analog converter is to assign an appropriate analog value to the output given a set of digital inputs. Figure 9.3 shows the basic implementation of an n-bit DAC, where n binary-weighted current sources are connected to the output through n switches controlled by n digital inputs. If the unit current source I is equal to 1 LSB, the input combination can be selected uniquely so that the total output current is anywhere from 0 to (2^n-1)I with an increment step of I = 1LSB.

9.2.1 DAC Implementation in Superconducting Technology

Our first proposal of implementation of a DAC is to use transformer coupling. The simplified schematic diagram is shown in Fig. 9.3. The total output current available in the

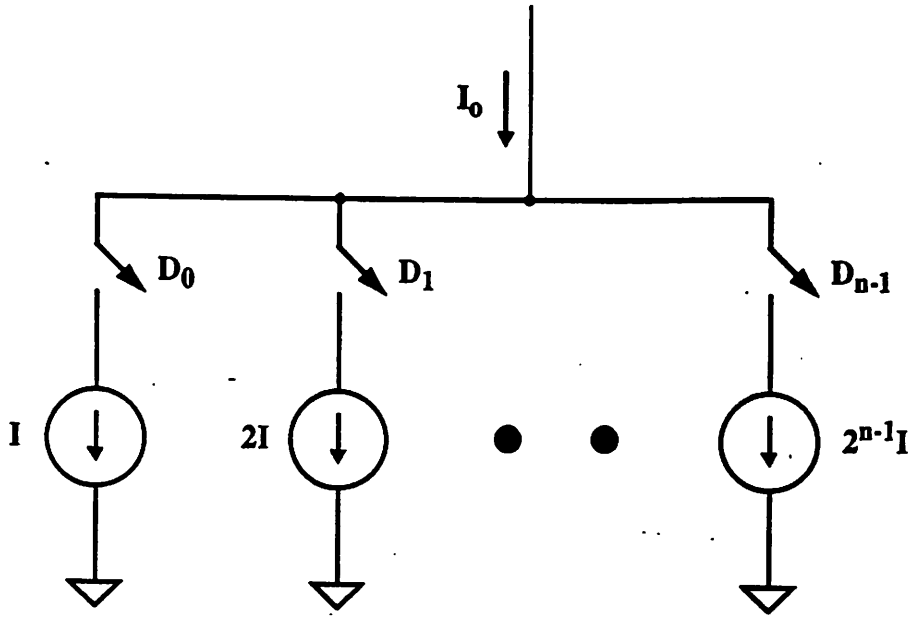


Fig. 9.3 Basic implementation of a n-bit digital-to-analog converter.

secondary transformer depends not only the values of the input currents applied to the primary transformers but also on the coupling inductances between the transformers. Superconducting transformer coupling can be controlled relatively well provided that the absolute inductance values are large enough. However, the disadvantage of this design is the speed limitation due to the large inductance required for the secondary transformer.

To increase the speed of the DAC, we propose to replace transformer with Josephson junctions or SQUIDs. Shown in Fig. 9.5 is a possible realization of such DAC where SQUIDs are used as fast switches to divert appropriate current to the output if high inputs are applied. It can be derived that, as expected for a digital-to-analog converter, the total output current I_o is given by

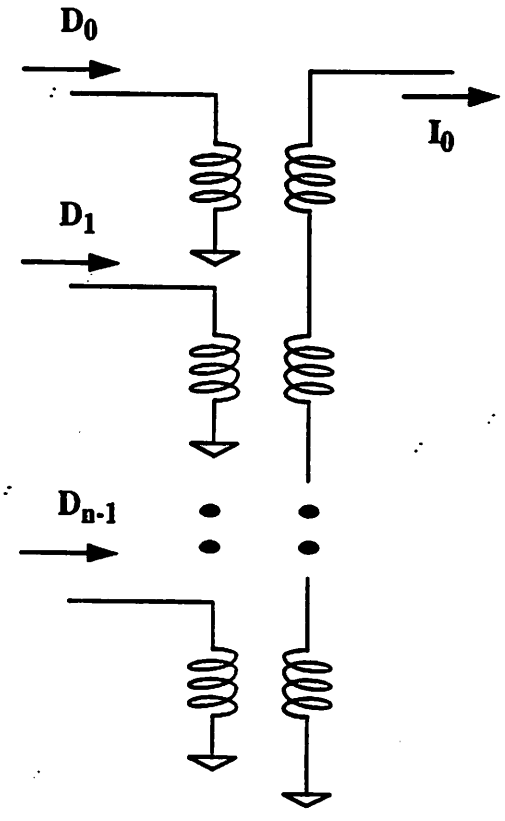


Fig. 9.4 Proposed implementation of an DAC using transformer coupling.

$$I_o = \frac{V_g}{R}(D_0 + 2D_1 + \ldots + 2^{n-1}D_{n-1}) \qquad (9.1)$$

where V_g is the gap voltage, R is the load resistance for the LSB bit, and D's are digital levels of inputs being 0s or 1s depending on whether the corresponding digital inputs are low or high.

This approach can be very fast. In fact, the conversion speed is only limited by the switching time of the SQUIDs. However, the maximum output current from each SQUID is limited to the ratio of the gap voltage and its load resistance. It is therefore not a simple

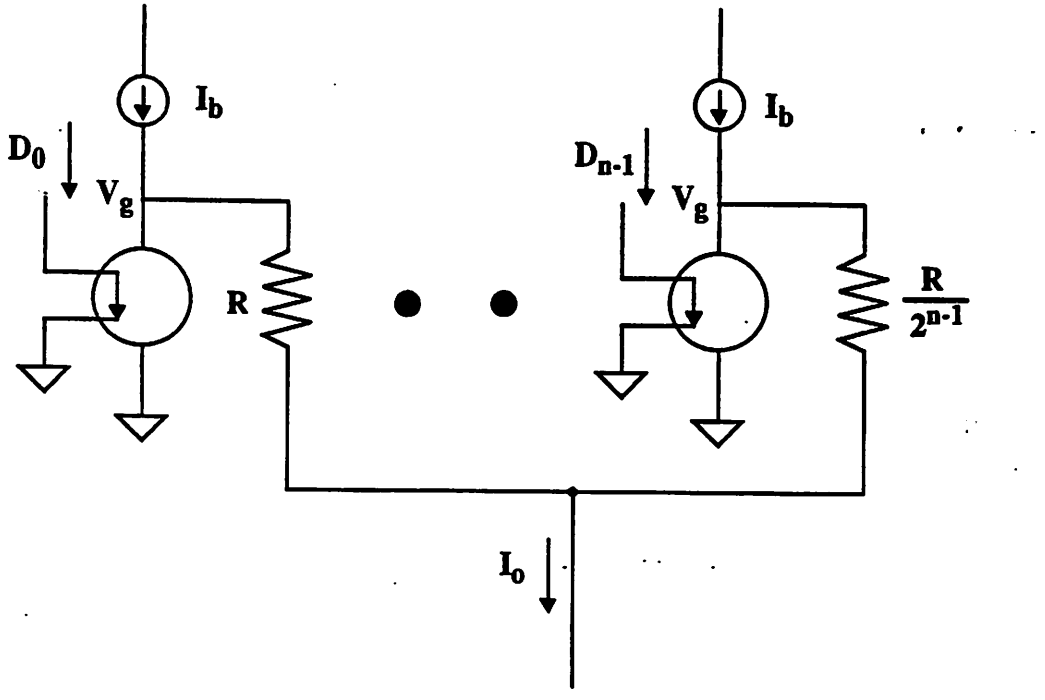


Fig. 9.5 Proposed implementation of an DAC using SQUIDs as switches.

task to obtain a very wide range of output current for SQUIDs. Notice that if single Josephson junctions with digital input current directly injected are used in place of the SQUIDs, the SQUID inductors would not be needed and much of the chip area would be saved.

The requirement of wide range of output current for SQUID devices in an implementation with binary-weighted current source can be avoided by simply using 2^n identical unit current sources instead of n-1 binary-weighted current sources. This approach is very costly in terms of hardware but surely simplifies the design significantly. In addition, the use of unit elements can guarantee monotonicity and good linearity for the converter.

Another possible implementation of a fast DAC is to use logic AND or OR gates in place of SQUIDs as fast switches. As shown in Fig. 9.6, the ultra-fast logic AND gates described in Chapter 6 can be used to switch appropriate amount of current to the output depending on the input combination. Since the logic gates have larger circuit margins

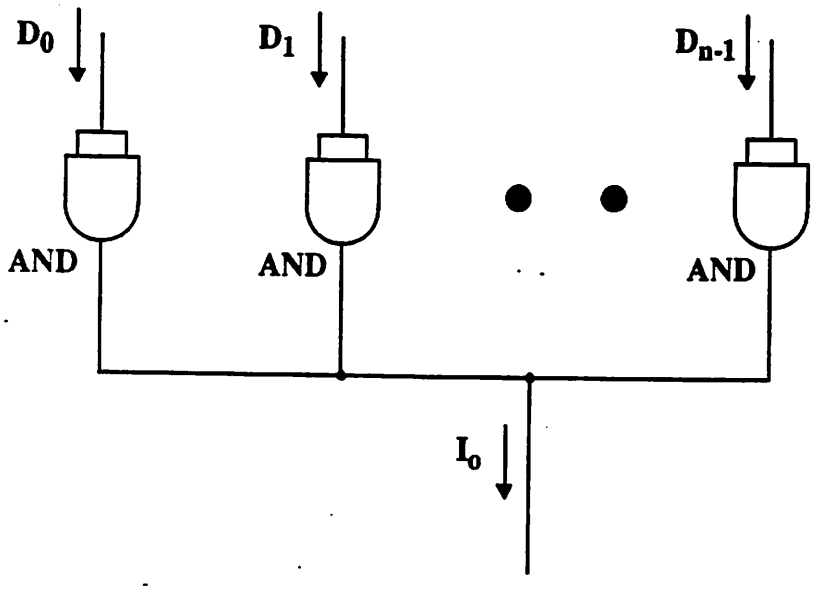


Fig. 9.6 Proposed implementation of an DAC using logic AND gates.

while requiring inputs with smaller amplitude than SQUIDs, this approach promises to yield a converter with better performance. Similar to SQUID implementation, this design has a problem with providing wide range of output current for the logic gates, and therefore the unit-element implementation is much preferred to the binary-weighted one.

Figure 9.7 shows the simulation results at a clock frequency of 2 GHz of a six-bit digital-to-analog converter using logic gates as fast switches. In this design, the resistive

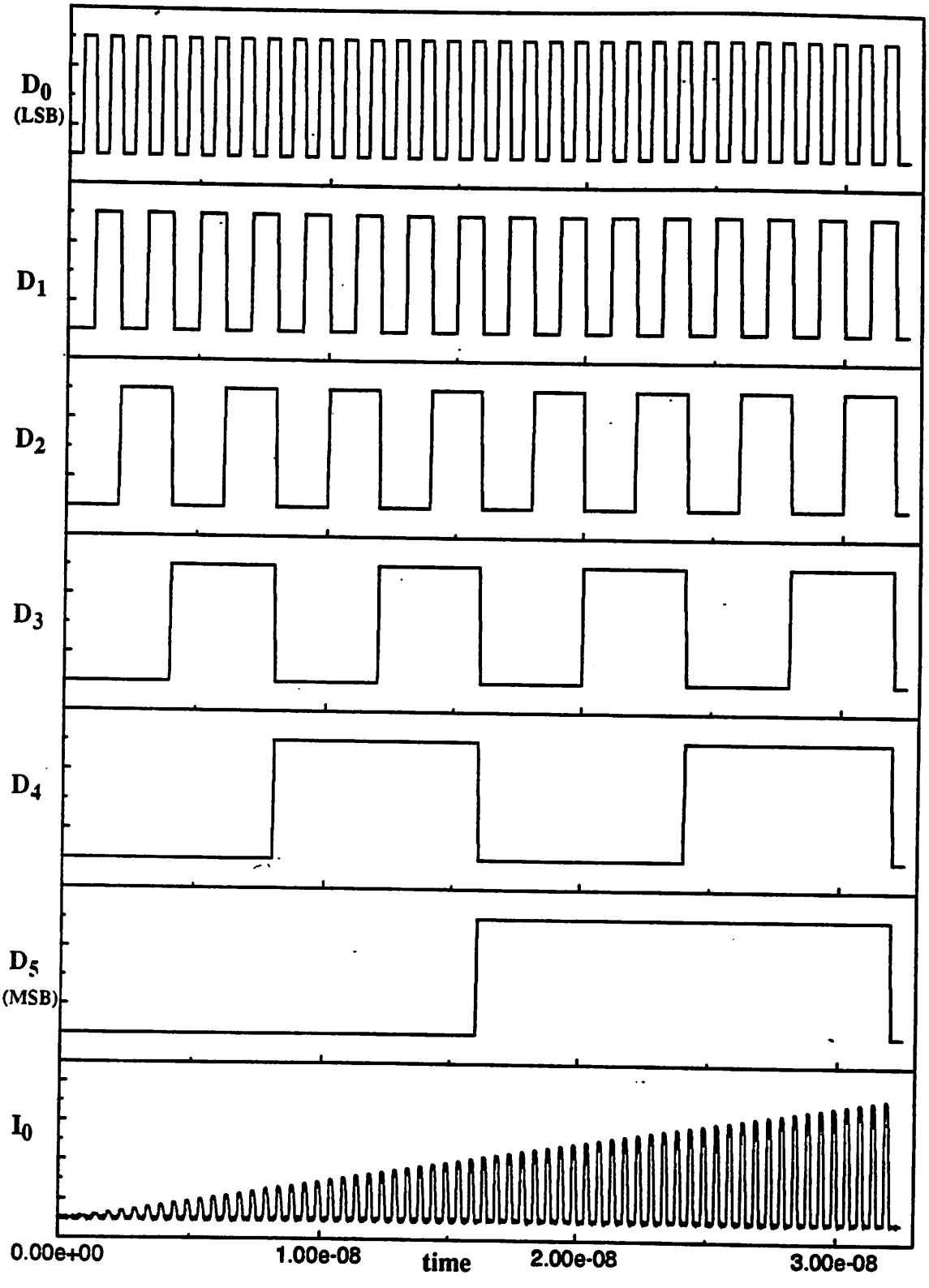


Fig. 9.7 Simulation results for a six-bit digital-to-analog converter at 2 GHz clocks.

loads for the logic gates are scaled in such a way that binary-weighted output currents are achieved. The first six graphs are the six digital inputs starting from the least significant bit from the top, and the graph at the bottom is the corresponding analog output. As expected, the output is a very linear ramping signal which steps up uniformly every clock cycle starting from zero to a maximum level of sixty-three times the unit current element and thus corresponds to a resolution of six bits.

The chip layout of the six-bit digital-to-analog converter is shown in Fig. 9.8. The resistive loads are built based on identical unit resistors R. A gate that delivers a current of $2^m I$ to the output, where m is an integer from zero to six, has an resistive load of $R/2^m$ by connecting 2^m unit-element resistors in parallel. This technique consumes a lot of chip area but ensures that any mismatch in the unit resistor due to lithography would be distributed equally and uniformly to all the resistors and thus guarantees a high accuracy. For symmetry, eight gates and eight output lines are laid out, but only six of them are connected for the measurement purpose. The two extra, at the very top and bottom, are used for process testing and monitoring.

9.2.2 Calibration of Current Sources for DAC Using CMOS

Since the amount of current delivered to the output from each gate depends on the ratio of the gap voltage and the corresponding resistive load, the overall accuracy of the DAC necessarily depends on how well these process parameters can be controlled. With the existing uniformity of the gap voltage and with a use of many parallel unit resistors, a six-bit DAC can be achieved easily. However, circuit calibration for the current sources is needed to achieve higher accuracy. During calibration, the actual current that would be

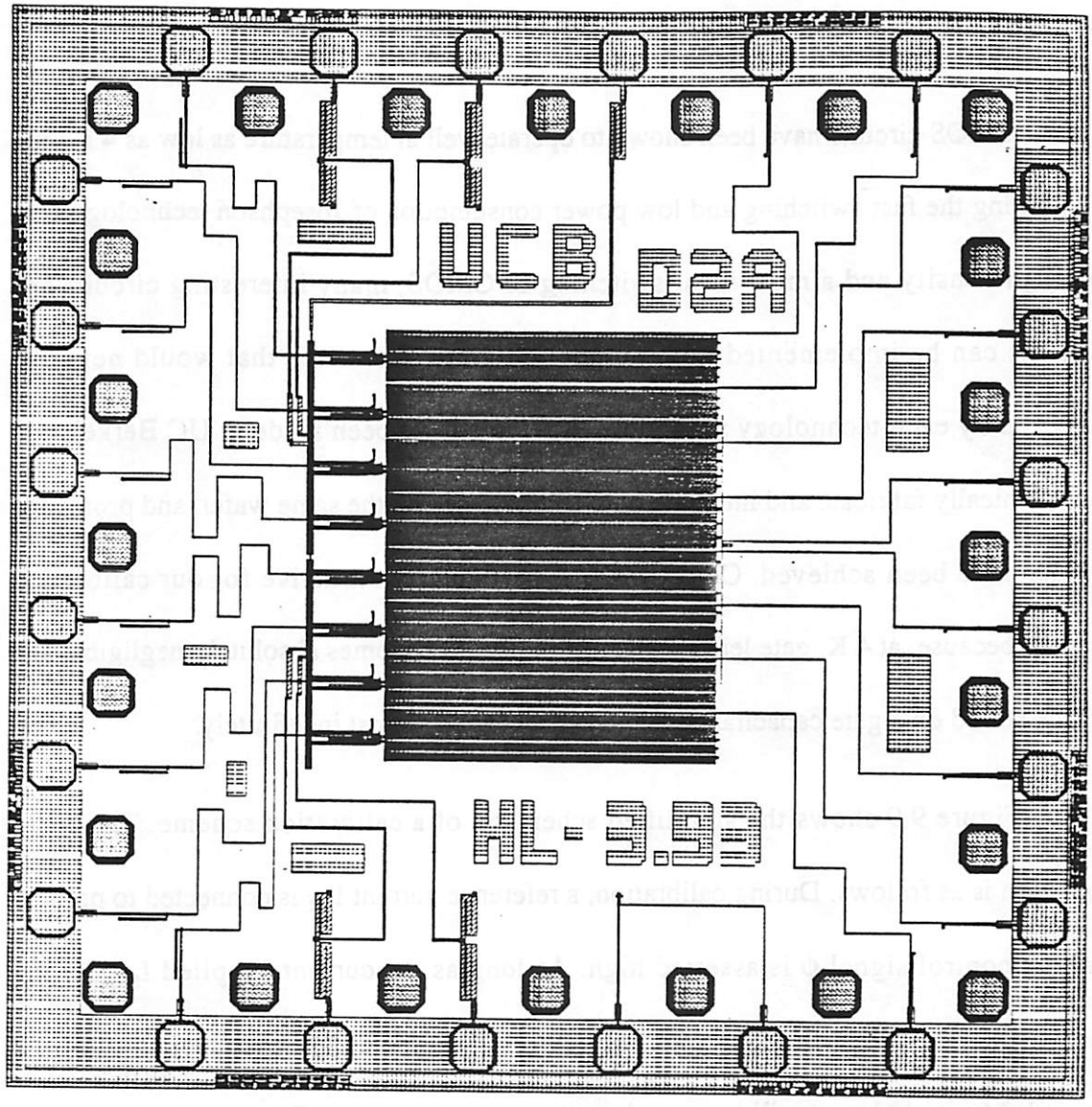


Fig. 9.8 Chip layout of the 6-bit digital-to-analog converter (DAC) using AND gates.

delivered by each gate is measured, and the difference from that current to the desired current is stored in a memory. During conversion, both the gate and the difference from the memory will be delivered to the output. Due to a lack of storage elements in

superconducting technology, we propose to perform calibration and to store the difference using CMOS devices operating at 4K.

CMOS circuits have been shown to operate well at temperature as low as 4 K [70]. Combining the fast switching and low power consumption of Josephson technology with the high density and almost ideal switching of CMOS, many interesting circuits and systems can be implemented with uniquely high performance that would never be achieved by each technology separately. Attempts have been made at UC Berkeley to monolithically fabricate and integrate both technologies on the same wafer, and promising results have been achieved. Cold CMOS is particularly attractive for our calibration scheme because, at 4 K, gate leakage current in CMOS becomes absolutely negligible and charge stored on a gate capacitance remains unchanged almost indefinitely.

Figure 9.9 shows the simplified schematic of a calibration scheme. The basic operation is as follows. During calibration, a reference current I_{ref} is connected to point A and the control signal ϕ is asserted high. As long as the current supplied I_{sup} by the Josephson gate is less than the reference current I_{ref}, the difference current will flow through M_0, and charge will be stored on the gate capacitance C_0 accordingly. During conversion mode, ϕ is kept low, and node A is connected to the output inductor L_L through the switch SW. Since the transistor M_1 is off, the original charge remains fixed on the gate capacitance C_0, the transistor M_0 will feed the same current existing during calibration, and the inductor L_L will see a total of current of $I_{sup} + I_{cal} = I_{ref}$. It is desired to have the switch SW controlled by the input signal D_0 in such a way that when the input D_0 is low, node A is disconnected from the load inductor L_L, and the calibrated current

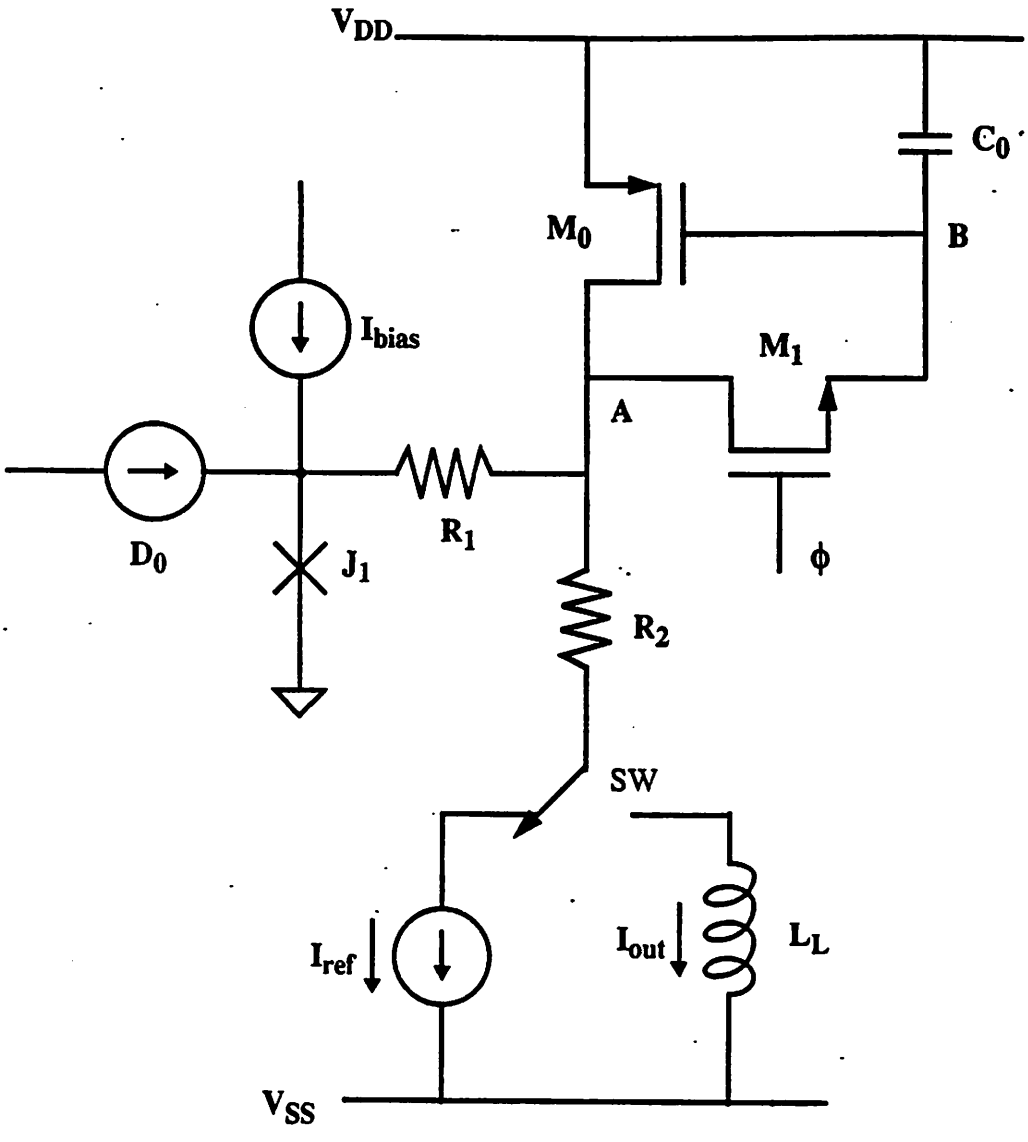


Fig. 9.9 Simplified schematic of a calibration scheme for DAC's current sources.

stored in CMOS devices is not transferred to the output. However, there exists neither a fast switch in semiconductor technology nor a good switch in superconducting technology. A solution for this is to use a resistor R_2 in series with the switch SW as shown in the figure. For the whole scheme to work appropriately, it is necessary that R_2 is

much larger than R_1. During conversion, if the input D_0 is high, the junction J_1 will switch to the voltage state with a very high impedance. As a result, all the current calibrated and stored in the MOS device M_0 will flow through R_2 to the inductive load L_L as desired. If the input D_0 is low, the junction J_1 will remain in the superconducting state with a zero impedance. In this case, most of the calibrated current stored in M_0 will flow through R_1 to J_1 and only a negligibly small current will be delivered to the inductive load L_L.

In practice, even though leakage current is no longer a concern, there exist other secondary effects that may cause variation in the actual charge stored on the MOS gate capacitance and thus the actual calibrated current. These effects include charge injection during switching and channel-length modulation effect of MOS devices. Fundamentally, it can be derived that the change in the calibrated current ΔI_{ds} is equal to

$$\Delta I_{ds} = g_m \Delta V_{gs} = \frac{3}{2}\sqrt{\frac{2\mu}{C_{ox}}}\frac{\Delta q}{L}\sqrt{\frac{I_{ds}}{WL}} \tag{9.2}$$

where g_m is the MOS transconductance, V_{gs} is the gate-to-source voltage, μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, q is the charge stored on the gate capacitor, I_{ds} is the stored current, and W and L are the width and length of the storage MOS device. Clearly, to minimize the current change, it is desirable to minimize the change in stored charge and voltage, to minimize the actual calibrated current, and to maximize the device dimensions. Change in charge, mainly due to charge injection during switching, have been minimized by adding dummy switches; and change in voltage have been reduced by using large switches. Notice that we can afford to use large switches here because the problem with larger leakage current for larger switches virtually disappears at

4 K. Cascode design can be used to minimize the channel-length modulation effect of MOS device. Finally, it is critical to keep the impedance load at node A constant before and after calibration to ensure that the same current is delivered from the Josephson gates. Various techniques, including feedback and bias-shifting, have been considered for this purpose.

Due to slow switching time of CMOS circuits, even at 4 K, the time required for calibration using cold CMOS would inevitably be much longer than the actual conversion time. However, it should not affect the converter's performance. Calibration can be as slow as necessary and needs to be done only once before any conversion. Once it is done, the converter should be able to operate at its optimal superconducting speed.

9.3 Sample-And-Hold Circuit

Figure 9.10 shows the circuit schematic of the proposed sample-and-hold together with how it functions in both sample mode and hold mode. In the sample mode, the clock ϕ is low and its complement clock $\bar{\phi}$ is high. As a result, J_2 and J_3 are in the high-impedance state whereas J_1 is in the low-impedance state.The input current I_{in} flows through J_1 and L_1 to ground. Since very little current flows through J_2 and J_3, the output current in L_1 samples or tracks the input signal very closely. In the hold mode, the clock ϕ is raised high; J_1 switches to high-impedance state, and J_2 and J_3 switch to low-impedance state. Any change in the input current will flow through J_2 into ground. The sampled current in L_1 remains constant in the superconducting loop formed by J_2 and L_1. What is novel about this design, distinguishing itself from previous sample-and-hold circuits [71] [72] [73], is that the input current is completely diverted and isolated from the inductor

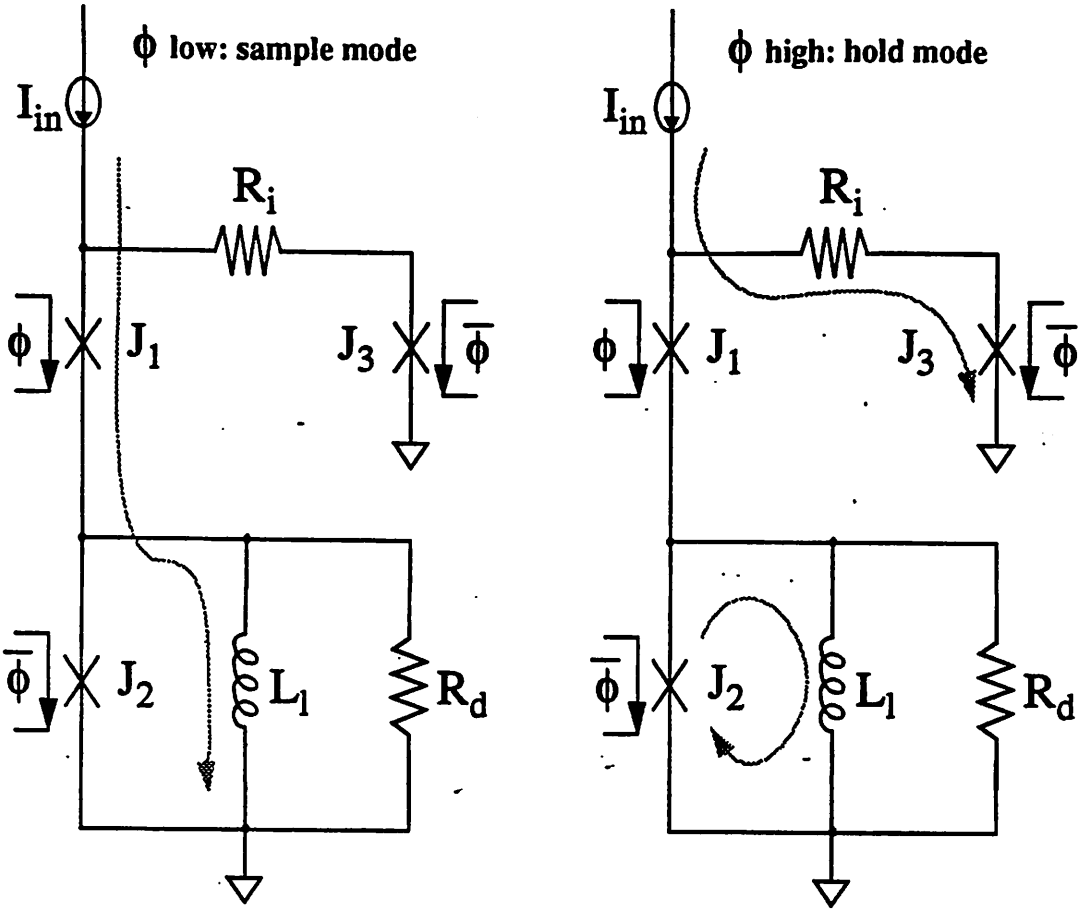


Fig. 9.10 Schematic of the sample-and-hold showing sample and hold operation.

during the hold operation, which results in a higher accuracy for a given inductance value or a lower inductance value and a higher speed for a given accuracy.

Shown in Fig. 9.11 is the simulation results for the sample-and-hold with a clock frequency of 2 GHz, an input frequency of 1 GHz, and a resolution of 6 bits. The speed is determined mainly by the value of the holding inductor L_1. If the inductor is too small, the output signal would droop too much during the hold mode that the resolution would suffer. On the other hand, if the inductor is too large, the resetting time would dominate and limit

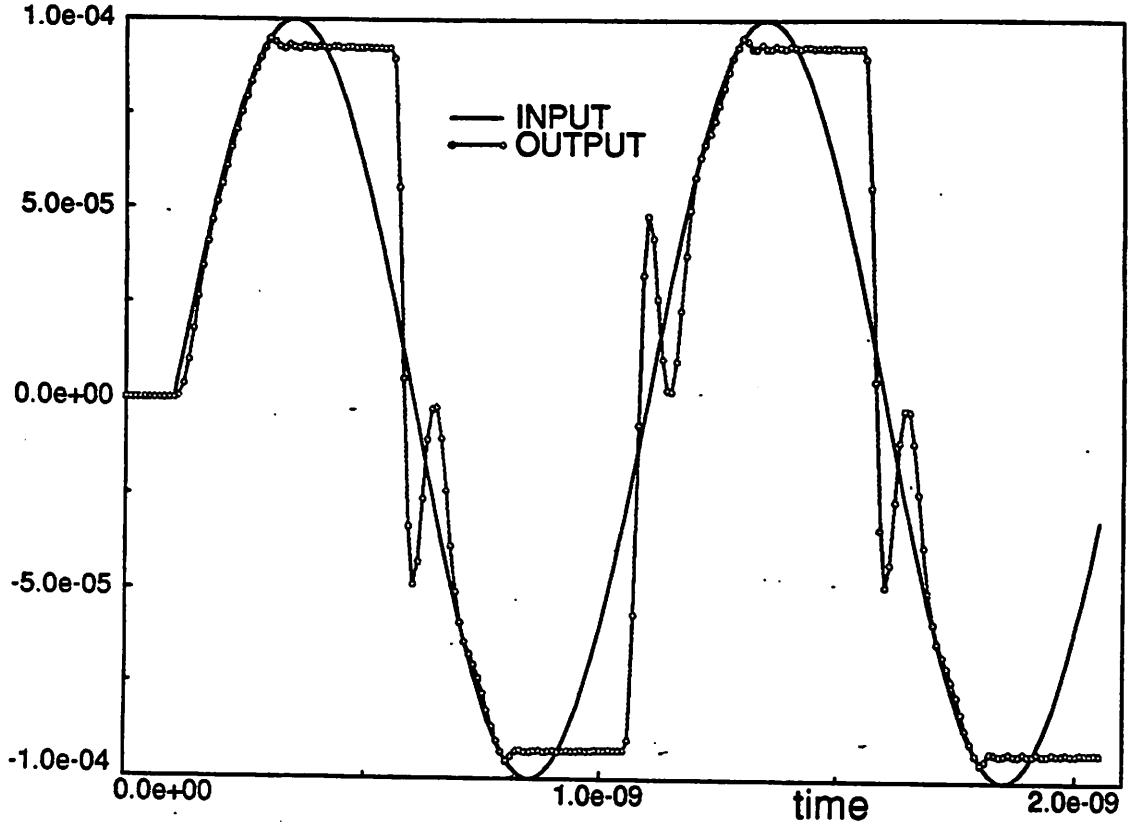


Fig. 9.11 Simulation results of the sample-and-hold at f_{in} = 1 GHz, f_{clk} = 2 GHz.

the overall speed. It is essential to include a resistor R_i in series with J_3 to improve isolation and to connect another resistor R_d in parallel with the inductor L_1 to critically damp high-frequency oscillation.

9.4 Subtractor And Amplifier

Because good amplifiers are not available in superconducting technology, we propose to use transformer coupling to perform both current subtraction and amplification simultaneously. By designing a transformer with a current ratio equal to the desired current gain and coupling two input currents in opposite directions, the desired amplified

version of the current difference can be conveniently obtained in the secondary transformer. Although transformers that can operate at multi-gigahertz frequencies have been implemented [32], it may still be difficult to design a transformer with a high current ratio at high speed. However, for our proposed subranging digital-to-analog converter, where only a current gain of 4 or 8 is required for each stage and the overall speed is limited to only few gigahertz, there should be no major problem.

9.5 Summary

This chapter presented the preliminary results on our study of the feasibility of realizing a multi-step subranging ADC in superconducting technology. Main challenges for this implementation include the designs of accurate digital-to-analog converters and high-performance sample-and-hold circuits. We have proposed different ways to implement superconducting DACs. We have designed and simulated successfully a six-bit superconducting DAC at clock frequency of 2 GHz. However, from simulations, six bits is the maximum resolution achievable with the existing process control and variation, limited mainly by the nonuniformity of junction gap voltages and resistor values. Higher resolution can be achieved by employing cold CMOS in a self-calibration scheme to provide accurate current sources for the DACs. A novel sample-and-hold circuit has been conceived and simulated successfully at clock frequency of 2 GHz and input frequency of 1 GHz. Subtractor and amplifier can be implemented using inductive transformer.

Chapter 10

CONCLUSION

Fully parallel analog-to-digital converters capable of working at multi-gigahertz clock and input frequencies have been designed, fabricated, and fully tested. These converters are not only the first superconducting ADCs ever reported that included the thermometer-to-binary encoder to achieve a binary output but also are at least one order of magnitude better than their semiconductor counterparts in terms of speed and active power.

The comparators were implemented with a one-junction SQUID as a sampler followed by a two-junction SQUID as a readout device. By using a one-junction SQUID as a pulser at the input of the comparators, a small aperture time and high performance were achieved for the converter. The same comparator building block was reconfigured to realize a new logic family used for the thermometer-to-binary encoder. Quasi-three-input and quasi-four-input XOR gates were conceived and helped reduce significantly the gate count and the chip area required.

The comparators and the logic gates have been fully tested, and their correct operations have been verified experimentally at clock frequencies up to 3 GHz, which was limited by our existing test equipment but, on the other hand, was the highest speed ever

demonstrated in our laboratory. A three-bit quantizer and a three-bit thermometer-to-binary encoder have been successfully demonstrated. The encoder was the largest working circuit in terms of the junction count and complexity that has ever been fabricated and demonstrated at Berkeley. Due to the process variations in junction critical currents, circuits with larger sizes and more complexity, including a four-bit quantizer, a three-bit ADC, and a four-bit ADC, were only partially functional. Experimentally, we found that the operating regions of the individual gates, in particular the comparators, did not have enough overlap for the whole circuit to work. A redundant scheme has been developed for four-bit quantizers and has been demonstrated to help improve the chance of getting the circuits to work properly.

A completely new ultra-fast logic family, capable of operating at frequencies up to 12.5 GHz, has also been designed based on the comparator building block and has been used to implement the thermometer-to-binary encoder required for the flash ADC. To test these logic gates at their highest possible speed, pseudo-random bit sequence generators have been built. An inverter was included in the forward path of the PRBSG to make sure the generator would be self-triggered and could never get stuck in the all-zero state. Two of such generators are connected to an XOR gate for bit-error-rate measurement. Again, due to wide spread of junction critical current, the whole circuit failed to work.

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APPENDIX A: SQUID THRESHOLD CURVES

This appendix shows how the dc transfer curve of a one-junction SQUID and the threshold characteristic curve of a two-junction SQUID can be derived.

A.1 One-Junction SQUID

Referring to Fig. 3.6 in Chapter 3, the dc transfer curve of a one-junction SQUID, which is simply the relationship between the output current I_L in the inductor and the input current I_{in}, can be calculated as follows. From Kirchoff's current law:

$$I_{in} = I_L + I_C \sin\phi \tag{A.1}$$

But we also have:

$$\frac{d\phi}{dt} = \frac{2\pi}{\Phi_0} V \qquad V = L\frac{dI_L}{dt} \tag{A.2}$$

Therefore,

$$\phi = \frac{2\pi L I_L}{\Phi_0} + K = \beta_L \frac{I_L}{I_C} + K \qquad \text{where} \qquad \beta_L = \frac{2\pi L I_L}{\Phi_0} \tag{A.3}$$

and as a result,

$$\frac{2\pi LI_{in}}{\Phi_0} = \frac{2\pi LI_C}{\Phi_0}\sin\left[\frac{2\pi LI_L}{\Phi_0}\right] + \frac{2\pi LI_L}{\Phi_0} \tag{A.4}$$

A.2 Two-Junction SQUID

The threshold characteristic curve of a two-junction SQUID can be defined as the relationship between the control current I_{con} and gate current I_g when the SQUID is in the voltage state. The condition for the SQUID to transition to the voltage state is that the total admittance seen by the gate current is zero, that is, when a small change in the gate current would cause a large change in output voltage. With this assumption, the threshold curve can be calculated as follows.

First of all, recall that the small-signal inductance of a Josephson junction is given by

$$L_J = \frac{\Phi_0}{2\pi I_C \cos\phi} \tag{A.5}$$

Therefore, referring to Fig. 3.7 in Chapter 3, the total admittance Y seen by the gate current I_g is

$$Y = \frac{1}{j\omega L_1 + j\omega\dfrac{\Phi_0}{2\pi I_{C1}\cos\phi_1}} + \frac{1}{j\omega L_2 + j\omega\dfrac{\Phi_0}{2\pi I_{C2}\cos\phi_2}} \tag{A.6}$$

Setting Y to zero to obtain the following condition for the SQUID to be in the voltage state

$$\frac{1}{\cos\phi_1} + \frac{1}{\cos\phi_2} + \beta_{L1} + \beta_{L2} = 0 \tag{A.7}$$

Using the fact that total flux in a superconducting loop is quantized to an integral number n, it can be found that:

$$n = \frac{(M_1 + M_2) I_{con}}{\Phi_0} + \frac{\phi_1 - \phi_2}{2\pi} + \frac{L_1 I_{C1} \sin\phi_1 - L_2 I_{C2} \sin\phi_2}{\Phi_0} \tag{A.8}$$

Finally, the relationship of the gate current to the two junction currents is given by;

$$I_g = I_{C1} \sin\phi_1 + I_{C2} \sin\phi_2 \tag{A.9}$$

The threshold curve of the two-junction SQUID can be obtained by combining all three Eqs. (A.7), (A.8), and (A.9).

A.3 Lagrange Multiplier Method

The Lagrange multiplier method can also be used to calculate mode boundaries and threshold curves of a superconducting loop. As a matter of fact, this method not only is simpler but also can be applied generally to any complicated superconducting circuit [74]. As a demonstration, here we show how the method can be applied to obtain the phase condition for a symmetric two-junction SQUID shown in Fig. A.1 to transition to the voltage state.

The total phase around the loop ϕ_T can be found to be:

$$\phi_T = \phi_1 - \phi_2 + 0.5\beta_L (\sin\phi_1 - \sin\phi_2) \tag{A.10}$$

and the total gate current I_g is given by:

$$I_g = I_1 + I_2 = I_C (\sin\phi_1 + \sin\phi_2) \tag{A.11}$$

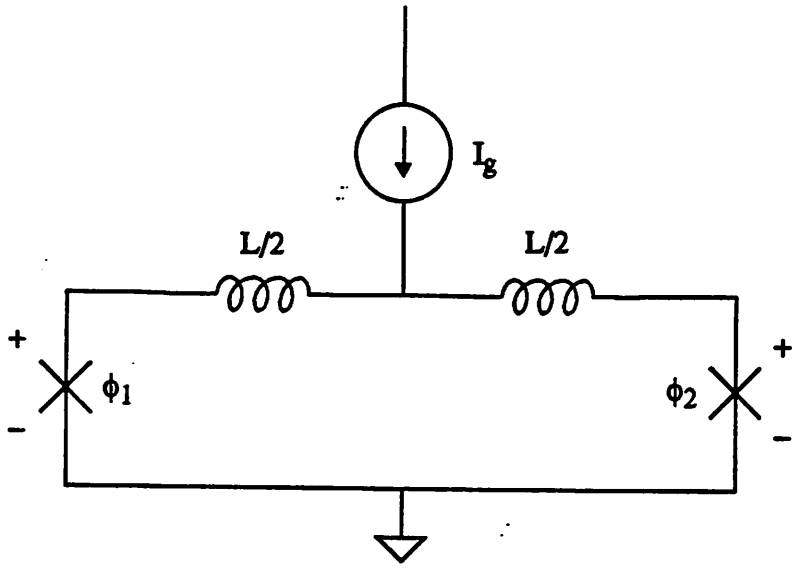

Fig. A.1 Circuit schematic for a symmetric two-junction SQUID.

Introduce the Lagrange multiplier α, where:

$$\tilde{I}_g = I_g + \alpha\phi_T = I_C(\sin\phi_1 + \sin\phi_2) + \alpha[\phi_1 - \phi_2 + 0.5\beta_L(\sin\phi_1 - \sin\phi_2)], \quad \text{(A.12)}$$

and eliminate the multiplier by taking partial derivative with respect to ϕ_1 and ϕ_2 to get

$$\frac{\partial\tilde{I}_g}{\partial\theta_1} = I_C\cos\phi_1 + \alpha(1 + 0.5\beta_L\cos\phi_1) = 0 \quad \text{(A.13)}$$

$$\frac{\partial\tilde{I}_g}{\partial\theta_2} = I_C\cos\phi_2 - \alpha(1 + 0.5\beta_L\cos\phi_2) = 0 \quad \text{(A.14)}$$

From Eqs. (A.13) and (A.14),

$$\alpha = \frac{I_C \cos\phi_1}{1 + 0.5\beta_L \cos\phi_1} = -\frac{I_C \cos\phi_2}{1 + 0.5\beta_L \cos\phi_2} \tag{A.15}$$

As a result,

$$\frac{1}{\cos\phi_1} + \frac{1}{\cos\phi_2} + \beta_L = 0 \tag{A.16}$$

Notice that this is exactly the same result obtained for Eq. (A.7) earlier if the two-junction SQUID is set to be symmetric, ie. if $L_1 = L_2 = L/2$ and $I_{c1} = I_{c2} = I_c$.

APPENDIX B: PERFORMANCE EVALUATION OF HIGH-SPEED ADCS

There are many different sources of error in an ADC. The most prominent include quantization error which is intrinsic to any ADC, harmonic distortion caused by nonlinearities in the ADC, and additive thermal noise. The output data of a converter can be acquired and evaluated in many different ways. Depending on each application, some particular tests and parameters may be more important or preferred to the others. As examples, for high-resolution ADCs used in instrumentation, where the quantities to be measured are the differential nonlinearity and integral nonlinearity, the so-called "code density" test is a good choice. On the other hand, for flash ADCs used in military or radar receivers, where the parameters of utmost interest are harmonic distortion and signal-to-noise ratio, it would be the most appropriate to perform the test in the frequency domain and to calculate the fast Fourier Transform (FFT) for the output signal.

B.1 Reconstruction and Fitting

Typically, the measured digital outputs of an ADC are reconstructed by using either appropriate digital-to-analog converters or computer programs that map each digital output to its corresponding analog value. Appendix C.4 lists the C program we have written to do the reconstruction. The reconstructed data was fitted with the sinusoidal

curve that gives the least root mean square error. Errors are detected by deviations from a smooth sinusoidal output waveform, missing codes appear as discontinuities in the sine wave, and oversize codes are observed as widening the individual codes.

A sine-wave fitting algorithm that recursively calculates the amplitude, offset and phase of an ideal sine wave that best fits the reconstructed data is described by Demler in [75], and the C program we have written to implement the algorithm is shown in Appendix C.5.

Once the output signal is reconstructed and fitted, the dynamic-quantization error plot can be obtained by subtracting the fitted sine wave from the reconstructed signal. the signal-to-noise ratio SNR (in dB) can be obtained by calculating the ratio of the root-mean-squares (RMS) of the signal $S_{s,rms}$ and of the noise $S_{n,rms}$ as follows [75].

$$SNR = 20\log\frac{S_{s,rms}}{S_{n,rms}} \tag{B.1}$$

In an ideal ADC with only quantization noise, for a full-scale sinusoidal input,

$$S_{s,rms} = \frac{2^N q}{2\sqrt{2}} \qquad S_{n,rms} = \frac{q}{\sqrt{12}} \tag{B.2}$$

where q is the quantization step, the signal-to-noise ratio SNR becomes

$$SNR\,(dB) = 6.02N + 1.76 \tag{B.3}$$

Dynamically, in the presence of noise and harmonic distortion, the effective bit resolution N_{eff} of the ADC becomes

$$N_{eff} = \frac{SNR\,[dB] - 1.76}{6.02} = \log_2 SNR - \frac{1}{2}\log_2 1.5 \qquad (B.4)$$

If the input signal amplitude S_{in} is smaller than the full scale level S_{FS}, a correction factor must be included [32]

$$N_{eff} = \frac{SNR\,[dB] - 1.76}{6.02} = \log_2 SNR - \frac{1}{2}\log_2 1.5 - \log_2 \frac{S_{in}}{S_{FS}} \qquad (B.5)$$

B.2 Code-Density Test

This test constructs a histogram of the digital output codes to measure and dynamically characterize the differential nonlinearity (DNL) and the integral nonlinearity (INL) of the ADC. A missing code would be represented by an output code with a code density of zero and an offset error would be seen as a shift in the code density.

The input for a code-density test can be either a ramp or a sine wave. A ramping input would result in equal number of samples per output code; however, it would require an ultra-linear ramp generator since even a small error would quickly accumulate and make it impossible to measure the integral nonlinearity. On the other hand, for a sinusoidal input, oscillators with very low distortion can be used as the generator, and the code densities for all output codes can be calculated precisely although they are no longer equal [76] [77]. To cover all possible output codes without accumulating large differential nonlinearity, the sinusoidal input should be selected so that the clock frequency is non-harmonically related to the input frequency.

The disadvantages of this test is that a large number of samples required for an accurate measurement of INL. If the testing time is too long, the amplitude of the test signal may drift, which may significantly affect the INL.

B.3 Signal-To-Noise Ratio Test

A signal-to-noise-ratio (SNR) test can be used to obtain the fast Fourier transform (FFT) and power spectrum of the ADC output, which then are used to calculate the signal-to-noise ratio SNR and the effective bit resolution N_{eff}.

The spectral power is calculated as the sum of squares of the real and imaginary parts of the complex FFT results. The signal energy of the fundamental component is the integral of the spectral power over the FFT bins around the fundamental peak, and the noise and harmonic distortion energy is the integral of all other bins. The signal-to-noise ratio SNR is obtained as the square root of the ratio of the fundamental over the noise and distortion [75].

Typically, the SNR is measured as a function of input amplitude and reported with a quantization noise plot. In order to achieve meaningful results, it is important to select the input frequency which is subharmonically related to the clock frequency. Because the number of samples required for this test is much smaller than that required for a code-density test, a signal-to-noise-ratio test does not suffer from the amplitude-drift problem associated with a code-density test and thus can measure the quantization noise and distortion more accurately and in a shorter period of time.

Disadvantageously, no specific nonlinearity measurements can be obtained directly with a SNR test. In addition, the test is very sensitive to frequency drift in the

input and clock signals as well as the clock jitter. As a result, a good test setup is necessary to carry out the test effectively.

B.4 ADC's Jitter Effect

The performance of an ADC can be significantly reduced if the clock jitter is too large. In this section, we will show how jitter affects the signal-to-noise ratio and the effective bit resolution.

Assume that jitter has a Gaussian probability density function $p(\tau)$ with a standard deviation σ, that is:

$$p(\tau) = \frac{1}{\sqrt{2\pi}\sigma}\exp\left(-\frac{\tau^2}{2\sigma^2}\right) \tag{B.6}$$

For a sinusoidal input signal, $S(t) = A\sin(2\pi ft)$, the RMS value of the conversion error due to the jitter E_{jrms} can be calculated as [78] [79]:

$$E_{jrms}^2 = \frac{1}{T}\int_0^T \left(\frac{\partial S(t)}{\partial t}\left[\int_{-\infty}^{\infty}|\tau|p(\tau)\,d\tau\right]\right)^2 dt = 4\pi(Af\sigma)^2 \tag{B.7}$$

Since the quantization error E_{qrms} is given by:

$$E_{qrms} = \frac{A}{2^N\sqrt{3}} \tag{B.8}$$

the signal-to-noise ratio SNR becomes:

$$SNR = 20\log\left[\frac{A/(\sqrt{2})}{\sqrt{E_{jrms}^2 + E_{qrms}^2}}\right] = 20\log\left[\frac{1}{\sqrt{(\sqrt{8\pi}f\sigma)^2 + (2^N\sqrt{1.5})^2}}\right] \tag{B.9}$$

and the effective bit resolution N_{eff} becomes:

$$N_{eff} = N - \frac{1}{2}\ln\{1 + \frac{E_{jrms}^2}{E_{qrms}^2}\} = N - \frac{1}{2}\ln\{1 + [\sqrt{12\pi}f\sigma 2^N]^2\} \qquad (B.10)$$

From Eqs. (B.9) and (B.10), it is clear that the jitter error can be neglected if the following condition is met:

$$E_{jrms} \ll E_{qrms}$$
$$\sigma \ll \frac{0.16}{2^N f} \qquad (B.11)$$

For our converter prototype, where f = 5 GHz, N = 4, the standard deviation of the jitter must be less than 2 ps.

In practice, the timing jitter of an ADC can be measured by splitting the clock signal and applying one of the split signals to the ADC input through a variable delay line. By continuously varying the delay until the outputs change, the timing jitter can be estimated.

APPENDIX C: C PROGRAMS FOR LAYOUT GENERATION & DATA ANALYSIS

Layout for many subcells, including junctions and resistors, can be automatically generated using simple C programs. Of particular interest is a program to generate sinusoidal-shaped junctions since it can be easily modified for other nonrectangular junctions. All programs have been written for various processes and technologies, including those from Berkeley, Hypres, and TRW. All source codes are available in /home/swordfish/hoaluong/Programs/C and executable files are in /home/swordfish/hoaluong/bin.

As reference, shown below are simple programs we have used to generate rectangular junctions, sinusoidal-shaped junctions, and resistors. In addition, included are C programs that have been used for data acquisition and testing of a converter. More specifically, the first program is used to reconstruct the acquired data for either a three-bit or four-bit analog-to-digital converters, and the second program is used to find the best fitting sinusoidal curves for a set of data.

C.1 Program For Rectangular Junction Layouts

```
/* This is to generate a rectangular junction for Berkeley's process. For JC, the JJ value is recalculated
and subtracted from the minimum spacing 1um.
*/
```

```
#include <math.h>
#include <stdio.h>
#define SPACEJJJC 1 /* UCB design rules (in um) */
#define SPACEMBJJ 3 /* in um */

main(int argc, char *argv[])
{
FILE *infile, *out, *area;
int jjlength, jjwidth, spacejjjc, spacembjj;
float WIDTH, LENGTH, LAMBDA;

if(argc<2) {
        fprintf(stderr,"usage: jj outputfile\n");
 exit(1);
 }
if((out=fopen(argv[1],"w"))==NULL) {
        fprintf(stderr, "could not open output file\n");
 exit(2);
 }
printf("Enter the length, width, and LAMBDA: \n");
scanf("%f %f %f", &LENGTH, &WIDTH, &LAMBDA); /*read in LENGTH and WIDTH*/
jjlength = LENGTH / LAMBDA; /* 1 magic unit = 0.2um */
jjwidth = WIDTH / LAMBDA; /* 1 magic unit = 0.2um */
 spacejjjc = SPACEJJJC / LAMBDA;
 spacembjj = SPACEMBJJ / LAMBDA;

 fprintf(out,"magic\n"); /*write MAGIC header - using jjnb technology file*/
 fprintf(out,"tech jjnb\n");
 fprintf(out,"timestamp 720703502\n");

 fprintf(out,"<< JJ >>\n");
fprintf(out, "rect %d %d %d %d\n", 0, 0, jjlength, jjwidth);

 fprintf(out,"<< JC >>\n");
fprintf(out, "rect %d %d %d %d\n", spacejjjc, spacejjjc, jjlength-spacejjjc, jjwidth-spacejjjc);

 fprintf(out,"<< MB >>\n");
fprintf(out, "rect %d %d %d %d\n", -spacembjj, -spacembjj, jjlength+spacembjj, jjwidth+spacembjj);
```

```
fprintf(out,"<< MC >>\n");
fprintf(out, "rect %d %d %d %d\n", -spacembjj, -spacembjj, jjlength+spacembjj, jjwidth+spacembjj);

fprintf(out,"<< end >>\n");

fclose(out);
}
```

C.2 Program For Sinusoidal-Shaped Junction Layouts

```
/* This is to generate a sine-shaped junction.The corners are filled up by the averaged value of the 2
adjacent values.The total area is also calculated and stored in the file called "area"*/

#include <math.h>
#include <stdio.h>

#define SPACEMBJJ 3 /* in um */
#define SPACEJJJC 1 /* in um */
#define WIDTHJJ 3 /* in um */

main(int argc, char *argv[])
{

FILE*infile, *out, *area;
int i, j, k, m, n, p, prej, jjlength;
int nwidthjj, nspacejjjc; /* nwidthjj = normal jj width */
int jjamp, mbamp, count, jjstart, jjactleng, spacembjj;
float pi, WIDTH, LAMBDA, LENGTH, rawarea, truncarea;

pi = 3.1415927;
rawarea = 0;
truncarea = 0;

if(argc<2) {
        fprintf(stderr,"usage: sinjj outputfile\n");
        exit(1);
        }

if((out=fopen(argv[1],"w"))==NULL) {
```

```
        fprintf(stderr, "could not open output file\n");
        exit(2);
        }

if((area=fopen("area","w"))==NULL) {
        fprintf(stderr, "could not open area file\n");
        exit(2);
        }

printf("Enter the length, width, and lambda (in micron): \n");
scanf("%f %f %f", &LENGTH, &WIDTH, &LAMBDA); /*read in LENGTH, WIDTH, LAMBDA*/

jjlength = LENGTH / LAMBDA ;/* 1 magic unit = 0.2um */
jjamp = WIDTH / (2 * LAMBDA) ;/* 1 magic unit = 0.2um and double */
spacembjj = SPACEMBJJ / LAMBDA;
mbamp = jjamp + spacembjj;/* 1um spacing between jj and mb */

fprintf(out,"magic\n");/*write MAGIC header - using jjnb technology file*/
fprintf(out,"tech jjnb\n");
fprintf(out,"timestamp 720703502\n");

fprintf(out,"<< JJ >>\n");
prej = 0;
jjactleng = 0;/* actual laid-out length for JJ */
jjstart = 0;
nwidthjj = WIDTHJJ / LAMBDA;
nspacejjjc = SPACEJJJC / LAMBDA;

for (i=0; i<jjlength/2 ; i++) /* starting from 3um away from MB edge */
        {
        m=2*i; /* 2*i for offset */
        j= jjamp * sin((pi*i)/(jjlength/2)) + 0.5;
        if (j> nwidthjj/2 && prej==0)
                k = j;
        else
                k=(j+prej)/2;
        if (k > nwidthjj/2 ) {/*minimum dimension for jj is WIDTHJJ*/
                fprintf(out, "rect %d %d %d %d\n", m, -k, m+1, k); /* to fill up the corners by averaging
                        the 2 adjacent values */
                rawarea = rawarea + 2 * k * LAMBDA * LAMBDA; /* 0.04 is the normalizing factor */
                jjactleng++;
                if (j >nwidthjj/2) { /* minimum dimension for jj is 3 um = 15 units */
```

```
                fprintf(out, "rect %d %d %d %d\n", m+1, -j, m+2, j);
                rawarea = rawarea + 2 * j * LAMBDA * LAMBDA; /* 0.04 is the normalizing
                        factor */
                jjactleng++;
                }
            }
        else if (k<nwidthjj/2 && jjactleng == 0) {
            jjstart = jjstart + 2;
            truncarea = truncarea + 2 * k * LAMBDA * LAMBDA;
            }
        prej = j; /* store the current value for averaging in next step */
        }

/* write data into the file "area" */
fprintf(area,"Sine-shaped junction:\n\n");
fprintf(area,"Length (um) : %d\n", LENGTH);
fprintf(area,"Width (um) : %f\n", WIDTH);
fprintf(area,"Total area (um2) : %f\n", rawarea);
fprintf(area,"Total truncated area (um2) : %f\n", truncarea);
fprintf(area,"Percentage total area truncated (um2) : %f\n", truncarea/rawarea);

fprintf(out,"<< JC >>\n");
prej = 0;
count = 0;
m=(jjstart+4);

for (i=0; i<jjlength/2 ; i++) /* starting from 3um away from MB edge */
        {
        m=2*i; /* 2*i for offset */
        j= jjamp * sin((pi*i)/(jjlength/2)) + 0.5;
        if (j>nwidthjj/2 && prej==0)
                k = j;
        else
                k=(j+prej)/2;
        if (k >nwidthjj/2 ) {/*minimum dimension for jj is nwidthjj units */
                if (++count>2 && m<jjstart+jjactleng) {
                        fprintf(out, "rect %d %d %d %d\n", m, -k+nspacejjjc, m+1, k-nspacejjjc);
                        if (j >nwidthjj/2)/* minimum dimension for jj is nwidthjj units */
                                fprintf(out, "rect %d %d %d %d\n", m+1, -j+nspacejjjc, m+2, j-nspacejjjc);
                                }
                        }
        prej = j; /* store the current value for averaging in next step */
        }
```

```
fprintf(out,"<< MB >>\n");
fprintf(out, "rect %d %d %d %d\n", jjstart-spacembjj+2, -mbamp, jjstart+jjactleng+spacembjj+4,
mbamp);

fprintf(out,"<< MC >>\n");
fprintf(out, "rect %d %d %d %d\n", jjstart-spacembjj+2, -mbamp, jjstart+jjactleng+spacembjj+4,
 mbamp);

fprintf(out,"<< end >>\n");

fclose(area);
fclose(out);
}
```

C.3 Program For Resistor Layouts

```
/* This is to generate a resistor with MB-MC contacts at the 2 ends
 Howard, 12/92.
*/
#include <math.h>
#include <stdio.h>
#define WIDTHRC 15
#define SPACEMBRC 5

main(int argc, char *argv[])
{
FILE*infile, *out, *area;
int length, width;
float WIDTH, LENGTH;

if(argc<2) {
        fprintf(stderr,"usage: jj outputfile\n");
        exit(1);
        }

if((out=fopen(argv[1],"w"))==NULL) {
       fprintf(stderr, "could not open output file\n");
       exit(2);
       }
```

```
printf("Enter the length and width (at least 3): \n");
scanf("%f %f", &LENGTH, &WIDTH); /*read in LENGTH and WIDTH*/

length = LENGTH * 5;/* 1 magic unit = 0.2um */
width = WIDTH * 5;/* 1 magic unit = 0.2um */

fprintf(out,"magic\n");/*write MAGIC header - using jjnb technology file*/
fprintf(out,"tech jjnb\n");
fprintf(out,"timestamp 720703502\n");

fprintf(out,"<< MR >>\n");
fprintf(out, "rect %d %d %d %d\n", 0, 0, length+2*WIDTHRC, width);

fprintf(out,"<< RC >>\n");
fprintf(out, "rect %d %d %d %d\n", 0, -5, WIDTHRC, width+5);
fprintf(out, "rect %d %d %d %d\n", length+WIDTHRC, -5, length+2*WIDTHRC, width+5);

fprintf(out,"<< MB >>\n");
fprintf(out, "rect %d %d %d %d\n", -5, -10, WIDTHRC+5, width+10);
fprintf(out, "rect %d %d %d %d\n", length+WIDTHRC-5, -10, length+2*WIDTHRC+5, width+10);

fprintf(out,"<< end >>\n");

fclose(out);
}
```

C.4 Program For ADC'S Data Reconstruction

```
/* This program is used to automatically select and null out the low outputs from the JSIM simulation of
a 4-bit adc (with the higher significant bits coming before the lower, ie. MSB, .., LSB) and then
automatically calculate and generate the reconstructed signal. Moreover, it removes all the zeros
between the samples The bit resolution, frequency and stepsize are specified by the user.
*/

/* Main Deck */
#include <stdio.h>
#define DELAY 2e-9
#define DURATION 0.2e-9
```

```
main(int argc, char *argv[])
{
int count, totalcount, modcount;
int fs, stepsize, numberPerSample, numberBits;
double v751, v761, v771, v781;
double vout, time;
FILE *fp, *fout, *fopen();

if(argc<3) {
        fprintf(stderr,"usage: reconst input output \n");
        exit(1);
        }

if((fp=fopen(argv[1],"r"))==NULL) {
        fprintf(stderr, "could not open input file\n");
        exit(2);
        }

if((fout=fopen(argv[2],"w"))==NULL) {
        fprintf(stderr, "could not open output file\n");
        exit(2);
        }

vout = 0;
v751 = 0;
v761 = 0;
v771 = 0;
count = 0;
totalcount = 0;
printf("Enter the number of bits for the ADC:\n");
scanf("%d", &numberBits);
printf("Enter the clock frequency (GHz) and the stepsize (ps) used in simulation:\n");
scanf("%d %d", &fs, &stepsize);
numberPerSample = 1000/(stepsize*fs);
if (numberBits == 3) {
        while(fscanf(fp, "%lf %lf %lf %lf", &time, &v751, &v761, &v771) != EOF) {
        if ( time >= DELAY + DURATION/2 ) {
                count ++;
                modcount = count - ( count/numberPerSample )* numberPerSample;
                if ( modcount == 0 ) {
                        vout=0;
```

```
                    if (v751 > 0.7e-3)
                        vout += 1;
                    if (v761 > 0.7e-3)
                        vout += 2;
                    if (v771 > 0.7e-3)
                        vout += 4;
                    totalcount ++;
                    fprintf(fout, "%d %g\n", totalcount, vout);
                    }
                }
            }
        }

    if (numberBits == 4) {
        while(fscanf(fp, "%lf %lf %lf %lf %lf", &time, &v781, &v771, &v761, &v751) != EOF) {
        if ( time >= DELAY + DURATION/2 ) {
            count ++;
            modcount = count - ( count/numberPerSample )* numberPerSample;
            if ( modcount == 10 ) {
                vout=0;
                if (v751 > 0.7e-3)
                    vout += 1;
                if (v761 > 0.7e-3)
                    vout += 2;
                if (v771 > 0.7e-3)
                    vout += 4;
                if (v781 > 0.7e-3)
                    vout += 8;
                totalcount ++;
                fprintf(fout, "%d %g\n", totalcount, vout);
                }
            }
        }
    }

    fclose(fp);
    fclose(fout);
    }
```

C.5 Program For Calculation Of The Best Fitting Sine Curve

/* This program is used to implement an algorithm to calculate the best-fit sine wave, described in Demler [75], pp 176-179. Given the input frequency and the sampling interval, it estimates the

```
amplitude, phase, and offset and put in a file specified on the command line. The data are reconstructed
from output of ADC's and are normalized.
*/

/* Main Deck */
#include <stdio.h>
#include <math.h>
#define PI 3.1415927

main(int argc, char *argv[])
{
int i, count;
double fin, ts, normfin, vref;
double s1, s2, s3, s4, s5;
double s6, s7, s8, s9;
double Error1, Error2, Error3, ErrorRMS, Error, Neff;
double An, Ad, Bn, Bd, A, B, C;
double meany, meanAlpha, meanBeta, yn, ynprime;
FILE *fp, *fout, *fout2, *fopen();

if(argc<4) {
        fprintf(stderr,"usage: reconst input output output2 \n");
        exit(1);
        }

if((fp=fopen(argv[1],"r"))==NULL) {
        fprintf(stderr, "could not open input file\n");
        exit(2);
        }

if((fout=fopen(argv[2],"w"))==NULL) {
        fprintf(stderr, "could not open first output file\n");
        exit(2);
        }

if((fout2=fopen(argv[3],"w"))==NULL) {
        fprintf(stderr, "could not open second output file\n");
        exit(2);
        }

count = 0;
```

```
s1 = 0;
s2 = 0;
s3 = 0;
s4 = 0;
s5 = 0;
s6 = 0;
s7 = 0;
s8 = 0;
s9 = 0;
printf("Enter the input frequency (MHz) and the sampling interval (ps):\n");
printf("(fin * ts should be 1/period, ie. 2 and 10 for a period of 50)\n");
scanf("%lf %lf", &fin, &ts);
printf("Enter the normalized reference voltage (for SNR calculation):\n");
scanf("%lf", &vref);
normfin = 2 * PI * fin * ts * 0.001; /* normalized input angular frequency */
while(fscanf(fp, "%lf", &yn) != EOF){
        count ++;
        s1 += yn;
        s2 += cos(normfin * count);
        s3 += sin(normfin * count);
        s4 += cos(normfin * count) * sin(normfin * count);
        s5 += cos(normfin * count) * cos(normfin * count);
        s6 += sin(normfin * count) * sin(normfin * count);
        s7 += yn * cos(normfin * count);
        s8 += yn * sin(normfin * count);
        s9 += yn * yn;
}
meany = s1 / count;
meanAlpha = s2 / count;
meanBeta = s3 / count;
An = (s7 - meany * s2)/(s4 - meanBeta * s2) - (s8 - meany * s3)/(s6 - meanBeta * s3);
Ad = (s5 - meanAlpha * s2)/(s4 - meanBeta * s2) - (s4 - meanAlpha * s3)/(s6 - meanBeta * s3);
Bn = (s7 - meany * s2)/(s5 - meanAlpha * s2) - (s8 - meany * s3)/(s4 - meanAlpha * s3);
Bd = (s4 - meanBeta * s2)/(s5 - meanAlpha * s2) - (s6 - meanBeta * s3)/(s4 - meanAlpha * s3);
A = An / Ad;
B = Bn / Bd;
C = meany - A * meanAlpha - B * meanBeta;
Error1 = s9 + A * A * s5 + B * B * s6 + C * C * count;
Error2 = A * s7 + B * s8 + C * s1;
Error3 = A * B * s4 + A * C * s2 + B * C * s3;
Error = Error1 - 2 * Error2 + 2 * Error3;
```

```
ErrorRMS = sqrt( Error/count);
Neff = log(vref/sqrt((double)12)/ErrorRMS) / log((double)2); /* REF = vref */
fprintf(fout2, "Number of samples: %d\n", count);
fprintf(fout2, "Input frequency: %g GHz\n", fin);
fprintf(fout2, "Sampling interval ts: %g ps\n", ts);
fprintf(fout2, "Estimate for A (cosine coefficient): %g\n", A);
fprintf(fout2, "Estimate for B (sine coefficient): %g\n", B);
fprintf(fout2, "Estimate for C (dc offset): %g\n", C);
fprintf(fout2, "Estimate for Error (error): %g\n", Error);
fprintf(fout2, "Estimate for ErrorRMS (RMS error): %g\n", ErrorRMS);
fprintf(fout2, "Effective number of bits of resolution (Neff): %g\n", Neff);
for (i=1; i<=count; i++) {
        ynprime = A * cos(normfin * i) + B * sin(normfin * i) + C;
        fprintf(fout, "%d %g\n", i, ynprime);
        }
fclose(fp);
fclose(fout);
fclose(fout2);
}
```

APPENDIX D: SETUP AND DESIGN FOR THE DEGAUSSER

This section describes our design and implementation of a test setup to generate appropriate magnetic field to demagnetize the shields prior to each testing. The test setup is shown in Fig. D.1, where a current from current source is passed through a coil and

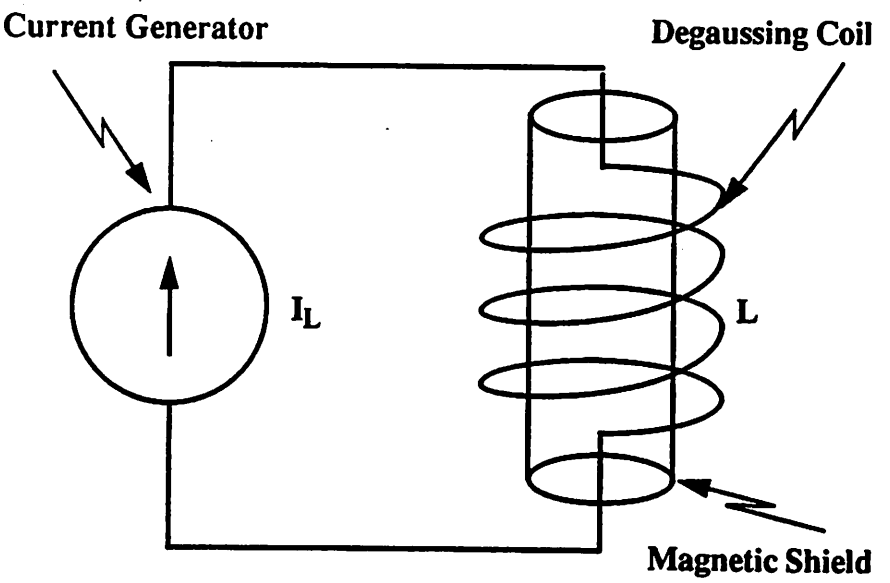

Fig. D.1 Test setup for our degausser to demagnetize the shield prior to testing.

generates enough magnetic field to demagnetize the shield when inserted inside the coil. We will show how to determine the frequency and the amplitude of the current required to generate a desired field and how to design and build a circuit to generate such a current.

It has been found by experiments that it is the most effective to use an exponentially decaying sinusoidal signal at a frequency of approximately 6-8 cycles/s and a minimum saturating field of 10 AT/cm to degauss magnetic shields [80]. The reason for a choice of such a low frequency is that if the frequency is much higher, the skin effect becomes significantly large.

Before calculating the current required to generate the desired saturating field, we need to figure out the inductance of our degaussing coil. According to Wheeler [81], the inductance of a coil L with a length $l > 0.8R$ is:

$$L = \frac{\pi\mu R^2 N^2}{1 + 0.9N} \tag{D.1}$$

where R is the radius of the cross section in meters and N is the total number of turns.

For our degaussing coil, l = 6 inches, R = 0.6875 inches, N = 540 turns, and therefore L = 2.08 mH. To double check this theoretical calculation, we have conducted direct measurements by applying an ac voltage source across the coil and measuring the current flowing in the coil. At a frequency of 10 kHz, V_L = 6.37 V, we measured a current of I_L = 43 mA, translating to an inductance of L = 2.36 mH, which checks out very closely with the calculated value above.

Knowing the inductance of the coil, we are ready to calculate how the flux generated by the coil is related to the current flowing through the coil. Theoretically, for a solenoid, the flux linkage is:

$$\Psi_m = N\oint B \cdot ds = N\pi R^2 \mu H_z = LI \tag{D.2}$$

It follows that:

$$H_z = \frac{LI}{N\pi R^2 \mu} = \frac{NI}{1+0.9N} = 32.12 \cdot I\,[AT/cm] \tag{D.3}$$

According to this relationship, for a magnetic flux of H_z = 10AT/cm, we need a current of approximately 300 mA

Our degaussing coil uses No. 30 enameled wire and has a total of 540 turns in a length of 6 inches, which is equivalent to 35 turns/cm or 90 turns/inch. Since degaussing requires a saturating field of 10 AT/cm, we would need a current I_L of 10 AT/35T = 300 mA, which is exactly the same amount of current we calculated above.

The simplest and most feasible way to generate an exponentially decaying sinusoidal signal for an inductive coil is to connect several operational amplifiers in a feedback configuration to implement a second-order underdamped RLC circuit. Figure D.2 shows a complete circuit schematic of such a circuit, which has been built, tested, and used successfully.

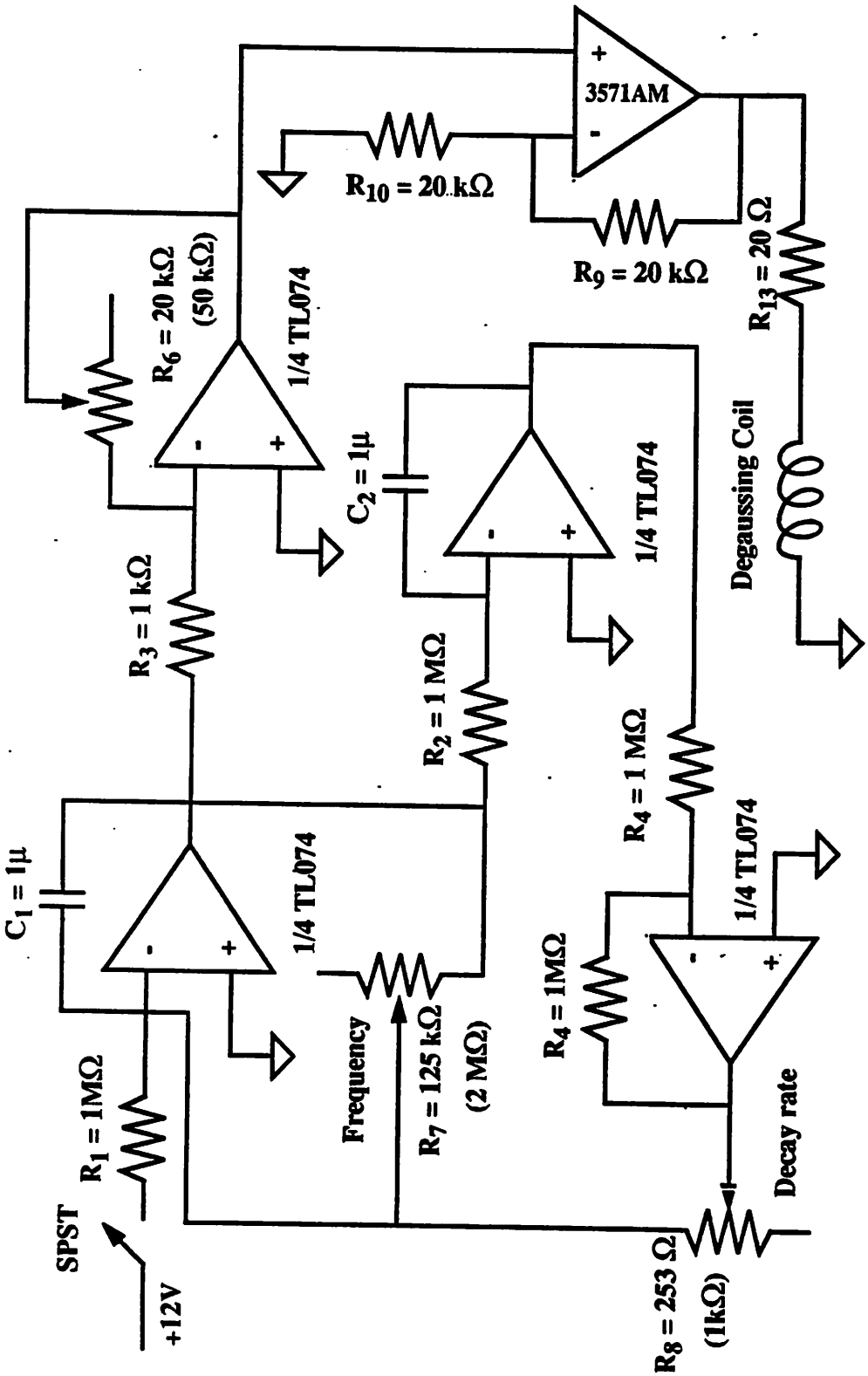

Fig. D.2 Second-order RLC circuit to generate an exponentially decaying sinusoidal signal for the degausser.