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New Approaches for On-Chip Power Switching Noise Reduction*

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The effect of power supply switching noise is gaining importance with increasing switching speeds and density of VLSI chips. Yet, today's design methodology does not adequately address this problem at chip level. This paper proposes two approaches for on-chip power switching noise reduction. The first approach aims at reducing Delta-I noise by inserting decoupling capacitors in an optimized manner. The second approach reduces the switching noise by wire-sizing power bus segments near each power pin. Both approaches are assessed by simulation of a circuit, in which power supply rails are modeled as lossy transmission lines. The results of the simulated example demonstrate the effectiveness of our approaches.

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1 Introduction

The current trend in VLSI sub-micron technology leads to the continuous increase in chip size and decrease in feature size of the interconnect. This trend results in longer paths from power source to sinks, higher peak current, smaller power supply level, and smaller wire spacing combined with higher switching frequency. These effects can cause severe power supply noise in today's high performance design. In particular, the switching noise which traditionally occurs only at packaging level, must now be addressed properly at on-chip level. The switching noise is caused by switching current through transmission line effect of the power bus. It may cause severe power supply voltage variations, which are responsible for extra delay and the corruption of data transmissions.

Presently, decoupling capacitors are added by designers so as to reduce the Delta-I noise, but without help of any optimization techniques. This type of conventional approaches to ensuring signal integrity is becoming not only ineffective but also costly. For instance, manually added decoupling capacitors reportedly occupy as much as 10% of the chip area in some known designs. A comprehensive and rigorous treatment of power switching noise at on-chip level is much needed in today's design flow. To this end, this paper presents two approaches for on-chip switching noise minimization.

Our first algorithm concentrates on reducing simultaneous switching noise by optimizing decoupling capacitors. Decoupling capacitor placement is formulated as an optimization problem and solved via nonlinear programming. This approach requires an accurate sensitivity analysis of noise with respect to decoupling capacitors as well as an efficient nonlinear programming technique. The sensitivity analysis and optimization methods have been implemented on the circuit simulator SWEC [1] to solve the decoupling capacitor placement problem. The program exploits the accuracy and efficiency of SWEC, while interactively guiding the designer for adequate decoupling capacitor selections. It is appropriate for design of a macro block.

Our second approach achieves noise minimization by power bus wiresizing. We model each power supply wire as a uniform transmission line and switching current as an independent current source. Since the amplitude of the noise at power pin is inversely proportional to the width of the transmission line, the switching noise can be effectively reduced by wiresizing the line segment near each power pin. The length of wiresizing segment must be over a

certain threshold value in order to avoid overlapping between the noise and its reflection waveform. As only a small portion of the power bus needs to be wiresized, the routing resource for signal nets is not affected. We use SWEC to test the effectiveness of the second method.

In Sections 2 and 3, the first and second approaches are discussed. In Section 4, experimental results of noise reduction are presented.

2 Noise Reduction via Optimization of Decoupling Capacitors

The first approach for noise reduction involves a placement of decoupling capacitors. First the design is represented as a transistor-level circuit, with power buses modeled as lossy transmission lines. Then, the noise-variation-to-decoupling-capacitor sensitivity is calculated for each node of interest, in conjunction with a transient analysis of the circuit. For each simulation run, the value of the objective function and its gradient with respect to the decoupling capacitor values are obtained. At the end of a simulation run, we revise the solution vector (decoupling capacitor vector) along the current gradient and repeat the cycle. This cycle of a simulation and a sensitivity analysis is iterated until the gradient reaches zero. We then determine the location and exact size of each decoupling capacitor based on the values of the solution vector of the last iteration. The sensitivity formulation is described in Section 2.1, and the optimization algorithm is explained in Section 2.2.

2.1 Sensitivity Analysis

Our transient sensitivity analysis is based on the direct differentiation method. It is performed in conjunction with a transient simulation of the circuit. The KCL equation of a no-inductor circuit in its general form is

$$G(t)v(t) + C\dot{v}(t) = I(t)$$

where $G(t)$ is a linear time-varying admittance matrix and $I(t)$ is the vector of independent current sources. The integration of $v(t)$ is performed according to the following system.

$$(G + \frac{2}{h_n}C)v_n = I_n + \frac{2}{h_n}Cv_{n-1} + C\dot{v}_{n-1}$$

where h_n and v_n denote n^{th} time step and voltage values, respectively. The sensitivity of a node voltage v with respect to a decoupling capacitor p at n^{th} time step, denoted as ${s_{vp}}^{(n)}$, can be obtained by directly differentiating the above system.

$${s_{vp}}^{(n)} = (G + \frac{2}{h_n}C)^{-1}(\frac{2}{h_n}C{s_{vp}}^{(n-1)} + C\dot{s}_{vp}^{(n-1)} - \frac{\partial f}{\partial p})$$

where

$$\frac{\partial f}{\partial p} = \frac{2}{h_n} C(v^{(n)} - v^{(n-1)}) - v^{(n-1)} + \frac{\partial G}{\partial p} v^{(n)} + \frac{\partial I_n}{\partial p}$$

Transient sensitivity analysis involves solving a sensitivity matrix whose dimension is same as the circuit matrix, with identical right-hand-side vector.

2.2 Optimization Algorithm

The objective function of the optimization problem is constructed as a weighted sum of various constraints. To minimize the total decoupling capacitance and total noise levels, the objective function is expressed as

$$f(C, V) = \alpha \sum_{i=1}^{N} V_i + \beta \sum_{i=1}^{N} C_i, \tag{1}$$

where α and β are weight constants and N is the number of nodes on p/g rail. V_i and C_i are the peak noise and decoupling capacitor at node i. The constraints can be generally expressed as:

$$\sum_{i=1}^{N} C_i \leq K, \;\; 0 \leq C_i \leq K_c, \;\; 0 \leq V_i \leq K_v$$

where K, K_c, and K_v are upper bounds for sum of capacitors, individual capacitor, and noise level of each node, respectively. To solve this optimization problem, we use a variation of the nonlinear programming algorithm in [2]. In short, we start with an initial solution vector $\hat{p}$ and iteratively improve the value of the objective function $f(\hat{p})$ by moving the solution vector along the direction of the gradient. The iterations stop when the gradient is near zero. The following steps are iterated until a local optimum is obtained.

1. Begin with initial solution vector $\hat{p}$ and $f(\hat{p})$
2. At each iteration $f(\hat{p} - k\nabla f(\hat{p}))$ is calculated. If $f(\hat{p} - k\nabla f(\hat{p})) < f(\hat{p})$, then $\hat{p} - k\nabla f(\hat{p})$ becomes the new solution vector.
3. Repeat step 2 until the stopping criterion is met.

k is a scalar constant which exponentially decreases at each iteration. The noise reduction result of the decoupling capacitor placement using this optimization scheme is quite promising. It is given in Section 4.

3 Noise Reduction via Power Bus Wiresizing

The power switching noise is triggered by the transmission line effect of the power bus. As the R, L, C values of the power bus are functions of its width and length, the switching noise can be reduced by adjusting the physical parameters of the bus. Since the length of power bus segments between the power pad of the chip and power pin on each macro is fixed under a given floorplan, we develop the second approach for switching noise minimization via power bus wiresizing.

3.1 Problem Formulation

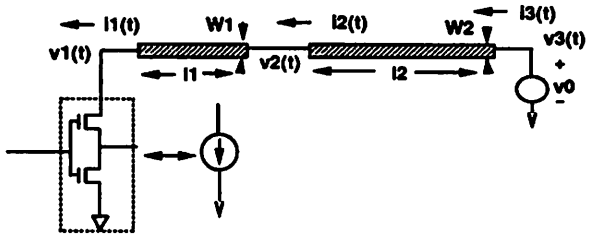


Fig. 1 Power Bus Modeling

The power bus between power pin 1 on macro cell and power source 3 with supply voltage v_0 is modeled as two cascaded uniform transmission lines with length l_1, l_2 and width W_1, W_2 respectively. The switching current of the macro cell is modeled as an independent current source $i_1(t)$ (Fig.1). R, L, C are parameters of a transmission line with $R = R_0/W, L = L_0/W$ and $C = C_0W$, where R_0, L_0, C_0 are unit parameters of transmission line with minimum width W_0.

3.2 Switching Noise Analysis

TheABCD matrix of a uniform transmission line can be obtained by solving the Laplace

transforms of its Telegraph Equations with $v(0^-) = v_0, i(0^-) = 0$.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \frac{1}{2} \begin{bmatrix} e^{\lambda l} + e^{-\lambda l} & \dfrac{(e^{-\lambda l} - e^{\lambda l})}{Y(s)} \\ (e^{-\lambda l} - e^{\lambda l})Y(s) & e^{\lambda l} + e^{-\lambda l} \end{bmatrix}$$

where $\lambda = \lambda(s) = \sqrt{(sL + R)sC}$, and
$Y(s) = Y_0(s)W = \sqrt{sC_0/(sL_0 + R_0)}W$
As $V_0 = V_3 = v_0/s$, the relation between V_1, I_1, I_3 can then be expressed as:

$$\begin{bmatrix} V_1 - V_0 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} B_2 \\ D_2 \end{bmatrix} I_3$$

The impact of W_1, W_2 on switching noise $v_1(t) - v_0$ is studied in the following cases, where the following definitions are used:
$V_{sn}(s) = V_1 - V_0/s$, $v_{sn}(t) = v_1(t) - v_0$ and
$h_0(t) = \mathcal{L}^{-1}(I_1(s)/Y_0(s))/W$.

Case 1. $W_1 = W_2$
As $W_1/W_2 = 1$, the two segments are equivalent to one uniform transmission line.

$$V_{sn}(s) = \frac{I_1}{Y_0(s)W_1} \left[\frac{e^{-\lambda(l_1+l_2)} - e^{\lambda(l_1+l_2)}}{e^{-\lambda(l_1+l_2)} + e^{\lambda(l_1+l_2)}} \right]$$

Switching noise $v_{sn}(t)$ in time domain can be expressed as:

$$v_{sn}(t) = -h_0(t) + 2\sum_{n=1}^{\infty}(-1)^{n+1}h_0(t - nT_1)e^{-d_1 n}$$

Here $T_1 = 2(l_1 + l_2)\sqrt{L_0C_0}$, $d_1 = (l_1 + l_2)R_0\sqrt{C_0/L_0}$.

Case 2. $W_1 = W$, $W_2 \to \infty$
As W_1/W_2 decreases from 1 to 0, the switching noise changes to:

$$V_{sn}(s) = \frac{I_1}{Y_0(s)W_1}\left[\frac{e^{-\lambda l_1} - e^{\lambda l_1}}{e^{-\lambda l_1} + e^{\lambda l_1}}\right]$$

$$v_{sn}(t) = -h_0(t) + 2\sum_{n=1}^{\infty}(-1)^{n+1}h_0(t - nT_2)e^{-d_2 n}$$

Here $T_2 = 2l_1\sqrt{L_0C_0}$, $d_2 = l_1R_0\sqrt{C_0/L_0}$.

The switching noise has the same waveform pattern but with a higher frequency compared with Case 1 (Fig. 2).

Case 3. $W_1 = W$, $W_2 \to 0$

As W_1/W_2 increases from 1 to ∞, the noise becomes:

$$V_{sn}(s) = \frac{I_1}{Y_0(s)W_1}\left[\frac{e^{-\lambda l_1} + e^{\lambda l_1}}{e^{-\lambda l_1} - e^{\lambda l_1}}\right]$$

$$v_{sn}(t) = -h_0(t) - 2\sum_{n=1}^{\infty}h_0(t - nT_2)e^{-d_2 n}$$

The frequency of $v_{sn}(t)$ is also higher than Case 1, and each pulse is negative (Fig. 3).

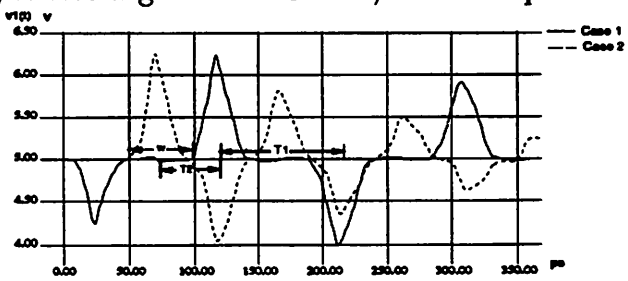


Fig. 2 Switching Noise $v_{sn}(t)$ (Case 1 and 2)

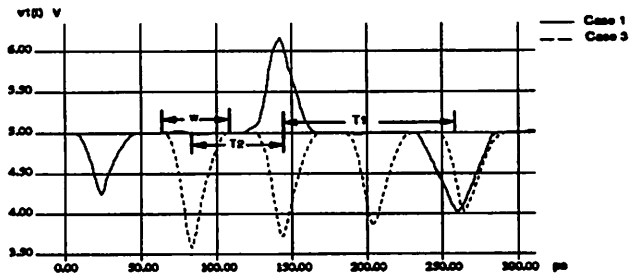


Fig. 3 Switching Noise $v_{sn}(t)$ (Case 1 and 3)

It can be observed from analysis above that:
1.The amplitude of switching noise, $|v_{sn}(t)|$, can be significantly reduced by increasing W_1, as the amplitude of pulse $|h_0(t)|$ is inverse proportional to W_1.
2. W_2 does not affect $|h_0(t)|$, but W_1/W_2 determines the frequency of the waveform.

3.3 Switching Noise Estimation

If l_1 is too short, $T_2 = 2l_1\sqrt{L_0C_0}$ may become less than the width of pulse $h_0(t)$, w, and result in overlapping of adjacent pulses which may increase the noise amplitude $|v_{sn}(t)|$ in Case 3 above. The threshold for l_1, l_{Th}, can be calculated as: $l_{Th} = w/(2\sqrt{L_0C_0})$.

3.3.1 Noise Estimation with $l_1 \geq l_{Th}$

When $l_1 \geq l_{Th}$, the change of frequency caused by W_1/W_2 does not result in waveform overlapping, thus $|v_{sn}(t)|$ is determined solely by $|h_0(t)|$. Under the following approximation:

$$y_0^{-1}(t) \approx \frac{1}{2\sqrt{L_0C_0}}(2L_0\delta(t) + R_0u(t))$$

The amplitude of the power noise $|v_{sn}(t)|$ can be bounded by:

$$|v_{sn}(t)| < 2|h_0(t)| \leq |i(t)|\frac{(2L_0 + R_0)}{\sqrt{L_0C_0}W_1} = K/W_1 \tag{2}$$

Eqn (2) means that amplitude of switching noise is inverse proportional to W_1 when $l_1 \geq l_{Th}$.

3.3.2 Noise Estimation with $l_1 < l_{Th}$

If $l_1 < l_{Th}$, we define $d(a,b) = a - b$, when $a \geq b$; $d(a,b) = 0$, when $a < b$. $d(l_{Th}, l_1)$ reflects the extent of overlapping between adjacent pulses.
1. When $W_1 < W_2$, according to Case 2 above, the negative pulse will overlap with adjacent positive pulse and the amplitude of noise does not increase, so Eqn (2) is still applicable.
2. When $W_1 > W_2$, two adjacent pulses may be both negative as shown in Case 3 above and

their overlapping would increase the noise amplitude.

An approximated formula for power noise amplitude $|v_{sn}(t)|$ can then be expressed as:

$$|v_{sn}(t)| < K/W_1(1 + \alpha(\frac{W_1}{W_2} - 1)d(l_{Th}, l_1)) \quad (3)$$

Where α is a coefficient which reflects the effect of overlapping on $|v_{sn}(t)|$. Notice that Eqn (2) is a special case of Eqn (3) when $d(l_{Th}, l_1) = 0$.

3.4 Switching Noise Reduction via Wiresizing

Analysis in previous section implies that only the part of power bus within l_{Th} distance from power pin i, PB_i, may affect the amplitude of switching noise at i. PB_i can be further divided into two parts with different widths:

Part 1: $0 \rightarrow l_{i1}$ distance from i, with width W_{i1}.

Part 2: $l_{i1} \rightarrow l_{Th_i}$ distance from i, with width W_{i2}.

The objective is to reduce the switching noise at each power pin to satisfy its specified bound while minimizing the routing area consumption.

Denote P as the set of power pins. Given noise constraint NC_i for each power pin $i \in P$, the power bus wiresizing problem is formulated as:

Minimize

$$\sum_{i \in P} \sum_{e_j \in PB_i} l_j W_j$$

Subject to:

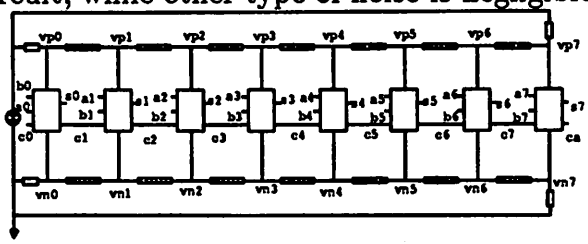
$$K_i/W_{i1}(1 + \alpha_i(\frac{W_{i1}}{W_{i2}} - 1)d(l_{Th_i}, l_{i1})) \leq NC_i, \forall i \in P$$
$$0 < W_{ik} \leq W_{ik_{ub}}, \ \forall i \in P, \ k \in \{1, 2\}$$

Here, l_j, W_j are length and width of segment $e_j \in PB_i$, with $l_j \in \{l_{i1}, l_{i2}\}$ and $W_j \in \{W_{i1}, W_{i2}\}$ (notice that PB at different power pins may overlap).

Our wiresizing approach can achieve consistency between minimization of switching noise and other power noises like IR-drop and metal migration[3] by embedding additional noise constraints into the formulation.

4 Experimental Results

The following full adder with about 800 transistors is used as the testing circuit, the length of power bus segment between two adjacent power pins is 300μ. Switching noise is the major source of noise in this circuit, while other type of noise is negligible.



The following table shows a result of the noise reduction using decoupling capacitors with $\alpha = \beta$ (i.e. equal emphasis on noise and area minimization). The second column shows the initial noises without decoupling capacitors. The third column shows the initial gradient of the objective function. The final noise and sensitivity values are shown in columns 4 and 5. Column 6 shows the inserted decoupling capacitors. The run required seven iterations. A variety of results can be obtained by varying the problem formulation. In the table, total noise of 0.802V and total decoupling capacitance of 0.363pF are shown. With $\alpha = 1$ and $\beta = 0$, the total noise of 0.251V and total decoupling capacitance of 1.491 pF were obtained after 8 iterations.

Node No.	Init. Noise (V)	Init. Sens. (pF^{-1})	Final Noise (V)	Final Sens. (pF^{-1})	Decl. Cap. (pF)
vp_1	0.318	-1.663	0.091	0.022	0.065
vp_2	0.389	-1.188	0.118	0.186	0.068
vp_3	0.524	-7.788	0.172	-0.011	0.067
vp_4	0.519	-5.125	0.126	0.014	0.053
vp_5	0.464	-7.674	0.166	0.076	0.051
vp_6	0.441	-5.607	0.129	0.059	0.059
Total	2.655	N/A	0.802	N/A	0.363

For the experiment on power bus wiresizing approach, only the part of routes within $l_{i1} = 25\mu$ from each pin i is wiresized to $W_{i1} = 4W_0$, the rest part of the bus is sized with $W_{i2} = W_0$. The following table shows the simulation results of the power bus wiresizing approach in terms of the final noise margin and area consumption (measured in amount of capacitance) at each power pin.

Node No.	Initial Noise (V)	Final Noise (V)	Area Consump.(V)
vp_1	0.318	0.050	0.09
vp_2	0.389	0.050	0.09
vp_3	0.524	0.075	0.09
vp_4	0.519	0.070	0.09
vp_5	0.464	0.065	0.09
vp_6	0.441	0.050	0.09
Total	2.655	0.360	0.54

The above table indicates that the wiresizing approach can reduce power switching noise significantly with moderate routing space consumption which will not affect the routing of other signal nets.

Both of our approaches tested adopt SWEC2.1 for simulation which enjoys a $12x$ speed up compared with Spice.

Acknowledgement

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References

[1] S. Lin, E. Kuh, and M. Marek-Sadowska, "StepWise Equivalent Conductance Circuit Simulation Technique", *IEEE Trans. CAD, May 1993, pp. 672-683*

[2] W. Nye, D. C. Riley, A. Sangiovanni-Vincentelli, and A. L. Tits, "DELIGHT-SPICE: An Optimization-Based System for the Design of Integrated Circuits", *IEEE Transactions on Computer-Aided Design, Vol. 7, No. 4, April, 1988*

[3] S. Chowdhury, M. Breuer, "Minimal Area Design of Power/Ground Nets having Graph Topologies", *IEEE Trans. Circuit and Systems, Dec. 1987, pp. 1441-1451*