THE IMPLEMENTATION OF A HIGH SPEED EXPERIMENTAL TRANSCEIVER MODULE WITH AN EMPHASIS ON CDMA APPLICATIONS

by

Arya Reza Behzad

Memorandum No. UCB/ERL M95/40

2 June 1995

THE IMPLEMENTATION OF A HIGH SPEED EXPERIMENTAL TRANSCEIVER MODULE WITH AN EMPHASIS ON CDMA APPLICATIONS

by

Arya Reza Behzad

Memorandum No. UCB/ERL M95/40

2 June 1995

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

Acknowledgments

I am deeply grateful to all the people who in one way or another have helped me during the course of this seemingly endless project.

First, I would like to thank my parents for all that they have done for me, and for all the hardships that they have put up with in order for me to be able to study and succeed half way across the globe. That also goes for my brother, Arash, whom I frequently miss his company.

Next, I would like to express my great appreciation and love to my (now) wife, Maryam, who has patiently awaited the completion of this thesis.

Now, to Berkeley... I am very thankful to Professor Bob Brodersen, my research advisor, for all of his patience, and for his guidance in my research work and other matters. From the first day that I was handed the rough sketch of a receiver block diagram (I will never forget how confused I was) by Professor Brodersen, I have very much enjoyed working and collaborating with him on various issues.

I also have a great appreciation for the patience of Professor Bob Meyer in his long wait for a completed copy of this thesis. During my studies at Berkeley, I have had the pleasure of taking one class and sitting-in in another class instructed by Professor Meyer. These classes have been the best and the most instructive classes that I have ever had. I have also been fortunate in having the opportunity to consult with Professor Meyer in many occasions on the various aspects of this project.

I would also like to express my gratitude to Professor Paul Gray for his patience and for the very instructive enlightening discussions that I had with him during my studies at Berkeley. I would also like to express my special thanks to Professor Gray for being instrumental in recruiting me into Berkeley during my search for a suitable graduate school. I have very much enjoyed the two years that I spent at Berkeley, and I have no doubt that I made the best choice.

During my studies at Berkeley, I very much enjoyed working with Sam Sheng. I have learned an incredible amount from Sam, and I appreciate every bit of his help. Sam helped me (and just about everybody else in Cory) in everything ranging from the studies for prelims, to various topics on my thesis.

My house-mates, Andy Abo, Srenik Mehta and Tony Stratakos... they were the best. It was always great to bike home and spend a couple of hours relaxing with three of my best friends (and no--I did not get tired of seeing them in Cory *and* at home, well maybe sometimes!).

The other guys "living" in 550 Cory: Arthur Abnous, Keith Onodera, Anantha Chandrakasan, Chris Rudell, Greg Uehara, Cormac Conroy, Ken Nishimura, Andy Burstein, Craig Teuscher, Tom Burd, Tom Truman, Dave Lidsky, Lapoe Lynn, Robert Chu, Ranjit Gharpurey, Cynthia Keys, Thomas Cho, Robert Neff, Todd Weigandt, Pramote Piriyapoksombut, Shankar Narayanasamy, Sekhar Narayanaswami, Roger Doering, Arnold Feldman, and many others whom have been great friends and whom I have very much enjoyed working with, and many of which have helped me with respect to this thesis.

I am also grateful to the great amount of help I have received from the staff; ranging from registration issues to ordering parts for this project to system administration issues to entering parts into the Racal library to... Peggie Brown, Kevin Zimmerman, Tom Boot, Heather Brown, Sue Mellers, Ken Lutz... Thanks for all of your help and support.

I would also like to thank Bill Baringer for his assistance in the initial phases of this project, and for his long patience in waiting for this thesis to materialize.

Many thanks to Jennie Chen for her help during the final stages of this design, especially in the documentation of the schematics.

Thanks to Professors Jan Rabaey, Ed Lee, Bernhard Boser, and David Messerchmitt for their great classes.

My appreciation also goes to my colleagues at MicroUnity and especially to Rick Meller, Saman Behtash and Jean-Yves Michel for their review of portions of this write-up. Also thanks to Paul Berry for his hints on the use of Frame Maker.

Last, but certainly not least, I would like to express my appreciation to my uncle, Nasser Djavadi, my aunt, Gayle, and my cousin, Jeffrey. Since my arrival in the United States in 1988, I have been very fortunate to have their support and love. I owe many of my accomplishments to them.

There have been many, many people that have assisted me during my work at Berkeley and I apologize for any names that I may have not acknowledged here.

Table of Contents

List of Figures

Introduction

In order to satisfy the front-end requirements for the baseband Infopad system, three alternatives methods have been investigated. First, as a short-term solution, a commercial radio modem was utilized. The use of a commercial modem, however, restricted the baseband system in many ways. The data rate was not high enough, multiple access could not be easily achieved, and the commercial modem did not allow for much flexibility in testing various scenarios and empirically investigating various issues.

As an intermediate solution to these problems, the front-end system presented here was designed and implemented, reducing or eliminating the restrictions outlined above. Some restrictions do still exist which will be eliminated in the final solution to the front-end requirements of the Infopad system. For example, a rake receiver cannot be implemented using this module, but such a receiver will be implemented in the final version of Infopad. Furthermore, the power consumption, component count and cost of this module is relatively high. These issues are also addressed in the final, fully integrated, version of Infopad [1].

Section 1.0, "An overview of the Infopad Project," discusses a summary of the communication-system issues relating to the Infopad. Much of the work in this section has been performed by Sam Sheng, Craig Teuscher and Professor Bob Brodersen.

The report continues on to discuss the many issues that had to be considered in the design of this module. In general, in every section, the related background theory is presented and then the specifics of the issues as related to this system are outlined. In some sections, the specifics of the issues are not presented separately as the background theory section applies directly.

CDMA Transceiver

1.0 An overview of the Infopad Project

1.0.1 Function of Infopad

The primary goal of the Infopad project is to provide a high-speed communication network for indoor environments. This project encompasses all the design aspects of such a high speed system, including high level communication system design, front-end transceiver design, baseband digital design, mechanical case design, software protocol design, etc. The end result of the Infopad project is a wireless system capable of supporting one-way real-time video communication, and a low-power portable multimedia terminal with hand writing recognition, speech recognition and many other capabilities.

1.0.2 Applications of Infopad

A portable wireless indoor communication system can be beneficial in many future applications. The "future classroom" would be one example whereby the professor uses his Infopad instead of the blackboard with many enhanced multimedia capabilities, and concurrently students receive the same information on their own Infopads. This information can be selectively saved by each student, while additional commentary notes can be added by each student and stored on the backbone mass storage system. Another application of the Infopad system would be in a large manufacturing facility, where the workers/supervisors are mobile and move to different areas of the manufacturing facility. At any time they can record information (inventory, observations, etc.), while being able to retrieve high speed video information if necessary (on the operation/trouble shooting of a particular piece of equipment, for example).

1.0.3 Advantages of Portability & Cost Justification

Clearly a portable system is superior to an equivalent-performance, non-portable system. A question that frequently arises is whether or not this portability is economically a viable solution. Although the cost of implementing such a system for a building with an existing wire-line communication system may be relatively high, such a wireless network may be less costly to implement in a new building, since much of the cost of a wire-line communication network is associated with the cost of the routing of the wires to *every user* in the system. An example of such a scenario is the Nation-wide fiber-optics network. The cost of bringing fiber to every home from a central hub is far more than the cost of nation-wide network itself (the so-called "last-mile" problem), and is not economically justifiable. For the "last-mile" therefore, it has been proposed to use existing coaxial cable lines for areas where a cable-network exists, and to use wireless communications for new developments.

An additional benefit of a wireless system is that expanding such a system is typically much simpler than expanding a wire-line network.

1.1 The Infopad Vision of Wireless Computing

1.1.1 Indoor Wireless Computing, the Infopad Way

The Infopad project has a rather unique vision of an indoor wireless computing environment. This vision is summarized in FIGURE 1. A wireless multimedia terminal is utilized by each user in the system. These multimedia terminals--the Infopads--offer x-terminal, video display, digital audio input and output, and pen recognition capabilities. The Infopads are linked via a high-speed wireless link to a base-station which is connected to a variety of resources through a very high bandwidth fiber-optic backbone. These resources include high speed compute servers, compressed video databases, speech recognition databases, and a multitude of commercial databases such as news servers and financial databases.

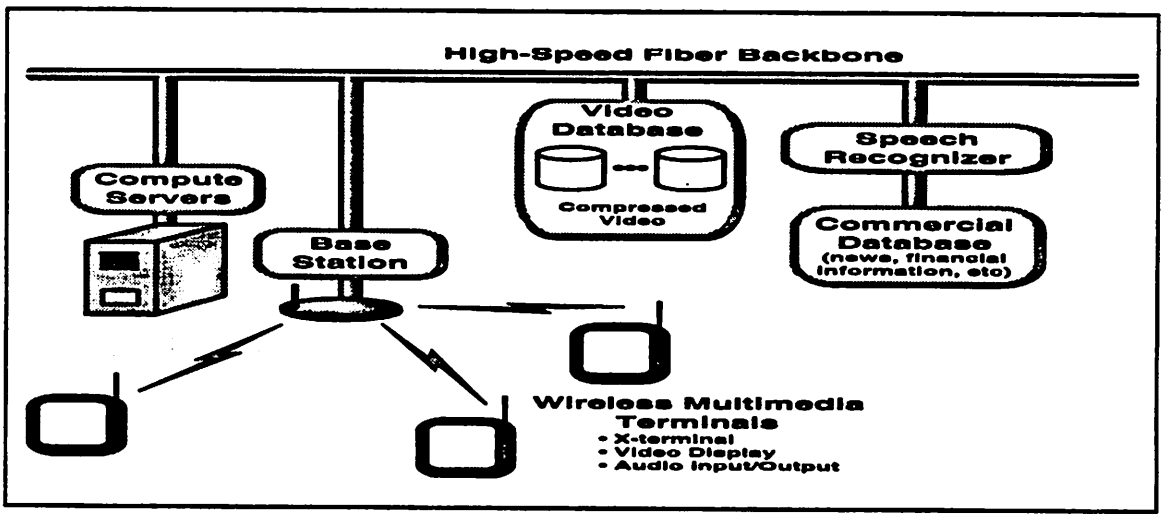


FIGURE 1. Indoor wireless communications as envisioned by the Infopad project

1.1.2 The Lack of Use of a General Purpose Microprocessor in the Infopad

In the present form, Infopad does not utilize a general-purpose microprocessor, and leaves all the general-purpose number crunching tasks to the backbone compute-servers. In effect, Infopad relies on the high speed communication link to provide for any computational needs, thereby eliminating the power consumption, board space, and cost factors associated with having a general purpose microprocessor on board. On the other hand, the Infopad is unable to perform any task if not in a covered pico-cellular area. A commercially adopted version of the Infopad may or may not have a general purpose microprocessor on board.

1.1.3 Asymmetric Communication Link

In the present form, the communication link between the Infopads and the base-station is asymmetric. The downlink (base-station to Infopad) data link is designed to be operating

at a much higher speed than the uplink connection. This is because downlink video communications is required, but no provisions are currently made for an uplink video communication capability (as required for example in a portable video-phone). As described in Section 1.1.3, "Asymmetric Communication Link," a CDMA based spread-spectrum system is used for the downlink communications whereas it has been decided to use a TDMA uplink communication scheme.

1.1.4 Pico-Cellular Based System

The system is based on a pico-cellular communication scheme. The word "pico-cellular" is used because the cells can be as small as a conference room or a classroom. The use of a pico-cellular scheme allows for more overall users in the system [2]. This fact can be intuitively understood by realizing that the smaller the cells, the more the possibility of reusing the same frequencies for transmitting information to other users. On the other hand, the smaller the cells, the more the number of base stations in the system and the lower the transmitted power by each base station.

1.1.5 Frequency Re-use

In a traditional cellular system (e.g. the Advanced Mobile Phone System, AMPS), the cell frequencies are reused, but the cell sizes are typically large. One method of increasing capacity for congested urban areas is to reduce the cell size as described above. FIGURE 2 displays a typical cellular system with a frequency re-use factor of K=7. This cellular method relies on the fact that the amplitude of the signals coming from cells operating at the same carrier frequency (which are never adjacent) are attenuated significantly by the time they reach the cell of interest such that they do not cause appreciable overall performance degradation. In reality the cell coverage is not hexagonal, and overlap areas exist between adjacent cells, resulting in a potential SNR degradation in those areas (due to out-of-band leakage). Given the frequency re-use scheme shown in figure FIGURE 2, an overall bandwidth seven times larger than the bandwidth of each cell would be required. Other common frequency reuse patterns utilize K=4, K=12, etc.

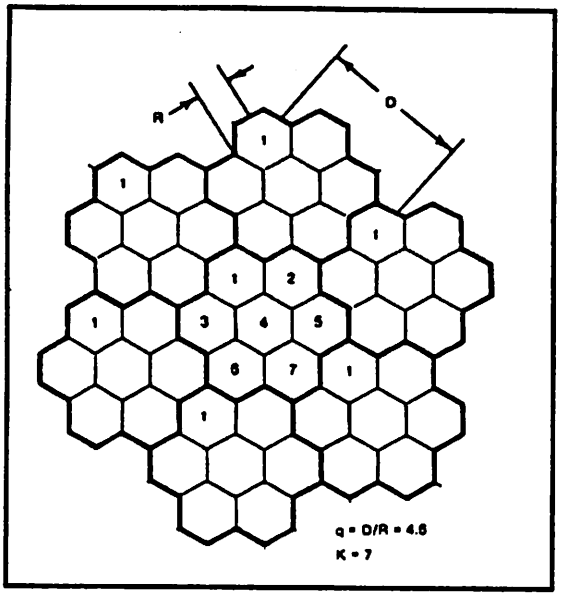


FIGURE 2. An example of a frequency reuse pattern in a traditional cellular communication system with K=7 (after [39])

The Infopad system specifications, 2 MbPS (mega bits per second) per user and 63 or 64 users per cell (with a processing gain of 64), requires the availability of a bandwidth of 128MHz per cell. If a traditional frequency allocation scheme were to be used with this system, a bandwidth of 768MHz would be necessary. Clearly this is not feasible. The Infopad system, therefore operates at the same carrier frequency in all the cells. The signal amplitude of each neighbor cell, therefore will have to be as low as possible to minimize the amount of interference and resulting SNR degradation in adjacent cells. The hand-off schemes are significantly different in such a system than the traditional cellular system. These hand-off schemes require the base-stations' PN sequences to be offset from one another by a predetermined amount. The backbone network and/or a global positioning system (GPS) can provide such "synchronization."

1.2 Multiple Access

1.2.1 TDMA, FDMA, & CDMA

There are two traditional methods of multiple access; i.e. multiple users accessing a common resource through a shared communication link. These are time division multiple access (TDMA) and frequency division multiple access (FDMA). In a TDMA system, the communication channel is allocated to a single user at any instant of time for a predetermined period. After the expiration of each users time slot, the channel is allocated to the next user. In a TDMA system all users operate at the same frequency. In an FDMA system, all users operate at the same time but are allocated a fraction of the available spectrum. In a TDMA system users are differentiated from one another because their communication links are orthogonal in "time-space." In FDMA the users communicate in a mutually orthogonal "frequency-space."

Another method of achieving multiple access is through the use of "code-space." This is utilized in spread-spectrum systems in the form of frequency-hopping or direct-sequence

communication schemes. A discussion of these methods of communication is presented in the next section (See section 1.3, "The Basics of Spread-Spectrum").

1.2.2 Stochastic vs. Deterministic Multiple Access

FDMA and TDMA are examples of deterministic methods of achieving multiple access. There are other methods of multiple access which rely on a stochastic scheme, where no user is allocated any channel in advance. In a carrier sense multiple access (CSMA) scheme (used on the ethernet in the form of CSMA-CD (collision detect) for example) each user transmits his/her packet at a pseudo-random time after it has obtained a carrier. If the user then hears (senses) a collision, he/she will wait for a random period of time and retransmit the same packet. Since the wait periods are random, the probability of collision with the same packet is very small on the subsequent tries. The ALOHA wireless system is also based on collision detection.

A spread-spectrum system is a pseudo-deterministic (or pseudo-stochastic) communication scheme.

1.3 The Basics of Spread-Spectrum

1.3.1 Frequency Hop: Probability of Error and Processing Gain

There are two customary methods of spread-spectrum communications. A frequency-hop spread-spectrum system relies on a "hopping" local oscillator modulating the signal to different carrier frequencies. The pattern of the hop (the frequency which the oscillator jumps to) is typically determined by a pseudo-random (PN) sequence. Since each user has a different PN code, the signals are guaranteed not to overlap, as long as their transmitters are synchronized. A frequency-hop (FH) spread-spectrum system is similar to a frequency division multiple access system (FDMA) in which each user is transmitting at a different frequency at any given time. The difference lies in the fact that in an FDMA system each user is assigned a fixed frequency, whereas in a FH system this frequency is variable and is determined in a pseudo-random fashion (FIGURE 3.c). In general, for many modulation schemes, in a frequency-hopping spread spectrum system, the faster the hopping rate the less the probability of error. On the other hand, the hopping rate does not affect the "processing gain" of the frequency-hop spread-spectrum system. The processing gain of a frequency-hop spread spectrum system is given by

$$\text{Processing Gain}_{FHSS} = 10\left(\log_{10}\frac{\text{allowable hopping bandwidth}}{\text{data bandwidth}}\right) \qquad \text{(EQ 1)}$$

which is equal to the number of frequency choices. In reality this definition is identical to the definition of processing gain in a CDMA system given by equation [3].

A simplistic model for the probability of error in a FHSS system with a binary FSK modulation scheme is given by the cumulative binomial expansion [3].

$$P_e = \sum_{i=r}^{c} \binom{c}{r} \left(\frac{J}{N}\right)^i \left(1 - \frac{J}{N}\right)^{c-i} \qquad \text{(EQ 2)}$$

where J is equal to the number of "jammers"[1] in the allowable hopping spectrum and N is the number of frequency choices (and hence J/N is the probability of error for a 1chip/bit system). Further more, c is the number of chips transmitted per bit and r is the number of wrong chips required to cause a bit error. Using this formula and a "majority decision" slicer, we can observe that a system transmitting three chips per bit which would require at least two chips to be in error to make an erroneous bit detection ($c = 3$, $r = 2$) would have a $P_e = 7.21\times10^{-4}$ in the presence of a single jammer in a system with $N = 64$, whereas with $c = r = 1$, we would obtain $P_e = 1.6\times10^{-2}$, or a factor of 21 worse. This difference is much more pronounced for spread spectrum systems with higher processing gains. The so-called "fast-hop" FHSS systems utilize $c > 1$. Unfortunately such systems require fast settling (agile) frequency synthesizers that are difficult to design. Most existing agile synthesizers are based on direct digital synthesis (DDS) systems.

As described above, most implementations of frequency-hop spread-spectrum systems are "radio-intensive" whereas, as described below, most implementations of direct-sequence spread-spectrum systems are DSP intensive.

1.3.2 CDMA: Processing Gain

In a CDMA system, each user's data bits are encoded into a sequence of "chips" before transmission. In the time domain, the chip rate is N times the bit rate, where N is defined to be the "spreading factor." Because of the reciprocity relation between the time and frequency domains, the transmit bandwidth is increased by a factor of N over the non-spread data bandwidth, hence the name "spread-spectrum." FIGURE 3.a & FIGURE 3.b show the effects of spreading a signal in the time and the frequency domains.

The processing gain of a CDMA spread-spectrum systems is defined to be equal to its spreading factor express in decibels. In other words

$$\text{Processing Gain} = 10 \log_{10} N \qquad \text{(EQ 3)}$$

Almost all advantages associated with the use of a spread-spectrum system are proportional to the system's processing gain. It is important, however, to mention that a spread-spectrum system is effective against additive (peaked) noise. In other words, a spread-spectrum system is neither better nor worse than a non-spread system in response to white noise (See section 4.4.1.1, "Effect of CDMA on System Noise Bandwidth"). Any "jamming" peaked (sinusoidal) signal however which is added to the signal on the transmission

1. A deep null in a multipath channel can be considered to be a jammer in this context.

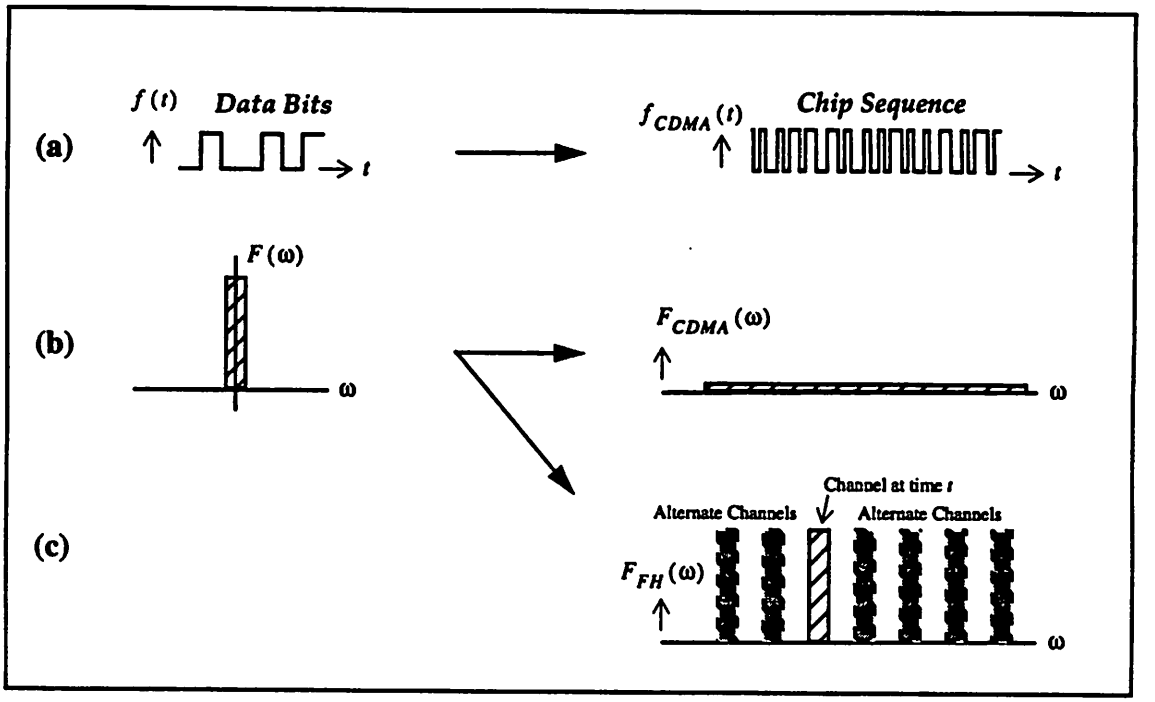


FIGURE 3. The effect of (CDMA) spreading a signal in the (a) time domain and (b) frequency domain (simple model, see FIGURE 9 for the more realistic spread signal) (c) the same baseband signal as (b) in an ideal frequency hop spread spectrum system.

channel will be effectively spread at the receiver correlator and hence its effect will be reduced by a factor proportional to the processing gain[1].

Typically, with a spreading factor of N, a maximum of N users can be multiplexed in the system. If a spreading factor of N is used, but less than N users are multiplexed in the system, the remaining processing gain can be utilized to achieve a higher SNR and a better BER in the system.

1.3.3 PN Codes

Various families of codes can be used in implementing a CDMA-based system. Most of these implementations utilize the pseudo-noise (PN) code in one way or another[2]. A pseudo-noise code gets its name from the fact that it appears to be statistically white. In

1. It is important to note that the processing gain of a DSSS system is typically larger than the "jamming margin" of the system. The processing gain of a system is the quantity by which a narrow-band jamming signal (assumed to be in the middle of the band) has to exceed the wanted signal in order to generate a signal with the *same* power at the output of the despreader as the wanted signal *in a loss-less receiver.* This will effectively yield an SNR of 0 at the slicer which is clearly not acceptable. The jamming margin effectively takes into account the minimum desired SNR at the slicer for a proper BER and the loss in the receiver.
2. Another name for a PN sequence is a "maximal linear" sequence. This name arises from the fact these codes are the longest codes than can be generated by a linear feedback shift register of a given length. For a complete list of properties of these codes see [3] and [4].

other words, its autocorrelation function possesses a very strong peak when it is completely synchronized with itself (no time offset), and it is almost zero everywhere else FIGURE 4.a. This property can be very effectively utilized for timing recovery (synchronization) at the receiver. For an M-tap shift register (FIGURE 4.b), however, there are relatively few distinct code-sequences that can be generated. To obtain 64 mutually orthogonal PN-sequences in a 64 user system, a shift register of length M = 11 has to be utilized with resulting PN sequences of length N = 2047[1]. This is typically not practical. Furthermore, the few PN codes that do exist do not posses nice cross-correlation properties. An approximate relation for the SNR of N equal-power, equal-length PN sequences is given by [3]

$$\mathrm{SNR}_N = \frac{S}{\sqrt{N\left(K_1^2 + \frac{T_0}{T_{cc}}\right)}} \qquad \text{(EQ 4)}$$

where K_1 is the value of the DC correlation, T_{cc} is the cross-correlation integration period, and T_0 is the code bit period. It is clear from this relation that if the cross-correlation integration period is long as compared to the bit period, its effect is averaged out and the SNR is not affected by this component.

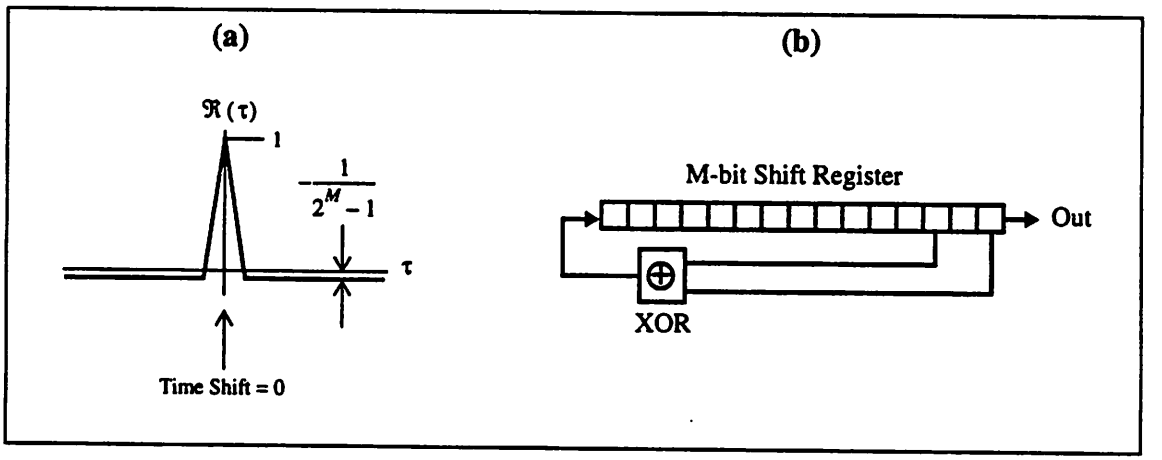


FIGURE 4. (a) Autocorrelation of a PN sequence. (b) Hardware generation of a PN sequence.

Hardware generation of a PN sequence is very simple. Generating a length $2^M - 1$ PN sequence requires an M-bit shift register with XOR gates tapped on at specific locations along the shift register (FIGURE 4.b).

---

1. The actual number of distinct PN sequences using a M-tap shift register is given by $\frac{\Phi(2^M - 1)}{M}$ where $\Phi(2^M - 1)$ is an Euler number, the number of positive integers, less than $2^M - 1$, that are relatively prime to $2^M - 1$ [3].

1.3.4 Gold Codes

Gold codes are an alternative to PN sequences. They are slightly more complicated than PN sequences to generate (they are effectively generated by a modulo-2 addition of two PN-sequences), but have many advantages over PN sequences. For example, they generate a much larger number of codes for a given M-tap shift register than PN-sequences. Furthermore, it can be mathematically proven that they have bounded cross-correlation properties, whereas it is not possible to guarantee the maximum bound of the cross-correlation of two PN-sequences.

1.3.5 Walsh Codes

Walsh sequences are a family of orthogonal ±1 codes. The logic diagram of a system that can generate a walsh code of length 2^k is displayed in FIGURE 5. Note that in this configuration, logic *0* is equivalent to Walsh code *+1*, and logic *1* is equivalent to Walsh code *-1*.

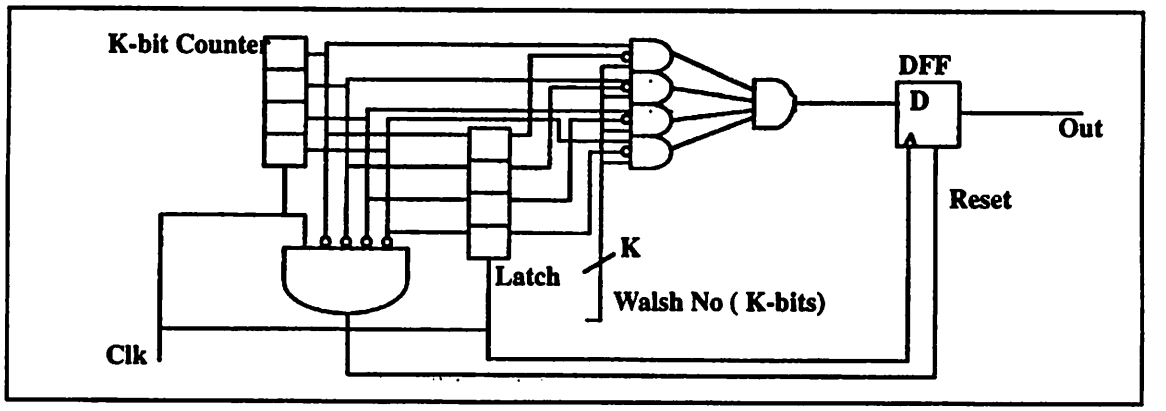


FIGURE 5. Hardware generation of a Walsh sequence

A walsh code of length 32 is displayed in FIGURE 6. There are several important observations to make here.

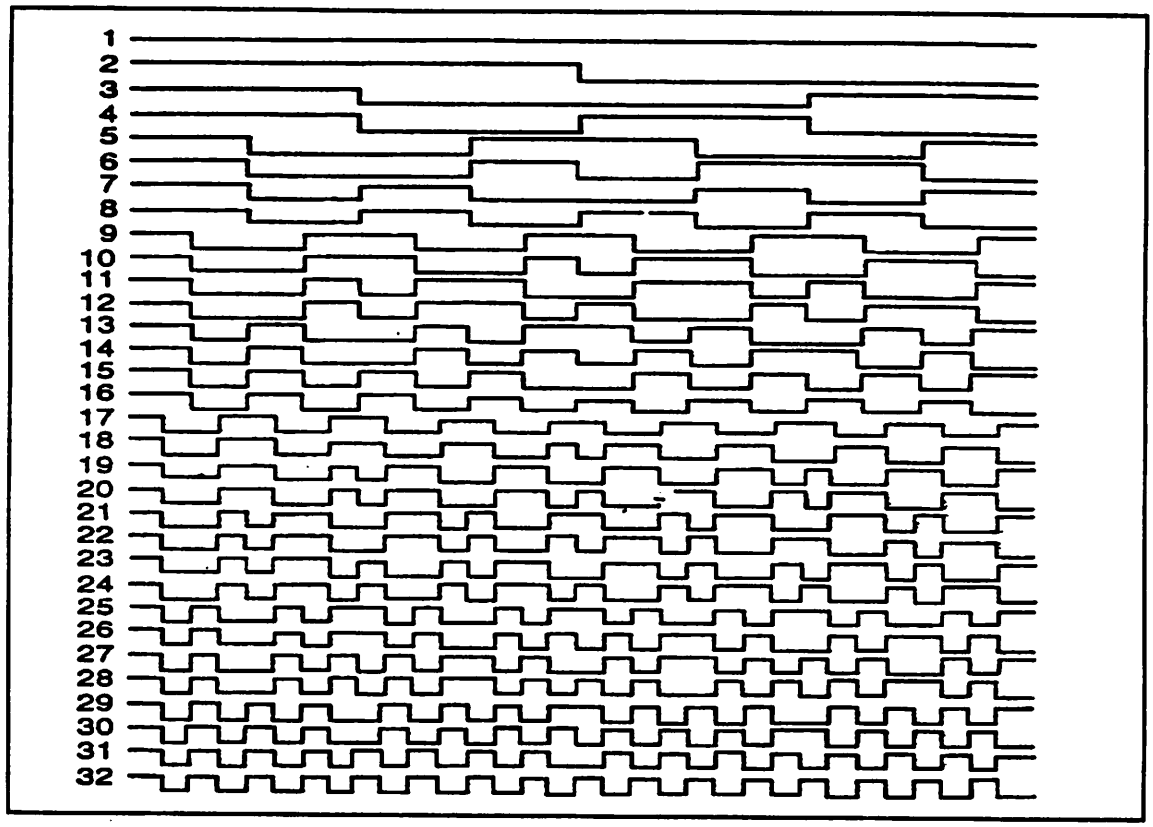


FIGURE 6. The 32-long Walsh orthogonal family of codes

- The *0'* th order Walsh code (code #1 in FIGURE 6) is simply a DC tone.
- A subset of the Walsh functions are the Hadamard codes which are obtained simply by dividing the *0'* th order code by two consecutively. This corresponds to codes numbered *2, 4, 8, 16* and *32* in FIGURE 6. Although such codes are easier to generate in hardware, they provide only $\log_2(K)$ orthogonal codes. Hence, generating 64 orthogonal codes for 64 users would require a code of length 2^{64}.
- All the codes are mutually orthogonal (the cross-correlation of two codes is equal to zero); i.e. take any two distinct codes, multiply them through, and take the integral over one period. The result is zero.
- The orthogonality property is only preserved as long as the codes are synchronized. If a code is time shifted in comparison to another code, the cross-correlation will no longer result in zero. This is a very important limitation and will be discussed further below (See section 1.3.7, "Asymmetry of Channel as it Relates to the Codes").
- The Walsh functions do not have a "nice" auto-correlation property. In other words, they do not have a strong peak in their auto-correlation function at a time offset of zero as compared to finite time offsets. This fact is not immediately obvious from FIGURE 6, but can be easily shown analytically or by simulation.

1.3.6 A Walsh PN Sequence Overlay

In order to overcome the shortcomings of the PN sequence in the cross-correlation arena and the shortcomings of the Walsh sequences in the auto-correlation arena, the Infopad utilizes a Walsh/PN sequences overlay as shown in FIGURE 7.

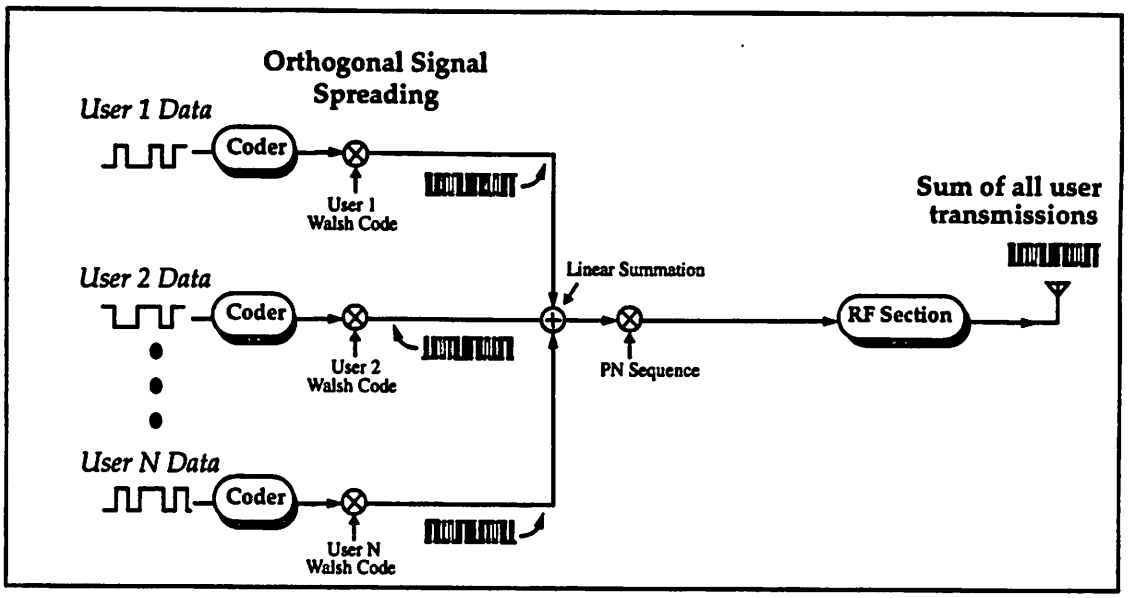


FIGURE 7. The Walsh/PN sequence overlay as used in the Infopad [1].

In this configuration, each users data is encoded into a DQPSK (differential quadrature phase shift keying) signal and fed into a multiplier[1] where the data stream is multiplied by a Walsh sequence which is unique to that user. The resulting encoded sequence of all *N-1* users are then linearly summed and multiplied by a common PN sequence. *N-1* users are supported (as opposed to *N*) because the zeroth order Walsh code in conjunction with the PN sequence are transmitted as a pilot tone and are used in timing recovery at the receiver. Multiplying the PN sequence by a constant (the zeroth order Walsh function) preserves the nice autocorrelation properties of the PN sequence, allowing it to be used in the timing recovery.

1.3.7 Asymmetry of Channel as it Relates to the Codes

It is important to note that since the Walsh codes are mutually orthogonal *only* if they are properly synchronized as received at the receiver, this method can only be utilized in the downlink. This is because at the base-station transmitter, one can guarantee the synchronization of all the transmitted signals. Furthermore, all the signals have the same propagation delay time in arriving to a *certain* user. Therefore they will all be synchronized at the

1. In reality an XOR gate with proper coding is used because the inputs are simply multiplied by +1 or -1.

receiver. A more detailed discussion of the down-link communication channel is presented in Section 4.4.3, "A Simple SNR / BER Model".

On the uplink however, each user may transmit at different times. Even if the users could be made to transmit at the same time by using some kind of synchronous polling scheme, since the distances from each user to the base-station and hence the propagation time is different, the received signals would not be mutually orthogonal. This will result in a major degradation in the system SNR. In the presence of large offsets the system will completely cease to operate.

1.3.8 Co-User Noise in an Uplink Channel

In general, the co-user noise in an uplink channel is primarily due to the lack of perfect synchronization on the received signals between the different users. The aggregate co-user noise is the summation of several independent noise sources, and can be modelled to have a Gaussian distribution. At the same time, to the first order, the *co-user* noise at the despreader output, in the bandwidth of interest for the *user* can be modeled as white (note that the despreader *despreads* the *user* signal but *spreads* the *co-user* signal). Therefore for exact modelling and analysis of the system performance, the power spectral density of white noise, W_N, used in SNR should be the sum of the receiver noise (modelled through the receiver noise figure) and the modelled white noise due to the co-users. In addition, any other factor such as adjacent channel interference should be taken into account.

It can easily be shown, and it is intuitively clear, that in the ideal case (when the spreading codes have ideal low pass spectra) the total noise contribution of the co-users in an up-channel model is

$$P_{N(Couser)} = (k-1)\frac{P_0}{N} \qquad \text{(EQ 5)}$$

where $P_{N(Couser)}$ is the total power contribution of the co-users to the system noise, k is the total number of users in the system, P_0 is the total power received from each co-user, and N is the spreading factor. Equation [5] assumes a perfect power control system which would eliminate any near-far problem (power transmitted to a far receiver is increased in order to compensate for the distance based attenuation). Clearly, the higher $P_{N(Couser)}$ the less the number of users that can be supported on the up-link channel.

The Spectral Inefficiency Factor and Adjacent Cell Interference

In reality, the situation is even worse. One has to account for the "spectral inefficiency factor," F_{sie} due to the non-ideal low-pass spectra of the spreading code as well as the non-perfect power control. For a PN-spread CDMA system, with the PN sequence band limited to the chip-rate, F_{sie} is 1.64 [5].

It can be easily shown that the power spectral density of noise in the system is given by [5]

$$W_N = F_{sie}F_{ac}(k-1)\frac{P_0}{Nf_1} + W_{N(rcvr)} \qquad \text{(EQ 6)}$$

where F_{ac} is the adjacent cell interference factor (See section 4.4.3.3, "Effect of Adjacent Cell Interference in the Uplink on Minimum Receiver Sensitivity Required"), f_1 is the bandwidth of the unspread signal, and $W_{N(rcvr)}$ is the power spectral density of the receiver noise which is a function of the receiver noise figure.

The total number of users in the up-channel is therefore given by

$$k = N\frac{\left(\frac{E_b}{W_N}\right)^{-1} - \left(\frac{E_b}{W_{N(rcvr)}}\right)^{-1}}{F_{sie}F_{ac}F_{pc}} + 1 \qquad \text{(EQ 7)}$$

where E_b is the average energy per bit and F_{pc} is the factor by which the power is reduced in the worst case due to imperfect power control. E_b / W_N is determined by the bit-error-rate (BER) required in the system and the modulation scheme (See section 4.4.2, "Modulation Scheme and its Effect on SNR Requirements").

1.3.9 Number of Users Supported in an Down-Link Channel

It is clear from equation [7] that in an up-link case many factors beside the noise figure of the receiver enter the equation for determining the maximum number of users in the system. In the down-link case where orthogonality of the co-user signals can be guaranteed at the receiver, the situation is much better. One needs to worry about only the adjacent cell interference, the NF of the receiver, and signal interference due to multipath (See section 4.4, "Receiver sensitivity"). The strong dependence of system BER in a down link to the channel response is shown in FIGURE 9, curves ❶ & ❸.

Due to the difficulties described above in an up-channel spread spectrum system, the Infopad does not utilize a spread-spectrum uplink system. In general, implementing up-link CDMA systems is possible, but maintaining (or adaptively equalizing for) orthogonality becomes more and more difficult at higher data rates and larger covered areas. In the Infopad system a relatively simple TDMA system is utilized for the uplink communication.

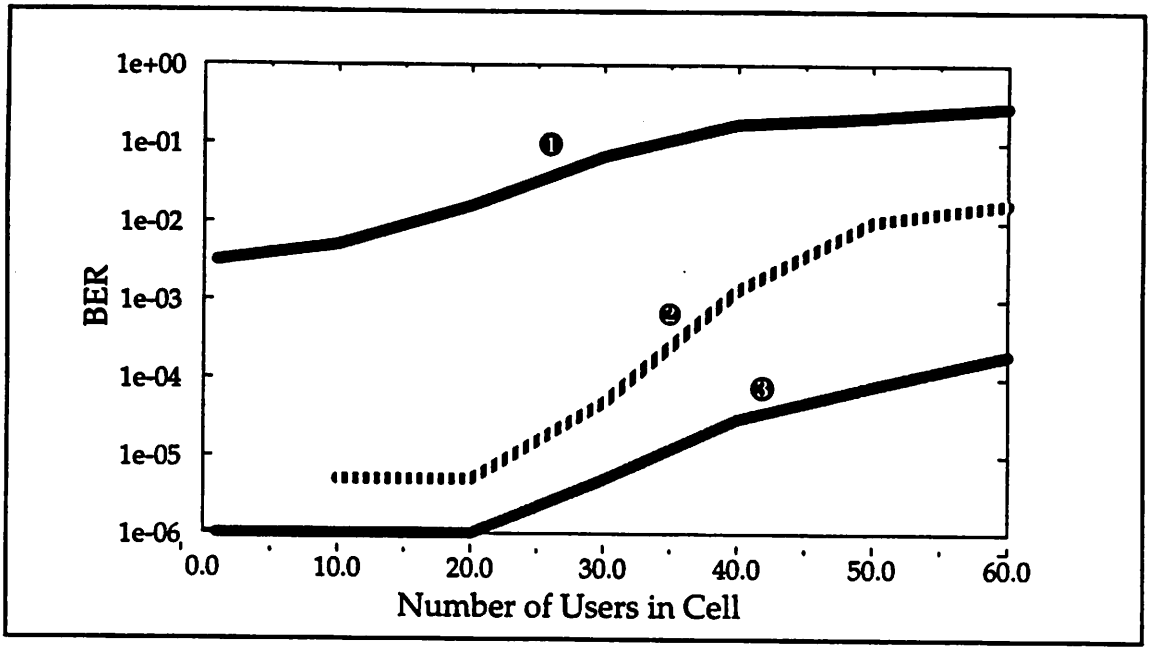


FIGURE 8. Simulated relative BER degradation as a function of increasing number of users in a down link indoor environment for ❶ a deep fade channel with no RAKE receiver, ❷ a deep fade channel with a RAKE receiver, and ❸ a "good" channel, with relatively flat fading (after [38]).

2.0 Objectives in Implementing This Experimental Transceiver

2.1 Requirements

2.1.1 No Frequency Re-use, Low Transmit Power

As an intermediate-level solution to the front-end needs of Infopad this system has to satisfy requirements for an indoor communication system. These requirements, in some cases are quite different from those required by outdoor communication systems. Furthermore, Infopad is unique in that because of its use of CDMA and the requirement for a high data rate it requires a large amount of bandwidth (in the order of 100MHz). Certainly the traditional method of frequency reuse, of the kind done with the traditional cellular phone system, would require several hundred MHz of BW. For example, if K is the distinct number of bandwidths (or frequency reuse factor) used in the system and D is the distance of two nearest unity-radius base-stations transmitters operating at the same frequency the most common frequency reuse patterns utilize: $K = 4$ with $D = 3.46R$, $K = 7$ with $D = 4.58R$, or $K = 12$ with $D = 6R$ (FIGURE 2, also see [2]). At the present time, there is no portion of the usable spectrum that is this wide. Therefore in the infopad system (and in most other CDMA systems), the *same* bandwidth is used for all adjacent cells. Therefore it is important to keep the inter-cell interference to the minimum possible level.

2.1.2 AGC Circuitry

Another distinct difference between indoor and outdoor environments is the requirements on the AGC circuitry. The slow movement of the objects in an indoor environment simplifies the design of the AGC loop. Since rather infrequent updates are required on the gain setting of the VGA stage, the AGC loop bandwidth can be relatively small. Maintaining stability in a small loop bandwidth AGC is much more readily achieved than in a wideband AGC loop. For example for a typical indoor environment, fading occurs at a slow rate of about 1KHz. An AGC loop bandwidth of about 100μs (10KHz) would be a safe compromise between the ability to rapidly respond to fades and the possibility for oscillations in the loop.

2.1.3 Flexible Design

The module described in this report was primarily designed to be an intermediate-level solution to the front-end needs of the Infopad *base-station* transmitter and the *portable unit* ("Infopad") receiver utilizing a CDMA system. However this board was also intended for testing alternative baseband systems, some of which had conflicting front-end requirements. Flexibility was therefore one of the major goals in the design of this module. The system was to be designed to be able to interface with in-house and commercially available baseband systems (e.g. analog correlators, digital correlators, etc.). It was also intended to be used in investigating various uplink/downlink modulation schemes. Reasonable engineering judgement was used in the design of the module in making trade-offs between flexibility and complexity (size, design time, cost, etc.).

2.1.4 Empirical Measurements of Effects of Phase Noise and Multipath on BER

This module is also intended for empirically quantifying the effects of variables such as multi-path response in an indoor environment, phase noise of oscillators, and other elements on the overall performance of a digital receiver (BER degradation). For example, crude and complicated closed form mathematical solutions exist for calculating the effects of phase noise of an oscillator in a receiver NF. Simulation tools are also available to assist the designer in calculating the effects of phase noise on the NF and the overall BER. However, since phase noise is a complicated phenomena these equations and models have to be empirically verified. This module, allows injecting phase noise in various ways to the system and observing its effect on the overall performance of the receiver.

2.1.5 Evaluation of the State of the Art Commercial Components

Another objective in designing this board is to evaluate the state-of-the-art commercial components, their advantages and their shortcomings, and use this information to assist chip and system designers in making better decisions. The information regarding commercial filters gathered during the design of this module has proven particularly helpful to chip designers.

2.1.6 A Superheterodyne Architecture

The use of commercial components, however, limits the system designer's options in many respects. For example, we were forced to use a superheterodyne architecture (as opposed to direct conversion architecture) because of the lack of the availability of commercial IC's for other receiver architectures. Also the frequencies selected for the front-end (RF and IF) were a function of the quick availability of commercial parts. This dictated a carrier frequency of 888 MHz and an IF frequency of 70 MHz.

2.1.7 Low Power Consumption

Low power consumption was also an objective. Although there was not much that could be done in this respect besides selecting the commercial components which consumed the least amount of power while satisfying the other system specifications. In many cases this was at odds with the flexibility objective.

2.2 Specifications in Order to Achieve the Required Objectives

2.2.1 Communication System Specifications

The emphasis of this module is to satisfy the needs of a direct-sequence broadband CDMA baseband system. The modulation scheme intended for this system is QPSK (Quadrature Phase Shift Keying)/DQPSK (Differential QPSK). The IF bandwidth supported by this module is 32 MHz, limited by the bandwidth of the IF SAW (surface acoustic wave) filter. The excess bandwidth intended for this system is between 40 to 100% depending on the details of the baseband unit. If the baseband unit utilizes an FIR pulse shaping filter such as a root raised cosine filter, then about 40% of excess BW would suffice and 23 MCPS (mega chips per second) of throughput can be achieved. This can be utilized in a 715 KSymbPS, 1.43 MbPS system with a processing gain of 32 or a 1.42 MSymbPS, 2.48 MbPS system with a processing gain of 16. Otherwise, if no FIR pulse shaping is utilized and the pulses are shaped by the band-limiting analog filters, then approximately 100% excess BW would be a reasonable sacrifice between ease of achieving initial synchronization, throughput, and overall required bandwidth (FIGURE 9). This will result in a system with a throughput of 16 MCPS which can be used in a 500 KSymbPS, 1 MBPS system with a processing gain of 32 or in a 1 MSymbPS, 2 MBPS system with a processing gain of 16. Of course larger processing gains can be accommodated at the expense of lower data rates (given the same modulation scheme).

2.2.2 CDMA Power Spectral Density

The spectrum of a CDMA signal is shown in FIGURE 9 along with a mathematical $[\sin(x)/x]^2$ function. It is clear from the figures, and can be shown that the shape of the *envelope* of the power spectral density of such a signal is in the form of $[\sin(x)/x]^2$ (and the voltage signal has the shape of $[\sin(x)/x]$)[1]. The peak of the first sidelobes are down by 13dB, and approximately 90% of the energy of the signal is contained in the

main sidelobe, and this fact must be considered when determining the excess bandwidth utilized in the system. The advantage of an FIR pulse-shaping filter is that it concentrates more of the energy in the main sidelobe, hence increasing the signal power but maintaining the same noise power. One form of an ideal, but unrealizable pulse shaping FIR filter would be a brick-wall LPF, which would maximize the SNR of the system by allowing the entire wanted signal in, but minimizing the amount of noise admitted in the system.

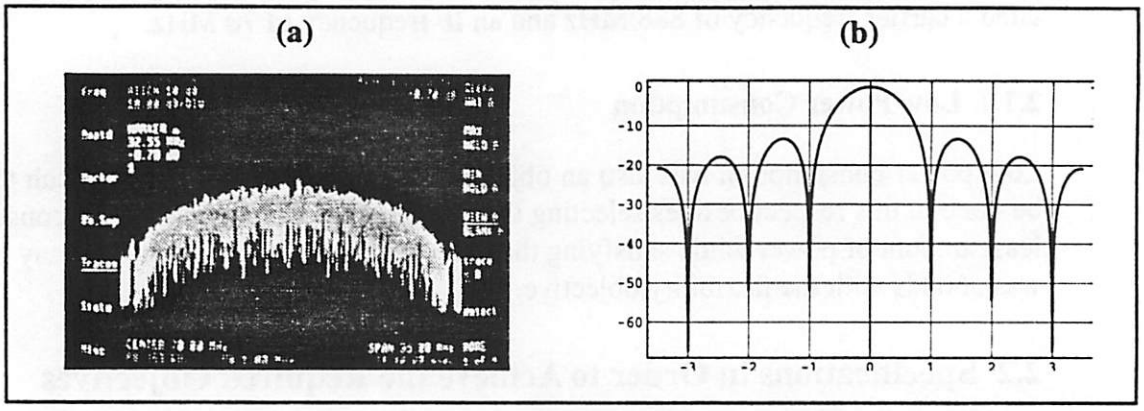


FIGURE 9. (a) The power spectrum of a QPSK modulated CDMA signal. (b) the mathematical function $[\sin(x)/x]^2$ **normalized and expressed in dB** ($10\log_{10}([\sin(x)/x]^2)$).

The loss of the out of band energy is not the only problem with bandlimiting the spread signal to the main sidelobe. Since most of the energy of the harmonic contents is contained in the sidelobes, the bandlimiting effectively smoothens the time-domain sharp edges of the transmitted pulses by the LPF action. Furthermore, the sharp triangular autocorrelation peak of the PN sequence shown in FIGURE 4 is rounded, resulting in potential difficulties in the timing recovery process.

It can easily be shown that the SNR can actually be increased by bandlimiting the receiver to less than the main lobe of the spread spectrum. This fact arises because of the non-white spectrum of the spread-spectrum signal (highest concentration of energy around the center frequency as shown in FIGURE 9). For example band limiting the receiver to 65% of the main sidelobe would reduce the signal power by only 5% (0.22 dB) as compared to bandlimiting the receiver to a full sidelobe as it can be verified by calculating

$$\text{Reduction in normalized signal power} = 1 - \frac{\int_0^{0.65} \left(\frac{\sin(\pi x)}{\pi x}\right)^2}{\int_0^1 \left(\frac{\sin(\pi x)}{\pi x}\right)^2} \qquad \text{(EQ 8)}$$

1. Although the figure shown is for a QPSK modulated signal, the shape of the spectrum, as seen on a spectrum analyzer would be the same for a BPSK signal or any other M-ary phase modulation scheme, since the spectrum analyzer does not display any phase information.

whereas the white noise power is reduced by 35% (1.9 dB). This results in an improvement in system SNR by approximately 1.7dB. The timing recovery, however is more difficult in this case, however, since the sharp peak of the autocorrelation function has been smoothed out even more so than before.

In summary, the excess bandwidth of this system is adjustable and determined by the baseband circuitry. An optimal value of excess bandwidth would insure the proper operation of the system while maximizing the throughput for a given BER.

2.2.3 Use of This Board for Other Modulation Schemes

This board is simply an "RF channel" and can be utilized with any baseband modulation scheme such as QAM64 (64-constellation quadrature amplitude modulation). High order constellation modulation schemes, however, are usually used on more reliable channels such as wired links and not over wireless channels.

3.0 An Overview of the Transceiver Architecture

3.0.1 Board Block Diagram

The simplified block diagram of the transceiver is shown in FIGURE 10. It is important to realize that, as implemented, the receiver acts as the receiver in the portable units, whereas the transmitter would be used in the base-stations. This transceiver, thus, forms a complete broadband transmission/reception system. In the final version of the infopad, the channel is asymmetric: i.e. the data-rate in the downlink is very high in order to support real-time video, whereas in the uplink it is relatively low, only enough to support raw data for pen and speech recognition. It has therefore been decided to use a CDMA in the downlink and TDMA in the uplink and therefore the structure of the final version of the receivers (and transmitters) in the base-station will be different than that of the mobile units.

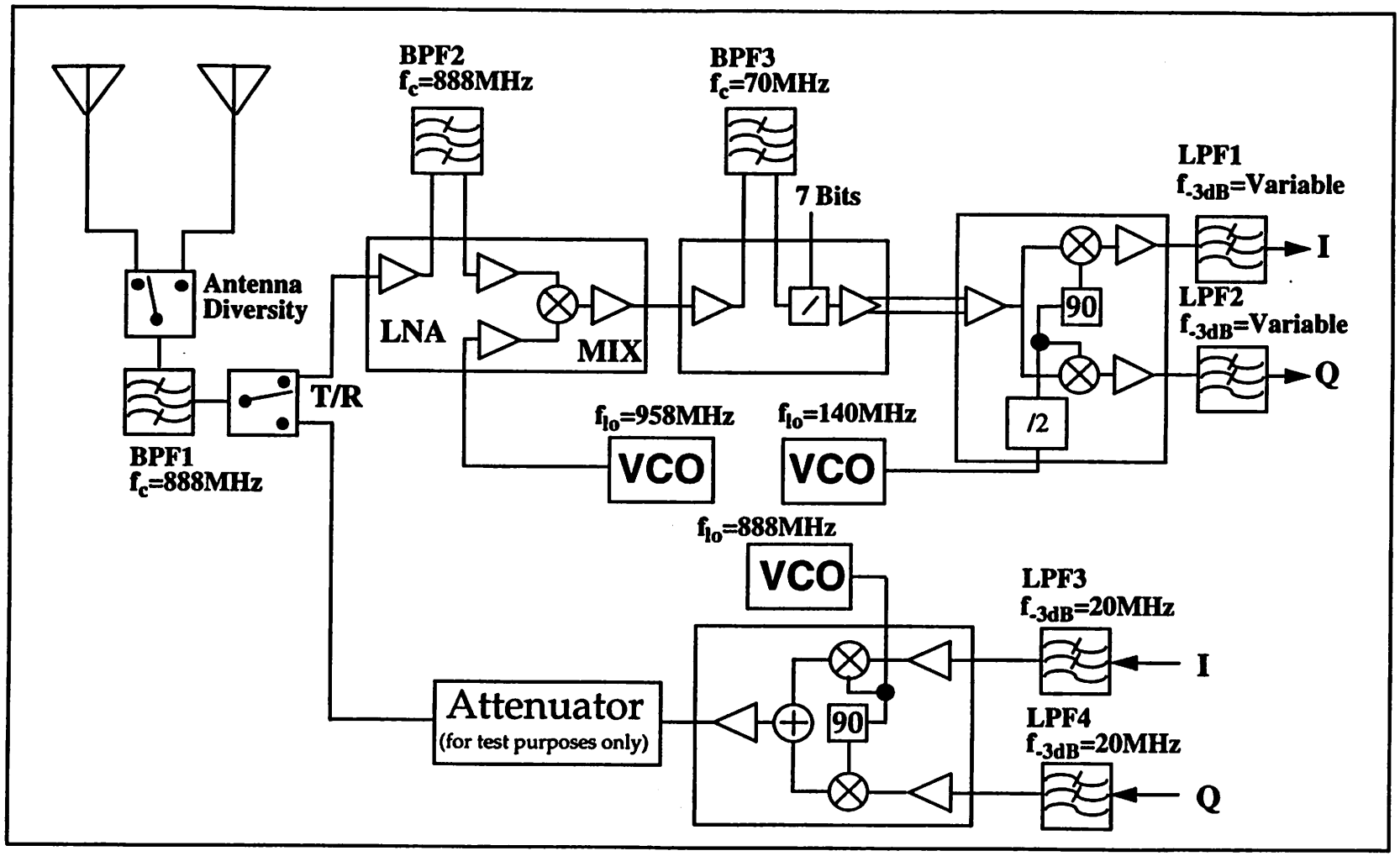


FIGURE 10. Simplified block diagram of the transceiver

3.1 The Receiver

The receiver uses two antennas in order to achieve antenna (spacial) diversity. The use of two antennas provides some immunity to deep fades due to multipath response (See section 4.1.2, "Multipath Fading"). The antenna with the stronger magnitude signal is selected by an auxiliary analog circuit or through baseband DSP which would switch the high speed GaAs antenna diversity switch to the proper state (for test purposes manual selection can also be made). This signal is then fed into a ceramic preselect filter operating at 888 MHz, with a bandwidth of 32 MHz. The signal then passes through the transmit/receive switch (in the receive mode) into the input of the LNA (low noise amplifier)/mixer IC. An external ceramic filter identical to the preselect filter rejects any image components. Furthermore, even in the absence of any received image components, the filter will reject the *image noise* component, improving the noise performance of the system (See section 4.4.1.2, "The use of Filters to avoid noise aliasing in the system"). The signal then is passed back into the chip for down conversion to the 70 MHz IF frequency. At 70MHz, the signal is filtered with a simple LC filter, and passed onto the first stage of the IF VGA (variable gain amplifier). After this first stage the signal is passed off-chip to a SAW filter, and then taken back on chip to the second stage of the VGA. Internal to this stage, the signal is converted from single ended to differential. This is done so that the signal becomes insensitive to common mode interferers that can couple in. This is particularly important because no filtering is performed at this stage. The analog I/Q (in-phase, quadrature-phase) demodulator then converts the signal to a baseband signal or to a lower IF frequency where it could then be directly sampled at IF by two A/D converters or even one A/D converter using the *I* or *Q* output to perform a simple (not a true single sideband) down-conversion digitally. The LO (local oscillator) for the demodulator is provided by a third-overtone crystal oscillator. This LO frequency is actually 2x the IF frequency (if it is desired to take the signal to baseband) to simplify the generation of the *I* and *Q* LO's and is divided internally by 2 to generate the 90° offset (sin, cos) required for I/Q demodulation. The *I* and *Q* signals are then passed into anti-aliasing filters prior to being sampled by the high-speed A/D's.

3.2 The Transmitter

The transmitter structure is based on a single stage analog up-conversion scheme. The baseband signal can be fed directly into the *I* & *Q* ports of the transmitter or they can be up-converted to some IF frequency in the digital domain (or analog domain), and then fed into the *I* and *Q* inputs. The I/Q modulator has an output power of approximately 0 dBm (1mW), which would suffice for most of our indoor communication needs, avoiding the need for a power amplifier. The modulator is followed by a voltage controlled attenuator which is used primarily for test purposes in the channel characterization. The signal is then fed into the T/R switch (in the transmit mode), the band-limiting transmit filter, the antenna diversity switch and into the antenna. Depending on the antenna structure used, some kind of external transformer (e.g. balun) may be required for impedance matching the antenna to the transmitter for maximum power transfer or to the receiver for best noise performance (See section 7.5, "Impedance Matching of the Antenna").

4.0 Receiver Dynamic Range

In most front-end receiver systems, the most important specification of the system is its dynamic range. The dynamic range of the receiver determines the range by which the system can properly receive the data and pass it on to the baseband unit. In the high end, the dynamic range is limited by the distortion of the front-end components. In the low end, it is noise that limits the performance of the system.

4.1 Transmission Path Losses

In general there are several factors that attenuate the transmitted signal. A detailed analysis can be made by solving Maxwell's equations. A grossly simplified model for the channel attenuation can be formulated as follows:

$$L\,[\mathrm{dB}] = -\,[\text{reference 1m path loss} + A\log_{10}(d) + \text{Maximum multipath fade}] \qquad \text{(EQ 9)}$$

Where L is the channel attenuation and d is the propagation distance. The reference 1 meter path loss accounts for the near field attenuation of the signal, where the electric and magnetic fields must be considered separately, and not as a TEM wave where the electric and magnetic fields are in time phase but space quadrature.

4.1.1 Distance Based Path Loss

The second term above accounts for the distance based attenuation of the signal, and in most cases is the most significant attenuation factor. A is very much environment dependent and is the exponent in the d^{-A} attenuation factor. A has been measured to be as low as 2 and as high as 6 for an indoor environment ([7], [6], [2]), although the extreme low and high ends occur under special circumstances only. For example a distance based attenuation with a 6 factor could occur in a very humid environment when the transmission frequency is about the resonant frequency of the Oxygen-Hydrogen bonds of water (one of the Industrial, Scientific, Medical--ISM--bands for example). At the other extreme, if a spherical spreading of the wave-front is assumed and it is further assumed that no energy is absorbed by the medium (a major assumption), the signal would attenuate as d^{-2}. A widely accepted A factor for a "typical" indoor environment is A=2.6 [2]. Note that in reality, the multipath indoor channel can be very complicated with different A factors in different regions within the building, resulting in a *non*-spherical distance based attenuation contour.

4.1.2 Multipath Fading

The third factor, the "multipath fade," is also very much environment specific, but would typically not exceed about 20dB in an indoor environment (FIGURE 8). Multipath is a phenomena caused by the multiple arrivals of the transmitted signal to the receiver due to reflections off of "scatterers." The gain and phase of these reflections can be modelled as being somewhat random. Multipath is usually much more of a problem if a direct line-of-sight (LOS) path does not exist between the transmitter and the receiver. In this scenario,

the *change* in the magnitude of the received vector as compared to the mean value of the magnitude of the received vector is small, resulting in a Ricean distribution (FIGURE 12). FIGURE 12.b shows the vector-space representation of the multipath reception in the presence of a LOS path. Vector $\vec{a}$ represents the resultant vector from the LOS path (1) and the multi-path receptions (2), (3), and (4). The magnitude of vector $\vec{r} = \|r\|\angle\phi$ represents the *mean value* of the possible resultant vectors. The area of the circle indicates the 50% contour for this Ricean distribution. It is clear from this figure that multipath response rarely affects the decision variable significantly in such a scenario.

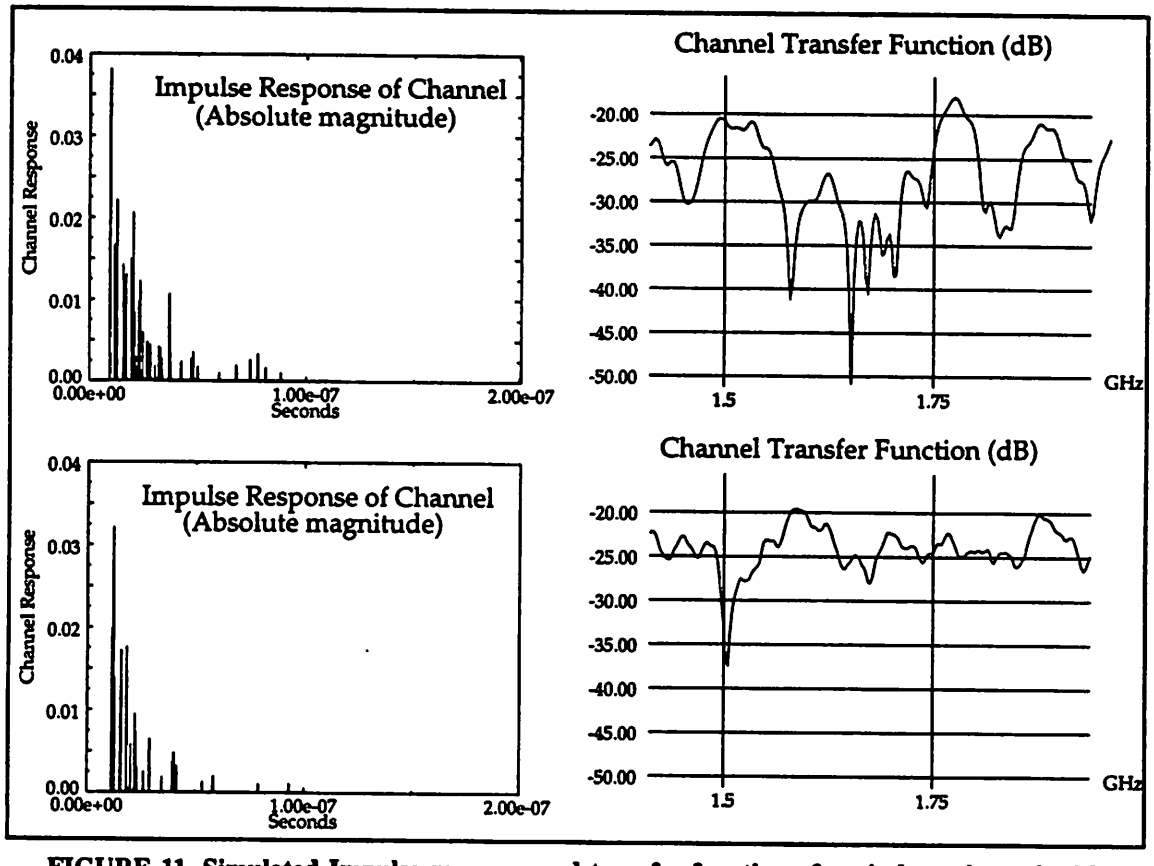


FIGURE 11. Simulated Impulse response and transfer function of an indoor channel with no multipath fading at 1.5GHz (top) and with a severe multipath null at 1.5GHz (after [2])

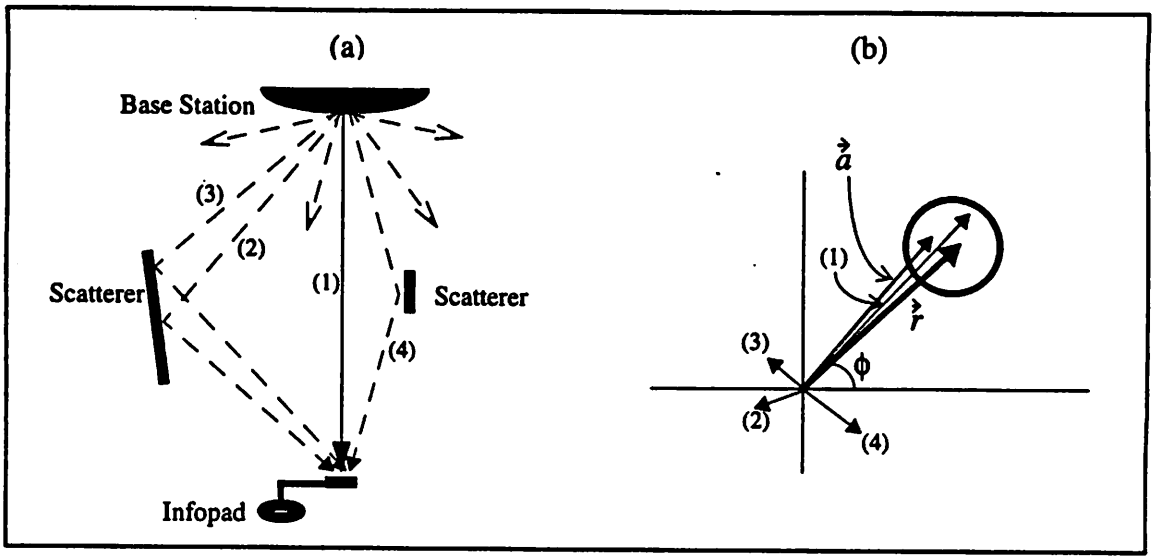


FIGURE 12. (a) Multipath in the presence of a line-of-sight signal (b) Vector-space representation

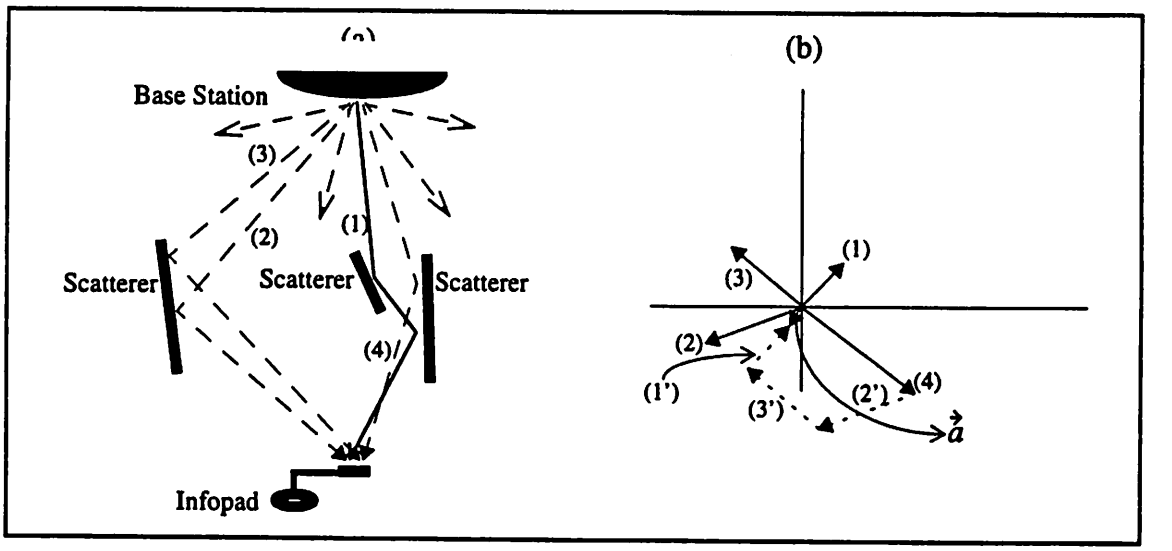


FIGURE 13. (a) Multipath response in the absence of a line-of-sight signal (b) Vector-space representation. Note that the vector magnitudes have been scaled 2:1 as compared to FIGURE 12 in order to simplify visualization.

FIGURE 13.a. displays the multipath channel in the absence of an LOS path. FIGURE 13.b. shows the vector-space representation of such a response. Vectors (2), (3), and (4) represent the reflected signals at the receiver. Vector (1) represents the intended LOS signal which has been interrupted and reflected multiple times by the scatterers. Vectors (1'), (2'), (3') and (4') represent the vectors used to find the resultant vector, $\vec{a}$. It is clear that vector $\vec{a}$ is very small in magnitude, resulting in a high probability of error at the slicer. For large number of scatterers, the channel can be modeled to have a Rayleigh distribution, with about 10% probability of a resultant vector with a magnitude less than half

the magnitude of the mean. Note that in this case the mean ± 25 % contour in the vector space is not a circle because of the asymmetry of the Rayleigh density function about it's mean value.

4.1.2.1 Antenna Diversity

Antenna Diversity, a form of spacial diversity, can be effectively utilized to reduce the effect of multi-path fades. A signal transmitted at the speed of light, c, at a frequency f, with a wavelength $\lambda = c / f$, will experience a delay $\tau = d / c$ in arriving to its destination (d is the *total* distance, accounting for all reflections). As a result, the transmitted signal will have a phase offset when received at the destination

$$\phi = 2\pi f\tau = 2\pi\frac{d}{\lambda} \qquad \text{(EQ 10)}$$

Any change in overall path length, d (due to the movement of a scatterer, the transmitter, or the receiver) causes a change in delay, τ which causes a change in this phase offset

$$\Delta\phi = \frac{2\pi\Delta d}{\lambda} \qquad \text{(EQ 11)}$$

It is clear from equation [11] that a Δd of $\lambda / 2$ would result in a 180° phase shift in the received signal. It is therefore important to note that only radial movement (and not angular movement) would cause a $\Delta\phi$ since Δd for angular movement about a point is 0.

FIGURE 14.a. shows a hypothetical situation where the only two signals containing any significant energy are those shown by (1) and (2). These signals are received at antenna A of a mobile unit such that $\angle\vec{S} = \angle\vec{S}' + \pi$ where $\vec{S}$ indicates the signal received through path (1) (transmitted over a distance $r_1 + r_{2a}$) and $\vec{S}'$ indicates the signal received through path (2) (transmitted over a distance r_1'). FIGURE 14.b. shows the vector-space representation of the two received signals as well as the resultant vector, $\vec{R}$. Now consider antenna B as shown in FIGURE 14.a. Assume antenna B is in a location such that the path for signal (2) remains r_1' but the transmit path for signal (1) is now $r_1 + r_{2a} - (\lambda / 2)$ where λ is the wave length at the carrier frequency. Using equation [11] the vector-space plot is shown in FIGURE 14. Now the vectors $\vec{S}$ and $\vec{S}'$ add instead of subtract. Note that at 1GHz, λ = 0.3 m and hence using two antennas that are physically $\lambda / 2$ apart is possible.

Clearly the hypothetical case considered above is an oversimplified representation of the situation. It does however give an intuitive feeling as to how antenna diversity helps combat multipath fades. Realistically, antenna diversity is more helpful in cases where no direct LOS path exists (since in this case usually no one received signal is dominant in magnitude). Furthermore, particularly when a direct LOS does not exist, one needs to be

concerned with more multipath responses than two. Even if only two signals were to be considered the received signals are not exactly 180° phase offset. However the two antennas would normally receive signals with powers that are significantly different. Although it is possible for both antennas to be in multipath fades concurrently, statistically this is an unlikely occurrence. This situation can occur, for example, in FIGURE 14.a if it is assumed that $r_1 + r_{2a} \approx r_1'$ (or equivalently $\alpha \approx 180°$) and antenna *B* is placed at location indicated by **X** in the figure, $\lambda / 2$ below antenna *A*. In this case *both* signals would go through a 180° phase shift which would result in the same $\|\overrightarrow{R}\|$ as indicated in FIGURE 14.b.

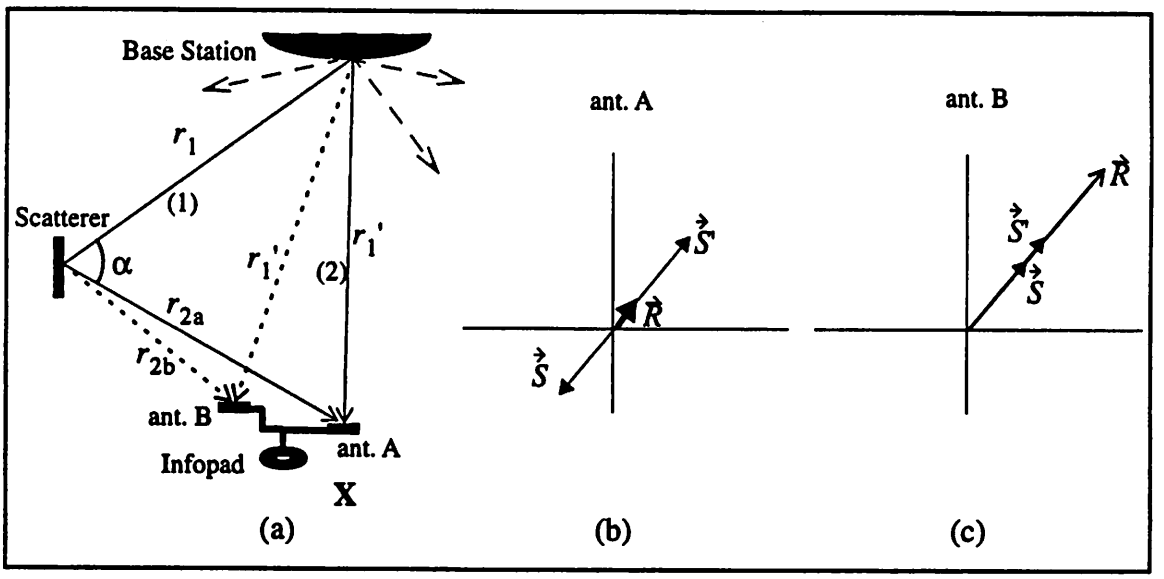


FIGURE 14. (a) Effect of antenna diversity on multipath response (b) Vector-space representation of the received signal at antenna *A* (c) Vector-space representation of the received signal at antenna *B*.

4.1.2.2 The Rake Receiver

Consider a "typical" indoor environment. The difference between the distance that two "significant" and comparable magnitude multipath signals would travel is typically between 3m to 15m. At the speed of light it will take the signal 10ns to 50ns to travel such a distance. This is defined to be the delay spread of the signal, τ_{ds}. In order to quantify "significant" a new variable, the RMS delay spread is defined. To obtain RMS delay spread, the delay power spectrum is normalized such that the area under the curve is equal to one. Taking the square root of the variance of the normalized curve results in the RMS delay spread. Using the "Ray" model [8] it can be shown that for a typical indoor environment with a probability of almost unity, the delay spread is greater than 10ns. This probability reduces to about 96% for a delay spread of 15ns and 45% for a delay spread of 31ns. These facts are used below in the discussion of a rake receiver.

A rake (otherwise known as maximum ratio combining) receiver is one which utilizes multiple "fingers" with each receiver tuned to a different multipath arrival. The decision variable for a rake receiver is based on a weighted sum of the received signals by each finger. Each finger is weighted proportionally to the amplitude of its received signal (hence the name maximum ratio combining), then *coherently* summed with the weighted results of the other fingers. In this way, the phase difference between the different path arrivals which can result in multipath fades is actually taken advantage of. In other words, if a rake receiver is properly used in a multipath environment, the decision variable would statistically be more reliable than a simple receiver in a non-multipath environment. Note that if the rake receiver is not properly designed such that the finger results are not summed coherently, the resulting rake receiver performance may be worse than a non-rake receiver. It can be statistically shown that it would suffice to use only three fingers for indoor environments ([8], [2]), since the Ray model predicts that the expected power in a path decrease exponentially as the delay increases, making the subsequent arrivals insignificant.

The coherence bandwidth of a system is defined to be the inverse of its RMS delay spread. In order for a rake receiver to be able to "resolve" multipath responses in an indoor environment it needs to have a sufficiently wide bandwidth. The receiver implemented here has an IF bandwidth of 32MHz and would statistically only be able to resolve 45% of the multipath arrivals if used as the front-end for a baseband rake receiver. The final version of the front-end for infopad, a single chip front-end has an IF bandwidth of 64MHz corresponding to a delay spread of 15ns. It can therefore statistically resolve multipath responses 96% of the time in a rake receiver configuration. Note that in a practical implementation of a rake receiver, a single front-end receiver feeds the multiple fingers (correlators).

It is important to note that for most practical purposes, in an indoor environment a rake receiver can only be implemented for CDMA systems (this is a major advantage of a CDMA system over frequency hop and TDMA systems). This is because a CDMA system offers an extremely wideband front-end without sacrificing system noise performance (See section 4.4.1.1, "Effect of CDMA on System Noise Bandwidth"). The simulated result of the advantage of a rake receiver over a simple receiver in a multi-user CDMA system is shown in FIGURE 8.

4.1.3 Total Calculated Signal Propagation Attenuation in this System

By using A=2.6, d = 5m (base-station to portable distance) and a maximum multipath fade of 20dB (in equation [9]), the total signal attenuation amounts to 63 dB. Considering the fact that the integrated spread spectrum transmit power is approximately 0 dBm, to the first order, this will require the receiver to have a sensitivity of at least -63 dBm[1]. As it is

1. Assuming that the received signal is band-limiting to the main sidelobe of the spread signal, approximately 10% of the signal energy (0.46 dB) is lost. This lost energy is small and is therefore ignored in this analysis.

shown in Section 4.4.3, "A Simple SNR / BER Model," the receiver sensitivity has to be much better when accounting for second order effects.

4.2 Doppler Shift in an Indoor Environment

Unlike outdoor channels, because of the slow speed of moving objects in an indoor environment, doppler shift of the carrier frequency, or even the doppler spread of the carrier frequency (resulting from the doppler effect on every received multipath signal), is insignificant and is typically ignored in the system design. For example the doppler spread for a carrier frequency of 1GHz with moving objects with a speed of 3m/s is about 20Hz.

4.3 Receiver Noise Figure

The overall noise factor of the receiver can be calculated by using the Friis NF formula for cascaded stages[1]

$$F_{Cascade} = F_1 + \frac{F_2 - 1}{G_1} + \ldots + \frac{F_n - 1}{\prod_{i=1}^{n-1} G_i} \qquad \text{(EQ 12)}$$

where $F_{Cascade}$ is the overall noise factor due to the contribution of all elements, F_1 is the noise factor of the first element, G_1 is its *available power gain*, and F_2 is the noise factor of the 2nd element, etc. Note that in this equation F_i, G_i are in absolute numbers and not in dB's (hence the name noise factor, as opposed to noise figure). Although useful for computer calculations, the above formula is cumbersome to deal with for hand calculations and does not shed much light into the detailed contribution of each stage to the overall NF. It is important in using the above formula to note that only the *noise factors* (in ratios) can be added as stated in equation [12]. It would be incorrect to calculate the *noise figure* (in dB) of each stage as referred to the input and add the contributions.

The two common methods for calculating cascaded noise figure are:

1. To find the contribution of each component to the input referred noise factor, add the contributions, and then convert to an input referred noise figure (i.e. using equation [12] directly).
2. To find the cumulative cascaded NF moving up from the *end* of the chain, taking two elements at a time[2] and using only the first two terms of equation [12].

---

1. This relation can be mathematically derived by using the definition of noise factor, $F = N_o / N_i G$ (where N_o is the output noise power, N_i is the input noise power, and G is the gain of the stage) and calculating the output noise contribution of each stage. Another method of driving this formula is the use of equivalent input noise temperature and its relation to noise factor.

FIGURE 15 summarizes the contribution of each element to the overall NF of this receiver using both methods mentioned above[1]. Row (1) in FIGURE 15 lists the noise figure (or insertion loss in the case of passive elements) of the components as listed by the manufacturer (except for the SAW filter as explained below). Row (2) uses the first method indicated above and equation [12] to calculate the system overall noise factor. For example the first entry in this row (i.e. "1.148") corresponds to F_1 in equation [12], the second entry, ("0.672") corresponds to $(F_2 - 1) / G_1$ in equation [12], etc. Therefore, if the entries in row (2) are summed and converted to dB, the overall NF of the system would be obtained (=7.46 dB). It is important to note that in the use of this formula, the equivalent power conversion gain of the passive stages is equal to the negative of their insertion loss, as listed in row (3). Row (4) in FIGURE 15 calculates the NF of the system using the second method mentioned above. Clearly the result obtained from this method, system NF=7.46 dB agrees with that obtained from the first method.

2. In this method, the gain used in the Friis formula is the gain of the first of the two elements. This calculation can also be done by starting at the front of the chain and moving back two elements at a time. In that case, however, the gain used in the Friis formula must be the gain of the cascade up to and including the first element of the two-element segment.

1. Clearly the dish-antenna shown in this figure is not the kind of antenna used in the Infopad! This is simply a symbolic representation for an antenna.

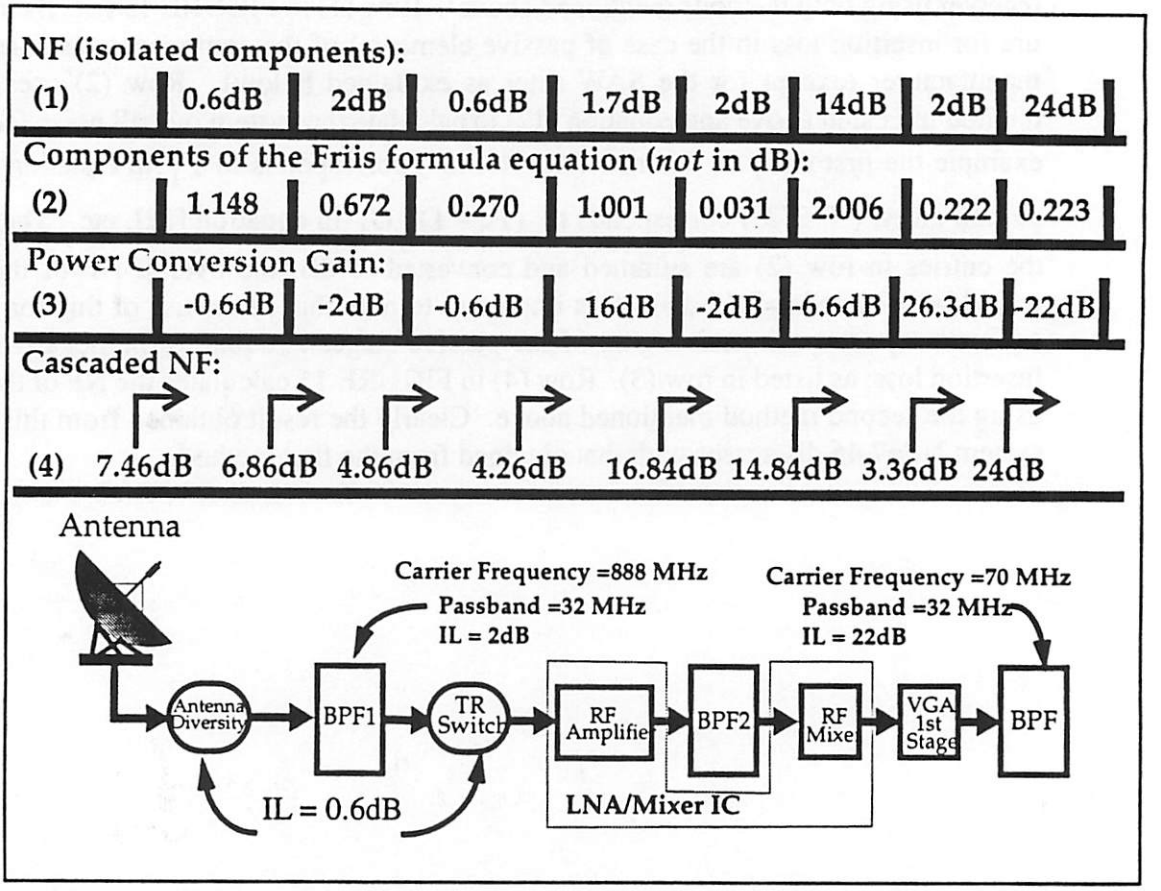


FIGURE 15. Noise figure calculation for the receiver. The overall NF of this system referred to the antenna is 7.46dB. See text for details.

In the Friis formula equation [12], one needs to account for the contribution of the elements starting from the very front-end until there is "sufficient" gain such that the noise contribution of the following elements are negligible. This is the reason for not accounting for the components following the SAW BPF in FIGURE 15.

Another point to make is that NF must be stated for a certain source resistance, and is otherwise meaningless. In the case of most high frequency front-end receivers, this source resistance is 50Ω (75Ω for most cable TV systems) which is also used as the characteristic impedance of the board transmission lines to achieve matching and avoid reflections. If the source and load resistances of each stage are equal (in this case 50Ω) then the power conversion gain is equal to the voltage conversion gain (in dB, or $A_p = A_v^2$ in ratios), and either one can be used in the Friis equation. Otherwise the available power conversion gain must be used to account for the unequal source and load impedances. The relation between the voltage conversion gain and power conversion gain of an active stage is given by

$$A_p = A_v^2\left(\frac{R_s}{R_l}\right) \qquad \text{(EQ 13)}$$

where A_p is the power conversion gain, A_v is the voltage conversion gain, R_s is the source resistance, and R_l is the load resistance of the active device (at its output).

The specified power conversion gain of the front-end mixer used in this system as specified in the data sheet is -2.6dB. This agrees with its voltage conversion gain of 10.4dB given that it is specified for $R_s = 50\Omega$ and $R_l = 1000\Omega$. In this system, however, the load resistance presented to this mixer is approximately 400Ω. Passive impedance transformation does not provide a significant improvement as explained in Section 7.8.1, "The RF-Mixer VGA1 Interface" and is therefore not used at this stage. Assuming the voltage gain of this stage is proportional to the value of the load resistance (a good assumption since the output of the mixer is an open collector stage driving the load resistance), the effective voltage gain in this configuration is reduced by a factor of 2.5 as compared to the specified voltage gain. The power conversion gain can be obtained by using equation [13] and is deteriorated to -6.59dB. This deteriorates the system NF by about 0.1 dB as compared to a $1K\Omega$ load for the mixer. Similarly, the voltage conversion gain of the first stage of the VGA (in the ON mode) is specified at 32dB. Once again the power conversion gain (=26.3 dB) has been calculated using equation [13] and used to calculate the system NF.

The Friis formula for cascaded noise figure can be used as long as the NF stated by the manufacturer (or calculated with some post-processing off of SPICE) is for the same source resistance as that used in the actual cascaded system. Otherwise, the NF should be calculated for the source resistance used in the system. For example, the NF of the first stage of the VGA used in this system is specified for a 400Ω source resistance at 2 dB. The effective source resistance in this system is approximately $1.6K\Omega$. The NF for this source resistance can be calculated from the noise factor equation [9]

$$F = 1 + \frac{\overline{v_i^2}}{4KTR_s\Delta f} + \frac{\overline{i_i^2}}{4KT\frac{1}{R_s}\Delta f} \qquad \text{(EQ 14)}$$

where $\overline{v_i^2}$ and $\overline{i_i^2}$ are the input referred voltage noise and current noise of the component. Clearly, equation [14] can be evaluated only if $\overline{v_i^2}$ and $\overline{i_i^2}$ are known, *if* one or the other is dominant. For example, if the voltage noise were dominant, the new F can be calculated from

$$F_{R_{s2}} = (F_{R_{s1}} - 1)\frac{R_{s1}}{R_{s2}} + 1 \qquad \text{(EQ 15)}$$

which in this system results in a NF of 0.59 dB for the component and a cascaded NF of 7.33 dB. Similarly, if the current noise is dominant, the new noise factor can be calculated from

$$F_{R_{s2}} = (F_{R_{s1}} - 1)\frac{R_{s2}}{R_{s1}} + 1 \qquad \text{(EQ 16)}$$

which in this case results in a NF of 5.23 dB for the component and 7.95 dB for the system.

Since $\overline{v_i^2}$ and $\overline{i_i^2}$ are not specified by the manufacturer and the optimal source resistance of this part for noise purposes is not known, a NF of 2 dB is used for the system calculations with the understanding the system noise performance may be slightly off from predicted.

It is essential to choose passive components with minimum insertion loss up front because of the lack of gain prior to these stages. The insertion loss of these elements add directly (in dB) to the system NF. This is one of the main reasons for the almost global use of ceramic filters as the preselect filters in high sensitivity receivers. The system designer, however, needs to be aware of the application. If the man-made noise and interference noise are significantly larger than the thermal noise referred to the antenna, the system performance would not improve by decreasing the system noise figure; i.e. the system is externally noise limited[1].

The main IF filter used in this receiver is a broadband SAW filter with very high insertion loss (nominally 22 dB, and 24 dB in this system because of the terminations used; Section 7.8.3, "VGA1-SAW-VGA2 Interface (Sensitivity of SAW Filters to Terminal Impedance Mismatches)"). If this filter were placed prior to the first stage of the VGA, the overall system NF would be increased to more than 20 dB and the system performance would degrade significantly. For this reason it has been placed after the first stage of the VGA which has 26.3 dB of available power gain.

On a practical point of view, it is important to note that spectrum analyzers typically have a NF of about 35 dB with the 10 dB attenuator engaged, and about 25 dB without the 10 dB attenuator. Therefore low noise figure measurements can not be done with a spectrum analyzer. A low-noise preamplifier can be utilized before the spectrum analyzer to reduce the NF of the spectrum analyzer.

The measured spot NF of this receiver is 8.1 dB at 888MHz input signal frequency with all stages at maximum gain setting. The excess NF over the predicted value is due to parasitic front-end component and board losses.

1. In an outdoor environment, below about 300 MHz, atmospheric noise dominates the antenna noise. Over 300 MHz, typically galactic noise dominates. Man-made noise typically dominates indoor environments and outdoor urban areas.

4.4 Receiver sensitivity

The sensitivity of the receiver (minimum required signal level for a given BER) in a digital communication system is a function of the total noise power at the input of the slicer and the modulation scheme used.

4.4.1 The Total Noise Power

The total noise power at the input of the slicer can be calculated by using the overall NF of the system, which is used to calculate the total noise of the system referred to the input. There are two methods to do this:

1. Using the common definition of *excess* noise factor (a measure of the *total* noise that all noise sources, including the source resistance, contribute to the system noise)

$$F = \frac{N_{oA} + N_{oB}}{N_{oB}}$$

$$= 1 + \frac{N_{oA}}{N_{oB}} \qquad \text{(EQ 17)}$$

where N_{oA} is the total noise contribution of the system (excluding the source resistance) and N_{oB} is the noise contribution of the source resistance. The noise factor calculated in section Section 4.3, "Receiver Noise Figure", however, is the so-called *operating* noise factor of the system, which excludes the contributions of a source resistance (radiation resistance of antenna, for example). The noise factor which should be used for noise power calculations in this case, therefore is given by

$$F_{op} = \frac{N_{oA}}{N_{oB}} \qquad \text{(EQ 18)}$$

Assuming the input referred current noise is negligible

$$F_{op} = \frac{\overline{v_i^2}}{4kTR_s\Delta f} \qquad \text{(EQ 19)}$$

where v_i is the input referred voltage noise, R_s is the source resistance (50Ω in this case), F_{op} is the calculated system operating noise factor, k is the Boltzman constant (1.38×10^{-23} Joules / Degrees Kelvin) and Δf is the bandwidth of the system. Solving for $\overline{v_i^2} / R_s$ in equation [19]

$$\frac{\overline{v_i^2}}{R_s} = (F_{op})\,(4kT\,\Delta f) \qquad \text{(EQ 20)}$$

The rms noise voltage of a source resistance is, however, equally divided between the source and load resistance if $R_s = R_l$ as it is typically the case for the front-end of high frequency receivers because of VSWR considerations. The "available" noise power of the system (delivered to the load) is therefore effectively reduced by a factor of 4 as compared to that given by equation [20][1], and is given by

$$N_{\text{available}} \approx \frac{\overline{v_i^2}}{4R_s} = (F_{op})\,(kT\,\Delta f) \qquad \text{(EQ 21)}$$

where N is the total noise power. Note that $kT\,\Delta f = 4\times10^{-21}\Delta f$ watts at room temperature (290 K). Using an effective noise bandwidth (Δf) of 1MHz (see Section 4.4.1.1, "Effect of CDMA on System Noise Bandwidth" for the reason for using 1MHz as opposed to the baseband spread bandwidth of 16MHz), and a noise factor of $F = 5.57$ in equation [21] we obtain $N = -106.5$ dBm.

or,

2. A simpler and more intuitive method would be to start from the thermal noise floor of $KT\Delta f = -174$ dBm/Hz at room temperature, add the bandwidth (in dB) to this number (60 dB for 1MHz), and finally deduct the receiver noise figure from the resultant number (7.46 dB, in this case). This method also results in a noise power of $N_{\text{available}} =$ -106.5 dBm.

4.4.1.1 Effect of CDMA on System Noise Bandwidth

It is important to make a few notes. At first glance, one may assume that a spread-spectrum system would degrade the noise performance of the system since they widen the bandwidth and therefore allow in more noise, by a factor equal to the processing gain. If this were truly the case, spread-spectrum systems would never find wide-spread use, and there would not be much advantage in using such a system. Intuitively, a direct-sequence spread-spectrum system requires a correlator in the receiver path somewhere in the chain (whether analog or digital). A correlator is effectively an integrator with a $1/s$ transfer function, which is also the transfer function of a low pass filter. The point is that the correlator effectively narrows the noise bandwidth by the spreading gain factor. A more rigorous proof of this fact is presented below using FIGURE 16.

1. The same is true for the signal gain calculations, i.e. the "available" power gain of the system must be used in above calculations. Manufacturers typically specify S_{21} which is effectively the available power gain of the component.

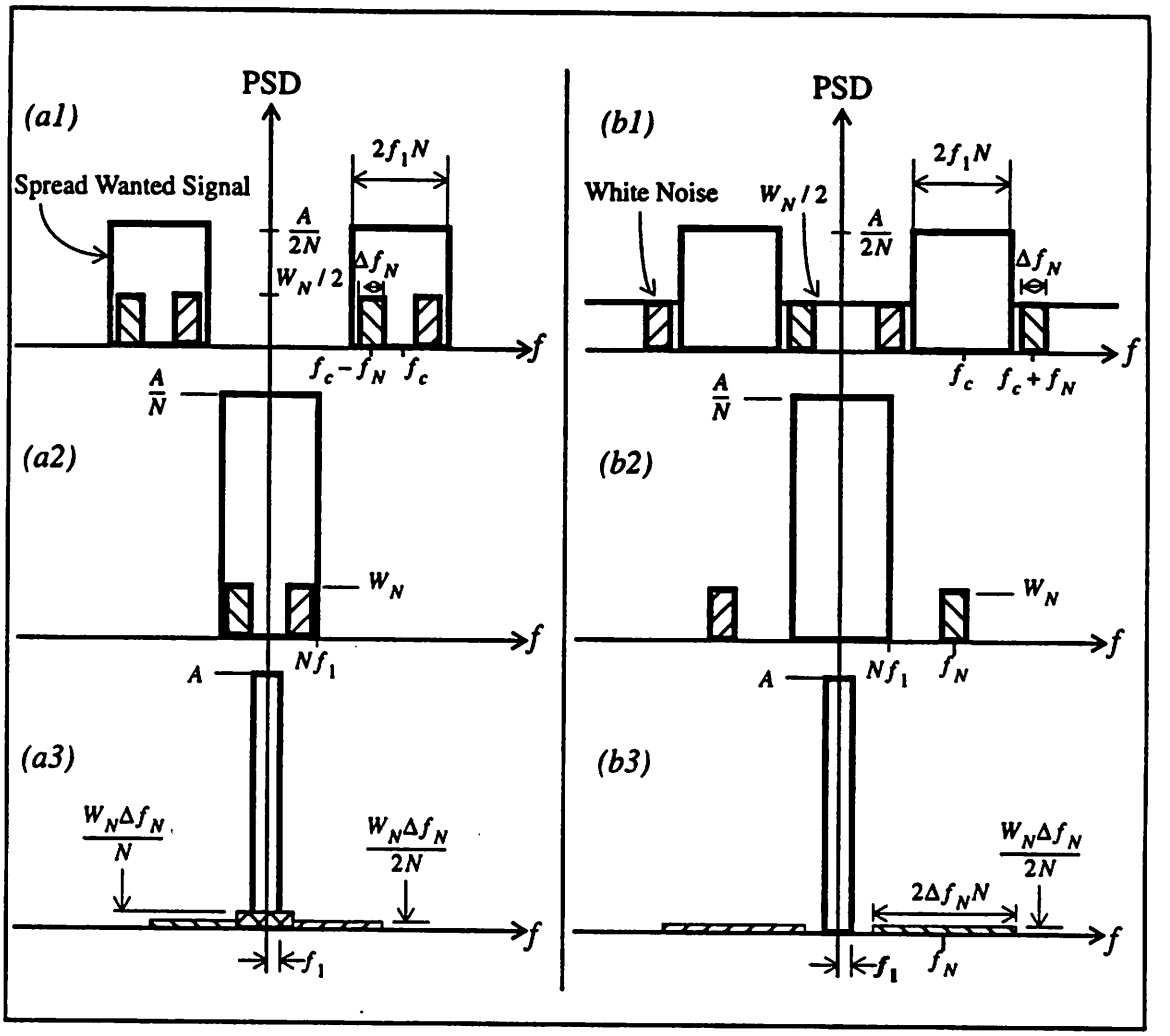


FIGURE 16. Effect of CDMA on white noise. *(a)* In-band white noise (a1) Modulated signal (a2) Down-converted to baseband (demodulated) (a3) Signal despread (noise spread) *(b)* Out of band white noise. (b1) Modulated signal (b2) Down-converted to baseband (demodulated) (b3) Signal despread (noise spread).

In FIGURE 16.a the effect of in-band white noise on a CDMA system is investigated. Consider a small frequency segment of the in-band noise, Δf_N, before demodulation and despreading, as shown in FIGURE 16.a1. The signal and noise are subsequently demodulated to baseband as shown in FIGURE 16.a2. After despreading, a portion of the noise Δf_N (which is now effectively spread), falls in the bandwidth of interest, f_1 (FIGURE 16.1c). Overall, there will exist $2Nf_1 / \Delta f_N$ noise segments of bandwidth Δf_N whose (spread) spectrum would fall within the decorrelators bandwidth. The overall noise power contributed by these noise segments would be

$$\frac{2Nf_1}{\Delta f_N} \bullet \frac{W_N \ \Delta f_N}{N} = 2f_1 W_N \qquad \text{(EQ 22)}$$

FIGURE 16.b1 through b3 illustrate that any out of band segment of noise would demodulate and subsequently spread (in the decorrelator) entirely out of the bandwidth of interest, and would therefore not contribute to the noise power. Therefore the overall white noise contribution to the CDMA system is $2f_1W_N$ which is *exactly* what would be obtained for a non-spread spectrum system.

Hence, a spread-spectrum system is "insensitive" to broadband noise. In this respect it neither has an advantage nor a disadvantage compared to non-spread modulation schemes.

4.4.1.2 The use of Filters to avoid noise aliasing in the system

The noise bandwidth of the system is determined by the narrowest filter bandwidth in the system *if* proper filtering is provided before each non-linear stage (in a CDMA system, it would be narrowest filter bandwidth / processing gain). In other words, it is not necessary to use a filter after each stage in the system in order to improve the noise performance of the system (although a filter may be required for other reasons). However before any non-linear stage (e.g. frequency mixing, analog to digital conversion, etc.) it *is* necessary to use a band limiting filter to avoid the mixing or aliasing of the noise back into the band of interest which would increase the system noise figure.

As discussed in Section 4.4.1.2, "The use of Filters to avoid noise aliasing in the system," despite a direct hit on the insertion loss, the use of the front-end filter, BPF1 in FIGURE 15, is necessary to avoid the saturation of the LNA due to strong out of band components. It may be conceived that the use of BPF2 is then not necessary since the image signal has been attenuated by more than 40 dB by BPF1 (see FIGURE 44). Even if 40 dB of image suppression were sufficient, the image noise of the broad-band LNA and the transmit/receive switch which have not been attenuated by BPF1 must be filtered before entering the mixer. If BPF2 is not used in this system, for example, the effective noise power at the input of the mixer will be increased by the noise power at the image band (1012 MHz to 1044 MHz) of the T/R switch and the LNA. In order to calculate the effect of the elimination of BPF2 on the system NF, it is assumed that the LNA gain and noise at the image band are approximately equal to that of the desired band[1]. The LNA and the switch can be combined into a composite element, with a NF of 2.3 dB and a gain of 15.4 dB. When BPF2 is eliminated the noise power at the input of the mixer is doubled, resulting in a composite element NF of 3.80. Using this value to calculate the system NF along with eliminating BPF2 in the chain results in a cascade NF of 7.72 dB, which is worse than that achieved with the filter in the system (7.46 dB). In reality, the composite element effective noise power at the input of the mixer may more than double, since higher frequency noise may mix with the harmonics of the LO and fold in band, deteriorating the NF even more.

An image reject mixer with a high image rejection capability would yield the best result; BPF2 could be eliminated without deteriorating system NF. On the other hand, achieving more than 30 dB of image suppression at 900MHz is difficult (See section 5.1.6, "Ampli-

1. In reality, the gain of the LNA is lower in this image band and its NF is higher.

tude and Phase Tracking in Image Reject Mixers"). Further more an image reject mixer typically requires more elements, resulting in a higher noise figure as compared to a non-image-reject mixer.

4.4.2 Modulation Scheme and its Effect on SNR Requirements

The modulation method of choice for the downlink high speed communication is differential quadrature phase shift keying (DQPSK). In a differential modulation scheme the slicer relies on the previous symbol in order to resolve the present symbol. Because of this fact, a DQPSK modulation scheme is relatively phase invariant (of course since it is a single-amplitude modulation scheme it is also relatively amplitude invariant). If the phase rotation of the arriving symbols due to the channel or receiver/transmitter hardware as compared to the symbol rate is small, the slicer will be able to slice the received symbol properly. This is one of the unusual situations where higher speed is easier to design for. Furthermore, coherent demodulation and sophisticated schemes such as Costas Loops are not required. Again, if the frequency offset of the demodulated signal from baseband causes a *small* constellation rotation between every symbol and its successor the slicer can properly slice the incoming symbols.

Differential modulation comes at an expense however. To achieve the same BER with DQPSK as compared to QPSK, 2.3dB to 3dB more SNR is required[1] [10].

4.4.3 A Simple SNR / BER Model

4.4.3.1 Low BER requirements for the Infopad: P_e VS SNR and P_e VS E_b/N_o

Many systems require very low probabilities of error (e.g. ethernet 10^{-10}). The Infopad system, however, is designed for a BER of only 10^{-3}. There are several reasons behind this choice. First, the Infopad is primarily intended for full-motion video. Simulations with BER of 10^{-3} do not show much degradation of quality to the observer compared to the very low BER's (because of the relative insensitivity of the human eye). However, if the BER is increased further, the video quality degrades significantly to the observer. Furthermore because of the refresh rate the pixels in error will disappear rather quickly[2]. Even in non-video type applications, the data is transmitted to the Infopads in bitmap fashion (e.g. Frame Maker), and not in ASCII format. If this were not the case, a BER of 10^{-3} would have not been acceptable since characters may have interchanged whereas in the bitmap mode a pixel or two of a character may get corrupted. Furthermore this is the

1. The noise variance of a DQPSK system is twice as large as a QPSK system (3dB worse), assuming that the noise terms for two succeeding samples to the detector are uncorrelated. It can be shown that the actual degradation in SNR due to differential detection is actually about 2.3dB at high values of SNR, when the correlation between the noise terms is taken into account.
2. In an MPEG2 compression scheme the error bits may not refresh quickly if they are in th "still" part of the video (e.g. background). Primarily due to its simple and low-power decompression algorithm, vector quantization and not MPEG2 has been used as the compression algorithm in the Infopad.

worst case scenario and the BER will decrease dramatically with a few dB's of SNR improvement (see FIGURE 17[1]). Finally, for critical information (header packets, etc.) forward error correction is used to achieve a significantly better BER.

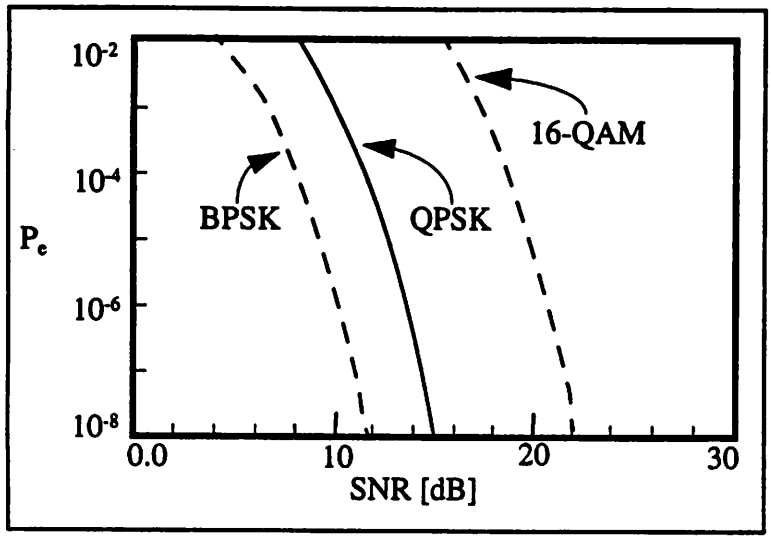


FIGURE 17. Probability of error as a function of SNR for various modulation schemes.

Given the above conclusions and assumptions, and assuming omni-directional antennas with no antenna gain (in reality the base station antennas will probably transmit downwards only, achieving an antenna gain of 3 dB), and using FIGURE 17[2] one observes that for a P_e of 10^{-3} in a QPSK modulation scheme, a SNR greater than 10.5dB is required. Accounting for the penalty due to differential modulation, the SNR required for DQPSK would be 12.9dB[3]. Therefore

$$\begin{aligned} \text{Min. Power Referred to the Antenna} &= \text{Total Noise Power} + \text{Required SNR} \\ &= (-106.5\ \text{dBm}) + 12.9\ \text{dB} \\ &= -93.6\ \text{dBm} \end{aligned} \qquad \text{(EQ 23)}$$

which is the minimum integrated spread spectrum signal power at the receiver antenna[4].

4.4.3.2 Effect of Multiple Users on Receiver Sensitivity Required

There is about 31 dB of margin in the receiver sensitivity with the above assumptions on transmission power (assumed 0dBm), path loss (assumed 63dB), and receiver sensitivity. One should recall however that this calculation was performed assuming a single user. The SNR required for multiple user in the system would increase for a given BER. In a CDMA down-link the deterioration of the SNR due to the co-users is much less pronounced than a CDMA up-link. This is because near perfect orthogonality can be guaranteed for the down-link but it can not be established for the up-link (See section 1.3.7, "Asymmetry of Channel as it Relates to the Codes"). The primary source of SNR degradation due to multiple users in the down-link is due to the multipath channel and is very difficult to mathematically model. Furthermore, the signal deterioration due to co-users is

significantly different for rake receivers versus non-rake receivers as shown in FIGURE 8. Using FIGURE 8 it is clear that in a deep fade channel, the BER for a 32-user non-RAKE system is approximately 30 times worse than that achieved for a single-user non-RAKE system. Using FIGURE 17, the SNR has to be increased by about 4dB in order to compensate for the added users and achieve a similar BER to the single-user system. Section 1.3.8, "Co-User Noise in an Uplink Channel," for a brief discussion of the effect of co-users on SNR for the up-link.

4.4.3.3 Effect of Adjacent Cell Interference in the Uplink on Minimum Receiver Sensitivity Required

Adjacent cell interference would require the allocation of even a higher SNR for the same BER. Assuming 6 adjacent cells (on the same floor of a building, for example), with the same number of users per cell, an empirical model has been developed for the adjacent-cell interference [5]

---

1. This figure displays the probability of *symbol* error as a function of SNR. Clearly, the bit error is always equal to the symbol error in the case of BPSK. In the case of a QPSK system, each erroneous symbol can result in one or two bits to be in error, resulting in a probability of bit error worse than that shown in FIGURE 17. If Gray coding is used, however, the probability of bit error approaches the probability of symbol error, particularly at high SNR, and therefore the probability of bit error curve as a function of SNR would be almost identical to that shown in this figure. Gray coding is a coding method by which the nearest constellation points have binary codes that only differ in one binary digit. Since the most likelihood error would be a symbol being mistaken for one of its closest constellation neighbors, this method of coding reduces the probability of bit error.

   Many publications plot P_e as a function of E_b / N_o (where E_b is the signal energy per symbol and N_o is the power spectral density of white noise (= W_N as used in this paper). For a PSK signal, the SNR can be related to E_b / N_o using the following relation

$$\frac{E_b}{N_o} = \frac{S}{N}\left(\frac{f_N}{R}\right) \qquad \text{(EQ 1)}$$

   where S/N is the SNR, f_N is the effective noise bandwidth, and R is the effective symbol rate. For the same data rate (bit rate) as an equivalent BPSK system, $R_{QPSK} = \frac{1}{2}R_{BPSK}$, but since nearest constellation points for QPSK are closer to one another ($d_{QPSK} = \frac{1}{\sqrt{2}}d_{BPSK}$), the signal power is also halved. Therefore the P_e vs (E_b/N_o) curve would be identical for BPSK and QPSK systems, particularly for high SNR. This can be intuitively understood by realizing that the I and Q signals are orthogonal, and therefore their probability of errors should not interact. This statement no longer holds for higher order M-ary PSK modulation schemes and the required E_b / N_o for a given P_e increases for these modulation methods.

   In a sense, FIGURE 17 is not a fair comparison since the effective bit rates of the different modulation schemes are different, whereas a graph of P_e vs (E_b/N_o) would take that fact into account.

$$F_{ac} \approx 4\left(1 - 2^{\frac{-1}{A}} + 4^{-\left(1+\frac{1}{A}\right)}\right) \qquad \text{(EQ 24)}$$

Where F_{ac} is the total adjacent cell interference and A is the distance based attenuation factor discussed previously. This equation results in a F_{ac} of 1.52 for $A = 2.6$ and F_{ac} of 1.28 for $A = 5$. This adjacent cell interference factor can be taken to be approximately equal to the factor by which the number of users is reduced in a system as compared to a system with no adjacent cells (equation [7] shows the effect of this variable on the overall number of users in an up-link CDMA system). It is clear from equation [24] that the larger the distance based attenuation factor A, the less the adjacent cell interference. equation [24] is plotted in FIGURE 18.

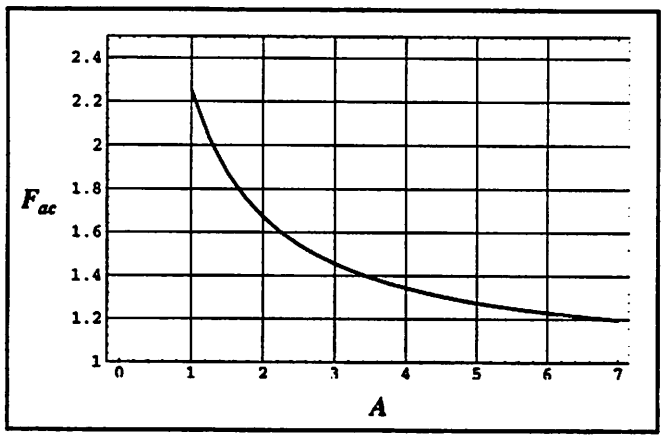


FIGURE 18. Adjacent cell interference factor as a function of the distance based attenuation factor A as predicted by equation [24].

With $A = 2.6$, and a resulting F_{ac} of 1.52, it is clear from FIGURE 8 and FIGURE 17, the SNR has to be increased by approximately 1.5dB in order to compensate for the effect of the adjacent cells.

2. FIGURE 17 is the plot of the following equation

$$P_{e_{QPSK}} = 2Q(\sqrt{SNR}) - Q^2(\sqrt{SNR}) \approx 2Q(\sqrt{SNR}) \qquad \text{(EQ 1)}$$

where Q is the "tail" of a Gaussian distribution function (1 - the Gaussian distribution function) [31].

3. The increase in BER for a given SNR due to the use of compression algorithms is ignored here.

4. Note that this is the *integrated* signal power at the antenna, and not the peak of the of the signal. Such a small magnitude signal, if relatively wideband, would be below the noise floor of many spectrum analyzers which typically have a NF of about (25 dB). With a reasonable spreading gain, most spread spectrum this signal would fall below the noise floor of a spectrum analyzer.

4.5 Receiver Linearity

4.5.1 Linearity as a Function of Modulation Scheme and Linearity of Stages

In general, in a receiver (for a given BER), the maximum allowable received input power is determined by the modulation scheme utilized and the "linearity" of the various stages in the system. The modulation scheme determines the maximum amount of non-linearity allowed in the system. In general hard-limiting based receivers in which the amplitude information is not used are much less sensitive to amplitude nonlinearities in the system. These receivers are frequently used with FM and PM in analog communications and FSK and PSK used with digital communications. Even in such systems, second order effects of "premature" front-end nonlinearities result in a degradation in the system SNR and an increase in BER in digital communication systems. This is particularly problematic when severe amplitude distortion generates phase distortion in some modulation schemes.[1]

4.5.2 Linearity Measures

The linearity of a receiver can be characterized by various means. A common non-linearity measure used for other systems, the harmonic distortion, is typically not used in the receiver design world. The reason lies in the fact that harmonic distortion components are typically significantly out of band and can therefore be easily filtered out. The most frequently used measures for the linearity of a receiver are the -1 dB compression point, $P_{-1\,dB}$, and the input referred or output referred third order intercept points, I_{IP3} and O_{IP3}. The -1 dB compression point refers to the input level power of a desired (in-band) single tone causing the output power of the device under test to deviate (reduce) from its linear value by 1 dB. The *third* order intermodulation products are caused by closely spaced input signals (for example, f_1 and f_2 which are in-band or slightly out of band) distorting and generating frequency components at or near the front-end frequency band of interest ($2f_1 - f_2$ and $2f_2 - f_1$). Since these signals are very close to the band of interest, it is practically very difficult or impossible to filter them. In general the only method of reducing the adverse effect of this kind of nonlinearity in the system is to reduce their generation. The O_{IP3} refers to the theoretical output power value where the linear gain would become equal to the third order intermodulation distortion in the system when two equal amplitude closely spaced tones are input to the system. O_{IP3} is related to I_{IP3} by the simple relation

$$O_{IP3} = I_{IP3} + G \qquad \text{(EQ 25)}$$

1. In general, limiting detectors reduce the effectiveness of a BPSK or QPSK modulated spread spectrum system and should be avoided if possible [3].

where G is the gain of the stage. I_{IP3} is usually of interest in receiver design, whereas in other systems such as power amplifiers (used in transmitters) O_{IP3} is usually of interest. Second order intermodulation distortion component, $f_1 - f_2$, can be important in the mixer stage of direct-conversion receivers but is usually filtered out in other systems and not of consequence.

It can mathematically be shown that under certain conditions[1] the third order harmonic distortion, the third order intermodulation distortion and the 1 dB compression point are related by the following equations [11]

$$IM_3 = HD_3 + 9.54 \text{ dB} \quad \text{(EQ 26)}$$

$$O_{IP3} = P_{-1dB} + 9.64 \text{ dB} \quad \text{(EQ 27)}$$

The desensitization level is defined as the input signal level of an *undesired* signal which would cause the device's small signal gain to be reduced by a specified amount. It can mathematically be shown that the 3 dB desensitization level is approximately equal to the 1 dB compression point of a device. Note that the 1 dB compression point refers to the output signal compression due to the high amplitude of a *desired* signal. For many narrow-band applications such as in the analog cellular phone system, the desensitization level is particularly important for the front-end components since adequate selective filtering of the undesired signals cannot be provided by the front-end filters and is typically achieved at the IF stage.

4.5.3 Cascaded Third Order Intercept

Several methods can be used to determine the input referred or output referred equivalent third order intermodulation intercept point of a cascade of elements. These methods are outlined below for calculating O_{IP3}.

1. The simplest method is to ignore the interaction between the intermodulation distortion of the various blocks in the chain and simply find the "weak link" by referring all the $O_{IP3,i}$ to the output of the cascade and estimate the overall $O_{IP3,\,cascade}$ to be equal to $\min\langle O_{IP3,i}\rangle$ where i refers to the ith stage of the cascade. This yields an overly opti-

1. These conditions are in general valid where the power series approach to distortion analysis is valid since they are derived using the power series approach. Some of these relations also hold in the frequency dependent distortion region (Voltera series) also, but in general these relations become too complicated with many frequency-dependent terms in the Voltera region. The major assumptions made for a power series based distortion analysis are that the gain is relatively flat as a function of frequency, the transfer functions are smooth, single valued, and contain no discontinuities or kinks, and that the effects of frequency dependent distortion is minimal. Note that these requirements are not necessarily mutually exclusive.

mistic result which is unlikely to be met in reality as the intermodulation distortion of all of the components do contribute to the overall intermodulation distortion level. In summary, using this method the following relations hold for an n-stage cascaded block

$$O_{\text{IP3, cascade}} = \min\left(O_{\text{IP3},i} \prod_{j=i+1}^{n} G_j \right) \qquad \text{(EQ 28)}$$

or in terms of dB

$$(O_{\text{IP3, cascade}})_{dB} = \min\left((O_{\text{IP3},i})_{dB} + \sum_{j=i+1}^{n} G_{j,dB} \right) \qquad \text{(EQ 29)}$$

where G_j is the power gain of the jth stage of the cascade.

The second and third methods of calculating cascaded intermodulation distortion take the cumulative effect of all of the elements in the chain into account and yield a more realistic result than the first method. The assumptions in obtaining the following results are that the gain and the input and output impedances are flat with frequency over the intermodulation distortion frequencies of interest and that the nonlinearities of the stages do not interact. The second method is differentiated from the third by the effect of the correlation coefficient, c.

2. In general the phase of the distortion products is not known. If the distortion components are perfectly correlated ($c = 1$), the intermodulation products will combine coherently increasing the IM levels (decreasing the intercept points). This yields a worst case result but for large systems it is probably the most accurate model as it is likely that somewhere in the chain the intermodulation components will actually add in-phase. It can be shown that for a two-stage cascade, the output referred intermodulation distortion is given by [12]

$$(O_{\text{IP3, cascade}})^{c=1}_{\text{2-stage}} = \frac{G_2 O_{\text{IP3,1}} O_{\text{IP3,2}}}{G_2 O_{\text{IP3,1}} + O_{\text{IP3,2}}} \qquad \text{(EQ 30)}$$

This equation can be used recursively to calculate the intermodulation performance of the cascade, starting from the *first* two blocks in the cascade. For computer implementations, the n-stage cascade third order intercept point is given by

$$[(O_{\text{IP3, cascade}})^{c=1}_{n\text{-stage}}]^{-1} = (G_2 \ldots G_n O_{\text{IP3,1}})^{-1} + \ldots + (G_n O_{\text{IP3},n-1})^{-1} + (O_{\text{IP3},n})^{-1}$$

$$= \sum_{i=1}^{n} \left(\prod_{j=i+1}^{n} G_i O_{\text{IP3},j} \right)^{-1}, \ (G_{n+1} \equiv 1) \qquad \text{(EQ 31)}$$

Note that in calculating the intermodulation intercept points using this method the intercept points are referred to the output (by multiplying each intercept point by the amount of gain following it) and then obtaining the cascade intercept point in an equa-

tion similar to that of the equivalent resistor of parallel resistors. Therefore, as expected, the smallest output referred intercept points determine the overall intercept point of the cascade.

3. If the distortion products are completely uncorrelated ($c = 0$), the output intercept point of a two-stage cascade can be shown to be [12]

$$(O_{\text{IP3, cascade}})_{\text{2-stage}}^{c=0} = \frac{G_2 O_{\text{IP3,1}} O_{\text{IP3,2}}}{\sqrt{(G_2 O_{\text{IP3,1}})^2 + (O_{\text{IP3,2}})^2}} \quad \text{(EQ 32)}$$

In this case, the denominator components add in an rms fashion (similar to the manner uncorrelated noise components add) resulting in a smaller denominator in equation [32] than in equation [31]. Therefore as intuitively expected the overall distortion performance of the chain is better in this case and this method yields a more optimistic result. Note that the parameters and the results obtained from equation [31] and equation [32] are *not* in terms of dB's.

In reality, usually the $O_{\text{IP3, cascade}}$ falls in between that predicted by the second and third method. If there is a major "weak link" in the chain which determines the ultimate intermodulation performance of the chain, all three methods yield approximately the same result.

4.5.4 Nonlinearities in This System

As mentioned in Section 2.1, "Requirements," this system is primarily intended for use on a DQPSK modulation scheme in a CDMA environment with a BER of 0.001 which requires a SNR of at least 12.9 dB for a single user system, and approximately 17 dB for a 32 user system (down-link and ignoring the adjacent-cell factor). As a first order approximation, it is assumed that the distortion components must be below the desired signal by an amount equal to the required SNR in the system. In order to allow for maximum flexibility and testing of various baseband systems and modulation schemes, the system can be used in a system with 8 bit A/D converters, requiring about 50 dB of SNR and SFDR under certain conditions[1].

In this receiver, the maximum input signal that the receiver can handle with "sufficient" linearity is primarily determined by the distortion the first stage of the VGA and the front-end mixer stage (in that order). "Sufficient" linearity can be approximated to be equal to the receiver third order intermodulation distortion in terms of dBc for the particular kind of modulation scheme used. This is because the harmonics and the even order intermit levels of the signal can typically be easily filtered out. In case of the existence of weak links

1. This amount of SFDR is typically not required in digital modulation schemes for wireless applications. For example, a single-user QAM-64 modulation with BER of 10^{-8} requires a SNR of approximately 28 dB. The SNR requirement for a multi-user QAM-64 in a multipath environment is difficult to predict; it is a very strong function of the multipath environment, and typically very high. High-constellation point modulation scheme are therefore typically not used in unpredictable environments such as wireless links.

in the receiver chain for high level inputs, the linearity of the system, to the first order, is specified by requiring the signal powers at the weak link elements to be a certain level below the third order intercept point (or 1 dB compression point) of those elements[1]. This maximum allowable signal can then be referred to the antenna and specified as the maximum allowable received signal for proper operation of the receiver. For example, given that the 1 dB compression point of the mixer is -4 dBm, the through mode loss of the LNA (S_{21}) is -7 dBm, the total insertion loss of the components prior to the LNA (i.e. filters, switches, etc.) is -5.2 dBm, and allowing for operations 20 dB below the -1 dB compression point of the mixer, we achieve

$$P_{in,max} = -4 - 20 + 5.2 + 7 = -11.8 \text{ dBm} \qquad \text{(EQ 33)}$$

This is certainly acceptable given the fact that the transmit power is about 0 dBm.

A (worst case) more accurate approximation to the maximum allowable signal may be made by the analysis of the nonlinearities of the system which is based on the 2nd method outlined in Section 4.5.3, "Cascaded Third Order Intercept,", using equation [31].

4.5.5 System Dynamic Range Performance

In this system, the system dynamic range performance can be calculated by requiring a 250 mVp-p (-25.9 dBm on 3KΩ) differential signal at the input of the demodulator IC. This level of signal will produce optimal performance on the demodulator with no relative linearity or noise limitation induced by the demodulator IC. With this assumption, the system variable gain must be adjusted to achieve such a signal on the demodulator inputs. The system power gain is then calculated and properly distributed among the gain elements. Clearly the power distribution can be achieved in various ways, with linearity and noise performance which are superior in some distribution methods as compared to others. In general, gain must be minimized prior to low IP_3 elements in the chain in order to minimize distortion generation in the system. On the other hand, gain must be maximized prior to lossy or noisy elements in the system for noise considerations. These requirements may be at odds for various gain settings. For example, in this system gain must be maximized prior to the SAW filter, but minimized before the first stage of the VGA.

1. The *accurate* calculation of the maximum allowable input level to the system and the quantitative effect of large input signals on system BER is difficult to determine analytically for large systems. Even with sophisticated time and frequency domain simulation tools obtaining such quantitative models is difficult. The complexity of the problem and the answer to the question is also very much a function of the modulation scheme used, and whether or not the signal is hard-limited or the amplitude information is actually used. The method presented in this section is a first order approximation.

   In general, angle modulation schemes are relatively insensitive to amplitude distortions in the system.

P_{in} = 0 dBm	Antenna Diversity Switch	Pre-Select Ceramic Filter	T/R Switch	LNA	Interstage Ceramic Filter	Front-end Mixer	IF VGA First Block	SAW IF Filter	IF VGA Second Block
NF_{stage} [dB]	0.6	2	0.6	7.0	2	14	15	24	12
NF_{cum} [dB][a]	0.6	2.6	3.2	10.2	12.2	26.2	34.4	43.1	54.6
$A_{P,\,stage}$ [dB]	-0.6	-2.0	-0.6	-7.0	-2.0	-6.6	0.26	-24	16.7
$OIP_{3,\,stage}$ [dBm]	45.4	100	45.4	19.0	2.0	-0.6	-1.0	100	5.0
$OIP_{3,\,cum}$ [dBm]	45.4	43.4	40.9	18.9	16.9	-0.9	-3.9	-27.9	-11.3
P_{out} [dBm]	-0.6	-2.6	-3.2	-10.2	-12.2	-18.8	-18.5	-42.5	-25.9
$IM_{3,\,out}$ [dBm]	-92.6	-94.6	-91.4	-68.3	-70.3	-54.5	-47.9	-71.9	-55.1

a. Starting from the front and referred to the antenna

TABLE 1. System dynamic range performance for P_{in} = 0 dBm.

Table 1 details the system dynamic range performance for an input signal level of 0 dBm. Clearly in this case the system performance is limited by the intermodulation distortion in the system, and particularly by the low intermodulation intercept levels of the front-end mixer and the first block of the VGA. Even under these circumstances, an IM_3 of 29.2 dBc is achieved which is sufficient for the single user spread spectrum system as described in Section 4.4.3, "A Simple SNR / BER Model," and marginal for a 32-user spread spectrum system. In reality, the output of the base station is 0 dBm, and considering the fact that the base station is at least 1 meter away from the portable units, an input signal power of 0 dBm is not likely to be received. Of course strong in-band interference (unwanted signals) of such a high level may occur which will degrade the system performance. The transmitters of the mobile units in the final version of Infopad will operate at a different frequency band and will therefore not interfere with the spread spectrum receiver.

Table 2 details the system dynamic range performance for an input signal level of -15 dBm. At this signal level both the intermodulation distortion and the noise performance of the system are limiting factors, but the system SNR and IM_3 [dBc] of over 50 dB ensure proper system operation for many modulation schemes, and certainly for a 32-user CDMA system.

P_{in} = -15 dBm	Antenna Diversity Switch	Pre-Select Ceramic Filter	T/R Switch	LNA	Interstage Ceramic Filter	Front-end Mixer	IF VGA First Block	SAW IF Filter	IF VGA Second Block
NF_{stage} [dB]	0.6	2	0.6	7.0	2	14	15	24	4
NF_{cum} [dB][a]	0.6	2.6	3.2	10.2	12.2	26.2	34.4	43.1	46.8
$A_{P,\,stage}$ [dB]	-0.6	-2.0	-0.6	-7.0	-2.0	-6.6	0.26	-24	31.7
$OIP_{3,\,stage}$ [dBm]	45.4	100	45.4	19.0	2.0	-0.6	-1.0	100	7.0
$OIP_{3,\,cum}$ [dBm]	45.4	43.4	40.9	18.9	16.9	-0.9	-3.9	-27.9	2.1
P_{out} [dBm]	-15.6	-17.6	-18.2	-25.2	-27.2	-33.8	-33.5	-57.5	-25.9
$IM_{3,\,out}$ [dBm]	-138	-140	-136	-113	-115	-100	-92.9	-117	-81.9

a. Starting from the front, and referred to the antenna.

TABLE 2. System dynamic range performance for P_{in} = -15 dBm.

Table 3 summarizes the system dynamic range performance for various input signal levels. The proper NF and output referred IP_3 has been used for each gain setting to obtain the overall system noise and distortion performance. In general, the NF of a variable gain stage increases with reduced gain settings and the input referred IP_3 increases (while the output referred IP_3 stays relatively constant). The details of the variation of IP_3 and NF with the gain settings are specific to the internal design of the particular stage and can vary significantly.

Due to several gain setting stages, the system performance can be optimized for a certain input level and gain by selecting a specific pattern of gain setting. For example, Table 3 shows the system performance for two different gain settings at an input signal power level of -40 dBm. Both the distortion and noise performance of the system is improved slightly in the second method. Often, however, a trade-off exists between the proper gain setting for noise performance versus the proper gain setting for distortion performance. Because of the multiple variable gain setting blocks, the VGA control circuitry should "intelligently" select the proper gain settings for the optimal system performance. The strength of the received signal along with the apriori knowledge of the system front-end should be used to develope the variable gain control circuitry algorithms where the full dynamic range capability of the front-end system is to be utilized.

Input	Cascaded NF [dB]	"Min. Detectable Signal" [dBm]	SNR_{out} [dB]	Cascaded Power Gain [dB]	Gain Settings[a] (LNA, VGA1, VGA2)	Power Level @ Demod. Input	IM3 [dBc]	$OIP_{3,cum}$ [dBm]	$IIP_{3,cum}$ [dBm]	Limiting Factor
0.00	54.6	-59.4	*59.4*	-25.9	-7, 0.3, 16.7	-25.9	*29.2*	-11.3	14.6	DISTO
-15.0	46.8	-67.2	*52.2*	-10.9	-7, 0.3, 31.7	-25.9	*56*	2.1	13.0	BOTH
-40.0	26.9	-87.1	*47.1*	14.2	-7, 32.3, 24.7	-25.9	*52.3*	0.3	-13.8	NOISE
-40.0[b]	25.7	-88.3	*48.3*	14.2	16, 0.3, 33.6	-25.9	*55.7*	1.9	-12.1	NOISE
-60.0	7.46	-106.5	*46.5*	34.1	16, 32.3, 21.7	-25.9	*47.7*	-2.1	-36.2	BOTH
-80.0	7.46	-106.5	*26.5*	54.1	16, 32.3, 41.7	-25.9	*67.1*	7.6	-46.5	NOISE
-93.6	7.46	-106.5	*12.9*	58.5	16, 32.3, 46	-35.1	*86.1*	7.9	-50.6	NOISE
-100	7.46	-106.5	*6.5*	58.5	16, 32.3, 46	-41.6	*98.8*	7.9	-50.6	NOISE

a. $-7\ dB < A_{P,\,LNA} < 16\ dB$, 2 settings; $0.3\ dB < A_{P,\,VGA1} < 32.3\ dB$, 2 settings; $7\ dB < A_{P,\,VGA2} < 46\ dB$, 64 settings.

b. Different gain setting comparison

TABLE 3. System dynamic range performance summary for various input signal levels referred to the antenna.

Although it is in general true that at high signal input levels the system performance is limited by distortion considerations and at low input signal levels by noise considerations, the system limitation may not monotonically change in between these two extremes due to various possible gain settings in the systems. For example, in this system at -40 dBm and -80 dBm input signal levels, noise limits the system performance. However, at -60 dBm, both the front-end gain stages must be set to a maximum gain setting in order to deliver the desired signal to the input of the demodulator. With such a high level of front-end gain at this input level the first block of the VGA starts to compress and the system OIP_3 reduces significantly.

As evident from Table 3, this front-end system can provide over 45 dB of SNR at the output with a relatively low intermodulation distortion for input powers of about -10 dBm to -65 dBm. Below -65 dBm the available output SNR drops such that at -93.6 dBm of input power level the output SNR is 12.9 dB, sufficient for a single-user Infopad system. This agrees with the result derived in equation [23].

The mixer is a limiting element in our system for strong input signals because for such signals where front end gain is not required, the LNA could be set to a bypass mode where it basically turns into a lossy MOS bypass switch, and its input IP_3 increases to 26dBm.

Therefore in this mode of operation, the LNA is no longer the limiting distortion component.

4.6 Dynamic Range Requirements for Analog Systems As Compared to Digital Systems

In general, digital modulation schemes can achieve extremely good BER's for relatively low SNRs. For example a good quality analog NTSC TV requires an SNR of more than 45dB, whereas an equivalent QAM64 modulated video signal would require an SNR of about 28dB for a BER of 10^{-8}.

5.0 System Components

Several factors are considered in selecting the appropriate commercial components for this module. Linearity, noise, power consumption and the availability of a power-down mode, size (footprint), requirements for impedance matching and cost were among these considerations.

5.1 The LNA/MIXER

The Philips Signetics NE600 was used as the LNA/mixer in this system. The general issues involved in the selection and use of front-end LNA's and mixers are outlined below along with the particular aspects related to the NE600. The issue of power conversion gain vs. voltage conversion gain is covered in Section 4.3, "Receiver Noise Figure".

5.1.1 Small Input Shunt Inductance to LNA

By using an external shunt inductor of approximately 15 nH at the input RF port of the LNA, the NF of the LNA and hence the entire system is improved by approximately 0.3 dB. Furthermore input matching, S_{11}, is also improved by about 3.6 dB. The LNA gain also slightly increases. The reason for this phenomena is that the shunt inductor effectively tunes out some of the input capacitance of the LNA, providing for more gain at higher frequencies (and hence a better NF), and a better *resistive* 50 Ω impedance (since the input impedance of the LNA is capacitive) and hence a better S_{11} (FIGURE 19). This technique is more effectively used with GaAs devices since for bipolar devices the base resistance of the front-end transistor buffers the input capacitance from the external inductor reducing the effectiveness of the tuning process.

5.1.1.1 Impedance Matching at the Input of the LNA Using a Smith Chart

The optimal value of the tuning inductor can be obtained by various methods. One method would be to use the Smith Chart. FIGURE 19.a displays the loci of points obtained on a Smith Chart by increasing the value of the shunt inductance at the input of the LNA. The reflection coefficient of the LNA is measured to be $\Gamma = 0.332\angle -162°$

($|S_{11}|$ = −9.57 dB , VSWR = 1.99 : 1, Z = 25.66 - j 6.62 Ω) at 958 MHz, the center frequency of operation[1]. This untuned reflection coefficient corresponds to point ❶ in FIGURE 19.a. By using an *ideal* shunt inductance of 18 nH we obtain point ❷ in FIGURE 19.a. This point corresponds to $\Gamma = 0.29\angle 0°$ ($|S_{11}|$ = −10.66 dB , VSWR = 1.82 : 1, $Z = 27.33 + j\,0\Omega$), a 1 dB improvement in the return loss. The actual measured improvement in return loss is approximately 3.6 dB at 958 MHz. Point ❸ in FIGURE 19.a corresponds to a shunt inductor of 0 nH which as expected corresponds to the short circuit point on the Smith Chart.

It is important to note that the matching is implemented for a particular frequency. One advantage of using a Smith chart is that after the narrow-band match is implemented, its effect on a wideband system can be observed on the Smith Chart. In this case since the bandwidth of interest (32 MHz) is relatively small as compared to the center frequency, our result yields an improvement in the broadband match also.

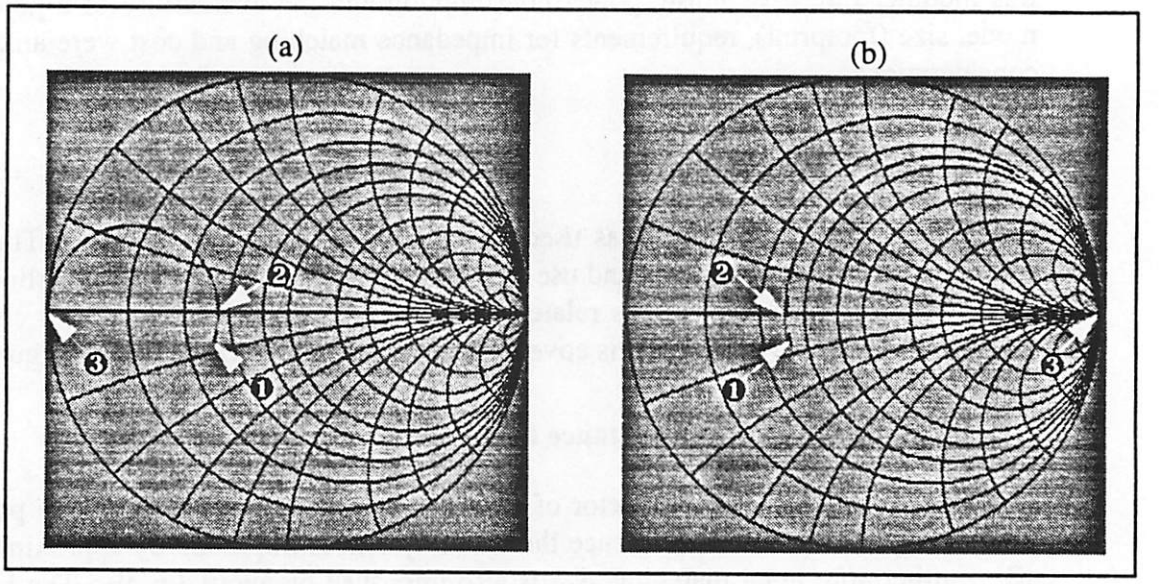


FIGURE 19. The effect of a tuning inductor at the input of the LNA on the input match, S_{11}. (a) Using a single ideal shunt inductor and (b) using a single ideal series inductor.

FIGURE 19.b displays the effect of a series tuning inductor on the input match of the LNA. Similar to FIGURE 19.a, point ❶ corresponds to the unmatched case of $\Gamma = 0.332\angle -162°$ ($|S_{11}|$ = −9.57 dB , Z = 25.66 - j 6.62 Ω) at 958 MHz. Point ❷ corresponds to the best match obtainable by using this method, with a *series* inductor of 1.1 nH, with $\Gamma = 0.320\angle 0°$. Clearly in this case this method does not yield much improvement to the input match and the other parameters. Furthermore, the value of 1.1 nH is too small to realize reliably. Point ❸ in this figure corresponds to an infinite large series

1. This value is slightly more capacitive than that specified by the manufacturer.

inductor and as expected yield the open circuit point on the Smith chart. There are situations where a series match would yield a better result than a shunt match.

5.1.1.2 SRF of the Tuning Inductor at the Input of the LNA

The self resonance frequency of the inductors should also be considered in implementing this match. Since typical 15 nH surface mount inductors are very close to their self-resonant frequency at 958 MHz, a smaller value inductor (with a higher SRF) may actually yield a better shunt match. At 958 MHz the result obtained for the 15 nH inductor was almost identical to that of a 10 nH inductor. At the lower frequencies however, the 10 nH inductor yielded a slightly better result and at frequencies above 1 GHz, the 10 nH inductor yielded a better result.

5.1.2 Impedance Matching to External Filters

The two-stage LNA provides 50Ω input and output matching. At the output the matching is obtained by the use of combined local series and shunt feedback internally to the chip. In order to minimize the NF of the LNA, however, at the input, inductive emitter degeneration (using the bond-wire of the package) has been utilized. This inductance, when referred to the input by the capacitive high-frequency beta roll-off, results in a resistive input impedance ($Z_i \approx \beta(j\omega) Z_E = 2\pi f_T L_E \approx 50\Omega$) [13]. The 50Ω matching provided by the LNA satisfies the termination requirements of front-end RF filters. The input of the mixer is also 50Ω matched. Therefore no impedance matching is required at the RF ports. The output of the mixer however, is an open collector. The gain of the mixer is defined by using an external pull-up resistor (in parallel with a choke which is used for biasing the collector) to V_{cc}. In order to provide for sufficient gain, this resistor should nominally be about 1KΩ. In a narrow-band application, this is also a good choice of input impedance for the IF filter. This is because narrow-band IF filters (e.g. SAWs) typically require about 1KΩ of input and output impedance, and hence no impedance matching would be required at this stage. In the case of this system, however, the filtering needs are quite different. In a narrow band application, such as the 900 MHz cordless telephone, it is usually required to filter the incoming signal to the bandwidth of interest before a significant amount of gain. Since this selectivity cannot be provided at the RF front-end (because of the high-Q filters required), it is typically provided *before* any IF amplification so that an undesired signal (within the RF bandwidth) would not saturate the IF stages. In a broad-band system where the RF bandwidth is approximately equal to the IF bandwidth it is not necessary to place such a filter immediately before a high gain stage. In this system, for example, the SAW IF filter is placed after the first IF gain stage (with a voltage gain of 38 dB) in order to reduce the NF. A simple LC filter has been placed after the RF mixer in order to attenuate the high-band mixer output and the LO leakage through the mixer.

5.1.3 Local Oscillator Frequency Selection

In this system the choice of the carrier frequency was made primarily by the "immediate" availability of commercial filters and VCO's for that frequency. But in general, given a carrier frequency, should one use a local oscillator frequency which is higher than or lower than the carrier frequency? In other words should $f_{lo} > f_c$ or $f_{lo} < f_c$?

5.1.3.1 Choice of LO for Tunable Receivers

Traditionally, most tunable receivers chose a $f_{lo} > f_c$ for typical super-heterodyne architectures. Consider traditional AM broadcasting, for example. The IF frequency is fixed at 455KHz, and the signals range from 550KHz to 1.600MHz. The upconverting f_{lo} would be required to tune to 1.005MHz to 2.055MHz, whereas the down-converting LO would be required to tune to 95KHz to 1.145MHz. The frequency *ratio* of which the former needs to tune to is much smaller. Practically designing such an oscillator is much easier.

5.1.3.2 Choice of LO in This System

This system, however, is not bound by such a constraint since it is a fixed frequency system (i.e. it does not need to tune to different carrier frequencies). FIGURE 20 however, clearly indicates that operating at a higher LO frequency reduces the image problem significantly, as the image band is much "cleaner" for the high side LO. The measurement which FIGURE 20 is based on was performed on the roof of Cory Hall, the EECS department at U.C. Berkeley. Therefore, the same measurement at a different geographical location would yield a different result. Due to FCC partitioning of the different bands, within the U.S., however, measurements would look similar. Of course in the future the FCC regulations may change and the 1028 MHz band may become completely occupied, but for the time being, because of the lack of any opposing reason, the high side LO was chosen.

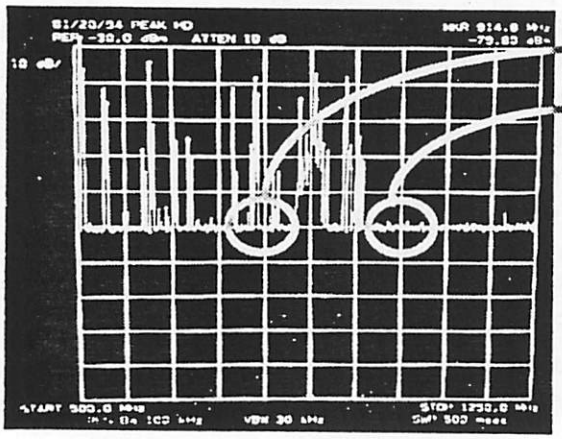


FIGURE 20. The "cleanliness" of the spectrum at the possible image frequencies for the receiver system. The 1028MHz image band appears to be much "cleaner." This spectrum was measured at the roof of Cory Hall, the Dept. of EECS, at UCB.

5.1.4 Up-Converting IF vs. Down-Converting IF

Relatively narrow-band systems generally use an IF frequency which is lower than the incoming RF frequency primarily because designing active high gain stages as well as elements such as variable gain amplifiers is much easier to accomplish at the lower frequencies. At times, particularly for very wideband tunable applications, it is beneficial to take advantage of an upconverting first IF stage. The reasons for such a choice are explained below.

The superheterodyne architecture was invented primarily to overcome the necessity of designing high-selectivity-tunable filters and gain stages. If a down-converting IF stage is used in a broadband system, a tunable image reject (pre-select) filter would be required to attenuate the image. The need for such a filter significantly reduces the effectiveness and simplicity of a superheterodyne architecture. For example, consider a CAble TV (CATV) tuner. It is required to tune from 54MHz to about 1GHz[1]. If an IF frequency of say 30MHz were to be used and assuming $f_{lo} > f_c$, the image would fall anywhere between 104MHz to 1060MHz. Obviously a fixed frequency image-reject filter could not be used as this would eliminate some of the channels. If an up-convert first IF stage is used however, a wideband fixed-frequency LPF or a narrowband fixed-frequency bandpass filter can act as the image-reject filter. For example if 1.1GHz were to be used as the first IF frequency, the image frequency would fall in the range from 2.254GHz to about 3.2GHz. Clearly this can be filtered out using a LPF $f_{-3dB} \cong 1.2\text{GHz}$ or BPF $(f_c \approx 1.1\text{GHz}, f_{BW} \geq 6\text{MHz})$.

Furthermore, by using up-conversion the oscillator tuning range is significantly reduced; for the above example, from approximately a decade (10:1) to an octave (2:1). Design of the latter oscillator is much simpler.

When the first IF frequency is high enough that providing sufficient gain is difficult at that frequency, a second low frequency IF can be used to provide a significant amount of gain and functions such as AGC. In the above example, 30MHz can be used as the *second* IF frequency.

5.1.5 LO Power

There is typically a trade-off in the selection of the LO power between the mixer NF and its IP_3 for both single balanced (2-quadrant analog-multiplier based) and double balanced (Gilbert Cell based) active mixers. For the NE600, which uses a single balanced mixer, this is shown in FIGURE 21.a. Initially, as the LO power increases, both the distortion performance and the noise performance of the mixer improve. This is to be expected, since higher LO drives cause transistors Q3, Q4, Q5 and Q6 in FIGURE 21.b in the Gilbert Cell (and Q2 and Q3 for the single balanced mixer of FIGURE 21.c) to switch faster, more closely resembling ideal switches with no non-linearity contribution. On the other

1. Present cable systems can not support the higher end of the band, but the reasoning here remains valid.

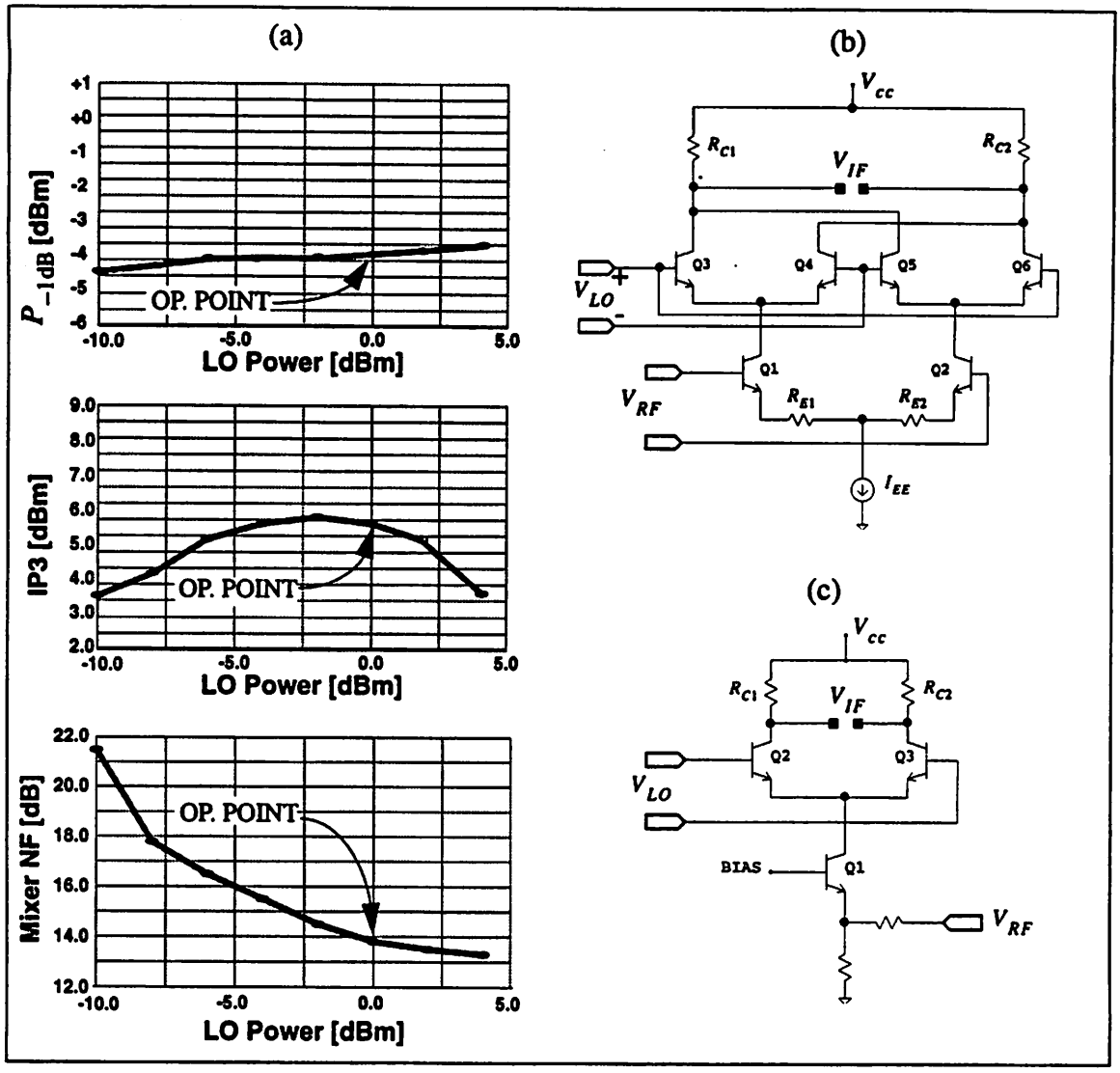


FIGURE 21. (a) Trade-off between mixer noise figure and mixer IP_3 (b) Shematic for a double balanced mixer (c) Schematic for a single balanced mixer similar to the one used in the NE600.

hand, low values of LO drive, cause all switching transistors to be conducting simultaneously for a relatively long period of time, resulting in higher distortion levels. The physical origins of the decrease in IP_3 for larger LO drives are not known [14] but this effect is observed in both single balanced and double balanced mixers. It is interesting that in this region, the -1 dB compression point of the mixer keeps on increasing. Therefore as seen in FIGURE 21.a equation [27] which relates P_{-1dB} to O_{IP3} no longer holds.

It is apparent from FIGURE 21.a that too low of a LO drive level will increase the mixer NF. This can be attributed to the fact that in general the faster transistors Q3, Q4, Q5 and Q6 in FIGURE 21.b in the Gilbert Cell (and Q2 and Q3 for the single balanced mixer of FIGURE 21.c) switch the less the time spent in the transition region and hence the less their contribution to the mixer noise. This is because in the transition region when the LO is switching from one state to another, all of the switching transistors are on, reducing the amount of degeneration that these devices see which increases their noise contributions.

For example for the Gilbert Cell mixer, when transistors Q3, Q4, Q5, and Q6 are equally on (V_{LO} = 0 V), Q3 is only degenerated by $1 / g_{m4}$, Q4 is only degenerated by $1 / g_{m3}$, etc. and therefore Q3 contributes

$$\overline{v_{eq}^2} = \overline{v_3^2}\left(\frac{\frac{g_{m4}}{2}}{\frac{g_{m1}}{1+g_{m1}R_{E1}}}\right)^2 \qquad \text{(EQ 34)}$$

to the input referred equivalent noise (note that $g_{m4} = g_{m1} / 2$ in this case). The same argument can be made for Q4, Q5, and Q6. Note that any attempt to reduce R_{E1} in order to improve the noise performance of the mixer will result in a reduction of the mixer IP_3.

On the other hand, in the fully switched states, for example when $V_{LO} > 3V_T$ ($V_T = kT / q$), Q4 is conducting almost no current and therefore Q3 is degenerated by approximately r_{o1}, and therefore its noise contribution to the equivalent input noise is significantly reduced to

$$\overline{v_{eq}^2} = \overline{v_3^2}\left(\frac{\frac{g_{m4}}{1+g_{m4}r_{o1}}}{\frac{g_{m1}}{1+g_{m1}R_{E1}}}\right)^2 \qquad \text{(EQ 35)}$$

a similar argument can be made for Q6. Furthermore, in this state Q4 and Q5 contribute no noise to the equivalent input referred noise of the mixer. In summary, to minimize the contribution of these devices to the noise of the mixer, the time spent in the transition region should be minimized.

By using FIGURE 21.a it is observed that an LO power of approximately 0 dBm is a happy medium between mixer IP_3 performance and its noise figure. In this system the LO power is set to 0 dBm.

5.1.6 Amplitude and Phase Tracking in Image Reject Mixers

An image reject mixer is often preferable to a simple mixer. In this system, for example, the use of a front-end image reject mixer would have eliminated the need for the inter-stage ceramic filter (BPF2 in FIGURE 10) with its associated cost, area and insertion loss[1]. The block diagram of a typical image reject mixer is shown in FIGURE 22.

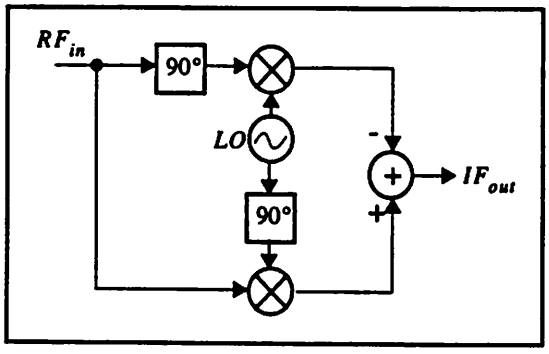


FIGURE 22. The block diagram of an image reject mixer.

Theoretically, an image reject mixer offers the complete suppression of the image band while generating the desired band. However, it is practically difficult to achieve more than 25 to 30 dB of image suppression in today's technology due to phase and amplitude mismatches from the theoretical desired values. In order to achieve an infinite suppression of the image while maintaining the maximum power in the desired sideband, the following conditions must be satisfied in the block diagram of FIGURE 22

$$i_1 = q_1, i_2 = q_2, \angle p_1 = \angle p_2 = 90° \quad \text{(EQ 36)}$$

where i_1 and q_1 are the amplitude of the in-phase and "quadrature" components of the input signal, i_2 and q_2 are the amplitude of the in-phase and "quadrature" phase of the local oscillator signal and $\angle p_1$ and $\angle p_2$ are the angles of the "quadrature" components of the input and LO signals respectively relative to their in-phase components.

With the simplifying assumption that $i_1 = q_1$ and $\angle p_1 = 90°$ in FIGURE 22 (i.e. the mismatches in one of the two sources only is considered) the amount of the rejection of the image frequency in dB is given by (See section B, "Image Suppression Degradation Due to Amplitude Mismatches and Quadrature Phase Inaccuracies").

$$R_{\text{image}_{e_{G,p}}} = 10 \log\left(\frac{1 + G^2 + 2G\sin p}{1 + G^2 - 2G\sin p}\right) \quad \text{(EQ 37)}$$

where $G = q_2 / i_2$ indicates the mismatch in the (voltage) amplitude tracking of the LO quadrature generation and $\angle p = \angle p_2$ is the angle of the quadrature signal of the LO. Clearly the image rejection is infinite only when $G = 1$ and $\angle p = 90°$. FIGURE 23 displays the reduction of the image suppression due to mismatches in the gain G, and offsets from $\angle p = 90°$.

1. The noise generated by an image reject mixer is typically higher than a non-image reject mixer for the same power consumption due to its higher count of components. This added noise is traded off for the reduction in the system noise due to the elimination of the BPF.

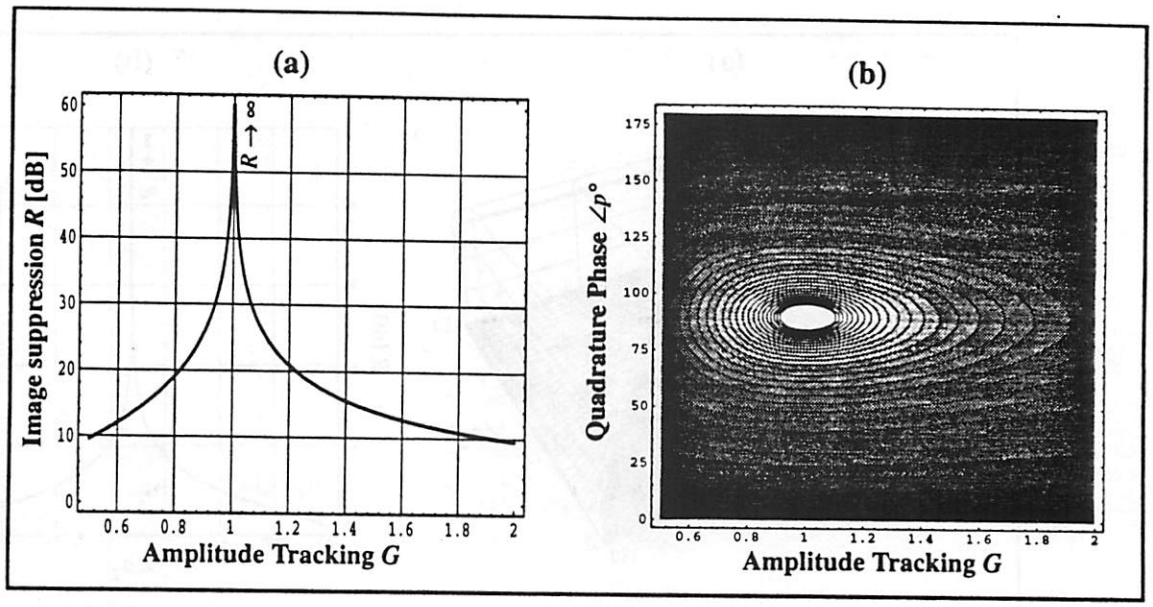


FIGURE 23. (a) Image suppression as a function of amplitude tracking of the LO assuming perfect quadrature phase (b) Contour plot of image suppression as a function of amplitude tracking and quadrature phase of the LO. Both plots assume perfect amplitude tracking and quadrature angle on the incoming signal. Based on reciprocity, the same plots apply for a perfect LO and mismatched incoming signal gain and phase.

The image suppression of the mixer can also be studied assuming perfect amplitude tracking in both the incoming signal and the LO generation and considering the phase offsets of both of the quadrature generation circuitry simultaneously. With these assumptions, the image rejection can be calculated from (See section B, "Image Suppression Degradation Due to Amplitude Mismatches and Quadrature Phase Inaccuracies").

$$R_{image_{p1,p2}} = 10 \log\left(\frac{1+\cos(p_1-p_2)}{1+\cos(p_1+p_2)}\right) \quad \text{(EQ 38)}$$

where p_1 and p_2 are as mentioned previously. FIGURE 24 displays the effect of quadrature offsets on the image suppression of the image reject mixer.

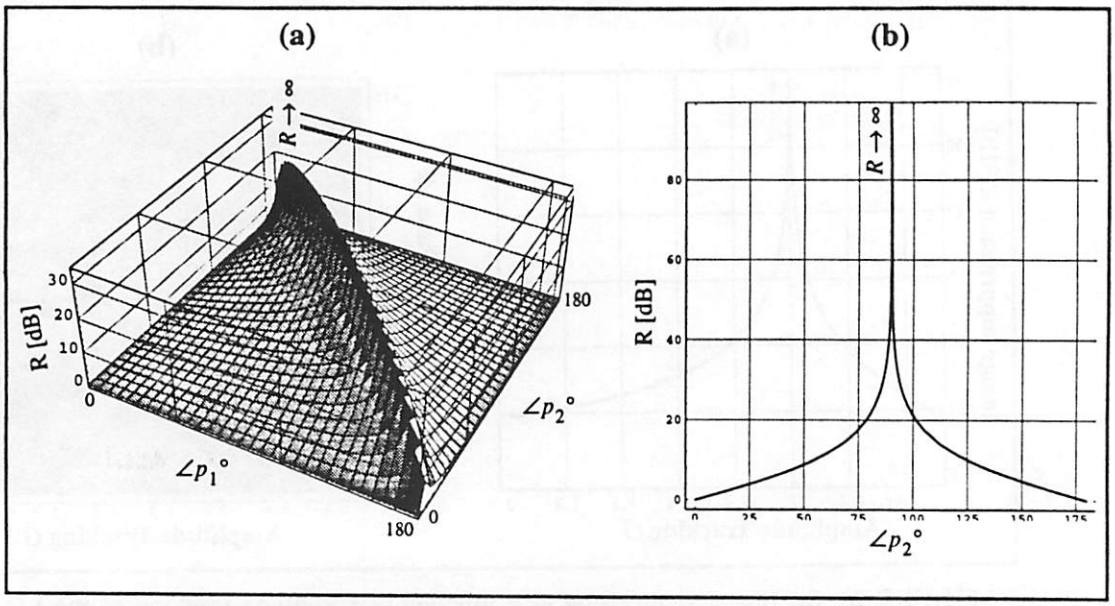


FIGURE 24. (a) Image suppression as a function of quadrature phase offsets of the LO and the incoming signal, assuming perfect amplitude tracking. (b) Image suppression as a function of mismatch in the quadrature phase of the LO signal alone ($\angle p_1 = 0$).

From equation [53] and FIGURE 24 it is clear that the image suppression is infinite as long as $\angle p_1 + \angle p_2 = 180°$ while $\angle p_1$ and $\angle p_2$ are non-zero. In other words it is possible to obtain perfect image rejection for example by using $\angle p_1 = 145°$ and $\angle p_2 = 45°$. On the other hand the maximum amplitude of the desired signal is obtained for $\angle p_1 = \angle p_2 = 90°$ and other angle combinations are rarely used in practice.

It is interesting to note that equation [37] and equation [38] are independent of the LO and incoming signal frequencies. Maintaining quadrature phase accuracy (and to a lesser extent gain balance), however, at the higher frequencies is more difficult (1° at 1GHz is only 17ps). Image suppression is therefore much easier to accomplish at lower frequencies.

As an example, the quadrature demodulator used in this system, displays a typical phase offset of 4° and amplitude accuracy of 1.03 (at 70MHz). Assuming this demodulator were used for the LO quadrature generation in an image reject mixer application with an *ideal* quadrature generated incoming signal, the image signal would be suppressed by 28.4 dB as predicted by equation [37]. This prediction is verified in FIGURE 25 by taking the Fourier Transform of the resultant signal.

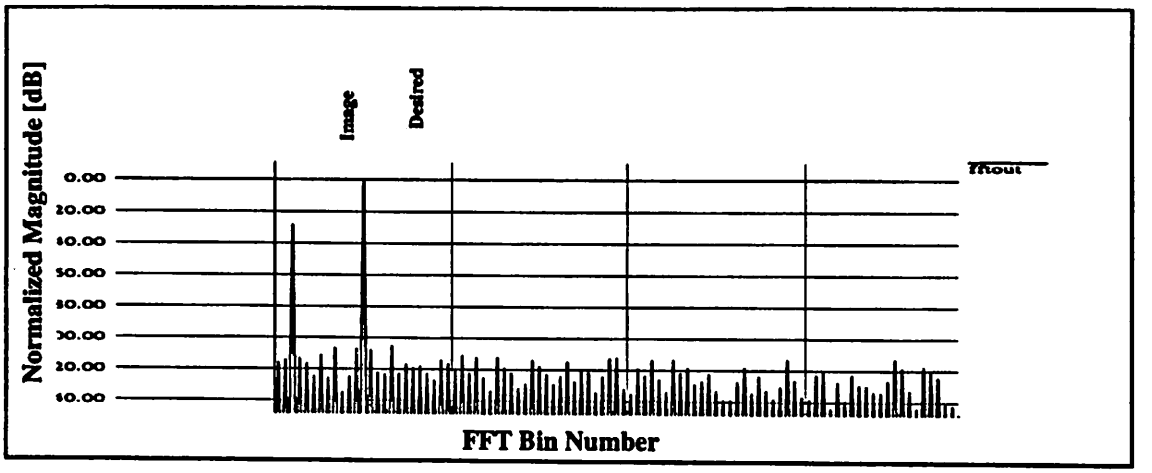


FIGURE 25. Fourier transform of the output of the image reject mixer of FIGURE 22 for a perfect incoming signal quadrature generation but gain mismatch of 1.03 and phase offset of 4° in the LO quadrature generation.

On a practical note, mismatches in phase quadrature and amplitude tracking result from systematic and/or random mismatches in the design and fabrication of the quadrature circuitry. In order to obtain maximum image suppression, therefore, it is very important to follow proper layout methodology such as common-centroid geometry schemes and the use of large components. Furthermore, frequently dummy elements are utilized in the layout to obtain a symmetrical layout in order to minimize systematic offsets. Offset trimming techniques can also be utilized to maximize image suppression. Finally, often external pins are provided on IC packages for the user to maximize image suppression by biasing the pin to the proper voltage.

The above discussion on image suppression of a mixer also applies directly to the issue of sideband suppression in the modulator output of a single sideband modulated signal.

5.2 The IF Variable Gain Amplifier

This IC includes two sections with taps provided for external inter-stage filtering. The gain of this IC is digitally controllable with a resolution of 1dB, a maximum voltage gain of 87dB, and a minimum voltage gain of 16dB. In this system, the gain can be set using dip-switches for testing purposes, or with external control circuitry during normal operations.

This IC is specified for "normal" operations with an IF frequency of up to 70MHz. It was experimentally verified that the slight loss of gain in this IC at the high side of the CDMA signal (70Mhz to 86MHz) was acceptable for operations in this system.

Issues regarding the noise and linearity of this stage are discussed in See section 4.0, "Receiver Dynamic Range".

5.3 The Demodulator Used in This System and its Limitations

The commercial demodulator used in this system was designed for narrow bandwidth systems (such as the cellular phone), and therefore did not have the proper output bandwidth. This demodulator was the only DC coupled monolithic I/Q demodulator commercially available at the time. In order to provide maximum flexibility in the system it was of interest to provide the DC coupling option so that true baseband signals could be used. Furthermore, other monolithic AC coupled I/Q demodulators did not offer a 16MHz BW either, although they did provide a significantly higher BW than the DC coupled one. The use of passive demodulators was also not attractive primarily because of their large physical size.

The (dc-coupled) demodulator used in this system presented a 5KΩ output impedance. Clearly this part was not intended for wideband applications, considering that a 2pF parasitic capacitance at the output node would generate a pole at about 16MHz, which is in the bandwidth of interest. Since the manufacturer of the part was unwilling to provide any insight into the output driver used, the output driver schematic of the chip was determined to be as shown in FIGURE 27.a (this was done by various trial and error reverse engineering measurements, consideration of what the logical output stage would be and the likely internal configuration of the chip).

This configuration would make sense. The mixer cell is most likely a gilbert cell configuration which is extremely broadband. The front end of the mixer is specified to be able to accept signals as high as 100MHz. Therefore, it is reasonable to assume the bandwidth limitation is due to the output stage driver. Once again, as this chip was intended for narrowband voiceband applications, by using a 5KΩ output impedance, the designers both tightly bandlimit the noise of the mixer at the output as well as avoided the design of a large output stage which would be required to drive a healthy voltage swing on a small value output load (and would be very power hungry). In a "typical" application for this part the device would connect to a very high impedance load and have a baseband bandwidth of less than 100KHz.

5.3.1 Effects of Harmonics of the LO on *I* and *Q* Generation in a Simple RC Quadrature Generation Circuit

Many methods exist for generating quadrature signals. One method commonly used for off-chip implementations is shown in FIGURE 26.a. This method can also be used for integrated circuit applications although the capacitor sizes may become relatively large. This method of generating quadrature components, however, is sensitive to harmonic contents in the LO signal. For example, a perfect sinusoidal input generates a 90° phase offset between the *I* and *Q* outputs, but as the input signal migrates towards a square wave, the phase offset asymptotically approaches 180°. This fact is shown in FIGURE 26.b in which the horizontal axis represents the number of harmonics *(j)* considered in the Fourier series expansion of a 50% duty cycle square wave to be input as the LO signal to the quadrature circuit

$$V_{LO}(t) = \sum_{n=1}^{j} A_n \cos(n\omega_c t) = \sum_{n=1}^{j} \frac{\sin(n\pi/2)}{(n\pi/4)} \cos(n\omega_c t) \qquad \text{(EQ 39)}$$

Clearly in this method, the quadrature accuracy also depends on component matching between the resistors (R) and capacitors (C) in the quadrature circuit. Furthermore, although the quadrature phase accuracy is maintained over a wide bandwidth of sinusoidal LO signals, the relative amplitude of the I and Q signals varies significantly for different input LO frequencies.

The operation of the circuit of FIGURE 26 can be intuitively understood by realizing that the I output is the output of a first order LPF with an LO signal applied exactly at its 3 dB cutoff frequency with a -45° phase offset and the Q output is the output of a HPF with the LO signal applied at its 3 dB high-pass cutoff frequency with a +45° phase offset. The overall circuit therefore yields the desired quadrature signals.

As the LO signal approaches a square wave, more and more components of the LO are subject to larger amount of phase shift by the LPF and the HPF. Ultimately, for a perfect square wave, the poles exert a +90° and -90° phase shift on the LO signal resulting in a 180° "quadrature" circuit.

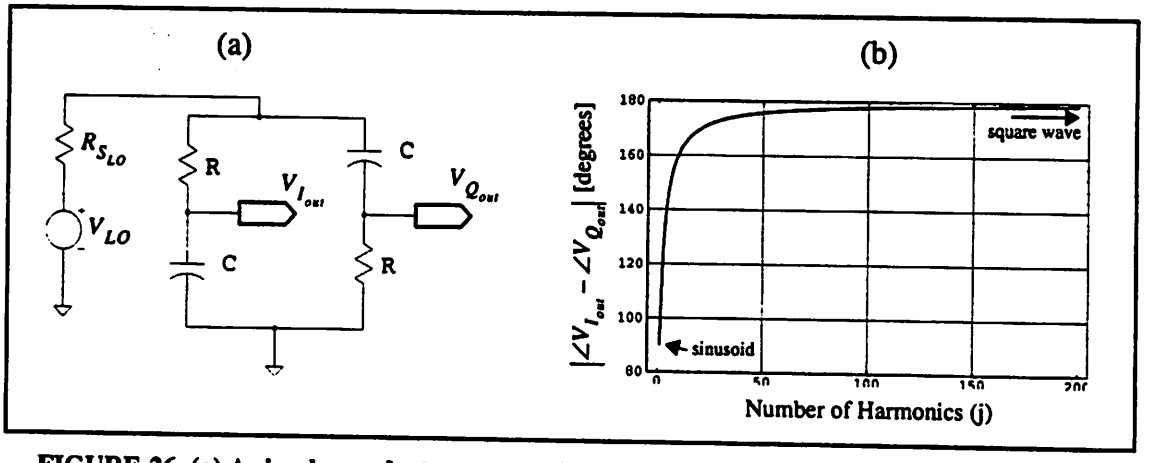


FIGURE 26. (a) A simple qaudrature generation circuit for sinusoidal input signals (b) Relative phase difference between the "in phase" and the "quadrature" component as the sinusoidal signal approaches a square wave. The horizontal axis displays the number of harmonic components of an equivalent square wave.

5.3.2 Other Methods of Generating Quadrature Signals

There are more suitable methods for on-chip implementation of the quadrature generation circuitry. One such method utilizes digital flip-flops. If an LO signal 4x the quadrature components of interest can be generated, the quadrature generation using flip-flops is almost trivial and the phase and amplitude accuracy is usually very good. Otherwise a 2x LO should be generated for this purpose and a slightly more complicated scheme is used to generate the quadrature components with a small penalty in phase and amplitude track-

ing as compared to the 4x method. Furthermore, both methods offer good amplitude tracking over a wide bandwidth of LO signals. A side-benefits of using an LO frequency other than the actual IF frequency is a reduction in the possibility of oscillation (regeneration) in the circuitry. Furthermore, in coherent demodulation schemes, the possibility of the demodulator capturing the LO signal instead of the incoming IF signal is reduced.

Typically, when the flip-flop method of LO generation is used, the LO signal is hard-limited internal to the IC in order to ensure that the system performance is relatively insensitive to the LO drive level. For example in the demodulator used in this system, the demodulator performance does not vary significantly for LO levels of 0.3V to 1.0V. It is empirically found, however, that best quadrature accuracy in the demodulator used in this system (at room temperature) is obtained for an LO level of about 500mV.

This method of quadrature generation is typically insensitive to the type of LO waveform used, except for signals with strong even harmonic content. For example one-side clipped sine wave inputs as well as non-50% duty-cycle square wave LO signals will degrade the *I* and *Q* tracking in the demodulator.

5.4 The ADC Buffering and Filtering Stage

5.4.1 Bandwidth Enhancement of the Demodulator IC

Since it was concluded that the bandwidth limitation was directly due to the output stage driver, two options were available. First, to load down the output of the demodulator *I* and *Q* signals with a shunt resistor (pull-up or pull-down) at the output and sacrifice the gain (and output swing) for a higher bandwidth and makeup for the gain further down the chain. The value of the resistor would be determined by the minimum voltage required to keep the transistors out of saturation in addition to bandwidth enhancement criteria.

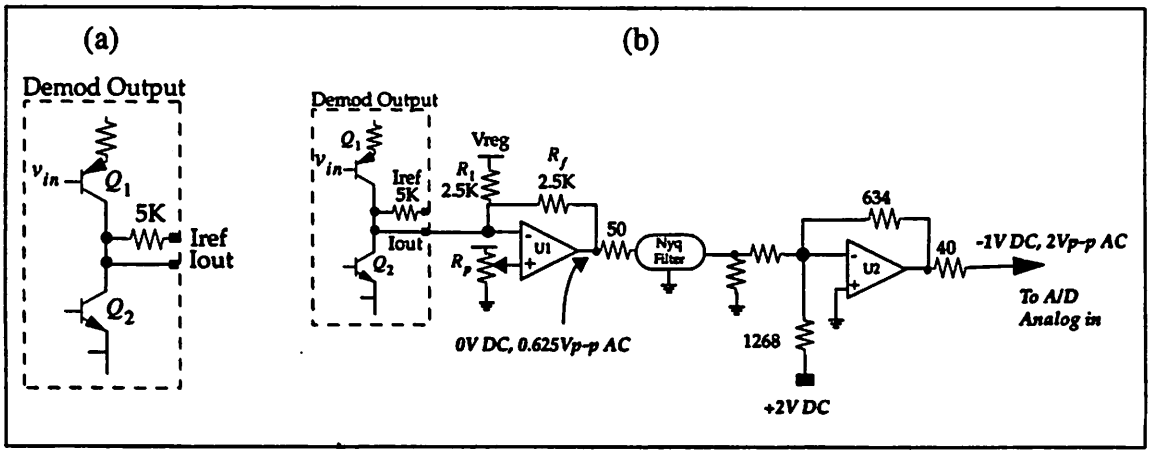


FIGURE 27. (a) The "extrapolated" output stage of the demodulator IC used in this system. (b) The simplified schematic of the output stage of the system as configured for a specific ADC interface.

The second option was to use a high speed opamp in the shunt feedback configuration to provide a very low impedance to the output *I* and *Q* signals and enhance their bandwidth considerably (U_1 in FIGURE 27.b). At the same time, the DC operating point can be set by using the same opamp. This method would avoid the trade-off between the gain and bandwidth as presented by the first method. Furthermore, this method would allow presenting a 50Ω impedance to the anti-aliasing filter that would follow. In addition, one would be able to level shift the output signal to 0V DC in order to simplify the subsequent stage buffer and the interface to the A/D converter[1]. Clearly, this method was chosen over the first alternative.

5.4.2 Output Signal

If this board were to be used as a separate test vehicle for various applications, the output of U_1 would have come out of the box as an output signal. This would have required the user to select the appropriate antialiasing filter followed by the proper gain and level-shifting opamp and implement it with the A/D and digital circuitry on a separate PCB. To simplify the task of the users, however, these elements were also integrated on the same board, with the understanding that this setup could not be as versatile as the first. Therefore output ports were provided at the output of U_1 and its quadrature counterpart for users with special requirements not met by the final buffering stage of this board.

5.4.3 The Antialiasing Filter

An antialiasing filter follows U_1. The bandwidth and skirt-steepness of this filter depends on the highest frequency of interest and the sampling rate. If the signal is oversampled, the specifications on the skirt-steepness of this filter can be relaxed. Even if the signal is oversampled significantly, the bandwidth of this filter should be kept as low as possible and its steepness as sharp as possible in order to minimize the amount of noise let into the A/D converter. A hybrid LC LPF with a bandwidth of 20MHz was chosen here and utilized on the PCB with special sockets in order to allow the use of other filters for applications where the entire bandwidth of the system is not required.

Ideally the anti-aliasing (Nyquist) filter should be placed immediately before the A/D converter. In reality, however, many A/D converters present highly capacitive and to some extent undetermined input impedances which would significantly change the pole/zero locations and hence the performance of the anti-aliasing filter. It is therefore essential to buffer the filter from the input of the A/D by another high speed opamp. In this system, this opamp, U_2, serves to set the proper swing as well as the proper DC value for the A/D converter as well as buffering the filter from the A/D. Furthermore it presents the output of the antialiasing filter with a 50Ω impedance. U_2's output noise is only bandlimited by the natural RC time constant at this node and will therefore degrade the performance of

1. This is essential because of the flexibility requirement. This feature will facilitate interfacing to various A/D's with different reference signal levels, as well as various top of the ladder and bottom of the ladder levels.

the system slightly (the effect here is more than just the integrated noise power, because one needs to account for the effect of the sampling of the noise also (the higher frequency noise aliasing back into the bandwidth of interest due to sampling).

5.4.4 Effect of Buffer Opamps on System Performance

It is clear that the choice of the proper opamps is critical to the performance of the system. As far as DC performance of these opamps is concerned, small offsets usually can be tolerated (although this will also depend on the specifics of the system, the number of bits of resolution of the A/D, etc.). Large offsets, however, must be avoided as they could result in the clipping of the A/D converter. The overall offset drift is determined by the output drift of the driving opamps plus the offset drift of the ADC.

As far as AC performance is concerned, the driving amplifiers should have a better performance than the ADC. In other words the driving amplifiers should not be the weak link in the baseband system. In order to achieve an effective number of bits (ENOB) of 8, assuming no oversampling[1] a 49.9dB SFDR at the entire analog frequency band of interest would be required (this is most difficult to satisfy at the higher frequencies).

Some other considerations that were taken into account for choosing the best possible commercially available opamps for this system included:

- Power consumption, because of the portable nature of the application.
- Power supply rejection ratio. PSRR was an issue primarily because DC to DC converters were to be used to supply the $-V_{cc}$ of the opamp. Since DC to DC converters are noisy, good PSRR, especially to the negative voltage supply was essential. Note that many times the operation frequency of the DC to DC is relatively low, and effective bypassing requires large value capacitors and is therefore difficult and costly to implement. Assuming an 8-bit ADC with an input signal swing of 2Vp-p result in a 0.5LSB=4mVp-p. The effect of any ripple on the driving opamps, therefore, has to be significantly less than 4mV. The peak-to-peak ripple voltage generated by the charge-pump converter used in this system can be approximated by

$$V_r = \left(\frac{1}{2f_{pump}C_2} + ESR_{C2}\right)I_{out} \qquad \text{(EQ 40)}$$

1. Oversampling the input signal does help reduce the quantization noise for a given analog anti-aliasing filter. This is because with oversampling the RMS quantization noise ($q / \sqrt{12}$) is spread across a larger bandwidth, a large portion of which can be filtered. With oversampling the SNR (due to quantization noise only) is given by $SNR = 6.02N + 1.76\text{dB} + 10\log\left(\frac{f_s}{2f_a}\right)$ where N is the effective number of bits, f_s is the sampling rate, and f_a is the analog filter cutoff frequency.

where I_{out} is the output current of the converter, C_2 is the external capacitor at the output node of the charge-pump (DC-DC) converter, ESR_{C2} is the effective series resistance of that capacitor, and f_{pump} is the operating frequency of the charge pump (which is equal to half the oscillator frequency). In this system, $I_{out} < 20$ mA, $C_2 = 150\ \mu F$, $ESR_{C2} < 0.4\Omega$, and f_{pump} is selectable at 5KHz or 21.5KHz. In the worst case, this results in a fundamental peak-peak voltage ripple of 21.3 mV ($f_{pump} = 5$Khz). The current-feedback opamps used in this system (which have a much worse PSRR performance than their voltage-feedback counterparts) have a PSRR of approximately 45dB at low frequencies. This translates to a ripple of 120μ Vp-p on the desired signal which is clearly negligible.

The charge-pump does generate harmonics at higher frequencies also. However, the PSRR of the opamps are maintained to a reasonably high degree at these frequencies and the harmonics do not cause any problems. For the current-feedback opamps, the PSRR is about 40dB at 10MHz.

Finally, the peak-peak ripple of the opamp can be reduced by increasing the charge-pump operating frequency at the expense of added power consumption and higher frequency harmonics. This option is provided on this board by the use of jumpers.

• Common mode input range. Since the opamps were to operate with a ±5V supply, and since the demodulator required a DC operating point such that Q_1 and Q_2 in FIGURE 27 would not saturate for the largest possible output swings, the CMIR of the opamp was very important. 5V supply based current feedback opamps were ruled out for this stage primarily because of their poor CMIR performance.

• Maximum output current. For example, in the configuration shown in FIGURE 27, opamp U_1 is required to drive a 100Ω load at the proper voltage swing i.e. about 6 mA of current.

• High loop gain at the highest frequency of interest. All the benefits of feedback begin to vanish at the higher frequencies as the loop gain starts to decrease in magnitude. These benefits for a shunt-shunt feedback stage, as constructed with U_1 and U_2 include low distortion, low input impedance as observed by the demodulator, and low output impedance as required by the filter. A high loop gain is therefore necessary at the highest frequency of interest. This can be obtained by using an opamp with a high open-loop DC voltage gain and/or wide open-loop bandwidth (for voltage feedback opamps), and with a high open-loop DC transimpedance gain and/or wide open-loop bandwidth for current feedback opamps.

5.4.5 Voltage vs. Current Feedback Opamps

Two different family of opamps were investigated for the buffering stages in this system. These are the current feedback (transimpedance) family of opamps and the voltage feedback (traditional) opamps.

5.4.5.1 Theory of Operation

FIGURE 29.a display a high level model for a traditional voltage feedback amplifier. In an ideal voltage feedback opamp, $R_{in} \rightarrow \infty$ and $a \rightarrow \infty$ where a is the voltage gain of the open loop amplifier (the gain of the *voltage dependent voltage source* in FIGURE 29.a).

FIGURE 29.b displays a high level model for a current feedback opamp. In an ideal current feedback opamp, $R_{in} \rightarrow 0$, $e(j\omega) \rightarrow 1$, $i_{err} = 0$, and $Z(j\omega) \rightarrow \infty$ (not all these relations are independent). In this case, $e(j\omega)$ is ideally a unity gain voltage buffer and $i_{err}Z(j\omega)$ is the gain of a *current dependent voltage source* (a *transimpedance* stage). V_d is kept small in a voltage feedback amplifier by the use of negative feedback, whereas in a current feedback amplifier V_d is made small by requiring $e(j\omega) \rightarrow 1$ and $R_{in} \rightarrow 0$. In a sense, in a current feedback amplifier, the inverting input of the opamp is truly an output port.

At a high level, the operation of the current feedback amplifier in a non-inverting mode can be explained as follows (the inverting operation is much easier to understand using the actual transistor-level schematic and will not be discussed here; at the transistor level the inverting circuit operation can be explained by analogy to the explanation given here). Assuming the opamp had been in steady state operation, when a step input is presented at the non-inverting input, the step voltage is very quickly transferred to the inverting input through the unity gain buffer. Since the signal has not yet propagated to the output, a transient current is generated across the feedback resistor. This generates a voltage at the gain node and subsequently at the output node of the opamp approximately equal to $i_{err}Z(j\omega)$. The transient current i_{err} will then flow until equilibrium is reached and $V_d = 0$ again.

5.4.5.2 Circuit Operation

Circuit-wise, the high speed and very high slew rate performance of current feedback amplifiers is provided through the use of *current* stages (current can be handled much quicker than voltage since generally capacitive parasitics dominate over inductive parasitics and bipolar transistors are much faster current handlers than they are voltage handlers, e.g. ECL logic). To interface to the outside world however, the opamp needs to present the final signal in the form of an amplified *voltage*. In order to achieve these objectives, a class AB input stage is utilized (FIGURE 28). This input stage is followed by current mirrors (Wilson or simple) and the outputs of the current mirrors are converted into a voltage at the high impedance gain node of the opamp. This voltage is then buffered by using a class AB output stage. In order to avoid the gain node from significantly reducing the bandwidth of the opamp, the parasitic capacitance at this node must be minimized. This is achieved by minimizing the Miller effect at that node and by buffering the gain node through an emitter follower stage.

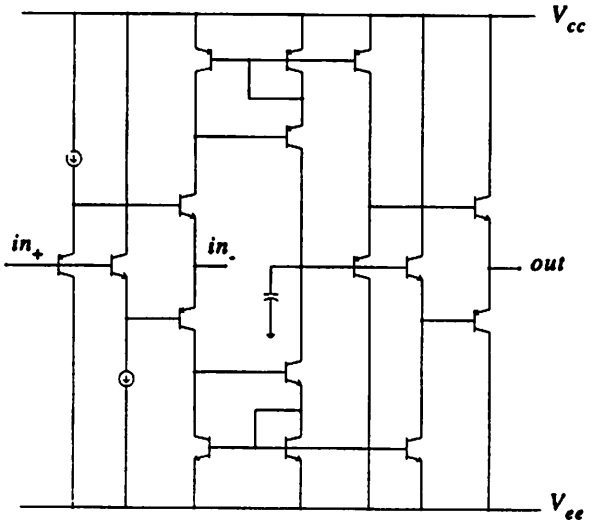


FIGURE 28. Schematic of a typical current-feedback opamp.

5.4.5.3 Slew Rate and Settling Time Issues

The high slew rate performance of current feedback opamps (1300V/μs in the case of CLC412, used in this system) offers very low distortion for large magnitude, high frequency signals, offering a very high full-power bandwidth. In other words, the high slew rate allows the amplifier to operate in the single pole exponential region during the transient and avoid the nonlinearities introduced due to the slow linear slewing. In theory current feedback opamps are slew limited by the amount of capacitance present at their gain node. Slew rate limitation can however occur at the class AB input stage under certain conditions. Because of the use of class AB stages, the quiescent current can be small without significantly limiting the slew performance of the opamp, although in reality non-idealities can cause the current consumption of the high speed current feedback opamps to be more than that of their voltage feedback counterparts.

Current feedback opamps do offer extremely fast settling times to about 0.1% of the final value, and this fact makes them suitable for use in application with requirements of up to about 10 bits of resolution. "Thermal tails," caused by the unequal current flow in the different branches of the class AB stages as well as the current mirrors cause very slow settling for applications requiring more than 10 bits of resolution. Thermal errors in the current mirror can be reduced by using a Wilson current source (in a simple current source, one side dissipates more power than the other, due to unequal V_{ce}'s). Thermal tails are usually of no consequence in applications where the low frequency behavior (below about 100KHz) is not of interest since these tails vary very slowly.

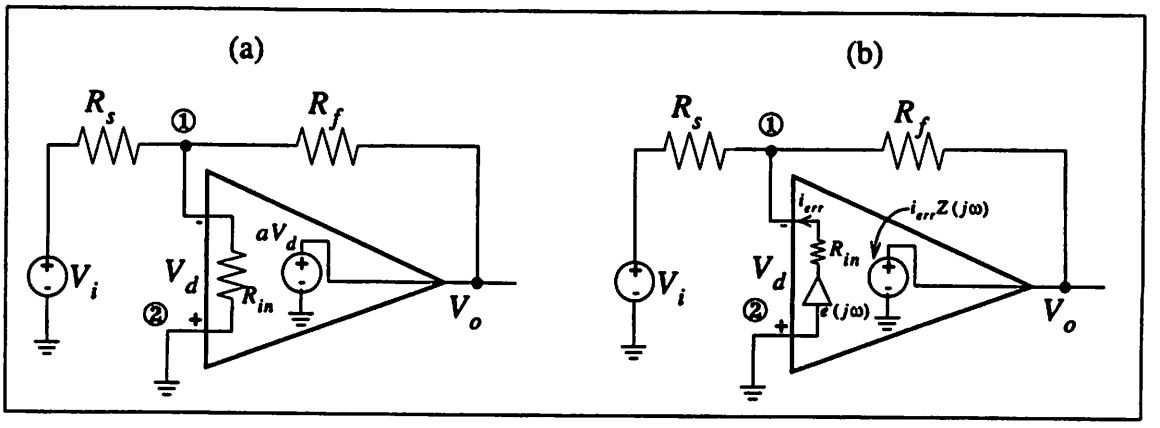


FIGURE 29. High level models for voltage feedback (a) and current feedback (b) amplifiers in a shunt-shunt feedback (inverting) configuration.

5.4.5.4 Constant Bandwidth vs. Gain Setting

The main advantage of current feedback opamps as compared to their voltage feedback counterparts is their relatively constant bandwidth for different values of closed loop gain. A high level discussion of this property of the current feedback opamps is presented here.

By summing the currents at the inverting node of a voltage feedback opamp (node ① in FIGURE 29.a), and using the fact that $V_o = a(j\omega)V_d$ it is easy to calculate the closed-loop bandwidth of the voltage feedback amplifier, $A(j\omega)$

$$A(j\omega) = \frac{V_o}{V_i}(j\omega) = \frac{-R_f/R_s}{1+\frac{1+R_f/R_s}{a(j\omega)}} \qquad \text{(EQ 41)}$$

where $-R_f/R_s$ is the DC closed loop gain of the amplifier, A_0, and $\frac{1+R_f/R_s}{a(j\omega)}$ is the inverse of the loop gain of the opamp (as it can be verified by breaking the loop in FIGURE 29.a and examining the loop). $a(j\omega)$, the open loop gain of the amplifier, can be typically approximated as a single pole response with a 3dB frequency, ω_{3dB},

$$a(i\omega) = \frac{a_0}{1-j\frac{\omega}{\omega_{3dB}}} \qquad \text{(EQ 42)}$$

The bandwidth of the closed loop amplifier is increased from the open loop bandwidth by a factor equal to the loop gain. This increase, however, is reduced as the closed-loop gain $-R_f/R_s$ is increased, and hence the well-known gain bandwidth product "limitation" of conventional opamps[1].

The equation for the closed loop gain of a current feedback amplifier can be developed by writing KCL at the inverting node (①) of the amplifier shown in FIGURE 29.b and using the fact that $V_- = -i_{err}R_{in}$ at this node and that $V_o = i_{err}Z(j\omega)$ at the output node. The closed loop gain, A, is therefore given by

$$A(j\omega) = \frac{-R_f/R_s}{1+\frac{1}{T(j\omega)}} \qquad \text{(EQ 43)}$$

where $-R_f/R_s$ is the dc closed loop signal gain of the amplifier similar to a voltage feedback amplifier, and $T(j\omega)$ is the loop gain of the current feedback amplifier given by

$$T(j\omega) = \frac{Z(j\omega)}{R_f + R_{in}(1+R_f/R_s)} \qquad \text{(EQ 44)}$$

Assuming a single pole roll-off for $Z(j\omega)$, similar to that given by equation [42], with a 3dB bandwidth of ω_{3dB}, the closed loop response can be calculated explicitly.

Unlike a voltage feedback amplifier, In the ideal case where $R_{in} \rightarrow 0$ the bandwidth of the current feedback amplifier is *only* dependent on the feedback resistor. Therefore, to the first order, the dependence between the closed loop gain and the closed loop bandwidth of the amplifier has been eliminated.[1] In practice, the value of R_{in} is closely related to the $1/g_m$ of the inverting input transistors, and therefore reduces with increasing bias currents. It is typically few tens of ohms. For example, the effect of R_{in} along with other second order effects not accounted for in equation [44] can reduce the bandwidth of a current feedback amplifier with a closed loop gain of 10 to half of its unity gain bandwidth, which is still impressive as compared to a voltage feedback amplifier.

---

1. It is interesting to note that even at a signal gain of unity in the inverting gain configuration, the bandwidth of the amplifier is only half of the "unity-gain bandwidth." This is because in the inverting mode configuration assuming $R_f = R_s$, the effect of shunt feedback loading at the input of the opamp reduces the open loop gain of the amplifier by a factor of 2. Therefore the loop gain of the amplifier is also reduced by a factor of 2, and consequently the bandwidth of the closed loop amplifier is only half of the unity gain bandwidth. In a non-inverting unity gain buffer application, due to series feedback at the input, the open loop gain is *not* reduced due to feedback network loading. This is why the "noise gain" of an amplifier is different from the signal gain of the amplifier in an inverting mode application. Furthermore this is why the opamps typically exhibit more peaking and are more prone to oscillation in the non-inverting unity gain configuration. The bandwidth of the inverting unity gain configuration approaches that of the non-inverting unity gain configuration only if the supply approaches an ideal current source (e.g. photo-diode application), $R_s \rightarrow \infty$ or when $R_f \ll R_s$.

1. A similar relation can be developed for the voltage feedback and current feedback opamps in the non-inverting mode. The inverting mode relations has been developed here since the opamps on this board have all been utilized in this mode.

5.4.5.5 Graphical Representation

The equation for the loop gain of a current feedback amplifier can be used to obtain a graphical aid in determining the stability of the current feedback amplifier, very similar to the analysis done for a voltage feedback amplifier. This can be done by plotting the open loop magnitude and phase of $Z(j\omega)$ in $dB\Omega$ and degrees respectively. Then the phase margin is determined by the location where the denominator of the loop gain (equation [44]) in $dB\Omega$ is equal to the magnitude of $Z(j\omega)$ in $db\Omega$ (i.e. where the loop gain = 0dB) (FIGURE 30). For the current feedback opamp used in this system CLC412

$$R_f + R_{in}(1 + R_f/R_s) \approx 634 + 100(1 + 634/1268)$$
$$= 784\Omega$$
$$= 58dB\Omega$$

Using FIGURE 30, $58dB\Omega$ of open loop transimpedance gain corresponds to a phase margin of approximately 60°.

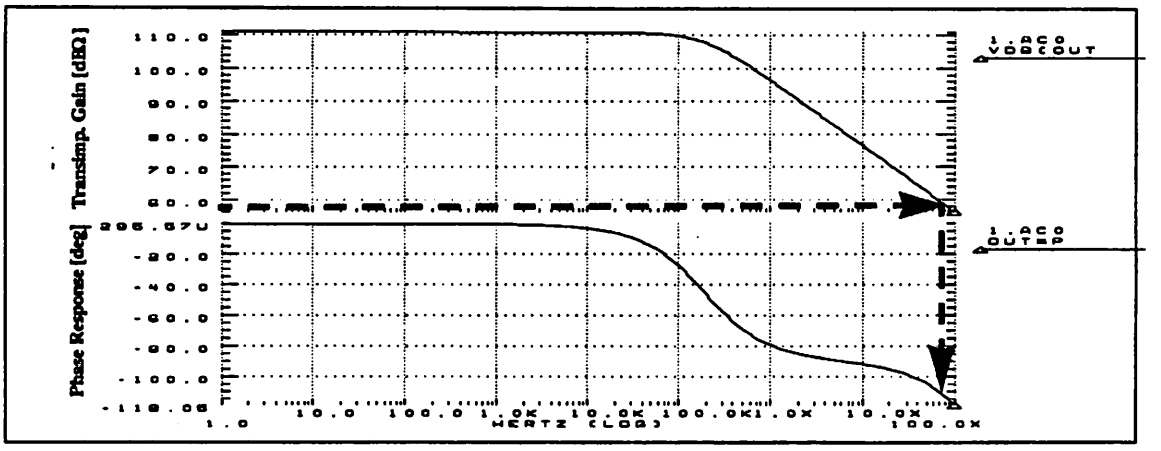


FIGURE 30. The simulated (inverting) open loop gain and phase response of the current feedback amplifier used in this system.

Using equation [44] and FIGURE 30 it is clear that to the first order, specifying R_f specifies the bandwidth of the system and its stability. Increasing R_f will make the system more stable with a smaller closed loop bandwidth whereas decreasing R_f increases the bandwidth at the expenses of peaking and potential instability. By increasing R_f, therefore, the noise bandwidth of the system could have been reduced in this system. This method was not used, however, since this would cause a premature degradation of the loop gain at the higher frequencies of interest resulting in an increase in the distortion of the

amplifier, an increase to the output impedance of the amplifier and in general a reduction in the benefits of feedback at these frequencies.

5.4.5.6 Offset Voltage of Opamps

Using FIGURE 31.a the output referred offset voltage of an opamp is given by

$$V_{O_{offset}} = \pm V_{os}\left(1+\frac{R_f}{R_{s1}}\right)\pm\left(I_{b-}+\frac{I_{os}}{2}\right)(R_f)\mp\left(I_{b+}-\frac{I_{os}}{2}\right)\left(1+\frac{R_f}{R_{s1}}\right)R_{s2} \qquad \text{(EQ 45)}$$

where V_{os} is the input referred offset voltage of the opamp, I_{b-} and I_{b+} are the inverting and non-inverting bias currents respectively, and I_{os} is the input referred offset current of the opamp. In an uncompensated-bias-current voltage feedback opamp where $I_{b-} = I_{b+}$, assuming I_{os} is negligible, the output offset voltage can be minimized by the system designer by selecting the external resistors such that the opamp input ports observe an equal value of resistance. For example in FIGURE 31.a, $R_{s1} \parallel R_f = R_{s2}$ would eliminate the systematic offset voltage at the input of the opamp due to the bias currents (this can be verified using equation [45]). This method does not reduce the input referred offset voltage of bias current compensated opamps (examples of bias-current compensated front stages is shown in [9]). Since typically in voltage feedback opamps the drift voltage is related to the offset voltage, this method effectively reduces the opamp's drift voltage also.

The asymmetry of current feedback opamps results in unequal input bias currents which often have different temperature coefficients. As a result the above method of equating the inverting and noninverting resistances in order to reduce the input referred offset voltage and drift is not useful and is not used. Because of this fact and some other second order effects, the absolute DC accuracy of current feedback opamps is normally not as good as their voltage feedback counterparts.

In ADC buffering applications using high speed opamps, usually small DC offsets are not of consequence. However, if the combined offset (and/or drift) of the opamp and the ADC is large, the gain of the system would have to be reduced in order to avoid clipping the ADC's, resulting in a reduction in the system dynamic range.

5.4.5.7 Noise Performance of Opamps

Using FIGURE 31.b The output referred voltage noise of an opamp is given by

$$V_{O_N}^2 = \mathrm{BW}_{\mathrm{noise}}\left\{I_{i-}^2R_f^2 + I_{i+}^2R_{s2}^2\left(1+\frac{R_f}{R_{s1}}\right)^2 + V_i^2\left(1+\frac{R_f}{R_{s1}}\right)^2 + 4KT\left[R_f + R_{s1}\left(\frac{R_f}{R_{s1}}\right)^2 + R_{s2}\left(1+\frac{R_f}{R_{s1}}\right)^2\right]\right\} \qquad \text{(EQ 46)}$$

where i_{i-}, i_{i+} and v_i are the input referred noise sources of the opamp. equation [46] applies to both current feedback and voltage feedback opamps, with the difference that i_{i-} and i_{i+} are approximately equal (but uncorrelated) in the case of a voltage feedback opamp but are significantly different in the case of a current feedback opamp. v_i accounts for the input referred voltage noise of *both* of the opamp inputs, assuming a high common mode rejection ratio (otherwise, two independent input referred voltage sources would have to be used in the model). BW_{noise} is the noise bandwidth of the opamp. If no external bandlimiting is utilized, and assuming a two-pole, maximally flat closed loop response, this bandwidth would be approximately $1.1\omega_{3dB,\ closed\ loop}$ [9].

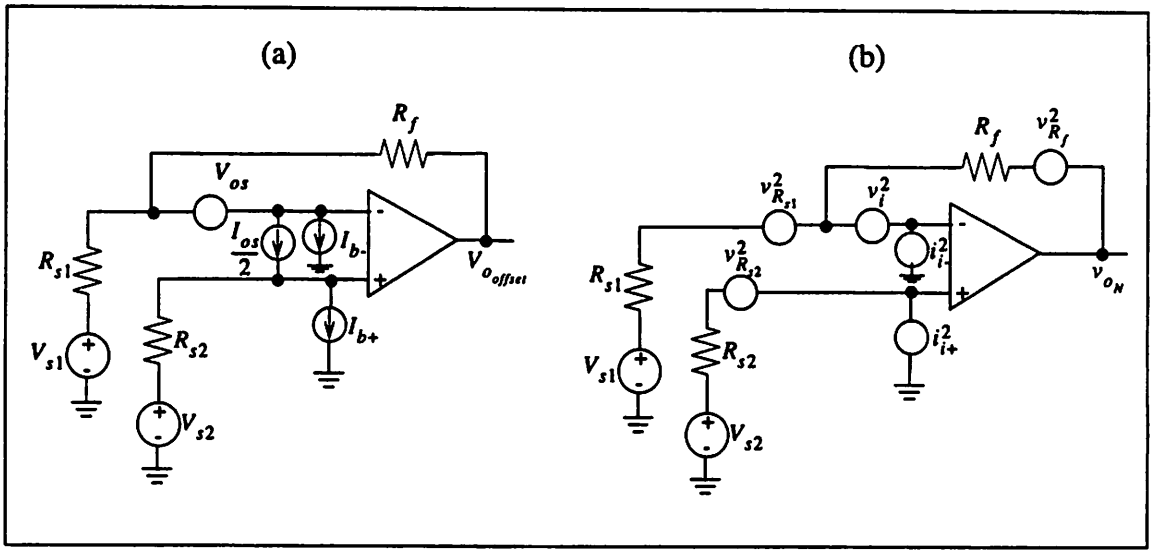


FIGURE 31. Models for output referred offset voltage of an opamp (a), and output referred noise voltage of an opamp (b). Models apply to both current feedback and voltage feedback opamps.

In voltage feedback opamps, for relatively small source resistances (most applications), typically the input referred voltage noise is the dominant source of noise. At the output, this noise is seen as multiplied by the noise gain of the opamp. In current feedback opamps, the dominant noise source is typically the inverting current noise, i_{i-}. The reason i_{i-} is significantly more in current feedback opamps than in voltage feedback opamps is that the inverting input of the opamp has no current gain relative to the current mirrors in the circuit (FIGURE 28). The noise of the current mirror is then transferred to the input with no attenuation. This does not occur in a voltage feedback amplifier because the input stage is usually a differential common emitter (or common source) amplifier with a current gain of β.

5.4.5.8 Noise Reduction in Opamps

In general, the noise performance of opamps, both current feedback and voltage feedback, can be improved by using external impedance transformers by matching the source resistance to the ratio of the input referred voltage noise to the input referred current noise of the opamp.

5.4.5.9 Opamp Summary

In summary, voltage feedback opamps have symmetrical inputs (differential amplifier), and therefore traditional bias cancelation schemes work well on them. They, in general, offer a lower power consumption and a larger CM input range than their current feedback counterparts. Voltage feedback opamps, however, suffer from the traditional constant gain bandwidth product problem; i.e. the bandwidth of the closed loop amplifier reduces as the feedback elements are changed in order to achieve a higher amount of gain such that the gain-bandwidth product remains approximately constant.

Current feedback opamps have non-symmetrical inputs, and hence traditional input bias cancellation schemes are not effective on them. In general their inverting input current noise dominates, and can be substantial. The feedback network is *fixed* for optimal performance (highest BW). Current feedback opamps present a relatively constant bandwidth for different amounts of gain.

5.4.6 Buffer Opamp Selection in this System

Many factors, including all of the factors mentioned in Section 5.4.5, "Voltage vs. Current Feedback Opamps," were considered in selecting the proper buffering opamps for the ADC's in the receiver and for the DACs in the transmitter. For example, the noise performance of several different commercial opamps which were considered for U_1 in FIGURE 27.b is shown in FIGURE 32. Note that in general the noise performance of the current feedback opamps (CLC412, CLC409, AD9617) are significantly inferior to the noise performance of the voltage feedback opamps in this configuration[1].

As expected and shown in FIGURE 32, SNR improves with increasing R_f. In the case of current feedback opamps, however, the value of R_f is fixed for best bandwidth performance and is typically less than $1.5K\Omega$. This value of R_f results in a poor noise performance for these opamps.

Although the value of the feedback resistor is not fixed for optimal bandwidth performance in the case of a voltage feedback opamp, excessively large R_f would result in the generation of relatively dominant poles (as a result of R_f and parasitic capacitances in the

1. Noise performance of these buffers are relatively unimportant when the front-end gain is high. They could limit the system noise performance, however, in cases where the front-end is in a low-gain mode.

system) which could significantly reduce the phase margin and eventually result in oscillation.

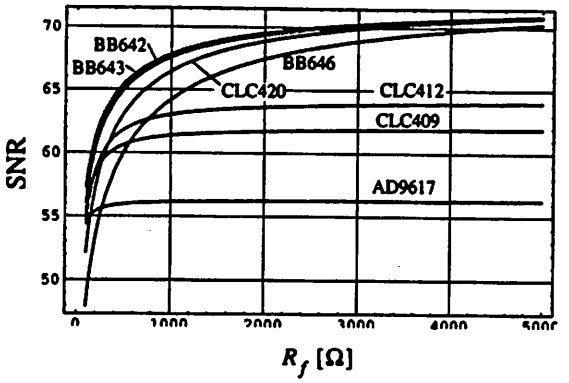


FIGURE 32. SNR vs. R_f for various commercial candidates for U_1 in FIGURE 27.b. The SNR shown here takes into account noise due to this stage only. Results are for $R_1 = 3K\Omega$, $R_p = R_1 \| R_f$, and a Nyquist bandwidth of 21.4MHz which corresponds to the bandwidth of the LPF which follows this buffer.

A voltage feedback opamp was selected for U_1 in FIGURE 27.b primarily because of its superior noise performance and its relatively large common mode input range. R_f was selected to be 2.5KΩ which results in a relatively good noise performance while maintaining a reasonable phase margin.

U_2 was chosen to be a current feedback opamp so that it can deliver a relatively large gain while maintaining a high bandwidth. The noise performance and common mode range are relatively unimportant for this stage.

5.5 The Transmitter Modulator

The input frequency range of the IQ modulator used for the transmitter of this system ranges from 0 to 100 MHz. The transmitter implemented in this system utilizes a single stage up-conversion. However, the data can be upconverted to an intermediate frequency by a digital upconverter, and then upconverted to the RF frequency by using this modulator. Such a two stage upconversion scheme in general can be easily AC coupled eliminating any DC offset problems. Further more, a two stage upconversion scheme reduces the possibility for the RF LO to be transmitted through the antenna, allowing for the use of a single balanced mixer in the modulator. Furthermore, a two stage up-conversion scheme allows for the generation of the quadrature LO signals at a lower frequency and/or in the digital domain which would result in a better amplitude and phase tracking between these signals. A single upconversion scheme, would require very good isolation on the mixer LO port and its output port. In general this is achieved by using a double balanced mixer. If a single balanced mixer such as the one shown in FIGURE 21.c is used in a single-stage upconversion scheme (and sometimes even for double upconversion modulation), the LO is input through Q1, and the baseband signal through Q2 and Q3. This is done to achieve maximum rejection to the LO at the output port of the mixer.

Generally, single balanced mixers offer a better noise performance than their double balanced counterparts for the same power consumption, and are therefore more frequently used in front end receiver applications. In a transmitter application, however, noise performance is typically much less of an issue than the isolation of the output port to the incoming signal and to the LO, and hence double balanced mixers are typically utilized in these applications.

The quadrature modulator used in this system is based on a double balanced architecture and is manufactured in GaAs technology.

5.5.1 DC Offsets

5.5.1.1 DC offsets in CDMA systems

DC offsets in a DC coupled systems can be extremely devastating. For example in a CDMA application, if the amplitude of the carrier signal generated due to the DC offset is larger than the processing gain of the system, the system will completely die and the BER will tend to go to unity. This is because in effect the DC offset generates a DC voltage at the input ports of the differential amplifier of the mixer input (FIGURE 33). When this DC signal is mixed with the LO, it generates a tone at the carrier frequency. In other words, DC offsets degrade the carrier rejection of the mixer. The amplitude of the carrier tone will be a function of the DC offset, the LO power and the gain of the mixer.

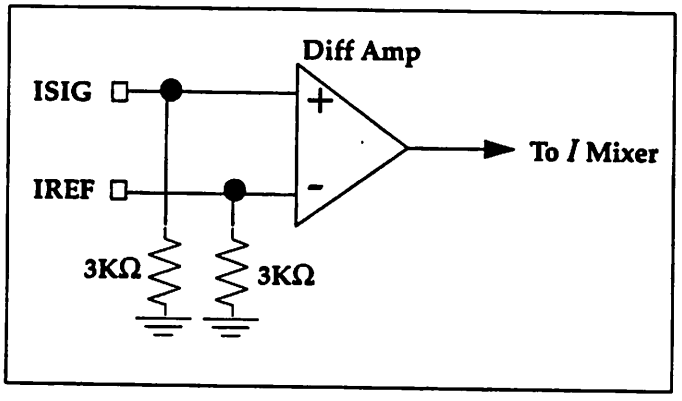


FIGURE 33. Model of the in-phase (*I*) port of the quadrature modulator

In a CDMA application, the strong carrier resulting from a DC offset (or from any other means, e.g. LO feed-through in a direct up-conversion transmit scheme, or in a homodyne receive scheme) is in a sense an in-band interferer, at its worst. At the receiver despreader, any interfering signal is *spread*, whereas the wanted signal is *despread*. If the interfering signal is at the center of the band of interest, its entire energy will fall in band after being spread by the receiver correlator. Hence if the amplitude of the interfering signal at the carrier frequency is higher than the spread signal by a factor equal to the spreading gain of the system, after the despreader the achieved SNR would be 1 or 0dB. Clearly this will result in an extremely poor BER. In the case of a sinusoidal interferer which is not in the center of the band (military jamming, for example where the enemy does not exactly know the carrier frequency, or a microwave oven operating at a frequency different than the car-

rier frequency of the transmitted signal), only the portion of the spread jammer signal that falls in band affects the system performance.

Any DC offset resulting in a carrier more than 15dB over the spread signal will annihilate this system if the system were operating with a 15dB processing gain. In out particular modulator, this translates into about 100mV of offset on the *I* or *Q* channel inputs. Of course this is a very large offset and would typically not occur unless the system is poorly designed.

5.5.1.2 DC offsets in Suppressed Carrier Analog Modulation Systems

In suppressed carrier analog modulation schemes the in band carrier is undesirable because it carries much power with no information content. The high signal power of the carrier can result in the generation of excessive distortion in the transmit and receive circuitry, reducing from the dynamic range of the system. On the other hand, unsuppressed modulation schemes such as the traditional AM take advantage of the carrier at the receiver envelope detection.

5.5.1.3 Causes of DC offsets in the transmitter section of this system

In the case of this system, DC offsets can be caused by the input differential amplifiers of the modulator itself and by the digital circuitry (when directly feeding the modulator) and/or the DAC and its output buffers. Furthermore, PCB layout can also contribute to DC offsets.

5.5.1.4 Methods of reducing DC offsets

The DC offset can be reduced by utilizing a DAC at each of the reference inputs of the modulator with a resolution equal to the offset error required (based on FIGURE 34). The DC offset generated may also be reduced by injecting a digitally generated offset in the *I* and *Q* input sources.

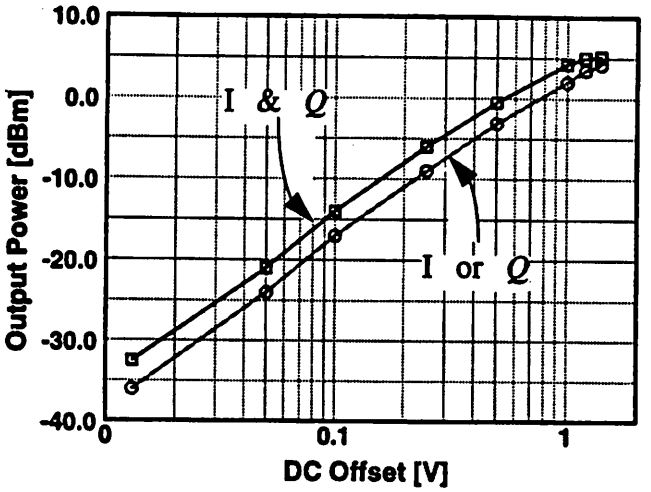


FIGURE 34. Measured output power when only dc offset(s) is applied to the input ports of the modulator IC.

FIGURE 34 shows the resulting carrier output power as a function of the DC input voltage, when no other signal but the DC offset is applied to the system. For this measurement the LO power was set to 0dBm. In the best case, when no external DC offset exists, the carrier rejection of the system is about -36dBm and is primarily a function of DC matching within the IC. The "I & *Q* Offset" indicates the case where the indicated DC offset voltage is applied to both the *I* & *Q* ports, whereas the "I or *Q* Offset" indicates when the offset was only applied to one of the ports. In reality for the latter case, the *I* port was subjected to the offset, and the *Q* port inputs were tied to a 2.5V DC voltage. As expected, the output power of the carrier is 3dB (2x) more for the "I & *Q* Offset" as compared to the "I or *Q* offset." Over 1V of DC offset causes the mixers to distort significantly (the limiting seen in FIGURE 34).

5.5.2 AC vs. DC Coupling of the Inputs

Whether a system is designed to be AC or DC coupled is dependent on many criteria. For example, in general, DC coupling is best for single up-conversion systems. In such systems, the baseband signal is directly upconverted to the carrier frequency. If AC coupling is used to couple the input to the upconverting mixer, a portion of the baseband spectrum will have to be chopped off, since AC coupling is in effect a high pass filter. The filter cutoff frequency is dictated primarily by the capacitance of the AC coupling stage and the resistance which it sees. Since many times this resistance is fixed by other system requirements, the only flexibility the designer has is to change the coupling capacitor's value.

5.5.2.1 Start-up and Streak Transients

In AC coupled systems, the designer has to be aware of the start-up transients. As the system initially starts operation, many symbols may be lost due to the initial transient introduced by using the AC coupling capacitors. Furthermore, the designer should be aware of the effect of long streaks of 1's or 0's in the system performance, as this will cause the common mode voltage of the system to drift up or down, resulting in a major system per-

formance degradation. The start-up or streak transients, in effect cause a DC signal at the input of the modulator resulting in all the problems that DC offset voltages cause in a DC coupled system.

The start-up transient problem may be solved by using tri-statable output stages at the output of the DAC so that the common mode signal stays at the proper voltage (around 2.5V for our system) during the non-active times.

The streak transient problem is not a problem in CDMA applications. This is because the data is encoded by a pseudo-random (PN) sequence which has approximately the same number of 1's and 0's in one period. Furthermore, the nature of a PN sequence guarantees that no more than a small determined number of 1's or 0's will come in a sequence. For non-CDMA applications, the problem of streak transients may be overcome by utilizing some kind of line-coding scheme (multiplication by a PN sequence, is in fact one method of line coding).

Based on the above arguments, AC coupling of the inputs is best for 2 (or more) stage up-conversion systems. In our system, for example, AC coupling could be effectively used in sequence with a digital modulator taking the baseband signal to an IF of less than 100MHz (since 100MHz is the highest input frequency that the analog modulator can accept).

If a DC-coupled system is used with no provisions to avoid start-up transients, some symbols will be lost at the initialization of the transmission sequence. The number of symbols lost is dependent on the size of the coupling capacitor, the symbol rate, and other factors. The smaller the size of the capacitor, the less time it will take for the DC offset across the input ports of the modulator to disappear and the signal to "settle." On the other hand, the smaller capacitor will chop-off more of the baseband signal of interest, hence the trade-off. At the same time, a larger capacitor will cause it to take more symbols during a streak transient to cause problems and drift-off.

The start-up transient issue may or may not be a problem depending on the system configurations. On true CDMA applications, where multiple access is achieved by orthogonal codes, once data transmission is initiated, it will stay in effect until the user shuts down or moves into a different cell (where there may or may not be an initial transmission transient issue). Therefore in such systems, the initial transient issue may not be a problem, particularly at high data rates. The first n symbols can be ignored at the receiver if necessary before a proper link is established. In other systems, such as a CDMA/TDMA based systems, where CDMA is only used to lower the power spectral density of the transmitted signal, but multiple access is achieved through time division, the initial transient may be an important issue, since the problem arrises at the beginning of the transmission *every* time a user is selected (at the beginning of the users time slot).

5.5.3 Methods of AC Coupling and DC Coupling in this System

To offer maximum flexibility, this system is designed to offer both AC coupling and DC coupling on the transmitter.

FIGURE 35 shows how the AC coupling part of the system is configured. This configuration is based on the equivalent input circuit for the input port of the modulator as shown in FIGURE 33. The high pass filter roll-off is dictated by the RC time constant where R is almost 100 ohms and C is the value of the bypass cap. The 2.5V reference supply needs to be able to source 3.2mA of current (2.5V on four 3.1KΩ loads). Note that in this case since both signal and reference are tied to the same reference voltage, the only systematic external DC offset (and resulting deterioration of the carrier suppression) would be due to any mismatches on the 100 ohm resistors. Note also that the driving signal source (I_{in} and Q_{in}) will have to be able to provide the required voltage swing on a 100Ω load.

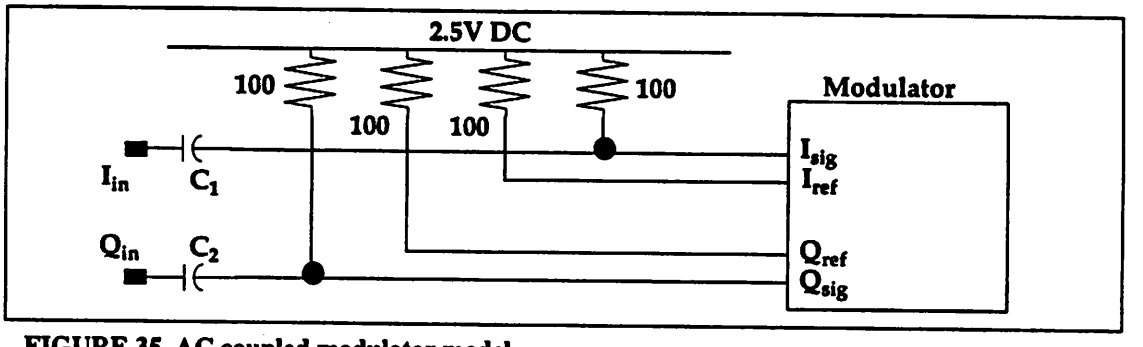


FIGURE 35. AC coupled modulator model

To illustrate the start-up and streak transients discussed above, the model was further simplified and simulated (FIGURE 36). It is important to note that the value of the resistor was chosen *much* smaller than what would really be used in the system to allow for a reasonably short simulation time.

It may seem at first glance that the steady state voltage at node *A* is approximately 2.5V, and since the voltage across the capacitor can not change instantaneously, every time a pulse is applied at the input the voltage at node *A* will have to follow, and hence the system will never settle. In reality, however, the voltage at node *A* will slowly move towards the common mode voltage of node *B* (the input) and the transient problem will be eliminated. As mentioned before, observing in a real system, this may take thousands of symbols, and hence require a very long simulation time on SPICE to observe. In a system with a symbol rate of 1MSPS, however, this will only take a few milliseconds and should be transparent to the user.

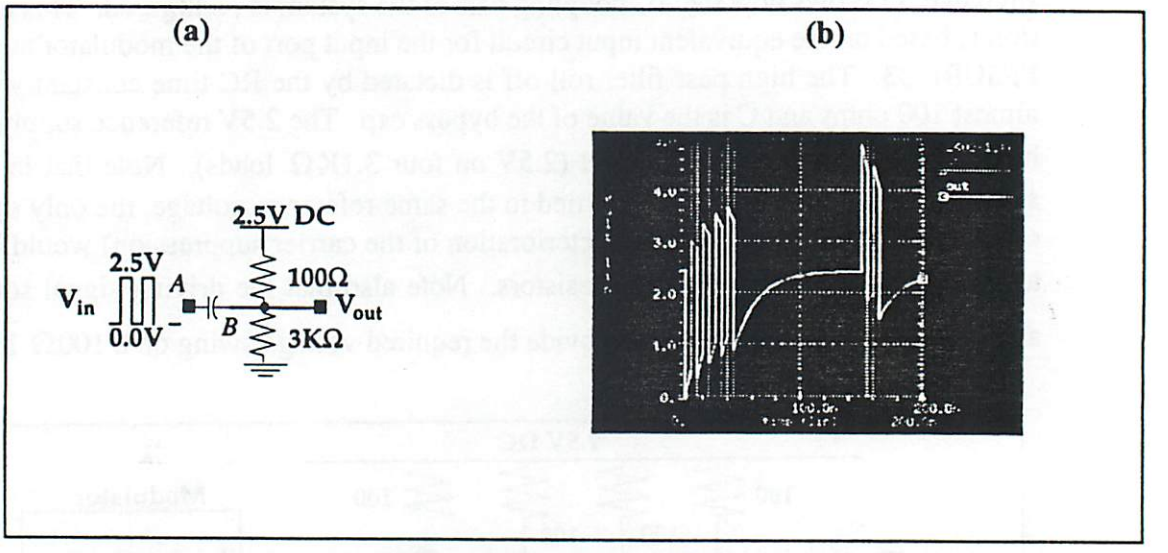


FIGURE 36. Start-up and streak transients due to AC coupling. (a) Simplistic model. (b) Transient Behavior

The DC coupled system (transmitter side) is shown in Appendix F, "The Schematics".

5.5.4 The Local Oscillator Level

The LO signal is internally hard-limited within the modulator IC for reasons explained in section Section 5.1.5, "LO Power". The limited signal is subsequently used to generate the quadrature components of the LO. In general, the higher the LO level, the less sensitive the system is to mismatches in the switching transistors, and therefore the better the phase and amplitude tracking on the *I* and *Q* channels. A high LO level also translates to a better noise and distortion performance on the mixer. A high LO level, however, can degrade the carrier suppression of the system. A proper compromise therefore has to be made between the above factors in the system.

5.5.4.1 Output Power Control on the Modulator

A system designer has a modest control on the modulator output power through the amplitude of the LO signal. Furthermore, the output signal level is a function of the magnitude of the voltage swing imposed on the input ports of the modulator (clearly the distortion generated by the modulator increases with increasing input signal levels). FIGURE 37 shows the output power of the modulator IC as a function of the LO power for two different peak-to-peak input levels. Based on the factors discussed in the previous sections and the desired output power from the modulator, and the voltage swing imposed on the input ports of the modulator, an LO power can be selected. For example, input sinusoidal signal levels of 1 Vp-p and an LO level of 0 dBm would yield an output signal of approximately -4dBm. Although a power amplifier has not been designed in the transmitter of this module, OSMT miniature coaxial connectors have been provided at the output of the modulator for the use of an external power amplifier if required. In the above scenario, a power

amplifier with a gain of approximately 7 dB can be utilized for 0 dBm delivered power to the antenna (this accounts for the loss in the front end switches and filter).

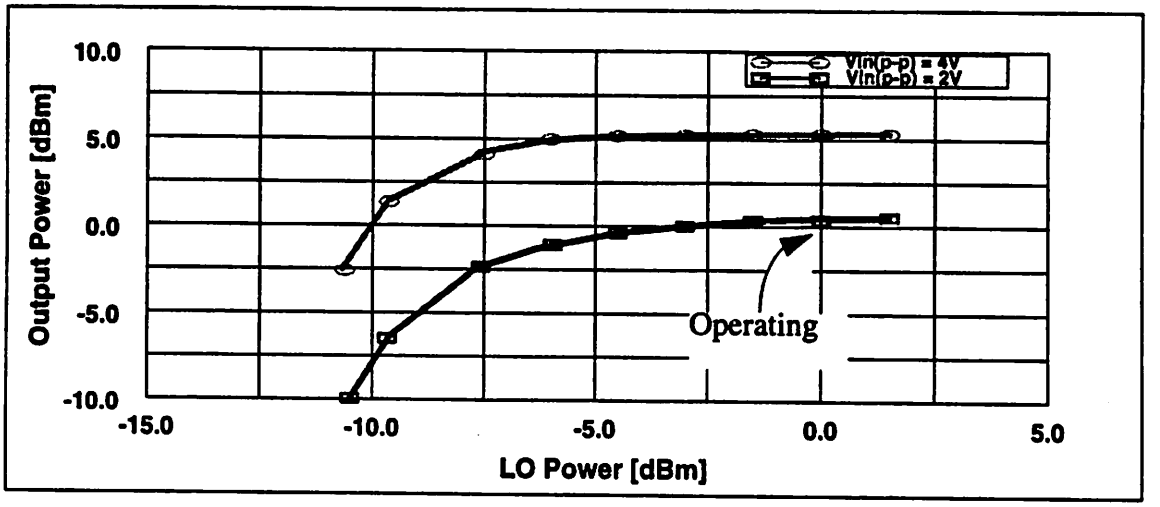


FIGURE 37. Double sideband output power of modulator IC as a function of the LO power for two different values of input I and Q swings.

The (double sideband) output third order intercept point of the output amplifier of the modulator is approximately +13 dBm. Therefore two -4 dBm output tones would result in third order intermodulation components at -38 dBm, or a third order intermodulation rejection of 34 dB. If this system were to be used with the Infopad QPSK/DQPSK modulation, a modulator output level of 0 dBm would yield acceptable linearity performance (third order intermodulation rejection of 26 dB).

It is not necessary to filter the output of the DAC immediately before the modulator as long as the extra power of the aliases do not cause premature distortion of the modulator or its buffer amplifiers. The filtering can be performed after the modulation process, or partially before the modulator and partially after the modulator. The latter scheme is the one utilized in this system. A simple relatively wide-band LPF filters the output of the DAC before the modulator. The remaining of the filtering is performed by the front-end ceramic filter. The total filtering required is primarily dictated by the amount of attenuation required out of the operation bandwidth as dictated by the regulatory agencies (e.g. FCC).

5.6 The Transmitter DAC Buffers

Many criteria, including those mentioned in Section 5.4.5, "Voltage vs. Current Feedback Opamps," were considered in selecting the DAC buffers. These buffers were selected to be of the voltage feedback type primarily because of the large input common mode range required.

5.7 Filters

System designers are well aware of the problems associated with filters. In general, filters are very costly, often, the most expensive elements of the system. They typically consume large board areas. Furthermore, non-active filters require impedance matching at their inputs and outputs.

5.7.1 System Architecture Implications on Filtering in the System

Many elements govern the type of filters used in a system, the number of filters used, and their placement. One of these factors is the system architecture. For example the superheterodyne architecture was mainly designed to overcome the need for a costly sharp tunable front-end filter for tunable frequency applications such as the AM radio. This architecture is by far the most common receiver architecture used to date for both tunable applications and fixed-frequency applications.

5.7.1.1 Homodyne vs. Superheterodyne Receiver Architectures

There is a major motivation to move to a direct conversion (homodyne) receiver, particularly for fixed frequency applications. A homodyne architecture eliminates the IF stage and its associated filters, reducing the cost and area required by the system considerably. Furthermore, much of the filtering can now be performed in a LPF form as opposed to a BPF format at baseband. Many attempts have been made to design homodyne receivers. The success of homodyne receivers has been relatively limited, and specific to a few relatively low-speed applications.

There are many difficulties associated with a direct conversion architecture. Some of these problems are listed below:

- The LO of the receiver can leak through to the antenna and be radiated
- The isolation of the LO from the RF port should be very good. Depending on the application this isolation may need to be as good as 100dB or more. Achieving such isolation is very difficult particularly in monolithic technologies because of substrate coupling effects. The problem arises from the fact that the fed-through LO signal can mix with itself and generate a DC component. Since in general for a homodyne receiver the system components cannot be AC coupled at baseband, this introduces a DC offset. If an offset cancellation scheme is not used, depending on the gain of the baseband amplifiers, this DC offset can saturate the baseband components.
- The gain of the receiver will have to be distributed in two stages only. Since achieving high amounts of gain at the RF frequency is difficult if not impossible, most of the gain will have to be realized at baseband. Having stages with very high amounts of gain makes those stages and the system prone to instability due to potential high frequency feedback paths and the associated high loop gain.

In quadrature receivers (e.g. QPSK) there are additional problems also associated with a homodyne receiver:

- The quadrature demodulation (IQ separation) will have to be performed at the RF frequency (since it clearly cannot be performed at baseband). The generation of high frequency, accurate quadrature LO's is very difficult and would consume more power than its low frequency counterparts (e.g. many IQ demodulators rely on a 2X or 4X LO frequency to generate the Sin and Cos). Therefore it would be difficult to maintain phase and frequency accuracy between the *I* and the *Q* channels.
- Since the IQ separation is performed early on, the signal path is separate for much of the receiver chain. This would further degrade the phase and amplitude balance between the IQ channels as they are subject to different components down the chain (mismatch effect).

Despite all of the above problems, because of the reduction in the overall number of filters in the system, a homodyne architecture should be investigated carefully as it can result in an elegant, compact and low cost solution.

In the case of this board, the availability of commercial components limited the system architecture to a superheterodyne.

5.7.2 Filter Types

A system designer has several choices in choosing a filter. Below, a few of these choices are listed with some explanation of their advantages and disadvantages.

5.7.2.1 Commercial LC Filters (Hybrids)

These filters are typically available from DC to over 1GHz. At the high frequency end, these filters are limited primarily by the self-resonant frequency (SRF) of the inductors which is to the first order due to the parasitic capacitance of the package. Depending on the type of filter, the *Q* of the inductors (as determined by their series resistance) may also limit the upper frequency range. Furthermore, for the higher frequencies, the small values of the inductors and/or capacitors (which become comparable to the package/board parasitics) and the associated tolerance levels also become a limitation. In some filters the parasitic series inductance of capacitors can also become a major source of problems. This is particularly true for the larger value capacitors (See section 5.7.2.1.D, "Physical Capacitors").

At the very low frequencies, the size of the capacitors and inductors may get prohibitively large.

At the higher frequencies, printed circuit board parallel plate capacitors and spiral inductors become practical to utilize (See section 5.7.2.2.A, "On Board Capacitors and Inductors"). For an input and output impedance of 50 or 75 ohms, typical of many communication systems, this "higher" frequency is about 1GHz. It is interesting to note that the upper UHF bands of 500MHz to 1GHz have been traditionally a region where the proper size L's and C's have been difficult to come-by. The surface mount chip capacitors and inductors typically support filters up to about 500MHz, and the PCB type L's and C's support the bands over 1GHz.

Commercial LC filters can typically achieve a wide range of fractional bandwidths (3dB bandwidth / carrier frequency) ranging from less than 5% to over 90%.

The insertion loss of these filters is typically low, and primarily a function of the series resistance of the inductors used in the filter (the Q of the inductors). In many cases, the highest frequency an LC filter can support is determined by the self resonant frequency of the inductors.

5.7.2.1.A Physical Inductors

The SRF of an inductor is primarily a function of the parasitic capacitance associated with that inductor. This parasitic capacitance is mostly caused by package capacitance. The SRF of an inductor (or capacitor) is given by the simple resonance formula

$$\omega_{SRF} = \frac{1}{\sqrt{LC}} \qquad \text{(EQ 47)}$$

Hence, inductors with larger values (for a given package type) will typically have a lower SRF. Effectively, the impedance of these inductors increases with frequency as it should until the SRF, after which it starts to decrease (capacitive behavior). This behavior is shown in FIGURE 38.(a), (b), and (c) as predicted by an impedance analyzer, network analyzer and SPICE respectively. A simple lumped element model for a physical inductor is shown in FIGURE 38.d. Ideally, an inductor should be modelled as a distributed element with intermitting parasitic capacitance, self inductance, mutual inductance and resistance. The resulting model would be too complicated for most practical applications. FIGURE 38.d represents a good compromise between complexity and accuracy.

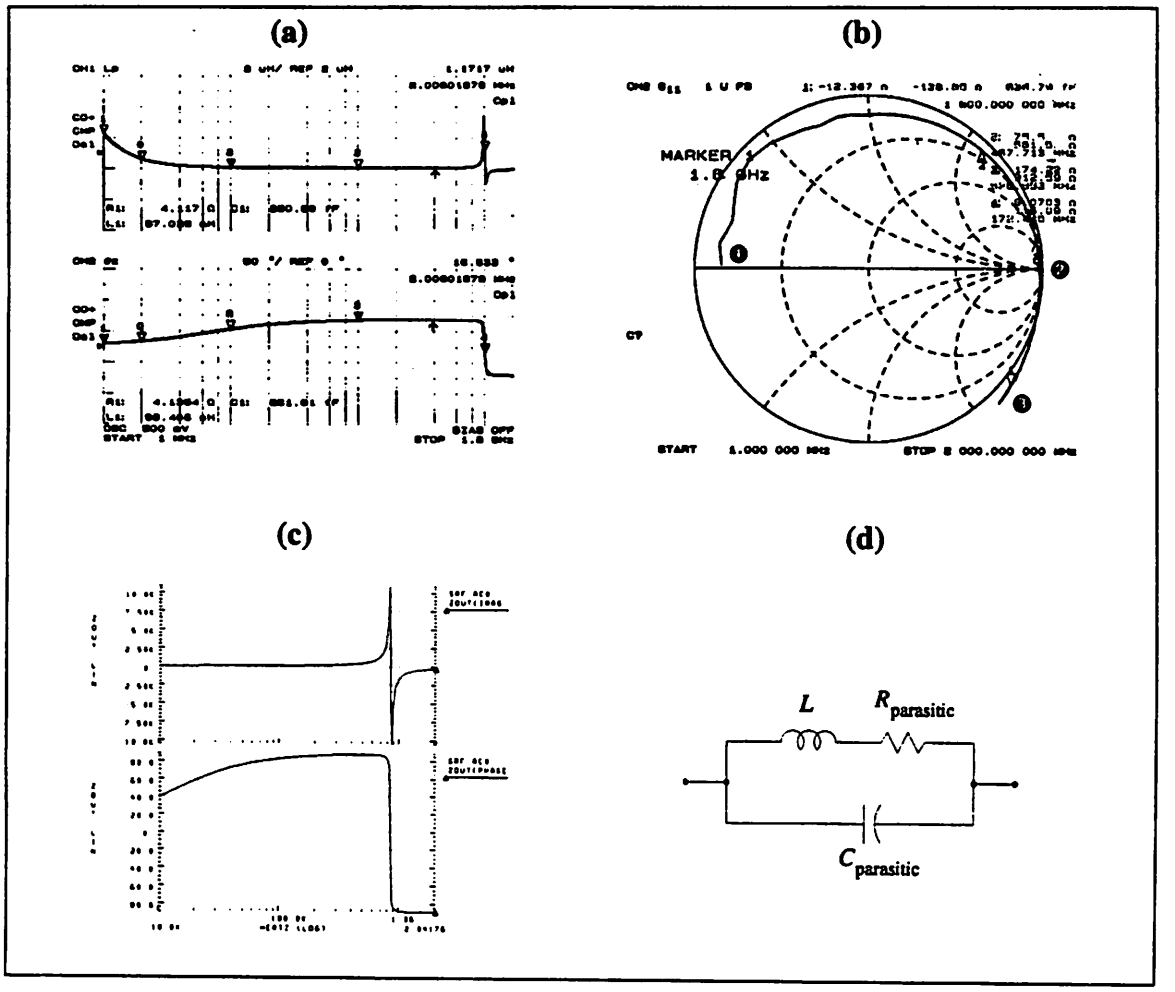


FIGURE 38. The behavior of a surface mount 1206 (12 mil x 6 mil) inductor as a function of frequency. (a) Measured with an impedance analyzer (b) Measured with a network analyzer (c) Simulated with SPICE (100nH, 7Ω, 350pF). (d) Physical model. The manufacturer specifies the part as 100nH ± 5% at 200 MHz, with a minimum SRF = 850 MHz and $R_{dc,\,max} = 7\Omega$.

One of the most accurate methods of obtaining the impedance of a component is the use of an impedance analyzer. An impedance analyzer is a specialized network analyzer with a significantly higher accuracy at high values of VSWR than a general purpose network analyzer, along with specialized calibrated fixtures for various size components.

5.7.2.1.B Network Analyzers vs. Impedance Analyzers for Measuring Inductance

A general-purpose network analyzer can also be used for measuring the value of an inductor or capacitor in the Smith Chart S_{11} measurement mode. Since a general purpose network-analyzer does not have sufficient resolution at high values of VSWR (e.g. on the outer perimeter of the Smith Chart) the measurements are typically not accurate. If the measurements are performed at a frequency significantly below the SRF of the component, however, the measurement is relatively accurate. Furthermore, the network analyzer provides a single reading for the imaginary part of the impedance (which is calculated

from the impedance of the two-port at that frequency and the value of its resistance at that frequency). This value is the *net* reactance of the two-port. WIth a single measurement, it would not be possible to determine the values of the L and $C_{parasitic}$ of FIGURE 38.d. The value of the inductance obtained with this method is therefore accurate for frequencies significantly below the SRF of the component. At the higher frequencies a significant and unrealistic variation of the value of the inductance is observed as a function of frequency.

As expected, the 100nH inductor behaves as a short circuit at low frequencies (point ❶ of FIGURE 38.b). As the frequency is increased it passes through its SRF at point ❷, and resembles a capacitor at higher frequencies. An inductor with an infinite Q (zero series resistance) would lie on the outer most circle of the Smith Chart. The fact that the measured curve lies inside the Smith Chart for frequencies below SRF signifies resistive losses in the inductor. Theoretically, the Q of the inductor at any frequency can be measured using this method on the network analyzer, but typically the calculated values are very inaccurate. At point ❸ of FIGURE 38.b the inductor displays gain. Clearly this is not possible and is due to calibration error on the network analyzer.

Simple equivalent models of physical components can be defined for many impedance analyzers. The impedance analyzer can then use the obtained impedance at multiple frequencies to calculate the values of the equivalent model. This allows for a much more realistic measurement of the value of a component.

The SRF obtained on a spectrum analyzer is typically on the pessimistic side.

5.7.2.1.C Monolithic Inductors

In an effort to achieve a single chip receiver, much research has been done and continues in the area of monolithic LC filters. In a traditional Si process, relatively good performance capacitors can be achieved. The capacitor values that can be achieved, however, are small, and therefore well suited for high frequency LC filters (over 1GHz). The Q of the achievable inductors, however, are very low to be suitable for most filtering applications (typically less than 5). This is because of the parasitic series resistance associated with metal traces (aluminum). Widening the traces, will reduce the series resistance and allow a better Q, but at the same time, it increases the parasitic capacitance and hence reduces the SRF. A trench-isolated "thicker" metal trace may be an interesting solution (maintains low series resistance and low capacitance). In GaAs processes, the parasitic capacitance of the substrate layer is smaller, and therefore higher Q inductors with relatively high SRF can be achieved.

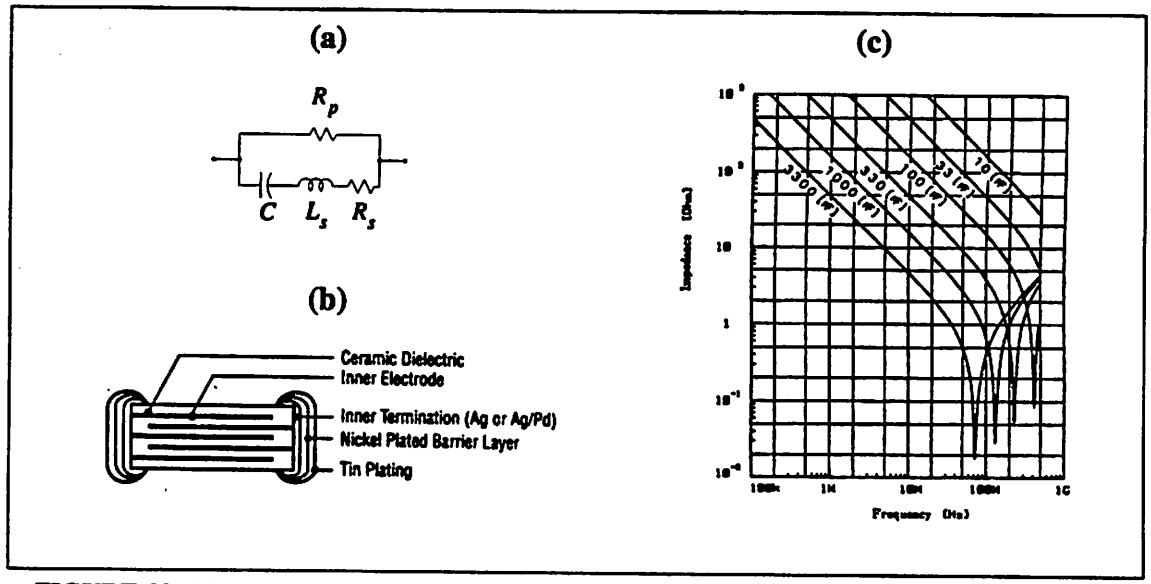


FIGURE 39. (a) Model for a physical surface mount capacitor. (b) Physical structure of a multilayer surface mount capacitor (after [32]). (c) Impedance of a family of surface mount capacitors as a function of frequency, displaying the SRF and the series resistance (the value of the impedance at resonance).

5.7.2.1.D Physical Capacitors

A model for a real capacitor is shown in FIGURE 39. R_p is due to the capacitor dielectric leakage, it is in the 10's of KΩ and results in a finite Q for the capacitor ($Q_c = \omega C R_p$). R_s represents the series resistance of the (inductance associated with the) capacitor and is in the 100's of mΩ for surface mount capacitors. The series inductance is due to the package and the leads (in the case of a through hole component) and translate into a finite SRF. Clearly, surface mount packages offer the smallest amount of parasitic inductance and hence the highest SRF. As a general rule, for a given type of package, the SRF of the capacitor reduces with the increasing value of the capacitor according to the simple resonance equation [47]. In some cases, however, higher value capacitors can be composed of multiple layers, with a reduction in L_s and R_s as compared to the smaller valued capacitors with the same package type. For example for small 1206 (12 mil x 6 mil) surface mount capacitors $L_s \approx 1$ nH, whereas for larger value 1206 capacitors $L_s \approx 0.5$ nH.

5.7.2.1.E Effect of Finite Q on Filter Performance

Low Q inductors can be used effectively in applications such as chokes. The requirement for better Q's and better tolerances, however, are more outstanding in high order filters and particularly in filters with a high sensitivity to pole (and zero) locations (e.g. elliptic, Chebychev). For example, a tenth order Bessel filter would require components with a Q of about 2 whereas a tenth order 1 dB ripple Chebychev filter would require a Q of more than 60. In general, as a result of finite Q elements, the insertion loss of the filter is increased, but typically the stopband-rejection is maintained. Finite Q components also cause the

amplitude response to become smoothened (rounded) and tend to reduce the ripples in a Chebychev filter, and reduce the rejection of elliptic filters in the vicinity of the zeros.

In the s-plane, the effect of a finite Q is to shift the poles to the left by an amount equal to 1/Q (increase the magnitude of the real component of the pole at the same imaginary component magnitude). Therefore, the effect of the finite Q of the elements can be compensated for by "pre-distorting" the pole locations to the right by an amount equal to 1/Q. Clearly, the limitation here is governed by the highest Q pole in the filter. The poles can be pre-distorted by a maximum amount equal to $Re\,(s_i)$ where s_i is the location of the highest Q pole of the filter in the s-plane.

5.7.2.1.F Frequency and Impedance Scaling in LC Filters

Another important issue is the scaling of the filter components with the required input and output terminations and with the operating frequency. Since the impedance of a capacitance is given by $Z_C = 1 / j\omega C$ and the impedance of an inductor is given by $Z_L = j\omega L$, it is clear that *for the same input and output termination*, as the frequency increases (is scaled up), the inductors and capacitors both get smaller. On the other hand, by Bartlett's Bisection Theorem, the input and output impedances are scaled up, *for the same frequency*, in order to maintain the same impedances throughout the filter, the values of the inductors are scaled up and the values of the required capacitors are scaled down.

Many times, particularly at the IF frequencies (about 100MHz), IC designers prefer to drive large impedance external nodes to reduce the power consumption and the need for sourcing (and sinking) large amounts of current. Many commercial filters however require 50Ω or 75Ω input and output impedance. This is because for the higher impedance input and output filters (say $1K\Omega$), the values of the capacitors get too small to maintain a reasonable tolerance and the values of the required inductors increases such that maintaining a high enough SRF would become very difficult (FIGURE 40).

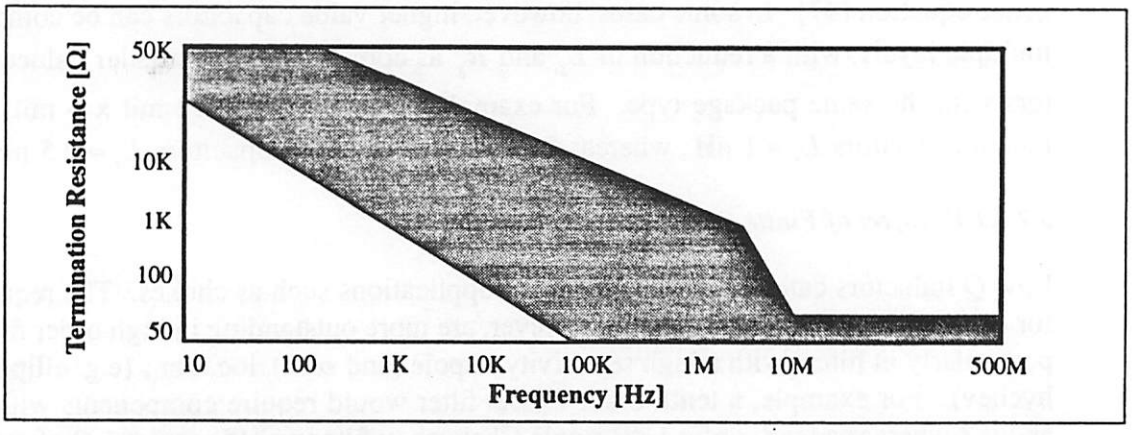


FIGURE 40. Typical available commercial LC filters as a function of frequency and input and output termination. Higher frequency LC filters require lower values of input and output termination due to physical limitations.

5.7.2.1.G Tolerance and Matching of Components in LC Filters

Another important issue is the tolerance and matching of the components. With discrete implementations of LC filters, much effort is spent in tuning variable capacitors and inductors to achieve the proper response. In a production type environment this is a very costly operation. In a monolithic implementation, tuning such filters would be even more of a challenge. Switch capacitor type filters overcome the matching problem by making the poles of the system depend on the *ratio* of capacitors as opposed to their absolute value.

5.7.2.1.H Classical Amplitude vs. Phase Trade-off in LC Filters

LC filters suffer from the well-known amplitude vs. phase trade-off. In other words sharp amplitude filters such as the Chebychev have a non-linear phase response (non-constant group delay) whereas linear-phase (constant group delay) filters suffer from a slow roll-off in the amplitude response.

5.7.2.1.I Use of Bond Wires as On-Chip Inductors

Currently research is also underway in the use of the package bond wire as the inductive elements. This approach seems to be a reasonable one, since a bond wire offers an inductance of approximately 1nH/mm. This approach has been utilized in the LNA/mixer IC used in this system.

Researchers are also working on the application of printed capacitors and inductors in multi-chip module (MCM) technologies.

5.7.2.1.J Air Core Inductors vs. Ferromagnetic Core Inductors

In general, ferromagnetic core inductors offer a higher amount of inductance in a smaller area than their air-core counterparts (this is due the ferromagnetic material's $\mu \gg 1$). Furthermore, they help contain the magnetic field and reduce EMC problems. On the other hand, they are typically more difficult to manufacture and very fragile. Because of core losses, they typically have a lower Q than the air-wound inductors. Finally the ferromagnetic core can be driven into saturation due to large amount of current.

5.7.2.1.K Use of Metal Cans to Contain Fields in Filters

Hermetically sealed or metal canned LC filters reduce coupling effects between the LC filter and their surrounding world, and reduce the interaction between the filter and other system components. Of course this comes at the expense of added weight and cost of filter. It is important to note, however, that typical metal cans (packages) do *not* significantly reduce the low frequency magnetic coupling between the filter and the outside world. Low frequency magnetic fields are the most difficult to contain. The containment of these signals requires the use of ferromagnetic material packages which increases the cost of the package significantly and is usually not done (See section 6.9.2, "Magnetic Shielding vs. Electric Shielding").

5.7.2.2 Custom LC filters

Custom LC filters in general have the same characteristics as the commercial ones listed above. A few exceptions are outlined in this section.

5.7.2.2.A On Board Capacitors and Inductors

The use of printed circuit board inductors and capacitors is popular at frequencies above 1GHz. Obtaining both printed circuit board capacitors and inductors, however, may be at odds. This is because, to obtain high valued capacitors, one needs to place adjacent PCB layers closely (small width of dielectric, d, in equation [48]). However this causes the inductors printed on the same layers to have a low SRF because of the high valued *parasitic* capacitance. One solution may be to use multiple layer printed circuit boards (PCB) with different dielectric widths. It is important to note that, however, PCB manufacturers prefer producing PCB's that are symmetric with respect to the center (e.g. in a four layer board, layer 2 has the same distance from the middle of the board as does layer 3, and the dielectric thickness between layers 1 to 2 is equal to the dielectric thickness between layers 3 and 4).

In general, the simple capacitance equation, given by

$$C = \frac{\varepsilon A}{d} \qquad \text{(EQ 48)}$$

applies in calculating the PCB printed capacitance, as long as the fringing effects are minute. This would require the capacitor area to be large in comparison to the capacitor perimeter. The largest area/perimeter geometries would produce the most consistent and smallest tolerance capacitances for two main reasons. First, the fringing capacitance is due to a much less contained field than the actual parallel plate capacitance, and is therefore much more prone to the capacitor's outside world (which may vary from time to time). Second, because of random edge effects (inaccuracies in the edge definitions in the manufacturing process), it is usually best to maximize the above mentioned ratio. It is therefore advantageous to use geometries that offer large area/perimeter such as circles and squares.

A rule of thumb for the inductance of a *free-space* wire is about 1nH/mm. This rule of thumb works as long as the length of the wire is much longer than its (cross-sectional) diameter. This is why in general IC packaging bond wires offer a good source of inductance for potential use in IC technologies. As the diameter of the wire increases, its inductance decreases, and as it approaches the length of the wire, the above approximation no-longer holds.

The free-space inductance per unit length of a wire can be approximated from

$$L_{free-space} = 2\times10^{-1}\left[2.303\left(\log\frac{2l}{r}\right)-0.75\right] \text{ [nH/mm]} \qquad \text{(EQ 49)}$$

and the inductance of a straight wire parallel to a ground plane with one end grounded can be approximated by

$$L_{adj\_gnd} = \frac{1}{l}\left(4.605\times10^{-1} l\left\{\log\left[\frac{2h}{r}\left(\frac{l+k}{l+p}\right)\right]\right\} + 2\times10^{-1}\,(p-k+0.25l-2h+r)\right)$$

(EQ 50)

where l is the wire length in mm, r is the wire radius in mm, h is the height of the wire over the infinitely large ground plane, $p = \sqrt{l^2-4h^2}$, and $k = \sqrt{l^2+r^2}$.

equation [49] and equation [50] have been plotted in Figure 41 for r = 1mm. Clearly, both equations apply for regions where l is relatively large as compared to h and r. Otherwise these equations would result in a negative or complex inductance value.

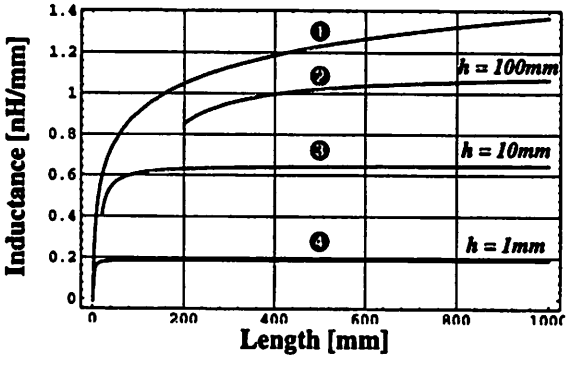


FIGURE 41. Self inductance of a wire. ❶ Straight wire in free space using equation [49]. ❷,❸, and ❹ Straight wire parallel to a ground plane with one end grounded using equation [50]. r = 1mm in all cases.

As evident from Figure 41, the rule of thumb mentioned above does apply to printed circuit board inductors if they are separated from an underlying ground plane by a small distance. The existence of an adjacent ground plane reduces the inductance value significantly and no simple rule of thumb then applies. The existence of the ground plane, however, results in an unit length inductance value which is relatively constant as a function of the length of the inductor.

Due to space limitations on printed circuit boards, square or circular spiral inductors are frequently utilized to achieve reasonable size inductor values (more recently printed inductors are also being utilized on Si IC's as well as MCM technologies). The simplest model for the inductance of a square spiral printed inductor is given by [15]

$$L_{sq\_spiral} = 8.5\sqrt{A}n^{5/3}\ \text{[nH]} \qquad \text{(EQ 51)}$$

where n is the number of turns and A is the area of the spiral in cm^2. The accurate modelling of the impedance of a spiral inductor requires considerations of self-inductance,

mutual inductance and the capacitance of the turns and requires CAD tools. A significant amount of the overall inductance of a spiral inductor is due to the mutual inductance between adjacent sections. It is important to note that the current flows in the same direction in adjacent sections, increasing the overall inductance of the structure.

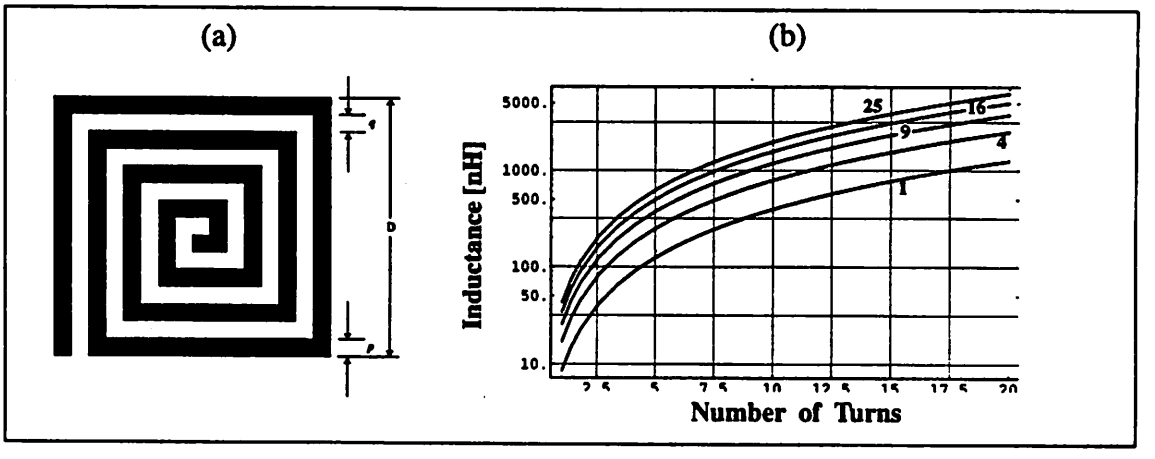


FIGURE 42. (a) A printed circuit board (or MCM) spiral inductor. (b) The inductance of the spiral inductor based on equation [51]. The numbers on the curves indicate the area of the spiral inductor A in cm^2.

5.7.2.2.B Input and Output Impedance Control

An advantage of custom LC filters is that the system designer has the control over input and output impedance (within physical constraints mentioned in Section 5.7.2.1.F, "Frequency and Impedance Scaling in LC Filters") and is therefore not locked into the input and output impedance offered by commercial filter manufacturers.

5.7.2.2.C Dielectric Loss Effects on Filter Response

It is important to consider the effect of a finite dielectric loss for PCB based capacitors and inductors, particularly at the higher frequencies and when high Q elements are required. Since Q is defined as the energy stored to energy dissipated per radian of oscillation, any factor that increases the dissipation in the system, reduces the effective Q. This is one of the reasons why low-loss dielectrics (substrates) such as ceramics are used instead of FR4 at the higher frequencies and/or when high Q 's are required.

5.7.2.2.D Modular Design of Systems that Utilize High Order Passive Filters

As a matter of practicality, for high volume productions, higher order custom filters are usually designed on daughter boards. This is because these filters require extensive tuning, which can be done in parallel with the main board assembly process, reducing the overall time of assembly. Furthermore, these daughter boards are many times sent overseas for inexpensive assembly and tuning. Utilizing a daughter board removes the need for sending the entire system overseas and back.

5.7.2.3 Active Filters (Custom and Commercial)

In general active filters offer many advantages over passive LC filters for certain applications. Most types of active filters do not require inductors. They obtain the reactive element by using principles of feedback (a shunt feedback mechanism for example offers inductive impedances). This fact makes them very attractive for Si monolithic implementations. Furthermore, they are in effect a buffering stage and therefore do not require input or output impedance matching.

A simple RC filter locates the poles of the filter on the negative real axis. In order to achieve complex pole values in a non-active filter more than two reactive elements must be used. In an active circuit this task is accomplished by using principles of feedback.

On the other hand, active filters require gain stages (typically opamps) with a high frequency response. The required frequency response is very much a function of the type of filter and the Q required, but in general should be at least several times more than the highest bandpass frequency of the filter for linear active filters. This requirement is typically even more severe for switch capacitor type of filters. This requirement has traditionally limited the use of such filters to lower frequency ranges. The advent of higher frequency processes and opamps in the recent years has resulted in an increase of the use of active filters at the higher frequencies, particularly for fully integrated solutions.

The traditional Sallen-Key filter is a popular linear active filter particularly for applications where a steep roll-off is not required, but a linear phase response and simplicity are desirable. For example, the use of a Sallen-Key filter along with a single transistor in the emitter follower configuration as its gain element can offer a high frequency response active filter which is useful as an ADC antialiasing filters [16]. FIGURE 43.a displays the schematic of a simple emitter-follower Sallen-Key filter. Note the positive feedback loop in this circuit. Underdamped ($C_1 < C_2$), critically damped ($C_1 \approx C_2$) and overdamped ($C_2 < C_1$) responses can be easily obtained from this structure as shown in FIGURE 43.b as indicated by ❶, ❷ and ❸ respectively. The bandwidth of this filter in the case of the maximally flat response is chosen to be 20 MHz (as required by this system operating at its maximum speed).

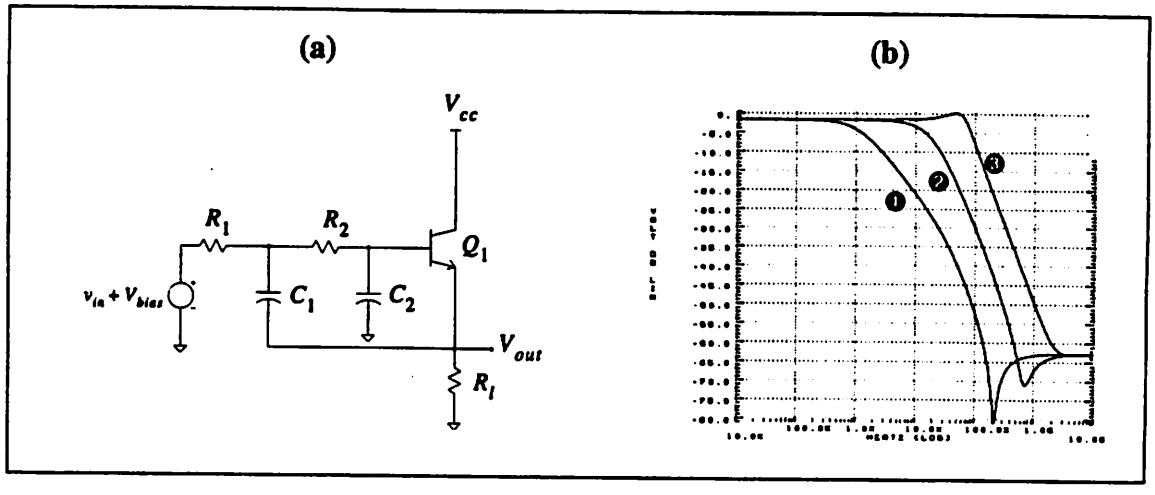


FIGURE 43. (a) Schematic of a emitter-follower based Sallen-Key low pass filter. (b) Output voltage of the Sallen Key filter for various ratios of C_1 / C_2.

FIGURE 43.b also displays the complex valued zero in the response of the filter. This zero is due to the forward transmission path from input to output due to C_1. Sallen-Key filters can be cascaded if necessary.

Active filters can also be implemented as sections of "biquads", with each biquad requiring two active gain stages and possessing a complex-valued pole as well as a complex-valued zero. Low-pass, high-pass, band-pass and notch filters can therefore be implemented using biquad sections. Each biquad section of a high-order active filter can be "impedance-scaled" independently to allow for realizable and convenient capacitor values for that section. The entire filter, however, has to be frequency scaled by the same factor. Due to difficulties of driving large valued resistors in monolithic CMOS technologies as well as due to the difference in the temperature coefficients of the L's and C's used on chip and its resulting time constant variations, active RC biquad sections are rarely used in IC forms [16].

Higher order filters can also be implemented by using a ladder structure. It can be shown that the transfer function of a ladder structure and its resulting filters are relatively insensitive to variations in component values. Subsequently, integrated gyrator-type active filters can be easily designed by substituting every inductor in the passive LC ladder filter schematic with a capacitor-gyrator (which behaves like an inductor). These filters exhibit small sensitivity to variations in the component values due to processing or temperature gradients.

Both biquad and ladder filters can be represented in flow-graph form, requiring integration, multiplication and addition operations, with integration as the most challenging operation at the higher frequencies. Continuous-time filters can be designed using the flow-graph representation and a variety of methods for implementing the integrators. The most popular high-speed continuous-time filters are based on transconductance-C integrators [16]. Tuning of such filters is generally difficult as compared to switched capacitor filters, but they offer much higher speed operation than the switch-cap approach.

Switch capacitor filters offer two major advantages as compared to other types of filters. First their response does not depend on exact values of capacitors, but on *ratios* of capacitors, which is much easier to control over temperature and process. Second, they can very easily be tuned by changing the switching frequency of the driving circuit (clock). On the other hand, the user must be aware and take proper precautions to avoid problems due to clock feed-through and aliasing of signals at frequencies close to the clock frequency. Furthermore, the clock circuitry can generate unwanted ripple on the supply lines which could interfere with sensitive circuitry on the same chip (and even on the board). Proper layout techniques should be utilized to minimize the effects of this noise on the low-noise front-end elements. The limited speed of switched-capacitor filters is due to their strong dependence on amplifier settling times.

Active filters suffer from the noise and distortion introduced by the active gain stage of the filter. Noise of the active element limits the use of active filters in the front stages of a receiver whereas the distortion of the gain elements limits the use of the filter in the latter stages of the receiver (the noise problem in the front-ends is usually more of an issue). Furthermore, active filters consume power which is at a premium in portable applications.

Active filters usually yield very predictable results, with measured filter characteristics very close to design/simulation. The effect of finite Q elements is typically of no consequence in these filters (unlike passive LC filters).

Commercially available active filters are not sufficiently broadband for any application in this system. Furthermore the frequency response of commercially available opamps limits the use of custom active filters to the ADC anti-aliasing section of the receiver. Custom active filters were not utilized in that section, however, due to the availability of relatively compact high-order hybrid LC filters for the frequency bandwidth of interest. The use of such passive filters in the present form of this system reduces the power consumption, distortion, and noise of the system with almost no board area penalty. Active filters would have been an attractive alternative, however, in a more integrated implementation of such a receiver where the anti-aliasing filter could have been integrated on chip along with the demodulator or the ADC's. Such a scheme would have saved a significant amount of board area while avoiding the necessity for driving low termination impedance off-chip passive filters.

5.7.2.4 Ceramic (dielectric-resonator) filters[1]

5.7.2.4.A Bandpass Filters vs. HP-LP filters

The frequency response of a typical Butterworth bandpass six pole (three pole equivalent LPF) ceramic filter is shown in FIGURE 44.a. This filter was used as our front-end "preselect" filter with f_c = 888 MHz, and BW_{3dB} = 32 MHz. This filter achieves 30 dB of attenuation at 50 MHz from center. At first glance this result may be surprising since 938 MHz is only 34 MHz away from the upper 3 dB frequency and 938 MHz / 904 MHz is

1. These filters are quite different from the "bulk resonator" ceramic filters which are typically used at the IF stage of AM radios (455 KHz).

much less than an octave, and such "steep" attenuation may require a filter with many more number of poles. This is not the case however, and the above transfer function completely agrees with the theoretical expectations *if* the location of the poles is considered in the *equivalent* LPF (FIGURE 44.b), which is the basis of the LPF to BPF translation. The reason for this lays in the fact that in the BPF we are not dealing with simple real poles. The poles are now high-Q complex conjugate poles, which can offer a much steeper response than an equivalent low-pass--high-pass filter.

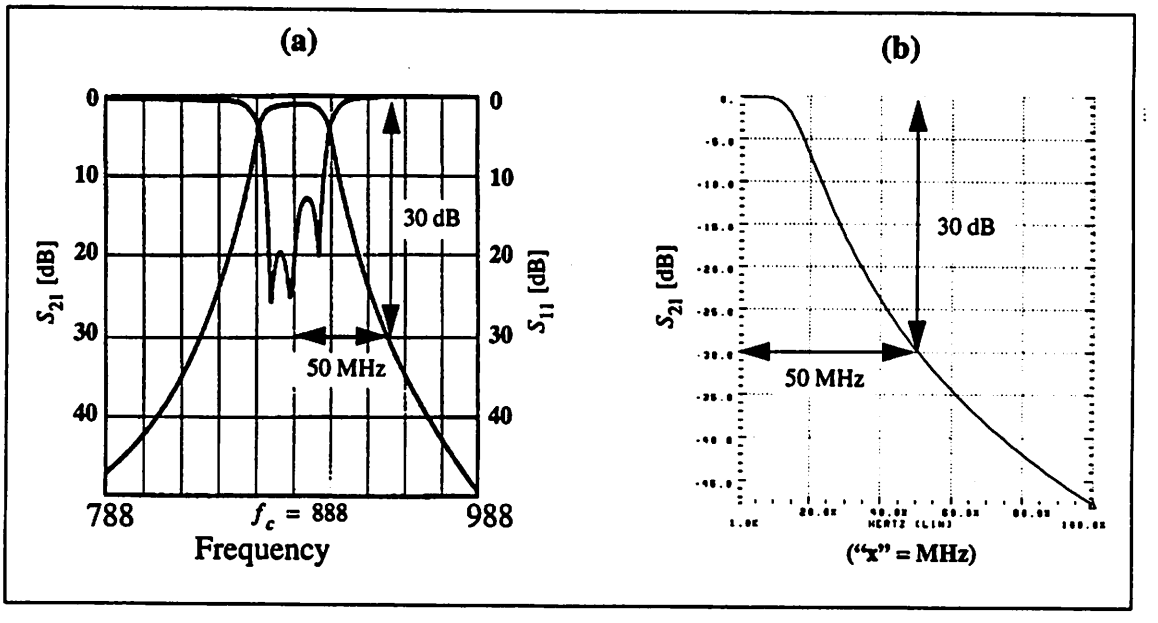


FIGURE 44. (a) The frequency response of the Ceramic bandpass filter used in this system (b) The simulated low-pass equivalent of the BPF (three pole Butterworth). Note that the attenuation at a certain *offset* frequency is approximately equal in both filters.

The frequency response of an ideal high-pass--low-pass filter with a high-pass cutoff frequency of 872 MHz and a low-pass cutoff frequency of 904 MHz is compared to that of a true bandpass filter in FIGURE 45.a. Although the ultimate rejection of both filters is equal at an infinitely large offset frequency from the center frequency, the "near-in" rejection of the two filters are dramatically different. For most applications, such a LP-HP filter would be effectively useless. In addition to an extremely poor rejection, the ideal LP-HP filter in this case suffers from significant pass-band attenuation due to the droop introduced in the pass-band response by the proximity (nearness) of the LP and HP cutoff frequencies (the high Q nature of the filter). The simulation results shown in FIGURE 45.a are obtained from behavioral SPICE models using the POLE and LAPLACE analyses in HSPICE.

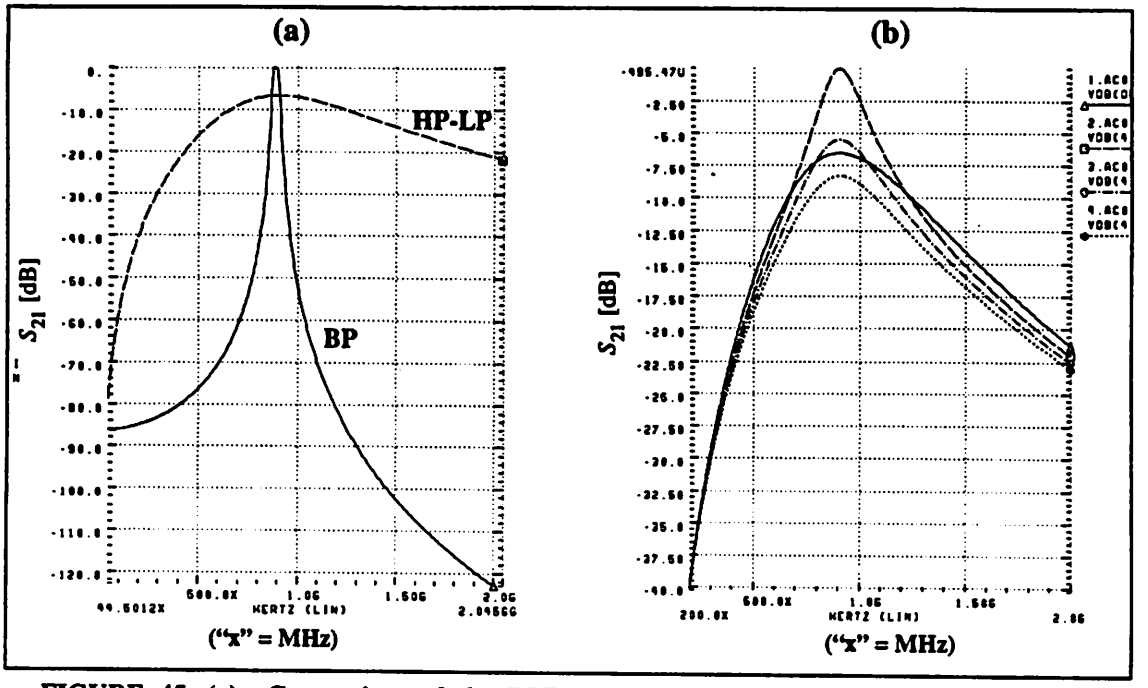


FIGURE 45. (a) Comparison of the BPF response with an ideal HP-LP response. (b) Comparison of an ideal HP-LP response (*1.AC0*) to a cascaded HP-LP response (*2.AC0*), a cascaded HP-LP response with a 3 dB interestage resistive pad (*3.AC0*) and a cascaded HP-LP response with a 6dB interstage resistive pad (*4.AC0*).

In addition to suffering from a poor rejection and significant in-band attenuation due to the droop, the realistic (non-ideal) HP-LP section suffers from a significant amount of interaction between the HP and LP sections of the filter. This problem is much more severe in high-Q filters such as the one being discussed here, and as shown in FIGURE 45.b (curve *2.AC0* is the non-ideal case and curve *1.AC0* is the ideal case) can introduce significant peaking in the passband response and also increase the group-delay variation of the filter in the passband. This problem can be alleviated by isolating the LP section from the HP section of the filter. One method is the use of resistive attenuators (pads) in the form of a PI section or a T-section (See section 7.6.3, "Resistive Networks"). The use of a 3-dB pad results in the *3.ac0* curve in FIGURE 45.b and the use of a 6-dB pad results in the *4.ac0* curve in FIGURE 45.b. Clearly the isolation is achieved at the expense of additional passband loss in the filter which is not acceptable for front-end filters. An alternative solution for the isolation problem in lower frequency HP-LP filters is the use of a buffer amplifier between the two stages of the filter.

The clear disadvantage of a LP-HP solution in this case arises from the high-Q requirement of the BPF. When the Q retirements of the BPF is not as severe, a HP-LP filter may be superior to a true BPF. This is because a HP-LP filter is much easier to tune, does not require as high of a Q for the components, and is less sensitive to component value tolerances.

The pole locations in the s-plane of the filters discussed here are shown in FIGURE 46. The poles of the BPF, its equivalent LPF, the low-pass section of the HP-LP filter, and the high-pass section of the HP-LP filter are indicated by ■, ❑, ○, and ✘ respectively on this

figure. The high-Q nature of the BPF as compared to the LP-HP section is clear. The low-pass to band-pass transformation has also been indicated in the figure by the arrows.

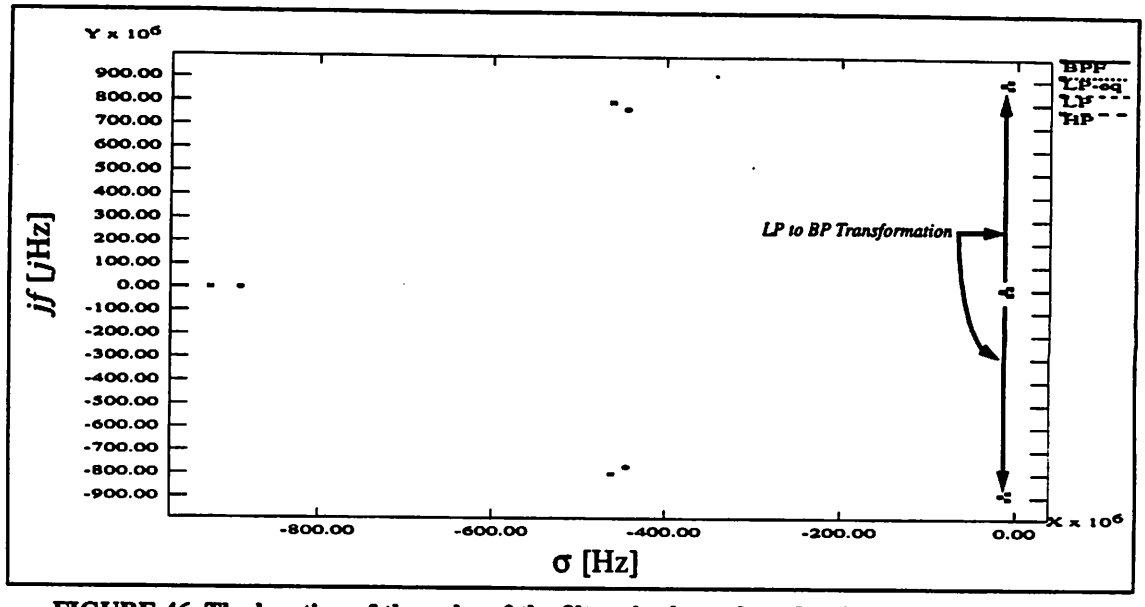


FIGURE 46. The location of the poles of the filters in the *s*-plane for the BPF of FIGURE 44.a, the equivalent LPF of FIGURE 44.b, and the LP-HP filter of FIGURE 45.a.

5.7.2.4.B Component Q Requirements for BPF's

The *minimum* component Q for a third-order Butterworth LPF is approximately equal to 3 [37]. The minimum Q required for the equivalent BPF constructed by transforming the LPF, however, is approximately Q_{filter} times higher. In this case, for example, the minimum Q required is approximately 83. Such high Q inductors are difficult to obtain at the 900 MHz band of interest. Other means are therefore used to construct such filters.

5.7.2.4.C Ceramic Filters

There is not much available on ceramic filters in the literature. There are a relatively few companies manufacturing these filters and for the most part they hold most of the patents on these filters. In general in these filters, the frequency response is shaped by the resonance of the dielectric resonator, typically at the quarter wavelength of the propagating signal in the dielectric. The quarter wave length, is therefore what dictates the physical size of the filter. At the lower frequencies, these filters become prohibitively large, whereas the tolerances achievable in the manufacturing process determine the highest frequency of which ceramic filters can be used at. At the higher frequencies, when using a quarter wavelength becomes prohibitively small, half wavelength sections are typically used.

Ceramic filters offer a very low insertion loss and are therefore commonly utilized as the front-end filters in a system. This is because the insertion loss of a filter prior to a gain stage adds directly to the overall NF of the system (in dB).

Ceramic filters are based on multi-section coaxial ceramic resonators. In order to understand the operation of ceramic filters, a brief description of the theory of operation of coaxial ceramic-based resonators is presented below.

5.7.2.4.D Coaxial Resonators

Coaxial resonators typically offer long-term stability (negligible aging effects), very high dielectric constants (between 30 to 100, which reduces the size of the circuitry) and low loss (which reduces the system noise figure). They are typically used as a parallel resonant structure with very high Q (200 to 1000, typical), or as very high quality inductors.

The frequency range of operation of coaxial resonators is between 300MHz to about 5GHz. In general higher profile coaxial resonators offer higher Q values (at the expense of size). The cutoff frequency for the high profile ceramic resonators is generally lower than the low profile ceramic resonators. When the profile dimension of the ceramic TEM mode resonator becomes comparable to the wavelength, higher order modes are excited. This affects the device operation and should be avoided. Since the cutoff frequency is determined by when the profile dimensions (physical dimension) become comparable to the wavelength (electrical dimension), higher dielectric constants reduce the cutoff frequency of the ceramic resonator. The actual operating frequency of the ceramic resonator is determined by the length of the coaxial resonator element for a given profile and a given type ($\lambda/2$ or $\lambda/4$).

Coaxial components can also be used as high quality inductors. Structurally, coaxial inductors are similar to coaxial resonators, except they are specified with a precise value of inductance, and a specified self resonant frequency. For example, a $3.0\text{nH} \pm 5\,\%$ can easily be obtained with a Q of 400 and a SRF of 2GHz, using a 0.5cm long coaxial element [17]. In order to avoid SRF effects, these inductors are typically operated at a maximum frequency of about 2/3 of the SRF.

In order to utilize the coaxial resonator in a $\lambda/4$ mode, the coaxial resonator is short circuited at the load. It is clear from FIGURE 47.a that in this mode, at the odd multiples of $\lambda/4$ the transmission line behaves similar to a parallel resonant circuit. Furthermore, the coaxial element may be used as an inductor if the length of the section is less than $\lambda/4$. In order to use the coaxial segment as a half wave length parallel resonant element, the end of the segment is left as an open, resulting in an impedance versus wavelength curve shown in FIGURE 47.b. In this case, segments smaller than $\lambda/4$ can be used as high quality capacitors, and segments with $\lambda/4 < l < \lambda/2$ can be used as high quality inductors.

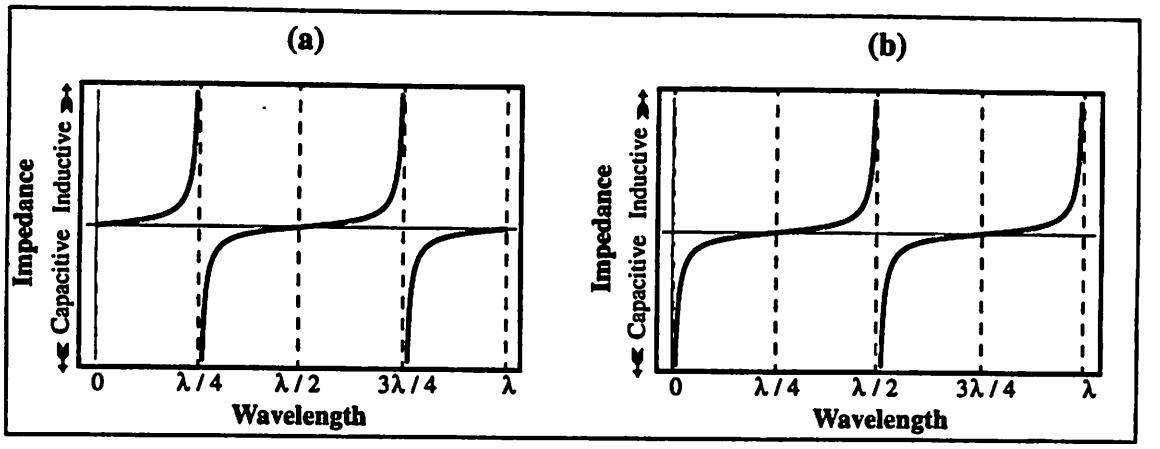


FIGURE 47. The impedance of a coaxial resonator as a function of its length for (a) a short circuited stub and (b) an open-circuited stub.

5.7.2.5 SAW filters (transversal)

In a surface acoustic wave (SAW) filter, the input electromagnetic signal is transformed into a SAW signal[1], which is then (frequency domain amplitude) shaped, and subsequently converted back into an electromagnetic signal (FIGURE 48). The principal of operation of a SAW filter (except for resonator type SAW's) is much like a digital FIR filter; the SAW transducer finger lengths are based on the taps of the desired impulse response for the filter. An overall desired frequency response is obtained by designing a two stage cascaded FIR system, one for the input transducer, and another for the output transducer. The impulse response of these two sections is then etched on the surface of a piezoelectric substrate such as quartz. The choice of the dielectric is primarily a function of the fractional bandwidth required. The input RF signal causes the surface of the crystal to expand and contract appropriately.

5.7.2.5.A High Insertion Loss in SAW Filters

Since an ideal SAW transducer is a *bidirectional* radiator, 3dB of the input signal power is lost in the input transducer as the RF signal is transformed into an acoustic signal. Similarly, another 3dB of signal is lost in the conversion from acoustic signal to the electromagnetic signal. Therefore, the minimum insertion loss of a traditional transversal SAW filter is 6dB. Issues such as coupling efficiency, mismatches, and resistive losses increase this insertion loss to 15 to 35dB.

As the fractional bandwidth of a SAW filter is increased for a given substrate, the number of inter-digitated electrodes on the surface of the substrate decreases, resulting in a degradation of the coupling efficiency, and hence an increase in the insertion loss (note that this is typically opposite to that obtained for LC filters, where a narrower bandwidth filter would require a high number of sections, and therefore have a higher insertion loss). In order to keep the insertion loss due to coupling inefficiencies to a minimum, substrates with better coupling coefficients must be used. The SAW filter used in this system has a

1. SAW waves discussed here are similar to the kind of waves generated by earth quakes.

128° Lithium Niobate substrate with a very high coupling efficiency as required for such a filter (45% fractional bandwidth at 70MHz). The better coupling coefficient is at times in conflict with the drift performance of the filter.

5.7.2.5.B Triple Transit in SAW Filters

A lower insertion loss for the traditional transversal SAW filter is not necessarily desirable. This is due to the so-called "triple transit" effect. Part of the signal that is radiated to the output transducer is reflected back as shown in FIGURE 48. This signal is again radiated by the input transducer and appears at the output terminal three time constants after the original signal had arrived at the input transducer. This is shown in the impulse response of FIGURE 49.a for the SAW filter used in this system. This triple transit signal is attenuated by twice the insertion loss of the signal as compared to the fundamental signal arriving at the output since it travels the path twice more than the fundamental. Any reduction in the insertion loss of the signal would cause a stronger triple transit signal.

In the frequency domain, the triple transit introduces both amplitude and phase ripple in the response.

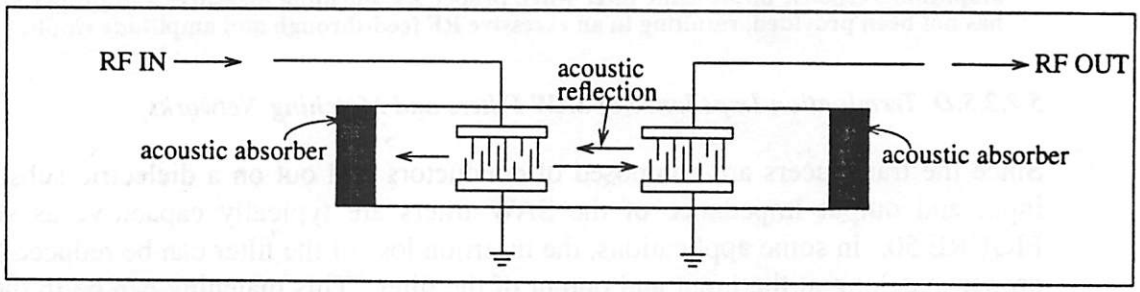


FIGURE 48. Basic structure of a transversal SAW filter.

5.7.2.5.C RF Feed-through in SAW Filters

Ripple can also be observed in the frequency response of a transversal SAW filter due to "RF feed-through." The effect of RF feed-through could be seen in an impulse response at a delay of 0 seconds as compared to the propagation delay time of the acoustic wave (this is not shown in FIGURE 49.a since the time scale starts at 1 μ s). In the case of improper SAW filter layout on the PC board (e.g. capacitive/inductive coupling paths between the input and output of the filter, or improper grounding), the RF signal can quickly travel through and arrive at the output long before the intended filtered signal. In addition to causing ripple in the frequency response of the filter, RF feed-through reduces the selectivity of the filter.

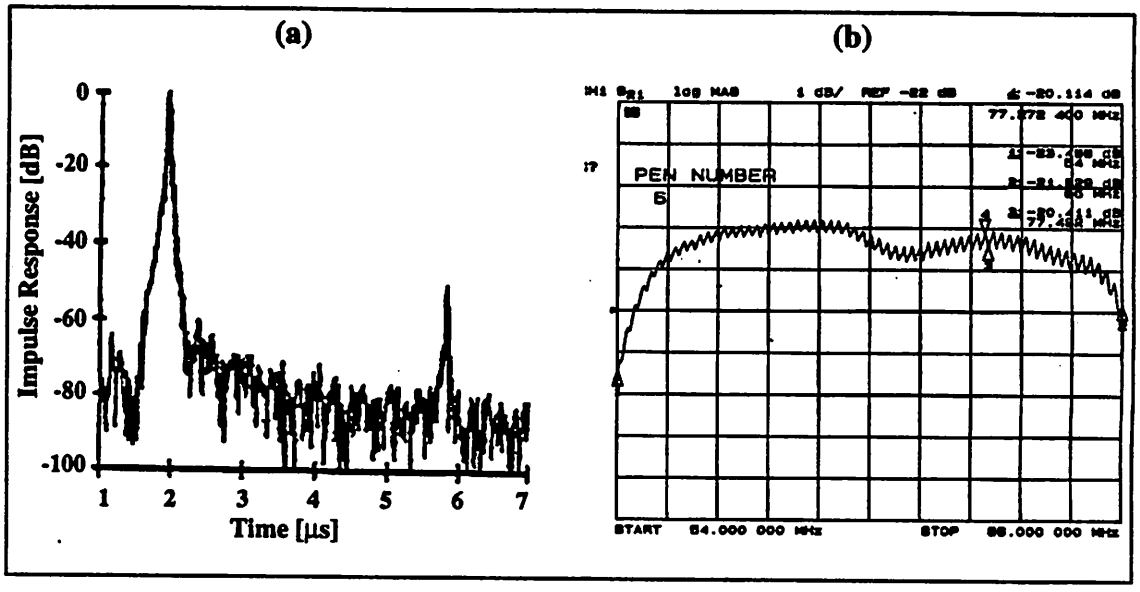


FIGURE 49. (a) The impulse response of the SAW filter used in this system displaying the triple transit spur attenuated by about 52dB. RF feed-through is not shown in this figure. (b) The amplitude response of the same filter when proper RF shielding measures and proper grounding has not been provided, resulting in an excessive RF feed-through and amplitude ripple.

5.7.2.5.D Termination Impedance of SAW Filters and Matching Networks

Since the transducers are composed of conductors laid out on a dielectric substrate, the input and output impedance of the SAW filters are typically capacitive as shown in FIGURE 50. In some applications, the insertion loss of the filter can be reduced by using proper matching at the input and output of the filter. This matching can be in the form a simple inductive matching, or an LC section. Although matching can reduce the insertion loss of the filter, one needs to be aware of its consequences. As explained above, a reduced insertion loss results in a larger triple transit effect and hence degraded amplitude and phase response. Furthermore, for broadband applications, a simple high Q matching network would introduce peaking in the resultant amplitude response of the filter. Finally, one needs to be aware of the potential coupling of the matching elements at the input and the output which could introduce RF feed-through problems.

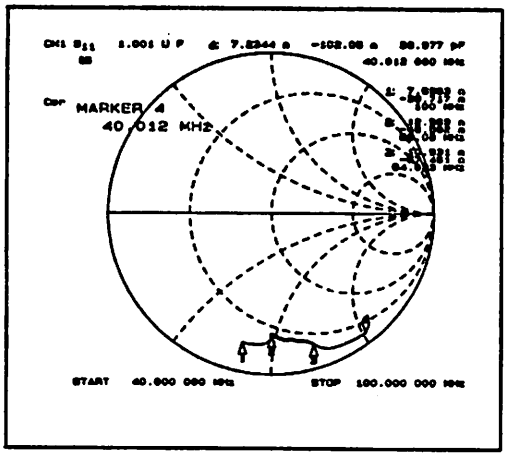


FIGURE 50. The capacitive input impedance of the SAW filter used in this system.

In this system, transformers are used to match the high input and output resistance of the VGA to the low input and output impedance of the SAW filter, for the proper functionality of the SAW (See section 7.8.3, "VGA1-SAW-VGA2 Interface (Sensitivity of SAW Filters to Terminal Impedance Mismatches)"). No attempt has been made to tune out the input and output capacitance of the SAW filter in order to reduce its insertion loss (because of the reasons explained above). A complete analysis of the effects of impedance matching on SAW filters is relatively complicated and requires CAD packages.

5.7.2.5.E Physical Size of SAW Filters

The propagation speed of an acoustic signal is typically about 100,000 times slower than the propagation of an electromagnetic signal. Therefore, as far as the physical dimensions are concerned, relatively low frequency SAW filters are practical to implement (their size is not too large). For example at 70MHz, a quarter wave length section implemented on FR4 would have a length of approximately 0.5m, whereas the corresponding acoustic wavelength would be 11μm in length. On the other hand, this limits the use of transversal SAW filters at the higher frequencies; they are too small to manufacture reliably. With the advent of better SAW processing techniques, currently 1GHz SAW filters are available which consume a fraction of the area of their ceramic counterparts at the expense of a higher insertion loss.

5.7.2.5.F Phase Response of SAW Filters

Due to their FIR-like characteristics, transversal SAW filters inherently present a linear phase response, and the traditional trade-off between the amplitude and phase response does not exist. Furthermore, the phase response and amplitude response can be independently designed for applications that require delay equalization. Similar to an FIR filter, a steeper amplitude response would require a higher number of taps. In a SAW filter with a given substrate, this results in a physically longer SAW filter.

5.7.2.5.G Amplitude Response of SAW Filters

The ultimate close-in rejection of a SAW filter is typically very high (> 50dB) if proper layout guidelines are followed. Frequently however, a region of the spectrum centered at

the *n*th harmonic of the center frequency of the SAW, with a bandwidth of approximately *n* times the bandwidth of the SAW exists where the input signal is only attenuated by about 10 to 20dB (FIGURE 51.b). This is effectively a second passband for the SAW and is a result of the "dispersive" design of such filters. The constant *n* is typically equal to the number of fingers in the SAW design minus one. In the case of the SAW filter used in this system, the filter is composed of four fingers (per side) and $n = 3$.

5.7.2.5.H Impedance Matching for SAWs

The effect of the undesired pass-band can be reduced by using proper input and output matching networks for narrow-band applications. For broad-band applications, however, external tuning is usually not an option as explained in Section 7.8.3, "VGA1-SAW-VGA2 Interface (Sensitivity of SAW Filters to Terminal Impedance Mismatches)". In many systems, however, (e.g. this system) the existence of a second passband is not of consequence as other filters in the system, as well as the natural roll-off frequencies of the active components reject this band.

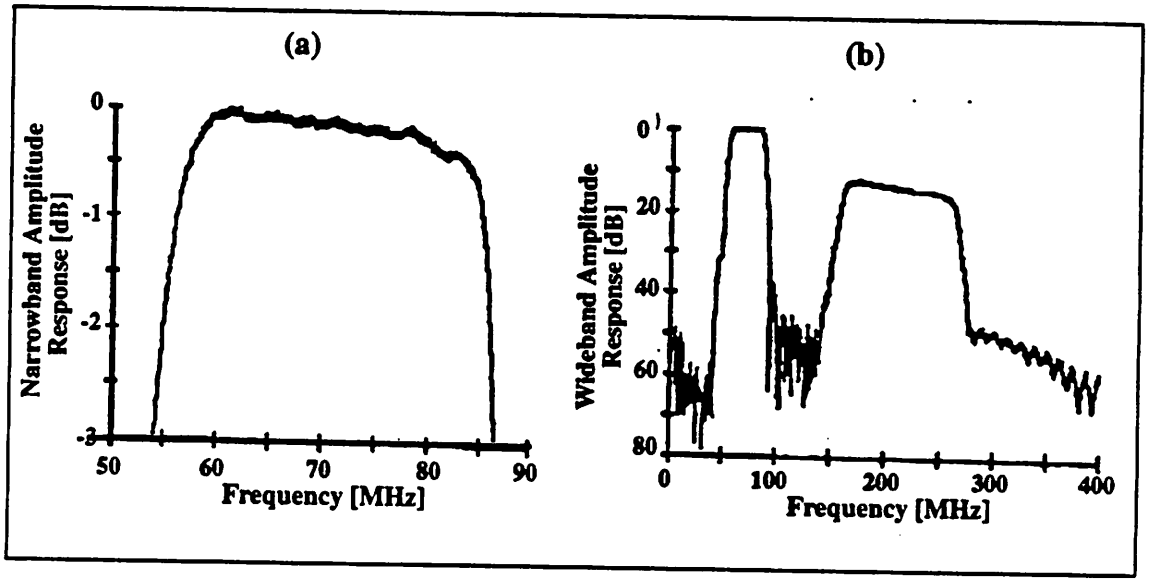


FIGURE 51. (a) The near-in amplitude response of the SAW (b) The amplitude response of the SAW in a broad bandwidth. Both figures are normalized and do not display the filter insertion loss.

5.7.2.5.I The Phase Response of the SAW Filter

The phase response of a transversal SAW filter is very linear (FIGURE 52.a) and often much better than that achieved with LC filters. The group delay response (FIGURE 52.b), however, displays a significant amount of ripple. This is because group delay is the derivative of the phase response with respect to frequency, and the phase response displays rapid but small perturbations as a function of frequency due to time spurious signals (RF feed-through, triple transit, etc.). These rapid variations are usually of no consequence in the system. It is important, however, to maximize the attenuation of time spurious signals by proper layout in order to keep the group delay variation to a minimum.

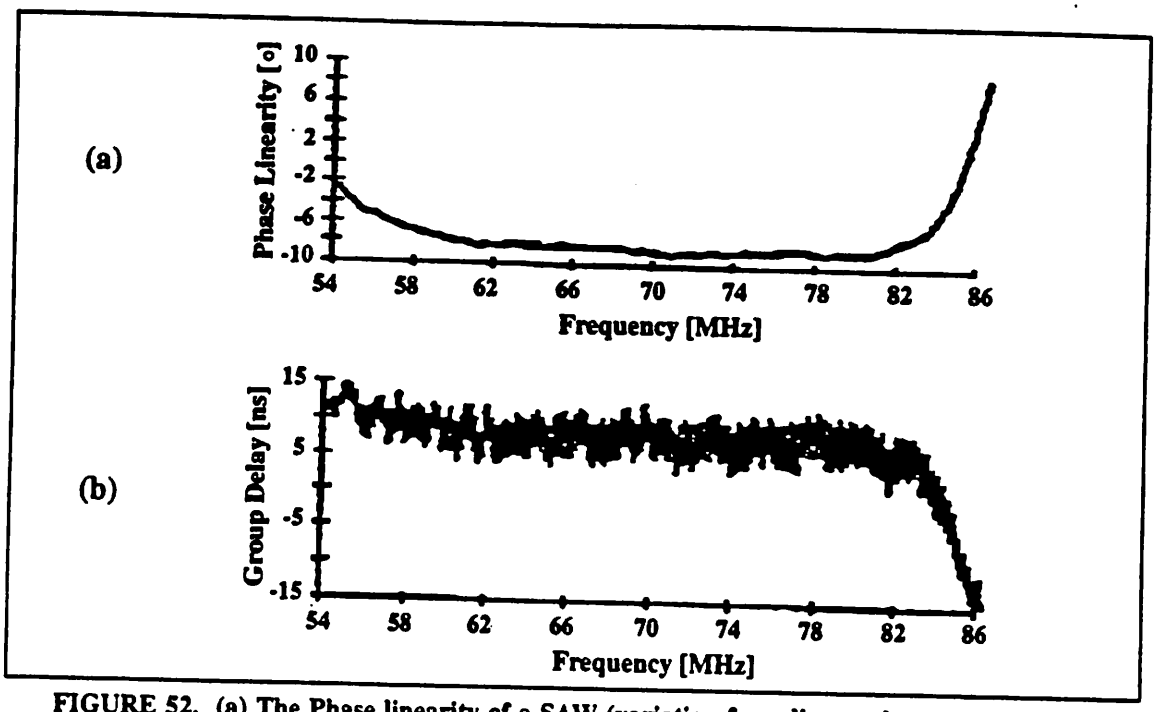


FIGURE 52. (a) The Phase linearity of a SAW (variation from linear phase response) (b) The group delay of the SAW.

5.7.2.5.J Low-Loss SAW Filters and Resonator SAW Filters

The discussions regarding SAW filters presented here pertain to transversal SAW filters, such as the one used in this system. Two other major family of SAW filters exist, the "low-loss" SAW filters and the resonator SAW filters. Low-loss SAW filters do not show the trade-off between insertion loss and triple transit as stated above, but cannot be realized for fractional bandwidths of more than 10%. Impedance matching therefore can be very effectively used for such filters to tune out the input and output capacitance of the low-loss SAW filter, as it will not increase the triple transit problem, nor will it cause significant peaking in the response (since it is a low-fractional bandwidth filter).

Resonator SAW filters, are significantly different than the transversal SAW filters. They behave more like LC filters and show the characteristic phase and amplitude trade-offs observed in LC filters. Furthermore, they can have fractional bandwidths of a maximum of 1%. Resonator SAW filters, similar to transversal SAW filters, can be manufactured for operation in frequencies as high as 3GHz.

5.7.3 Filters for Wideband Applications: A Summary

Table 4 summarizes the qualitative characteristics of the filters discussed above as used in wideband applications.

	Custom LC	Commercial LC	Active Analog	Transversal SAW	Ceramic
f_c Range[a]	RF	BB[b] IF RF	BB	IF RF	RF
BW	--	>80% f_c	Small	>50% f_c	>15% f_c
Loss	Low	Low	--	High Low	Low
Size	Small	Lg Lg Sml	Medium	Large Small	Small
Matching	Critical	Critical	Not Critical	Very Critical	Critical
Special Issues	Tolerance, Q, SRF, EMI	Limited Selection, EMI	Power, Noise, Disto	FIR, Layout	Nice for front-end

a. Center frequency range

b. Baseband

TABLE 4. Qualitative summary of some available filters for wideband applications.

5.7.4 Filter Selection, Placement and Purpose in This System

5.7.4.1 Out-of-Band Protection and Image Rejection

In the system diagram, FIGURE 10, the "pre-select" filter BPF1 serves several functions. In the receiver mode, it ensures that the front-end LNA and mixer do not saturate due to strong out-of-band signals. Furthermore, it serves as the first anti-image filter in the system. However, since there is no gain prior to this stage, its insertion loss adds directly to the overall NF of the system (in dB). In the presence of BPF2 for image-rejection purposes along with some frequency selectivity in the antenna, it may be possible to eliminate this filter in the receiver path, to obtain a much better NF (about 2dB better). This could be done only in a controlled environment and the resulting receiver would be very much prone to the saturation of the front-end in other environments.

The LNA used in this system, the NE600, is a true wideband amplifier with a frequency response from near DC to about 1GHz (as a matter of fact, the low frequency gain of this amplifier is much larger than its gain at the 900 MHz band). If it were a tuned amplifier, the system designer would have been more likely to be able to eliminate BPF1 in the receiver chain. But even in this case, the operational environment would have had to be carefully studied. Unfortunately, implementing tuned amplifiers in Si monolithic technology is currently difficult because of the lack of high-Q on chip inductors. Tuned amplifiers are commonly used, however, in discrete designs as well as GaAs MMIC's. In summary, BPF1 has been selected to be a coaxial resonator ceramic filter in order to mini-

mize system NF. In the transmit path, this filter acts as the main bandlimiting filter for regulatory purposes.

BPF2 is the main image and image noise rejection filter in the system prior to the RF mixing stage. BPF2 is also a ceramic filter with a low loss (2 dB). Relatively low-loss (5 dB) SAW filters could have been used at this stage with a slight penalty in system NF, but a significant saving in board area. A SAW filter was not used at this stage due to the lack of the commercial availability of such filters for the band of interest at the time of the system design.

A simple LC filter has been provided between the output of the RF mixer and the input of the IF VGA. This filter along with the natural roll-off of the VGA eliminates the possibility of the saturation of the VGA due to strong out-of-band signals. This filter is not shown in the block diagram of FIGURE 10.

5.7.4.2 Noise Limiting

BPF3 is selected as a transversal SAW filter with very high selectivity and very good phase response. This filter is the main noise suppression filter in this system. Due to a significant amount of gain prior to the SAW filter, its high loss can be tolerated.

The alternative filter for this stage is an LC filter. For the same rejection, the size of the commercially available LC bandpass filters are significantly larger than the SAW filter. If a good phase response is also required from the LC filter, phase equalization circuitry can be used, adding to the size and cost of the LC filter.

BPF3 has been placed in between the two stages of the VGA. Placement of the filter prior to this stage (closer to the front-end) would have caused a significant increase in the system NF.

The output of the IF VGA and the demodulator IC are in a differential form. Any radiative or conductive noise pickup at the interconnects, therefore, is common mode and will be rejected by the CMRR of the demodulator. No filtering has been provided at this point.

5.7.4.3 Anti Aliasing

LPF1 and LPF2 are the anti-aliasing filters priors to the ADC's in this system. They are hybrid LC filters and possess a good amplitude response at a relatively small size. Sockets have been provided for these filters on the PCB so that a variety of LPF's can be used for different bandwidth communications.

5.7.4.4 Pulse Shaping, Saturation Protection and Band Limiting in the Transmitter

LPF3 and LPF4 are custom elliptic LPF's which prevent the premature overloading of the *I* and *Q* buffer amplifiers due to strong out-of-band harmonics of the incoming signals. In cases where digital pulse shaping (raised cosine or root raised cosine) and DACs are utilized in the transmitter, noise and out of band signal limiting would be the primarily role of these filters. When digital pulse shaping and DACs are not used and the digital signal is

directly fed into the input of this system, these filters also act to shape the pulses. Clearly such a (RLC) pulse shaping as compared to an optimum Nyquist pulse shaping is poor and reduces the "eye-opening" in the received and demodulated signals.

LPF3 and LPF4 also aid BPF1 in band-limiting the signal prior to transmission.

5.8 Local Oscillators

5.8.1 Microstrip vs. Coaxial Resonator Oscillators

This transceiver utilizes three local oscillators; two in the form of a voltage controlled local oscillators (VCO), and one in the form of a third overtone fixed oscillator. The VCO's used in this system were in the form of an encapsulated module and came in a surface mount package. They utilized a microstrip resonator as the resonance element. In general microstrip based resonators offer a smaller size and lower power consumption than their coaxial resonator based counterparts at the expense of a lower Q and higher oscillator phase noise.

The VCO modules used in this system were based on a Colpitt structure, with a varactor based tuning element.

5.8.2 Output Power vs. Supply Voltage

The VCO's used were specified to operate at $4.2\text{V} \pm 0.25\text{V}$. A nominal 4.2V supply generated an output power of 0 dBm. In the case of both the transmitter and the receiver this was a desirable output level, and hence this VCO was operated at the 4.2V specified (the supply for these VCO's is fed from an adjustable low-dropout voltage regulator and can be adjusted to provide any other desired supply voltage). It is empirically found that the noise performance of the oscillator was not significantly affected by increasing the supply voltage over 3.6V. Although this was experimentally verified for the specific VCO's used in this system, many Colpitt based VCO's behave similarly. A certain minimum supply voltage is required to satisfy the necessary conditions for oscillation (loop gain > 1 and 180° phase inversion). The oscillator noise will reduce for higher supply voltages to a certain amount, but after that limit is obtained, an increase in the supply voltage does not significantly reduce the noise of the oscillator, but the output power of the oscillator will continue to change. In our case a supply voltage in the range of $3.6\text{V} < V_{sup} < 5.0\text{V}$ corresponded to an output power level of $-3\text{ dBm} < P_{out} < 2\text{ dBm}$. Therefore, the output power level can be simply adjusted by operating the VCO at different supply levels through the adjustable voltage regulators.

5.8.3 VCO Sensitivity to Control Voltage

Many VCO's used in wireless applications have a relatively wide tuning range. For example the receiver VCO used in this system had a tuning range of $952\text{ MHz} < f_c < 977\text{ MHz}$ corresponding to a control voltage ranging from $1\text{V} < V_c < 4\text{V}$. This translates into

an oscillator gain (sensitivity) of 8.3 MHz / V or 8.3 KHz / mV. This means that the control voltage must be extremely clean to minimize noise. In the case of a phase locked VCO, this criteria is much easier to achieve, since the "near" phase noise is dictated by the fixed reference oscillator which typically has a very good noise performance. Furthermore, any low frequency noise within the bandwidth of the LPF used as the loop filter will be significantly corrected for by the loop. In the case of a free-running VCO, however it is in general more difficult to supply a very clean control line, since the control voltage is supplied by an open loop system with no feedback to adjust for small control voltage variations (over time, temperature, etc.). In many applications it is desirable to reduce this high sensitivity to the control voltage by reducing the gain of the VCO and making up for the reduced range by using a larger tuning voltage range. Clearly supplying such high voltage ranges in portable wireless applications is unpractical and would require the use of step-up dc-dc converters. In other applications such as broadband TV tuner systems which may be required to tune from about 50MHz to 1GHz, the front-end VCO has to be able to tune over an octave (from f_{IF1} + 50 MHz to f_{IF1} + 1 GHz). In many cases the first IF frequency is at about 1.1 GHz (the high side IF frequency is selected to reduce the broadband image problem; See section 5.1.4, "Up-Converting IF vs. Down-Converting IF"). Even with a large tuning voltage range the sensitivity of the oscillator is relatively high.

5.8.3.1 Effect of Voltage Regulation and Filtering of the VCO Control Line on Noise

In various experiments with free running VCO's it was found that the following causes can contribute significantly to the noise performance of the VCO.

- Unregulated control signal. If the control voltage is supplied from a common supply with many other circuitry, particularly high current consumption switching circuitry, the noise of the oscillator will be effected. Fast switching control voltage fluctuations can be significantly filtered by a LPF but are not affected by the linear voltage regulator as the regulation of linear regulators drops very rapidly with increasing frequency. For example, the linear voltage regulator used in this system (LP2951) offers over 80 dB of rejection for ripple frequencies of below 1 KHz, but only 30 dB of rejection at 10 KHz for a 10 mA load. Clearly, regulating the power supply does help the rejection of low-frequency noise.
- Unfiltered control signal. This element is probably the most deteriorating element affecting the noise of a free-running oscillator. A simple low pass filter can significantly improve the noise of the VCO (FIGURE 54). In our case, since the control signal fed directly into a varactor and there was no DC current consumption on the control signal, a high valued resistor was used to achieve a low-pass cutoff frequency (FIGURE 53). If there were a DC power consumption, the maximum value of this resistor would have been set by the maximum voltage drop allowable across it. In an ideal case, to achieve a certain low-pass cutoff frequency, it is desirable to increase the value of the capacitors as opposed to the value of the resistor. This is because for high-valued resistors, the noise of the resistive element may itself cause added noise in the output signal, whereas by using larger valued capacitors and smaller resistors, the KT / C noise will be reduced. In the real case, however, large value capacitors typically are physically large. Furthermore, they have a relatively low self resonant

frequency and will therefore not be able to provide effective filtering at the higher frequencies. Some times parallel capacitors are used to accomplish this task (See section 5.7.2.1.D, "Physical Capacitors").

As an example, in the simple LPF used in this system (FIGURE 53), the noise bandwidth is $1.57 / (2\pi RC)$ which is equal to 0.34 Hz. The rms noise voltage in this bandwidth due to the thermal noise of the resistor is 23.7 nV rms. This amount of noise on the control signal of the VCO used in the receiver of this system (8.3 MHz / V) will introduce a 0.2 Hz variation which is clearly negligible.

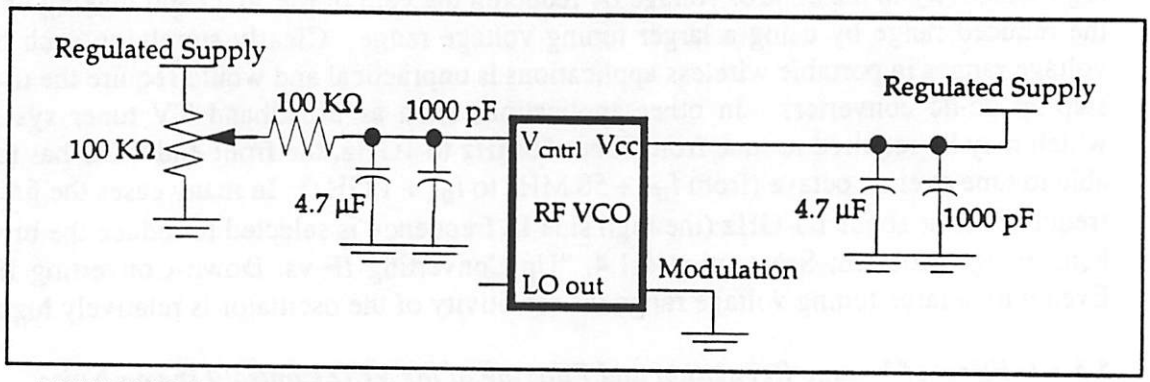


FIGURE 53. Low noise operation for free-running VCO.

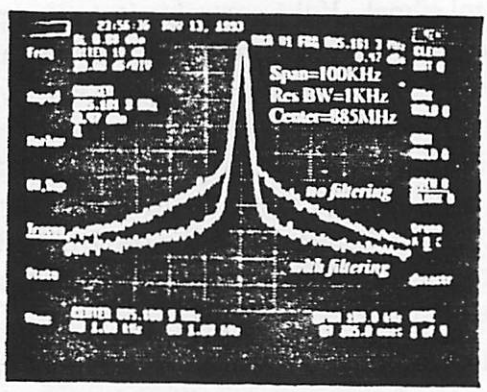


FIGURE 54. The effect of unfiltered control signal on a free-running VCO output.

It is important to note that using a bypass capacitor alone at the control signal input to the VCO does not provide a good enough bypassing and filtering. This is because the power supply is effectively in parallel with the control voltage line and the resistance seen by the capacitor is small and therefore the low pass cutoff frequency is not sufficiently low. In our case, even a 1000 µF bypass capacitor could not provide nearly enough bypassing. In a sense, a finite source resistance is useful in this case. Furthermore, the bypassing here is different from a supply bypassing scheme in that in a supply bypassing scheme often LC networks are used for bypassing (the L is in the form of a regular inductor or a ferrite bead), where as here an RC bypass serves better. This is because while the LC filter

slushes the high frequency noise back and forth, the RC filter dissipates it and turns it into heat. RC filters are impractical in supply bypassing because of the finite current consumption of the line and the resulting DC voltage drop across the resistor.

5.8.3.2 The Determination of the LP Cutoff Frequency for the Control Line Filter

In general the low pass cutoff frequency is determined by the required tuning speed of the oscillator. In variable frequency systems where the oscillator has to tune to different frequencies, usually a free-running VCO is not used. If a free-running VCO were to be used in such a system, however, the low pass cutoff frequency would have to be large enough to allow for the control signal to settle to the proper value in the specified amount of time.

5.8.3.3 Effect of Shielding on VCO Noise

Another factor affecting the phase noise performance and in general the cleanliness of the output signal is the proper shielding of the oscillator and its driving circuitry. In general local oscillators, particularly at the higher frequencies radiate a significant amount of energy which could affect the performance of the other parts of the system. At the same time the radiation of other elements in the circuit can significantly affect the output spectrum of a VCO. In particular, two adjacent VCO's which are not properly shielded can cause the "pulling" of one another. Even when the VCO's are used in a phase lock loop configuration, the pulling effect can pull the locked VCO out of lock and cause major system problems. Even other equipment in the vicinity such as computers can significantly modify the output spectrum of a VCO. For example it was observed that a computer located at about 2 meters away could cause modulation sidebands on the output spectrum similar to sidebands generated by a BPSK modulating signal.

5.8.3.4 Effect of Ground Loops on VCO Output

The added noise introduced by connecting the common port of the power supply used as the control signal to the power supply's ground connection is shown in FIGURE 55.a and the output of the VCO when this connection is removed is shown in FIGURE 55.b. No significant filtering of the control signal was provided in this case. When the common ground connection is removed on the power supply, the low frequency noise is significantly reduced. This is probably an artifact of the measurement mechanism. When the ground is connected to the common on the power supply, two return paths exist for the signals to ground: one through the power supply ground, and another through the spectrum analyzer probe. This causes a ground loop which significantly degrades the noise performance of the VCO. When the ground to common connection is removed on the power supply, a single point of return exists for the probing signal, which removes the ground loop problem. Obviously, when the signal is not being probed through a spectrum analyzer, the ground loop problem does not exist.

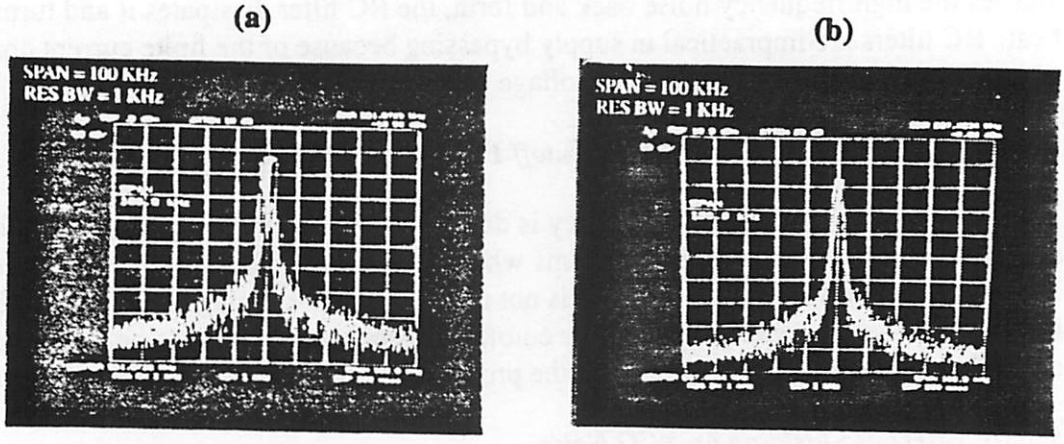


FIGURE 55. (a) The effect of a ground loop on the VCO output. (b) Output of the same VCO with the ground loop removed.

5.8.4 Effect of Power Supply Cleanliness on the VCO Output

In another test with a single 900 MHz free-running oscillator it was observed that the signal was being modulated (FIGURE 56). After extensive investigation and isolating all possible sources of the problem, the issue was attributed to the power supply used as the control element. Despite the fact this power supply was designated as a lab power supply, it induced a very small magnitude signal with a frequency of about 3 KHz on the control line causing the modulation effect. It was practically very difficult to track down the source of this problem since by looking at the output of this power supply with an oscilloscope one would not observe this 3 KHz signal due to its very small magnitude. Looking at the output of this power supply directly with a spectrum analyzer provided no information on the problem-causing 3 KHz signal since the spectrum analyzer which was used had a minimum frequency limit higher than 3 KHz. Only when the signal was upconverted through the oscillator in test, this 3KHz signal was observed. When this power supply was exchanged for another one of the same brand and model number the problem disappeared. Note that again, in this case no RC filtering was provided on the control line of the VCO.

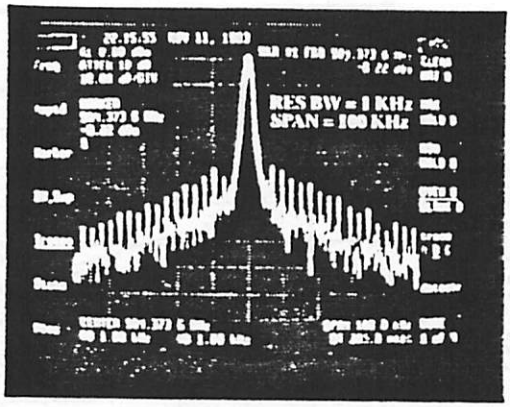


FIGURE 56. The effect of an unclean power supply on the control voltage.

All the above indicate the high sensitivity of high gain oscillators to noise. It is therefore essential to follow the previously mentioned precautions in using these oscillators. Many times it may be required to test the circuitry in an electromagnetically sealed environment to isolate the problem.

5.8.5 Phase Noise Specification and Measurement

In measuring the single sideband phase noise of an oscillator (free running or phase locked), at a certain frequency offset from the carrier frequency, one measures the magnitude of the signal at that offset frequency on the spectrum analyzer and expresses the result in terms of the peak of the carrier in dBc (i.e. dB's below carrier), FIGURE 58. However, since phase noise is defined to be the power of the signal offset from the carrier in a *1Hz bandwidth*, one needs to deduct from the above 10 $\log_{10}$(resolution bandwidth) of the spectrum analyzer[1]. This is required because for example a resolution bandwidth setting of 1000 Hz is effectively admitting 1000 times more noise than the definition for phase noise would call for.

Very low phase noise measurements can not be performed with a spectrum analyzer due to the relatively high phase noise of the synthesized LO of the spectrum analyzer itself. The limitation of a few different models of spectrum analyzers in measuring phase noise is shown in FIGURE 57. A phase noise measurement instrument with a very high spectral purity oscillator is typically used for measuring small values of phase noise.

1. This is for most applications a reasonably accurate estimate. In reality the noise bandwidth of the spectrum analyzer is slightly larger than its resolution bandwidth.

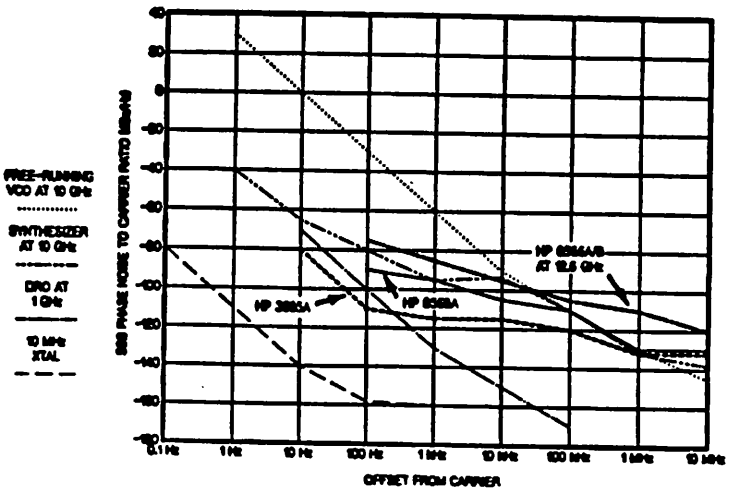


FIGURE 57. Limitation of a few different models of spectrum analyzers in measuring phase noise (after [30]).

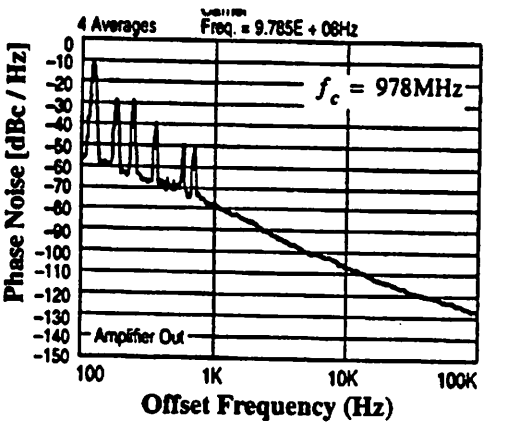


FIGURE 58. Phase noise behavior of a typical coaxial resonator type VCO as accurately measured using a phase-noise meter.

5.8.5.1 Analytical Treatment of Phase Noise

Oscillator noise and phase noise[1] are analytically difficult to analyze. Their contribution to the system performance, however, can be significant and therefore they have to be taken

1. Oscillator noise close in to the carrier is almost entirely due to phase modulation (PM) of the carrier and therefore phase noise and oscillator noise are effectively synonymous in that region. Far out from the carrier, as the phase noise is reduced, AM noise may become a significant contributor to the oscillator noise. To make the issue more complicated, AM to PM conversion can also enter the picture.

into account. A perfect oscillator would oscillate only at one frequency and have a frequency domain impulse shape. Real oscillators however can produce a significant amount of energy outside of the desired carrier frequency. This is referred to as oscillator noise. The oscillator noise, for example, can effect a transmitter in causing the transmission of signal above and below the carrier frequency of interest. In a receiver, the oscillator noise can cause the mixing of undesired signals into the IF bandwidth. In many cases, the inter-channel separation is limited by the phase noise of the local oscillator.

The oscillator output can be represented by

$$V(t) = A(t)[\cos(\omega_0 t) + \theta(t)] \qquad \text{(EQ 52)}$$

If A(t) is relatively constant (as it usually is), the oscillator noise would be due to the phase noise, $\theta(t)$. If V(t) were frequency modulated by a sinusoid with a frequency ω_m the resulting signal would be

$$V(t) = A\cos\left(\omega_0 t + \frac{\Delta\omega}{\omega_m}\sin(\omega_m t)\right) \qquad \text{(EQ 53)}$$

where $\Delta\omega$ is the peak frequency variation and $\Delta\omega / \omega_m$ is the modulation index, β. β indicates the peak *phase* variation. In this system, provisions have been provided for deliberately introducing phase noise on the oscillators and observing the system performance in the presence of phase noise. In this way the effect of phase noise on system BER, for example, can be quantified and analytical models can be refined accordingly. In order to inject phase noise in the system, the "modulation" input of the oscillators has been made available to the user. The input signal is usually tied to this input in a direct-FM modulator, resulting in a FM modulated signal at the output. In this system, this pin has been made available for phase noise injection.

Using equation [53], it can be shown that if the peak phase deviation is small, ($\beta << 1$), the phase deviation results in frequency components on the two sides of the carrier at frequencies $\omega_0 \pm \omega_f$, hence the name *phase* noise. If this noise power $S_\phi(\omega_m)$, normalized to the carrier frequency magnitude and ω_m away from the carrier frequency, is interpreted as being due to a single sideband phase modulating noise at a frequency ω_m it can be shown that [18]

$$S_\phi(\omega_m) = \frac{\beta^2}{2} \qquad \text{(EQ 54)}$$

Where β can be interpreted as the *peak* value of the phase modulation. The larger the phase modulation, the larger the oscillator phase noise.

Leeson has proposed the following relation for the output noise power spectral density of a free-running oscillator

$$S_\phi(\omega) = S_\theta(\omega)\left(1 + \frac{\omega_0^2}{4Q^2\omega^2}\right) \qquad \text{(EQ 55)}$$

where Q represents the Q of the resonance element and $S_\theta(\omega)$ the noise power spectral density of the feedback amplifier used in the construction of the oscillator. If ω_{amp} is assumed to be the flicker noise corner of the amplifier (FIGURE 59), then two different scenarios are possible, depending on the Q of the oscillator tank (FIGURE 59 a, b). If the tank has a high Q (case a), the near phase noise (region 1) is dominated by the flicker noise of the amplifier as well as the Q of the resonator as dictated by equation [55]. Because of the high Q of the resonant element, the flicker noise of the amplifier would be the only major factor affecting the phase noise of the oscillator in region (2). In the absence of any external noise filtering, the ultimate noise performance of the oscillator for frequencies far away from the center frequency (region 3) would be determined by the noise floor of the amplifier. A similar explanation could be made for the case of a low Q resonant oscillator (FIGURE 59.b) where the amplifier flicker noise corner modulated to the carrier frequency is smaller than $\omega_0 / 2Q$. The above is a gross simplification of the actual situation but it does help in the understanding of the complex phase noise phenomena. For example, the figures shown below ignore any other frequency dependent noise of the feedback amplifier besides its flicker noise. Bipolar amplifiers in general tend to have a lower flicker noise frequency and would therefore be much preferred as far as phase noise performance is concerned over field effect devices in designing oscillators. Furthermore, Si devices tend to have a lower flicker noise corner than their GaAs counterparts.

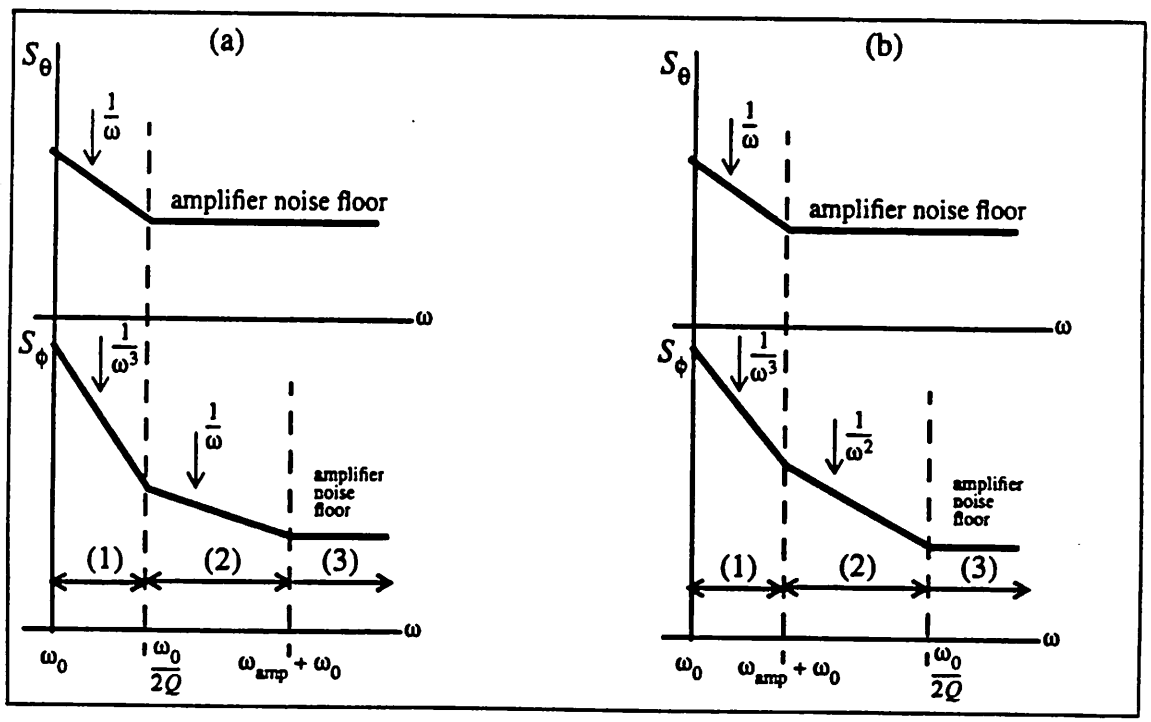


FIGURE 59. Output noise power spectral density of a free-running VCO. (a) with high Q resonance element(s) (b) with low Q resonance element(s).

The analysis of the phase noise performance of an oscillator in a phase-locked loop configuration can get very complicated, particularly if non-linear models are used for the PLL. It can be intuitively stated and analytically shown, however, that the phase noise performance of the oscillator is primarily determined by the phase noise of the reference oscillator (and the phase detector's phase noise) within the loop filter bandwidth. Outside of this region, the phase noise performance of the oscillator is determined by the phase noise of the free-running VCO, as the feedback loop cannot do much in correcting any phase variations. It is therefore essential for low phase noise operation to use a reference oscillator with a good medium to long-term stability (low phase noise for low offset, "nearby," frequencies) and a VCO with good short term stability (low phase noise at high offset frequencies).

It can mathematically be shown that frequency division by N reduces the noise power spectral density by N^2.

Finally, it is interesting to note that in ring-type oscillators, phase noise can be minimized by minimizing the timing jitter in the inverter stages since the spectral density of the phase fluctuations $S_\Phi(f)$ is related to the normalized frequency fluctuations spectral density $S_y(f)$ by

$$S_\Phi(f_m) = \left(\frac{f_0}{f_m}\right)^2 S_y(f_m) \qquad \text{(EQ 56)}$$

where $y(t) = \Delta f(t) / f_0$ is the normalized frequency fluctuations, f_m is the offset frequency from the carrier and f_0 is the carrier frequency [19].

6.0 Board layout and EMI Issues

6.1 Ground and Power Distribution Methods

In the design of high frequency analog and digital systems, the use of ground planes is essential. Because of cost considerations, however, many times system designers have to opt to a 2 layer board for example with no dedicated ground or power planes. Special techniques exist for such cases which can be used for relatively low frequency applications (e.g. the "cross-hatched system," or the "grid system" [20], [21]). Due to much higher return-path inductance the resultant board will not have as good of a performance, however, as an equivalent board with dedicated ground and power planes.

6.2 Grounds and Power Planes

6.2.1 Reduction of Magnetic Coupling Due to the Use of Ground Planes

Signals follow the path of minimum *impedance*. At the lower frequencies, the resistive part of the impedance is dominant and the signals will typically follow the shortest return path to the source (FIGURE 60.a). However at higher frequencies, the dominant part of the impedance is its imaginary part due to the inductive behavior of the traces, i.e. reactance. Therefore, these signals do not necessarily follow the shortest physical path to the source. In the presence of a ground plane (and this is one of the major advantages of using a ground plane), the high frequency signal will flow on a return path exactly underneath the forward signal (FIGURE 60.b) resulting in a better cancellation of the radiated fields by the original signal. The forward current generates a magnetic field in one direction (right hand rule), and the return current generates a magnetic field in the opposite direction (right hand rule). At high enough frequencies the return signal will automatically flow underneath the forward signal because this path offers the minimum loop area which corresponds to the minimum inductance and minimum impedance. The frequency at which the reactance component of the impedance becomes dominant is primarily a function of physical dimensions of the board. For a 1 oz. (1.4 mil thick) copper, the resistance is approximated as 0.64mΩ/❑ [22] and the (loop) inductance is approximated as 0.18nH/❑ [23] and therefore for $f \gg (R/L \approx 0.6\text{MHz})$ the return current flows exactly underneath the forward current. Note that the 0.6 MHz value is only an approximation, as the actual inductance of the loop clearly depends on the dielectric thickness used in between the copper layers. The larger the dielectric thickness, the lower the frequency where the impedance is dominated by the inductance.

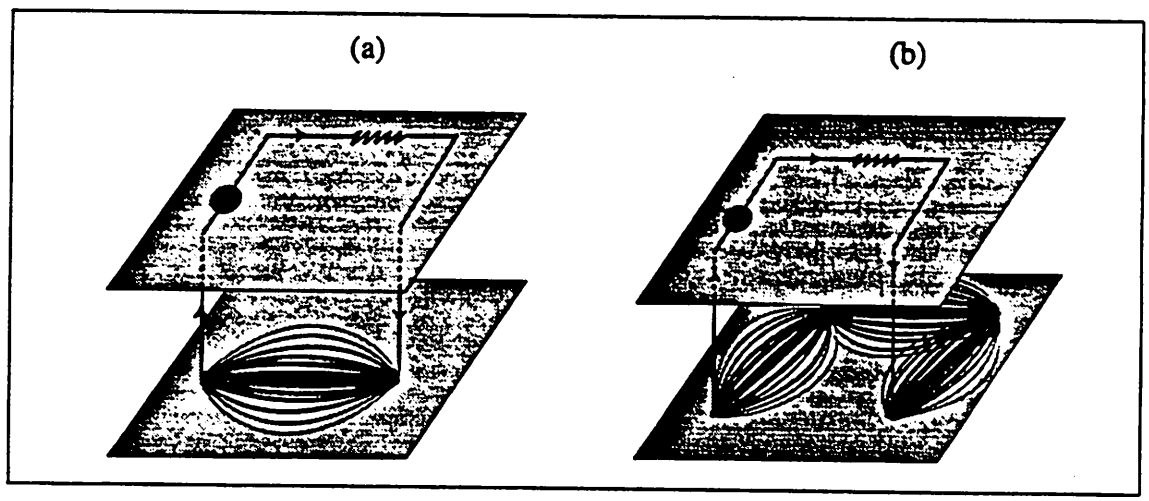


FIGURE 60. (a) DC currents take the path of minimum *resistance* (b) AC currents take the path of minimum *inductance*, minimizing the loop area by flowing underneath the forward signal and cancelling the induced magnetic field to the first order.

It is also important to note that in the absence of a ground plane the signals will still follow the path of minimum impedance, but this path will most likely not fall exactly under the forward signal (since there is no conductive trace there), resulting in a partial or no cancel-

lation of the fields. As far as the field cancellation is concerned, the less the dielectric thickness, the better the field cancellation. In other words, a thinner dielectric layer reduces the loop area which results in the reduction of the inductance, and hence the reduction of the radiation and cross-talk (note that inductive cross talk is directly proportional to the mutual inductance between two wires, and that mutual inductance is related to the self-inductance of each of the wires).

6.2.2 Reduction of Far-Field Electric Interference Through the Use of Ground Planes

The strength of an electric field in the far field at a distance d from a magnetic dipole source with a current magnitude I and current frequency ω is given by [20]

$$|E| = 2.09 \times 10^{-15} \frac{\omega^2 IA}{d} \text{ [V/m]} \qquad \text{(EQ 57)}$$

It is clear from equation [57] that reducing the enclosed loop area A reduces the radiated electric field proportionally. Note that the strength of the radiated signal in the far field is typically much more of interest in the study of electromagnetic compatibility (EMC) issues, such as passing FCC requirements for a product. However, as the board sizes and operating frequencies increase, segments of the board will be in the far field in reference to some noise sources on that board and therefore the study of the signal strengths in the far field becomes also important to the functionality of the board. For example at 1GHz, a distance of more than approximately $\lambda / 2\pi \approx 5\text{cm}$ away from a source is considered to be in the far field.

6.2.3 Effect of Ground Planes on Near-Field Electric Coupling (Cross-Talk)

The use of a ground plane can also help reduce the capacitive (electric field) cross-talk between signals by referring a significant part of the electric flux to the ground plane instead of the other signal [24]. This is shown visually in FIGURE 61, assuming that the dielectric material in the PCB is linear and homogenous. The electric flux density is higher in the FR4 dielectric than it is in the air due to the higher dielectric constant of FR4.

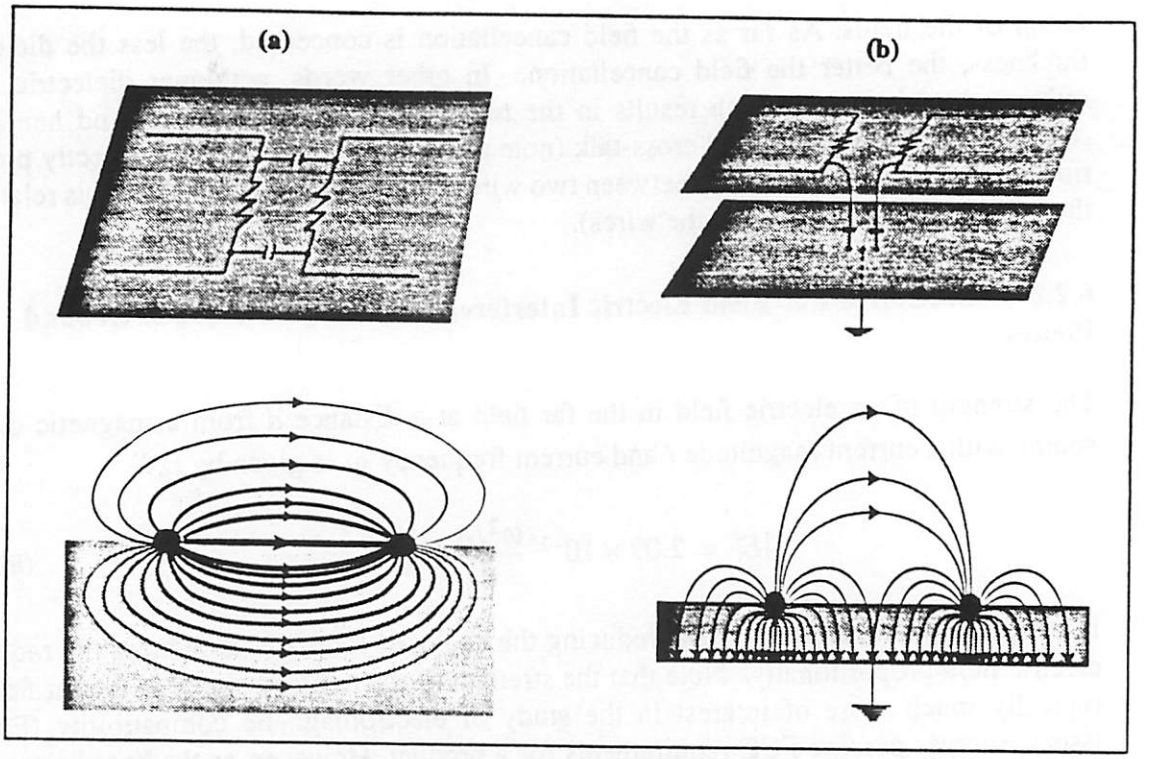


FIGURE 61. (a) Capacitive coupling and electric displacement in the absence of a ground plane. (b) Capacitive coupling and electric displacement in the presence of a ground plane.

6.2.4 The Use of Slitted Ground Planes

An effective means of isolating the different parts of a PCB is the use of slitted ground and power planes. This mechanism may be useful in isolating the digital side of the board from the analog side, or the transmitter from the receiver in a transceiver (as utilized in the second revision of this board and shown in Appendix G, "Artwork"), or for providing a clean I/O region for inter-board wires. There is usually a *single* point of contact between the two regions of the slitted ground plane.

6.2.5 Ground Loop Issues

A single-point of contact is used to avoid ground loop induced noise problems. If there exists more than a single point of contact in a slitted ground plane, AC and DC currents can flow between the contact points resulting in potential difference between the points. The existence of this "loop" makes the circuit more vulnerable to external magnetic fields. The loop also can act as a transmitting antenna, radiating signals which would otherwise be contained. In a receiver application for example, where the input signal is often a fraction of a microvolt, such a ground current is intolerable. Therefore unless it can be guaranteed that the multiple points of contact for a slit are sufficiently equipotential, a single point of contact method should be utilized. Even in a single point of contact method, care must be taken to prevent the slit acting as a slit antenna.

Ground loops are usually more of a problem when the separation between the grounding points are far apart and/or when the ground connections are connected to the ac power ground (generating a very large loop through the ac supply grid). Similar to any other noise source, a ground loop induced noise is not of consequence as long as the magnitude of the induced noise is small enough to allow for the designed SNR in the system. Ground loops typically exist at relatively low frequencies only.

6.2.5.1 Combatting Ground Loops

Many methods exist for reducing the effects of ground loops. These include the use of baluns[1] (common mode chokes), transformers, differential circuitry, and optical couplers. The above methods work by effectively breaking the ground loop and/or making the ground loop induced noise voltage appear as a common mode signal. The effectiveness of these methods is therefore determined by the amount of parasitic capacitive coupling of the ground loop signal and/or the matching of the differential circuitry. It is important to note that at high frequencies, a single point of contact ground may act as a multiple point of contact ground due to parasitic capacitances, and therefore require attention to the ground loop problem.

6.2.5.2 Optocouplers

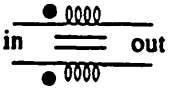
In order to reduce the potential for digital circuitry noise affecting high sensitivity analog front end circuitry, the use of optocouplers was considered for the connection between the output of the demodulator to the input of the ADC's and for the connection between the output of the DACs and the input of the modulator. High linearity wideband optocouplers as needed in this application (approximately 20MHz of bandwidth with 8bits of linearity) are not available at the present time. An alternative method would be to use the optocouplers at the digital side of the ADC's and DACs where linearity is not an issue. This would require 8 optocouplers, however for each ADC/DAC and is unpractical.

6.2.6 Discontinuities in the Ground Planes

The major advantage offered by using ground planes is the reduced enclosed loop area by the currents. It is therefore essential to eliminate any mechanism that would result in large loop areas. A slitted ground/power plane mentioned above will cause large loop areas *if* signals are routed across the slit on the component or the solder side of the board

---

1. Although the term "balun" is usually referred to a transmission line transformer, a tightly coupled 1:1 wire-wound transformer configured as



also is sometimes referred to as a balun. The primary difference in the use of a transformer for breaking the ground loop as opposed to a balun is that a balun would allow dc coupling of the signal.

(FIGURE 62.a). Similar problems can be caused by routes carved out on the ground plane or any other improper discontinuities in the ground plane.

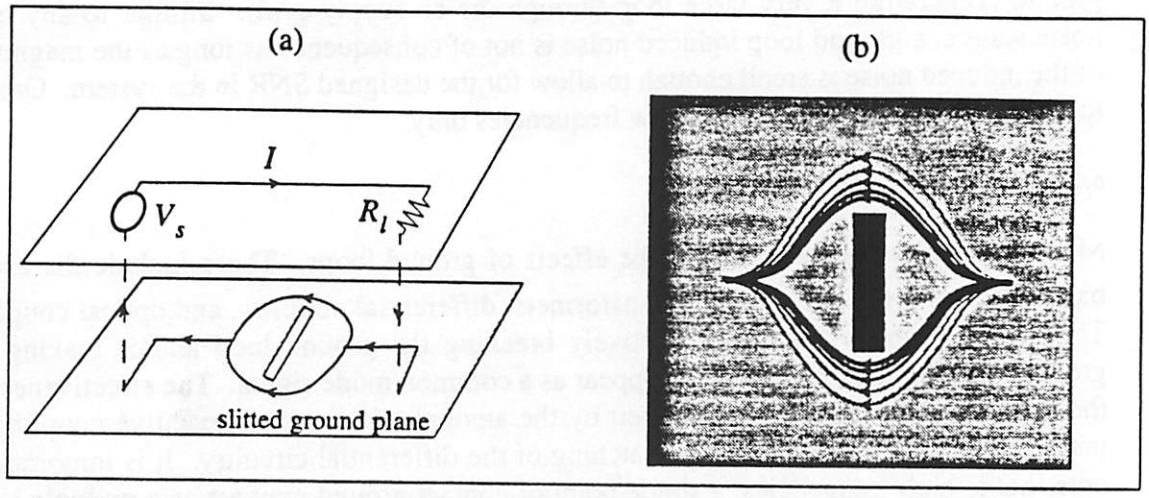


FIGURE 62. (a) Effect of an improperly routed signal over a slitted ground plane on return currents. This configuration can also generate ground loops. (b) A more realistic view of the return current displaying the current density.

6.3 Power Supply Bypassing

6.3.1 Bypassing for High-Speed Digital Circuitry

The use of proper power supply bypassing is also essential. In the case of digital circuitry, the high speed switching of signals and the inductive bond wire path from high speed digital components' power supply connection and ground connection to the PCB result in a power and ground bounce effect which can cause the supply and the ground potential to change significantly. For modern digital circuits, the ac component of the bias current is composed of narrow spikes of several nano-seconds of duration. At such speeds, the ac bias current must be treated as a high frequency RF signal as opposed to a dc bias signal. Without the use of local bypassing capacitors, the ac bias current will have to be provided directly by the supply, frequently located far away from the digital load element. Even if the presence of a long inductive path from the supply to the digital load is not a problem from the stand point of the digital component, the fact that these noise spikes have to travel a long distance can cause major disturbances to the more sensitive analog circuitry (and sometimes even other digital circuits). Furthermore, the ac current can induce a magnetic field on the long supply lead causing it to act as an antenna and radiate noise. The point of using local bypassing capacitors for high speed digital circuitry is then to provide for a local charge reservoir to compensate for such fluctuations, provide the ac component of the current locally, and hence prevent the spikes from distributing.

6.3.2 Bypassing for Analog Circuitry

In the case of analog circuitry, particularly low noise components, proper bypassing is also essential. Even if there are no digital circuits present in the system (which is an unlikely

scenario in modern electronics) and no ground and supply bounces exist, proper bypassing of the supply lines provides for an effective filtering scheme against the high frequency components on the ground and power lines. The use of shunt capacitors provides for a LPF which shunts the high frequency components to ground. Theoretically, one could simply use the largest value capacitor that space limitations allow in order to achieve the best bypassing, but in reality large valued capacitors ar ineffective at the higher frequencies.

In a digital component bypassing case, the amount of the ac current provided by the local bypass capacitor is determined by the impedance of the bypass capacitor at the frequency of interest as compared to the impedance of the supply line as seen by the load at that frequency. In the case of an analog component the low pass cutoff of the bypassing circuitry is determined by the reactance of the bypass capacitor and the supply impedance that it sees (assuming that the supply impedance is much smaller than the load impedance which is often the case).

An ideal decoupling mechanism would provide a zero impedance path for the DC signal to the load (through the decoupling elements) and an infinite impedance path for all other frequencies. This translates into the use of the highest value bypass capacitors. In the real world, high valued capacitors are usually of the electrolytic form which have a very low self resonant frequency (primarily because of the particular type of packaging which is used for these type of capacitors and because of their high value as explained in Section 5.7.2.1.D, "Physical Capacitors") and cannot provide a low impedance path to ground at the higher frequencies because of their inductive behavior. Tantalum capacitors are slightly better in that sense but typically cannot achieve as high of a value. Surface mount ceramic chip capacitors typically offer a very high self resonant frequency, but have a maximum value of about 1uF.

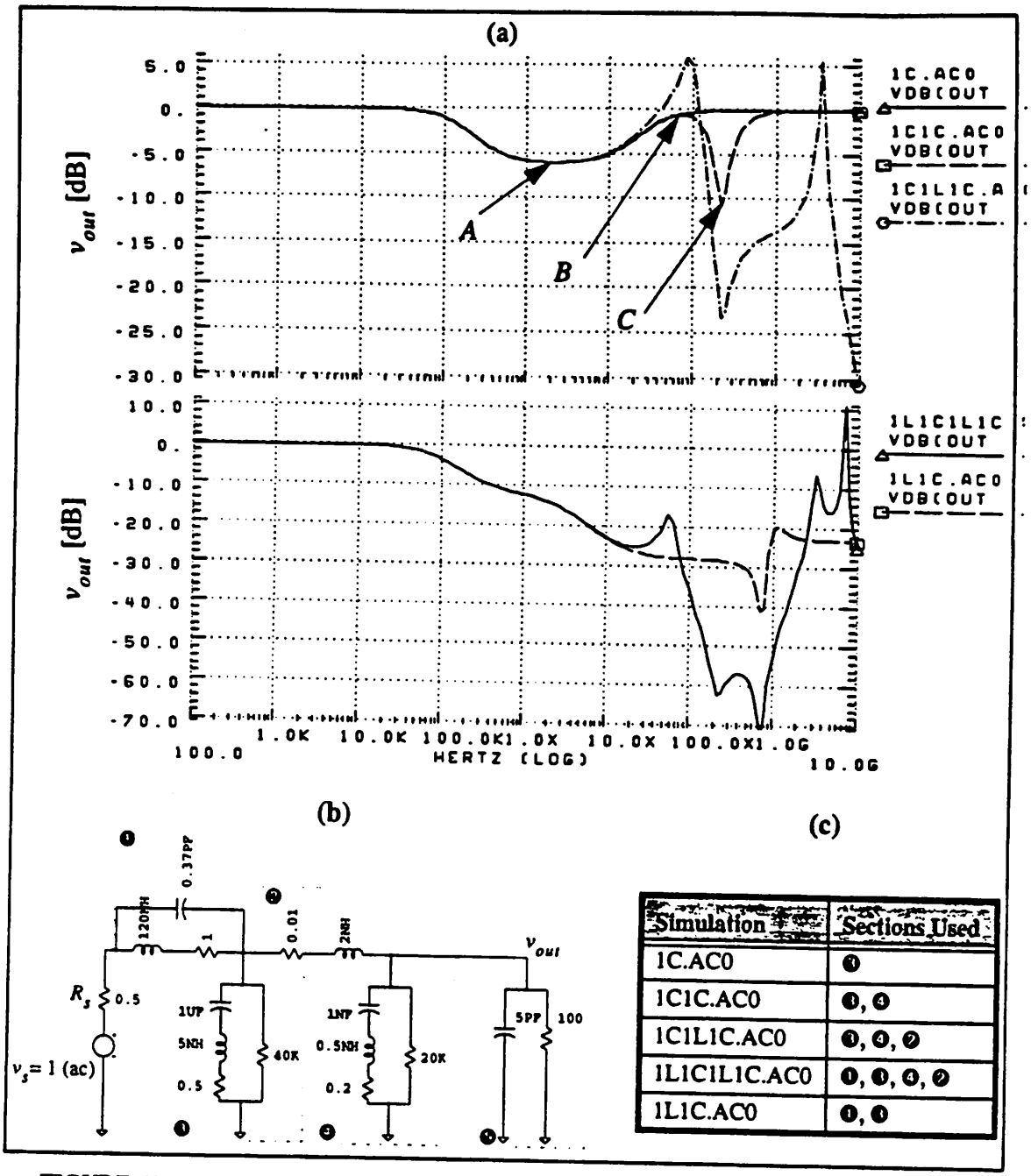
To summarize, the problem is that large value capacitors offer a low impedance path to ground at the lower frequencies, but not at the higher frequencies. Smaller value capacitors do the opposite.

6.3.3 Various methods of Supply Bypassing

Examples of various methods of bypassing a component from the power supply are shown in FIGURE 63. It is evident from FIGURE 63.a, curve 1C.AC0 that a single bypass capacitor does not offer much of an attenuation of power supply noise; at the lower frequencies because of its small capacitance and resulting large impedance as compared to the load, and at the higher frequencies due to its self resonance and its large impedance as compared to the load. To overcome the problem of bypassing at the higher frequencies, multiple different value capacitors can be used in parallel. A potential problem with this scheme is that the inductance of the larger value capacitors can resonate (parallel resonance) with the capacitance of the smaller capacitors at particular frequencies resulting in a very high impedance to ground at those frequencies which makes the bypassing ineffective at those frequency. For example, FIGURE 63.a, curve 1C1C.AC0 displays the result of using the circuit of FIGURE 63.b with capacitor blocks ❸ and ❹ used as bypassing elements. At first glance this method provides a better decoupling than a single capacitor at

all frequencies (for this particular example). The resonance points have been identified on the figure as points *A* (1μF capacitor self resonating with its 5nH capacitor; series resonance), *B* (5nH inductor resonating with 1nF inductance of second capacitor; parallel resonance), and *C* (1nF capacitor self resonating with its 0.5nH inductance; series resonance). Clearly, in this case, the series resonance of the elements provides a high impedance path to ground resulting in a better decoupling, but the parallel resonance provides for a low-impedance path to ground and loss of effective decoupling.

The problem with using multiple valued capacitors in parallel is more pronounced when the value difference between the capacitors is large. However this scheme can be particularly dangerous if the bypass capacitors are placed physically far apart. This results in a series inductance on the trace connecting the capacitors as shown in block ❷ of FIGURE 63.b and simulated as curve 1C1L1C.AC0 of FIGURE 63.a. Although the decoupling is improved at most frequencies, two clear resonant points are generated that *boost* the unwanted noise on the power supply as seen by the load. Of course the series resistance of the interconnect trace reduces the peak of the resonance, but the magnitude of the series resistance is typically small. Inserting a small damping resistor will cause an IR drop across the resistor. In any case, one needs to be very careful in using multiple different value capacitors as the bypass elements. This is why many designers use a single capacitor for bypassing and choose the value of this capacitor such that it provides a low impedance path to ground up to the highest frequency of interest while accounting for its self resonance frequency. Sometimes it helps to put two capacitors *with the same value* in parallel, and very closely spaced. This reduces the effect of the series inductance by as much as 50% by putting the inductors in (pseudo) parallel. The limitation here is that more than two capacitors in parallel usually does not improve the situation by much as the PCB parasitics take over as the dominant parasitic inductive elements.



Simulation	Sections Used
1C.AC0	❸
1C1C.AC0	❶, ❹
1C1L1C.AC0	❶, ❹, ❷
1L1C1L1C.AC0	❶, ❶, ❸, ❷
1L1C.AC0	❶, ❸

FIGURE 63. (a) SPICE ac sweep outputs for several methods of supply bypassing, split into two graphs for clarity. Points *A*, *B*, and *C* designate resonance points of the 1C1C.AC0 curve. The complete schematic is shown in (b) and the various sections used for curves shown in (a) are outlined in (c). Various blocks shown in (b) are: ❶ Inductor bypassing at the source. The inductor parasitics are also shown. ❷ Approximate series resistance and inductance of a 1 cm long interconnect wire on the PCB. ❸ Large bypass capacitor and associated parasitics. ❹ Small bypass capacitor and associated parasitics. ❺ The load. This load was used for all simulations outlined in (c).

Many times, in addition to the bypass capacitor(s) a series inductor is added to help the bypassing scheme (FIGURE 64.b, block ❶). This method allows for a higher order LPF, and often even at resonance with the bypass capacitor will provide a very low pass impedance to ground as seen by the source (curve 1L1C.AC0 in FIGURE 63.a). In other words,

with no bypass series inductor, the resistance of the bypass node is typically very low (as it is in parallel with the source resistance) and the low-pass cutoff frequency is therefore very high, resulting in an inefficient bypassing scheme. By providing a series inductor, the impedance seen by the capacitor is increased significantly, resulting in a much better bypassing scheme. It is important to note that peaking resonant situations can occur in this case also.

In general, in order to maximize decoupling efficiency, it is essential to keep the bypass capacitor as close as possible to the supply pin on the IC package. The bypass inductor (ferrite bead, etc.) can be placed as far as necessary from the IC package.

6.3.3.1 Use of Ferrite Beads for Supply Bypassing

The use of ferrite beads is also common for supply series bypassing. Ferrite beads are inductors wound on a ferromagnetic material, and can be to the first order modelled as a resistor in series with an inductor. They typically offer a higher value inductance along with a higher value SRF as compared to their air-wound counterparts. They are, however, lossy even at DC, and therefore have a typically low Q (which is desirable in a supply decoupling application). They are also often used to dampen high frequency parasitic-based oscillations in a circuit. Ferrite beads are typically specified with a characteristic curve which shows their impedance (and resistance) as a function of frequency (FIGURE 64.b). At the higher frequencies they are typically purely resistive, whereas at the lower frequencies they display more of an inductive behavior. Due to use of a ferro-magnetic core, ferrite beads are prone to magnetic saturation as a result of excessive amounts of current.

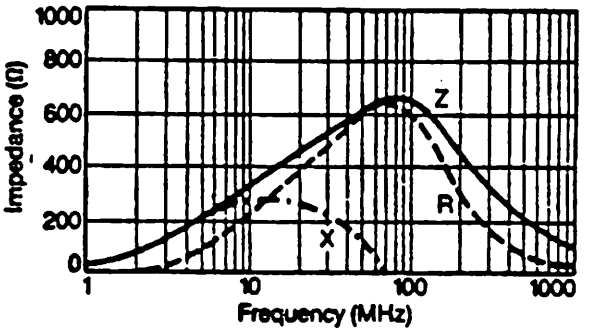


FIGURE 64. The characteristics of a ferrite bead: typically reactive at lower frequencies and resistive at the higher frequencies.

6.4 Splitted or Slitted Power Planes

Another method commonly used in reducing the coupling between the different sections of a board is to slit or split the ground and power planes. If properly used, this method can significantly reduce the cross talk between the different sections of the circuit. What is commonly done for example, in circuits where both high speed digital circuitry and low

noise analog circuitry exist, is to separate the power and ground planes into two sections and distribute the power to these sections with a single point of contact at the power supply. If more than one point of contact exists between the analog and digital sections, ground loops may be created.

6.5 EMI Issues on the I/O Section

6.5.1 I/O Cables and EMI

When some critical signals have to travel from one board to another via unshielded wires, it is best to keep the I/O section of the board as far apart as possible from the noisy elements of the circuit. These unshielded wires behave as good antennas and are prone to both electromagnetic radiation and pickup. The most preferred wired method of inter-board communications for critical signals is the use of coaxial cables. The use of such cables however is expensive and difficult, and many designers opt for a twisted pair wire or a ribbon cable. In general twisted pair wires (signal with accompanying ground) offers a better performance than ribbon cable wires. If a ribbon cable is used, it is best to have a ground wire for every signal wire as shown in FIGURE 65 where the return signal can return in the two adjacent ground wires, forming a crude coplanar transmission line, which is much more immune to radiation and pickup than a single wire. This reduces the co-wire interference because each wire has its own return path[1]. In any case, it is best to keep the inter-board cables as short as possible.

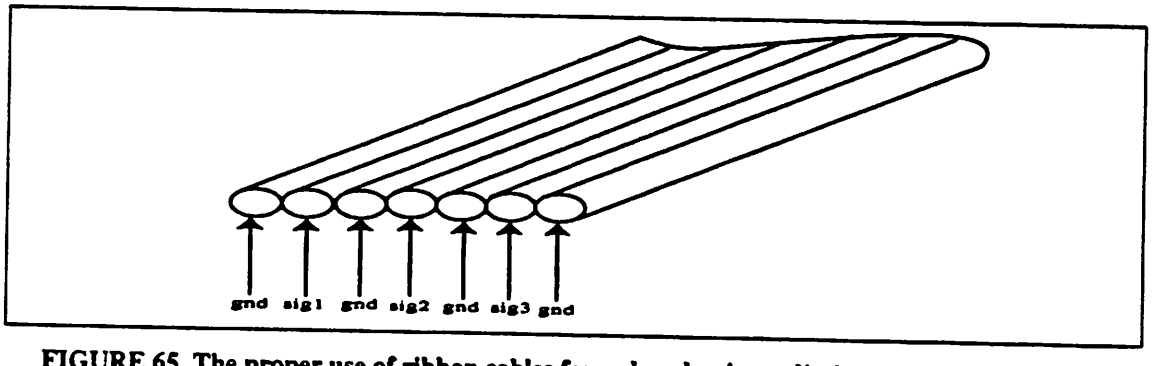


FIGURE 65. The proper use of ribbon cables for reduced noise radiation and pickup.

6.5.2 I/O Region Board Layout

Sometimes it is useful to separate the noisy part of the board from the I/O region by using a clean I/O ground regions. This is accomplished by connecting the I/O ground plane to the main board ground plane by the use of a single point of contact method (FIGURE 66). This may provide a quiet ground region by providing a high impedance path to the signals that do not belong in that area.

1. .The use of alternating ground lines could be used effectively to reduce cross-talk in SIP resistors also.

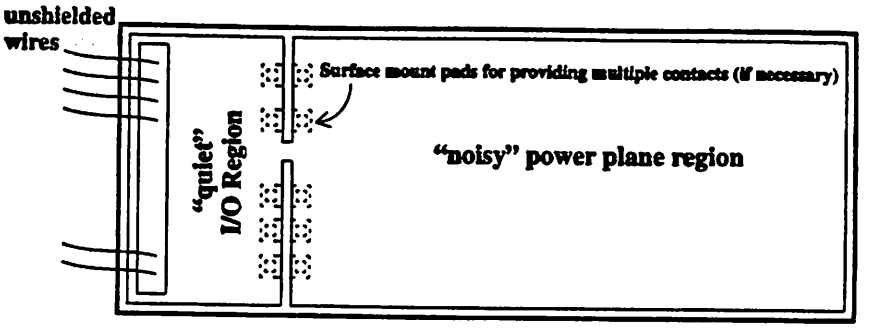


FIGURE 66. A dedicated "quiet" I/O ground region may reduce EMI radiation and pickup.

In general, proper layout for minimization of coupling of signals and EMI is much more of an art than a science at this time. Many EMI experts for example, recommend the use of multiple pads across the slitted/splitted ground planes so that the performance of the system can be evaluated by inserting zero ohm resistors across these pads; a purely trial and error based system (FIGURE 66). Fortunately, sophisticated 2 dimensional and 3-dimensional modeling tools are slowly emerging which could help in the analyzing of these very difficult problems by solving Laplace's equations by various finite element methods. Solving Laplace's equation for most real world problems is an extremely computationally intensive task.

6.6 Controlled Impedance Lines

6.6.1 When To Use Transmission Lines

The use of controlled impedance lines is essential in high frequency boards where the lengths of the traces becomes comparable to the wavelength of the highest frequency of interest, λ. A rule of thumb which is typically used in RF applications for this purpose is to use controlled impedance lines when the trace length is larger than 1/32 λ. In high speed digital circuit boards, the use of transmission lines is recommended when the "electric length," defined as

$$l_e = \frac{t_r}{v_p(\varepsilon_{eff})} \qquad \text{(EQ 58)}$$

is smaller than 1/6 the physical length of the trace carrying the signal. In equation [58] t_r is the rise time of the signal and $v_p(\varepsilon_{eff})$ is the propagation speed of the waves in the dielectric as a function of the effective permittivity of the material (see equation [101]). Clearly the above guidelines are only rules-of-thumb and different literature may quote different guidelines.

The two extremes of when transmission lines are to be used is for power distribution lines (60 Hz, 100's of Km's long), to RF circuit boards (GHz range signals, a few cm's long).

The principles are the same in both cases. With the present day technology it is rarely necessary to consider transmission line effects on IC's.

6.6.2 Advantages of Using Transmission Lines

In general, transmission lines offer less distortion, less far-field radiation, and less near-field cross-talk than non-transmission line point-to-point connections. In order for the transmission line to be effective, however, the system designer has to pay particular attention to the special requirements imposed by using such distributed sub-circuits. For example, distributed sub-circuits *always* "ring" if they are not properly terminated (lumped circuits can ring if they have a high Q; for example, high inductance (thin) wire driving large capacitive loads).

Transmission lines reduce EMI and near-field cross talk by somewhat containing the fields (the amount of containment depends on the particular type of transmission line used). Further more, by reducing the overall area enclosed by the current, and hence reducing the inductance, they reduce the amount of generated magnetic field. The magnetic field of one loop caused by a changing current in that loop can cause cross talk by interacting with the magnetic field of another loop (mutual inductance) and hence generating a noise voltage on the second loop.

6.6.3 Intuitive Explanation of Transmission Line Operation

A transmission line is a delicate balance of distributed shunt capacitors and series inductors. This distributed network is shown in FIGURE 67.a for a differential (symmetrical) transmission line where the signal path and its return path are similar (e.g. twisted pair transmission line). The distributed network for a non-symmetrical transmission line, such as that used in a micro-strip is shown in FIGURE 67.b where the return path is assumed to have a very low inductance (a ground plane).

By choosing the proper values for the distributed C and L elements in a transmission line, one effectively tunes out the capacitance and inductance of the transmission line such that the impedance observed at the two port input (port A in FIGURE 67) of an infinitely long ideal transmission line is equal to the characteristic impedance (= characteristic resistance) of the line. For a transmission line that is not infinitely long, but is properly terminated, the same rule applies. For example, in an ideal case, a long RG58 coax cable connecting the 50Ω output of an oscillator to a spectrum analyzer does not cause any capacitive or inductive loading on the oscillator. The oscillator will only be *resistively* loaded by the spectrum analyzer's 50Ω input impedance. In practice a very long RG58 coaxial cable cannot be modelled as an ideal transmission line since its total resistance can become comparable to the characteristic impedance of the line (50Ω) and will therefore introduce amplitude and phase distortion in the signal (See section 6.6.6, "Non-Ideal Transmission Lines").

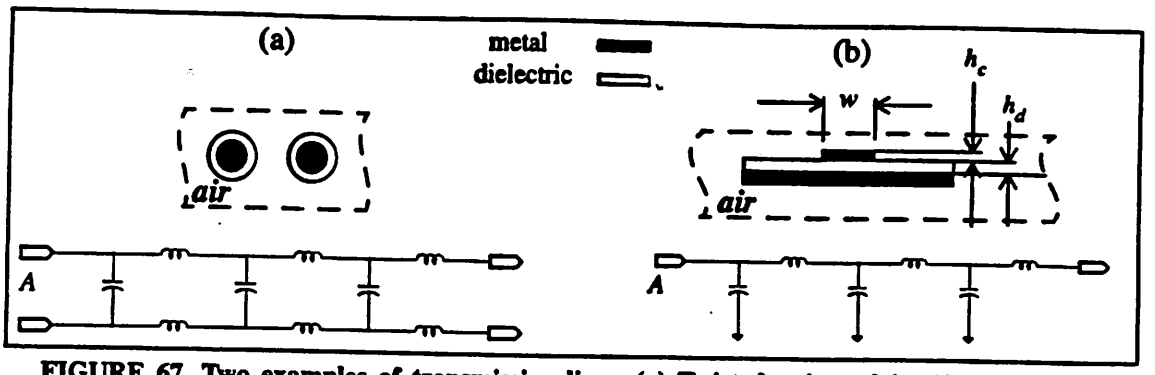


FIGURE 67. Two examples of transmission lines. (a) Twisted pair and its (distributed) ideal circuit model (b) Microstrip and its (distributed) ideal circuit model

6.6.4 Ideal Transmission Lines

In an ideal transmission line, the signals of interest propagate with no phase or amplitude distortion and no signal attenuation. In an ideal transmission line, the propagation speed of the wave is equal to $1 / \sqrt{LC}$ where L and C are the inductance and capacitance of the transmission line per unit length respectively. Since this relation is frequency independent, the resultant signal will have no phase distortion. Furthermore since the transmission line is loss-less for all frequencies, no amplitude distortion exists. For an ideal transmission line, the characteristic impedance is given by the following important relation

$$Z_0 = \sqrt{\frac{L}{C}} \qquad \text{(EQ 59)}$$

For any physical structure transmission line, in order to maintain a constant characteristic impedance, it is essential to keep the above ratio constant. For example, as a crude approximation, the equation for the characteristic impedance of a microstrip with $w \leq h_d$ is given by

$$Z_0 = \frac{\eta_0}{2\pi\sqrt{\varepsilon_e}} \ln\left(8\frac{h_d}{w}\right) \qquad \text{(EQ 60)}$$

A simple way to remember the relations in the above equation is to use the fundamental relation given by equation [59]. For example, if the unit length capacitance, C, is increased by reducing h_d in FIGURE 67.b, the inductance should be increased by the same factor in order to maintain the same characteristic impedance. This can be achieved by reducing w (thinner wires have more inductance). As another example, if the same microstrip is implemented on a different substrate material with a higher dielectric constant, in order to maintain the same characteristic impedance, one needs to increase the unit length inductance L, in order to compensate for the higher capacitance due to the higher permittivity of the dielectric. This line of reasoning can be used for all physical

constructions of transmission lines (coplanar, etc.) as well as for obtaining higher/lower characteristic impedances (e.g. a 50Ω microstrip transmission line will have a wider w on the same layer of a board than its 75Ω counterpart).

As indicated in equation [60] for a microstrip transmission line, the value used for the permittivity of the dielectric is *not* simply the dielectric permittivity. This is because the dielectric on top of the transmission line is air with a relative permittivity of approximately 1. Since the fields are not completely contained in the microstrip dielectric, the epsilon used should be a weighted average of the two dielectrics, ε_e. The relation for ε_e is given in Appendix C, "Characteristic Impedance of Microstrip Transmission Lines".

6.6.5 The Skin Effect

Skin effect is a phenomena which causes the ac current to concentrate on the outermost section of a conductor resulting in the higher frequency components of the signal to experience higher amounts of attenuation.

Intuitively the skin effect phenomena can be explained as follows. Consider the cross section of the stripline given in FIGURE 67.b as shown in FIGURE 68.a. The conductor wire can be imagined as multiple rectangular rings as shown in the magnified view. At higher frequencies, the current takes the path of minimum inductance (since this is the path of minimum impedance). The inner rings display a much higher inductance than the outer rings, and hence the current distributes itself concentrated around the outermost rings. This higher density of current at the outer rings can be modeled as an ac resistance known as the skin effect. Note that in reality, the mutual inductance of these rings also forces the current to concentrate in the outer rings. FIGURE 68.b displays the exponential current density distribution associated with the skin effect. The ac resistance of a square copper line in Ω/in is approximated by [21]

$$R_{ac}(f) = \frac{2.16 \times 10^{-7}}{\text{wire perimeter [in]}} \sqrt{f} \qquad \text{(EQ 61)}$$

(note the square root relation dependence on frequency) and the overall resistance of the square copper is approximated by

$$R(f) = \sqrt{R_{dc}^2 + R_{ac}^2(f)} \qquad \text{(EQ 62)}$$

In the transmission lines used in this system, the skin effect is dominant at frequencies above 6MHz.

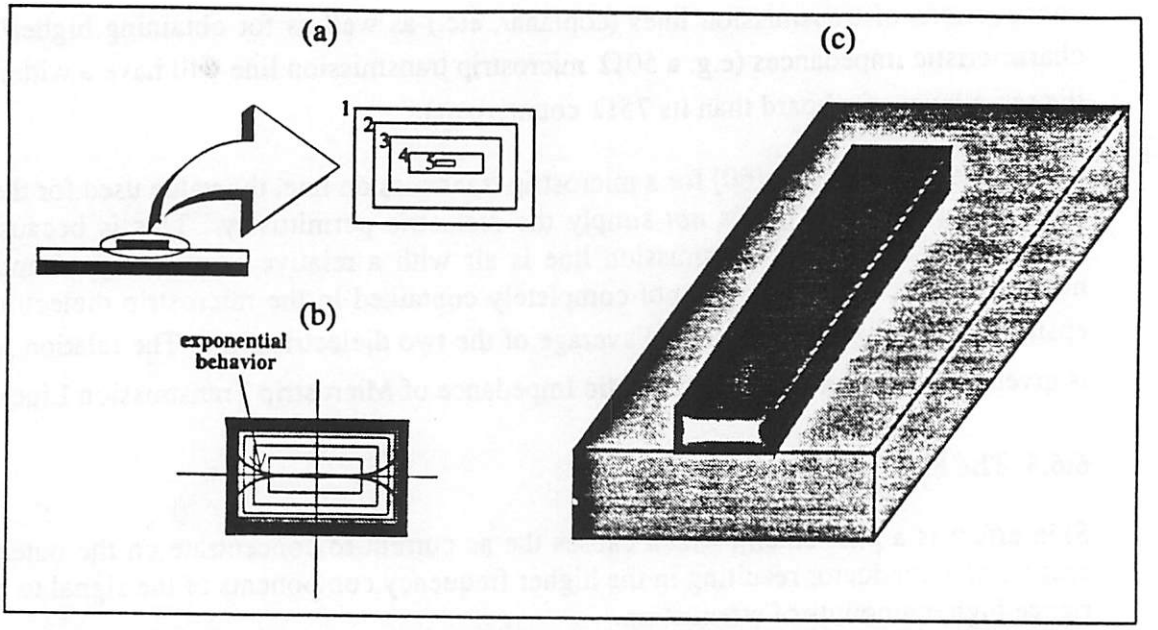


FIGURE 68. Skin effect in a stripline transmission line (a) Physical structure (b) Current density contour plot (cross section) for ac currents in the conductor. Note that current density drops *exponentially* as we get farther away from the surface of the conductor. (c) 3-D model

6.6.6 Non-Ideal Transmission Lines

In a non-ideal transmission line, signals experience a frequency-dependent attenuation due to the skin effect of the conductor. Skin effect is the primary cause of amplitude distortion in transmission lines operating at *high enough* frequencies. Phenomena such as the proximity effect are relatively frequency independent and do not contribute to the amplitude distortion of a transmission line.

In a non-ideal transmission line, the finite series resistance of the line causes phase distortion also. The phase shift introduced by the transmission line is given by[1]

$$\Delta\phi(\omega) \approx \exp\left(-lj \operatorname{Im} \sqrt{(R(\omega) + j\omega L)\ (j\omega C)}\right) \qquad \text{(EQ 63)}$$

where l is the propagation distance, and R, L, and C are the resistance, capacitance and inductance of the transmission line per unit length. For an ideal transmission line ($R = 0$) and for a "low-loss" transmission line ($\omega \approx R\ /L$ and before skin effect becomes dominant) equation [63] results in a linear phase relation and hence no phase distortion. It can similarly be shown that an ideal transmission line or a low-loss transmission line do not introduce amplitude distortion.

The above statements ignore the finite loss in the dielectric material. This loss can be typically ignored for microstrip transmission lines with FR4 dielectric material for operation

1. This relation can be easily derived from equation [66].

at relatively low frequencies. When the dielectric thickness becomes very thin, however, the fields can no longer propagate freely, causing an increase in dialectic losses. In such cases, the dielectric losses may have to be considered. The power loss due to the finite conductivity of a dielectric can be modeled by the dielectric's loss tangent which is given by

$$\tan\delta \approx \frac{\sigma}{\omega\varepsilon_r\varepsilon_0} \qquad \text{(EQ 64)}$$

where σ is the dielectric conductivity and ε_r is the dielectric relative permittivity. The loss tangent for a typical FR4 is approximately 0.02. The loss tangent is a very weak function of frequency, and its dependence on frequency is ignored here.

For a microstrip line the conductance of the dielectric medium, G, in mho/unit-length can be related to the loss tangent (through equation [64]) and the physical properties of the microstrip as follows

$$G = \frac{\sigma}{\varepsilon_r\varepsilon_0}C \qquad \text{(EQ 65)}$$

The amplitude and phase distortion of a non-ideal but infinitely long transmission line which has finite conductor and dielectric losses can be calculated using the complex "transfer function" of a transmission line[1]

$$Y_l(\omega) = e^{-[(R+j\omega L)(G+j\omega C)]^{1/2}} \qquad \text{(EQ 66)}$$

equation [66] can be also applied to a properly terminated, finite length transmission line.

A non-ideal transmission line's operation as a function of frequency can be broken down to three regions. The first region, the so-called "RC transmission line" is the region where amplitude losses are low (and relatively frequency independent) but the phase is proportional to $\sqrt{\omega}$ resulting in a non-linear phase response. This region is characterized by $\omega \ll R/L$. Second, the low-loss region, which is characterized by a relatively constant amplitude attenuation as well as a relatively linear phase response. This region corresponds to frequencies where ω is comparable to R/L. Obviously, given a non-ideal transmission line, this is the best region to operate in. The third region in a transmission line corresponds to $\omega \gg R/L$ where the skin effect is dominant introducing amplitude distortion in the frequency response.

6.6.6.1 Reflections on Transmission Lines

The discussions and relations stated above apply to *infinitely* long transmission lines, where no signals are ever reflected back on the line. Although infinitely long transmission

1. This equation is identical to the equation for the unguided propagation of a plane wave in a lossy media.

lines are impossible to construct, one may achieve the desirable properties of infinitely long transmission lines by using proper terminations.

A system which attempts to carry a high frequency signal over an uncontrolled impedance line, an improperly terminated line, or an unmatched source impedance will face several problems. For example, much of the power of the source will be reflected back and forth between the load and the source and ultimately the total amount of power delivered to the load will be less than a perfectly matched system.

The reflection coefficient of a transmission line, Γ, indicates the fraction of the transmitted signal which is reflected back on the transmission line and is given by

$$\Gamma = \frac{Z - Z_0}{Z + Z_0} \qquad \text{(EQ 67)}$$

where Z is the source or load impedance and Z_0 is the characteristic impedance of the line. Ideally, for a "matched" transmission line where no signals are reflected back we need $\Gamma = 0$ which can be achieved only if $Z = Z_0$. Clearly we can provide proper termination at the load only, at the source only, or at both ends. Providing a termination at the source only can be dangerous since the intermediate circuitry (such as bias elements located between the source and the load) will see one reflection of the transmitted signal. Since a load resistance equal to the source resistance provides maximum power transfer, proper terminations (passive or active) are almost always provided at both ends of the line for RF applications.

It is important to note that the reflection coefficient Γ relates to the scattering parameter S_{11} through the relation

$$S_{11}\,[\text{dB}] = 20\log\Gamma \qquad \text{(EQ 68)}$$

The scattering parameters are the 2-port parameters of choice in the high frequency system and circuits analysis.

6.6.6.2 Right Angle Bends on Transmission Lines

Right angle bends in a microstrip transmission line, if not properly rounded or chamfered, have the effect of a parasitic small capacitance to ground as shown in FIGURE 69.a. This extra capacitance, if large enough compared to the distributed capacitance of the line, can disturb the delicate balance between the line's capacitance and inductance which was shown in FIGURE 67. The amount of parasitic capacitance can be approximated by the simple parallel plate capacitance $C = \varepsilon A / h$, but because of the large fringing field area as compared to the parallel plate area this estimate will not be accurate. A better estimate which relates the amount of capacitance to the properties of the transmission line is given by [21]

$$C \approx 0.61 w \frac{\sqrt{\varepsilon_r}}{Z_0} \qquad \text{(EQ 69)}$$

where w is given in mils, Z_0 in ohms, and C in pF. For the board in this system, if rounding of the right angles had not been performed, the parasitic capacitance would have amounted to 67fF, a small value indeed.

The effect of a parasitic capacitance on the transmission line, as far as the S_{11} is concerned, is a small reflection on the line. Using the reflection coefficient relation, equation [67], substituting $C \parallel Z_0$ for $Z_L = Z$ and assuming $2 \gg \omega Z_0 C$, we obtain

$$\Gamma(\omega) \approx -\frac{1}{2} j\omega Z_0 C \qquad \text{(EQ 70)}$$

which is similar to the s-domain relation for a negative differentiator. In this system, for example, a 1GHz input sinusoid would reflect back an inverted cosinusoidal signal with 1% of the transmitted power when passing through a transmission line with a single right angle bend[1].

6.6.6.3 Transmission Lines Traversing Through Vias

The physical structure of a via and an equivalent circuit model for it are shown in FIGURE 69.b. The parasitic capacitances of the via are primarily due to its pads, whereas its inductance is primarily due to its barrel. For typical size vias in a PCB operating at typical RF frequencies, the capacitance of the via is negligible as compared to its inductance, and the via therefore behaves inductively.

Using the reflection coefficient relation, equation [67], substituting $Z_0 + j\omega L$ (inductive via in series with the transmission line segments) for $Z_L = Z$ and assuming $2 \gg (\omega L \ / \ Z_0)$, we obtain

$$\Gamma(\omega) \approx + \frac{1}{2} \frac{j\omega L}{Z_0} \qquad \text{(EQ 71)}$$

which is similar to the *s*-domain relation for a positive differentiator. In this system, for example, a 1GHz input sinusoid passing through a standard size via (16 mil in diameter, 63 mil length, with an average estimated inductance of 820pH) would reflect back a cosinusoidal signal with 0.82% of the transmitted power.

1. If rounding of the right angles had not been performed.

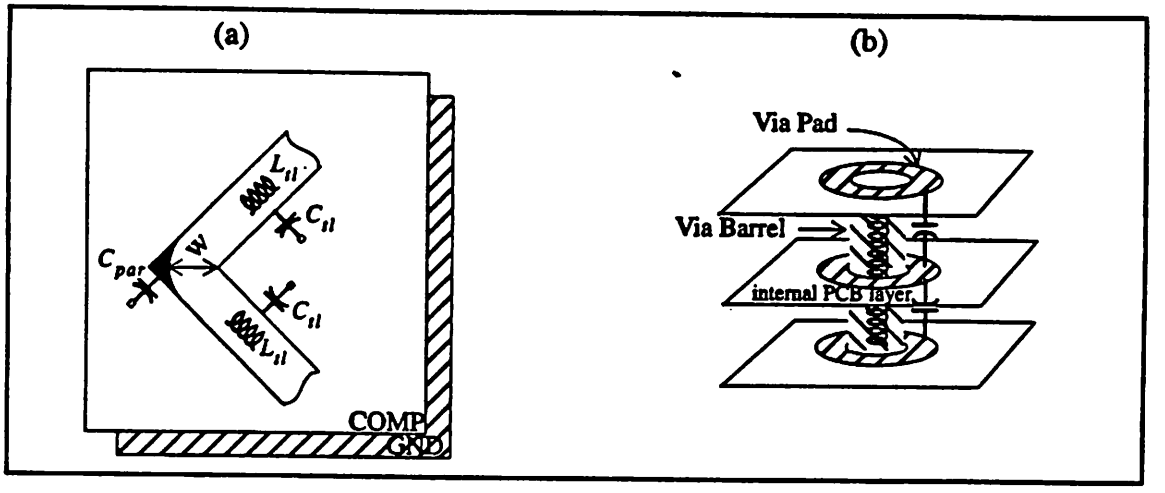


FIGURE 69. (a) Effect of right angle corners on microstrip transmission lines. (b) A via structure and an equivalent circuit for it.

Using the "physical" model of a transmission line in HSPICE, the effect of a signal traversing through multiple vias is investigated and displayed in FIGURE 70. The inductance of each via is estimated at 820pH (based on the three methods presented in Appendix E, "Via Inductance Relations"). The signal is passed through four 1 inch segments of transmission line, going through one via at each transition point. The effect of these vias on the S_{11} and S_{21} of the transmission line are displayed in FIGURE 70 for: via inductance = 0 (ideal case), and via inductance = 820pH compensated with various size capacitors on the two sides of the via. It is clear from FIGURE 70 that this compensation is relatively sensitive to the actual value of the via inductance.

In some applications, it is possible to take advantage of the above results and compensate for the added series inductance of a via to the transmission line by fattening the traces going to the via and hence increasing the local transmission line capacitance (FIGURE 72.a).

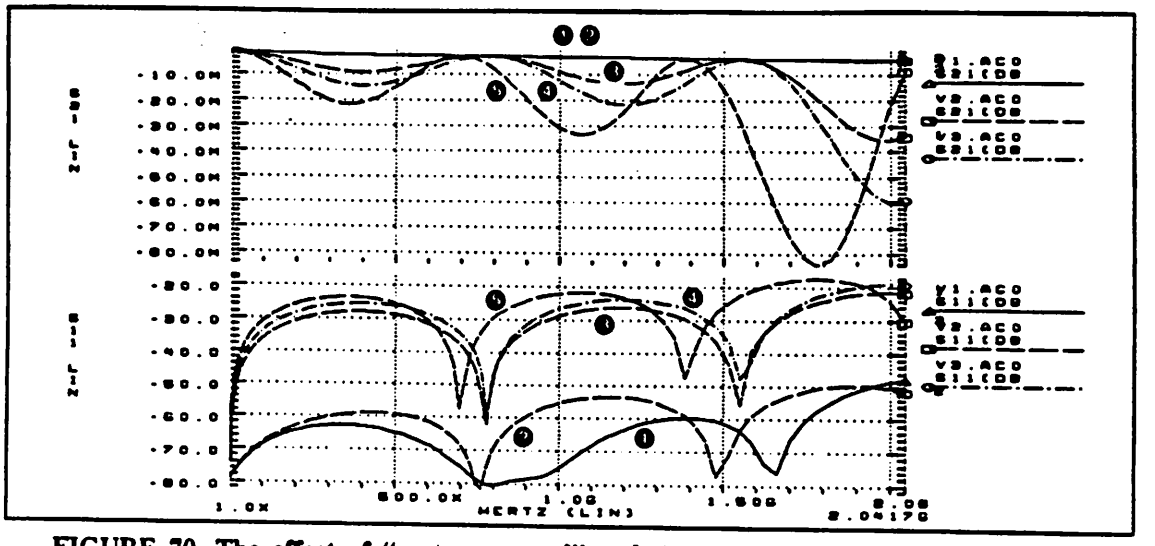


FIGURE 70. The effect of "uncompensated" and "compensated" vias on transmission line characteristics (S_{11} and S_{21}); ❶ with via inductance = 0; and with compensated capacitors on the two sides of each via with ❷ 170fF, ❸ 40fF, and ❹ 400fF; and ❺ with no compensation capacitors.

The inductance of a via in pH, to the first order can be determined by [21]

$$L_{via} = 5.08\times10^{3}h\left[\ln\left(\frac{4h}{d}\right)+1\right] \qquad \text{(EQ 72)}$$

where h is the length of the via and d its diameter. The inductance of a via as a function of its length and its diameter using three different relations is shown in FIGURE 71.

As evident from FIGURE 71, the estimates are at times more than 100% different from one another. This points out to the fact that the actual via inductance is very much PCB process dependent and it is also strongly a function of measurement method. For example, depending on how sharp or dull the drill bits used in PCB manufacturing are, the via inductance can vary significantly (drill bits loose their sharp edges after long periods of use). The values obtained for via inductance, therefore should be used as a crude estimate only. As a general rule of thumb, via inductance increases almost linearly with increasing via length, but decreases logarithmically with increasing via diameter. Increasing via diameter, therefore does little to reduce via inductance.

The relations resulting in the graphs of FIGURE 71 are given in Appendix E, "Via Inductance Relations". It is important to note that all of these relations have their range of validity, beyond which they can result in a negative inductance value.

As a final note on this subject, it is interesting to note that graphs have been compiled from experimental measurements of the inductance of a via [36]. One important factor included in these graphs is the ratio of the via diameter to the width of the traces that the via ties to one another. The larger this ratio, the smaller the effective via inductance, as in this case, on average the current has to traverse a shorter path to reach the via.

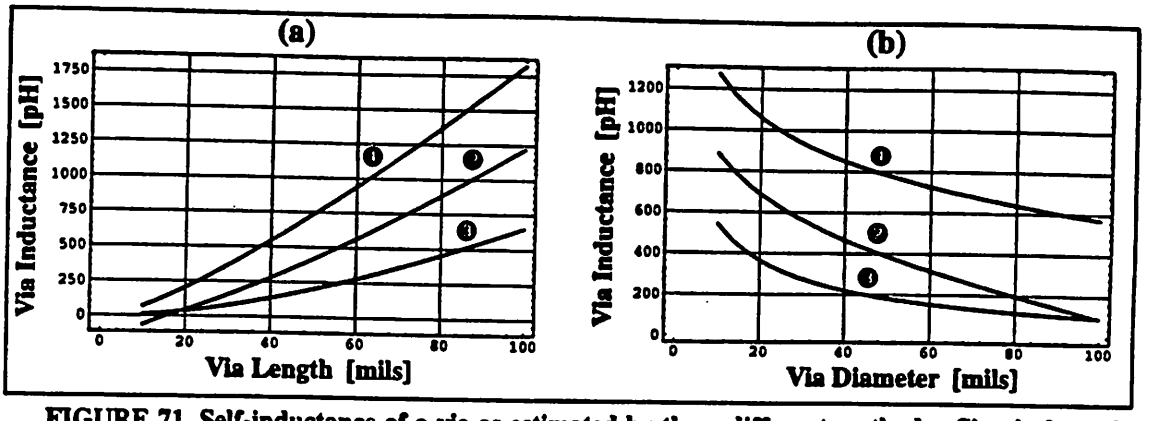


FIGURE 71. Self-inductance of a via as estimated by three different methods. Simple formula given by equation [72] (❶), using the relation for semi-empirical relation for the inductance of a cylinder (❷), and using a relatively complex semi-empirical via inductance equation (❸). (a) as a function of via length for a diameter of 30 mils, and (b) as a function of via diameter for a length of 60 mils.

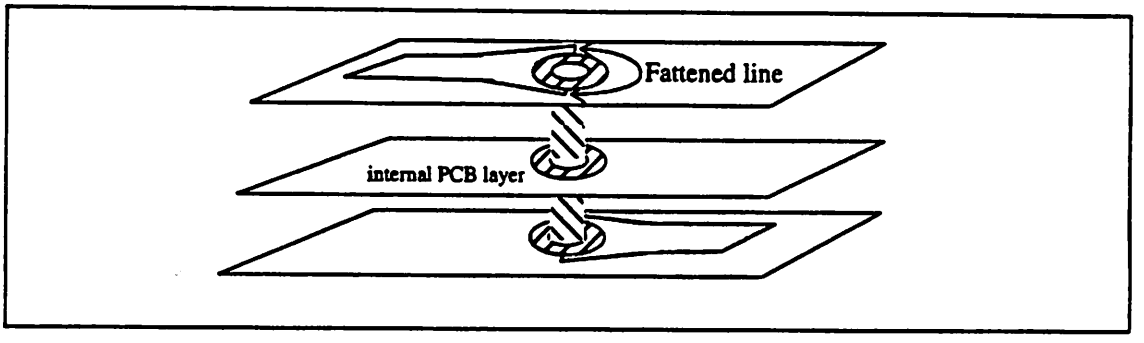


FIGURE 72. Fattened transmission lines may be used to compensate for the inductive behavior of a via on a transmission line in narrowband applications.

6.6.6.4 Difficulties of Designing Wideband Transmission Lines

Using equation [70] and equation [71] it is clear that shunt capacitive parasitics and series inductive parasitics on a transmission line can cause significant distortion in wideband RF and digital systems. There is much less of a distortion problem for narrowband RF systems due to these parasitics. In general, however, a high valued reflection coefficient in an RF application (even a narrow-band one) can cause the reduction of system SNR, cause instability problems for conditionally stable high-frequency amplifiers and change the transfer functions of high-Q filters by modifying their input and output impedances.

6.6.7 Time Domain vs. Frequency Domain Characterization of Transmission Lines

In the laboratory a transmission line can be cauterized using two methods, in the time - domain by using a time-domain reflectometer (TDR), or in the frequency domain by using a network analyzer. By using a network analyzer one can determine the characteristic impedance of the line at different frequencies using various display techniques (Smith Chart, log-magnitude, etc.). Using a simple network analyzer, however, it would be difficult to determine the physical causes attributing to discrepancies between the expected

characteristic impedance and the measured characteristic impedance. A TDR system, on the other hand, launches a very fast rise-time (100's of ps, typical) pulse into the transmission line and displays the time-domain response of the pulse on the screen. Using this method one can easily observe the effects of changes in the physical properties of the line (width, height, going through right angle curves, passing through a via, etc.) on the characteristic impedance of the line *exactly at the location where the perturbation of the line occurs* and therefore be able to pinpoint potential problems and their causes on the transmission line. Using equation [70] it is clear that the "step" function applied to the transmission line by a TDR system will cause a reflected inverted "impulse function" at the location of the capacitive load. Similarly, equation [71] indicates that the TDR step function would cause a non-inverted impulse function reflection when passing through a (inductive) via. If the rise-time of the incoming pulse is fast-enough and if the parasitic capacitance or inductance of the line is large enough, the magnitude (peak) of the reflected impulse may be used to estimate the amount of parasitic capacitance or inductance on the line. In general this kind of an estimate is much more valid when there is a single perturbation on the line. This is because multiple perturbations change the characteristics of the incoming TDR pulse. For example the transmission coefficient (= 1 - reflection coefficient) has a low-pass characteristic when the signal is transmitted through a capacitive load, and therefore any subsequent perturbation on the transmission line may observe an incoming pulse which has been distorted by a low-pass characteristic.

A network analyzer with an inverse FFT option is very useful in characterizing transmission lines. The inverse-FFT of the measured frequency-domain response is equivalent to the reflection response obtained from a TDR test set. If the TDR signal obtained by the inverse FFT option is showing multiple perturbations on the transmission line, one can *electronically* eliminate that portion of the transmission line in the time-domain response and subsequently observe the frequency-domain response of the line. By going back and forth between the time-domain and frequency-domain responses and performing multiple "what-if" analyses, the designer can exactly pinpoint the sources of the perturbations on the transmission line and their effect on the overall time and frequency responses of the transmission line.

6.6.8 Transmission Lines Referred to Power Planes (as Opposed to Ground Planes)

A question that frequently arises is whether it is allowable to use a power plane as the return path for a microstrip transmission line as opposed to a ground plane. The need for such transmission lines occurs for example in a four layer board where the second layer is a ground plane and th third layer is a power plane. Any microstrip transmission line routed on the fourth layer (solder side) will be referenced to the power plane. Ideally, as far as the (high frequency) transmission line signals are concerned, there is no difference between a ground plane and a power plane. Realistically, however, it is always best to use the same return path for the signals as they are referenced to, so that any noise on the reference would act as common mode and be rejected. For example, it is best to reference an incoming signal from an antenna to the same potential as the antenna "ground" which is usually signal ground (and hence use a ground layer underneath the microstrip transmission line connecting to the antenna). On the other hand it is best to reference a microstrip carrying the output signal of a resistively loaded common emitter amplifier to the supply.

The selection of a proper return signal path is much more critical in low noise applications such as the front end of a receiver. When the signal has a sufficiently large amplitude as compared to the noise levels on the power planes the problem is much less pronounced.

In a board with perfect supply bypassing, it would make no difference whether the signal is referenced to a supply or ground. The return signal will easily find a nearby bypass capacitor and flow through it to the proper layer and then propagate underneath the forward current (in order to minimize the loop area). In a four layer board, for example, the distributed capacitance between the power and ground plane (particularly if thickness of the dielectric between these layers is small) facilitates such transition.

If an RF signal propagating through a microstrip transmission line has to change layers through a via, it is important to provide the proper path for the return current as well. For example if the signal traverses from the component layer (layer 1) to the solder layer (layer 4) in a four layer board, the return signal will have to flow from layer 2 to layer 3. A local bypass capacitor near the via will provide such a return path (depending on the closeness of the internal layers to one another, the distributed plane capacitance may also provide such a transition path).

A similar situation arises when the forward signal on the stripline traverses the boundary between two partial power (or ground) planes which are on the *same* layer of a PC board. The situation is more complicated than the previous case in that no direct distributed capacitance exists between the two partial planes, and therefore local bypassing must be used (with a 0603 capacitor for example). One must be aware, however, that by using such a bypassing capacitor high frequency noise signals are now coupled between the two partial planes.

In either of the above scenarios, if a low impedance transition path does not exist for the return signal, the return signal will have to take a long inductive path. On a TDR system, this can be observed as a large positive going impulse-type blip. Further more, the large loop area enclosed by the current will cause a significant amount of radiation and cross talk.

6.6.9 Effects of Bias Stubs on Transmission Lines

Almost all active discrete RF components as well as some RF IC's require an external bias for the high frequency RF circuitry. If a pull-up, pull-down, or a combination of the two method of biasing is used, it is important to observe the following guidelines

1. If the biasing resistors are not intended to act as load terminations, one needs to assure that their equivalent resistance is significantly more than the characteristic impedance of the line, e.g. $(R_{b1} \parallel R_{b2}) \gg Z_0$ in FIGURE 73.a.

2. One needs to assure that the biasing stubs are very short as compared to the wavelength of the frequencies of interest. If there is a long distance between the power line and the transmission line, the bias elements should be kept as close as possible to the transmission line side and lengthened on the other side of the biasing resistors as shown in FIGURE 73.a. This effectively buffers the transmission line against being loaded by a

long stub. If $(R_{b1} \| R_{b2}) \gg Z_0$ and the biasing layout is similar to that shown in FIGURE 73.b, and the stub length approaches a quarter of the wavelength at the frequency of interest, the stub will act as an impedance transformer. The worst cases occur where the stub length is equal to an odd multiple of $\lambda / 4$, transforming the high impedance R_{b1} and R_{b2} into low impedances as seen at node ❶ and given by

$$Z_1 = Z_0 \| \frac{Z_0^2}{R_{b1}} \| \frac{Z_0^2}{R_{b2}} \qquad \text{(EQ 73)}$$

This will clearly attenuate the RF signal of interest. If the microstrip transmission line is intended for relatively narrowband signals (such as that in many RF applications), and if the frequencies of interest are large enough and board dimensions allow, one can intentionally provide a low impedance at nodes ❷ and ❸ by using C_1 and C_2 as shown in FIGURE 73.c. Now the low impedances at nodes ❷ and ❸ are transformed into a high impedance as seen at node ❶. Using this method it is not required for $(R_{b1} \| R_{b2}) \gg Z_0$ as long as $(1/\omega C_1) \ll R_{b1}$ and $(1/\omega C_2) \ll R_{b2}$.

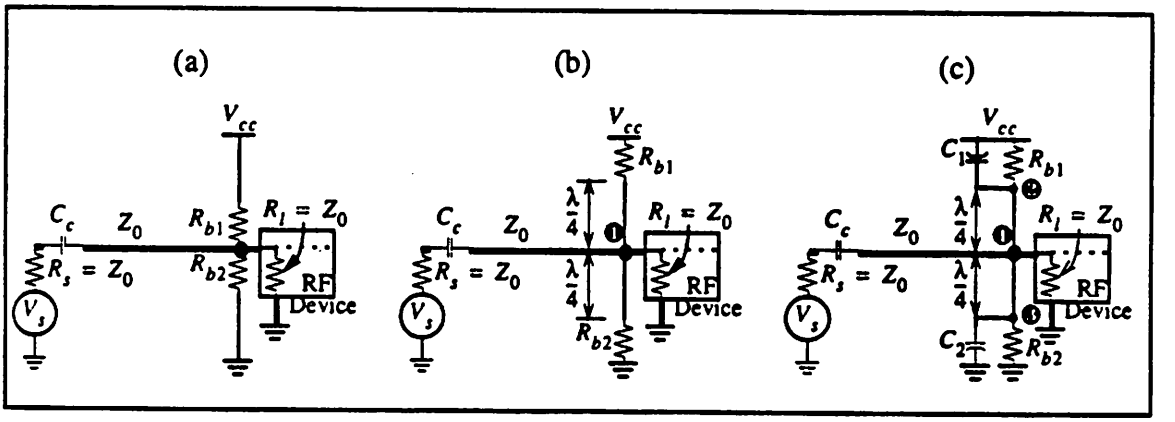


FIGURE 73. (a) Proper biasing of a transmission line assuming $(R_{b1} \| R_{b2}) \gg Z_0$ (b) Improper biasing of a transmission line assuming $(R_{b1} \| R_{b2}) \gg Z_0$. (c) One possible solution to the bias stub loading problem usable in narrowband applications.

6.6.10 Transmission Lines Used in This System

Many equations have been derived and reported for microstrip transmission lines. The simple relation given by equation [60] works well as a first order approximation but does not take into account many second order effects. It also does not give an accurate estimate for cases where $w \geq h_d$. One set of equations used in obtaining the characteristic impedance for this board are outlined in Appendix C, "Characteristic Impedance of Microstrip Transmission Lines". Since most transmission line equations which take second order effects into account are semi-empirically derived and do not exactly agree with one another, the average of two different methods were used to obtain the dimensions of the

transmission lines used on this board. The physical characteristics of the transmission lines used in the second version of the board are[1] .

$$
\begin{aligned}
w &= 26\text{mil} \\
t &= 2.8\text{mil (2oz copper)} \\
Z_0 &= 50\Omega \text{ (averaged over two methods)} \\
\frac{w}{h_d} &= 1.73 \\
\varepsilon_r &= 4.5 \\
\varepsilon_{eff} &= 3.37 \text{ (averaged over two methods)} \\
C &= 3.59 \text{ pF/in (averaged over two methods)} \\
L &= 9.07 \text{ nH/in (averaged over two methods)} \\
R_{dc} &= 9.36 \text{ m}\Omega\text{/in (return path resistance negligible)} \\
\text{attenuation} &\approx 0.026 \text{ dB/in (see table below)} \\
\frac{\partial Z_0}{\partial w} &= -1.10\Omega\text{/mil}
\end{aligned}
$$

(EQ 74)

In this system, with physical properties described in equation [74] and equations given in Appendix C, "Characteristic Impedance of Microstrip Transmission Lines", the R/L frequency is about 200KHz which is much below the RF carrier frequency and the transmission lines therefore operate well within the skin effect region. In this system, however, the distortion introduced across the bandwidth of interest, 872MHz to 904MHz is negligible even for the skin effect region of operation. Using equation [61], equation [62], equation [64], equation [65] and equation [66] the results of Table 5 are obtained for the ac resistance, phase shift, and attenuation at the band edges of interest.

1. SI is used throughout this report as the standard unit system. For discussion of PCB issues, however, the inch-based system has been used to conform to that industry's standards.

	@ 872MHz	@ 904MHz
AC Conductor Resistance [Ω/in]	0.111131	0.113138
Conductor Loss [dB/in]	0.004801	0.004888
Dielectric Loss [dB/in]	0.042935	0.044510
Total Loss [dB/in]	0.047736	0.049398
Ideal Phase Shift (linear) [Degree/in]	-56.64608	-58.72483
Phase Shift With Cond. Loss Only [Degree/in]	-56.64611	-58.72487
Phase Shift With Dielectric Loss Only [Degree/in]	-56.64891	-58.72777
Phase Shift With All Losses [Degree/in]	-56.64831	-58.72716

TABLE 5. Amplitude and phase distortion on the microstrip transmission lines used in this system at the band-edges of interest.

The results of Table 5 indicate the significance of dielectric losses in the microstrips used in this system as compared to the conductor losses. This fact can be partially attributed to the fact that the transmission lines used were composed of 2oz (2.8mil) copper with relatively large surface area and a low dc resistance. Furthermore, the dielectric layer was relatively thin resulting in a higher dielectric loss than a typical FR4 PCB microstrip. FIGURE 74.a compares the amplitude attenuation due to dielectric losses and conductor losses of the microstrips used in this system. FIGURE 74 also indicates that for most purposes the microstrip transmission lines used in this system can be assumed lossless and distortionless at the frequencies of interest.

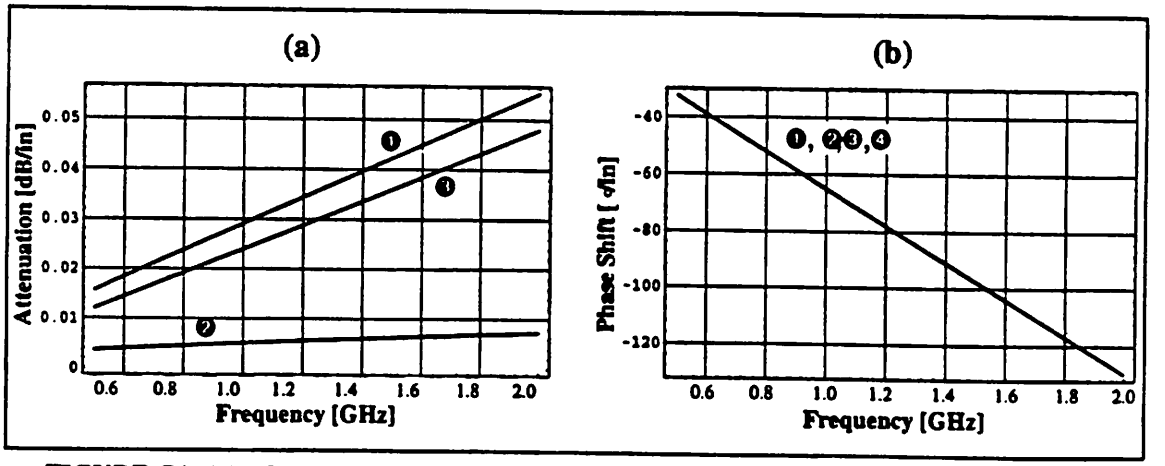


FIGURE 74. (a) Overall attenuation/inch vs. frequency (❶) in the microstrips used in this system, composed of conductor losses (❷) and dielectric losses (❸). (b) Phase linearity is preserved to a very high degree despite the conductor and dielectric losses. Curve (❹) represents a lossless, distortionless microstrip.

Stripline transmission lines behave reasonably distortionless as long as the bandwidth of interest is relatively narrow. In ultra-wideband applications such as wide-band radar systems, however, the distortion introduced by the transmission line should be seriously considered. Similarly, very-high speed digital circuitry utilizing transmission lines should also consider such effects since the harmonics of the signals of interest are typically several decades higher in frequency than the fundamental. The distortion introduced by the nonlinearities of the transmission line, for example, can generate intersymbol interference and the smoothening of the high-speed pulses in high speed digital communication systems.

6.6.10.1 Test Patterns on the First Board

A set of test patterns were imprinted on the first revision board for this system (FIGURE 75). Many of the conclusions of the previous sections were experimentally verified using these test pattern.

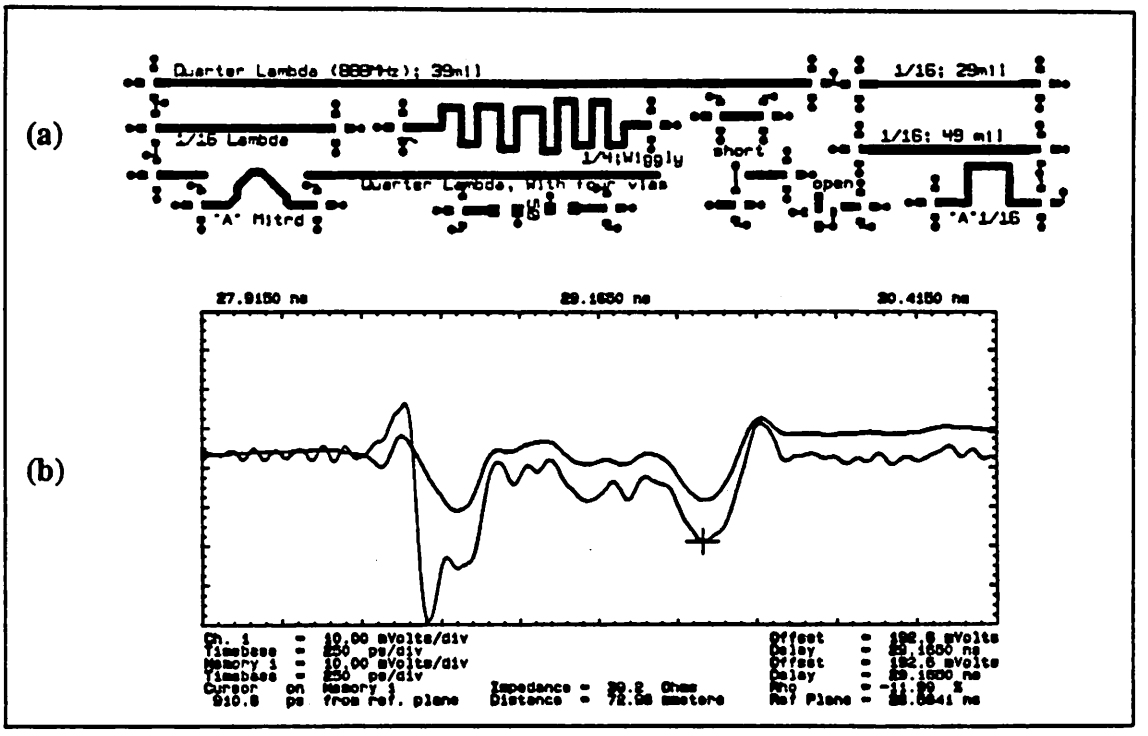


FIGURE 75. (a) Test patterns for investigating various microstrip effects, implemented on the first revision board of this system. (b) TDR response for a signal launched on the ("A" Mitr'd) of (a). The two curves correspond to two differnt rise times for the TDR input pulse. Note that in order to resolve small perturbations to the impedance of the transmission time very fast rise time stimulating pulses are required.

6.7 Some General Layout Rules of Thumb for RF Application

Many high sensitivity components require a partial ground plane immediately under them on the same layer as they are soldered on. These partial plane are connected to the main ground plane through multiple vias distributed around the plane. In the case of passive

elements such as filters this reduces the parasitic ground inductance thereby preserving the intended transfer function. For active components such as MMIC amplifiers this reduces the inductance on the ground pins of the package, thus reducing the danger of unwanted oscillation.

When very high levels of isolation is desired between two signals (e.g. diplexers, T/R switches, etc.) it is best to route the traces orthogonally to one another, minimizing field interaction and reducing mutual inductance between the lines. Furthermore, signals that require a high degree of isolation can be routed on the different sides of the ground plane. These measures can reduce the coupling by several tens of dB's.

It is important not to route high frequency or high sensitivity signals underneath the IC packages, as they can pickup and/or radiate unwanted signals. Because of relatively low conductivity, the IC substrate is not considered a good ground plane and cannot decouple the signals routed underneath a chip from the signals on the chip effectively.

6.8 Special Issues on PCB Layout for SAW Filters

SAW filters, as discussed previously, can offer a very sharp amplitude response, rejecting the nearby out of band signals by more than 60dB. The designer must pay very close attention to PCB layout issues in order to achieve such a high degree of isolation. In addition to following the good layout guidelines mentioned in Section 6.7, "Some General Layout Rules of Thumb for RF Application,", one must:

- Provide for a partial ground plane underneath the filter with many distributed vias connecting the partial plane to the main ground plane. The filter must be in direct contact with this partial plane, and if possible soldered to this plane at multiple points.
- A plated slit (or a double row of plated through holes) must be provided in the middle of the partial ground planes tieing these partial planes to the main board ground plane. The lack of such a slit can cause triple beat effects (Section 5.7.2.5.B, "Triple Transit in SAW Filters") on the output of the filter. This is because the electromagnetic signal which travels about 100,000 times faster than the acoustic signal can couple directly from input to the output in the absence of such a slit due to the dielectric leakage of the board material.
- Narrowband matching vs. broadband matching network. If impedance matching components are used external to the SAW filter, the output matching components must be placed on the PCB orthogonal to one another, and if possible hermetically shielded from one another. It would also be useful to place them on the opposite sides of the PCB so that the ground plane can provide the necessary isolation between them.

6.9 Shielding

6.9.1 Intuitive Explanation of Shielding

Enclosing high sensitivity/noisy components inside a metallic cage can provide significant EMI shielding in two ways. First, through reflective shielding. The effectiveness of this shielding is dependent in the type of the incident field (electric vs. magnetic vs. electromagnetic) and the wave impedance. Reflective shielding is most effective at the lower frequencies.

Second, shielding is provided by absorption. Absorptive shielding is independent of the type of the incident field: it behaves similarly in response to near or far, electric or magnetic fields. This type of shielding is most effective for higher frequencies.

Alternatively, the incident field can be thought of generating currents in the shield. These currents then generate fields apposing the incident field, thereby reducing the effect of the incident noise. The above qualitative statements are quantified and further justified below.

6.9.2 Magnetic Shielding vs. Electric Shielding

In general, a shield provides for different amounts of shielding for electric and magnetic fields, particularly in the near field. The overall effectiveness of a shield can be calculated simply by adding the reflective shielding and the absorptive shielding of the cage

$$S\,[\mathrm{dB}] = A\,[\mathrm{dB}] + R\,[\mathrm{dB}] \qquad \text{(EQ 75)}$$

In general, low frequency magnetic (inductive) fields are the most difficult to stop. Proper shielding of such signals requires the use of ferromagnetic material for the cage, which are typically more expensive and heavier than non-ferromagnetic material used for shielding. Furthermore, they typically do not offer as good of an isolation against electric and electromagnetic fields.

6.9.2.1 Low Frequency Magnetic Shielding

Since non-ferromagnetic shields provide little isolation against low frequency magnetic fields, the magnetic field penetrates through the shield. Part of the penetrated signal reflects multiple times inside the shield and part of the signal penetrates out. Because of all of these complicated and multiple reflections, penetrations and absorptions, equation [75] does not accurately model the shielding effectiveness against low frequency magnetic fields. See [20] for a thorough discussion of this subject.

6.9.3 Shielding Mechanisms

6.9.3.1 Absorptive Shielding

Absorption loss through a conductor increases exponentially with conductor thickness and is proportional to $e^{-d/\delta(\omega)}$ where d is the metal thickness and $\delta(\omega)$ is the skin depth of the

metal. $\delta(\omega)$ decreases with the square root of frequency, providing better isolation at higher frequencies. A similar argument can be made for magnetic and electromagnetic fields. It can easily be shown that thicker metals provide better absorptive isolation at a rate of about 8.7dB for each $\delta(\omega)$ of thickness.

FIGURE 76 displays the wave impedance as a function of the observation distance. Wave impedance is defined to be the ratio of the electric field to the magnetic field

$$Z_w = \frac{E}{H} \qquad \text{(EQ 76)}$$

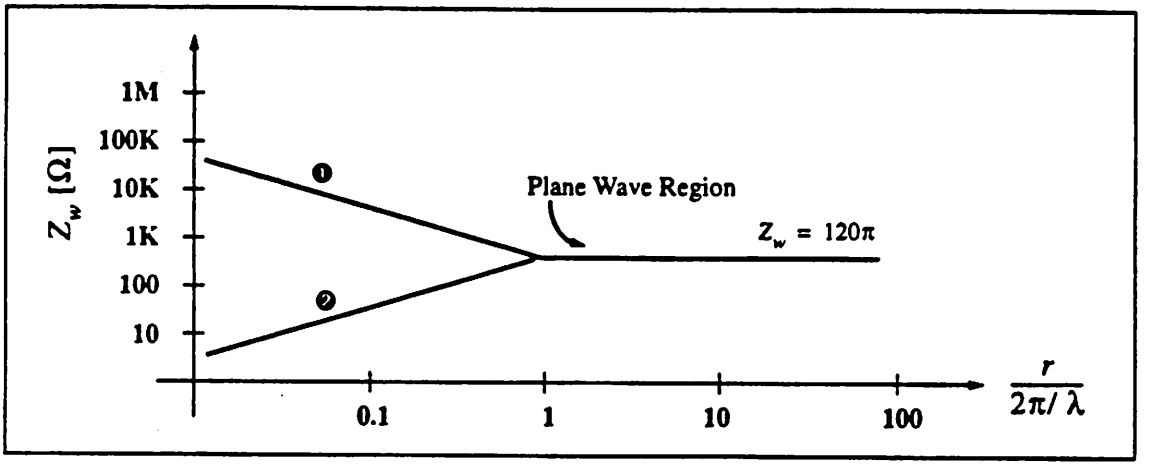


FIGURE 76. Wave impedance as a function of observation distance for a predominantly electric source (❶) such as a straight wire antenna, and a predominantly magnetic source (❷). In reality the wave impedance behaves in a complex manner at an observation distance of about $\lambda / 2\pi$. This behavior is not shown in this figure.

For near fields, the wave impedance is much higher for electric radiators than for magnetic radiators. The near field is defined to be the area enclosed by a sphere centered at the radiator (assuming the radiator can be modelled as a point source), with a radius equal to $\lambda / 2\pi$. In the near field the electric and magnetic fields behave very differently, where as sufficiently far enough from the source, they both behave as electromagnetic waves, with a wave impedance approaching 377Ω in free space. In the case of a 100KHz magnetic interfering source, for example, the magnetic field would dominate in a radial distance of 5m, in which the magnetic field attenuates by $1 / r^3$ and the electric field attenuates by $1 / r^2$, with a low wave impedance. As observed at a radial distance of greater than 5m, the wave behaves as an electromagnetic (plain) wave with the intrinsic impedance of free-space, 377Ω.

6.9.3.2 Reflective Shielding

The amount of reflective shielding offered by the cage is only a function of the incident wave impedance Z_w and the metal impedance Z_m and is given by [25]

$$R\,[\mathrm{dB}] = 20\log\frac{(Z_m + Z_w)^2}{4Z_m Z_w} \qquad \text{(EQ 77)}$$

Except for when we are dealing with a near-magnetic field, equation [77] simplifies to

$$R\,[\mathrm{dB}] = 20\log\frac{Z_w}{4Z_m} \qquad \text{(EQ 78)}$$

and therefore the reflective shield effectiveness is only a function of the ratio of the wave impedance to the metal impedance. From equation [77] and FIGURE 76 it is apparent that near-field magnetic fields are not easily prone to reflective shielding since Z_w and Z_m are comparable in magnitude. From the discussion on absorptive shielding we know that absorptive shielding is much more effective to high frequency radiators, and therefore does not offer much isolation against low frequency magnetic radiators. FIGURE 77 displays the shielding effectiveness and its components reflective and absorptive as a function of frequency for an *ideal* shield with no perturbations of the metal.

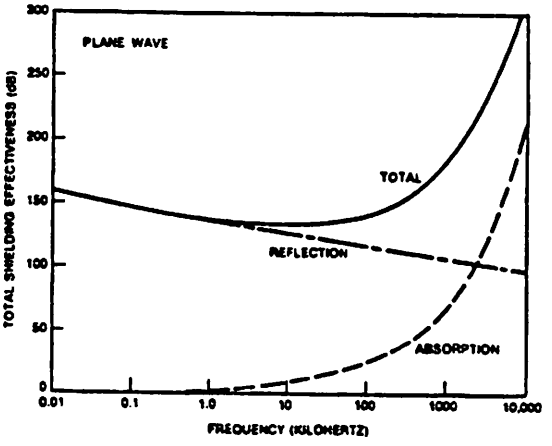


FIGURE 77. The reflective and absorptive components of the shielding mechanism as a function of frequency for an ideal (no seams or holes) 0.5mm copper in the plane-wave region (far-field) (after [20]).

Since equation [77] is completely symmetric with respect to Z_w and Z_m, the reflective shield should be effective whether $Z_w >> Z_m$ or $Z_m >> Z_w$. Since

$$Z_m = \sqrt{\frac{\omega\mu}{\sigma}} \qquad \text{(EQ 79)}$$

One can make an effective shield against low frequency magnetic radiators by using high permeability ferromagnetic material ("mu-metal") such as iron ($\mu >> 1$). Unfortunately such material do not offer as good of a shielding against other radiators since their Z_m is comparable to the wave impedance for such radiators.

6.9.4 Apertures and "Discontinuities" in Shields

In general, most metallic materials offer a very substantial amount of shielding against unwanted electric and magnetic signals (except low frequency magnetic as mentioned before). Apertures in the shield which are often required to route traces in and out of the shielded area or provided for tuning purposes are usually the main culprits in reducing the effect of shielding. Due to the lower wave impedance of magnetic fields in the near field, apertures in the shield affect the magnetic field leakage more than the electric field leakage.

The amount of leakage due to shield discontinuity depends primarily on the maximum linear dimension (not the area) of the opening, the wave impedance, and the frequency of the source. This can be intuitively explained as follows. As mentioned before, the incident field generates currents on the shield which in turn generate opposing fields to the incident field, resulting in the cancellation of the incident noise in a certain region. Any mechanism that perturbs the natural generation and flow of such currents would result in the reduction of the effectiveness of these currents in generating opposing fields. For example a shield with an aperture length equal to or greater than half a wave length offers no isolation to the incident field. Shorter apertures act as wave guides which are operating below their cutoff frequencies, and therefore attenuating the incoming signal. In this case the attenuation offered by the slitted shield is given by [25]

$$S_a = R_a + A_a \qquad \text{(EQ 80)}$$

where S_a is the total shielding, R_a is the reflection loss due to impedance discontinuity between the incident field and the *aperture*, and A_a is the attenuation of the incident field due to the operation below the cutoff frequency of the aperture (waveguide). If the source of the field is far from the shield as compared to the maximum linear dimension of the aperture, then the following approximate equations apply

$$R_a[\text{dB}] = 20\log\left\|\frac{(Z_a + Z_W)^2}{4Z_aZ_W}\right\| \qquad \text{(EQ 81)}$$

(note similarity of equation [81] to equation [77]) where Z_a is the aperture impedance and is given by

$$Z_a \approx \frac{j\omega\mu_0 l}{3.4}\ [\Omega] \qquad \text{(EQ 82)}$$

where l is the maximum linear dimension of the aperture and is expressed in meters. Note that for small l, $Z_a << Z_W$ for typical electric and electromagnetic fields. A large difference between the two impedances produces a large amount of attenuation of the incident field. As l increases, Z_a becomes comparable to Z_W which results in less attenuation of the incident field.

The "waveguide attenuation" of the incident field, A_a is approximately given by

$$A_a[\text{dB}] \approx 30\frac{t}{l} \qquad \text{(EQ 83)}$$

where t is the thickness of the shield. Note that splitting a 1cm slit into 4 0.25cm slits in a 2mm thick shield improves A_a by about 18dB.

Two comments are in place. First, both equation [82] and equation [83] are approximations. In reality both equation constants (3.4 in equation [82] and 30 in equation [83]) are a function of the geometry of the aperture. The equation constants stated here are averaged values for circular and rectangular apertures. Second, these equations do not apply to shield attenuation when the radiator is *inside* the shield and the distance between the source and the aperture is small as compared to l. In this case the equations become complicated. Although analytical equations exist for such cases, 3-D electromagnetic simulation or physical measurements will produce the most reliable results.

6.9.5 Shielding Provided in This System

On the second revision of this board, provisions have been made for the enclosement of the receiver and transmitter VCO's and some of their associated circuitry in a metal cage (Appendix G, "Artwork"). Minimum size apertures have been provided for signals to exit and enter the cage).

In some other parts of the board, partial ground planes and ground strips have been utilized to minimize cross-talk. As a rule-of-thumb, cross-talk between adjacent microstrip transmission lines is halved by placing a third grounded (at two ends) microstrip between the two lines, and halved again if the strip is grounded at multiple intermediate points.

Critical traces have been routed on the opposite side of the board when possible, shielded from each other through the internal power planes. Finally, critical signals on the same layer have been routed orthogonal to one another where possible in order to reduce the coupling of the fields.

7.0 Impedance Matching Issues

7.1 Impedance Matching for Optimal Noise Figure

At the RF frequencies, impedance matching is frequently used for several reasons. For example, a particular low noise amplifier, requires a unique optimal value for its source resistance in order to provide the lowest overall noise. This unique value is only a function of the input referred voltage of the LNA and its input referred current noise according to

$$R_{s_{opt}} = \sqrt{\frac{\overline{v_i^2}}{\overline{i_i^2}}} \qquad \text{(EQ 84)}$$

For example for MOS devices the required source resistance approaches infinite.

Since typically this value of R_s is different than the characteristic impedance of the line and/or the driving source resistance impedance matching can be used to provide this optimal source resistance to the low noise amplifier. It is important to account for any insertion loss in the impedance matching network. For example, high frequency baluns that may be used for impedance matching may have an insertion loss as much as 2 dB. This insertion loss will degrade the system NF significantly.

7.2 Impedance Matching for Maximum Power Transfer

At other times it is desirable to provide maximum power transfer to a load. This requires the source resistance to be equal to the load resistance (in the case of impedance, the load must be the complex conjugate value of the source for maximum power transfer, but a well designed system requires a *resistive* load equal to the characteristic impedance of the line any ways). Once again, impedance matching can be used to provide such a match. Unfortunately the source resistance required for maximum power transfer is usually different than that required for best NF performance, although often these values are sometimes close in magnitude. The reason for the difference in optimal source resistance for noise purposes and maximum power transfer is that an optimal maximum power transfer source resistance results in a noise gain / signal gain that is larger than that achieved by using an optimal NF source resistance.

7.3 Feedback for Impedance Matching

In typical implementation of LNA's feedback type-impedance matching is used at the input and output to reduce the system noise figure[1]. As compared to brute-force resistive matching, this can result in a significantly better noise figure. For example, in a fiber-optic preamplifier where the source resistance of the detector diode is high, the NF of a preamplifier implemented with a passive 50Ω input matching with a NF of 3 dB can be ideally reduced by approximately 1.25 dB to 1.75 dB through the use of a shunt-feedback input stage[2].

1. Resistive matching at the output stage of an LNA implemented in an integrated circuit fashion may be used in the case of multi-stage amplifiers. The effect of the added noise due to passive matching is reduced by the gain of the first stage(s) of the LNA.
2. Note that the NF is not reduced by 3 dB, but the current noise is reduced by 3 dB.

7.4 External Impedance Matching Requirements in This System

The LNA and the front-end mixer implemented in this system provide on-chip 50Ω matching. At the time of the design of this system, however, it was found that most commercial components were not geared towards large fractional bandwidths at the low IF frequencies (below 300 MHz). In the design of this system this was the primary area of need for the use of impedance matching schemes.

7.5 Impedance Matching of the Antenna

An impedance matching network is commonly needed at the antenna of a transceiver. The VSWR in such a case is determined by the matching of the *load* to the transmission line. In a receiver application, the load is the receiver input circuitry, and in a transmitter case the load is the antenna. Typically, optimal transmitter operation requires a maximum power transfer, and therefore the radiation resistance of the antenna should be matched to the output resistance of the transmitter for optimal power transfer to the antenna and matched to the free-space characteristic impedance for optimal power radiation into the medium. Typically optimal receiver operation requires the best NF match, and hence the radiation resistance of the antenna should be matched to a resistance determined by the ratio of noise voltage to noise current of the input receiver circuitry. For time division duplex systems where the same antenna is used for both transmission and reception, the matching circuitry are typically different.

In order to provide the match for a relatively narrowband system, a quarter wavelength transformer may be used. The characteristic impedance of the matching section is given by

$$Z_{\lambda/4} = \sqrt{Z_{ant} Z_0} \qquad \text{(EQ 85)}$$

where Z_0 is the characteristic impedance of the line to be matched as shown in FIGURE 78[1]. Note that Z_{ant} may be very difficult to obtain analytically and may require some measurements in order to obtain accurate values for Z_{ant}.

1. Clearly, this will reduce the gain (S_{21}) due to more reflections, but the loss in the noise gain is more significant than the loss in the signal gain, resulting in an improvement in system noise performance.

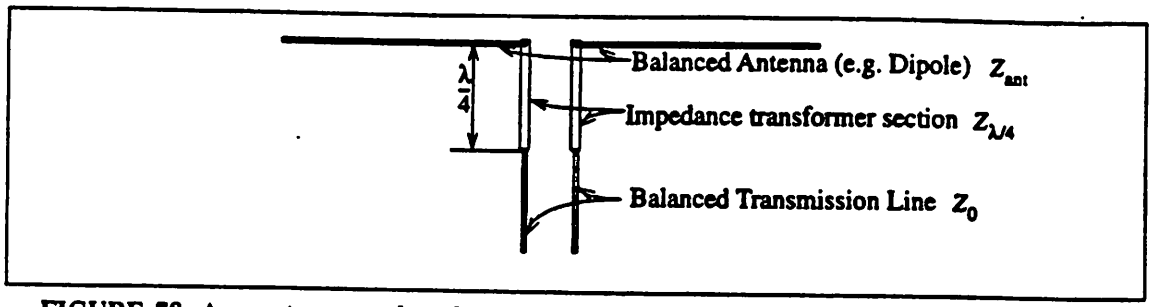


FIGURE 78. A quarter wave length section used to match the characteristic impedance of a balanced antenna to the characteristic impedance of a balanced transmission line.

7.5.1 Single Ended to Differential Conversion for Antenna Feed

Due to the additional noise when using a differential amplifier as compared to a single ended input, LNA's are commonly designed with a single ended (common emitter) input stage. Many transmitter power amplifiers are also designed with a single ended output stage. On the other hand, many antennas are symmetric with respect to the feed point (balanced). Further more, both microstrip lines and coaxial cables often used to drive antennas are not of the balanced form. In order to preserve the symmetrical feed to the antenna and avoid problems with radiation/pickup on the feeding transmission line, some method of power efficient single ended to differential (unbalanced to balanced) transformation must be used. This is commonly achieved by the use of a balun.

7.6 Passive Impedance Matching Networks

There are several common alternatives for impedance matching networks. Some of these methods which are applicable to frequencies of up to 2GHz are discussed in the following subsections. Wider bandwidth methods such as quarter wave transmission line transformers are not discussed here as they typically consume large areas for frequencies below 2GHz and are therefore not practical.

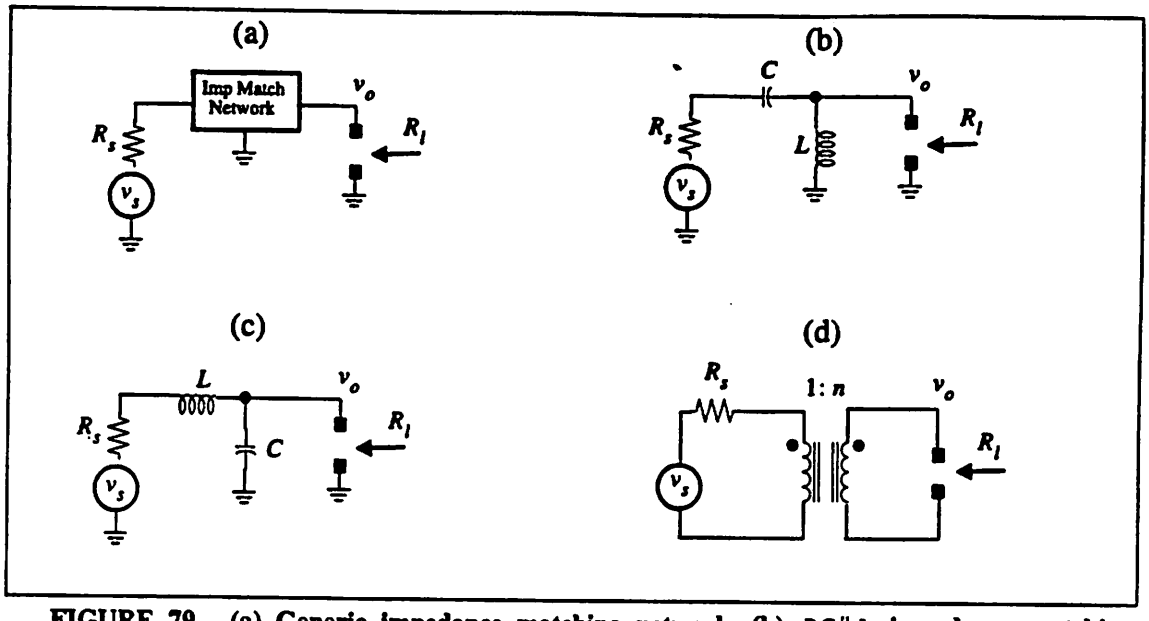


FIGURE 79. (a) Generic impedance matching network. (b) $RC \| L$ impedance matching network. (c) $RL \| C$ impedance matching network. (d) Transformer impedance matching network.

7.6.1 LC Networks

LC networks can be used effectively to satisfy impedance matching requirements. For narrowband applications in the IF stage, this method is the single most common method used for impedance matching. It is quite simple and provides a cost-effective means of performing this task. Because of the high-Q nature of single stage LC impedance matching networks, it is required to use multiple sections of LC networks in order to achieve a broadband matching networks (approximately fractional bandwidth of over 5%). As an example, in order to implement the impedance matching network required for the IF VGA output to the SAW filter input in this system, a 1500Ω to 50Ω impedance matching network would be required. If implemented in a maximally flat form with 0.1dB loss at the band edges (54MHz and 86MHz) this filter would require 8 reactive elements[1]. This usually becomes difficult to accomplish and the networks performance becomes highly dependent on the tolerance, SRF and Q of the elements. In general broadband LC matching networks require multiple sections and extensive tuning and are not a wise alternative.

FIGURE 79.c and FIGURE 79.d display two simple LC matching networks. The impedance matching element values for the network of FIGURE 79.b is given by

$$L = \frac{\sqrt{R_s R_l}}{\sqrt{R_l - R_s}\,\omega_0}, \quad C = \frac{1}{\sqrt{R_s (R_l - R_s)}\,\omega_0} \qquad \text{(EQ 86)}$$

1. If the band edges were allowed to have 3dB of attenuation, the impedance matching network could be implemented using a simple 2-element LC network.

where ω_0 is the center frequency of interest for the impedance transformation. The values of the matching elements for the network of FIGURE 79.c can be shown to be

$$L = \frac{\sqrt{R_l R_s - R_s^2}}{\omega_0}, \quad C = \frac{\sqrt{R_l - R_s}}{\sqrt{R_s} R_l \omega_0} \qquad \text{(EQ 87)}$$

From equation [86] and equation [87] it is clear that the networks can be used in this configuration for impedance matching only if $R_l \geq R_s$. Clearly the "inverted" networks can be used for impedance matching when $R_s \leq R_l$ is required.

Theoretically, only two reactive elements are required to match any two resistances in a narrow bandwidth. Even for narrowband applications however, the values of these reactive elements could be impractical. Three element reactive matching networks can then be used in order to overcome this problem, with one additional degree of freedom in the element values.

7.6.2 Transformers

Transformers are commonly used when a broadband match is required, both at RF and IF frequencies. Baluns (balanced-unbalanced), which are typically referred to transmission line transformers are most common at the high RF frequencies and/or where a very wideband response is required.

An ideal transformer preserves the power of the signal on its two sides and it is therefore very useful at the higher frequencies where power is the means of information transfer in the circuitry; it could be very effectively utilized to maximize power gain by presenting a source resistance equal to the load resistance.

7.6.2.1 Maximum Voltage Gain Obtained From a Transformer

In order to obtain a certain R_l as seen at the output (FIGURE 79.d), the turns ratio of the transformer should be selected as

$$n = \sqrt{\frac{R_s}{R_l}} \qquad \text{(EQ 88)}$$

It is interesting to note that equation [88] also satisfies the situation for maximum voltage gain as seen at the output (this can be easily shown by solving for n in $(dv_o / dn) = 0$). It can be shown that In passive impedance matching schemes, whether transformers or LC networks, the maximum achievable voltage gain (for n selected as equation [88]) is given by

$$v_o = \frac{v_o'}{2}\left(\sqrt{\frac{R_s}{R_l}} + \sqrt{\frac{R_l}{R_s}}\right) \qquad \text{(EQ 89)}$$

where v_o' is the output voltage obtained when the load resistance is connected to the source directly. equation [89] clearly indicates that under all circumstances $v_o \geq v_o'$ and using an impedance matching network always results in a higher gain. Using a passive matching network, it is possible to obtain *voltage* gain $v_o > v_s$ if $R_l > 4R_s$.

The same results apply to other forms of passive impedance matching networks.

7.6.2.2 Baluns

The frequency response of conventional wire wound transformers are typically limited by the resonance of the interwinding capacitance with the leakage inductance which could result in peaking in the passband response and roll-off at the higher frequencies. Baluns are transmission line transformers in which the interwinding capacitance is accounted for in the characteristic impedance of the transmission line through the physical arrangement of the turns. This could result in a very wideband frequency response. At the lower frequencies, the response is limited by the primary inductance. High permeability core material is often used to enhance the low-frequency response of baluns.

A balun is structured as shown in FIGURE 80. It is clear that unlike conventional coupling transformersm, a dc path exists between the input and the output.

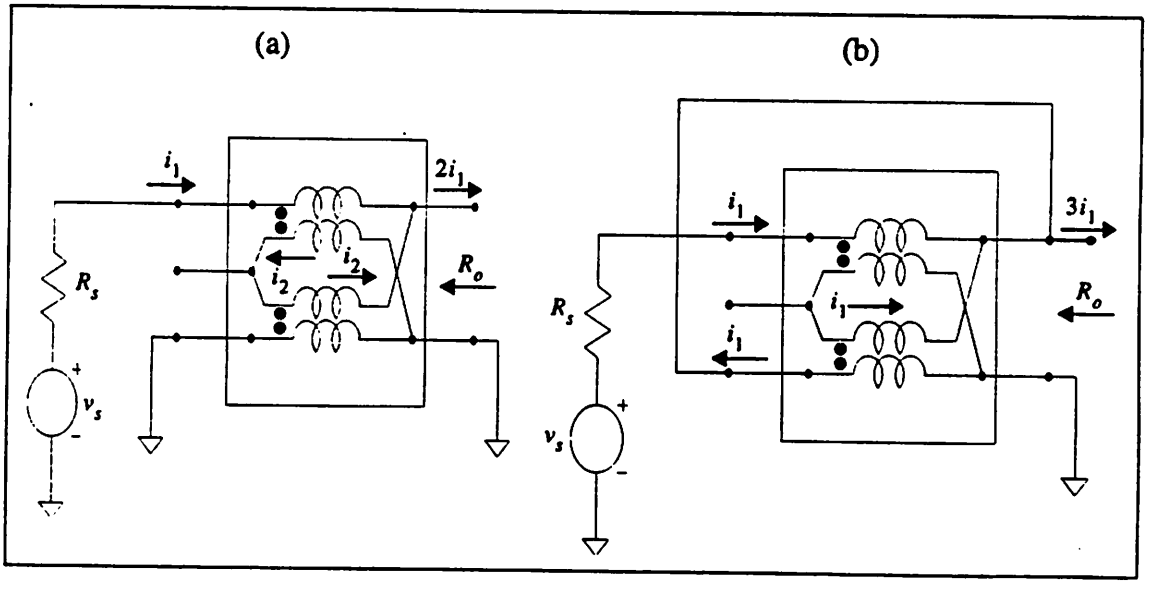


FIGURE 80. (a) A balun in a 4:1 impedance transformation configuration. and (b) 9:1 impedance transformation configuration.

Typical balun impedance transformation ratios are 2:1, 4:1, 8:1, 9:1, etc. The 4:1 impedance transformation in FIGURE 80 can be explained as follows. The current i_1 is input into the input of the balun. By transformer action, a current i_2 is produced which is equal in magnitude and 180° out of phase with i_1. The output current, therefore is equal to $2i_i$. Because of conservation of power in a transformer

$$i_1^2 R_s = (2i_1)^2 R_o \qquad \text{(EQ 90)}$$

which results in $R_o = 4R_s$. A similar arguement can be made for a balun in the configuration shown in FIGURE 80.b to show that $R_o = 9R_s$.

7.6.3 Resistive Networks

The simplest and most economical method of providing impedance matching is through the use of *PI* or *T* resistor networks as shown in FIGURE 81. The network can be designed to provide the desirable R_o and R_{in} given R_l and R_s along with an attenuation factor $v_o / v_1 = A_v$. It is important to note that for a given required input and output resistance, a minimum value of attenuation exists for which the network can be designed. If the attenuation is specified as less than this minimum, the resultant resistors can have negative values. The equations for resistive networks are algebraically complex. These equations are outlined in Appendix D for the *PI* network. The values of the elements for a *T* network can be calculated from the *PI* elements or directly.

These resistive networks can also be used as pads (attenuators). They can provide attenuation over an extremely broad bandwidth. The equations of Appendix D apply.

Due to the insertion loss of resistive networks, they are rarely used in the front stages of receivers for impedance matching purposes.

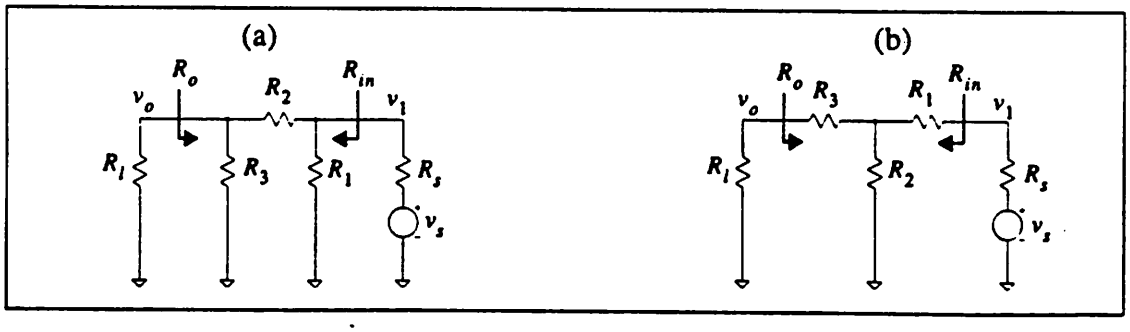


FIGURE 81. Resistive matching (and attenuation) networks. (a) *PI* configuration. (b) *T* configuration

7.7 Active Buffers as Impedance Matching Elements

Active buffers are another alternative in achieving impedance transformations. A high frequency amplifier (or opamp) in the unity gain configuration has a very high input impedance and a very low output impedance. A shunt resistor at the non inverting side can therefore provide the desired input match whereas a series resistor at the output can provide the proper output resistive match.

Active buffers, however, suffer from the same shortcomings as the active filters. They add noise to the system, worsen the systems distortion performance, and consume DC power. The distortion problem is more severe at the higher frequencies as the loop gain of the feedback amplifier starts to reduce. For the higher IF frequencies very high performance active buffers would be required.

7.8 Impedance Matching in This System

Impedance matching was used in several places in this system. In general, LC networks were ruled out for this system because of their narrowband characteristics.

7.8.1 The RF-Mixer VGA1 Interface

As explained in Section 5.1.2, "Impedance Matching to External Filters," the output of the front-end mixer is an open collector. In order to obtain the desired gain, this stage required a load resistance of approximately $1K\Omega$. The input of the first stage of the VGA presented a 400Ω load, and would therefore load down the voltage gain of the mixer. Broadband transformers could be used in this stage to improve the voltage gain of this stage, but this would add unnecessary complexity to the system and improve the voltage gain only by only a small factor. Using equation [88] and equation [89], $n_{opt} = 0.63$ and $v_o = 1.11 v_o'$. The added gain was not significant enough to justify the use of such a (custom) transformer. The reduced gain of the mixer was therefore accepted and accounted for in the system calculations.

7.8.2 THE RF-MIXER OUTPUT FILTER

A 1600Ω pull-up resistor was used at the output of the mixer (see Appendix F, "The Schematics"). A low order LC filter was placed between the two stages. This filter was designed for a source impedance of 1600Ω and a load impedance of 400Ω. Higher order filters could not be used here because of the required high value input and output impedances and the resulting high valued inductors and small valued capacitors (Section 5.7.2.1.F, "Frequency and Impedance Scaling in LC Filters").

7.8.3 VGA1-SAW-VGA2 Interface (Sensitivity of SAW Filters to Terminal

Impedance Mismatches)

After the first stage of the VGA, the signal is brought off chip for external filtering. The SAW filter is utilized at this stage. SAW filters are typically extremely sensitive to proper impedance matching. In an LC filter, if the filter is not properly terminated, this results in the movement of the location of the poles in the filter. Typically the center frequency of the filter does not vary as this is primarily a function of the L's and C's, but the ripple, the bandwidth, the stop-band rejection, and the insertion loss are all affected. This is in general true about SAW filters also. In either case if the termination is grossly off from the designed value, the filter output spectrum may not even look like a filter anymore. However, the SAW filters show much more sensitivity to terminal impedances. To investigate the sensitivity of SAW filters to input and output resistances, a test was performed. The test setup is shown in FIGURE 82. Analytical investigation of the sensitivity of these filters requires sophisticated CAD packages and is very difficult to do by hand.

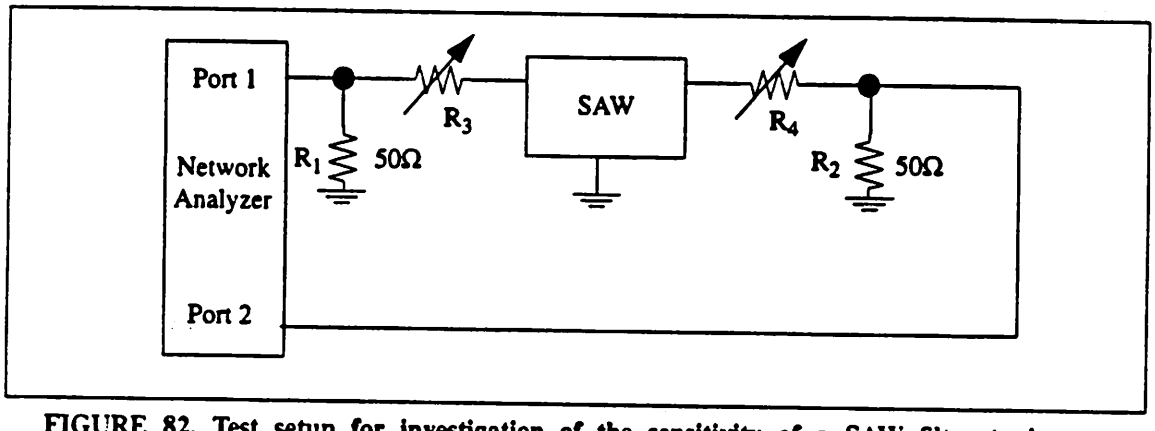


FIGURE 82. Test setup for investigation of the sensitivity of a SAW filter to improper terminations.

R_1 and R_2 make sure the network analyzer sees approximately 50Ω. For each measurement the network analyzer was calibrated with the SAW filter shorted out, and then the measurement was performed with that particular calibration. FIGURE 83 shows the results. The traces are the result of 16 running averages.

These results indicate that the effect of mismatch on input and output of this filter is to reduce the nice filter characteristics of SAWs (increase pass-band ripple, reduce attenuation of stop-band, increase insertion loss, etc.).

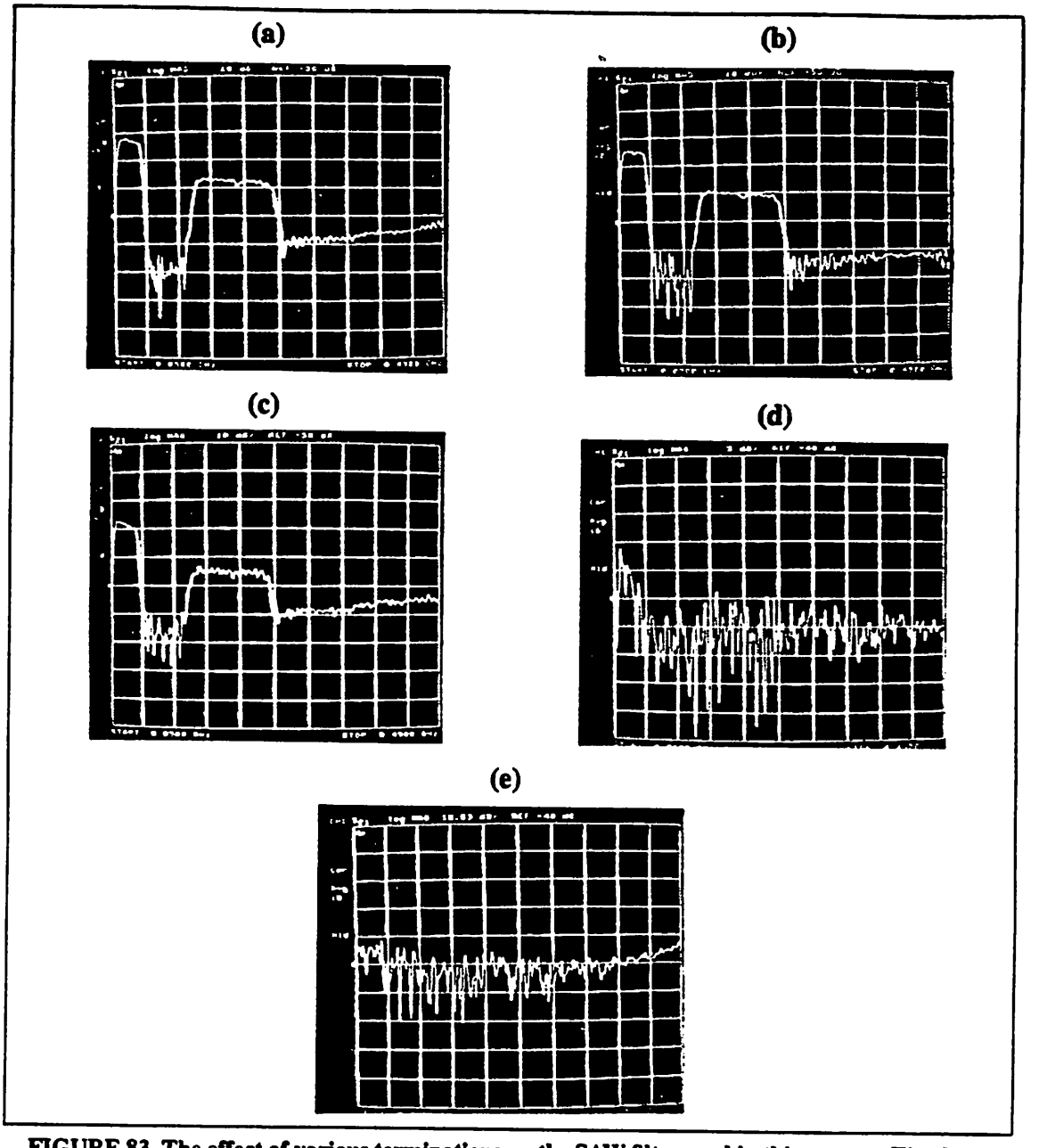


FIGURE 83. The effect of various terminations on the SAW filter used in this system. The device is specified for operation under 50Ω input and output termination. (a) R3=R4=25Ω (SAW sees Rin=Rout=50Ω) (b) R3=R4=75Ω (SAW sees Rin=Rout=100Ω) (c) R3=R4=175Ω (SAW sees Rin=Rout=200Ω) (d) R3=975Ω, R4=200Ω (SAW sees Rin=1KΩ, Rout=200Ω) (e) R3=R4=975Ω (SAW sees Rin=Rout=1KΩ)

Based on the plots presented above, in this system it was decided that a 100Ω input and output impedance would be acceptable while enabling the use of commercially available 16:1 (n= 4:1) transformers which transform the 1500Ω impedances of the IF amplifier to 94Ω. The IF amplifier was designed with a 1500Ω input and output impedance because this impedance level is what is typically required by *narrow-band* IF filters. At the time of

design of this board there were no commercially available IF VGA's providing low impedance input and output interstage characteristics.

Although difficult to quantify, it is estimated that an input and output impedance of about 300Ω presented to the SAW would cause significant degradation in this system's performance.

7.8.4 The Baseband Interfaces

Active buffers were used as the impedance transforming network at the baseband stages. Active buffers were selected for these stages instead of transformers because they satisfy other needs simultaneously while providing the proper impedance transformations. Furthermore, because of the lower frequency content at these stages, the use of active buffers becomes much more practical. Section 5.4, "The ADC Buffering and Filtering Stage".

8.0 Power Consumption Issues

Table 6 summarizes the power consumption of the various components used in the receiver part of this system. The table is broken down into two sections to illustrate how the power consumption of the ADC dominates the system power consumption. From Table 6.a, it is clear that most of the components used in the system consume an amount of power which is in the same order of magnitude as others (except for the ADC's). Most of these components operate on a single +5V supply. Some, however do require dual rail operation (the demodulator buffers for example). The board allows for these components

to be fed via an external -5V supply or by selecting the proper mode on the board, with an on-board switching regulator (see Appendix A, "Board Operation Details").

(a)

Part	P_{sup} (mW)
LNA/Mixer	65
IF VGA	60
Demod	30
RF Osc.	40
IF Osc.	50
Synthesizer	20
Demod Buffers	40
Buffer Loads	20
Others	20
TOTAL (-ADC)	345

(b)

Receiver A/D	P_{sup} (mW)
8 bits, 75MSPS (x2)	2000
8 bits, 50MSPS, Dual	770
6 bits, 77MSPS, (x2)	1400
10 bits, 20MSPS (x2)	70

TABLE 6. Details of receiver power consumption (a) excluding the ADC's. (b) Alternative commercially available ADC's. Note that the 10 bits, 20MSPS ADC's were in-house ADC's designed at UCB [26]. In all cases, power is stated for two ADC's, one for the *I* channel and one for the *Q* channel.

The power consumption for the transmitter components of this system are outlined in Table 7. If this board were to be used in an Infopad application, the power consumption of the wideband transmitter would be of little significance since it would be utilized in a (non-portable) base-station.

(a)

Part	P_{sup} (mW)
Modulator	120
Modulator Buffers	45
TOTAL (-DAC)	*165*

(b)

Transmitter DAC	P_{sup} (mW)
8bits, 40MSPS, Dual	165
6bits, 40MSPS, (x2)	160

TABLE 7. Breakdown of the power consumption of the transmitter part of the system. (a) Without DACs (b) Alternative DACs.

8.1 ADC Requirements and Relation to Power Consumption

This board can support an A/D converter with as high as 8 bits of resolution, and signals with a bandwidth as high as about 16MHz. If this board were to be used for CDMA applications at its fullest speed, it would require the A/D to operate at 64MSPS (16MHz base-

band bandwidth • 2 (anti-aliasing) • 2 (digital correlators require tchip/2 in order to be able to resolve early and late samples in the delay lock loop fine acquisition). Almost all commercially available A/D's operating at 8 bits with such a high bandwidth are of the flash architecture. Flash A/D's are notorious for high power consumption, particularly when the higher frequencies dictate the use of bipolar circuitry as opposed to CMOS. The bipolar flash ADC's often require dual rail supplies of ±5V. Furthermore flash ADC's present a very high input capacitance.

Table Table 6.b summarizes some of the ADC's that were investigated for use in this system. The ADC's that offer internal reference generation simplify the external circuitry considerably (see Appendix F, "The Schematics").

For lower speed applications, the board can be used with lower speed ADC's, reducing the power consumption significantly. The default anti-aliasing filters should be substituted by lower bandwidth filters to avoid excessive out of band noise.

The high power consumption of these ADC's results from several factors. First, they are primarily based on the flash architecture. Second, they have to drive external loads (off-chip) with the associated parasitic capacitance, which particularly at the higher speeds consumes considerable amount of power. An integrated solution, not only consumes less space, but it also reduces the power consumption of the ADC significantly.

Obviously a system with such high power consumption could not be utilized in a portable application (e.g. Infopad). Several steps are being taken so that the power consumption of the overall system in the final version of Infopad would be acceptable for a portable application. First, the possibility of analog correlators is being investigated (Section 8.1.2, "Power Consumption Issues Relating to the use Analog vs. Digital Correlators"). Second, in the digital correlator case, the integrated ADC would be driving small on-chip loads, and special measures are being undertaken to insure low power consumption [33]. Low power ADC converters have been successfully designed and implemented by other Berkeley students. For example "TC0001" offers 10 bits of resolution, 20MSPS, with 1pF single ended input capacitance, and only 35mW power consumption [26]. To achieve such low level of power consumption, a pipeline architecture has been utilized. This ADC, for example can be used with this system in applications where the full bandwidth of the receiver is not required.

8.1.1 Number of Bits of Resolution Required in this System

Another question of major significance is the number of bits of resolution which are actually required in the system. As mentioned before, this board can offer a high enough SNR and has the proper buffering amplifiers for an 8-bit application under certain conditions. The use of 8-bit ADC's at the required data rates is very power consuming. The system designer for the overall system will have to determine what the actual number of bits required are for the proper operation of the system and choose the proper ADC for that application. In traditional military use of spread-spectrum CDMA, where CDMA was only used to immune the signal to jamming (and not for multiple access) a one bit ADC (a comparator) would often suffice as the digitizing component of the system. This can be

intuitively attributed to the fact that a spread-spectrum signal has a *negative* SNR, and a high resolution ADC does not help much in digitizing such a signal. In multiple access CDMA systems, however, a higher number of bits of resolution is required. Simulations have shown that for 64 users in a system, the system would require approximately 4 bits of resolution [27]. The above reasoning assumes a digital correlator. In the analog correlator case the sampling rate required would be much lower, but the number of bits of resolution for the ADC would be higher.

8.1.2 Power Consumption Issues Relating to the use Analog vs. Digital Correlators

A direct-sequence spread-spectrum system is required to perform a correlation between the incoming signal and a a known sequence. This is initially required to lock to the correlation peak (coarse synchronization). Once lock is achieved, the transmitted signal can be properly despread.

The correlation (despreading) can be performed in the digital domain (traditional method) or in the analog domain[1]. In order for the correlator to operate in the digital domain, the analog incoming signal will have to be sampled at twice the chip rate (twice because of early and late samples for fine synchronization). Sampling at such high speeds requires considerable amount of power.

In an analog correlator approach, the despreading is performed before the signal is digitized. A correlator can be thought of as an integrator. A simple analog correlator then consists of a capacitor as the negative feedback element to a high gain stage. Unfortunately this approach does not perform well due to the amplifier noise and distortion. More importantly in portable applications, such a correlator does not yield a low-power solution.

The gain stage typically used for such a correlator is an operational transconductance amplifier (OTA). In this kind of an integrator, the settling time of the OTA is proportional to its transconductance and hence inversely proportional to the square root of the power. In other words, in order to double the speed of the integrator, the power consumption would have to be quadrupled.

A novel alternative approach is to use a sampled data FIR structure with "passive" integration [34]. In this approach, no OTA or active gain block is required and thus no DC power is consumed. Only dynamic power is consumed in order to clock the switches of the correlator.

1. The digital despreading can be performed using a true matched filter approach where coarse synchronization can be achieved much faster than a correlator approach at the expense of added circuitry and power consumption. The true-matched filter approach is commonly used in CDMA-TDMA systems where synchronization has to be achieved quickly every time the time slot is allocated to a certain user. True CDMA systems typically use a correlator approach for synchronization.

9.0 The Boards

9.1 The First Revision

The first version of the board is shown in FIGURE 84. This board was made of a test section on the edge (which was used for characterizing the controlled impedance lines, the effects of vias on controlled impedance lines, etc.), not shown in this figure. The main section of the board was composed of the receiver, the transmitter and the common front-end components (transmit/receive switch, "pre-select" filter, antenna diversity switch). The largest area on this board was consumed by the filters, the local oscillators and the dipswitches which provided the gain controls for the IF stage and the power down features for many of the ICs used. The antenna diversity and transmit/receive switches were controlled by connector 1 which was a 28 pin ribbon connector. Additionally, the supply voltage, ground, VCO tuning voltages, IQ modulator phase adjust voltage and other signals were provided by this connector. The high bandwidth I/O signals, I_{in}, Q_{in}, I_{out}, Q_{out} utilized an OSMT connector which connected to the outside world through a small-diameter coax cable.

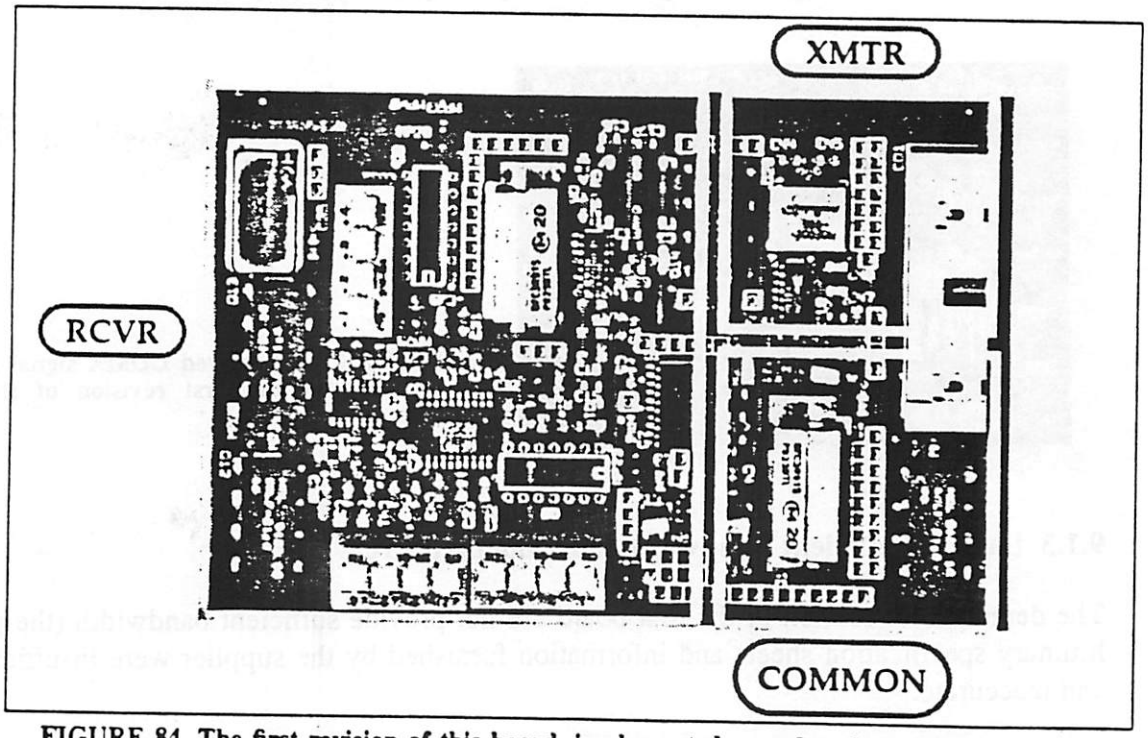


FIGURE 84. The first revision of this board, implemented on a four layer PCB. The board dimension, excluding the test structure, is 13.4cm X 7.6cm.

The main board dimensions are 13.4cm X 7.6cm, consuming an area of 102 cm^2. The board size could be reduced by eliminating the dipswitches which were provided for testability. The board had a total of less than 100 components. The standard surface mount capacitor and resistor used on the board were of the 1206 size. The elements were stuffed on the primary layer ("component") only.

9.1.1 Layer Stack-up

The board constituted four layers. Since vias were to be avoided (to avoid reflections on the line) for the controlled impedance lines, these lines were routed on the primary (component) layer only. The control signals were routed on the solder layer (fourth layer). The second layer was the ground plane and the third layer was the power plane. The dielectric material was FR4. Section 6.6.10, "Transmission Lines Used in This System". The power plane in parallel with the ground plane spaced approximately 30 mil apart provide for a relatively large high-frequency distributed capacitance ($C \approx 0.5\text{nF}$) which is effective in the supply decoupling process.

9.1.2 Transmitted and Received Signal

FIGURE 85 shows a received signal at the IF frequency of the first revision of the board. The signal was obtained by transmitting a BPSK modulated PN sequence through the transmitter section of one of these boards, and receiving it in another corner of the room by another one of these boards. On the receiver the signal is passed all the way through the receiving chain and is viewed on the spectrum analyzer at the IF frequency of 70MHz. The original transmitted signal had a chip rate of 16MCPS. An excess bandwidth of 100% is used here. On this figure, the spectrum analyzer span is set to is 33MHz.

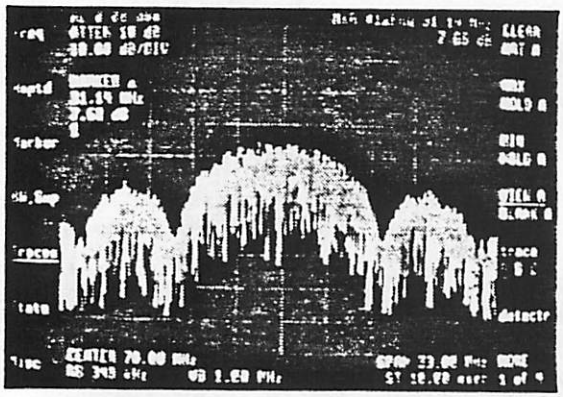


FIGURE 85. Received CDMA signal at IF stage of the first revision of this system.

9.1.3 Lack of Sufficient Bandwidth in Demodulator IC

The demodulator section of the first board did not provide sufficient bandwidth (the preliminary specification sheets and information furnished by the supplier were insufficient and inaccurate.

9.2 The Second Revision

After extensive investigations and characterizations on the first board, it was decided to implement a second board. The second board was to provide much more functionality and flexibility, while curing the shortcomings of the demodulator section of the first board and

some excessive transmitter/receiver cross-talk issues[1]. The second board provides the following additional features:

- Specified throughput requirements are met (no longer limited by the demodulator IC output section)
- Both AC and DC coupling options are provided for the modulator input ports
- Both phase locked and free-running VCO options are provided. In the phase locked case, the reference oscillator can be supplied externally, or the on-board reference crystal oscillators can be used. In the first version of the board, all VCO's were implemented as free-running. In the absence of extreme temperature variations (or when the signal BW of interest is small in comparison with the system filter bandwidths) the signal can be properly demodulated to some (varying) not-exactly-baseband frequency. The signal could then be completely demodulated to baseband with the use of a digital carrier recovery loop. This system would not work properly, however without some kind of feedback mechanism, digital or analog, to keep the received signal "close enough" to baseband.

  The phase-locked option will provide the feedback mechanism which is required to keep the baseband signal "close-enough" to true baseband. If both the transmitter VCO and the receiver VCO are locked to a stable crystal, the received baseband signal can be guaranteed to be within a "small" offset of baseband. In a differential modulation scheme, such as DQPSK used in the Infopad, as long as this offset is small as compared to the symbol rate, this would not cause for any problems, since the next symbol will arrive quickly enough such that the rotation in the constellation due to the frequency offset is insignificant. As a simplistic example, if the symbol rate were 1MSPS and the "baseband" signal were offset by 10KHz, the constellation rotation during one symbol would amount to 3.5° which is certainly tolerable in a differential QPSK system. Theoretically, a baseband offset of greater than 125KHz (45°) would be required in such a system to cause symbol errors. Clearly this is only a theoretical limit and practical and statistical considerations limit this offset to much smaller values. This is one of the odd occasions where a higher symbol rate simplifies the design of the system.

  The use of a phase locked system also compensates for long term frequency drifts in the VCO's due to effects such as temperature changes. In a non-phase-locked system this may cause the signal to be improperly truncated by the filters in the system.

1. In reality this cross-talk is not an issue, since in the final version of the Infopad the uplink channel (transmitter) is on a different frequency bandwidth. If this system were to be used in a time-duplexed fashion, however, the LO leakage of the transmitter to the receiver should be minimized. This is because typically it is not possible to shut-down the LO during the receive periods due to the relatively large "settling" time required for the LO. The transmitter modulator IC can typically be shut-down, however, which in conjunction with the T/R switch isolation should provide a significant amount of isolation to the LO. In such cases, the board layout becomes the dominant factor in determining the amount of LO leakage.

- Internal or external control of the VGA gain stages. The internal mode is primarily used for testing purposes. The external mode is used in conjunction with a gain control feedback loop. In a typical indoor environment, the frequency of the gain control updates is relatively slow as compared to an outdoor environment since the speed of the moving objects are low.
- Internal or external control of power downs on IC's. Most of the IC's used on this board have a "sleep" mode. In this mode the power consumption of these IC's is reduced significantly. Depending on the application this feature may or not be utilized. The internal control mode is primarily for testing purposes.
- The I_{in} and Q_{in} signals are fully buffered and level shifted to allow interfacing with various DACs. The I_{out} and Q_{out} signals are also fully buffered and level shifted to allow interfacing to various ADC's.
- The board can operate on a single +5V supply voltage. Although most components on this board require a 5V supply, the -5V required for the high speed opamps is provided by the use of on-board switching voltage supplies. An external -5V supply connector is also provided.
- All reference voltages are generated internally.

The result of the various enhancements mentioned in this section is a flexible transceiver board which can be utilized for various applications.

The pictures of the two sides of the board are shown in FIGURE 86.

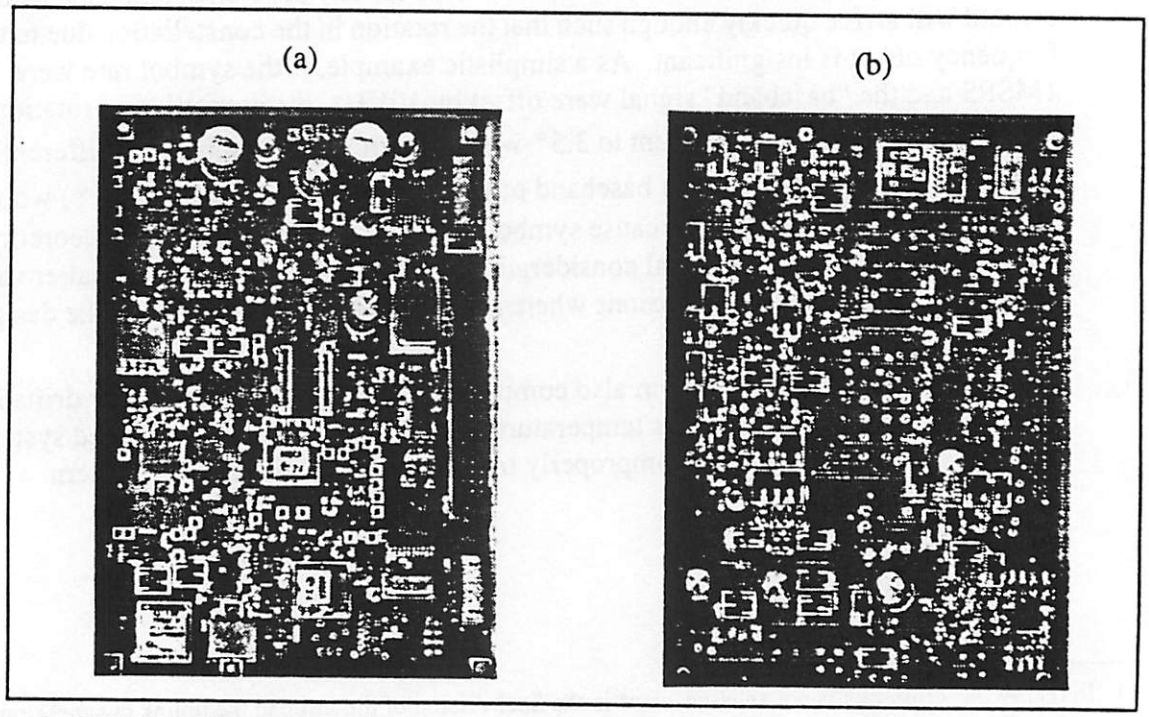


FIGURE 86. The second revision of the board. (a) component side. (b) solder side.

Appendices

APPENDIX A. Board Operation Details

A.1 Warnings

CAUTION: It is important to connect the $+V_{cc}$ and $-V_{ee}$ inputs properly. If they are swapped many components will be damaged. SMA Connector CON37 (the one closer to the middle of one side of the board is $+V_{cc}$ (+), and CON38, another SMA, closer to the edge of the board is $-V_{ee}$ (-).

Since the power is supplied to the board through an SMA connector, an SMA/banana converter cable must be used. Attention has to be made to the polarity on the banana side.

In order to provide maximum flexibility, many jumpers and switches have been provided on this board. This increased the risk of damaging the system by jumpering the wrong connector, etc. Therefore, at all times the user must be awarwe of the current meter reading on the power supplies. If a sudden surge in current consumption is observed, the power supplies must be shut down immediately. A better option is to use a power supply with automatic current limiting capability.

A.2 Important Notes

Loading: The loading of the components due to long cables and multiple connections to signal generators, spectrum analyzers, etc. should be considered. Most test equipment are 50 Ohms. The cable presents a rather large capacitive or inductive load that can alter the operation of the circuits if not properly terminated to 50Ω. For example, if a coax connector is used to observe the output of the VCO's in the synthesized mode, the synthesizer will not be able to operate properly, since it is loaded by the 50Ω input resistance of the spectrum analyzer in parallel with the 50Ω input impedance of the VCO and the impedance of the modulator/demodulator. In these cases the high frequency probe (HP), with 1MΩ input resistance, and 2pF capacitive load should be used to observe the signal.

Cables: The cables themselves can be very unreliable; especially the OSMT ones. It is best to check the proper operation of the cable *at the frequency of interest* before using the cable. The proper operation of these connectors at DC does not guarantee their proper operation at 1GHz.

Static Shielding: Some of the parts used on this board are *extremely* static sensitive (class A, i.e. 20V static can zap them, i.e. no internal static protection whatsoever). Always use proper grounded wrist strap.

HDR PINS: The header pins should not be arbitrarily disconnected. Furthermore, prior to the powering-up of a board *for the first time* (only), all the proper header pins must be in place. This is because power down has been provided for all the opamps on the board, by

disconnecting their V_{cc} line. If any significant voltage exists at any of the other pins of the opamp, the opamp can be destroyed. In general, the opamps should be "powered-down" with great caution. In other words, the opamp supply jumper headers should be connected under normal operation.

A.3 General notes

The following information simplifies the task of using/testing/debugging of this board:

1) the viewlogic schematics

2) this information section

3) the layout printouts generated by Racal for the component layer and the solder layer.

In general, the simplest method of locating a component in the layout is the use of the "component search" command in the layout program, Racal.

In order to design a new revision of this board, or if this method of schematic entry and capture is to be used for other designs (Viewlogic schematic entry, and Racal layout), the placement information should be entered in Racal (since Viewlogic does not give you placement information with this method). The following steps should be followed:

1. The file ~aryab/viewlogic/rinf.cfg should be used instead of the default configuration file.
2. After translating the netlist into Racal, a placement grid should be generated and activated.
3. The autoplace-distribute option should be used to randomly distribute the components on the grid.
4. The critical components should be placed and "fixed" in their place.
5. The autoplace-place command should be used. This gives an initial placentae which can then be modified as required.

A.3.1 Regarding the Synthesizers

There are various ways to program the synthesizers. One simple method that facilitates testing is the use of the following PC program installed on the PC in the Cory 403 lab.

C:\users\arya\lmx2315;

This program uses the serial port on the PC to communicate through the proper pins on the board connector *CON39* with the synthesizer. The proper cable is also built and in the lab.

A.3.2 Where to Find On-line Information

The viewlogic schematic of the current implementation is in:

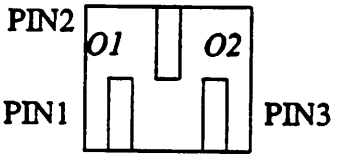
~aryab/viewlogic/xmtr.1

The Racal layout is in:

~aryab/Racal/work/nxcvr2-3

A.3.3 HDR PINS and Their Functions

Below is the information regarding all of the HDR-pins used on this board. The information has been broken down into transmitter (xmtr), receiver (rcvr) and common. The name of the header pin is typically followed by (2R), (3R), (2X) or (3X). In this context, *R* is rcvr, *X* is xmtr, 2 indicates a 2 pin header-pin, and 3 indicates a three pin header-pin. For three pin header-pins, the description follows the two states of the header pins *O1* and *O2*. This is marked on the schematics, but not on the board silkscreen. Here is the guide:



For the 2 pin header pins, state "1" indicates shorted (jumpered), and "0" indicates open (no jumper). In both cases "D" indicated the default state.

A.4 The Receiver

A.4.1 Header Pins

HDR1: (3R) Allows the option for selecting a free-running VCO for the receiver where the oscillation frequency of Q23 is determined by POT1, or a synthesized VCO, controlled by U1.

O1 (D):Synthesized

O2:Free-running

HDR9: (3R) Allows the use of an external power supply (through pin 10 of *CON39*) for the charge pump supply of the receiver synthesizer (U1). This feature could be useful to isolate the main board supply (Vcc) from the synthesizer charge pump noise injection.

O1: Use external supply

O2 (D):Use board Vcc

HDR10: (3R) Allows the use of an external reference (e.g. signal generator) through CON19 (OSMT connector) for the receiver synthesizer (U1). For compatibility with lab equipment (e.g. signal generator) there is a 50 Ohm termination on the board (R63).

O1: use external reference

O2 (D): use internal TCXO (Q9) for reference

HDR11: (3R) Allows the option of using an external -5V supply through SMA connector CON38 as opposed to using the internal DC-DC converter for this section (first stage of the receiver output buffer). This option is provided so that the user can eliminate the switching noise which is injected into the circuitry due to the DC-DC converter. HDR11 selects between DC-DC converter U6 and the external supply. Note that U6 feeds the negative supplies for the opamps U5 and U7. Also note that if an external Vee is used set HDR25=0 to power down U6.

O1 (D):Generate -5V for U5, U7 using U6

O2: Use external -5V supply

HDR12: (3R) Allows the option of using an external -5V supply through SMA connector CON38 as opposed to using the internal DC-DC converter for this section (first stage of the receiver output buffer). This option is provided so that the user can eliminate the switching noise which is injected into the circuitry due to the DC-DC converter. HDR12 selects between DC-DC converter U8 and the external supply. Note that U8 feeds the negative supplies for the opamps U19 and U17 as well as provides the negative supply for the class B output stage transistors (Q3,Q4) and (Q5,Q7).

O1 (D):Generate -5V U8

O2: Use external -5V supply

HDR13: (3R) Allows the option of using the same TCXO for both the transmitter and the receiver. In this mode both the transmitter and the receiver synthesizers will use the transmitter TCXO (Q10) as references.

O1: Both synthesizers use Q10

O2 (D): Each synthesizer uses its own local TCXO

HDR15: (2R) Powers down the receiver synthesizer (U1), receiver VCO (Q23) and the receiver free-running VCO control section by shutting down their voltage regulator, U4.

1:Shutdown

0(D):No shut-down

HDR16: (2R) Selects the operating frequency of the oscillator of the CMOS voltage (DC-DC) converter U6.

1:45KHz

0(D):10KHz

HDR17: (2R) Selects the operating frequency of the oscillator of the CMOS voltage (DC-DC) converter U8.

1:45KHz

0(D):10KHz

HDR23: (2R) Power down for receiver TCXO (Q9) by shutting down supply to its voltage regulator, Q16.

1 (D): ON

0:OFF

HDR24: (2R) Shuts down power to the on-board 140MHz IF 3rd overtone crystal oscillator by disconnecting its voltage regulator, Q13 from VCC.

1(D):ON

0:OFF

HDR25: (2R) Disconnects DC-DC converter U6 from power. If this mode is selected, an external -Vee must be supplied and proper selection be made on HDR11.

1(D):U6 ON

2:U6 OFF

HDR26: (2R) Disconnects Opamp U5 from Vcc. Note that powering down this opamp could be *dangerous*. Because, at all time the opamps must not see any voltage exceeding the supply voltages at non-supply pins. Since this opamp is fed from Q18 and also from voltage regulator Q14, the user MUST ensure that pins 2, 3 of this opamp (the inputs) are at about zero volts during the opamp shutdown (e.g. power down Q14 also, by setting HDR36=0). For complete shut-down, the HDR11 must also be open.

1(D):U5 connected to Vcc

2 (*dangerous*):U5 disconnected from Vcc

HDR27: (2R) Disconnects Opamp U7 from Vcc. Note that powering down this opamp is *dangerous*. Because, at all time the opamps must not see any voltage exceeding the supply voltages at non-supply pins. Since this opamp is fed from Q18 and also from voltage regulator Q14, the user MUST ensure that pins 2, 3 of this opamp (the inputs) are at about zero volts during the opamp shutdown (e.g. power down Q14 also, by setting HDR36=0). For complete shut-down, the HDR11 must also be open.

1(D):U7 connected to Vcc

2 (*dangerous*):U7 disconnected from Vcc

HDR28: (2R)Disconnects the quad opamp which generates the top of the ladder, bottom of the ladder reference voltages and also level shifts the main signals (U19) from the Vcc signal line. To shut down U19, HDR12 should be left open also (which shuts down the -Vcc supply to U19).

1 (D):U19 Vcc ON

2:U19 Vcc OFF

HDR29: (2R) Disconnects the Positive supply from the Vcc input of opamp U17. IN order to completely shut this opamp off, HDR12 must be left open also.

1 (D):U17 Vcc ON

2:U17 Vcc OFF

HDR35: (2R) Shut down option for 2.5V reference generator Q11 for the second stage of the rcvr output buffer. To avoid damage to U19, this HDR must be open if U19 is powered down.

1(D):Q11 ON

2:Q11 OFF

HDR36: (2R) Power down of Q14 voltage regulator by disconnecting its VCC connection.

1(D):Q14 ON

2:Q14 OFF

HDR37: (2R) Power down for the receiver synthesizer. This HDR is used as an extra "dipswitch."

1:Powered down

0 (D):Powered

A.4.2 POTS

POT1 (100K): Free-running RF VCO control option. The output of the VCO Q23 changes by about 11MHz/V by tuning it through this pot. Note that this tuning is also affected by the setting on the output of the voltage regulator U4. Assuming an output voltage of 4.2V on U4, and a desired LO frequency of 958MHz on the RF Mixer Q19 (this requires approximately. 1.95V on the control pin of the VCO):

Nominal Val:46.42K (2-3); approximately 1.782 Volts on the control line. Note that the connection of the voltmeter probes offsets the frequency slightly.

Adjustments:Adjust and observe output frequency of Q23 on spectrum analyzer. Set to 958 MHz, or whatever the desired LO frequency is.

POT2 (5K): Used to set the DC operating point of the *I* channel of I/Q receiver demodulator Q18 and also get 0V DC at the output of OPAMP U5. Note that this is not the standard way of utilizing this component, but necessary to enhance the output BW of Q18. Since R18=R17=2.5K (see schematic), both conditions (proper DC biasing of output stage of demodulator (Q18) AND 0V DC output of U6 can be satisfied simultaneously using this pot.

Nominal Val:2.5K (across pins 2-1 of pot)

Adjustments:Adjust such that the DC output voltage of U5 (pin 6) is zero.

POT3 (5K): Used to set the DC operating point of the *Q* channel of I/Q receiver demodulator Q18 and also get 0V DC at the output of OPAMP U7. Note that this is not the standard way of utilizing this component, but necessary to enhance the output BW of Q18. Since R19=R20=2.5K (see schematic), both conditions (proper DC biasing of output stage of demodulator (Q18) AND 0V DC output of U7 can be satisfied simultaneously using this pot.

Nominal Val:2.5K (across pins 3-1 of pot) (pinswap)

Adjustments:Adjust such that the DC output voltage of U7 (pin 6) is zero.

POT4 (1K):Adjusted such that output of LPF-I channel (FIL1) sees 50 Ohm. Since POT4 || POT7 is the resistance seen by the output of the filter, first POT7 should be adjusted to obtain the desired gain and swing for the particular A/D that will be utilized, and then POT4 adjusted such that POT4 || POT7 = 50 Ohms. Assuming POT7 adjusted to 100 Ohms,

Nominal Val:100 Ohms (across pins 1-2 of pot)

Adjustments: Adjust such that the resistance seen at FIL1 (pin 8) is 50 Ohms.

POT7 (1K):Adjusted to provide the top-of-the-ladder to the bottom-of-the-ladder swing (gain) for the particular type of A/D used on the *I* channel. Note that R23, the feedback resistor around opamp U17 is fixed at 634 Ohms since this is a trans-impedance (current-feedback) opamp. Assuming a 2Vp-p output required, and assuming an input swing of 0.312V at the output of FIL1-6,

Nominal Val:approximately 100 Ohms (across pins 1-2 of pot)

Adjustments: Adjust to get the proper gain (and swing) and observe U17, pin 7.

POT8 (10K): Used to set the reference (top-of-the-ladder or bottom-of-the-ladder) for the particular A/D's used. With the given configuration, this reference voltage can be -2.5V<Vref<+2.5V. If references in excess of these values are required, R21 will have to be swapped for a smaller resistance. These references are buffered using a class B discrete output stage to be able to provide high currents (this is required since typical high-speed flash A/D's have very low ladder resistances). Note that this reference voltage (available through OSMT connector CON3) can be used for both channels; or alternatively CON3 can be used for one channel and CON2 for the other. Often, the top-of-the-ladder or bottom-of-the-ladder is referenced to ground, in which case one reference output from this board will be sufficient. Otherwise, both reference. outputs can be used. Assuming a -2V reference output desired:

Nominal Val:9K (across pins 2-3 of pot)

Adjustments: Adjust to get the proper (DC) voltage at CON3, in this case -2V DC.

POT9 (10K): Used to set the proper output DC level on the main *I* signal output and main *Q* signal output for the particular A/D's used. Since there is no independent control for the two channels at this point, any small mismatch between the two channels must be compensated for using the DC adjusting pots of the previous buffer stage, POT2 (*I*) and POT3 (*Q*). Note that this pot is not referenced to ground, but to a -1.5V reference. Assuming a -1V DC at output of *Isig* (U17, pin 7) and *Qsig* (U17, pin 1) is required:

Nominal Val:9K (2-3)

Adjustments:Adjust to get the proper DC output voltage at U17, pin 7 and U17, pin 1 (in this case -1V DC); or can observe U19-12 and set it to the proper voltage, in this case +2V.

POT10 (10K): Used to set the reference (top-of-the-ladder or bottom-of-the-ladder) for the particular A/D's used. With the given configuration, this reference voltage can be -2.5V<Vref<+2.5V. If references in excess of these values are required, R31 will have to be swapped for a smaller resistance. These references are buffered using a class B discrete output stage to be able to provide high currents (this is required since typical high-speed flash A/D's have very low ladder resistances). Note that this reference voltage (available through OSMT connector CON2) can be used for both channels; or alternatively CON3 can be used for one channel and CON2 for the other. Often, the top-of-the-ladder or bottom-of-the-ladder is referenced to ground, in which case one reference output from this

board will be sufficient. Otherwise, both reference. outputs can be used. Assuming a -2V reference output desired:

Nominal Val:9K (across pins 2-3 of pot)

Adjustments: Adjust to get the proper (DC) voltage at CON2, in this case -2V DC.

POT11 (1K):Adjusted to provide the top-of-the-ladder to the bottom-of-the-ladder swing (gain) for the particular type of A/D used on the *Q* channel. Note that R23, the feedback resistor around opamp U17 is fixed at 634 Ohms since this is a trans-impedance (current-feedback) opamp. Assuming a 2Vp-p output required, and assuming an input swing of 0.312V at the output of FIL2, pin 6,

Nominal Val:approximately 100 Ohms (across pins 1-2 of pot)

Adjustments: Adjust to get the proper gain (and swing) and observe U17, pin 1.

POT19 (100K): Vout = (approximately) Vref (1 + POT19 / R11); Vref = 1.235V, R11=25K. As voltage regulator U4's output voltage is controlled by this pot, and since U4 control's Vcc of synthesizer U1 (which can operate as low as 3.5V Vcc, and it prefers the lower voltages), RF VCO Q23 (which has a nominal Vcc of 4.2V, but can operate up to 5V), and the free-running VCO control section, a reasonable setting for the POT is as follows:

Nominal Val:60K (across pins 1-2 of pot)

Adjustment:Adjust POT19 to achieve desired output voltage on U4, pin 1, nominally this voltage would be 5V.

POT20 (1K):Adjusted such that output of LPF-Q channel (FIL2) sees 50 Ohm. Since POT20 || POT11 is the resistance seen by the output of the filter, first POT11 should be adjusted to obtain the desired gain and swing for the particular A/D that will be utilized, and then POT20 adjusted such that POT20 || POT11 = 50 Ohms. Assuming POT11 adjusted to 100 Ohms,

Nominal Val:100 Ohms (across pins 1-2 of pot)

Adjustments: Adjust such that the resistance seen at FIL2, pin 8 is 50 Ohms.

A.5 Transmitter

A.5.1 Header Pins

HDR2: (3X) AC/DC coupling option for the input signals to the transmitter, *I* channel. For AC /DC coupling of the *I* channel all of the above setting must be made:

I channel:

AC:

HDR5 (3X): O1 (pinswap)

HDR20 (2X) = 1

HDR4 (3X): O1

DC:

HDR5: O2

HDR20=0

HDR4: O2

Q channel:

AC:

HDR2 (3X): O2

HDR18 (2X) = 1

HDR3 (3X): O1

DC:

HDR2: O1

HDR18=0

HDR3: O2

HDR3: AC/DC coupling. See "HDR2" above.

HDR4: AC/DC coupling. See "HDR2" above.

HDR5: AC/DC coupling. See "HDR2" above.

HDR6: (3R) Allows the use of an external power supply (through pin 15 of *CON39*) for the charge pump supply of the transmitter synthesizer (U2). This feature could be useful to isolate the main board supply (Vcc) from the synthesizer charge pump noise injection.

O1: use external supply

O2 (D):use board Vcc

HDR7: (3R) Allows the use of an external reference (e.g. signal generator) through CON6 (OSMT connector) for the transmitter synthesizer (U2). For compatibility with lab equipment (e.g. signal generator) there is a 50 Ohm termination on the board (R56).

O1: use external reference

O2 (D): use internal TCXO (Q10) for reference

HDR8: (3X) Allows the option of using an on-board pot (pot18) to set the attenuation of U13; or the use an external control voltage for the same purpose. The external control voltage is input through pin 35 of CON39

O1:External control

O2 (D):Internal control through POT18

HDR14: (3R) Allows the option for selecting a free-running VCO for the transmitter where the oscillation frequency of Q6 is determined by POT21, or a synthesized VCO, controlled by U2.

O1:Free-running

O2 (D):Synthesized

HDR18: AC/DC coupling. See "HDR2" above.

HDR19: (2R) Selects the operating frequency of the oscillator of the CMOS voltage (DC-DC) converter U10.

1:45KHz

0(D):10KHz

HDR20: AC/DC coupling. See "HDR2" above.

HDR21: (2X) Power down for transmitter TCXO (Q10) by shutting down supply to its voltage regulator, Q15.

1 (D): ON

0:OFF

HDR22: (2X) Powers down the RF attenuator by disconnecting it from Vcc. DANGER: in power down mode, make sure that HDR8 = 0 to avoid damage to part. No danger of damaging part at input pin (3) by powering down here because it is ac coupled and output of RF2402 is small.

1(D):ON

0:OFF

HDR30: (2R) Powers down the receiver synthesizer (U2), receiver RF VCO (Q6) and the receiver free-running RF VCO control section by shutting down their voltage regulator, U12.

1:Shutdown

0(D):No shut-down

HDR31: (3X) Allows the option of using an external -5V supply through SMA connector CON38 as opposed to using the internal DC-DC converter for this section (first stage of the receiver output buffer). This option is provided so that the user can eliminate the switching noise which is injected into the circuitry due to the DC-DC converter. HDR31 selects between DC-DC converter U10 and the external supply. Note that U10 feeds the negative supplies for the opamps U11 and U9. Also note that if an external Vee is used, HDR32 must be set to "0" (open) to power down U10.

O2 (D):Generate -5V for U9, U11 using U10

O1: Use external -5V supply

HDR32: (2X) Disconnects DC-DC converter U10 from power. If this mode is selected, an external -Vee must be supplied and proper selection be made on HDR31

1(D):U10 ON

0:U10 OFF

HDR33: (2X) Disconnects Opamp U11 from Vcc. Powering down this opamp is *dangerous* because, at all times the opamps must not see any voltage exceeding the supply voltages at non-supply pins. Since this opamp is fed from an input and also from reference generator Q12, the user *must* ensure that pins 2, 3 of this opamp (the inputs) are at about zero volts during the opamp shutdown. For complete shut-down, the HDR31 must also be open.

1(D):U11 connected to Vcc

0(dangerous):U11 disconnected from Vcc

HDR34: (2X) Disconnects Opamp U9 from Vcc. Note that powering down this opamp is *dangerous*. Because, at all time the opamps must not see any voltage exceeding the supply voltages at non-supply pins. Since this opamp is fed from an input and also from reference generator Q12, the user *must* ensure that pins 2, 3 of this opamp (the inputs) are at about zero volts during the opamp shutdown. For complete shut-down, the HDR31 must also be open.For complete shut-down, the HDR31 must also be open.

1(D):U9 connected to Vcc

0(*dangerous*):U9 disconnected from Vcc

A.5.2 POTS

POT5 (10K): Used to correct for phase mismatches between the *I* and *Q* channel. Usually not required except for "precision" applications.

Nominal Val: --

Adjustments: Adjust to cancel any phase mismatches.

POT6 (100K): Vout =(approximately) Vref (1 + POT6 / R80); Vref = 1.235V, R80=25K. As voltage regulator U12's output voltage is controlled by this pot, and since U12 control's Vcc of synthesizer U2 (which can operate as low as 3.5V Vcc, and it prefers the lower voltages), RF VCO Q6 (which has a nominal Vcc of 4.2V, but can operate up to 5V), and the free-running VCO control section, a reasonable setting for the POT is as follows:

Nominal Val:60K (across pins 1-2 of pot)

Adjustment:Adjust POT6 to achieve desired output voltage on U12, pin 1; nominally this voltage would be 4.2V.

POT12 (2K): This pot is used for offset voltage cancellation of U9 due to the unequal input bias currents. Should be adjusted such that (POT13 || (R58+R548)) = POT12 || POT 17. This POT should be adjusted *after* the adjustment of POT13.

Nominal Val:DC Coupling: --

AC Coupling: 830 Ohms

Adjustments:Adjust as noted above for offset voltage cancellation due to input bias currents.

POT13 (2K): Set the gain of the input buffered signal from the *Q* channel DAC. The gain should be adjusted for the proper swing at the input terminals of the modulator, U20. Note that especially in case of DC coupling the output voltage range of the opamps will dictate the max gain achievable, as these are relatively low; nominally +3.6V. Note that the swing on the input terminal of the modulator determines the output power of the modulated signal. POTs 12 and 17 will have to be adjusted after the adjustment of this POT. Assuming a 2V swing desired on the inputs of the modulator,

Nominal Val:665 Ohms

Adjustments: Observe U20-7 and adjust to obtain desired swing.

POT14 (2K): This pot is used for offset voltage cancellation of U11 due to the unequal input bias currents. Should be adjusted such that (POT15 || (R65+R54)) = POT14 || POT 16. This POT should be adjusted *after* the adjustment of POT15.

Nominal Val:DC Coupling: --

AC Coupling: 830 Ohms

Adjustments:Adjust as noted above for offset voltage cancellation due to input bias currents.

POT15 (2K): Set the gain of the input buffered signal from the *I* channel DAC. THe gain should be adjusted for the proper swing at the input terminals of the modulator, U20. Note that especially in case of DC coupling the output voltage range of the opamps will dictate the max gain achievable, as these are relatively low; nominally +3.6V. Note that the swing on the input terminal of the modulator determines the output power of the modulated signal. POTs 14 and 16 will have to be adjusted AFTER the adjustment of this POT. Assuming a 2V swing desired on the inputs of the modulator,

Nominal Val:665 Ohms

Adjustments: Observe U20-4 and adjust to obtain desired swing.

POT16 (2K): This POT should be adjusted *after* the adjustment of POT15.

In case of DC coupling: this pot is used to set the DC level of the signal to ideally such that we get 2.5V DC at the output of U11 so that there would be no offsets at the inputs of the 2701 input differential pair (*I*-signal). Nominally the output voltage range of CLC420 opamps is ±3.6 V, and for a 2V p-p swing this should be acceptable. However, worst case swing for the CLC420 is ±3.0 V, and therefore it may clip. In order to avoid this, the DC level may be set to for example 2V at the output of U11. The lower limit in this case is the acceptable DC range for RF2402 (U20) the modulator. If this is to be done, an extra pot must be "surgically inserted" between the output of the voltage reference Q12 and the Iref and Qref inputs of the modulator (Q20 pin 5, Q20 pin 6). This POT can be added in the board design and layout for any future revs. This POT will then be used to set the DC voltage at the reference inputs of RF2402 to the proper value (in this example +2V). Assuming a +2.5V DC desired at the output of U11:

Nominal Val:1.680K

Adjustments: Observe U11 (pin 6) and adjust for proper DC voltage. Alternatively, observe DC voltage across U20 (pin 4) and U20 (pin 3) and adjust to minimize offset (i.e set to 0V DC), this will maximize carrier rejection.

In case of AC coupling, if the front-end filtering and buffering is required; set such that the output DC voltage U11-6 is close to zero so that output signal swing can be maximized.

POT17 (2K): This POT should be adjusted *after* the adjustment of POT13.

In case of DC coupling: this pot is used to set the DC level of the signal to ideally such that we get 2.5V DC at the output of U9 so that there would be no offsets at the inputs of the 2701 input differential pair (Q-signal). Nominally the output voltage range of CLC420 opamps is +-3.6V, and for a 2V p-p swing this should be OK. However, worst case swing for the CLC420 is +-3.0V, and therefore it may clip. In order to avoid this, the DC level may be set to for example 2V at the output of U9. The lower limit in this case is the acceptable DC range for RF2402 (U20) the modulator. If this is to be done, an extra pot must be "surgically inserted" between the output of the voltage reference Q12 and the Iref and Qref inputs of the modulator (Q20 pin 5, Q20 pin 6). This POT can be added in the board design and layout for any future revs. This pot will then be used to set the DC voltage at the reference inputs of RF2402 to the proper value (in out example +2V). Assuming a +2.5V DC desired at the output of U11:

Adjustments: Observe U9-6 and adjust for proper DC voltage. Alternatively, observe DC voltage across U20-6 and U20-7 and adjust to minimize offset (i.e set to 0V DC)

In case of AC coupling (if the front-end filtering and buffering is required) set such that the output DC voltage U9-6 is close to zero so that output signal swing can be maximized.

Nominal Val:1.680K (across pins 1-2 of pot)

Adjustments:Observe U9 (pin 6) and adjust for OV DC.

POT18 (50K): Used to set the control voltage on the transmitter attenuator, U13 when in an internal control mode.

Nominal Val:--

Adjustments:Observe output signal of U13 (pin 7) and adjust POT18 to set to desired output level power.

POT21 (100K): Free-running RF VCO control option. The output of the VCO Q6 changes by about 11MHz/V by tuning it through this pot. Note that this tuning is also affected by the setting on the output of the voltage regulator U12. Assuming an output voltage of 4.2V on U12, and a desired LO frequency of 888MHz on the RF Mixer Q19 (this requires approximately. 2.5V on the control pin of the VCO):

Nominal Val:59.5K (across pins 2-3 of pot)

Adjustments:Adjust and observe output frequency of Q6 on spectrum analyzer. Set to 888MHz, or whatever the desired LO frequency is. The control voltage at this point should be around 2.485V, assuming the voltage regulator is set properly.

A.6 COMMON

A.6.1 Header Pins

HDR38: (2C) Disconnects all board LEDs (D1, D2, D3) from ground (open circuits) to save power. This option has been established because LEDs are high power consumption elements.

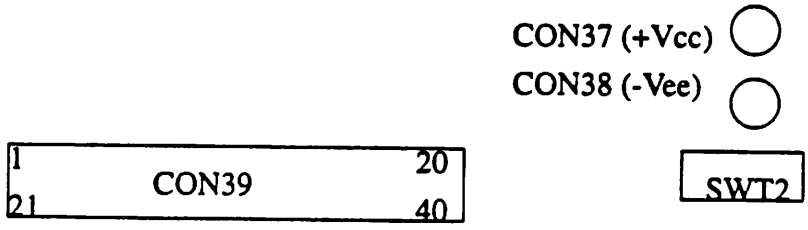
1:LED's active

2 (D):LED's deactivated

A.6.2 Connectors

CON39: (40-pin connector) Pinout information:

Pinout on the connector (other parts have been shown to indicate orientation of CON39):



1	GND
2	G1(Pins 2 through 8 are gain control pins for IF VGA)
3	G2
4	G4
5	G8A
6	G8B
7	G16
8	G32
9	GND

10	VP_RCVR(External charge pump supply for receiver synthesizer)
11	GND
12	ANTDIV_CNTRL
13	TR_CNTRL(External transmit/receive control)
14	GND
15	VP_XMTR(External charge pump supply for transmitter synthesizer)
16	X_TCXO_MOD(Transmitter TCXO modulation pin)
17	X_VCO_MOD(Transmitter VCO modulation pin)
18	X_MOD_PD(Transmitter modulator external power-down control)
19	PD_XMTR_SYNTH(Transmitter synthesizer external power-down control)
20	GND
21	GND
22	LE_R_SYNTH (blue on ribbon cable)
23	DATA_R_SYNTH (yellow on ribbon cable)
24	CLOCK_R_SYNTH (orange on ribbon cable)
25	GND
26	PD_IF
27	PD_DEMOD
28	PD_RCVR_SYNTH
29	LNA_ENABLE
30	GND
31	R_TCXO_MOD
32	R_VCO_MOD
33	DEMOD_REFIN(Receiver demodulator external reference voltage)

34	GND
35	ATTEN_CNTRL(Transmitter external attenuator voltage control)
36	GND
37	LE_X_SYNTH (blue on ribbon cable)
38	DATA_X_SYNTH (yellow on ribbon cable)
39	CLOCK_X_SYNTH (orange on ribbon cable)
40	GND

NOTES: • PD = Power Down

• R = Receiver

• X = Transmitter

• Pins 22, 23, 24 are used to program the receiver synthesizer. Pins 37, 38, 39 are used to program the transmitter synthesizer

• Pins 17, 18 can be used to investigate effects of phase noise on transmitter operation. Pins 31, 32 can be used to investigate effects of phase noise on receiver performance.

CON37: SMA Vcc and GROUND coax input. ***DANGER*** do not connect -Vee

voltage to this pin. This could damage many parts. Also note that the center connectro of the coax is Vcc and the braid is GND.

CON38: SMA -Vee and GND coax in. ***DANGER*** do not connect -Vee

voltage to this pin. This could damage many parts. Also note that the center connectro of the coax is -Vee and the braid is GND.

A.6.3 LEDs

(note LED's are disabled (CON38=0) or enabled (CON38=1).

D1-1:RED LED. If illuminated, Receiver synthesizer is *not* in lock.

D1-2:RED LED. If illuminated, XMTR synthesizer is *not* in lock.

D2: GREEN LED. If illuminated, Vcc is connected to board.

D3: ORANGE LED. If illuminated, external -Vee is being supplied.

A.6.4 Dipswitches

Used for internal on board controls.

SWT1 (7-segment DIP): Controls the gain of the VGA U18. ***NOTE*** For external control of the gain switches, all segments must be set to open circuit (OFF).

In the following, if the SWITCH is "ON" the gain is OFF.

1:	G1
2:	G2
3:	G4
4:	G8A
5:	G8B
6:	G16
7:	G32

SWT2: Used for on-board controls of power downs, antenna diversity selection, etc. *NOTE:* For external control through CON39, all dipswitches shold be in the OFF position.

1:	ANTDIV_CNTRL, ON: ANT1, through CON8; OFF: ANT2, through CON7
2:	TR_CNTRL, OFF: RCVR active ON: XMTR active
3:	X_MOD_PD, ON: Powered down (this provides about 50 dB of attenuation of the LO at the output port)
4:	PD_XMTR_SYNTH, ON: Powered down
5:	LNA_ENABLE, ON: Disabled
6:	PD_DEMOD,ON: Powered down

7: PD_IF, ON: Powered down

HDR37 (used as the eighth switch): HDR37=1 (i.e. jumpered)==> receiver synthesizer powered down (PD_RCVR_SYNTH)

APPENDIX B. Image Suppression Degradation Due to Amplitude Mismatches and Quadrature Phase Inaccuracies

The image suppression of the mixer can be obtained by obtaining the time-domain output of the non-ideal image suppression mixer and taking the Fast Fourier Transform of the output waveform. This method works well for obtaining the amount of image suppression due to specific values of non-idealities. In order to obtain a closed form solution, however, the method presented here is preferable.

The mixer image suppression can be solved in the most general form by considering all the variables of FIGURE 22 $\angle p_1$, $\angle p_2$, i_1, q_1, i_2 and q_2. In order to simplify the algebra, however, the following discussion assumes $\angle p_1 = 90°$ and $i_1 = q_1$ (the incoming signal is in perfect quadrature). Using FIGURE 22 the output of the image reject mixer is given by

$$v_{out} = q_2 \sin(\omega_1 t) \sin(\omega_2 t + p_2) \pm i_2 \cos(\omega_1 t) \sin(\omega_2 t) \qquad \text{(EQ 91)}$$

where the + would signify the suppression of the lower sideband and the - would result in the suppression of the upper sideband. Assuming that the upper sideband is the desired signal, equation [91] can be rewritten as

$$2v_{out} = [q_2 \cos(\Delta\omega t - p_2) - i_2 \sin(\Delta\omega t)] + [i_2 \sin(\omega_{1,2} t) - q_2 \cos(\omega_{1,2} t + p_2)] \qquad \text{(EQ 92)}$$

where $\Delta\omega = \omega_1 - \omega_2$ and $\omega_{1,2} = \omega_1 + \omega_2$. The power of the lower sideband can be calculated by integrating the square of the first part of the right side of equation [92] over one period

$$P_{LSB} = \Delta\omega \int_0^{\pi/\Delta\omega} [q_2 \cos(\Delta\omega t - p_2) - i_2 \sin(\Delta\omega t)]^2 dt \qquad \text{(EQ 93)}$$

which results in

$$P_{LSB} = k[i_2^2 + q_2^2 + 2 i_2 q_2 \sin(p_2)] \qquad \text{(EQ 94)}$$

where k is a constant.

Similarly, the power in the upper sideband can be calculated by integrating the square of the second part of the right side of equation [92] over one period

$$P_{USB} = \omega_{1,2} \int_0^{\pi/\omega_{1,2}} [i_2 \cos(\omega_{1,2}t - p_2) - q_2 \sin(\omega_{1,2}t)]^2 dt \qquad \text{(EQ 95)}$$

which results in

$$P_{USB} = k[i_2^2 + q_2^2 - 2i_2 q_2 \sin(p_2)] \qquad \text{(EQ 96)}$$

The normalized image suppression is given by dividing the image power by the power in the desired sideband. In terms of dB

$$R_{i,q,p} = 10 \log \frac{i_2^2 + q_2^2 + 2i_2 q_2 \sin(p_2)}{i_2^2 + q_2^2 - 2i_2 q_2 \sin(p_2)} \qquad \text{(EQ 97)}$$

equation [97] can be rewritten as

$$R_{G,p} = 10 \log\left(\frac{1 + G^2 + 2G \sin p}{1 + G^2 - 2G \sin p}\right) \qquad \text{(EQ 98)}$$

where $G = q_2 / i_2$ is the gain mismatch.

equation [38] can be derived using a similar method.

APPENDIX C. Characteristic Impedance of Microstrip Transmission Lines

The characteristic impedance of the microstrip lines used on this board were designed using an averaging of two different set of formulas. The results were verified using two computer aided design tools. Equation [99] through equation [102] ([35], [36]) outline of the two methods used for obtaining the physical characteristics of the microstrip lines.

The characteristic impedance of the microstrip can be calculated from

$$\begin{cases} Z_0 = \dfrac{\eta_0}{2\pi\sqrt{\varepsilon_{eff}}} \ln\left(8\dfrac{h_d}{w'} + \dfrac{w'}{4h_d}\right), & \text{if } \left(\dfrac{w}{h_d} \le 1\right) \\ Z_0 = \dfrac{\eta_0}{\sqrt{\varepsilon_{eff}}}\left[\dfrac{w'}{h_d} + 1.393 + 0.667\ln\left(\dfrac{w'}{h_d} + 1.444\right)\right]^{-1}, & \text{if } \left(\dfrac{w}{h_d} \ge 1\right) \end{cases}$$

(EQ 99)

where w and h_d are as given in FIGURE 67.b. The constant $\eta_0 = 120\pi$ is the intrinsic impedance of free space. The ratio w' / h_d is used instead of w / h_d in order to account for the effect of the finite thickness of the copper line, h_c, and is given by

$$\begin{cases} \dfrac{w'}{h_d} = \dfrac{w}{h_d} + \dfrac{1.25}{\pi}\dfrac{h_c}{h_d}\left(1 + \ln\dfrac{4\pi w}{h_c}\right), & \text{for } \left(\dfrac{w}{h_d} \le \dfrac{1}{2\pi}\right) \\ \dfrac{w'}{h_d} = \dfrac{w}{h_d} + \dfrac{1.25}{\pi}\dfrac{h_c}{h_d}\left(1 + \ln\dfrac{2h_d}{h_c}\right), & \text{for } \left(\dfrac{w}{h_d} \ge \dfrac{1}{2\pi}\right) \end{cases}$$

(EQ 100)

The variable ε_{eff} is used instead of $\varepsilon = \varepsilon_r\varepsilon_0$ in order to account for the fact that some of the field is not contained in the (FR4) dielectric, but it is formed in the air ($\varepsilon_r \approx 1$) and is given by

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} F\left(\frac{w}{h_d}\right) - \left(\frac{\varepsilon_r - 1}{4.6}\right)\frac{h_c / h_d}{\sqrt{w / h_d}} \qquad \text{(EQ 101)}$$

where

$$\begin{cases} F\left(\frac{w}{h_d}\right) = \left(1 + 12\frac{h_d}{w}\right)^{-0.5} + 0.04\left(1 - \frac{w}{h_d}\right)^2 & \text{for } (w/h_d) \le 1 \\ F\left(\frac{w}{h_d}\right) = \left(1 + 12\frac{h_d}{w}\right)^{-0.5} & \text{for } (w/h_d) \ge 1 \end{cases}$$

(EQ 102)

APPENDIX D. Pi Attenuator/Matching-Network Equations

The relations for the PI attenuator/impedance matching network of FIGURE 81.a is presented here. The *Mathematica* program was used to solve for the three unknown resistor values given the voltage attenuation factor, the source and load resistance, and the desired input and output resistance. The equations for the T network can be calculated in a similar way, or the resistor values for the T network can be calculated from the PI to T transformation rules.

D.1 The mathematica code

```
par[R1_,R2_] := R1 R2 / (R1 + R2)

f=Solve[{

Rin==par[(par[Rl,R3]+R2),R1],

Ro==par[R3,(R2+par[Rs,R1])],

Av== par[Rl,R3]/(par[Rl,R3]+R2)},

{R1,R2,R3}]

r1=R1/.f;

r2=R2/.f;

r3=R3/.f;
```

D.2 The Results

$$R_1 = \frac{R_{in}(R_{in}R_lR_o - A_V^2R_{in}R_lR_s - A_v^2R_{in}R_oR_s + R_lR_oR_s)}{-A_vR_{in}^2R_l + A_v^2R_{in}^2R_l - A_vR_{in}^2R_o + A_v^2R_{in}^2R_o + R_{in}R_lR_o - A_vR_{in}R_lR_s - A_vR_{in}R_oR_s + R_lR_oR_s} \quad \text{(EQ 103)}$$

$$R_2 = \frac{R_{in}R_lR_o - A_v^2R_{in}R_lR_s - A_v^2R_{in}R_oR_s + R_lR_oR_s}{A_v(R_{in}R_l + R_{in}R_o + R_lR_s + R_oR_s)} \quad \text{(EQ 104)}$$

$$R_3 = \frac{R_l(-R_{in}R_lR_o + A_v^2R_{in}R_lR_s + A_v^2R_{in}R_oR_s - R_lR_oR_s)}{-R_{in}R_l^2 + A_vR_{in}R_l^2 + A_vR_{in}R_lR_o - A_v^2R_{in}R_lR_s - R_l^2R_s + A_vR_l^2R_s - A_v^2R_{in}R_oR_s + A_vR_lR_oR_s} \quad \text{(EQ 105)}$$

APPENDIX E. Via Inductance Relations

Mathematica was used to plot the via inductance relations of FIGURE 71. The relations are given in the *Mathematica* script below.

L_1 uses the inductance of a cylinder to estimate the inductance of a via. The variable *lnsig* is the ln of a best fit factor, *sig*, used in estimating L_1 [28].

L_2 is a relatively complex semi-empirical relation for estimating the inductance of a via [29].

L_3 is a very simple relation for estimating the inductance of a via [21]. It's results are typically on the pessimistic side (too large).

via.ma 1

```
In[109]:=
  lmil=60;
In[103]:=
  d2mil=30;
In[39]:=
  r2mil:=d2mil/2
In[40]:=
  r1mil:=r2mil+1
In[41]:=
  l:= lmil*0.0025
In[42]:=
  r1:=r1mil*0.0025
In[43]:=
  r2:=r2mil*0.0025
In[66]:=
  mu0 = Pi/2500000;
In[71]:=
  h := lmil*0.000025
In[72]:=
  r := (d2mil*0.000025)/2
In[95]:=
  L1 := 10^6 0.002*l*Log[(2*l)/r1 + lnsig - 1]
In[120]:=
  lnsig := 0.25009128 - 0.0017049618*(r2/r1) -
  0.51598981*(r2/r1)^2 +   0.37420782*(r2/r1)^3 -
  0.10669571*(r2/r1)^4

In[93]:=
  L2 :=10 ^ 12 (mu0*(h*Log[(h + Sqrt[r*r + h*h])/r] +
   1.5*(r - Sqrt[r*r + h*h])))/(2*Pi)
In[98]:=
  L3:=1000 * 5.08*lmil*0.001* (Log[(4*lmil/d2mil)]+1)
```

APPENDIX F. The Schematics

F.1 General Information

The schematics of the transceiver board is presented in two forms in this appendix. First, the "hierarchical" representation which was *manually* generated from the flat original schematic for documentation purposes only. The actual schematics from which the artwork (layout) was generated is shown in Section F.1.2, "Flat".

F.1.1 "Hierarchical"

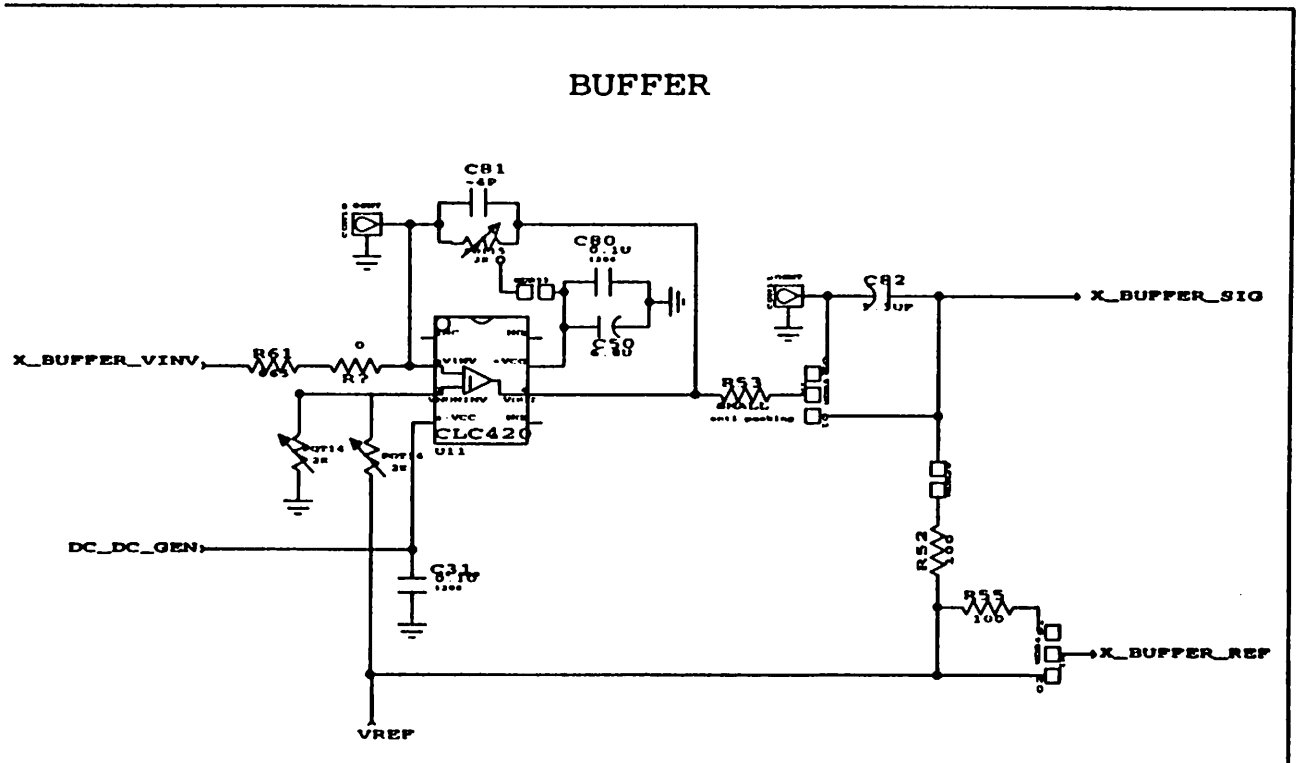
This section presents the flattened version of the "hierarchical" schematics of this board. Flattening of the schematics is essential for back-annotation of the reference designators. The schematics presented in this section are intended to simplify the understanding of the operation of this board by presenting the schematics in modular blocks.

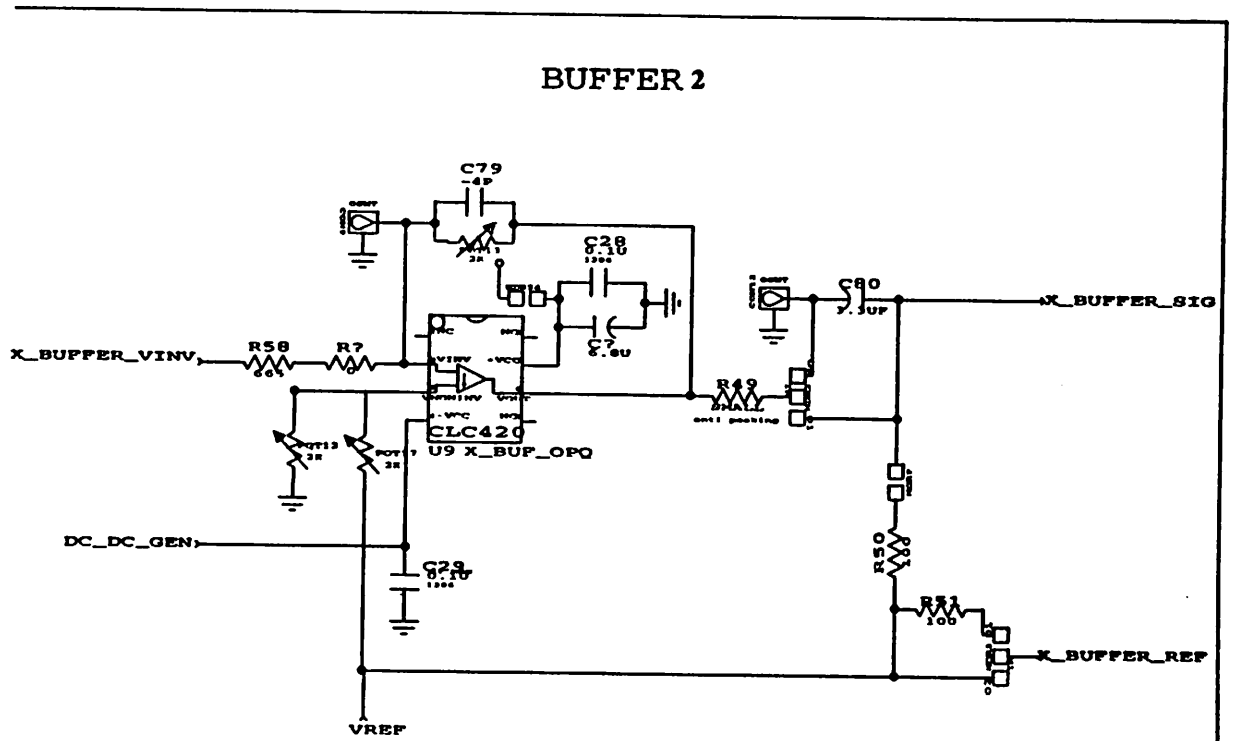
As a general rule, the blocks using signal names starting with the letter "x" relate to the transmitter and the blocks using signal names starting with the letter "r" relate to the receiver.

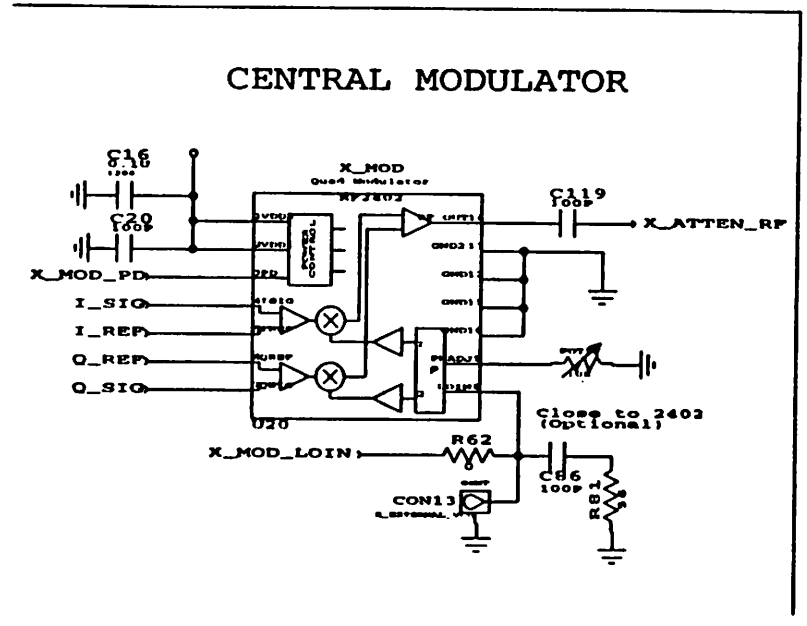
The schematics are presented in alphabetical order of the block names.

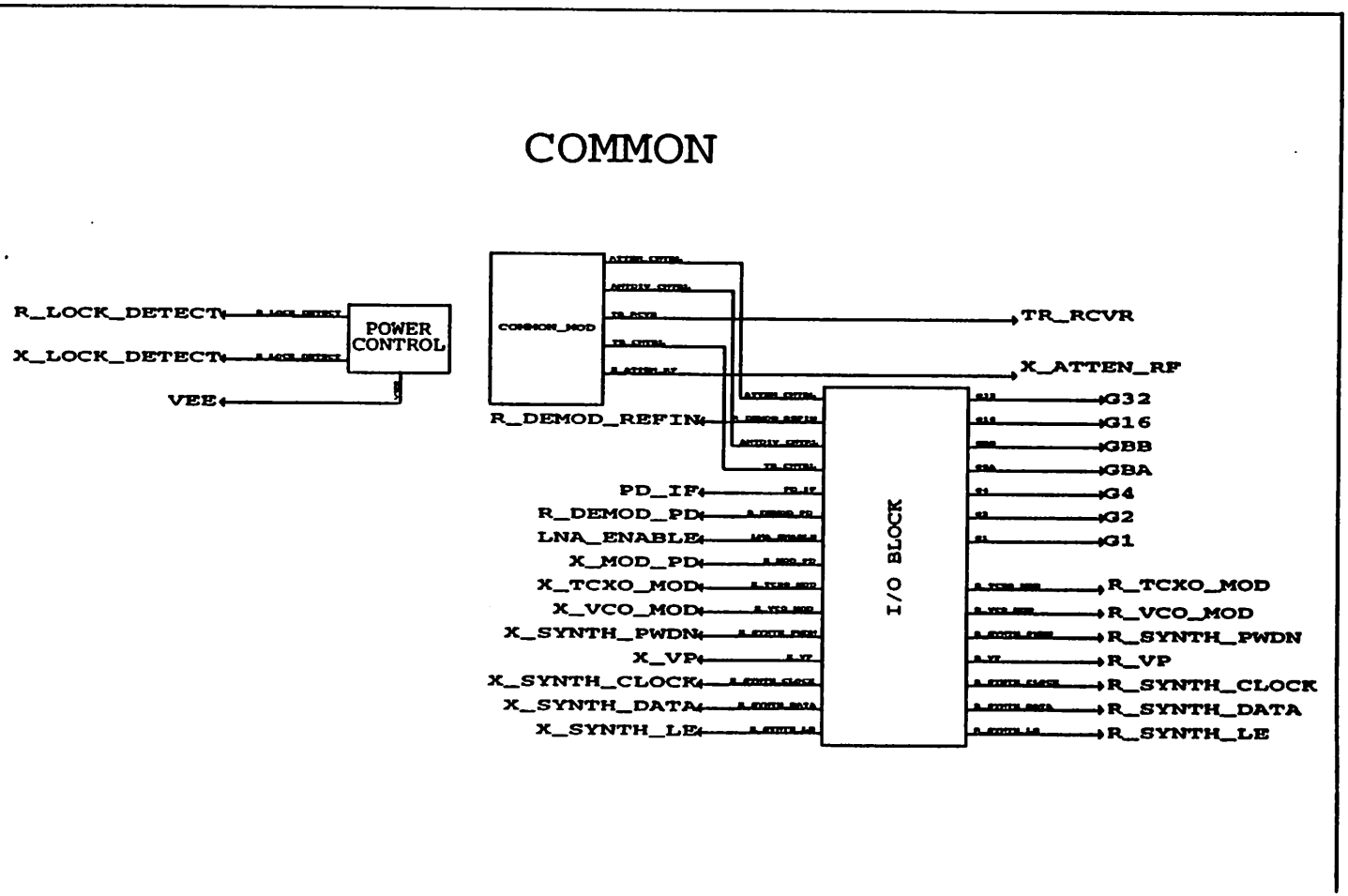
F.1.2 Flat

The flat schematics are presented at the end of the schematic list, marked as "Receiver-Flat" and "Transmitter Flat."

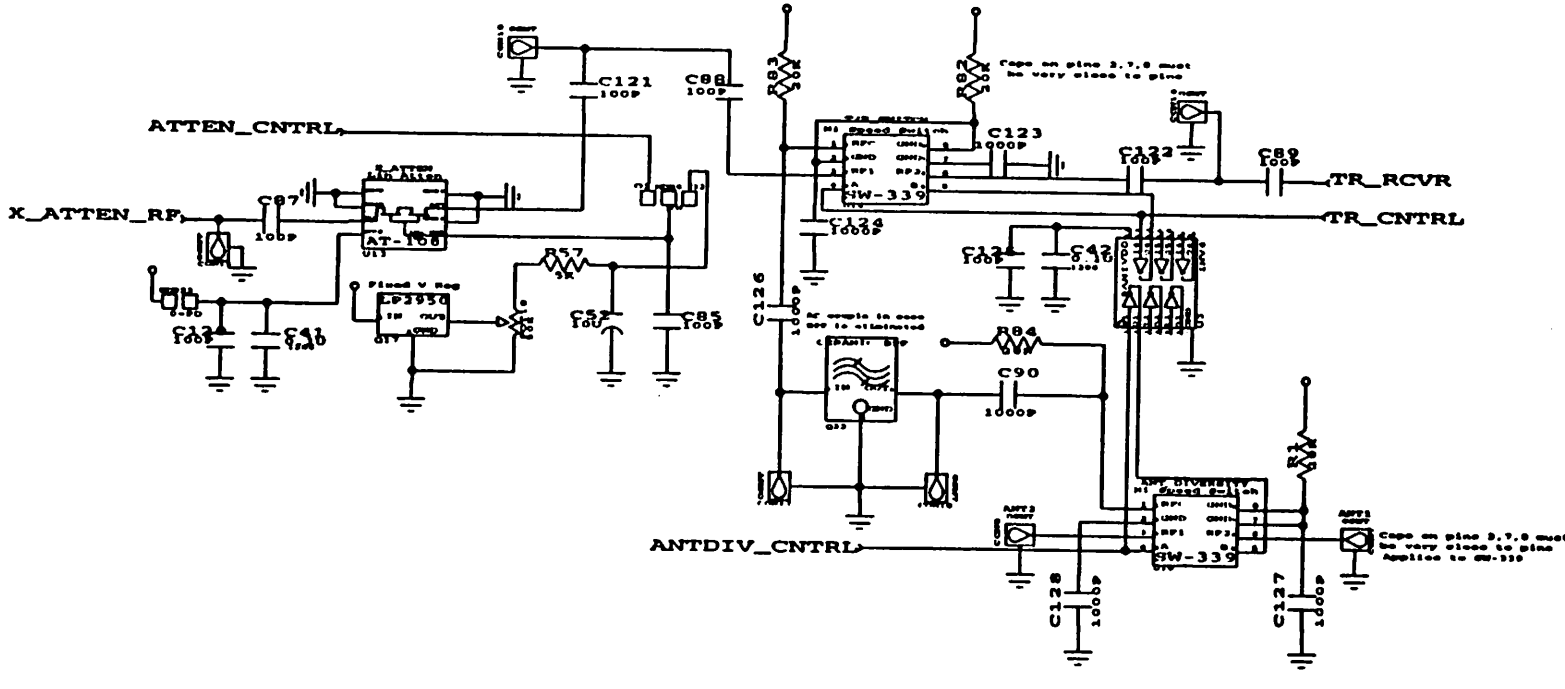

BUFFER
C81
-4P
C80
0.1U
C92
1UF
X_BUFFER_SIG
X_BUFFER_VINV
R61
0
R7
R53
CLC420
U11
R52
R55
100
X_BUFFER_REF
DC_DC_GEN
C31
0.1U
VREF

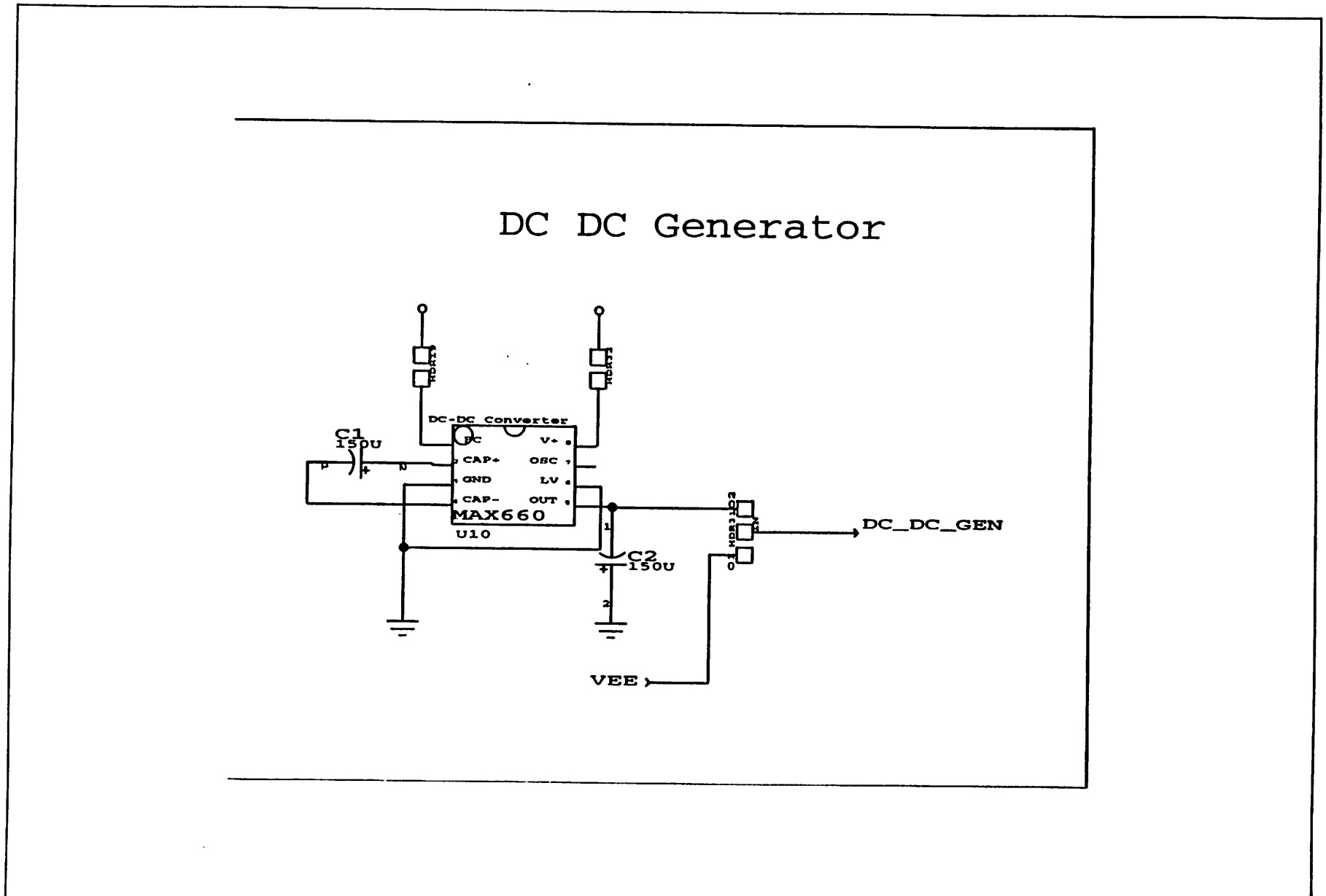

BUFFER 2
C79
C28
C80
X_BUFFER_SIG
X_BUFFER_VINV
R58
R7
C7
R49
CLC420
U9 X_BUF_OPQ
DC_DC_GEN
C29
R50
R51
X_BUFFER_REF
VREF


CENTRAL MODULATOR
C16
C20
X_MOD
C119
X_ATTEN_RF
X_MOD_PD
I_SIG
I_REF
Q_REF
Q_SIG
U20
Close to 2402
(Optional)
X_MOD_LOIN
R62
C86
100P
CON13
RB1

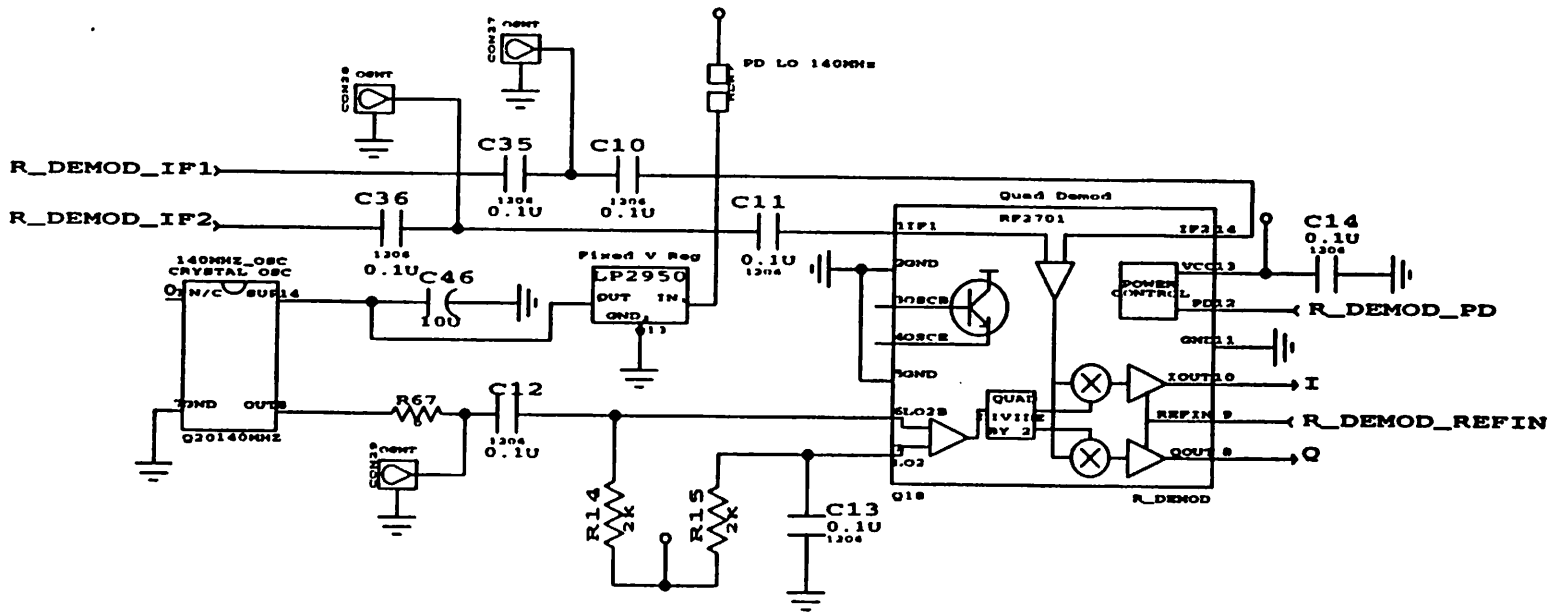

COMMON
R_LOCK_DETECT
X_LOCK_DETECT
POWER CONTROL
VEE
COMMON_MOD
TR_RCVR
X_ATTEN_RF
R_DEMOD_REFIN
PD_IF
R_DEMOD_PD
LNA_ENABLE
X_MOD_PD
X_TCXO_MOD
X_VCO_MOD
X_SYNTH_PWDN
X_VP
X_SYNTH_CLOCK
X_SYNTH_DATA
X_SYNTH_LE
I/O BLOCK
G32
G16
GBB
GBA
G4
G2
G1
R_TCXO_MOD
R_VCO_MOD
R_SYNTH_PWDN
R_VP
R_SYNTH_CLOCK
R_SYNTH_DATA
R_SYNTH_LE

COMMON_MOD

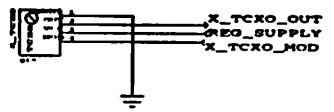

ATTEN_CNTRL
X_ATTEN_RF
C121
C98
C97
C123
C122
C89
TR_RCVR
TR_CNTRL
C124
C125
C42
R57
C52
C85
C126
R84
C90
R1
ANTDIV_CNTRL
C128
C127
SW-339
AT-166


DC DC Generator
DC-DC Converter
C1
150U
CAP+
GND
CAP-
V+
OSC
LV
OUT
MAX660
U10
C2
150U
DC_DC_GEN
VEE

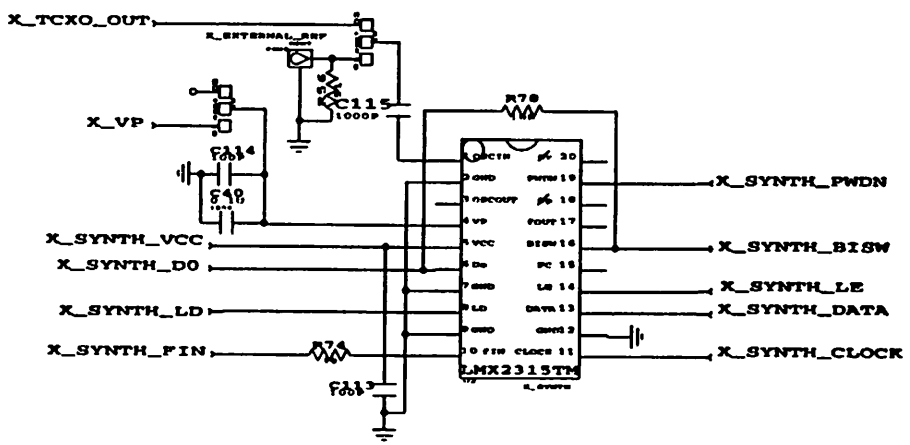
Demodulator



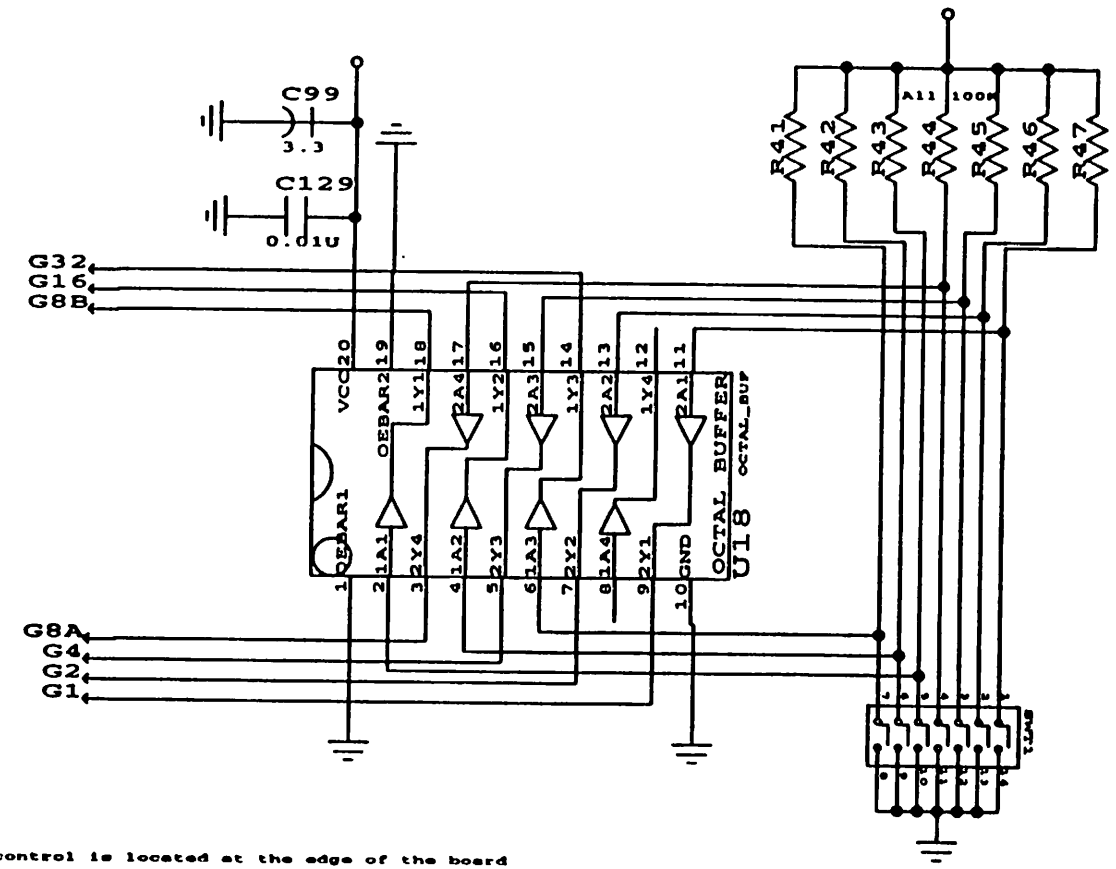
FREQUENCY REFERENCE GENERATOR



FREQUENCY SYNTHESIZER

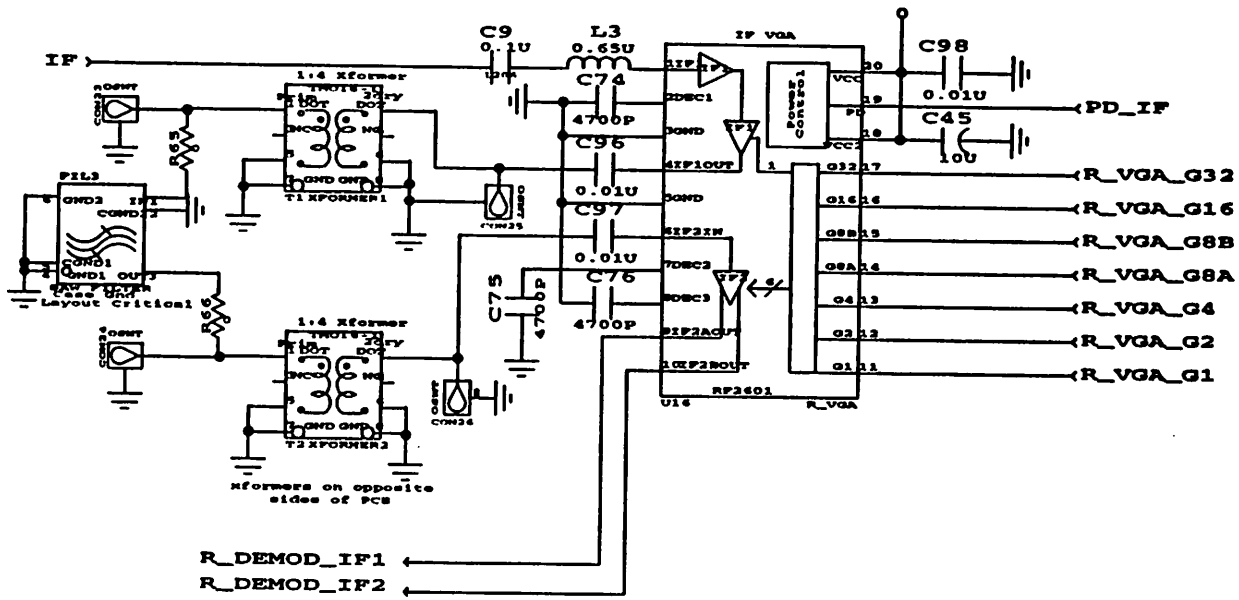


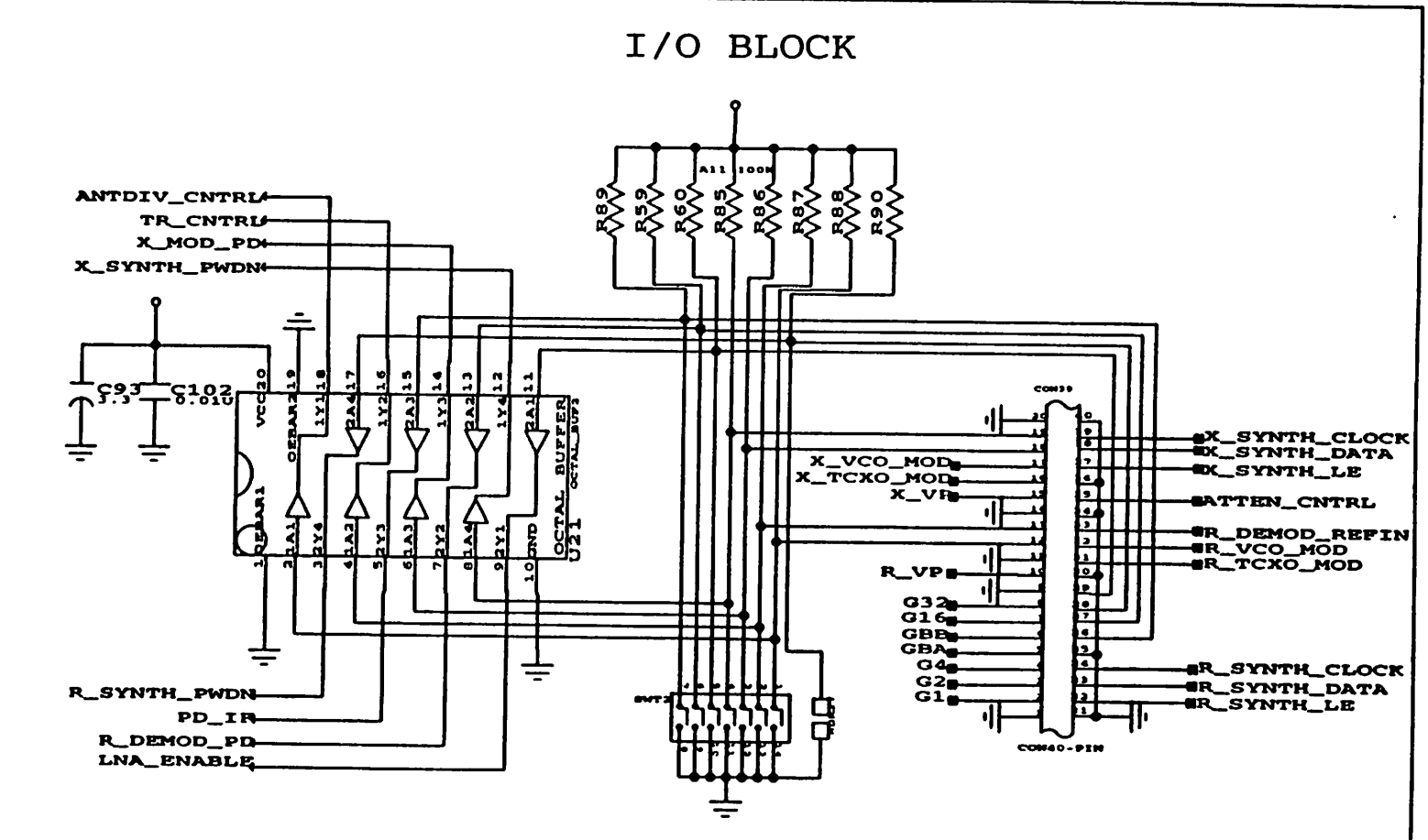
GAIN CONTROL

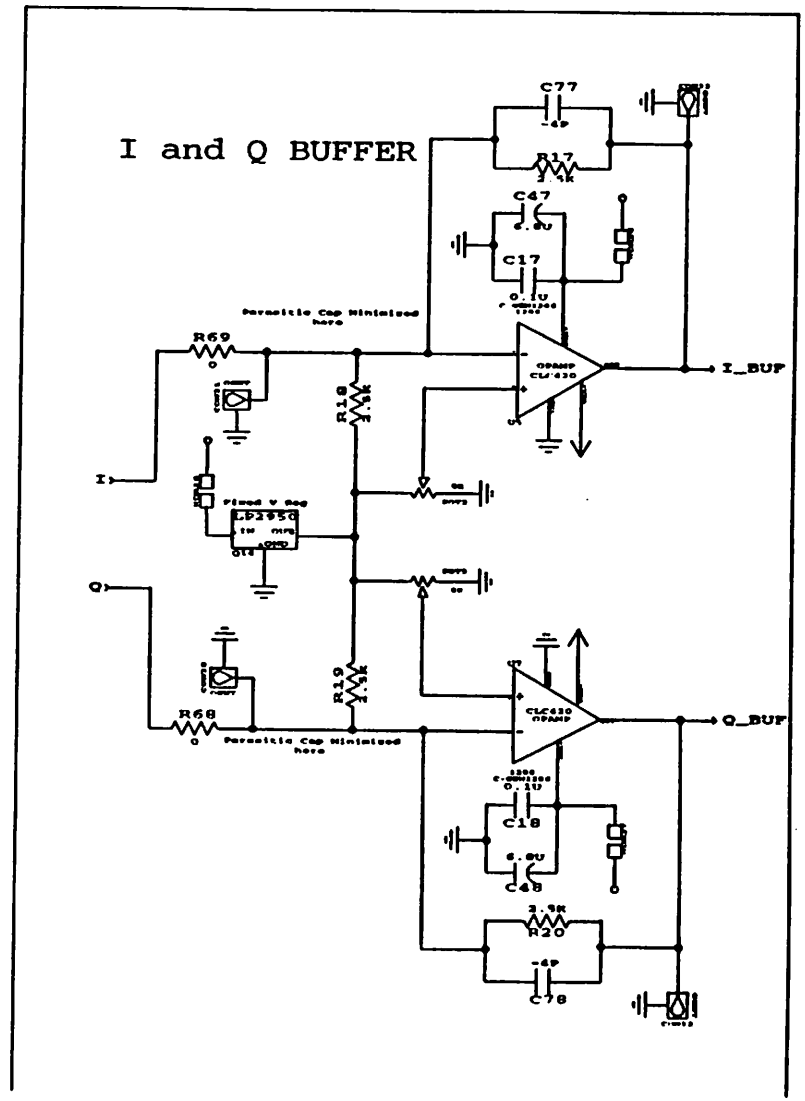


NOTE: Gain control is located at the edge of the board

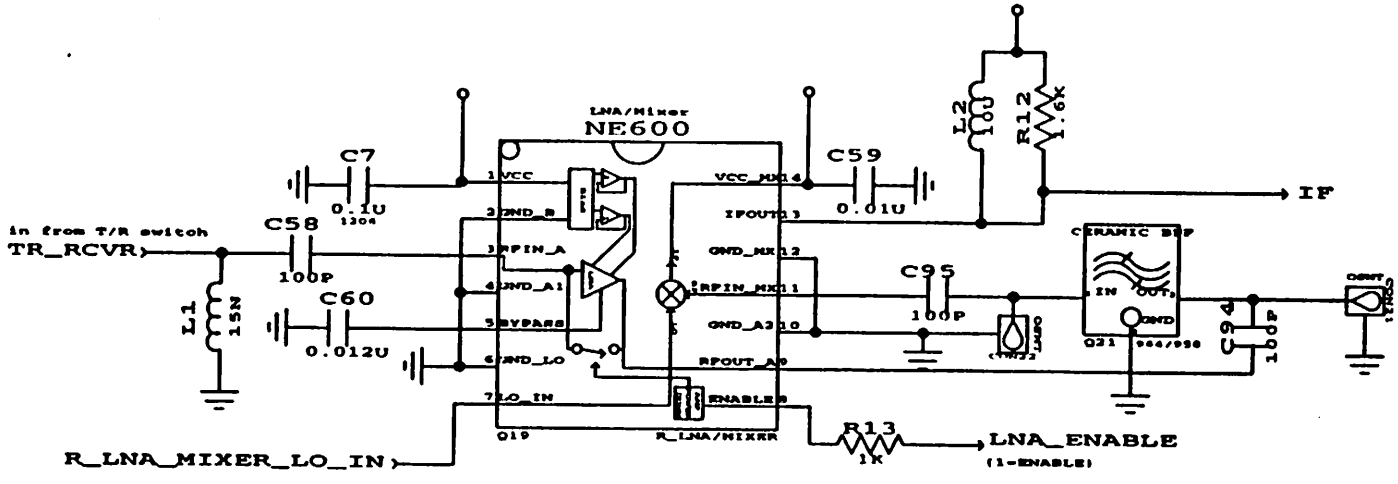
IF and Variable Gain Amplifier



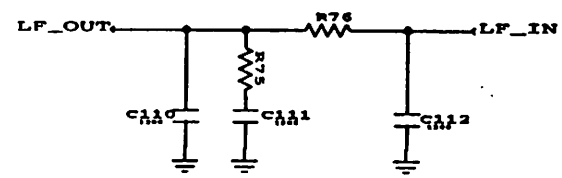

I/O BLOCK
ANTDIV_CNTRL
TR_CNTRL
X_MOD_PD
X_SYNTH_PWDN
R89
R59
R60
R85
R86
R87
R88
R90
C93
3.3
C102
0.01U
VCC20
OCTAL_BUFFER
U21
R_SYNTH_PWDN
PD_IR
R_DEMOD_PD
LNA_ENABLE
X_VCO_MOD
X_TCXO_MOD
X_VP
R_VP
G32
G16
GBB
GBA
G4
G2
G1
CON40-PIN
X_SYNTH_CLOCK
X_SYNTH_DATA
X_SYNTH_LE
ATTEN_CNTRL
R_DEMOD_REFIN
R_VCO_MOD
R_TCXO_MOD
R_SYNTH_CLOCK
R_SYNTH_DATA
R_SYNTH_LE


I and Q BUFFER
C77
R17
C47
C17
R69
R18
I_BUF
I
Q
R19
R68
Q_BUF
C18
C48
R20
C78

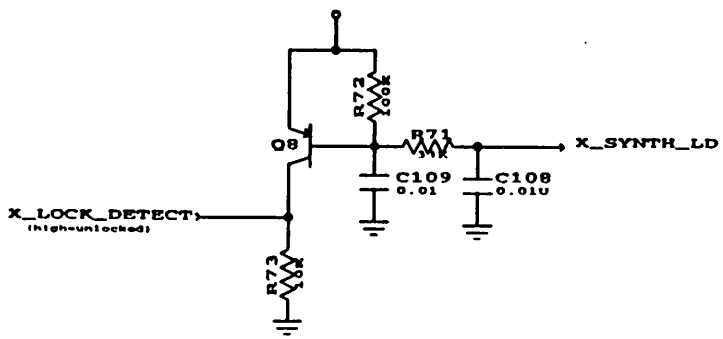
LNA/MIXER


LNA/Mixer
NE600
C7
0.1U
C58
100P
C60
0.012U
L1
15N
C59
0.01U
L2
10U
R12
1.6K
IF
in from T/R switch
TR_RCVR
C95
100P
CERAMIC BPF
C94
100P
R13
1K
LNA_ENABLE
(1-ENABLE)
R_LNA_MIXER_LO_IN
R_LNA/MIXER

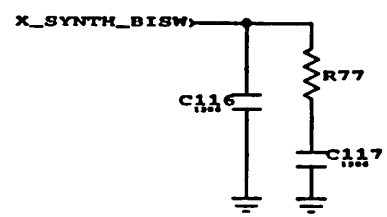
LOOP FILTER



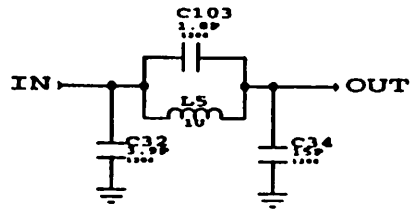
LOCK DETECT



LOOP FILTER II (OPTIONAL)



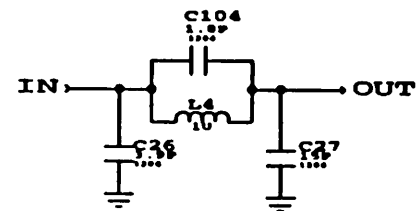
LOW PASS FILTER



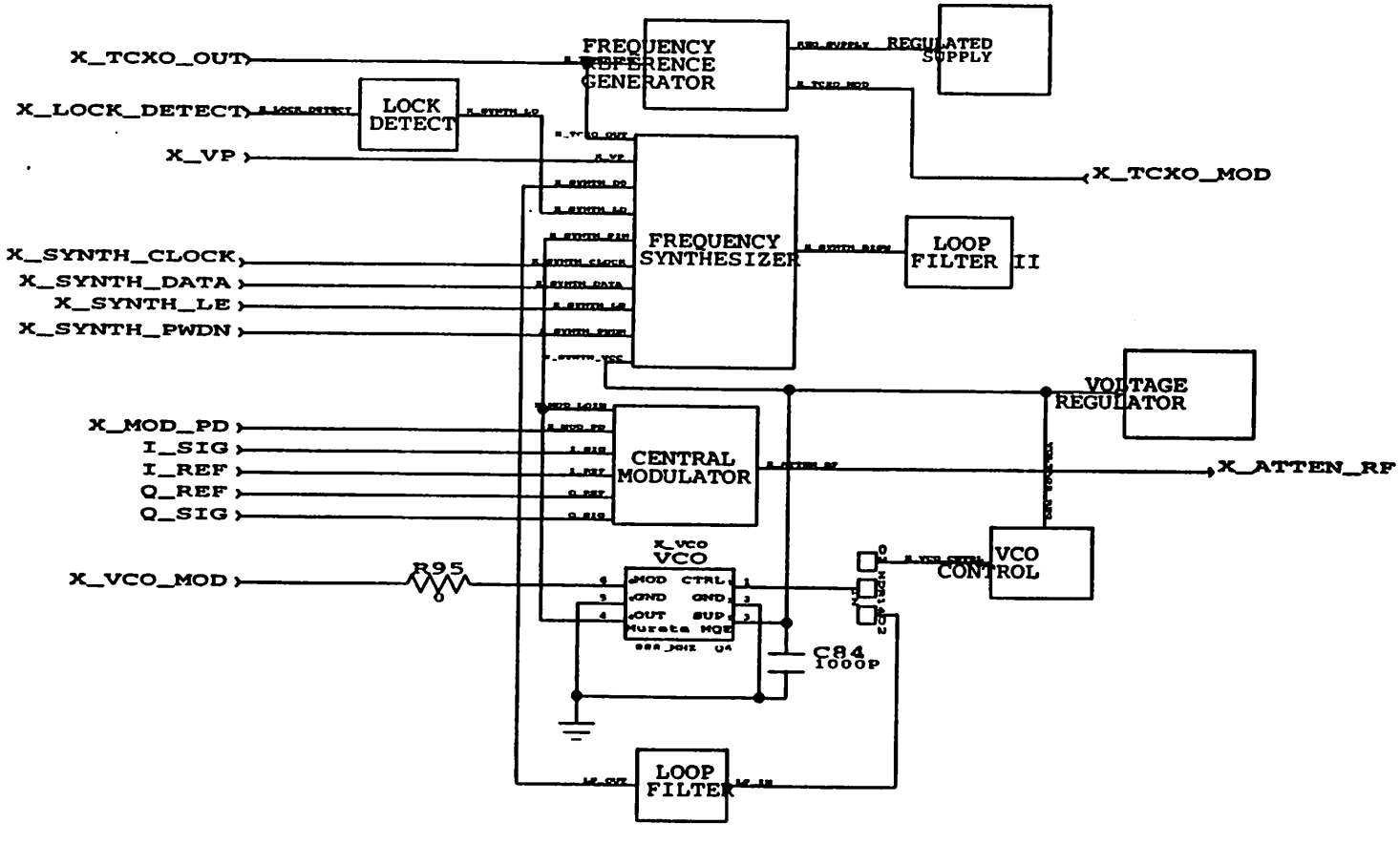
Transmitter

Transmitter

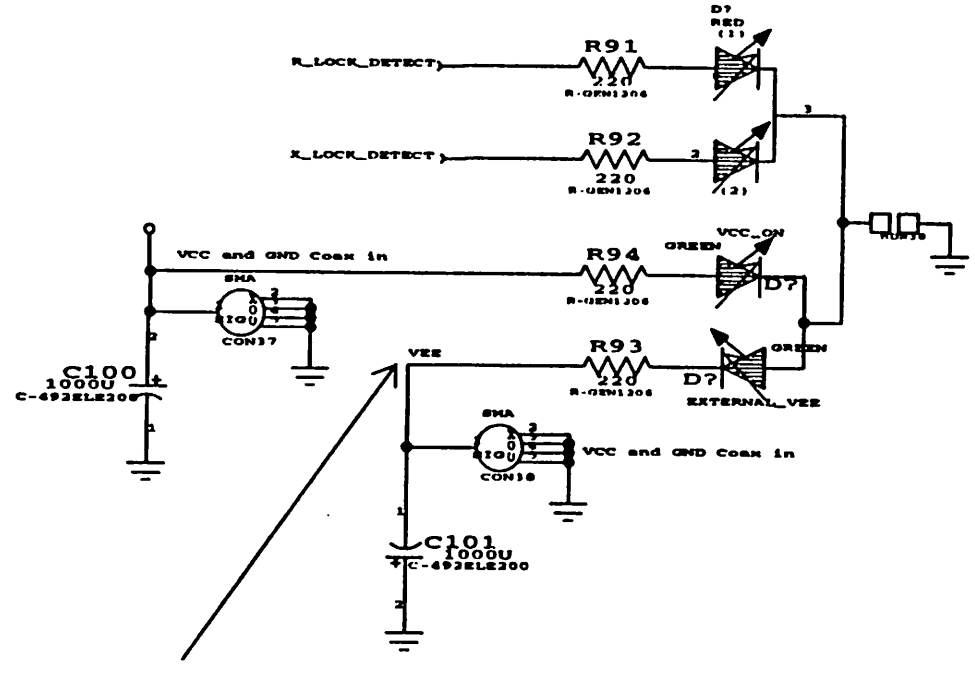
LOW PASS FILTER



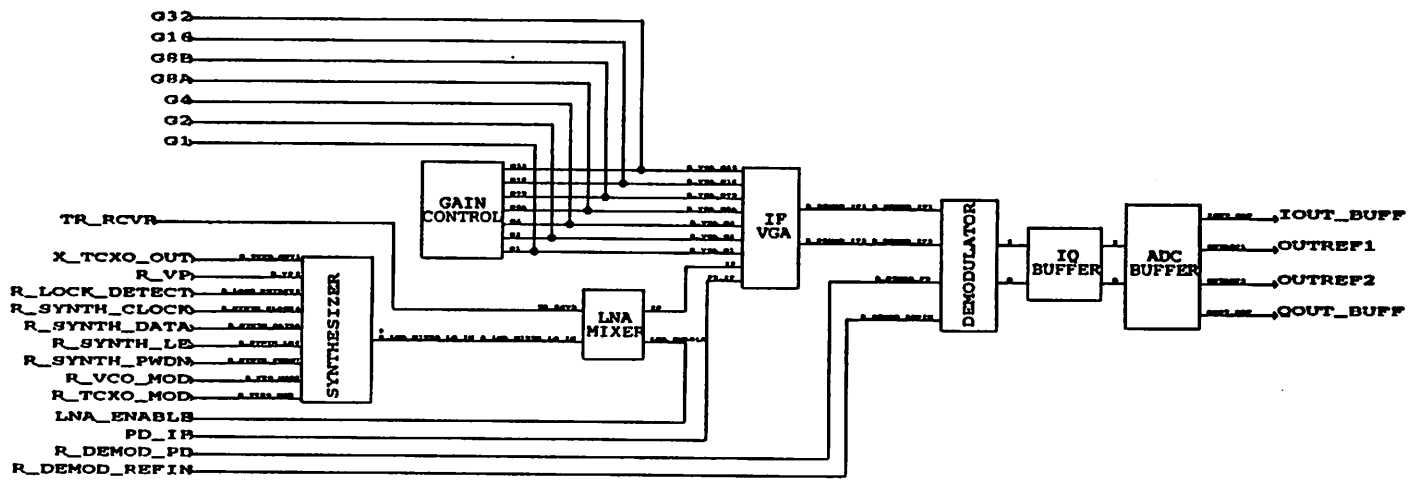
MODULATOR


X_TCXO_OUT
FREQUENCY REFERENCE GENERATOR
REGULATED SUPPLY
X_LOCK_DETECT
LOCK DETECT
X_VP
X_TCXO_MOD
X_SYNTH_CLOCK
X_SYNTH_DATA
X_SYNTH_LE
X_SYNTH_PWDN
FREQUENCY SYNTHESIZER
LOOP FILTER II
VOLTAGE REGULATOR
X_MOD_PD
I_SIG
I_REF
Q_REF
Q_SIG
CENTRAL MODULATOR
X_ATTEN_RF
X_VCO_MOD
R95
X_VCO
VCO
VCO CONTROL
C84
1000P
LOOP FILTER

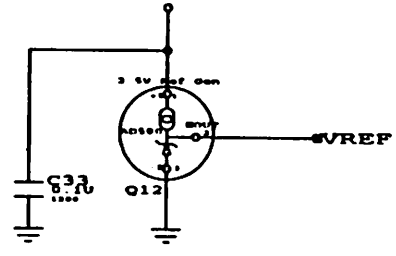
POWER CONTROL



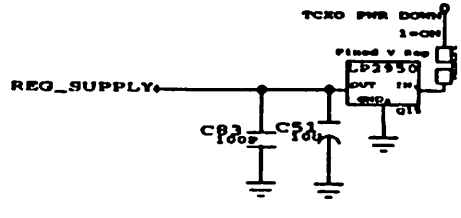
IMPORTANT: IN ROUTING BRING XMTR AND RCVR VEE's USING SINGLE POINT OF CONTACT


RECEIVER
G32
G16
G8B
G8A
G4
G2
G1
GAIN CONTROL
IF VGA
DEMODULATOR
IQ BUFFER
ADC BUFFER
IOUT_BUFF
OUTREF1
OUTREF2
QOUT_BUFF
TR_RCVR
X_TCXO_OUT
R_VP
R_LOCK_DETECT
R_SYNTH_CLOCK
R_SYNTH_DATA
R_SYNTH_LE
R_SYNTH_PWDN
R_VCO_MOD
R_TCXO_MOD
LNA_ENABLB
PD_IB
R_DEMOD_PD
R_DEMOD_REFIN
SYNTHESIZER
LNA MIXER

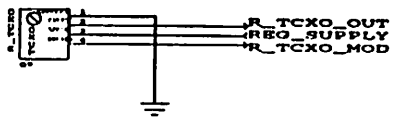
REFERENCE GENERATOR



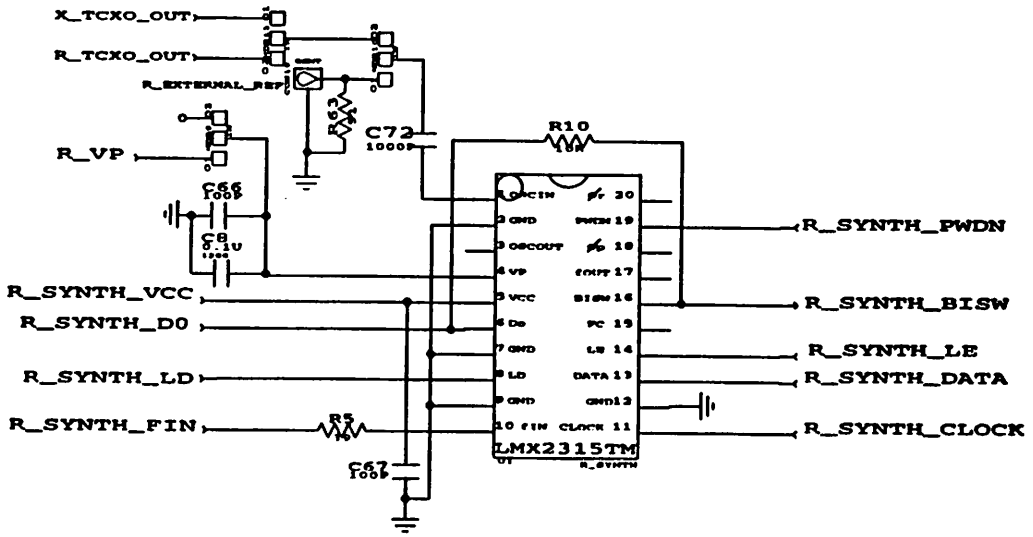
REGULATED SUPPLY

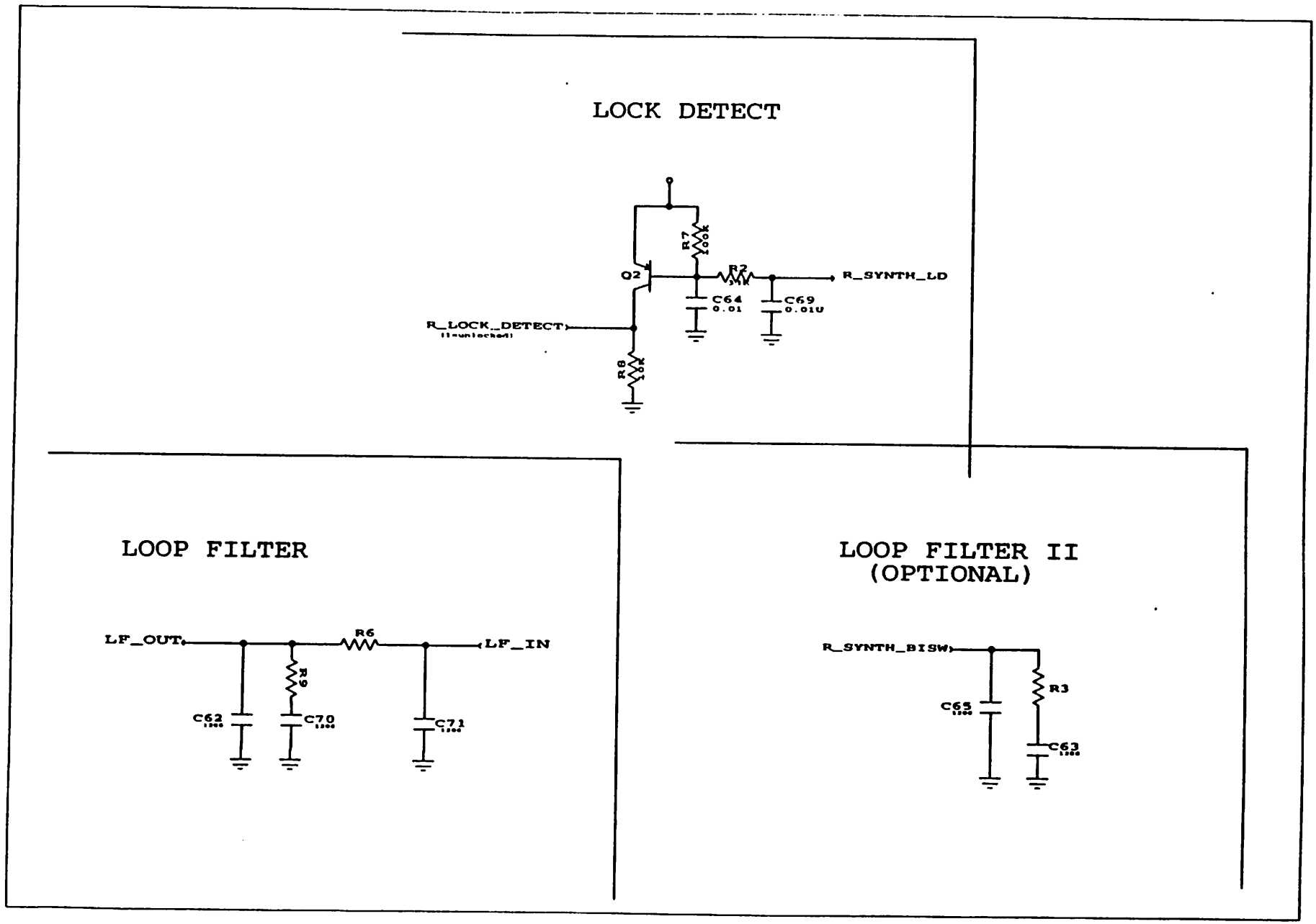


FREQUENCY REFERENCE GENERATOR

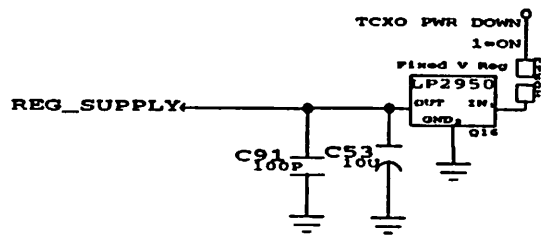


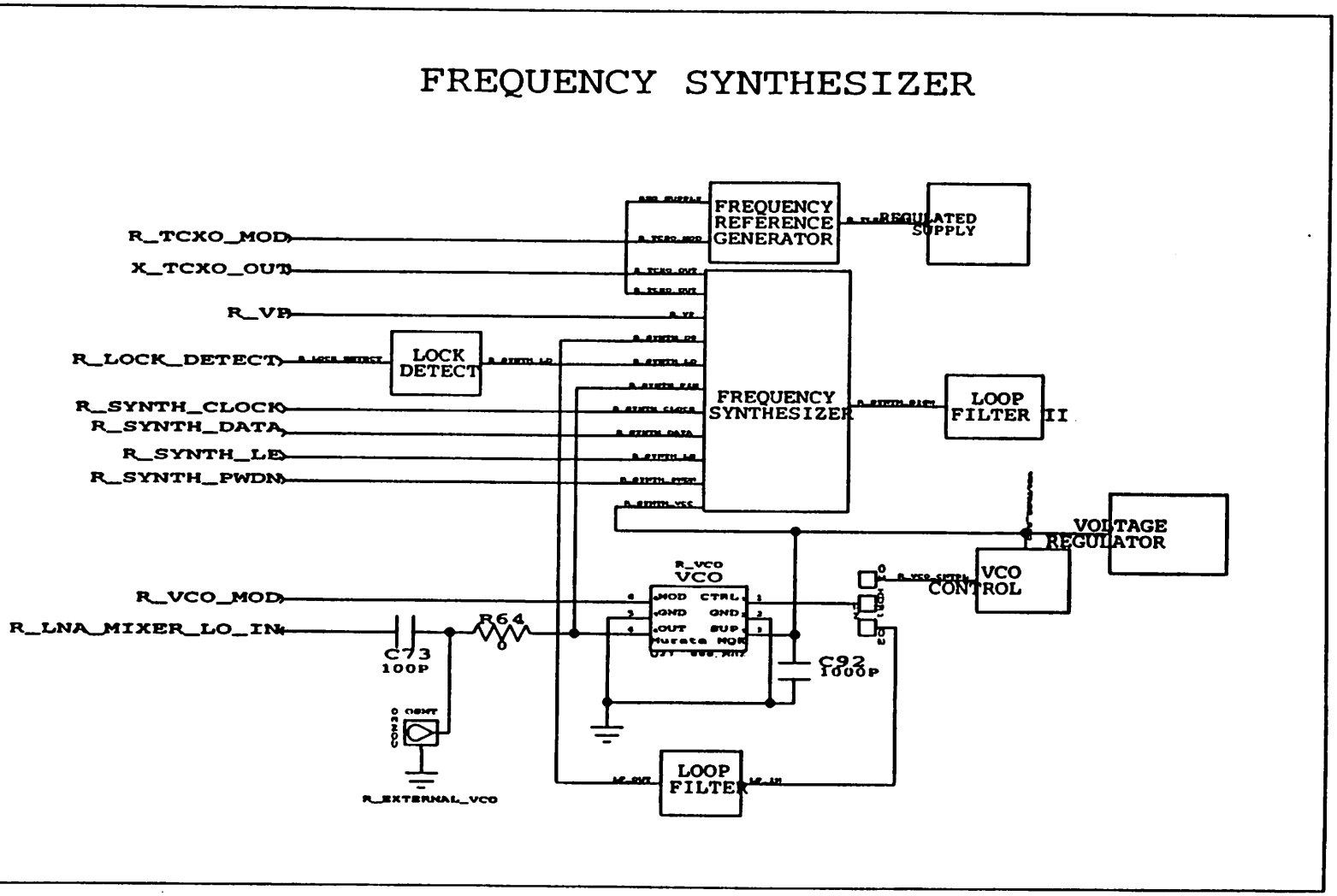
FREQUENCY SYNTHESIZER



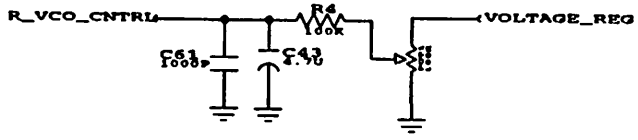

LOCK DETECT
R7
100K
Q2
R2
R_SYNTH_LD
C64
0.01
C69
0.01U
R_LOCK_DETECT
(1=unlocked)
R8
10K
LOOP FILTER
LF_OUT
R6
LF_IN
R9
C62
C70
C71
LOOP FILTER II
(OPTIONAL)
R_SYNTH_BISW
R3
C65
C63

REGULATED SUPPLY

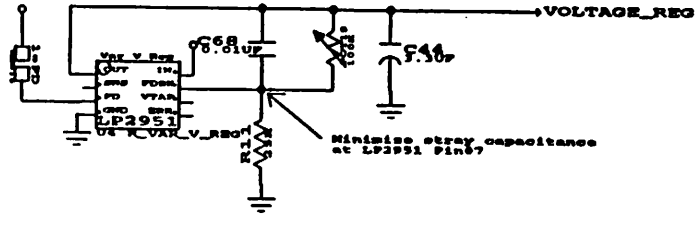



FREQUENCY SYNTHESIZER
FREQUENCY REFERENCE GENERATOR
REGULATED SUPPLY
R_TCXO_MOD
X_TCXO_OUT
R_VP
LOCK DETECT
R_LOCK_DETECT
FREQUENCY SYNTHESIZER
LOOP FILTER II
R_SYNTH_CLOCK
R_SYNTH_DATA
R_SYNTH_LE
R_SYNTH_PWDN
VOLTAGE REGULATOR
VCO CONTROL
R_VCO
VCO
R_VCO_MOD
R_LNA_MIXER_LO_IN
R64
0
C73
100P
C92
1000P
R_EXTERNAL_VCO
LOOP FILTER

FREE RUNNING VCO CONTROL

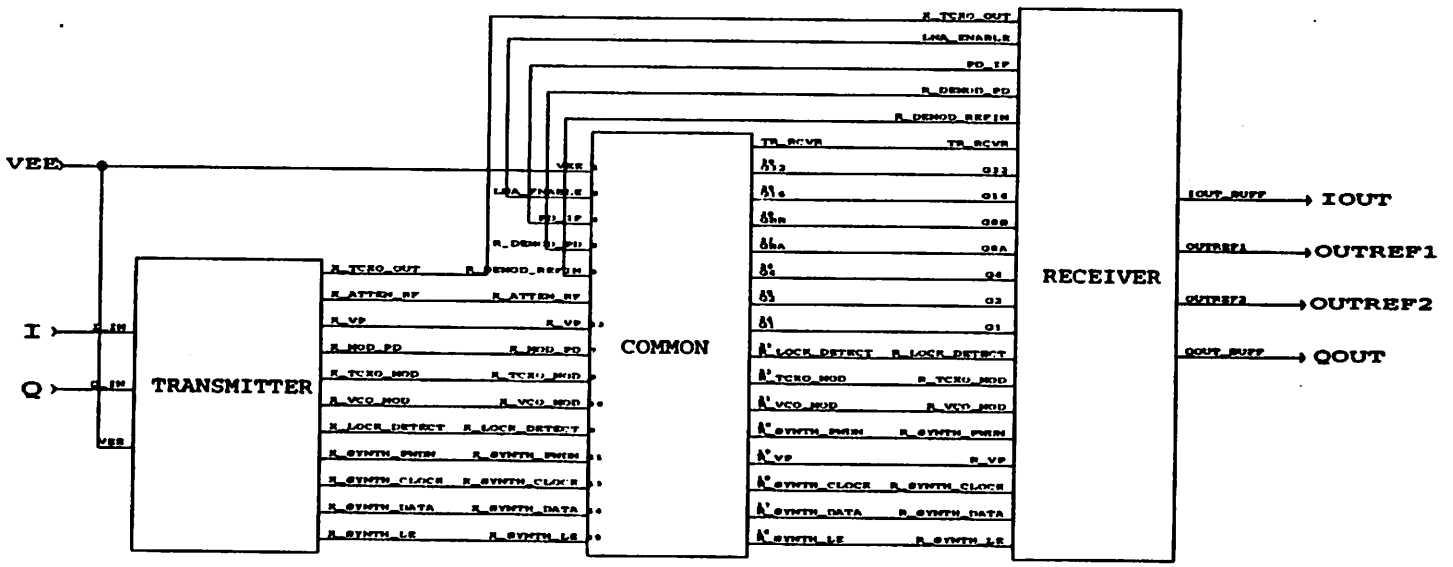


VOLTAGE REGULATOR

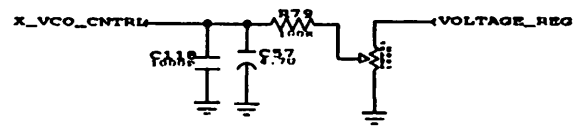


Place voltage regulator close to synthesiser, VCO, TCXO

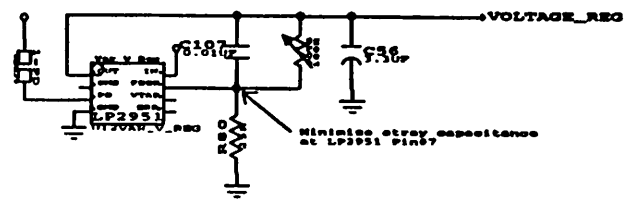
TRANSCEIVER



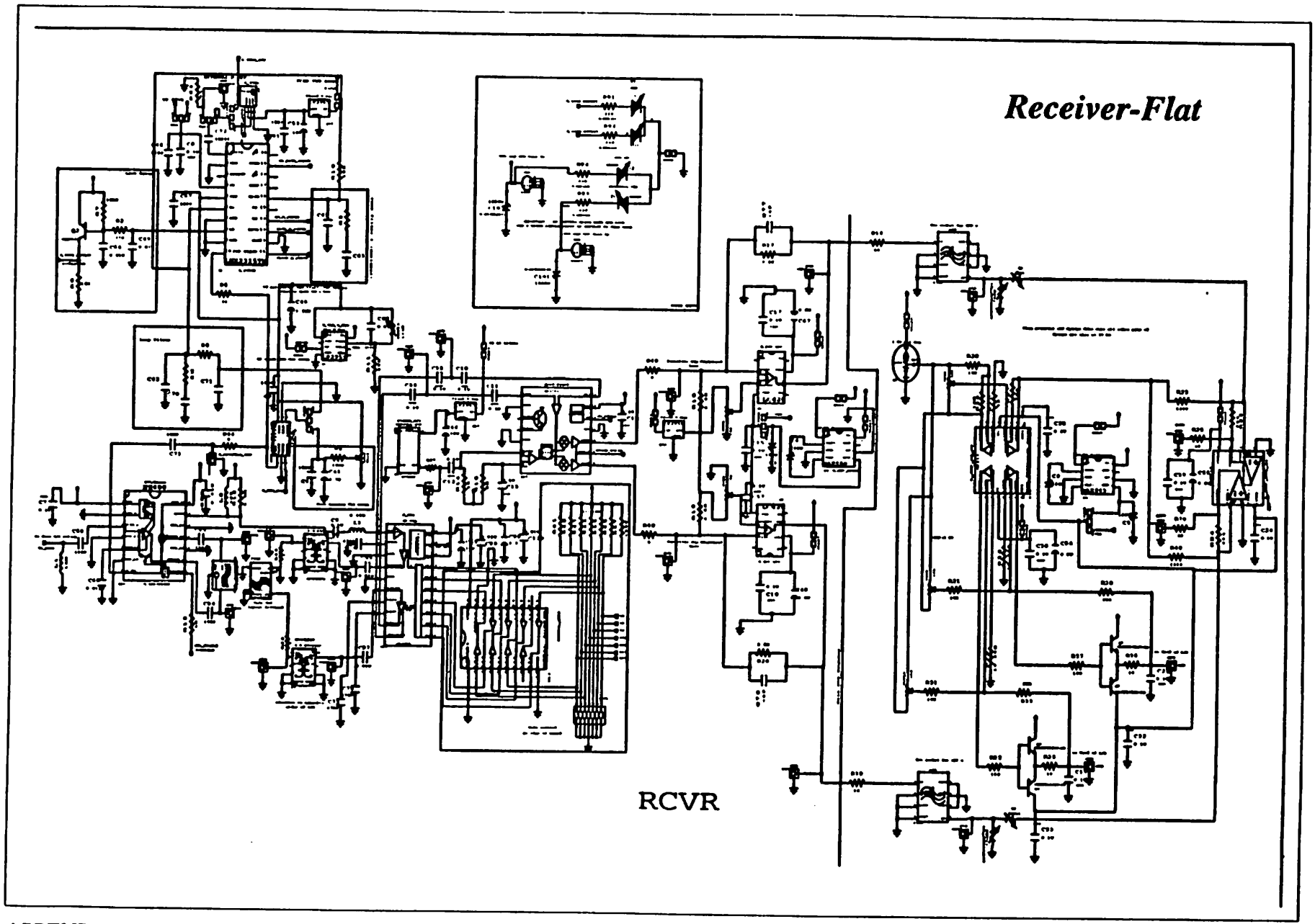
FREE RUNNING VCO CONTROL



VOLTAGE REGULATOR

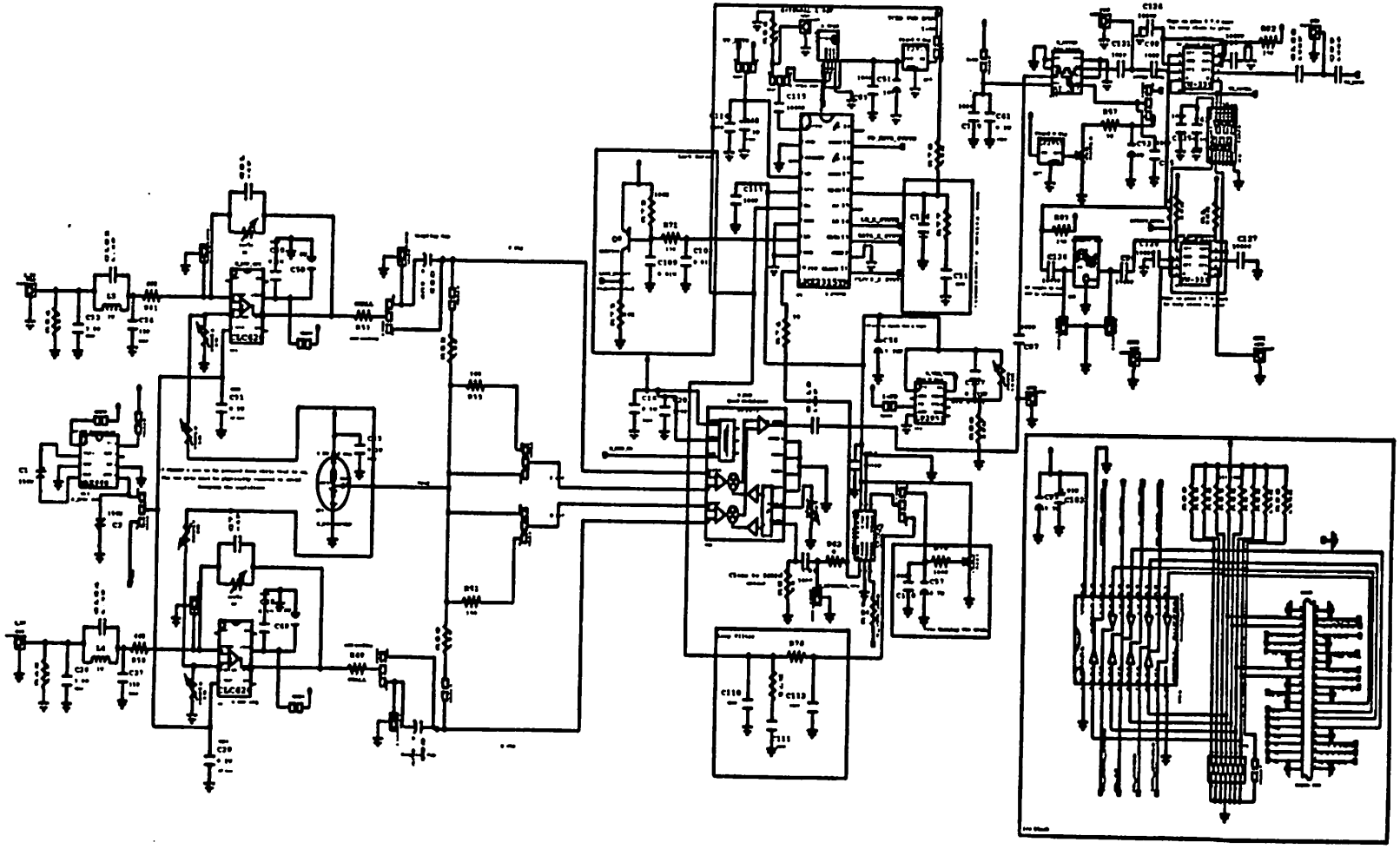


Place voltage regulator close to synthesiser, VCO, TCXO


Receiver-Flat
RCVR

Transmitter-Flat

XMTR

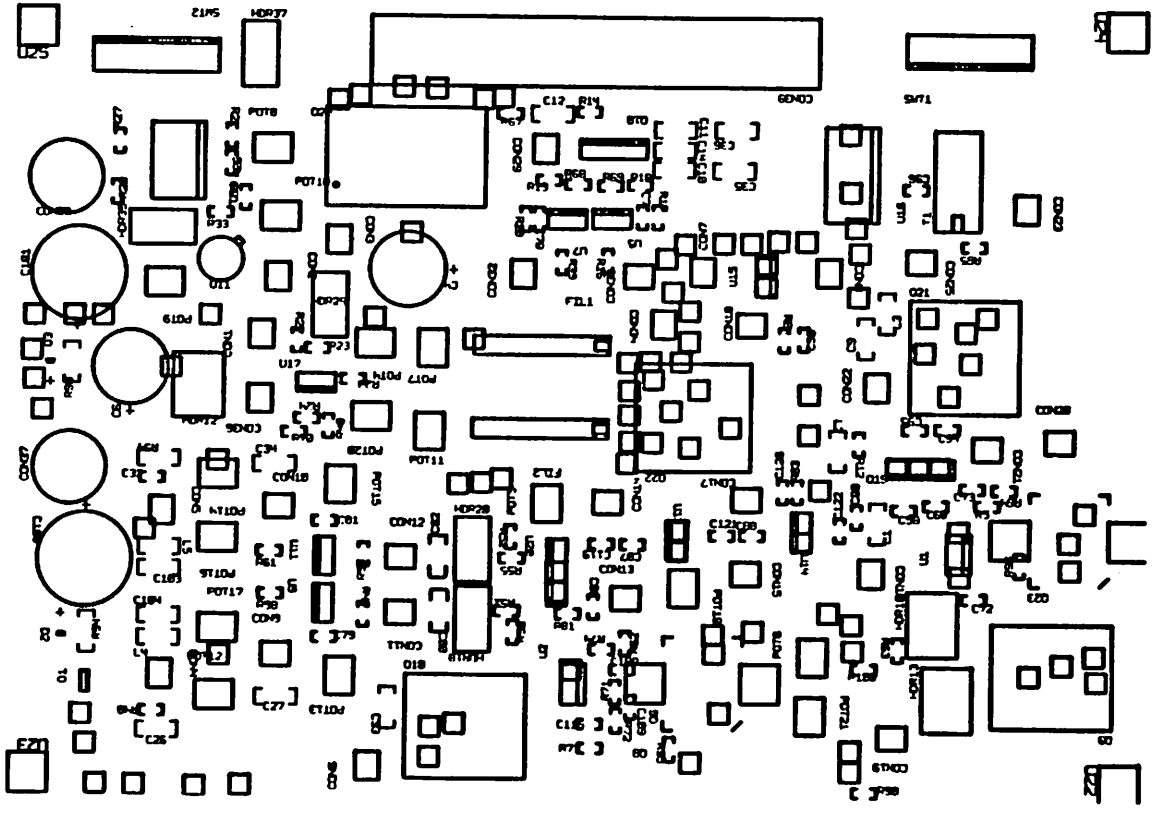


APPENDIX G. Artwork

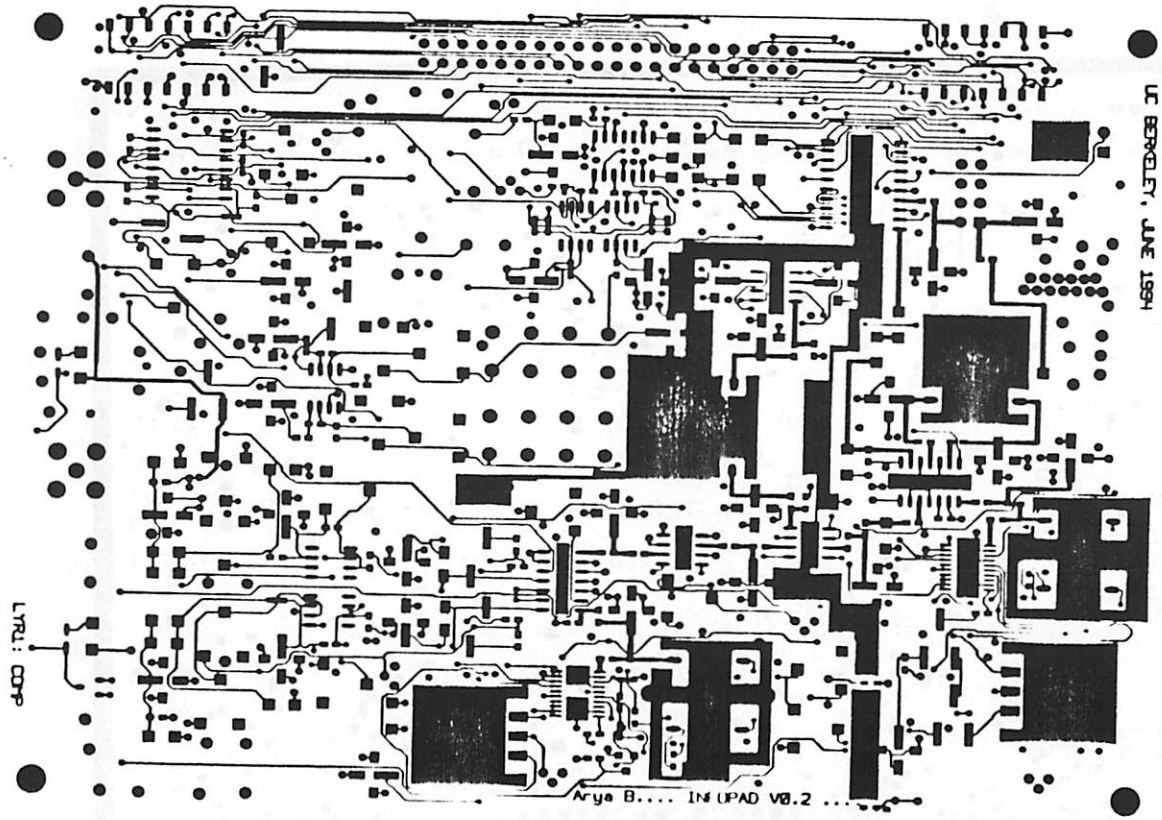
G.1 General Information

The postscript version of the gerber files is presented in this appendix. The artwork for the four layers of the board, the two silk-screens, and an "overall" plot are shown here only. Plot scale is 1:1.

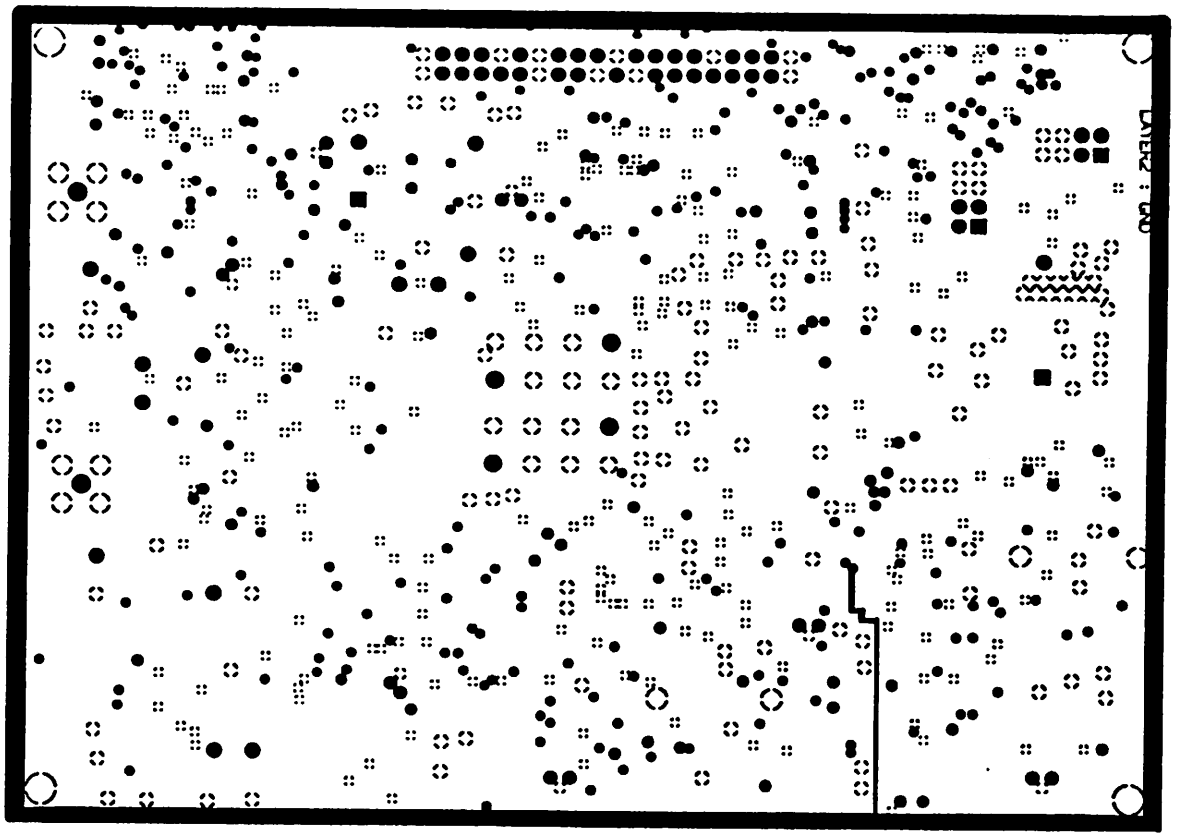
Component Silk Screen



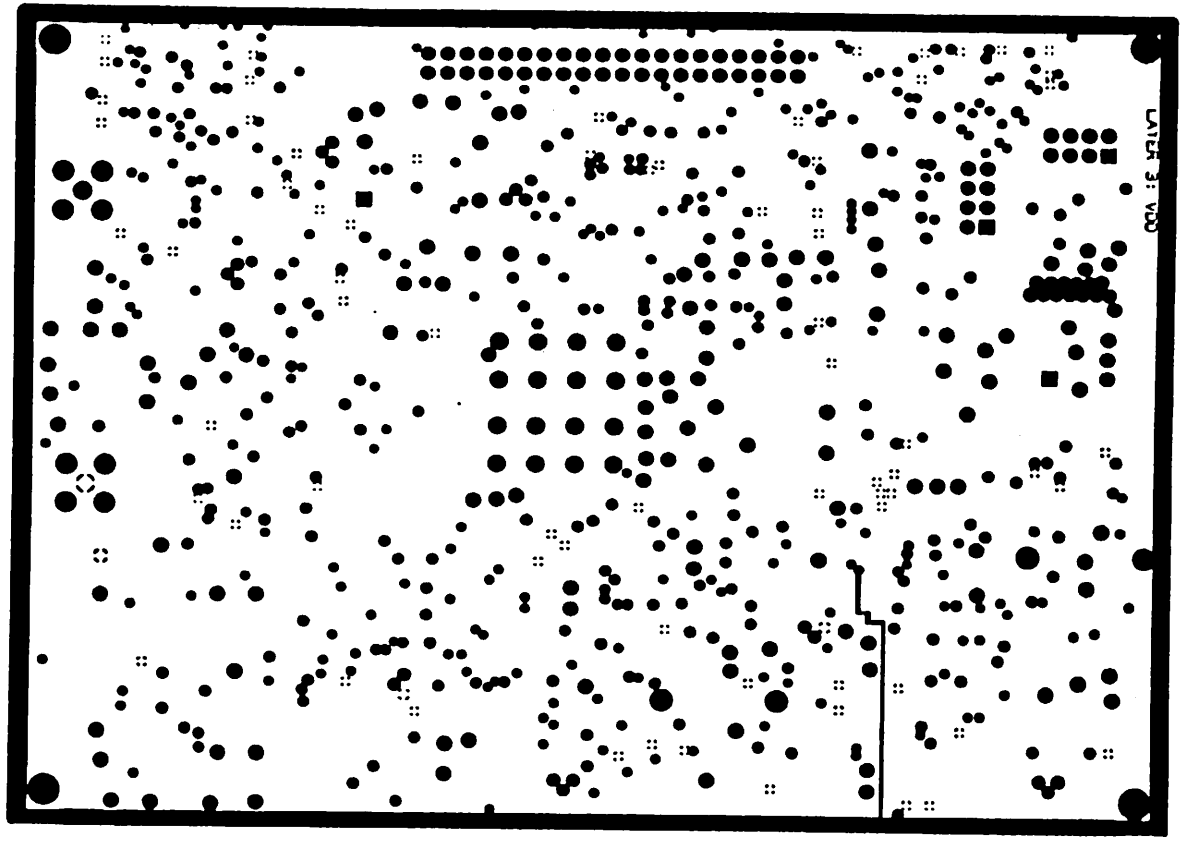
Component Layer



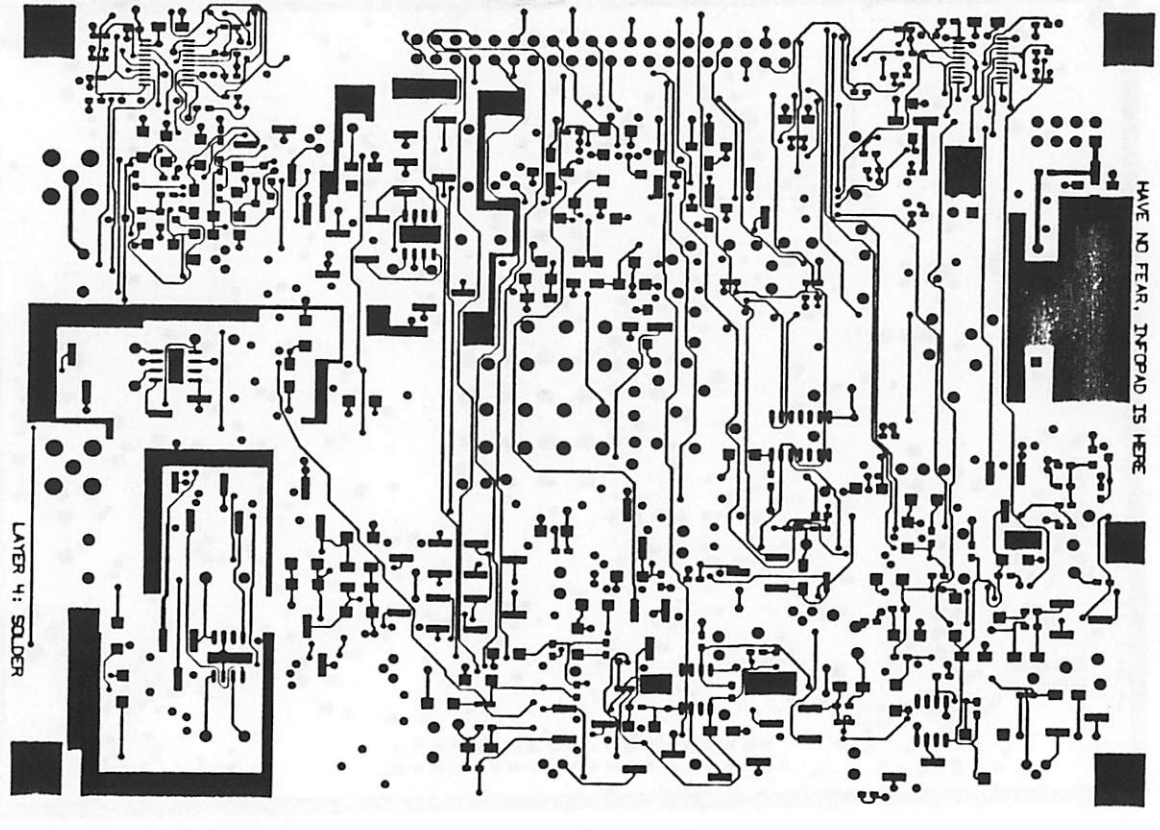
GND Layer (Negative)



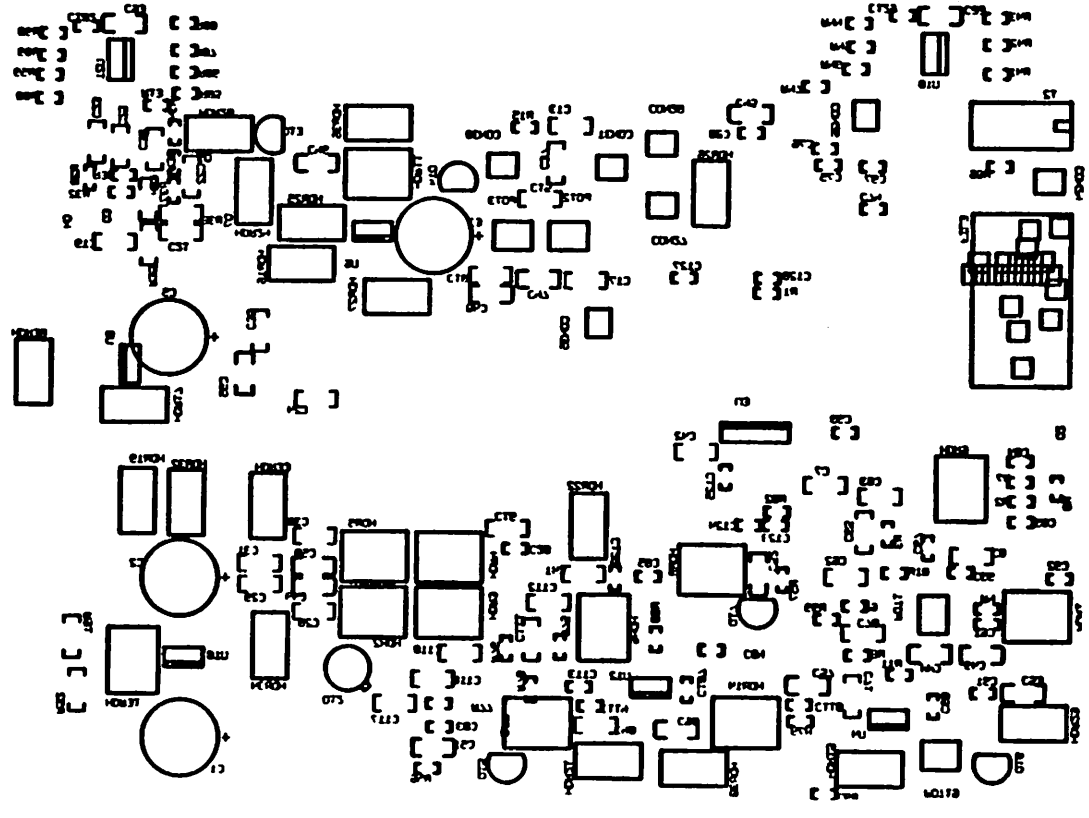
Power Layer (Negative)



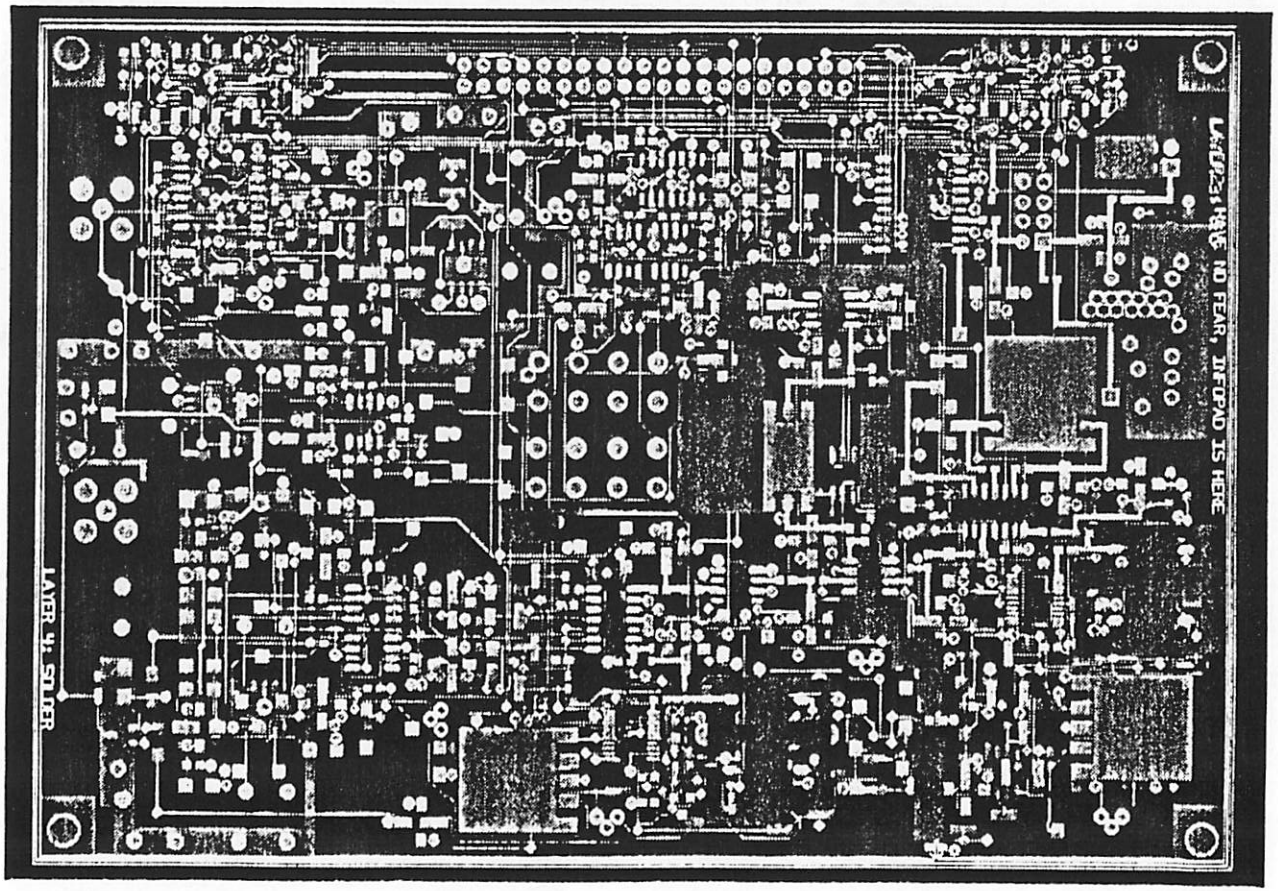
Solder Layer



Solder Side Silk Screen



Multi-Layer View



APPENDIX H. Bill Of Materials & Component Cross Listings

1.0 PARTIAL BOM

ITEM	QUAN.	PART NAME/SPEC
1	2	888CA Murata Ceramic 3 pole RF Filters
REF DES:	Q22,Q21	
2	1	HC04A Hex Inverter MOTOROLA, SM
REF DES:	U3	
3	2	SW-339 MaCOM, High Freq GaAs Switch
REF DES:	U14,U15	
4	1	AT108 MaCom, Voltage var. attenuator
REF DES:	U13	
5	5	C 1206 Surface Mount Caps for Loop Filters; user spec'd
REF DES:	C117,C116,C112,C111,C110	
6	1	MQE001-888 Murata VCO SM 888_MHZ
REF DES:	Q6	
7	1	RF2402 RF MicroDevices, IQ Modulator
REF DES:	U20	
8	6	MAXC001 Maxim Electrolytic Low ESR Cap 150UF
REF DES:	C6,C5,C4,C3,C2,C1	
9	1	851854 SAWTEK IF SAW Filter
REF DES:	FIL3	
10	1	NE/SA600D Philips/Signetics LNA Mixer
REF DES:	Q19	
11	2	CT2077LPSTM-ND DIPSW7; Surface Mount Dipswitch
REF DES:	SWT1, SWT2	

ITEM	QUAN.	PART NAME/SPEC
12	2	74VHCT244MSCX OCTAL_BUFFER National Semi, TSSOP
REF DES: U21,U18		
13	2	IMBT3904DI BJT NPN
REF DES: Q7,Q3		
14	1	OP413 Quad Low noise and offset opamp, Aanalog Dev
REF DES: U19		
15	1	CLC412 COMLINEAR dual high speed transimpedance opamp
REF DES: U17		
16	2	AD580 Analog Devices Voltage References
REF DES: Q12,Q11		
17	4	POT Surface mount potentiameter 10K
REF DES: POT10,POT9,POT8,POT5		
18	2	POT Surface mount potentiameter 1K
REF DES: POT20,POT4		
19	3	MAX660 Maxim Switching Inverting Voltage Converters
REF DES: U10,U8,U6		
20	4	CLC420 COMLINEAR high speed voltage feedback opamp
REF DES: U11,U9,U7,U5		
21	5	LP2950 National Semi Linear Voltage Regulators (Fixed)
REF DES: Q17,Q16,Q15,Q14,Q13		
22	1	SW5L-2 IF_OSC Conner Winfield 140MHZ
REF DES: Q20		
23	1	RF2701 RF MICRODEVICES Quadrature Demod
REF DES: Q18		
24	2	TMO16-1 MINICIRCUITS 16:1 impedance xformers
REF DES: T2,T1		

ITEM	QUAN.	PART NAME/SPEC
25	1	RF2601 RF MICRODEVICES IF VGA

REF DES: U16

26	1	T-1050-2AO TCXO Oscillatek, 9.6MHz

REF DES: Q10

27	1	T-1050-2AO TCXO Oscillatek, 15.36MHz

REF DES: Q9

28	2	LP2951 National Semi Linear Voltage Regulators (Var)

REF DES: U12,U4

29	2	LMX2315TM National Semi Frequency Synthesizer

REF DES: U2,U1

30	1	MQE001-964 Murata VCO 964/958_MHz

REF DES: Q23

31	5	C Surface Mount Capacitors, LF, user defined

REF DES: C71,C70,C65,C63,C62

32	6	R Surface Mount Res. User Def'd

REF DES: R77,R76,R75,R9,R6,R3

33	11	C 0.012UF

REF DES: C60,C109,C108,C102,C129,C98,C97,C96,C69,C64,C59

34	21	C 100PF

REF DES: C125,C122,C121,C120,C119,C114,C113,C20,C95,C94,C91,C89, C88,C87,C86,C85,C83,C73,C67,C66,C58

2.0 Component Cross Reference List

COMPONENT LIST

Job name : nxcvr2-3 Date : Thu Jun 30 1994 Time : 16:36:27

Comp	Part number	Part type	Description	Position x	Position y	Surface	Loadout	
C1	C-MAXC001EL	MAXC001EL	CAPACITOR,ELECTROLYTIC,MAXC001 PKG	1.010	0.139	bom	a	
C2	C-MAXC001EL	MAXC001EL	CAPACITOR,ELECTROLYTIC,MAXC001 PKG.	0.999	0.960	bom	a	
C3	C-MAXC001EL	MAXC001EL	CAPACITOR,ELECTROLYTIC,MAXC001 PKG.	2.296	2.753	bom	a	

C4	C-MAXC001EL	MAXC001EL	CAPACITOR,ELECTROLYTIC,MAXC001 PKG,		1.945	2.593	top	a	
C5	C-MAXC001EL	MAXC001EL	CAPACITOR,ELECTROLYTIC,MAXC001 PKG,		0.931	2.214	btm	a	
C6	C-MAXC001EL	MAXC001EL	CAPACITOR,ELECTROLYTIC,MAXC001 PKG,		0.422	1.963	top	a	
C7	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	4.288	1.459	btm	c		
C8	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	4.913	1.094	btm	c		
C9	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	4.219	2.177	top	c		
C10	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	3.286	3.122	top	c		
C11	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	3.291	3.327	top	c		
C12	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.513	3.407	top	c		
C13	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.963	3.329	btm	c		
C14	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	3.287	3.223	top	c		
C15	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.675	2.950	btm	c		
C16	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.523	1.223	btm	c		
C17	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	3.048	2.525	btm	c		
C18	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.425	2.550	btm	c		
C19	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	0.614	2.713	btm	c		
C20	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	2.601	1.119	btm	c		
C21	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	0.818	2.765	btm	c		
C22	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	0.939	3.123	btm	c		
C23	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	0.449	3.165	btm	c		
C24	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	1.662	1.892	btm	c		
C25	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	0.571	3.142	btm	c		
C26	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	0.513	0.167	top	c		
C27	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	1.122	0.342	top	c		
C28	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	1.660	0.789	btm	c		
C29	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	1.381	0.930	btm	c		
C30	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	1.660	1.178	btm	c		
C31	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	1.377	1.036	btm	c		
C32	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	0.507	1.583	top	c		
C33	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	1.763	0.361	top	c		
C34	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	1.102	1.557	top	c		
C35	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	3.597	3.117	top	c		
C36	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	3.607	3.327	top	c		
C37	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.823	3.069	btm	c		
C38	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	0.748	3.128	btm	c		
C39	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	1.300	2.182	btm	c		
C40	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.986	0.211	btm	c		
C41	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	3.050	0.989	btm	c		
C42	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	3.625	1.630	btm	c		
C43	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	5.039	0.588	btm	c		
C44	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	4.767	0.589	btm	c		
C45	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	3.821	3.397	btm	c		
C46	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	1.585	3.128	btm	c		
C47	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	2.736	2.529	btm	c		
C48	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	2.497	2.450	btm	c		
C49	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	1.593	0.918	btm	c		
C50	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	1.591	1.022	btm	c		
C51	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	2.219	0.093	btm	c		
C52	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	3.883	0.994	btm	c		
C53	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	5.254	0.392	btm	c		
C54	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	0.717	2.936	btm	c		
C55	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	1.222	2.026	btm	c		
C56	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	3.467	0.191	btm	c		
C57	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	4.139	0.424	btm	c		
C58	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.392	1.338	top	c		
C59	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.353	1.736	btm	c		
C60	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.558	1.363	top	c		
C61	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	5.097	0.746	btm	c		
C62	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	4.398	0.985	btm	c		
C63	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	4.572	1.402	btm	c		
C64	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	5.262	1.589	btm	c		
C65	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	4.423	1.149	btm	c		
C66	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.894	1.011	btm	c		
C67	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.754	1.103	btm	c		
C68	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.789	0.288	btm	c		
C69	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	5.269	1.273	btm	c		
C70	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	4.355	0.696	btm	c		
C71	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	4.370	0.438	btm	c		
C72	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.759	0.875	top	c		
C73	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.746	1.452	top	c		
C74	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.425	2.910	btm	c		
C75	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.254	3.137	btm	c		
C76	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.235	3.222	btm	c		

Comp	Part number	Part type	Description	Position x	Position y	Surface	Loadout
C77	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.055	2.905	top	c
C78	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	2.517	2.891	top	c
C79	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	1.402	0.655	top	c
C80	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	2.026	0.798	top	c
C81	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	1.399	1.260	top	c
C82	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	2.015	1.079	top	c
C83	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	2.282	0.198	bom	c
C84	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.614	0.602	bom	c
C85	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.346	0.979	bom	c
C86	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	2.819	0.856	top	c
C87	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.053	1.150	top	c
C88	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.608	1.199	top	c
C89	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.181	1.269	top	c
C90	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.797	2.200	top	c
C91	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	5.078	0.391	bom	c
C92	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	5.470	0.980	bom	c
C93	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	0.584	3.844	bom	c
C94	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.613	1.767	top	c
C95	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.509	1.763	top	c
C96	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.502	3.026	top	c
C97	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.483	3.128	bom	c
C98	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.795	3.301	bom	c
C99	C-3216TAN	C3216TAN	Capacitor,Surface Mount, Tantalum,3 C3216TAN	4.794	3.913	bom	c
C100	C-492EL	CAP492EL	CAPACITOR,ELECTROLYTIC,200mil speci CAP492EL	0.193	1.151	top	a
C101	C-492EL	CAP492EL	CAPACITOR,ELECTROLYTIC,200mil speci CAP492EL	0.147	2.457	top	a
C102	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	0.361	3.830	bom	c
C103	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	0.514	1.008	top	c
C104	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	0.514	0.760	top	c
C107	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.519	0.364	bom	c
C108	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	2.942	0.498	top	c
C109	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.017	0.337	top	c
C110	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.419	0.580	bom	c
C111	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.719	0.583	bom	c
C112	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.874	0.841	bom	c
C113	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	2.996	0.408	bom	c
C114	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	2.990	0.311	bom	c
C115	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	2.773	0.215	top	c
C116	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.278	0.444	bom	c
C117	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General C1206	2.084	0.319	bom	c
C118	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.066	0.325	bom	c
C119	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	2.827	1.152	top	c
C120	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.145	1.001	bom	c
C121	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.453	1.199	top	c
C122	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.094	1.199	top	c
C123	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.000	1.248	bom	c
C124	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.862	1.248	bom	c
C125	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.709	1.530	bom	c
C126	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.797	1.399	top	c
C127	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.519	2.542	bom	c
C128	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	3.948	2.542	bom	c
C129	C-GEN0603	C0603	Capacitor,Surface Mount Pkg,General C0603	4.568	3.914	bom	c
CON1	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	1.108	2.243	top	c
CON2	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	1.164	2.545	top	c
CON3	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	1.478	2.743	top	c
CON4	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	0.579	0.455	top	c
CON5	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	0.582	1.308	top	c
CON6	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	1.676	-0.013	top	c
CON7	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	3.384	2.589	top	c
CON8	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	4.015	2.588	top	c
CON9	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	1.185	0.575	top	c
CON10	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	1.193	1.323	top	c
CON11	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	1.823	1.087	top	c
CON12	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	1.823	0.773	top	c
CON13	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	2.989	0.856	top	c
CON14	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	2.890	1.359	top	c
CON15	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	3.610	1.011	top	c
CON16	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	4.248	1.005	top	c
CON17	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	3.612	1.399	top	c
CON18	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector OSMT4	3.627	2.298	top	c

Comp	Part number	Part type	Description		Position x	Position y	Surface	Landout
CON19	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	4.375	0.162	top	c
CON20	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	5.230	1.692	top	c
CON21	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	4.855	1.674	top	c
CON22	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	4.290	1.985	top	c
CON23	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	5.033	2.929	top	c
CON24	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	5.369	3.069	btm	c
CON25	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	4.502	2.659	top	c
CON26	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	4.424	3.395	btm	c
CON27	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	3.372	2.930	btm	c
CON28	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	3.367	3.251	btm	c
CON29	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	2.535	3.226	top	c
CON30	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	2.550	3.111	btm	c
CON31	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	3.108	3.103	btm	c
CON32	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	2.450	2.572	top	c
CON33	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	3.040	2.575	top	c
CON34	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	3.161	2.311	top	c
CON35	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	3.061	2.301	btm	c
CON36	CO-180-OSMT4	OSMT4	OSMT 4 pin surface mount connector	OSMT4	1.102	1.902	top	c
CON37	CO-210-SMAJ	210SMAJ	SMA CONNECTOR,STRAIGHTJACK	210SMAJ	0.108	1.531	top	c
CON38	CO-210-SMAJ	210SMAJ	SMA CONNECTOR,STRAIGHTJACK	210SMAJ	0.077	3.057	top	c
CON39	CO-10-1040_V	CON40V	40 PIN CONNECTOR, .100" SPACING,VER	CON40V	3.755	3.692	top	a
D1	LED-SM2GW	LEDSM2GW	2LEDs,surface mount,gull wing	LEDSM2GW	0.255	0.375	top	c
D2	LED-SM1GW	LEDSM1GW	1LED,surface mount,gull wing	LEDSM1GW	0.077	0.705	top	c
D3	LED-SM1GW	LEDSM1GW	1LED,surface mount,gull wing	LEDSM1GW	0.001	2.042	top	c
FIL1	L-PA01TH8	PA01TH8	MiniCircuits LPF; nominal 21.4MHz	PA01TH8	2.841	2.297	top	a
FIL2	L-PA01TH8	PA01TH8	MiniCircuits LPF; nominal 21.4MHz	PA01TH8	2.836	1.856	top	a
FIL3	L-GEN14-6P	GEN6	14 pin pkg,6 pins,SAWTEK SAW Filter	GEN14_6P	5.079	2.135	btm	a
HDR1	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	5.222	0.706	btm	c
HDR2	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	1.999	0.867	btm	c
HDR3	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	2.191	0.705	btm	c
HDR4	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	2.191	0.991	btm	c
HDR5	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	2.005	1.153	btm	c
HDR6	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	3.010	0.814	btm	c
HDR7	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	2.655	0.141	btm	c
HDR8	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	3.744	1.095	btm	c
HDR9	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	4.844	1.546	btm	c
HDR10	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	4.498	0.641	top	c
HDR11	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	1.804	2.994	btm	c
HDR12	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	0.694	1.869	top	c
HDR13	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	4.576	0.249	top	c
HDR14	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	3.926	0.310	btm	c
HDR15	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	4.365	-0.043	btm	c
HDR16	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	1.611	2.643	btm	c
HDR17	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	0.556	1.817	btm	c
HDR18	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	2.237	0.857	top	c
HDR19	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	0.717	1.257	btm	c
HDR20	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	2.155	1.018	top	c
HDR21	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	3.019	-0.011	btm	c
HDR22	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	3.047	1.138	btm	c
HDR23	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	5.209	0.197	btm	c
HDR24	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	1.222	3.079	btm	c
HDR25	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	1.662	2.857	btm	c
HDR26	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	3.662	2.883	btm	c
HDR27	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	2.109	2.472	btm	c
HDR28	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	0.979	3.237	btm	c
HDR29	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	1.406	2.300	top	c
HDR30	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	3.661	0.033	btm	c
HDR31	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 3 PINS,2m	2002SMHDR	0.584	0.633	btm	c
HDR32	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	0.969	1.249	btm	c
HDR33	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	1.310	1.433	btm	c
HDR34	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	1.408	0.513	btm	c
HDR35	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	0.680	2.759	top	c
HDR36	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	2.003	3.377	btm	c
HDR37	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	1.032	3.605	top	c
HDR38	CO-200-2SMHDR	2002SMHDR	CONNECTOR,HEADER,1 ROW OF 2 PINS,2m	2002SMHDR	0.093	2.127	btm	c
L1	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General	C1206	4.288	1.201	top	c
L2	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General	C1206	4.081	1.717	top	c
L3	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General	C1206	4.329	2.311	top	c
L4	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General	C1206	0.513	0.645	top	c
L5	C-GEN1206	C1206	Capacitor,Surface Mount Pkg,General	C1206	0.513	1.117	top	c
POT1	R-SMPOTSTSW	SMPOTSTSW	Potentiometer- ST5W Package, SM	SMPOTSTSW	4.672	0.695	btm	c

Comp	Part number	Part type	Description		Position x	y	Surface	Leadout
POT2	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	2.989	2.642	btm	c
POT3	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	2.704	2.642	btm	c
POT4	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	1.780	2.315	top	c
POT5	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	2.687	1.264	top	c
POT6	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	4.076	0.469	top	c
POT7	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	2.093	2.080	top	c
POT8	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	1.044	3.101	top	c
POT9	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	0.693	2.626	top	c
POT10	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	1.088	2.748	top	c
POT11	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	2.079	1.639	top	c
POT12	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	0.775	0.237	top	c
POT13	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	1.402	0.551	top	c
POT14	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	0.978	1.616	top	c
POT15	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	1.396	1.551	top	c
POT16	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	0.978	1.283	top	c
POT17	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	0.788	0.584	top	c
POT18	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	3.174	1.022	top	c
POT19	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	4.732	0.184	btm	c
POT20	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	1.763	1.927	top	c
POT21	R-SMPOTST5W	SMPOTST5W	Potentiometer- ST5W Package, SM	SMPOTST5W	3.836	0.360	top	c
Q2	TR-GENSOT23	SOT23	Transistor, Surface Mount Pkg - SOT	SOT23	5.377	1.596	btm	c
Q3	TR-GENSOT23	SOT23	Transistor, Surface Mount Pkg - SOT	SOT23	0.544	2.803	btm	c
Q4	TR-GENSOT23	SOT23	Transistor, Surface Mount Pkg - SOT	SOT23	0.444	2.887	btm	c
Q5	TR-GENSOT23	SOT23	Transistor, Surface Mount Pkg - SOT	SOT23	1.118	3.048	btm	c
Q6	L-GENMQE000-6	MQE000_6	MQE000 Murata VCO	3.393	0.428	top	c	
Q7	TR-GENSOT23	SOT23	Transistor, Surface Mount Pkg - SOT	SOT23	1.115	2.971	btm	c
Q8	TR-GENSOT23	SOT23	Transistor, Surface Mount Pkg - SOT	SOT23	3.017	0.109	top	c
Q9	L-OS5SMT	OS5SMT	TCX Oscillator, Surface Mount, 5 lead,	OS5SMT	5.196	0.475	top	c
Q10	L-OS5SMT	OS5SMT	TCX Oscillator, Surface Mount, 5 lead,	OS5SMT	2.164	0.198	top	c
Q11	TR-GENTO52	TO52	Transistor, Dip Pkg - TO52, General	TO52	0.881	2.685	top	a
Q12	TR-GENTO52	TO52	Transistor, Dip Pkg - TO52, General	TO52	1.771	0.448	btm	a
Q13	TR-GENTO92	TO92	Transistor, TO92 pkg,General Part	TO92	1.362	3.222	btm	c
Q14	TR-GENTO92	TO92	Transistor, TO92 pkg,General Part	TO92	2.268	3.037	btm	c
Q15	TR-GENTO92	TO92	Transistor, TO92 pkg,General Part	TO92	2.649	0.012	btm	c
Q16	TR-GENTO92	TO92	Transistor, TO92 pkg,General Part	TO92	5.149	0.028	btm	c
Q17	TR-GENTO92	TO92	Transistor, TO92 pkg,General Part	TO92	3.931	0.817	btm	c
Q18	L-GENSO14NB	SO14NB	Surface Mount General Part - 14 pin	SO14NB	3.051	3.327	top	c
Q19	L-GENSO14NB	SO14NB	Surface Mount General Part - 14 pin	SO14NB	4.359	1.454	top	c
Q20	L-OS4DIP14	OS4DIP14	Crystal Osc Pkg, 4 pins, DIP 14 Pkg	OS4DIP14	1.529	3.029	top	a
Q21	L-FILBFA	FILBFA	Surface Mount Filter, Part #PO25BFA	FILBFA	4.505	1.985	top	c
Q22	L-FILBFA	FILBFA	Surface Mount Filter, Part #PO25BFA	FILBFA	3.492	1.594	top	c
Q23	L-GENMQE000-6	MQE000_6	Surface Mount, MQE000 package, 6 te	MQE000_6	5.282	1.187	top	c
R1	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	3.944	2.466	btm	c
R2	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	5.269	1.380	btm	c
R3	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.546	1.240	btm	c
R4	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	5.032	0.824	btm	c
R5	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.825	1.364	top	c
R6	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.427	0.582	btm	c
R7	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	5.262	1.481	btm	c
R8	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	5.420	1.481	btm	c
R9	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.348	0.833	btm	c
R10	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.614	1.006	btm	c
R11	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.645	0.484	btm	c
R12	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.189	1.717	top	c
R13	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.726	3.424	btm	c
R14	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.739	3.418	top	c
R15	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.695	3.321	btm	c
R16	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.876	2.673	top	c
R17	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	3.135	2.905	top	c
R18	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	3.071	3.040	top	c
R19	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.534	3.063	top	c
R20	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.448	2.891	top	c
R21	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.931	3.311	top	c
R22	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.600	2.009	top	c
R23	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.352	2.172	top	c
R24	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.364	1.800	top	c
R25	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.277	2.243	top	c
R26	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.929	3.105	top	c
R27	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.353	3.213	top	c
R28	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.414	3.078	btm	c
R29	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.343	2.949	top	c

Comp	Part number	Part type	Description		x	y	Position	Surface	Loadout
R30	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.557	3.060	btm	c	
R31	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.004	2.989	top	c	
R32	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.610	2.972	btm	c	
R33	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.846	2.879	top	c	
R34	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.851	3.315	btm	c	
R35	R-GEN1206	R1206	Resistor, Surface Mount Pkg,General	R1206	0.722	2.632	btm	c	
R36	R-GEN1206	R1206	Resistor, Surface Mount Pkg,General	R1206	0.953	2.863	btm	c	
R37	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.847	3.013	btm	c	
R38	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.849	3.094	btm	c	
R39	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.637	2.667	top	c	
R40	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.445	1.728	top	c	
R41	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	5.122	3.612	btm	c	
R42	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	5.120	3.763	btm	c	
R43	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	5.115	3.902	btm	c	
R44	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.342	3.871	btm	c	
R45	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.353	3.748	btm	c	
R46	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.327	3.633	btm	c	
R47	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.120	3.542	btm	c	
R48	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.582	0.265	top	c	
R49	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.633	0.806	top	c	
R50	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.404	0.658	top	c	
R51	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.404	0.799	top	c	
R52	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.387	1.218	top	c	
R53	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.633	1.054	top	c	
R54	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.572	1.481	top	c	
R55	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.427	1.074	top	c	
R56	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.220	-0.014	btm	c	
R57	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.006	0.999	btm	c	
R58	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.122	0.878	top	c	
R59	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.237	3.578	btm	c	
R60	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.233	3.459	btm	c	
R61	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.115	1.100	top	c	
R62	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.988	0.603	top	c	
R63	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.400	0.641	top	c	
R64	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.976	1.447	top	c	
R65	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.808	2.729	top	c	
R66	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	5.142	3.134	btm	c	
R67	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.330	3.407	top	c	
R68	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.683	3.042	top	c	
R69	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.920	3.035	top	c	
R70	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	1.236	1.727	top	c	
R71	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.938	0.349	top	c	
R72	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.942	0.266	top	c	
R73	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.777	0.090	top	c	
R74	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.897	0.603	top	c	
R75	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.865	0.582	btm	c	
R76	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.590	0.572	btm	c	
R77	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.213	0.319	btm	c	
R78	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.718	0.361	btm	c	
R79	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.137	0.240	btm	c	
R80	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	3.358	0.688	btm	c	
R81	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	2.654	0.787	top	c	
R82	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.008	1.319	btm	c	
R83	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	3.873	1.399	top	c	
R84	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	3.899	2.268	top	c	
R85	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.874	3.485	btm	c	
R86	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.866	3.593	btm	c	
R87	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.866	3.707	btm	c	
R88	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.863	3.848	btm	c	
R89	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.246	3.678	btm	c	
R90	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	0.254	3.794	btm	c	
R91	R-GEN1206	R1206	Resistor, Surface Mount Pkg,General	R1206	0.347	0.721	btm	c	
R92	R-GEN1206	R1206	Resistor, Surface Mount Pkg,General	R1206	0.377	0.313	btm	c	
R93	R-GEN1206	R1206	Resistor, Surface Mount Pkg,General	R1206	0.116	2.019	top	c	
R94	R-GEN1206	R1206	Resistor, Surface Mount Pkg,General	R1206	0.209	0.605	top	c	
R95	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	3.223	0.119	top	c	
R96	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	5.026	1.020	top	c	
R97	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.264	-0.135	btm	c	
R98	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.203	-0.135	top	c	
R99	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.268	0.766	btm	c	
R100	R-GEN0603	R0603	Resistor,Surface Mount Pkg,General	R0603	4.195	0.506	top	c	

Comp	Part number	Part type	Description		Position x	Position y	Surface	Leadout	
SWT1	SW-SMDP7	SWSMDP7	SURFACE MOUNT DIP SWITCH, 14 PIN	SWSMDP7	4.440	3.585	top	c	
SWT2	SW-SMDP7	SWSMDP7	SURFACE MOUNT DIP SWITCH, 14 PIN	SWSMDP7	0.837	3.855	top	c	
T1	L-PA03TH8	PA03TH8	MiniCircuits Transformer 16:1	PA03TH8	4.738	2.921	top	a	
T2	L-PA03TH8	PA03TH8	MiniCircuits Transformer 16:1	PA03TH8	5.367	3.297	bsm	a	
U1	L-GENTSOP20	TSOP20	Surface Mount,20 pin,thin shrink sm	TSOP20	4.825	0.997	top	c	
U2	L-GENTSOP20	TSOP20	Surface Mount,20 pin,thin shrink sm	TSOP20	2.832	0.307	top	c	
U3	L-GENSO14NB	SO14NB	Surface Mount General Part - 14 pin	SO14NB	3.711	1.832	bsm	c	
U4	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	4.557	0.252	bsm	c	
U5	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	2.896	2.863	top	c	
U6	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	1.880	2.774	bsm	c	
U7	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	2.662	2.859	top	c	
U8	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	0.631	2.071	bsm	c	
U9	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	1.428	0.829	top	c	
U10	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	0.922	0.550	bsm	c	
U11	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	1.431	1.077	top	c	
U12	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	3.332	0.406	bsm	c	
U13	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	3.246	1.175	top	c	
U14	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	3.897	1.224	top	c	
U15	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	3.698	2.565	top	c	
U16	L-GENSO20WB	SO20WB	Surface Mount General Part - 20 pin	SO20WB	4.327	2.878	top	c	
U17	L-GENSO8NB	SO8NB	Surface Mount General Part - 8 pin	SO8NB	1.380	1.988	top	c	
U18	L-GENTSOP20	TSOP20	Surface Mount,20 pin,thin shrink sm	TSOP20	4.880	3.830	bsm	c	
U19	L-GENSO16WB	SO16WB	Surface Mount General Part - 16 pin	SO16WB	0.846	2.971	top	c	
U20	L-GENSO14NB	SO14NB	Surface Mount General Part - 14 pin	SO14NB	2.529	1.152	top	c	
U21	L-GENTSOP20	TSOP20	Surface Mount,20 pin,thin shrink sm	TSOP20	0.680	3.774	bsm	c	

---------- END OF REPORT ----------

List of References

[1] Sam Sheng, *Ph.D. Dissertation*, Electronic Research Laboratory, UC Berkeley, to be published, 1995.

[2] S. Sheng, "Wideband Digital Portable Communications: A System Design," *Masters Thesis*, Electronic Research Laboratory, UC Berkeley, December 1991.

[3] R. C. Dixon, Spread Spectrum Systems, Second Edition, John Wiley & Sons, 1984.

[4] R. C. White, Jr., "Experiments With Digital Computer Simulation of Pseudo-Random Noise Generators," *IEEE Transaction on Electronic Computing*, June 1967.

[5] J. E. Salt, S. Kumar and D. Dodds, *Spread Spectrum for Indoor Wireless Communications*, TR Labs and National Wireless, 1991.

[6] T.S. Rappaport and S. Sandhu, "Radio-Wave Propagation for Emerging Wireless Personal-Communication Systems," IEEE Antennas and Propagation Magazine, vol. 36, pp. 14-24, October 1994.

[7] S. Y. Seidel, T. S. Rappaport, "914 MHz Path-Loss Prediction Models for Indoor Wireless Communications in Multi-floored Buildings, "IEEE Transactions on Antennas and Propagation, vol. 40,pp. 207-17, February 1992.

[8] A. M. Saleh, R. A. Valenzuela, "A Statistical Model for Indoor Multipath Propagation," IEEE Journal of Selected Areas of Communications, vol. SAC-5, pp. 128-137, February 1987.

[9] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, Third Edition, John Wiley & Sons, 1993.

[10] E. A. Lee and D. G. Messerschmitt, Digital Communications, Second Edition, Kluwer Academic Press, 1994.

[11] R. G. Meyer, *Advanced Analog for Communications Systems*, Class Notes, UC Berkeley, 1994.

[12] R. S. Carson, *Radio Concepts: Analog*, John Wiley & Sons, 1993.

[13] R. G. Meyer, W. D. Mack, "A 1-GHz BiCMOS RF Front-End IC," *IEEE J. Solid-State Circuits*, vol. 29, pp. 350-355, March 1994.

[14] R. G. Meyer, "Intermodulation in High-Frequency Bipolar Transistor Integrated - Circuit Mixers," IEEE J. Solid-State Circuits, vol. SC-21, August 1986.

[15] S. Y. Liao, *Microwave Circuit Analysis and Amplifier Design*, Prentice-Hall, 1987.

[16] G. T. Uehara, "Circuit Techniques and Considerations for Implementation of High Speed CMOS Analog-to-Digital Interfaces for DSP-Based PRML Magnetic Disk Read Channels," *Ph.D. Dissertation*, Electronic Research Laboratory, UC Berkeley, August 1993.

[17] *Transtech Ceramic Filter Component Specifications.*

[18] J. Smith, *Modern Communication Circuits*, McGraw-Hill, 1986.

[19] T. Weigandt, "Timing Jitter and Phase Noise in Ring-Oscillator Phase-Locked-Loops," UC Berkeley Internal Presentation, January 1994.

[20] H. W. Ott, Noise Reduction Techniques in Electronic Systems, Second Edition, John Wiley & Sons, 1988.

[21] H. W. Johnson and M. Graham, High-Speed Digital Design, PTR Prentice Hall, 1993.

[22] The American Radio Relay League, *The ARRL Handbook*, Seventy-First Edition, ARRL, 1994.

[23] E. McCune, "Ground Current Control in RF and High Speed Digital Circuits," *RF Expo West Conference Proceedings*, RF Design, 1994.

[24] R. G. Meyer, "High Frequency IC Design Techniques," UC Berkeley IC Seminar, 1993.

[25] T. A. Jerse, "Shielding Basics," *RF Design*, March 1990.

[26] T. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter," IEEE J. Solid-State Circuits, vol. 30, pp. 166-172, March 1995.

[27] C. Teuscher and S. Sheng, Private Conversation.

[28] F. W. Grover, *Inductance Calculations*, Dover Publications, 1962.

[29] M. E. Goldfarb and R. A. Pucel, "Modeling Via Hole Grounds in Microstrip," *IEEE Microwave and Guided Wave Letters*, vol. 1, pp. 135-137, June 1991.

[30] Hewlett Packard, *RF & Microwave Phase Noise Measurement Seminar Notes*, HP.

[31] E. A. Lee and D. G. Messerschmitt, Digital Communications, First Edition, Kluwer Academic Press, 1988.

[32] Murata Electronics, *RF and Microwave Products Catalog*, 1994.

[33] L. Lynn, K. Stone, S. Sheng, Personal Conversation.

[34] K. Onodera, "Low Power Analog Correlator for Direct Sequence Spread Spectrum Systems," *Industrial Liaison Program Conference*, UC Berkeley, March 1994.

[35] I. Bahl and P. Bhartia, *Microwave Solid State Circuit Design*, John Wiley & Sons, 1988.

[36] B. C. Wadell, *Transmission Line Design Handbook*, Artech House, 1991.

[37] A. B. Williams and F. J. Taylor, *Electronic Filter Design Handbook*, Second Edition, McGraw-Hill, 1988.

[38] S. Sheng and C. Teuscher, "Wideband Digital Portable Communications," *UC Berkeley Industrial Liaison Conference*, March 1994.

[39] W. C. Lee, *Mobile Cellular Telecommunications Systems,"* McGraw-Hill, 1989.

Bibliography

[1] G. D. Vendelin, A. M. Pavio and U. L. Rohde, *Microwave Circuit Design Using Linear and Non-Linear Techniques*, John Wiley & Sons, 1990.

[2] F. M. Gardner, *Phaselock Techniques*, John Wiley & Sons, 1979.

[3] D. K. Cheng, *Field and Wave Electromagnetics*, Second Edition, Addison Wessley, 1989.

[4] S. Ramo, J. R. Whinnery and T. Van Duzer, *Fields and Waves in Communication Electronics*, Second Edition, John Wiley & Sons, 1984.

[5] U. L. Rohde and T. T. Bucher, *Communication Receivers: Principles and Design*, McGraw-Hill, 1988.

[6] S. A. Maas, *Nonlinear Microwave Circuits*, Artech House, 1988.

[7] R. G. Meyer, W. D. Mack, "A wideband low-noise variable-gain BiCMOS transimpedance amplifier," *IEEE J. Solid-State Circuits*, vol.29, pp. 701-706, June 1994.

[8] C. D. Hull and R. G. Meyer, "A systematic approach to the analysis of noise in mixers," *IEEE Transactions on Circuits and Systems*, vol. 40, pp. 909-919, December 1993.

[9] N. M. Nguyen and R. G. Meyer, "A 1.8 GHz monolithic LC voltage-controlled oscillator," *1992 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 158-159, February 1992.

[10] C. Conroy, "A High-Speed Parallel Pipeline A/D Converter Technique in CMOS," *Ph.D. Dissertation*, Electronic Research Laboratory, UC Berkeley, 1994.

[11] A. P. Chandrakasan, A. Burstein and R. W. Brodersen, "A low-power chipset for a portable multimedia I/O terminal," *IEEE J. Solid-State Circuits*, vol. 29., pp. 1415-1428, December 1994.

[12] R. W. Brodersen, A. Chandrakasan and S. Sheng, "Design techniques for portable systems," *1993 IEEE International Solid-State Circuits Conference Proceedings*, pp. 168-169, February 1993.

[13] S. Sheng, A. Chandrakasan and R. W. Brodersen, "A portable multimedia terminal," *IEEE Communications Magazine*, vol. 30, pp. 64-75, December 192.

[14] A. P. Chandrakasan, S. Sheng and R. W. Brodersen, "Low Power CMOS Digital Design," *IEEE J. Solid-State Circuits*, vol. 27, pp.473-484, April 1992.

[15] C. Conroy, D. W. Cline, and P. R. Gray, "An 8-b 85-MS/s Parallel Pipeline A/D Converter in 1-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 28, pp 447-454, April 1993.

[16] S. Sheng and C. Teuscher, "Wideband Digital Portable Communications," *UC Berkeley Industrial Liaison Conference*, March 1994.

[17] M.J. Feuerstein, et. al., "Path loss, delay spread, and outage models as functions of antenna height for micro-cellular system design," *IEEE Transactions on Vehicular Technology*, vol. 43, pp. 487-98, August 1994.

[18] J. C. Liberti and T. S. Rappaport, "Analytical results for capacity improvements in CDMA," *IEEE Transactions on Vehicular Technology*, vol. 43, pp. 680-690, August 1994.

[19] S. Y. Seidel and T. S. Rappaport, "A ray tracing technique to predict path loss and delay spread inside buildings," *IEEE Global Telecommunications Conference Abstracts*, vol. 2, pp. 649-653. December 1992.

[20] M. J. Feuerstein and T. S. Rappaport, ed., *Wireless Personal Communications*, Kluwer Academic Publishers, 1993.

[21] T. S. Rappaport, et. al, eds., *Wireless Personal Communications: Trends and Challenges*, Kluwer Academic Publishers, 1994.

[22] D. O. Pederson and K. Mayaram, *Analog Integrated Circuits for Communication*, Kluwer Academic Press, 1991.

In addition, application notes and specification sheets from many vendors including those listed below were used as reference material.

[23] Comlinear

[24] Elantec

[25] Analog Devices

[26] Transtech

[27] National Semiconductor

[28] Philips Semiconductor

[29] RF Microdevices

[30] Sawtek

[31] Maxim

[32] Hewlett Packard

[33] Murata