CMOS BASELINE PROCESS
IN THE
UC BERKELEY MICROFABRICATION LABORATORY

by

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in the

UC Berkeley Microfabrication Laboratory

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Abstract

This project describes the characterization of the Berkeley CMOS Baseline, a joint project by several research groups. The process supports 2 μm n-well technology, with double poly-Si, double metal, and defines the standard process modules in the Microlab. Statistical process control data, geometric design rules and BSIM3 SPICE model parameters are presented.

CMOS Baseline Process in the UC Berkeley Microfabrication Laboratory

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1 Introduction

In an educational laboratory like the UC Berkeley Microfabrication Laboratory, each project is different and students need to identify a starting point from which they can carry on their own research. This is one of the reasons why the Microlab reestablished the baseline CMOS process in April 1992, based on the previous Microlab CMOS process [1]. The baseline also serves to monitor CMOS process equipment, to quickly discover and fix process problems, and to specify standard process modules for VLSI operations. We have developed both p-well and n-well, 2 μm, double poly and double metal CMOS processes and while these are running we embarked upon developing a 1.3 μm, twin-well, double poly, double metal CMOS process.

Our baseline provides "standard" CMOS circuits to various research groups. The advantage is that the designers are close to processing, can follow it in detail, can feedback their circuit performance results to process engineering and thus improve the process. The baseline has fabricated lots for several research groups: The Berkeley Sensor and Actuator Center (BSAC), the Berkeley Computer Aided Manufacturing (BCAM) group, the Solid-State Devices and Technology group, the Cryoelectronics Research group, and the Integrated Circuits group. The baseline process consists of standard steps. Each process step can also be used as a process module by different groups for their own process design.

Statistical process control (SPC) has been applied to the baseline. Standard in-line measurements have been established to monitor critical steps. The electrical test structures, designed by David Rodriguez [2] for testing on an automatic probe station, enable collection of statistical data. The test structures are placed in the scribe lanes of each wafer. Tests are performed on each wafer and

the resulting data are statistically analyzed to determine whether the process is in control.

During the development of our baseline process, we compared the n-well and p-well processes and found that the n-well process has the advantage of fewer process steps, easier threshold voltage control, and better device performance. In this memo we will describe the n-well CMOS baseline process in detail, with process simulations, materials characterization and electrical measurement results. Process and device parameter targets and circuit design rules are also included.

2 Process Design

The Microlab's 2 μm, double poly and double metal CMOS process was designed mainly for analog circuit fabrication. The objective is to fabricate good performance 2 μm CMOS circuits with a simple and stable process. The process has 5 implant steps and 11 lithography steps. The starting material is a 4" 8-12 Ω-cm p-type, <100> wafer, on which 2μm N-channel MOSFETs can be fabricated without a punchthrough implant. There is no n-field implant, because the phosphorus concentration at the n-well surface is high enough for a field threshold voltage greater than 12V. The baseline process specifications are given in Appendix A.

2.1 Process Flow and Cross Sections

A brief process flow with device cross sections is shown in Figure 1. All the process steps are done in the Microlab with the exception of ion implant steps, which are carried out at Ion Implant Services (Sunnyvale, California). The detailed information is in the process outline in Appendix C, which includes the equipment used in the Microlab for the CMOS process.

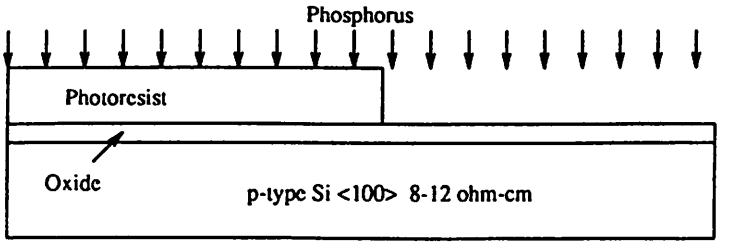
Ion Implantations

Process Step	Species	Energy (KeV)	Dose (/cm^2)
Well Implant	Phosphorus	150	$5x10^{12}$
P-Field Implant	Boron	70	$1.5x10^{13}$
Threshold Adjustment Implant	Boron	30	$1.7x10^{12}$
N+ S/D Implant	Arsenic	160	$5x10^{15}$
P+ S/D Implant	Boron	30	$5x10^{15}$

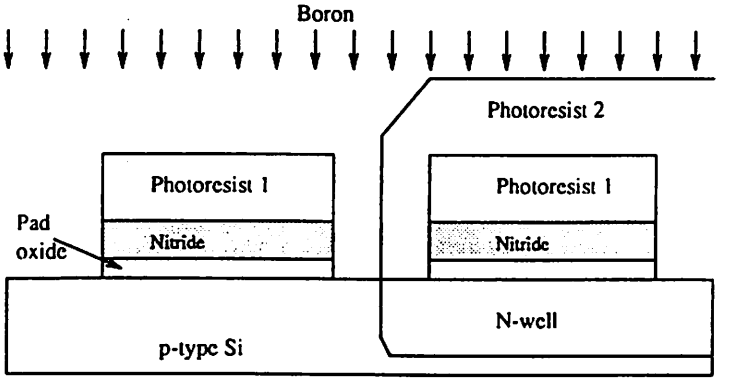
2.2 Mask Definitions

Mask Name	Type	Field	Align Sequence
NWELL	chrome	dark	
ACTIVE	emulsion	clear	NWELL
PFIELD	emulsion	clear	ACTIVE
POLY	emulsion	clear	ACTIVE
CAP-CE	emulsion	clear	POLY
N+ S/D	chrome	dark	POLY
P+ S/D	emulsion	clear	POLY
CONT	chrome	dark	POLY
METAL1	emulsion	clear	CONT
VIA	chrome	dark	METAL1
METAL2	emulsion	clear	VIA

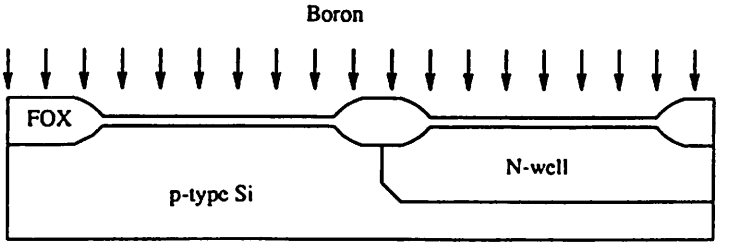
2 um CMOS Process Flow and Cross Sections



1. Initial oxidation: 100nm oxide
2. Well photo
3. Well implant:
   phosphorus, 150KeV, 5×10^{12} /cm^2

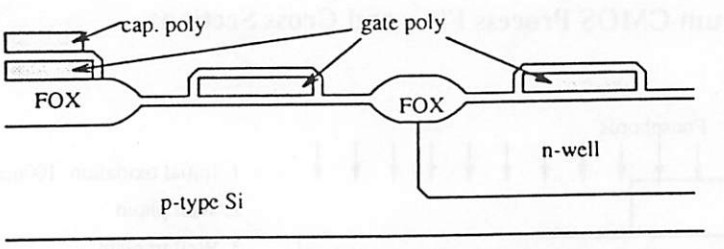


4. Well drive-in: Xj = 3.4um
5. Pad oxidation: 30 nm
6. Nitride deposition: 100nm
7. Active area photo (PR1)
8. Nitride etch
9. P-field photo (PR2)
   double photoresist process
10. P-field implant:
    boron, 70KeV, 1.5×10^{13} /cm^2

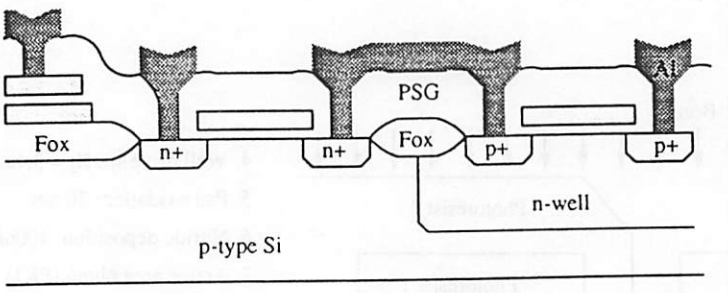


11. LOCOS:
    field oxide (FOX): 650-700nm
12. Nitride removal
13. Pad oxide removal
14. Sacrificial oxide: 20nm
15. Threshold implant:
    boron, 30KeV, 1.7×10^{12} /cm^2

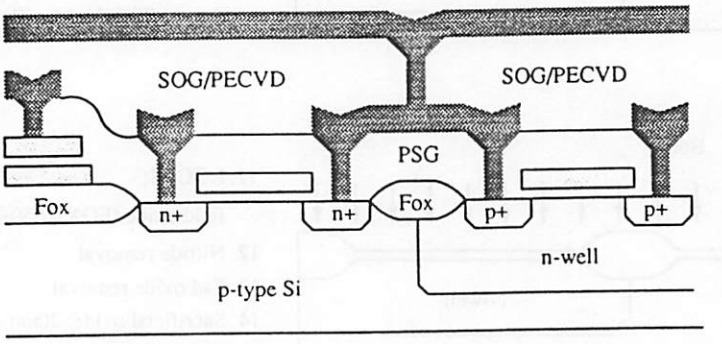
Fig. 1 Process flow and cross sections.



16. Sacrificial oxide removal
17. Gate oxidation: 30nm
18. Gate poly deposition: 450nm
19. Gate poly photo
20. Gate poly etch
21. Capacitor oxidation: 80nm on poly
22. Capacitor poly deposition: 450nm
23. Capacitor photo
24. Capacitor etch



25. N+ S/D photo
26. N+ S/D implant
As, 160KeV, $5x10^{15}$/cm^2
27. N+ S/D anneal
28. P+ S/D implant
B, 30KeV, $5x10^{15}$/cm^2
29. PSG deposition: 700nm and densification
30. Contact photo
31. Contact etch
32. Al sputtering: 600nm
33. Al definition



34. PECVD thin oxide: 40nm
35. Spin-On-Glass 500nm
36. PECVD thick oxide: 300nm
37. VIA photo
38. VIA etch
39. Al sputtering: 800-900nm
40. Al photo
41. Al Etch
42. Sintering

Fig. 1 (cont.) Process flow and cross sections.

3 Process Simulation and Material Characterization

The results of SUPREM3 and Spreading Resistance Analysis (SRA) are presented here. The SRA was performed by Solecon Laboratories (San Jose, CA). The SRA samples were made from the lot cmos39.

3.1 N-Channel

Doping profiles in the N-channel region are shown in Figures 2 and 3. The simulated gate oxide thickness is 29.2 nm. The simulated surface concentration ($3.9x10^{16}/cm^2$) is about two times of that from SRA ($2x10^{16}/cm^2$). In Section 4, we will see the SRA result is close to the statistical data obtained from electrical measurements on cmos39. See Figure 24 (a).

3.2 P-Channel

Figures 4 and 5 are the doping profiles in the P-channel region. From simulation, the well junction depth and threshold implant junction depth are 3.4231 and 0.24135 μm, respectively. SRA data show a shallower N-well junction of 2.748 μm and no threshold implant junction. However, SRA P^+ source-drain profile in Figure 9 shows an N-well junction depth of 3.224 μm which is close to the simulation result.

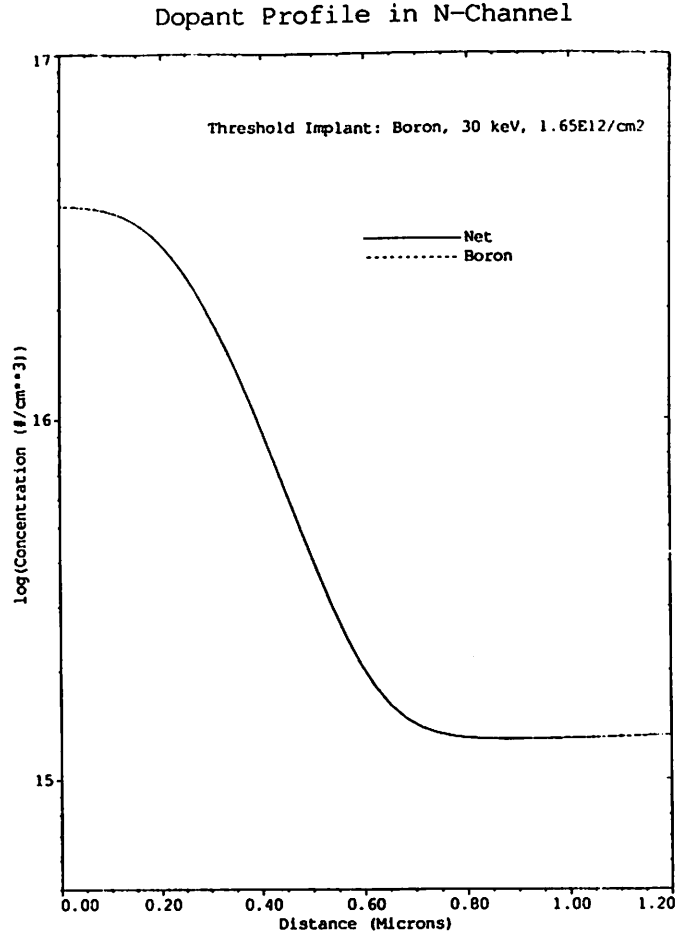


Fig. 2 N–channel dopant profile simulated by SUPREM3.

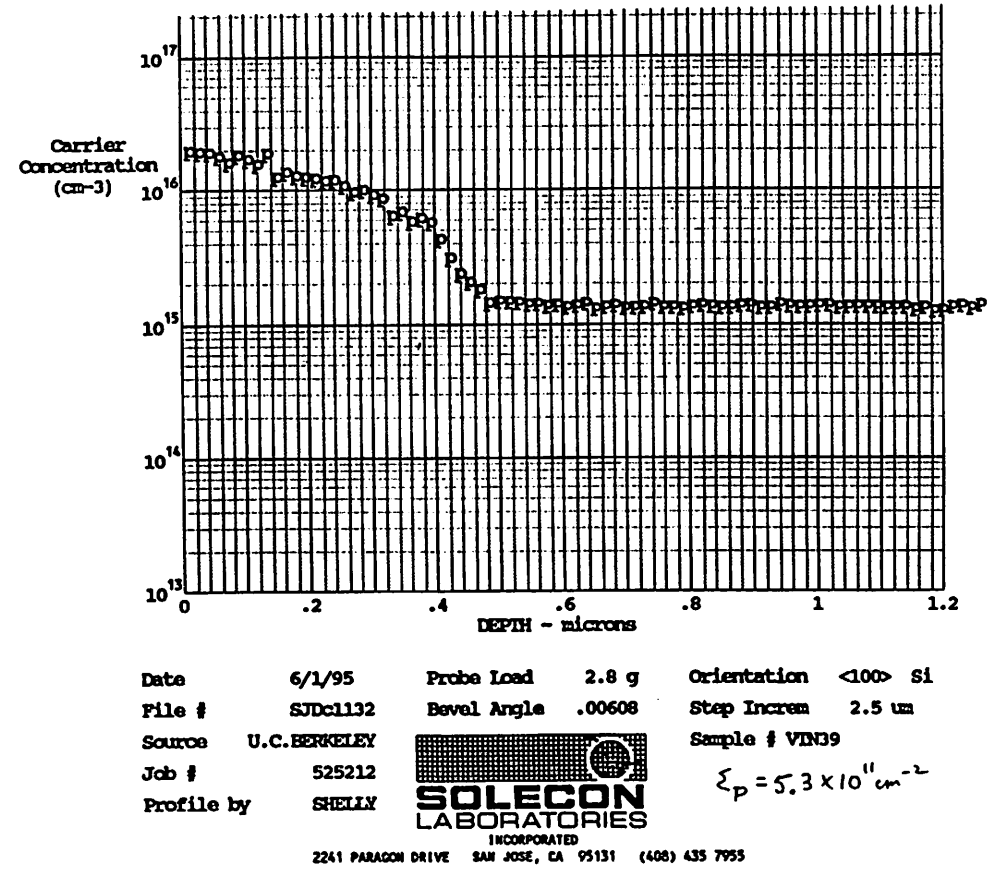


Fig. 3 N–channel dopant profile obtained from SRA.

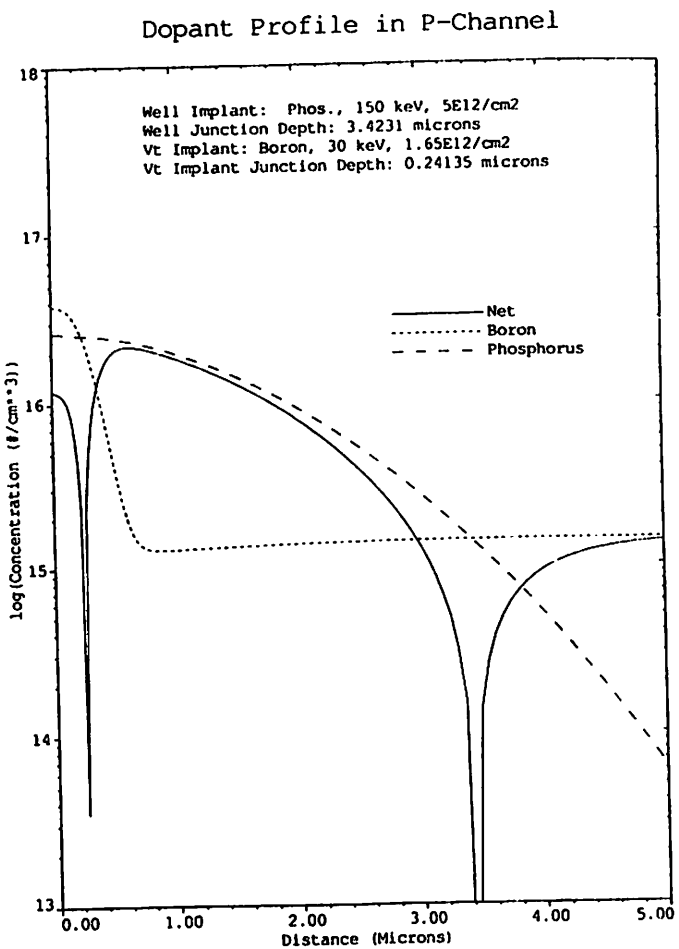


Fig. 4 P–channel dopant profile simulated by SUPREM3.

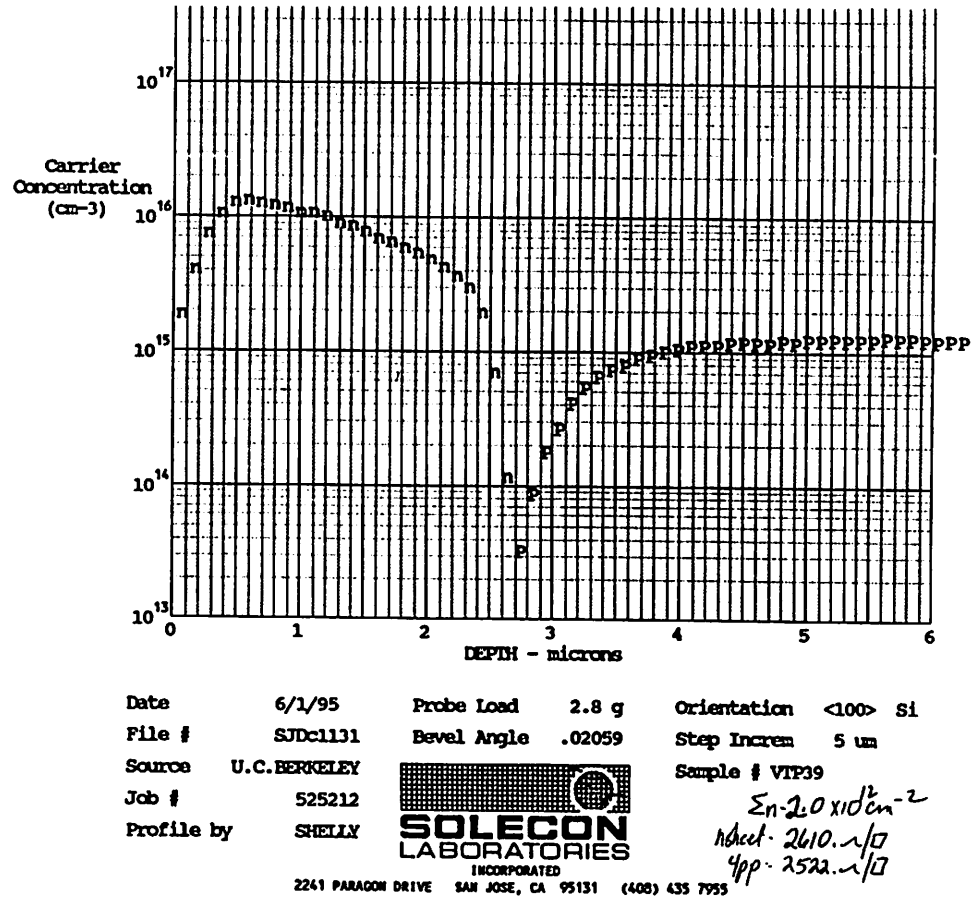


Fig. 5 P–channel dopant profile obtained from SRA.

3.3 N^+ Source-Drain

The simulated As doping profile (Fig.6) shows a tail which results in a junction depth of 0.7 μm. An extrapolation of the doping profile without the tail gives a junction depth of 0.31 μm which agrees with the SRA result (Fig. 7). The sheet resistance calculated from SRA and measured with the four-point probe on the same sample are 38 and 37 Ω/square, respectively. From electrical measurement, the average sheet resistance is 43.64 Ω/square (Fig. 29 (a)).

Parameter	Simulated	Measured from SRA sample	Calculated from SRA	Electrical Measurement
Junction Depth, X_j (μm)	0.31	0.313		
Sheet resistance (Ω/square)		38	37	43.64

3.4 P^+ Source-Drain

The simulated junction depth (Fig.8) is 0.55784 μm, while the SRA junction depth (Fig 9) is 0.645 μm. The sheet resistance calculated from SRA is 67 Ω/square. The four-point probe measurement on the same sample shows 51 Ω/square. Both are within the range from 51.5 to 67.5 Ω/square as can be seen from the average of electrical measurements (Fig. 30 (a)).

Parameter	Simulated	Measured from SRA sample	Calculated from SRA	Electrical Measurement
Junction Depth, X_j (μm)	0.55784	0.645		
Sheet resistance (Ω/square)		51	67	59.5

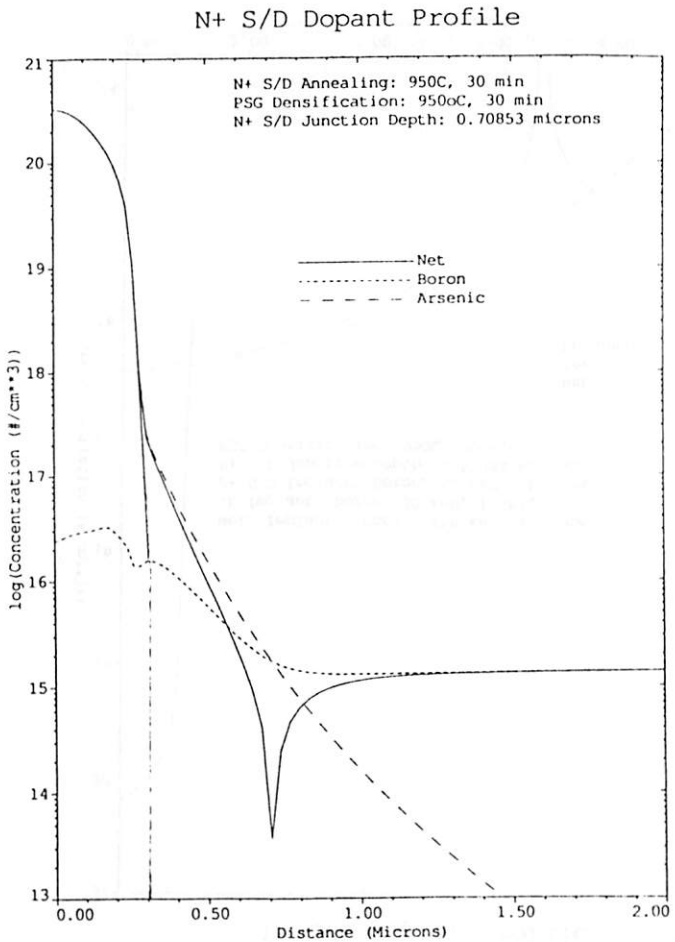


Fig. 6 N+ source−drainl dopant profile simulated by SUPREM3.

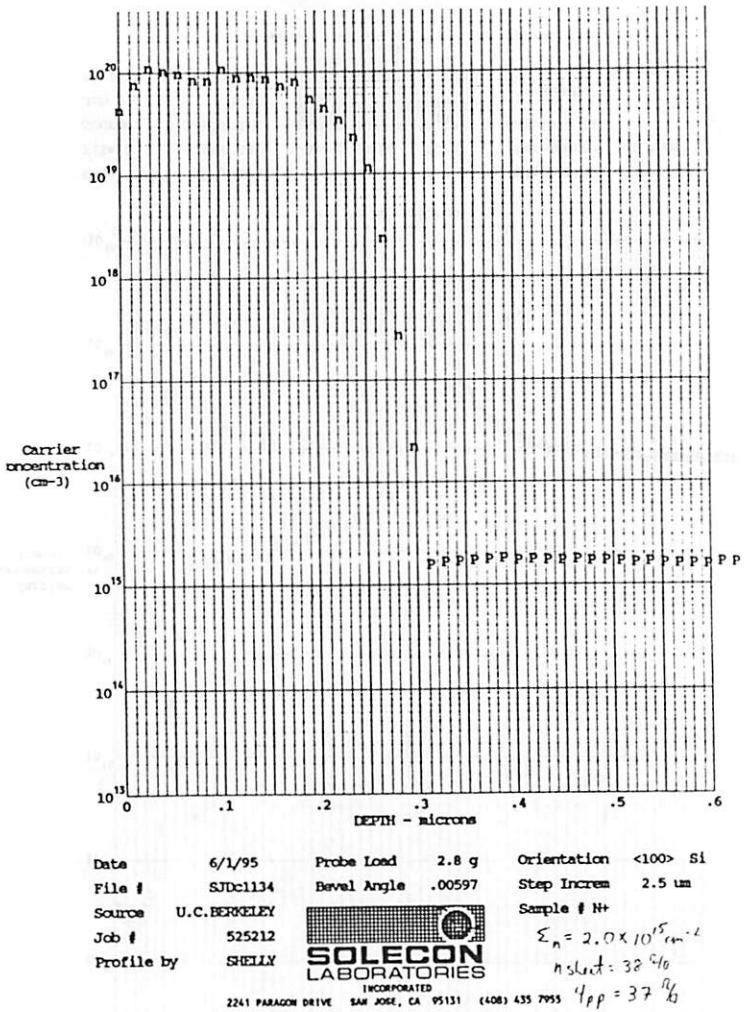


Fig. 7 N+ source−drain dopant profile obtained from SRA.

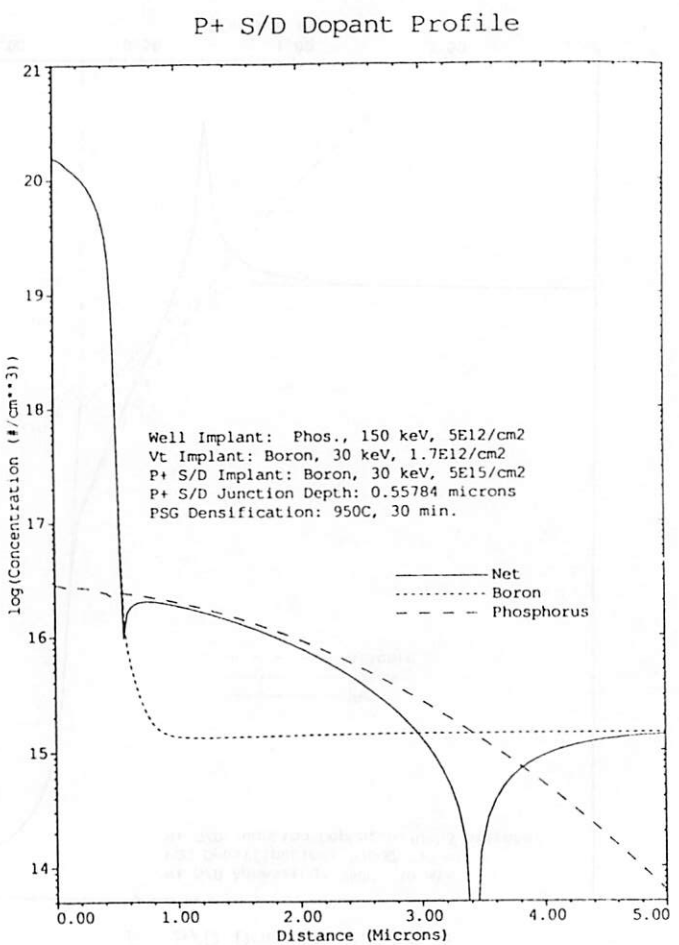


Fig. 8 P+ source–drainl dopant profile simulated by SUPREM3.

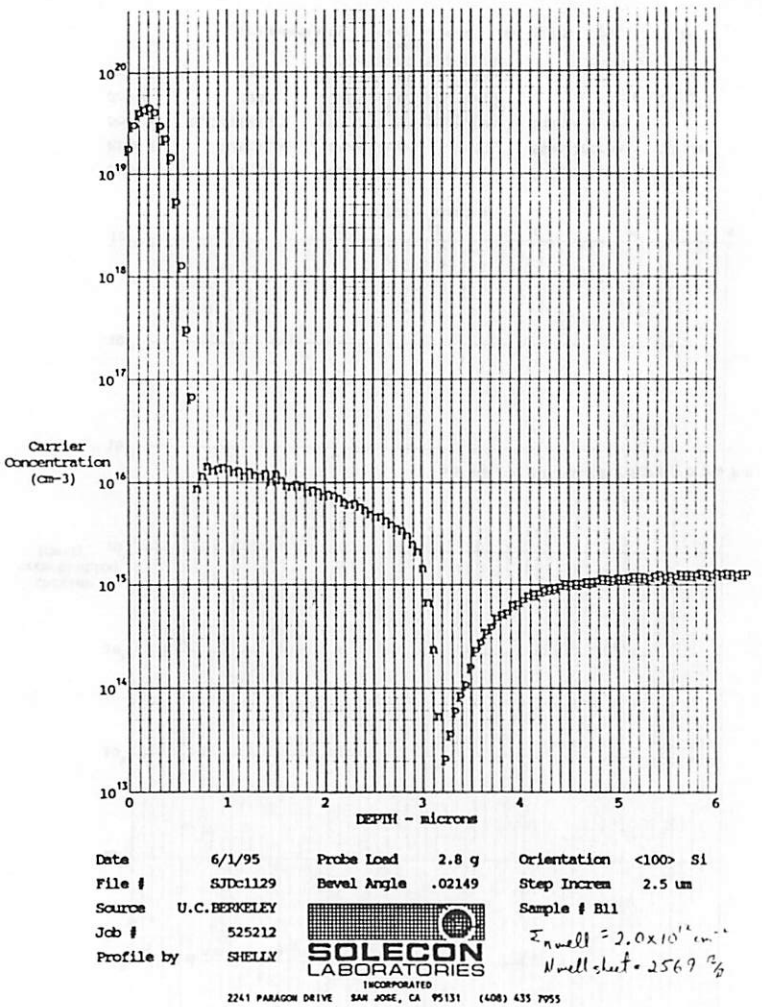


Fig. 9 P+ source–drain dopant profile obtained from SRA.

4 Electrical Measurement Results

The HP4145 Semiconductor Parameter Analyzer and an automatic probe station (autoprober) were utilized to make electrical measurements on each lot. The autoprober consists of the Electroglas Model 2001X, an HP 4085A Switching Matrix, an HP4084 Switching Matrix Controller, an HP4141A Source/Monitor and a UNIX workstation. The test structures for the autoprober were designed by D. Rodriguez [2] and they were included in the scribe line of each wafer.

4.1 HP4145 Measurement Results

Figures 10 through 15 are NMOS and PMOS characteristics measured with HP4145. Both devices have W/L of 10/2.

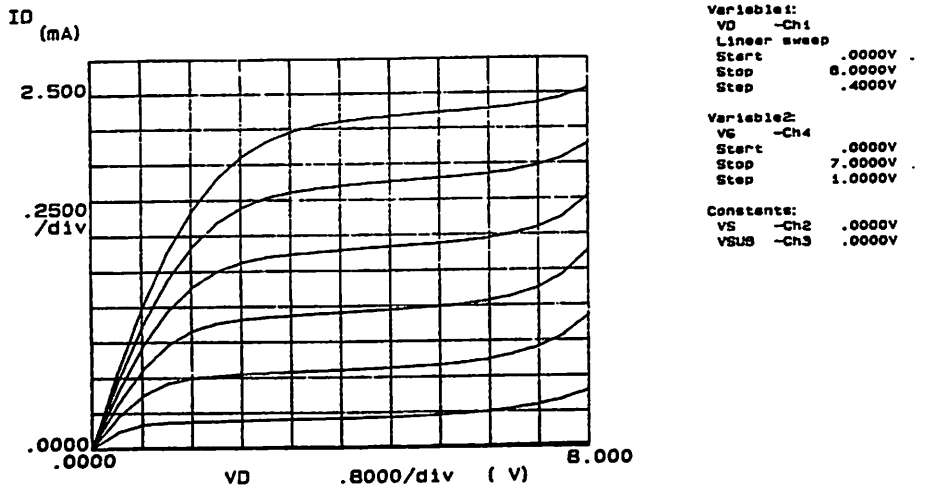
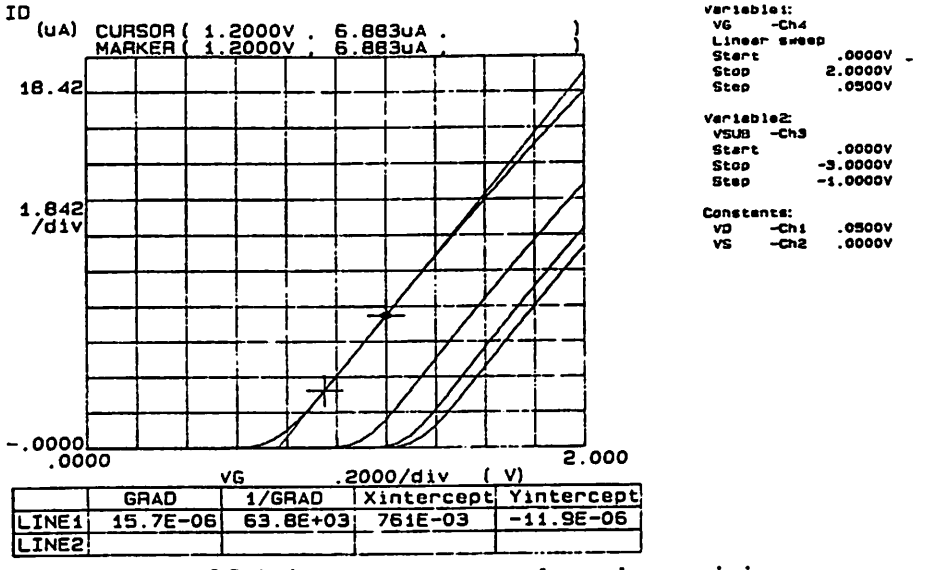
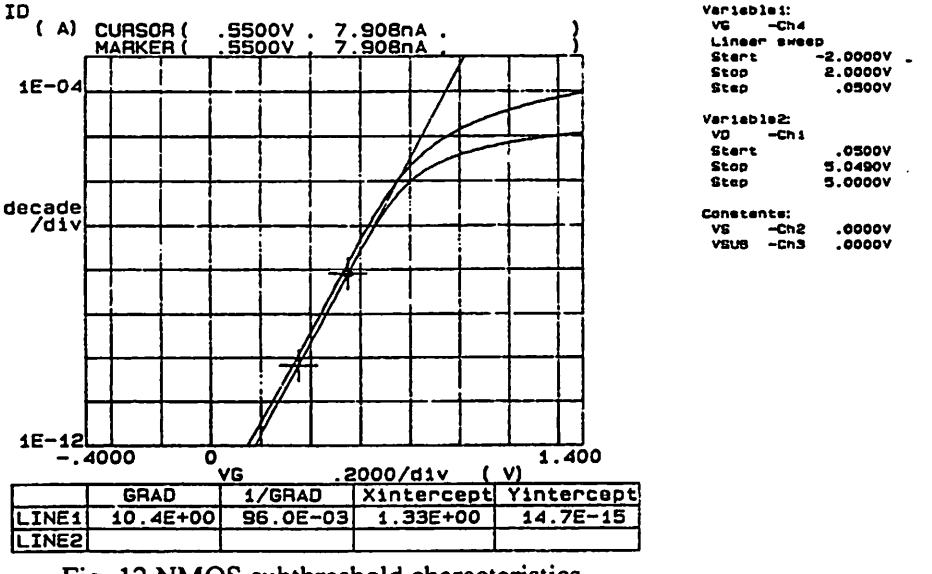


Fig. 10 NMOS drain current vs. drain voltage characteristics.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	15.7E-06	63.8E+03	761E-03	-11.9E-06
LINE2				

Fig. 11 NMOS drain current vs. gate voltage characteristics.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	10.4E+00	96.0E-03	1.33E+00	14.7E-15
LINE2				

Fig. 12 NMOS subthreshold characteristics.

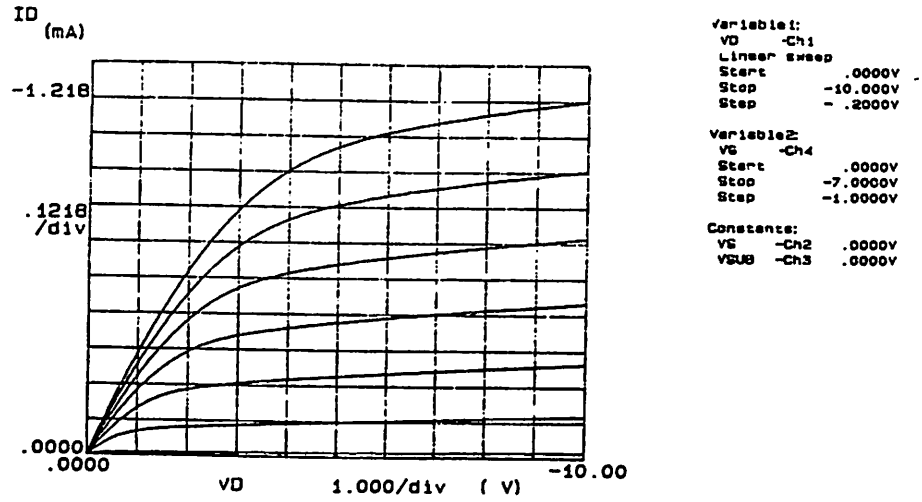
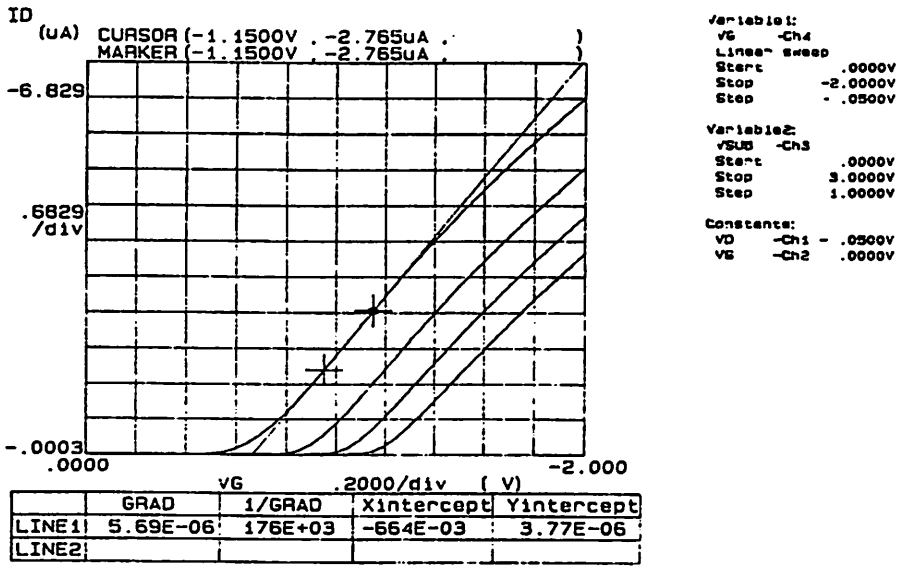
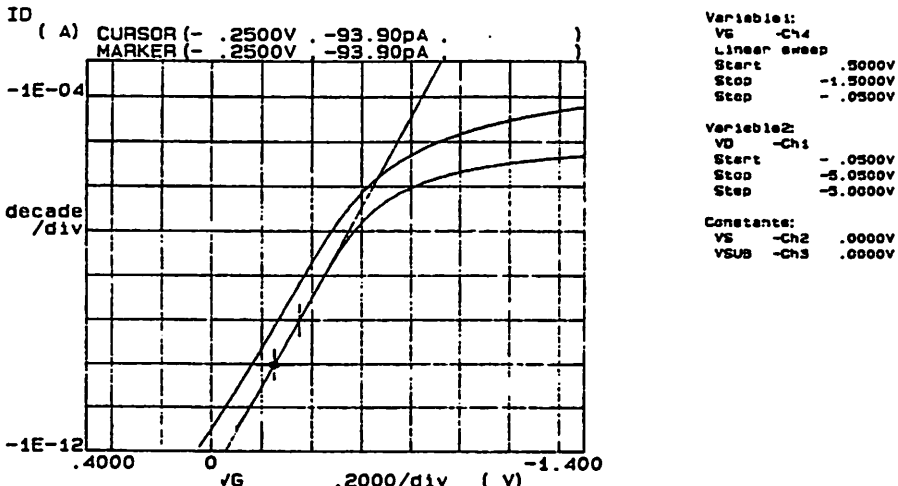


Fig. 13 PMOS drain current vs. drain voltage characteristics.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	5.69E-06	176E+03	-664E-03	3.77E-06
LINE2				

Fig. 14 PMOS drain current vs. gate voltage characteristics.



	GRAD	1/GRAD	Xintercept	Yintercept
LINE1	-10.1E+00	-98.5E-03	-1.24E+00	-273E-15
LINE2				

Fig. 15 PMOS subthreshold characteristics.

4.2 Statistical Measurement Data

Autoprober testing enables the baseline to collect large amounts of data for monitoring the process and extracting device parameters. Figures 16 through 31 are the statistical results from autoprober measurements. For threshold voltage, fifty-two dies across each wafer were tested and for other parameters, ten to twenty dies across each wafer were measured. These measured dies were uniformly distributed across the wafer. Two sets of data, (a) and (b), are presented here. In (a), each data point is the average of the measurements on one wafer and is connected by a line indicating a process lot. Avg is the average of the data points in the figures, which is the average of a wafer. UCL and LCL stand for Upper and Lower Control Limits, respectively. In (b), each point is the standard deviation across the wafer corresponding to the point in (a).

In effective channel length and width measurements (Fig.18-21), the resistance and conductance methods [3,4] were used. L_d and W_d are the parameters in the following equations:

$$L_{eff} = L - \Delta L = L - 2L_d,$$

$$W_{eff} = W - \Delta W = W - 2W_d.$$

In Figures 22 and 23, k'_n and k'_p are the current factors μC_{ox} /2 and were measured while the devices were at saturation.

Since the dopant concentration is not uniform in the ion-implanted channel regions, γ_1 and γ_2 were extracted at low and high substrate bias [5,6]. Based on these results, dopant concentrations at the surface and substrate (or n-well for PMOS) were obtained. The surface dopant concentrations are shown in Figures 24 and 25. The surface doping concentrations measured this way can be used to monitor the process, although they are not precise surface doping concentration measurements.

In Figures 27 and 30, cmos39 was not included, because BF_2 was implanted to make shallow P^+ S/D junctions for investigation of 1.3 μm PMOS.

Both NMOS and PMOS source-drain leakage currents were also measured at V_{ds}=5V and V_{gs}=0V on the wafer cmos40-1. Fifty-two dies were tested across the wafer. The leakage current average and standard deviation for NMOS and PMOS are 0.855pA/μm and 0.0487pA/μm, and -1.99pA/μm and 0.9546pA/μm, respectively.

A summary of the measurements, Process and Device Parameter Targets, is attached in Appendix A. These parameters will be updated with the improvements in the baseline process. Some capacitance parameters will be added after the autoprober capacitance measurement routines are available to extract capacitance parameters.

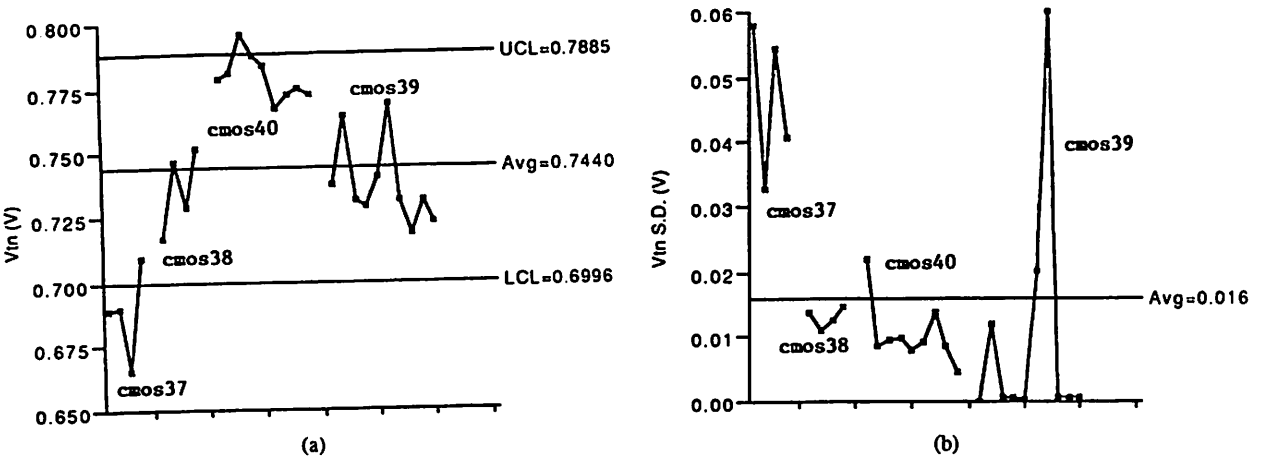


Fig. 16 (a) NMOS threshold voltage distribution in the 2um N-well CMOS process. Each data point is the average of fifty-two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

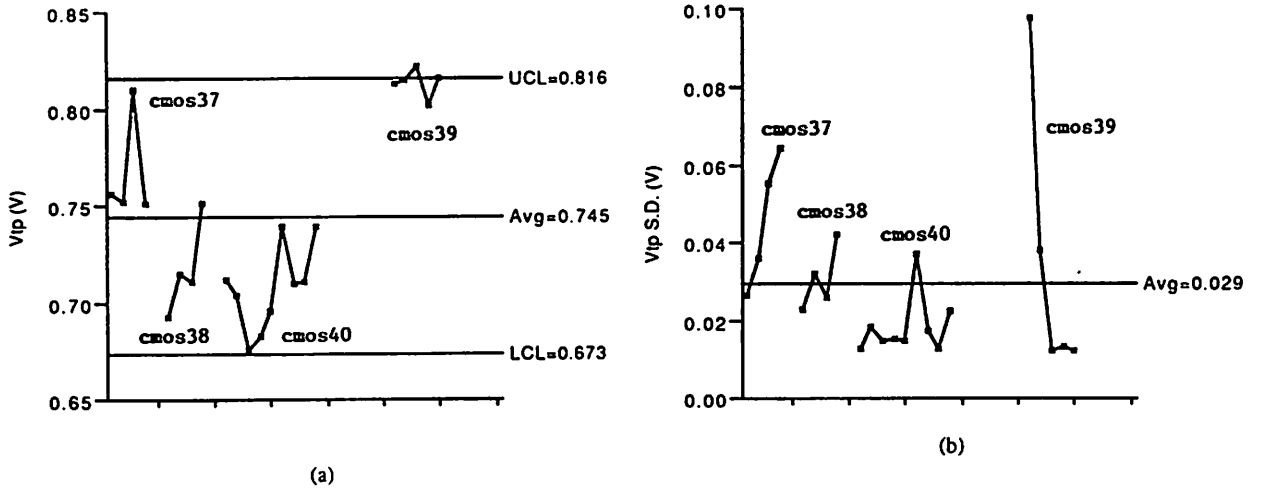


Fig. 17 (a) PMOS threshold voltage distribution in the 2um N-well CMOS process. Each data point is the average of fifty-two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

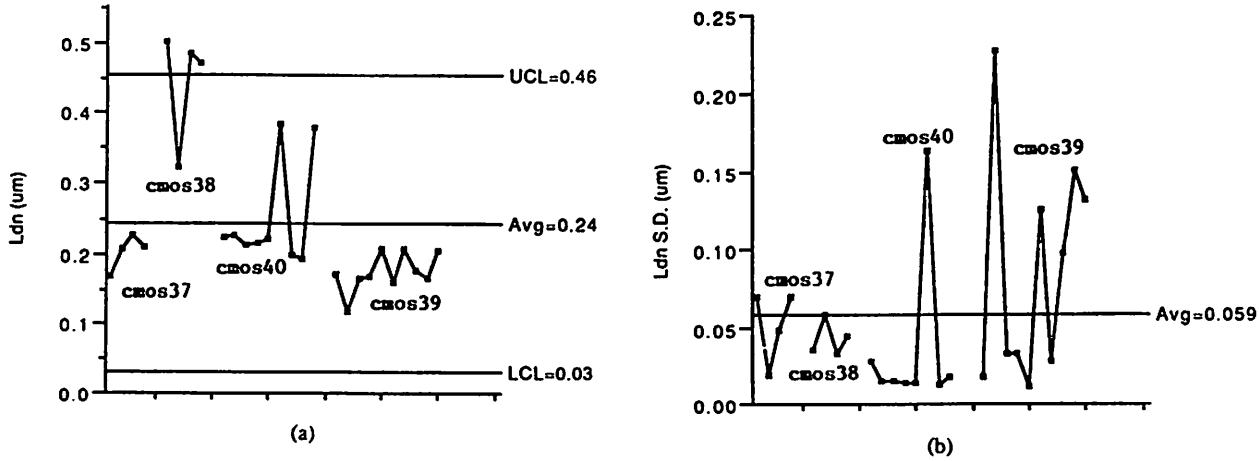


Fig. 18 (a) NMOS effective channel length distribution in the 2um N-well CMOS process. Each data point is the average of fifty-two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

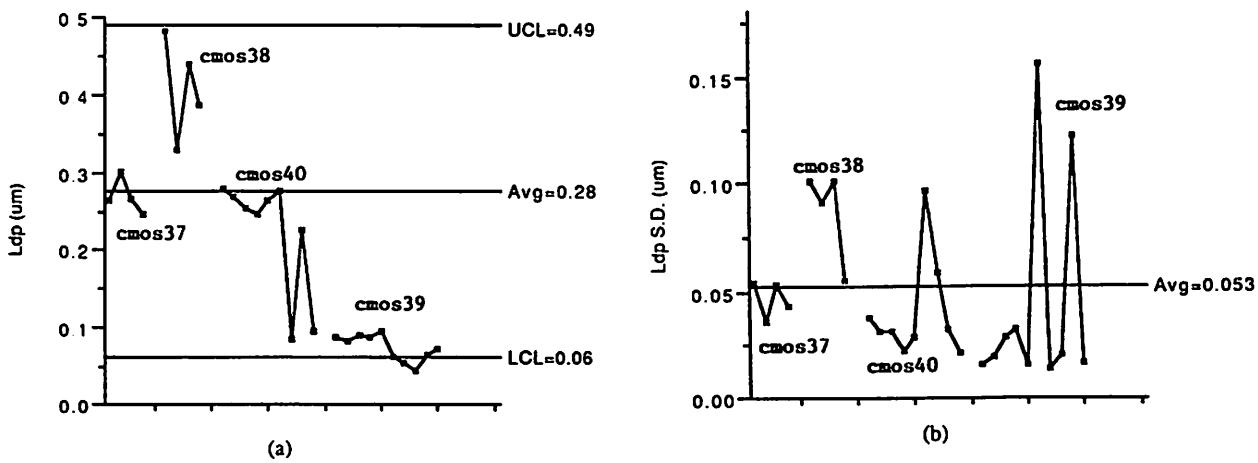


Fig. 19 (a) PMOS effective channel length distribution in the 2um N-well CMOS process. Each data point is the average of fifty-two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

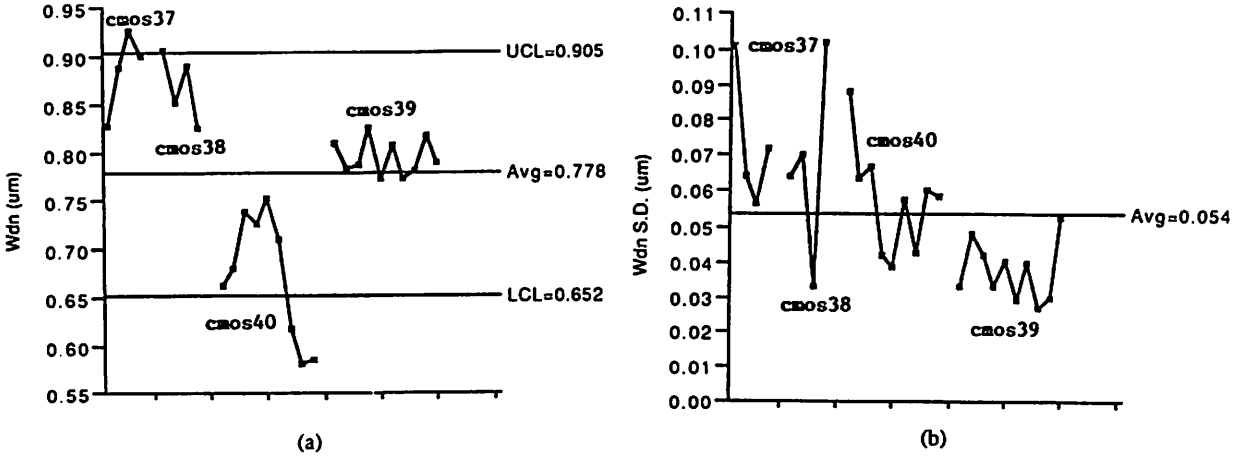


Fig. 20 (a) NMOS effective channel width distribution in the 2um N-well CMOS process. Each data point is the average of fifty-two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

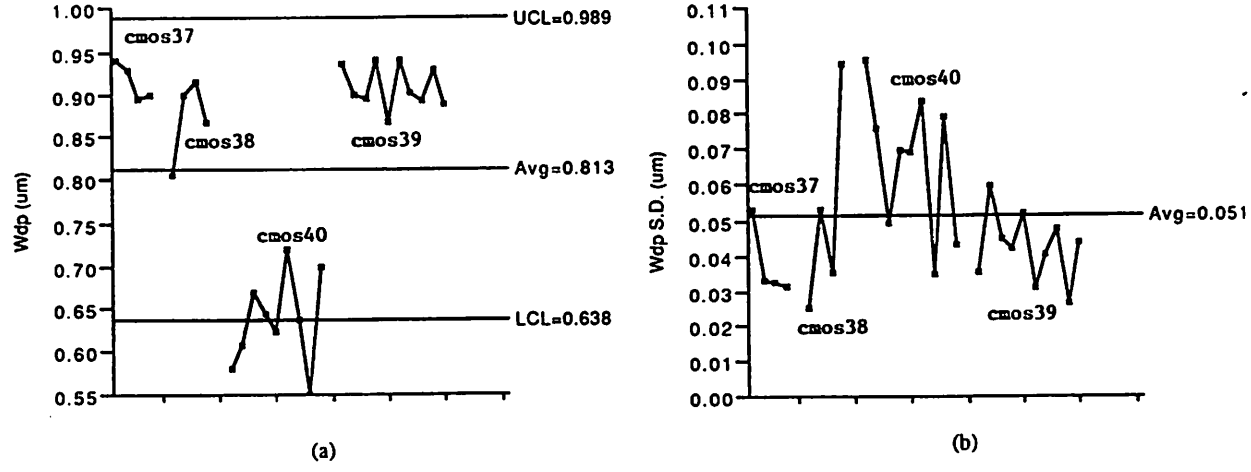


Fig. 21 (a) PMOS effective channel width distribution in the 2um N-well CMOS process. Each data point is the average of fifty-two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

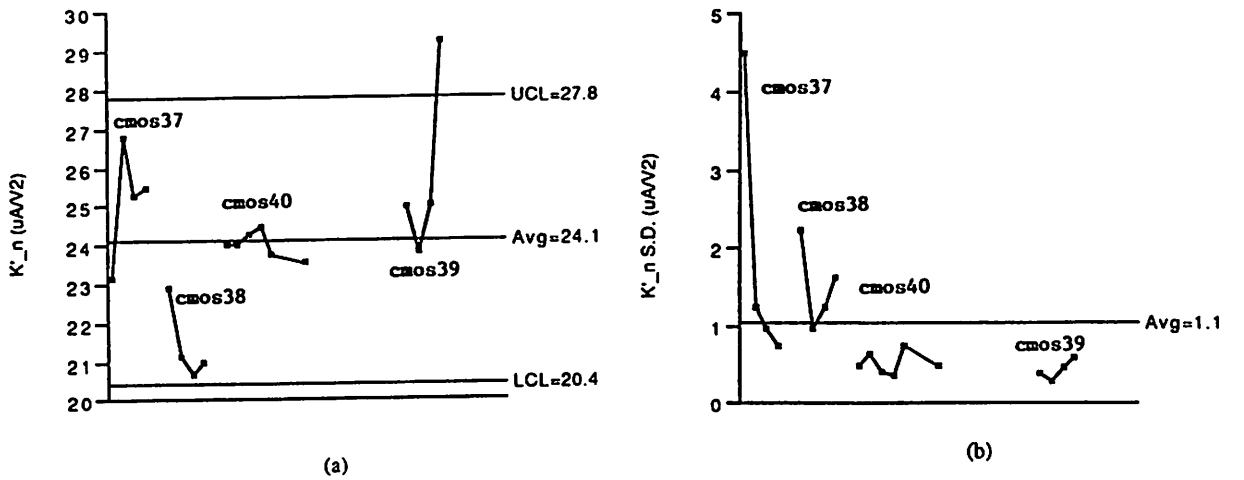


Fig. 22 (a) NMOS k' distribution in the 2um N-well CMOS process. Each data point is the average of ten dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit.
(b) Each data point is the standard deviation corresponding to the data point in (a).

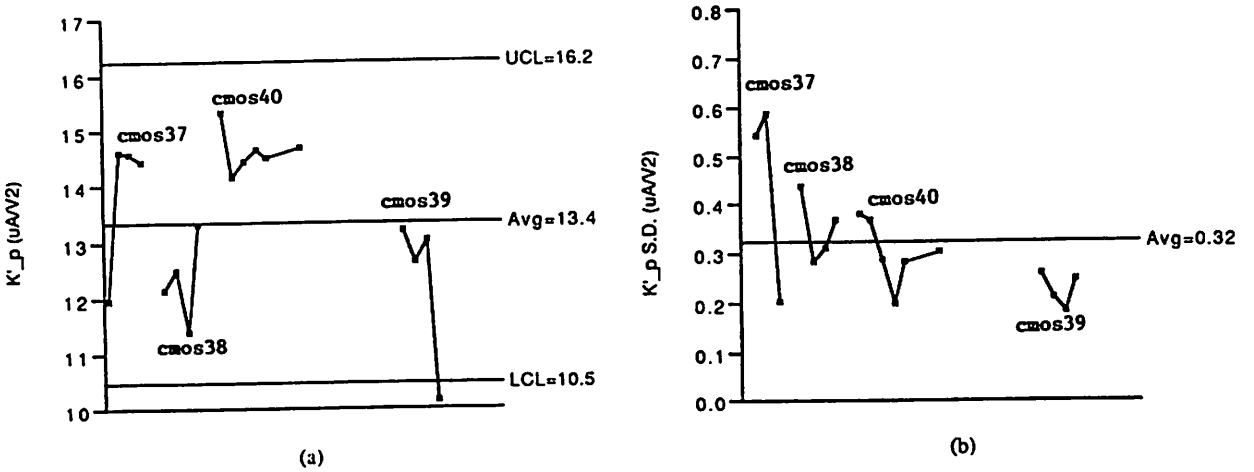


Fig. 23 (a) PMOS k' distribution in the 2um N-well CMOS process. Each data point is the average of ten dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit.
(b) Each data point is the standard deviation corresponding to the data point in (a).

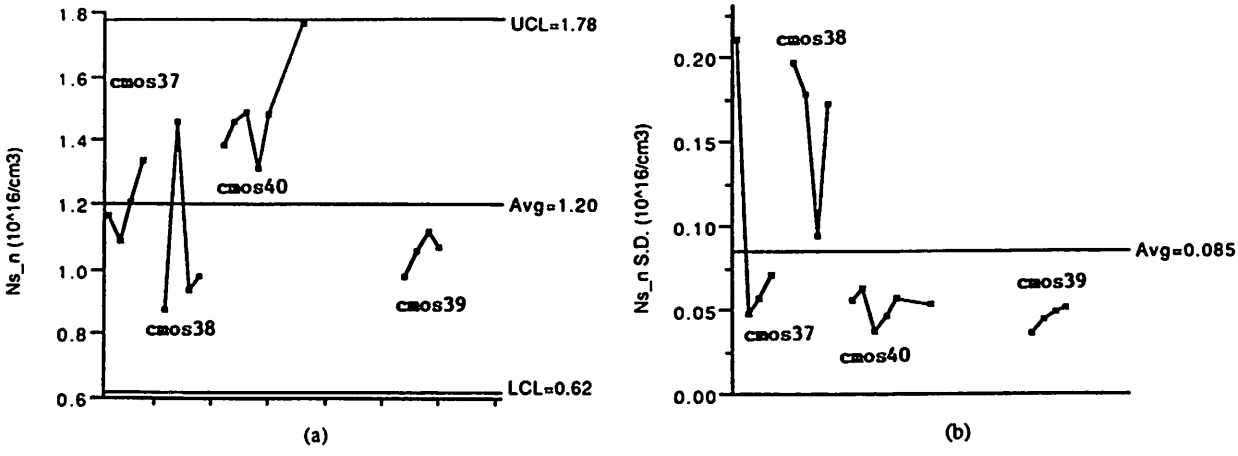


Fig. 24 (a) NMOS surface dopant concentration (Ns) distribution in the 2um N-well CMOS process. Ns was extracted from gamma1 measurement. Each data point is the average of ten dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

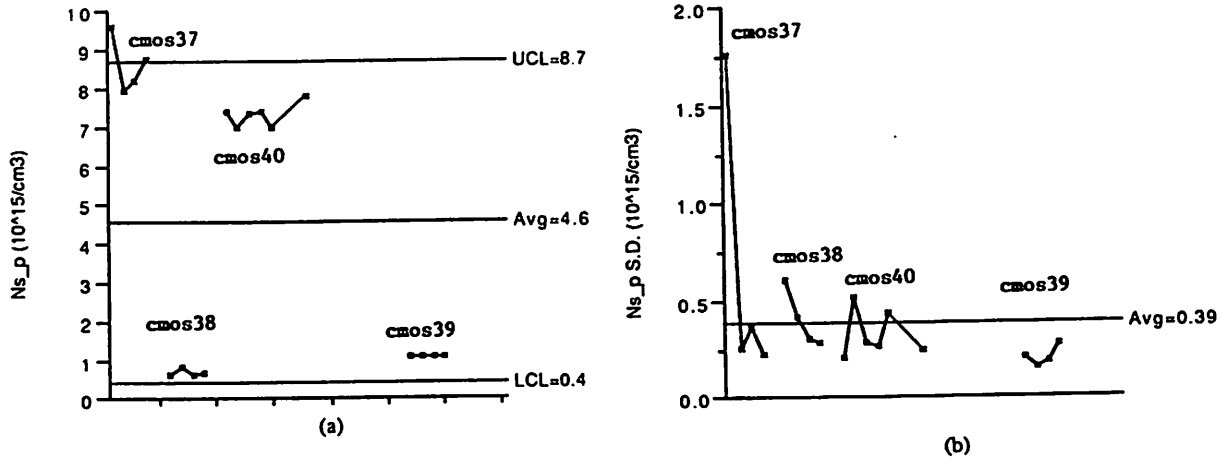


Fig. 25 (a) PMOS surface dopant concentration (Ns) distribution in the 2um N-well CMOS process. Ns was extracted from gamma1 measurement. Each data point is the average of ten dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

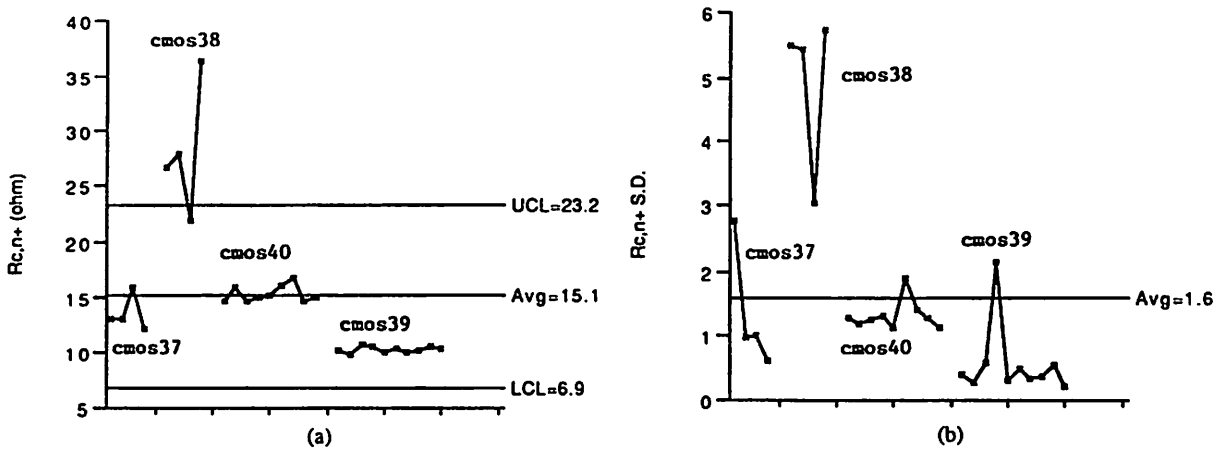


Fig. 26 (a) Al–N+ contact resistance distribution in the 2um N–well CMOS process. Each data point is the average of fifty–two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

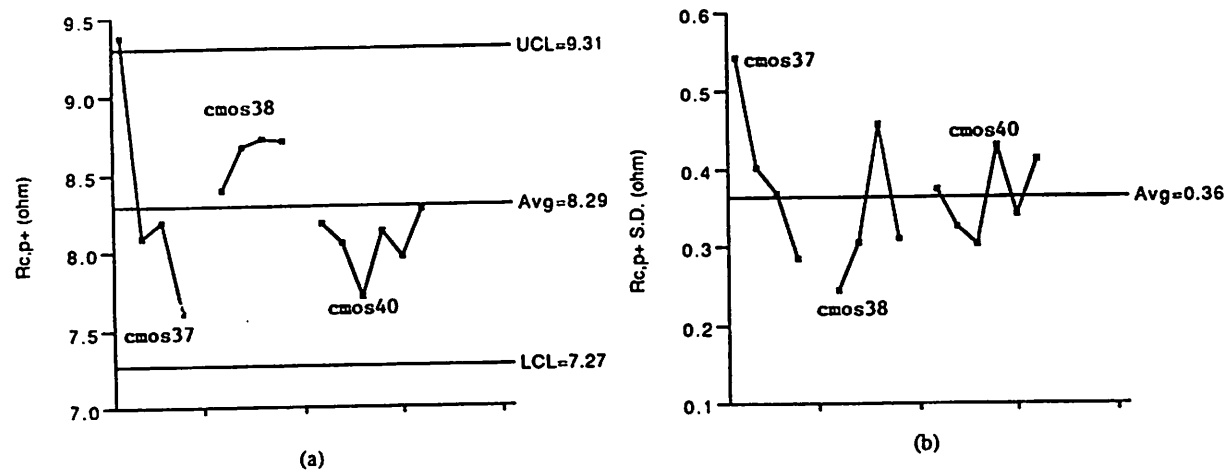


Fig. 27 (a) Al–P+ contact resistance distribution in the 2um N–well CMOS process. Each data point is the average of fifty–two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

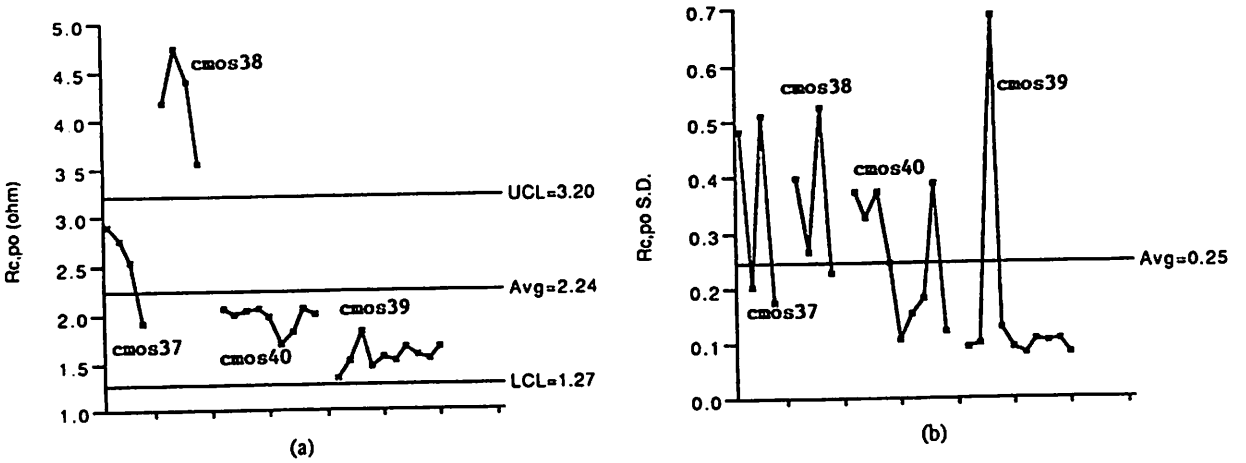


Fig. 28 (a) Al–Poly contact resistance distribution in the 2um N–well CMOS process. Each data point is the average of fifty–two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

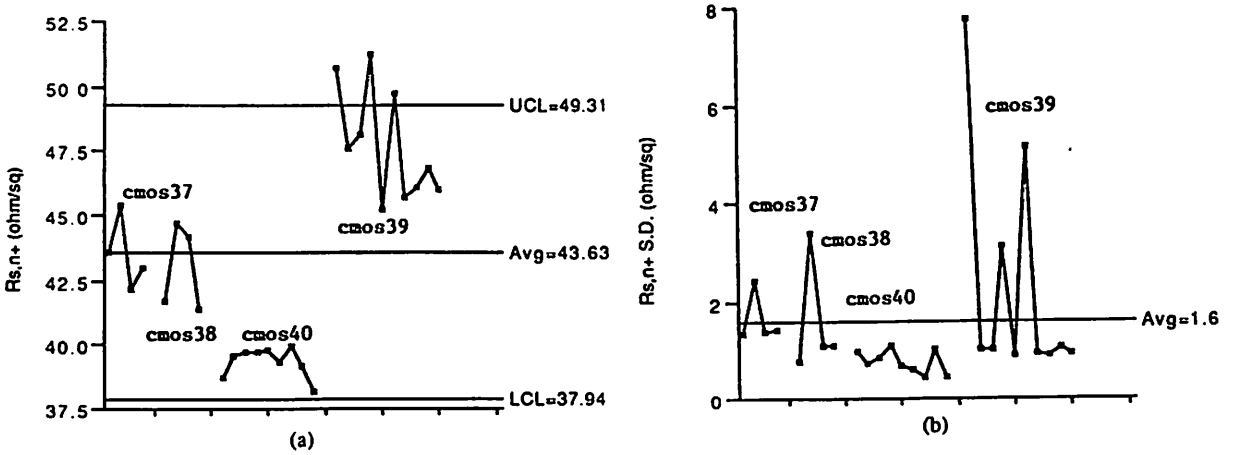


Fig. 29 (a) N+ diffusion sheet resistance distribution in the 2um N–well CMOS process. Each data point is the average of fifty–two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

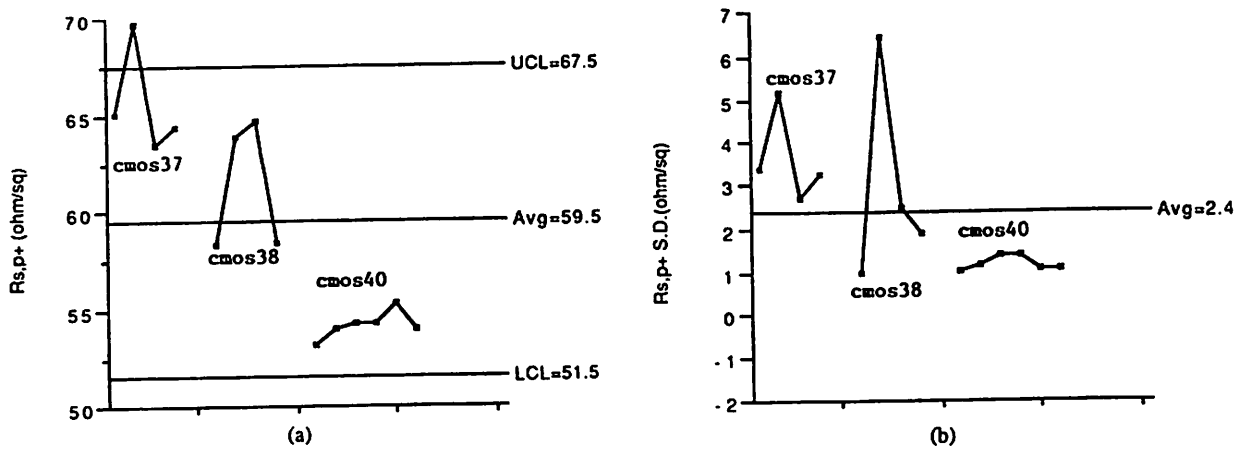


Fig. 30 (a) P+ diffusion sheet resistance distribution in the 2um N-well CMOS process. Each data point is the average of fifty-two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

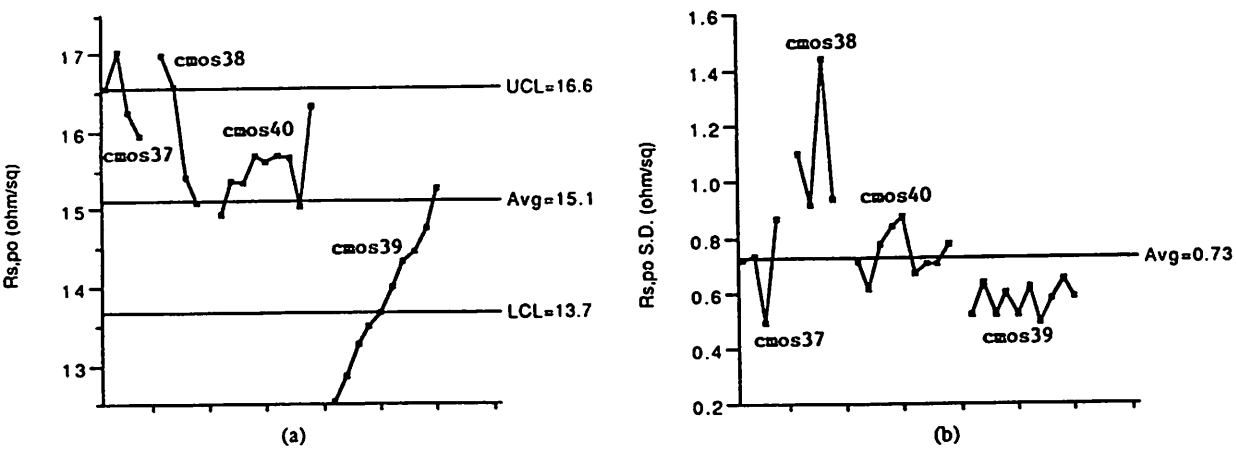


Fig. 31 (a) Doped poly sheet resistance distribution in the 2um N-well CMOS process. Each data point is the average of fifty-two dies measured across one wafer. UCL: Upper Control Limit. LCL: Lower Control Limit. (b) Each data point is the standard deviation corresponding to the data point in (a).

5 SPICE Parameter Extraction

Parameters for BSIM3, a SPICE model developed by the device group at UC Berkeley [7], was extracted by BSIMPro [8]. Figures 32 and 33 contain I-V characteristics of both NMOS and PMOS. Some extraction results are shown in Figures 34 through 36. On the next two pages are the output of BSIMPro. This data does not include capacitance parameters. These will be added when the capacitance measurement routines are available for the autoprober.

Output of BSIMPro:

```
*model = bsim3
*Cadence Compatibility Mode
*LogName=cmos40 UserName=sfang Date=07-13-1995
* Lmin= 2 Lmax= 25 Wmin= 5 Wmax= 50
*
* GENERAL PARAMETERS
*
.model NMOS NMOS
+Level=      10
+Tnom=27.0
+Npeak= 6.906394E+16  Tox=3.27000E-08 Xj=3.00000E-07
+dl= 1.96500E-07 dw= 6.98499977588654E-07
+SatMod= 2  SubthMod= 2
+BulkMod= 1
*
* THRESHOLD VOLTAGE PARAMETERS
*
+Vth0= .7476673  Phi= .7949965  K1= 1.433851  K2=-.2482773  K3= 46.17294
+Dvt0= .5664904  Dvt1= .5311641  Dvt2=-.7567183
+Nlx= 0  W0= 2.088732E-05
+K3b=-17.6259
*
* MOBILITY PARAMETERS
*
+Vsat= 107632.1  Ua= 2.175036E-09  Ub=-2.723978E-18  Uc=-7.168329E-03
+Rds0= 71.9  Rdsw= 769  U0= 670
+A0= .3190749
+Keta=-2.304753E-02  A1= 5.444023E-02  A2= .7
*
* SUBTHRESHOLD CURRENT PARAMETERS
*
+Voff=-.0551213  NFactor= .9818507  Cit=-1.738184E-04
+Cdsc=-1.186696E-04  Vglow=-.12  Vghigh= .12
+Cdscb=-2.228673E-05
+Eta0= 6.305706E-03  Etab=-1.986577E-02
+Dsub= .1730233
*
* ROUT PARAMETERS
*
+Pclm= .8851407  Pdibl1= .0171912  Pdibl2= 2.364713E-03
+Drout= .103091  Pscbe1= 2.085241E+08  Pscbe2= 2.270365E-05
+Pvag=-.8659828
+Eta= 0  Litl= 1.715517E-07
+Ldd= 0
```

```
* GENERAL PARAMETERS
*
.model PMOS PMOS
+Level=      10
+Tnom=27.0
+Npeak= 8.734341E+15  Tox=3.27000E-08 Xj=6.50000E-07
+dl= 3.44191E-07 dw= 8.19282412528992E-07
+SatMod= 2  SubthMod= 2
+BulkMod= 1
*
* THRESHOLD VOLTAGE PARAMETERS
*
+Vth0=-.6993924  Phi= .6880878  K1= .5099099  K2= 2.812088E-02  K3=-.1192135
+Dvt0= .9119751  Dvt1= .5007811  Dvt2=-7.716554E-02
+Nlx= 5.441865E-07  W0=-3.535396E-06
+K3b= 9.917567E-03
*
* MOBILITY PARAMETERS
*
+Vsat= 213574.9  Ua= 3.401969E-08  Ub=-8.815556E-17  Uc=-.292751
+Rds0= 180.8564  Rdsw= 342.9426  U0= 670
+A0= .655002
+Keta=-2.507999E-02  A1= .0637029  A2= 1.387779E-16
*
* SUBTHRESHOLD CURRENT PARAMETERS
*
+Voff=-5.633137E-02  NFactor= .8165306  Cit= 2.800296E-04
+Cdsc=-1.961542E-04  Vglow=-.12  Vghigh= .12
+Cdscb=-1.145162E-05
+Eta0= .2236274  Etab=-6.512475E-03
+Dsub= .5180283
*
* ROUT PAR*
+Pclm= 3.331738  Pdibl1= 1.023179  Pdibl2= 6.430786E-04
+Drout= .5563746  Pscbe1= 0  Pscbe2= 1E-28
+Pvag= 6.604128
+Eta= 0  Litl= 2.525173E-07
+Ldd= 0
```

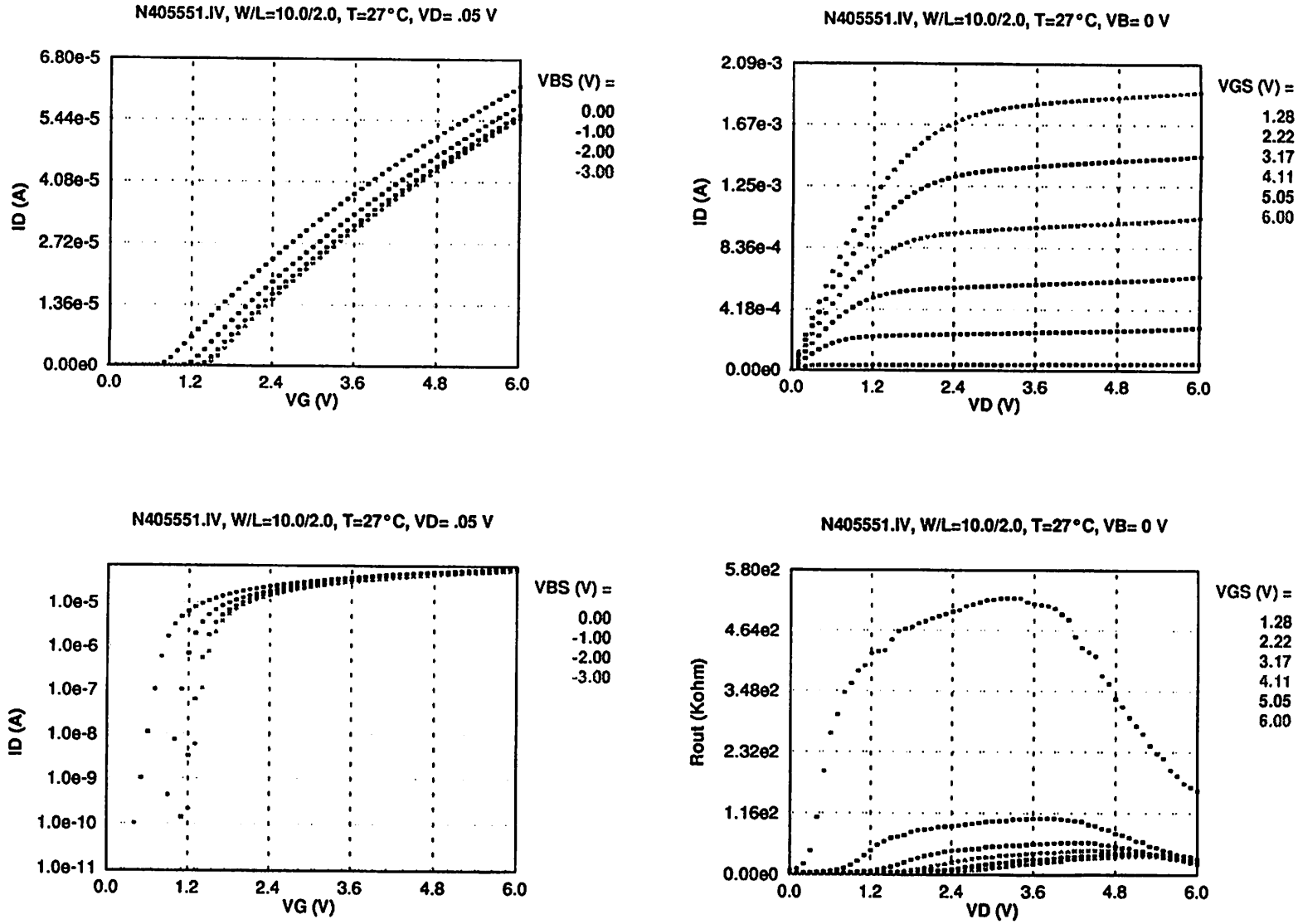


Fig. 32 I–V characteristics of an N–channel MOSFET (W/L=10/2), measured with BSIMPro.
(a) Id vs. Vg. (b) Id vs. Vd. (c) Subthreshold. (d) Output resistance.

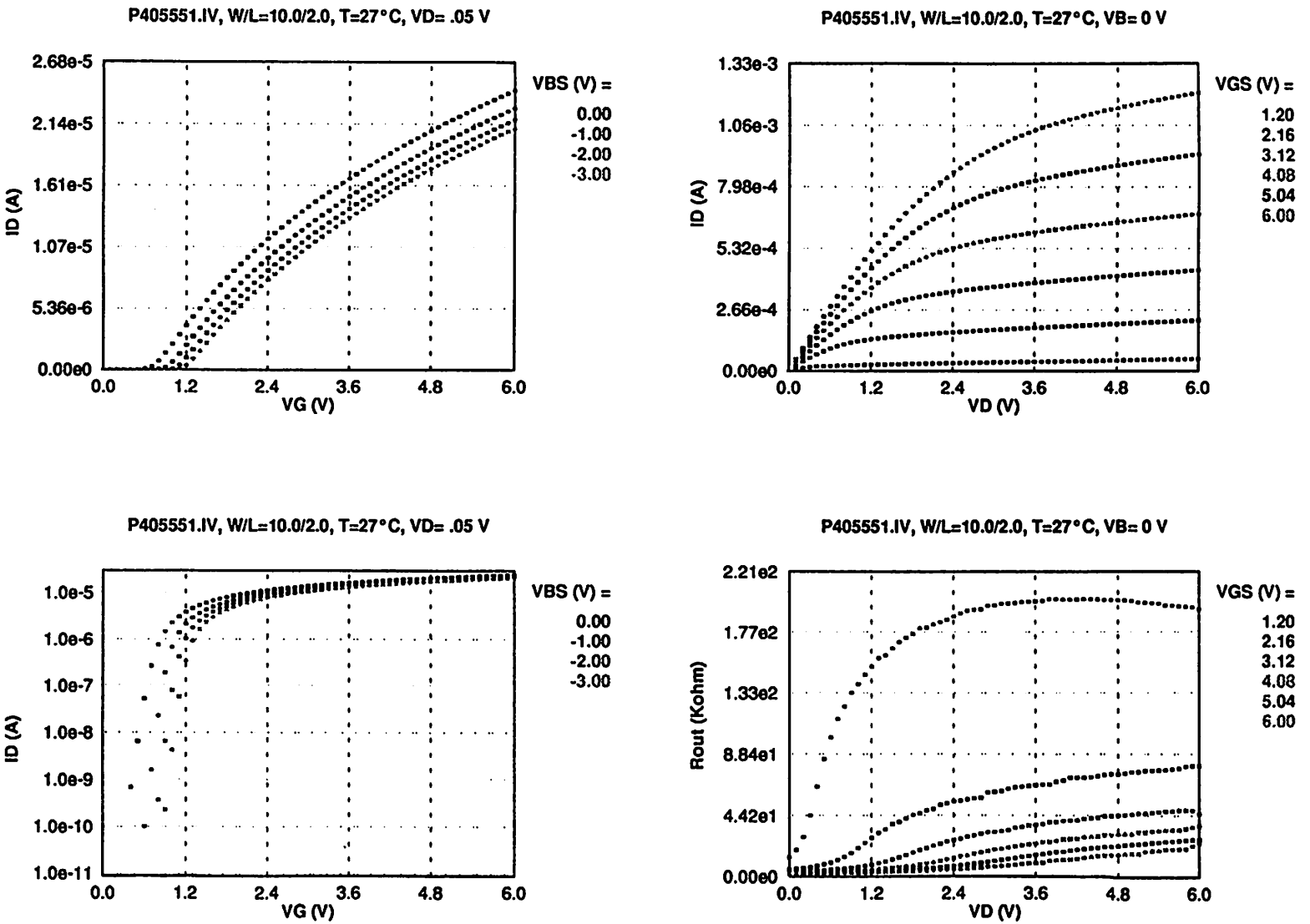


Fig. 33 I–V characteristics of a P–channel MOSFET (W/L=10/2), measured with BSIMPro.
(a) Id vs. Vg. (b) Id vs. Vd. (c) Subthreshold. (d) Output resistance.

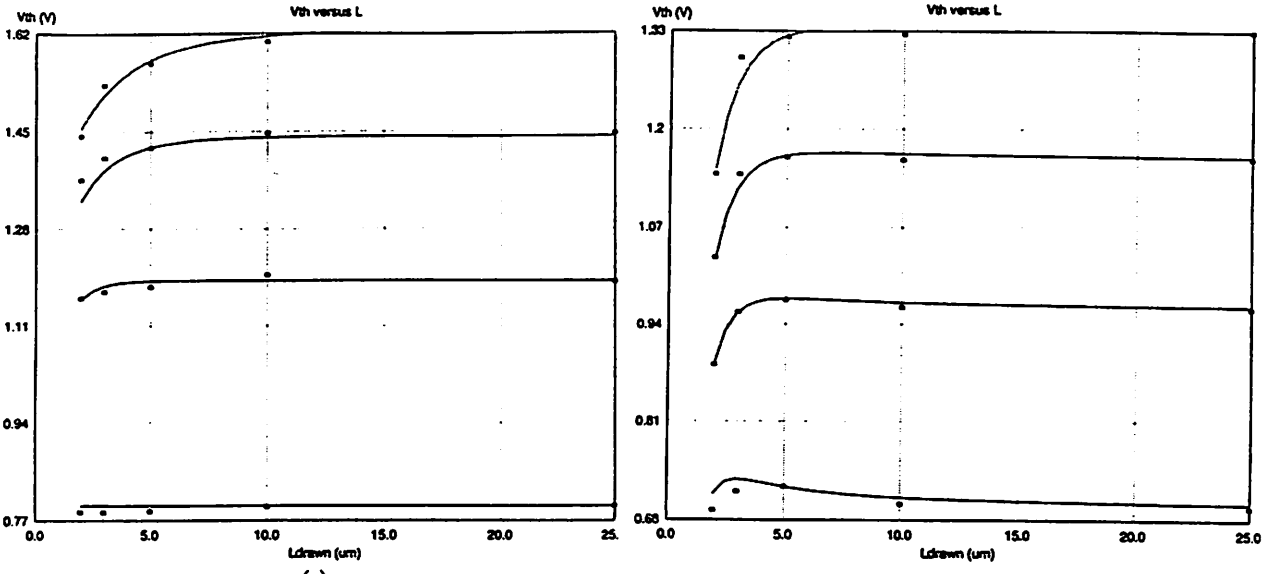


Fig. 34 Threshold voltage vs. channel length (drawn) with different substraste biases. (a) NMOS. (b) PMOS.

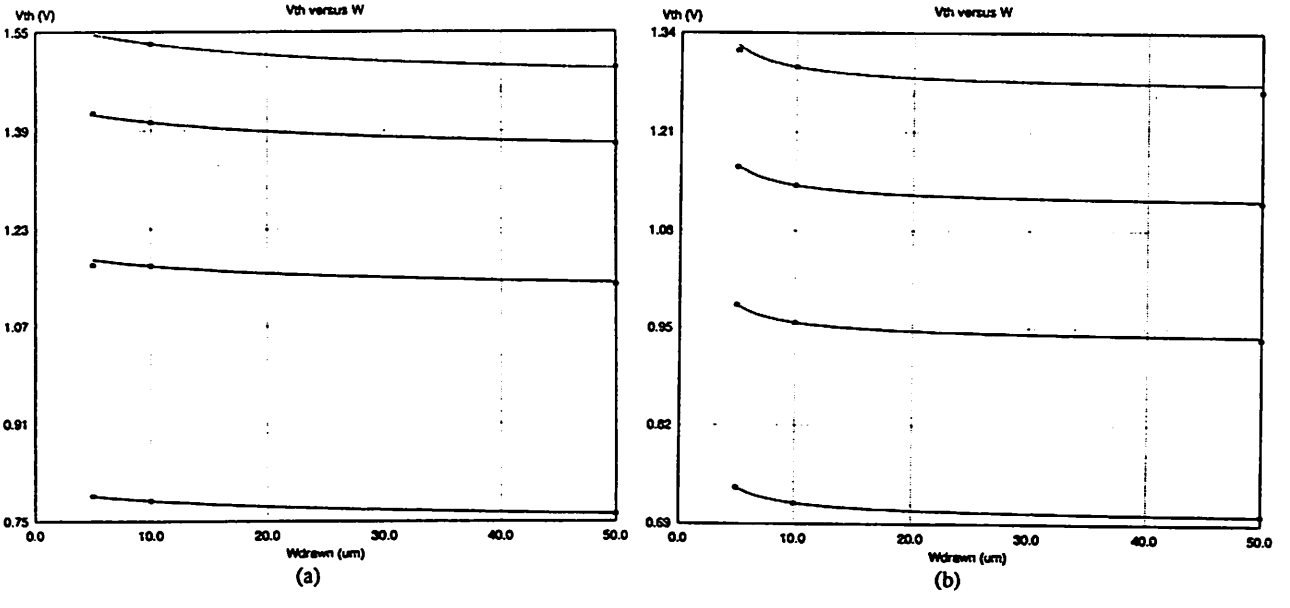
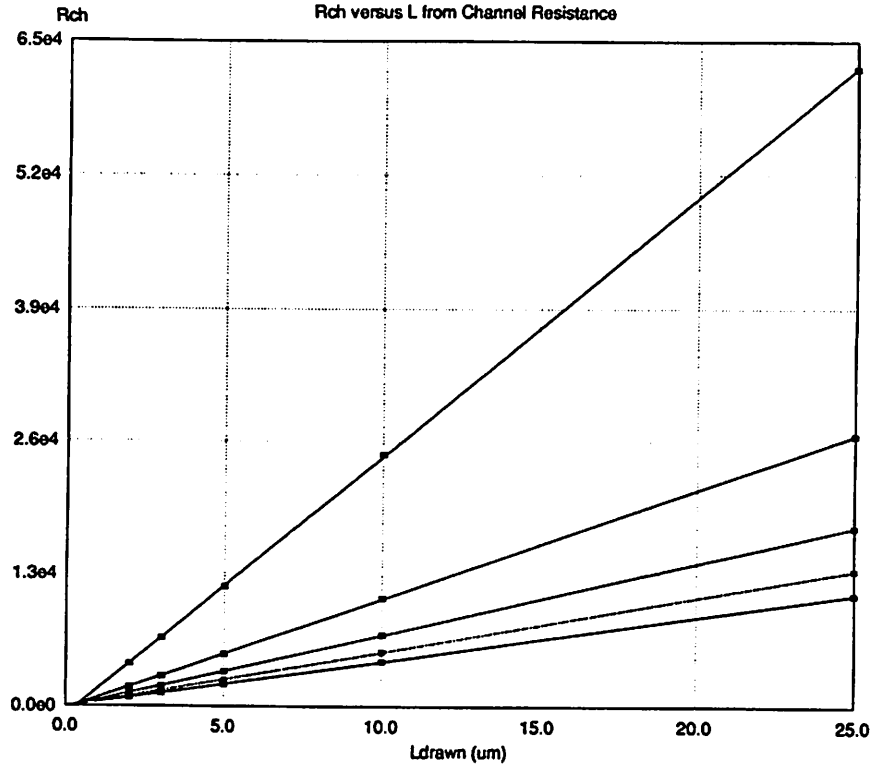
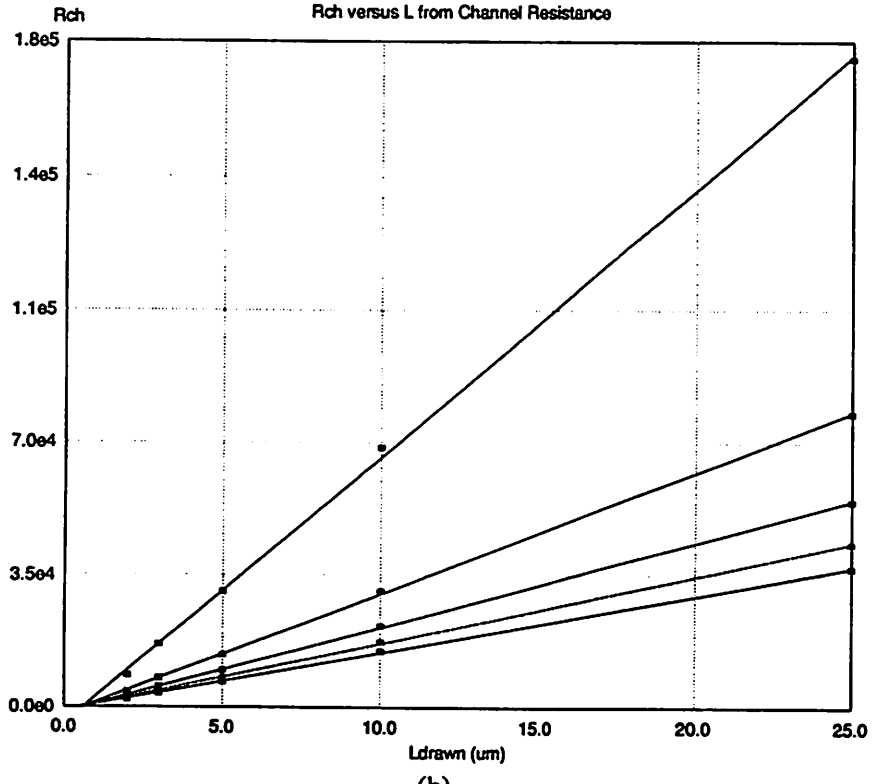


Fig. 35 Threshold voltage vs. channel width (drawn) with different substraste biases. (a) NMOS. (b) PMOS.



(a)



(b)

Fig. 36 Effective channel length extraction with BSIMPro. (a) NMOS. (b) PMOS.

6 Summary

The UC Berkeley CMOS baseline is available for participating groups to submit designs for processing, using the device parameter targets in Appendix A, the geometric design rules listed in Appendix B and BSIM3 model for SPICE simulation. Test structures for autoprobe testing are added for statistical evaluation. Successful runs have been completed by the baseline, cooperating with several research groups.

The CMOS baseline continues evolution with future projects including the extension of BSIM3 model support and development of 1.3 μm technology.

Acknowledgments

The baseline project is supported by the following research groups in the Microlab: Berkeley Sensors and Actuators Center, Profs. R. Howe, R. Muller, A. Pisano, R. White; Computer Integrated Manufacturing, Profs. D. Hodges, C.J. Spanos; Devices and Technology, Profs. N. Cheung, C. Hu, P.K. Ko; Integrated Circuits, Prof. P. Gray; Cryoelctronics, Prof. T. Van Duzer; Materials Science, Prof. M. Ferrari; and Microlab operating funds.

The author wishes to acknowledge the generous guidance of Prof. Costas J. Spanos and Microlab Manager Katalin Voros.

References

[1] Katalin Voros and Ping K. Ko, *MOS Processes in the Microfabrication Laboratory*, Memorandum No. UCB/ERL M87/12, Electronics Research Laboratory, University of California, Berkeley (10 March, 1987).

[2] David Rodriguez, *Electrical Testing of a CMOS Baseline Process*, Memorandum No. UCB/ERL M94/63, Electronics Research Laboratory, University of California, Berkeley (30 August 1994).

[3] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, New York: John Wiley & Sons, Inc., 1986.

[4] D. K. Schroder, *Semiconductor Material and Device Characterization*, New York: John Wiley & Sons, Inc., 1990.

[5] S. M. Sze, *Physics of Semiconductor Devices*, New York: John Wiley & Sons, Inc., 1981.

[6] Gary S. May, *MOSTCAP-An MOS Transistor Characterization and Analysis Program*, M.S. research project report, Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, 11 December 1987.

[7] Industrial Liaison Program, *Research Software, 1994-1995*, University of California at Berkeley, Electrical Engineering and Computer Sciences.

[8] *BSIMPro for Windows, User's Manual*, BTA Technology, Inc., February 1994.

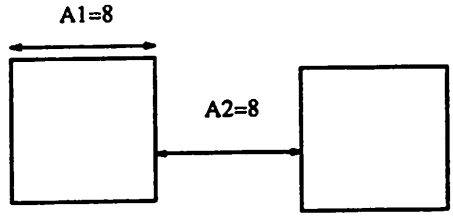
Appendix A 2 μm N-Well, Double Poly-Si and Double Metal CMOS Process and Device Parameters Targets

Parameters	Units	N-Channel	P-Channel
V_t	V	0.74 +/- 0.08	0.74 +/- 0.1
k' ($\mu C_{ox}/2$)	$\mu A/V^2$	24 +/- 4	13+/-3
ΔL (L_{drawn}-L_{eff})	μm	0.4-0.8	0.5-0.9
ΔW (W_{drawn}-W_{eff})	μm	1.2-1.8	1.2-1.9
γ_1 (low V_{BS})	$V^{1/2}$	0.4-0.65	0.4-0.55
γ_2 (High V_{BS})	$V^{1/2}$	0.15-0.2	0.35-0.55
S (Subthreshold Slope)	mV/decade	96 +/- 4	98 +/- 4
T_{ox}	Angstrom	300 +/- 30	300 +/- 30
X_j (S-D)	μm	0.3	0.6
X_w (well depth)	μm		3.2
R_{diff} (sheet resistance)	Ω/square	44 +/- 6	59 +/- 8
R_{poly} (sheet resistance)	Ω/square	15.1 +/- 1.5	15.1 +/- 1.5
R_{well} (sheet resistance)	KΩ/square		1.5 +/- 0.3
$R_{c\ m1\text{-}diff}$ (2μmx2μm)	Ω	15 +/- 8	8.3 +/- 1
$R_{c\ m1\text{-}poly}$ (2μmx2μm)	Ω	2.24 +/- 1	2.24 +/- 1
$\lvert V_{th\text{-}field}\rvert$	V	>10	>10
|S-D Breakdown|	V	>10	>10
S-D Leakage Current (V_{ds} = 5V, V_{gs} = 0V.)	pA/μm	0.8	2
Ring Oscillator (31 stages)	MHz	35	

Appendix B 2 um, N-well, Double Poly and Double Metal CMOS Design Rules

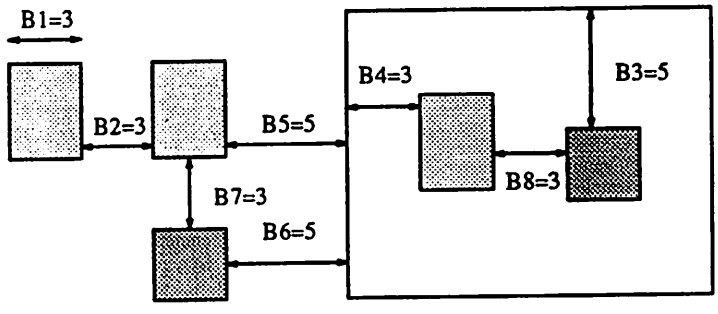
A. N-well Layer

A.1 Minimum size: 8μ
A.2 Minimum spacing: 8μ



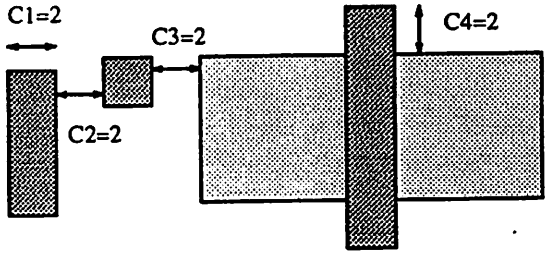
B. Active Area

B.1 Minimum size: 3μ
B.2 Minimum spacing: 3μ
B.3 N-well overlap of P+: 5μ
B.4 N-well overlap of N+: 3μ
B.5 N-well space to N+: 5μ
B.6 N-well space to P+: 5μ
B.7 N+ to P+ in substrate: 3μ
B.8 P+ to N+ in n-well: 3μ



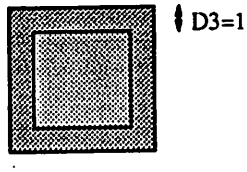
C. Poly 1 (Gate Poly)

C.1 Minimum size: 2μ
C.2 Minimum spacing: 2μ
C.3 Spacing to active: 2μ
C.4 Gate extension: 2μ



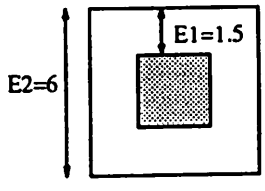
D. Poly 2 (Capacitor Poly)

D.1 Minimum size: 2μ
D.2 Minimum spacing: 2μ
D.3 Poly 1 overlap of poly 2: 1μ



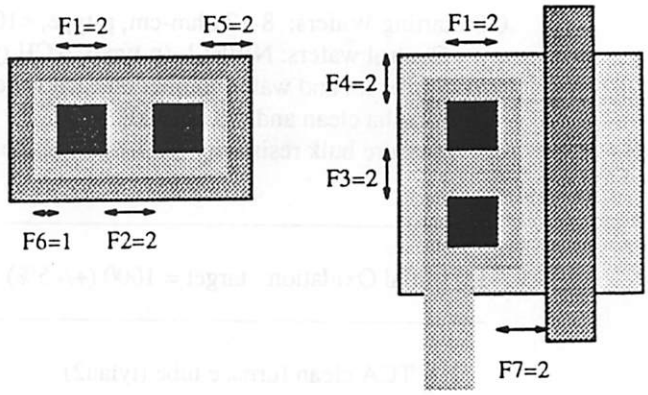
E. p-plus/n-plus Implant

E.1 Minimum overlap of active: 1.5μ
E.2 Minimum size: 6μ



F. Contact

F.1 Minimum size:	2μ
F.2 Minimum spacing (on poly):	2μ
F.3 Minimum spacing (on active):	2μ
F.4 Minimum overlap of active:	2μ
F.5 Minimum overlap of poly:	2μ
F.6 Minimum overlap of metal 1*:	1μ
F.7 Minimum spacing to gate:**	2μ

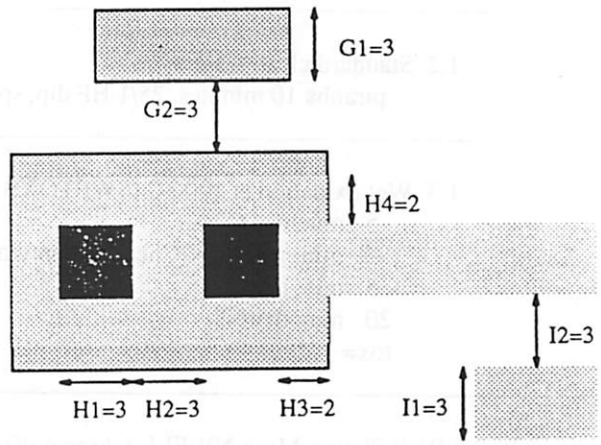


G. Metal 1

G.1 Minimum size:	3 μ
G.2 Minimum spacing:	3 μ

H. Via

H.1 Minimum size:	3 μ
H.2 Minimum spacing:	3 μ
H.3 Minimum overlap of metal1:	2 μ
H.4 Minimum overlap of metal2:	2 μ



I. Metal 2

I.1 Minimum size:	3 μ
I.2 Minimum spacing:	3 μ

*: 2 μ for BSAC group.

**: 3 μ for BSAC group.

Appendix C Microlab CMOS Baseline Process Log

Microlab CMOS Process
2 um, N-well, double poly-Si, double metal

0.0 Starting Wafers: 8-12 ohm-cm, p-type, <100>
Control wafers: NWELL (p-type), NCH (p-type)
Scribe lot and wafer number on each wafer, including controls.
Piranha clean and dip in sink8.
Measure bulk resistivity (ohms-cm) of the controls on sonogage.
R =

1.0 Initial Oxidation: target = 1000 (+/- 5%) A

1.1 TCA clean furnace tube (tylan2).

1.2 Standard clean wafers:
piranha 10 minutes, 25/1 HF dip, spin-dry.

1.3 Wet oxidation at 1000 C (SWETOXB):
5 min. dry O2
~9 min. wet O2 (Check the previous run result)
5 min. dry O2
20 min. dry N2
tox=

2.0 Well Photo: Mask NWELL (chrome-df)
(Control wafers are not included in any photoresist step)
Standard I-line process:
HMDS, spin (and soft bake), expose, post exposure bake,
develop, inspect, descum and hard bake.

3.0 Well Implant: phosphorus, 5E12/cm2, 150 KeV. Include NWELL.

4.0 Well Drive-In: target xj = 3.43 um, tox = 3000 A

4.1 TCA clean furnace tube (tylan2).

4.2 Etch pattern into oxide in 5/1 BHF. Include NWELL.

4.3 Remove PR in O2 plasma and clean wafers in sink8.

4.4 Standard clean wafers in sink6, include NWELL and NCH.

4.5 Well drive at 1150 C (WELLDR):
1 hr temperature ramp from 750 C to 1150 C
4 hrs dry O2
1 hr dry N2
a) Measure oxide thickness.
tox (well)= tox (outside) =
b) Strip oxide from NWELL and NCH, measure Rs
Rs (NWELL) =

4.6 TCA clean the furnace tube after well drive-in is done.

5.0 Pad Oxidation/Nitride Deposition:
target = 300 (+60) A SiO2 + 1000 (+100) A Si3N4

5.1 TCA clean furnace tube (tylan5). Reserve tylan9.

5.2 Remove all oxide in 5/1 BHF until wafers dewet.

5.3 Standard clean wafers. Include NWELL and NCH.

5.4 Dry oxidation at 950 C (SGATEOX):
~1 hr. dry O2
20 minutes dry N2 anneal.
Measure tox on NCH. Tox=. NCH proceed to 12.2.

5.5 Deposit 1000 (+100) A of Si3N4 immediately (SNITC):
Include NWELL only.
approx.time = 22 min., temp.= 800 C.
Measure nitride thickness on NWELL, using tox value
obtained in 5.4. NWELL proceed to Step 10.2.
tnit =

6.0 Active Area Photo: Mask ACTV (emulsion-cf)
Standard G-line process (First PR).

7.0 Nitride Etch in lam1 (Process #3)
Plasma etch in lam1.
Recipe: Power: Ave. etch time: Overetch:
Measure Tox on each work wafer. (2 pnt measurement).
Do not remove PR. Inspect.
Measure PR thickness covering active area with as200.
PR must be >8 kA. Hard bake again for >2hrs at 120 C.

8.0 Field (P-) Implant Photo: Mask PFIELD (emulsion-cf)
Reversed NWELL mask)
Standard G-line process. (Second PR)
Well area is covered with PR. Outside well, N-channel
MOSFET active areas are covered with Si3N4 and PR.

9.0 Field (P-) Ion Implant: B11, 70 KeV, 1.5E13/cm2.

10.0 Locos Oxidation: target = 6500 A

10.1 TCA clean furnace tube (tylan2).

10.2 Remove PR in O2 plasma and piranha clean wafers.
Standard clean wafers; dip until field area dewets.
Include NWELL.

10.3 Wet oxidation at 950 C (SWETOXB):
5 min. dry O2
4 hrs. 40 min. wet O2
5 min. dry O2
20 min. N2 anneal
Measured tox on 3 work wafers.Tox=

11.0 Nitride Removal (Include NWELL.)

11.1 Dip in 5/1 HF for 30 sec to remove thin oxide on top of Si3N4.

11.2 Etch nitride off in phosphoric acid at 145 C.

12.0 Sacrificial Oxide: target = 200 (+/- 20) A

12.1 TCA clean furnace tube (tylan5).

12.2 Standard clean wafers. Include NWELL and NCH.
Dip in 10:1 BHF until NWELL and NCH dewet.

12.3 Dry oxidation at 950 C (SGATEOX):
30 minutes dry O2
20 minutes N2 anneal
Measure Tox on 3 wfrs. Tox=

13.0 Threshold Implant (blanket): B11, 30 KeV, 1.7E12/cm2.

14.0 Gate Oxidation/Poly-Si Deposition:
target = 300 (+/- 30) A SiO2 + 4500 (+/- 300) A poly-Si

14.1 TCA clean furnace tube (tylan5).
Reserve poly-Si deposition tube (tylan11).

14.2 Standard clean wafers, including NWELL, NCH and, five
Tox and one Tpoly1 monitoring wafers.

14.3 Dip off sacrificial oxide in 10/1 HF
until PWELL and PCH dewet (approx. 1 min).

14.4 Dry oxidation at 950 C (SGATEOX):
~1 hrs dry O2 (Check previous run result)
20 minutes N2 anneal.
Measure 5 pnts on 3 Tox monitoring wfrs. Tox=

14.5 Immediately after oxidation deposit 4500 A of phos.doped
poly-Si (SDOPOLYH).
approx.time = 2 hr. 50 min., temp.= 610 C
Include Tpoly1, PWELL and PCH.
Tpoly1= Measure 5 pnts on Tpoly1, PWELL and PCH.
Tpoly1, NWELL and NCH proceed to Step 19.2.

15.0 Gate Definition: Mask POLY (emulsion-cf)
Standard I-Line process.

16.0 Plasma etch poly-Si

16.1 Etch poly in Lam4.

16.2 Measure Tox in S/D area of each work wafer.

17.0 Capacitor Formation:
target = 800 A SiO2 on 1st poly + 4500 A 2nd poly.

17.1 TCA clean furnace tube (tylan2). Reserve tylan11.

17.2 Standard clean wafers, including NWELL and NCH, Tpoly1
and one of gate oxidation monitoring wafers as a
2nd poly monitoring wafer, Tpoly2.
Tpoly2 proceeds to Step 19.4.
From here on: only 10 sec dip in 25/1 H2O/HF after piranha.

17.3 Dry oxidation at 950 C (SDRYOXB):
56 min dry O2 (Check the previous lot result).
20 min N2 anneal.
Measure oxide thickness on poly with nanoduv:
tox(NWELL) = tox(NCH) =
NCH proceeds to 23 and NWELL proceeds to Step 26.

17.4 Second poly-Si deposition: immediately after oxidation
deposit 4500 A of phos.doped poly-Si (SDOPOLYH):
approx.time = 2 hr. 50 min, temp.= 610 C. Tpoly2=

18.0 Capacitor Photo: Mask CAP-CE (emulsion-cf),the same mask for pwell.
Standard I-Line process.

19.0 Plasma etch poly-Si:

19.1 Etch 2nd poly in Lam4. Inspect.

19.2 Measure Tox in S/D area on each work wafer.
Remove PR in O2 plasma.

19.3 Measure line width of 2 um gates on each work wafer.
Piranha clean wfrs in sink8.
Dehydrate wfrs in oven for > 30 min. at 120 C.

20.0 N+ S/D Photo: Mask N-S/D (chrome-df)
Stnd I-line process. Inspect. Hard bake.

21.0 N+ S/D Implant: Arsenic, 160 keV, 5E15/cm2, incl. NWLL and NCH.

22.0 N+ S/D Anneal

22.1 TCA clean furnace tube (tylan7).

22.2 Remove PR in O2 plasma and piranha clean wafers
in sink8 (no dip here).

22.3 Standard clean wafers in sink6, include NCH.

22.4 Anneal in N2 at 950 C for 1 hr (N2ANNEAL).

23.0 P+ S/D Photo: Mask P-S/D (emulsion-cf)
Stnd I-line process. Inspect!
All areas are covered with PR except P-channel areas.

24.0 P+ S/D Implant: B11 at 30 keV, 5E15/cm2, include NWELL.

25.0 PSG Deposition and Densification: target = 7000 A

25.1 Remove PR in O2 plasma and piranha clean wafers
in sink8 (no dip).

25.2 Stnd clean wfrs in sink6 (10 sec dip).
Include NWELL, NCH and one PSG monitoring wafer.

25.3 Deposit 7000 A PSG, PH3 flow at 10.3 sccm (SDOLTOD).
approx.time = 35 min. (check current dep. rate)
temp. = 450 C

25.4 Densify glass in tylan2 at 950 C, immediately after
PSG deposition (PSGDENS). Include PSG control.
5 min dry O2, 20 min wet O2, 5 min dry O2.
Measure tPSG=
Etch oxide on NWELL and NCH, and measure poly
sheet resistivity on NWELL and NCH with prometrix.

25.5 Do wet oxidation dummy run afterwards to clean tube:
1 hr wet oxidation at 950 C (SWETOXB).

26.0 Contact Photo: Mask CONT (chrome-df)
Stnd I-Line process.

27.0 Contact Etch:
Plasma etch in Lam2.

28.0 Back side etch:

28.1 Remove PR in O2 plasma, piranha clean wfrs in sink8 (no dip).
Dehydrate wafers in oven at 120 C for >30 min.

28.2 Etch backside:
(NWELL and PWELL can be included in b), c) and d).
a) Spin PR on front side, hard bake.
b) Dip off oxide (PSG) in 5:1 BHF.
c) Etch poly-Si (poly2 thickness) in lam4.
d) Etch oxide off in 5:1 BHF (cap. ox. thickness).
e) Etch poly-Si (poly1 thickness) in lam4.
f) Final dip in BHF until back dewets.
g) Remove PR in PRS2000, piranha clean wfrs in sink8 (no dip).

29.0 Metallization: target = 6000 A
Stnd clean wfrs and do a 30 sec. 25/1 H2O/HF dip just
before metallization.
Sputter Al/2% Si on all wafers in CPA.

30.0 Metal Photo: Mask METAL1-CM (emulsion-cf)
Stnd I-line process. Hard bake for >2 hrs.

31.0 Plasma etch Al in Lam3.
Remove PR in PRS2000 or technics-c. tAl=
Probe test devices.

32.0 Sintering: 400 C for 20min in forming gas (tylan13).
No ramping, use SINT400 program.

33.0 Testing:
2um N- and P-channel devices, capacitors and inverter
Measure the sheet resistivities of NWELL and
NCH on prometrix.

34.0 Planerization and Dielectric Film Deposition:

34.1 PECVD thin oxide (500 A) in technics-B:
N2O: 54.0, Silane: 14.0, Pwr: 15 W, Pressure: 360-420 mT.
~5 min. Measure Tox on dummy wafers.

34.2 SOG coating on the Headway spinner at 3000 rpm, 20 sec.

34.3 SOG cure:
a) Oven in Y2, 120 C, 30 min.
b) Oven in R1, 200 C, 30 min.
c) Tylan14 (SVANNEAL): 400oC, 30 min.
d) Measure Tox and refractive index on dummy wafers.

34.4 PECVD thick oxide (to total SOG & PECVD 8000 A) in technics-B:
N2O: 54.0, Silane: 14.0, Pwr: 15W, Pressure: 360-420mT
Use the dep. rate obtained from 34.1 and calculate
the dep. time. Rotate the wafers 180 degrees
at the half way point of the deposition.
Measure Tox and refractive index on dummy wafers.

35.0 VIA Photo:
I-line 1.6 um thickness process. Descum in technics-c.
Hard bake.

36.0 Etch VIA in lam2.
Need overetch. Test metal1 patterns on the wafers
with 4-pnt probe to see if the end point is reached.

37.0 Metal2 Metallization. target = 8000-9000 A
Remove PR in PRS2000 or technics-c. Rinse the wafers in
sink7 and spin dry.
Sputter Al/2% Si on all wafers in CPA.

38.0 Metal Photo: Mask METAL1-CM (emulsion-cf)
G-line double thickness process. Descum in technics-c.
Hard bake for >2 hrs.

39.0 Plasma etch Al in Lam3.
Remove PR in PRS2000 or technics-c.

40.0 Sintering: 400 C for 20min in forming gas (tylan13).
No ramping, use SINT400 program.

41.0 Testing:
Measure Metal1 and Metal2 contact chain.

End of Process
