Proposal to:
The Air Force Office of Scientific Research
6 February 1997- 5 February 2000

JOINT SERVICES ELECTRONICS PROGRAM
Bolling Air Force Base
Washington, DC

Proposal No. UCB/ERL-96/137

Renewal of the Joint Services Electronics Program's
Support of the Basic Research Program of the
Electronics Research Laboratory

Principal Investigator: Jeffrey Bokor
Co-Principal Investigator: Diogenes Angelakos

Amount Requested: $2,410,206
Duration: 6 February 1997- 5 February 2000

Submitted by:

The Regents of the University of California
College of Engineering
Electronics Research Laboratory

TABLE OF CONTENTS

DIRECTOR'S OVERVIEW

This proposal presents a program for continued research at the Electronics Research Laboratory (ERL) under the Joint Services Electronics Program (JSEP) for the period February 6, 1997 through February 5, 2000. This period takes us into the next millennium. At such a crossroads, we are compelled to seek perspective from the past, and are inspired to look as far as we can into the future.

The JSEP program has a long and extremely productive history at Berkeley. Now, more than ever, it is essential to the vitality of our electronics research portfolio because it is one of the very few remaining sources of support for research in the basic science that underpins electronics technology. The widespread availability and cost effectiveness of the modern electronics that have revolutionized both military and civilian hardware can be directly traced to fundamental advances in basic science.

At the same time, we see that the mission of the US Department of Defense is undergoing dramatic change. Warfighting is becoming increasingly dependent on technology, with particular reliance on electronics. As we look ahead in science we continue to see many opportunities for fundamental breakthroughs that will sustain exponential increases in the capabilities of electronics for decades to come, thereby meeting the challenge of the DoD mission for the next millennium.

With this in mind, we have formulated a proposal that is as forward-looking as possible. Significant changes have been made in many aspects of our program. Before describing these, we first review some of our most outstanding accomplishments since our last major proposal.

In the area of Semiconductor Physics and Devices, we have maintained a balanced program of research in both electronics and optoelectronics, with efforts in basic physics, materials, and devices.

In basic physics, one of the frontiers we have concentrated on is the area of ultrafast carrier dynamics in semiconductors, which is so important in determining the ultimate limits of high speed electronic and optoelectronic devices. We have developed new instrumentation for studying these problems, including methods suitable for the study of carrier dynamics in silicon, which is difficult to characterize using conventional femtosecond laser techniques. A new method for directly measuring carrier dynamics in quantum-well semiconductor diode lasers was also developed. In a classic example of scientific serendipity leading to a practical application that was totally unanticipated, it was found that hot carriers created in silicon by femtosecond laser pulses can release surface microminiature structures which had failed due to stiction. This offers a potential solution to an important problem in micro-electromechanical systems (MEMS) technology.

In the materials area, a unique hollow anode nitrogen source was developed for ion-assisted MBE growth of GaN. This source provides high fluxes of low kinetic energy ions, which minimizes damage, leading to excellent structural and luminescent properties. It also has the additional advantage of very low contamination. A breakthrough was also made in the synthesis of silicon-on-insulator material using the separation by plasma implantation of oxygen (SPIMOX) technique. The process involves the use of plasma immersion implantation (PII) a technique pioneered at Berkeley. A combination of careful study of the plasma physics, the implantation physics, and the annealing process using a full suite of materials analysis techniques was crucial to this success.

In the devices area, research in nanoscale silicon devices has continued to produce numerous outstanding accomplishments. MOSFET's with gate oxide thickness of only 1.5 nm were fabri-

cated and shown to be promising for future VLSI. MOSFET's with channel lengths down to 800 nm were also successfully fabricated and studied. Saturation velocity and overshoot velocity in inversion layers was quantitatively measured using special test structures invented at Berkeley. Most notably, a highly promising new device structure called dynamic-threshold MOSFET (DTMOS) was invented and demonstrated to provide high speed and low leakage at power supply voltage as low as 0.5 V. This device will have a major impact in the low-power mobile electronics area.

In our companion theme of artificial neural networks, a new cellular neural network (CNN) algorithm was developed for facsimile image processing. This algorithm produces superior quality output on originals that contain a mix of text, glossy images, and coarsely halftoned images by distinguishing the different image types, processing them separately, and then assembling the final output. Neural network ideas were also used to a develop speech recognition system that is robust to background noise (telephone speech with car noise added), and to make significant advances in the ability to process images of textured scenes and extract information from them.

Strong interactions with industry and technology transfer have long been a hallmark of UC Berkeley electronics research. Many projects are carried out with the direct collaboration of industry, greatly facilitating technology transfer. The current JSEP program contains many examples.

Professor Kam Lau's research on high speed semiconductor lasers is carried out in close collaboration with Dr. C. E. Zah of Bellcore, who supplies the lasers used in the research. A model of thin oxide scaling for MOSFETS developed by Professor Chenming Hu's group was adopted by the Semiconductor Industry Association Roadmap Coordinating Group as a basis for projecting future semiconductor technology. Professor Hu's group and Professor Jeff Bokor's group has collaborated on the calibration of a commercial device simulator from TMA. Dr. Henry Gaw of Intel Corp. collaborated with Professors Hu and Bokor on the direct measurement of saturation velocity and overshoot velocity in silicon inversion layers. Professor Nathan Cheung's research with Professor Hu on SIMOX formation has collaborations with Intel, Advanced Micro Devices, Eaton Corp., and LAM Research Corp. Professor Eicke Weber's research with Professor Cheung is pursued in collaboration with America Xtal Technology and Cree Research. Several companies are considering the incorporation of CNN technology developed by Professor Leon Chua into products. These include VLSI Technology, Visioneer, Inc., Phase Metrics, Inc., and Teleview Research Inc. Finally, Dr. Timothy Ross, with the Pattern Theory Group and Air Force Wright Patterson Laboratories evaluated the performance of the decision graph algorithm developed by Professor Alberto Sangiovanni-Vincentelli's group, and found that it significantly outperformed all tested alternatives in their benchmark.

In the spirit of looking far into the future discussed earlier, we have made significant technical and personnel changes in this proposal relative to the previous one.

First, a new faculty member in optoelectronics, Professor Connie Chang-Hasnain, has recently joined the Berkeley faculty. Professor Chang-Hasnain was previously on the faculty at Stanford University, and part of the JSEP program there. Her research is in the area of vertical cavity semiconductor lasers with emphasis on applications to wavelength division multiplexing systems for all-optical communications networks. Her work will complement Professor Kam Lau's research on semiconductor lasers, and she brings great energy and enthusiasm to our program overall.

We are proposing a dramatic change in the part of our program dealing with information science and algorithms. The artificial neural network theme is being replaced with a new one in nanoelectronic systems. The neural network program has evolved into an emphasis on the applications over the fundamental algorithmic work. It is therefore appropriate that it transition to other funding

sources than JSEP. Professors Avideh Zakhor, Jitendra Malik, and Nelson Morgan are making this transition. Simultaneously, we perceive a great opportunity in nanoelectronics and quantum computing. While we have some device research in this area being conducted by Professors Hu and Bokor, and there is a great deal of it elsewhere, by comparison, there is very little systems perspective in the field. There now exists a critical mass of faculty in this area at Berkeley who have an interest and innovative research ideas in this field. Three new work units involving four faculty members are proposed. Professors Chua and Sangiovanni-Vincentelli are continuing in our program in this new area. In addition, we are adding two eminent Computer Science theorists, Professor Umesh Vazirani, and Professor Christos Papadimitriou to the program in this area.

Indeed this is a very forward-looking and high-risk enterprise. Some of the work proposed is highly theoretical. However, there is great interest and excitement on the part of the device researchers in our program for this new thrust. We have the expectation that as this effort gels, collaborations between the device researchers and the systems researchers will form.

Taken together, the proposed research involves 10 faculty and will provide support for 14 graduate students. The proposed budget envelope of $802K was developed in consultation with the JSEP TCC, which does represent a continuation in the reduction over time we have seen in recent years. We recognize that this is necessary in the face of the declining overall JSEP budget. However, we believe that the proposed program meets our objectives of a coherent, well formulated set of work units of the highest quality, with a strong emphasis on issues of greatest interest to JSEP.

PART I. SEMICONDUCTOR PHYSICS AND DEVICES

AREA OVERVIEW

In the area of Semiconductor Physics and Devices, we are pursuing a program in both electronics and optoelectronics, with efforts in basic physics, novel materials research, and novel device research.

This is a particularly interesting time in the world of silicon CMOS device research, an area in which Berkeley has traditionally maintained a very strong effort. The reason is that the ultimate limits of the MOSFET are beginning to come into focus. Production CMOS technology today has devices with minimum drawn gate lengths of about 0.35 μm, and advanced product development in progress at leading edge companies for 0.25 μm gate length. Extensive studies carried out at various laboratories in recent years, including ours supported by JSEP, have shown that devices with gate length down to 0.1 μm are practical. Although major technological and economic challenges must be met and overcome, today's best prediction is that production CMOS will reach 0.1 μm in about 10 years. At 0.1 μm dimensions and below, we should really be measuring in nm, and thus we leave the realm of microelectronics and enter into the world of nanoelectronics. The interesting question we now ask is whether the first practical nanoelectronic device will be some version of a MOSFET. We can see that a number of physics issues bear on this question and what the ultimate limit might be. A few of the more important limiting phenomena are statistical variations in device characteristics due to the small number of dopants in each device, carrier scattering lengths that become comparable to device dimensions, direct tunneling in thin gate dielectric, and quantum phenomena for confined carriers.

Progress in material processing can have a significant impact in this area by making possible novel device structures. In particular, silicon-on-insulator (SOI) material enables a new degree of freedom in the design of silicon nanoelectronics. SOI is made possible by recent innovations in subsurface electronic material synthesis. Further progress in this area can provide even greater flexibility by making it possible to form other buried materials including silicon nitride, silicon carbide, and even buried microvoids.

In optoelectronics, we see a similar interplay of research in physics, materials, and device structures leading to innovations that can be incorporated into optical systems. A driving force in this area is the pull from the systems side for components that enable wavelength division multiplexing (WDM) for ultra-wideband all-optical data networks. Such networks are envisioned to support up to about 30 wavelength channels, with a data rate in each channel of 10 Gbit/sec. A major challenge in such a system is all-optical packet routing, in which data packets are routed through the network from the launch point all the way to the ultimate destination without ever being converted into electronic signals.

Another area of great excitement in optoelectronics today is the use of GaN based hetero-structures for blue LEDs and in December, 1995, the first blue solid-state laser based on GaN technology came out of Japan. The burning desire for a practical blue diode laser source for a tremendous variety of uses had been unfulfilled in spite of great efforts until this breakthrough occurred. The same key materials processing advance that has made GaN based optoelectronic devices possible, namely p-type doping, also makes possible GaN electronic devices which, due to the wide bandgap of GaN, have great potential for high temperature, high power operation.

The first three work units comprise a tightly coupled effort in physics, materials, and device structures aimed at silicon nanoelectronics. Professors Hu and Bokor share a strong interest in explor-

ing the physics issues that will ultimately limit silicon MOSFET's. They have collaborated strongly and published jointly during the current contract period. Professor Hu's work emphasizes measurements in device structures, and device innovation, while Professor. Bokor's research involves the use of novel techniques in ultrafast laser spectroscopy to study carrier transport physics under high field conditions in silicon. Both efforts are well supported by facilities in the Berkeley Microlab. A new Ti:sapphire femtosecond laser system was built in Professor Bokor's laboratory during the current contract period, partially supported by JSEP funding. Professors Hu and Cheung are co-investigators on the use of sub-surface materials synthesis. This research focuses on the synthesis of SOI material, which has been identified by Professor Hu's device research as a very promising substrate for silicon nanodevices. They will also explore the possibilities of synthesizing other buried layer materials including silicon nitride and silicon carbide for use in more novel device structures. A specially constructed plasma immersion implantation (PII) reactor is available for these studies. Materials characterization facilities including cross-sectional TEM and Rutherford backscattering analysis are available on campus and at nearby Lawrence Berkeley National Laboratory.

Professor Lau and Professor Chang-Hasnain interact in their respective work units aimed at components for all-optical WDM networks. Professor Lau's concentration is on the influence of carrier dynamics on modulation and frequency translation in edge-emitting quantum well lasers, while Professor Chang-Hasnain's concentration is on vertical cavity surface emitting laser (VCSEL) fabrication and characterization. They plan to collaborate on noise and modulation response in VCSELs. A workhorse MBE facility has been made available in Cory Hall for Professor Chang-Hasnain's use in growing GaAs epi-layers for VCSELs. She has completely overhauled an oxidation furnace in the Berkeley Microlab for research on AlAs oxidation for oxide-confined VCSELs. Her work also makes heavy use of materials characterization facilities on campus including TEM, photoluminiscence, X-ray diffraction, and Auger analysis. Professor Bokor interacts with Professor Lau and Chang-Hasnain in the area of ultrafast carrier dynamics in GaAs. Professor Bokor is also interacting with Professors Weber and Cheung in the GaN effort. His group will explore the use of GaN for optoelectronic switching as well as study high field carrier dynamics in GaN using THz pulses.

All of these work units will make use of a new adjunct to the Berkeley Microlab known as the Integrated Materials Lab (IML). This new facility, funded by NSF under an Academic Research Infrastructure grant became fully operational during the current contract period. The IML contains an MBE system equipped with a plasma nitrogen source for GaN growth, a modified SEM for electron-beam lithography, a high resolution X-ray diffractometer, and a pulsed laser ablation deposition system.

Chenming HU

Current Position:

Professor, Electrical Engineering and Computer Sciences, University of California at Berkeley.

Education:

Ph.D. and M.S., Electrical engineering, University of California at Berkeley, 1970-1973.

B.S., National Taiwan University.

Area of Research:

VLSI devices, silicon-on-insulator devices, hot electron effects, thin dielectrics, electromigration, circuit reliability simulation, nonvolatile semiconductor memories, electro-optics, solar cells and power electronics.

Experience:

1976-Present: Professor, Electrical Engineering, University of California at Berkeley.

1973-Present: Consultant, Electronics industry and advisor to many governmental and educational institutions.

1980-1981: Manager of nonvolatile Memory Development at National Semiconductor.

1973-1976: Assistant Professor, Massachusetts Institute of Technology.

Honors and Awards:

Honorary Professor of Beijing University and Tsinghua University, China and of the Chinese Academy of Science.

Fellow of the Institute of Electrical and Electronic Engineers.

1993 Semiconductor Research Corporation Outstanding Inventor Award

1991 Design News Excellence in Design Award and the 1991 Semiconductor Research Corporation Technical Excellence Award for leading the development of an IC reliability simulator, BERT.

Relevant Publications:

Books and Book Chapters

1. C. Hu and R.M. White, *Solar Cells -- from Basics to Advanced Systems,* McGraw-Hill, New York, 267 pages, 1983.

2. C. Hu, *Hot Carrier Effects,* Chapter 3 of Advanced MOS Device Physics, N. G. Einspruch, Editor, Academic Press, pp. 119-160, 1989

3. C. Hu, Editor, *Nonvolatile Semiconductor Memories -- Technologies, Design and Applications,* IEEE Press, New York, 479 pages, 1991.

4. C. Hu, *Devices and Technology Impact on Low Power Electronics,* Chapter 2 of Low Power Design Methodologies," J.M. Rabaey and M. Pedram Editors, Kluwer Publishers, 1996.

Articles

Over 450 research articles including these recent ones:

1. F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P.K. Ko, C.Hu, "A Dynamic Threshold Voltage MOSFET (DTMOS) for Very Low Voltage Operations," *IEEE Electron Devices Letters,* Vol. 15, no.

12, December 1994, pp. 510-512.

2. M. Chan, J.C. King, P.K. Ko, C. Hu, "SOI/Bulk Hybrid Technology on SIMOX Wafers for High Performance Circuits with Good ESD Immunity," *IEEE Electron Device Letters*, Vol. 16, no. 1, January 1995, pp. 11-13.

3. Invited Paper, C. Hu, "Circuit Reliability Simulation," *Materials Research Society Spring Meeting Abstracts*, San Francisco, CA, April 1995, p. 17.

4. T. Horiuchi, J.D. Burnett, C. Hu, "Bipolar Transistor Degradation Under Dynamic Hot Carrier Stress," *Solid State Electronics*, Vol. 38, no. 4, April 1995, pp. 787-789.

5. S.B. Kuusinen, C. Hu, "Hot-Carrier Induced Degradation Paths Modeled by Rule-Based Analysis," *Proceedings of 1995 IEEE Custom Integrated Circuits Conference*, San Jose CA, May 1995, pp. 69-72.

6. J.C. Chen, C. Hu, Z. Liu, P.K. Ko, "Realistic Worst-Case SPICE File Extraction Using BSIM3," *Proceedings of 1995 IEEE Custom Integrated Circuit Conference*, San Jose, CA, May 1995, pp. 375-378.

7. Invited Paper, C. Hu, N.W. Cheung, J. Tao, "Electromigration Under Bidirectional Current Stress," *Electrochemical Society Symposium Abstracts*, Reno, NV, May, 1995, p. 127.

8. Y.C. King, B. Yu, J. Pohlman, C. Hu, "Punch through Transient Voltage Suppressor for Low Voltage Electronics," *IEEE Electron Device Letters*, Vol. 16, no. 7, July 1995, pp. 303-305.

9. W.S. Choi, F. Assaderaghi, Y.J. Park, H.S. Min, C. Hu, R.W.Dutton, "Simulation of Deep Submicron SOI N-MOSFET Considering the Velocity Overshoot Effect," *IEEE Electron Device Letters*, Vol. 16, no. 7, July 1995, pp. 333-335.

Jeffrey BOKOR

Current Position:

Professor, Electrical Engineering and Computer Sciences, University of California at Berkeley.

Education:

Ph.D., Electrical Engineering, Stanford University,1980.

M.S., Electrical Engineering, Stanford University, 1976.

B.S., Electrical Engineering, Massachusetts Institute of Technology, 1975.

Area of Research:

Deep sub-micron VLSI technology, fabrication, and device physics
Ultrafast carrier dynamics in electronic materials
EUV and soft x-ray optics and lithography

Experience:

1992-present: Professor, Electrical Engineering and Computer Sciences, University of California, Berkeley.

1990-1992: Department Head, ULSI Technology Research Department, AT&T Bell Laboratories, Murray Hill, NJ.

1987-1990: Department Head, Laser Science Research Department, AT&T Bell Laboratories, Holmdel, NJ.

1980-1987: Member of Technical Staff, Quantum Electronics Research Department, AT&T Bell Laboratories, Holmdel, NJ.

Professional Activities/Memberships:

American Physical Society

Institute of Electronics and Electrical Engineers

American Association for the Advancement of Science

Honors and Awards:

Fellow, Optical Society of America.

Fannie and John Hertz Foundation, Graduate Fellowship, 1976-1980.

Relevant Publications:

1. "Advanced lithography for ULSI," J. Bokor, A. R. Neureuther, and W. G. Oldham, IEEE Circ.and Dev. **12,** 11 (1996).

2. "At-wavelength testing of optics for EUV," K. A. Goldberg, R. Beguiristain, J. Bokor, H. Medecki, K Jackson, D. T. Attwood, G. E. Sommargren, J. P. Spallas, And R. Hostetler, Proceedings of the SPIE **2437**, 347 (1995).

3. "Progress towards λ/20 extreme ultraviolet interferometry." K. A. Goldberg, R. Beguiristain, J. Bokor, H. Medecki, D. T. Attwood, K Jackson, E. Tejnil, and G. E. Sommargren, J. Vac. Sci. Technol. B **13,** 2923 (1995).

4. "Surface Adhesion Reduction in Silicon Microstructures Using Femtosecond Laser Pulses",

N.C. Tien, S. Jeong, L.M. Phinney, K. Fushinobu, and J. Bokor, Appl. Phys. Lett. **68,** 197 (1995).

5. "A Dynamic Threshold Voltage MOSFET (DTMOS) for Very Low Voltage Operation," F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P.K. Ko and C. Hu, IEEE Electron Device Lett. **15**, 510 (1994)

6. "Saturation velocity and Velocity Overshoot of Inversion Layer Electrons and Holes, "F. Assaderaghi, D. Sinitsky, H. Gaw, J. Bokor, P.K. Ko, and C. Hu, IEDM Technical digest, p. 479, 1994.

7. "Point Diffraction Interferometry at EUV Wavelengths," K.A. Goldberg, R. Beguiristain, J. Bokor, H. Medecki, K. Jackson, D.T. Attwood, G.E. Sommargren, J.P. Spallas, and R. Hostetler, in Extreme ultraviolet Lithography, D.T. Attwood and F. Zernike, eds. (Optical Society of America, Washington, DC, 1994)

8. "Undulator Radiation for at Wavelength Interferometry of Optics for Extreme-Ultraviolet Lithography," D. Attwood, G. Sommargren, R. Beguiristain, K. Nguyen, J. Bokor, N. Ceglio, K. Jackson, M. Koike, and J. Underwood, Appl. Opt. **32**, 7022 (1993).

9. "Soft-X-Ray Projection Lithography Experiments Using Schwarzchild Imaging Optics", D.A. Tichenor, G.D. Kubiak, M.E. Malinowski, R.H. Stulen, S. J. Haney, K.W. Berger, L. A. Brown, W.C. Sweatt, J.E. Bjorkholm, R.R. Freeman, M.D. Himel, A. A. MacDowell, D. M. Tennant, O. R. Wood II, J. Bokor, T.E. Jewell, W. M. Mansfield, D.L. White, W. K. Waskiewicz, and D. L. Windt, Appl,. Opt. **32** 7068 (1993)

10. "Ultrashallow p^+n junctions formed by diffusion from a RTCVD-deposited B:Ge layer," B. Park, C. A. King, D. J., Eaglesham, T. W. Sorsch, B. Weir, H. Luftman, J. Bokor, and Y. O. Kim, Proceedings of the SPIE **2091**, 122 (1993).

11. "Efficient coupling of high-intensity subpicosecond laser pulses into solids," M. Murnane, H. Kapteyn, S. Gordon, J. Bokor, E. Glytsis, and R. Falcone, Appl. Phys. Lett. **62,** 1068 (1993).

12 "Direct measurement of nonequilibrium electron-energy distributions in subpicosecond laser-heated gold films," W. S. Fann, R. Storz, H. Tom, and J. Bokor, Surface Sci. **283,** 221 (1993).

13. "High intensity above-threshold ionization of He," U. Mohideen, M. H. Sher, H. W. K. Tom, G. D. Aumiller, O. R. Wood II, R. R. Freeman, J. Bokor and P. H. Bucksbaum, Phys. Rev. Lett. **71,** 509 (1993).

14. "Soft-x-ray projection imaging using a 1:1 ring-field optic," A. A. MacDowell, J. E. Bjorkholm, K. Early, R. R. Freeman, M. D. Himel, P. P. Mulgrew, L. H. Szeto, D. w. Taylor, D. M. Tennant, O. R. Wood, J. Bokor, L. Eichner, T. E. Jewell, W. K. Waskiewicz, D. L. White, D. L. Windt, R. M Souza, W. T. Silfvast, and F. Zernike, Appl. Opt. **32,** 7072 (1993).

15. "89 GHz fTRoom-temperature Silicon MOSFET's," R.H. Yan, K.F. Lee, D.YI Jeon, Y.O. Kim, B.G. Chin, M.D. Morris, K. Early, P. Mulgrew, W. M. Mansfield, R.K. Watts, A. M. Voschenkov, J. Bokor, R.G. Swartz and A. Ourmazd, IEEE Electron Device Lett. **13** 256 (1992)

16. "Direct Measurement of Nonequilibrium Electron-energy Distributions in Subpicosecond Laser-heated Gold Films," W. Fann, R. Storz, H.W.K. Tom and J. Bokor, Phys. Rev. Lett. **68**, 2834 (1992).

17. "Ultrashallow Junctions for ULSI Using As Dimer Ion Implantation and Rapid Thermal Anneal," B. Park, J. Bokor, H. Luftman, C. Rafferty, and M. Pinto, IEEE Electron Device Lett. **13**, 507 (1992).

Nathan W. CHEUNG

Current Position:

Professor, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley.

Education:

Ph.D., Applied Physics, California Institute of Technology, 1980.

B.S., Physics, Massachusetts Institute of Technology, 1971.

Area of Research:

Ion-beam and plasma technologies, Silicon and III-V integrated-circuit processing, electronic materials, integrated-circuit reliability and thin-films technologies.

Experience:

1984-1989: Associate Professor of Electronics Engineering and Computer Sciences, University of California at Berkeley.

1980-1983: Assistant Professor of Electronics Engineering and Computer Sciences, University of California at Berkeley.

1986-Present: Associate Faculty, Center for Advanced Materials, Lawrence Berkeley Laboratory.

1987: Visiting Associate Professor, National Research Resources for Submicron Structure, Cornell University, 1987.

1980: Research Fellow, California Institute of Technology.

1979: Visiting Associate, Bell Telephone Laboratories, Murray Hill, New Jersey.

1976: Research Physicist, Exxon Research Laboratory, Linden, New Jersey.

Professional Activities:

Chairman, 6th International Conference on Ion Implantation Technology, 1986.

Chairman, First International Conference on Semiconductor and Integrated Circuit Technology, 1986.

Chairman, MRS Symposium on Electronic Materials Characterization, 1986.

Chairman, MRS Symposium on Advanced Ion Beam Processing of Electronic Materials, 1989.

Member, Advisory Committee of International Conference of Ion Implantation Technology, 1986-Present.

Member, Advisory Committee of International Symposium on Materials Synthesis and Modification by Ion Beams and Laser Beams, 1992-Present.

Editorial Advisory Board, Semiconductor International, 1993.

Honors and Awards:

IBM Faculty Development Award, 1983.

Relevant Publications:

N.W. Cheung, "Plasma Immersion Ion Implantation," Transactions of the Materials Research Society of Japan, Vol. 17, pp.543-548 (1994). **[invited paper]**.

Seongil Im, Jack Washburn, Ronald Gronsky, Nathan W. Cheung, Kin Man Yu, and Joel W. Ager, "Optimization of Ge/C ratio for compensation of misfit strain in solid phase growth of SiGe layers," Appl. Phys. Lett., Vol. 63, pp.2682-2684 (1993).

Seongil Im, Jack Washburn, Ronald Gronsky, Nathan W. Cheung, and Kin Man Yu, "Defect Control During Solid Phase Epitaxial Growth of SiGe Alloy Layers", Appl. Phys. Lett., Vol. 63, pp. 929-931 (1993).

Ashawant Gupta, M. Mahmudur Rahman, Jianmin Qiao, Cary Y.Yang, Seongil Im, Nathan W. Cheung, and Paul K.L. Yu, "Donor Complex Formation due to High-Dose Ge Implant into Si," J. Appl. Phys., Vol. 75, No. 8, pp. 4252-4254 (1994).

E.C. Jones, W. En, S. Ogawa, D.B. Fraser, and N.W. Cheung, "Anomalous Behavior of Shallow BF3 PIII," J. Vac. Sci. Technol., Vol. B12, No. 2, pp. 956-961(1994).

W. En and N.W. Cheung, Analytical Modeling of Plasma Immersion Ion Implantation Target Current Using the SPICE Circuit Simulator," J. Vac. Sci. Technol., Vol. B12, No.2, pp.833-837 (1994)

C. Yu and N.W. Cheung, Trench Doping Conformality by Plasma Immersion Ion Implantation," IEEE Elec. Dev. Lett., Vol. 15, pp. 196-198 (1994).

W. En, M. Lieberman, and N.W. Cheung, Comparison of Experimental Target Currents With Analytical Model Results for Plasma Immersion Ion Implantation," IEEE Tran. Plasma Sciences, Vol. 23, No. 3, pp. 415-421 (1995).

W. En and N.W. Cheung, "Modeling of charging effects in plasma immersion ion implantation," Nuclear Instrum. Methods, Vol. B96, pp.435-439 (1995).

X. Lu and N.W. Cheung, *Solid Phase Epitaxy of Implanted Si-Ge-C Alloys,* Materials Research Society Proceedings, Vol.388, pp. (1995).

N.W. Cheung, W. En, J. Gao, S.S. Iyer, E.C. Jones, B.P. Linder, J.B. Liu, X. Lu, J. Min and B. Shieh, *Plasma Immersion Ion implantation for Electronic Materials Applications,* Ext. Abstr. of 1995 Int. Conf. on Sol. St. Dev. and Mater., (Osaka, Japan, August 1995), pp 351-353. **[invited paper].**

J.B. Liu, S.S.K. Iyer, J. Min, P.K. Chu, R. Gronsky, C. Hu, and N.W. Cheung, *Synthesis of Buried Oxide by Plasma Implantation with Oxygen and Water Plasma,* Proceedings of IEEE International SOI Conference, pp.166-167, 1995.

Kam-Yin LAU

Current Position:

Professor, Electrical Engineering and Computer Sciences, University of California at Berkeley.

Education:

Ph.D., Electrical Engineering, California Institute of Technology, Pasadena. Thesis Title: Ultra-high Frequency Dynamics of Semiconductor Injection Lasers, June 1981.

MS, Electrical Engineering, California Institute of Technology, Pasadena, June 1978.

B.S., Engineering and Applied Science, California Institute of Technology, Pasadena. GPA: 4.1/4.0. Class ranking: 1/166,1978.

Area of Research:

High speed optoelectronic devices, millimeter wave frequency mode-locked lasers, optically controlled phased-array antennae, lightwave networks.

Experience:

7/90-Present: Professor, Department of Electrical Engineering and Computer Science, University of California at Berkeley.

10/88-7/90: Associate Professor of Electrical Engineering, Columbia University. Director of Lightwave Communication Laboratory of the NSF Center for Telecommunications Research at Columbia University.

10/81-10/88: Ortel Corporation, Chief Scientist.

6/81-10/81: Research Fellow, California Institute of Technology.

6/79-6/81: Jet Propulsion Laboratory, Pasadena, California. Engineer, Fiber-Optics Development.

6/78-8/78: Bell Laboratories, Holmdel, New Jersey. Summer Research Associate.

6/77-9/77: Bell Laboratories, Crawford Hill Laboratory, Holmdel, New Jersey. Summer Research Associate.

Patents:

US Patent # 4239337, Magneto-optic Waveguide Modulator

US Patent # 4287606, Fiber-optic Precise Frequency and Timing Stabilization Scheme

US Patent # 4562569, Bistable Injection Laser

US Patent # 4764934, High Power Superluminescent Diode

Honors and Awards:

J.E. Froehlich Memorial Award for undergraduate research, California Institute of Technology, 1977.

Presidential Young Investigator Award, 1989.

Fellow, Optical Society of America.

Relevant Publications:

1. D.M. Curtrer, J.B. Georges, T.H. Le and K.Y. Lau, "Dynamic range requirements for optical

transmitters in fiber-fed microcellular networks", IEEE Photonics Technology Letters, vol.7, no. 5, pp. 564 (1995)

2. D. M. Cutrer and K. Y. Lau, "Ultralow power optical interconnect with zero-biased ultralow threshold laser- how low is enough?" IEEE Photon. Tech. Lett., vol. 7, pp 4 (1995).

3. J.B. Georges, D. M. Cutrer, M. H. Kiang and K. Y. Lau, "Multichannel millimeter wave subcarrier transmission by resonant modulation of monolithic semiconductor lasers", IEEE Photon. Tech. Lett., vol. 7, pp 431, (1995).

4. D.M. Cutrer, J.B. Georges, T.C. Wu, B. Wu and K. Y. Lau, "Resonant modulation of single contact monolithic semiconductor lasers at millimeter wave frequencies", Appl. Phys. Lett., vol 66, pp. 2153 (1995).

5. J.B. Georges, D. M. Cutrer and K. Y. Lau, "Theory of resonant modulation at millimeter wave frequencies of inhomogeneously biased monolithic quantum well-lasers", IEEE Photon. Tech. Lett., vol. 7, pp 263, (1995).

6. K. Y Lau, C. M. Gee, T. R. Chen, N. Bar-Chaim and I. Ury, "Signal-induced noise in fiber-optic links using directly modulated Fabry-Perot and distributed feedback laser diodes", IEEE J. Lightwave Tech., vol. 11 1216 (1993).

7. D.M. Cutrer, J.B. Georges and K. Y. Lau, "Building the fiber-optic infrastructure for wireless communications", IEEE Circuit and Device Magazine, July, 1995, pp. 13.

Connie CHANG-HASNAIN

Current Position:

Professor, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley.

Education:

Ph.D., 1987, Electrical Engineering, University of California at Berkeley

M.S.,1984, Electrical Engineering, University of California at Berkeley

B.S., 1982, Electrical and Computer Engineering, University of California at Davis

Area of Research:

Two-dimensional Semiconductor Optoelectronic Devices

Novel Epitaxial Growth and Fabrication Techniques

Novel Interconnects and Communications Applications

Experience:

1/96-Present: Professor, Electrical Engineering and Computer Sciences, University of California at Berkeley

9/95-12/95: Associate Professor, Electrical Engineering, Stanford University

4/92-8/95: Assistant Professor, Electrical Engineering, Stanford University

10/87-3/92: Member of Technical Staff, Photonic Science and Technology Research Division, Bellcore, Red Bank, NJ

Professional Activities:

Program Chair, Conference on Lasers and Electro-Optics (CLEO), Baltimore, May 1997

Conference Chair, Conference on High Speed Optoelectronic Devices and Systems, Snowbird Utah, August 11-15, 1996

Editor of the IEEE Circuits and Devices Magazine, 1994-1996

Chair of Optoelectronics Technical Group, OSA Technical Council, 199401996

Chair, CLEO Semiconductor Lasers Program Committee, 1994-1996

Chair, The 12th Semiconductor Lasers Workshop, 1995

Honors and Awards:

Presidential Faculty Fellow, 1994

Alfred P. Sloan Research Fellow, Sloan Foundation, 1994-1996

Distinguished Lecturer Award of IEEE Lasers and Electro-Optics Society, 1994

Young Alumnus of the Year, University of California at Davis, 1993

Reid and Polly Anderson Faculty Chair, 1992

Packard Fellow, Davis and Lucile Packard Foundation, 1992

National Young Electrical Engineer Award, National Science Foundation, 1992

Outstanding Young Electrical Engineering Award Winner, Eta Kappa NU, 1992

D.J. Sakrison Prize for the Best Ph.D. Dissertation from University of California at Berkeley, 1989.

Relevant Publications:

Authored 60 papers in leading technical journals, 2 invited papers, 3 book chapters, presented 40 invited talks and 59 conference presentations.

Y.A. WU, G.S. Li, R. Nabiev, K.D. Choquette, C. Caneau and C.J. Chang-Hasnain, "Performance of Passive Antiguide Region Vertical Cavity Lasers", IEEE J. of Selected Topics in Quantum electron, 1,2, June, 1995.

L.E. Eng, K. Bacher, W. Yuen, J.S. Harris and C.J. Chang-Hasnain, "Multiple Wavelength Vertical-Cavity Laser Arrays on Patterned Substrates". IEEE J. of Selected Topics in Quantum Electron, 1,2, June 1995.

E.C. Vail, M.S. Wu, G.S. Li, L.E. Eng, and C.J. Chang-Hasnain, "Highly Tunable (70 nm) Optical Filter using GaAs DBR Movable Cantilevers", Electronics Letters, 31,3, pp 228-229, Feb. 2, 1995.

C.J. Chang-Hasnain, Y.A. Wu, G.S. LI, G. Hasnain, K.D. Choquette, C. Caneau and L. T. Florez, "Low Threshold Buried Heterostructure Vertical Cavity Surface Emitting Laser," "Applied Physics Lett., Vol. 63, No. 10, pp 1307-1309, Sept.6, 1993.

C.J. Chang-Hasnain, J.P. Harbison, C.E. Zah, M.W. Maeda, L.T. Florez, N.G. Stoffel, and T.P. Lee, "Multiple Wavelength Tunable Vertical Cavity Surface Emitting Laser Arrays", IEEE J. Quantum Electron, 27, 6 pp. 1368-1376, June, 1991.

Eicke WEBER

Current Position:

Professor, Materials Science, Department of Materials Science and Mineral Engineering, University of California at Berkeley.

Education:

Ph.D., University of Cologne, West Germany (Thesis: Point Defects in Deformed Silicon),1976.

M.S., University of Cologne, West Germany, 1973.

B.S., University of Cologne, West Germany 1970.

Area of Research:

Nature and Electronic Properties of Defects in III/V and II/VI.

Compounds Defects Formed in III/V Thin Films and Interfaces.

Transition Metal Gettering in Silicon.

Electron Paramagnetic Resonance of Defects in Semiconductors.

Scanning Tunneling Microscopy of Thin Films and Interfaces.

Experience:

1991-Present: Professor, Materials Science, University of California at Berkeley.

1987-1991: Associate Professor of Materials Science, University of California at Berkeley.

1983-1987: Assistant Professor of Materials Science, University of California at Berkeley.

1987-Present: Principal Investigator, Center for Advanced Materials, Lawrence Berkeley Laboratory.

1982-1983: Research Associate, University of Lund (Sweden).

1978-1979: International Fellow, Institute for the Study of Defects in Solids, SUNY, Albany.

1976-1982: Scientific Assistant, University of Cologne, West Germany.

1973-1976: Assistant Lecturer, Technical University of Aachen, West Germany.

Professional Activities:

Program-chair, 7th International Conference on Semi-Insulating III/V Materials, 1992.

Co-chair, MRS Symposium on Defect Engineering in Semiconductor Technology, 1992.

Co-chair, MRS Symposium on Low-Temperature GaAs and Related Compounds, 1991.

Co-chair, MRS Symposium on Electronic and Device Properties of Heterostructures, 1989.

Chair, Gordon Conference on Defects in Semiconductors, 1987.

Chair, 2 International Conference on Defect Recognition and Image Processing in III-V Semiconductors, 1987.

Vice-chair, Gordon Conference on Defects in Semiconductors, 1985.

Session chair at Gordon Conferences and other National and International meetings.

Member, National Research Council panel for the Associateship program 1993.

Member, DOE Research Assistance Task Force on Photovoltaic Materials, 1992.

Member, Electronic Materials Committee of TMS 1989-Present.

Member, International Advisory Committee.

International Conference on Gettering and Defect Engineering in Semiconductors (GADEST) 1987-Present.

International Conference on Defects in Semiconductors (ICDS), 1986-92.

International Conference on Defect Recognition and Image Processing in Semic, (DRIP) 1985-1991.

Member, Program Committee of ICDS, 1982, 1984, 1991.

Honors and Awards:

Prince Distinguished Lecturer, Arizona University, Tempe, 1983.

IBM Faculty Development Award, 1984.

Visiting Professor, Tohoku University, Sendai, 1990.

Outstanding Performance Award, Lawrence Berkeley Laboratory, 1994

Visiting Fellow, Australian National University, Canberra 1994

Humboldt Senior US Scientist Award, 1994.

Relevant Publications:

T.C. Fu, N. Newman, E. Jones, J.S. Chan, X. Liu, M.D. Rubin, N.W. Cheung, and E.R. Weber, "The influence of nitrogen ion energy on the quality of GaN films grown with molecular beam epitaxy," J. Electr. Mat. 24, 249 (1995).

N. Newman, T. C. Fu, X. Liu, Z. Liliental-Weber, M. Rubin, J. S. Chan, E. Jones, J. T. Ross, I. Tidswell, K. M. Yu, N. Cheung, and E. R. Weber, "Fundamental materials-issues involved in the growth of GaN by molecular beam epitaxy," MRS Symp. Proc. vol. 339, 483 (1994).

J.F. Zheng, M. Salmeron and E.R. Weber, "Atomic resolution studies of dopant effects on intermixing in AlAs/GaAs short period superlattices,"Solid State Commun. 93, 419 (1995).

X. Liu, A. Prasad, J. Nishio, E.R. Weber, Z. Liliental-Weber, and W. Walukiewicz, "Native Point Defects in low-temperature grown GaAs," Appl. Phys. Lett. 67, 279 (1995).

H.Fujioka, J.Krueger, A.Prasad, X.Liu, E.R.Weber, and A.K.Verma, "Annealing Dynamics of Arsenic-Rich GaAs formed by Ion Implantation," J. Appl. Phys. 78, 1470 (1995).

A.K. Verma, J.S. Smith, H. Fujioka, and E.R. Weber, "Characterization of low-temperature Al/sub x/Ga/sub 1-x/As lattice properties using high resolution X-ray diffraction," J. Appl. Phys. 77, 4452 (1995).

H. Fujioka, E.R. Weber, and A.K. Verma, "Conduction mechanism in arsenic implanted GaAs," Appl. Phys. Lett.66, 2116 (1995).

P. Phatak, N. Newman, P. Dreszer, and E.R. Weber, "Experimental Determination of the Pressure Dependence of the Barrier Height of Metal (n-type GaAs) Schottky Contacts: a Critical Test of Schottky-Barrier Models," Phys. Rev. B51, 18003 (1995).

Y. Chen, X. Liu, Z. Liliental-Weber, and E. R. Weber, "Structures and electronic properties of misfit dislocations in ZnSe/GaAs(001) heterojunctions, "Appl. Phys. Lett. 65, 549 (1994).

A.K. Verma, J.S. Smith, H. Fujioka, and E.R. Weber, "Characterization of low-temperature AlGaAs lattice properties using high resolution X-ray diffraction," J. Appl. Phys. 77, 4452 (1995).

K. Uchida, P.Y. Yu, N. Noto, Z. Liliental-Weber, and E.R. Weber, "Comparison Between Photolu-

minescence and Raman Scattering in Disordered and Ordered Alloys of GaInP," Phil. Mag. B70, 453 (1994).

X.W. Lin, Z. Liliental-Weber, J. Washburn, E.R. Weber, A. Sasaki, A. Wakahara, and Y. Nabetani,

"Molecular Beam Epitaxy of InAs and its Interaction with a GaAs Overlayer on Vicinal GaAs (001) Substrates, "J. Vac.Science & Techn. B12, 2562 (1994).

M. VanSchilfgaarde, E.R.Weber, and N. Newman, "Pressure Dependence of III-V Schottky Barriers - A Critical Test of Theories for Fermi Level Pinning," Phys. Rev. Lett., 73, 581 (1994).

J.F. Zheng, J.D. Walker, M.B. Salmeron, and E.R. Weber, "Interface Segregation and Clustering in Strained-Layer InGaAs/GaAs Heterostructures Studied by Cross-Sectional Scanning Tunneling Microscopy," Phys. Rev. Lett. 72, 2414 (1994).

J.F. Zheng, X. Liu, N. Newman, E.R. Weber, D.F. Ogletree, and M. Salmeron, "Scanning Tunneling Microscopy Studies of Si Donors in GaAs," Phys. Rev. Lett. 72, 1490 (1994)

UNIVERSITY: UC BEKELEY **LAB: ERL**
JOINT SERVICES ELECTRONICS PROGRAM **RESEARCH UNIT: I-A**
LAST YEAR'S RESEARCH UNIT: I-B

TITLE OF INVESTIGATION: Silicon MOSFET Scaling Limits for Low Power Electronics

SENIOR INVESTIGATORS: Chenming Hu **TELEPHONE:** 510-642-3393

JSEP FUNDS (CURRENT):

PI	TITLE	PERIOD	AMOUNT (1994-1997)
CH	Silicon Bipolar and MOS Devices Nanometer Dimensions	6/94-1/97	$268,551

JSEP FUNDS (PROPOSED):

1997-1998	$95,000
1998-1999	$95,000
1991-2000	$95,000

OTHER FUNDING:

PI	TITLE	PERIOD:	AMOUNT:	SPONSOR:
CH	IC Manufacturing-Induced Oxide Damage	7/1/94-6/30/97	$159,000	ONR
CH JB	Advanced Silicon Fet Physics and Device Structures	10/1/94-9/30/96	$400,000	AFOSR
CH	Circuit Reliability Hot-Electron Model and Simulation	9/1/95-10/31/96	$169,167	SRC
CH	MOS Device Research (Pending)	7/1/96-6/30/97	$209,000	MICRO
CH	A VLSI-Compatible New Device for 0.5V Low-Power Electronics (Pending)	1/15/96-9/30/98	$363,891	ONR
CH	A New Silicon Device for Low-Voltage Low Power VLSI (Pending)	6/1/96-5/31/2000	$430,000	NSF

TOTAL NUMBER OF PROFESSIONALS

CURRENT - FACULTY:	1 @ 1 week of summer
CURRENT - STUDENT:	1 @ 49.9% academic; 100% summer
PROPOSED FACULTY:	1 @ 1 week of summer
PROPOSED STUDENTS:	1 @ 49.9% academic; 100% summer

Silicon MOSFET Scaling Limits for Low Power Electronics

FACULTY INVESTIGATORS: CHENMING HU

SCIENTIFIC OBJECTIVE

The objective is to investigate the physical limits, behaviors, and new phenomena in MOS with dimensions below 100 nm(0.1 μm). For the MOS devices, topics to be studied include statistical variations of device behaviors due to small number of dopants in each device, mobility and velocity overshoots, gate induced band-to-band tunneling, direct tunneling in thin gate dielectric, single- electron Random Telegraph Noise, quantum phenomena in confined carriers, hot-carrier phenomena, radiation effects, reliability and speed at low operating voltages below 1V, and SOI devices.

STATE-OF-THE-ART

CMOS technology today has devices with minimum drawn dimensions of about 0.25 μm. Extensive studies carried out at various laboratories in recent years, including ours supported by JSEP, have demonstrated that devices with channel length down to 0.1 μm are practical. Although technological and financial roadblocks still exist, today's best prediction is that production CMOS technologies will reach 0.1 μm in about 10 years. The outlook beyond that is however unclear.

While there is general agreement that velocity overshoot will become significant in very small-size MOS devices, whether it has a major effect on the drain current of devices with channel length around 0.1μm at room temperature remains a controversial subject after several years of exploration. Further experimental and theoretical studies that extend beyond the 0.1μm boundary are necessary to clarify the picture. As circuit speed is directly proportional to the device current, the findings will determine the performance of the future CMOS technology.

It is generally recognized that the minimum channel length of MOSFET will depend on the minimum acceptable gate oxide thickness. However, it is not clear what that minimum acceptable oxide thickness would be – time-dependent breakdown reliability has not been studied in such small thickness and low voltage regime. Tunnel current itself may set a lower bound for oxide scaling due to power or fuctionality considerations. It is not known if oxide charge trapping in the presence of very large tunneling current will set the oxide scaling limit.

In order to use very thin gate oxide, the substrate doping concentration must be raised to achieve a certain threshold voltage. Another scaling limit may be maximum substrate doping concentration, above which there would be too much junction leakage. This value is often assumed to be 10^{18} cm^{13} without support data. There may be other ways of adjusting the threshold voltage and controlling the short-channel effect without using very high substrate doping concentrations.

PROGRESS SINCE LAST MAJOR PROPOSAL

Using the "ashing" technique and scaling guidelines we developed under previous JSEP support, we have successfully fabricated MOSFET with channel lengths down to 0.08 μm.

Fabricated 0.25μm MOS-BJT Hybrid Device [1].

Published a study of future CMOS scaling and reliability [1][8].

Conducted a study of SOI for high speed ULSI [3].

Developed a novel method for contacting the body of SOI MOSFET and for making SOI MOSFET [4] in very thin silicon film with low series resistance [5].

Demonstrated that SOI MOSFET has very good hot electron reliability in comparison with bulk

device [6] and that ESD tolerance is only half that of bulk device [7].

Developed a model for defect breakdown in very thin SiO_2 at low voltage [9].

Conducted a study of electron and hole velocity overshoot in inversion layers [10].

Invented a novel dynamic – threshold MOSFET that can operate at ultra-low 0.5V with high speed and low leakage [11].

LIST OF PUBLICATIONS CITING JSEP SPONSORSHIP

[1] J.C. Chen, Z. Liu, J.T. Krick, P.K. Ko, C. Hu, "Degradation of N_2O Annealed MOSFET Characteristics in Response to Dynamic Oxide Stressing," *IEEE Electron Device Letters,* Vol. 14, No. 15, May 1993, pp. 225-227.

[2] S.A. Parke, C. Hu, P.K. Ko, "Bipolar -FET Hybride-Mode Operation of Quarter-Micrometer SOI MOSFET's," *IEEE Electron Device Letters,* Vol. 14, No. 15, May 1993, pp. 234-236.

[3] K.F. Schuegraf, C.C. King, C. Hu, "Impact of Polysilicon Depletion in Thin Oxide CMOS Technology," *Proc. of Tech. Papers, IEEE Int'l Symp. on VLSI Technology, Systems and Applications,* Taipei, Taiwan, May 12-14, 1993, pp. 86-90.

[4] F. Assaderaghi, K. Hui, S. Parke, J. Duster, P.K. Ko, C. Hu, "Study of Current Drive in Deep Sub-Micrometer SOI PMOSFET's," *Proc. of Tech. Papers, IEEE Int'l Symp. on VLSI Technology, Systems and Applications,* Taipei, Taiwan, May 12-14, 1993, pp. 232-236.

[5] K. Schuegraf, C. Hu, "Oxide Breakdown Model for Very Low Voltages," *IEEE Symp. on VLSI Technology,* Kyoto, JAPAN, May 1993, pp. 43-44.

[6] **Invited Paper**, C. Hu, "Future CMOS Scaling and Reliability," *Proc. of the IEEE,* Vol. 81, No. 5, May 1993, pp. 682-689.

[7] F. Assaderaghi, S. Parke, J. King, J. Chen, P.K. Ko, C. Hu, "High-Performance Sub-Quarter-Micrometer PMOSFET's on SOI," *IEEE Electron Device Letters,* Vol. 14, No. 6, June 1993, pp. 298-300.

[8] **Invited Paper**, C. Hu, "Silicon-on-Insulator for High Speed ULSI," Extended Abstracts of the *Int'l Conf. on Solid State Devices and Materials,* Chiba, Japan, August 1993, pp. 137-139.

[9] F. Assaderaghi, C. Hu, P.K. Ko, J. Duster, D. Sinitsky, J. Bokor, "Direct Observation of Velocity Overshoot in Silicon Inversion Layers," *TECHCON* Extended Abstracts, Sept. 1993, pp. 265-267.

[10]F. Assaderaghi, P.K. Ko, C. Hu, "Observation of Velocity Overshoot in Silicon Inversion Layer," *IEEE Electron Device Letters,* Vol. 14, No. 10, Oct. 1993, pp. 484-486.

[11]F. Assaderaghi, P.K. Ko, C. Hu, "Room Temperature Observation of Velocity Overshoot in Silicon Inversion Layers," *Proc. IEEE Int'l SOI Conf.*, Oct. 1993, pp. 116-117.

[12]K.F. Schuegraf, C. Hu, "Defect Breakdown Lifetime Projection of Thin SiO2 at Low Voltages," *Proc. Int'l Semiconductor Device Research Symp.*, Dec. 1993, pp. 253-256.

[13]M. Chan, Z.J. Ma, F. Assaderaghi, C.T. Nguyen, P.K. Ko, C. Hu, "A Low-Barrier Body Contact Scheme for SOI MOSFET's to Eliminate the Floating Body Effect," *Proc. Int'l Semiconductor Device Research Symp.*, Dec. 1993, pp. 341-344.

[14]M. Chan, F. Assaderaghi, S. Parke, C. Hu, P.K. Ko, "Recessed-channel Structure for Fabricating Ultrathin SOI MOSFET with Low Series Resistance," *IEEE Electron Device Letters,* Vol. 15, No. 1, January 1994, pp. 22-24.

[15]Z.J. Ma, H.J. Wann, M. Chan, J. King, Y.C. Cheng, P.K. Ko, C. Hu, "Characterization of Hot-Carrier Effects in Thin-Film Fully Depleted SOI MOSFET's," *1994 IEEE International Reliability Physics Symposium Proceedings,* April 1994, pp. 52-56.

[16]K.F. Schuegraf, C. Hu, "Effects of Temperature and Defects on Breakdown Lifetime of Thin SiO_2 at Low Voltage," *1994 IEEE International Reliability Physics Symposium Proceedings*, April 1994, pp. 126-135.

[17]M. Chan, S.S. Yuen, Z.J. Ma, K.Y. Hui, P.K. Ko, C. Hu, "Comparison of ESD Protection Capability of SOI and Bulk CMOS Output Buffers," *1994 IEEE International Reliability Physics Symposium Proceedings*, April 1994, pp. 292-298.

[18]K.F. Schuegraf, C. Hu, "Hole Injection SiO_2 Breakdown Model for Very Low Voltage Lifetime Extrapolation," *IEEE Transactions on Electron Devices*, Vol. 41, No. 5, May 1994, pp. 761-767.

[19]**Invited Review**, K.F. Schuegraf, C. Hu, "Reliability of Thin SiO_2," *Semiconductor Science and Technology*, Vol. 9, No. 5, May 1994, pp. 989-1004.

[20]Z.J. Ma, H.J. Wann, M. Chan, J.C. King, Y.C. Cheng, P.K. Ko, C. Hu, "Hot-Carrier Effects in Thin Film Fully-Depleted SOI MOSFET's," *IEEE Electron Device Letters*, Vol. 15, No. 6, June 1994, pp. 218-220.

[21]C. Hu, "MOSFET Scaling in the Next Decade and Beyond," *Semiconductor International*, June 1994, pp. 105-114.

[22]K. Schuegraf, C. Hu, "Effect of Temperature and Defects on Breakdown Lifetime of Thin SiO_2 at Very Low Voltages," *IEEE Transactions on Electron Devices*, Vol. 41, No. 7, July 1994, pp. 1227-1232.

[23]Z.J. Ma, Z. H. Liu, J.T. Krick, H.J. Huang, Y.C. Cheng, C. Hu, P.K. Ko, "Optimization of Gate Oxide N_2O Anneal for CMOSFET's at Room and Cryogenic Temperatures," *IEEE Transactions on Electron Devices*, Vol. 41, No. 8, August 1994, pp. 1364-1372.

[24]K.F. Schuegraf, C. Hu, "Metal-Oxide-Semiconductor Field-Effect-Transistor Substrate Current during Fowler-Nordheim Tunneling Stress and Silicon-Dioxide Reliability," *Journal of Applied Physics*, Vol. 76, no. 6, September 15, 1994, pp. 3695-3700.

[25]R. Tu, C. Wann, J. King, P.K. Ko, C. Hu, "SOI MOSFET Modeling Using an AC Conductance Technique to Determine Heating," *1994 IEEE International SOI Conference Proceedings*, Nantucket, MA, October 1994, pp. 21-22.

[26]M. Chan, J.C. King, P.K. Ko, C. Hu, "High Performance Bulk MOSFET Fabricated on SOI Substrate for ESD Protection and Circuit Applications," *1994 IEEE International SOI Conference Proceedings*, Nantucket, MA, October 1994, pp. 61-61.

[27]K. Hui, M. Chan, F. Assaderaghi, C. Hu, P.K. Ko, "Body Self Bias in Fully Depleted and Non-fully Depleted SOI Devices," *1994 IEEE International SOI Conference Proceedings*, Nantucket, MA, October 1994, pp. 65-66.

[28]Z.J. Ma, Z.H. Liu, Y.C. Cheng, P.K. Ko, C. Hu, "New Insight into High-Field Mobility Enhancement of Nitrided-Oxide N-MOSFET's Based on Noise Measurements," *IEEE Transaction on Electron Devices*, Vol. 41, No. 11, November 1994, pp. 2205-2209.

[29]C. Hu, "Ultra-Large-Scale Integration Device Scaling and Reliability," *Journal of Vacuum Science and Technology B12 (6)* Nov/Dec 1994, pp. 3237-3241.

[30]**Invited Paper**, C. Hu, "An Engineering Model of VLSI Gate Oxide Breakdown," *25th IEEE Semiconductor Interface Specialist Conference Abstracts*, San Diego, December 1994, p. 1.

[31]F. Assaderaghi, D. Sinitsky, H. Gaw, J. Bokor, P. Ko, C. Hu, "Saturation Velocity and Velocity Overshoot of Inversion Layer Electronics and Holes," *International Electron Devices Meeting Technical Digest*, San Francisco, December 1994, pp. 479-482.

[32]K. Schuegraf, D. Park, C. Hu, "Reliability of Thin SiO_2 at Direct-Tunneling Voltages," *Interna-*

tional Electron Devices Meeting Technical Digest, San Francisco, December 1994, pp. 609-612.

[33]F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. Ko, C. Hu, "A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation," *International Electron Devices Meeting Technical Digest*, San Francisco, December 1994, pp. 809-812.

[34]F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P.K. Ko, C. Hu, "A Dynamic Threshold Voltage MOSFET (DTMOS) for Very Low Voltage Operations," *IEEE Electron Devices Letters,* Vol. 15, no. 12, December 1994, pp. 510-512.

[35]M. Chan, J.C. King, P.K. Ko, C. Hu, "SOI/Bulk Hybrid Technology on SIMOX Wafers for High Performance Circuits with Good ESD Immunity," *IEEE Electron Device Letters,* Vol. 16, no. 1, January 1995, pp. 11-13.

[36]R.H. Tu, C. Wann, J.C. King, P.K. Ko, C. Hu, "An AC Conductance Technique for Measuring Self-Heating in SOI MOSFET's," *IEEE Electron Device Letters,* Vol. 16, no. 2, February 1995, pp. 67-69.

[37]M. Chan, S.S. Yuen, Z.J. Ma, K.Y. Hui, P.K. Ko, C. Hu, "ESD Reliability and Protection Schemes in SOI CMOS Output Buffers," *IEEE Transactions on Electron Devices,* Vol. 42, no. 10, October 1995, pp. 1816-1821.

[38]M. Chan, B. Yu, Z. J. Ma, C.T. Nguyen, C. Hu, P. K. Ko, "Comparative Study of Fully Depleted and Body-Grounded Non-Fully-Depleted SOI MOSFET's for High Performance Analog and Mixed Signal Circuits," *IEEE Transaction Electron Devices,* Vol. 42, No. 11, Nov. 1995, pp. 1975-1981.

LIST OF PUBLICATIONS UNDER OTHER SPONSORSHIP WHICH ARE RELATED TO WORK UNIT

1. H-J. Wann, P.K. Ko, C. Hu, "A Channel Field Model of SOI MOSFET," *Proc. of Tech. Papers, IEEE Int'l Symp. on VLSI Technology, Systems and Applications*, Taipei, Taiwan, May 12-14, 1993, pp. 133-37.

2. S. Parke, F. Assaderaghi, C. Hu, P.K. Ko, "Nearly-fully-depleted (NFD) 0.15 μm SOI CMOS in a CBiCMpOS Technology," *Proc. of Tech. Papers, IEEE Int'l Symp. on VLSI Technology, Systems and Applications*, Taipei, Taiwan, May 12-14, 1993, pp. 168-172.

3. **Invited Paper**, C. Hu, "Towards ULSI Reliability by Design," *Proc. of the 4th Int'l Symp. on Ultra Large Scale Integration Science and Technology: Electrochemical Society (ECS),* May 1993, Vol. 93-23, pp. 158-162.

4. H. Shin, K. Noguchi, C. Hu, "Modeling Oxide Thickness Dependence of Charging Damage by Plasma Processing," *IEEE Electron Device Letters.*, Vol. 14, No. 11, Nov. 1993, pp. 509-511.

5. W.M. Huang, R. Racanelli, B.Y. Hwang, Z.J. Ma, P.K. Ko, C. Hu, "ULSI-Quality Gate Oxide on Thin-Film-Silicon-on-Insulator," *Tech. Digest, Int'l Electron Device Meeting*, December 1993, pp. 735-738.

6. C. Hu, "Low Voltage CMOS Device Scaling," *Digest of Technical Papers, International Solid-State Circuits Conference*, February 1994, pp. 86-87.

7. **Invited Paper**, C. Hu, "Critical Issues of ULSI Gate Dielectrics," *SRC Topical Conference on ULSI Gate Dielectrics*, Raleigh NC, May 11-12, 1994.

8. C. Hu, "MOSFET Scaling in the Next Decade and Beyond," *Semiconductor International*, June 1994, pp. 105-114.

9. S.B. Kuusinen, C. Hu, "Hot-Carrier Induced Degradation of Critical Paths Modeled by Rule-Based Analysis," *Proceedings of 1995 IEEE Custom Integrated Circuits Conference,* San Jose CA, May 1995, pp. 69-72.

10. H.C. Wann, C. Hu, K. Noda, D. Sinitsky, F. Assaderaghi, J. Bokor, "Channel Doping Engineering of MOSFET with Adaptable Threshold Voltage Using Body Effect for Low Voltage and Low Power Application," *1995 International Symposium on VLSI Technology, Systems, and Applications, Proceedings of Technical Papers,* May 1995, pp. 159-163.

LIST OF TECHNOLOGY TRANSFER SINCE LAST PROPOSAL

A model of thin oxide scaling model was adopted by the Semiconductor Industry Association Roadmap as the basis for projecting future semiconductor technology.

Velocity overshoot model and data were transferred to Intel for calibrating simulator and design of future MOSFET's. We have also calibrated a commercial energy-transfer device simulator by TMA so that the IC industry in general can design future MOSFET with velocity overshoot.

AC hot electron model and thin oxide reliability model are widely used in the development of 0.5μm, 0.35μm, and 0.25μm technologies.

The work on velocity overshoot in inversion layers has been carried out in collaboration with Intel Corp. (H. Gaw).

PROPOSED RESEARCH PROGRAM

Approach

The phenomena we will investigate include the statistical variations of device behaviors due to dopant density fluctuation, mobility and velocity overshoot effects, size dependent gate-induced band-to-band tunneling, single-electron phenomena such as Random Telegraph Noise, quantum phenomena in spatially confined carriers, hot-carrier phenomena, radiation effects, and reliability and speed at low operating voltages below 1V.

We will continue to investigate the transport properties of carriers in the inversion layer using the thick-gate uniform channel field MOS transistor [10]. Using devices with sub-100 nm channel lengths, we will perform an extensive investigation of ballistic transport in inversion layer under uniform field condition. We will measure v-E curves of carriers with different channel lengths over a wide temperature range. The experiment results should provide insights on the basic mechanics of velocity overshoot and ballistic transport, the conditions under which they become significant, and provide parameters for advanced device simulations.

We will investigate the quantization and profile of inversion-layer carriers. The result will determine the performance of thin-gate-oxide transistors. This is because the thickness of the inversion layer will add to the gate insulator thickness.

Our recent results of nitrided thermal oxide in a N_2O environment show that it offers many advantages over pure thermal oxide. Some of its virtues, at thickness of about 5 to 10 nm, are lower trapping rate, higher charge to breakdown, less vulnerability to hot-carrier damage, and higher inversion layer electron mobility at high gate field.

We will investigate whether this nitrided oxide is superior to thermal oxide at 4 nm or thinner for use in sub-0.1μm MOS devices. We will study the physics of direct tunneling in nitrided oxide and compare the results with those obtained in thermal oxide of similar thicknesses. We are particularly interested in the physics of tunneling in small areas ($<0.1\mu m^2$). Possible quantum oscillation of the tunneling current may have significant impact on the operation of nanometer-size MOS devices.

Many device structures have been proposed to achieve very short channel length. These include delta-doped devices, double-gated devices, very-thin SOI devices as well as our own dynamic

threshold MOSFET. We will compare their potentials for providing devices at or below 0.05μm.

Expected Result/Impact

We expect this work unit to be the most productive of silicon nanodevice research programs at universities. It will help to bridge the gap between the traditional silicon IC devices and the illusive future devices. We will systematically and methodically clarify as many outstanding questions as possible and thus, draw a roadmap for the evolution from 0.2μm devices to 0.05 micron devices.

By projecting the scaling limits and performance of silicon MOSFET's, this work unit will not only predict the future for CMOS devices but also provide the benchmark for any new nanodevices to measure up to.

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[8] C. Hu, "MOSFET Scaling in the Next Decade and Beyond," *Semiconductor International*, June 1994, pp. 105-114.

[9] K. Schuegraf, C. Hu, "Effect of Temperature and Defects on Breakdown Lifetime of Thin SiO_2 at Very Low Voltages," *IEEE Transactions on Electron Devices*, Vol. 41, No. 7, July 1994, pp. 1227-1232.

[10]F. Assaderaghi, D. Sinitsky, H. Gaw, J. Bokor, P. Ko, C. Hu, "Saturation Velocity and Velocity Overshoot of Inversion Layer Electronics and Holes," *International Electron Devices Meeting Technical Digest*, San Francisco, December 1994, pp. 479-482.

[11]F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. Ko, C. Hu, "A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation," *International Electron Devices Meeting Technical Digest*, San Francisco, December 1994, pp. 809-812.

UNIVERSITY: UC BEKELEY **LAB: ERL**
JOINT SERVICES ELECTRONICS PROGRAM **RESEARCH UNIT: I-B**
LAST YEAR'S RESEARCH UNIT: I-C

TITLE OF INVESTIGATION: Ultrafast High Field Response in Semiconductors

SENIOR INVESTIGATORS: Jeffrey Bokor **TELEPHONE:** 510-642-4134

JSEP FUNDS (CURRENT):

PI	TITLE	PERIOD	AMOUNT (1994-1997)
JB	Novel Time Resolved Probes of Carrier Dynamics in Semiconductors	6/94-1/97	$284,045

JSEP FUNDS (PROPOSED):

1997-1998	$100,000
1998-1999	$100,000
1999-2000	$100,000

OTHER FUNDING:

PI	TITLE	PERIOD:	AMOUNT:	SPONSOR:
JB	Fabrication of sub-5 nm silicon nano-wires and nano-devices (AAsert)	6/1/95-5/31/98	$150,000	AFOSR
JB	Femtosecond Laser Probing of Non Thermal Electronic Transport	6/1/93-5/31/96	$189,139	AFOSR
JB CH	Advanced Silicon FET Physics and Device Structures	11/1/93-10/31/96	$400,000	AFOSR
JB	Development and Applications of Intense Terahertz Radiation Sources (Pending)	10/1/96-9/30/99	$1,543,070	NSF
JB	Research Network for Lithography at 100nm and Beyond (Pending)	1/97-12/2002	$6,850,000	ARPA/SRC
JB	California Sematech Center of Excellence on Optical Lithography	11/1/95-10/31/96	$875,000	SRC

TOTAL NUMBER OF PROFESSIONALS

CURRENT - FACULTY: 1 @ 2 weeks summer
CURRENT - STUDENT: 2 @ 50% academic year; 100% summer

PROPOSED FACULTY: 1 @ 2 weeks summer
PROPOSED STUDENTS: 2 @ 50% academic year; 100% summer

Ultrafast High Field Response in Semiconductors

FACULTY INVESTIGATOR: JEFFREY BOKOR

SCIENTIFIC OBJECTIVE

The primary goal of this research is to develop a detailed fundamental understanding of the transient response of charge carriers subjected to strong electric fields in semiconductors. Our emphasis will be on Si and GaN, two materials of great technological importance whose high field behavior is not as well understood as is necessary to fully exploit their ultimate device applications. We will continue to develop and utilize novel techniques to measure material parameters related to high-speed carrier dynamics that are difficult or impossible to obtain by existing methods.

STATE-OF-THE-ART

Although a great deal is known about the properties of silicon, high-field and hot carrier effects have not been a focus of attention until relatively recently. One reason is that these effects are difficult to study in silicon. They have been very extensively studied in the III-V compound semiconductors, facilitated by the direct optical band-gap, which makes possible a rich variety of ultrafast optical measurement techniques. Silicon, with its indirect bandgap, is less amenable to such techniques. Another factor is that the primary impact of hot carrier effects in today's silicon devices is in the device reliability area. Reliability is, of course, of great importance to the IC industry, and a great deal of effort has been expended in developing methods for engineering devices for reliability. However, it is the case that very simple, semi-empirical models for the hot carrier physics have proven to be sufficient for this purpose up to now.

Research on MOSFET scaling at Berkeley (JSEP sponsored collaboration between C. Hu, P. K. Ko, and J. Bokor) as well as elsewhere has uncovered the tantalizing prospect of velocity overshoot, a high-field, hot carrier related effect which has the potential to significantly increase the current drive of transistors with channel lengths of 0.1 μm and below. To effectively design devices to fully take advantage of velocity overshoot, detailed understanding of the physics is very clearly needed. It is also likely that as the regime of velocity overshoot is reached, with the inherently non-thermal carrier distributions that give rise to the effect, the models used for hot-carrier related device reliability physics will no longer be applicable either.

For GaN, fairly little is known regarding high field carrier dynamics since it has only relatively recently received intense interest due to breakthroughs that have enabled its application to blue light emitting diodes and diode lasers, as well as high power, and high temperature electronics. Based on its wide bandgap, and recently developed processing flexibility, GaN may have application in the high-speed optoelectronic switching area. This prospect has not yet been explored.

PROGRESS SINCE LAST PROPOSAL

Upgrade of experimental facilities

Several improvements in experimental facilities in our ultrafast laser laboratory were made during this period.

A completely new Ti:sapphire femtosecond laser system including oscillator, and 1 kHz repetition rate regenerative amplifier was procured and installed. The system generates 100 fs pulses with up to 1 mJ of energy per pulse at variable repetition rate up to 1 kHz. The laser center wavelength is at 800 nm. JSEP funding provided partial support for the purchase of this system.

Ultraviolet harmonics of this laser are used for time-resolved photoemission experiments. Third and fourth harmonic generators based on BBO nonlinear crystals were constructed. Care was

taken to maintain the harmonic pulsewidths below 180 fs.

The time-resolved photoemission spectroscopy apparatus was modified to allow scale-up of the data collection system for 1 kHz operation. Additional modifications were made to enable preparation of clean silicon surfaces in the ultrahigh-vacuum (UHV) chamber.

A high power source of single-cycle THz electromagnetic pulses was constructed, based on large-area photoconducting antenna technology [1]. We demonstrated for the first time that such sources could be scaled in pulse repetition rate from 10 Hz rates previously reported to 1 kHz using our system. In contrast to expectations, this source actually exhibits higher efficiency per pulse when operated at 1 kHz (see Fig. 1). We performed a careful parametric study of the characteristics of the source [2].

Time-resolved photoemission experiments

We have succeeded in observing time-resolved pump-probe photoemission experiments on silicon samples. An example photoemission spectrum taken with 800 nm pump radiation and 266 nm probe radiation (third harmonic of the laser) is shown in Fig. 2. We observe an extremely fast (<100 fs) decay of this signal, and believe that it is related to rapid surface charging which then creates a very thin space-charge region at the surface. Previous experiments [3] using 50 ps pulses observed similar behavior and we now see that this phenomena occurs even on the sub-100 fs time scale. Slight differences among the various surfaces we have studied (clean Si(100), Si(111), and poly-Si) indicate that the details of the surface structure do play a role, but do not dominate the dynamics.

Surface adhesion reduction in silicon microstructures using femtosecond laser pulses

Our work on femtosecond laser heating of metals and semiconductors tells us that very high transient electron temperatures can be produced for a few ps. Other workers have shown that these "hot electrons" are capable of inducing desorption of molecules from metal surfaces. Discussions with N. C. Tien, a researcher working in the Berkeley Sensors and Actuators Center (BSAC) on surface micromachined micro-electromechanical systems (MEMS) in silicon suggested a potential practical application of this seemingly esoteric phenomenon.

Silicon MEMS often emply suspended microstructures that have large areas but small gap distances to the underlying substrate. Under certain conditions, these microstructures make contact with and become adhered to the substrate because their restoring force is insufficient to overcome the surface adhesion. This sticking and high static friction is often termed stiction and is a device failure mechanism of major concern in MEMS. A major contributor to stiction appears to be from adsorbed water layers on the structure's surfaces.

In collaboration with Dr. Tien, we demonstrated that 100 fs laser pulses at 800 nm were effective in freeing MEMS structures that had failed due to stiction[4]. The yield of freed structures was observed to be dramatically higher for 100 fs pulses compared to 2.7 ps pulses, for a fixed laser pulse energy. Since we know that the hot electron temperature induced in the silicon exhibits a strong pulsewidth dependence, we believe that the hot electrons are responsible for the stiction reduction via desorption of the adsorbed water molecules which cause the suspended microstructure to stick to the substrate.

High field carrier transport in silicon and GaAs

In collaboration with Professor C. Hu's group, we have made direct measurements of the saturation velocity and velocity overshoot of silicon inversion layer electrons and holes[5]. These measurements were obtained from DC current-voltage characteristics of specially fabricated FET test structures.

Based on these results, we have used simulations to estimate the field strengths necessary for these effects to lead to nonlinear absorption of THz pulse radiation in doped silicon and silicon inversion layers. Representative results are shown in Fig. 3. These results indicate that using optimal focusing with our existing THz source, we should be able to observe nonlinear absorption, and study it in detail in order to further elucidate the underlying hot electron physics.

Since inversion layers are so thin, and cannot be stacked like multiple quantum wells to build up appreciable optical absorption, the study of silicon inversion layers by THz spectroscopy was uncertain. We have shown that the excellent signal/noise ratio that is achievable using THz spectroscopy techniques is more than adequate to observe absorption by silicon inversion layers [6]. This technique allows us to measure inversion layer mobility prior to the high temperature process steps normally required to form source and drain contacts, which may be of value in evaluating advanced Si/SiO2 interface structures.

Novel Si FET device structure

We have collaborated with C. Hu's group in the invention, characterization and analysis of a novel dynamic-threshold MOSFET that can operate at very low voltage (0.5 V), with high speed and low off-state leakage current [7,8]

List of Publications Citing JSEP Sponsorship

1. E. Budiarto, J. Margolies, S. Jeong, J. Son, and J. Bokor, "High intensity THz pulses at 1 kHz repetition rate," (submitted to IEEE J. Quantum Electron., in press).

2. N. C. Tien, S. Jeong, L. M. Phinney, K. Fushinobu, and J. Bokor, "Surface adhesion reduction in silicon microstructures using femtosecond laser pulses," Appl. Phys. Lett. **68**, 197 (1995).

3. F. Assaderaghi, D. Sinitsky, H. Gaw, J. Bokor, P. K. Ko, and C. Hu, "Saturation velocity and velocity overshoot of inversion layer electrons and holes," International Electron Devices Meeting Technical Digest, San Francisco, December 1994, pp. 479-482.

4. F. Assaderaghi, C. Hu, P. K. Ko, J. Duster, D. Sinitsky, and J. Bokor, "Direct observation of velocity overshoot in silicon inversion layers," TECHCON Extended Abstracts, Sept. 1993, pp. 265-267.

5. J. -H. Son, S. Jeong, and J. Bokor, "Non contact probing of metal-oxide-semiconductor inversion layers: annealing temperature dependence of mobility," (submitted to Appl. Phys. Lett.)

6. F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. Ko, and C. Hu, "A dynamic threshold MOSFET (DTMOS) for ultra-low voltage operation," International Electron Devices Meeting Technical Digest, San Francisco, December 1994, pp. 809-812.

7. F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P. Ko, and C. Hu, "A dynamic threshold MOSFET (DTMOS) for very low voltage operation," IEEE Electron Device Lett. **15**, 510 (1994).

List of Publications Under other Sponsorship Which are Related to Work Unit

"Advanced lithography for ULSI," J. Bokor, A. R. Neureuther, and W. G. Oldham, IEEE Circ.and Dev. **12,** 11 (1996).

"At-wavelength testing of optics for EUV," K. A. Goldberg, R. Beguiristain, J. Bokor, H. Medecki, K Jackson, D. T. Attwood, G. E. Sommargren, J. P. Spallas, And R. Hostetler, Proceedings of the SPIE **2437**, 347 (1995).

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"Ultrashallow p^+n junctions formed by diffusion from a RTCVD-deposited B:Ge layer," B. Park, C. A. King, D. J., Eaglesham, T. W. Sorsch, B. Weir, H. Luftman, J. Bokor, and Y. O. Kim, Proceedings of the SPIE **2091**, 122 (1993).

"Efficient coupling of high-intensity subpicosecond laser pulses into solids," M. Murnane, H. Kapteyn, S. Gordon, J. Bokor, E. Glytsis, and R. Falcone, Appl. Phys. Lett. **62,** 1068 (1993).

"Direct measurement of nonequilibrium electron-energy distributions in subpicosecond laser-heated gold films," W. S. Fann, R. Storz, H. Tom, and J. Bokor, Surface Sci. **283,** 221 (1993).

"High intensity above-threshold ionization of He," U. Mohideen, M. H. Sher, H. W. K. Tom, G. D. Aumiller, O. R. Wood II, R. R. Freeman, J. Bokor and P. H. Bucksbaum, Phys. Rev. Lett. **71,** 509 (1993).

"Undulator radiation for at-wavelength interferometry of optics for extreme-ultraviolet lithography," D. Attwood, G. Sommargren, R. Beguiristain, K. Nguyen, J. Bokor, N. Ceglio, K. Jackson, M. Koike, and J. Underwood, Appl. Opt. **32,** 7022 (1993).

"Soft-x-ray projection lithography experiments using schwarzschild imaging optics," D. A. Tichenor, G. D. Kubiak, M. E. Malinowski, R. H. Stulen, S. J. Haney, K. W. Berger, L. A. Brown, W. C. Sweatt, J. E. Bjorkholm, R. R. Freeman, M. D. Himel, A. A. MacDowell, D. M. Tennant, O. R. Wood II, J. Bokor, T. E. Jewell, W. M. Mansfield, W. K. Waskiewicz, D. L. White, and D. L. Windt, Appl. Opt. **32,** 7068 (1993).

"Soft-x-ray projection imaging using a 1:1 ring-field optic," A. A. MacDowell, J. E. Bjorkholm, K. Early, R. R. Freeman, M. D. Himel, P. P. Mulgrew, L. H. Szeto, D. w. Taylor, D. M. Tennant, O. R. Wood, J. Bokor, L. Eichner, T. E. Jewell, W. K. Waskiewicz, D. L. White, D. L. Windt, R. M Souza, W. T. Silfvast, and F. Zernike, Appl. Opt. **32,** 7072 (1993).

LIST OF TECHNOLOGY TRANSFER

The work on velocity overshoot in inversion layers has been carried out in collaboration with Intel Corp. (H. Gaw).

PROPOSED RESEARCH PROGRAM

Approach

We will continue time-resolved photoemission experiments on silicon. Our goal is to use this technique to follow the evolution of the energy distribution of laser-heated electrons in silicon. In order to accomplish this, we must first eliminate the rapid surface dynamics which apparently mask the dynamics we wish to study. We will modify the surface electronic structure by hydrogen and oxide passivation, and we will also use cesiation to create a negative electron affinity surface, in an effort to suppress the surface effects so that the bulk dynamics become visible.

In collaboration with E. Weber's group we will begin to study GaN using time-resolved photoemission, to see if ultrafast carrier dynamics in that material can be observed using this powerful technique.

We will attempt to draw a more conclusive connection between the reduction of adhesion of silicon microstructures (stiction) with hot electron driven molecular surface desorption. Toward this end, we will use time-of-flight mass spectroscopy to look for desorption of water or other molecular species from femtosecond laser irradiated silicon surfaces.

Our simulations indicate that we are on the threshold of observing nonlinear transmission of THz pulse radiation in Si and GaAs. We will pursue several strategies for scaling the peak focused intensity, including tighter focusing, increasing the source area, and building microfabricated antenna array structures. We will also explore the use of GaN material for use in THz transmitters as well as study the response of doped GaN to high-field THz radiation. Observation of nonlinear transmission will be a clear indication of significant carrier heating, as indicated in Fig. 3. We will try to characterize the hot carrier distribution using several probe techniques, including luminescence spectroscopy, and photoemission spectroscopy. Such measurements can then be compared with simulations, in pursuit of our ultimate goal of validating physically based simulation tools that can then be used in the design of devices.

Expected Results/Impact

As semiconductor technology development becomes increasingly expensive, the physics models used in device design must evolve from a simple capability to fit device characteristics measured from test devices, to a capability to predict the characteristics of devices before they are fabricated. The only way that this can be achieved is for the fundamental underlying physics to be understood in detail, through a combination of development of theoretical models, and simple experiments that verify them. The impact of our work is expected to be found in the increased reliance of technology developers in both the silicon CMOS as well as high-speed III-V semiconductor laser worlds on sophisticated physically based simulation tools that have been validated, at least in part, against our experimental results.

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[2] E. Budiarto, J. Margolies, S. Jeong, J. Son, and J. Bokor, "High intensity THz pulses at 1 kHz repetition rate," (submitted to IEEE J. Quantum Electron.).

[3] Halas Si paper.

[4] N. C. Tien, S. Jeong, L. M. Phinney, K. Fushinobu, and J. Bokor, "Surface adhesion reduction in silicon microstructures using femtosecond laser pulses," Appl. Phys. Lett. 68, 197 (1995).

[5] F. Assaderaghi, D. Sinitsky, H. Gaw, J. Bokor, P. K. Ko, and C. Hu, "Saturation velocity and velocity overshoot of inversion layer electrons and holes," International Electron Devices Meeting Technical Digest, San Francisco, December 1994, pp. 479-482.

[6] J. -H. Son, S. Jeong, and J. Bokor, "Non contact probing of metal-oxide-semiconductor inversion layers: annealing temperature dependence of mobility," (submitted to Appl. Phys. Lett.)

[7] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. Ko, and C. Hu, "A dynamic threshold MOSFET (DTMOS) for ultra-low voltage operation," International Electron Devices Meeting Technical Digest, San Francisco, December 1994, pp. 809-812.

[8] F. Assaderaghi, S. Parke, D. Sinitsky, J. Bokor, P. Ko, and C. Hu, "A dynamic threshold MOSFET (DTMOS) for very low voltage operation," IEEE Electron Device Lett. 15, 510 (1994).

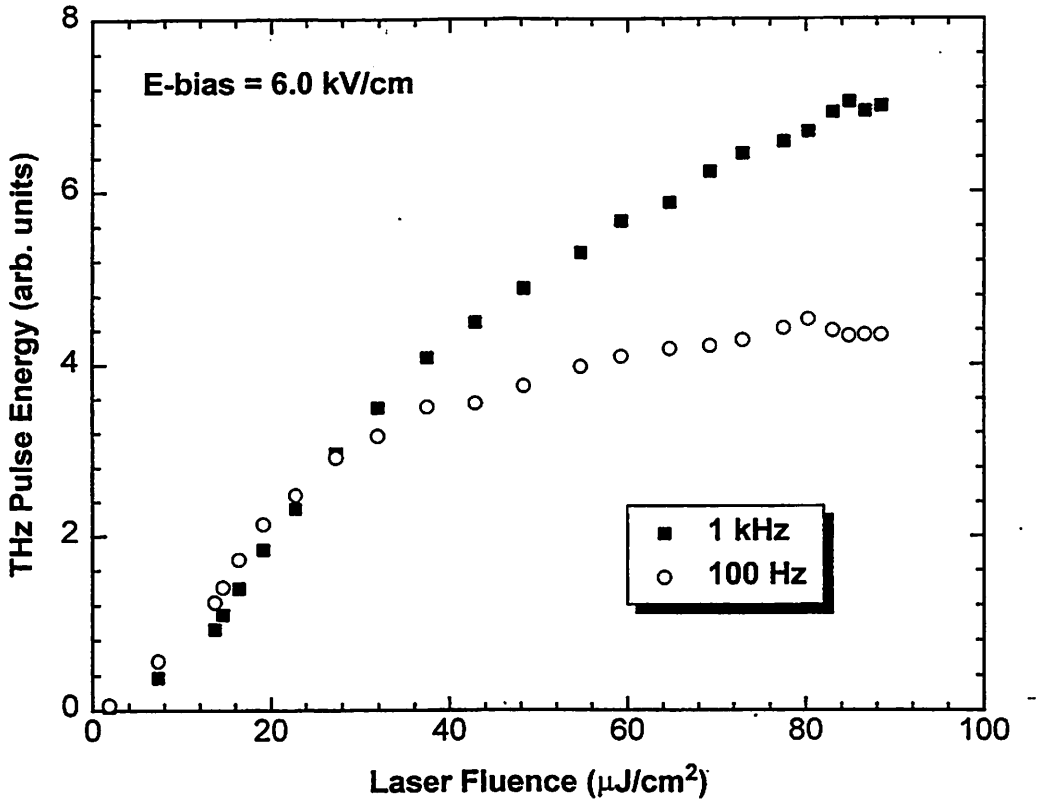
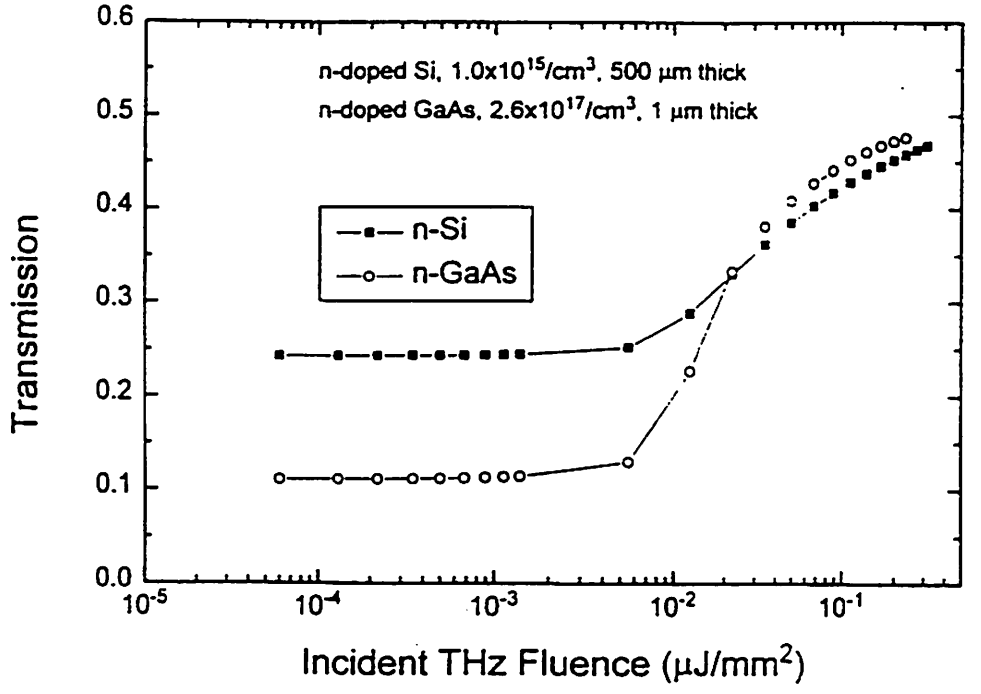


Figure 1. THz output energy vs. laser fluence at 6.0 kV/cm bias field. The THz output pulse energy at 1 kHz repetition rate is 60% greater than that obtained at 100 Hz or 10 Hz repetition rate.



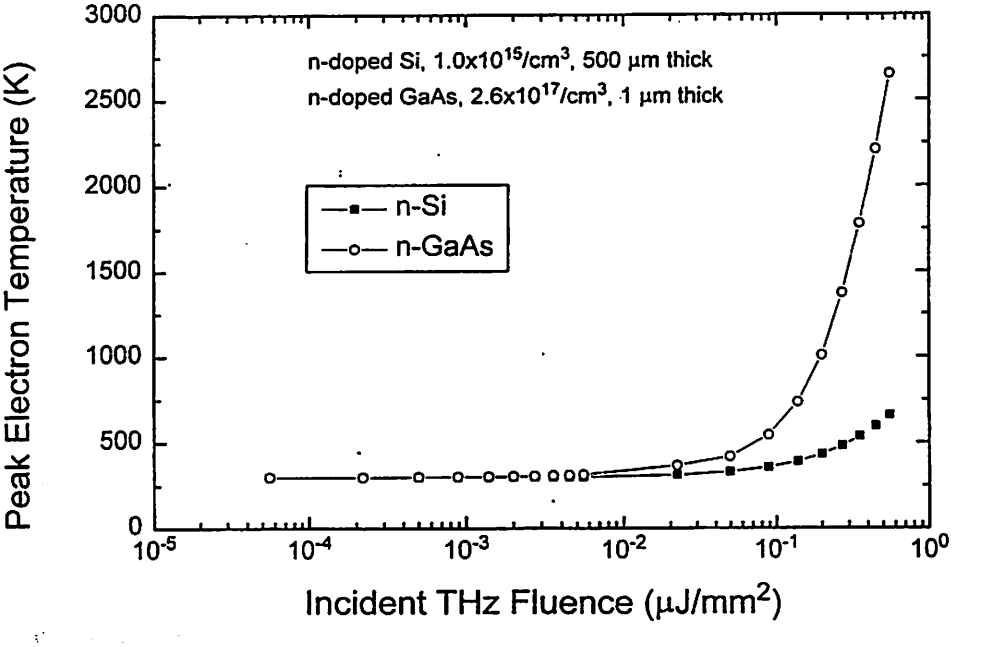


Figure 2. (a) THz absorption saturation in Si and GaAs calculated using an energy balance approach. The onset of absorption saturation occurs near 0.1 uJ/mm2, corresponding to a peak field strength of about 50 kV/cm. (b) Peak electron temperature obtained from the same calculation used for (a). The onset of absorption saturation corresponds to the onset of significant electron heating by the THz field.

UNIVERSITY: UC BEKELEY **LAB: ERL**
JOINT SERVICES ELECTRONICS PROGRAM **RESEARCH UNIT: I-C**
LAST YEAR'S RESEARCH UNIT: I-D

TITLE OF INVESTIGATION: Subsurface Electronic Material Synthesis With Plasma Implantation

SENIOR INVESTIGATORS: Nathan Cheung **TELEPHONE:** 510-642-1615
Chenming Hu 510-642-3393

JSEP FUNDS (CURRENT):

PI	TITLE	PERIOD	AMOUNT (1994-1997)
NC CH	SIMOX Formation by Plasma Immersion Ion Implantation	6/94-1/97	$274,015

JSEP FUNDS (PROPOSED):

1997-1998	$82,000
1998-1999	$82,000
1999-2000	$85,000

OTHER FUNDING:

PI	TITLE	PERIOD:	AMOUNT:	SPONSOR:
NC CH	Circuit Reliability Hot-Electron Model and Simulationl	9/1/95-10/31/96	$169,167	SRC
NC	Plasma Doping Investigation	1/15/96-12/31/96	$60,000	Eaton Corp
NC	Plasma Implantation for the Formulation of Ultra Shallow Junctions	12/15/95-12/30/96	$80,000	Sematech
NC	Plasma Processing Effects (Pending)	7/1/96-6/30/97	$32,000	MICRO

TOTAL NUMBER OF PROFESSIONALS

CURRENT - FACULTY: 2 @ 1 week summer (each)
CURRENT - STUDENT: 1 @ 49.9% academic year; 100% summer

PROPOSED FACULTY: 2 @ 1 week summer (each)
PROPOSED STUDENTS: 1 @ 49.9% academic year; 100% summer

Subsurface Electronic Material Synthesis With Plasma Implantation

FACULTY INVESTIGATORS: NATHAN W. CHEUNG, CHENMING HU

SCIENTIFIC OBJECTIVE

The extremely high dose-rate *plasma immersion ion implantation (PIII)* technique provides a unique opportunity to investigate subsurface synthesis of electronic materials within semiconductor substrates. Nucleation and growth mechanisms of material are expected to be different from surface deposition methods since the buried nuclei are bounded by both the top and bottom substrate interfaces. The first material system we propose to study is the Silicon-on-insulator structure where we will use both oxygen and nitrogen to formed buried dielectrics. The second material system is the formation of buried dielectrics and SiC with implantation of hydrides (e.g., H_2O, NH_3, and CH_4). We expect the synergism between hydrogen and the major implant species will lead to phase formation mechanisms which have not been reported in the literature. The third material structure is the controllable formation of buried microcavities inside Si using hydrogen and helium implantation. The motivations for this microcavity engineering technique are for bonded wafer SOI structures using the Smart-Cut approach and the formation of light-emitting porous Si.

STATE-OF-THE-ART

Silicon-on- Insulator (SOI) technology is attractive for near-term low voltage, low-power applications because the devices scale well with low threshold voltages. In addition to low voltage, SOI reduces power consumption by eliminating source-drain junction capacitance and reduces interconnect capacitance through more compact layout. Device isolation, shallow junction, latch-up, radiation hardness and other considerations have also indicated SOI may be the main stream CMOS technology for 0.15 mm generation and beyond [1,2]. Although 1-Mb SRAM and 256-Mb DRAM have been successfully produced and long-term device reliability demonstrated, high volume use of and serious commitment to SOI are unlikely until the IC manufacturers are shown a SIMOX wafer manufacturing concept that will make true low-cost SIMOX wafers available. The high cost of SIMOX is due to the high dose of oxygen implantation (~$10^{18}cm^{-2}$) required and the high amortization cost of the implanter.

Plasma immersion ion implantation (PIII), a technique pioneered at UC Berkeley for electronic materials synthesis, provides a breakthrough opportunity for economical SIMOX production [3]. With the PIII technique, ions are extracted directly from a plasma environment (in which the target is located) and accelerated through a high voltage sheath into the target. It was previously believed that a DC operation mode is not possible because of arcing but we have identified the proper plasma conditions to alleviate the gas breakdown problem. The DC operation mode (Child-Langmuir regime) has the highest effective implantation flux.

PROGRESS SINCE LAST MAJOR PROPOSAL:

In the past two years, our main achievements have been the demonstration of the feasibility of making SIMOX by the Plasma Immersion Ion Implantation (PIII) technique using an oxygen plasma. In the process, we also found an innovative method for making double SIMOX which could have many novel application in device structures as well as in microsensors. We also succeeded in obtaining a water-vapor plasma, which could be an alternate oxygen plasma source for making SIMOX. We have already demonstrated the formation of SOI structure using water implantation and observed rapid oxygen diffusion in the presence of high hydrogen concentrations. Initial results also show the feasibility of forming well-defined cleavage planes using he implantation which will be useful for bonded wafer SOI structures. We have upgraded the plasma implanter and annealing furnaces - a dedicated annealing furnace was built for the purpose of

annealing the SIMOX wafers (up to 1300 degrees C), a new power supply with higher voltage and current capabilities (100KV, 1A) was installed, and a mass spectrometer was set up to monitor plasma ionic species Lead panels were installed around the implantation chamber for X-ray shielding.

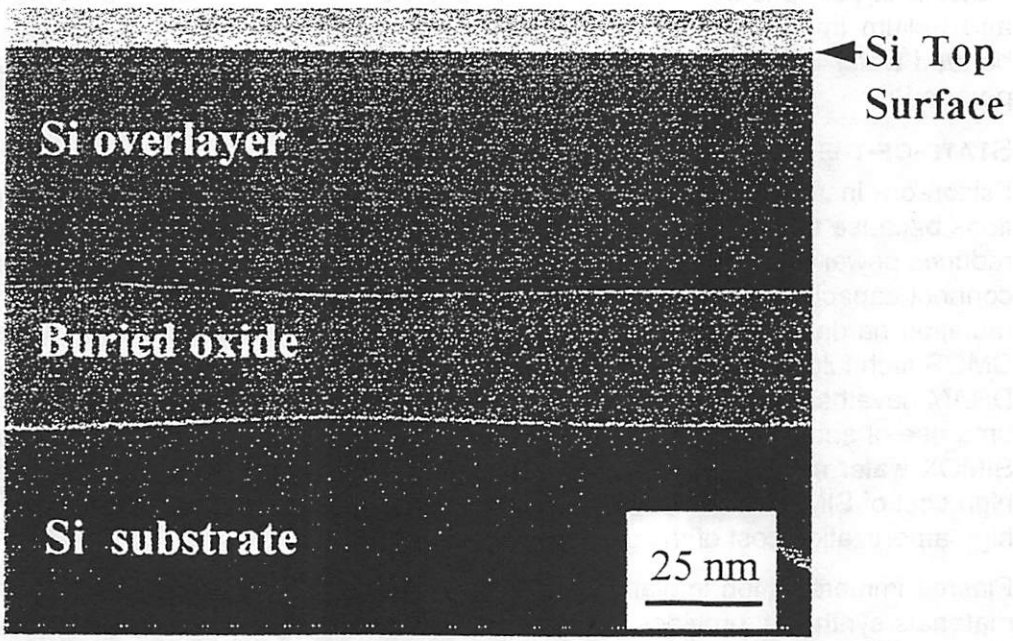


Figure 1. XTEM micrograph of SIMOX structure formed by plasma implantation. The acceleration voltage is 60kV and the oxygen dose is about 3 x $10^{17}/cm^2$. The sample was annealed at 1300 degrees C for 2 hours after implantation.

Our innovation for high throughput SIMOX synthesis is based on a combination of the following key ideas:

1) SIMOX synthesis depends on a **peaked** oxygen implantation profile and sharp Si/SiO_2 interfaces formed during the high temperature post-implantation annealing. To make the concentra-

tion of implanted oxygen exhibit a clear peak at the desired depth from the surface, either (a) a single ionic species in the oxygen plasma is maximized, or (b) oxygen hydride (i.e., H_2O) is used as the plasma gas.

2) PIII can operate in the DC bias mode at voltages exceeding 70kV provided the plasma pressure is below 0.1mTorr. The DC operation mode can provide an implantation dose rate as high as $10^{16}/cm^2/$ sec. Since the plasma is collisionless at these low pressures, nearly monoenergetic energy distribution for each ion species can be achieved.

3) Efficient ionization plasma source (e.g., electron cyclotron resonance, helicon, or transformer coupled plasma) have to be used for the low pressure excitation of ions. The relative abundance of ion species can be tuned by optimizing the plasma pressure, gas composition, and plasma source excitation power to favor one dominant charge state.

4) ***The implantation time*** with PIII for producing SIMOX is ***independent of wafer diameter*** because the entire wafer receives ion implantation simultaneously. Whole wafer implantation from the plasma ion source and the elimination of mass spectrometer lead to over 100 times improvement in throughput and reduction of the equipment cost respectively. The advantage is substantial as production trend is towards larger diameter wafers (> 200mm).

Using this Separation by Plasma Implantation of Oxygen (SPIMOX) technique, we have recently achieved a breakthrough in high-dose rate SIMOX synthesis using an oxygen plasma[4,5]. We succeeded in maintaining high voltages (>70kV) across the plasma sheath by using extremely low gas pressure (<0.1 mTorr) but efficient ionization plasma sources (ECR). An oxygen dose of $3 \times 10^{17}/cm^2$ is accomplished within 3 minutes as compared to hours when using conventional ion implantation. By implanting with a DC bias of >50kV to the substrate, an oxygen plasma excited by ECR source in the low sub-mTorr pressure range, and post-implantation annealing at 1300 degrees C for 2 hours, a continuous buried SiO_2 layer is formed underneath a single-crystalline silicon overlayer of about 30nm [Figure 1]. This breakthrough leads to a patent disclosure[6] and a paper presented at the IEEE SOI Conference in 1995 won the second best paper award [7].

LIST OF PUBLICATIONS CITING JSEP SPONSORSHIP SINCE LAST PROPOSAL

1. N.W. Cheung, "Plasma Immersion Ion Implantation," Transactions of the Materials Research Society of Japan, Vol. 17, pp.543-548 (1994). [invited paper]

2. J.B. Liu, S.S.K. Iyer, J. Min, P. Chu, R. Gronsky, C. Hu, and N.W. Cheung, "Formation of Silicon on Insulator with Separation by Plasma Implantation of Oxygen (SPIMOX)", Materials Research Society Proceedings, Vol. 354,1994.

3. X. Lu and N.W. Cheung, *Solid Phase Epitaxy of Implanted Si-Ge-C Alloys,* Materials Research Society Proceedings, Vol.388,(1995).

4. J.B. Liu, S.S. Iyer, R. Gronsky, C. Hu, N.W. Cheung, J. Min, P.K. Chu, "Formation of Buried Oxide in Silicon Using Separation by Plasma Implantation of Oxygen," Appl. Phys. Lett., Vol. 67, pp. 2361-2363 (1995).

5. J.B. Liu, S.S. Iyer, R. Gronsky, C. Hu, N.W. Cheung, J. Min, P.K. Chu, "Competitive Oxidation Process of Buried Oxide Formation Using Separation by Plasma Implantation of Oxygen (SPIMOX)", Materials Research Society Proceedings, Vol. 388 (1995)

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10. J.B. Liu, S.S.K. Iyer, N.W. Cheung, J. Min, P.K. Chu, "Nucleation Mechanism of SPIMOX (Separation by Plasma Implantation of Oxygen)", to be published in Surface and Coating Technology, 1996.

LIST OF PUBLICATIONS UNDER OTHER SPONSORSHIP RELATED TO WORK UNIT

1. Seongil Im, Jack Washburn, Ronald Gronsky, Nathan W. Cheung, Kin Man Yu, and Joel W. Ager, "Reducing Dislocation Density by Sequential Implantation of Ge and C in Si", Materials Research Society Proceedings, Vol. 298, 139(1993)

2. Seongil Im, Jack Washburn, Ronald Gronsky, Nathan W. Cheung, Kin Man Yu, and Joel W. Ager, "Optimization of Ge/C ratio for compensation of misfit strain in solid phase growth of SiGe layers," Appl. Phys. Lett., Vol. 63, pp.2682-2684 (1993).

3. Seongil Im, Jack Washburn, Ronald Gronsky, Nathan W. Cheung, and Kin Man Yu, "Defect Control During Solid Phase Epitaxial Growth of SiGe Alloy Layers", Appl. Phys. Lett., Vol. 63, pp. 929-931 (1993). Ashawant Gupta, M. Mahmudur Rahman, Jianmin Qiao, Cary Y.Yang, Seongil Im, Nathan W. Cheung, and Paul K.L. Yu, "Donor Complex Formation due to High-Dose Ge Implant into Si," J. Appl. Phys., Vol. 75, No. 8, pp. 4252-4254 (1994).

LIST OF TECHNOLOGY TRANSFER SINCE LAST PROPOSAL

Six graduate research students and two visiting scientists are involved with the PIII program. One student, Jingbao Liu obtained his doctoral degree in the SIMOX project in 1995. We have established collaboration with both semiconductor manufacturers such as Intel Corporation and Advanced Micro Devices, and equipment vendors such as Eaton Corporation and Lam Research Corporation.

PROPOSED RESEARCH PROGRAM

Approach

Ion implantation is not constrained by thermal equilibrium and, thus, implanted concentrations greater than the solid solubility and novel concentration depth profiles can be achieved by the appropriate choice of ion energy and dose.

(A) SIMOX Synthesis

In the case of buried dielectric (e.g. SIMOX) formation, the high substrate temperature ensures that dynamic annealing occurs, which is necessary to retain the integrity of the single crystal silicon overlayer. Once the peak concentration of the implanted oxygen profile exceeds the oxide nucleation value (~$10^{22}/cm^3$) subsequent annealing between 1200 to 1350 degrees C creates a net transport of oxygen towards the buried oxide, against the oxygen concentration gradient. This process ceases when all the oxygen in the "wings" of the implanted oxygen distribution is consumed by the growth of an abrupt buried oxide /Si interface. This SiO_2/Si system will provide a wealth of information on mechanisms for internal oxidation, precipitate gettering and dissolution, and surface interfacial morphology development.

In recent work on thin SIMOX formation (e.g., dose < 3 x10^{17}/cm^2), excellent planar insulator/Si interface morphology using both oxygen and nitrogen implantations have been obtained. It was observed that the oxygen migrated and was gettered by nuclei of silicon nitride during annealing to form a continuous buried oxynitride layer. The preparation of nitrided SIMOX (i.e., SIMON) by PIII is much easier than by conventional ion implantation, because either N_2 or NH_3 can be used as the feedstock gas. SIMON combines the advantages of both SIMOX and buried nitride. A buried oxynitride layer may also present better radiation hardness performance than a pure SIMOX layer. In addition, usually the annealing temperature is at 1200 degrees C, lower than the SIMOX annealing temperature. Nucleation and growth of this buried ternary material system will add to a better understanding of subsurface material synthesis. We expect variations of the technique to form buried oxynitride (SIMON), oxygen-doped Si epitaxial film (OXSEF), and buried semiconductor heterojunctions (e.g., Si/SiC/Si and Si/silicide/Si) will yield other exciting results.

For thin SIMOX formation, quality of the overlying Si strongly depends on the annealing thermal cycle and annealing ambient. Si inclusion inside the buried oxide also has to be eliminated for better reliability of MOS channels and oxide charge trapping. We will investigate the Sequential Implantation and Anneal (SIA) method to obtain defect-free SIMOX. Two or three SIA steps will be employed with the aim to dissolve oxide precipitates in the overlayer before they become so numerous that the passage of interstitial Si to the surface is impeded. The total SIMOX dose will be performed in several steps with annealing at 1300 degrees C between the implantations. Each annealing step will release strain created by the Si interstitial. We anticipate this approach will eliminate dislocation nucleation.

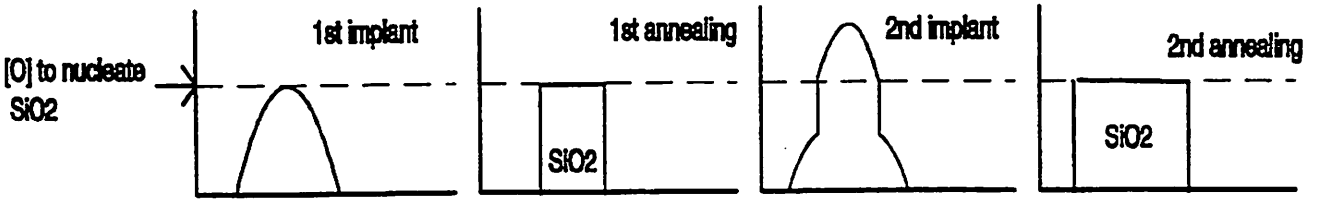

Figure 2. Sequential Implantation and Anneal (SIA) for defect-free SIMOX

Trace element contamination either from the plasma source or chamber walls has to be avoided. Thus, hot-filament plasma sources cannot be used. We opt for cathodeless plasma source designs such as ECR or TCP. We will eliminate the unwanted ion species in the plasma by the use of quartz liners for the PIII chamber and the use of quartz holders completely surrounding the silicon wafer. All exposed surfaces to the plasma will contain only silicon and oxygen. We propose the following design for contamination control and wafer heating.

(B) Hydride Implantation for SOI Structures

We also propose another approach for SPIMOX using a H_2O plasma which consists of H_2O^+,OH^+ and O^+ ions. Since the kinetic energies carried by the oxygen atoms in these species differ only by a slight amount, a single oxygen peak is formed in the total oxygen concentration profile (Figure 3). In this work, we will minimize low energy ion components by using low gas pressure (<1mTorr) to avoid ion scattering in the ion sheath during substrate bias. The implantation of hydrogen in Si is not important since hydrogen will diffuse rapidly towards the Si surface at the implantation temperature of >600 degrees C.

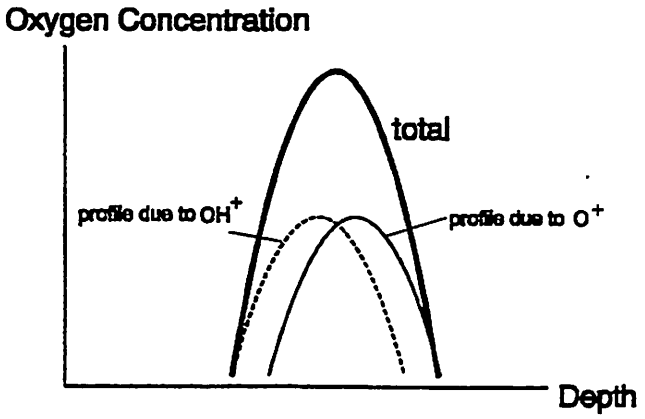

Figure 3. Oxygen profile in Si due to approximately equal implantation dose of O^+ (mass =16) and OH^+ (mass =17) ions. The resultant oxygen profile still has a single maximum due of the slight kinetic energy difference carried by the oxygen atoms.

Initial work has shown it is feasible to form SOI structures using water plasma implantation, demonstrating validity of the concept. Figure 4 shows the XTEM micrograph of the SOI structure formed with 60 kV implantation and with an oxygen dose of $4 \times 10^{17}/cm^2$. SIMS profiling showed that the as-implanted oxygen profile has significantly broader than the theoretical value, indicating hydrogen enhanced oxygen diffusion during the implantation process. We will investigate this new diffusion mechanism in detail in our studies. We also propose to synthesize buried SiC layers inside Si analogous to SIMOX. The difference is that here we will have heterojunctions formed because SiC is a wide bandgap semiconductor. Buried SiC can be formed by methane (CH_4) or acetylene (C_2H_2) plasma implantation. PIII of hydrides creates a single peaked implantation profile even without mass separation because all XH_n molecular species have mass very close to pure X. For the carbide synthesis work, the lower C diffusivity in Si probably will require a higher implantation temperature (>700 degrees C) and diffusion temperature (>1300 degrees C) to enhance the Ostwald ripening mechanism. Various Si substrate orientations (e.g., <100> and <111>) will be used to form buried SiC to verify the concept that different interfacial strain can preferentially nucleate particular polytypes of SiC.

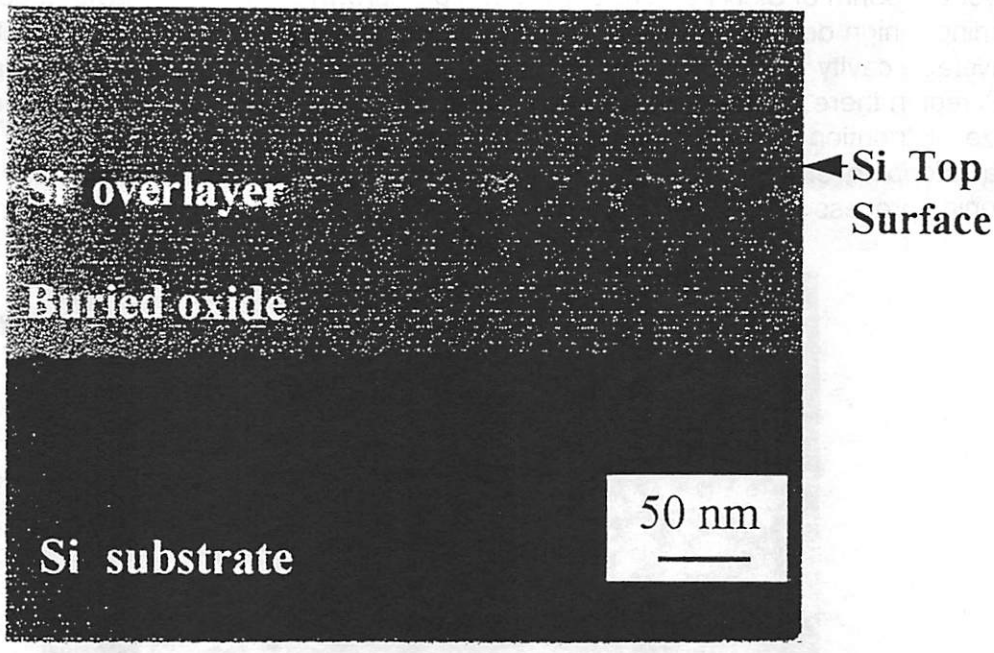

Figure 4. XTEM micrograph of SOI structure formed by water plasma implantation after annealing at 1250 degrees C for 2 hours. The water plasma contains more than 95% H_2O+ and the implanted oxygen dose is about 4 x $10^{17}/cm^2$.

(C) Microcavity Engineering

Buried microcavities have been formed in Si by conventional He ion implantation by several laboratories for investigation of impurity gettering [8]., internal surface science studies [9], and nanocrystalline optical properties [10]. Recently it was reported by Raineri et al [11], that it is possible to produce buried oxide layers in Si by He implantation to produce microcavities, followed by trench etching and an oxidation step. Since the dose requirement for these applications is on the order of 10^{17} atoms/cm2, the plasma immersion ion implantation technique is well suited for this purpose.

We have performed preliminary experiments to form these buried microcavity layers. A nominal dose of $2x10^{17}/cm^2$ was used for He implantations. We have also demonstrated we can control the nulcleation depths of the buried microcavities using dual implantation of He and oxygen. Two sets of samples were prepared in this study: (1) 34kV He-implanted Si and (2) 10kV He-implanted and subsequently 33keV oxygen implanted Si. Samples were observed by cross-sectional transmission electron microscopy (XTEM) both after implantation and after annealing. Due to the high ion fluxes used, the substrate temperature was around 200 degrees C for the He implants, but around 600 degrees C for the oxygen implants. After implantation, the Si wafer surface was capped by a Si_3N_4 layer (about 155nm) deposited by PECVD. Post-implantation annealing was carried out in an oxygen ambient for 30 minutes followed by nitrogen for 10 minutes.

Figure 5 shows XTEM micrographs of a $2x10^{17}/cm^2$ He-implanted sample before and after annealing at 1050 degrees C for 30 minutes. Before annealing, no bubbles are visible. Since XTEM microscopy can generally not resolve bubbles smaller than 1-2 nm, that sets an upper limit on the bubble size, if any are present in the damaged Si layer. After the anneal (Fig.5), under the

top layer of 155nm of Si3N4 and about 170 nm of regrown Si, there is a layer about 230 nm thick containing a high density of cavities. There is an increasing average cavity diameter with depth. The average cavity diameter in the deeper region is about 50 nm. Near the boundary with the poly-Si region there are many small bubbles with diameter from 5 nm to 12 nm. We find the bubble size distribution agrees well with the as-implanted He depth profile, rather than with the nuclear stopping energy deposition. The higher concentration band there may have been a coarsening process as small bubbles coalesced into larger ones during annealing.

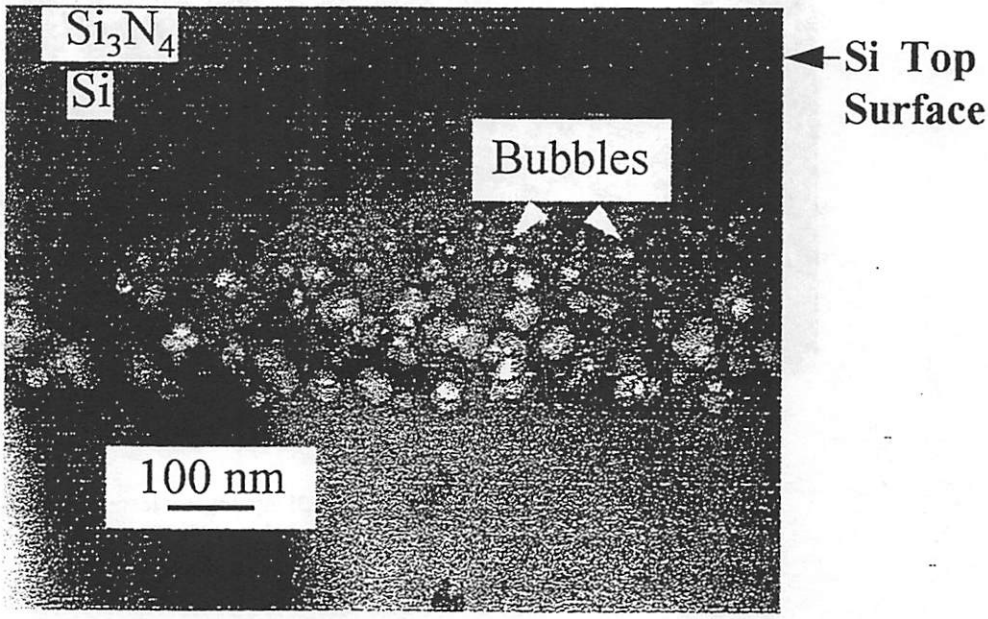

Figure 5. XTEM micrograph of buried microcavities formed by He plasma implantation.

As an application of microcavity engineering, we have used the microcavity band to control buried oxide formation. Si was implanted with $2x10^{17}/cm^2$ He at 10kV and subsequently $2x10^{17}/cm^2$ oxygen at 33kV. The projected range is about 115nm for He at 10kV and 82nm for oxygen at 33kV according to TRIM simulations. XTEM results show that we have been able to shift the band of bubbles to the shallower projected range of the oxygen implant.

With initial success to control the microcavity nucleation process, we propose to investigate using PIII as a microcavity engineering tool. The goals are to form (i) a well-defined cleavage plane for the Smart-Cut process for SOI wafers [12] and (ii) the formation of porous Si with controlled distribution of internal surfaces. The control parameters used in this study are: the implantation dose rate, the substrate temperature, and the post-implantation thermal annealing cycle. We will also use dual-specie (e.g., H and He) and also multiple implantation steps to control the size distributions of these microcavities. The bonded SOI technique will be used to study internal fracture mechanisms. For the porous Si studies, we will use the bubble sizes to vary quantum confinement effects. Photoluminescence will be used to evaluate the photo-emission properties. We believe this method will give cleaner internal surfaces than the aqueous etching method which will provide more information on the photoemission properties of quantum structures.

(D) Material and Device Characterization

Our extremely high dose-rate implantation technique can lead to metastable phase formation in

the as-implanted state. We will investigate such possibilities by studying the kinetics of oxide precipitation and growth and their interaction with defect nucleation by transmission electron microscopy and Rutherford Backscattering Spectrometry (RBS).

For electrical testing of the SPIMOX material produced in this project we propose to fabricate and investigate MOS capacitors and MOSFET's. MOS capacitors with 3 to 20nm thick thermal oxide and polysilicon gates will be studied. Active metal impurities or defects in the Si film, if present will reduce the capacitance recovery time in C-t test or the Zerbst plot. The energy levels and time constants of the traps can be studied with DLTS.

Excessive interface trap density (measured by quasi-static CV test) is also an indication of impurity or defects. Impurities incorporated into the thermal oxide may be detected as charge traps or through excess oxide current due to resonant tunneling. This may be particularly obvious in very thin oxides, e.g., 4nm oxide, and low voltage (<3V) in the direct tunneling regime of oxide current transport.

We are capable of making channel lengths as small as 0.1μm and gate oxide as thin as 30 A°. We have set the world speed record for ring oscillators using conventional SIMOX wafers and have extensive experience comparing SIMOX, bulk and BESOI materials in terms of device performance and reliability. These capabilities will be brought to make SPIMOX a truly transferable SIMOX technology.

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UNIVERSITY: UC BEKELEY **LAB: ERL**
JOINT SERVICES ELECTRONICS PROGRAM **RESEARCH UNIT: I-D**
LAST YEAR'S RESEARCH UNIT: I-A

TITLE OF INVESTIGATION: Wavelength Translation Via Four-Wave Mixing in Resonantly Enhanced Well Laser Diodes

SENIOR INVESTIGATORS: Kam Lau **TELEPHONE:**510-642-6251

JSEP FUNDS (CURRENT):

PI	TITLE	PERIOD	AMOUNT (1994-1997)
KL	Fundamental Studies of Ultrafast Dynamics and Their Impact on High Speed Modulation in Quantum Well Lasers	6/94-9/97	$276,988

JSEP FUNDS (PROPOSED):

1997-1998	$100,000
1998-1999	$100,000
1999-2000	$100,000

OTHER FUNDING:

PI	TITLE	PERIOD:	AMOUNT:	SPONSOR:
KL	Device and System Research in Millimeter Wave Fiber Optic Links and Distributed Antenna Networks for Cellular and Personal Communications	6/15/95-5/15/98	$650,000	AF
KL	An All-Optical Frequency Translator Crossbar Switch System	3/6/95-3/5/98	$169,000	Hughes Research Lab
KL CCH	Very High Frequency Mode-Stabilized VCSELs for Linear/RF Photonic Applications (Pending)	3/1/96-2/28/99	$900,00	ONR

TOTAL NUMBER OF PROFESSIONALS

CURRENT - FACULTY: 1 @ 1 week summer
CURRENT - STUDENT: 1 @ 49.9% academic year; 100% summer

PROPOSED FACULTY: 1 @ 1 week summer
PROPOSED STUDENTS: 2 @ 49.9% academic year; 100% summer

Wavelength Translation Via Four-Wave Mixing in Resonantly Enhanced Quantum Well Laser Diodes

FACULTY INVESTIGATOR: KAM Y. LAU

SCIENTIFIC OBJECTIVE

This proposal involves fundamental studies of four-wave mixing via ultrafast carrier dynamics in high speed quantum well laser devices, with the objective of performing the function of all-optical conversion of optical data between multiple carrier wavelengths. The wavelength converter is designed for use in a standard wavelength division multiplexed (WDM) system, with channels spaced by roughly 1nm over the 30nm bandpass width of erbium-doped fiber amplifiers and with a data rate of greater than 10Gbit/sec. The converter is designed to be transparent to data modulation format and should have an efficiency of better than -10dB in order to be useful. Since WDM systems use evenly spaced, discrete carrier wavelengths, continuously tunable wavelength conversion is not necessary; the proposed device is step-tunable between the carrier wavelengths.

Since conventional four-wave mixing effects in laser amplifiers suffer a high conversion loss and a high noise figure at large conversion ranges (over 10nm), we will study a wavelength conversion device using cavity-enhanced four-wave-mixing (FWM) in a semiconductor Fabry-Perot laser. The test laser is injection-locked into a single mode, which serves as the FWM pump, and the probe signal is injected at a frequency Δf from the pump. The signal is then impressed on the FWM conjugate wave at a frequency - Δf from the pump frequency, resulting in an effective conversion of the carrier frequency by -2 Δf. This is a potentially useful method of wavelength conversion over a discrete comb of wavelengths spaced at the modal separation of the test laser. In addition to fundamental studies of carrier dynamics responsible for the four-wave mixing process, we also plan to perform measurements and analysis of noise, distortion, and other parameters relevant to transmission of information using such a wavelength conversion device.

STATE-OF-THE-ART

Wavelength conversion devices are proposed as a key component of all-optical WDM networks. It is well recognized that the number of wavelengths to be used in WDM is going to be limited by the ability to generate and control these wavelengths, and therefore some form of wavelength reuse is inevitable. Thus it may be necessary for a data packet launched into an all-optical WDM network to switch its wavelength during its traversal through different parts of the network before it reaches its destination, so as to avoid conflict with other packets that are launched locally which happens to have the same wavelength. Furthermore, it is sometimes necessary to "block-translate" many WDM channels simultaneously. Although wavelength conversion devices using gain or absorption saturation effects achieve high conversion efficiencies, these devices are not transparent to data modulation format, and the information bandwidth is typically limited by the carrier lifetime. Wavelength conversion devices based on four-wave mixing are transparent to modulation format, but the efficiency of such devices is a recurrent problem. Vahala, et al have demonstrated four-wave mixing in travelling wave amplifiers for pump-probe detunings of up to 3THz; the efficiency with which the resulting frequency-shifted signal is generated is extremely poor (<-40dB) for frequency detunings exceeding the inverse carrier lifetime over several orders of magnitude[1].

The proposed device uses resonant enhanced four-wave mixing in a semiconductor laser to perform step wavelength conversion. The laser is injection-locked into a single dominant lasing

mode at f_1. The input carrier signal at f_2 is injected into the laser cavity and beats with the lasing mode at f_1, thereby shifting the data to a third signal arising at $f_3=2f_1-f_2$ due to the $\chi(3)$ material optical nonlinearity. Dageneis, et al have demonstrated a resonant-enhanced peak in the efficiency of four-wave mixing signal generation in semiconductor lasers; when the pump-probe detuning $\Delta f = |f_1 - f_2|$ matches the cavity round trip frequency, a 60dB enhancement of the efficiency is measured [2]. Murata, et al use this resonant enhanced four-wave mixing technique to demonstrate up-conversion of a 1Gbit/sec signal over 1THz with an efficiency of -1dB [3]. In the proposed wavelength conversion device, the cavity length of the test laser is selected so that the inverse cavity round trip time matches the carrier wavelength spacing of the WDM system in which the converter is to be applied; thus, any two potential carrier wavelengths are separated by an integer multiple of the device resonance frequency. Given an input at carrier wavelength f_2 and a desired output carrier wavelength at f_3, the laser is injection-locked into the appropriate mode at $f_1=(f_2+f_3)/2$ in order to shift the input data to the generated carrier at f_3 via resonant-enhanced four-wave mixing.

Although resonantly enhanced four-wave mixing has been demonstrated, the conversion efficiency, noise and distortion characteristics of these devices relate to fundamental carrier dynamics of the laser gain medium, in this case a quantum well, and is currently not well understood. By using results we obtained in the previous JSEP program in which ultrafast dynamics of carrier transport, carrier heating and spectral hole-burning have been delineated and studied in detail using novel spectrally and time-resolved measurement techniques, we anticipate a new level of understanding as to how the fundamental performance of a wavelength translator relates to device design.

PROGRESS SINCE LAST MAJOR PROPOSAL

We have demonstrated a novel measurement technique for determining the contribution of carrier transport effect on the highest modulation bandwidth in quantum well lasers. This technique independently measures the ratio of the effective carrier-capture to escape times, as well as contribution from the intraband damping mechanisms, in an *operating laser*. Every single parameter in the present model for modulation dynamics of quantum well lasers can now be determined experimentally, which enables a consistency check on its validity.

It is currently understood that the highest modulation bandwidth of quantum well (QW) lasers should have is limited by several damping mechanisms: (1) intraband damping mechanisms, including spectral hole-burning and carrier heating, which are collectively represented by a "gain-compression" parameter in the common rate-equation analysis of laser dynamics; (2) carrier diffusion in the barrier regions and quantum capture into the QW's, collectively known as "transport" effects. The maximum 3dB bandwidth is inversely proportional to the so-called K factor, with K given by:

$$\frac{K}{4\pi^2} = \tau_p + \frac{\varepsilon}{A} + \tau_{cap}^{E}\frac{R^E}{1+R^E} \qquad \text{Eq. (1)}$$

where, τ_p is photon lifetime, R^E is the ratio of τ_{cap}^{E} to τ_{esc}^{E} where the former is the effective carrier capture time (including diffusion) and the latter carrier escape time, ε is the nonlinear gain coefficient representing all the intraband damping mechanisms, and A is differential gain. Except for certain devices with atypical structures, made specifically to accentuate one or more of the above effects for the purpose of illustration, it is difficult to quantify the relative importance of the numerous mechanisms at play in a typical operating QW laser. New measurement techniques have been introduced to independently measure τ_{cap}^{E} but assumptions still need to be made on

the values of other parameters in Eq. (1).

We have succeeded in demonstrating new static and dynamic spontaneous measurements which enable us to independently determine the intraband gain-compression parameter ε, as well as the factor R^E. With these results, every term in Eq. (1) can now be independently known through measurements, not assumptions. For the devices we measured, we found that the measured value of K is indeed consistent with the sum of the three contributing terms in Eq. (1), so that there are no major discrepancies in the current understanding of modulation damping in QW lasers.

To explain our measurement technique, we use the small signal analysis of rate equations to derive the phase φ which is the phase between n_2 and s, where n_2 and s are the small variations of the carrier density in QW and photon density, respectively. The parameter n_2 can be measured by observing the spontaneous emission from the test laser which is collected by an objective lens from the sideward direction, then coupled into a multimode fiber. A pair of gratings is used to spectrally resolve the spontaneous emission from the QW (proportional to n_2) and the scattered laser light (s). The spectrally resolved output is observed on an ultrafast streak camera with a time resolution of 2ps. A synthesizer is used for modulating the test laser and synchronizing the streak camera so that the time-resolved small signal response of n_2 and s can be observed on streak camera under synchroscan mode. From these results, the relative contribution of each term in Eq. (1) can now be evaluated. The values of $K/4\pi^2$, τ_p, and ε/A are 9 ± 1 ps, 2 ps, and 5.8 ps, respectively. Hence, from Eq. (1), the contribution from the carrier transport effect is only about 1.2 ps, and τ_{cap}^{E} can be calculated to be about 60 ps, which is consistent with experimental measurements reported previously as well as theoretically estimated. Furthermore, the threshold carrier density can be calculated to be about 6.7×10^{18} cm^{-3}, consistent with theoretical expectations.

We can further use the spontaneous emission data to determine the carrier temperature in our device, hence determining the extent to which carrier heating contributes to damping. The near-linear "tail" at high energies can be utilized to derive the carrier temperature. It appears that very substantial carrier heating, both for 2D and 3D carriers, occurs in this device, with 2D carriers at approximately 470K and 3D carriers at 420K.

To summarize, we demonstrated a novel spontaneous emission measurement that can resolve the relative importance between the interband and intraband damping in an *operating laser*. With these new measurements, all the parameters in the rate equations can now be determined through experimental measurements. Hence, this is a useful tool for a complete understanding of high speed modulation in quantum well laser.

LIST OF PUBLICATIONS CITING JSEP SPONSORSHIP SINCE LAST PROPOSAL

1. D. Vassilovski, T. C. Wu, S. C. Kan, K. Y. Lau, and C. E. Zah, "Unambiguous determination of quantum capture, carrier diffusion, and intrinsic effects in quantum well laser dynamics using wavelength-selective optical modulation," IEEE Photonics Technology Letters, vol. 7, no. 7, pp. 706-708, 1995.

LIST OF TECHNOLOGY TRANSFER SINCE LAST PROPOSAL

This work was carried out in close collaboration with Dr. C.E. Zah of Bellcore who supplied us with the lasers used in this work. This organization is deeply involved in quantum well laser manufacturing, as well as being the lead organization in one of the ARPA consortiums on all-optical WDM networks. Fundamental understanding of carrier dynamics in quantum well lasers was quite instrumental in development of high performance quantum well laser devices that can operate at high temperature as well as high speed.

PROPOSED RESEARCH PROGRAM

Approach

We plan to build the proposed resonant enhanced four-wave mixing wavelength converter and study its experimental characteristics. Simultaneously, theoretical models will be developed using results obtained in our previous phase of JSEP on ultrafast dynamics of quantum well lasers. The setup is planned to be entirely in fiber, except for the light sources and test laser in which the four-wave mixing is to be performed. The test laser is a quantum well Fabry-Perot laser, with an intermodal spacing of roughly 0.9nm. A New Focus 6248 Tunable Laser centered at 1300nm with narrow linewidth (100kHz) is used to injection-lock the test laser into a single dominant mode; light is coupled into and out of the front facet of the test laser via a microlens etched onto a bare fiber tip. We will first demonstrate injection-locking with this setup for the five central modes of the test laser, with a side-mode suppression ratio of roughly 20dB in each case. A second New Focus 6248 Tunable Laser provides the input tone, and the device response will be observed using an optical spectrum analyzer.

This four-wave mixing device will be used for several experimental purposes, with the ultimate goal of creating a useful wavelength converter. First, we will characterize the resonant peaks of the signal generation efficiency, determining the height and width of both up and down shifted successive resonant peaks, and these experimental measurements will be compared with theoretical derivations in order to better characterize this effect. The width of these peaks is of particular importance since it limits the information bandwidth of the proposed wavelength converter. We will demonstrate conversion of both analog and digital data at the resonant frequencies and characterize the limitations on bit rate, bit error rate, signal amplitude, and magnitude of the frequency shift for this type of device. Finally, we propose to explore the temporal response of the device, determining the turn-on time and characterizing transient effects.

Theoretical treatment will involve modeling the carrier-photon interaction process through a set of rate equations which describes the carrier injection dynamics into the quantum well. Carrier heating mechanism will be taken into account through the power-dependent gain of the quantum well medium, which is computed self-consistently from the Fermi distribution of the carriers at the elevated temperature. Spectral hole-burning will be taken into account by a power-dependent gain in addition to carrier heating. The form of the equations and the numerical values will be extracted from the results of our prior JSEP contract on ultrafast dynamics of quantum well lasers. These carrier equations are then solved self-consistently with optical field equations (the standard Lamb equations), which include more than one longitudinal mode and allow for detuning of the optical signals in order to investigate the bandwidth of the resonantly enhanced conversion. This model should be able to yield all the relevant parameters of the performance of this device as a wavelength translator as mentioned above.

Expected Results/Impact

It is expected that this study will yield a firm understanding of the fundamental performance limitation of a wavelength translation device, with translation efficiency of better than -10dB over a range of 10nm or more, and which has high performances in terms of noise and distortion which makes it an essential component for all-optical WDM networks. We expect to experimentally investigate this device as well as perform a detailed but practical theoretical modeling of the performance of this device, based on fundamental carrier dynamics in quantum wells and their interaction with optical modes in a Fabry-Perot resonator. Advancement in device technology as well as understanding in fundamental ultrafast dynamics in quantum well lasers is anticipated.

REFERENCES

[1] J. Zhou, N. Park, J. Dawson, K. Vahala, M. Newkirk, and B. Miller; "Terrahertz Four-Wave Mix-

ing Spectroscopy For Study Of Ultrafast Dynamics In A Semiconductor Optical Amplifier"; Applied Physics Letters, Vol 63, No 9; 30 August 1993; pp.1179-1181.

[2] S. Jiang and M. Dagenais; "Observation Of Nearly Degenerate And Cavity-Enhanced Highly Nondegenerate Four-Wave Mixing In Semiconductor Lasers"; Applied Physics Letters; Vol 62, No 22; 31 May 1993; pp.2757-2759.

[3] S. Murata, A. Tomita, J. Shimizu, and A. Suzuki; "THz Optical-Frequency Conversion of 1Gb/s-Signals Using Highly Nondegenerate Four-Wave Mixing in an InGaAsP Semiconductor Laser"; IEEE Photonics Technology Letters; Vol 3, No 11; November 1991; pp.1021-1023.

UNIVERSITY: UC BEKELEY **LAB: ERL**
JOINT SERVICES ELECTRONICS PROGRAM **RESEARCH UNIT: I-E**
LAST YEAR'S RESEARCH UNIT: N/A

TITLE OF INVESTIGATION: Single Transverse Mode Vertical Cavity Surface Emitting Laser

SENIOR INVESTIGATORS: Connie Chang-Hasnain **TELEPHONE:**510-642-4315

JSEP FUNDS (CURRENT):

PI	TITLE	PERIOD	AMOUNT (1994-1997)
CH	Single Transverse-Mode Vertical Cavity Surface Emitting Laser	12/95-1/97	$195,704

JSEP FUNDS (PROPOSED):

1997-1998	$100,000
1998-1999	$100,000
1999-2000	$100,000

OTHER FUNDING:

PI	TITLE	PERIOD:	AMOUNT:	SPONSOR:
CH	Presidential Faculty Fellow Award	1/1/96-9/30/97	$124,400	NSF
CH	Systems & Device in all Optical Wavelengh Routed Switching Networks	9/1/93-2/28/97	$152,309*	NSF
CH	Optoelectronic Materials Center	12/20/93-12/19/96	$128,334	University of New Mexico
CH KL	Very High Frequency Mode Stabilized VCSELs for Linear RF Photonic Applications (Pending)	3/1/96-2/28/99	$900,000	ONR
CH	Widely-Tunable Vertical Cavity Surface Emitting Laser Array GaAs Micro-machines (Pending)	1/1/96-12/31/96	611,661	ARO

TOTAL NUMBER OF PROFESSIONALS

CURRENT - FACULTY:	1 @ 1 week summer
CURRENT - STUDENT:	2 @ 49.9% academic; 100% summer
PROPOSED FACULTY:	1 @ 1 week summer
PROPOSED STUDENTS:	2 @ 49.9% academic; 100% summer

Single Transverse Mode Vertical Cavity Surface Emitting Laser

FACULTY INVESTIGATOR: CONNIE J. CHANG-HASNAIN

SCIENTIFIC OBJECTIVE

The vertical cavity surface emitting laser (VCSEL) has emerged as one of the most important laser structures because of its unique topology facilitating wafer-scale processing and testing. The potential for low-cost, large volume production makes them a serious candidate for many applications with many industry-led research and development efforts underway. In spite of much activity in the field, there is very little understanding on many essential laser characteristics such as high frequency modulation, laser linewidth, chirp, noise, etc. Further, the role of the high finesse single wavelength cavity on carrier dynamics and, effective laser modulation response, has never been examined. There is a fundamental basis to expect superior characteristics in these parameters. The lack of all these measurements is due to the lack of single mode VCSEL's.

By single mode, we necessarily mean not only a single transverse and longitudinal mode but also a single, fixed polarization mode. Stable single mode operation mandates a laser to possess a waveguide encompassing its active region to selectively guide a desired mode. Further, either a polarization-selective gain, mirror, or waveguide should be present to warrant a stable single polarization operation. Our recent studies on buried heterostructure (BH) VCSEL and oxide-confined (OC) VCSEL show that both structures can lead to stable single transverse mode operation with fixed polarization. The polarization selectivity is attributed to strain introduced to the gain region breaking its degeneracy. The origin of the strain is not clearly understood and needs further investigation.

In the program, we propose to explore further both buried heterostructure and oxide-confined structures to achieve single mode VCSEL's. We plan to investigate the origin of the polarization selection mechanism and to design new structures to fully exploit this mechanism. We will perform thorough characterization of various operating characteristics of our single mode VCSEL's. In addition, we will examine the effect of Fabry-Perot wavelength detuning on carrier dynamics and modulation response.

STATE-OF-THE-ART

Currently, there are two well-understood VCSEL structures: laser-post-type index-guided laser and proton-implanted gain-guided lasers. Neither of them warrantees VCSEL's with a stable single mode at a reasonable yield. The laser-post-type index-guided VCSEL's typically emit multiple transverse modes due to a large index step between the laser core and air cladding. The gain-guided VCSEL's emit a single fundamental mode within limited current ranges near thresholds. However, they usually exhibit random polarizations.

In order to achieve simultaneous current and optical confinements with stability, it is desirable to fabricate a buried heterostructure (BH) VCSEL to provide a built-in index difference in the transverse direction. However, due to the high Al content in the Bragg reflectors, the regrowth of cladding layers has been one of the major obstacles. The oxide-confined structure, on the other hand, provides excellent current confinement and moderate optical confinement. The most important issue to resolve for this structure is the understanding of the oxide structure, its interface quality and stability under various environmental changes. Under previous JSEP support, we demonstrated the first reported single mode VCSEL's with outstanding characteristics. Details are described in the following.

PROGRESS SINCE LAST MAJOR PROPOSAL

Buried Heterostructure VCSEL

A VCSEL is fundamentally not very different from a regular edge emitting laser and, thus, the structures that can stabilize edge emitting lasers should do the same to VCSEL's. A buried heterostructure (BH) is therefore a natural choice for controlling the transverse modes. A schematic of a BH VCSEL we fabricated is shown in Fig. 1. A BH structure is typically fabricated by etching lasers to form posts, which are the core of the laser waveguides, and then perform a second growth, also known as regrowth, to form a cladding with lattice-matched material having a determined refractive index. To obtain a strong single mode control, stable for high power operation, in laser size which is reasonably large to match to a single mode fiber, we have intentionally used a higher index material for the cladding to form an anti-index guided laser structure. This antiguide provides optical losses to all modes. Since the higher order transverse modes have larger optical intensities near the cladding, they leak out more and thus suffer higher losses. We have circumvented some of the regrowth difficulties in the fabrication of such lasers and experimentally demonstrated a very low threshold, 800 μA, single mode VCSEL. With this structure, we obtained stable single mode operation up to 12 times laser threshold current [1-2].

We performed detailed measurements of near field and far field intensity profiles on the BH VCSEL's at various current levels. Most of 8 and 16 μm diameter lasers emit in a single transverse mode with a fixed polarization. Although the single transverse mode behavior is indeed designed and expected, the fixed polarization was not clearly understood. The origin of polarization selectivity is most likely due to a polarization-dependent gain, which may be introduced by the regrowth surrounding the InGaAs strained quantum wells. To investigate this effect, we are in the process of fabricating several different laser structures with regrowth just above and below the quantum well regions.

Oxide-confined VCSEL

Oxide-confined VCSEL refers to a new structure that utilizes the natural oxidation process in AlAs to form a current and optical confinement layer at desirable places within a laser structure. Fig. 2 shows one such example. Due to the fact that this confinement layer can be placed very near to the laser active region, extremely efficient current funneling can be obtained, which leads to an extremely low threshold current. This structure has led to tremendous progress in the field recently. However, very little understanding of the oxidation process has been attained. It has been found that the oxidation rate is highly dependent on the Al content and drops exponentially when the Al composition is reduced slightly from 1. This allows one to tailor the VCSEL design and to control the position of the oxidation layer. The oxidation process is a diffusion/reaction process; an AlAs layer is oxidized and becomes AlOx when it is exposed to water vapor at 400-500 °C. Typically a VCSEL post with fairly sizable diameter is first formed by etching and then placed in an oxidation furnace to allow the AlOx layer to form.

We recently reported a highly stable single mode oxide-confined VCSEL with excellent polarization control up to 18 times threshold [3], shown in Fig. 3. We also obtained very low threshold currents of 183 μA under continuous wave (CW) operation at room temperature (Fig. 4). We believe the excellent modal behavior of our VCSEL's is a result of our fabrication and oxidation processes which caused different oxide formation from some of the others' reports.

LIST OF PUBLICATIONS CITING JSEP SPONSORSHIP SINCE LAST PROPOSAL

1. C. J. Chang-Hasnain, Y. A. Wu, G. S. Li, G. Hasnain, K. D. Choquette, C. Caneau, and L. T. Florez, "Low Threshold Buried Heterostructure Vertical Cavity Surface Emitting Laser," Applied Physics Letters, Vol. 63, No. 10, pages 1307-1309, September 1993.

2. Y. A. Wu, C. J. Chang-Hasnain, and R. Nabiev, "Single mode Emission from a Passive-Antiguide-Region Vertical-Cavity Surface-Emitting Laser," Electronics Lett., Vol. 29, No. 21, pages 1861-1862, October 1993.

3. Y. A. Wu, C. J. Chang-Hasnain, and R. Nabiev, "Transverse Mode Selection with a Passive Antiguide Region in Vertical Cavity Surface Emitting Lasers," IEEE Photonics Technology Lett., Vol. 6, No. 8, pages 924-926, August 1994.

4. C. J. Chang-Hasnain, Y. A. Wu, L. E. Eng and G. S. Li, "Vertical Cavity Surface Emitting Laser Arrays for Wavelength Division Multiplexing Applications," International Journal of High Speed Electronics and Systems, Vol. 5, No. 4, pages 569-592 (1994).

5. R. Nabiev and C. J. Chang-Hasnain, "Voltage Drop in n- and p-Type Bragg Reflectors for Vertical-Cavity Surface-Emitting Lasers," IEEE Photonics Technology Lett., Vol. 7, No. 7, pages 733-735, July, 1995.

6. Y. A. Wu, G. S. Li, R. F. Nabiev, Kent D. Choquette, C. Caneau and C. J. Chang-Hasnain, "Single-Mode Passive Antiguide Vertical Cavity Surface Emitting Laser", IEEE J. of Selected Topics in Quantum Electron., Vol. 1, No. 2, pages 629-637, June 1995.

7. Rashit F. Nabiev, E. C. Vail and C. J. Chang-Hasnain, "Temperature Dependent Efficiency and Modulation Characteristics of Al-Free 980-nm Laser Diodes," IEEE Journal of Selected Topics in Quantum Electronics, Vol. 1, No. 2, pages 234-243, June 1995.

8. G. S. Li, W. Yuen, K. Toh, L. E. Eng, S. F. Lim and C. J. Chang-Hasnain, "Accurate Molecular Beam Epitaxial Growth of Vertical Cavity Surface-Emitting Laser using Diode Laser Reflectometry," IEEE Photonics Technology Letters, Vol. 7, No. 9, pages 971-973, September 1995.

9. G. S. Li, S. F. Lim, W. Yuen and C. J. Chang-Hasnain, "Polarization and Modal Behavior of Low Threshold Oxide and Air-Gap Confined Vertical Cavity Lasers," Electronics Letters., Vol. 31, 23, pp. 2014-5, Nov. 1995.

List of Publications Under Other Sponsorship Which Are Related To Work Unit

1. L. E. Eng, K. Bacher, W. Yuen, J. S. Harris, Jr. and C. J. Chang-Hasnain, "Multiple Wavelength Vertical Cavity Laser Arrays on Patterned Substrates," IEEE Journal of Quantum Electronics, Vol. 1., No. 2, pages 624-628, June, 1995.

2. L. E. Eng, K. Toh, K. Bacher, J. S. Harris, Jr. and C. J. Chang-Hasnain, "Periodic Mode Shift in Vertical Cavities Grown by Molecular Beam Epitaxy," IEEE Photonics Technology Letters, Vol. 7, No. 3, pages 235-237, March 1995.

3. C.J. Chang-Hasnain, "Vertical Cavity Surface Emitting Laser Arrays", book chapter in *Diode Laser Arrays* edited by D. Botez and D.R. Scifres, Cambridge University Press, 1993.

List of Technology Transfer Since Laser Proposal

We have begun a close collaboration with Dr. David Dolfi and his research team in Hewlett Packard Laboratories on a new project on WDM optical interconnects for local area network applications. This project will be using our multi-wavelength VCSEL arrays and tunable tracking detectors as the transmitters and receivers. The fundamental studies and fabrication process in this proposal are of tremendous interest and importance to HPL.

Proposed Research Program

Approach

1. Buried-Heterostructure VCSEL Fabrication

The advantages of using an antiguided BH structure are numerous. First, the device size and indices of the waveguide and cladding are precisely determined by lithography and epitaxy,

respectively, leading to high reproducibility. Secondly, the laser core is surrounded by lattice-matched material, which is promising for long lifetime. Thirdly, the structure provides both current and optical confinement, leading to desirable high performance.

The disadvantages, however, include the difficulty in obtaining high quality regrowth. The shape of the laser is limited to have a trapezoidal vertical profile, limited by crystal-orientation dependent regrowth. This typically gives the top DBR which has a higher resistance, and a smaller contact area. In this program, we will evaluate many variations of etching and regrowth processes to attain high yield, reproducible, stable single mode VCSEL's. We will also study the effect of 3-D strain in QW's by fabricating a simple diode with InGaAs strained QWs and a lateral GaAs regrowth. Temperature dependent electro-luminescence will be measured to study the gain characteristics. In-plane edge emitting BH lasers with InGaAs QW's will also be fabricated and measured. Theoretical calculation of the third-dimension strain will also be undertaken.

2. Oxide-confined VCSEL Fabrication

Oxide-confined VCSELs have exhibited superior performance in record low threshold current and efficiency. Our own single mode results also show that this structure is extremely promising for mode control. However, from our preliminary data, we observed laser degradation through low and gentle temperature cycles. This may be devastating for long-term reliability and stability. Hence, it is extremely important to understand the exact nature of this oxide and to explore a reliable oxide fabrication method. Another common but totally disregarded problem relating to oxide-confined lasers is the high nonuniformity in laser aperture sizes, both for a given run and run to run. This is a highly important problem to overcome, since it is the high yield and wafer-scale processing that made VCSEL's attractive in the first place. In this program, we will address both of these issues.

To study the material property of the AlOx, we plan to perform many experimental material characterizations, such as TEM studies, PL, X-ray diffraction measurements, optical measurements, and Auger analysis. We have already started an active collaboration with Professor E. Weber of Material Science Department and Dr. Z. Liliental-Weber at the Lawrence Berkeley Laboratory to examine the AlOx formed under various oxidation conditions. Our preliminary study revealed the nature of the oxide and its interface property. We identified that the oxide is γ-Al_2O_3, which confirmed a recent report from IBM [4]. The interface between AlOx and AlGaAs appears to be rough and has voids, which are detrimental for device applications. We are currently experimenting with the oxidation parameters to eliminate this characteristic. Finally, a substantial amount of As precipitation is observed on the upper and lower interfaces of the graded AlxGa1-xAs and on the top surface of GaAs. Further work is needed to determine the role of As during oxidation process and the As precipitation in the rest of the heterostructure.

We plan to resolve the problem of oxidation control with two measures. First, we designed a new oxidation tube and acquired a new furnace. The new tube was designed to insure uniform vapor flow through the samples and the new furnace has a temperature feedback loop to insure temperature stability. With this new apparatus, we dramatically improved our oxidation rate, uniformity and run-to-run repeatability recently. In addition to these new additions, we will introduce an in-situ optical monitor to measure the oxidation rate and process. This in-situ measurement will be essential in controlling the ultimate laser diameter, which cannot be otherwise controlled reliably and reproducibly since it is measured only by the diffusion time.

3. VCSEL Characterization

Thorough characterizations will be performed on our single mode BH and OC VCSELs, including polarization and modal behavior, high speed modulation response, noise, chirp and linewidth.

The polarization selection mechanism will be investigated through both device modeling as well as experimental measurements. With respect to laser noise and modulation, we have already started an active collaboration with Professor Kam Lau's group. We will be examining laser dynamics as a function of the detune between the Fabry-Perot wavelength and gain peak. This effect had been previously visited for DFB (distributed feedback) lasers. However, typical DFB lasers have much smaller finesse and narrower free spectra range. These two factors can play a major role in carrier dynamics and laser response. We expect a weaker wavelength dependence in the 3dB bandwidth of VCSEL, promising for WDM applications. We will perform both theoretical and experimental measurements including examining the spontaneous emission from the top and edges of VCSELs above and below thresholds.

Expected Result/Impact

The proposed work represents a serious effort to attain single mode VCSEL's, which will enable a tremendously wide range of applications, both military and civilian. Our past work has already demonstrated promising results and we will expand upon those in this program. In addition to device design and modeling, fabrication and characterization, our study includes fundamental studies of strain-induced polarization selectivity, laser dynamics and AlAs oxidation process. The result of this study will lead to reproducible fabrication of high performance single mode VCSELs and fundamental knowledge of materials and device processing, which will be useful for other optoelectronic devices.

REFERENCES

[1] Y. A. Wu, G. S. Li, R. Nabiev, K. D. Choquette, C. Caneau and C. J. Chang-Hasnain, "Performance of Passive Antiguide Region Vertical Cavity Lasers", IEEE J. of Selected Topics in Quantum Electron., 1, 2, pp. 629-637, June 1995.

[2] A. Wu, G. S. Li, W. Yuen, and C. J. Chang-Hasnain, "High yield Continuous Wave Operation of a Passive Antiguide Region Vertical-Cavity Surface-Emitting Laser", LEOS Annual Meeting, San Francisco, CA, Nov. 1995.

[3] G. S. Li, S. F. Lim, W. Yuen and C. J. Chang-Hasnain, "Polarization and Modal Behavior of Low Threshold Oxide and Air-Gap Confined Vertical Cavity Lasers," Electronics Letters., Vol. 31, 23, pp. 2014-5, Nov. 1995.

[4] S. Guha, F. Agahi, B. Pezeshi, J. A. Kash, D. W. Kisker and N.A. Bojarczuk, Appl. Phys. Lett. 68, 906, 1996.

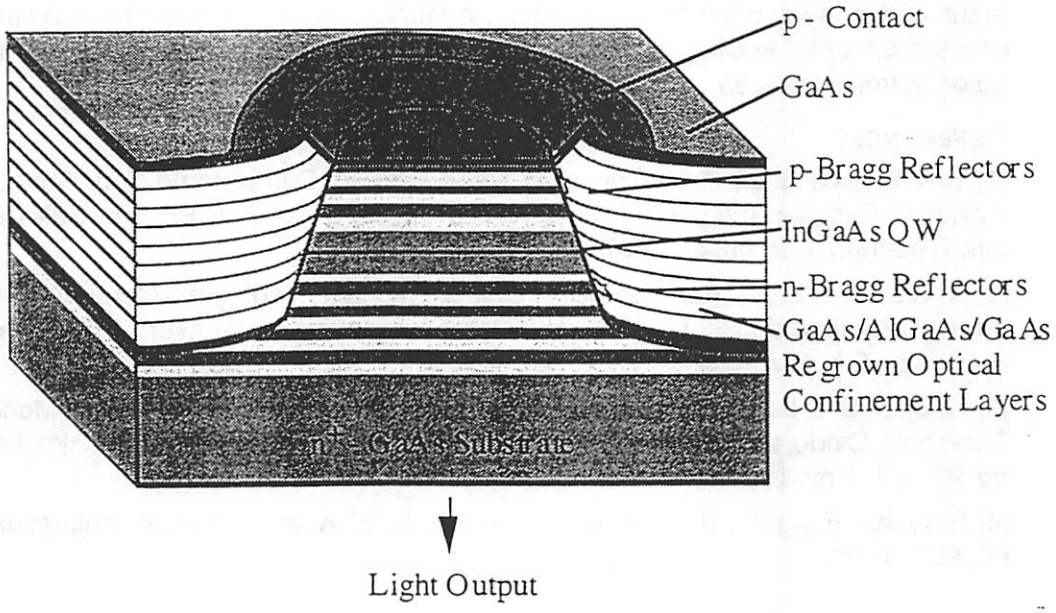


Figure 1. Schematic of a buried heterostructure VCSEL with regrowth to form optical cladding providing current and optical confinements

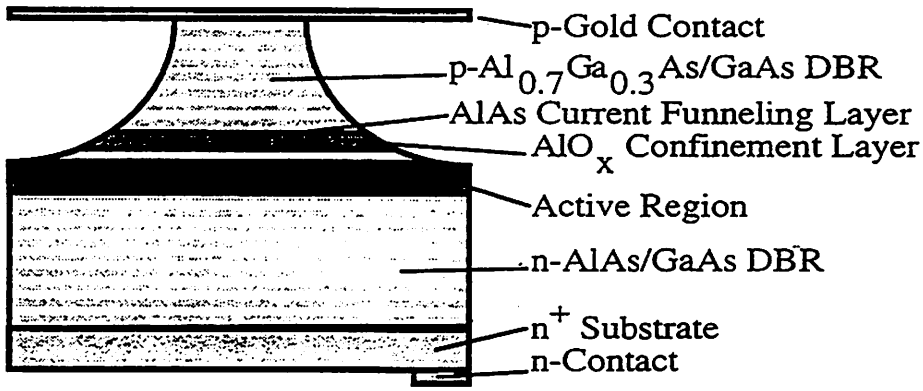


Figure 2. Schematic of an oxide-confined VCSEL

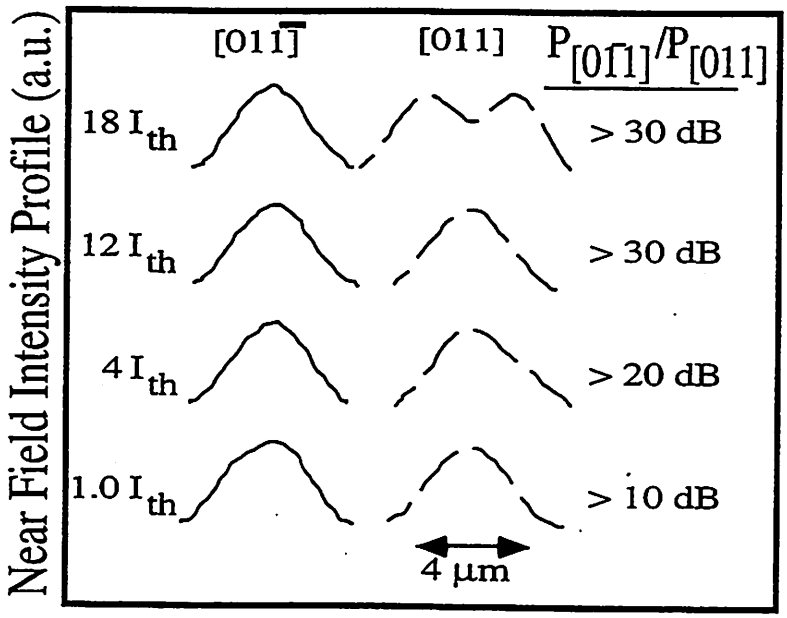
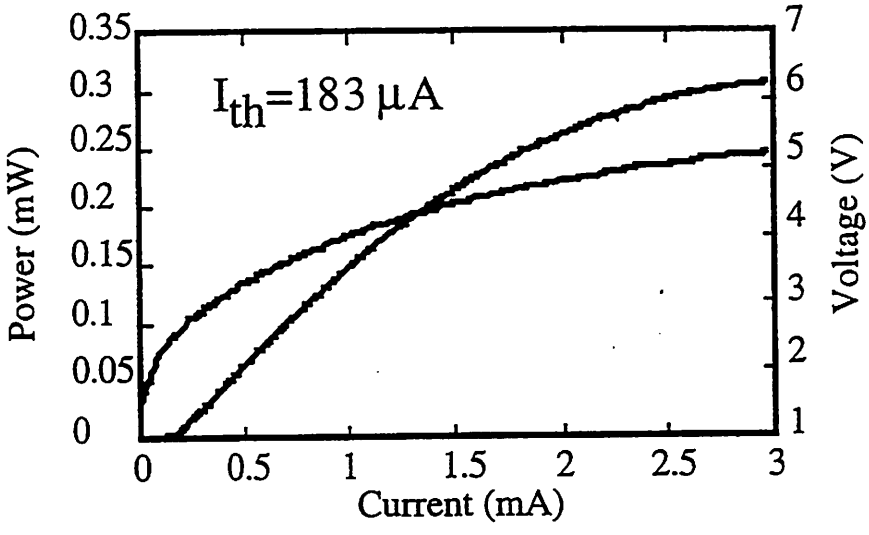


Figure 3. Near field intensity profiles of an oxide-confined VCSEL with excellent polarization control up to 18 times threshold.



4. Light vs. current and voltage vs. current curves for a typical OC VCSEL under continuous wave (CW) operation at room temperature

UNIVERSITY: UC BEKELEY **LAB: ERL**
JOINT SERVICES ELECTRONICS PROGRAM **RESEARCH UNIT: I-F**
LAST YEAR'S RESEARCH UNIT: I-E

TITLE OF INVESTIGATION: Synthesis and Characterization of GaN-Based Heterostructures

SENIOR INVESTIGATORS: Eicke Weber **TELEPHONE:**510-642-0205
Nathan Cheung 510-642-1615

JSEP FUNDS (CURRENT):

PI	TITLE	PERIOD	AMOUNT (1994-1997)
EW NC	Growth and Characterization of ALxGA1-xN and ALN/GAN Superlattices	6/94-1/97	$268,148

JSEP FUNDS (PROPOSED):

1997-1998	$100,000
1998-1999	$100,000
1999-2000	$100,000

OTHER FUNDING:

PI	TITLE	PERIOD:	AMOUNT:	SPONSOR:
EW	Stability and Reliability of Non-Stoichiometric Layers of III/V Semiconductors (Pending)	6/1/96-5/31/99	$243,166	AFOSR
EW	Identification and Control of Lifetime Reducing Defect in Polycrystalline Silicon Photovoltaic Materials (Pending)	2/1/96-1/31/97	$136,000	NREL
EW	Defect Reduction in Gallium Nitride for Microwave Power Amplifiers (Pending)	3/1/96-2/28/99	$1,248,352	BMDO
NC	Circuit Reliability Hot-Electron Model and Simulationl	9/1/95-10/31/96	$169,167	SRC
NC	Plasma Doping Investigation	1/15/96-12/31/96	$60,000	Eaton Corp
NC	Plasma Implantation for the Formulation of Ultra Shallow Junctions	12/15/95-12/30/96	$80,000	Sematech
NC	Plasma Processing Effects (Pending)	7/1/96-6/30/97	$32,000	MICRO

TOTAL NUMBER OF PROFESSIONALS

CURRENT - FACULTY:	2 @ 1 week summer (each)
CURRENT - STUDENT:	2 @ 49.9% academic year; 100% summer

PROPOSED FACULTY: 2 @ 1 week summer (each)
PROPOSED STUDENTS: 2 @ 49.9% academic year; 100% summer

SYNTHESIS AND CHARACTERIZATION OF GaN-BASED HETEROSTRUCTURES

FACULTY INVESTIGATORS: EICKE WEBER AND NATHAN W. CHEUNG

SCIENTIFIC OBJECTIVE

The objective of this project is to synthesize thin films of GaN, AlGaN/GaN and InGaN/GaN superlattice layers on different substrates with emphasis on reduction of the density of structural defects and background doping. The growth will be performed mainly by ion-assisted Molecular Beam Epitaxy, building up on the expertise in ion-assisted MBE growth of GaN gained within the first years of this project. In addition to the commonly used substrates of sapphire and SiC, it is intended to investigate the use as substrates layers of AlN and GaN deposited by pulsed laser deposition (PLD). Preliminary studies have shown that PLD-deposited layers have a surprisingly good surface morphology, making them very promising for overgrowth by ion-assisted MBE. We will also use laser annealing to investigate dopant activation and the formation of metastable GaAlN alloys. Defects in the thin film structures will be analyzed by detailed electronic and structural defect analysis, including magnetic resonance and state-of-the-art electron microscopy techniques. Fabrication and testing of simple devices will be the ultimate test of the success of the growth effort.

STATE-OF-THE-ART

The progress in the use of GaN for optoelectronic devices has been breathtaking within the last few years. The first discovery of successful p-type doping of GaN in 1989 was rapidly followed by the demonstration of the first LED, the first commercial LED, and, in December of 1995, the demonstration of the first solid state laser based on GaN technology. However, all these devices exhibit an extraordinary high defect density with more then $10^8/cm^2$ dislocations, and it is extraordinary that despite the high defect density LED's with a respectable external quantum efficiency of 8% are commercially available.

However, a whole set of serious materials problems are still to overcome before the great promise of GaN and the related heterostructures can be realized in both fields, optoelectronic and electronic devices. This project will address some of these problems, in close collaboration with ongoing work in Lawrence Berkeley National Laboratory and with other academic and industrial groups.

PROGRESS SINCE LAST MAJOR PROPOSAL

A unique Hollow Anode Nitrogen Source (HAS) [1] has been developed in Berkeley for the ion-assisted MBE growth of GaN and is currently being improved. Constructional changes were required to increase the nitrogen ion flux to obtain a more reasonable GaN growth rate of ~ 0.25 μm. Our MBE-grown GaN films are n-type with carrier concentrations up to $10^{19}/cm^3$. The films exhibit typically an x-ray rocking curve width of 20 arcmin at half maximum (FWHM). In single instances almost semi-insulating material or material with better structural quality (5 arcmin) were grown. The large n-type conductivity prohibited first attempts to grow p-type films by doping with Mg. and Ca. The n-type conductivity is thought to be caused by native defects. In fact, the stoichiometry of our films varies: Ga rich, N rich and stoichiometric GaN have been grown. Thus, our research focuses now on the control of stoichiometry, on the reduction of n-type carrier concentrations and a reproducible growth of high quality material with the HAS. This seems necessary to achieve p-doped GaN films of competitive structural quality that could be used for the fabrication of device prototypes. Growth on different substrate materials was evaluated. Homoepitaxially MBE grown films on small (2mmx2mm) GaN bulk substrates exhibit outstanding

structural and optical properties [2]. For the first time, homoepitaxy was used to provide a benchmark for the calibration of stress that is present in almost all heteroepitaxially grown thin films as shown in Figure 1. Stress values of more than 1 GPa modify the band gap of GaN greatly. It changes by ~40 meV per GPa of hydrostatic pressure. Strain in GaN thin films is caused by the presence of extended defects, the change of stoichiometry, the growth of buffer layers, the lattice mismatch and the different thermal expansion coefficients of substrates and GaN films. The thermal expansion coefficients of SiC and sapphire were found to extend or compress the GaN films, respectively, during the post-growth cooling. This introduces a difference into GaN films that were either grown on SiC substrates or on sapphire. In this respect, it is a strength of the MBE growth that it typically proceeds at much lower growth temperature (~700 degrees C) than MOCVD or MOVPE (~1050 C) GaN thin film growth because this minimizes thermal strain. Also, it is of practical importance to see that a low-temperature grown GaN buffer layer minimizes the stress in the GaN films in comparison with growth on AlN or growth without a buffer layer (Figure 2). Details of these phenomena are not well understood. We speculate that strain relaxation by change of stoichiometry may contribute. Currently, a model is being developed that links strain relaxation by the introduction of non-stoichiometric defects or impurities with the biaxial strain that is caused by the lattice mismatch or the cooling of heteroepitaxially grown GaN. In Figure 1 it can be seen that the strain in many crystals, grown by different methods, can well be described by a linear elastic model. The model also explain the large deviations from the average values seen in Figure 3. The control and the understanding of strain effects in GaN was found to be crucial for a further development of the material [3]. The surface roughness of different substrate materials and GaN films was investigated by atomic force microscopy and transmission electron microscopy. Results characterizing the surfaces by their root mean square (RMS) roughness are summarized in figure 3. Sapphire clearly exhibits a smoother surface than SiC does. This is why we now commonly use sapphire as substrate material for MBE growth and LASER ablation. It also can be seen that 3 - 5 μm thick GaN films obtained from Japanese groups exhibit a RMS of 0.8 and 1 nm. These values set goals for our short term research and it can be seen that our best LASER ablated AlN buffer layers can well compete with the smallest values [4]. Figure 4 depicts that the RMS roughness and the surface morphology of LASER-ablated AlN films depend on the nitrogen partial pressure in the growth chamber. Atomically flat surfaces can reproducibly be obtained for an N2 partial pressure of 10-3 Torr in the chamber. The N2 partial pressure affects the growth rate and the chemical composition of the ablated films [4]. On the other hand, it is now clear from the MBE and the MOCVD growth that LT-GaN buffer layers can relax the strain in the films more efficiently than the AlN layer, Therefore, it is most desirable to extend our ablation experiments to the growth of GaN buffer layers. The fabrication of LED's or LASER diodes requires growth of InN layers of a certain composition into the GaN thin films to lower the band gap energy to a desired value. However, the segregation coefficient of In in GaN is very low. As a consequence GaN/InGaN/GaN quantum wells are expected to exhibit rough and asymmetric interfaces. We show in Figure 5 that, very recently, it became possible to locally measure the In distribution in GaN/InN/AlN quantum wells at an atomic scale for the first time [5]. Such unique characterization tools would certainly help to develop and to improve LASER structures because it is this local In distribution that determines the color purity of LASERS's and LED's.

List of Publications Citing JSEP Sponsorship

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2. J.S.Chan, T.C.Fu, N.Cheung, N.Newman, X.Liu, J.T.Ross, M.D.Rubin and P.Chu, "Metallization of GaN Thin Films Prepared by Ion Beam Assisted Molecular Beam Epitaxy", Mat. Res. Soc.

Symp. Proceedings, Vol. 339, pp.223-227 (1994).

3. T.C. Fu, N.Newman, E. Jones, J.S. Chan, X. Liu, M.D. Rubin, N.W. Cheung, and E.R. Weber, "The influence of nitrogen ion energy on the quality of GaN films grown with molecular beam epitaxy", J. Electronic Mat.,Vol. 24, pp.249-255, 1995.

4. J.S. Chan, N.Newman, T.C. Fu, M.D. Rubin, and N.W. Cheung, "Recipe for molecular beam epitaxy growth of aluminum nitride", Handbook of Thin Film Process Technology, ed. by D.A. Glocker and S.I. Shah, Institute of Physics Publishing (Bristol and Philadelphia), June,1995.

5. J.S. Chan, N.Newman, T.C. Fu, M.D. Rubin, and N.W. Cheung, "Recipe for RF magnetron sputtering of aluminum nitride", Handbook of Thin Film Process Technology, ed. by D.A. Glocker and S.I. Shah, Institute of Physics Publishing (Bristol and Philadelphia), June,1995.

6. T.C. Fu, N.Newman, E. Jones, J.S. Chan, X. Liu, M.D. Rubin, N.W. Cheung, and E.R. Weber, "The influence of nitrogen ion energy on the quality of GaN films grown with molecular beam epitaxy", J. Electronic Mat.,Vol. 24, pp.249-255, 1995.

7. D. Feiler, A.A. Talin, J. Ren, R.S. Williams, J.S. Chan, and N.W. Cheung, "Pulsed laser Deposition of Epitaxial Wurzitic and Zincblende GaN Thin Films", Materials Research Society Proceedings,1995.

8. A.A. Talin, J. Ren, R.S. Williams, J.S. Chan, and N.W. Cheung, "Pulsed Laser Deposition of Epitaxial Wurzitic and Zincblende GaN Thin Films", to be published in MRS Proceedings, Fall Meeting, 1995.

9. J.S. Chan,N.W. Cheung, N. Newman, E. Jones, X. Liu, A. Gassmann, L. Schloss, E.R. Weber, and M.D. Rubin, "Si and Mg implantation into ion beam assisted molecular beam epitaxillay grown GaN", to be published in Appl. Phys. Lett., 1996.

List of Publications Under Other Sponsorship Which are Related to Work Unit

N/A

List of Technology Transfer Since Last Major Proposal

This project is pursued in close collaboration with America Xtal Technology that supplies the homoepitaxial substrates and collaborates with us in the surface preparation of GaN and SiC substrates. Cree Research is also a partner in evaluating the quality of their MOCVD GaN films.

Proposed Research Program

Approach

In this stage of the project it is crucial to demonstrate that reproducible growth of high quality GaN films can be performed with our new Hollow Anode Source. It will be used to grow Al/In/GaN heterostructures and p-doped films. The nucleation layer, the buffer layer thickness and the composition of the GaN film that is determined by the nitrogen and Ga fluxes are known to be sensitive growth parameters. We will address these questions by investigating the film surfaces with AFM at any step of the growth procedure. Whenever needed, other characterization tools will be employed. In particular, we will apply quantitative high resolution electron microscopy to characterize AlN/GaN/InN heterostructures. One of our highest priorities is to reduce the intrinsic n-doping level to values below $10^{17}/cm^3$ to allow for an effective p-doping with Mg or Ca. The experience gained in this process will be used to further improve our Hollow Anode Source design.

Once the synthesis of GaN films of different doping is satisfactorily implemented, the next step will be to grow layers of InGaN and AlGaN. Special interest will be devoted to the interface between the heterostructures and the doping range: current data indicate that in AlGaN the

donor level deepens at higher Al mole-fraction, which would severely limit the applicability of high-Al layers for applications as active device layers.

Our pulsed laser deposition (PLD) experiments will be extended for both laser ablation and pulse laser annealing experiments (Figure 6). For the ablation experiments, we plan to use compressed GaN and AlN powders and thick VPE grown GaN films as targets for the ablation process. Our experience with the fabrication of AlN buffer layers will allow for a rapid evaluation of the PLD deposited GaN films. It is obvious that the fabrication of p-doped buffer layers could be very beneficial for the goals of this project.

The rapid cooling after PLD deposition should allow deposit of ternary compounds even in concentration ranges that are not accessible to near-equilibrium growth processes. We will thus explore the possibility of depositing metastable III-nitride compounds by this technique.

Previous experiments of ion implantation for doping of III-nitrides showed very limited success. It appears to be promising to explore laser annealing after implantation as an alternative approach to activate dopants in these materials. In Figure 7, we show preliminary results which demonstrate the effectiveness of pulse laser annealing to recover crystalline damage after Mg implantation. AlN cap was used in the laser annealing experiments because it is transparent to the 248nm wavelength of the laser and maximum heat absorption is expected at the AlN/GaN interface. After Mg implantation to a dose around $1^{15}/cm^2$, we observe generation of many intergap states from cathodoluminescence measurements. However, after laser annealing, we have recovered from most of the implantation damage and the height of the band-edge exciton peaks indicates the annealed sample is even better than that of the as-grown sample which has not been implanted. We will pursue this pulse annealing technique for dopant activation in GaN. If proven successful, implantation is definitely the method of choice for fabricating monolithic III-nitride device arrays.

On the characterization side, we plan to investigate in detail strain-related phenomena. In particular, the impact of the GaN buffer layer composition on its morphology and its ability to relax strain are poorly known. This project will be part of our ongoing investigations that also includes the mapping of the In distribution at the atomic scale in GaN/InGaN/GaN quantum wells. Results will be correlated with the light emission of diodes and/or PLD structures. Also, the characterization and optimization of different substrate materials for homoepitaxial and heteroepitaxial growth of GaN will be an issue of central interest.

Expected Results/Impact

In view of the fact that the field of GaN-based heterostructures is so immature with many fundamental questions not yet answered, it is to be expected that this project will continue to have an impact on the progress in this field. Of special relevance will be the use of PLD-deposited layers as substrates and buffer layers for subsequent IA-MBE overgrowth, as well as the analysis of these layers directly and their use for devices.

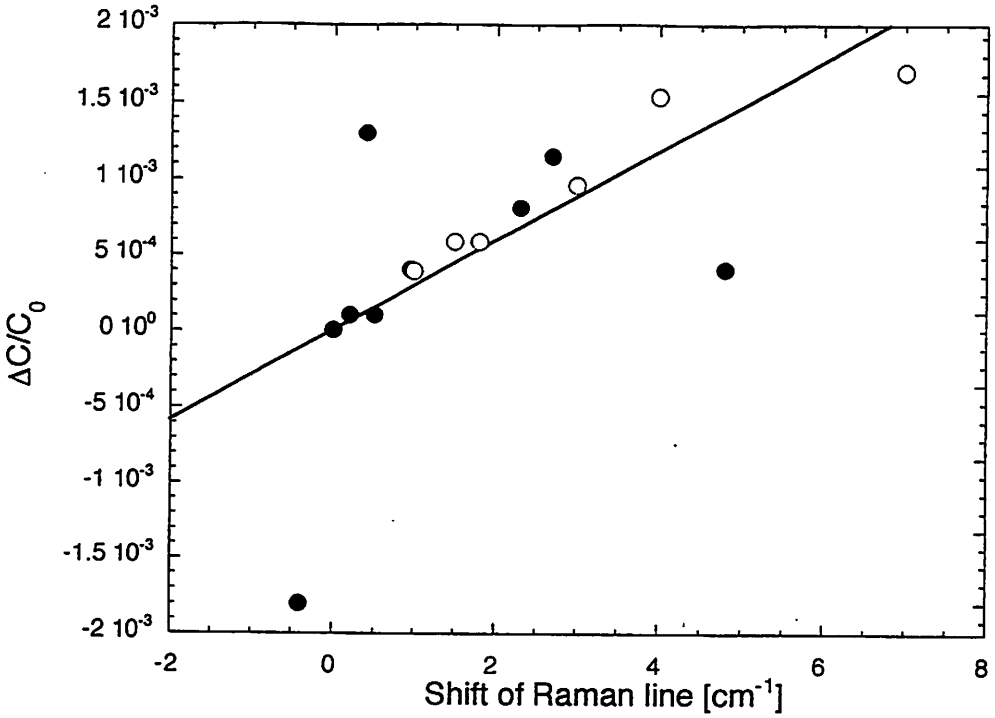

Figure 1: Change of the c lattice constant caused partly by the biaxial stress in the GaN layers that can be compressive and tensile. Raman shifts of the E2 phonon mode were used to determine the amount of stress (1 GPa induces a shift of ~3.1 cm^{-1}). The large scatter of some of the data could be caused by sample cracking or by deviations from a stoichiometric composition of some films. The straight line is calculated from an linear elastic model. Homoepitaxy provided a zero strain calibration.

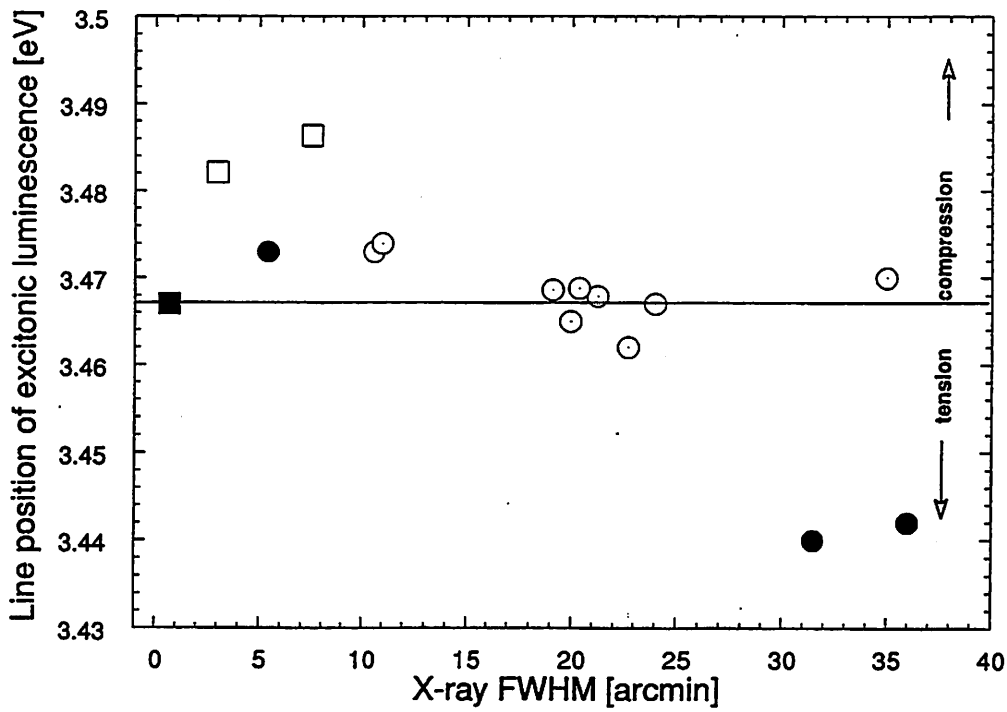

Figure 2: Homoepitaxy (filled square) provides a zero stress calibration for near band edge photoluminescence lines that shift with stress induced changes of the band edge. Samples are found to exhibit tensile and compressive stress. MBE growth on a low temperature GaN buffer layer minimizes the stresses (open circles). The effect is almost independent of the extended defect density as determined by the x-ray rocking curves (FWHM). For comparison: growth with no buffer layer (filled circles) can induce tension; MOCVD growth on AlN buffer layers (open squares) induces compression into the GaN films.

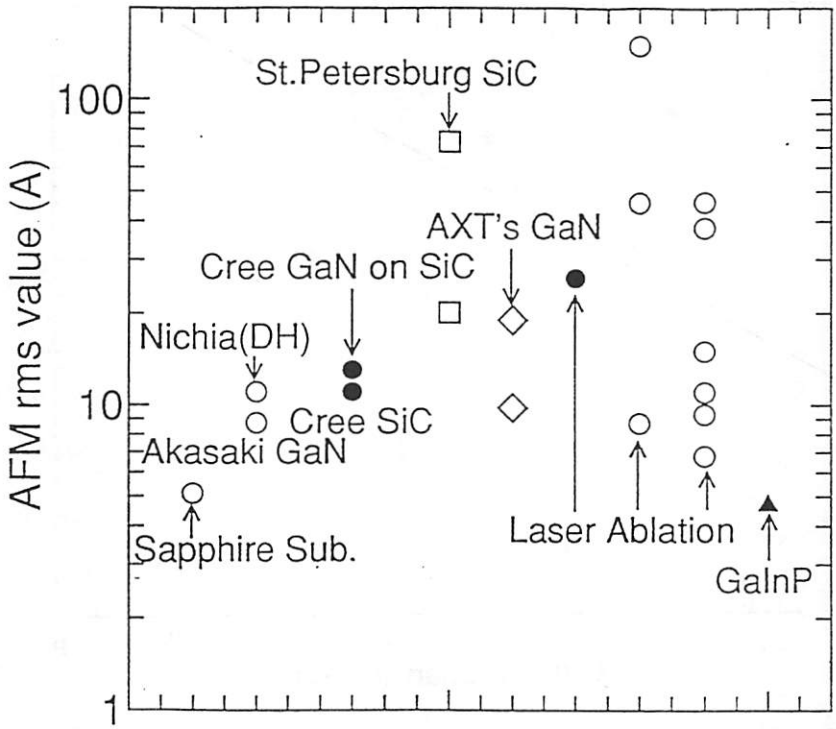

Figure 3: Surface characterization of different substrate materials and thin film materials. The listed root mean square roughness values were obtained by atomic force microscopy for a 2um x 2um area.

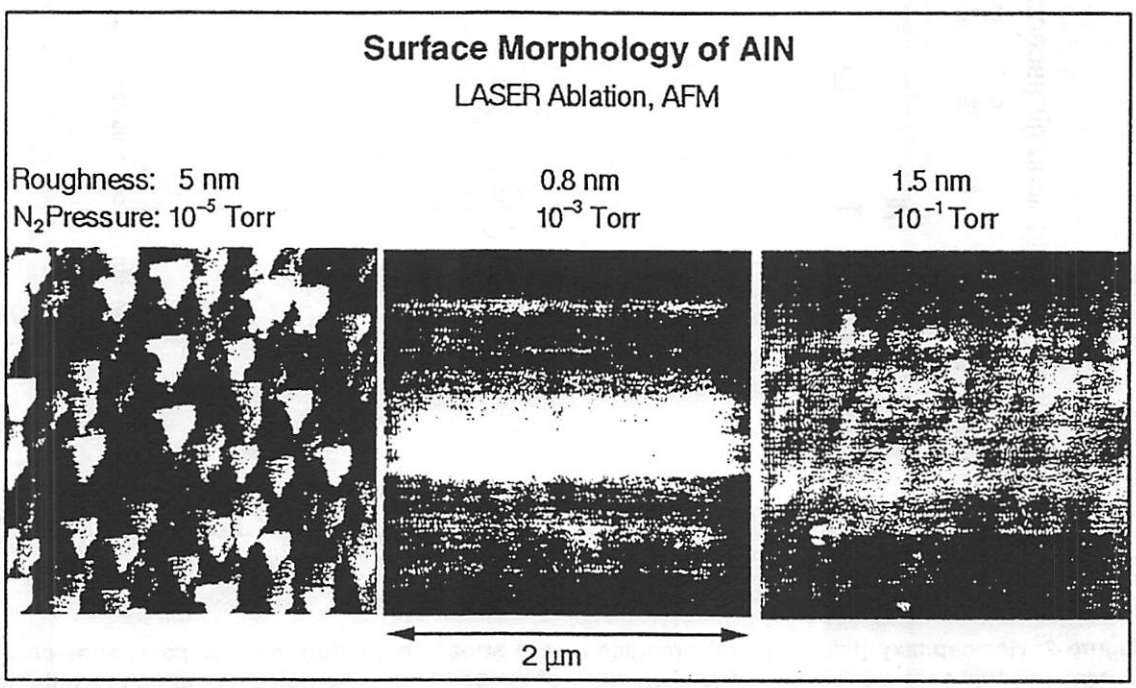

Figure 4: Surface morphology of AlN buffer layers obtained by LASER ablation. For details see text.

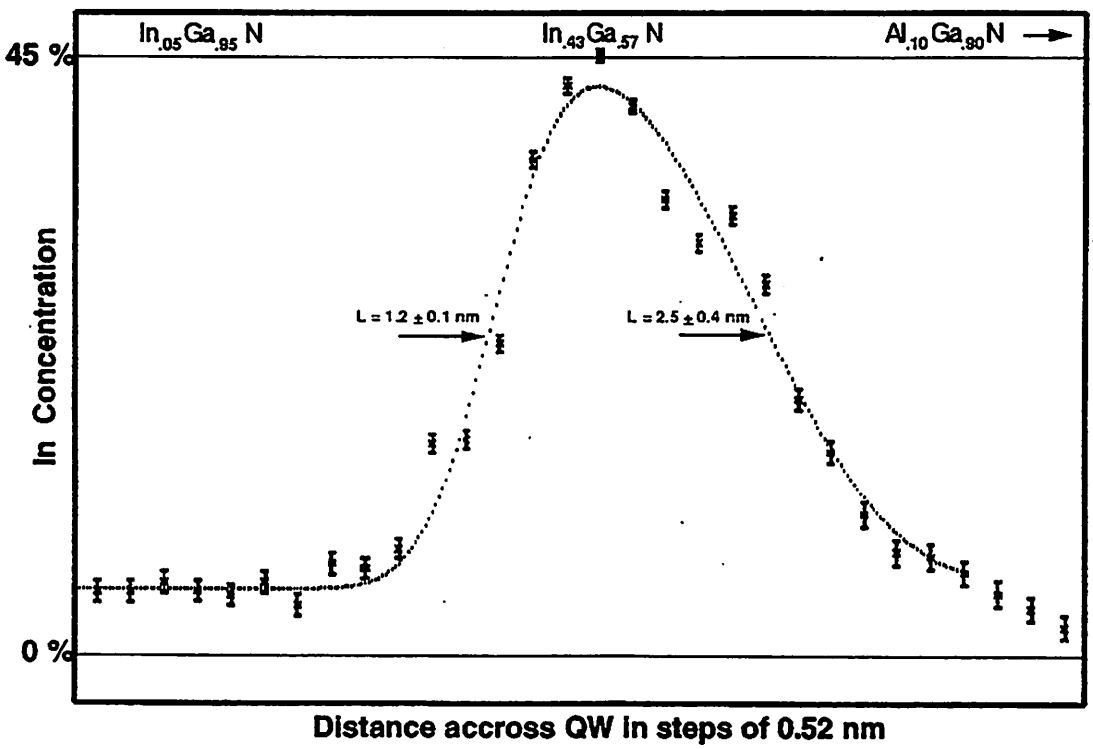

Figure 5: Composition profile across an GaN/InN/GaN quantum well of a Laser diode. Note the accuracy as to which the roughness of the interfaces (L) and the quantum well width can be determined.

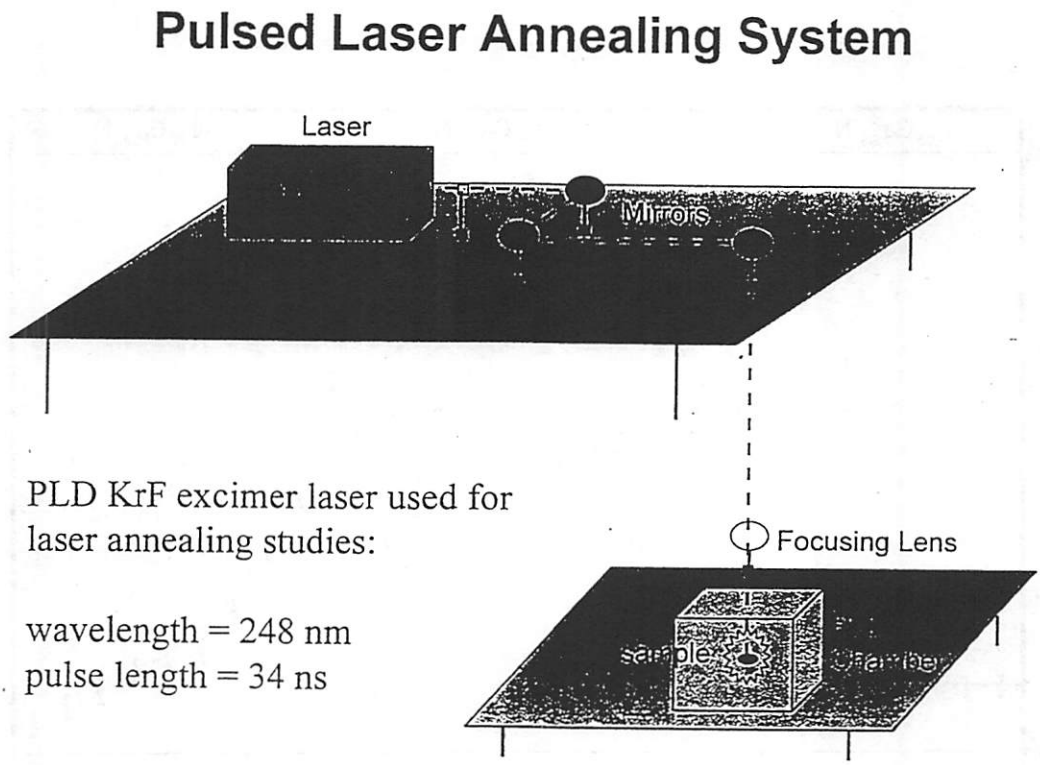

Figure 6: Schematic showing modification of the Berkeley laser ablation system which will also be used for laser annealing experiments.

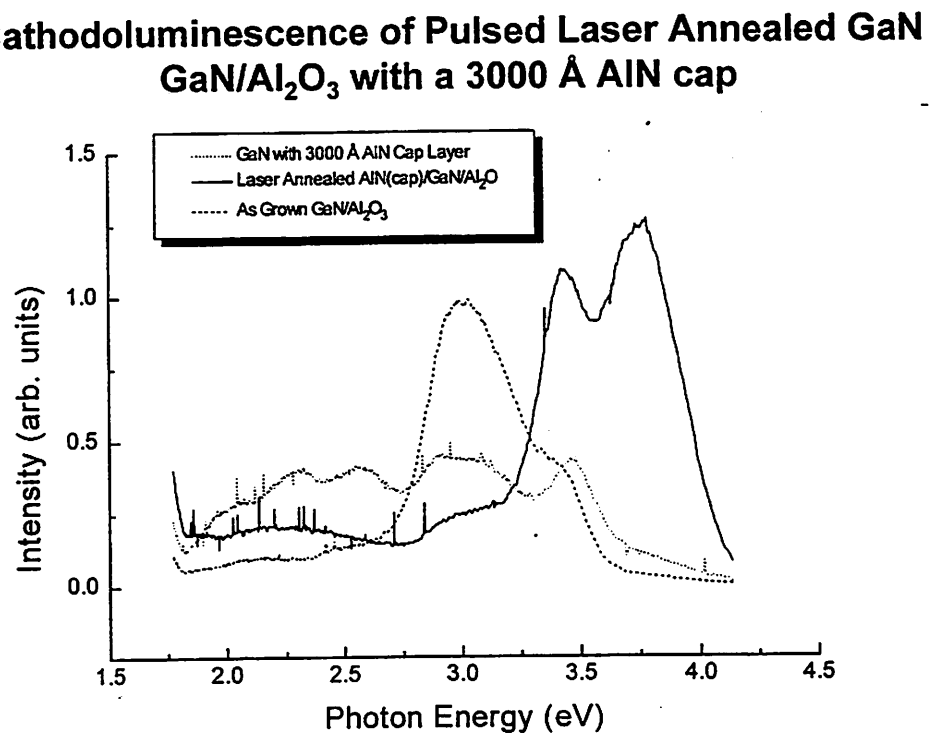

Figure 7: Cathodoluminescence of GaN samples grown on Sapphire. After Mg implantation, many intergap states exist within the energy gap. After laser annealing, the crystallinity improves drastically and the 3.5eV exciton peak is even better than the as-grown sample.

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PART II. NANOELECTRONIC SYSTEMS

AREA OVERVIEW

There is a considerable effort around the world today in the field of quantum dot devices, coulomb blockade devices, and other devices that operate in the nanometer size regime. There is also some very fundamental research on quantum logic gates that operate on quantum bits (qubits). On the other hand, research on silicon CMOS devices in our own JSEP program as well as elsewhere suggests that the evolution of MOSFET's may extend well into the nanoelectronics regime.

The question of which device or approach is best has little meaning absent a systems context. Yet, by comparison with the amount of nanodevice research being conducted worldwide, there is rather little work on systems using these devices. Generally, the new devices that have been proposed to date have characteristics that make them difficult to integrate into systems: they have poor input/output isolation, or low current drive, or both.

For these reasons, we propose to initiate a new thrust in the Berkeley JSEP program on nanoelectronic systems. It is our intention that this work be synergistic with our own device research. Some of it is well coupled at the outset, while some of it is more adventurous, and will likely only stimulate interest on the part of device researchers once some progress is made in demonstrating that these new systems concepts have a general computational capability.

Professor Sangiovanni-Vincentelli's work unit addresses the circuit and systems design issues that emerge as silicon CMOS devices shrink into the nanoelectronics regime. Under this scenario, it is expected that chip design will become dominated by the need to cope with rapidly rising parasitics associated with the interconnections among transistors. At the same time, integrated circuit systems will become ever larger and more complex, and thus designers will become even more dependent on automatic computer-aided-design (CAD). Current integrated circuit CAD strategies deal with parasitics locally, at the lowest level of the design hierarchy: mask layout. In the nanoelectronics regime, the dominance of interconnection parasitics will demand that transistors be connected only to relatively near-neighbors. This forces the need for interconnect to be incorporated into higher representational levels in the CAD process. This work unit will attempt to accomplish this at the logic synthesis level. Success in this endeavor will be essential to continue the evolution of CMOS device technology into the nanoelectronics regime. It is therefore highly synergistic with Professor Hu's device research.

Professor Chua's cellular neural network (CNN) paradigm offers a natural architecture for quantum dot cellular automata architectures. His extensive research on the CNN will provide a solid framework for evaluating the capabilities of a large number of quantum dots interacting only via nearest neighbor coupling. The CNN universal machine that operates in his laboratory will be used to simulate and validate the local interaction rules that will accomplish particular desired behaviors of a large quantum dot array.

Finally, Professors Vazirani and Papadimitriou, both eminent theoretical computer scientists who are new to JSEP will collaborate on radically new bases for computation that may offer attractive architectures for future nanoelectronics systems. They propose to research quantum computing and DNA computing. Both of these new computing ideas have recently been shown to be capable of solving certain particular computational problems that are way beyond the reach of conventional computers. It is noteworthy that the problem solved by quantum computing is that of prime factorization, the intractability of which forms the basis of modern cryptography. In this

work unit, they will seek to develop new principles and algorithms that can harness the tremendous potential capabilities of both of these new computing models to solve a larger and more general class of problems.

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Professor of Electrical Engineering and Computer Science, University of California, at Berkeley

Education:

Doctor of Engineering, Politecnico di Milano, Italy, 1971

Area of Research:

Computer aided analysis and design, VSLI circuits, large scale system analysis, integrated circuits

Experience:

University of California faculty member since 1976

Visiting Scientist, IBM T.J. Watson Research Center, 1980

Visiting Professor: MIT 1987, University of Torino, University of Bologna, University of Pavia, University of Pisa and University of Rome

Professional Activities:

Consultant for several major U.S. (including ATT, IBM, DEC, GTE, NYTEX, General Electric), European (Alcatel, Bull, Olivetti, SGS-Thomson, Fiat) and Japanese companies (Kawasaki steel).

Member of the Program Committees of International Symposium on Circuits and Systems, Custom Integrated Circuit Conference, Design Automation Conference, International Conference on Circuits and Computers, International Symposium on VLSI Technology, Systems and Applications, International Conference on Computer-Aided Design, Technical Program Committee Chair for 1989, Conference Chairman, 1990, Euro-DAC, 1991-1992, Workshop on Computer Aided Verification, 1993.

Member of the International Advisory Board of the Institute for Micro-electronics, Singapore (with Dr. I. Ross, ATT, Chairman, Dr. P. Pistorio, SGS-Thomson, CEO, Mr. Kawanishi, Toshiba, Senior Executive Vice-President, Dr. Fischer, Siemens, executive Vice President).

Member of the advisory board of the Lester Center of Entrepreneurship and Management of Technology of the Haas School of Business Administration, University of California, at Berkeley.

Elected fellow for "contributions to circuit simulation and computer aids for the design of integrated circuits.", Institute of Electronics and Electrical Engineers (IEEE).

Honors and Awards:

1981, Distinguished Teaching Award, University of California

1986-87, Darlington Award for best paper of the IEEE Transactions published by the Circuits and Systems Society for bridging theory and practice

1989, IEEE CAD Transactions Best Paper Award

1991, Best Paper Award, Design Automation Conference, San Francisco, june 1991.

1991,Medal of Scuola Sant'Anna, University of Pisa.

Relevant Publications:

Books

R.K. Brayton, G. Hachtel, C. McMullen and A. Sangiovanni-Vincentelli, "Logic Minimization Algorithms for VLSI Synthesis" Kluwer Academic Publishers, 1984.

J. White and A. Sangiovanni-Vincentelli, "Relaxation Techniques for the Simulation of VLSI Circuits," Kluwer Academic Publishing, October 1986.

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S.M., Massachusetts Institute of Technology 1961.

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General nonlinear network and system theory

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Editor, IEEE Transaction on Circuits and Systems, 1973-1975.

President, IEEE Society on Circuits and Systems, 1976.

Editor, International Journal of Bifurcation and Chaos.

Deputy Editor, International Journal of Circuit Theory and Applications.

Honors and Awards:

5 USA Patents

Fellow of IEEE, 1973

IEEE WRG Baker Prize

IEEE Browder J. Thompson Prize, 1973

IEEE Centennial Medal, 1985

Doctor Honoris Causa, Ecole Polytechnique Federal-Lausanne, Switzerland, 1983.

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Honorary Doctor, Technical University of Dresden, Germany, 1992.

Doctor Honoris Causa, Technical University of Budapest, Hungary, 1994.

Doctor Honoris Causa, University of Santiago De Compostela, Spain, 1995.

Doctor Honoris Causa, University of Frankfurt, Germany, 1996.

Technical Achievement Award by the IEEE Circuits and Systems Society, 1993.

M.E. Van Valkenburg Prize from the IEEE Circuits and Systems Society, 1995,

Relevant Publications:

L. Chua, M. Hasler, G. Moschytz, and J. Neirynck, "Autonomous Cellular Neural Networks: A Unified Paradigm for Patter Formation and Active Wave Propagation," IEEE Trans. CAS-I, Oct. 1995.

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L. Chua and L. Yang, "Cellular Neural Networks," IEEE Trans. CAS, Oct. 1988.

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Ph.D., 1986 Computer Science, University of California at Berkeley, Minor Fields: Algebra, Operations Research

B.S., 1981 Computer Science, Massachusetts Institute of Technology

Area of Research:

Quantum computation, computational foundations of randomness, computational complexity theory, computational learning theory.

Experience:

1991-Present: Associate Professor of Computer Science, University of California at Berkeley

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1987: Visiting Scholar, University of Paris-sud, Orsay

1986-1987: Thomas J. Cabot, Harvard University, Assistant Professor of Computer Science

1986-1987: Consultant, AT\&T Bell Labs, Murray Hill, NJ

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1984: Summer Visitor, IBM Yorktown Heights Research Laboratory

Professional Activities:

Editor, Computational Complexity.

Editor, Combinatorics, Probability and Complexity.

Program Committee Member, FOCS 1986.

Program Committee Member, STOC 1990.

Program Committee Member, FOCS 1995.

Organizer: Dagstuhl workshop on ``Randomized Algorithms", 1991.

Organizer: Berkeley workshop on ``Randomized Algorithms", 1995.

Honors and Awards:

IBM Graduate Fellowship, 1983 and 1984.

Friedman Mathematics Prize, 1985.

Presidential Young Investigator Award, 1987.

Young Faculty Development Award, University of California at Berkeley, 1988.

IBM Faculty Development Award, Electronics Education Foundation, 1989.

Publications:

`Matching is as Easy as Matrix Inversion, with K.Mulmuley and V.V.Vazirani, invited paper in

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1. "Quantum Complexity Theory" with E. Bernstein, invited to special issue of Siam J. Comp. on quantum computation.

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3. "Go-with-the-winners algorithms," with D. AldousFOCS, 1994.

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5. "A Simple and Efficient Leader Election Protocol," with R. Ostrowsky, S. Rajagopalan, STOC 1994.

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7. "Quantum Complexity Theory" with E. Bernstein, STOC, 1993.

8. "A Markovian Extension of Valiant's Learning Model," with D. Aldous, FOCS, 1990. Final version in Information and Computation, Vol 117, No. 2, pp 181-186, 1995.

9. "An Optimal Online Bipartite Matching Algorithm," with R.M. Karp and V.V. Vazirani, STOC, 1990.

10. "G^2 and Approximations for Chromatic Number," with N.Linial, FOCS, 1989.

11. "Polytopes, Permanents and Graphs with Large Factors," with P. Dagum, M. Luby and M.

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14. "Sampling a Population Using a Single Semi-Random Source," with V.V.Vazirani, FSTTCS Conference, New Delhi, India, 1986; invited paper in Theoretical Computer Science.

15. "Random Polynomial Time is Equal to Semi-Random Polynomial Time,'" with V.V. Vazirani, FOCS, 1985.

16. "Towards a Strong Communication Complexity Theory or Generating Quasi-Random Sequences from Two Communicating Semi-Random Sources" STOC, 1985; final version invited to appear in Combinatorica Vol. 7, No. 4, 1987.

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Education:

1972: Diploma in Electrical Engineering, National Technical University of Athens.

1976: Ph.D., Princeton University.

Experience

1976-1978: Gordon McKay Assistant Professor of Computer Science, Harvard University.

1978-1979: Miller Fellow for Science, University of California, Berkeley.

1979-1983: Assistant Professor of Computer Science, Massachusetts Institute of Technology. Associate Professor, as of July 1981.

1976-present: Consultant with AT\&T Bell Laboratories, Murray Hill.

1981-1988: Professor of Computer Science, National Technical University of Athens.

April 1983-1988: Professor of Computer Science and Operations Research, Stanford University.

1988-Present: Irwin Mark and Joan Klein Jacobs Professor of Computer Science and Engineering, University of California at San Diego.

1989: Visiting Researcher, Computer Technology Institute, Patras, Greece.

1989:Visiting Professor, Laboratory for Intelligent Decision Systems, M.I.T.

Professional Activities:

On the Editorial board of J.ACM 1983-1986, J. of Computer and Systems Sciences, Combinatorica, Journal of Computer Science and Technology, Beijing, China, Algorithmica, Information and Computation, J. of Operations Research and Computer Science, Journal of AI Research, SIAM J. on Discrete Mathematics, Annals of Mathematics and Artificial Intelligence, and Journal of AI Research

On the program committee of several international conferences.

Chair of the Program Committee for the 1989 STOC. Chair of the organizing committee for the 12th ICALP (1985, Nafplion, Greece).

Chair of the IEEE Computer Society's Technical Committee on the Mathematical Foundations of Computing (1986-89).

Publications:

Books:

1. H.R. Lewis, C. H. Papadimitriou Elements of the Theory of Computation, Prentice-Hall, 1981.

2. C. H. Papadimitriou, K. Steiglitz Combinatorial Optimization: Algorithms and Complexity, Prentice-Hall, 1982.

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UNIVERSITY: UC BEKELEY **LAB: ERL**
JOINT SERVICES ELECTRONICS PROGRAM **RESEARCH UNIT: II-G**
LAST YEAR'S RESEARCH UNIT: II-C

TITLE OF INVESTIGATION: Logic Synthesis for the Nanodevice Era

SENIOR INVESTIGATORS: Alberto Sangiovanni-Vincentelli **TELEPHONE:**510-642-4882

JSEP FUNDS (CURRENT):

PI	TITLE	PERIOD	AMOUNT
AS	Inductive Learning Synthesis of Minimal Complexity Networks	6/94-1/97	$195,704

JSEP FUNDS (PROPOSED):

1997-1998	$65,000
1998-1999	$65,000
1999-2000	$65,000

OTHER FUNDING:

PI	TITLE	PERIOD:	AMOUNT:	SPONSOR:
AS	The Castle Project: A Proposal to the DOE for Integrated Parallel Scientific Computing	5/1/94-4/30/97	$910,000	DOE
AS	Center of Excellence in Design Automation	1/1/96-12/31/96	$378,000	SRC
AS	Design and Verification of Analog Integrated Circuits (Pending)	7/1/96-6/30/97		MICRO

TOTAL NUMBER OF PROFESSIONALS

CURRENT - FACULTY:	1 @ 1 week summer
CURRENT - STUDENT:	1 @ 49.9% academic; 100% summer
PROPOSED FACULTY:	1 @ 1 week summer
PROPOSED STUDENTS:	1 @ 49.9% academic; 100% summer

Logic Synthesis for the Nanodevice Era

FACULTY INVESTIGATOR: ALBERTO SANGIOVANNI-VINCENTELLI

SCIENTIFIC OBJECTIVE

The design of a VLSI chip consists of a number of steps. At first, the design is specified at the behavioral level. This is followed by functional partitioning, architectural synthesis, logic synthesis, floorplanning, placement and routing and ends with a detailed specification of the layout mask level geometries. At each of these steps, various optimizations are done (manually or using CAD tools) to minimize area, increase performance or reduce power consumption. Typically, these optimizations proceed as a series of transformations to the design representation which are believed to improve the quality of the overall chip. Incorrect decisions made at a higher level of abstraction may lead the design so far away from the globally optimum solution that the subsequent stages of optimization may never be able to find it. In order to properly guide the optimization process, we need a model of the design which accurately reflects the cost of the final implementation taking into account the effects of subsequent steps of the design.

Optimization of circuits at the logic level to achieve lower area and power and higher performance is a key step in the automatic design of an integrated circuit. This step, known as logic synthesis, can be divided into two distinct phases. The first phase performs technology-independent transformations on the logic equations (which are described as a multilevel network) and the second phase performs technology-dependent mapping to implement the design using gates in the target technology.

Conventionally, logic synthesis has focused on active cells to optimize for area, delay or power and has largely ignored the effects of interconnect. This is mainly because very little information about the interconnect is available at the logic level. Ignoring the layout issues during logic synthesis can lead to designs which are very difficult to route and hence have excessive interconnect area or delay. This problem is becoming more pronounced with the advent of nanodevice processes. The speed of an MOS transistor increases as the dimensions of an MOS transistor shrink. On the other hand, an increased integration level allows the chip area to increase, causing the length of the interconnect to increase. As a consequence, for large chips with extremely small geometries, the time delay associated with the interconnects becomes an appreciable portion of the total time delay and the circuit performance can no longer be decided by the gate performance only. The importance of the problem is captured in Figure 1 where interconnection and gate delay are plotted as a function of time for the largest chip fabricated that year using the state-of-the-art technology. This figure is taken from [12] and the data shown was collected from various publications, conference proceedings, and product announcements by various manufacturers.

In this project, we plan to incorporate interconnect effects during the technology independent phase of logic optimization. As a first step towards this goal we will create a model which can be used to predict the effects of various transformations on the post layout quality of the chip. The measure of quality can be either the total chip area, or the delay or the power consumption.

We will first consider the problem of performance optimization at the logic level. The overall delay of a circuit can be divided into the following two components:

- **active gate delay**
- **interconnect delay**

Most of the present work has focussed on the active gate delays. The two most popular models for the gate delays are: 1) unit-delay model with a unit-fanout term and 2) library model. The unit-

delay model besides being fast to evaluate has little justification. The delay under this model is expressed in arbitrary units making it difficult to relate it to the designer's constraints. Arbitrary units also make it difficult to compare the gate delay with interconnect delay. In the library model, the delay through a node is calculated by mapping it into cells in the target library. While this is more accurate, it takes much longer to run. Since this procedure has to be called many times during the optimization phase it can be prohibitively time consuming. As already mentioned, very little attention has been paid so far towards rigorously modeling the interconnect delay at the logic level.

In this work, we propose to find a more realistic model for the gate delay. We will represent factored form expression for the gate function as an RC interconnect network and calculate its Elmore delay. Each transistor will be replaced by a resistor and a capacitor. For a given technology, the values of these resistors and capacitors will be calculated by using standard statistical regression techniques. Not only will this allow us to model the delay more accurately but also we will get the result in real time units so that it can be compared with the interconnect delay. Further, we will identify the statistically significant parameters which effect the interconnect delay. These parameters will be identified by evaluating the effects of logic independent optimizations on the post layout quality of the chip. Based on these parameters, we will construct an "explicit factor model" for the interconnect delay. The factor model for the interconnect will be combined with the RC interconnect model and will provide the capability to make decisions which involve trade-offs between gate and interconnect delays.

A similar methodology will be used to model the effects of interconnect on the overall chip area and power. We believe that this will be the first attempt which tries to rigorously model the effects of interconnect at the logic level.

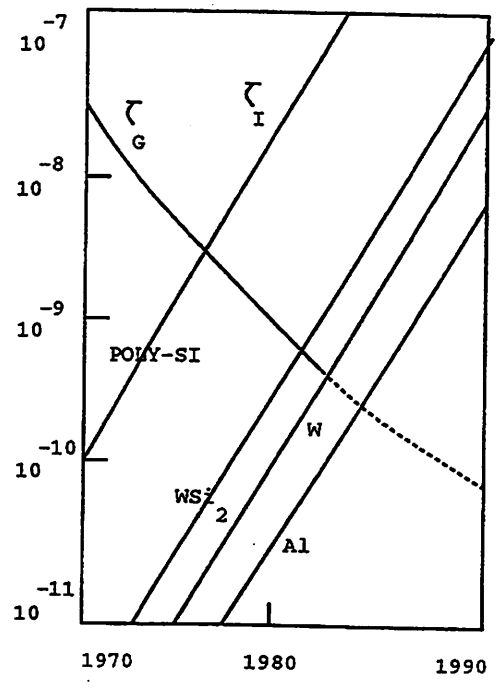

Figure 1. Interconnection time delay and average gate delay versus year of fabrication for the state-of-the-art chip fabricated that year.

STATE-OF-THE-ART

As we mentioned in the previous section, very little work has been done to model the effects of interconnect at the logic level. In this section we briefly review some of the studies that have attempted to incorporate the effects of physical design at logic and higher levels of synthesis.

The high-level layout area and delay estimation techniques can be broadly divided into two categories:

- **analytical**
- **constructive**

In analytical techniques, a mathematical model is used to estimate the layout phase. Constructive models keep a crude placement solution and use that to evaluate the layout cost. Most of the techniques [8], [5], [4], [3] which try to estimate the layout effects deal with datapaths at the register-transfer level. In [8] a bit-slice architecture is assumed to model the datapath. To minimize the overall layout cost, strongly connected blocks are placed in close proximity. A companion placement solution along with an analytical tool is used to estimate the overall floorplan and dimension of the bit-slice. Controller is assumed to have a random logic and the layout cost estimation is done using a companion placement solution. It is recognized that this technique is not very effective for random logic. In [5] analytical formulas based on the connectivity information is used with a companion placement solution to estimate the dimensions of physical layout. They try to model the standard cell methodology by dividing the process in two phases. In the first phase all the cells are placed in a single row. All possible orientations are tried and the one with least connection length is selected. The connection length is calculated by using the connectivity information of different modules. In the second phase, the single row design is folded to get the desired aspect ratio. Additional wiring needed to connect different rows is calculated by using an analytical model. In this technique, a large number of different orientations have to be considered and hence is not practical when the number of components is large as at the logic level. Further, the accuracy of the model goes down as the number of components increases. In [3] propose a probabilistic model for area estimation of VLSI layouts. Based on Rent's rule, a geometric distribution for the wire lengths is assumed. A model is constructed for the standard cell design style and analytical expressions are derived for estimating the layout area. Most of these models are either computationally very intensive and can deal with only a few blocks at the RTL level (and hence not feasible for a large number of gates at the logic level) or make assumptions about the architectures which are not valid in the case of random logic.

At the logic level, attempts have been made to model the effect of layout during both technology independent and technology mapping phases. In [7] a technology mapper, LILY is implemented which takes the interconnect delay into account. The interconnect cost is estimated using a placement solution and is incorporated in the standard tree mapping algorithm. In [9] a fanout optimization algorithm is proposed which maintains the order of the fanouts to simplify routing. This order is generated using a companion solution. An $O(n^3)$ algorithm is proposed which results in an improvement of about 8-14%. A similar idea is used in [1] to minimize routing factor during logic synthesis. The approach is based on lexicographical expression of Boolean function controlling input dependency. In a lexicographic expression, for a given sum of products form, all the literals respect the same order in each product term. Maintaining this order in all expressions results in a simpler layout which takes less area. An average improvement of more than 20% was reported but the experiments were performed only on a few examples. In [6] various algorithms used in conventional logic synthesis like kernel extraction and technology decomposition are modified to incorporate a layout cost factor. This cost factor is evaluated using a companion placement solution and average improvements of about 27% in area and 12% in delay are

reported. In [10] a heuristic to minimize the layout cost is proposed which doesn't employ a companion placement solution. Although impressive gains are reported for some cases, the experiments designed to obtain these are not very realistic. All the input pins are located on one side of the chip and all the output pins are located on the other side of the chip. Their method is based on minimizing the average fanout range and evenly distributing the fanout range throughout the chip. A rigorous analysis of the effect of this cost function on the overall cost is not performed. In [2] an interesting approach of combining logic synthesis and routing is presented for FPGAs. Given a network, redundancy addition/removal techniques are used to identify alternative wires for every wire. Wires which have large number of alternative wires are given lower priority during routing and wires which don't have any alternatives are routed earlier. By combining synthesis and routing in this manner, they are able to complete routing of many circuits for the first time.

PROGRESS SINCE LAST MAJOR PROPOSAL

During this period, progress was made on two fundamental aspects of the research being developed: adaptation of the decision graph algorithms to a more general class of problems and study of alternative approaches for inductive inference in problems that are inherently sequential.

The algorithms developed for the influence of reduced ordered decision graphs from labeled training sets were limited to problems defined by a number of discrete attributes. Problems with continuously valued attributes had to had to be discretized by the user, based on field knowledge or some other approach.

To make sure the decision graph algorithms more general and applicable to a wider range of situations, an effort was developed to study the applicability of algorithms that can be used to discretize continuous features based on a technique that aims at minimizing the resulting entropy proved specially useful to the task at hand [13], and were therefore selected as the discretization algorithms of choice for this task.

An extensive effort was made to characterize the conditions under which inductive learning algorithms based on decision graphs significantly outperform existing alternatives. The results show that this approach is superior in problems where classes are represented by a number of distinct and disconnected regions. A significant fraction of problems are considered hard exactly because they exhibit this characteristic and the application of decision graph based algorithms may significantly improve the state-of-the-art of learning algorithms.

Research on algorithms for inductive inference in problems that are defined by sequences in time was concentrated on the search for more efficient algorithms for exact identification of finite state machines consistent with given samples of input/output behavior. There possible approaches were defined for this problem: algorithms based on explicit search of solution space, algorithms based on implicit search of the solution space, and algorithms that convert the problem in a Boolean satisfiability problem and solve it using existing algorithms for this problem.

The research has shown that algorithms based on explicit search attain basically the same performance as algorithms based on implicit search using Boolean decision diagrams to represent internally a set of possible solutions. A promising approach is the use of zero-suppressed Boolean decision diagrams because this type of representation is more effective for the representation of sparse sets like the ones that correspond to the set of solutions.

The study of implicit approached to the problem has also made clear that there exists a simple transformation of this problem to a Boolean satisfiability problem. This transformation is of interest because highly sophisticated search algorithms have been developed for this problem [14] and it may be possible to use the leverage provided by these results in an attempt to extend the set of problems that can be solved with reasonable computational effort.

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5. M. Chiodo, P. Giusto, A. Jurecska, L. Lavagno, H. Hsieh, K. Suzuki, A. Sangiovanni-Vincentelli and E.M. Sentovich, "Synthesis of Software Programs for Embedded Control Applications," Proceedings of the 32th ACM/IEEE Design Automation Conference, pp. 587-592, San Francisco, CA June 1995.

6. A. Aziz, F. Balarin, M.D. Di Benedetto, R.K. Brayton, A. Saldanha and A. Sangiovanni-Vincentelli, "Supervisory Control of Finite State Machines," Proceedings of Computer-Aided Verification: 7th International Conference, LNCS Vol. 939, Leige, Belguim, July 1995.

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LIST OF TECHNOLOGY TRANSFER SINCE LAST PROPOSAL

Dr. Timothy Ross, with the Pattern Theory Group and Air Force Wright Patterson Laboratories evaluated the performance of the decision graph algorithm developed by Professor Alberto Sangiovanni-Vincentelli's group, and found that it significantly outperformed all tested alternatives in

their benchmark.

PROPOSED RESEARCH PROGRAM

Approach

As a first step towards incorporating interconnect effects during logic synthesis, we will study the performance optimization step. Our approach consists of accurately modeling both the gate as well as the interconnect delay. We propose to do the following in this project

- For a given factored form expression of a node calculate the Elmore delay. This will be done by assuming an underlying transistor level implementation of this expression. This underlying transistor level circuit will be further approximated by an RC-circuit. We will use the standard switch level techniques to estimate the Elmore delay. For a given factored form expression, this delay will be in terms of 'R' and 'C' of a given technology. Values of 'R' and 'C' will be evaluated using standard regression techniques for a given library. We hope that the Elmore delay for a given factored form expression can be done implicitly by just working on the expression and hence will not be prohibitively time consuming. Also, since a more realistic model is being used, it should be more accurate than the unit-delay model. Regression has to be performed only once and hence can be done off-line.
- We will experiment with different technologies and see the percentage of interconnect delay in the overall delay. We will try to identify at what device sizes does the interconnect effect starts to dominate.
- We will identify statistically significant logic level parameters using standard regression techniques and will construct an explicit factor model for the interconnect delay them.
- This model will be incorporated in SIS for logic level performance optimization.

Once the performance optimization phase is thoroughly understood, we will extend the work for minimizing the overall chip area and power. Again, the goal will be to construct a factor model for interconnect effects which could be used in conjunction with the model for active gate area and power. Finally, we will try to identify new layout structures and architectures to minimize interconnects; for example, by limiting connections only between the nearest neighbor as is the case with datapaths.

Expected Results/Impact

At the end of this project, we expect to develop a suite of tools in SIS which incorporate the effects of layout during logic optimization.

We believe that our approach of rigorously modeling the interconnect effects at the logic level will have great impact on the way logic synthesis is done; especially in the submicron era where these effects dominate the total chip area, delay and power.

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UNIVERSITY: UC BEKELEY **LAB: ERL**
JOINT SERVICES ELECTRONICS PROGRAM **RESEARCH UNIT: II-H**
LAST YEAR'S RESEARCH UNIT: II-B

TITLE OF INVESTIGATION: Cellular Neural Network Models and Nonlinear Dynamics of Quantum-Coupled Nanoelectronics

SENIOR INVESTIGATORS: Leon Chua **TELEPHONE:** 510-642-3209

JSEP FUNDS (CURRENT):

PI	TITLE	PERIOD	AMOUNT (1994-1997)
LC	The Cellular Neural Network Universal Machine and Supercomputer	6/94-1/97	$205,970

JSEP FUNDS (PROPOSED):

1997-1998	$75,000
1998-1999	$75,000
1999-2000	$75,000

OTHER FUNDING:

PI	TITLE	PERIOD:	AMOUNT:	SPONSOR:
LC	Nonlinear Circuits and Neural Networks	12/1/88-11/30/97	$2,649,530	ONR
LC	Nonlinear Circuits & Neural Networks (AAsert)	8/1/94-7/31/97	$131,750	ONR
LC	U.S.-Hungary Research on Theory on Analogic Nonlinear Computing Structures	9/1/94-8/31/97	$55,000	NSF
LC	Spread Spectrum Communication Exploiting Chaos (Pending)	4/1/96-3/31/98	$630,000	ONR

TOTAL NUMBER OF PROFESSIONALS

CURRENT - FACULTY:	1 @ 1 week summer
CURRENT - STUDENT:	1 49.9% academic year; 100% summer
PROPOSED FACULTY:	1 @ 1 week summer
PROPOSED STUDENTS:	1 @ 49.9% academic year; 100% summer
	1 @ 49.9% academic year; 100% summer

JUSTIFICATION OF EQUIPMENT:

Equipment: VISUALIZE-48 Accelerated 2D/3D 24/24 bit graphics subsystem including PowerShade graphics and 16MB texture map memory. Estimated cost: $21,000

We request the acquisition of a VISUALIZE-48 high performance graphics subsystem for scientific computation and data visualization. This piece of equipment will be crucial in our investiga-

tion of many types of complex phenomena. Many of our research tasks require simulation of large systems of nonlinear differential equations which needs enormous graphics manipulation power in order to display this large amount of data. We will also need the ability to interactively manipulate system and data display parameters in real-time in order to help us gain valuable insight into the workings of complex electronic systems. This need requires dedicated high-speed 2D/3D graphics hardware and software. The acquisition of the VISUALIZE-48 graphics subsystem will allow us to satisfy many of these needs. Some of the specific projects requiring the computatio0nal and graphical power of this high performance graphics subsystem include studies in spatial-temporal chaos, stability and instability properties of quantum chaos, conditions of sustained generation and propagation of solitons, and fractal and nonlinear dynamics of large-scale electronic circuits and systems. This graphics subsystem will be installed into a HP9000-J210-XC computer which we are planning to acquire using funding from other sources. The HP9000-J210-XC will cost approximately $45,000 and the VISUALIZE-48 subsystem constitutes only a fraction of the cost of the total system. The total value of the complete research equipment is $66,000 and hence JSEP funds are significantly leveraged.

Cellular Neural Network Models and Nonlinear Dynamics of Quantum-Coupled Nanoelectronics

FACULTY INVESTIGATOR: LEON CHUA

SCIENTIFIC OBJECTIVE

Since its inception in 1988 [1], the cellular neural network (CNN) paradigm has been widely applied [2-9] and generalized to many disciplines, including brain science, chemistry, and physics [10]. The CNN paradigm unifies under a single framework the universe of dynamic arrays made of large numbers of simple dynamical units, such as quantum dots, which interact only with their local neighbors. This local interaction may take the form of CMOS transistors as in the CNN universal chip, or chemical neurotransmitters in the synaptic coupling between neurons, or quantum-mechanical coupling between quantum molecules in nanoelectronics. The first objective of our proposed research is to develop a unified CNN methodology for modeling nanoelectronic and molecular arrays in order that local interaction patters which are often too costly if not impossible to study experimentally may be made by programming the CNN universal machine to simulate and validate the local interactions rules for future system level designs.

Nonlinear waves in many bulk materials and active media do not behave like classical waves, such as electromagnetic waves. Rather, they can exhibit many counterintuitive if not bizarre phenomena. For example, two nonlinear waves can collide with each other like solitons without deterioration in shape. Others may annihilate each other upon collision with another nonlinear wave, or with an obstacle. Another important generic phenomenon of a nonlinear wave is its "domino-like" propagation mode. Several recent quantum-dot cellular automata computer architectures are actually based on such a propagating mode through quantum wires. Since the nonlinear dynamics of such triggered waves and its failure modes presently poorly understood, the second objective of our proposed research is to conduct an in-depth investigation of the spatio-temporal dynamics and bifurcation phenomena of nonlinear waves on various active media, including superlattices from nanoelectronics and arrays of excitable neurons.

STATE-OF-THE-ART

While dramatic progress has been made during the past decade in the fabrication of nanostructures and the physics of quantum size (or confinement) effects and the resonant tunneling phenomenon, only single quantum-based devises have so far been successfully built and demonstrated. The weak link in this area is the coupling of such devices into quantum-coupled computing arrays. There are numerous modeling and nonlinear circuit-theoretic issues at both the quantum device level and at the macrosystem level that need to be addressed and satisfactorily resolved before sustained progress is possible. Some of these modeling issues reflect a genuine lack of understanding at the most fundamental circuit-theoretic level. For example, even the classical concepts of a nonlinear resistor, inductor, and capacitor had become ambiguous at the quantum level and must be refined and generalized before it makes sense to talk about nonlinear lumped circuit models and v-i characteristics in nanoelectronics.

At the system level, the most promising system architecture that has been proposed so far coincides with that of the CNN paradigm where a firm nonlinear system-theoretic foundation is available. However, a clear understanding of the many elusive nonlinear dynamical and bifurcation phenomena of patterns and spatio-temporal dynamics remain a fundamental and challenging research problem.

PROGRESS SINCE LAST MAJOR PROPOSAL

We have made excellent research progress on all topics described in our last major proposal, as

well as several unexpected emergent properties of fundamental scientific interest related to the "local interaction" properties of cellular neural networks. Such emergent properties are self-organizing and synergetic in nature, and include, among other yet unexplained phenomena, spatio-temporal patterns, waves and chaos. These collective phenomena are highly relevant to the understanding of the complex but local interactions among quantum-coupled arrays in nanelectroncs. A Special Issue on these phenomena has been published in the IEEE Transactions on Circuits and Systems (October, 1995).

Our research on the CNN universal machine has produced two major breakthroughs since the last major proposal. The first break-through, which demonstrates that the CNN universal machine is a practical method of producing a supercomputer on a chip, had resulted in the award of a U.S. patent (no. 5,355,528 "Reprogrammable CNN & Supercomputer") to L. Chua and his collaborator, T. Roska. The second breakthrough, which provides the theoretical foundation for the capabilities of the CNN universal machine, proves that the CNN is equivalent to the Universal Turing Machine, and thus by Church's thesis, is capable of implementing any algorithm, as well as simulating every finitely realizable physical system.

Not only is the current research in CNN's international in scope, involving active researchers from 22 countries worldwide and 3 biannual IEEE sponsored international workshops devoted exclusively to CNN (held in Budapest, Munich and Rome), it is also multidisciplinary, drawing researches from many fields outside of electrical engineering. One of the inventors of the CNN Bionic Eye, F. Werblin, is a professor in the Molecular Biology Department at Berkeley. Several physicists have also been attracted by the unifying CNN paradigm. For example, Professor. W. Porod has called attention to the relationship between the CNN paradigm and quantum cellular automata, the physics of computing with arrays of quantum dot molecules. Likewise, Dr. G. Mayer-Kress from the University of Illinois Physics Department has applied the CNN paradigm to induce resonant transitions to ordered states in an array of threshold elements that are exponentially coupled to their nearest neighbors.

Our discovery of spatio-temporal chaos has led to an in-depth investigation on the design of basic nonlinear chaotic electronic circuits and their integration into a AVLSI array. We expect these investigations will lead to many novel applications, including the design of secure spread spectrum communication circuits. In such applications, chaos is harnessed, rather than suppressed, and used as the carrier in such novel communication systems.

LIST OF PUBLICATIONS CITING JSEP SPONSORSHIP

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20. L. Kovcarev, C. W. Wu, and L. O. Chua, "Complex Behavior in Digital Filters with Overflow Nonlinearity: Analytical Results," IEEE Transactions on Circuits and Systems, Part II: Analog and

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LIST OF TECHNOLOGY TRANSFER SINCE LAST PROPOSAL

Attracted by the 3 order-of-magnitude speed advantage, and the extreme low-power requirements of the CNN universal chip over conventional DSP and ASIC implementations, several high-tech companies are presently considering using CNN universal chips in their future product lines. One of these companies is:

VSLI Technology (San Jose California)

Mr. Herb Reiter, business manager from VLSI has been actively seeking business relationships with several high-tech companies for the purpose of manufacturing and distributing CNN universal chips to these companies who needed the speed and power advantages of the CNN.

PROPOSED RESEARCH PROGRAM

Approach

We will exploit the central principle of the CNN paradigm which asserts that the emergent complex behaviors of many unrelated physical and natural systems made of locally-interacting dynamical units can be analyzed, explained, and controlled via self-organization and synergetics. In particular, a homogeneous array, such as a bulk semiconductor, can self-organize via bifurcation dynamics and symmetry breaking, into *patterns, nonlinear waves,* and *spatio-temporal* chaos.

Pattern Formation is an ubiquitous phenomenon that can occur at both quantum scale level as well as at the macro scale level. For example, in a bulk material whose atoms behave magnetically via quantum-mechanical spins, the *local interaction* between neighboring atomic structures can align the magnetic moments in the same direction, resulting in ferromagnetism, or in the opposite direction, resulting in antiferromagnetism. An entirely similar phenomenon can lead to a spontaneous polarization of electronic charge in a quantum dot array. For example, in a CNN array of "quantum dashes", the Coulomb force between electrons in neighboring dashes can overcome the restoring force along the dash, thereby producing a net dipole moment in each dash and the minimum energy state for such an array is achieved by a spontaneous transition to an anti-ferroelectric arrangement [11-12]. In this case, the Lyapunov function associated with a completely stable CNN can be identified as the energy function whose Eulerian derivative along trajectories is negative definite except at local extrema. Other CNN arrays can give rise to many exotic Turing patterns widely observed in diverse active media endowed with two diffusion mechanisms, on excitatory, the other inhibitory [13-14]. We have developed during the last 3 years a unified CNN paradigm of pattern formation which we believe can be used to explain such quantum phenomenon as "frustration" in spin glasses and defects and dislocations in solid state materials. It may even be possible to control the defects in crystals by applying an appropriate input pulse at the outer edge of crystals.

Nonlinear trigger waves and spatio-temporal chaos are robust dynamical phenomena widely observed in active media which are open thermodynamic systems operating far from equilibrium [15-17]. The distinction between an active media and a passive media is that the former requires an external power supply. For example, in the brain, the active medium is provided by a sheet-like array of massively interconnected excitable neurons whose energy comes from the burning of

glucose with oxygen. In cellular neural network chips, the active medium is provided by the local interconnections of active cells, whose building blocks include active nonlinear devices (e.g., CMOS transistors) powered by dc batteries. The intricate interplay between the dissipative and the locally unstable nonlinear dynamics can, under appropriate parametric and boundary conditions, give rise to auto waves, spiral waves, scroll waves, and even spatio-temporal chaos in such active media, including semiconductor nanostructures and superlattices. For example, in lateral surface superlattices the 2-dimensional potential induced by the charge carriers could lead to a chaotic behavior in the ballistic motion of the charged carriers. In this case the chaotic particle dynamics is an anomalous diffusion process associated with 1/f-noise in the current fluctuation. Using the theory of nonlinear dynamics, we can explain and even predict this chaotic behavior by showing the existence of a self-similar hierarchy of broken KAM-tori with a Cantor set structure, usually referred to as Cantori in the physics literature.

As an application of the CNN paradigm, we will develop a CNN model of the quantum cellular automata architecture proposed in [18-19]. We will also develop CNN models for simulating the various relevant partial differential equations essential to a full numerical analysis of mesoscopic systems from first principles in quantum device physics.

So far, all proposed quantum array computers are based on the ground state or equilibrium state of quantum molecules. Since ultimate supercomputers will not likely exploit the infinitely richer dynamics of oscillatory and chaotic attractors, we will begin a modest but focused research on the application of chaotic attractors to both computing and communication systems, including secure communicaiton systems.

Expected Result/Impact

We believe our research during the next three years will contribute toward a much more rigorous and systematic approach to real-time parallel computing in general, and to quantum automata architecture in particular. We expect to derive the local interaction patterns in terms of quantum cell parameters. These patterns will then be translated into a family of CNN templates to be used by future system designers as subroutines in dedicated analogic programs. We hope that our long standing expertise on device modeling [20], negative resistance devices [21], and nonlinear dynamics [22] will provide the right backgrounds and synergisms for merging the physics of nanostructures and the theory of nonlinear dynamics in our future CNN models of quantum coupled nanoelecronics. Finally, we are confident of developing a self-consistent and axiomatic definition of nonlinear circuit elements which are relevant for modeling quantum dot devices. All of these results, along with a deeper understanding of the pattern formation, waves, and spatio-temporal dynamics will help strengthen the weak link cited earlier.

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UNIVERSITY: UC BEKELEY **LAB:ERL**
JOINT SERVICES ELECTRONICS PROGRAM **RESEARCH UNIT: II-I**
LAST YEAR'S RESEARCH UNIT: N/A

TITLE OF INVESTIGATION: QUANTIUM MECHANICS AND DNA: Exploring Two Novel Bases for Computation

SENIOR INVESTIGATORS: Umesh Vazirani, Christos Papadimitriou **TELEPHONE:**(510)642-0572

JSEP FUNDS (CURRENT):

PI	TITLE	PERIOD	AMOUNT (1994-1997)
UV	NONE		
CP	NONE		

JSEP FUNDS (PROPOSED):

1997-1998	$85,000
1998-1999	$85,000
1999-2000	$85,000

OTHER FUNDING:

PI	TITLE	PERIOD:	AMOUNT:	SPONSOR:
CP	Research in Algorithm, Complexity	7/1/96-6/30/99	$255,000	NSF
UV	A Proposal for Research on Randomized Algorithms, Complexity Theory and Quantum Computers	8/15/93-7/31/96	$162,000	NSF
UV	The Information Superhighway and the Decentralization of Organizations	8/15/95	$19,694	NSF

TOTAL NUMBER OF PROFESSIONALS

CURRENT - FACULTY: New work unit proposed.
CURRENT - STUDENT: New work unit proposed.

PROPOSED FACULTY: 2 @ 1 week summer (each)
PROPOSED STUDENTS: 2 @ 49% academic; 100% summer

QUANTUM MECHANICS AND DNA: Exploring Two Novel Bases for Computation

FACULTY INVESTIGATORS UMESH VAZIRANI, CHRISTOS PAPADIMITRIOU

SCIENTIFIC OBJECTIVES

In the half century since the first computers we have seen tremendous conceptual and technological improvements and breakthroughs in device physics, engineering, manufacturing, architecture, and software. However, throughout its modern history, computation has been based on a single medium and principle: Electronic circuitry obeying the laws of classical physics. Now two very recent and intriguing proposals challenge for the first time directly, credibly, and fundamentally this medium as the sole basis of computation: *Quantum computation,* departing from a suggestion by Richard Feynman [16], explores the theoretical advantages and technical feasibility of computation based on quantum mechanical principles. *DNA computation,* based on an idea of Adleman [1], further developed by Lipton [20], suggests that the Watson-Crick dioxyribonucleic acid, the medium whereby genetic information is stored, can be the basis of parallel computation at a scale (and energy parsimony) far beyond the potential of any other medium currently considered.[1] The plausibility and importance of both media has been demonstrated by developing algorithmic techniques that take advantage of their novel features to solve in principle certain important computational problems that had been beyond the reach of conventional computers (in the case of quantum computation, factoring integers[24], in the case of DNA computation, the Hamilton cycle problem [1] and other NP-hard problems [20].

The objective of this unit is to explore the potential and limitations of these two novel media, and to address two issues that we believe are of central importance to both: First, certain problems (such as noise and experimental errors) that lie in the path of their practical implementation; and second, to investigate new important applications for these media, beyond the severely restricted initial advances. For *quantum computation* we shall study certain new approaches to the problem of *decoherence*, the quantum mechanical interaction of the quantum computer with its environment that can have deleterious effects on the computation. We shall also explore applications of quantum computers beyond the number-theoretic ones studied so far; in particular, we shall investigate *vis a vis* quantum algorithms two central computational problems: finding shortest vectors in lattices, and computing the permanent of a matrix.

For *DNA computation* we shall address three central issues: (a) the problem of *errors* in biological experiments that may pollute and stymie computations; (b) *extracting parallelism* from DNA computations by identifying biological steps that may be executed concurrently; and (c) developing DNA-based optimization techniques for large-scale combinatorial optimization problems.

STATE OF THE ART

Quantum Computation. A great deal of interest has been generated by results in a new area called *quantum computation.* Computations obeying quantum-mechanical laws can be formalized in terms of a new model, the quantum Turing machine [14]. There is now strong evidence that quantum Turing machines represent an inherently new and more powerful model of computation [6, 26, 24].

There have been three main areas of theoretical work on quantum computation. The first area deals with formally defining quantum computers and how to program them. Early work in this area was done by Feynman [16] and by Deutsch [14]. A complexity theoretic approach was taken

1. Interestingly, DNA computation can also be seen as a response to another idea tossed by Richard Feynman [17}, namely that of computing in terms of molecular-level devices.

by Bernstein and Vazirani [6]. They showed that any quantum Turing machine can be efficiently simulated by a particular quantum Turing machine (a *Universal QTM*) which may be described as a deterministic Turing Machine augmented with a certain quantum coin-flip. They also showed that the complex number required to specify the quantum coin-flip may only be accurate to O(log *T*) bits of precision to correctly simulate *T* steps of the machine. This establishes the discrete nature of these machines. The results of Bernstein and Vazirani were limited to Deutsch's original definition of quantum Turing machine. Yao [28] later generalized these results, and established the equivalence of quantum Turing machines and quantum circuits. Two subsequent papers [2, 27] showed that the quantum coin-flips in the universal quantum Turing machines can be assumed to have a particularly simple form.

A second area considers the computational power of quantum Turing machines. The class of interest here is *BQP*, which is the set of languages recognized in polynomial time and with bounded error on a quantum Turing machine. It was proved in [6] that $BQP \subseteq PSPACE$, and therefore proving that *BQP* is strictly larger than *BPP* would resolve a long-standing open problem in complexity theory. They also showed that relative to an oracle, *BQP* is strictly larger than *BPP*. This result was improved by Simon [26] who showed that relative to an oracle there is a problem in *BQP* that requires exponential time on a probabilistic Turing machine.

Then Shor [24] proved a remarkable result; he showed that *prime factorization* and *discrete logarithm* can both be solved in polynomial time on a quantum Turing machine. Since the intractability of these two problems forms the basis of modern cryptography, whether or not quantum computation can be realized in practice has taken on a great deal of practical significance. It is natural to ask whether every problem in *NP* (and beyond) has a polynomial time quantum algorithm. Evidence to the contrary is presented in [5], where it is shown that relative to a random oracle, $NP \not\subseteq BQP$. The actual result is stronger and says that relative to a random oracle, quantum computation does not help by more than a quadratic factor over the straightforward exponential time simulation of *NP*. In a matching result, Grover [18] showed that a quadratic speedup can be obtained on a quantum Turing Machine for every *NP* problem.

The third area considers the problems of *noise* and *decoherence*, which are serious obstacles to the actual realization of quantum computers. A paper by Berthiaume, Deutsch and Jozsa [8] shows how to use the quantum watchdog effect to compute in the presence of coherent noise. Ideally we would like to design algorithms that are robust in the sense that they should compute correctly even if the system decoheres at some constant rate. Recently, there was an important breakthrough that probably has some implications for this issue. A paper of Shor [26] describes how to store an arbitrary state of n qubits using $9n$ qubits in a decoherence-resistance way. A generalization of this paper describes more general quantum codes [12].

Finally, a number of groups are actually working on realizing quantum computers in the laboratory. This includes Chirac and Zoller in Europe, Richard Hughes at the Los Altos Labs, and Kimble at Caltech.

DNA Computation. Adleman in [1] envisioned the tremendous level of parallelism that can be achieved in principle by DNA computation, and demonstrated the feasibility of DNA computation by actually solving a toy 7-node Hamilton cycle problem in the biology laboratory. Lipton [20] abstracted DNA computations in terms of three basic operations that can be performed on DNA test tubes: *extract* (use biotin-avidin affinity purification to find all DNA strands in a given test tube containing a pattern that encodes a Boolean value such as *x=1*), *merge* (mix together two test tubes), and *detect* (see if any strand is present in the test tube). Another useful operation is *length* (sort all strands in a test tube by increasing length using gel electrophoresis). He also demonstrated that DNA can be employed usefully to solve arbitrary NP-complete problems; this

was subsequently extended in various directions [21, 23, 22].

Much recent work [20, 9, 10] has explored the power of DNA computation to solve hard decision and optimization problems, including the *data encryption standard* [9]. The basic technique employed has been brute-force enumeration, exploiting the model's parallelism. Two exceptions are recent work by [13], which develops less than exhaustive techniques, and by [22] where DNA's potential for simulating more general parallel computation is explored. There has also been much work on identifying more complex biological steps that can be performed on test tubes [4, 11, 22], including complex techniques involving *DNA recombination.* [22].

One important issue that may inhibit the practical implementation of the DNA idea is the presence of *errors* in biological experiments. This problem, already anticipated in [1], was addressed in [19] by showing how the (most error-prone) *extract* operation can be made optimally reliable, and in [11] where errors are remedied by periodically boosting the contents of the test tube.

PROGRESS SINCE LAST MAJOR PROPOSAL

N/A (New work unit proposed.)

LIST OF PUBLICATIONS CITING JSEP SPONSORSHIP SINCE LAST PROPOSAL

N/A (New work unit proposed.)

LIST OF PUBLICATIONS UNDER OTHER SPONSORSHIP WHICH ARE RELATED TO WORK UNIT

1. E. Bernstein, U. Vazirani, "Quantum Complexity Theory" invited to special issue of Siam J. Comp. on quantum computation.

2. C. Bennett, E. Bernstein, G. Brassard, U. Vazirani, "Strengths and weaknesses of quantum computation" invited to special issue of Siam J. Comp. on quantum computation.

LIST OF TECHNOLOGY TRANSFER

None

PROPOSED RESEARCH PROGRAM

Approach

Both novel bases for computation that we are pursuing are at a tender and crucial stage of development. Their plausibility must certainly be pursued in the laboratory. But a perhaps even more challenging and important research direction is the development of the new principles and algorithmic ways of thinking that will harness their tremendous capabilities and will address the problems facing them. We are proposing to do such theoretical work on both topics. We intend to use computer simulations to validate our theoretical results whenever such validation is needed.

Quantum Computing

What is it about quantum mechanics that yields a new computational paradigm? Here is an intuitive explanation: in quantum mechanics, just describing a system of n particles, each of which can be in one of two states, requires 2^n complex numbers. Moreover, the time evolution of the system is described by the updating of the 2^n complex numbers according to a certain differential equation. This opens up the possibility of using a system consisting of n particles to perform an exponentially long computation in time proportional to n. Considering the fact that 2^n is larger than the number of particles in the visible universe even for $n = 200$, this gives the potential for an entirely new paradigm for computing.

In our research on quantum computing we propose to tackle two issues:

1. At present, we do not understand the power of quantum computers very well. We know that

quantum computers can solve two very basic number theoretic problems. Are there other problems that are not known to be efficiently solvable on classical computers that can be efficiently solved on quantum computers? At present, all non-trivial quantum algorithms use the ability of quantum computers to compute large Fourier transforms. This was the case in Shor's algorithms as well as the earlier algorithms of Bernstein and Vazirani, and Simon. Can we extend this ability of quantum computers and use it to solve other problems? We propose to study two specific computational problems. The first is the *shortest lattice vector* problem -given an integer lattic, find the lattice point closest to the origin. The second is the *permanent* -given a bipartite graph, estimate the number of perfect matchings in the graph. Both problems have numerous applications, and have been extensively studied from the point of view of classical computation. In the case of the second problem, it would be interesting to see if there are any techniques involving "negative probabilities" to solve this problem.

2. *Noise and decoherence* are serious obstacles to the actual implementation of quantum computers. Even the decoherence of a single bit during a crucial part of the computation can be fatal to the correct functioning of a quantum algorithm. There are two approaches to these problems. One approach is to isolate the quantum computer from the environment, so that a large number of steps of the quantum computer are possible before any decoherence actually takes place. The other approach is to modify the quantum algorithms in such a way that they are resistant to a certain rate of decoherence. The analogue of this approach was taken in the context of classical computation in the work of von Neumann on reliable computation. A first step towards realizing such a scheme was taken by Shor, in his work on decoherence resistant quantum memory. We have preliminary results which give a different way for achieving quantum codes than the work of Calderbank and Shor [12]. We are now trying to apply these results to the larger problem of carrying out quantum computation reliably in the presence of decoherence. In particular, we propose to show that there is a robust form of the quantum factoring algorithm that is decoherence resistant.

DNA Computation

Another approach to building faster computers is, of course, *massive parallelism*. However, current technology and physical constraints put a limit to the number of such devices that can be usefully deployed to a number well below, say, 10^{10}. Molecular-level computation, as implemented by DNA [1, 20], presents the potential of a level of parallelism well beyond 10^{20}, a level not envisioned in any other plausible context ---except, of course, quantum computation.

Such extreme parallelism comes with certain major restrictions. There can be very limited communication between processors (i.e., DNA strands). There is no input-output to speak of. And, more severely, computation steps are many orders of magnitude slower than conventional computers: For example, adding two eight-bit numbers may take days to carry out, as it involves dozens of time-consuming *extract* operations. (Still, the product of this extremely slow computer by 10^{20} can make for a very attractive speed.) Furthermore, errors in biological processes may cause the computation to degenerate and fail. Much conceptual algorithmic work remains to be done in order to surmount these obstacles and to make DNA computation a plausible alternative in a broad variety of applications and contexts.

Expected Results/Impact

We plan to address the following research problems:

1. The work in [19] has showed how the unreliability of the *extract* operation can be *optimally* enhanced; this enhancement is *modular*, in that it improves the reliability of each operation separately. An alternative way, involving a potentially expensive *boosting* operation that must be car-

ried out periodically, has been proposed in [11]. We intend to further improve our understanding of the reliability issue by developing *non-modular* techniques, which exploit the structure of DNA computations to enhance the reliability of the whole computation -we already have some promising initial results and ideas (this is very analogous to, but technically very different from, our research effort regarding decoherence in quantum computation described above). We shall also try to improve our method by exploiting the fact that *extract* can be two-sided, removing strands that correspond to both Boolean values.

2. There are several possible technological remedies for the slow speed of DNA computers, as currently conceived. First, the time estimates are based on current laboratory technology; however, this technology was developed with different applications and performance measures in mind. It is possible that, motivated by the specter of DNA computation, researchers in biotechnology will discover ways to speed up considerably the laboratory experiments that are critical to DNA computation. More importantly, DNA computations may not be carried out by hand in conventional biology laboratories, but by highly automated, intelligent, and programmable *robotic systems* (the rudiments of such technology already exists and has been deployed in biology laboratories). One of the important opportunities presented by such a robotic system would be to *parallelize* the sequence of biology experiments that have to be performed, by carrying out many non-interfering experiments concurrently. Since the 1960's, there has been extensive work by computer scientists on *extracting parallelism* from computation. For example, we now have much insight (although no totally general solutions) on how to parallelize numerical programs and Boolean functions. However, DNA computations exhibit a different (and, for the most part, much more restricted) potential for parallelism. For example, in simulations of Boolean formulae and circuits by DNA computations [20,10], only the subcircuits feeding OR gates can be parallelized -AND gates are sequential. As a result, the depth of a circuit is no longer a measure of its parallel complexity. We propose to develop the theoretical understanding of how to optimally parallelize formulae, circuits and other genres of algorithms in the context of DNA computations.

3. Most applications of DNA computation that have been proposed so far exploit the parallelism of DNA to exhaustively solve exactly hard combinatorial problems. The instances solvable by such approaches are limited, under favorable assumptions, by at most 70 Boolean variables. In [13] more intelligent than purely exhaustive, but still exact and exponentially slow algorithms, are considered; this stretches the limits to perhaps 100 or at most 200. On the other hand, we would like to solve combinatorial optimization problem instances ranging in the many hundreds and thousands. Such problems are currently attacked by heuristic techniques such as simulated annealing. We have some interesting ideas on how to exploit the massive parallelism of DNA computations to render such heuristics much more effective and potent, applicable to instances of size in the thousands. One particularly interesting genre of heuristics in this context are the so-called *go with the winners* algorithms [3], in which parallelism is a prime feature. We plan to do research on the major technical issues that must be settled for such an approach to become viable.

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ANNUAL BUDGET SUMMARY BY RESEARCH AREA AND WORK UNIT

RESEARCH AREA I:

WORK UNIT A	Silicon MOSFET Scaling Limits for Low Power Electronics	Hu	$95,000
WORK UNIT B	Ultrafast High Field Response in Semiconductors	Bokor	$100,328
WORK UNIT C	Subsurface Electronic Material Synthesis with Plasma Implantation	Hu/Cheung	$82,000
WORK UNIT D	Wavelength Translation Via Four-Wave Mixing in Resonantly Enhanced Well Laser Diodes	Lau	$100,000
WORK UNIT E	Single Transverse Vertical Cavity Surface Emitting Laser	Chang	$100,000
WORK UNIT F	Synthesis and Characterization of GaN Based Heterostructures	Weber/ Cheung	$100,000
	SUBTOTAL:		**$577,000**

RESEACH AREA II:

WORK UNIT G	Logic Synthesis for the SubMicron Era	SanGiovanni	$65,000
WORK UNIT H	Cellular Neural Network and Nonlinear Dynamics of Quantum Coupled Nanoelectronics	Chua	$75,000
WORK UNIT I	QUANTUM MECHANICS AND DNA: Exploring Two Novel Bases for Computation	Vazirani/ Papadimitriou	$85,000
	SUBTOTAL:		**$225,000**

TOTAL YEAR 1: **$802,328**

TOTAL THREE YEAR CONTRACT: **$2,410,206**

BUDGET SHEET 2/97 - 1/98

Title: Renewal of the Joint Services Electronics Program's Support of the Basic Research Program of ERL

Principal Investigator: Jeffrey Bokor; Co-Principal Investigator: Diogenes Angelakos

									Subtotal	Total
I. PERSONNEL: *										
A. Faculty										
Prof IV o/s Bokor	1	fac @	1	summer mth @	50.00%	@	10;585	per month	5,292	
Prof II Cheung	1	fac @	1	summer mth @	25.00%	@	8,066	per month	2,016	
Prof VIII Chua	1	fac @	1	summer mth @	25.00%	@	12,898	per month	3,224	
Prov VII Hu	1	fac @	1	summer mth @	25.00%	@	11,417	per month	2,854	
Prof V Lau	1	fac @	1	summer mth @	25.00%	@	9,892	per month	2,473	
Assoc Prof I Vasirani	1	fac @	1	summer mth @	25.00%	@	7,812	per month	1,953	
Professor VIII Papadimitriou	1	fac @	1	summer mth @	25.00%	@	13,693	per month	3,423	
Prof VIII Sangiovanni	1	fac @	1	summer mth @	25.00%	@	12,898	per month	3,224	
Prof II Weber	1	fac @	1	summer mth @	25.00%	@	8,320	per month	2,080	
Prof I o/s Chang-Hasnain	1	fac @	1	summer mth @	25.00%	@	7,950	per month	1,988	
										28,527
B. Grad. Stud. Researcher	14	stud. @	9	months @	49.00%	@	2,690	per month	166,081	
	14	stud @	3	months @	93.00%	@	2,690	per month	105,071	
										271,152
F. Admin. Support										
AAA III	1	staff @	11	months @	50.00%	@	2,583	per month	14,207	
	1	staff @	1	months @	50.00%	@	2,686	per month	1,343	15,550
Admin. Assist II	1	staff @	11	months @	60.00%	@	2,212	per month	14,599	
	1	staff @	1	months @	60.00%	@	2,300	per month	1,380	15,979
Analyst	1	staff @	11	months @	2.50%	@	3,583	per month	985	
	1	staff @	1	months @	2.50%	@	3,733	per month	93	1,078
										32,607
									TOTAL PERSONNEL	**332,286**
II. BENEFITS:										
A. Faculty			9.10%		of		28,527		2,596	2,596
B. Grad. Stud.										
Worker's Compensation	14	stud	Acad Year		1.30%	of	166,081		2,159	
	14	stud	Sum Appt		2.90%	of	105,071		3,047	
**Graduate Stu Health Ins.	14	stud	Spring				234		3,276	
	14	stud	Fall				234		3,276	
**Tuition fee remission	14	stud	Spring				1,978		27,696	
	14	stud	Fall				1,978		27,696	
**Nonresident tuition fee	3	stud. @	2	semesters @			3,850		23,097	
										90,246
C. Administrative Staff					24.50%	of	32,607		7,989	7,989
									TOTAL BENEFITS	**100,831**
TOTAL PERSONNEL COSTS:										**433,117**
III. PERMANENT EQUIPMENT:										
Visual High Performance Graphics Workstation									21,000	
									TOTAL EQUIPMENT	**21,000**
IV. TRAVEL:										
Domestic: to participate in technical									8,750	

BUDGET SHEET 2/97 - 1/98

Title: Renewal of the Joint Services Electronics Program's Support of the Basic Research Program of ERL

Principal Investigator: Jeffrey Bokor; Co-Principal Investigator: Diogenes Angelakos

	Subtotal	Total
meetings related to proposed research		
5 Trips @ $1750: (R/T East Coast airfare @$1200		
ground transp. $60, per diem for four days $190		
registration fee $300)		
TOTAL TRAVEL		**8,750**

V. OTHER DIRECT COSTS:

Microfabrication Laboratory Services							
Access Charge	13 users @	12	months @	79.90	per month	12,464	
Average Usage	13 users @	12	months @	444.00	per month	69,264	
Office (telephone, mailing, reprographic services)						1,885	1,885
Miscellaneous expendable research supplies						5,450	5,450
Machine Shop		130	hours @	51.00	per hour	6,630	6,630
Publication Costs						1,892	1,892
Computer Services							
Network Access Fee	15 users	12	months @	15.00	per month	2,700	
Labor/parts/vrs exp/Diva	4 wrkstn.	12	months @	109.00	per month	5,232	7,932
Computer Supplies						3,400	3,400
TOTAL OTHER COSTS							**108,917**

TOTAL DIRECT COSTS:	**571,784**

VI. INDIRECT COSTS:

(49.90% of 465,744)	**230,544**

TOTAL BUDGET:	**802,328**

* All salaries and wages are based on current rates with 4% cost-of-living raise effective 1/1/97. Selected faculty merit increases are budgeted at 5%.

** Graduate student health insurance , Tuition fee remission and Nonresident Tuition Remission fees are overhead exempt.

BUDGET SHEET 2/98 - 1/99

Title: Renewal of the Joint Services Electronics Program's Support of the Basic Research Program of ERL

Principal Investigator: Jeffrey Bokor; Co-Principal Investigator: Diogenes Angelakos

									Subtotal	Total
I. PERSONNEL: *										
A. Faculty										
Prof IV o/s Bokor	1	fac @	1 summer mth @	50.00%	@	11,559	per month	5,779		
Prof II Cheung	1	fac @	1 summer mth @	25.00%	@	8,388	per month	2,097		
Prof VIII Chua	1	fac @	1 summer mth @	25.00%	@	12,922	per month	3,231		
Prov VII Hu	1	fac @	1 summer mth @	25.00%	@	12,467	per month	3,117		
Prof V Lau	1	fac @	1 summer mth @	25.00%	@	10,287	per month	2,572		
Assoc Prof I Vasirani	1	fac @	1 summer mth @	25.00%	@	8,124	per month	2,031		
Professor VIII Papadimitriou	1	fac @	1 summer mth @	25.00%	@	14,241	per month	3,560		
Prof VIII Sangiovanni	1	fac @	1 summer mth @	25.00%	@	13,413	per month	3,353		
Prof II Weber	1	fac @	1 summer mth @	25.00%	@	8,653	per month	2,163		
Prof I o/s Chang-Hasnain	1	fac @	1 summer mth @	25.00%	@	8,268	per month	2,067		
										29,970
B. Grad. Stud. Researcher	14	stud. @	9	months @	49.00%	@	2,798	per month	172,724	
	14	stud @	3	months @	93.00%	@	2,798	per month	109,274	
										281,998
F. Admin. Support										
AAA III	1	staff @	11	months @	50.00%	@	2,690	per month	14,798	
	1	staff @	1	months @	50.00%	@	2,798	per month	1,399	16,197
Admin. Assist II	1	staff @	11	months @	60.00%	@	2,300	per month	15,183	
	1	staff @	1	months @	60.00%	@	2,392	per month	1,435	16,618
Analyst	1	staff @	11	months @	2.50%	@	3,726	per month	1,025	
	1	staff @	1	months @	2.50%	@	3,883	per month	97	1,122
										33,937
									TOTAL PERSONNEL	**345,905**
II. BENEFITS:										
A. Faculty			9.10%		of	29,970			2,727	2,727
B. Grad. Stud.										
Worker's Compensation	14	stud	Acad Year	1.30%	of	172,724			2,245	
	14	stud	Sum Appt	2.90%	of	109,274			3,169	
**Graduate Stu Health Ins.	14	stud	Spring			252			3,522	
	14	stud	Fall			252			3,522	
**Tutition fee remission	14	stud	Spring			2,176			30,465	
	14	stud	Fall			2,176			30,465	
**Nonresident tuition fee	3	stud. @	2 semesters @			4,234			25,407	
										98,795
C. Administrative Staff				24.50%	of	33,937			8,315	8,315
									TOTAL BENEFITS	**109,837**
TOTAL PERSONNEL COSTS:										**455,742**
III. PERMANENT EQUIPMENT:										
									TOTAL EQUIPMENT	**0**
IV. TRAVEL:										
Domestic: to participate in technical									8,930	
meetings related to proposed research										

BUDGET SHEET 2/98 - 1/99

Title: Renewal of the Joint Services Electronics Program's Support of the Basic Research Program of ERL

Principal Investigator: Jeffrey Bokor; Co-Principal Investigator: Diogenes Angelakos

	Subtotal	Total
5 Trips @ $1786: (R/T East Coast airfare @$1225		
ground transp. $60, per diem for four days $201		
registration fee $300)		
TOTAL TRAVEL		**8,930**

V. OTHER DIRECT COSTS:

Microfabrication Laboratory Services						
Access Charge	12 users @	12 months @	79.90	per month	11,506	
Average Usage	12 users @	12 months @	444.00	per month	63,936	
Office (telephone, mailing, reprographic services)					1,885	1,885
Miscellaneous expendable research supplies					6,500	6,500
Machine Shop	130 hours @		51.00	per hour	6,630	6,630
Publication Costs					892	892
Computer Services						
Network Access Fee	16 users	12 months @	15.00	per month	2,880	
Labor/parts/vrs exp/Diva	4 wrkstn.	12 months @	109.00	per month	5,232	8,112
Computer Supplies					3,200	3,200
TOTAL OTHER COSTS						**102,661**

TOTAL DIRECT COSTS:	**567,333**

VI. INDIRECT COSTS:

(49.90% of 473,952)	**234,607**
TOTAL BUDGET:	**801,940**

* All salaries and wages are based on current rates with 4% cost-of-living raise effective 1/1/97. Selected faculty merit increases are budgeted at 5%.

** Graduate student health insurance, tuition fee remission and Nonresident Tutition Remission are overhead exempt.

BUDGET SHEET 2/99 - 1/2000

Title: Renewal of the Joint Services Electronics Program's Support of the Basic Research Program of ERL

Principal Investigator: Jeffrey Bokor; Co-Principal Investigator: Diogenes Angelakos

									Subtotal	Total
I. PERSONNEL: *										
A. Faculty										
Prof IV o/s Bokor	1	fac @	1	summer mth @	50.00%	@	12,021	per month	6,011	
Prof II Cheung	1	fac @	1	summer mth @	25.00%	@	9,160	per month	2,290	
Prof VIII Chua	1	fac @	1	summer mth @	25.00%	@	13,950	per month	3,488	
Prov VII Hu	1	fac @	1	summer mth @	25.00%	@	12,966	per month	3,241	
Prof V Lau	1	fac @	1	summer mth @	25.00%	@	11,234	per month	2,808	
Assoc Prof I Vasirani	1	fac @	1	summer mth @	25.00%	@	8,871	per month	2,218	
Professor VIII Papadimitriou	1	fac @	1	summer mth @	25.00%	@	15,551	per month	3,888	
Prof VIII Sangiovanni	1	fac @	1	summer mth @	25.00%	@	13,950	per month	3,488	
Prof II Weber	1	fac @	1	summer mth @	25.00%	@	9,449	per month	2,362	
Prof I o/s Chang-Hasnain	1	fac @	1	summer mth @	25.00%	@	9,029	per month	2,257	
										32,051
B. Grad. Stud. Researcher	14	stud. @	9	months @	49.00%	@	2,910	per month	179,633	
	14	stud @	3	months @	93.00%	@	2,910	per month	113,645	
										293,278
F. Admin. Support										
AAA III	1	staff @	11	months @	50.00%	@	2,798	per month	15,390	
	1	staff @	1	months @	50.00%	@	3,026	per month	1,513	16,903
Admin. Assist II	1	staff @	11	months @	60.00%	@	2,392	per month	15,790	
	1	staff @	1	months @	60.00%	@	2,588	per month	1,553	17,343
Analyst	1	staff @	11	months @	2.50%	@	3,875	per month	1,066	
	1	staff @	1	months @	2.50%	@	4,191	per month	105	1,171
										35,417
									TOTAL PERSONNEL	**360,746**
II. BENEFITS:										
A. Faculty				9.10%		of	32,051		2,917	2,917
B. Grad. Stud.										
Worker's Compensation	14	stud	Acad Year		1.30%	of	179,633		2,335	
	14	stud	Sum Appt		2.90%	of	113,645		3,296	
**Graduate Stu Health Ins.	14	stud	Spring				292		4,093	
	14	stud	Fall				292		4,093	
**Tuition fee remission	14	stud	Spring				2,394		33,512	
	14	stud	Fall				2,394		33,512	
**Nonresident tuition fee	3	stud. @	2	semesters @			4,658		27,947	
										108,788
C. Administrative Staff					24.50%	of	35,417		8,677	8,677
									TOTAL BENEFITS	**120,382**
TOTAL PERSONNEL COSTS:										**481,128**
III. PERMANENT EQUIPMENT:										
									TOTAL EQUIPMENT	**0**
IV. TRAVEL:										
Domestic: to participate in technical									8,930	
meetings related to proposed research										
5 Trips @ $1786: (R/T East Coast airfare @$1225										
ground transp. $60, per diem for four days $201										
registration fee $300)										

BUDGET SHEET 2/99 - 1/2000

Title: Renewal of the Joint Services Electronics Program's Support of the Basic Research Program of ERL

Principal Investigator: Jeffrey Bokor; Co-Principal Investigator: Diogenes Angelakos

						Subtotal	Total
					TOTAL TRAVEL		8,930
V. OTHER DIRECT COSTS:							
Microfabrication Laboratory Services							
Access Charge	11 users @	12	months @	79.90	per month	10,547	
Average Usage	11 users @	12	months @	380.00	per month	50,160	
Office (telephone, mailing, reprographic services)						1,885	1,885
Miscellaneous expendable research supplies						5,750	5,750
Machine Shop		40	hours @	51.00	per hour	2,040	2,040
Publication Costs						1,892	1,892
Computer Services							
Network Access Fee	16 users	12	months @	15.00	per month	2,880	
Labor/parts/vrs exp/Diva	4 wrkstn.	12	months @	109.00	per month	5,232	8,112
Computer Supplies						2,800	2,800
					TOTAL OTHER COSTS		83,186
TOTAL DIRECT COSTS:							573,244
VI. INDIRECT COSTS:							
(49.90% of 470,087)							232,694
TOTAL BUDGET:							805,938

* All salaries and wages are based on current rates with 4% cost-of-living raise effective 1/1/97. Selected faculty merit increases are budgeted at 5%.

** Graduate student health insurance, tuition fee remission and Nonresident Tution fees are overhead exempt.