LOW POWER DESIGN USING PLAS AND STANDARD CELLS

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Abstract

The current trend in IC design is to opt for Standard Cell design over PLAs, because of its advantage in terms of area. With the emerging emphasis on low power design, the use of PLA as a design technique merits a fresh look. This project is a comparative study between low power Standard Cell and several low power PLA structures which were reported in recent years. Two controllers which are several hundreds transistors in size are implemented and their power dissipations are simulated with HSPICE at 20MHz operating frequency. The impact of technology scaling and supply voltage reduction on power dissipation is also investigated. The experimental results show that low power PLA structure 1 can achieve lower power dissipation at a small area penalty compared with low power Standard Cell implementation, for circuits which require small number of minterms in AND plane. This suggests that the low power PLA structure 1 has the potential of being a good alternative for some types of applications in circuit design.

1 Introduction

PLAs are used to implement control logic, boolean logic functions and generate next state vectors for finite state machines. The main advantages of the PLAs are its two level logic, which means less glitches, lower delays and regularity of layout for implementing complex logic. It also permits ease of microcode modification at later stages of design cycle. The current trend in IC design though, is to opt for Standard Cell design over PLAs, because of its advantage in terms of chip area.

Motivated by emerging applications which demand intensive computation in portable environments, techniques to reduce power consumption in CMOS digital circuits are of interest to IC design industry. With this growing emphasis on low power consideration, the best design is not necessarily the minimum area design (which was the main reason for the popularity of Standard Cell). Thus, the use of PLA as a design technique merits a fresh look. There has been some recent work in design of low power PLAs. This project is a comparative study of the power dissipation in low power Standard Cell designs and low power PLAs. We evaluate the power dissipation and chip area of the two design techniques by implementing some control logics involving several hundreds transistors with both methodologies (three latest low power PLA designs are implemented for comparison with low power Standard Cell). We also examine the effect of technology scaling and power supply voltage reduction on power dissipation for both low power PLAs and Standard Cell.

Section 2 explains several low power PLA structures which are implemented in the project; Section 3 describes our approach for this project; Section 4 presents the results of the comparison between low power PLA and Standard Cell in terms of power dissipation and area occupation; Section 5 gives the concluding remarks.

2 PLA Structures

2.1 Conventional PLA structures

The AND and OR planes of a typical self-timed dynamic conventional PLAs are both realized by a NOR configuration. Each plane precharges during the high phase of the clock. When clock is high, the AND plane uses p-channel devices to recharge the minterm buses which also precharges the row lines in the OR plane. Evaluation begins during the clock transition from high to low. This PLA is known to be the fastest, but at the expense of wasted power. The reasons are as follows.

1. During each cycle, all minterms buses in the AND array are forced high, and then all but the selected minterms are discharged.
2. During each cycle, the input and output tracking lines, which are constructed with the maximum capacitance among all input minterm loads, are forced high and then are always discharged to make the delayed clock for the OR array.
3. As the minterm lines change state, all buffers, except the selected ones, switch from low to high and then to low again.
4. The ground switches are charged and discharged every cycle.

2.2 Low Power PLA structures

Several new low power PLA structures have been proposed in recent years aimed at reducing the power consumptions of conventional PLA.

2.2.1 Low Power PLA Structure 1

The first low power PLA structure [3] reported by Linz is a NAND-NOT-NOR structure which combines several modifications to reduce power dissipation. First, the buffer input capacitors are precharged and all output buffers go low. For evaluation, only minterm lines that have all series transistors turned on will be discharged in addition to the tracking line. The virtual ground lines disappear, the number of buffers is halved and only two of them change state every cycle. The majority of the minterm lines remain charged from one cycle to the next. Thus, little power is wasted through discharging. The limitation of evaluating a large number of inputs can be minimized by using n-channel and p-channel pass transistors which eliminates the threshold voltage drop across the n-channel devices. The disadvantage of this structure is the series pass transistor logic may limit the speed when many input minterms are evaluated.

The structure of this sum of product PLA is shown in Fig. 1.

2.2.2 Low Power PLA Structure 2

The second low power PLA structure [2] proposed by Dhong and Tsang is a single phase dynamic CMOS POS (NOT-NOR)-(NOT-NOR)-(NOT-NOT) PLA in a product of sums (POS) using CMOS Dom-

ino logic in the OR array and charge sharing logic in the AND array. By using charge sharing for the implementation of a cascaded AND array and by applying triggered input decoders to replace ground switches during the precharge time (which reduces the power consumption by minimizing the capacitance of the input minterms of the PLA), faster PLA that require lower power dissipation than conventional CMOS SOP (NOT-NOR)-(NOT-NOT)-(NOR-NOT) PLA can be achieved. A noticeable difference from conventional PLA is that only the charges in the selected minterms are wasted. This POS PLA is particularly useful for the implementation of dynamic CMOS PLA that have a greater number of OR array minterms and a lower number of AND array output terms. The disadvantage of this PLA is the charging of the charge sharing capacitor which is two times the product term capacitance.

The structure of the PLA which consists of triggered 1-bit decoders, the OR array, the AND array, buffers, and double inverters as an amplifier is shown in Fig. 2.

2.2.3 Low Power PLA Structure 3

The third low power PLA structure [2] also reported by Dhong and Tsang is a single phase dynamic CMOS POS OR-(NOT-NOR)-(NOT-NOT) PLA in a product of sums using predischarged OR gates like NMOS Domino logic and charge sharing logic. Like low power PLA structure 2, it also adopts charge sharing for the implementation of a cascaded AND array and uses triggered input technique to replace ground switches. The reduction of buffers between the OR array and AND array is achieved by using predischarged OR gates. All minterms are predischarged when clock is low and charge is wasted only in the selected output lines according to the sate of the inputs. It may require longer predischarge time than the precharge time of structure 2 but the predischarged OR array consumes less power than structure 1. This effect of power reduction in the OR array becomes more significant at lower supply voltage because the logic swing of the pass transistor outputs is smaller than the supply voltage level.

The schematic of this structure using triggered 1-bit decoders, predischarged OR array and charge sharing AND array is shown in Fig. 3.

3 Our Approach

The goal of this project is to make a fair comparison between low power PLAs and low power Standard Cell structures [1]. We implemented two controller circuits using the three low power PLA structures discussed above. The existing Low Power Lager Standard Cell library available on the Zabriskie clustering was used for building the low power Standard Cell circuit for comparison with the low power PLA structures. The study focuses on the comparison of these implementations in terms of power dissipation, the impact of technology scaling and power supply voltage reduction which is typical for low power CMOS design. The power-area trade off is also investigated. The performance of the low power dynamic CMOS PLA implementations are measured for both precharge (or predischarge) and evaluation cycles under certain duty cycle assumption.

4 Experimental Results

Two controllers, referred to as Controller 1 and Controller 2 from IC Design Group of EECS at UC Berkeley are adopted for comparative study of the low power PLA and Standard cell designs. Their specifications are as follows:

Name	# inputs	#outputs	# SOP minterms	# POS minterms
Controller 1	4	10	10	18
Controller 2	4	10	16	18

Table 1: Controller Specifications

The layouts of three low power PLAs and Standard Cell generated using MAGIC are shown in Fig. 4, 5, 6, 7 respectively. The physical data of the layouts are listed in Table 2 and 3.

Size (λ x λ)	PLA 1	PLA 2	PLA 3	Std Cell
Area	309 x 278	423 x 305	409 x 287	243 x 424
# Gates	180	258	223	114

Table 2: Physical Data for Controller 1

Size (λ x λ)	PLA 1	PLA 2	PLA 3	Std Cell
Area	359 x 278	423 x 305	409 x 287	235 x 408
# Gates	216	261	227	116

Table 3: Physical Data for Controller 2

The correctness of the functionality and the power dissipations of the layouts are simulated by HSPICE. The Spice decks are extracted from MAGIC layout by ext2spice command. The circuits are operated at 20MHz frequency with 75% duty cycle. Different combination of signal sequence at 20MHz are applied at 4 independent inputs with equal probability of "0"s and "1's. The average power dissipation is computed for both precharge and evaluation cycles. To study the effects of supply voltage reduction on power dissipation, 4 supply voltages of 3.3V, 3V, 2.5V and 1.5 V are tested. In addition, spice decks are extracted for both 1.2 μm and 1.0μm technologies to investigate the impact of technology scaling on power consumption. Tables 4 and 5 show the power dissipation of Controller 1 and 2 under 1.2 μm technology; Tables 6 and 7 show the power dissipation of Controller 1 and 2 under 1.0 μm technology. The unit of power dissipation is μW.

Supply Voltage (V)		1.5	2.5	3.0	3.3
PLA 1	pre-charge	54.9	202.7	296.7	362.9
	evaluation	20.6	51.6	76.5	92.9
	total	29.3	89.6	131.8	160.5
PLA 2	pre-charge	-	708.9	1031.4	1264.1
	evaluation	-	164.4	314.3	422.5
	total	-	300.6	493.6	633.1
PLA 3	pre-charge	-	592.9	915.5	1121.5
	evaluation	-	132.8	275.1	391.9
	total	-	247.6	435.2	574.3
Std Cell	total	32.8	99.5	144.7	178.1

Table 4: Power Dissipation of Controller 1 under 1.2 μm

Supply Voltage (V)		1.5	2.5	3.0	3.3
PLA 1	pre-charge	63.3	263.9	387.9	474.2
	evaluation	24.4	46.6	68.8	83.0
	total	34.1	100.9	148.9	180.8
PLA 2	pre-charge	-	714.0	1043.9	1283.0
	evaluation	-	145.7	254.0	333.8
	total	-	287.8	451.4	571.7
PLA 3	pre-charge	-	561.4	858.3	1048.2
	evaluation	-	151.0	298.3	408.6
	total	-	253.6	438.3	568.5
Std Cell	total	29.6	93.6	142.4	177.4

Table 5: Power Dissipation of Controller 2 under 1.2 μm

The power dissipation during a typical precharge and evaluation cycle of Controller 1 under a supply voltage of 3V and 1.2 μm technology is shown in Fig. 8. Fig. 9 plots the curve of power dissipation vs. supply voltage of low power PLA1 and low power Standard Cell for Controller 1 under 1.2 and 1 μm technologies.

Supply Voltage (V)		1.5	2.5	3.0	3.3
PLA 1	pre-charge	52.8	174.1	257.7	317.7
	evaluation	16.1	42.3	64.3	78.4
	total	25.5	75.5	113.2	138.7
PLA 2	pre-charge	-	622.7	903.5	1098.0
	evaluation	-	169.0	283.3	376.3
	total	-	282.4	438.3	556.8
PLA 3	pre-charge	-	502.9	781.4	983.3
	evaluation	-	120.7	251.1	365.8
	total	-	216.5	383.9	520.7
Std Cell	total	24.6	75.4	111.9	139.0

Table 6: Power Dissipation of Controller 1 under 1.0 μm

Supply Voltage (V)		1.5	2.5	3.0	3.3
PLA 1	pre-charge	64.8	228.1	339.8	417.1
	evaluation	16.3	39.8	57.9	71.0
	total	28.4	86.9	129.1	157.5
PLA 2	pre-charge	-	630.4	915.9	1118.8
	evaluation	-	139.5	227.4	296.1
	total	-	262.2	399.4	501.8
PLA 3	pre-charge	-	477.2	726.0	892.8
	evaluation	-	136.1	281.5	379.2
	total	-	221.4	392.6	507.6
Std Cell	total	23.2	73.2	111.7	139.2

Table 7: Power Dissipation of Controller 2 under 1.0 μm

Several observations can be made based on the above experimental data:

- For Controller 1, low power PLA 1 consumes substantially less power compared with low power Standard Cell under 1.2 μm technology; Its power consumption is very close to Standard Cell (approximately 1 μW difference) under 1 μm technology.
- Based on its structure, low power PLA 1 benefits from having less number of minterms in its AND plane. Controller 2 is a pathological example which has exactly 2^n minterms for n inputs, which is the worst case possible in terms of power consumption. Even so, the power dissipation of low power PLA 1 for Controller 2 is comparable to that of low power Standard Cell (Again, 1.2 μm yields better results than 1 μm technology).

- Based on the testing data, low power PLA 2 and 3 consume substantially more power compared with the other two designs (the power dissipation of PLA 2 is less than PLA 3, which verifies the analysis in Section 2). In addition, they cannot function correctly under supply voltage of 1.5 V.
- The chip area of low power PLA 1 is comparable to low power Standard Cell design, while the areas of low power PLA 2 and 3 are larger than the area of Standard Cell.
- From the testing data, the power consumptions of all design style reduce significantly with the supply voltage. As expected, power dissipation under 1 μm technology is less than 1.2 μm technology.

5 Conclusions

In conclusion, low power PLA structure 1 consumes less power than low power Standard Cell design for circuits which requires reasonable number of minterms in the AND plane, especially under 1.2 μm technology. Even for the worst case example, the power dissipation of PLA1 is only slightly larger than low power Standard Cell. The penalty of area increase for low power PLA 1 is also moderate. Based on our observation, we believe PLA 1 would be a competitive choice especially for circuits with small number of minterms in AND plane.

Acknowledgments

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References

[1] P. Buch, and T. Xue, "A Comparative Study of PLAs and Standard Cell Design for Low Power Circuits," *EE 241 Project Report, University of California, Berkeley*, May 1994.

[2] Y. Dhong and C. Tsang, "High Speed CMOS POS PLA using Predischarge OR Array and Charge Sharing AND Array," *IEEE Transactions on Circuits and Systems-II*, vol. 39, no. 8, August 1992, pp. 557-564.

[3] A. Linz, "A Low Power PLA for a Signal Processor," *IEEE Journal of Solid State Circuits*, vol. 26, no. 2, February 1991, pp. 107-115.

[4] D. Anderson, "The 68040 32-b Monolithic Processor," *IEEE Journal of Solid State Circuits*, vol. 25, no. 5, October 1990, pp. 1178-1189.

[5] A. P. Chandrakasan, S. Sheng and R. W. Broderson, "Low Power CMOS Digital Design," *IEEE Journal of Solid State Circuits*, vol. 27, no. 4, April 1992, pp. 473-484.

[6] M. Kakumu, "Process and Device Technologies of CMOS Devices for Low Voltage Operation," *IEICE Transactions on Electron.* vol. E76-C, p. 672, 1993.

[7] W. H. Chang, B. Davari, M. R. Wordeman, Y. Taur, C.C-H Hsu and M. D. Rodriguez, "A High Performance 0.25 μm CMOS Technology: I-Design and Characterization," *IEEE Transactions on Electron. Devices*, vol. 39, pp. 959-966, 1992.

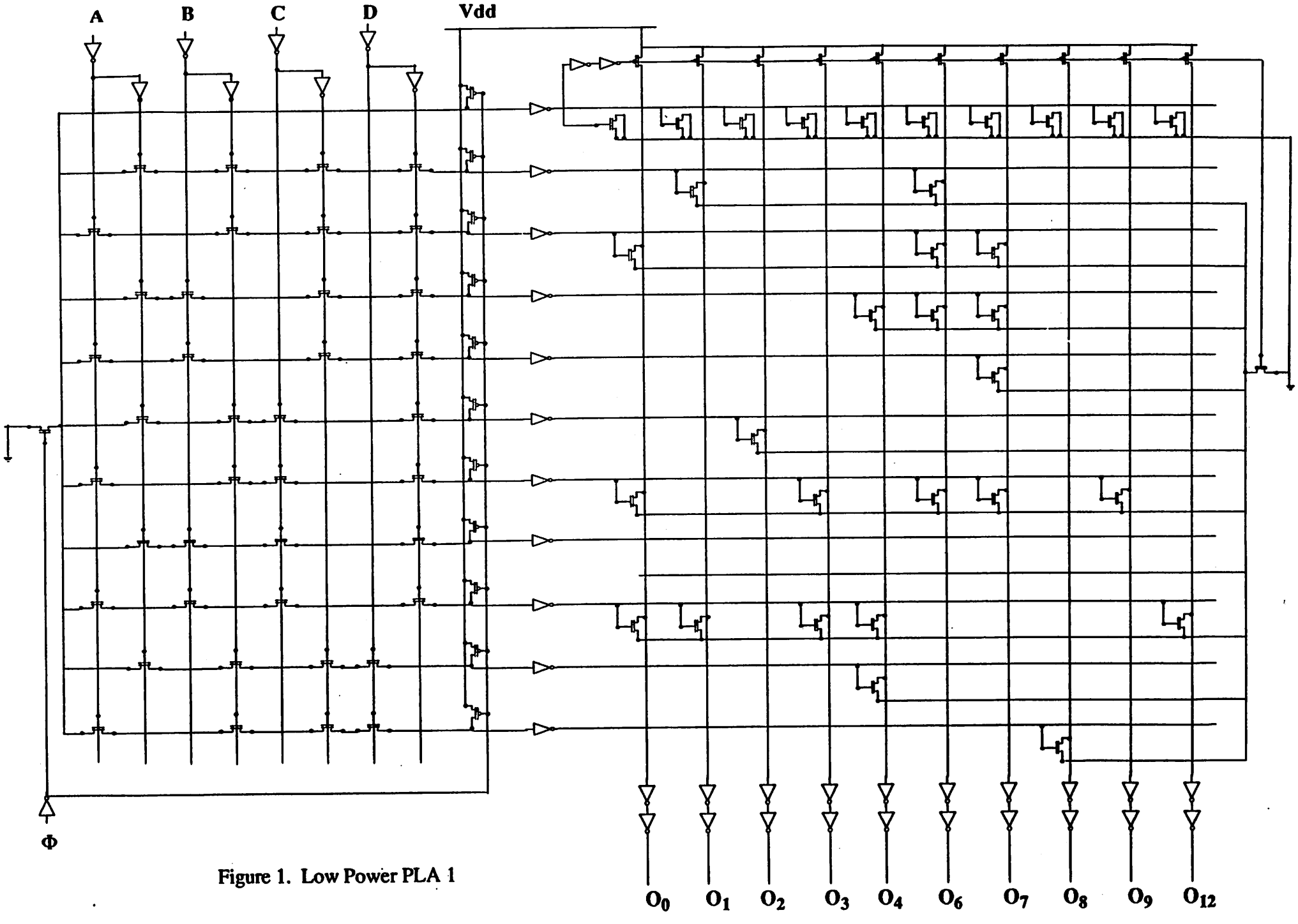

Figure 1. Low Power PLA 1

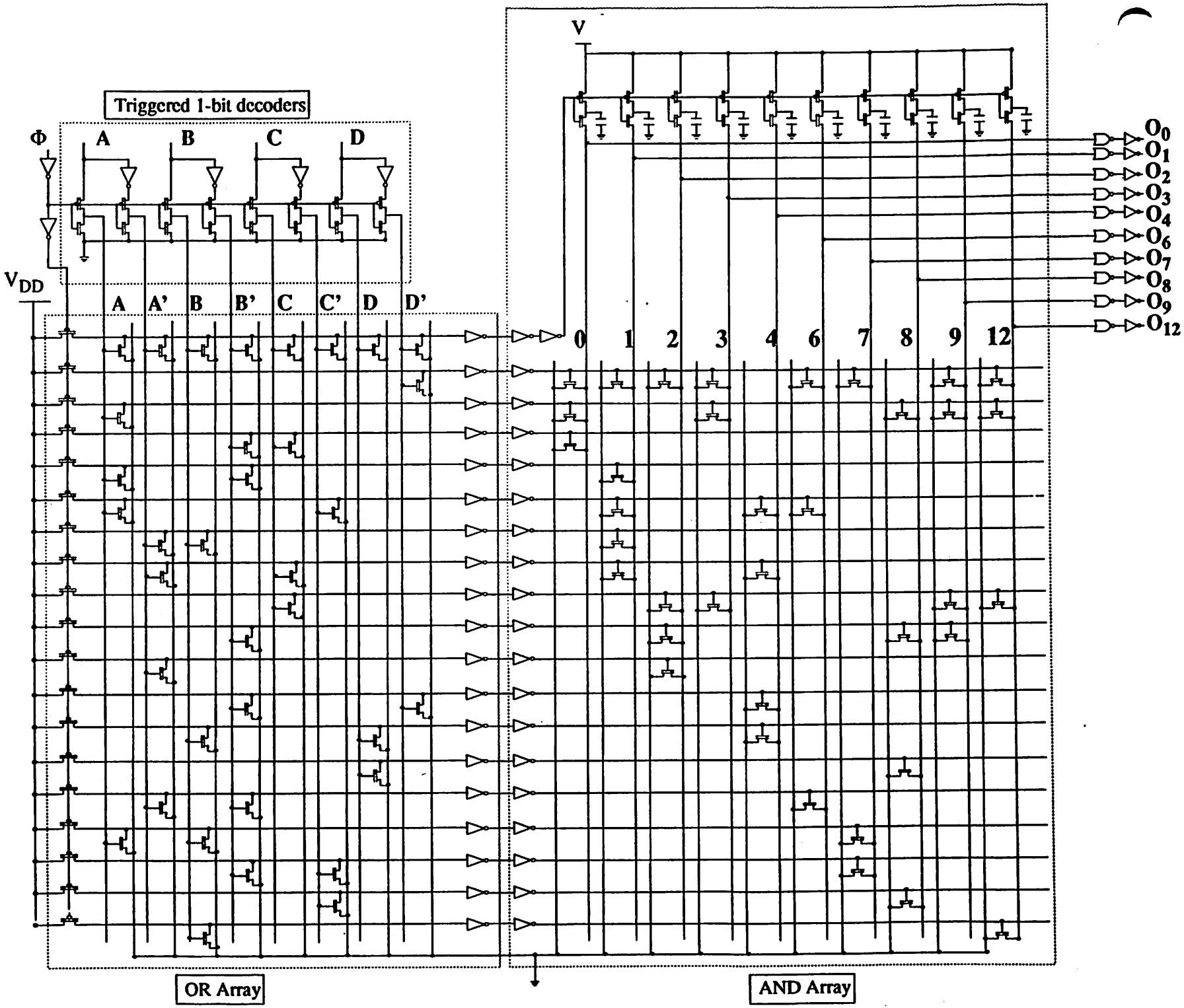

Figure 2. Low Power PLA 2

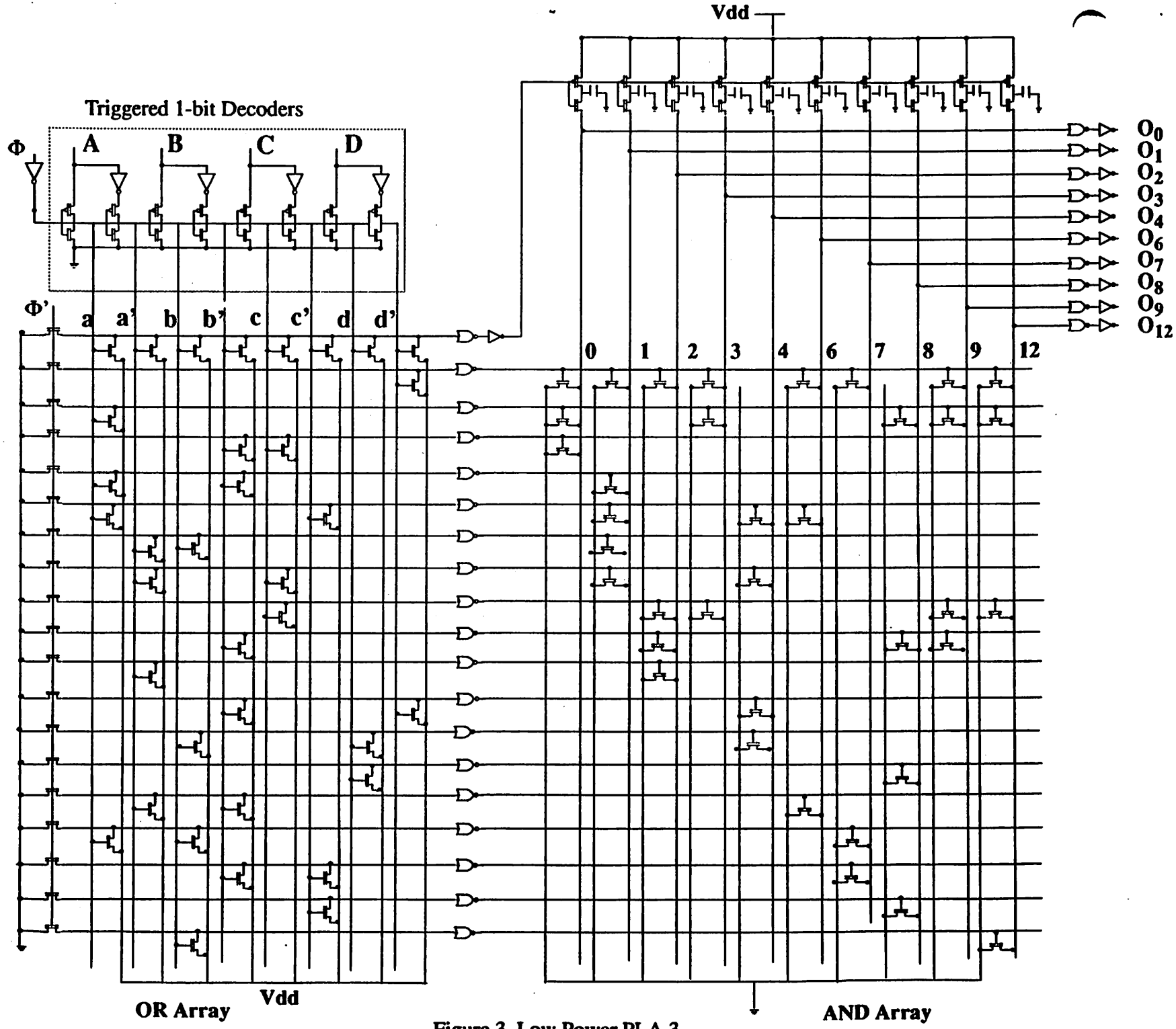

Figure 3. Low Power PLA 3

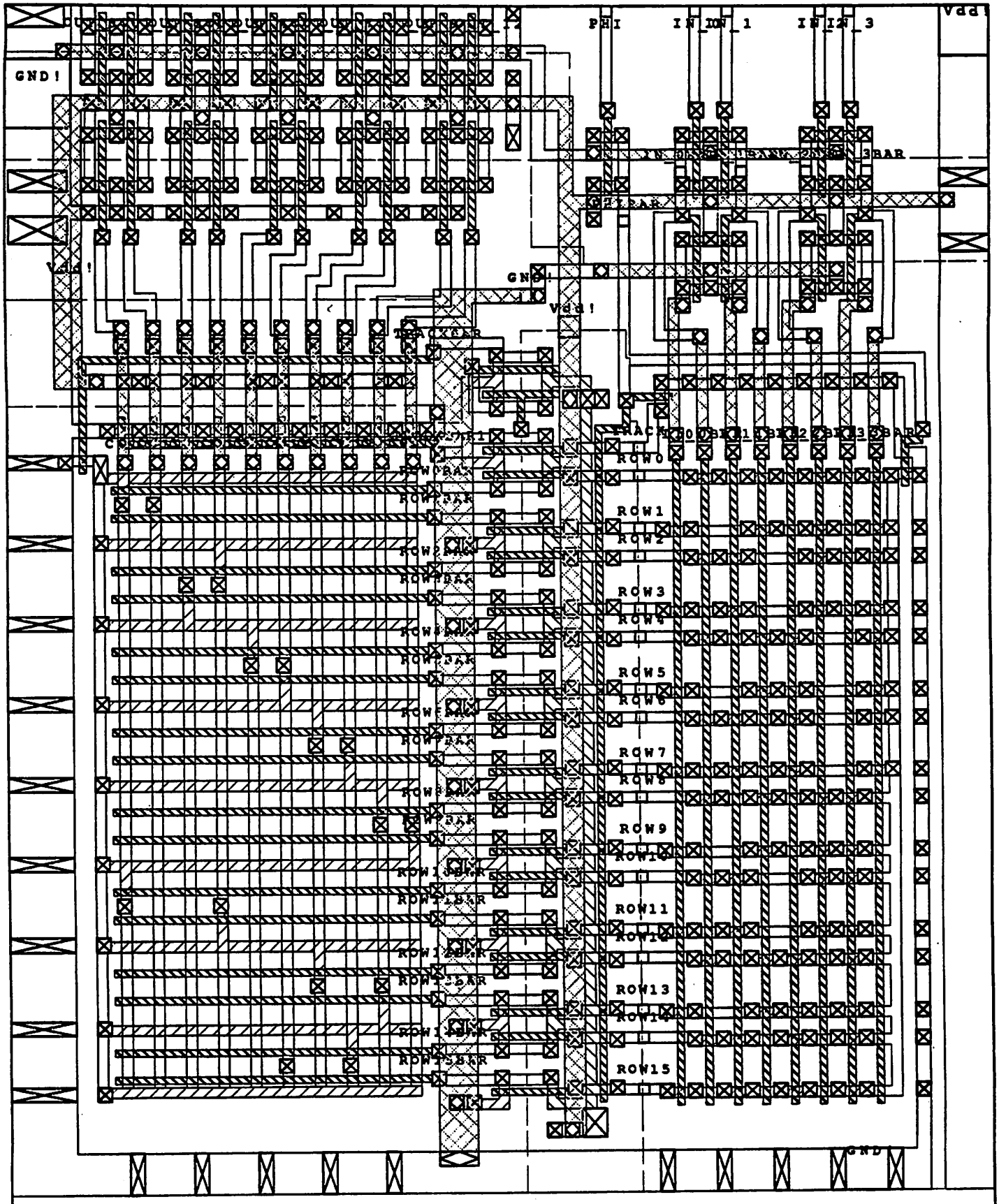

Figure 4: PLA 1

DATE: May 16, 1994

Scale: 38 lambda/inch

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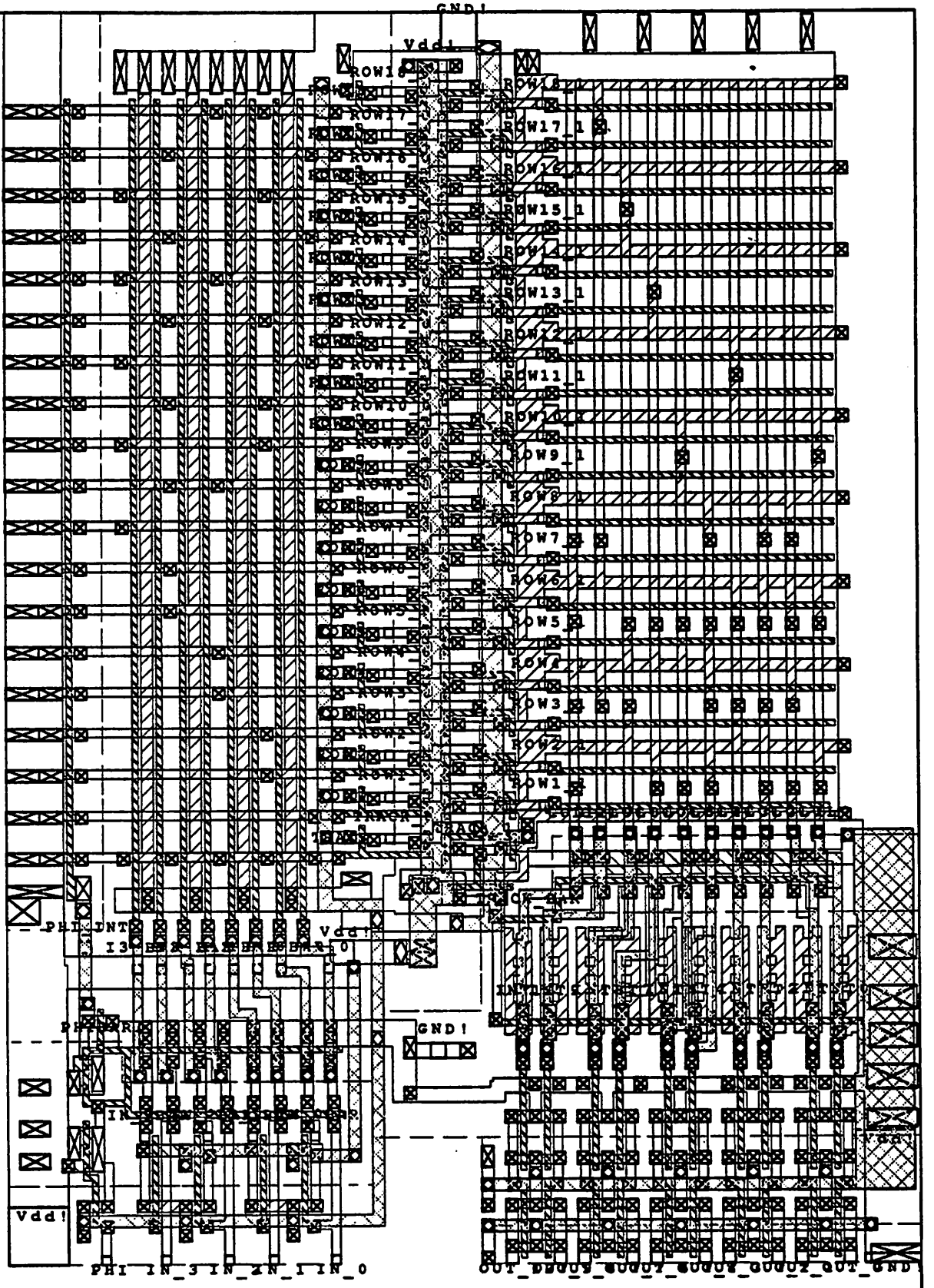

Figure 5: PLA 2	
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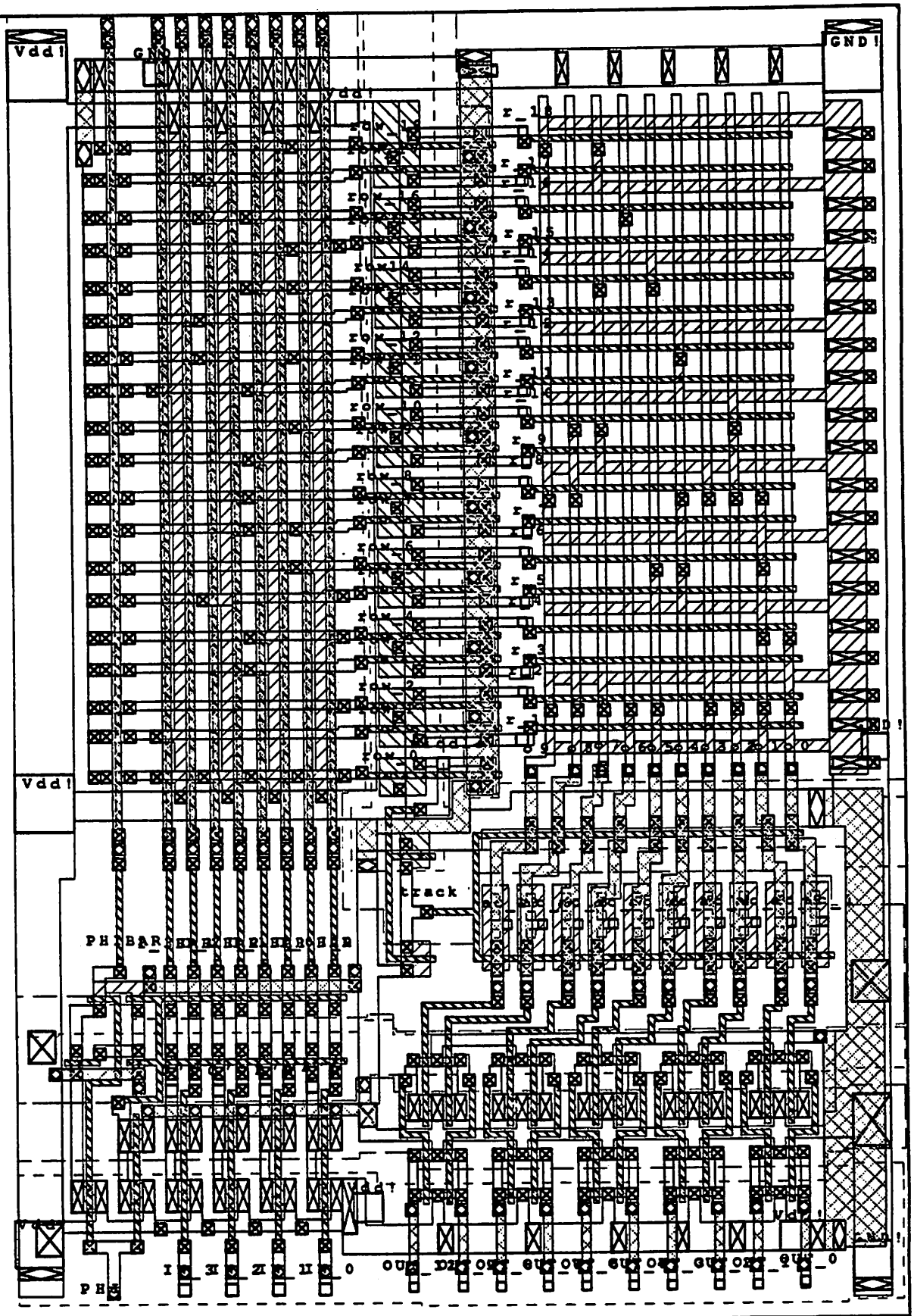

Figure 6: PLA 3	
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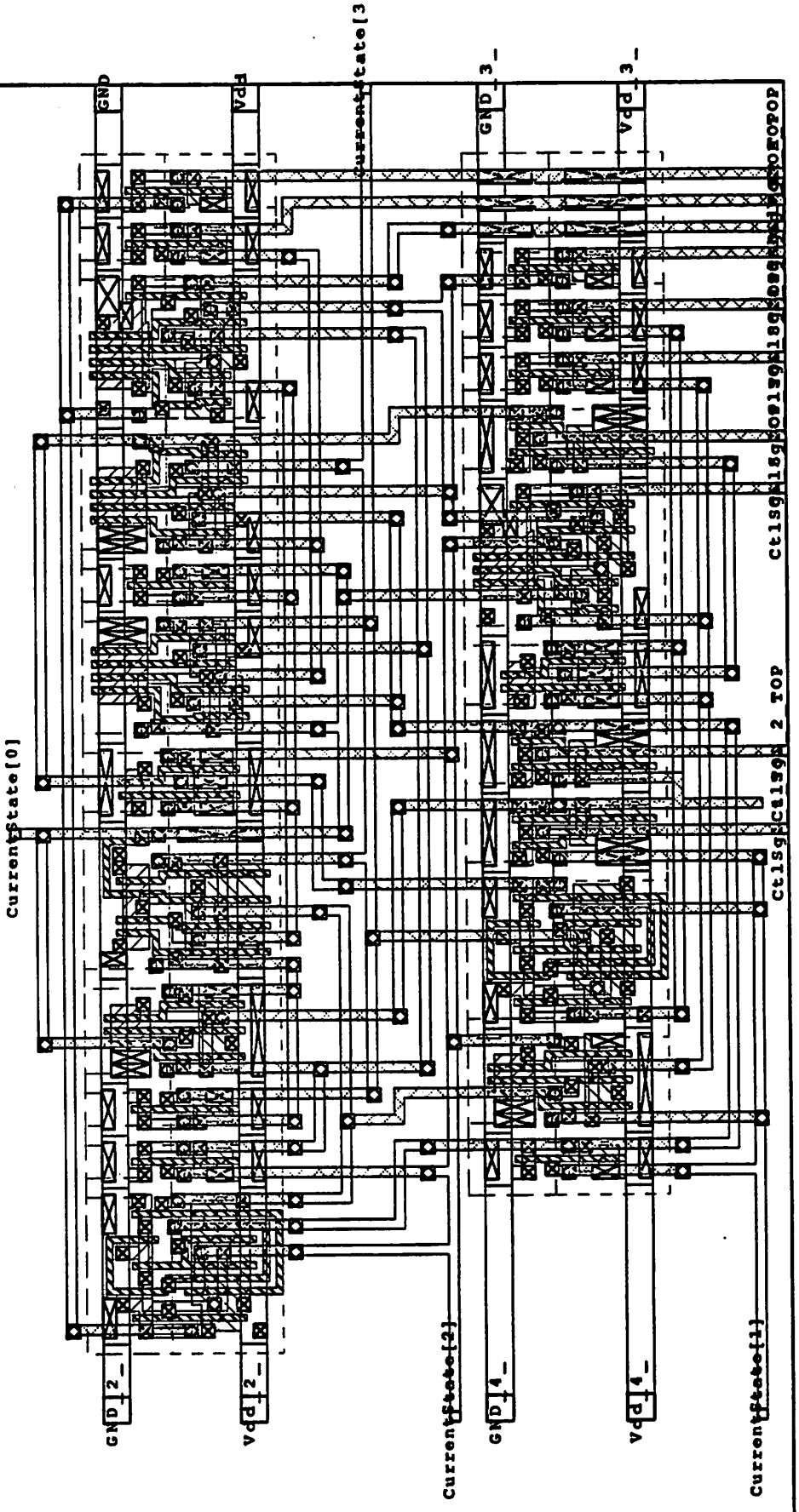

Figure 7: StdCell	
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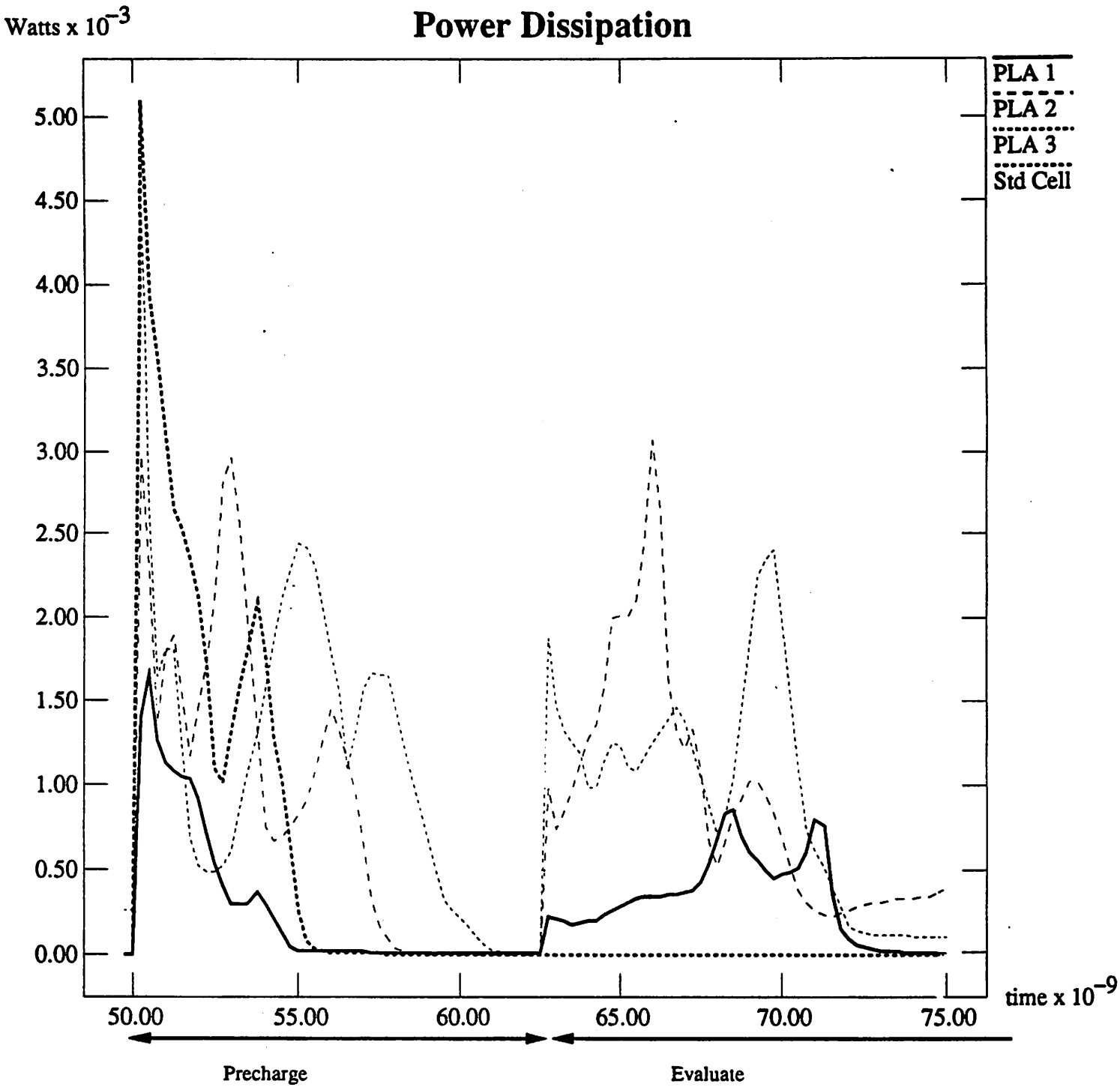

Figure 8. Power Dissipation (Controller 1)

Figure 9 : Power Dissipation Scaling (Controller 1)