HIGH SPEED, LOW POWER, LOW VOLTAGE PIPELINED ANALOG-TO-DIGITAL CONVERTER

by

George Chien

Memorandum No. UCB/ERL M96/27

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Abstract

The goal of this research is to design a high speed, low power and low voltage analog-to-digital converter. With the scaled CMOS technology, many device parameters are benefited from the reduced feature size and geometry. These parameters then translate into performance parameters in a larger system, such as an analog-to-digital converter. In this design, we push for the maximum performance with low power and low voltage for the given technology. In addition, several modifications are made to the previous design [1] mainly by taking advantage of the more advanced process. A prototype is designed in a 0.6μm CMOS process.

To demonstrate analog-to-digital converter being part of a larger system, a version of the A/D converter is integrated with a RF receiver which complies the DECT (Digital European Cordless Telephone system) standard. Many issues, such as low supply voltage, low power, are examined in the context of high integration. A prototype is fabricated with the other circuit blocks in the RF receiver on the same silicon also in a 0.6μm CMOS process.

Acknowledge

Having spent the last three years of my life in the Electrical Engineering Dept. at University of California, Berkeley was a unique experience. And working along with fellow graduate students with the same interests has been very inspiring. There are many people I'd like to thank for the completion of my Masters work.

I wish to express my sincere appreciation for my research advisor, Prof. Paul R. Gray. It has been my privileged to work under his supervision for my Masters work, as well as the upcoming Ph.D. work. Not only his incredible intuition toward the integrated circuit design amazes me, his care and understanding for each of the graduate students extends beyond the advisor-student relationship. Although he has high expectation from the graduate students, he will also help us to achieve that goal. And not to mention his continuous effort to provide an excellent environment and facilities for research.

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I am deeply indebted to Dr. Thomas B. Cho whom I worked very closely for the A/D, as well as the RF project. I really appreciate his explanation of the pipelined A/D converter theory. His clear understanding of everything that goes into an A/D converter answered all of my questions. His leadership for leading us through the design of the DECT radio project was excellent. Because of the size of the project and also the number of people involved, and also our lack of experience in a project in this magnitude, there have been numerous "heated" debate among us. However, Dr. Cho, being the project manager, has always been very patient and making sure that we did not tapeout without verifying every circuit to the capability of our simulation engines. And not to forget his help throughout the testing of the A/D circuit board.

There have been many people who had helped me throughout the last three years. I'd like to thank Dr. Thomas Cho and Jeff Jiajiunn Ou for proof-reading my Masters thesis; Dr. David Cline and Dr. Cormac Conroy for their insights to A/D converters; Andy Abo and Arnold Feldman for

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I'd like to express my appreciation to Level One Communications for their generous donation of wafer fabrication, National Semiconductor for their donation of focus ion beam work, Multek for printed circuit board manufacturing, Corwil Technology for chip-on-board bonding service and Accurel for FIB. Lastly, Semiconductor Research Corporation for their continuous support for Prof. Gray's research project and was also the support to this A/D project.

High Speed, Low Power, Low Voltage Pipelined Analog-to-Digital Converter

CHAPTER 1

Introduction

1.1 Motivation and Goal

With the explosive growth of wireless communication system and portable devices, the power reduction of integrated circuits have become a major problem. In applications, such as PCS (personal communication system), cellular phone, camcorders and portable storage devices, low power dissipation, hence longer battery lifetime, is a must. An example for low power application is a wireless communication system. With the rapid growth of internet and information-on-demand, handheld wireless terminals are becoming increasingly popular. (i.e. UPS and FeDex handheld pad for package delivery.) With limited energy in a reasonable size battery, minimum power dissipation in integrated circuit is necessary.

Many of the communication systems today utilize digital signal processing (DSP) to resolve the transmitted information. Therefore, between the received analog signal and DSP system, an analog-to-digital interface is necessary. This interface achieves the digitization of received waveform subject to a sampling rate requirement of the system. Being a part of communication system, the low power constraint, mentioned above, the A/D interface also needs to adheres to the low power constraint.

The trend of increasing integration level for integrated circuits has forced the A/D converter interface to reside on the same silicon with large DSP or digital circuits. By sharing the same supply voltage between A/D and digital circuit, it reduces the overhead cost for extra DC-DC converters to generate multiple supply voltages. Therefore, an A/D converter operating at the same voltage with the digital circuit is desirable.

With the rapid growth of Information Superhighway today, large amount of data are stored in storage devices and accessed frequently. In order to transmit large amount of data in a short period of time, a high trasnfer rate in storage devices is required. This translates directly into a higher data conversion rate in the read channels of magnetic storage devices, such as in a SCSI hard drive. In the commercial market today, transfer rate of 100MS/s can be commonly found with resolution of 6-8 bits. However, in order to achieve even higher transfer rate for some multimedia applications, the speed of A/D converter needs to improve.

To achieve the goals mentioned above (i.e. low power, low voltage and high speed), CMOS technology is very attractive for several reasons. First, the low cost and high integration level have made the CMOS technology superior over bipolar technology. Because of that, several low power CMOS design techniques have been developed. And with the scaled CMOS technology, it can achieve the high speed which was once reserved for bipolar or other fast processes.

With the above motivations, the goal of this research is to build a high speed, low power, low voltage A/D converter in 0.6μm CMOS technology.[1] For high integration, it will be shown that a version of this A/D converter is integrated with a wireless communication front-end receiver. Shown in the measurement chapter, a 10-bit 40MS/s A/D converter with a peak SNDR of 58.5dB measured with 100kHz sine wave input has been achieved.

1.2 Thesis Organization

In Chapter 2, several pipelined A/D converter architectures are reviewed. First, the evolution of pipelined A/D converters is presented. Then a detail description of pipelined A/D architecture is described with an emphasis on the advantages of pipelined A/D architecure for low power and high speed.

In Chapter 3, the design techniques used in this particular A/D converter is described. Several low power and low voltage techniques are briefly introduced here and modifications from the previous 1.2μm design [1][2][3] are also included in this section.

A prototype chip has been fabricated in 0.6μm DPTM CMOS process and evaluated. The measured results will be presented in Chapter 4. And the conclusion is in Chapter 5.

1. This work is based on a previously published work which was done here at University of California, Berkeley by Dr. Thomas B. Cho and Prof. Paul R. Gray. Please see the reference section for previous publications.

CHAPTER 2

Pipelined Analog-to-Digital Architecture

2.1 Overview

In this chapter, after a brief introduction of the evolution of pipelined A/D converter architecture, the power optimized pipelined A/D converter architecture will be described. The focus of this chapter will be the power optimization techniques on the architectural level, such as the choice of stage resolution, capacitor scaling and digital correction. The design of high speed, lower power A/D converter architectures have been investigated in detail and can be found in several publications [3][12][14] and will not be included in this thesis.

2.2 Evolution of Pipelined A/D Architecture

Since the existence of digital signal processing, A/D converters have been playing a very important role which interfaces between the analog and digital worlds. They perform the digitalization of analog signals at a fixed time period (frequency), the speed of A/D converters. The fixed time period is generally specified by the application. One typical example is the Nyquist Sampling Theorem which states:

A bandlimited signal having no spectral components above f_m Hz can be determined uniquely by values sampled at uniform intervals of Ts seconds, where $T_S \leq \frac{1}{2f_m}$

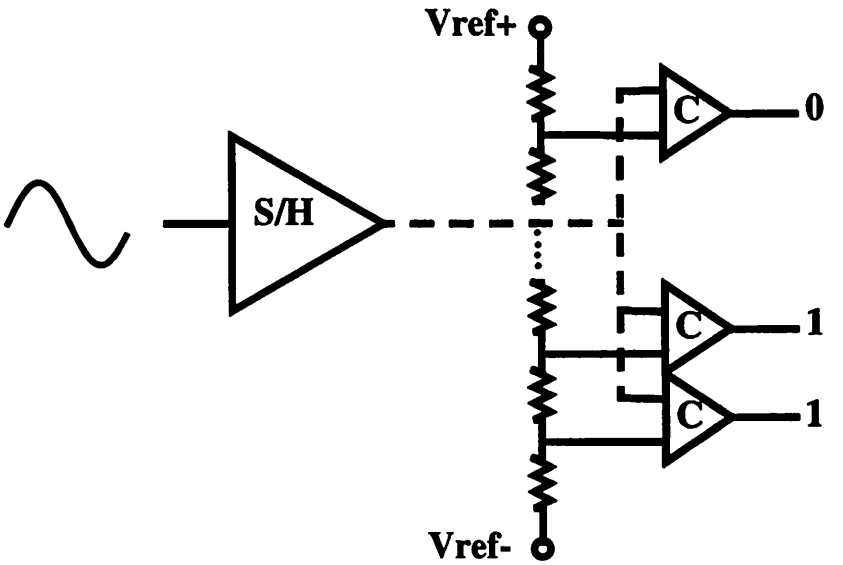


Figure 2.1 A conceptual diagram of a flash A/D converter

This condition needs to hold in order to reconstruct the original analog signal completely. Since algorithms can be implemented very inexpensively in digital domain and if the samples acquired satisfy the Nyquist Sampling Theorem, signals can be reconstructed perfectly after the digital signal processing. Hence, the A/D converter acts as a bridge between two domains and its accuracy is very critical to the performance of the system.

2.2.1 Flash Architecture

The most straightforward way to perform the A/D conversion is to compare the sampled analog signal with different reference levels. Figure 2.1 shows a conceptual diagram for such a converter. The input signal is first sampled by the Sample/Hold circuit (S/H); during the hold cycle, the comparators make decision whether or not the sampled value is greater or smaller than the reference voltages. The output data is then collected and construct a digital representation for the sampled analog signal. Because of the direct comparison, each reference level (See Appendix A for Reference Voltage Generator) needs to be one LSB apart from each other. Assuming a N bit A/D converter is desired, the number of comparators required is 2^N. Further assume that the full scale input is 1V, then the LSB size is 2^{-N}. Therefore, the offset of the comparator needs to be much less than this value, typically for 10 bit resolution is < 1mV. In CMOS, this offset requirement is difficult to achieve. Some special circuit techniques are required to reduce the offset of the comparator,

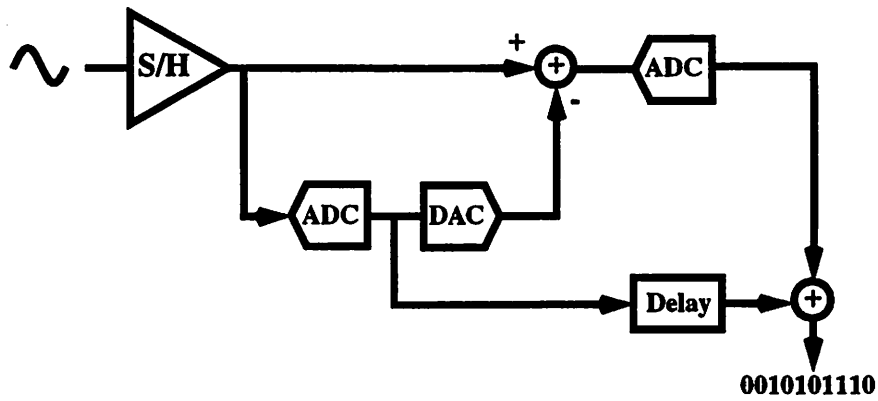


Figure 2.2 Block diagram of a 2-step flash A/D converter

i.e. preamp, offset compensation, etc. However, these techniques are generally power hungry and may not be practical. Therefore, this family of converters is limited to 8 bit or less resolution. And because of its fast conversion rate (only takes a single clock cycle to perform the conversion), the name, flash converter, is hence given to it.

The advantage of this architecture is its fast conversion rate. For low resolution application, one can achieve > 100MS/s conversion rate with the flash architecture. And the latency through the converter is only one clock cycle; for application which requires data immediately, i.e. in a feedback/feedforward loop, a flash converter is generally the choice of architecture. On the other hand, low tolerance on the process offset, hence low resolution, and high power dissipation due to large number of precision circuits drive the designers to look for an alternative for flash converters.

2.2.2 2-step Flash Architecture

The required large number of low offset comparators was the major problem in flash converters. Figure 2.2 shows a block diagram of 2-step flash A/D converter which reduces the comparator count down to $2^{\frac{N}{2}+1}$. Similar to flash converters, the analog input is first sampled by S/H circuit; during the hold period, the first flash ADC performs a coarse quantization on the held signal. The held signal is then subtracted from the output of DAC; the residue of the subtraction is then passed down for fine quantization to full resolution of the converter. Although this architecture still requires the low offset comparator with the full resolution of the converter, the number of low offset comparator required is reduced significantly. With $2^{\frac{N}{2}}$ coarse comparators required in the first half of the converter, the total number of comparators is also reduced. By using concurrent pro-

cessing, the throughput of this architecture can sustained the same rate as flash A/D. However, the converted outputs have a latency of two clock cycles due to the extra stage to reduce the number of precision comparators.

The advantage of this architecture is its low count on precision comparators, hence lower power. The throughput is the same as flash converters because of concurrent processing of signals, however, an extra clock cycle is required because it requires two steps to complete the conversion. If the system can tolerate latency of converted signal, 2-step flash is a lower power, smaller area alternative. The disadvantage is that both the subtraction and precision comparators still need to be the full resolution of the A/D. As mentioned earlier, it is very difficult to achieve resolution above 8 bit in CMOS without special techniques to compensate for the offset. Subtraction accuracy can be relaxed by using a wider range of precision comparators in the second stage, i.e. digital correction (described later in this chapter). Interstage gain can be used here to tolerate larger comparator offset for the second stage precision comparators.

2.2.3 Conventional Pipelined A/D Architecture

In the 2-step flash converter, an interstage gain amplifier can be used to relax the comparator offset in the second stage. In the same way, if we amplify the subtracted residue signal from the first stage to the full scale, the offset requirement of the 2nd-stage comparators can be relaxed. Figure 2.3 shows a 2-step flash converter with an interstage gain, A. However, the interstage gain needs to be carefully designed according to the first stage resolution and the overall A/D resolution. For example, a 10 bit 2-step flash A/D converter utilizes an switched capacitor interstage

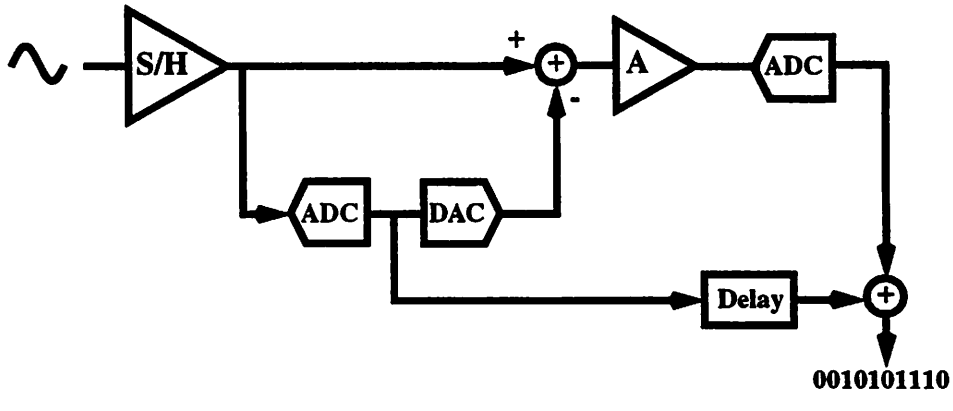


Figure 2.3 Block diagram of a 2-step flash A/D converter with interstage gain

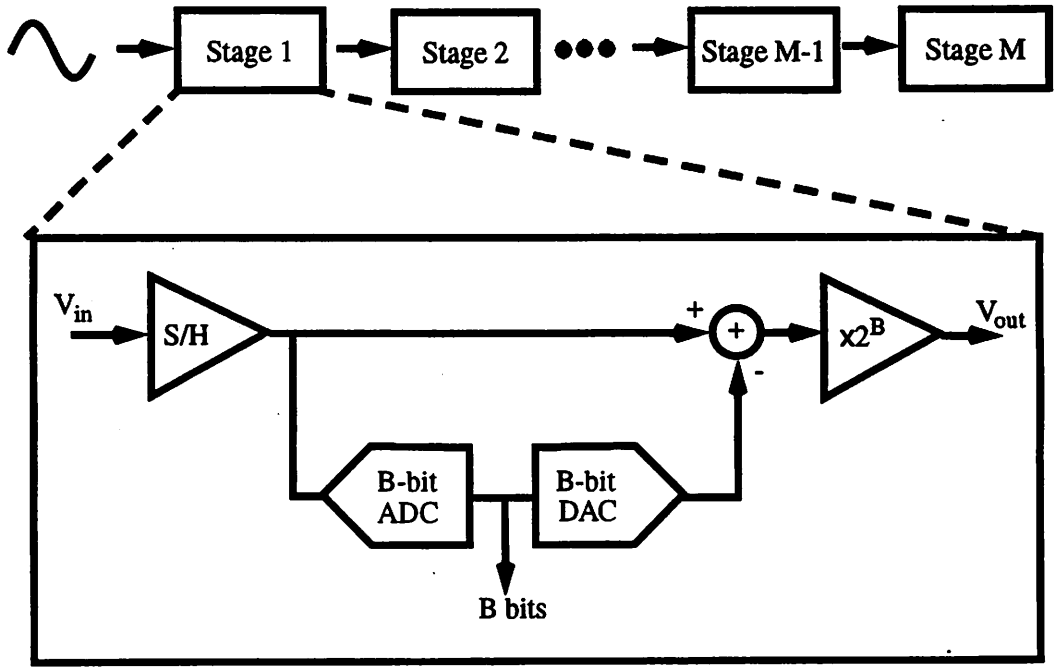


Figure 2.4 Block diagram of a conventional pipelined A/D converter

amplifier. The amplifier is required to settle to 10 bit resolution in roughly half the clock period with the gain of $2^5 = 32$. To meet this requirement in switched capacitor (SC) circuit at high speed is very difficult and may take a lot of power, mainly due to the small feedback factor.

In order to reduce the power even more, one can reduce the per-stage resolution and cascade more stages to get the full resolution. This particular architecture is called the Pipelined architecture, mainly because the analog input signal is passed through a pipeline of flash A/D (sub-ADC) and interstage gain blocks. Figure 2.4 shows the conventional pipelined architecture block diagram. As in previous architecture cases, the analog input signal is sampled by a S/H circuit. The sampled input signal is then converted to the resolution of the stage, B bits; concurrently is also subtracted from the DAC output of the present stage digital output. The residue is then amplified by the factor 2^B and passed down to the next stage. Identical operation is performed for each stage and the digital outputs are combined properly to achieve the required MxB bit full A/D resolution.

The advantage of this architecture is its reduced complexity. With a given per-stage resolution, an A/D converter of a given resolution can be achieved by cascading an appropriate number of identical pipelined stages. Therefore, the hardware cost is a linear function of resolution, given that

all the requirements are met. Some capacitor trimming techniques may be required to correct for the SC circuit gain and non-ideal subtraction (capacitor mismatch). With concurrent processing (interleaving between stages), the throughput achieved is the same as the flash case, a set of output bits per clock cycle. The major disadvantage of this architecture is the latency in the converter. Generally, if concurrent/interleaving processing is used, the delay through the converter is roughly $\frac{N}{2}$ clock cycles.

Up to now, the conventional pipelined architecture has the most flexibility and the least number of precision components required to be accurate to the full resolution of the converter. In next section, an attempt to optimize the power and eliminate precision circuit components is introduced.

2.3 Power-Optimized Pipelined A/D Architecture

To reduce the power, the trade-off between per-stage resolution and number of stages is investigated. And capacitor scaling method is described to reduce the power which was overdesigned in the later stages of a conventional pipelined architecture case. Lastly, the use of digital correction is introduced to eliminate precision comparator with inexpensive low power digital circuits.

2.3.1 Power-Optimized Per-Stage Resolution

In the conventional pipelined A/D architecture, the trade-off between the per-stage resolution and power is not clear. For a given sampling rate, when increasing the per-stage resolution, the required number of stages is reduced; however each stage will require more power because of multiple bits. When decreasing the per-stage resolution, the required number of stages is increased; however each stage will require less power. Below is an attempt to estimate the power for the conventional pipelined A/D architecture with different per-stage resolution.

Using the conventional pipelined A/D converter, each stage is identical and performs the same functionality. The power comparison can be found by comparing the power per stage and multiply by the number of stages. Majority of power in a stage is dissipated in the SC S/H/Gain circuit and

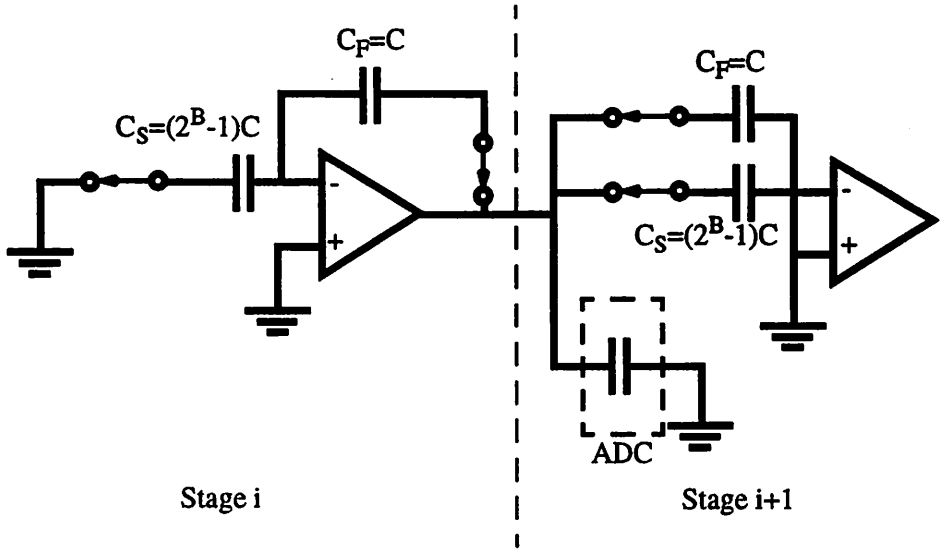


Figure 2.5 Power Estimation of Pipelined A/D (shown is the B=2 case)

the estimation of SC power can be done as follows. Figure 2.5 shows a stage in the pipeline loaded by the next stage. The load capacitance is $2^B C + C_{Flash}$ where C_{Flash} is the input capacitance of the flash ADC of the next stage. The total number of stages is roughly the full resolution of the converter divided by B, per-stage resolution. And the number of comparator required in each stage is about $2^B - 1$.

Knowing the load capacitance and the interstage gain of each stage, the power dissipation per stage can be estimated as a function of B, per-stage resolution. The result of this power estimation is shown previously in [3]. It has concluded that for 8 and 10-bit applications, as the sampling frequency increases, the interstage amplifier bandwidth must be increased to meet the faster settling time requirement. The power difference between 8 and 10-bit curves is much smaller than the $\frac{kT}{C}$ prediction for a given sampling frequency. This is due to the fact that noise is not limiting the performance at these resolutions. Where as in the higher resolution cases (12 or 14-bit), the power increase follows the $\frac{kT}{C}$ prediction of 16x increase in power for 2 bit increase resolution.

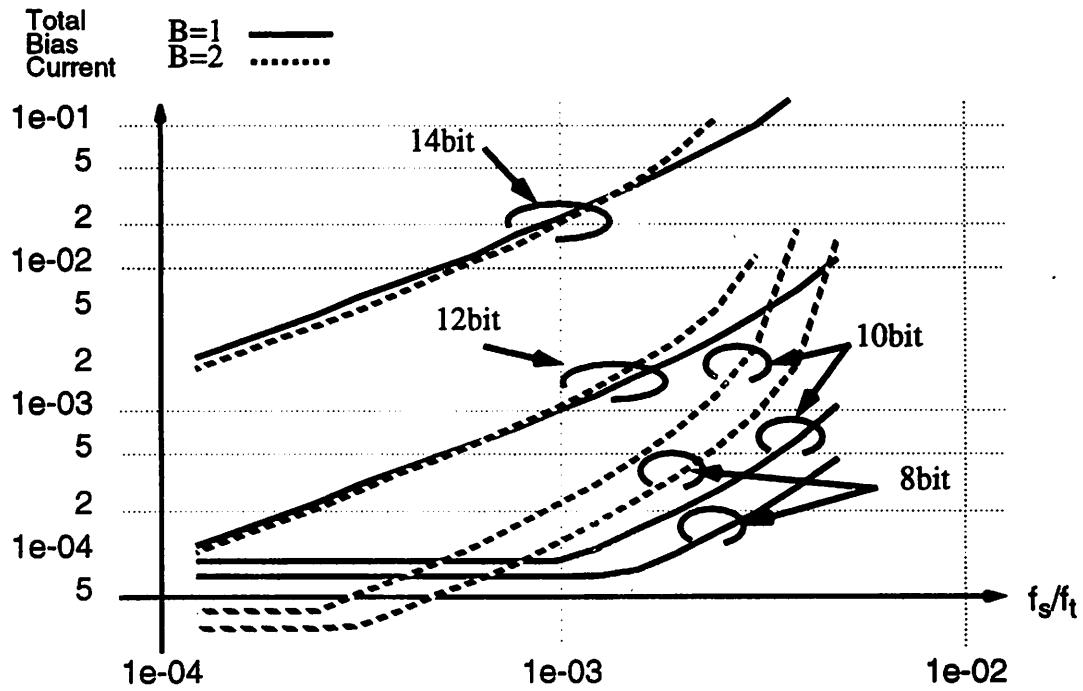


Figure 2.6 Power Comparison for B=1 and B=2 vs. $\frac{f_S}{f_t}$

Figure 2.6 shows the power comparison between B=1 and B=2 versus sampling rate normalized to f_t of technology [3]. For 8 and 10-bit resolution, minimum size pipeline stage can be used to meet the noise and speed requirement at low conversion rate. Therefore, the power is simply determined by the number of stages in the pipeline; less number of stages requires less power. However, as the sampling frequency increases, settling time becomes the determining factor in power dissipation. Shown in Figure 2.6, pipeline with lower per-stage resolution requires less power; this is due to the fact that for low per-stage resolution, the feedback factor for the interstage amplifier is the largest, hence better settling time performance.

For higher resolution (12 or 14-bit), the curves for B=1 and B=2 coincide with each other, meaning the power dissipation is roughly equal for both cases. Inherently, the B=1 case is more suitable for high conversion rate because of its large feedback factor; the B=2 case is preferred for low speed since its interstage gain attenuates the noise from later stages referred to the input. Therefore the power savings from the large feedback factor in B=1 case roughly cancels the larger capacitance required for noise performance; where as B=2 case, the greater OpAmp power is required to compensate for the smaller closed loop gain.

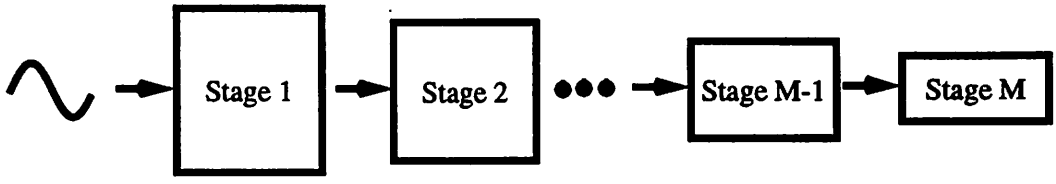


Figure 2.7 Conceptual Diagram of Scaled Pipelined A/D Architecture

From the above discussion, a simple conclusion can be drawn: at low sampling frequency, the minimum size OpAmp is sufficient to meet both the noise and settling requirement. Therefore, larger per-stage resolution, hence less stages, is preferred for low power. On the other hand, at high sampling frequency near the limit of technology, lower per-stage resolution (hence low closed loop gain) and smaller load capacitance is more suitable for low power.

2.3.2 Power-Optimized Capacitor Scaling

If we re-examine the conventional pipelined A/D architecture more closely, the performance of first stage is found to be the most critical one. Not only the comparator, interstage gain and subtraction need to be accurate to the full resolution of the converter, the $\frac{kT}{C}$ noise from sampling (Appendix C), also deserves some attention for high resolution application. Since the equivalent input-referred noise contribution from subsequent stages is attenuated by the interstage gain of all previous stages, the noise contribution from the first stage (or first S/H circuit) for noise limited pipelined architecture case determines the A/D performance. And because the input-referred noise is attenuated by the interstage gain for later stages, the effective resolution requirement for each stage decreases as the sampled analog signal travels down the pipeline.

Since the noise contribution is mostly coming from the capacitor sampling in the first stage, the capacitors can be scaled down for later stages in the pipeline. For example, assuming a 10-bit pipelined A/D converter with 5 stages (2 bits/stage), the noise performance of the first stage needs to be 10-bits. However, the second stage only needs to meet the noise performance of roughly 8-bit. The reduction of noise requirement can be translated into reduced capacitor sizes, hence smaller Op Amp for power optimized solution. Figure 2.7 shows a conceptual block diagram of a scaled pipelined A/D architecture. This is intended to illustrate that each stages of the pipeline,

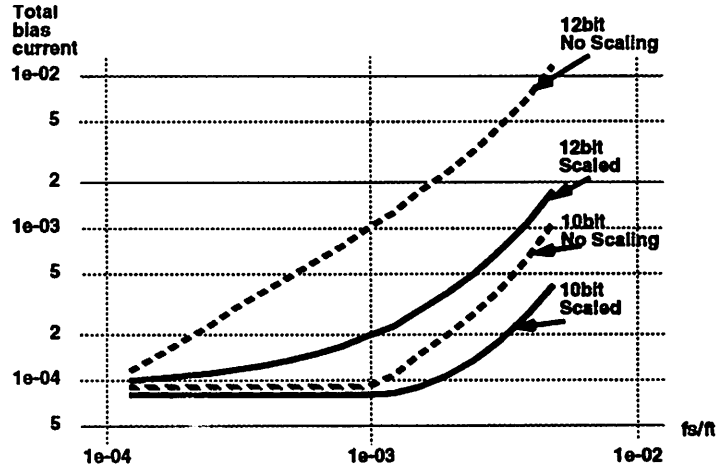


Figure 2.8 Power Comparison between Scaling and Non-Scaling Case

although with the same functionality, can be scaled appropriately according to the required resolution at the input of each stage.

Figure 2.8 shows the power comparison between scaling case and non-scaling case for B=1. It is apparent that at high sampling rate, the non-scaling 10 bit A/D power approaches that of a 12 bit converter with scaling. The power saving at the same resolution can be as much as 5 times. For B=2 case (Figure not shown, please refer to [3]), the power saving is slightly less than B=1 case. This is due to the fact that with B=1, the low interstage gain allows the amplifier configuration to have higher bandwidth, hence using an OpAmp design closer to the noise-limited minimum size.

In conclusion, a pipelined architecture employing capacitor scaling consumes much less power than the conventional pipelined architecture. And it is demonstrated again for high sampling rate, a low per-stage resolution (B=1) is more desirable than a high per-stage resolution (B=2). However, the disadvantage of this architecture is the increase in design time. In order to achieve the minimum power dissipation, each stages needs to be optimized carefully to achieve the lowest possible power for a given noise limitation; where as for the conventional case, the stages can be duplicated to reduce the design cycle.

2.3.3 Digital Correction

In the last two sections, methods to reduce power are shown for the proper choice of per-stage resolution and capacitor scaling. However, with a closer examination of the first stage, a precision flash ADC, subtraction and interstage amplifier to the full resolution of the converter are still

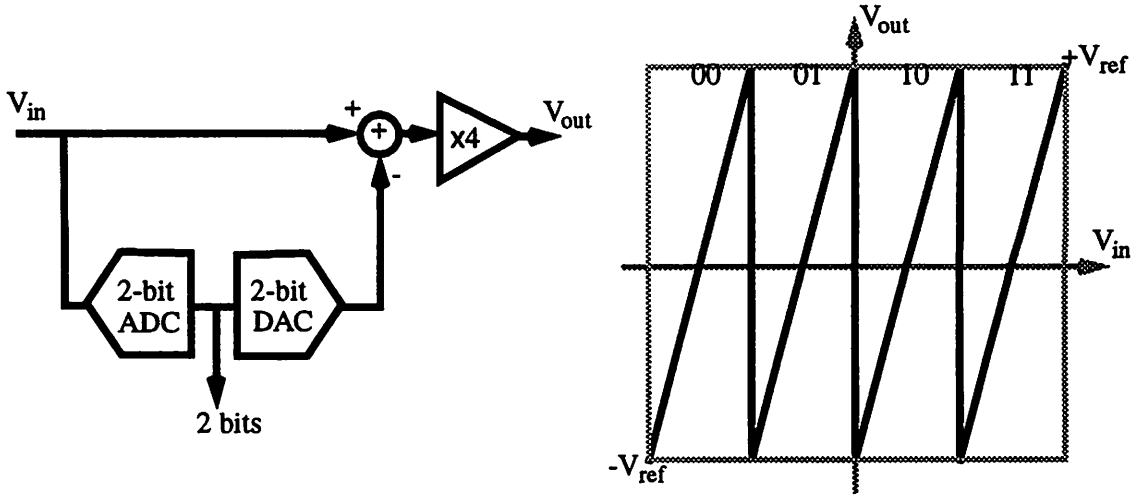


Figure 2.9 Ideal Transfer Function of a 2-bit Pipelined Stage

required to achieve the full resolution of the A/D. As demonstrated earlier, in CMOS, it's extremely difficult to design an A/D without calibration to 10-bit resolution; therefore, some correction algorithm is required for a robust design. In this section, the use of digital correction is introduced with an attempt to relax the comparator offset requirement.

In order to illustrate the algorithm behind digital correction, a 2-bit pipeline stage is presented here as an example. Figure 2.9 shows the ideal transfer function of 2-bit pipeline stage whose block diagram is shown on the left. When the input crosses one of the sub-ADC decision levels, the digital output for the stage is increased by one bit, whereas the stage output decreases by 2 V_{REF}'s. With the interstage gain of 4, the signal presented to the next stage is the full scale and does not allow any room for errors in sub-ADC and sub-DAC. When an offset occurs in the sub-

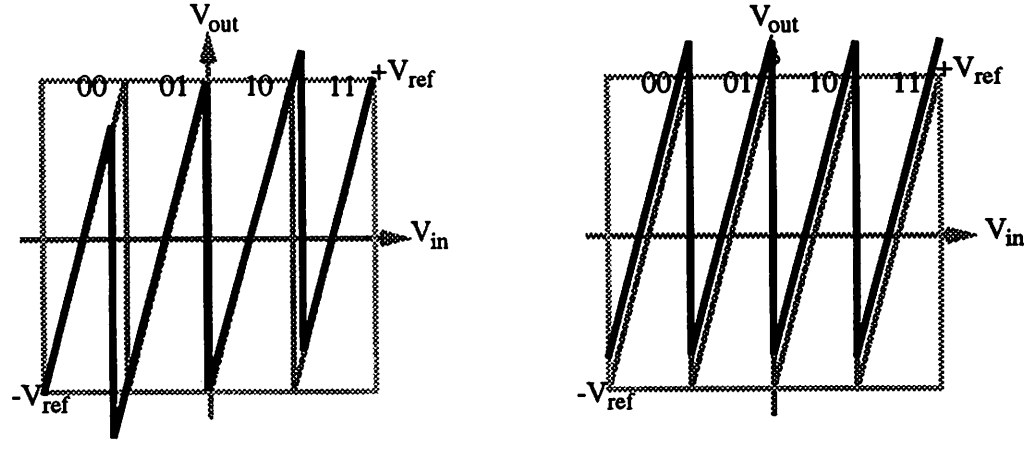


Figure 2.10 Transfer Function with sub-ADC (L) and sub-DAC (R) Errors

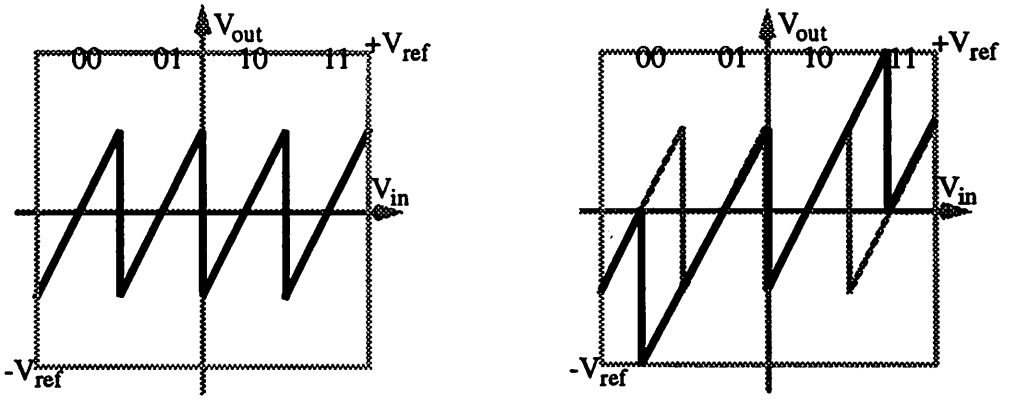


Figure 2.11 Transfer Function with Interstage Gain of 2 and sub-ADC Error

ADC or sub-DAC, the output of the first stage will exceed the range bounded by $\pm V_{REF}$; shown in Figure 2.10. This will saturate the second stage and cause missing information. To eliminate this problem, one can increase the range of the second stage sub-ADC or equivalently reduce the interstage gain of the first stage to tolerate sub-ADC error.

When the interstage gain is reduced to 2, the transfer function becomes Figure 2.11. This allows the sub-ADC error to be as large as $\frac{1}{4}V_{REF}$ and the output is still in the input range of the following stage. However, when a sub-ADC error is present without digital correction, the error will appear in the final digital output. In another words, if digital correction is not used, the first-stage sub-ADC must still be as linear as the entire converter. Whereas later stages, because of interstage gain, the requirements can be relaxed. Now, assume the first stage is ideal, with a full scale input to the first stage, the output is only between $-\frac{1}{2}V_{REF}$ and $\frac{1}{2}V_{REF}$, leaving an extra bit on top and bottom of the per-stage resolution. Digital correction simply utilizes the extra bit to correct the overranging section from the previous stage.

For example, when one of the sub-ADC thresholds has an offset, the output of the first stage will exceeds $\frac{1}{2}V_{REF}$. The second stage, sensing the overranging, will increase the output by one LSB. This bit will cause the first stage output to increase by one LSB during the digital correction cycle. In the same way, when the output of the first stage drops below $-\frac{1}{2}V_{REF}$, the second stage will sense the overranging and subtract one LSB during digital correction cycle. With this method, the sub-ADC error, as large as $\frac{1}{4}V_{REF}$, in the stage can be corrected by the following stage with digital correction.

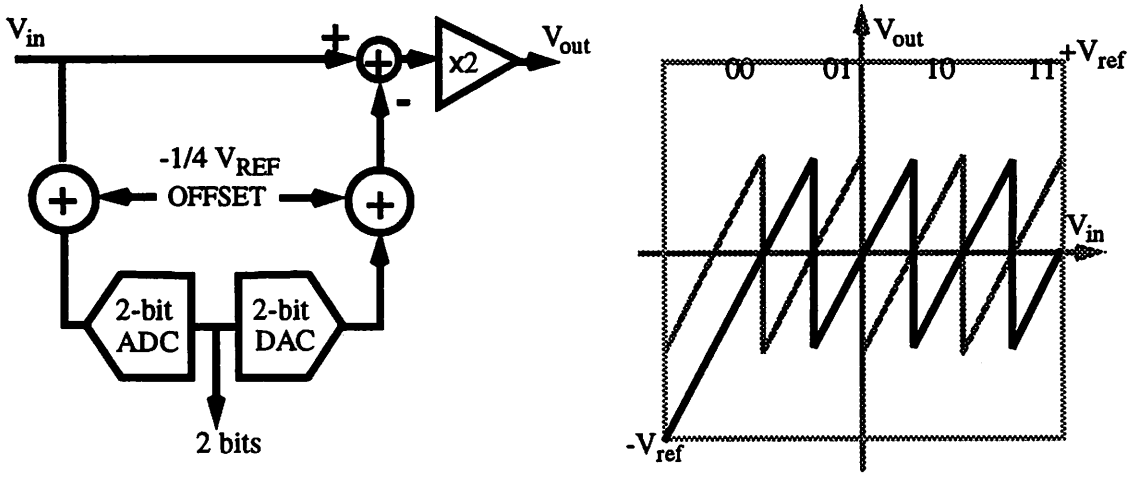


Figure 2.12 Conceptual Block Diagram of Modified Pipeline Stage and Coding

With the above digital correction algorithm, both addition and subtraction need to be present in the digital correction circuit which complicates the code assignment for the pipeline stage. Subtraction can be eliminated by intentionally adding an $-\frac{1}{4}V_{REF}$ offset to the sub-ADC and the output of sub-DAC. A conceptual block diagram and transfer function are shown in Figure 2.12. With this configuration, the sub-ADC error, up to $\frac{1}{4}V_{REF}$, can be tolerated and digital correction circuit is modified to contain adders only.

Since overranging in the transfer function can be detected by the next stage, one can simplify the design even more by eliminating a comparator at $\frac{3}{4}V_{REF}$. The final block diagram and transfer function is shown in Figure 2.13. The comparator thresholds (sub-ADC) are at $\frac{1}{4}V_{REF}$ and $-\frac{1}{4}V_{REF}$;

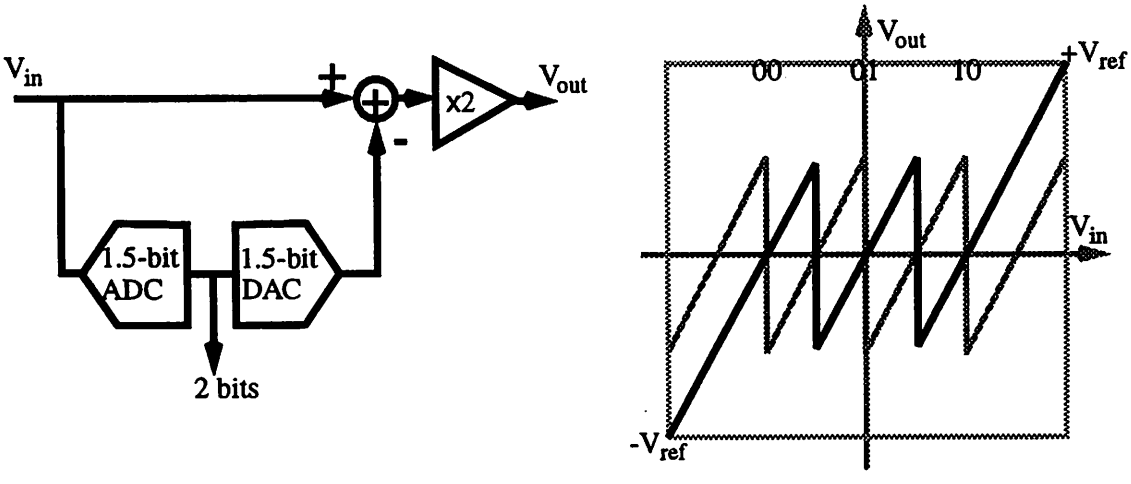


Figure 2.13 Final Block Diagram and Transfer Function with 2 Comparator Thresholds

the sub-DAC levels are at $-\frac{1}{2}V_{REF}$, 0 and $\frac{1}{2}V_{REF}$. The codes are shown on top of the transfer function and the overranging part on the transfer function will be digitally corrected by the next stage except the last stage of the pipeline. The 1.5-bit ADC and DAC here represent the effective bits per stage after digital correction [5].

2.4 Summary

In this section, the evolution of Pipelined A/D converter is presented. An power-optimized pipelined A/D converter architecture is described in detail. The low-power techniques include the choice of per-stage resolution, capacitor scaling and digital correction. It has been found for high conversion rate, a low per-stage resolution (hence low closed loop gain) is more desirable. With capacitor scaling and digital correction, each stage in the pipeline can be designed according to the noise limitation, hence reduce power dissipation.

With the above techniques, a CMOS implementation of such a power-optimized pipelined A/D converter will be presented. Some practical issues on circuit design will also be discussed.

CHAPTER 3

Circuit Techniques for Low Power, High Speed Pipelined A/D

3.1 Overview

Having determined the optimal pipelined A/D architecture, the implementation of this architecture is described in this chapter. The low power techniques used in this design include the dynamic comparators and capacitor scaling which are made possible with this architectural selection. To be compatible with the digital integrated circuit now running at 3.3V power supply, some techniques for low supply voltage are introduced, which include a 3.3V OpAmp and low voltage SC circuits. One of the modifications made to the previous design [3] was to include the digital correction circuit on chip, which provides real time digital correction. Lastly, bias circuits and clock generator are briefly described and followed by a summary.

Figure 3.1 shows the pipelined A/D architecture chosen for this design. It is consist of 9 stages in which the last stage is a flash A/D only. The analog signal is first sampled by S/H and quantized by the flash A/D in the first stage. The D/A, subtraction and amplification are accomplished by the SC circuit. The amplified output is then sampled by the second stage and identical operations are performed. The stages are interleaving and hence, the data is processed concurrently. Therefore, one can achieve high throughput with this pipelined architecture. The output digital bits from each stage are then collected and digitally corrected to achieve the 10 bit resolution.

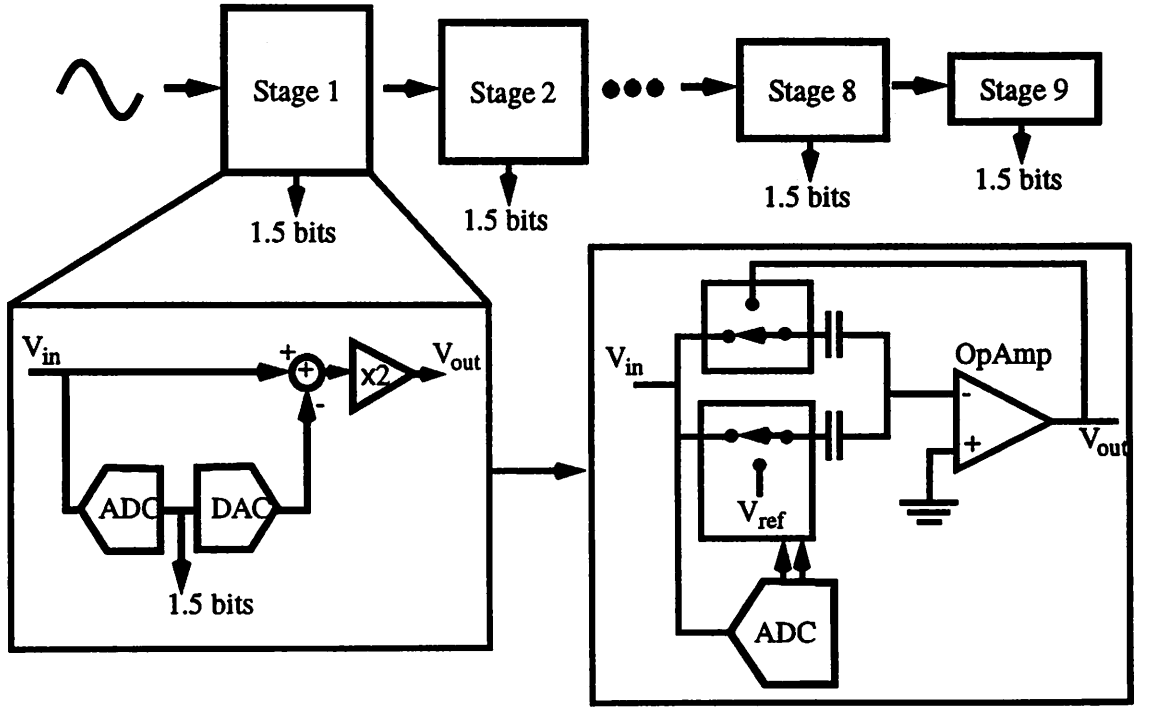


Figure 3.1 Pipelined Architecture used in this design

The per-stage resolution is chosen at 1.5 bit, mainly for two reasons. The tolerance on the comparator offset can be as much as $\pm\frac{1}{4}V_{REF}$ (described in the previous chapter) and the low closed loop gain for the SC circuit is essential for high speed operation. The capacitors in each stage is scaled appropriately for the noise requirement. The interstage gain amplifier has a gain of 2 and is implemented with a SC circuit which shares one of the sampling capacitor in the feedback path to achieve the gain of 2. (Note: for simplicity, only single ended circuit is shown in the block diagram. For practical implementations, differential signal path is employed throughout the converter.) Lastly, the subtraction is accomplished by connecting an appropriate V_{DAC} to one of the sampling capacitor.

3.2 Low Power Techniques

Having decided on the power-optimized pipelined A/D architecture from the previous chapter, the circuit is also implemented with low power in mind, pushing the limit of this architecture.

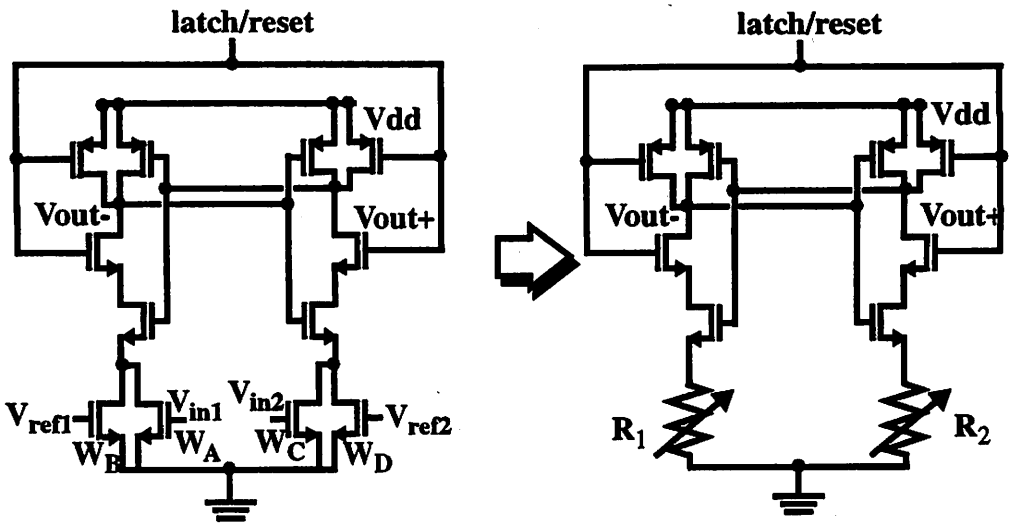


Figure 3.2 Circuit Schematic for Dynamic Comparator and its Simplified Conceptual Diagram

3.2.1 Dynamic Comparators

Employing digital correction in the pipelined architecture (described in Chapter 2), the comparator offset can be relaxed to as much as $\pm\frac{1}{4}V_{REF}$. With the chosen $V_{REF} = \pm 1V$, $\pm\frac{1}{4}V_{REF} = \pm 250mV$, dynamic comparators can be used to eliminate the static power in conventional comparators which are normally used in A/D converters. The thresholds of the comparator are designed at $\pm\frac{1}{4}V_{REF} = \pm 250mV$, determined by the digital correction and modified coding. (See Figure 2.13) Two dynamic comparators are used to implement two threshold voltages.

The circuit schematic for the dynamic comparator is shown in Figure 3.2. It is consist of two cross-coupled inverters controlled by a latch signal. The threshold of the comparator is set by two variable resistors formed with four NMOS transistors. The two parallel connected triode region NMOS's, whose gates are connected to V_{REF} and V_{IN}, determine the resistance. Shown on the right is a conceptual diagram of the dynamic comparator with two variable resistors. The conductances of R_1 and R_2 are determined by

$$G_1 = \frac{1}{R_A} + \frac{1}{R_B} = \mu_n C_{ox}\left[\frac{W_A}{L}(V_{in1} - V_t - V_{ds}) + \frac{W_B}{L}(V_{ref1} - V_t - V_{ds})\right]$$

$$G_2 = \frac{1}{R_C} + \frac{1}{R_D} = \mu_n C_{ox}\left[\frac{W_C}{L}(V_{in2} - V_t - V_{ds}) + \frac{W_D}{L}(V_{ref2} - V_t - V_{ds})\right]$$

Assuming $W_A = W_C$ and $W_B = W_D$, and $V_{ds} = 0$,the threshold of the dynamic comparator, given under the condition that $G_1 = G_2$, is

$$\frac{W_B}{W_A} = \frac{V_{in1} - V_{in2}}{V_{ref2} - V_{ref1}} = \frac{V_{in}}{V_{ref}}$$

Therefore, the ratio between W_B and W_A determines the comparator threshold. In order to achieve the threshold requirement for this architecture, the ratio of $\frac{1}{4}$ is chosen for the NMOS device sizes. By interchanging the position for V_{ref1} and V_{ref2}, the comparator with $\left(-\frac{1}{4}\right)V_{ref}$ threshold is achieved.

3.2.2 Capacitor Scaling

In an A/D converter having resolution higher than 10 bits, the fundamental noise limitation is the $\frac{kT}{C}$ noise due to sampling. [Appendix] The noise is inversely proportional to the sampling capacitor size. Therefore, for a specific thermal noise requirement, the minimum capacitor size can be determined. Assuming the A/D converter is ideal (power dissipated in charging and discharging capacitors only) except the $\frac{kT}{C}$ noise, the minimum power dissipation is set by the minimum size of sampling capacitor which satisfies the noise requirement to achieve the desired signal-to-noise ratio (SNR) without considering quantization error.

In practice, the SC power is dominated by the power dissipation in OpAmp's which drive the sampling and charging capacitors. Therefore, in order to minimize the power dissipation, one needs to minimize the power dissipation in the active circuits which, in turn, need to drive the capacitor whose $\frac{kT}{C}$ limits the SNR. In order to minimize the active circuit power, the sampling capacitors used must be at their minimum value which satisfy the noise requirement at any given

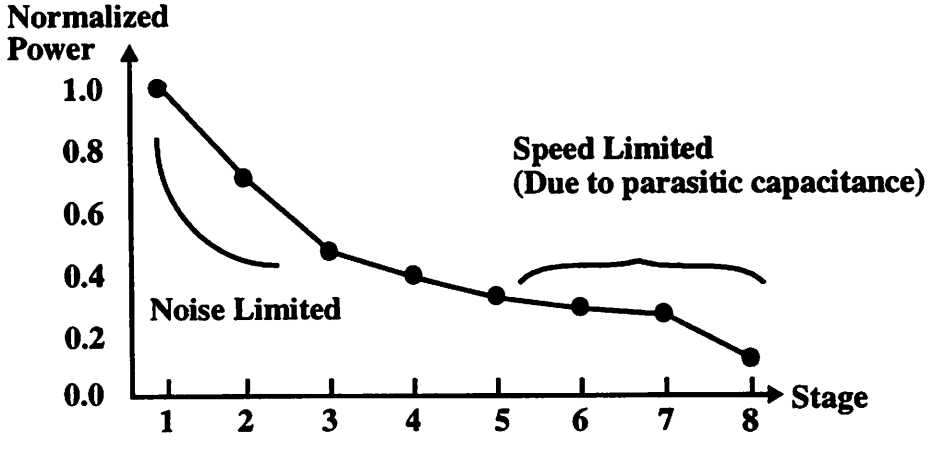


Figure 3.3 Power Dissipation of Pipelined Stages Normalized to the first stage

point of the pipeline. The sampling capacitors present themselves as loading capacitor to the previous stage, hence determine the size of the previous stage for a given sampling rate. Considering the source, load and feedback capacitors, feedback factor, speed and noise requirements, a suitable OpAmp can be designed for a particular location in the pipeline to minimize power.

As described in Chapter 2, the noise requirement relaxes greatly later in the pipeline. The effect of parasitic capacitor is becoming more and more apparent. Therefore, for later stages in the pipeline, the size of the OpAmp is mainly determined by the sampling rate rather than the noise constraint. Shown in Figure 3.3[3] is the power dissipation for each pipelined stages normalized to the first stage. It is shown that the front end is limited by the noise and the later stages are limited by the parasitic capacitance.

3.3 Low Voltage Techniques

To achieve high integration in today's integrated circuit design, A/D converter is becoming a circuit block in a large digital signal processing chip which shares the same supply voltage with the digital circuit. With the drive to low power and low voltage in digital circuits, the supply voltage for A/D has dropped to 3.3V. Inherently for analog circuits, dropping supply voltage means the loss of headroom and dynamic range which are critical to any active circuit design. In addition, for A/D converter implemented with SC circuits, low supply voltage also affects the on-resistance of MOS switches. Special techniques, described in this section, need to be employed to compensate for the loss of supply Volga.

3.3.1 2-stage 3.3V OpAmp

In the high speed pipelined architecture, the two most severe requirements of the OpAmp are the DC-gain and settling time for the first stage. To achieve 10 bit resolution, the DC gain over 60dB or 0.1% within the settling time (~11ns) is required. With minimum power dissipation in mind, it's difficult to design an OpAmp which meets all the requirements above with just a few mW's and 3.3V supply voltage.

The easiest way to achieve high gain and high speed is with a telescopic OpAmp. The signal path is only consist of NMOS transistors and the power dissipation is estimated to be small to the

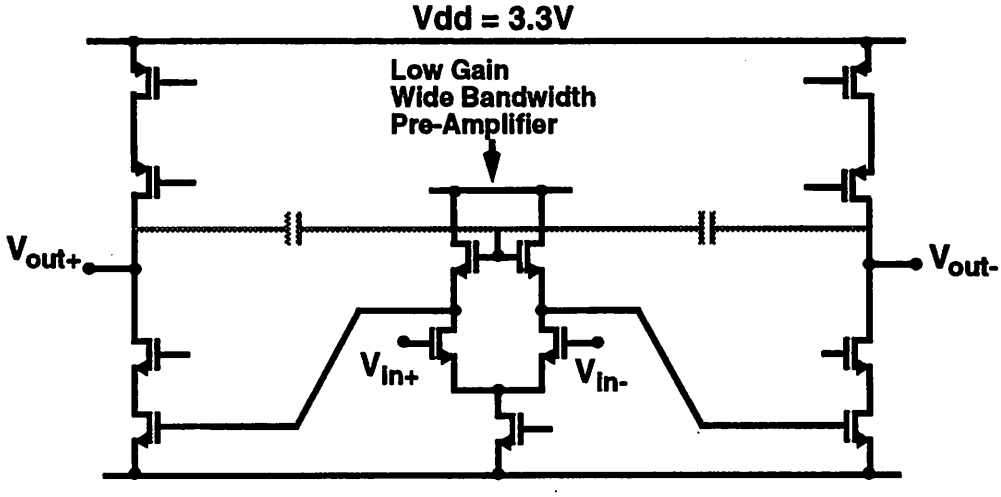


Figure 3.4 Cascode OpAmp with Low Gain Wide Band Pre-Amplifier

first order because of only one current branch. However, having multiple devices stacked on top of each other, the output swing may be small. Although the folded cascode OpAmp can achieve the necessary output swing at 3.3V supply voltage, the slow PMOS in the signal path degrades the speed of the OpAmp. And it may be difficult to achieve the DC-gain because of lower output resistance at the folding node.

To achieve high DC gain, multi-stage OpAmp with only NMOS's in signal path can be used along with pole-split compensation. However, in SC circuit configuration, having the non-dominant pole contributed from the load capacitance at the output and to drive the compensation capacitor, it's difficult to achieve the bandwidth and settling time required with minimum amount of power dissipation. Therefore, an OpAmp with the output resistance of a cascode stage and no compensation capacitor is desirable to meet the DC gain and settling time requirements.

One possible design is to use a cascode stage with a wide-bandwidth pre-amplifier shown in Figure 3.4. The core of the amplifier is consist of 2 NMOS's and 2 PMOS's cascodes and the output resistance is, to the first order, determined by

$$R_{out} = R_{NMOS} \| R_{PMOS}$$

Assuming R_{PMOS} is much smaller than R_{NMOS}, the output resistance is dominated by R_{PMOS}. Hence, the gain of the cascode stage is

$$A = gm_n r_o (gm_p \times r_o)$$

The wide bandwidth pre-amplifier is designed to have a gain of about 2. This helps to increase the safe margin for the OpAmp DC gain. This pre-amplifier is implemented with a differential pair input stage loaded with a low impedance diode-connected NMOS's to retain the wide bandwidth.

This OpAmp is consist of only NMOS's in the signal path and a desirable cascode output stage to achieve high output impedance. Furthermore, the pre-amplifier increases the effective transconductance as well as achieves the required level shift into the input of cascode stage. The dominant pole is at the output, therefore, the output load capacitance also serves as the compensation capacitor. However, the non-dominant pole is introduced at the input of the core amplifier (transconductance stage). Therefore, in order to push for the widest bandwidth possible and optimum settling time, the selection of pre-amplifier gain is critical. If the gain is too small, the effect of transconductance boost is negligible. However, if the gain is too large, the non-dominant pole will be brought down and limit the bandwidth.

Common mode feedback of the amplifier uses two capacitor connected between the output nodes and the gate of the NMOS load in the pre-amplifier. This provides a negative feedback around the transconductance stage to stabilize the output when the OpAmp is in action. (Also shown in Figure 3.4)

In the prototype, the pre-amplifier gain is chosen to be around 1.75. The gain boost amplifier is eliminated from the previous design [3], mainly due to the fact that the TSMC 0.6μm CMOS process used in this design has a reasonably high PMOS output resistance. The output resistance was verified by DC measurement of actual devices in the lab. By eliminating the gain boost amplifier, the power dissipation is further reduced for a given stage.

Running with 3.3V supply voltage, the first stage is implemented as described above. The SC circuit, simulated with the OpAmp, achieves <11ns settling time to 0.1%. The sampling capacitor for the first stage is about 350fF which is determined by the noise requirement. The load capacitance contributed from the second stage sampling capacitor is about 150fF each, and from flash A/

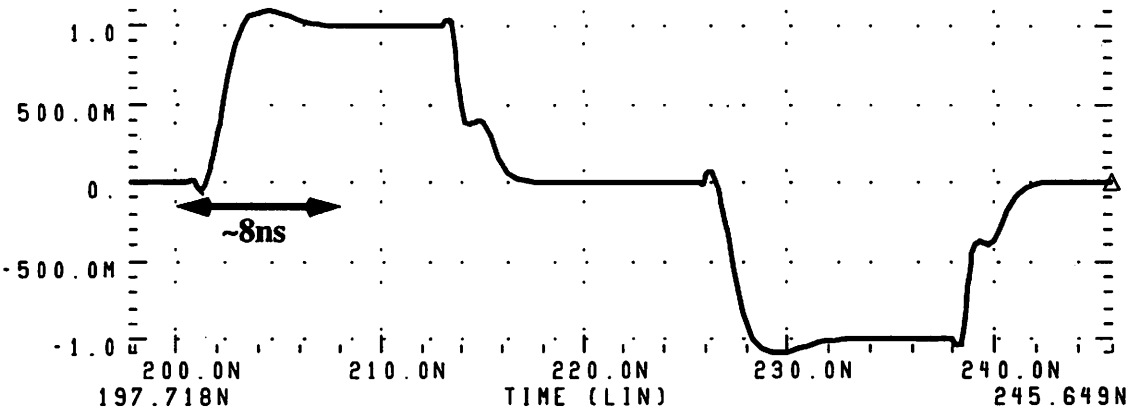


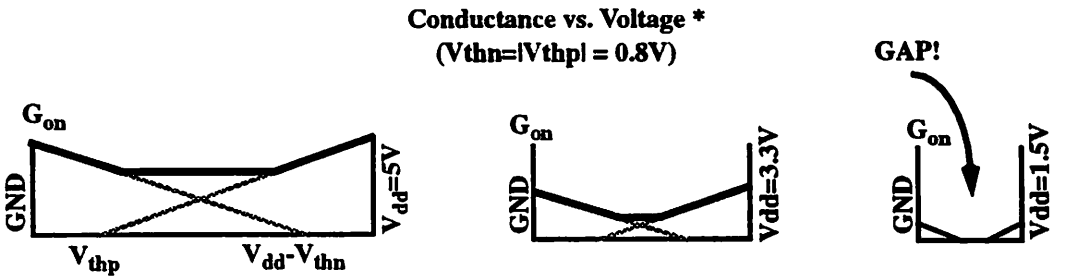
Figure 3.5 Simulation Result of First Stage SC circuit

D and wiring parasitic is on the order of 100fF. The power dissipation is estimated to be about 2.9mW for the first stage and the DC gain greater than 60dB is achieved.

3.3.2 Low Voltage SC Circuits

In switched capacitor circuits, the use of transmission gate to determine the sampling and charge transferring edge timing is essential. In conventional CMOS process, the threshold voltage is about 0.7 - 0.8V and does not scale with the supply voltage. When the supply voltage is dropped to 3.3V, the threshold voltage has become a larger portion of the supply voltage (the effective gate drive reduces), hence the on-resistance of a CMOS switch is increased. This is demonstrated in Figure 3.6.

One way to reduce the on-resistance is to use multiple NMOS's (effectively increase the width of transmission gate), however, this will also increase the parasitic capacitance associated with the switch and the RC product stays about constant. Same result with increased parasitic capacitance



*Integrated A/D&D/A Converter, OCATE, July 1991
Low Power ADC by Vlado Valencic

Figure 3.6 Conductance vs. Voltage for Different Supply Voltages

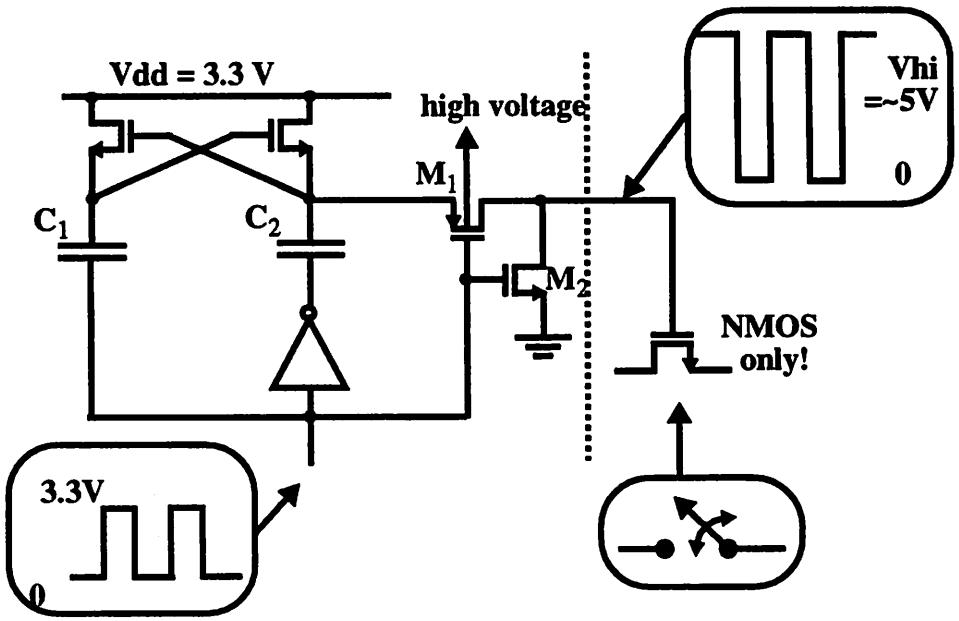


Figure 3.7 Charge Pump circuit to boost the Clock Voltage

is obtained with the use of both NMOS and PMOS transistors. Another possible solution is to reduce the threshold voltage for the switches. However, this requires a few extra mask steps in the process which are not available in typical CMOS process. The only option left is to increase the gate drive to the traditional 5V by either a DC-DC converter to create a global 5V supply or clock booster to generate a 5V clock.

The approach chosen here is to create an individual clock booster circuit locally for each transmission gate rather than a global 5V supply for the clocks. This approach will eliminate the possibility of cross-talks between different clock lines which might be coupled through the supply in the global 5V supply case and minimize the number of circuits running at 5V supply to reduce power dissipation. The approach is implemented with a dynamic charge pump circuit shown in Figure 3.7. By applying a 3.3V clock input, the capacitors C_1 and C_2 are self-charged to 3.3V through the cross-coupled NMOS transistors. And an inverted clock (when the input clock is low) will pump the voltage on C_2 to be greater than 3.3V and the PMOS M_1 will be ON to transfer the voltage to the NMOS switch. This ratio is determined by

$$V_{hi} = 2V_{DD}\frac{C_2}{C_2 + C_{parasitic} + C_{G,switch}}$$

Transistor M2 is responsible to discharge the high voltage node to ground when the input clock is high. Hence, the charge pump circuit is inherently an inverting stage and the 3.3V clock signal is converted to be a 5V clock signal. And because this high voltage generated is close to 2Vdd, and the analog common mode voltage is around 1-2 volts, only NMOS switches are necessary for the SC circuits in the pipeline.

To avoid latch up in the circuit, the well potential of the PMOS M_1 needs to be at least $V_{hi} - V_{pn}$. A high voltage generator is shown in Figure 3.8 for this purpose. By removing the discharging transistor M_2 from Figure 3.7 and increase charging capacitor (C_1 and C_2) sizes, the output will sustain a relatively high voltage as long as the input clock is applied. Lastly, because this is a 5 volt CMOS process, the reliability of charge pumping to ~5 volt will not be an issue. However, when a smaller feature size is used, charge pumping should be used with caution.

3.4 Digital Correction Circuit

In the previous design[3], the raw digital bits from each stage are collected and the digital correction is performed after the output samples are taken in the PC. In order to see the correct 10 bit output from the A/D converter, digital correction circuit needs to be integrated on chip. This also allows a real-time feedback for the gain control in the RF receiver application.

Since the stages in the pipeline are interleaving (meaning when odd stages are sampling, even stages are evaluating), the outputs for a given input sample are present at a $\frac{1}{2}$ clock cycle interval and progresses down the pipeline. When the output from the first stage is ready, the output from

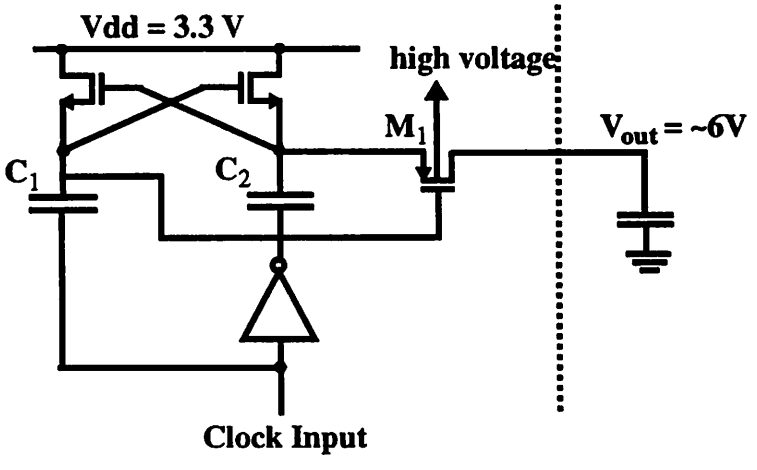


Figure 3.8 Charge Pump circuit for high voltage

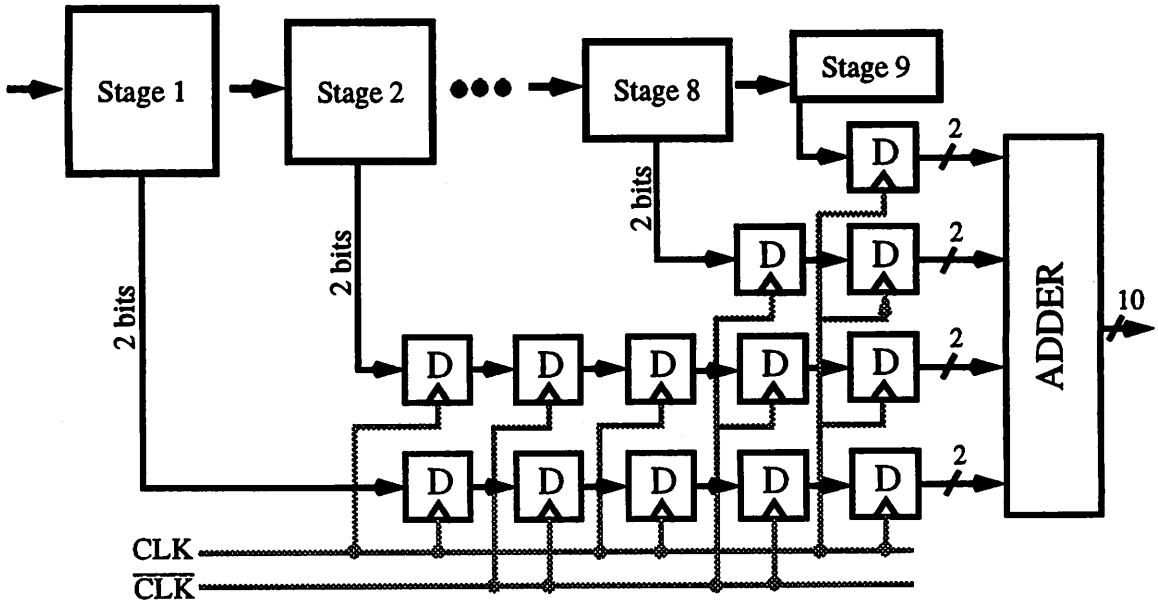


Figure 3.9 Conceptual Diagram for Digital Correction

the second stage will be ready $\frac{1}{2}$ clock cycle after, etc. Therefore, the sampled input signal can not be corrected until the last stage has finished the conversion.

Because of modified coding, only addition is required in the digital correction. Figure 3.9 shows a conceptual diagram of the digital correction. The output from stage N is delayed by $\left\lceil \frac{9-N}{2} \right\rceil + 1$ clock cycles before it's being corrected. The correction is done by taking (N+1)th stage output and added to Nth stage output with one bit overlap from the LSB. The carry will propagate in the direction of MSB. The maximum code each stage can output is 10 after modified coding; assuming a full scale input is applied, the full scale resolution of A/D conversion, after digital correction, will give 1023 codes (1 code short of ideal 10bit 1024 codes). This generally does not create a problem for normal operation.

The delay block is implemented with a P/N transmission gate and an static inverter; the adder is done with a full adder from standard digital library to minimize the design time. The silicon area for the digital correction is 340μm x 170μm and the power consumption is less than 3mW at 40MS/s and 3.3V power supply.

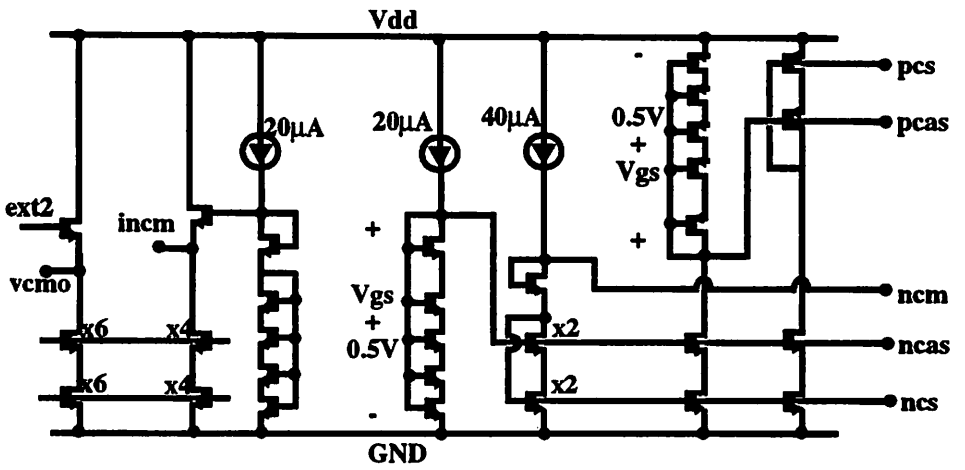


Figure 3.10 Circuit Schematic for OpAmp Bias Circuit

3.5 Bias Circuits and Clock Generation

The final section of the A/D implementation is the bias circuits and clock generation. Because of OpAmp scaling in the pipeline, bias circuits need to be designed carefully to ensure the OpAmp from each stage is operating within the proper range. Clock generation is also critical due to the fact that rise/fall edges and delay need to be carefully controlled to guaranteed precise SC circuit action. And with the increase in sampling rate (shorter clock period), rise/fall time and jitter are becoming larger portion of the clock period.

Figure 3.10 shows the circuit used to bias up the OpAmp. From the OpAmp schematic shown in Figure 3.4, two PMOS and one NMOS bias voltages are required for the cascode stage. A NMOS current source for the differential pair tail current is needed for the pre-amplifier; as well as the gate voltage for the pre-amplifier load transistor. Because each OpAmp has a different size, an unit bias condition is chosen in the bias circuit which is scaled appropriately in each OpAmp by scaling current mirrors. The DC characteristic of an ideal square law device is examined

$$V_{Dsat} = V_{gs} - V_t = \sqrt{\frac{2I_d}{\mu_n C_{ox}\frac{W}{L}}} = \sqrt{\frac{2\rho L}{\mu_n C_{ox}}}$$

If minimum channel length is used (L fixed), V_{Dsat} is only a function of ρ which is the current density, $\frac{I_d}{W}$, of a device. In another word, if the current density is fixed in the OpAmp, the bias condition for the OpAmp will be the fixed. Therefore, 1μA/μm is chosen to be the unit bias condition

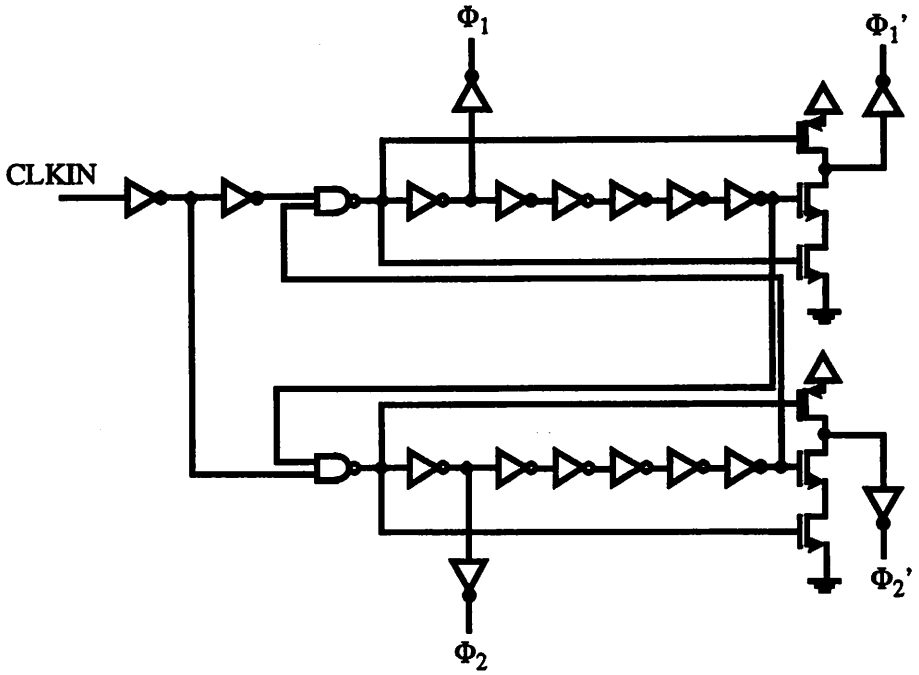


Figure 3.11 Block Diagram for Clock Generator

in the bias circuit and the current and width is scaled appropriately to keep the same current density for all stages.

The circuit is biased up with a 20μA current source driving a chain of triode devices to generate the necessary V_{ds} for the bottom current source. The diode connected NMOS provides the bias voltage for the gate of NMOS cascode device and tracks with the process to the first order. The similar idea is replicated for the PMOS bias voltages. The input common mode voltage, to reset the OpAmp, is generated in the similar fashion; where as the output common mode voltage is controlled externally. Two identical bias circuits are used, each provides bias voltages to four stages in the pipeline. This is to reduce the noise coupling through the bias lines. Each bias line is heavily bypassed with large on-chip capacitors to reject any AC signal that might be resident on the line.

Clock inputs are necessary to operate the SC circuit. Because multiple tasks take place during one clock cycle, the triggering edge of the clock signal need to be carefully controlled. Because the pipeline A/D performs conversion in a interleaving fashion, two sets of clock (clock or $\overline{\text{clock}}$) is required for even and odd stages. Figure 3.11 shows the block diagram of a clock generator.

When a reference clock is provided (CLK), the output Φ_1 and Φ_2 are 180 degrees out of phase. And Φ_1 and Φ_1' are separated by six inverter delays, where Φ_1' is used to trigger the digital logic and Φ_1 is the sampling clock. The small delay between these two phases is to ensure a quiet sampling edge when the input sample is taken. Four stages of buffer are added at each output to drive the wiring capacitance, as well as the input capacitance to the charge pump circuits.

The rise and fall time were simulated to be less than 1ns for 40MHz clock input. The delay between Φ_1 and Φ_1' is about 1ns, hence, the sampling is finished before the clock edge triggers the logic circuit. The power consumption of the clock generator including the buffer is estimated to be less than 3mW.

3.6 Summary

This chapter describes the implementation of the power optimized pipelined A/D architecture presented in Chapter 2. Taking advantage of the large offset tolerance on the comparator, a dynamic comparator, hence no DC power, is used. To avoid overdesigning by duplicating pipeline stages, scaling on OpAmp and capacitors, which pushes the noise limitation, is employed. Since the goal of high integration causes the supply voltage for A/D to decrease to 3.3V, a high gain, low voltage OpAmp is described here. The OpAmp achieves the required settling time and gain for 10 bit 40MS/s requirement. Lastly, charge pump circuit is shown to boost the 3.3V clock pulses to 5V, to reduce the on-resistance of MOS switches.

The circuit is designed, layout and fabricated with 0.6μm CMOS DPTM process and the experimental result will be shown in the next section.

CHAPTER 4

Experiment Prototype and Measurement Results

4.1 Prototype

A prototype of the pipeline A/D converter is designed and fabricated in 0.6μm CMOS DPTM process. The architecture used is described in Section 2.3 with nine pipeline stages where the last stage is only a pair of comparators. The sizes of beginning stages are scaled according to the noise limitation for optimum power and later stages are scaled to meet the speed requirement of the converter. The SC circuit in the first three stages also contains digital calibration, in essence, small capacitors are digitally switched between the sampling and feedback capacitor to compensate for capacitor mismatches. A die photo is shown in Figure 4.1. The active area is measured 1.2μm x 1.2μm shown on the right hand side of the die photo (Figure 4.1). Since the die size is fixed for this fabrication run, extra digital circuitry is added on the left, along with some dummy metal lines for process yield purposes.

The floor plan of the layout is to place the first four stages on top and fold the last five stages to the bottom to minimize the wiring capacitance on the clock lines and form a square active area. The clock lines are routed in the center of the active area where the appropriate phases are tapped off at the location of each stage in the pipeline. Although the analog circuits are scaled down the pipeline, the digital section remains roughly the same size for all stages. It is apparent from the die

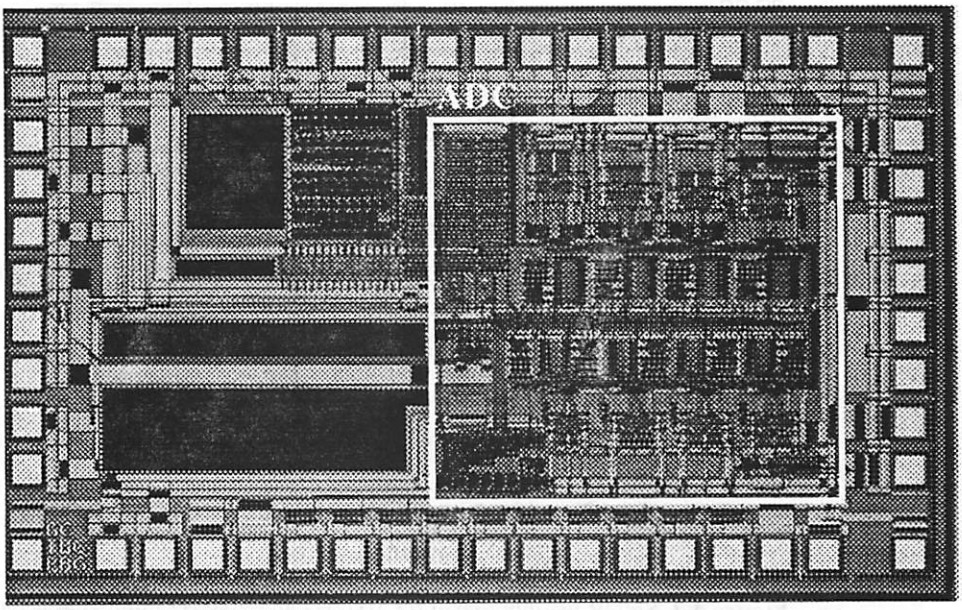


Figure 4.1 Die Photo

photo that the analog section which is away from the center line is scaled down the pipeline; where as the digital section which is close to the center clock lines stays about the same size. Digital correction is at the lower left corner of the active area; and 10 bit output is produced at the pads on the bottom.

The prototype of the A/D converter is, instead of mounted in a conventional package, mounted on a printed circuit board with chip-on-board technology. This technology allows silicon dice to be attached directly onto a printed circuit board which has very fine bondwire landing pads (similar to the ones in conventional packages.) This technology greatly reduces the bondwire and lead inductance because the die can be placed extremely close to the pads.

4.2 Experimental Results

The chip is fabricated and a printed circuit board is produced using the chip-on-board technology (described in the previous section). Figure 4.2 shows the SNDR vs. Input level for 100kHz and 20MHz sine wave inputs sampled at 40MS/s. The peak SNDR is 58.8dB for 100kHz input. A degradation in higher input frequency is expected due to the fact that the first stage does not have a dedicated S/H to drive the first stage input capacitors and flash A/D. The flash A/D is triggered at

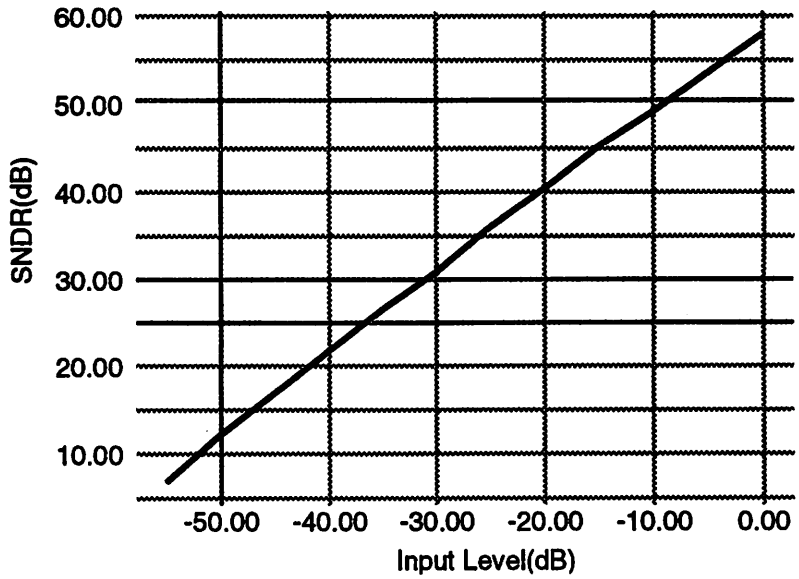


Figure 4.2 SNDR vs. Input level for 100kHz and 20MHz input sine wave

four inverter delays after the input signal is sampled; for higher frequency input, the difference between the inputs sampled by the capacitor and flash A/D might be large, hence create a large nonlinearity. However, for some applications, the input to the A/D is a held SC circuit output (Section 4.3), S/H is not required.

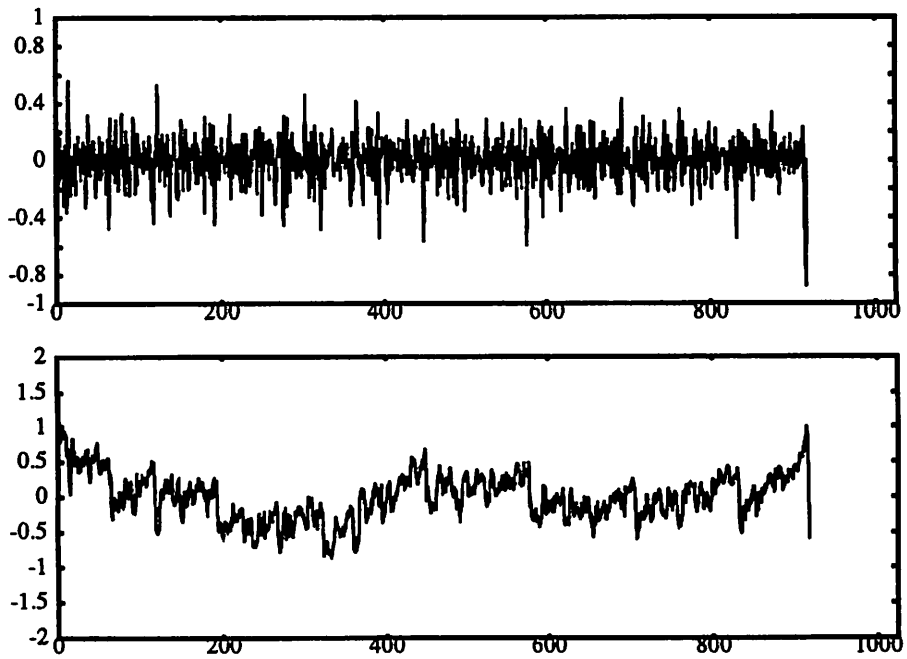


Figure 4.3 DNL and INL results

Code Density Test shows the DNL and INL are within one LSB, shown in Figure 4.3. A layout error, associated with a leaking pn junction at a critical node, had been found in this design. Silicon microsurgery had been done to fix the error. Although the SNDR has improved to a 10-bit resolution at 40MS/s; for a slower sampling rate, the SNDR decreases. It is believed that some connections for later stages were not made with the silicon microsurgery (about 50 connections were required to fix the error). The large offset in the output codes might also be contributed by the layout error.

4.3 Integrated A/D with DECT receiver

As an example of high integration, in addition to the stand alone A/D chip, it is also integrated with a RF receiver chip which is currently under development in the research group. The simplified block diagram is shown in Figure 4.4. The RF input signal is first amplified by the LNA (low noise amplifier) and frequency translates to baseband. (Note: Frequency translation can be done in several different ways. Since it is not the focus of the thesis, it will not be discussed here. Details can be found in other publications from the research group. [19]) After some low pass filtering and gain control, the signal is digitized by the A/D which outputs the digital representation of the information content to the DSP section. The specification of Digital European Cordless Telephony system (DECT - the system under development here) calls for a sampling rate of ~1MS/s or 10MS/s with resolution about 8 bits. This A/D is sufficient to satisfy the requirement.

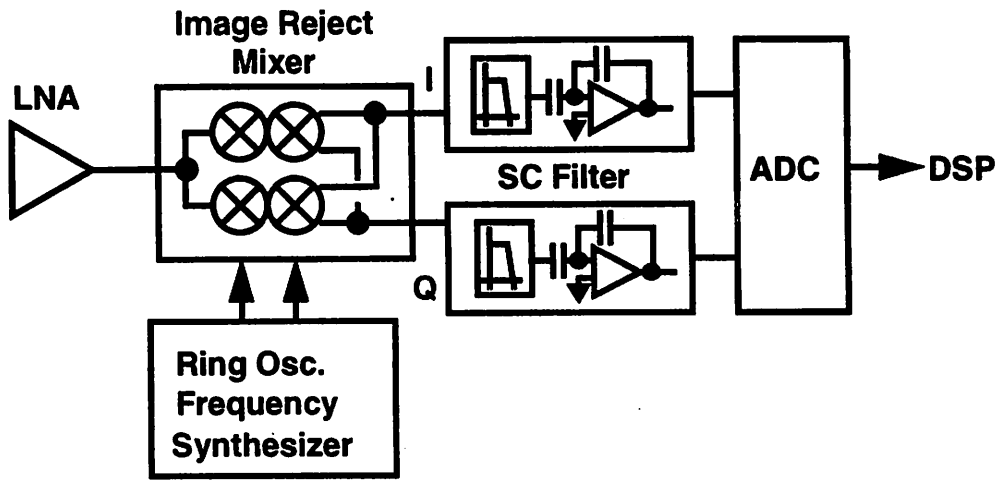


Figure 4.4 Simplified Diagram of a RF Receiver Architecture

Since the sampling rate is much slower, the settling requirement for each stage is relaxed. Therefore, the bias current for the active circuits can be scaled down to reduce the power consumption. Minor modifications need to be made to taylor the A/D to fit in the receiver chip. These include redesign on clock generator and re-routing of clock lines and output lines. Differential output with an attempt to minimize the noise injected into the substrate from the full CMOS logic swing is used. All the blocks shown in Figure 4.4 are implemented onto one single die including the ring oscillator based frequency synthesizer. The chip is currently under evaluation.

4.4 Summary

Experimental results for a 28mW 10b 40MS/s pipelined A/D converter is presented. Taking the advantage of scaled technology, the power dissipation and sampling rate of a pipelined converter have improved. The power comparison with some recent work is presented in Figure 4.5. The power consumption is close to what was predicted in [3] for the scaled technology.

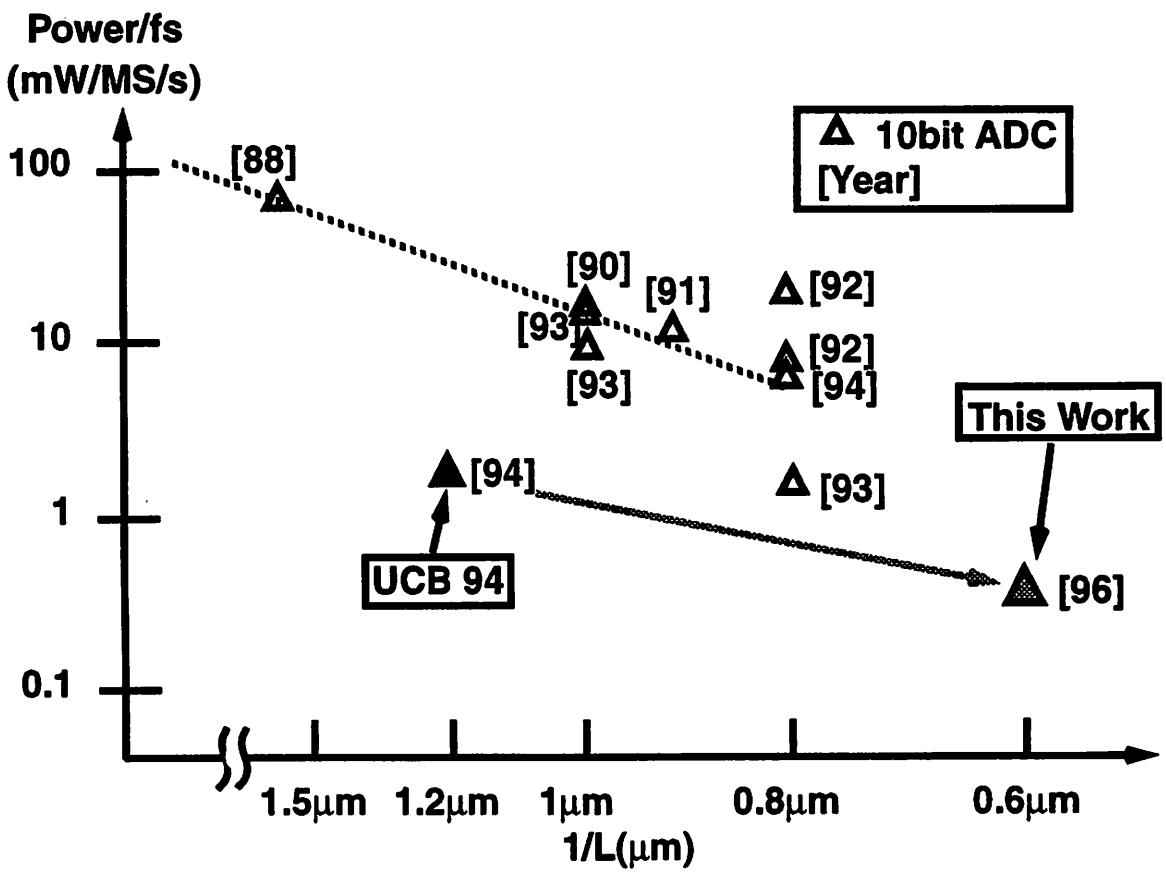


Figure 4.5 Normalized Power Comparison of Recent 10b ADC

CHAPTER 5

Conclusion

5.1 Conclusion

A high speed, low power and low voltage A/D converter with scaled technology has been investigated here. A prototype which achieves 28mW 10b 40MS/s A/D is presented. It has also been demonstrated that CMOS A/D can be integrated with other circuit blocks in a large system. For that, the prototype is integrated with a monolithic CMOS RF receiver for DECT system.

The techniques which contribute to the goals of this research can be categorized into two sections. In architectural level, the choice of per-stage resolution, coding and digital correction relaxes the requirements on some active circuit blocks which are conventionally known as power hungry blocks. Capacitor scaling (i.e. pipeline scaling) minimizes the overdesign for later stages in the pipeline. In circuit level, taking advantage of digital correction, dynamic comparators are used to eliminate static power consumption. Capacitor scaling reduces the OpAmp sizes for later stages. A high speed, low voltage OpAmp with a pre-amplifier and cascode transconductance stage is used to achieve fast settling and high DC gain. Lastly, clock boosting circuit is used to reduce the on-resistance due to low supply voltage.

A prototype is built in 0.6μm DPTM CMOS process and measured results are shown in Chapter 4. At conversion rate of 40MS/s, the A/D achieves a max SNDR of 58.5dB with 100kHz input. And DNL and INL curves show a good correspondence of the SNDR results.

In conclusion, having architectural and circuit techniques combined with scaled technology, a high speed, low power and low voltage A/D can be achieved. The next step will be to look into the effect of integrating such an A/D converter as a circuit building block in a larger system and how to deal with integration problems, such as substrate noise coupling, supply bounce, etc.

5.2 Power Comparison

As the CMOS technology scales to a smaller feature size, it is apparent that digital circuits will benefit from it in speed, power and area. These benefits can not be applied to analog circuits directly simply because the figures of merit in analog circuits extends beyond speed, power and area. Since the A/D converter is becoming a building block in a larger DSP or communication system, it is essential to study how the technology scaling will affect the performance of a mixed signal block, such as an A/D converter.

The comparison shown below will be between the 35mW 10b 20MS/s pipelined A/D converter in 1.2μm CMOS process and the 28mW 10b 40MS/s pipelined A/D converter in 0.6μm CMOS process. First, power savings in digital section due to technology scaling is examined. Following that is an attempt to compare the SC circuit when the performance is limited by $\frac{kT}{C}$ noise. Lastly, a quick look at the SC circuit when parasitic capacitance is limiting the performance. In order to simplify the comparison, the sampling rate for the 0.6μm example is first scaled to be 20MS/s (the same as the first case.) Then the effect of doubling the conversion rate will be discussed.

5.2.1 Digital Section

The digital section in this A/D design includes the clock generator, comparators, DAC logic and charge pump circuit. (in the 0.6μm example, the digital correction circuit is also included.) The power dissipation for a digital circuit is generally described as

$$P = C \cdot V^2 \cdot f$$

where f is the clock rate of the circuit. For a given sampling rate and supply voltage, the power dissipation is only a function of capacitance (shown in equation above). Assume, to the first order, the $\frac{W}{L}$ ratio is the same for both designs, only $\frac{1}{2}W$ for each device is required for the scaled process. Further assume that C_{ox} is increased rougly by a factor of 2[1], technology scaling makes the gate capacitance $\frac{1}{2}$ of that in the 1.2μm version. (shown in equations below)

$$C_{gs} = W \cdot L \cdot C_{ox}$$

$$C_{gs}' = \frac{W}{2} \cdot \frac{L}{2} \cdot 2C_{ox} = \frac{1}{2} \cdot C_{gs}$$

In addition to the gate capacitance, parasitics also play a very important role in power dissipation.

The effect of technology scaling on source/drain parasitic capacitance is not obviousbecause it depends on doping density, junction depth, source/drain area scaling, etc. If we assume that parasitics are only affected by the scaled feature size, the ratio of the source/drain parasitic capacitance between 1.2μm and 0.6μm process is roughly 2. Other sources of parasitics capacitance, such as wiring, overlapping, also change with technology. Although the line width of a metal line may decrease with technology, the coupling between two adjacent metal lines tend to increase because the minimum separation between metal lines are decreased. Other minor factors, such as metal resistance requirement, may determine the width for a long metal wire which will also affect the parasitic capacitance. In general, because the overall die size is about $\left(\frac{1}{2}\right)^2$ smaller, we can assume that the parasitic (if dominated by wiring and overlapping) is roughly $\left(\frac{1}{2}\right)^2$.

In summary, the power saving for the digital section in an A/D converter running at the same sampling rate is roughly between $\frac{1}{4}$ and $\frac{1}{2}$ depending on the dominating factor between gate and parasitic capacitances. One good example is the clock generator circuit. For the same $\frac{W}{L}$ ratio, the gate capacitance in the scaled technology is about $\frac{1}{2}$ of the previous version. In addition, parasitic capacitance is roughly $\frac{1}{4}$ of the 1.2μm version. Therefore, a power savings of $\frac{1}{4}$ to $\frac{1}{2}$ is expected

1. Cox for 1.2μm CMOS process is 1.55 fF/μm^2 and for 0.6μm CMOS process is 2.41 fF/μm^2.

for the scaled 0.6μm process. In the lab, the power is measured to be xxmW for the 1.2mm case and 2.2mW for 0.6μm case.

5.2.2 kT/C Limited Power Comparison

The power analysis for analog circuits is not quite as straight-forward as the digital circuits. Since the sampling capacitor in this design are scaled according to the noise requirement in the first few stages and settling requirement in the later stages, these two cases will be examined independently in the context of power dissipation with scaled technology.

In the 10-bit example, the capacitors in the first stage is determined by the $\frac{kT}{C}$ noise limitation, therefore, the required capacitor size is the same in both technologies. For a fixed conversion rate, the required time constant would also be the same and it follows,

$$\frac{1}{\tau} = \frac{g_m}{C_{load}} \cdot f$$

where

$$f = \frac{C_F}{C_F + C_S + C_{opamp}} \text{ and}$$

$C_{load} = C_F \cdot (1 - f) + C_L$ where C_L is the load capacitance from the next stage.

Let's assume the C_{load} and feedback factor, f, stay roughly the same value because parasitic capacitances are generally insignificant in this OpAmp topology. To get the same τ, g_m needs to be the same where it follows the equation

$$g_m = \mu_n C_{ox} \cdot \frac{W}{L} \cdot V_{DSat} = \frac{2 \cdot I_D}{V_{DSat}}$$

Assume V_{DSat} stays the same for both technologies. If C_{ox} is increased by a factor of 2 and L is decreased by a factor of 2, W only needs to be $\frac{1}{4}$ of the previous design to maintain the same g_m. From the second part of the above equation, it is obvious that I_D will remain the same, hence the power dissipation is the same to the first order.

In the 1.2μm design, a gain boost amplifier is used to compensate for the low output resistance on the PMOS transistors. The amplifier is eliminated in the 0.6μm design because the output resis-

tance performance is reasonably good. And by using longer channel devices, a sufficient output resistance can be achieved with the cascode PMOS current source. The power used in the gain boost amplifier was about 30% of the entire OpAmp. By eliminating it, the power dissipation is reduced significantly.

In reality, since C_S is kept the same for noise reasons, f_t is higher in the scaled technology for a particular bias condition and a fixed g_m. This translates to an increase of speed with the same power dissipation. Furthermore, V_{DSat} can also be lowered in the scaled technology to increase g_m. Also if we re-examine the SC circuit more carefully and with the condition described in the previous paragraph, the parasitic capacitances for both the OpAmp input and source/drain output capacitances are smaller in the scaled technology than the 1.2mm design. This improves the feedback factor, as well as the settling time.

In conclusion, most of the power saving in the scaled technology comes from the elimination of the gain boost amplifier. Although the analysis above shows no power gain in the amplifier; in reality, higher sampling rate is achieved with roughly the same amount of power in the noise limited stages. The increase of feedback factor due to the reduced parasitics also improves the power dissipation. It's been shown that the power dissipation for the first pipelined stage is ~4.5mW for the 1.2μm (20MS/s) case and ~3mW for the 0.6μm (40MS/s) case. (a power saving of roughly 30%, mainly due to the elimination of the gain boost amplifier.)

5.2.3 Parasitic Limited Power Comparison

In the later stages of the pipeline, the limitation on the capacitor is no longer the $\frac{kT}{C}$ noise, instead is determined by the parasitic capacitance. (i.e. the C_S and C_F need to be sufficiently larger than the parasitic to have a reasonable feedback factor.) By using an iterative method, the size of the OpAmp and capacitors are determined by the speed requirement of the A/D converter. If the A/D in both cases are running at the same speed, less parasitic capcitance, hence smaller capacitors and OpAmp, will contribute to lower power dissipation.

To achieve the same conversion rate, the same time constant is required for both cases. If the C_{load} is determined by the parasitic capcitance, it is decreased by about a factor of 2 when the technology is scaled. The factor of 2 comes from the fact that the parasitic capacitance is domi-

nated by the gate and source/drain capacitances in OpAmp's. And as described in the previous section, the capacitance for these is scaled by roughly a factor of 2 due to scaled geometries. This means g_m can be scaled by a factor of 2 as well. If V_{DSat} is kept constant for the OpAmp, the current required can be reduced by roughly a factor of 2, which translates to a power saving of $\frac{1}{2}$.

In conclusion, the power savings of 2 is estimated for parasitic limited pipelined stages running at the same speed. However, the power of these stages is usually insignificant in comparison with the overall power dissipation of the A/D converter because of the capacitor scaling which was used in the design. In the 1.2mm example, the first stage power dissipation is ~4.5mW where the last stage only consumes ~0.5mW.

To summarize, since the line between the $\frac{kT}{C}$ noise limited stage and parasitic limited stage is not clear, the power savings in analog circuit will be roughly less than $\frac{1}{2}$. (in $\frac{kT}{C}$ limiting case, power reduction is less than a factor of 2, mainly due to the increased f_t and decreased V_{DSat}; and in parasitic limiting case, the power saving is roughly a factor of 2.) However, because the elimination of the gain boost amplifier with the scaled process, the 30% of power is reduced with no penalty.

5.2.4 Conclusion

In conclusion, although a power saving is intuitive with scaled technology, it is difficult to quantify the power saving factor in relation with the technology scaling factor. However, from the above discussion, power dissipation in digital section will improve between $\frac{1}{2}$ and $\frac{1}{4}$; where the analog section will improve by roughly $\frac{1}{2}$ for a given samlping rate. The measured power dissipations for both cases running at 20MS/s are 35mW for 1.2μm and 17.4mW for 0.6μm; of which about 50% of power is dissipated in digital circuits. A factor of 2 in power saving is observed with the scaled technology which was predicted earlier in this chapter.

When pushing the sampling rate to the limit of technology, the 1.2μm achieves 20MS/s at 35mW, where as the 0.6μm achieves 40MS/s at 28mW. Doubling the sampling rate will double the power dissipation in digital circuits; therefore, the power saving of $\frac{1}{2}$ factor is compensated for the higher speed. In analog circuit, no power saving is observed for doubling the sampling rate in the

scaled technology; however, the elimination of gain boost amplifier reduces the power. Essentially, with a scaled technology, one can achieve a higher sampling rate with no power penalty.

Appendix A

Reference Voltage Generator

A.1 Introduction

In any A/D converters, some reference voltages are generally required to set a reference for the sampled input to be compared to. The accuracy of the reference voltages need to be as linear as the converter itself in most cases. For example, in flash converters, reference voltages are compared with the sampled input signal. Any error present on reference voltages will be added directly to the nonlinearity of the converter. The problem becomes even more severe at high resolution and high speed. In a high speed converter, switching noise on the chip can be coupled onto the reference lines and corrupt the conversion process.

Traditionally, there are two ways to generate reference voltages either by using a resistor string or capacitor array. Each one has its own limitations. It will be shown in Chapter 3 that with some architectural differences, the number of required voltage references has been reduced to two and the tolerance is relaxed with some trimming capacitor.

A.2 Resistor String Voltage Reference Generator

By using multiple passive resistors, one can generate several potential between supply and ground. In the case of a flash converter, the number of reference voltages required is 2^N, where N

is the resolution of the converter. By using 2^N equal value resistors in a string, one can interpolate 2^N different reference potentials between the supply and ground (or full scale input). Two major problems seen at this point are the matching of resistor and high speed operation.

Since the flash converter relies on the absolute value of the reference voltages, mismatch between the resistors during process will cause nonlinearity on the reference voltages. This directly affects the linearity of the output bits. For high resolution, where the LSB size is small, the tolerence on voltage references is even tighter.

For high speed operation, many sampling capacitors might be switched to a reference voltage on the resistor string. This will create a glitch on the refernece, and needs to settle (with the RC time constant) to the required accuracy within the period allowed. The largest RC time constant appears in the center tap of the resistor string, where the equivalent resistor value is $2^{N-1}R \| 2^{N-1}R$ (shown in Figure 1). This transient response causes a signal dependent settling of the DAC and creates harmonic distortion. In order to settle fast enough, small resistor value can be used; however, larger power will be dissipated for the voltage reference generation.

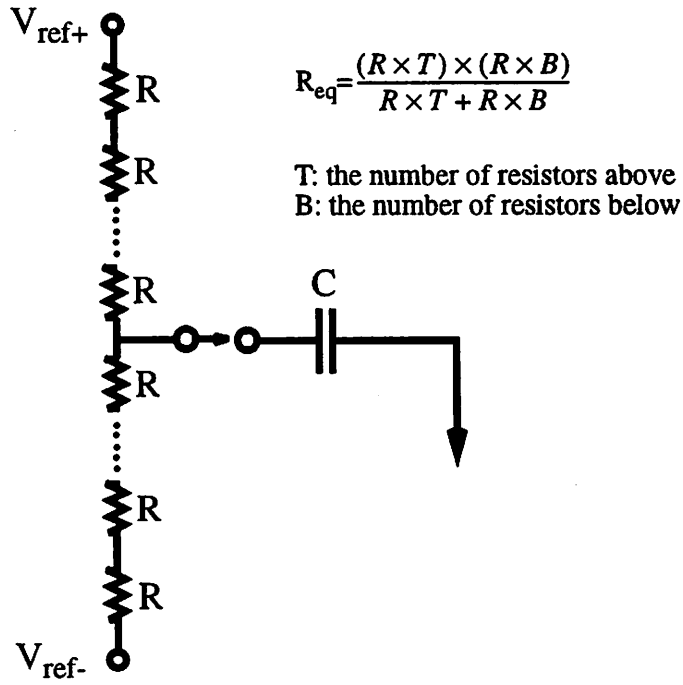


Figure A.1 Time Constant for a tap on the Resistor String

Assuming high power can be tolerated, the mismatch of resistors in the process will still determine the overall linearity of the A/D.

A.3 Capacitor Array Reference Voltage Generator

Another way to generate reference voltages is to use an array of binary weighted capacitors. A family of A/D converters based on this idea is called the successive approximation ADC's. The input is first sampled onto capacitors and then compared with a reference voltage to determine MSB. Then, the quantized MSB is added or subtracted from the input signal to zoom in to next bit resolution.

The typical binary weighted capacitor array is shown in Figure 2. The input is first sampled onto the capacitor array. If $V_{ref} = 0$, the bottom plates of the capacitors are grounded and $-V_{in}$ appears on the top node. However, if one of the capacitor is connected to V_{ref}, the output voltage magnitude will be reduced by the ratio of the specific capacitors to total capacitance times V_{ref} (shown in Figure 2). With this method, V_{ref}'s can be generated equivalently with the capacitor array by connecting various capacitors to the appropriate reference line.

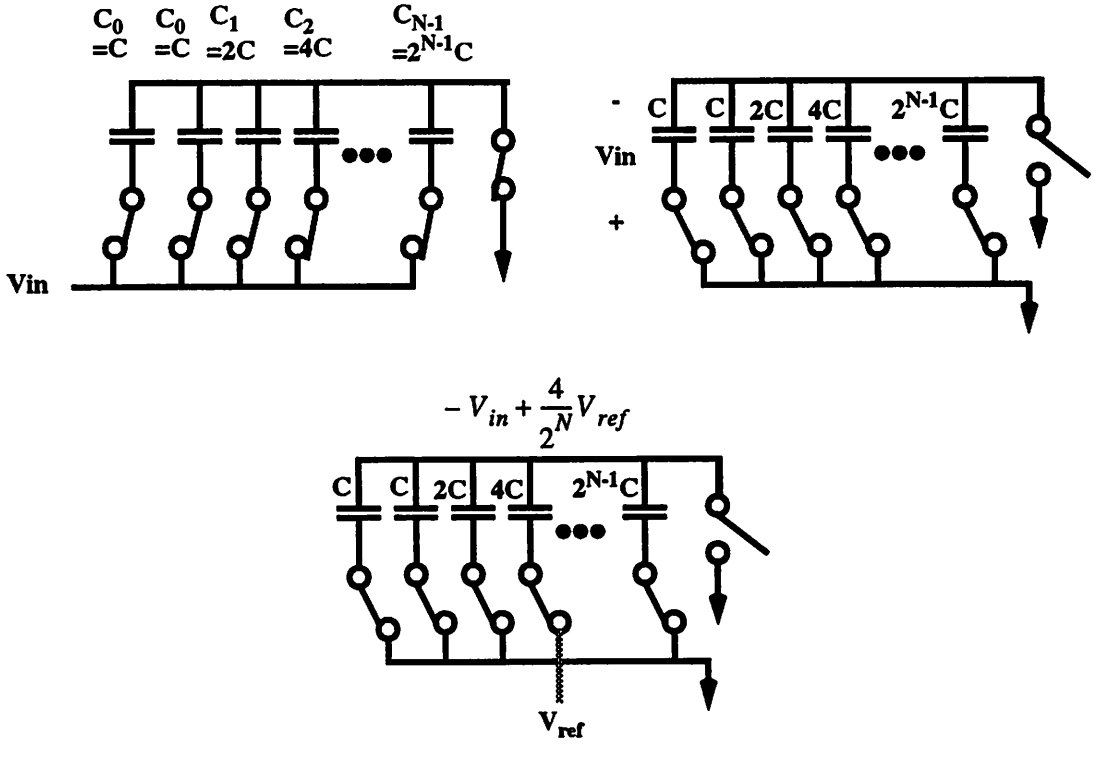


Figure A.2 Capacitor Array Voltage Reference Generator

Although this method does not require static power, the accuracy of the reference generation still relies on the absolute matching of the capacitors. Special techniques have been introduced over the years to improve the matching, however, without special trimming, the achievable resolution is about 8-9 bits.

It will be introduced in later chapters, with some architectural differences, one can eliminate multiple reference voltages and the dependence on the absolute capacitor matching.

Appendix B

MOS Sampling Circuits

B.1 Introduction

For any A/D converters, the first thing that the converters need to do is to sample the time varying input signal. In CMOS technology, sampling is generally done with a MOS switch and a sampling capacitor. This circuit function, like every other circuit blocks on the chip, is not ideal. Various sources of errors are associated with it. In this section, a brief discussion of three major sources of nonidealities is presented with reference for a full discussion to several Ph.D. theses in the research group. [12][14]

B.2 Finite Bandwidth

Figure 1 shows a simplest sample-and-hold circuit implemented with a MOS switch and a sampling capacitor. When the MOS switch is on, an on-resistance is associated with the switch depending on the switch size and gate drive. The on-resistance and the sampling capacitor form a RC time constant which defines the bandwidth. The -3dB frequency is given by

$$f_{-3dB} = \frac{1}{2\pi}\frac{1}{R_{sw}C_s} = \frac{1}{2\pi} \times \frac{\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_t)}{C_s} \text{ where}$$

$R_{sw} = \mu_n C_{ox}\frac{W}{L}(V_{gs} - V_t)$ and V_{ds} is small.

For a given switch size and fixed supply voltage, the -3dB frequency increases as the technology improves (increased C_{ox}). With scaled technology (reduced L), the -3dB frequency also increases. However, the -3dB frequency is also directly proportional the supply voltage. Therefore, reducing the supply voltage to be compatible with digital circuits and lower the power also degrades the input bandwidth of SC circuits.

In summary, to achieve high input bandwidth for a fixed sampling capacitor, the on-resistance needs to be small by increasing C_{ox} and reducing L. Although increasing W can also decrease the on-resistance of the switch, the added parasitic capacitance will cancel the effect. With the ongoing trend of low voltage, low power can only be achieved at the expense of input bandwidth.

B.3 Charge Injection

Figure 2 shows a MOS switch and a sampling capacitor. When the switch is on, the voltage across the sampling capacitor tracks the time-varying input signal within the bandwidth. Some charges are present in the MOS channel, this is a result of forming a conducting channel under the MOS gate. The charge in the channel is on the order of $C_{ox}(V_{gs}-V_t)$. When the switch is turned off, charges either flow to the input source or to the sampling capacitor and create a small $\Delta V = \frac{\Delta Q}{C_s}$. ΔQ is a function of several parameters which include input impedance, soure impedance, clock falling edge, etc. To the first order, 50% distribution between the input source and C_s can be assumed.

Charge injection is also a function of input voltage ($C_{ox}(V_g - V_{in} - V_t)$) and needs to be treated carefully to avoid signal dependent distortion. It has been shown that adding a dummy switch at half the size of the sampling switch can cancel the charge injection error to the first order. The dummy swtich is driven by the inverse clock which will absorbs the charge injected from the sam-

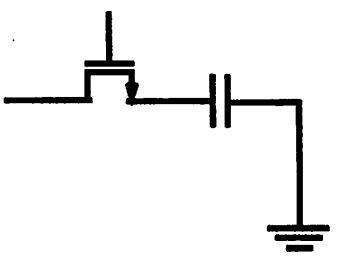


Figure B.1 A Simple Sample-and-Hold Circuit

pling switch instead of being added onto the sampling capacitor. This technique works the best when the clock edge is sharp which means a rough 50% distribution between the input source and sampling capacitor can be assumed. However, an absolute matching between transistors is required for this technique and impedance on both sides need to be roughly equal. For a low impedance input source, this is generally not possible.

Figure 2 shows a technique generally known as bottom plate sampling. This technique requires an additional switch, M2, which defines the sampling instance by turning off before M1. Since the switch M2 is always connected to the input common mode (AC ground), the charge injection is a constant. Therefore, we have eliminated the signal dependence in M2 charge injection. However, charge injection still occurs when M1 goes off. Since the samlping capacitor is floating at this point, the extra charge added onto the capacitor will be shorted to ground when M3 is on during the charge transfer phase in SC circuit.

Charge injection on a sample-and-hold circuit is a signal dependent error, which is really difficult to deal with. Special technique by adding an extra dummy switch can cancel the error to the first order. In differential circuit, the use of bottom plate sampling which results a common mode charge injection can be used.

B.4 Clock Feedthrough

Ideally, when the clock edges are switching, this will not affect the operation of SC circuit. However, due to some parasitic capacitance associated with the MOS switches, the voltage difference in clock switching may be coupled into the sampled input and create an error.

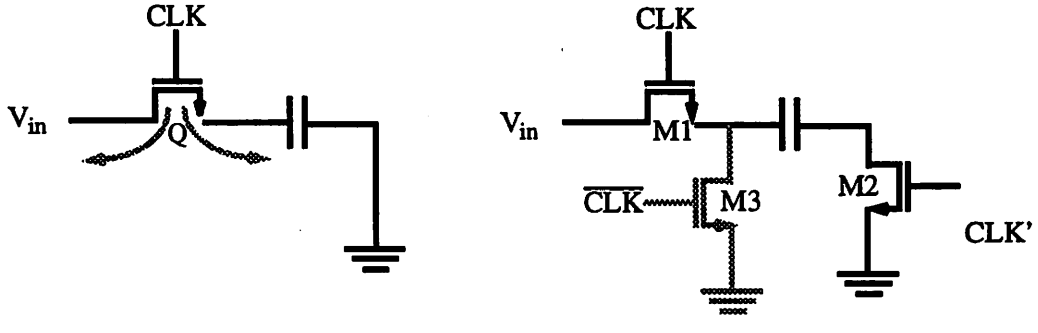


Figure B.2 Sample-and-Hold with Bottom Plate Sampling

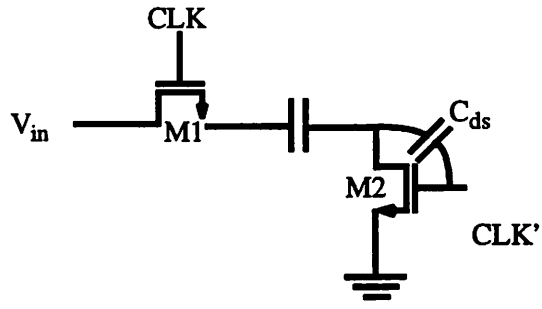


Figure B.3 Illustration for Clock Feedthrough

Figure 3 shows a typical sample-and-hold circuit employing the bottom plate sampling described in the previous section. C_{ds} is the overlapping capacitance between the gate and drain of the MOS switch. When the clock voltage on the gate switches between high and low, this voltage drop is coupled into the signal via the capacitor divider.

The clock feedthrough can be corrected to the first order by using a differential signal path. As long as the error is present on both signal inputs and the same magnitude, it can be cancelled by taking the input differentially. However, this technique, once again, depends on the absolute matching of transistors.

It will be shown later that these errors are carefully examined for the prototype and techniques mentioned above are used to correct these errors.

Appendix C

Nonidealities in SC Circuit

C.1 Introduction

In classical circuit analysis, ideal OpAmp's generally have infinite open loop gain. However, in real life, OpAmp's open loop gain is finite and it introduces error in feedback systems, such as SC circuits. After a brief discussion on OpAmp finite open loop gain, two major sources of non-idealities will be discussed. The thermal noise coming from sampling action and the inherent OpAmp noise will be analyzed and referred to input to be used as a measure of the SC circuit performance.

C.2 Finite Open Loop Gain

Figure 1 shows an SC circuit with finite OpAmp gain in two phases of SC actions. During phase 1, the input signal is sampled onto both C_S and C_F; in phase 2, C_F is folded back to the output and the input is grounded. All the charge on C_S is transfered to C_F to form a 2x gain ($C_F = C_S$) for the SC circuit. However, if the OpAmp gain, A, is finite, the resulting gain will be

$$\frac{V_{out}}{V_{in}} = \frac{C_1 + C_2}{\left(1 - \frac{1}{A}\right)C_2}$$

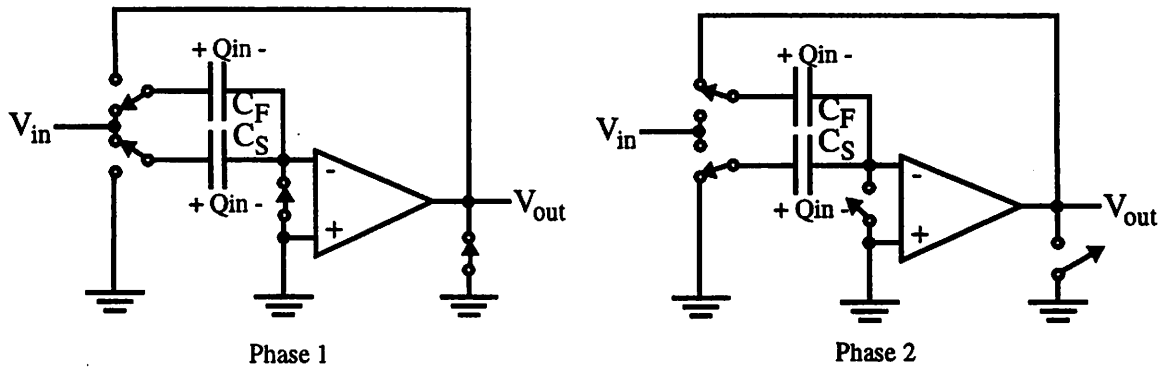


Figure C.1 Two Phases in SC Circuit Action

The non-ideal gain will affect the overall resolution of the A/D converter. The gain error needs to be less than $\frac{1}{2^N}$ which means the requirement of $A \approx 2^N$. In general, a safe margin of 2x factor is taken into consideration; therefore, A is usually required to be at least 2^{N+1}.

Therefore, the A/D resolution determines the minimum DC gain for the OpAmp in the SC circuit, other parameters in the OpAmp for an optimal design will be briefly discussed in the following two sections.

C.3 Noise Contributors in SC Circuit

When the time varying input signal is sampled onto the sampling capacitor by the SC circuit, $\frac{kT}{C}$ noise is sampled to the capacitor connected to the input of the OpAmp. (due to bottom plate sampling.) Its magnitude is

$$\overline{V^2} = \frac{kT}{C_S + C_F + C_{opamp}}$$

where C_{opamp} is the input capacitance of the OpAmp. When the feedback is closed around the OpAmp, the sampled input and noise charges are transfered to C_F and create a V_{out}. Assuming $V_{in} = 0$, the total noise charge sampled is

$$\overline{Q_n^2} = (C \bullet V)^2 = kT(C_S + C_F + C_{opamp})$$

and the output voltage is

$$\overline{V_{out}^2} = \frac{\overline{Q_n^2}}{C_F^2} = kT \bullet \frac{(C_F + C_S + C_{opamp})}{C_F^2} = \frac{kT}{C_F} \bullet \frac{1}{f}$$

where f is the feedback factor which equals to

$$f = \frac{C_F}{C_S + C_F + C_{opamp}}$$

Therefore, the input referred noise can be calculated by dividing the output noise by the gain square and is given by

$$\overline{V_{in}^2} = \frac{\overline{V_{out}^2}}{G^2} = \frac{kT}{C_F} \bullet \frac{1}{f} \bullet \left(\frac{C_F}{C_S + C_F}\right)^2 = kT \bullet \frac{(C_S + C_F + C_{opamp})}{(C_S + C_F)^2}$$

In addition to $\frac{kT}{C}$ noise in the SC circuit, the inherent OpAmp noise also contributes to the non-idealities. It's been shown in [3][12] that the input referred OpAmp noise variance is

$$\sigma^2 = \frac{2}{3} \cdot kT \cdot \frac{1}{f} \cdot \frac{1}{C_{LT}} \cdot \left(\frac{C_F}{C_S + C_F}\right)^2$$

where $C_{LT} = C_L + f \cdot (C_S + C_{opamp})$.

C.4 Total Input-Referred Noise

Combing the two input-referred noise contributors from above, the total input-referred noise for SC circuit is given by

$$\sigma_{Total}^2 = kT \bullet \frac{(C_S + C_F + C_{opamp})}{(C_S + C_F)^2} + \frac{2}{3} \cdot kT \cdot \frac{1}{f} \cdot \frac{1}{C_{LT}} \cdot \left(\frac{C_F}{C_S + C_F}\right)^2$$

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