A COMPARISON OF CONTINUOUS-TIME AND DISCRETE-TIME SIGMA-DELTA MODULATORS

by

Naiyavudhi Wongkomet

Memorandum No. UCB/ERL M96/41

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Abstract

The goal of this research is to investigate the issues involved in the design and implementation of continuous-time $\Sigma\Delta$ modulators and to compare continuous-time to discrete-time $\Sigma\Delta$ implementations.

The conditions necessary for single-loop and double-loop second-order continuous-time modulators to have the same noise shaping function as second-order discrete-time modulators are discussed. The noise shaping function and the dynamic range of generalized Lth-order continuous-time modulators are derived. The dynamic range of continuous-time modulators is shown to be the same as that of discrete-time modulators.

Nonidealities associated with the implementations of continuous-time modulators are investigated. Nonlinearity, leakage, gain error, and non-dominant poles of the integrators, the comparator delay time, and clock jitter are studied.

Compared to second-order discrete-time modulators, single-loop and double-loop second-order continuous-time modulators can achieve higher sampling frequency by approximately a factor of three and four, respectively. Continuous-time modulators, however, have to be carefully designed because of the low clock jitter requirement and the nonlinearity associated with continuous-time integrators.

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A Comparison of Continuous-Time and Discrete-Time Sigma-Delta Modulators

CHAPTER 1

Introduction

1.1 Goal and motivation

By exchanging sampling speed with resolution in amplitude, oversampled or ΣΔ analog-to-digital (A/D) converters can achieve high resolution compared to most Nyquist rate A/D converters. Because of the oversampling, oversampled A/D converters, however, are limited only to low- to medium-speed conversion rate. This is evidenced in Fig. 1.1, where the conversion rate and the dynamic range of oversampled and Nyquist rate A/D converters published during recent years are shown.

From Fig 1.1, a few observations are made as follows:

- Most Nyquist rate converters have a dynamic range limited to below 70dB due to component matching accuracy.
- Oversampled A/D converters are typically used for applications requiring more than 70dB dynamic range. Since these converters exchange resolution in time for that in amplitude, the conversion rate of these converters is lower than that of Nyquist rate converters.

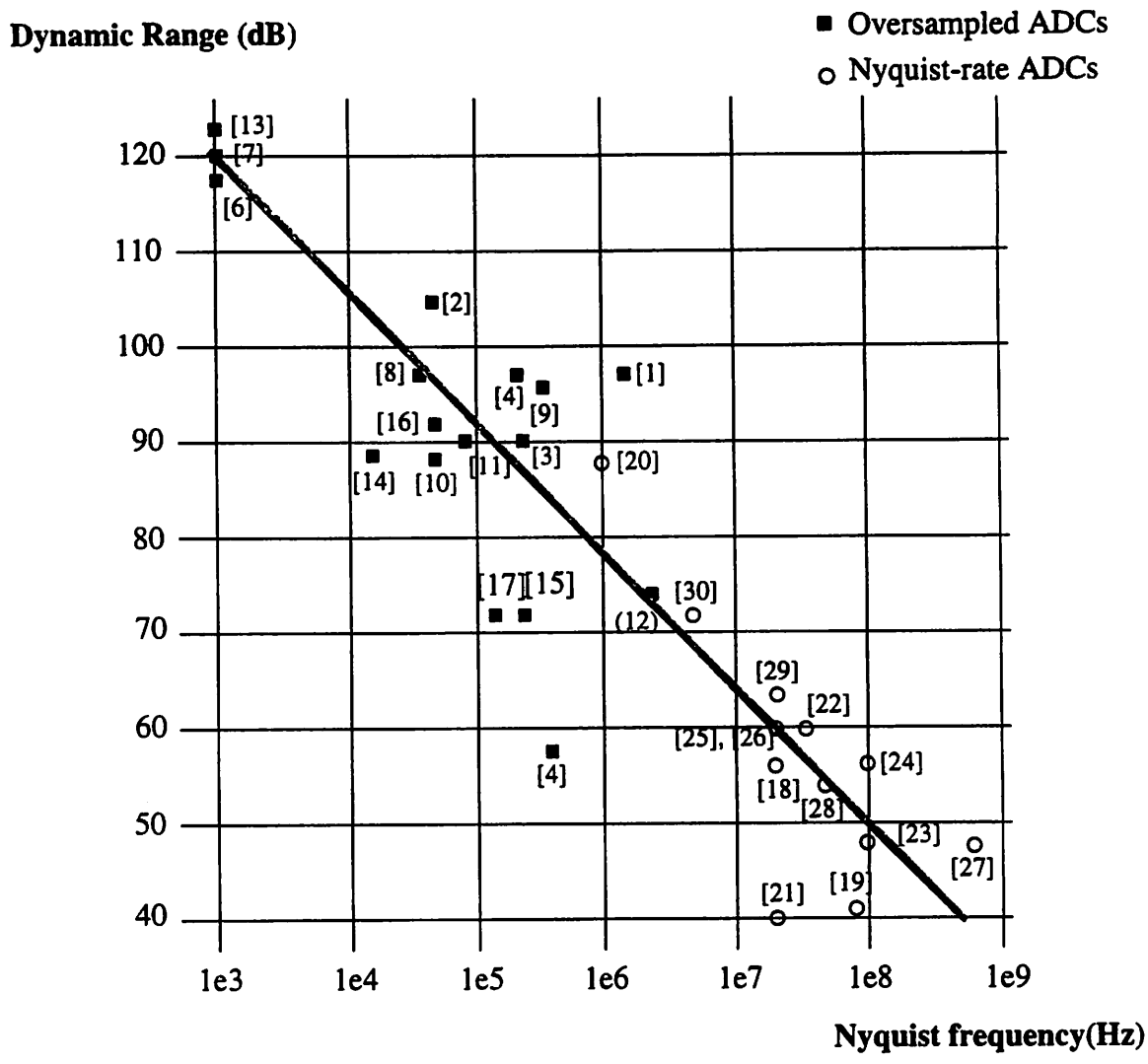


Figure 1.1 Conversion rate and dynamic range of oversampled and Nyquist-rate ADC

- In general, the tradeoff between the conversion rate and the dynamic range is approximately 14dB reduction of dynamic range for a decade increase of conversion rate, regardless of the architecture of the converter.
- Some of the converters in the lower left region do not reflect mediocre designs, but are optimized for low-power applications.

With increasing applications of converters for communications, consumer electronics, instrumentations, and medical imaging, the demand for high-speed high-accuracy A/D converters will

escalate. An approach to satisfy this demand is to implement oversampled or ΣΔ A/D converters at higher speed. The speed of discrete-time ΣΔ A/D converters is limited by the settling process of switched-capacitor integrators. A potential solution to alleviate this speed limitation is the continuous-time ΣΔ A/D converters. The objective of this research is to investigate the design and implementation of continuous-time ΣΔ A/D converters and to compare continuous-time to discrete-time converters.

1.2 Thesis organization

This thesis is organized into five chapters. In Chapter 2, the conditions which allow a double-loop second-order continuous-time modulator to have the same noise shaping function as single-loop continuous-time and discrete-time modulators are derived. The noise shaping function and the dynamic range of generalized Lth-order continuous-time modulators are derived. Chapter 3 describes how nonidealities in circuit implementations affect continuous-time modulators. The clock jitter requirement and other design criteria associated with integrators and comparators are discussed. In Chapter 4, continuous-time modulators are compared to discrete-time modulators. Advantages, disadvantages, and critical design issues are pointed out. The last chapter, Chapter 5, recapitulates the results of this study and draws conclusions.

CHAPTER 2

Architectures and Systems

2.1 Overview

$\Sigma\Delta$ modulators have been widely implemented in the discrete-time domain using switched-capacitor integrators. Continuous-time $\Sigma\Delta$ modulators, on the other hand, have not received the same attention despite their potential of achieving higher sampling frequency in a given technology [17].

In this chapter, the conditions necessary for double-loop second-order continuous-time $\Sigma\Delta$ modulators to have the same noise shaping function as single-loop second-order continuous-time $\Sigma\Delta$ modulators will be derived. The integrator time constant and loop stabilization of single-loop and double-loop continuous-time modulators will be discussed. The noise shaping function and the dynamic range of generalized Lth-order continuous-time $\Sigma\Delta$ modulators will be derived and shown that it is the same as discrete-time modulators.

2.2 Continuous-time $\Sigma\Delta$ Modulators

2.2.1 Topology

In [31], Candy proposes the single-loop second-order continuous-time modulator shown in Fig. 2.2 and shows that it has the same noise shaping function as a second-order discrete-time

modulator shown in Fig. 2.1. In this section, the derivation in [31] will be extended for a double-loop second-order continuous-time modulator.

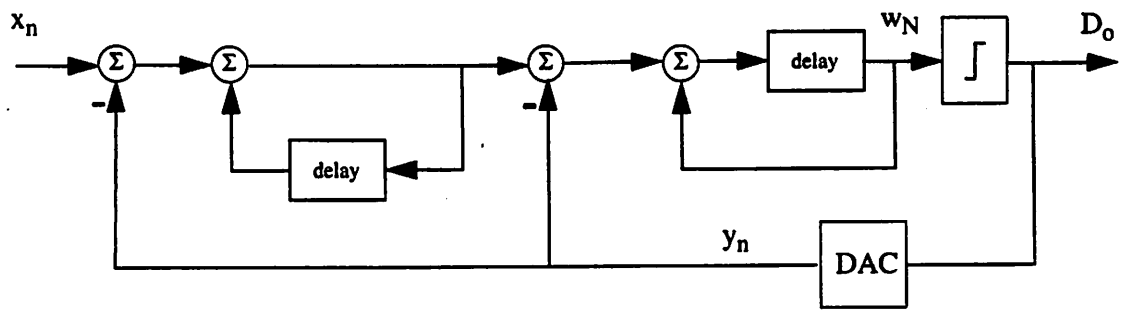


Figure 2.1 A double-loop second-order discrete-time ΣΔ modulator

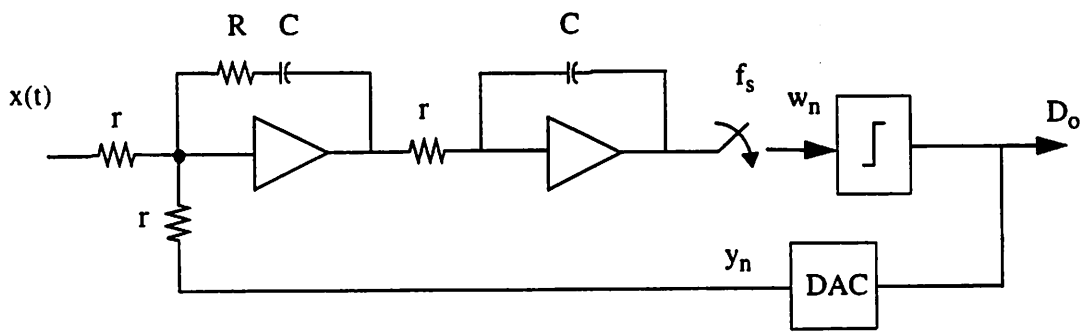


Figure 2.2 A single-loop continuous-time second-order modulator

The signal applied to the quantizer of the second-order discrete-time modulator shown in Fig. 2.1 is given in [31] as

$$w_N = \sum_{n=0}^{N-1} (N-n)x_n - \sum_{n=0}^{N-1} (N-n+1)y_n \tag{2.1}$$

provided all the signals are initially zero.

For the single-loop continuous-time modulator shown in Fig. 2.2, w_N is given as

$$w_N = \frac{(rC)^2}{T}\left(\sum_{n=0}^{N-1} (N-n)\left(x_{nT} + \left(\frac{RC}{T} - \frac{1}{2}\right)\left(x_{nT} - x_{(n-1)T}\right)\right) - \sum_{n=0}^{N-1} \left(N-n+\left(RC-\frac{1}{2}\right)\right)y_n\right) \tag{2.2}$$

where $T = \frac{1}{f_s}$ and

$$x_{nT} = \frac{1}{T} \int_{nT}^{(n+1)T} x(t)\,dt \tag{2.3}$$

The coefficients of y_n, or the noise shaping functions, in Eq. 2.1 and Eq. 2.2 are identical when

$$\frac{1}{rC} = f_s \tag{2.4}$$

$$\frac{1}{RC} = \frac{2}{3T} = \frac{2}{3}f_s \tag{2.5}$$

and the feedback signal is held constant throughout each sample interval. In this case, x_{nT} terms in Eq. 2.2 can be written as

$$x'_n = (x_{nT} + (\frac{RC}{T} - \frac{1}{2})(x_{nT} - x_{(n-1)T})) = 2x_{nT} - x_{(n-1)T} \tag{2.6}$$

which has spectral equivalent

$$X'(\omega) = \left(2 - e^{-j2\pi\frac{f}{f_s}}\right) \operatorname{sinc}(\frac{f}{f_s}) X(\omega) \tag{2.7}$$

Since the sampling frequency is much higher than the frequency of the input signal, the spectra of x_n and x'_n are approximately identical, i.e.

$$X'(\omega) \approx X(\omega) \qquad ; \text{for } f \ll f_s \tag{2.8}$$

The forward path transfer function of this modulator has two poles at the origin, and a finite zero at $(\frac{2}{3}f_s)$ rad/s that is needed to stabilize the feedback loop.

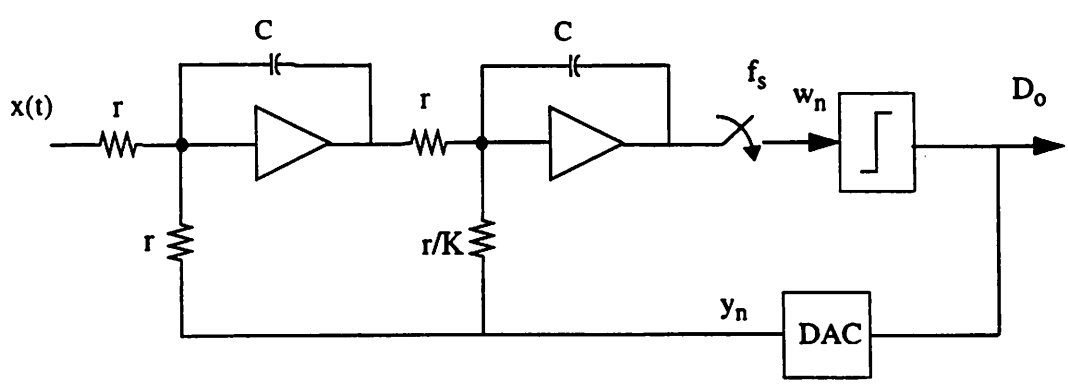


Figure 2.3 A double-loop continuous-time second-order modulator

The double-loop second-order continuous-time modulator in Fig. 2.3 uses the inner-feedback loop to implement the finite zero instead of using the resistor R as in the single-loop continuous-time modulator in Fig. 2.2. The input to the quantizer of this modulator can be written as

$$w_N = \frac{(rC)^2}{T}\left(\sum_{n=0}^{N-1}(N-n)\left(x_{nT}-\frac{1}{2}(x_{nT}-x_{(n-1)T})\right)-\sum_{n=0}^{N-1}(N-n+(K-\frac{1}{2}))y_n\right) \tag{2.9}$$

The double-loop modulator has the same noise shaping function as the single-loop modulator in Fig. 2.2 and the discrete-time modulator in Fig. 2.1 when

$$\frac{1}{rC} = f_s \tag{2.10}$$

$$K = 1.5 \tag{2.11}$$

and the feedback signal is held constant throughout each sample interval.

The inner-feedback loop with the gain $\frac{1}{K} = \frac{2}{3}$ results in a zero at $(\frac{2}{3}f_s)$ rad/s as in the single-loop modulator. Furthermore,

$$x'_n = 0.5\,(x_{nT}+x_{(n-1)T}) \tag{2.12}$$

which has spectral equivalent

$$X'(\omega) = 0.5\left(1+e^{-j2\pi\frac{f}{f_s}}\right)X(\omega) \tag{2.13}$$

For $f \ll f_s$,

$$X'(\omega) \approx X(\omega) \tag{2.14}$$

In Eq. 2.4 and Eq. 2.10, the conditions require the integrators in both single-loop and double-loop modulators to have the transfer function

$$H(s) = \frac{1}{srC} = \frac{1}{(\frac{s}{f_s})} \tag{2.15}$$

The time constant of this integrator is equal to $\frac{1}{f_s}$ and the unity-gain frequency is at $f_u = \frac{f_s}{2\pi}$.

Single-loop and double-loop modulators have different advantages when nonidealities are taken into account. This will become obvious after the discussion of different types of nonidealities in Chapter 3.

2.2.2 Performance Analysis

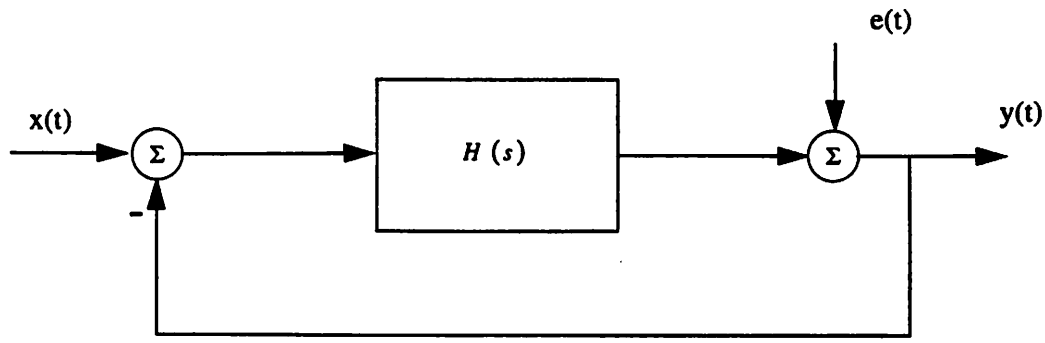


Figure 2.4 A linearized model of an Lth-order continuous-time modulator

To predict the dynamic range of ΣΔ modulators, it is necessary to know the noise shaping function of the modulators. The noise shaping function also gives us some insights into how the modulators perform in the presence of circuit nonidealities. In this section, the noise shaping function and the dynamic range of generalized Lth-order continuous-time modulators will be derived.

The analysis presented below is based on the assumption that the quantization error in the feedback loop of the modulator is uncorrelated. Thus, the quantizer error can be modeled as an additive white-noise source. The sampling switch at the input of the quantizer can be neglected because the bandwidth of interest is much lower than the sampling frequency. The issue of stability for modulators with order of two or higher is neglected. The linearized model of an Lth-order continuous-time modulator is represented in Figure 2.4, where

$$H(s) = \frac{1}{(srC)^L} = \frac{1}{(\frac{s}{f_s})^L} \tag{2.16}$$

The time constants of the integrators are the same as in Eq. 2.15.

The expression for the dynamic range of continuous-time modulators can be obtained using the same approach as for the discrete-time modulators in [14]. The noise shaping function of Lth-order continuous-time modulators can be written as

$$H_E(s) = \frac{Y(s)}{E(s)} = \frac{1}{1+H(s)} \approx \frac{1}{H(s)} = \left(\frac{s}{f_s}\right)^L \quad ; \text{for } |s| \ll f_s \tag{2.17}$$

The approximation can be made because the large magnitude response of the integrators in the baseband. By substituting $s = j\omega$ into Eq. 2.17,

$$H_E(\omega) = \left(\frac{j\omega}{f_s}\right)^L \tag{2.18}$$

The spectral distribution of the quantization noise is the product of the shaping function and the spectral density of the quantization error

$$S_{ee}(f) = |H_E(f)|^2 \cdot \frac{S_Q}{f_s} \tag{2.19}$$

Substituting Eq. 2.18 into Eq. 2.19 yields

$$S_{ee}(f) = \left(\frac{2\pi f}{f_s}\right)^{2L} \cdot \frac{S_Q}{f_s} \tag{2.20}$$

Integration over the baseband gives the total power of the inband quantization noise

$$S_B = \int_{-\frac{f_N}{2}}^{\frac{f_N}{2}} S_{ee}(f)\,df = \frac{\pi^{2L}}{(2L+1)M^{2L+1}} \cdot S_Q \tag{2.21}$$

where the oversampling ratio, M, is defined as the ratio of the sampling frequency to the Nyquist rate,

$$M = \frac{f_s}{f_N} \tag{2.22}$$

The quantization error power is given in [32] as

$$S_Q = \frac{\Delta^2}{12} \tag{2.23}$$

The forward path transfer function can be written as

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1+H(s)} \approx 1 \quad ; \text{for } |s| \ll f_s \tag{2.24}$$

and because the full scale input to the modulator is $\pm\frac{\Delta}{2}$, the maximum signal power at the output is

$$S_{sig} = \frac{\left(\frac{\Delta}{2}\right)^2}{2} = \frac{\Delta^2}{8} \tag{2.25}$$

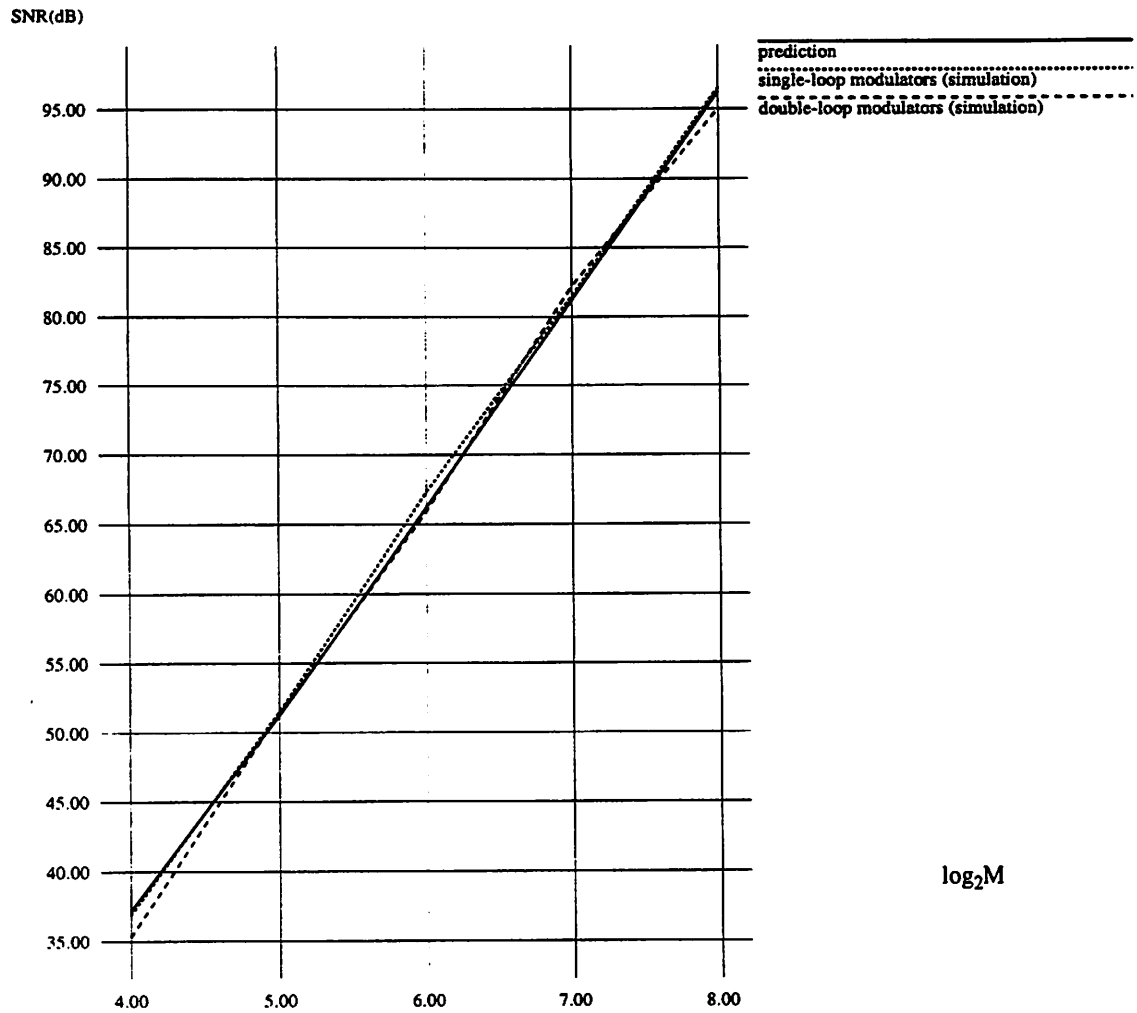


Figure 2.5 Dynamic range of second-order continuous-time $\Sigma\Delta$ modulators at different oversampling ratio with input 6dB below full-scale

The dynamic range can be obtained from Eq. 2.21, Eq. 2.23, and Eq. 2.25 as

$$DR = \frac{S_{sig}}{S_B} = \frac{3}{2}\frac{2L+1}{\pi^{2L}}M^{2L+1} \tag{2.26}$$

which is identical to the expression for discrete-time modulators as shown in [14].

Fig. 2.5 compares the dynamic range of second-order continuous-time modulators obtained from Eq. 2.26 to the simulation results of both single-loop and double-loop second-order continu-

ous-time modulators at different oversampling ratio. Fig. 2.6 shows the simulated signal-to-noise ratio (SNR) at different input level of both single-loop and double-loop second-order continuous-time modulators. The simulation results in Fig. 2.5 and Fig. 2.6 are in good agreements with the prediction based on Eq. 2.26.

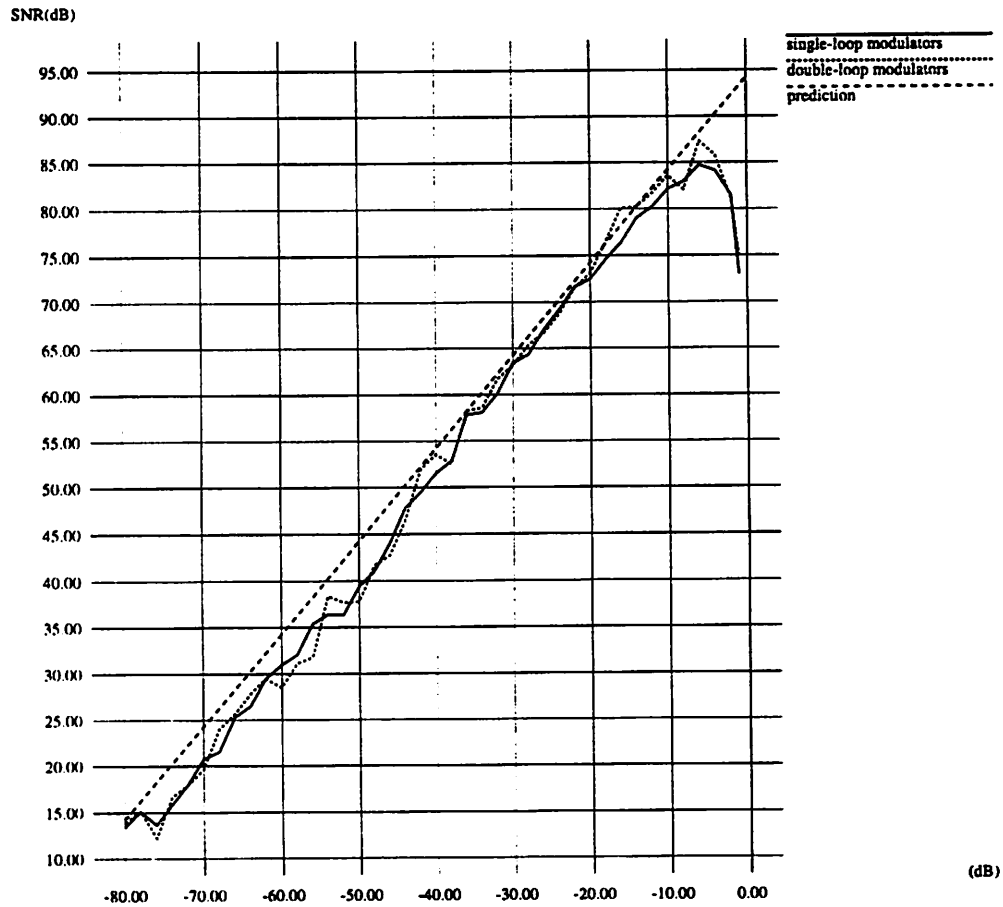


Figure 2.6 Signal-to-noise ratio of second-order continuous-time modulators as a function of sinusoidal input ($M=128$, $f_{signal}/f_{Nyquist}=10.771$)

2.3 Summary

Single-loop and double-loop second-order continuous-time $\Sigma\Delta$ modulators were discussed in this chapter. The conditions necessary for double-loop continuous-time modulator to have the same noise shaping function as single-loop continuous-time and discrete-time modulators were derived. The integrator time constants of single-loop and the double-loop continuous-time modulators are equal. A finite zero, which is needed to stabilize the loop, is implemented in the forward path in the single-loop modulator. In the double-loop modulator, the zero is implemented by the inner-feedback loop. The noise shaping function and the dynamic range of generalized Lth-order continuous-time modulators were derived. The dynamic range of continuous-time modulators is the same as that of discrete-time modulators.

CHAPTER 3

System Requirements

3.1 Overview

Circuit implementations of ΣΔ modulators do not achieve the performance of ideal modulators because of nonidealities present in analog circuit realizations. In this chapter, the design criteria for implementing continuous-time ΣΔ modulators will be discussed and compared to those of discrete-time modulators, when applicable. Critical design criteria will be pointed out and possible solutions will be suggested in Chapter 4.

The discussion will start from the clock jitter, a system design issue. This will be followed by nonidealities associated with specific building blocks. The discussion of integrator nonidealities will include nonlinearity, leakage, gain error, and non-dominant poles. Delay time of comparators will be examined. Lastly, the settling time of switched-capacitor integrators will be discussed because it will be referred to in the continuous-time and discrete-time modulator speed comparison in Section 4.2.

3.2 Clock Jitter

In discrete-time ΣΔ modulators, sampling clock jitter results in nonuniform sampling of input and increases the total error power in the quantizer output. This requirement, however, is relaxed

compared to Nyquist rate converters because of the oversampling. The worst case for jitter occurs when the input signal has the maximum rate of change. The inband jitter error power, assuming the jitter is an uncorrelated Gaussian random process, is given in [14] as

$$S_{\Delta t} < \frac{\left(\pi\Delta\frac{\sigma_t}{T_s}\right)^2}{8M^3} = \frac{(2\pi\Delta B\sigma_t)^2}{8M} \tag{3.1}$$

where B is the bandwidth of the input signal, $\frac{\Delta}{2}$ is the maximum input signal amplitude, and σ_t^2 is the jitter variance. This equation shows that for a fixed signal bandwidth and jitter error power, σ_t^2 increases with the oversampling ratio.

In continuous-time ΣΔ modulators, the major source of jitter error is the feedback current source. The duration of this current source is controlled by the clock as shown in the conceptual diagram in Fig. 3.1. Therefore, the error in the duration is due to the jitter in the rise and fall edges of the clock. Since the feedback current is subtracted from the input signal, the jitter error power adds directly to the input signal.

Assuming the jitter is an uncorrelated Gaussian random process, the variance of charge due to the clock jitter in the feedback current source can be written as

$$\sigma_Q^2 = I_{fb}^2(2\sigma_t^2) \tag{2.2}$$

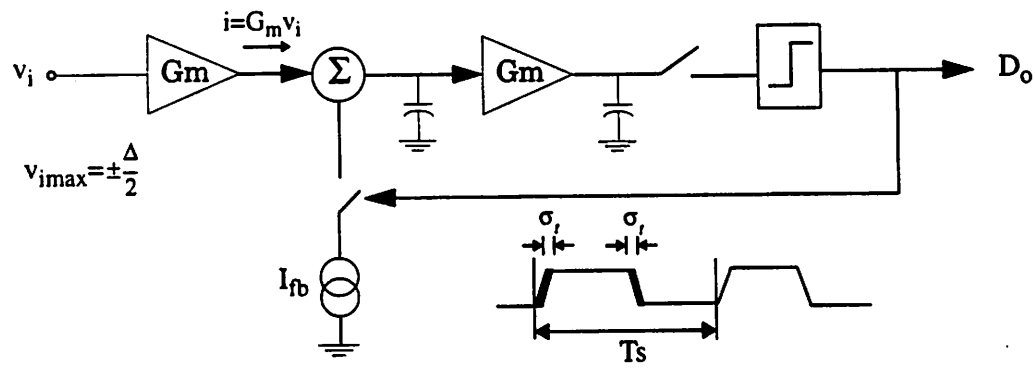


Figure 3.1 Typical circuit block diagram of continuous-time ΣΔ modulators

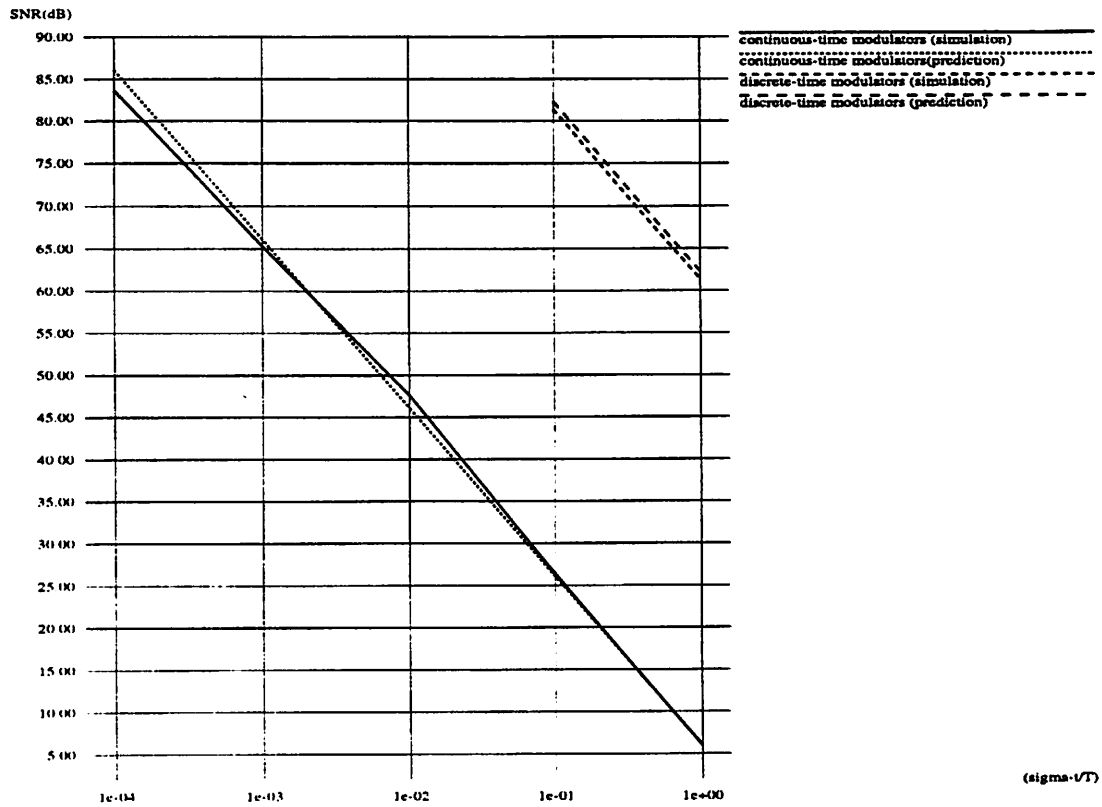


Figure 3.2 Predicted and simulation results show the effect of jitter on second-order $\Sigma\Delta$ modulators (M=128, A=-6dB)

The input-referred error voltage is

$$v_{error}^2 = 2\Delta^2\left(\frac{\sigma_t}{T_s}\right)^2 \tag{3.3}$$

where the duty cycle of the feedback current source is assumed to be 50%.

Since the spectrum of uncorrelated jitter is white, the inband error power can be written as

$$S_{\Delta t} = \frac{v_{error}^2}{M} = \frac{2}{M}\Delta^2\left(\frac{\sigma_t}{T_s}\right)^2 = 8M\,(\Delta B\sigma_t)^2 \tag{3.4}$$

The predicted and the simulation results of the effect of jitter for both discrete-time and continuous-time modulators are shown in Fig. 3.2.

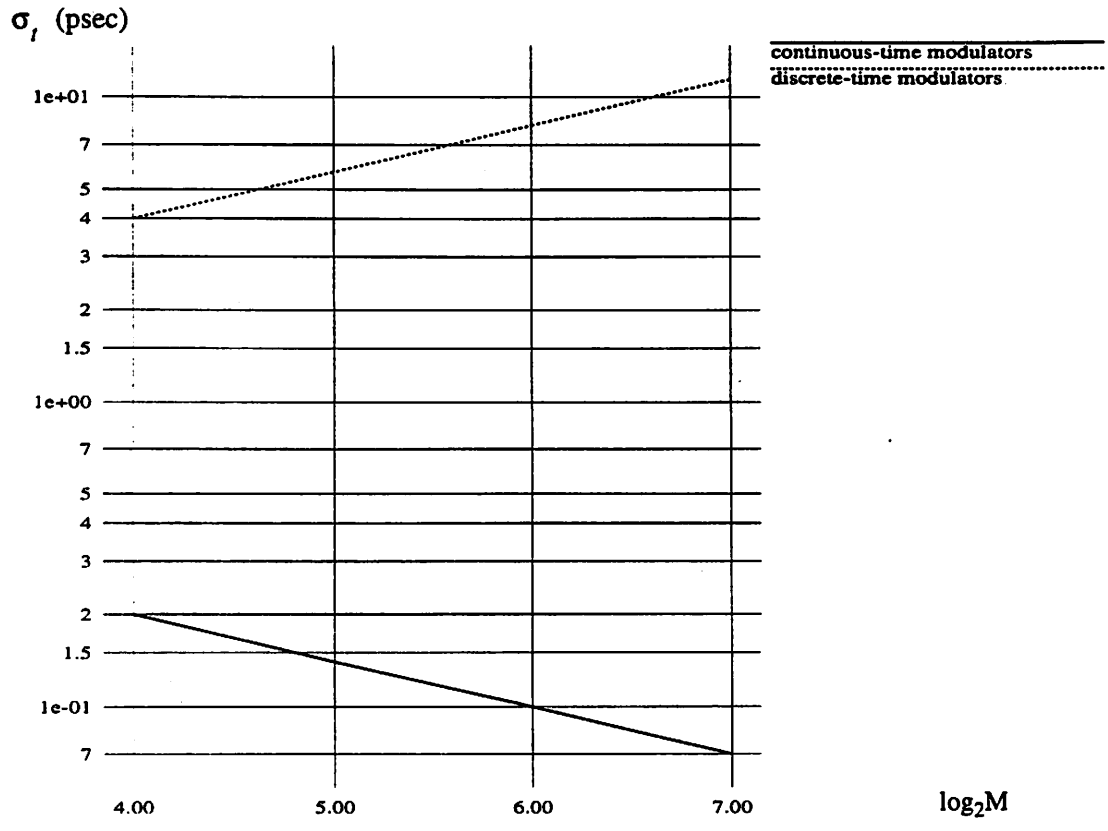


Figure 3.3 Clock jitter requirements of modulators with signal input bandwidth of 2.5MHz and inband jitter error power limited to 96dB below full-scale input signal power

In contrast to discrete-time modulators, the jitter error power of continuous-time modulators is constant regardless of the input frequency and amplitude, and the jitter variance is inversely proportional to the oversampling ratio for a fixed signal bandwidth and jitter error power.

To compare the jitter requirements of discrete-time and continuous-time modulators, Eq. 3.1 and Eq. 3.4 are set to be equal. The result yields

$$\frac{(\sigma_t^2)_{cont}}{(\sigma_t^2)_{disc}} = \left(\frac{\pi}{4M}\right)^2 \tag{3.5}$$

Consequently, for identical performance, the clock jitter in a continuous-time modulator must be approximately M^2 times smaller than in an equivalent discrete-time modulator. For example,

for an oversampling ratio M=100, the jitter power in a continuous-time modulator must be 40dB lower. For high speed or high accuracy converters, this represents a serious challenge. Fig. 3.3 shows the jitter requirement of continuous-time and discrete-time modulators with input bandwidth of 2.5 MHz and inband jitter error power limited to 96dB below the power of full-scale input signal. The continuous-time modulators in this figure require clock jitter in the range of 0.07-0.2 picosecond depending on the oversampling ratio.

3.3 Integrator Nonlinearity

It has been known that nonlinearity in analog circuits can cause harmonic distortion that limits the signal-to-noise ratio (SNR) at large signal levels. From the block diagram in Fig. 3.1, the integrator components which can generate harmonic distortion are the capacitors and the transconductors. Since monolithic capacitors are normally very linear, the concern is mainly on the transconductors.

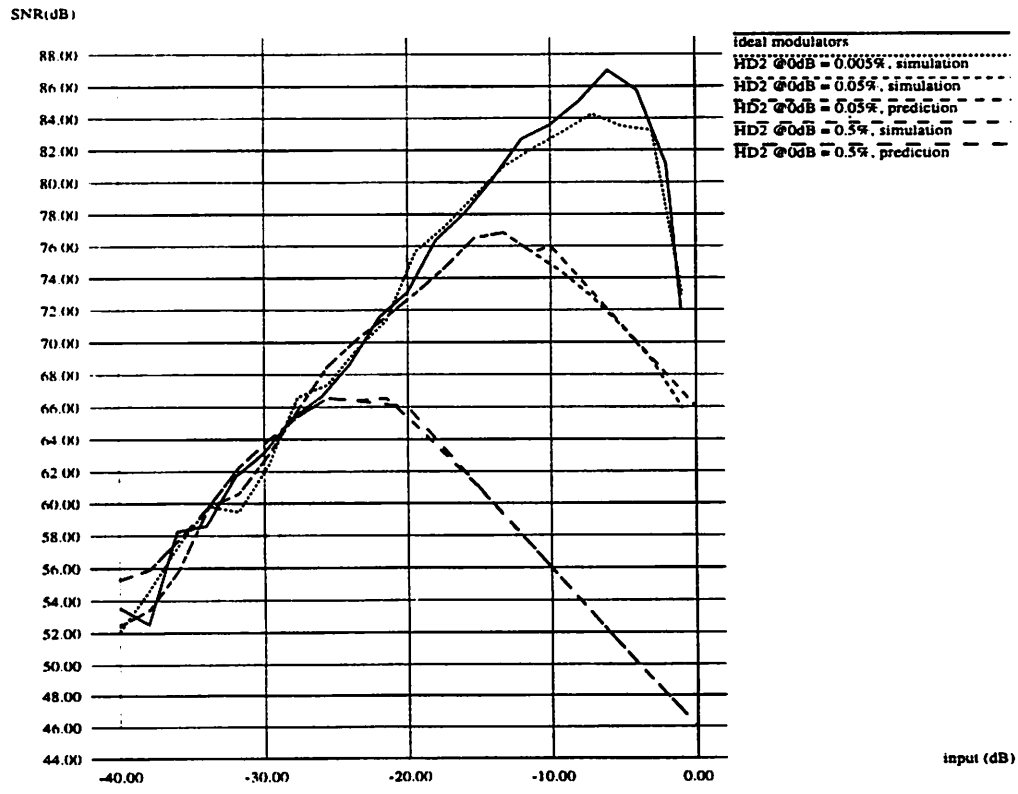


Figure 3.4 Influence of second-harmonic distortion from the first transconductor on second-order continuous-time modulator performance as a function of sinusoidal inputs (M=128)

By representing the transfer function of the transconductor as

$$i_o(t) = \alpha_1 v_i(t) + \alpha_2 v_i^2(t) + \alpha_3 v_i^3(t) + \ldots \tag{3.6}$$

the second and third harmonic distortion factors due to sinusoidal input signals are [35]

$$HD_2 = \frac{1}{2}\frac{\alpha_2}{\alpha_1} V_{iA} \tag{3.7}$$

$$HD_3 = \frac{1}{4}\frac{\alpha_3}{\alpha_1} V_{iA}^2 \tag{3.8}$$

where V_{iA} is the amplitude of the sinusoidal input signal.

The first transconductor is the main source of nonlinearity because its harmonic distortion adds directly to the input signal. This requires the linearity of the first transconductor, at the maximum input level, to be as good as the overall accuracy of the modulator. For example, a modulator with 85dB signal-to-noise ratio requires the first transconductor to have lower than 0.005% total harmonic distortion at maximum input signal level. The simulation and analytical results of the influence of second and third harmonic distortion of the first transconductor on the modulator performance are shown in Fig. 3.4 and Fig. 3.5, respectively.

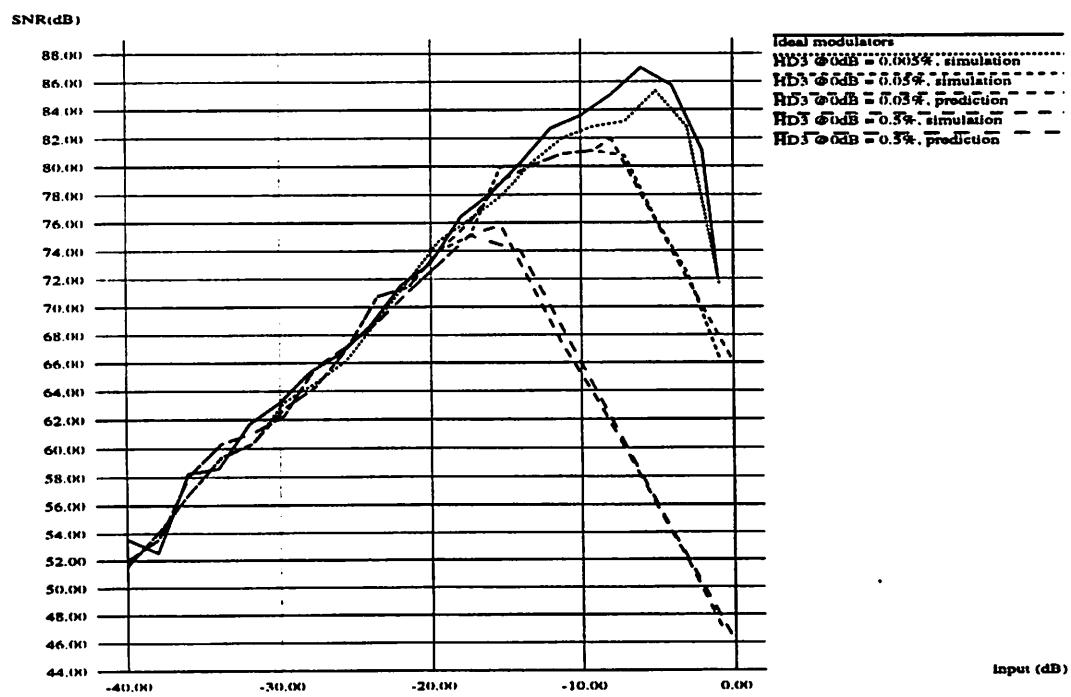


Figure 3.5 Influence of third-harmonic distortion from the first transconductor on second-order continuous-time modulator performance as a function of sinusoidal inputs (M=128)

In comparison to the harmonic distortion of the first transconductor, the harmonic distortion of the second transconductor is attenuated by the gain of the first integrator. Since the gain of integrators is inversely proportional to the frequency and the harmonics above the signal bandwidth are suppressed by the decimation filter (assuming no aliasing), the harmonics of the second transconductor are minimally attenuated at $f = \frac{f_N}{2}$.

From Eq. 2.15, the integrator transfer function is

$$H(s) = \frac{f_s}{s} \tag{3.9}$$

therefore, the integrator gain at $f = \frac{f_N}{2}$ is

$$\left|H(f=\frac{f_N}{2})\right| = \frac{f_s}{2\pi(\frac{f_N}{2})} = \frac{f_s}{2\pi(\frac{f_s}{2M})} = \frac{M}{\pi} \tag{3.10}$$

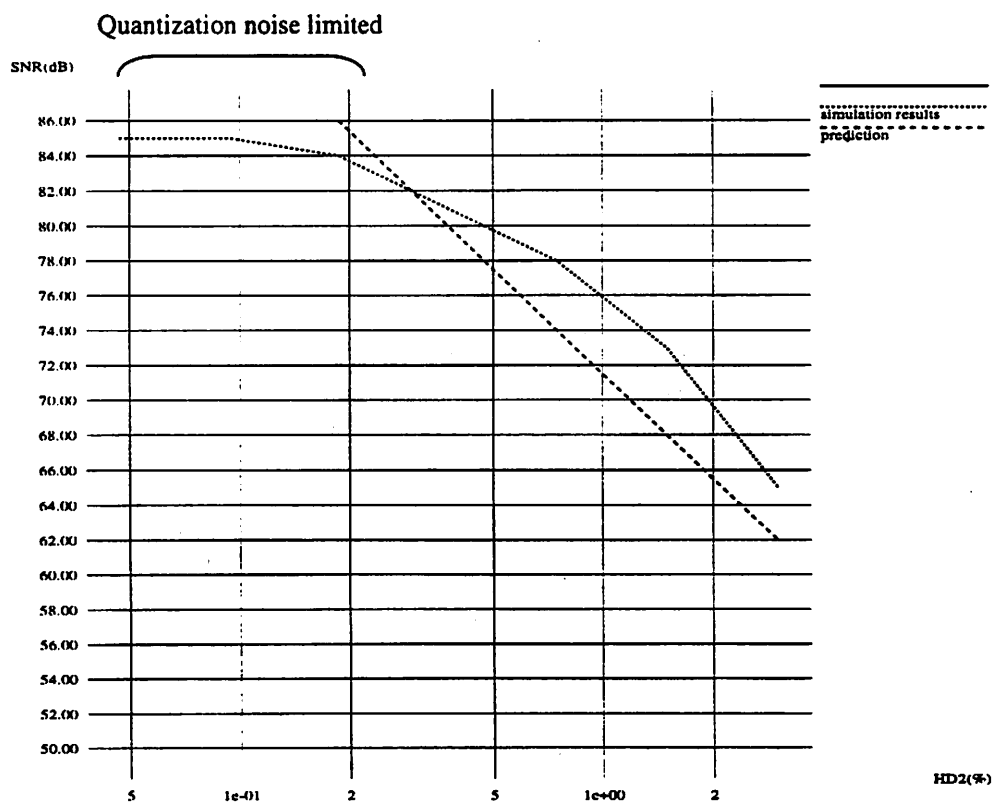


Figure 3.6 Influence of second-harmonic distortion from the second transconductor on the modulator performance. The modulator input level is -6dB below full-scale. (M=128, $f_x = \frac{f_N}{4.277}$)

Consequently, the linearity requirement for the second transconductor can be approximated as

$$-20\log(THD_{2nd\ transconductor}) < SNR_{modulator} - 20\log\left(\frac{M}{\pi}\right) \tag{3.11}$$

This equation shows that the linearity of the second transconductor can be approximately $(6 \cdot log_2 M - 10)$dB lower than the signal-to-noise ratio of the modulator. For example, for oversampling ratio M=128, the linearity of the second transconductor can be 32dB lower than the signal-to-noise ratio of the modulator. The prediction using this equation and the simulation results are shown in Fig. 3.6. The predicted and the simulation results match to within 4dB when the input to the second transconductor, which is not sinusoidal, is assumed to be sinusoidal with approximately the same amplitude as shown in Fig. 3.7. This assumption allows Eq. 3.7 and Eq. 3.8 to be used in calculating the harmonic distortion. The predicted and the simulation results in Fig. 3.6 shows that a modulator with oversampling ratio of 128 can achieve 85dB signal-to-noise ratio when the second transconductor has lower than 0.2% THD. Further discussions of integrator implementations are in Section 4.4.

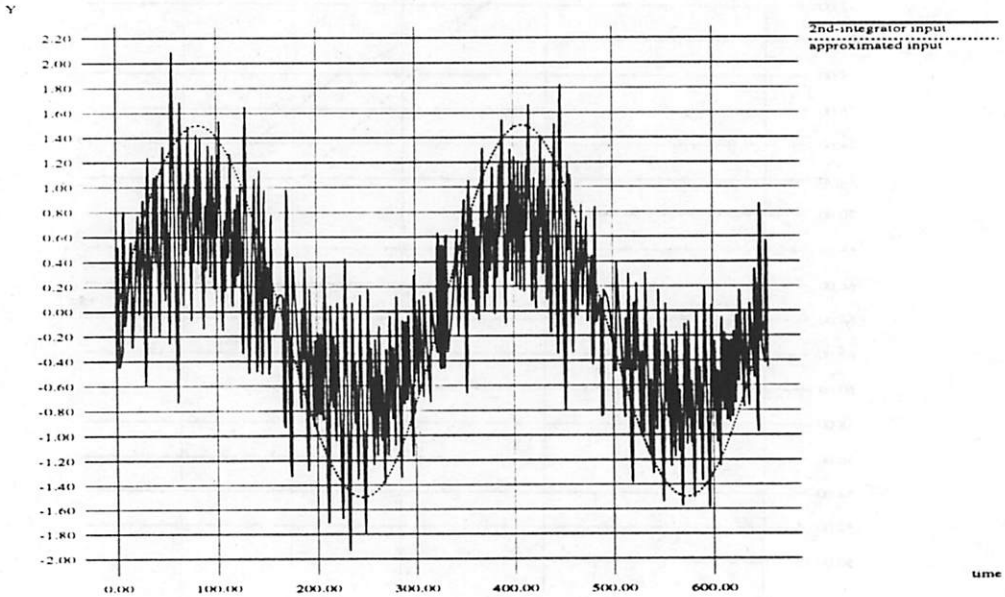


Figure 3.7 The actual input to the second transconductor and the approximated input used for calculation of harmonic distortion of the second transconductor

3.4 Integrator Leakage

The DC-gain of ideal integrators is infinite. In practice, the DC-gain is limited by circuit constraints. The effect of limited gain at low frequency is the reduction in the attenuation of quantization noise in the baseband. In the time-domain, only a fraction of the previous output is added to the new output.

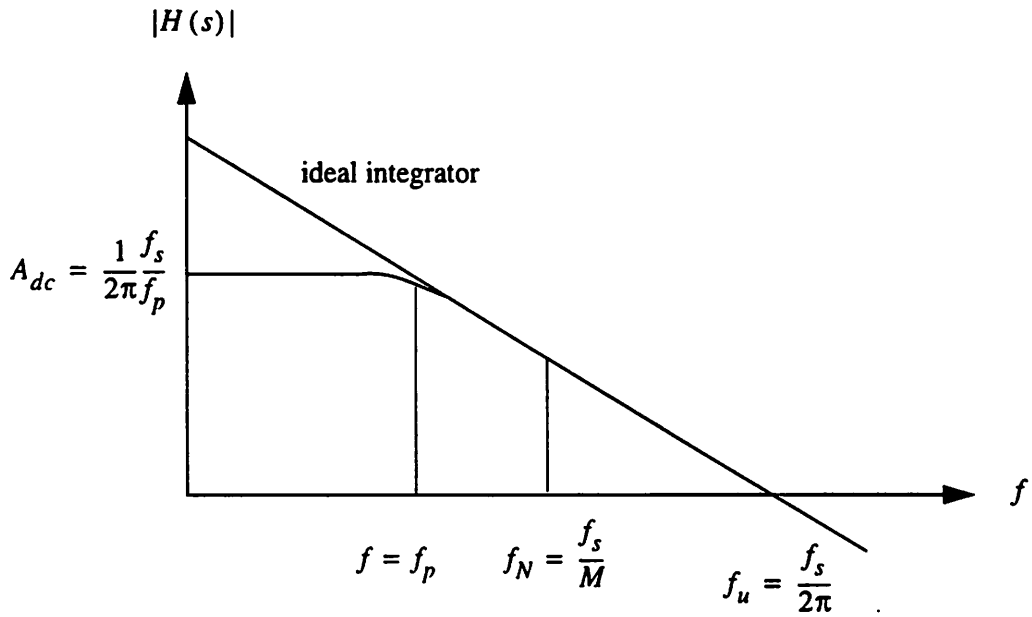


Figure 3.8 Frequency response of ideal and finite-gain integrators

Fig. 3.8 shows the frequency response of an ideal integrator with the transfer function given in Eq. 2.15 and a finite DC-gain integrator. For modulators using finite DC-gain integrators, the noise shaping function in Eq. 2.17 is modified to

$$H_E(s) \approx \frac{1}{H(s)} = \left(\frac{s+\omega_p}{f_s}\right)^L \tag{3.12}$$

where $\omega_P = 2\pi f_p$ and f_s is the sampling frequency in the unit of Hertz. By substituting $s = j\omega$ into Eq. 3.12,

$$H_E(f) = \left(\frac{j\omega+\omega_p}{f_s}\right)^L \tag{3.13}$$

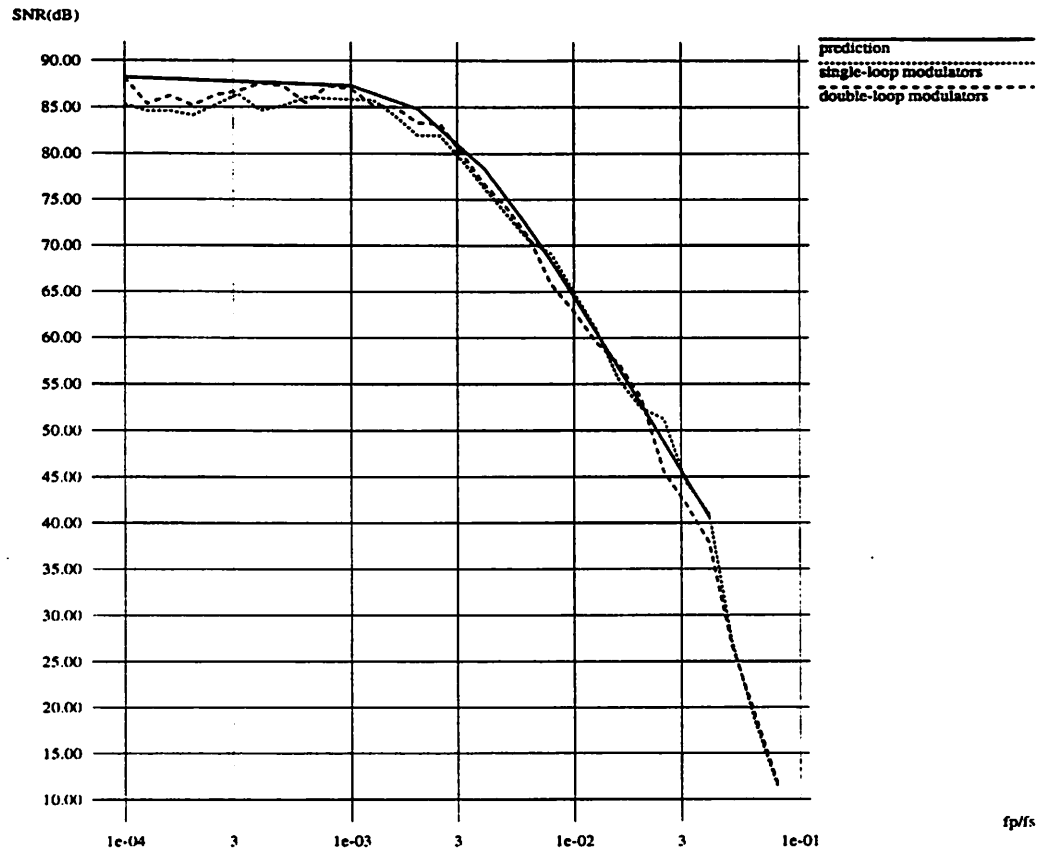


Figure 3.9 The effect of integrator leakage on the performance of continuous-time second-order $\Sigma\Delta$ modulators (A=-6dB, M=128) (consdm.graph2.1)

For second-order modulators, the spectral distribution of quantization noise and the inband quantization noise power are modified from Eq. 2.20 and Eq. 2.21 as

$$S_{ee}(f) = |H_E(f)|^2 \cdot \frac{S_Q}{f_s} = \left(\frac{2\pi}{f_s}\right)^4 (f_p^4 + f^4 + 2f^2 f_p^2) \cdot \frac{S_Q}{f_s} \tag{3.14}$$

and

$$S_B = \int_{-\frac{f_N}{2}}^{\frac{f_N}{2}} S_{ee}(f)\,df = \frac{(2\pi)^4}{M^5}\left(\left(\left(\frac{f_p}{f_N}\right)^2 + \frac{1}{12}\right)^2 + \frac{1}{180}\right) \cdot S_Q \tag{3.15}$$

From Eq. 3.15 and Eq. 2.21, the increase of the total inband quantization noise can be given as

$$\frac{S_B(\omega_P)}{S_B(\omega_p = 0)} = \frac{5}{\pi^4}\left(\frac{2\pi f_P}{f_s}\cdot M\right)^4 + \frac{10}{3\pi^2}\left(\frac{2\pi f_P}{f_s}\cdot M\right)^2 + 1 \tag{3.16}$$

Substituting $A_{dc} = \frac{f_s}{2\pi f_P}$ into Eq. 3.16 yields

$$\frac{S_B}{S_B(A_{dc}\rightarrow\infty)} = \frac{5}{\pi^4}\left(\frac{M}{A_{dc}}\right)^4 + \frac{10}{3\pi^2}\left(\frac{M}{A_{dc}}\right)^2 + 1 \tag{3.17}$$

It is noted that Eq. 3.17 is identical to the expression for discrete-time modulators given in [14]. The result of this equation and the simulation results are plotted in Fig. 3.9.

Eq. 3.16 and Eq. 3.17 demonstrate that in order to limit performance degradation due to integrator leakage to less than 1 dB,

$$f_p < \frac{f_s}{2\pi M} \quad \text{or} \quad A_{dc} > M \tag{3.18}$$

3.5 Integrator Gain Error

The factors that contribute to gain variation for discrete-time modulators, which use switched-capacitor integrators, are the capacitor matching and linear settling of the integrators. Linear settling of the integrator reduces the gain of the integrator by the settling accuracy factor. Nonlinear settling gives rise to harmonic distortion and will be mentioned in Section 3.8.

For continuous-time modulators, gain error results from the variation in RC or G_mC product of the integrators. Since RC and G_mC products are not as well-controlled as the capacitor matching, the performance degradation of continuous-time modulators due to the gain error can be substantial.

Gain variation of both integrators in single-loop continuous-time modulators and gain variation of the second integrator in double-loop continuous-time and second-order discrete-time modulators, do not directly affect the performance. This is because the variation is compensated by the one-bit quantizers. On the circuits level, gain variation, however, can affect the integrator output signal level, full-scale input level, etc. In contrast, gain variation of the first integrator in double-loop continuous-time and second-order discrete-time modulators affects the performance of the modulators because the first integrator output levels change relative to the inner feedback signals.

Changing the integrator gain affects the quantization noise attenuation and the modulator stability. The simulation results for both second-order discrete-time and double-loop continuous-time modulators are shown in Fig. 3.10. For integrator gain less than the nominal gain, the performance degradation is dominated by the reduction in quantization noise attenuation, and can be characterized as

$$\text{SNR reduction} = 20\log\left(\frac{G_1}{G'_1}\right) \tag{3.19}$$

where G_1 is the nominal gain and G'_1 is the gain in actual circuit implementation. Eq. 3.19 is invalid for gain larger than the nominal gain because the loop stability starts degrading. The modulators become unstable when G'_1/G_1 exceeds approximately 1.5.

In Fig. 3.10, it is shown that gain variation of ±30% results in performance degradation of less than 3dB

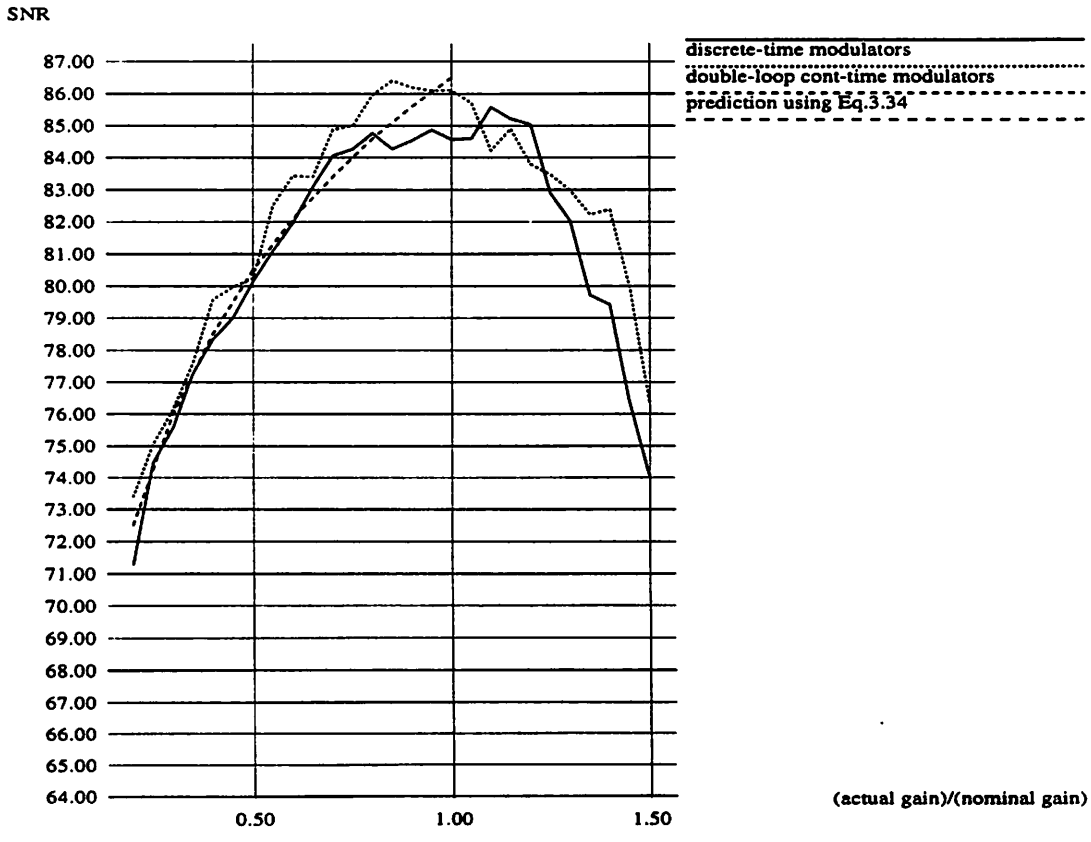
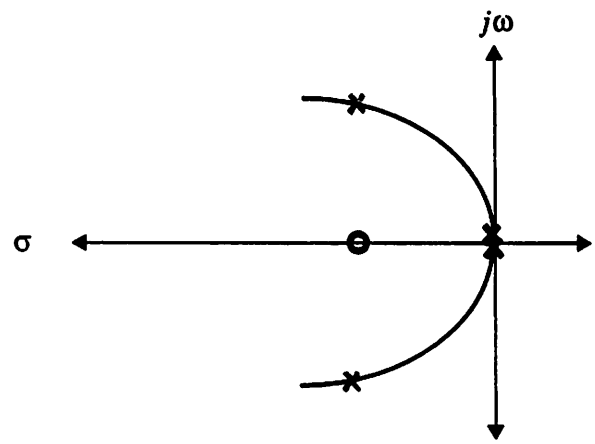


Figure 3.10 Predicted and simulated influence of gain error of the first integrator on second-order modulators performance

3.6 Integrator Non-dominant Poles

The function of the finite zeros in single-loop and double-loop second-order continuous-time modulators is to improve the loop stability by moving the closed-loop poles from the imaginary axis into the left-half plane. The non-dominant poles in the integrators degrade the loop stability by pushing the closed-loop poles closer to the imaginary axis and contribute excess phase lag at high frequencies. The root locus of the poles are shown in Fig. 3.11.

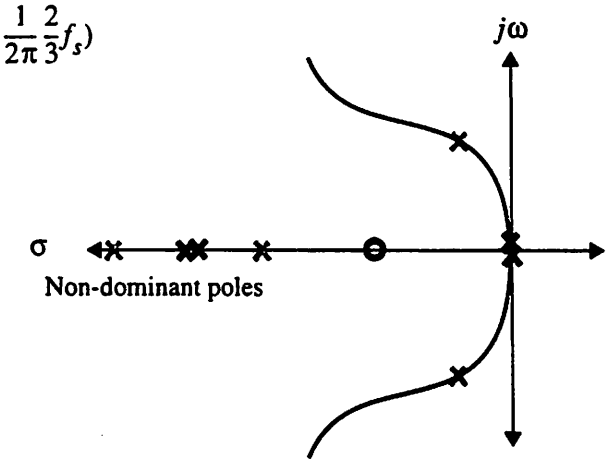


× open-loop pole

a) root-locus of modulators using ideal integrators

close-loop pole

O zero $(f_z = \frac{1}{2\pi}\frac{2}{3}f_s)$



b) root-locus of modulators using integrators with non-dominant poles

Figure 3.11 Root-locus of linearized continuous-time second-order modulators. The non-dominant poles degrade stability by pushing the closed-loop pole closer to the imaginary axis.

The effect of non-dominant poles on the modulator signal-to-noise ratio is determined by computer simulations as shown in Fig. 3.12. Each integrator is assumed to have one non-dominant pole. For single-loop modulators, the simulation results show that the non-dominant pole must be at least three times larger than the sampling frequency in order to limit the performance degradation to 3 dB. This requirement is equivalent to limiting the excess phase due to each integrator at the sampling frequency to less than 20 degrees. For double-loop modulators, the non-dominant pole can be two times larger than the sampling frequency in order to achieve the same level of performance.

The requirement of non-dominant pole frequency has a crucial implication because it limits the maximum sampling frequency which the modulator can be implemented for given integrators. The difference in non-dominant pole requirements also allows double-loop modulators to be operated at higher speed than single-loop modulators. This will be further described in Section 4.2.

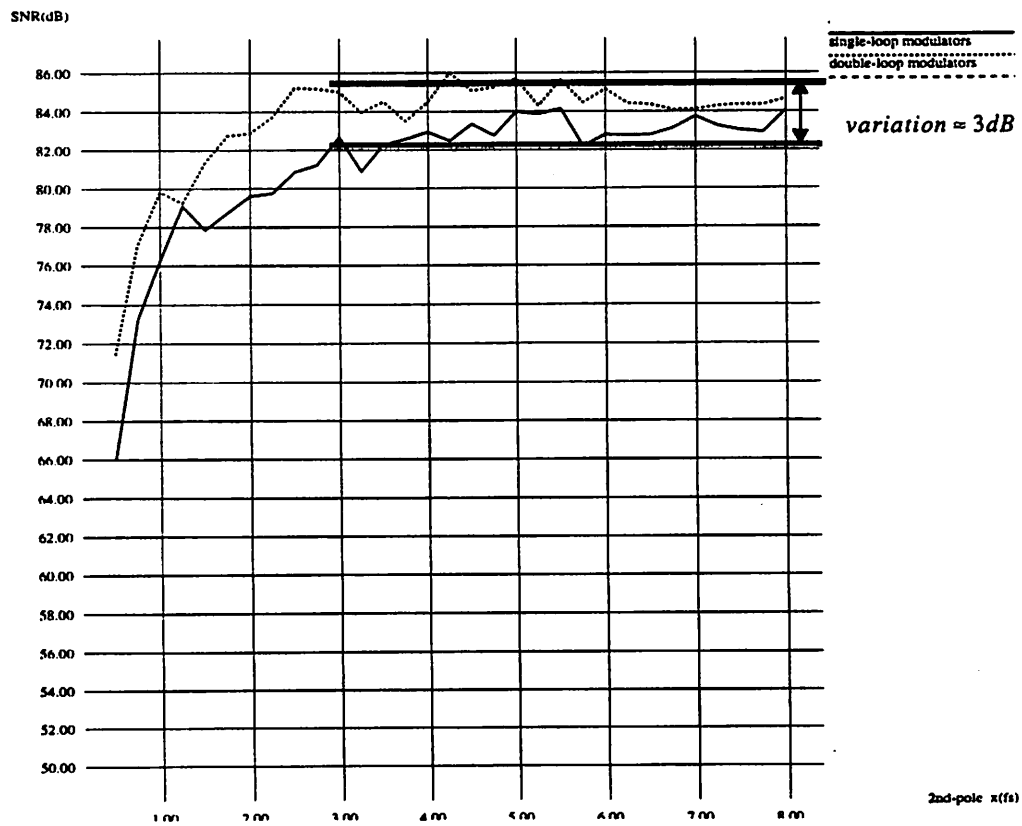


Figure 3.12 Simulated influence of integrator non-dominant poles on continuous-time second-order $\Sigma\Delta$ modulators (A=-6dB, M=128)

3.7 Comparator Delay

For first-order continuous-time modulators, it has been shown in [33] that delay time in the comparators can improve the performance of the modulators. This is due to the shift in the spectrum of the quantization noise according to the loop delay such that there is less quantization noise in the baseband. The result obtained from simulation is shown in Fig. 3.13 and Fig. 3.14. The delay time which yields optimum performance is $t_d = 0.25T$. The performance gain is as high as 15dB at small input levels. At higher input levels, the improvement becomes negligible. For $t_d = 0.75$, there is also performance gain at small input levels. However, at high input level, the performance is poorer than that of comparator without delay time.

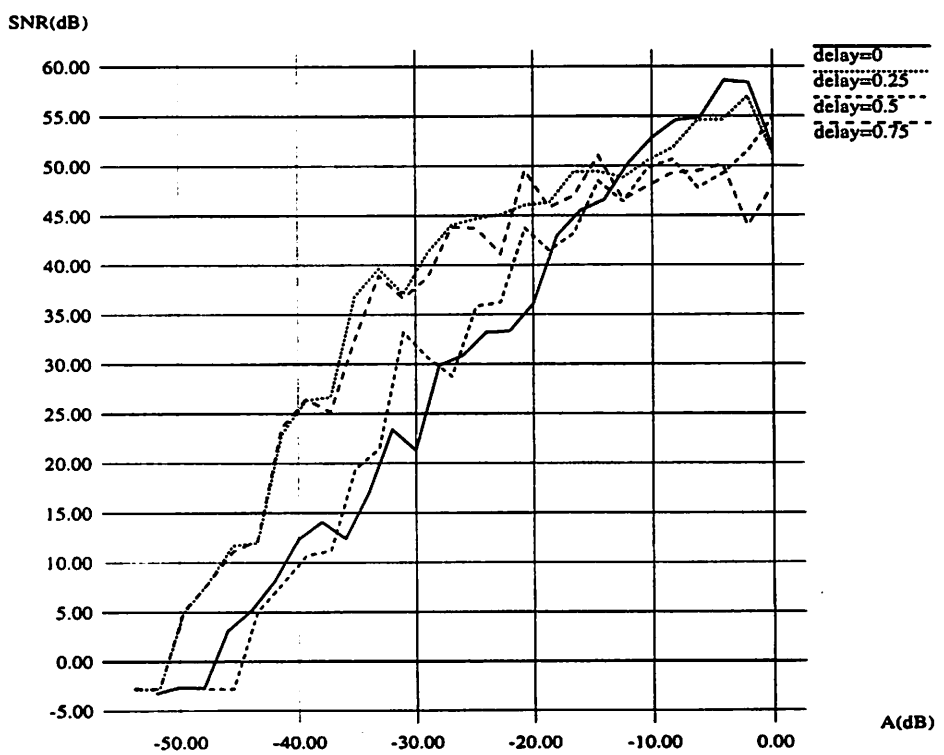


Figure 3.13 Simulated influence of comparator delay time on performance of first-order continuous-time modulators

For second-order continuous-time modulators, the delay time adds to the integrator excess phase; hence, the performance is degraded. The effect of delay time on single-loop and double-loop modulators are similar; therefore, only the results of single-loop modulators are shown in Fig.

3.14 in order not to clutter the graph. From the simulation results in Fig. 3.14, the comparator delay time must be less than $t_d = 0.2T$ for the SNR degradation to be less than 3dB.

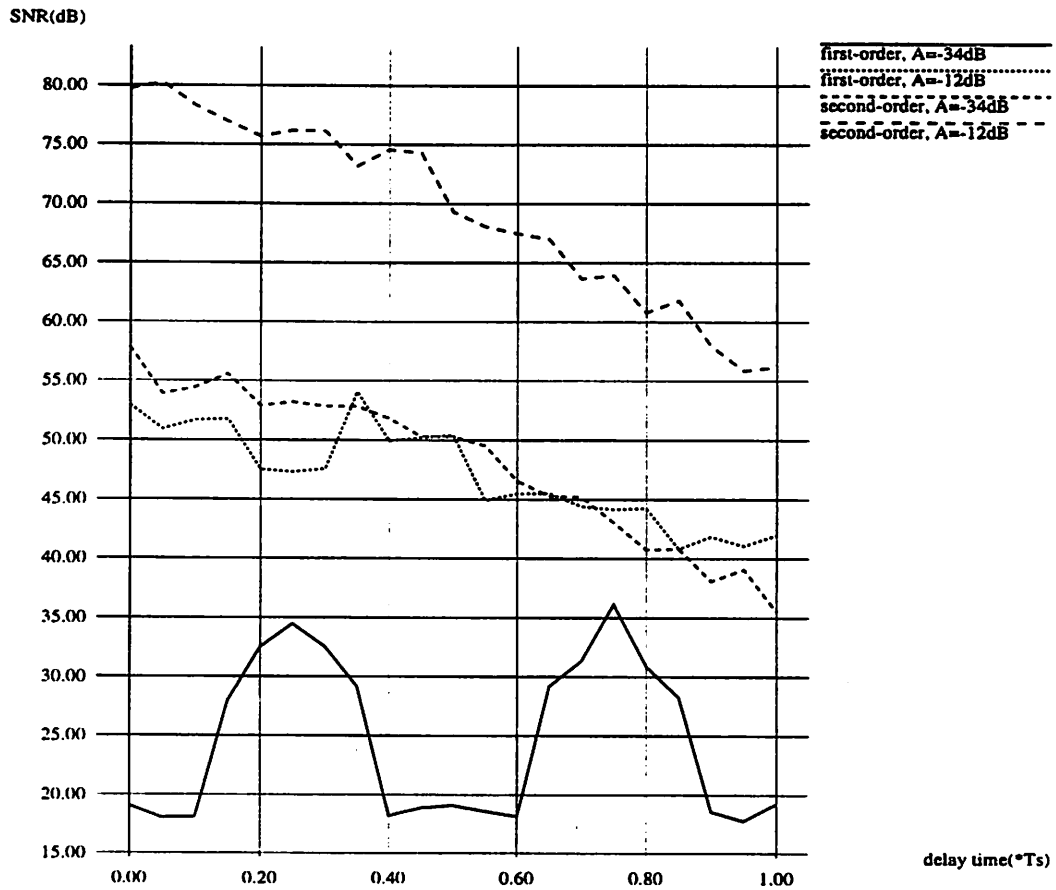


Figure 3.14 Performance degradation due to comparator delay time in first and second-order continuous-time modulators obtained from simulation (A=-6dB, M=128)

3.8 Integrator Settling Time

In switched-capacitor integrators, the settling process is dominated by two constraints: exponential decay output and finite slew rate. A one-pole model of the settling characteristics is given in [2] as

$$y((n+1)T_s) = y(nT_s) + g(x) \tag{3.20}$$

where

$$g(x) = \begin{cases} x\left(1 - e^{-\frac{T_s}{2\tau}}\right) & ;|x| < \tau\zeta \\ x - \mathrm{sgn}(x)\,\tau\zeta exp\left(\left(\frac{|x|}{\tau\zeta}\right) - \left(\frac{T_s}{2\tau}\right) - 1\right) & ;\tau\zeta \le |x| \le \left(\tau + \frac{T_s}{2}\right)\zeta \\ \mathrm{sgn}(x)\,\zeta\frac{T_s}{2} & ;|x| > \left(\tau + \frac{T_s}{2}\right)\zeta \end{cases}$$

where $\frac{T_s}{2}$ is the a half clock period available for integration, τ is the settling time constant of the integrator, and ξ is the maximum slew rate of the amplifier. For simplification, the slew rate is normalized as

$$\zeta_N = \frac{\zeta T_s}{2g\Delta} \tag{3.21}$$

where g is the gain of the integrator, and $\pm\frac{\Delta}{2}$ is the quantizer feedback level.

The number of settling time constants is defined as

$$n_\tau = \frac{T_s}{2\tau} \tag{3.22}$$

The settling characteristics can be explained for linear and non-linear settling cases as

Linear settling case ($|x| \le \tau\zeta$)

In this case, the integrators settle without slew rate limiting from the amplifiers; hence, the integrators settle to the same settling accuracy independent of the amplitude of the input signal. This is equivalent to reducing the integrator gain by a factor of $\left(1 - exp\left(-\frac{T_S}{2\tau}\right)\right)$. The effect of this gain reduction is explained as gain error in Section 3.3. For second-order modulators, the number of settling time constant, n_τ, can be as low as three or four due to their insensitivity to gain variation.

Non-linear settling case ($\tau\zeta < |x| \le \left(\tau + \frac{T_s}{2}\right)\zeta$)

From Eq. 3.20,

$$g(x) = x - \mathrm{sgn}(x)\,\tau\zeta exp\left(\left(\frac{|x|}{\tau\zeta}\right) - \left(\frac{T_s}{2\tau}\right) - 1\right) \tag{3.23}$$

Using Taylor series, this equation can be expanded into,

$$g(x) = x - A\,\mathrm{sgn}(x)\left(1 + \frac{|x|}{\tau\zeta} + \frac{|x|^2}{2!\,(\tau\zeta)^2} + \frac{|x|^3}{3!\,(\tau\zeta)^3} + \ldots\right) \tag{3.24}$$

$$= \mathrm{sgn}(x)\left(|x| - A\left(1 + \frac{|x|}{\tau\zeta} + \frac{|x|^2}{2!\,(\tau\zeta)^2} + \frac{|x|^3}{3!\,(\tau\zeta)^3} + \ldots\right)\right) \tag{3.25}$$

where $A = \tau\zeta e^{-1} exp\left(-\frac{T_s}{2\tau}\right)$. It is obvious that slew limiting integrators create harmonic distortion. In contrast to analog feedback loops, the feedback loops in $\Sigma\Delta$ modulators do not attenuate the harmonic distortion. This is because, in $\Sigma\Delta$ modulators, only the average of the feedback signal, not the feedback signal itself, tracks the input signal. Therefore, the amplitude of the first integrator input is not reduced as in analog feedback loops. Another interesting fact is that, due to the alternating feedback level between positive and negative values, even-order harmonics as shown in Eq. 3.24 and Eq. 3.25 are almost completely cancelled.

However, hand-calculating the amount of harmonic distortion using Eq. 3.24 proves to be very tedious; therefore, the effect of settling process on the performance of the modulators was determined by computer simulations. Fig. 3.15 shows results obtained from second-order modulators with integrator gain of 0.5, quantizer feedback level equal to ± 0.5, and the settling model incorporated in the first integrator. The harmonic distortion from the second integrator can be obtained by similar simulations, but the requirement is less stringent because the distortion is reduced by the gain of the first integrator.

In Fig. 3.15, the upper left region of the graph where $\zeta_N > n_\tau$ is the linear settling region. Due to the absence in harmonic distortion, high performance can be achieved even for slow operational amplifiers. The rest of the graph where $\zeta_N < n_\tau$ is the nonlinear settling region. The harmonic distortion from the integrators imposes the maximum performance which can be achieved from the modulators. It can be seen that at large n_τ, the amplifier settling speed is sufficiently fast to reduce the nonlinear effects of the slew limiting to negligible levels.

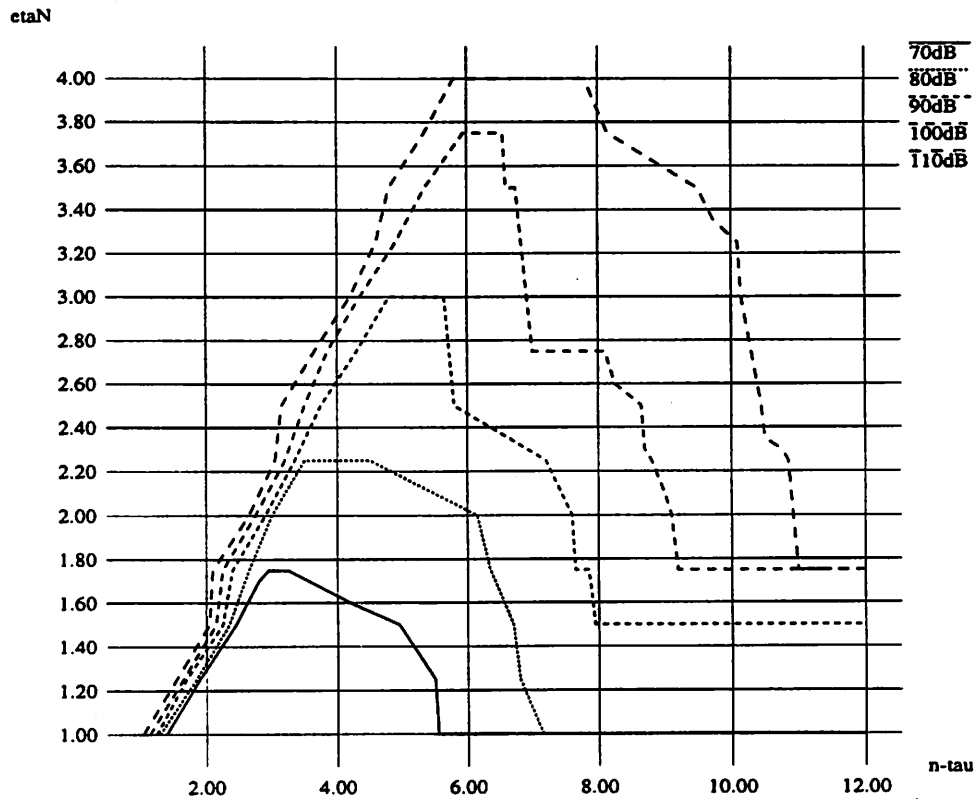


Figure 3.15 SNR versus settling of second-order $\Sigma\Delta$ modulators. The results in this figure are similar to that obtained in [2].

The model in Eq. 3.20 and the results in Fig. 3.15 are for integrators with one pole. To model actual integrators more accurately, the model should be extended for integrators with two poles or complex poles.

3.9 Summary

In this chapter, several nonidealities of continuous-time modulators were studied, then compared to that of discrete-time modulators. The results are summarized below in the order of their importance. The most two stringent requirements, clock jitter and transconductor linearity, will be further discussed along with potential solutions in Chapter 4.

- Compared to discrete-time modulators, continuous-time modulators are more susceptible to clock jitter by approximately a factor of M, the oversampling ratio. The required clock jitter level can be in the range of sub-picoseconds.
- The first transconductor of continuous-time modulators must be as linear as the overall accuracy of the modulator. The harmonic distortion from the second transconductor, on the other hand, is attenuated by the gain of the first integrator. The attenuation depends on the oversampling ratio and is given as $(6 \cdot log_2 M - 10)$dB.
- The speed of continuous-time modulators is limited by non-dominant poles of the integrators. To limit the performance degradation to within 3dB, non-dominant poles of the integrators in single-loop and double-loop modulators must be at least three times and twice larger than the sampling frequency, respectively.
- Comparator delay can improve the performance of first-order continuous-time modulators by as much as 15dB at small input levels. For second-order continuous-time modulators, the comparator delay time must be limited to less than 20% of the sampling period for the performance degradation to be less than 3dB.
- The performance of single-loop continuous-time modulators is not affected by the integrator gain variation. This is because the variation is compensated by the one-bit quantizers. For double-loop continuous-time modulators, only the gain variation in the second integrators is compensated by the one-bit quantizers. Nevertheless, double-loop modulators are quite insensitive to gain variation of the first integrator. Gain variation in the first integrator of ±30% reduces the modulator performance by less than 3dB.
- Finite DC-gain integrators degrade the performance of continuous-time modulators. To limit the performance reduction to within 1dB, the DC-gain of the integrators has to be larger than the oversampling ratio of the modulators.

Further discussions of the speed of the modulators, clock jitter, and integrator implementations are in Chapter 4.

As an example of realistic implementations, circuit requirements for continuous-time and discrete-time modulators with oversampling ratio of 128 are summarized in Table 3.1. It should be

noted that discrete-time modulators require higher frequency for the integrator non-dominant poles. This is related to the lower achievable sampling frequency of discrete-time modulators compared to continuous-time modulators and is discussed in Section 4.2.

Table 3.1 A summary of circuit requirements and performance of continuous-time and discrete-time second-order modulators. (M=128, A=-6dB)

	single-loop continuous-time modulator	double-loop continuous-time modulator	discrete-time modulator
Clock jitter (σ_t/T_s)	10^{-4}	10^{-4}	10^{-2}
First integrator HD_2 and HD_3	0.005%	0.005%	0.005%
Second integrator HD_2 and HD_3	0.2%	0.2%	0.2%
Integrator DC-gain	1000	1000	1000
Integrator non-dominant pole (f_{P2}/f_s)	3.5	2.5	10
Comparator delay (t_d/T_s)	0.15	0.15	0.5
First integrator gain	0.8	0.8	0.99
Peak signal-to-noise ratio	80	78	83
Ideal peak signal-to-noise ratio	86	85.5	87

CHAPTER 4

Comparison Between Continuous-time and Discrete-time modulators

4.1 Overview

The motivation for investigating continuous-time modulators is to find a solution to integrator settling time, the factor which limits the maximum speed of discrete-time modulators. In this chapter, it will be shown that continuous-time modulators can achieve higher speed compared to discrete-time modulators. Clock jitter and integrator nonlinearity, the two critical circuit requirements of continuous-time modulators, will be discussed and possible solutions will be suggested. Cascaded continuous-time modulators will be discussed as a means to increase the performance of continuous-time modulators by reducing the oversampling ratio.

4.2 Sampling Frequency

The main factor which limits the maximum sampling frequency of continuous-time modulators is the non-dominant poles of the integrators. The results in Section 3.6 show that to limit performance degradation to less than 3dB, the integrator non-dominant pole must be at least three times larger than the sampling frequency for single-loop modulators and two times for double-loop modulators.

For discrete-time modulators, the integrator settling time limits the maximum sampling frequency. The required slew rate and time constant for the integrators was shown in Fig. 3.15.

To illustrate the speed advantage of continuous-time modulators, an example is given here for an amplifier with the unity-gain frequency of 200 MHz, and a non-dominant pole at 400 MHz. For single-loop continuous-time modulators, choosing the non-dominant pole to be 3.5 times larger than the sampling frequency, the modulators can achieve sampling frequency of 115MHz. And for double-loop continuous-time modulators, choosing the non-dominant pole to be 2.5 times larger than the sampling frequency yields sampling frequency of 160MHz.

For discrete-time modulators, using the number of settling time constant of 10 (see Fig. 3.15), and only half of the cycle is available for integration. The integrator time constant is

$$\tau = \frac{1 + \frac{C_1}{C_2}}{2\pi f_u} = 1.2ns \tag{4.1}$$

where $\frac{C_1}{C_2}$ is the integrator gain and is assumed to be 0.5. Therefore,

$$f_s = \frac{1}{2 \cdot n_\tau \cdot \tau} = 42MHz \tag{4.2}$$

Compared to second-order discrete-time modulators, single-loop and double-loop second-order continuous-time modulators can achieve higher sampling frequency by approximately a factor of three and four, respectively.

4.3 Clock Jitter

In Section 3.2, the effect of clock jitter on discrete-time and continuous-time modulators was discussed. The ratio of the required clock jitter for both modulators was given in Eq. 3.5 as

$$\frac{\sigma_{t_{cont}}}{\sigma_{t_{disc}}} = \frac{\pi}{4M} \approx \frac{0.8}{M} \tag{3.19}$$

Depending on the oversampling ratio, σ_t for continuous-time modulators can be one to two orders of magnitude lower than that for discrete-time modulators. As shown in Fig. 3.3, a continuous-time modulator can require clock jitter in the range of sub-picoseconds. This level of jitter

cannot be attained by ring-oscillator based phase-locked loops, which achieve jitter in the range of tens of picoseconds. The clock for continuous-time modulators must be generated by crystal oscillators or phase-locked loops with off-chip tuned-LC tank circuits. Furthermore, clock distribution circuits must be carefully designed to minimize electronic noise and any interference from other sections of the circuits.

4.4 Integrator Implementations

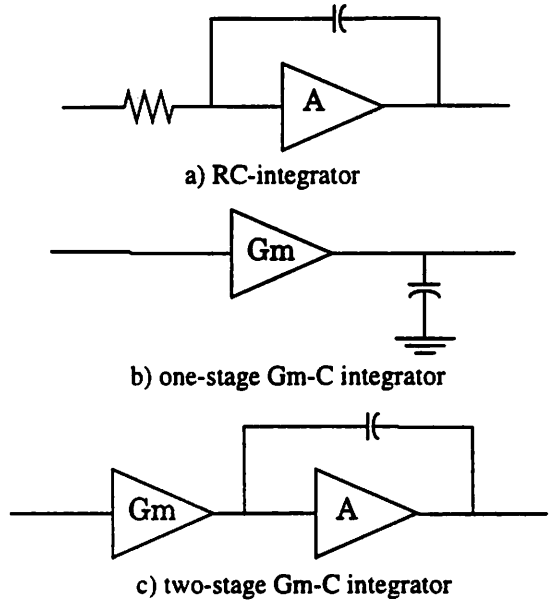


Figure 4.1 RC and Gm-C integrators

Continuous-time integrators can be implemented as RC-integrators or Gm-C integrators shown in Fig. 4.1. The advantages and disadvantages of each configuration are summarized here.

The main concerns for RC-integrators are the resistor linearity and the high value of integrated resistor and capacitor tolerances. The voltage coefficients of integrated resistors are normally an order of magnitude higher than that of integrated capacitance [35]. These coefficients can be too high for the integrated resistor to be used in the first integrator, which has to be as linear as the overall accuracy of the modulator (see Section 3.3). The solutions are to either use a high quality discrete resistor or eliminate the resistor by using current instead of voltage as the modulator input.

In contradict to switched-capacitor integrators in which the gain is determined by the capacitor matching, the time constant of RC-integrators is determined by the absolute value of integrated resistors and capacitors, which can have combined tolerances as high as ±30%. According to Section 3.5, second-order continuous-time modulators are quite insensitive to integrator gain error. Gain variation of ±30% in the first integrators of double-loop modulators results in performance degradation of less than 3dB. This high level of gain error, however, can be a problem in implementing cascaded continuous-time modulators, which require accurate gain to cancel quantization noise (see the discussion in Section 4.5). Another drawback of RC-integrators is the loading effect of the resistors presents to the previous stages.

Another approach to implementing continuous-time integrators is to use Gm-C integrators. The benefits of MOS Gm-C integrators are the adjustable time constants and the infinite input resistance. The main drawback is the limited linearity of Gm-stage of approximately 50dB [36]. This level of linearity, however, is usually high enough for the Gm-C integrator to be used as the second integrator as shown in Section 3.3. A discussion of one-stage and two-stage Gm-C integrators can be found in [37].

4.5 Higher-Order Modulators

It is shown in Section 4.2 that second-order continuous-time modulators can achieve sampling frequency approximately three times higher than second-order discrete-time modulators. However, there exist several methods to implement discrete-time modulators which can offset this speed advantage, namely, higher-order modulators, multibit modulators, etc. In this section, higher-order cascaded modulators will be discussed as an approach which can increase the performance of continuous-time modulators beyond second-order modulators.

The principle of cascaded modulators is to use a following stage or stages to measure the quantization error, then subtract it from the previous stage. Theoretically, there is no limit on the performance of cascaded modulators. In practice, however, the uncancelled quantization noise leakage from the first stage due to integrator gain error and integrator leakage, limits the maximum performance achievable from cascaded modulators.

The gain error requirement of higher-order cascaded modulators is stringent compared to second-order modulators. This is because the performance of cascaded modulators relies on noise cancellation. Hence, any gain mismatch both in the first and second integrators results in incomplete noise cancellation. The performance increase due to adding the cascaded stage is thus limited by gain error as shown below

$$\text{max SNR gain} = -20\log\left|1 - \frac{G_1' G_2'}{G_1 G_2}\right| \tag{4.3}$$

where G_1', G_1, G_2', and G_2 are the actual and nominal gain of the first and the second integrators in the first stage, respectively. This equation presents the fundamental limit of the performance which can be increased by adding cascaded stages. This equation also suggests that implementing cascaded continuous-time modulators is difficult because of the inaccuracy of RC products in continuous-time integrators. A possible solution to this problem is to use an LMS filter as a post-processor to correct the gain error.

When integrators have finite DC-gain, there is some leakage quantization noise from the first stage which cannot be canceled by the following stage. Therefore, the integrator leakage requirement of cascaded modulators is stricter compared to second-order modulators. The baseband quantization error power of cascaded modulators using finite DC-gain integrators and second-order modulators as the first stage is given in [12] as

$$S_B = S_{B0} + \frac{8\pi^2}{9M^3 A_{dc}^2} + \frac{2}{3MA_{dc}^4} \tag{4.4}$$

where S_{B0} is the baseband quantization error with infinite DC-gain.

Furthermore, there is a limit in performance increase for cascaded continuous-time modulators which does not exist in cascaded discrete-time modulators. This is because the noise shaping function and the delay of continuous-time modulators cannot be exactly realized in the digital domain as in discrete-time modulators. Computer simulations show that the limitation depends on the oversampling ratio and is different between single-loop and double-loop modulators.

4.6 Summary

Compared to second-order discrete-time modulators, single-loop and double-loop second-order continuous-time modulators can achieve higher sampling frequency by approximately a factor of three and four, respectively. The stringent linearity requirement of the first integrator in continuous-time modulators can be alleviated by using, either an external resistor to implement the first transconductor or current instead of voltage as the modulator inputs. The second-integrator, which requires lower linearity, can be implemented as an Gm-C integrator. The required clock jitter, in the range of sub-picoseconds, can be achieved by using crystal oscillators.

The oversampling ratio of continuous-time modulators can be reduced by using higher-order modulators such as cascaded modulators. The drawbacks, however, are stringent requirements on the the leakage and gain error of the integrators.

CHAPTER 5

Conclusion

5.1 Conclusion

In this research, second-order continuous-time modulators have been studied and compared to discrete-time modulators. Single-loop and double-loop second-order continuous-time modulators were discussed. The noise shaping function and the dynamic range of generalized Lth-order continuous-time modulators were derived. Nonidealities associated with the implementations of continuous-time modulators were investigated. The advantage and disadvantage of continuous-time modulators were shown.

Single-loop and double-loop continuous-time modulators require the same integrator time constants. Finite zeros are required in both single-loop and double-loop continuous-time modulators in order to stabilize the loops. The zero in the single-loop modulator is added to one of the integrators in the forward path, while the zero in the double-loop modulator is implemented by the inner-feedback loop. The dynamic range of continuous-time modulators are similar to that of discrete-time modulators.

Compared to second-order discrete-time modulators, single-loop and double-loop second-order continuous-time modulators can achieve higher sampling frequency by approximately a fac-

tor of three and four, respectively. The drawbacks of continuous-time modulators are in the implementations. In order to alleviate the strict linearity requirement of the first transconductor, an external resistor or a current input must be used. The requirement which is more difficult to meet is the clock jitter. The required clock jitter in the range of sub-picoseconds can be achieved by using crystal oscillators.

Even though second-order continuous-time modulators can achieve higher sampling speed compared to second-order discrete-time modulators, there are several methods which can reduce the oversampling ratio of discrete-time modulators, namely, higher-order modulators and multibit modulators. These techniques must be applied to continuous-time modulators in order to reduce the oversampling ratio of continuous-time modulators.

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