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BULK CMOS**

by

Eugene Lau Cheung

Memorandum No. UCB/ERL M96/57

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Abstract

The goal of this project is to investigate a circuit for generating 80V in a bulk CMOS technology. This voltage is needed for powering a micromachined electrostatic actuator, and it must be generated from a 5V supply. Although inductive circuits are the most power efficient, the application requires a monolithic solution, which limits circuit selection to switched-capacitor or charge-pump types. The Dickson charge pump is chosen for implementation.

A test circuit consisting of a two-stage Dickson charge pump has been fabricated in a standard 2 μ m n-well CMOS process. Ideally, such a circuit boosts the input voltage by up to two clock swings; practical devices and parasitics lower the voltage somewhat. A cascaded string of these stages of diodes and capacitors is required to attain higher voltages. Because true diodes are unavailable, the blocking device used is a PMOS transistor in an n-well, shunted by a parasitic substrate bipolar with substantial leakage current.

Measurement results show that the two-stage charge pump functions with input voltages up to $V_{IN}=73V$, which results in $V_{OUT}=80V$. The unloaded ($I_{OUT}=0$) voltage boost provided by the two-stage circuit over the input is measured to be 7.2V for input voltages from 0V to 73V. The leakage current from the parasitic bipolar, however, coupled with the finite output impedance of the circuit, limits the actual performance when stages are cascaded, in terms of current drive, output impedance, and attainable output voltage. However, 80V seems to be an achievable goal within the bulk CMOS technology, at a cost of added circuit area.

In order to make a higher performance circuit to meet the goals of this project, the device leakage may be circumvented by various techniques, or perhaps an IC technology such as silicon-on-insulator could provide a technological solution.

Acknowledgments

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1 Introduction

1.1. Application

In the field of magnetic data storage, data density increases constantly and rapidly, driven by a seemingly unbounded consumer demand for more storage capacity, and the more recent popularity of portable computing platforms. One proposal for the next generation of hard disk drives is projected to feature data bit density an order of magnitude higher than that of today's state of the art ($\sim 1\text{Gbit/in}^2$) drives [1]. Assuming a twofold increase in electrical system bandwidth, this implies a track pitch of approximately 25ktpi, as compared to 5ktpi in present-day advanced drives. Whereas present drives utilize servo bandwidths of approximately 500 to 600Hz for positioning the recording head, achieving 25ktpi will require a servo bandwidth of about 2.5kHz. At such frequencies, conventional single-stage arm actuation is insufficient. The bandwidth requirement can be met with a two-stage actuator that adds a fine-positioning stage for the recording head to supplement the coarse arm positioning provided by a conventional voice coil.

The desire for high speed, small size, and batch manufacturability has led to the choice of a microfabricated motor for the second-stage actuator, and existing fabrication technology is compatible with electrostatic actuation. The present system design (Figure 1-1) places the microactuator between the suspension and the slider, permitting the slider to move over several track widths [1]. The microactuator presently being fabricated (Figure 1-2) is actually a circular comb drive, with a single set of rotors interdigitated with two sets of stators. The two stators are biased at +40V and -40V, and the rotor is controlled by a signal with up to 25kHz bandwidth, to achieve an overall 2.5kHz loop bandwidth for the combined electrical and mechanical system. This differential voltage connection scheme allows a first-order linear force vs. voltage relationship.

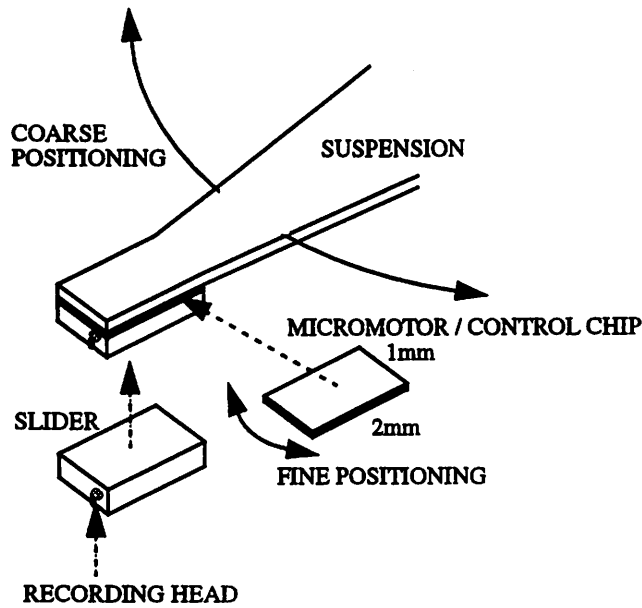


Figure 1-1. Disk drive arm.

This schematic closeup of the disk drive arm shows how the microactuator chip is placed between the suspension and the slider, which contains the magnetic read/write head [1].

Power to the micromotor must be provided by an IC the same size (1mm x 2mm now, 1mm x 1mm within 5 years) as the motor chip. Because of the impracticality of routing high-voltage lines down the disk drive arm, the power supply circuit must also provide DC-DC conversion from a nominal 5V or 3.3V (2.2V within 5 years) to the required +/-40V, or 0-80V [1].

1.2. Performance Requirements

The motor presents a variable capacitive load (Figure 1-3) to the drive circuit, with a maximum value of 8pF, including parasitics. The frequency of 25kHz results in a charging time of 20μs, which combined with the 40V swing implies a continuous charging current of 16μA. This is the minimum current which must be applied to the motor to meet the full-amplitude bandwidth requirement. In terms of output resistance of the high-voltage supply, the 25kHz frequency specification into the 8pF load corresponds to an output resistance of 800kΩ.

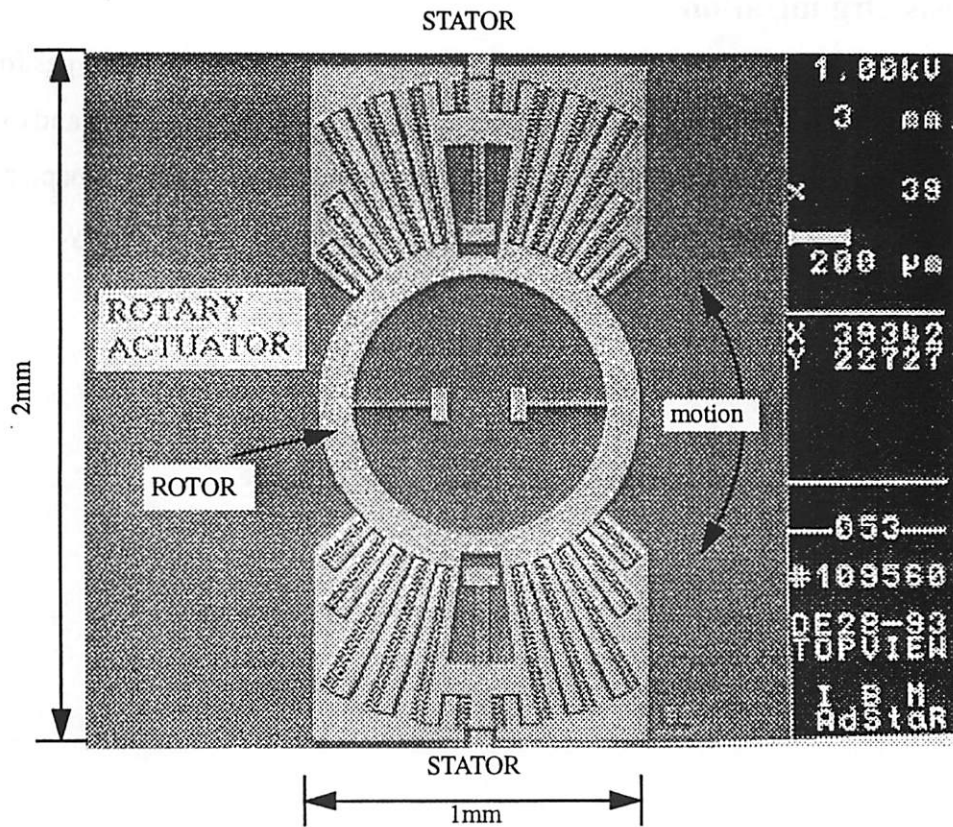


Figure 1-2. Rotary Microactuator

Micrograph courtesy of Dr. Long-Sheng Fan, IBM Almaden Research Center [2].

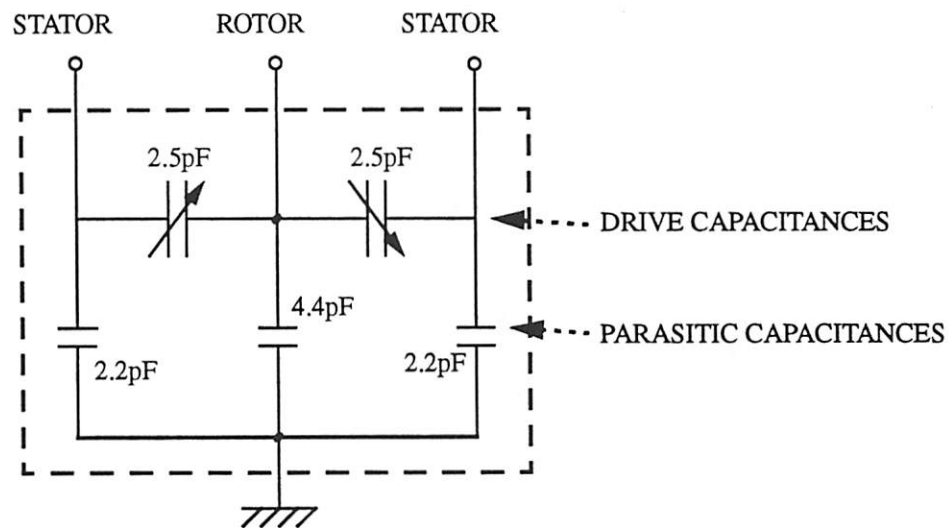


Figure 1-3. Electrical Schematic of Microactuator

1.3. Thesis Organization

This thesis consists of six chapters. Chapter 2 discusses the available circuit types for voltage conversion. Chapter 3 deals with the implementation of the chosen circuit and explains technology issues. In Chapter 4 test results and measurements are shown. Chapter 5 outlines possible directions for future work, and Chapter 6 summarizes this study.

2 Circuit Topology

2.1. Overview

There are basically two broad circuit types available for stepping voltage up, determined by whether or not inductive devices are used. Inductive circuits generally make use of inductors as current sources for charging capacitors above the supply rail voltage, or use mutual inductance to boost AC voltages before rectification and capacitive filtering. Purely capacitive circuits are based on redistribution of charge among various capacitors, and treat the capacitors as temporary voltage sources while switching their terminal connections.

2.2. Inductive Circuits

With the advent of thin-film monolithic inductors [3] and transformers [4], previously unattainable inductive circuits may be integrated onto the same substrates as the devices or circuits being powered. These developments promise gains in power density and efficiency compared to purely capacitive circuits, and higher integration and smaller size relative to discrete implementation, all at the expense of higher process complexity. Unfortunately, these magnetic devices are still unavailable outside of research laboratories.

2.2.1. Inductive Boost

For higher power discrete dc-dc conversion applications, the inductive boost circuit is often most attractive because of its high power density and efficiency, typically better than 95% [3]. One such circuit, the direct upconverter, is shown in Figure 2-1. In the high-frequency operation typically seen in practice, the input inductor approximates a current source which charges the output capacitor, and allows it to behave roughly as a voltage source even as it is drained by the output load.

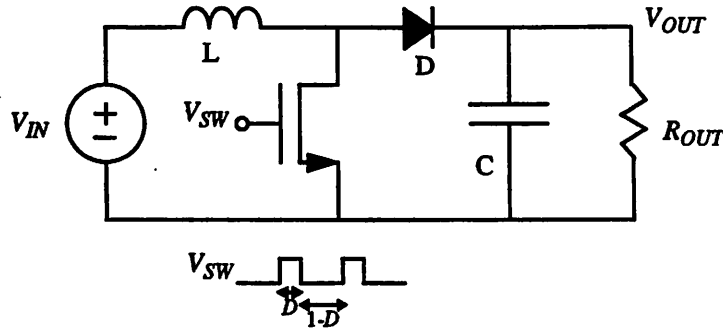


Figure 2-1. Direct Upconverter Circuit

When the switch, in this case a MOSFET, is operated with a duty cycle D , the output voltage is given by $V_{OUT} = 1/(1 - D) \cdot V_{IN}$.

2.2.2. Mutual Inductance

A simpler but possibly less energy-efficient method of conversion is voltage transformation followed by rectification, which is also widely used in discrete power supplies, but heretofore unseen in ICs. The same fundamental technology used for thin-film inductors may be used to fabricate similar transformers, which will multiply an input clock voltage (or two differential clocks) by the turns ratio [4]. The resulting high-voltage AC signal may then be rectified to supply a DC rail, as can be seen in the simplified schematic of Figure 2-2.

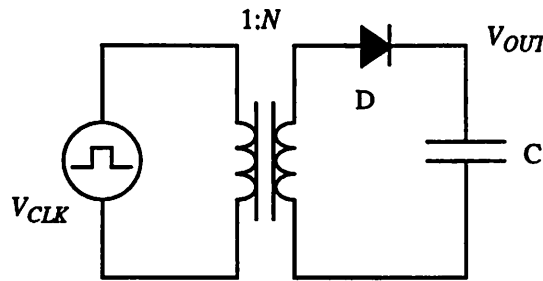


Figure 2-2. Simple Transformer-Rectifier Circuit

The transformer turns ratio N provides a voltage gain such that $V_{OUT} = N \cdot V_{CLK} - V_D$.

2.3. Switched Capacitor

In a switched-capacitor circuit, the switch frequency is generally high enough that the capacitor may be considered as a voltage source. Alternating between combinations of

series and parallel connections allows different rational voltage conversion ratios to be achieved. An example of such a circuit is shown in Figure 2-3. In this circuit, the switches

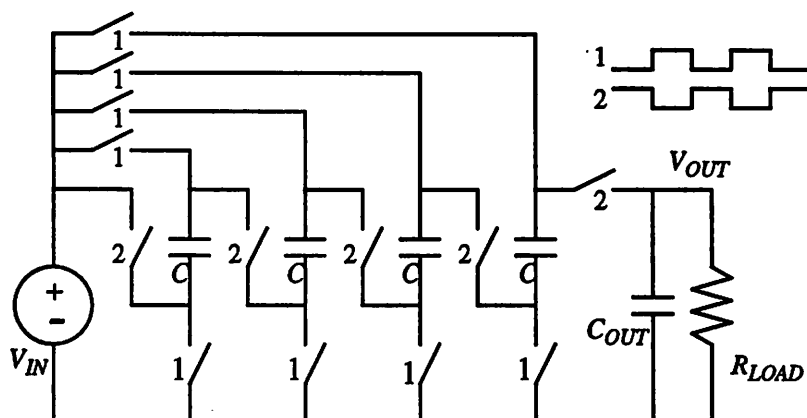


Figure 2-3. Switched-Capacitor Circuit from [5]

are connected to two non-overlapping clock phases. In phase 1, the capacitors C are connected in parallel, and are all charged to V_{IN} . In phase 2, the same capacitors are switched to be in series with V_{IN} , and V_{OUT} then becomes $5V_{IN}$.

2.4. Charge Pump

The diode-capacitor voltage multiplier, or charge pump, is one of the simplest methods for generating higher voltages from lower supplies. These circuits are purely capacitive, wherein one or more AC “clock” signals is generated and then fed into a circuit consisting of capacitors and diodes. In general, the diodes allow charge to flow only one way, from input to output or vice versa, hence allowing the output voltage to be much higher in magnitude than the input voltage.

For the given application, this seemed to be the most viable circuit option because of implementation considerations. The magnetic devices are not readily available yet, and the switched capacitor circuits require high switch control voltages while not offering any advantage in terms of area over the charge pump. The area of the circuit is inversely proportional to capacitance in both cases.

2.4.1. Dickson vs. Cockcroft-Walton

An early (ca. 1930) physicists' tool for generating very high voltages, still in use today [6], is the Cockcroft-Walton voltage multiplier [7]. Shown in Figure 2-4, it is an interconnec-

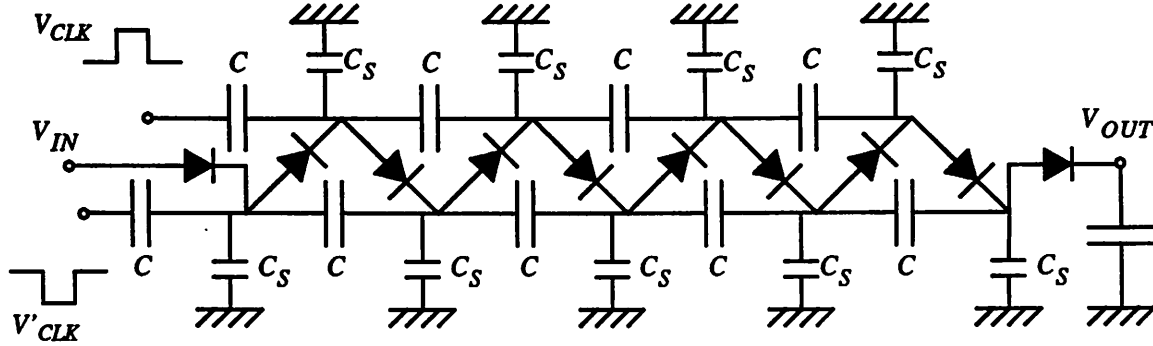


Figure 2-4. Cockcroft-Walton Voltage Multiplier

tion of diodes and series storage capacitors which provides, ideally, an output voltage

Equation 2-1.
$$V_{OUT} = V_{IN} - V_D + N \cdot [V_{CLK} - V_D]$$

where N is the number of stages, V_D is the diode turn-on voltage, and V_{CLK} is the clock swing. In reality, the stray capacitance C_S limits the voltage contributed by each stage, and this effect compounds geometrically into multiple stages:

Equation 2-2.
$$V_{OUT} = V_{IN} - V_D + (V_{CLK} - V_D) \cdot \frac{r - r^{N+1}}{1 - r}$$

where

Equation 2-3.
$$r = \frac{C}{C + C_S}$$

and so

Equation 2-4.
$$V_{OUT} \approx V_{IN} - V_D + (V_{CLK} - V_D) \cdot \frac{C}{C_S}$$

for large N .

In the discrete implementations for which the circuit was originally intended, these parasitics could be rendered negligible by using suitably large values of storage capacitor C . When constructed on monolithic substrates the effect dramatically worsens because of the substantial bottom-plate contribution to C_S , and so it is typically difficult to generate voltages of more than twice the clock voltage [8]. Therefore the Cockcroft-Walton circuit is not suitable for this application.

The newer Dickson multiplier circuit presented in [8], Figure 2-5, provides an alternate

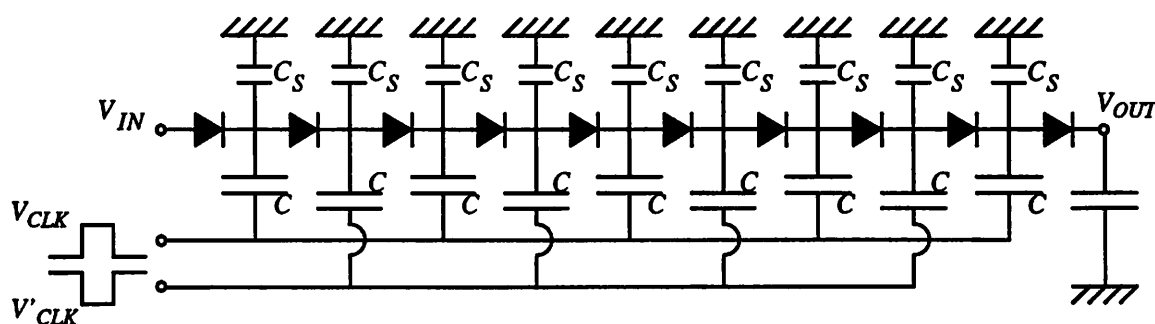


Figure 2-5. Dickson Voltage Multiplier

topology which ideally performs the same as the Cockcroft-Walton charge pump. In reality, however, the circuit is far less sensitive to stray capacitances, as these parasitics only divide into the per-stage voltage gain once, without the compounding evident in the Cockcroft-Walton case:

Equation 2-5.
$$V_{OUT} = V_{IN} - V_D + N \cdot (r \cdot V_{CLK} - V_D).$$

This circuit is commonly used in such IC applications as high-voltage supplies for EEPROMs and RS-232 drivers. Its one disadvantage relative to the older circuit is that capacitors in the later stages must handle voltages up to the output voltage. This would be a major shortcoming in the discrete case, with V_{OUT} in the kilovolts; it is less of a consideration in lower-voltage IC implementations.

2.4.2. Operation

In the Dickson multiplier, each stage dictates the minimum voltage for the following stage by means of the intermediate diode. For instance, ideally, the first diode holds a minimum

cathode voltage of $(V_{IN} - V_D)$, the following diode holds a minimum cathode voltage of $(V_{IN} - V_D + V_{CLK} - V_D)$, and so on. Each clock swing causes a boost of $(rV_{CLK} - V_D)$ volts at alternate nodes, and makes available a maximum charge of $C(rV_{CLK} - V_D)$ coulombs. This results in a maximum available current of $C(rV_{CLK} - V_D)f_{CLK}$, which when divided by the output voltage of $N(rV_{CLK} - V_D)$ results in an output resistance of N/Cf_{CLK} [8]. The quantitative circuit behavior is summarized in Chapter 4.

3 Circuit Design

3.1. Overview

There were two IC processes available to fabricate circuits for this application. One was the 2 μ m n-well “baseline” CMOS process available in the Berkeley Microlab, and the other was an experimental sub-micron thin-film fully-depleted CMOS SOI process made available through the Hong Kong University of Science and Technology (HKUST). The former is a very common technology, similar to many of the older, commercially available ones from established foundries, while the latter represents the state of the art in process design for high-speed digital circuits.

3.2. Bulk CMOS

In bulk CMOS, the common substrate can only provide junction isolation for separation of individual devices. Assuming an n-well process, the p-substrate must be connected to the lowest potential, and all devices must have junctions which will face this connection. Hence, for a Dickson charge pump, the last device in the chain must have a junction which will withstand a reverse bias potential of V_{OUT} ; all the other devices will see lower-magnitude potentials relative to the substrate. The source/drain doping levels for a typical 5V CMOS process are so high that breakdown voltages are usually in the 20V range. Therefore the obvious method of diode-connecting substrate devices is ruled out, even without considering the body effect problem discussed in [9].

Several test devices and circuits were fabricated in the Berkeley Microlab 2 μ m baseline CMOS run. One device is a “floating diode,” actually a bipolar transistor, as described in [10] and shown in Figure 3-1. The second device (Figure 3-2) is a compound one which consists of a diode-connected PMOS in parallel with the intrinsic substrate bipolar transis-

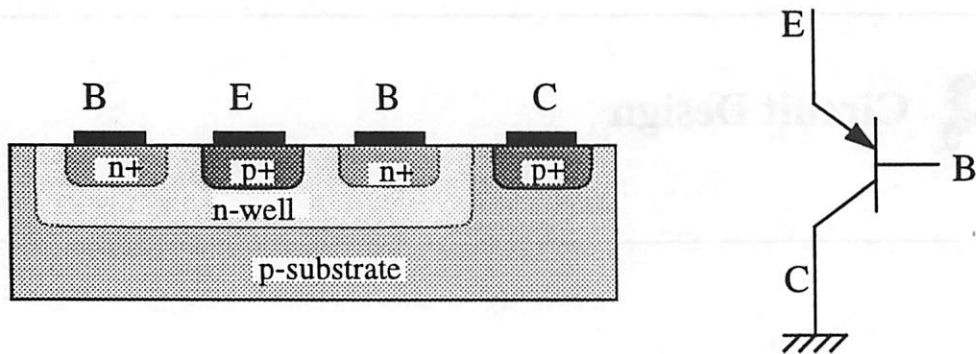


Figure 3-1. Substrate Bipolar Transistor

This is the substrate bipolar transistor provided by the n-well in schematic process (left) and electrical (right) form. The “floating diode” of interest is the E-B junction.

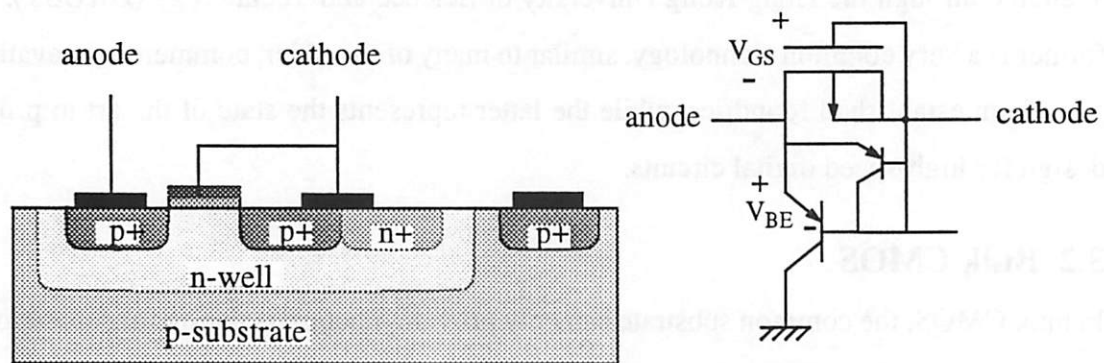


Figure 3-2. Compound PMOS and Bipolar Device

This device consists of the substrate bipolar transistor with the base-emitter junction shunted by a diode-connected PMOS. The PMOS actually functions as a bipolar in the subthreshold region of operation.

tor. This bipolar is comprised of the source, well, and substrate areas as emitter, base, and collector, respectively. Test circuits (Figure 3-3, Figure 3-3) consisting of two-stage Dickson charge pumps were fabricated using each device.

Table 3-1 summarizes the characteristics of the Microlab process, and the expected circuit performance is quantified and summarized in Chapter 4. Because of area constraints on the test chip, circuits were limited to two-stage charge pumps. Storage capacitors C were chosen to be nominally 2pF, and PMOS device sizes were chosen such that the parasitic

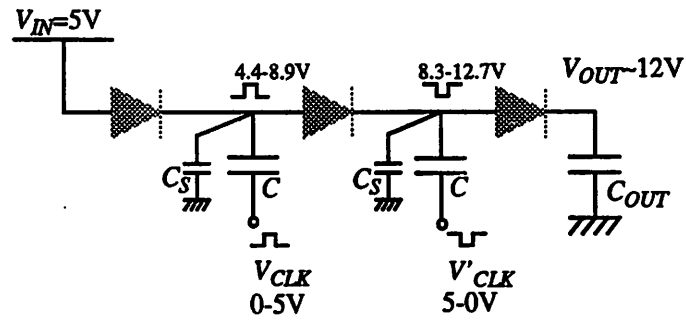


Figure 3-3. Electrical Schematic of Two-Stage Dickson Charge Pump Circuit

This test circuit is a Dickson voltage multiplier with two stages. The output voltage is given by Equation 2-5 with $N=2$.

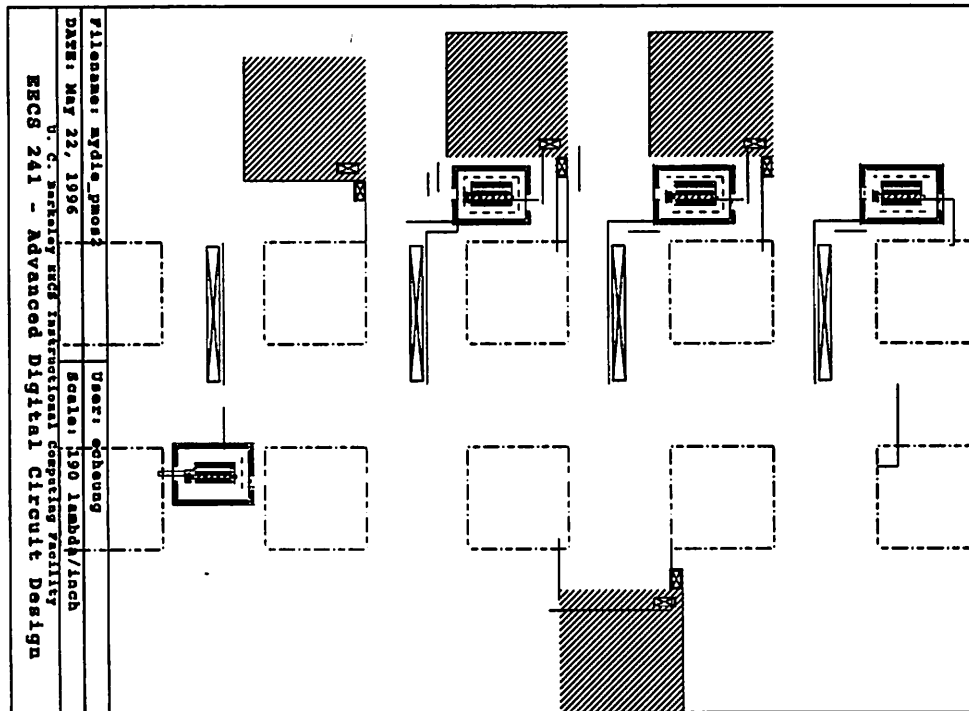


Figure 3-4. Layout of Two-Stage Charge Pump Circuit

The circuit layout for the test circuit, with PMOS/BJT device, as drawn in Magic.

Layer	Thickness	Impurity Concentration
p-type substrate		$1.3 \times 10^{15} \text{ cm}^{-3}$
n- well diffusion	$3.4\mu\text{m}$	10^{16} cm^{-3}
p-channel V_{th} diffusion	$0.2\mu\text{m}$	$1.3 \times 10^{16} \text{ cm}^{-3}$
p+ source/drain diffusion	$0.5\mu\text{m}$	10^{20} cm^{-3}
n-channel V_{th} diffusion	$0.5\mu\text{m}$	$14 \times 10^{16} \text{ cm}^{-3}$
n+ source/drain diffusion	$0.7\mu\text{m}$	$3 \times 10^{20} \text{ cm}^{-3}$
gate oxide	$0.03\mu\text{m}$	
poly1-substrate oxide	$0.65\text{-}0.7\mu\text{m}$	
poly2-poly1 oxide	$0.2\mu\text{m}$	

Table 3-1. Typical parameters for $2\mu\text{m}$ Microlab baseline CMOS process.

capacitance C_S was approximately 10-20% of C . This resulted in PMOSFETs with $W/L = 20\mu\text{m}/3\mu\text{m}$. The device length was chosen so that punchthrough would not be a factor at $V_{CLK}=5\text{V}$, which results in a maximum possible V_{DS} of 10V.

3.3. Silicon on Insulator

Silicon-on-insulator (SOI) CMOS has been a niche technology, as its fabrication cost is still considerably higher than that of bulk CMOS. The intrinsic device isolation is extremely beneficial in applications in which ultimate speed or radiation hardness are of importance; SOI is often an ideal alternative in these cases. However, in spite of its potentially simpler, and hence cheaper, fabrication process [11], SOI does not compete with bulk CMOS in most mainstream applications. Nonetheless, the natural oxide and air isolation afforded by the technology lends itself well to voltage conversion circuits.

Because all devices on SOI are isolated by air and/or oxide, floating diodes are naturally available, either in diode or MOSFET form. For these devices, the main consideration in SOI technology is device breakdown voltage, as opposed to device-substrate breakdown voltage. The diodes must handle twice the clock voltage, which may be a problem for MOSFETs with thin gate oxides and/or drain regions. Also, lateral diodes must have a low-doped intermediate region to handle any appreciable clock voltages. This low-doped region adds parasitic resistance and capacitance to the circuit, which can influence circuit behavior.

Charge pump circuits for $\pm 40\text{V}$ generation were fabricated in the Hong Kong University of Science and Technology, but were unavailable for testing.

4 Measurements and Analysis

4.1. Overview

The test circuit, comprising two stages, can only boost the input voltage by twice the clock voltage in the ideal case, and in practice will provide less than that. Therefore, for the application at hand, multiple identical stages will have to be cascaded in order to provide the necessary 80V level. There are questions of measurement concerning output voltage, output impedance, and the feasibility of cascading devices in the presence of the parasitic bipolar device.

This chapter gives an equivalent circuit for the charge pump, and explains quantitative circuit operation. The measurement methods are given. Expected results are calculated, and these are then compared to measured performance. The chapter concludes with an analysis of whether the stated goal of 80V can be achieved with this circuit in this technology.

4.2. Equivalent Circuit

A derivation of the Dickson voltage multiplier's (Figure 4-2) behavior is provided in [8]. In it, the circuit is found to be equivalent to a voltage source $\Delta V_{(unloaded)}$ (value given by Equation 4-3) relative to the input voltage, in series with an unknown variable output resistance R_{OUT} (typically in the $M\Omega$ range). There is an actual output capacitor C_{OUT} as well. R_{OUT} lowers the measured V_{OUT} when the output node is subject to a load current. The values of these equivalent parameters depend in turn on other, actual, circuit parameters, as discussed in "Equations" on page 17. The equivalent schematic of the circuit to be measured is shown in Figure 4-1.

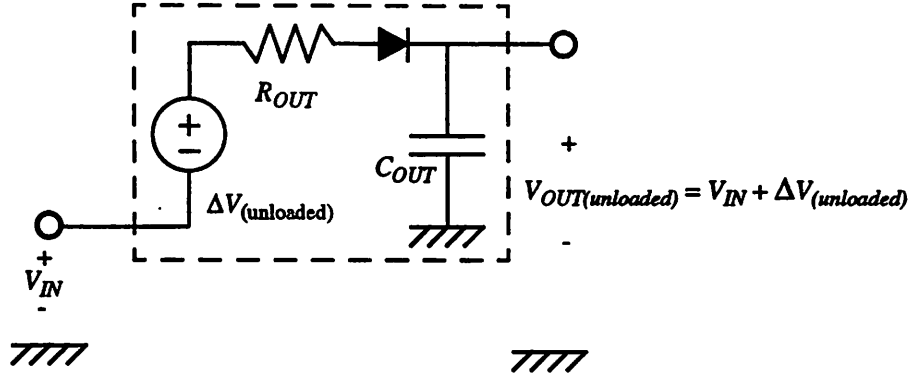


Figure 4-1. Equivalent schematic of circuit under test.

Because of the equivalent output impedances ($k\Omega$ to $G\Omega$) presented by the circuit, normally negligible input impedances of the test equipment, e.g. oscilloscopes and voltmeters, are significant, and will cause errors in measurement. Therefore these impedances have to be considered in measurement.

4.3. Equations

A two-stage Dickson charge pump (Figure 4-2) consists of $N=2$ stages, each consisting of

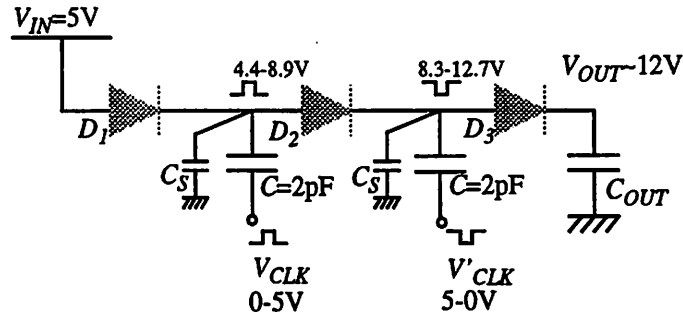


Figure 4-2. Schematic of two-stage Dickson charge pump.

a node capacitance ($C+C_S$) and a diode with diode turn-on voltage V_D . Each stage is fed a clock with amplitude V_{CLK} .

According to [8], the unloaded output voltage for the charge pump and its equivalent circuit (Figure 4-1) is

Equation 4-1. $V_{OUT(unloaded)} = V_{IN} - V_D + N \cdot [r \cdot V_{CLK} - V_D],$

where V_D is the diode turn-on voltage, N represents the number of stages, V_{CLK} is the clock swing, and

Equation 4-2.
$$r = \frac{C}{C + C_S}.$$

The output voltage in the presence of load current is

Equation 4-3.
$$V_{OUT(loaded)} = V_{IN} - V_D + N \cdot \left[r \cdot V_{CLK} - V_D - \frac{I_{OUT}}{(C + C_S)f_{CLK}} \right],$$

which, when compared to Equation 4-1, results in an equivalent output resistance

Equation 4-4.
$$R_{OUT} = \frac{N}{(C + C_S)f_{CLK}}.$$

From these equations, it appears that the voltage drop introduced by the R_{OUT} term is only evident when there is a load current I_{OUT} present at the output of the circuit. However, even with no external resistive load or current path at the output, the reverse leakage currents of the devices, from each stage to the preceding one, will constitute a loss. This must be compensated by charging of the node capacitance $(C + C_S)$ at the clock frequency f_{CLK} , and therefore will contribute to the I_{OUT} term in Equation 4-3.

In addition to reverse leakage across the blocking devices, there may be leakage to substrate. Unlike reverse leakage, which may be modelled as an output current with a linear effect on output voltage, substrate leakage has a compounding effect on output voltage: earlier stages must supply, while incurring a loss, the current which later stages lose. Therefore the voltage loss is nonlinear, and becomes worse as more stages are added.

4.4. Calculated Values

From Equation 4-1, diode turn-on voltage V_D and capacitive division ratio r are needed in order to predict $\Delta V_{(unloaded)}$ of the Dickson charge pump. These factors depend on process technology as well as circuit layout.

4.4.1. Bulk CMOS Voltage Multiplier

The diode turn-on voltage V_D is equal to $-V_{GS}=V_{BE}$ in this implementation (Figure 4-3). Its value depends on the level of current involved in charging and discharging the capacitors. Because of the presence of the parasitic substrate bipolar, proper operation requires that $V_{GS}<V_{BE(on)}$, or approximately 0.7V. Above this level, most current entering the source/emitter node (“anode”) is shunted to the substrate, and unavailable for charging the load, or subsequent stages. Hence this gives an upper bound for the value of V_D .

An expanded view of the device layout is shown in Figure 4-3, with calculated values for

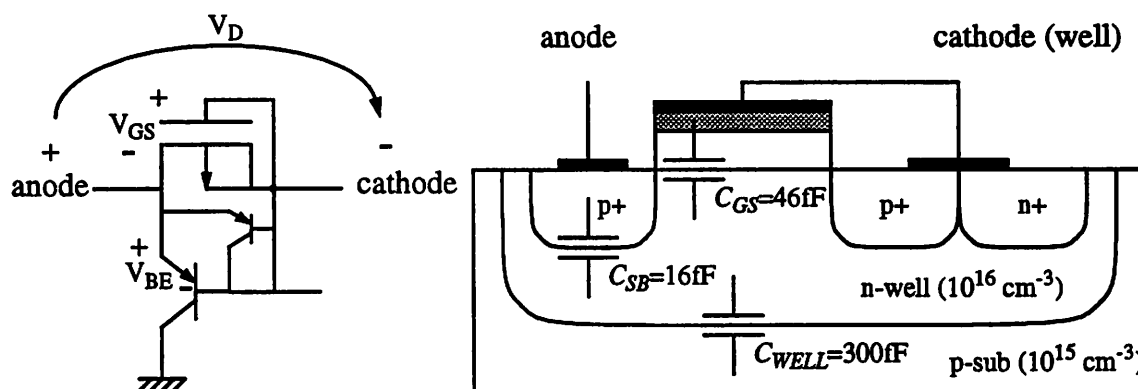


Figure 4-3. Schematic and parasitic capacitances of diode-connected PMOS in n-well.

the various capacitances under 5V reverse junction bias. The junction capacitances C_{WELL} and C_{SB} are calculated assuming abrupt junctions, so the actual values will be somewhat lower. The predicted parasitic capacitance contributed to C_S at each node is then equal to approximately 400fF for the worst case, and in practice should be less than that.

The coupling capacitors C (Figure 4-2) used in the circuit have bottom plates connected to the clock drivers, and top plates connected to the diodes. As such, coupling capacitor contribution to the total stray capacitance is minimal compared to device contribution.

Given these pessimistic values of $V_D=0.7V$ and $r=0.83$, the value of $\Delta V_{(unloaded)}$ predicted by Equation 4-1 is 6.2V.

Table 4-1. Calculated (pessimistic) circuit parameters.

V_D	r/C_S	$\Delta V_{(unloaded)}$	$\Delta V_{(ideal)}$
0.7V	0.83/0.4pF	6.2V	$2V_{CLK} = 10V$

4.5. Measurement Methods

4.5.1. Output Voltage and Output Resistance

The output resistance R_{OUT} given by Equation 4-4 is expected to be as high as $9G\Omega$ in the case of $f_{CLK}=100Hz$. Typical oscilloscope and multimeter input resistances of $10M\Omega$ are insufficient for direct measurement of output voltage $V_{OUT(unloaded)}$, since the current drawn into the $10M\Omega$ load through the $9G\Omega$ R_{OUT} would swamp out any output voltage present. The HP 4145B parameter analyzer, however, provides an input impedance of approximately $10^{12}\Omega$, which allows direct output voltage measurement even from these considerable output impedances. The circuit input and output current I_{IN} and I_{OUT} can also be swept through a range of values, which allows an assessment of the I-V characteristics of the circuit under loaded conditions.

The I-V method is illustrated in the schematic of Figure 4-4. Current source I_{OUT} is swept

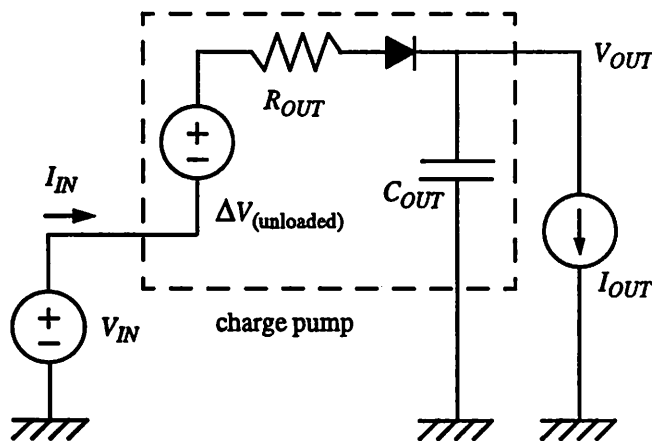


Figure 4-4. Measuring V_{OUT} vs. I_{OUT} with the HP 4145B.

through a range of values, and voltage source V_{IN} is stepped from 0V to 70V. V_{OUT} and I_{IN}

are measured. Because these are direct measurements, their accuracies depend directly on the resolution of the associated equipment. In the case of the HP 4145B, current resolution of 1pA is possible, and the voltage is accurate to 1mV.

4.5.2. Charge Pump Parameters

Once $\Delta V_{(unloaded)}$ has been measured, Equation 4-1 gives a relationship between the diode turn-on voltage V_D and capacitive division ratio r . Measuring different values of $\Delta V_{(unloaded)}$ by using different values of V_{CLK} should allow calculation of V_D and r .

4.6. Measured Values

The fabricated circuit and test device were measured on a Wentworth probe station.

4.6.1. Unloaded Output Voltage, Bulk CMOS

Unloaded output voltage vs. clock frequency is plotted in Figure 4-5, where $V_{CLK}=5V$. The visibly lowered V_{OUT} below around $f_{CLK}=10kHz$ are a result of leakage current into increasing values of R_{OUT} . The lines connect points calculated from Equation 4-3 based on a reverse leakage of 2nA, which matches well with both measured voltage V_{OUT} as well as measured device leakage. Therefore the individual device reverse leakage corresponds well to circuit leakage.

4.6.2. Loaded Output Voltage, Bulk CMOS

When the output is resistively loaded, the current draw results in a lowered V_{OUT} as compared to the unloaded case, due to the significant output impedance presented by the circuit. Loaded voltage gain ($V_{OUT} - V_{IN}$) with different values of input voltage V_{IN} is shown in Figure 4-6. In the range of input voltages shown (0-70V), there is very little difference in the output voltage referenced to the input voltage. In fact, output voltage $V_{OUT} - V_{IN}$

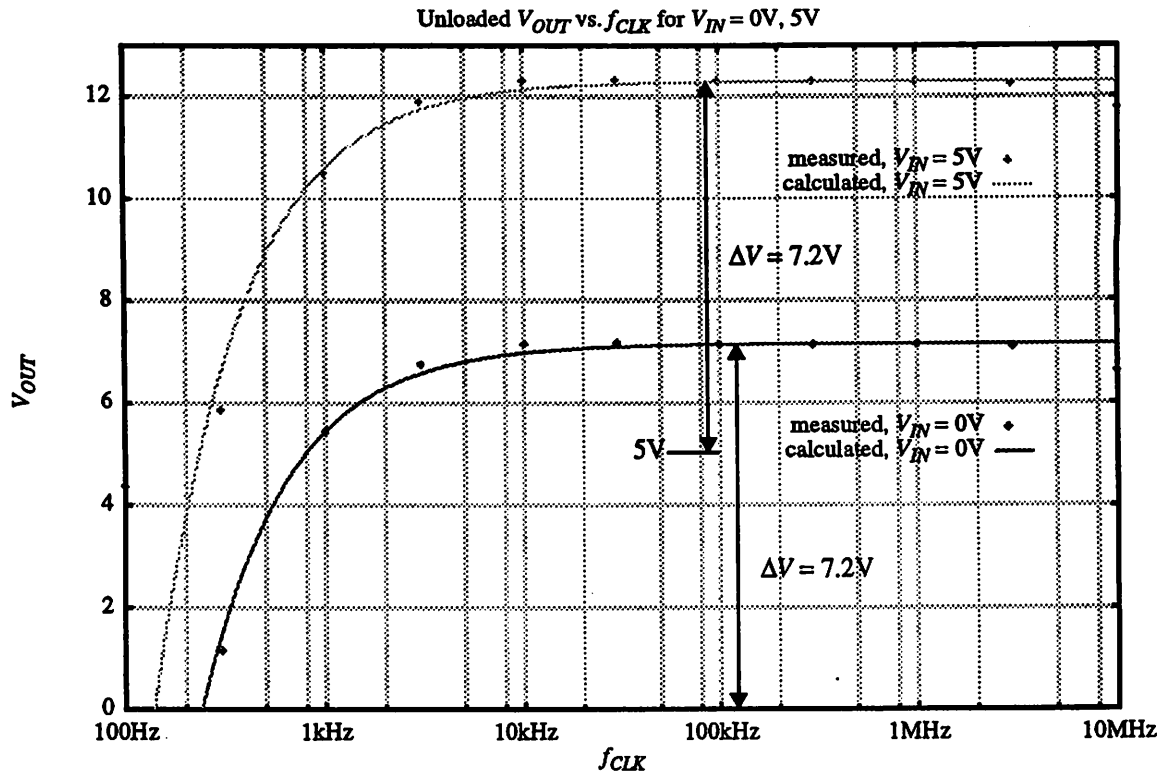


Figure 4-5. Unloaded V_{OUT} vs. f_{CLK} for Dickson voltage multiplier in bulk CMOS

$V_{CLK} \approx 5V$, $V_{IN} \approx 0V, 5V$. Points are measured data; lines are calculated based on device leakage of 2nA.

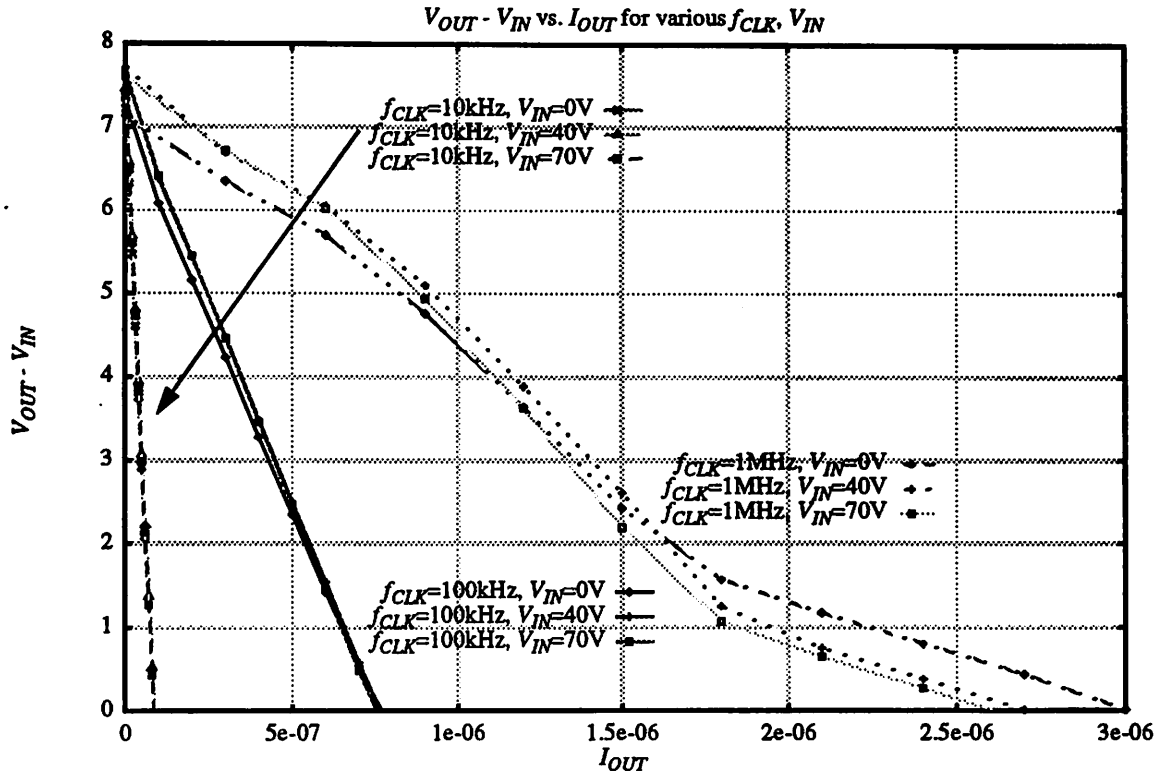


Figure 4-6. Measured output voltage $V_{OUT} - V_{IN}$ vs. I_{OUT}

$V_{OUT} - V_{IN}$ vs. I_{OUT} for $V_{IN}=0V, 40V, 70V$, and $f_{CLK}=10kHz, 100kHz, 1MHz$.

actually increases slightly with increasing V_{IN} , due to decreased parasitic depletion capacitances at higher voltages. Measured vs. calculated values of R_{OUT} are given in Table 4-2.

Table 4-2. Calculated and measured output impedance

f_{CLK}	10kHz	100kHz	1MHz
calculated R_{OUT}	85M Ω	8.5M Ω	0.85M Ω
measured R_{OUT}	85M Ω	9.7M Ω	2.4M Ω

As can be seen, measured output impedance deviates from calculated values more as f_{CLK} increases, due to the higher current levels involved, which will be discussed later.

4.6.3. Extracted Charge Pump Parameters

Since Equation 4-1 with $N=2$ gives the unloaded output voltage for this circuit, there are still two unknowns, capacitive ratio r and diode turn-on voltage V_D . These can be calculated for the actual circuit by using two values for V_{CLK} , which will result in two equations

for the two unknown variables. With $V_{OUT(unloaded)}=7.2V$ for $V_{CLK}=5V$, and $V_{OUT(unloaded)}=8.9$ for $V_{CLK}=6V$, the calculated values are $V_D=0.4V$ and $r=0.85$. The value of r results in an extracted parasitic capacitance $C_S=0.35pF$. These parameters are summarized in Table 4-3.

Table 4-3. Calculated and measured circuit parameters.

parameter	V_D	r/C_S	$V_{OUT(unloaded)}$
calculated value	0.7V	0.83/0.4pF	6.2V
measured value	0.4V	0.85/0.35pF	7.2V

4.6.4. Substrate Current Leakage

Current leakage to the substrate can be accounted for by the measurement of I_{IN} for given I_{OUT} and V_{OUT} . I_{IN} vs. I_{OUT} is shown in Figure 4-7. The worst-case leakage occurs for an

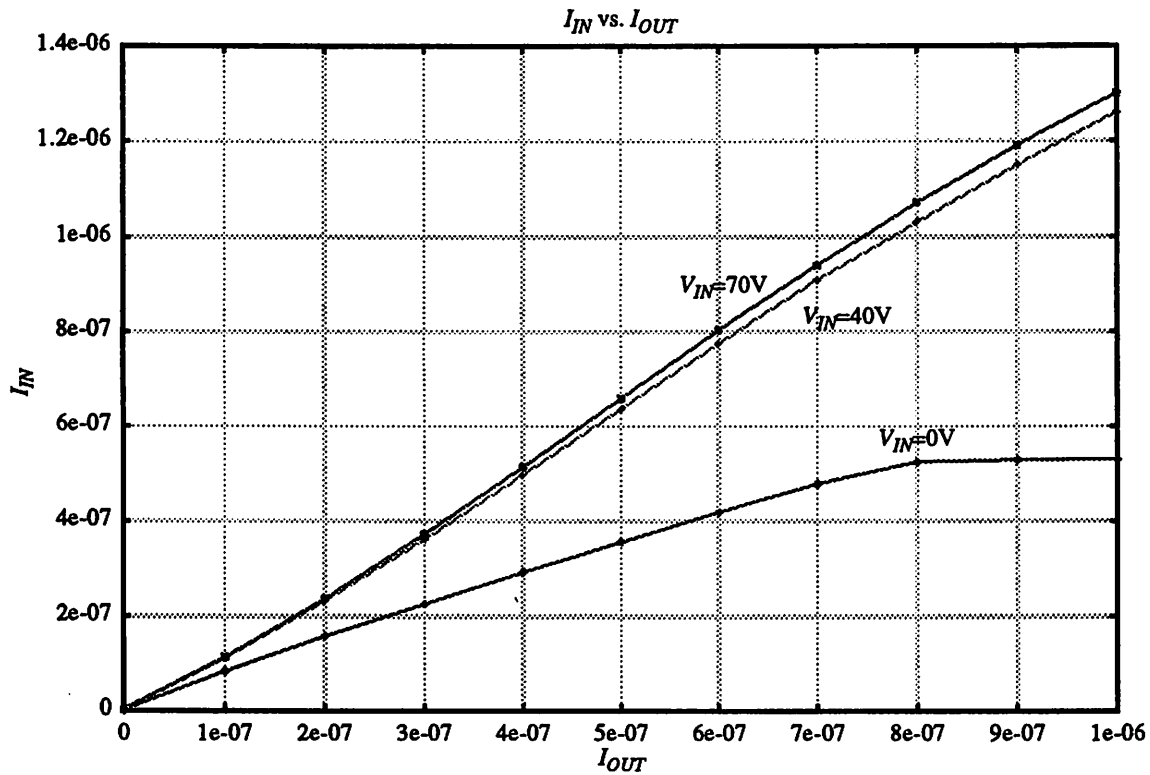


Figure 4-7. I_{IN} vs. I_{OUT} for different values of V_{IN} .

input voltage $V_{IN}=70V$, which can be bounded by the expression

Equation 4-5.

$$I_{IN} = 1.35I_{OUT} + 2nA.$$

Leakage is at a maximum at this highest input voltage because of the Early effect present in the parasitic substrate bipolar transistors, which causes collector (i.e., substrate) current to increase with increasing magnitudes of V_{CE} .

4.7. Analysis of Results

The primary question is whether, given the substantial substrate leakage, the goals of 80V output and 25kHz bandwidth can be achieved with the chosen circuit and blocking device in the chosen bulk CMOS technology. As mentioned previously in Section 4.3. on page 17, each stage must supply the current lost by all the following stages, which causes a voltage drop within each stage, as described by the expression for $V_{OUT(loaded)}$ in Equation 4-3. Combining with Equation 4-5, this gives a geometric series expression for the final $\Sigma V_{OUT(unloaded)}$,

$$\text{Equation 4-6. } \Sigma V_{OUT(unloaded)} = N \cdot V_{OUT(unloaded)} - 2nA \cdot R_{OUT} \left(\frac{1.35^{N+1} - 1.35}{0.35^2} - \frac{N}{0.35} \right),$$

with N =number of stages, and R_{OUT} given by Equation 4-2. Figure 4-8 shows the extrapolated $\Sigma V_{OUT(unloaded)}$ as a function of number of stages N for f_{CLK} =100kHz. As can be seen, cascading 24 stages results in $\Sigma V_{OUT(unloaded)}$ =79V, just under the stated goal. This result is actually somewhat pessimistic, since the analysis includes the third, rectifying, diode (D_3 in Figure 4-2) in the two-stage charge pump. That is, the cascaded charge pump does not require the filtering diode to be present in every third stage, since it simply serves to filter the voltage ripple at the output. The diode drop has a measured value of 0.4V, as listed in Table 4-3. Over 12 two-stage circuits (N =24), the presence of the diode after every two stages represents a loss of 4.4V in achievable output voltage $\Sigma V_{OUT(unloaded)}$.

There is a voltage penalty to pay for the presence of substrate leakage current, since the unloaded two-stage voltage $V_{OUT(unloaded)}$ was measured to be 7.2V. The ideal (no leakage) $\Sigma V_{OUT(unloaded)}$ for 12 two-stage circuits is then 86.4V, compared to the extrapolated 79V when leakage is considered. In cascading 12 two-stage circuits, then, there is a net loss of 7.4V, or just over the contribution of two stages.

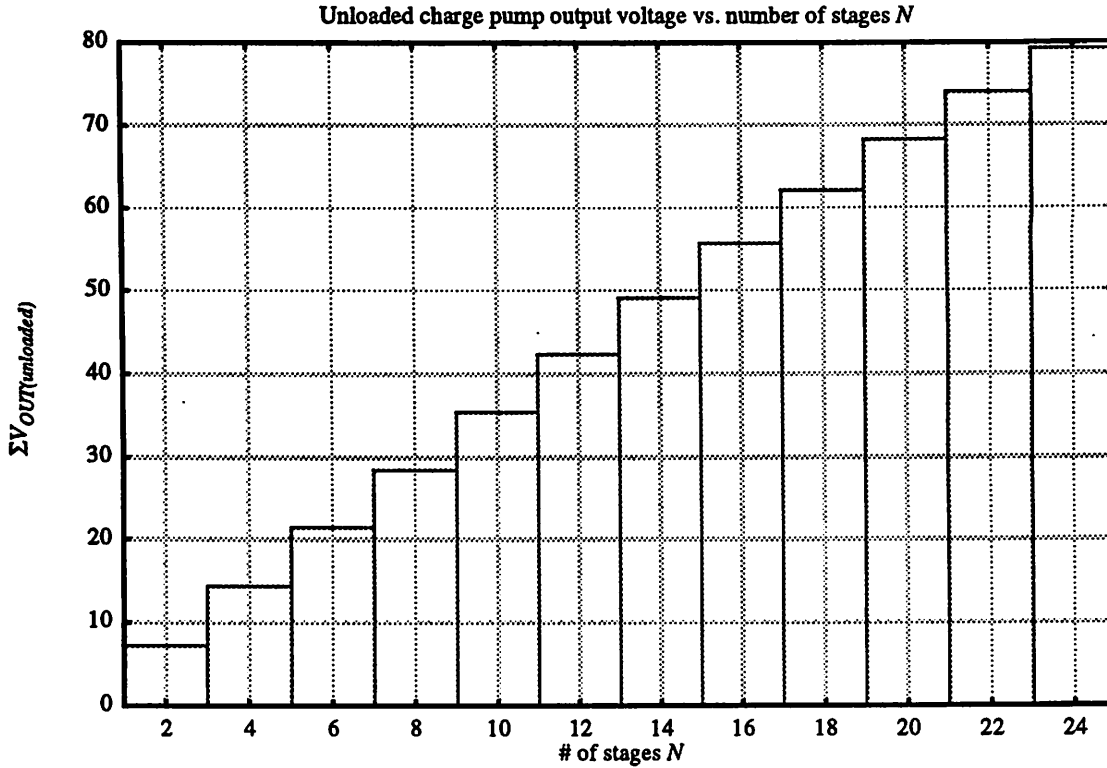


Figure 4-8. Extrapolated charge pump output voltage vs. number of stages N .

Current leakage also presents a penalty in terms of current drive and output impedance. Output current is lessened directly by the amount of leakage, and so output impedance is increased proportionally. This effect can be seen in Figure 4-6, where, for $f_{CLK}=1\text{MHz}$, the output impedance becomes much less linear than for the cases $f_{CLK}=10\text{kHz}, 100\text{kHz}$. This nonlinearity is a manifestation of the current leakage effects into higher current levels. In Table 4-2, the measured output impedance R_{OUT} of the $f_{CLK}=1\text{MHz}$ can be seen to be much greater than the calculated value. For the application, a total (for the 80V charge pump) R_{OUT} of approximately $1\text{M}\Omega$ is required, which translates into a two-stage (assuming 24 stages total) $R_{OUT}=40\text{k}\Omega$. So the circuit as designed does not meet the bandwidth requirements, and current leakage makes measured performance poorer.

In all, the substrate current leakage in the bulk CMOS technology used results in lowered current drive, lowered output voltage, and increased output impedance, which may be

compensated for with increased circuit area. Larger devices and capacitors would allow higher current levels in the presence of leakage.

5 Future Work

5.1. Overview

This research presents a method of generating a fixed high voltage from a lower-voltage rail. Practical systems, however, will require some form of modulation of the high-voltage signal. Also, in present bulk CMOS form, the circuit sinks substantial current into the substrate when providing unloaded ($I_{OUT}=0$) output voltage, and will sink more for finite output currents. The increased current loss will result in lowered output voltage, and hence an apparent increase in output resistance into higher current loads. This section will attempt to provide some ideas for solving these problems.

5.2. Modulation Schemes

With a fixed clock voltage V_{CLK} applied, the charge pump provides a fixed voltage V_{OUT} with a finite output impedance R_{OUT} . In order to be useful for driving loads such as the electrostatic motor, however, the output must be controllable by some external signal. Given a finite load resistance, the output voltage could be varied either by changing the output resistance R_{OUT} , e.g., by varying f_{CLK} , or by changing the load resistance.

The load resistance might be changed by turning on a high-voltage device attached to the output, as shown in Figure 5-1. Suitable high-voltage devices are presented in [12, 13, 14]. These devices, with maximum V_{DS} approaching the well-substrate breakdown voltage, can be transparently fabricated in conventional bulk CMOS processes, similar to the Microlab one used.

Alternatively, the output resistance R_{OUT} could be modulated by changing the supplied f_{CLK} , or by turning a single-frequency clock signal on and off.

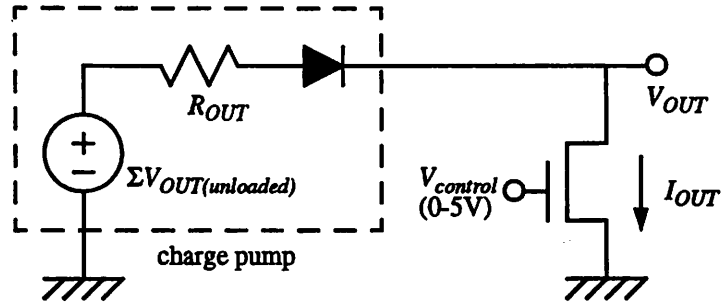


Figure 5-1. Output voltage modulation using high-voltage bulk CMOS.

A more complex modulation circuit is presented in [15]. Shown in Figure 5-2, it consists

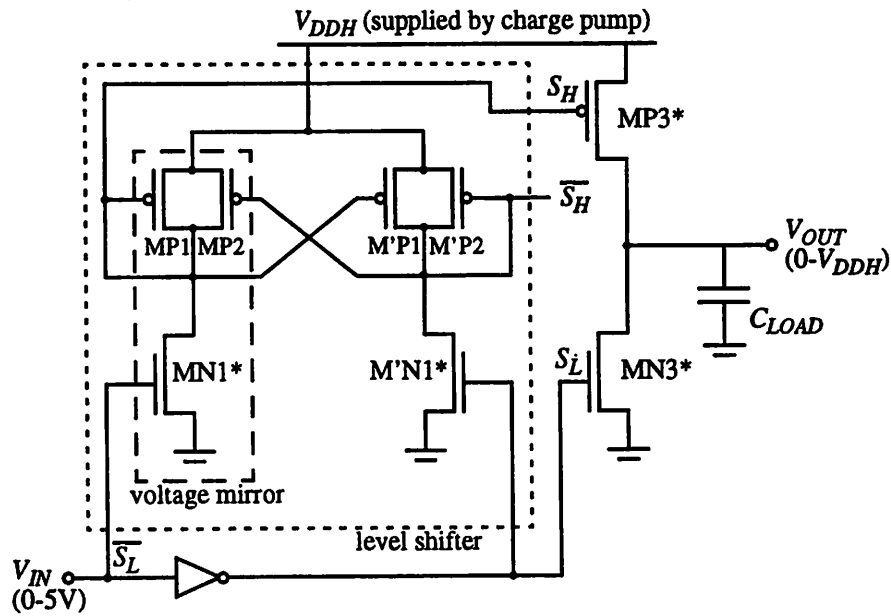


Figure 5-2. HVCMOS modulation circuit as presented in [15].

Asterisks (*) denote specially laid out high-voltage devices.

of a level shifter which provides the correct low-voltage swing (0 to 5V for NMOS, V_{DDH} to $V_{DDH}-5V$ for PMOS) at the gates of the high-voltage devices. Signal S_H swings down from V_{DDH} , and S_L swings up from ground. These complementary, but level-shifted, signals provide individual turn-on for the high-voltage PMOS and NMOS devices, respectively. Thus this circuit provides current drive, through MP3 or MN3, either to the high-

voltage supply V_{DDH} or to GND, while being controlled by a low-voltage (0-5V) signal V_{IN} .

5.3. Higher Efficiency

In the bulk CMOS charge pump circuit, as discussed in Chapter 4, the substrate bipolar sinks a substantial amount of current which serves only to lower the available output voltage. Worse yet, the effect compounds geometrically. The reason the bipolar is active is that the diode-connected PMOSFET has a body, the n-well, which is connected to the FET's gate and drain node. This connection can be avoided, along with the parasitic bipolar operation, if the n-well is instead connected to a higher potential. In longer cascades of stages, such voltages are available from subsequent higher-voltage stages. In this case the bipolar action would no longer be an issue, except for the ultimate and penultimate devices. There would be no compounding of current loss, which would be a net gain. This solution, however, requires the source/drain-to-well junctions to withstand reverse voltages of 4 times the per-stage gain, which may be a problem. Also, start-up conditions may be a problem, as forward-biased junctions may prevent desired circuit operation.

One negative aspect to the solution presented above is the fact that, since V_{SB} is now non-zero and negative, the body effect will raise the PMOS threshold voltage, which will subtract directly from the per-stage voltage gain. This effect in turn may be mitigated by a solution analogous to the one presented in [16], in which voltage loss (in an NMOS charge pump) due to body effect is compensated by connecting gates to higher voltages in the chain.

6 Conclusion

The application requires that 80V be generated from a 5V supply rail. The work presented has shown that it should be possible to achieve 80V from a charge pump circuit powered by 5V clocks within a standard bulk CMOS process. The design as shown has drawbacks in terms of current drive capability because of parasitic device leakage, but the voltage level required should be feasible. There are solutions in terms of circuit area and device layout which will ameliorate the problem somewhat, but they bring some drawbacks as well, which in turn may be dealt with. Another possibility is the use of silicon-on-insulator technology, which would eliminate many of the problems encountered.

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