THE DESIGN AND IMPLEMENTATION OF A SEMI-CUSTOM TRANSMITTER FOR A CDMA DIRECT SEQUENCE SPREAD-SPECTRUM TRANSCEIVER

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Abstract

High-performance wireless communications systems allow access to real-time data located on a high-speed network using portable, low-power terminals. For a pico-cellular network, a basestation within each cell serves as the interface between the backbone network and the various mobile units. A CDMA direct sequence spread-spectrum transmitter is presented which allows the basestation to provide a 1Mbps downlink to each of 15 portable multimedia terminals within the cell. The total transmit bandwidth is 41.6MHz centered at a carrier frequency of 1.056GHz. This design can be easily scaled to support up to 50 users within a single cell.

Acknowledgements

As with any endeavor, this research project could not have been completed without the help and support of others. Foremost, I wish to thank my research advisor Professor Robert Brodersen. Your guidance throughout the course of this project is greatly appreciated. I would also like to thank Professor Paul Gray for reviewing this thesis and providing helpful comments.

I am greatly indebted to Sam Sheng for his friendship and his selflessness in teaching me everthing I know about RF design. The success of this project would not have been possible without your guidance. Thanks Sam!

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Finally, I would like to thank my family and friends for their support and encouragement. I am very lucky to have wonderful friends like Richard, Bryant, Albert and Ben.

Yvette, you have made the last six years the richest and most fulfilling of my life. Thanks for your patience and understanding during the many evenings and weekends required for the completion of this project.

Dave, you are always there for me, even when you are over 800 miles away. Thanks big bro!

Mom and Dad, your continual love and encouragment have been a source of strength for the past 24 years. I dedicate this work to you with all my love.

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1 Introduction

Society's increasing demands for ubiquitous access to information have stimulated extensive research in the area of high-speed wireless digital communications systems. The InfoPad research project [Sheng92] proposes a solution which allows access to real-time multimedia data on a high-speed network using portable, low-power terminals. A basestation provides the communications interface between the backbone network and the multimedia terminals. In order to provide high-quality, full-motion video to each of the several multimedia terminals, the downlink must provide data rates of up to 2Mbps for each user in the system.

[Sheng96] describes the system-level architecture of a CDMA direct sequence spread-spectrum transceiver which is capable of supporting up to 50 users each with a 2Mbps maximum data rate. The receiver must be low-power and compact since it resides in the portable, battery-operated terminal. In order to achieve these objectives, monolithic integration of the receiver is imperative. These constraints, however, do not apply to the transmitter since it resides in the basestation, and thus, a semi-custom solution is adequate.

This report describes in detail the design and implementation of the CDMA direct sequence spread-spectrum transmitter. The report is organized into six chapters and one appendix. This chapter motivates the work presented in this report and provides an overview of the content. Chapter 2 provides a brief overview of the system-level architecture of the CDMA direct sequence spread-spectrum transmitter. This chapter reviews the architecture of the baseband modulator [Peroulas95] and discusses issues associated with digital-to-analog conversion. Chapter 3 focuses on different methods of single-sideband upconversion and concludes with a discussion of the trade-offs between the various architectures. Chapter 4 presents the final transmitter design and provides a

detailed description of the implementation procedure, including schematic entry, design simulation, and printed circuit board layout. A detailed listing of all relevant design files and directories is tabulated in Appendix A. Chapter 5 concentrates on testing and measurements. Measured results are compared with simulated results in order to evaluate the performance of the transmitter testboard. Power and speed measurements are also presented in this chapter. The chapter concludes with a discussion of the errors discovered in the baseband modulator chip as well as the transmitter testboard. A complete description of all inputs and outputs on the transmitter testboard is tabulated in Appendix A. Finally, concluding comments as well as a discussion of future directions are presented in Chapter 6.

2 Transmitter Architecture

The CDMA transmitter must support an aggregate data rate of 100Mbits/s over a wireless link. Consequently, the design of such a system is a nontrivial task. This chapter provides a brief overview of the transmitter architecture and discusses some of the implementation details of the baseband modulator. [Sheng96] provides more detailed discussions of the overall system architecture, whereas [Peroulas95] describes in detail the baseband modulator chip which performs the baseband digital processing and pulse-shaping.

2.1. Transmitter System-Level Overview

The transmitter architecture is depicted in Figure 2-1. The first major block is the baseband modulator chip which processes the digital data from 15 different users. Multiple chips may be used in parallel to meet the 50 user specification. The data converter block converts the digital output of the baseband modulator to an analog signal and the single-sideband modulator block mixes the IF signal to an RF of 1.088GHz. The design and implementation of the single-sideband upconverter is discussed in detail in the next chapter.

2.1.1. Baseband Modulator

The following functions are performed in the baseband modulator:

- differential quadrature-phase shift keying (DQPSK) encoding
- Walsh encoding
- pseudo-random number (PN) scrambling
- power control
- raised-cosine filtering
- IF modulation.

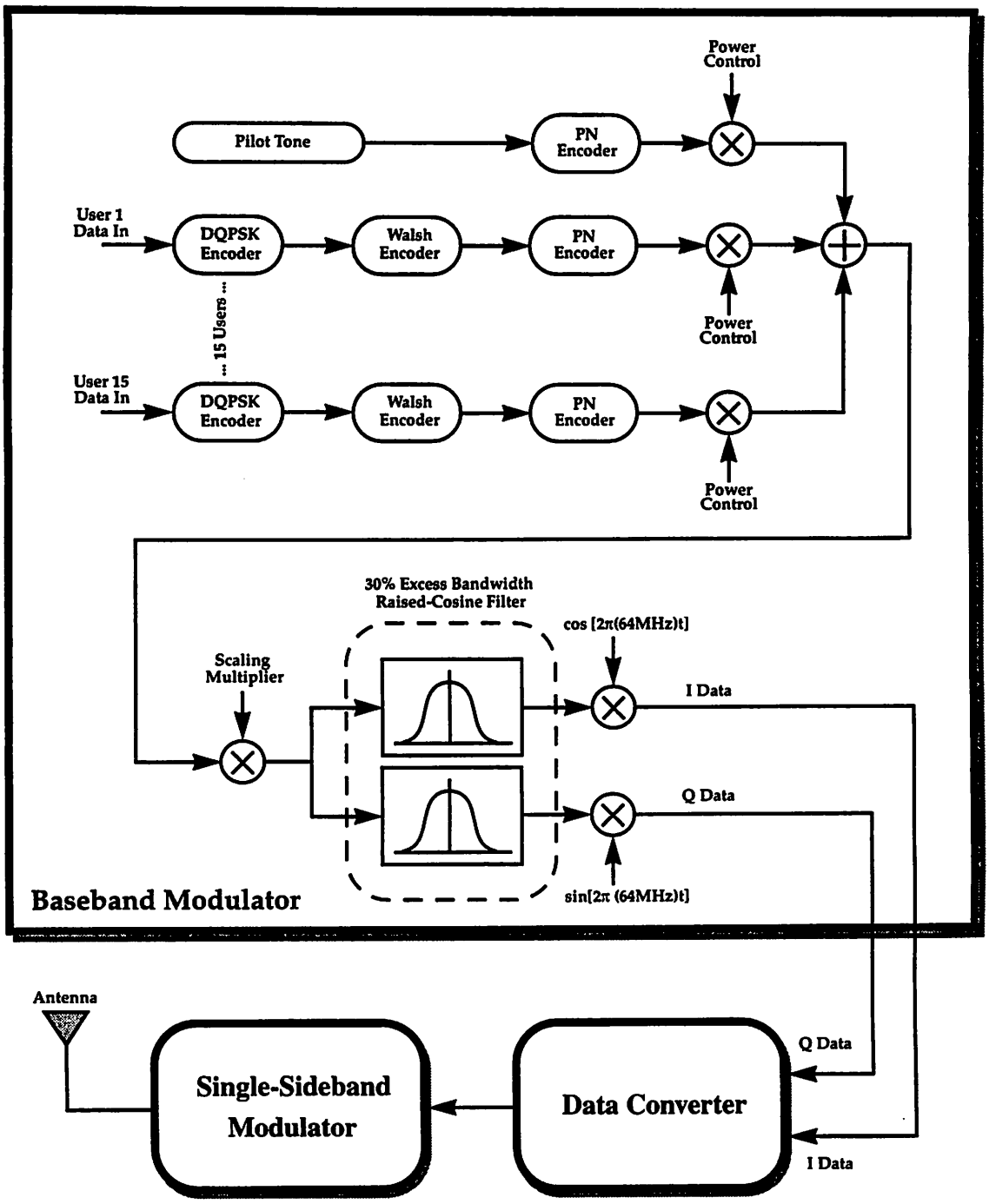


Figure 2-1. System Level Architecture of CDMA Transmitter

2.1.1.1. DQPSK Encoding

In phase shift keying (PSK) modulation techniques, the information is encoded into the phase of the carrier while the amplitude remains fixed. In QPSK, the signal constellation

consists of four symbols as depicted in Figure 2-2. The phase values of symbols A_0, A_1,

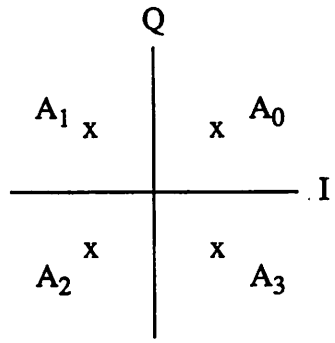


Figure 2-2. QPSK Symbol Constellation

A_2, and A_3 are $\pi/4$, $3\pi/4$, $5\pi/4$, and $7\pi/4$, respectively, while the magnitudes of all symbols are equal. The use of absolute position in PSK encoding schemes may result in incorrect decoding at the receiver due to constellation rotation, e.g., a rotation of $\pi/2$ in a QPSK signal constellation. Constellation rotation may be caused by rapid phase fluctuations in the channel due to multipath fading as well as frequency offsets between oscillators in the transmitter and the receiver in the absence of carrier recovery.

This problem may be avoided by using a differential encoding scheme for the phase information. In DPSK the symbols may be represented by the equation

$$A_m = ke^{j\phi_m}$$

where k is a constant and ϕ_m is determined by

$$\phi_m = \phi_{m-1} + \Delta_m$$

In this system, DQPSK data modulation is used and Δ_m is determined from the input bits based on Table 2-1. The input data of each user is presented to the baseband modulator

Table 2-1. DQPSK Encoding of Input Data

MSB	LSB	Δ_m
0	0	0
0	1	$\pi/2$
1	0	$3\pi/2$
1	1	π

chip two bits at a time each at a 1MHz rate. Table 2-2 summarizes the transmitted symbols if the following bit pairs, (MSB,LSB), are input to the baseband modulator chip: (0,0), (1,1), (1,0), (1,0), (0,0), (0,1), (1,0). It is assumed that $\phi_m=0$ for $m<0$.

Table 2-2. Example of Transmitted Symbols

m	(MSB,LSB)	Δ_m	ϕ_m
0	(0,0)	0	0
1	(1,1)	π	π
2	(1,0)	$3\pi/2$	$\pi/2$
3	(1,0)	$3\pi/2$	0
4	(1,1)	π	π
5	(0,1)	$\pi/2$	$3\pi/2$
6	(1,0)	$3\pi/2$	π

Finally, the values of ϕ_m need to be encoded digitally. Two bits are required to represent the four values of ϕ_m. Table 2-3 summarizes the digital representation of ϕ_m. A and B are

Table 2-3. Digital Representation of ϕ_m

ϕ_m	(A,B)
0	(0,0)
$\pi/2$	(1,0)
π	(1,1)
$3\pi/2$	(0,1)

called the in-phase and quadrature-phase components, respectively.

2.1.1.2. Walsh Encoding and PN Scrambling

Code-division multiple access (CDMA) is one of several multiple access schemes which may be used to accommodate 50 users. CDMA systems allow multiple users to

simultaneously share the same frequency channel. In a CDMA system each user's data is encoded with a unique user sequence. These user sequences should be mutually orthogonal as well as spectrally white. Typical CDMA systems employ pseudorandom sequences, which operate at a rate much higher than the symbol rate, for data encoding. Thus, modulation by these pseudorandom sequences results in a transmission bandwidth which is much greater than the bandwidth dictated by the symbol rate. The spread-spectrum nature of CDMA results in increased immunity to frequency-selective multipath fading as well as jamming.

Although pseudorandom sequences with good autocorrelation properties may be easily generated, such sequences usually exhibit poor cross-correlation which is necessary in order to distinguish between different users in a CDMA system. One strategy is to first encode each user's data with a user-specific code which is guaranteed to be orthogonal but not necessarily spectrally white. A common pseudorandom sequence is then applied for spectral whitening. One set of orthogonal codes is called the Walsh codes. These codes have a cross-correlation equal to zero and an autocorrelation equal to the length of the Walsh codes. The Walsh sequences in this system are length 64 and clocked at a 64MHz rate. Each user is assigned a unique Walsh sequence which is used to encode both in-phase and quadrature-phase data, both of which are clocked at 1MHz. Walsh code zero, which is simply a DC signal, is reserved for the pilot tone. The pilot tone is used for various functions such as clock recovery and channel estimation.

Finally, although the 1MHz data signal is spectrally spread to a bandwidth of 64MHz, the resulting signal is not pseudorandom. Many advantages of spread-spectrum communications are direct consequences of the pseudorandom nature of the transmitted signal. Thus, Walsh coding must be followed by PN scrambling. The same 64MHz pseudorandom sequence of length 32768 is used to encode the in-phase and quadrature-phase data of all users. Since the same pseudorandom sequence is used for all users, it may seem more efficient to implement the PN scrambling after the data of all users are combined. Since the combiner employs a two's complement number representation, such an implementation of the PN scrambling after the combiner would also require the use of a two's complement number representation. Multiplication with the pseudorandom

sequence, which consists of the values +1 and -1, may be performed much more efficiently by using a sign and magnitude number representation since multiplication by -1 simply requires toggling the sign bit. In contrast, multiplication by -1 in a two's complement number representation requires forming the bitwise complement and then adding one. The increased switching activity associated with negation of a two's complement number results in greater power consumption [Chandrakasan94]. Thus, PN scrambling is performed on the in-phase and quadrature-phase data of all users before the combiner.

2.1.1.3. Power Control

If the basestation transmits the data of all users at the same power level, then receivers which are near the basestation receive a much stronger signal than those which are further away. Power control allows all users to receive the same signal strength by controlling the power level of each user at the basestation. For example, data associated with receivers which are closer to the basestation are transmitted with a lower power level than those associated with receivers which are further away.

Six bits of power control are available for each user as well as for the pilot tone. Both in-phase and quadrature-phase data from the PN scrambler are multiplied by the power control value. The data from all 15 users and the pilot tone are then combined into two 10-bit data streams: one for in-phase data and one for quadrature-phase data. The combiner is followed by a multiplier which is used to scale the output signal. The 4-bit scaling factor guarantees full-scale inputs to the raised-cosine filters.

2.1.1.4. Raised-Cosine Filtering

A raised-cosine filter is used to avoid intersymbol interference. The raised-cosine pulse is given by

$$x(t) = \frac{\sin\left(\frac{\pi t}{T}\right)}{\frac{\pi t}{T}} \times \frac{\cos\left(\frac{\alpha \pi t}{T}\right)}{1-\left(\frac{2\alpha t}{T}\right)^2}$$

where α is called the rolloff parameter and T is the symbol period. For α=0, x(t) degenerates to a sinc pulse which has a bandwidth of f=1/T. As α varies from 0 to 1, the excess bandwidth varies from 0% to 100%. Although the tails of the pulses are infinite in extent for all values of α, as α increases, the magnitude of the tails becomes increasingly small. Thus, raised-cosine filters may be approximated as FIR filters by truncation of the sequence.

Two identical raised-cosine filters with 30% excess bandwidth are used in this transceiver system: one for the in-phase data and one for the quadrature-phase data. The number of filter taps, tap coefficient quantization as well as internal roundoff noise are optimized to meet a 40dB out-of-band rejection specification. The resulting filters each have 37 taps, all of which are quantized to three bits. Implementation details for these filters may be found in [Peroulas95].

In order to implement the raised-cosine filter with 30% excess bandwidth, an oversampling ratio of at least two is required. A large oversampling ratio is desirable since the rolloff requirement of the subsequent lowpass filter is less stringent. In addition, a large oversampling ratio minimizes the droop distortion introduced by the subsequent digital-to-analog converter, and thus eliminates the need for a droop compensation filter. However, a large oversampling ratio also results in clock rates which may be excessively high to be practically implemented using current process technology. An oversampling ratio of four is used in this transceiver system, resulting in an effective filter output data rate of 256MHz.

A direct implementation of the 256MHz FIR filters results in the filter structures depicted in Figure 2-3, where a_0-a_{36} are the 37 tap coefficients. The calculation along the critical path of one multiplier and 36 adders must be accomplished under 4ns, which is impossible using current process technology. A practical realization must take advantage of parallelism as well as pipelining [Samueli90]. Parallelization of the filter structure is a direct consequence of oversampling the input data. Upsampling by four is achieved by inserting three zeros between every input sample. Thus, if the inputs to the shaded delay elements in Figure 2-3 have non-zero values, then the inputs to the non-shaded delay

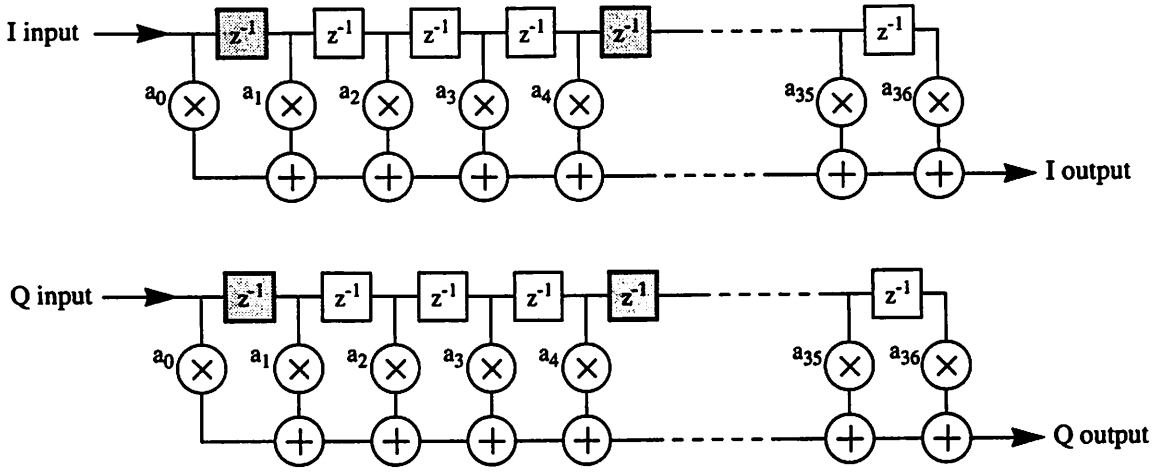


Figure 2-3. Direct Implementation of 256MHz 37-Tap Raised-Cosine Filter

elements are identically equal to zero. Multiplication by zero is trivial and does not need to be computed. The implication is that the 256MHz FIR filter may be divided into four parallel 64MHz subfilters as depicted in Figure 2-4. Since the in-phase and quadrature-

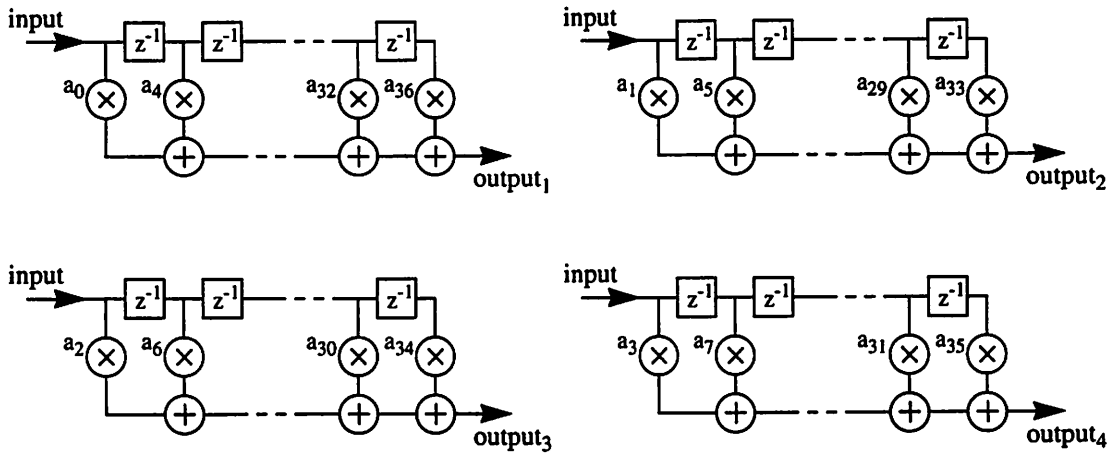


Figure 2-4. Implementation of 256Mhz Raised-Cosine Filter using Four Parallel 64MHz Subfilters

phase filters are identical, only one set of four subfilters is depicted. The output of the four subfilters may be interleaved using a multiplexer to generate the desired 256MHz output stream. The output of each subfilter consists of ten bits, which is determined by the capability of current digital-to-analog converters. Current high performance ECL

compatible digital-to-analog converters which operate in excess of 200MHz are limited to a maximum of ten input bits.

The critical path delay for the four subfilters is still greater than 4ns. For the first subfilter, the critical path consists of one multiplier and nine adders, and for the other three subfilters, the critical path consists of one multiplier and eight adders. A practical realization of the four subfilters must take advantage of pipelining. An example of a pipelined implementation of an FIR filter is illustrated in Figure 2-5. The critical path is now reduced

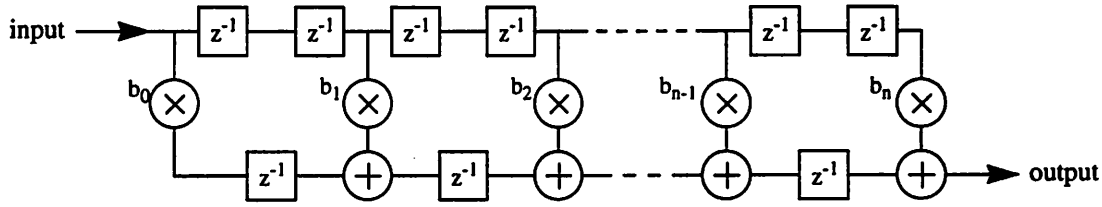


Figure 2-5. Pipelined Implementation of FIR Filter

to one multiplier and one adder at the expense of increased latency. Also since the tap coefficients are fixed, a general purpose multiplier is not required. Instead each multiplier may be replaced by a series of fixed shifts.

Additional hardware simplifications may be achieved by observing the truncated raised-cosine time-domain response. The assignment of the tap coefficients to the four subfilters is indicated in Figure 2-6. The third subfilter may be simplified to a simple delay since all

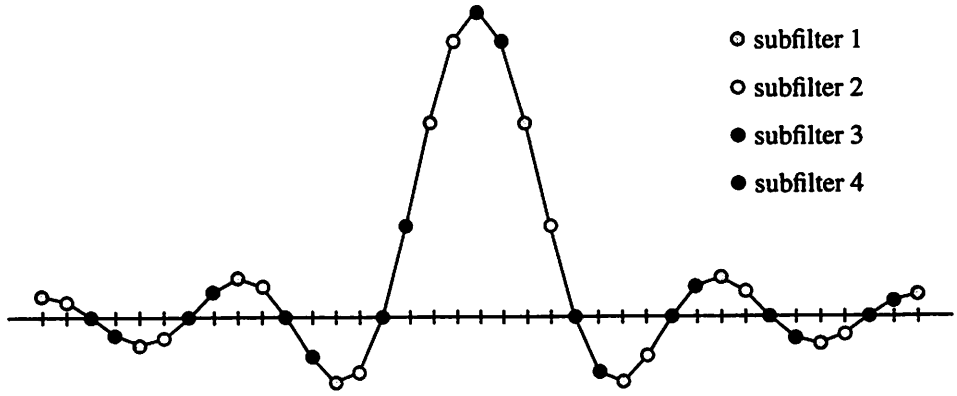


Figure 2-6. Truncated Raised-Cosine Pulse

but one coefficient are equal to zero. Also, the tap coefficients of the first filter are symmetric. As a result this ten-tap filter may be implemented using only five physical taps.

2.1.1.5. IF Modulation

Digital modulation of the baseband signal to an intermediate frequency before analog modulation to RF for transmission has two major advantages. First, since the digital data no longer has spectral energy at DC, AC coupling may be used in all subsequent stages in order to minimize data corruption from DC offsets as well as low frequency noise. Second, LO feedthrough in the analog mixers does not appear in the RF signal spectrum due to the IF offset.

Digital modulation may be performed by a direct digital frequency synthesizer (DDFS) [Nicholas91]. The main disadvantage of such an approach is the need for high-speed digital multipliers and adders. However, significant hardware reductions may be achieved by selecting an IF center frequency equal to 1/4 the sampling frequency. In fact, in addition to eliminating the need for a DDFS, the hardware complexity of the raised-cosine filter is also reduced by a factor of two. Instead of requiring eight subfilters for the in-phase and quadrature-phase data, only four subfilters are required.

Figure 2-7a illustrates the IF modulation process. The in-phase and quadrature-phase data are multiplied by $\cos[2\pi n/4]$ and $\sin[2\pi n/4]$, respectively. The digital mixers may be moved in front of the multiplexers as illustrated in Figure 2-7b. Since all even samples of $\cos[2\pi n/4]$ and all odd samples of $\sin[2\pi n/4]$ are equal to zero, the second and third subfilters for the in-phase data and the first and third subfilters for the quadrature phase data may be eliminated. In addition, multiplication by ± 1 may be incorporated into the tap coefficients of the remaining subfilters without the need for additional hardware. Finally, since all even samples of the in-phase data output and all odd samples of the quadrature-phase data output are equal to zero, the two data streams may be combined using one multiplexer instead of four adders as illustrated in Figure 2-7c. In addition, since the in-phase and quadrature-phase data streams are combined to form one data stream, only one digital-to-analog converter is required.

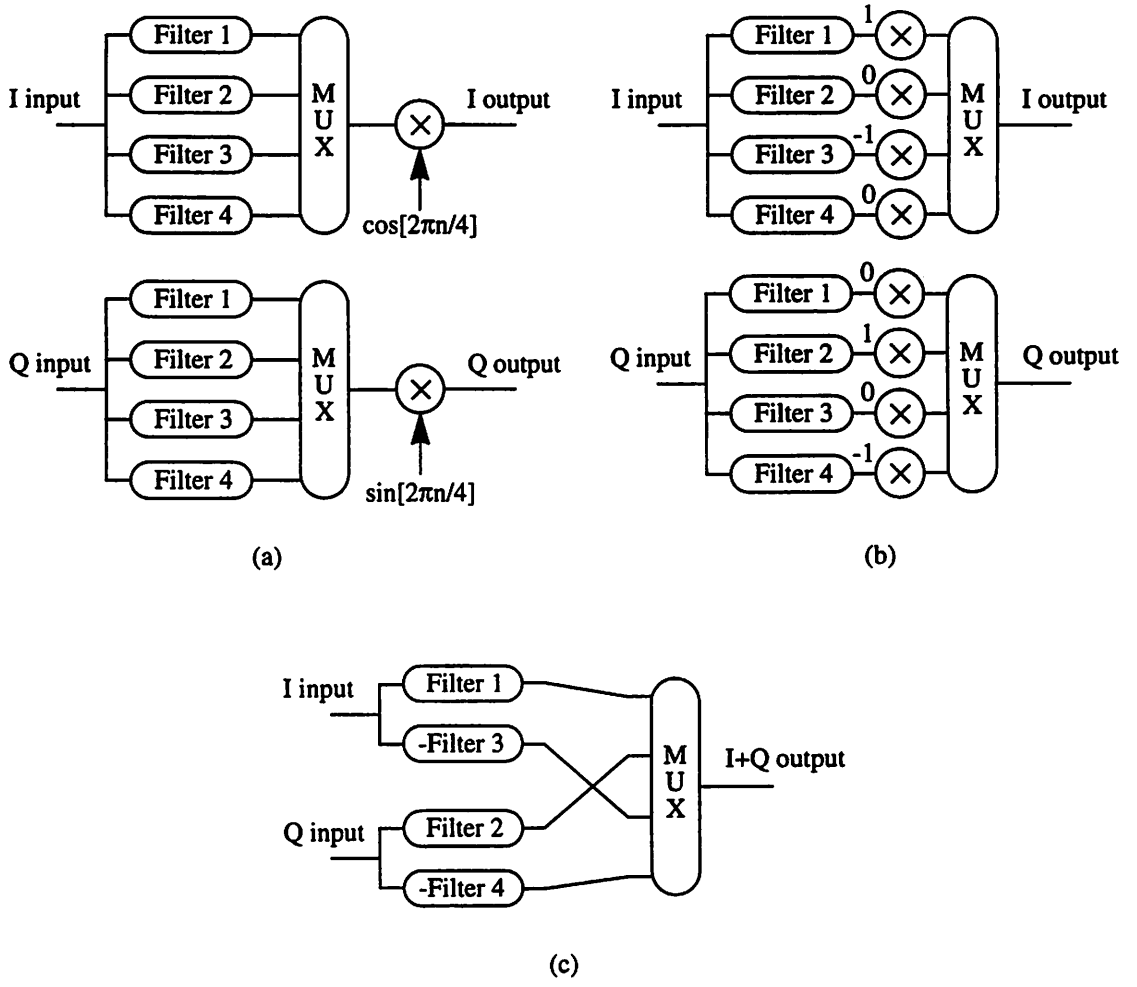


Figure 2-7. IF Modulation

(a) Modulation by $f_s/4$; (b) Combining Modulation Process with Raised-Cosine Subfilters; (c) Final Architecture

Although IF modulation significantly simplifies the hardware for the raised-cosine filter, it also complicates the architecture required to modulate the signal to RF for transmission. As illustrated in Figure 2-8a, a complex baseband signal may be upconverted to RF simply by multiplying the in-phase and quadrature-phase components by $\cos[2\pi f_c t]$ and $\sin[2\pi f_c t]$, respectively, where f_c is the carrier frequency. However, multiplication of the IF modulated signal by $\cos[2\pi(f_c - f_{IF})t]$ results in an undesired sideband at $f_c - 2f_{IF}$, where f_{IF} is the IF center frequency 64MHz. Correct modulation of the IF signal requires single-sideband upconversion techniques which will be discussed in the next chapter.

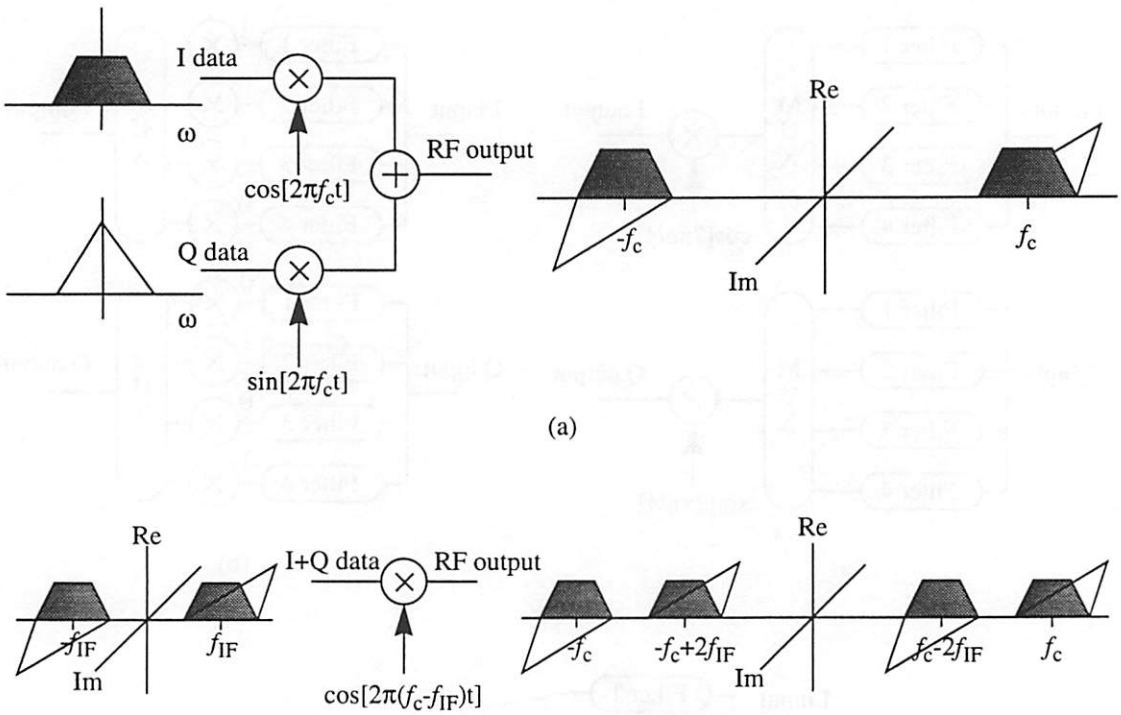


Figure 2-8. RF Modulation

(a) Direct Quadrature Upconversion of Baseband Signal; (b) Incorrect Modulation of IF Signal

2.1.2. Data Converter

The data converter block is responsible for converting the digital output of the baseband modulator chip to an analog signal for input to the single-sideband upconversion block. The following functions are performed in the data converter block:

- data combining
- digital-to-analog conversion
- droop compensation
- lowpass filter.

The specific implementation of these functions depends on the strategy used for single-sideband upconversion.

2.1.2.1. Data Combining

Except for the output of *-Filter 3*, each output of the other three subfilters consists of ten bits. The output of *-Filter 3* consists of nine bits. As already mentioned, this subfilter may be simplified to a simple delay. The maximum absolute value of the output for this subfilter is less than twice that of the other three subfilters. Since a two's complement number representation is used, only nine bits are required and the tenth bit is determined by sign extension. As indicated in Figure 2-7c, the outputs of the four subfilters must be combined using a multiplexer. This multiplexer is not implemented within the baseband modulator chip in order to increase flexibility in the data combining strategy.

2.1.2.2. Digital-to-Analog Conversion and Droop Compensation

High performance ECL digital-to-analog converters are required in order to meet the 10-bit, 256MHz specification. All digital-to-analog converters introduce droop distortion resulting from zero-order hold reconstruction. The magnitude frequency response of a zero-order hold filter is given by

$$|H(j\omega)| = \frac{\sin\left(\frac{\omega T}{2}\right)}{\frac{\omega}{2}}$$

At $\omega=\pi/T$, the amplitude attenuation is 3.92dB. The severity of the amplitude distortion depends on the bandwidth of the desired signal and the sampling period of the analog-to-digital converter. A large oversampling ratio results in less distortion in the frequency band of interest, and as a result, a droop compensation filter may not be necessary.

When the performance degradation due to droop is too severe, a droop compensation filter is required before or after the digital-to-analog converter. The frequency response of the compensation filter is simply the inverse of the zero-order hold filter response. Traditional implementations incorporate the droop compensation filter with the analog lowpass filter which follows the digital-to-analog converter. The main disadvantage of an analog approach is that the compensation filter is fixed-tuned to a specific sampling frequency. The droop compensation filter may also be implemented as a digital FIR filter before the

digital-to-analog converter. This approach allows for droop compensation at any sampling frequency by simply adjusting the clock rate of the digital filter. However, this filter must operate at the sampling frequency of the digital-to-analog converter. Such high-speed filters, although they consume a significant amount of power, are realizable using current submicron CMOS processes [Lin90].

2.1.2.3. Lowpass Filter

Finally, the spectral output from the digital-to-analog converter contains copies of the baseband spectrum at multiples of the sampling frequency. Although these copies are attenuated by the droop response of the digital-to-analog converter, an additional lowpass filter is necessary to further reject out-of-band components. Figure 2-9 illustrates the frequency spectrum after the digital-to-analog converter. The lowpass filter must have a

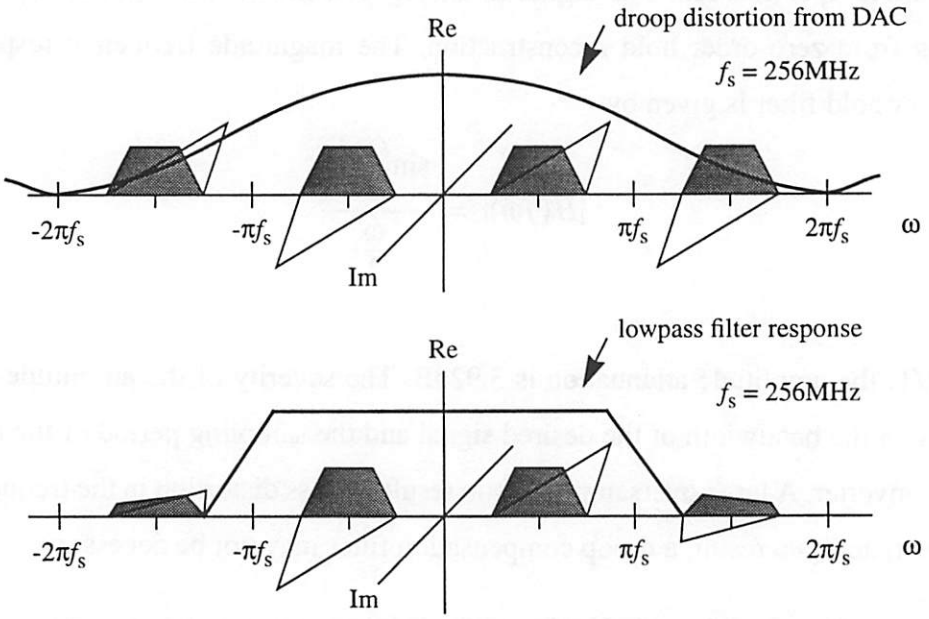


Figure 2-9. Lowpass Filter after Digital-to-Analog Converter

single-sided passband of 105.6MHz and at least 40dB of attenuation after 150.4MHz. Lowpass filters with these specifications are commercially available [Mini-Circuits92].

3 Single-Sideband Upconversion

The output of the baseband modulator chip consists of four 64MHz data streams: two for in-phase data and two for quadrature-phase data. A multiplexer combines the four data streams into one 256MHz data stream. The frequency response of the 256MHz data stream is illustrated in Figure 3-1. The in-phase and quadrature-phase data are modulated to a

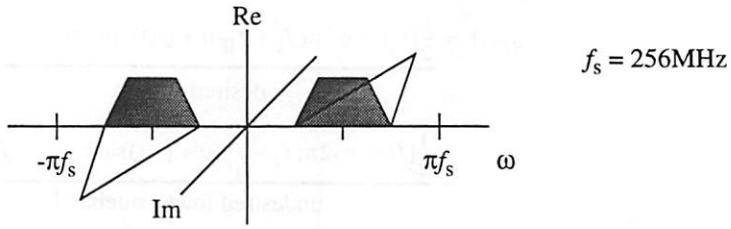


Figure 3-1. Frequency Response of Multiplexed Baseband Modulator Output

digital IF of 64MHz and may be represented by the following equation:

$$Y_{IF}(t) = I(t)\cos 2\pi(64MHz)t + Q(t)\sin 2\pi(64MHz)t$$

The spectrum of the desired signal for transmission at the RF of 1.088GHz appears in Figure 3-2. Direct upconversion by 1.024GHz of the IF signal results in an incorrect

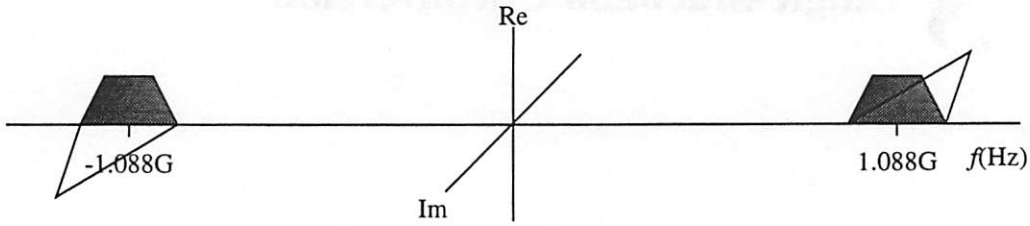


Figure 3-2. Frequency Response of Desired RF Output Signal

spectrum at RF due to the presence of lower sidebands located at 960MHz and -960MHz:

$$Y_{RF}(t) = [I(t)\cos 2\pi f_{IF}t + Q(t)\sin 2\pi f_{IF}t] \times \cos 2\pi f_c t, \quad f_{IF} = 64\text{MHz}, f_c = 1024\text{MHz}$$

$$Y_{RF}(t) = \underbrace{\frac{1}{2}[I(t)\cos 2\pi(f_c + f_{IF})t + Q(t)\sin 2\pi(f_c + f_{IF})t]}_{\text{desired signal}} + \underbrace{\frac{1}{2}[I(t)\cos 2\pi(f_c - f_{IF})t + Q(t)\sin 2\pi(f_c - f_{IF})t]}_{\text{undesired lower sideband}}$$

At least 40dB of sideband rejection is desirable in order to meet typical FCC out-of-band transmission rejection requirements. In order to achieve this sideband rejection, single-sideband upconversion is necessary. Three methods of single-sideband upconversion are listed below:

- filter method
- phase-shift method
- Weaver method.

The advantages and disadvantages of each method are discussed.

3.1. Single-Sideband Upconversion

3.1.1. Filter Method

The filter method is the most simple of the three methods. The block diagram of a possible implementation is illustrated in Figure 3-3. This method requires only one mixer and one

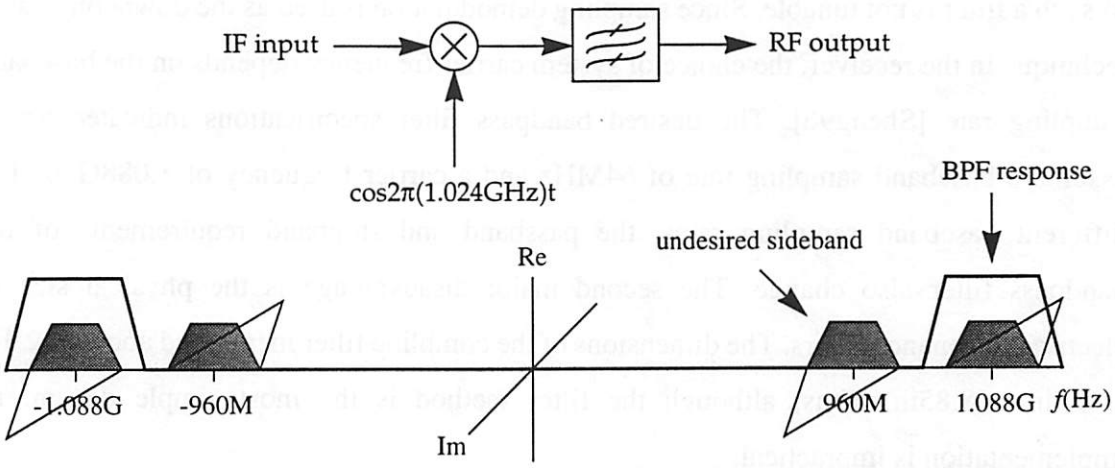


Figure 3-3. Filter Method

bandpass filter. The required bandpass filter has a passband of 83.2MHz centered at 1.088GHz. In addition, 40dB of attenuation is required within a 44.8MHz transition band, which is about 4% of the passband center frequency.

Several different types of bandpass filters exist. Tunable LC filters are attractive since they have center frequencies which may be adjusted for use with different carrier frequencies. However, the stopband attenuation of LC filters with center frequencies in excess of 1GHz falls well short of the desired 40dB rejection requirement. Mechanical resonance filters, such as ceramic resonators and SAW filters, offer high stopband rejection but are restricted to center frequencies under 1GHz. Finally, electrical resonance filters offer the high selectivity of mechanical resonance filters but also operate at center frequencies in excess of 1GHz. The characteristics of a custom eight-pole combline filter which meets the desired bandpass specifications for this application are tabulated in Table 3-1. The use of

Table 3-1. Combline Filter Characteristics

center frequency	1.088GHz
passband (-0.1dB ripple bandwidth)	1.046GHz - 1.130GHz

Table 3-1. Combline Filter Characteristics

attenuation at 1.0016GHz	44dB
attenuation at 1.1744GHz	53dB
insertion loss	0.6dB
dimensions	2.1in x 1.5in x 8.85in

electrical resonance filters is impractical for two major reasons. First, the center frequency of such a filter is not tunable. Since sampling demodulation is used as the downconversion technique in the receiver, the choice of system carrier frequency depends on the baseband sampling rate [Sheng96]. The desired bandpass filter specifications indicated above assume a baseband sampling rate of 64MHz and a carrier frequency of 1.088GHz. For different baseband sampling rates, the passband and stopband requirements of the bandpass filter also change. The second major disadvantage is the physical size of electrical resonance filters. The dimensions of the combline filter mentioned above is 2.1in x 1.5in x 8.85in. Thus, although the filter method is the most simple design, its implementation is impractical.

3.1.2. Phase-Shift Method

The phase-shift method is another way to achieve single-sideband upconversion. A block diagram of this method is illustrated in Figure 3-4. This method requires two mixers, an

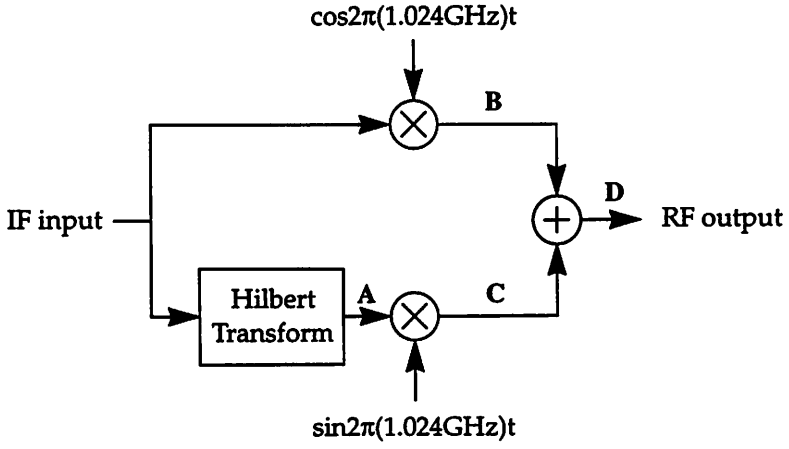


Figure 3-4. Phase-Shift Method

RF power combiner, and a Hilbert transformer. The Hilbert transformer is a wideband 90° power splitter defined as follows:

$$H(\omega) = \begin{cases} j, & \omega > 0 \\ -j, & \omega < 0 \end{cases}$$

The frequency response at points A, B, C, and D are illustrated in Figure 3-5. This method

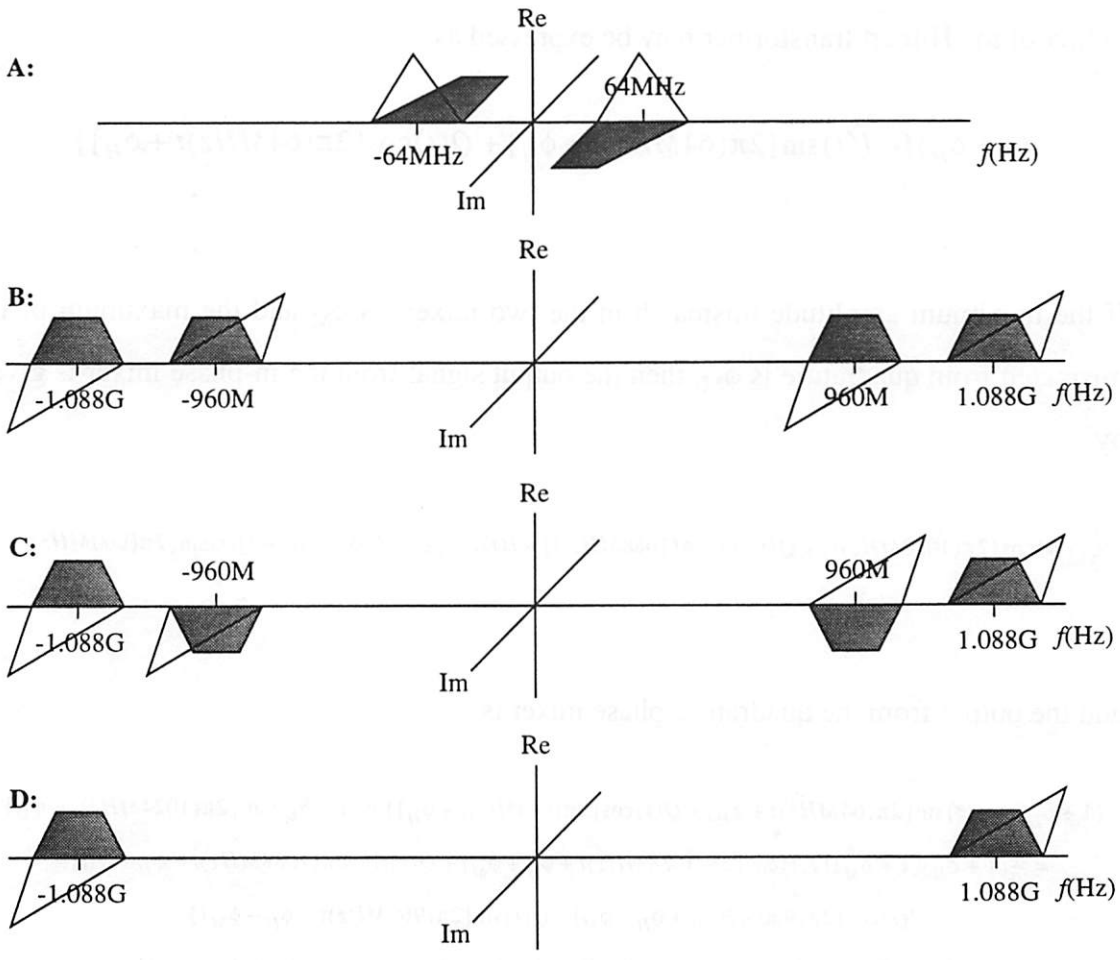


Figure 3-5. Frequency Response at Various Points for Phase-Shift Method

of single-sideband upconversion relies on the cancellation of the lower sideband. However, perfect cancellation is impossible in practical implementations due to amplitude and phase

mismatches in the two mixers as well as in the Hilbert transformer. The input signal may be expressed as

$$I(t)\cos[2\pi(64MHz)t] + Q(t)\sin[2\pi(64MHz)t]$$

If a practical implementation of the Hilbert transformer results in a maximum amplitude difference from unity of δ_H and a maximum phase difference from 90° of ϕ_H, then the output of the Hilbert transformer may be expressed as

$$(1+\delta_H)\{-I(t)\sin[2\pi(64MHz)t+\phi_H] + Q(t)\cos[2\pi(64MHz)t+\phi_H]\}$$

If the maximum amplitude mismatch in the two mixers is δ_M and the maximum phase mismatch from quadrature is ϕ_M, then the output signal from the in-phase mixer is given by

$$\frac{1}{2}\{I(t)\cos[2\pi(1088MHz)t] + Q(t)\sin[2\pi(1088MHz)t] + I(t)\cos[2\pi(960MHz)t] + Q(t)\sin[2\pi(960MHz)t]\}$$

and the output from the quadrature-phase mixer is

$$\begin{aligned}
&(1+\delta_H)\{-I(t)\sin[2\pi(64MHz)t+\phi_H] + Q(t)\cos[2\pi(64MHz)t+\phi_H]\} \times (1+\delta_M)\sin[2\pi(1024MHz)t+\phi_M] \\
&= \frac{1}{2}(1+\delta_H)(1+\delta_M)\{I(t)\cos[2\pi(1088MHz)t+\phi_H+\phi_M] + Q(t)\sin[2\pi(1088MHz)t+\phi_H+\phi_M] - \\
&\qquad I(t)\cos[2\pi(960MHz)t+\phi_H-\phi_M] - Q(t)\sin[2\pi(960MHz)t+\phi_H-\phi_M]\} \\
&= \frac{1}{2}(1+\delta_H)(1+\delta_M)\{\cos[2\pi(1088MHz)t][I(t)\cos(\phi_H+\phi_M) + Q(t)\sin(\phi_H+\phi_M)] + \\
&\qquad \sin[2\pi(1088MHz)t][Q(t)\cos(\phi_H+\phi_M) - I(t)\sin(\phi_H+\phi_M)] - \\
&\qquad \cos[2\pi(960MHz)t][I(t)\cos(\phi_H-\phi_M) + Q(t)\sin(\phi_H-\phi_M)] - \\
&\qquad \sin[2\pi(960MHz)t][Q(t)\cos(\phi_H-\phi_M) - I(t)\sin(\phi_H-\phi_M)]\}
\end{aligned}$$

Thus, after the outputs of the in-phase and quadrature-phase mixers are combined, residual energy in the sidelobe centered at 960MHz remains. In addition, interference from the quadrature-phase component appears in the in-phase sidelobe centered at 1.088GHz and interference from the in-phase component appears in the quadrature-phase sidelobe centered at 1.088GHz. A typical value of amplitude imbalance for a monolithic QPSK modulator is ±1.0 dB [Hewlett-Packard93] and a typical value of phase imbalance for a quadrature clock generator is ±2.0° [Mini-Circuits92]. A typical 90° power splitter exhibits ±1.2 dB of amplitude imbalance and ±2.0° of phase imbalance [Mini-Circuits92]. For a voltage swing of 1V, $|\delta_H|$=130mV, $|\phi_H|$=2.0°, $|\delta_M|$=100mV, and $|\phi_M|$=2.0°, resulting in about 20dB of sideband rejection. It is possible to increase the sideband rejection to about 35dB by adjusting the amplitude of the in-phase and quadrature-phase input signals to the QPSK modulator. Additional sideband rejection may be obtained by using a highpass filter after the RF power combiner.

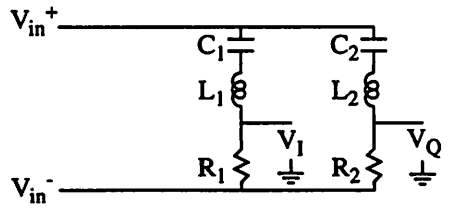
The most difficult aspect of using the phase-shift method for this application is implementation of a Hilbert transformer which operates between 22.4MHz and 105.6MHz (130% of the center frequency) with a phase imbalance no greater than 2.0°. Commercially available 90° power splitters which meet this specification do not exist. The next two sections discuss custom implementations of the Hilbert transformer. The first section focuses on analog implementations whereas the second section discusses digital implementations.

3.1.2.1. Hilbert Transformer: Analog Implementations

The main advantage of performing the Hilbert transform in the analog domain is that only one digital-to-analog converter is required for the entire transmitter. However, the realization of a Hilbert transformer with constant amplitude and phase outputs from 22.4MHz to 105.6MHz is nontrivial.

3.1.2.1.1. RLC Phase-Splitter Circuit

One passive network which produces in-phase and quadrature-phase outputs is depicted in Figure 3-6 [Luck49]. Selecting $\omega_1=2\pi(22.4\text{MHz})$ and $\omega_2=2\pi(105.6\text{MHz})$ gives



$$\omega_1^2 = \frac{\omega_0^2}{r^2} = \frac{1}{L_1 C_1}$$

$$\omega_2^2 = \omega_0^2 r^2 = \frac{1}{L_2 C_2}$$

$$Q^2 = \frac{L_1}{C_1 R_1^2} = \frac{L_2}{C_2 R_2^2}$$

Figure 3-6. RLC Phase-Splitter Circuit

$\omega_0=2\pi(48.6\text{MHz})$ and r=2.17. The phase difference ψ between V_I and V_Q is related to the frequency ω through the following equation:

$$\tan\frac{1}{2}\psi = \frac{\frac{1}{Q}\left(r-\frac{1}{r}\right)\left(\frac{\omega}{\omega_0}+\frac{\omega_0}{\omega}\right)}{\frac{1}{Q^2}-\left(r-\frac{1}{r}\right)^2-4+\left(\frac{\omega}{\omega_0}+\frac{\omega_0}{\omega}\right)^2}$$

Selecting the phase difference to be 90° at $\omega=\omega_0$ results in the following expression for Q as a function of r:

$$Q = \frac{\sqrt{2}-1}{r-\frac{1}{r}}$$

The corresponding value for Q is 0.242. A plot of ψ as a function of f is given in Figure 3-7. The maximum phase variation from 90° for this case is about 5°, which is too high if the desired sideband rejection of 40dB is to be achieved. The phase variation over the frequency band of interest may be decreased by using a different set of values for f_0, r, and Q. A plot of ψ as a function of f for f_0=48.6MHz, r=1.9, and Q=0.302 appears in Figure 3-8. The maximum phase variation from 90° for this case is only about 1°. Although this implementation of the Hilbert transformer appears very attractive due to the theoretical

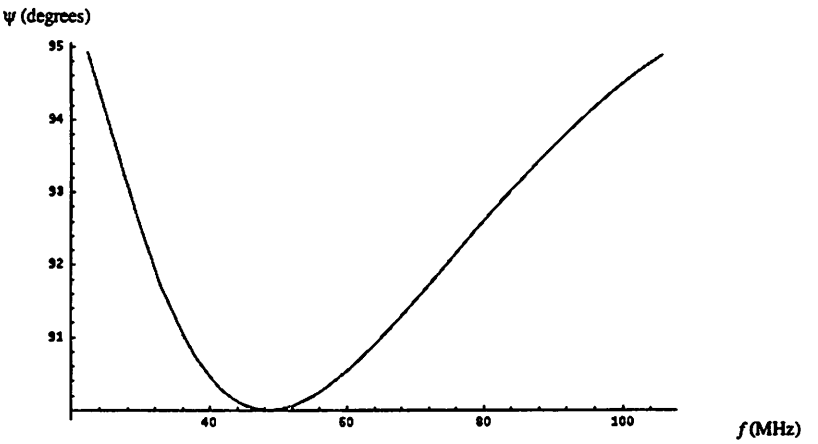


Figure 3-7. RLC Phase-Splitter ψ Response (f_0=48.6MHz, r=2.17, Q=0.242)

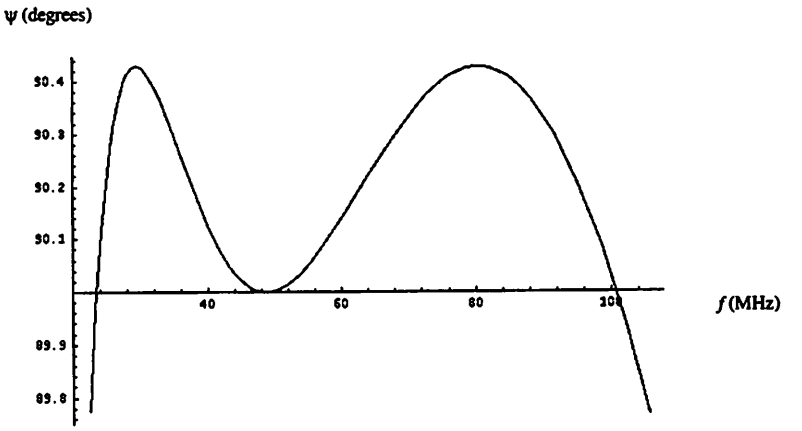


Figure 3-8. RLC Phase-Splitter ψ Response (f_0=48.6MHz, r=1.9, Q=0.302)

phase imbalance of only 1°, two major drawbacks exist: non-constant phase relationship of individual outputs; and component value variation and mismatch.

The phase dependence on frequency for both outputs is given below:

$$\tan\frac{1}{2}\phi_I = Q\left(\frac{\omega_0}{r\omega} - \frac{r\omega}{\omega_0}\right)$$

$$\tan\frac{1}{2}\phi_I = Q\left(\frac{\omega_0}{r\omega} - \frac{r\omega}{\omega_0}\right)$$

ϕ_I and ϕ_Q for f_0=48.6MHz, r=1.9, and Q=0.302 are plotted in Figure 3-9. Although ϕ_Q is

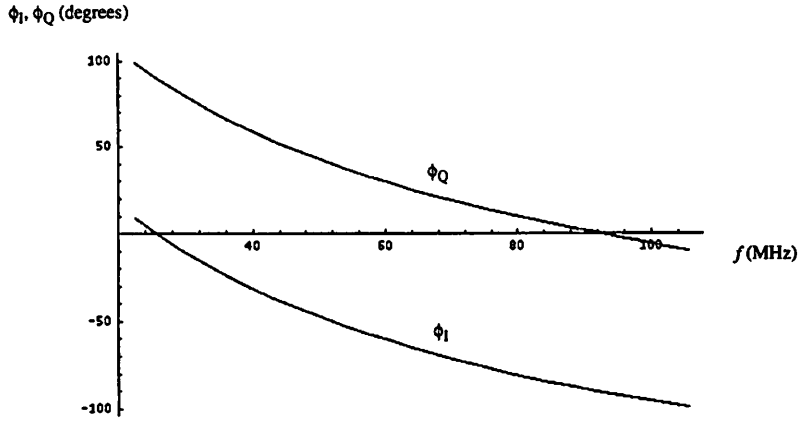


Figure 3-9. RLC Phase-Splitter ϕ_I and ϕ_Q Response (f_0=48.6MHz, r=1.9, Q=0.302)

offset from ϕ_I by 90° across the entire band of interest, the individual phase curves are not constant, resulting in non-constant phase offsets across the entire frequency band. The magnitudes of V_I and V_Q are equal to half the input voltage magnitude across the entire frequency band.

The implementation of this method is limited to the use of discrete components since a monolithic approach is not available. If a 100nH surface mount inductor with a 5% tolerance [Digi-Key96] is used for L_1 and L_2, then the following component values are required for f_0=48.6MHz, r=1.9, and Q=0.302: R_1=53.2Ω, R_2=192.1Ω, C_1=387pF, and C_2=29.7pF. SPICE simulation using the above component values results in the plots shown

in Figure 3-10. The SPICE results agree well with predicted performance. However, the

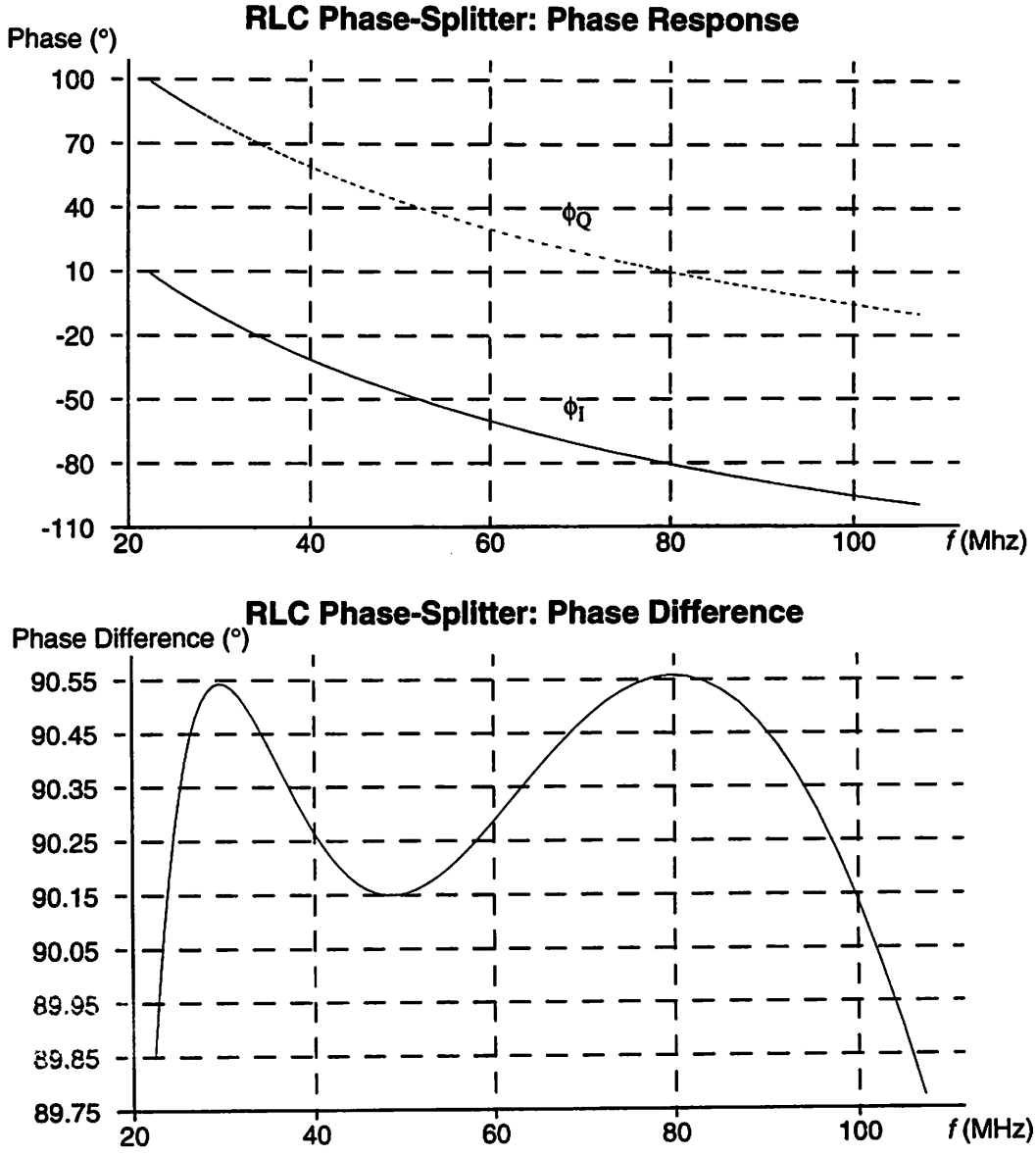


Figure 3-10. RLC Phase-Splitter Simulated Response (R_1=53.2Ω, R_2=192.1Ω, C_1=387pF, C_2=29.7pF, L_1=100nH, L_2=100nH)

component values used for this simulation are not commercially available, and in addition, this simulation does not take into account component tolerances. Minimization of parasitic resistance, capacitances and inductances requires the use of surface mount components with very small form factors, such as obtained in a 0603 package. Resistors with 1% tolerance are commercially available with values 53.6Ω and 191Ω [Digi-Key96].

Capacitors with 10% tolerance are commercially available with values 390pF and 27pF [Digi-Key96]. SPICE simulation of the RLC phase-splitter circuit using commercially available values results in the plots shown in Figure 3-11. For this case, the maximum

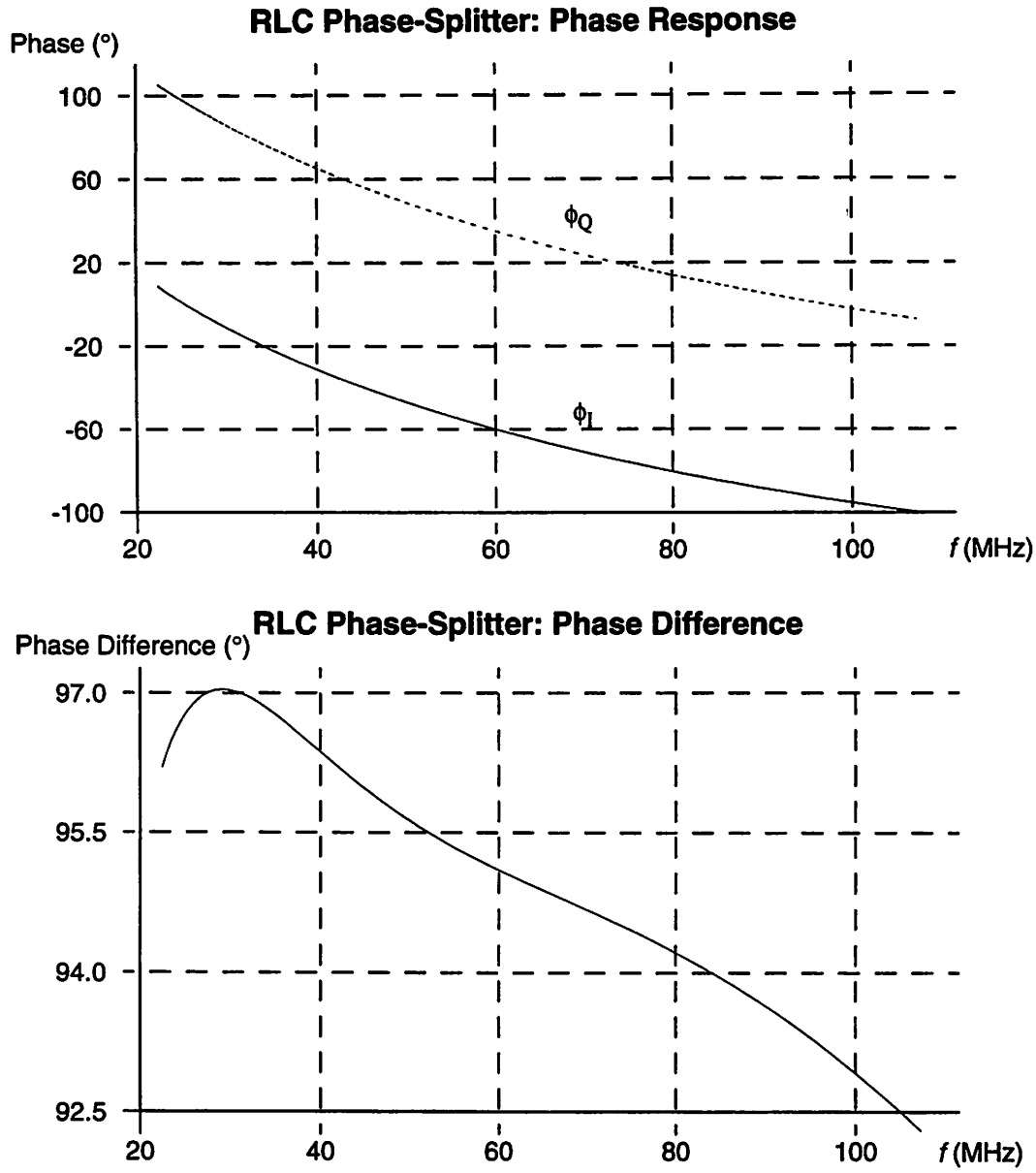


Figure 3-11. RLC Phase-Splitter Simulated Response with Commercially Available Component Values (R_1=53.6Ω, R_2=191Ω, C_1=390pF, C_2=27pF, L_1=100nH, L_2=100nH)

phase variation from quadrature is about 7°. Thus, the RLC phase-splitter network is very

sensitive to component value deviations and is not amenable to discrete component realizations.

3.1.2.1.1. Asymmetric Polyphase Networks

The most simple asymmetric polyphase network is the RC-CR structure depicted in Figure 3-12a. The voltage gain is unity for all frequencies and the phase of V_o is offset

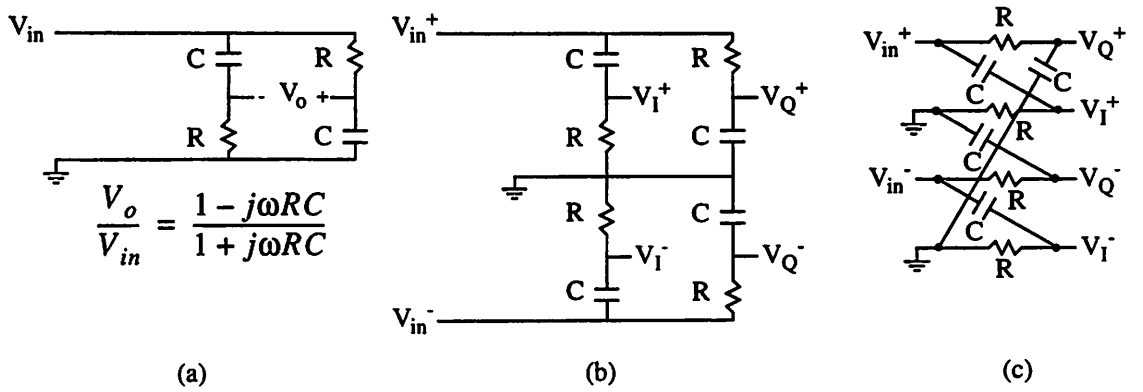


Figure 3-12. RC-CR Structure

(a) Single-Ended; (b) Differential; (c) Differential (Redrawn)

from that of V_{in} by 90° at ω=1/RC. A differential version of the RC-CR structure is depicted in Figure 3-12b. The differential output voltage $V_Q=V_Q^+-V_Q^-$ is offset from the differential output voltage $V_I=V_I^+-V_I^-$ by 90° at all frequencies and the amplitude of both output voltages is $1/\sqrt{2}$ times that of the input voltage at ω=1/RC. The results of a SPICE simulation for R=4.97kΩ and C=0.5pF are depicted in Figure 3-13. As seen in the SPICE results, perfect quadrature is maintained across the entire frequency band. However, the phase response of the individual outputs is not constant. SPICE results also confirm that the gain is equal to $1/\sqrt{2}$ at ω=1/RC and for a 1V input the maximum output amplitude mismatch is about 600mV. Figure 3-12c depicts a redrawn version of the same differential RC-CR network shown in Figure 3-12b.

A major disadvantage of the differential RC-CR polyphase network is that output voltage amplitudes are equal at only one frequency. One solution is to cascade multiple stages as

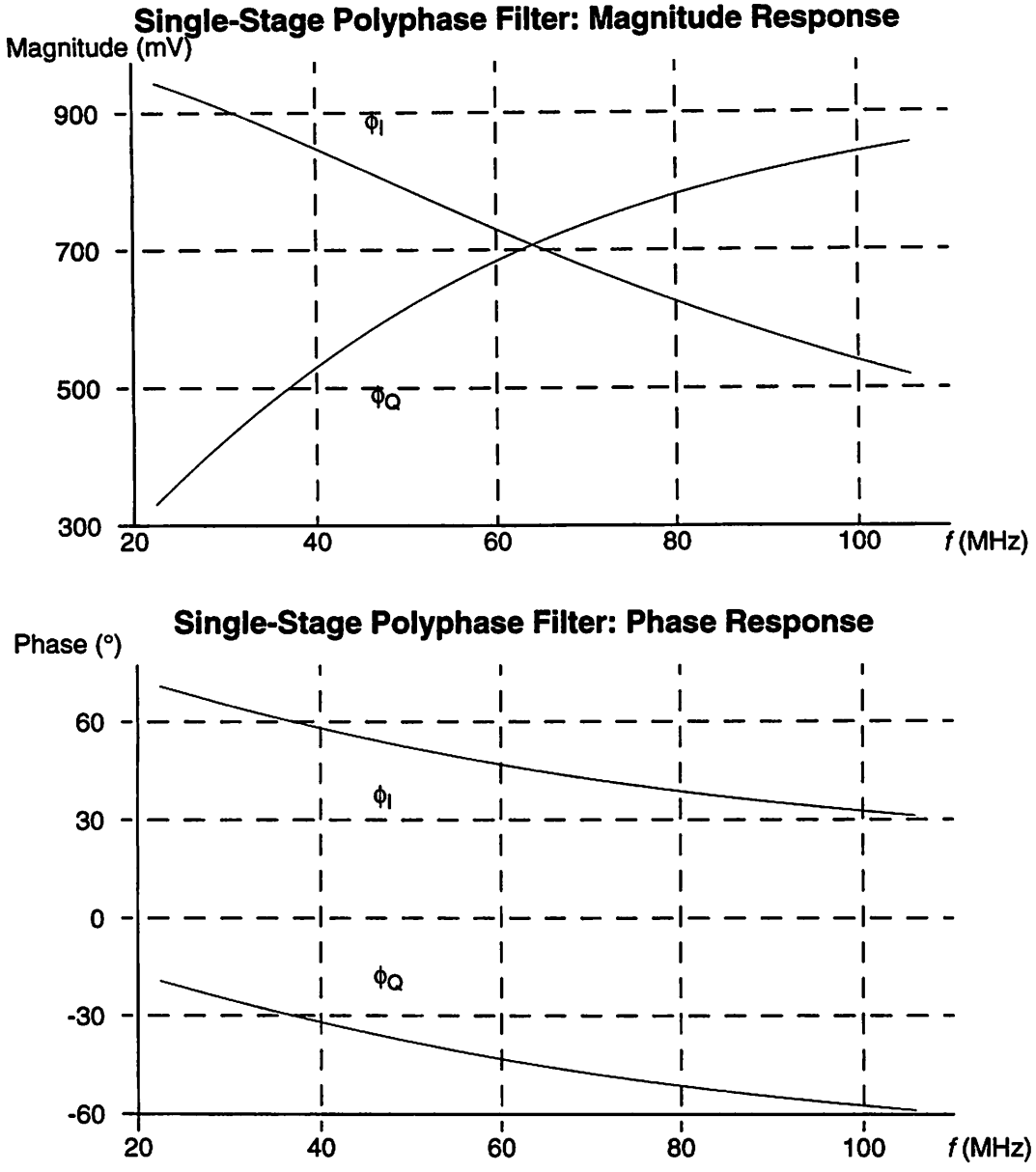


Figure 3-13. SPICE Simulation of Single-Stage Asymmetric Polyphase Filter (R=4.97kΩ, C=0.5pF)

depicted in Figure 3-14 [Gingell73][West91][Crols95]. Each stage contributes a pole at $s=1/R_xC_x$ and a zero at $s=-1/R_xC_x$. SPICE simulation for a two-stage asymmetric polyphase filter with $R_1=R_2=4.97k\Omega$ and $C_1=C_2=0.5pF$ results in the plots depicted in Figure 3-15. Again, perfect quadrature is maintained across the entire frequency band. However, for a 1V input voltage, the maximum output amplitude mismatch is now about

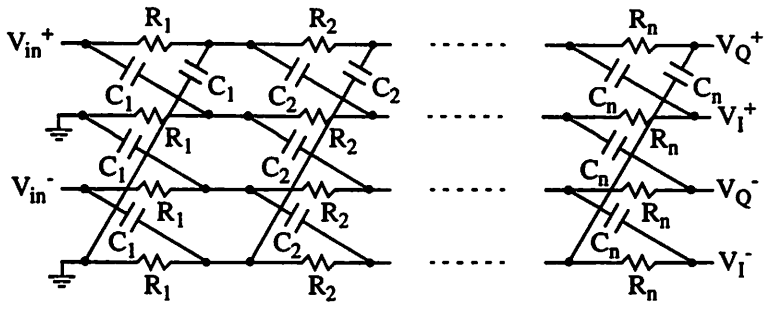


Figure 3-14. N-Stage Asymmetric Polyphase Filter

250mV. This mismatch may be decreased further by cascading additional filter stages. However, the insertion loss is directly proportional to the number of cascaded stages, and thus, the output signals may require amplification if many stages are used. Another way to decrease the amplitude mismatch is by selecting different values for ω_1 and ω_2. The results of a SPICE simulation for a two-stage asymmetric polyphase filter with R_1=14.21kΩ, R_2=3.01kΩ, and C_1=C_2=0.5pF are depicted in Figure 3-16. For this case, the maximum amplitude mismatch is about 100mV. The best amplitude mismatch is achieved by using multiple stages and selecting $\omega_x=1/R_xC_x$ of each stage to be a different value.

Although perfect quadrature is maintained over the entire frequency band, the individual phase response of each output varies as much as 40° over about 85MHz. Due to the non-constant phase response of these asymmetric polyphase filters, their utility is limited to narrow-band applications, such as generating in-phase and quadrature-phase LO signals.

3.1.2.2. Hilbert Transformer: Digital Implementations

The main disadvantage of implementing the Hilbert transform in the digital domain is that two digital-to-analog converters are required for the complete transmitter circuitry. However, since the transmitter resides in the basestation, the additional power consumption is not critical.

3.1.2.2.1. Post-Modulator Double-Sideband to Single-Sideband Converter

Multiplexing the in-phase and quadrature-phase output data streams from the baseband modulator results in a single 256MHz digital data stream, and thus, a 256MHz digital

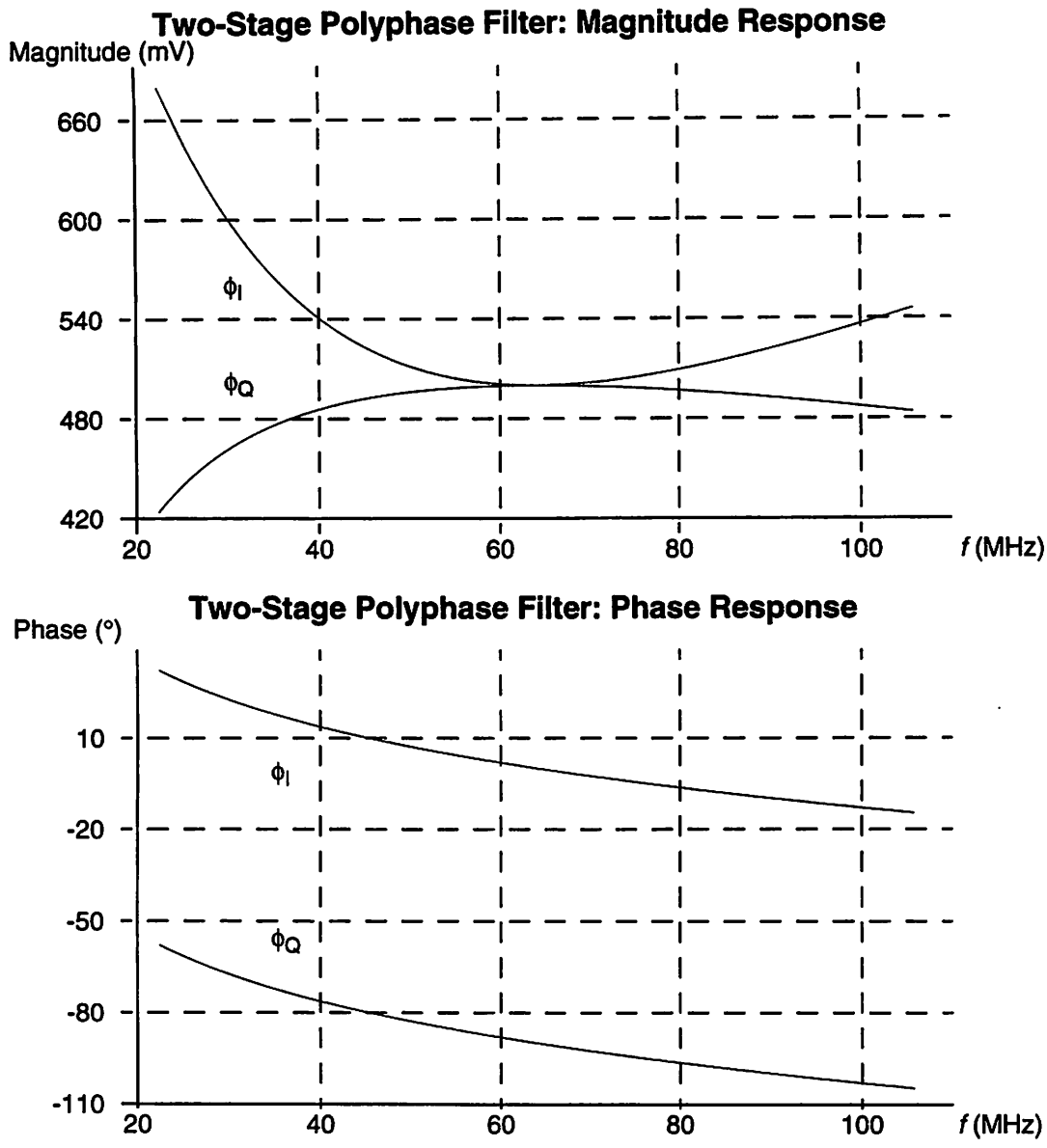


Figure 3-15. SPICE Simulation of Two-Stage Asymmetric Polyphase Filter (R_1=R_2=4.97kΩ, C_1=C_2=0.5pF)

Hilbert transformer is required. Digital Hilbert transformers have been designed which operate at frequencies as high as 300MHz [Hawley95].

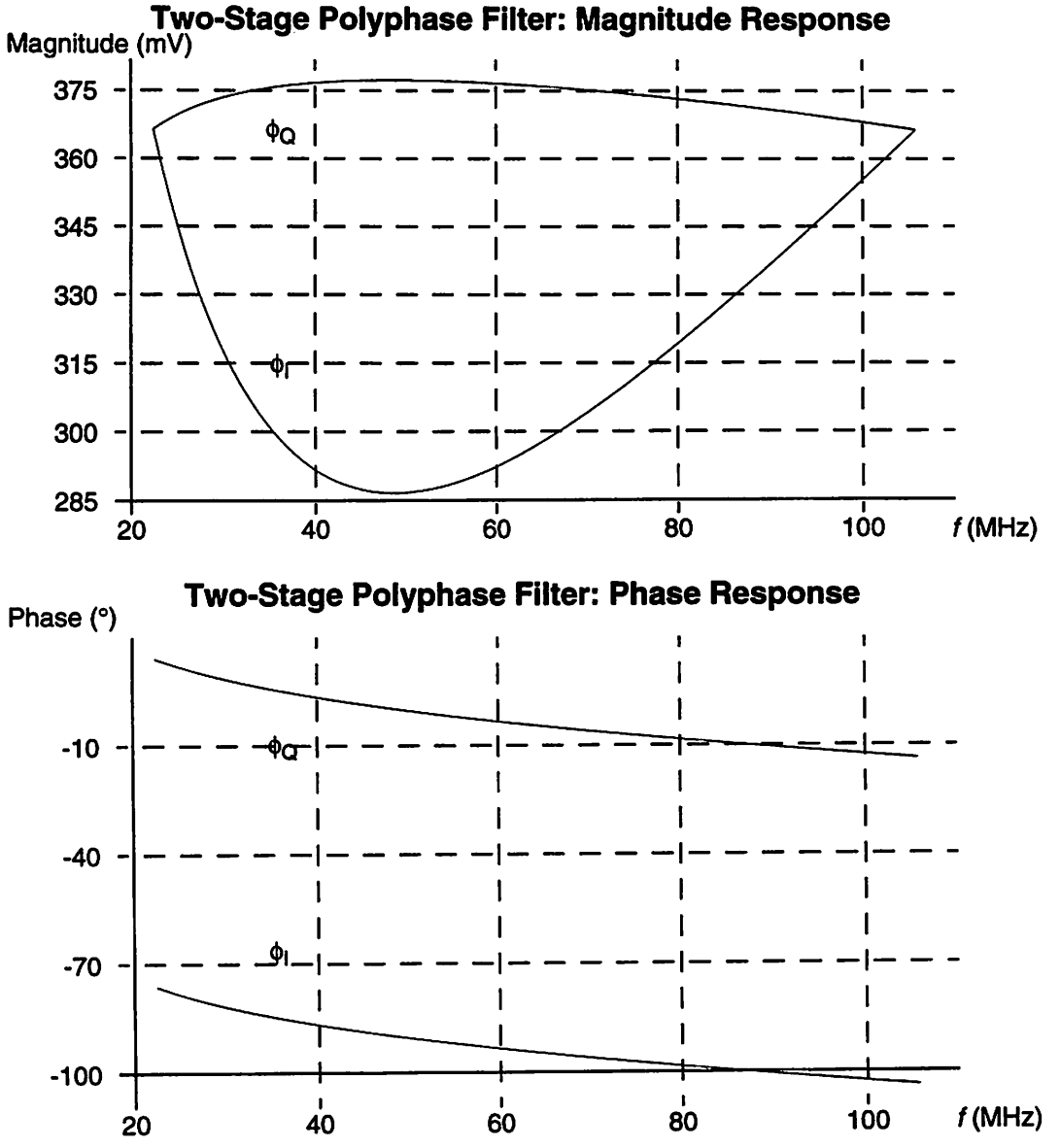


Figure 3-16. SPICE Simulation of Two-Stage Asymmetric Polyphase Filter (R_1=14.21kΩ, R_2=3.01kΩ, C_1=C_2=0.5pF)

The frequency response of an ideal Hilbert transformer is given by

$$H(\omega) = e^{-j\left(\frac{\pi}{2}\right)\mathrm{sgn}(\omega)}$$

and the corresponding time domain impulse response is given by

$$h[n] = \begin{cases} 0 & n = 0 \\ \dfrac{\sin^2(\pi n/2)}{\pi n/2} & n \neq 0 \end{cases}$$

The ideal transform is not physically realizable since it is noncausal and of infinite duration. A practical realization requires windowing and shifting the sequence, resulting in a finite and causal impulse response. However, such an implementation results in finite stopband energy as well as passband ripple. The number of taps as well as coefficient quantization and internal number representation must be optimized in order to minimize passband ripple and energy in the stopband.

One way of interpreting the output of the Hilbert transformer is that it is a sequence similar to the input but phase shifted by 90°. For example, the in-phase data is multiplied by cos[2πn/4] in the baseband modulator chip. Since cos[2πn/4] is equal to zero for all odd values of n, these values of the in-phase data need not be computed and are discarded. The function of the Hilbert transformer is to determine the values at these discarded points. This interpretation of the output of the Hilbert transformer suggests a more efficient way of performing single-sideband upconversion, which will be discussed in the next section.

3.1.2.2.2. Incorporation of Digital Hilbert Transformer within Baseband Modulator

The baseband modulator chip incorporates two important design simplifications. First, since both in-phase and quadrature-phase data sequences are oversampled by a factor of four, each corresponding 256MHz raised-cosine filter may be divided into four parallel subfilters each operating at 64MHz. Second, the in-phase and quadrature-phase data streams are modulated by cos[2πn/4] and sin[2πn/4], respectively. Since all odd samples of cos[2πn/4] are equal to zero and all even samples of sin[2πn/4] are equal to zero, the corresponding subfilters may be eliminated, and thus, only two parallel filters each operating at 64MHz are required for each 256MHz raised-cosine filter.

The outputs of the baseband modulator chip are I[n]cos[2πn/4] and Q[n]sin[2πn/4]. The Hilbert transforms of these two signal streams are I[n]sin[2πn/4] and -Q[n]cos[2πn/4].

Thus, the function of the post-modulator digital Hilbert transform is to reconstruct the samples of the in-phase and quadrature-phase data which have been discarded. Instead of reconstructing the values of I[n]sin[2πn/4] and -Q[n]cos[2πn/4] with a post-modulator Hilbert transformer, these values may be generated directly within the baseband modulator chip. The architecture is depicted in Figure 3-17. The signal I[n]cos[2πn/4]+Q[n]sin[2πn/

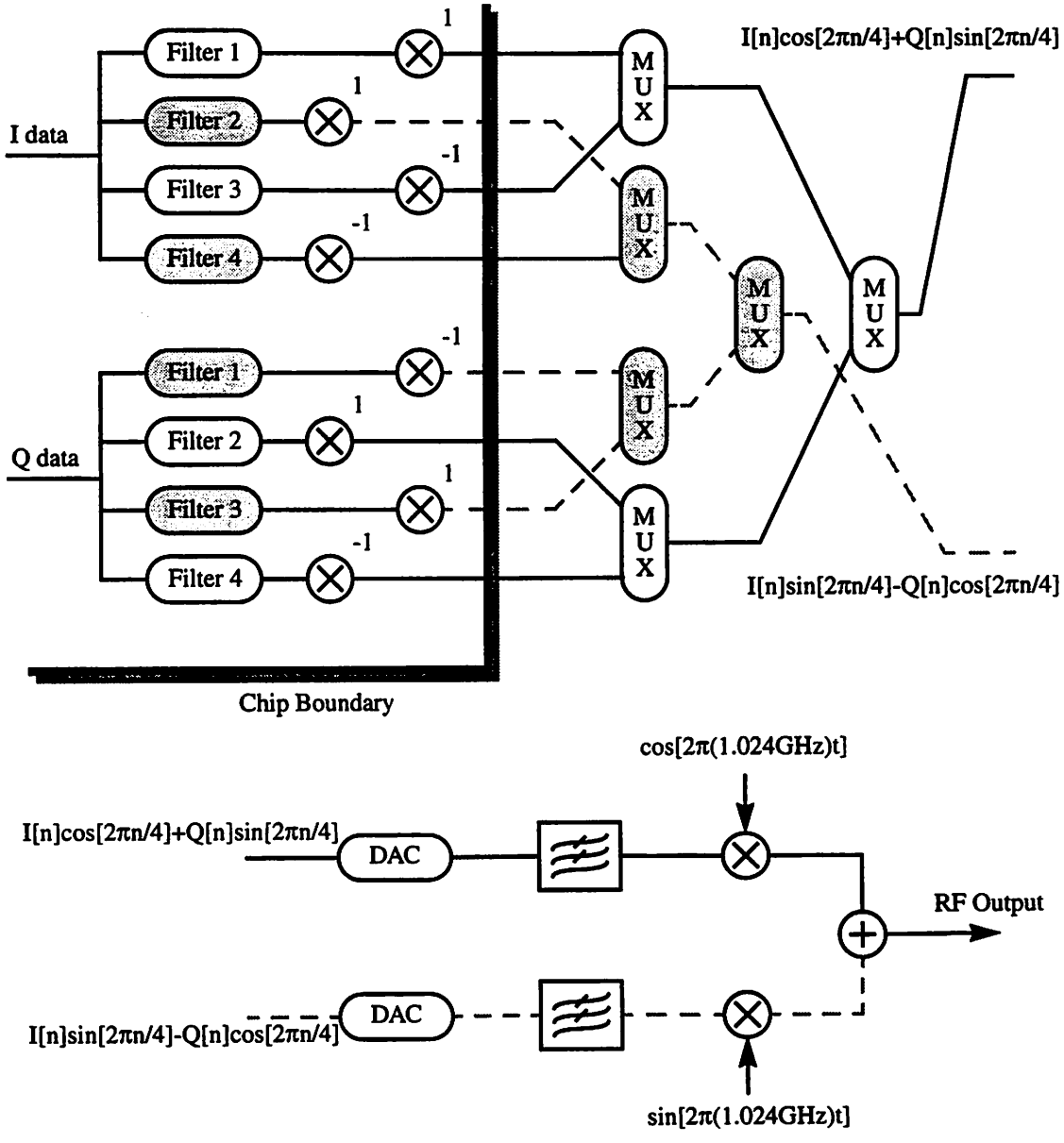


Figure 3-17. Architecture of Hilbert Transform Incorporated within Baseband Modulator Chip

4] along the signal path denoted by the solid lines is identical the output of the current

baseband modulator chip, which is illustrated in Figure 2-7c. The signal I[n]sin[2πn/4]-Q[n]cos[2πn/4] along the signal path denoted by the dashed lines is the corresponding Hilbert transform. The shaded subfilters, Filter 2 and Filter 4, used to generate the Hilbert transform output along the in-phase data path are identical to the unshaded subfilters, Filter 2 and Filter 4, along the quadrature-phase data path. Similarly, the shaded subfilters, Filter 1 and Filter 3, used to generate the Hilbert transform output along the quadrature-phase data path are identical to the unshaded subfilters, Filter 1 and Filter 3, along the in-phase data path. Thus, the procedure used to implement the subfilters in the current baseband modulator chip, which is described in [Peroulas95], may also be used to implement the additional four subfilters required to generate the Hilbert transform output. The filter coefficients of the subfilters are listed in Table 3-2.

Table 3-2. Quantized Filter Coefficients

Filter 1	Filter 2	Filter 3	Filter 4
0.005126953125	0.00634765625	0.0	-0.0136566162109375
-0.0263671875	-0.0244140625	0.0	0.0400390625
0.072265625	0.06353759765625	0.0	-0.09765625
-0.171875	-0.1572265625	0.0	0.28515625
0.623046875	0.890625	1.0	0.890625
0.623046875	0.28515625	0.0	-0.1572265625
-0.171875	-0.09765625	0.0	0.06353759765625
0.072265625	0.0400390625	0.0	-0.0244140625
-0.0263671875	-0.0136566162109375	0.0	0.00634765625
0.005126953125		0.0	

This method of generating the Hilbert transform results in minimum amplitude and phase distortion at the expense of increasing the complexity of the baseband modulator chip. The area of the current baseband modulator chip, which was fabricated in a 0.8μm CMOS process, is $1x1cm^2$. Since this method requires a total of eight subfilters instead of just four, incorporating the additional four subfilters onto the same chip may be impractical from an area standpoint unless the design is fabricated in a process with a smaller minimum feature size.

In addition to providing minimum amplitude and phase distortion, this method maintains the added benefit of modulating the baseband signal to an IF of 64MHz. Since the output

data from the baseband modulator chip has no spectral energy at DC, AC coupling may be used to minimize DC offset as well as low frequency noise introduced by the digital-to-analog converters. In addition, LO feedthrough in the mixers does not appear in the RF signal spectrum due to the 64MHz frequency offset.

Although this method is the most attractive solution, its implementation necessitates a re-design and re-fabrication of the baseband modulator chip. Due to time constraints, this method was not pursued. Instead a method which makes use of the existing baseband modulator chip was implemented. This method is a digital variant of the Weaver method and will be discussed later. Nevertheless, future versions of the transmitter should incorporate the techniques mentioned in this section.

3.1.3. Weaver Method

Another method of single-sideband upconversion is the Weaver method. A block diagram of the Weaver method appears in Figure 3-18. This method involves two stages of mixers

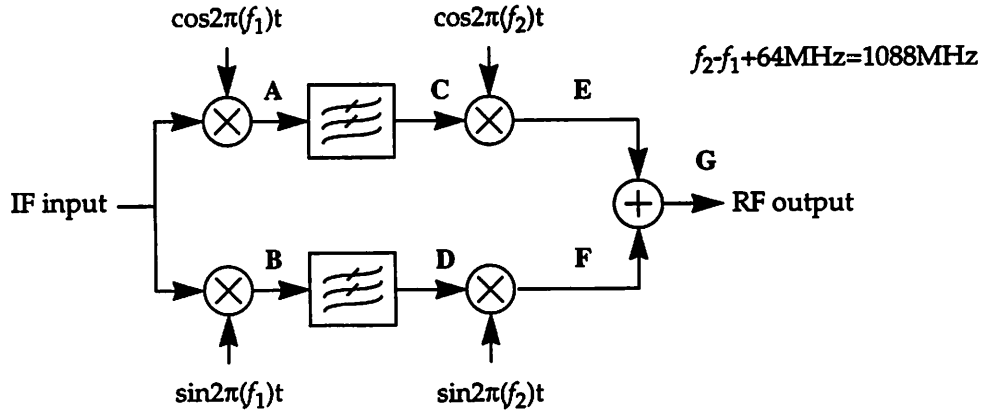


Figure 3-18. Weaver Method

as well as two lowpass filters. Quadrature clock generators are required for both frequencies f_1 and f_2. For f_{IF}=64MHz and f_c=1.088GHz, f_1 and f_2 must satisfy the following equation:

$$f_2 - f_1 + 64\text{MHz} = 1088\text{MHz}$$

3.1.3.1. Double Upconversion Method

In traditional implementations of the Weaver method, the frequency of the first stage of mixers is selected to be at least the single-sided bandwidth of the input signal. For an IF input signal with a single-sided bandwidth of 105.6MHz as illustrated in Figure 3-1, selecting f_1=110MHz requires f_2=1.134GHz and a lowpass filter with a passband from DC to 87.6MHz and a stopband after 132.4MHz with at least 40dB attenuation. The frequency response at points A, B, C, D, E, F, and G are depicted in Figure 3-19. The mixer gain constraints as well as the quadrature phase requirements of this method are similar to those specified for the phase-shift method. However, one major disadvantage of this method is the introduction of an extra LO frequency. The use of an extra LO frequency may be avoided by using a down-up Weaver method.

3.1.3.2. Down-Up Method

The Weaver method is traditionally used for single-sideband upconversion of baseband signals which have spectral energy down to DC. However, the input signal for this case has been digitally modulated to an IF of 64MHz. Thus, one way to achieve the desired RF output signal is to first undo the IF modulation and then directly mix the baseband signal to 1.088GHz. This may be achieved by using the Weaver method and selecting f_1=64MHz and f_2=1.088GHz. The demodulation may be efficiently performed in the digital domain by a simple ± 1 multiply as depicted in Figure 3-20. Since the baseband modulator chip operates at 64MHz, an additional LO is not required to generate f_1. However, the demodulated signal is no longer oversampled by a factor of four, since all odd samples of the in-phase data and all even samples of the quadrature-phase data have been discarded in the baseband modulator chip. The demodulation is equivalent to downsampling the signal by a factor of two, and thus, the effective oversampling ratio of the demodulated baseband signal is just two. The downsampling process is illustrated in Figure 3-21. Due to the lower oversampling ratio, droop introduced by the digital-to-analog converter becomes more significant. A reconstruction filter may be added to compensate for the frequency droop [Lin90].

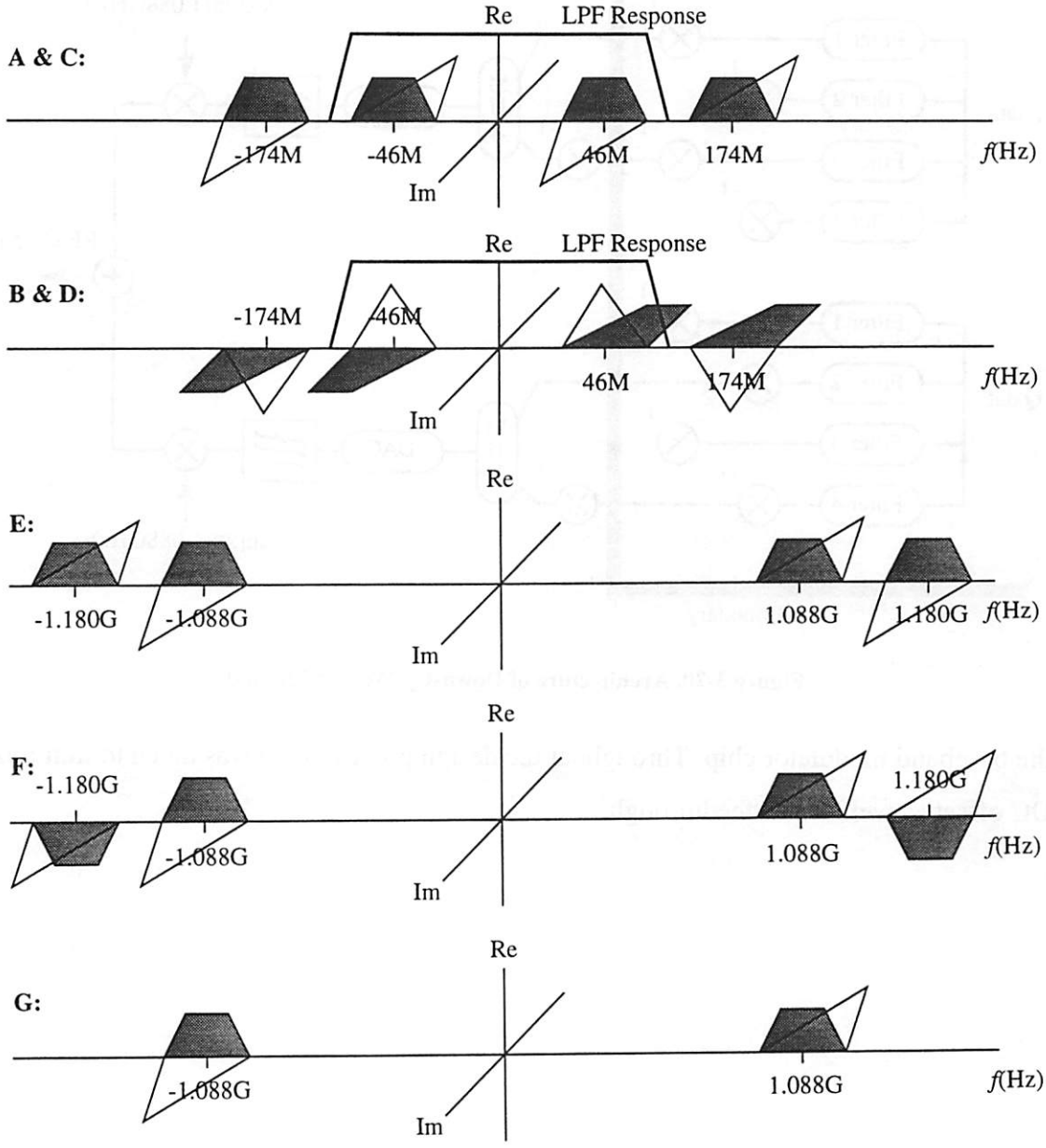


Figure 3-19. Frequency Response at Various Points for Double Upconversion Weaver Method

Although implementation of the down-up Weaver method requires two digital-to-analog converters, each converter operates at 128MHz rather than at 256MHz. Also, since the baseband in-phase and quadrature-phase signals now have spectral energy at DC, carrier feedthrough as well as DC offset become relevant issues. Despite these shortcomings, the down-up Weaver method was selected due to ease of implementation. A practical realization of this method requires the use of only commercially available components and

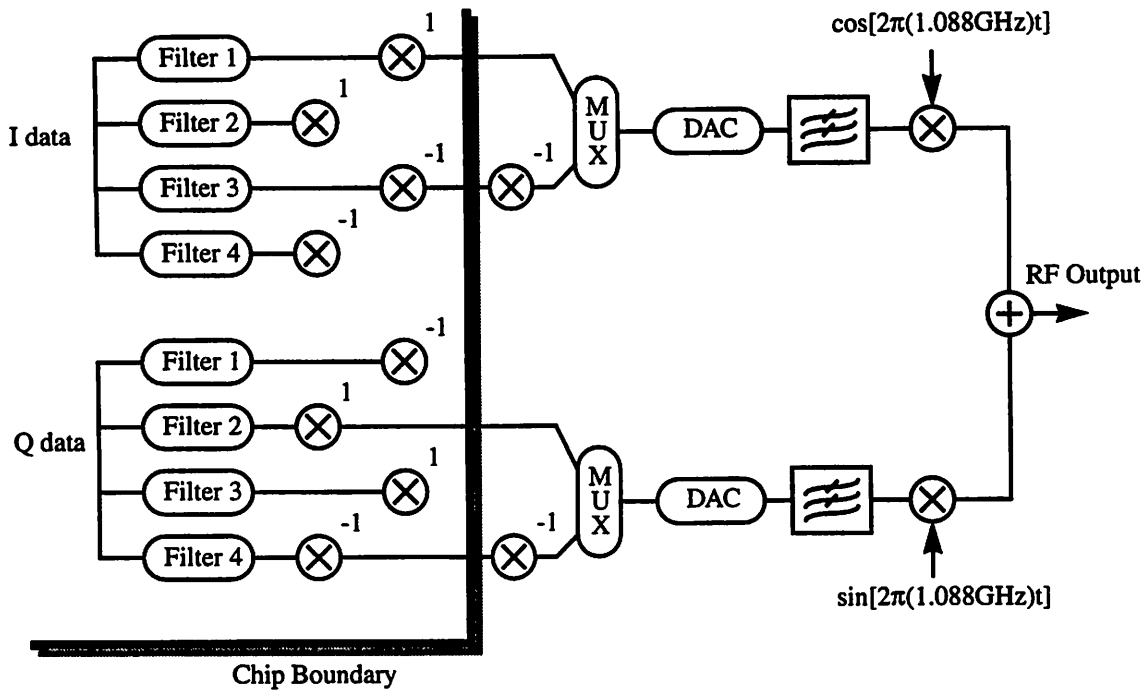


Figure 3-20. Architecture of Down-Up Weaver Method

the baseband modulator chip. Throughout the design process, care was taken to minimize DC offset as well as LO feedthrough.

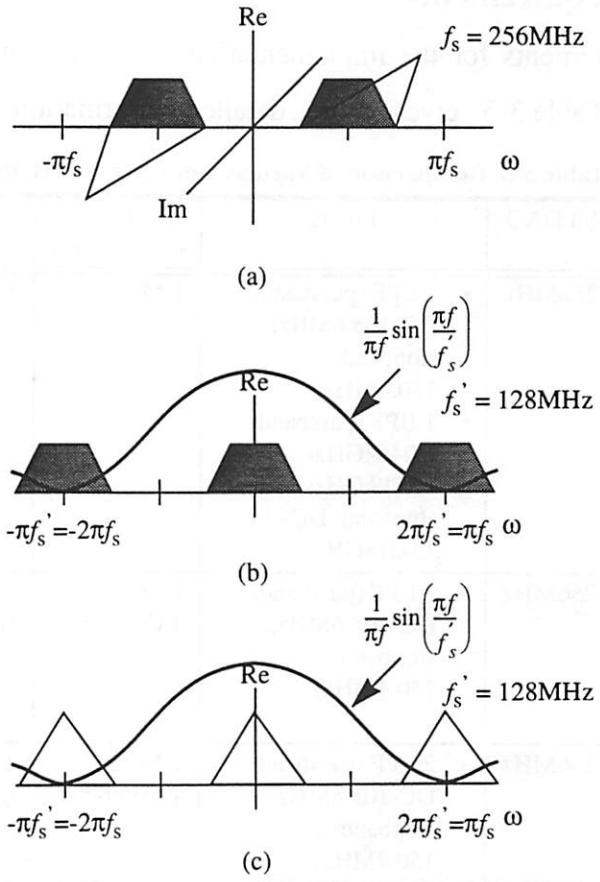


Figure 3-21. Downsampling Process

(a) Output of Baseband Modulator; (b) Downsampled In-Phase Data; (c) Downsampled Quadrature-Phase Data

3.2. Hardware Requirements

The hardware requirements for the implementation of the various methods have been described briefly. Table 3-3 gives more detailed information about the hardware

Table 3-3. Comparison of Various Upconversion Methods

Upconversion Method	10-bit DAC	Filters	RF Components	LO	Other
Filter	1@256MHz	• 1 LPF (passband: DC-105.6MHz; stopband: 150.4MHz) • 1 BPF (passband: 1.0464GHz-1.1296GHz; stopband: DC-1.0016GHz)	1 Mixer	1.024GHz	
Phase-Shift (Analog Hilbert)	1@256MHz	• 1 LPF (passband: DC-105.6MHz; stopband: 150.4MHz)	2 Mixers; 1 Combiner	1.024GHz (I&Q)	Analog Hilbert Transformer: 22.4MHz-105.6MHz
Phase-Shift (Off-Chip Digital Hilbert)	2@256MHz	• 2 LPF (passband: DC-105.6MHz; stopband: 150.4MHz)	2 Mixers; 1 Combiner	1.024GHz (I&Q)	Digital Hilbert Filter @256MHz
Phase-Shift (On-Chip Digital Hilbert)	2@256MHz	• 2 LPF (passband: DC-105.6MHz; stopband: 150.4MHz)	2 Mixers; 1 Combiner	1.024GHz (I&Q)	Requires re-design of baseband modulator chip.
Weaver (Double Upconversion)	1@256MHz	• 1 LPF (passband: DC-105.6MHz; stopband: 150.4MHz) • 2 LPF (passband: DC-87.6MHz; stopband: 132.4MHz)	4 Mixers; 1 Combiner	110MHz (I&Q); 1.134GHz (I&Q)	
Weaver (Down-Up)	2@128MHz	• 2 LPF (passband: DC-41.6MHz; stopband: 86.4MHz)	2 Mixers; 1 Combiner	1.088GHz (I&Q)	

specifications. All implementations but one make use of the existing baseband modulator chip which operates at 64MHz. The phase-shift method which incorporates the Hilbert transform within the baseband modulator chip requires the design of four more raised-cosine subfilters used to generate $I[n]\sin[2\pi n/4]$ and $-Q[n]\cos[2\pi n/4]$. All methods require

the use of multiplexers to combine the parallel output streams from the baseband modulator. However, these multiplexers are not indicated in Table 3-3 since they are not a significant factor in determining the feasibility of an implementation. For the same reason, the inverters required for downsampling in the down-up Weaver method are also not listed.

The filter method as well as the phase-shift method employing an analog Hilbert transformer are impractical due to the need for components which cannot be easily implemented. The former method requires a bandpass filter which provides at least 40dB attenuation within the transition band 1.0016GHz to 1.0464GHz and the latter method requires an analog Hilbert transformer with constant amplitude and phase response from 22.4MHz to 105.6MHz.

The two digital phase-shift methods are almost identical in terms of hardware complexity. The method which requires a digital Hilbert filter external to the baseband modulator chip is less attractive since the Hilbert filter must operate at 256MHz. On the other hand, incorporation of the Hilbert transform within the baseband modulator chip requires the design of four additional sub-filters, all of which operate at only 64MHz. Nevertheless both of these methods require significant time in order to design and fabricate the custom filters.

Implementation of the double upconversion Weaver method requires the largest number of components. The large component count makes this method an unattractive approach.

Finally, the down-up Weaver method is the most simple from an implementation standpoint. Although two digital-to-analog converters are required, each operates at only 128MHz instead of 256MHz. Also, other than the baseband modulator chip, only commercially available components are needed. As long as DC offset and LO feedthrough are carefully controlled, this method is the most viable in the short term of the six methods listed in Table 3-3. Its implementation is discussed in the next chapter.

4 Final Transmitter Design and Implementation

The complete transmitter architecture using the down-up Weaver method is depicted in Figure 4-1. Since the second and fourth ISI subfilters in the in-phase data path and the first

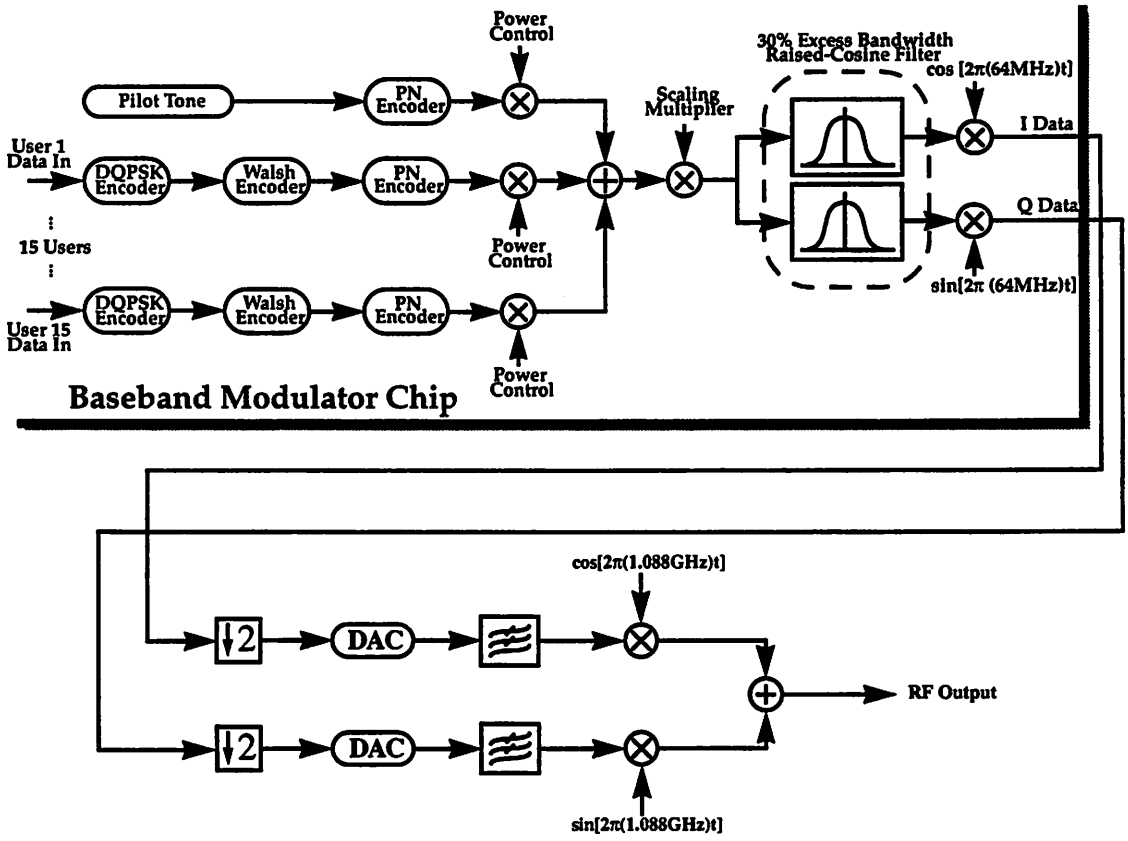


Figure 4-1. Final Transmitter Architecture

and third ISI subfilters in the quadrature-phase data path are not implemented, the IF output data from the baseband modulator chip cannot be demodulated to baseband while

maintaining the original oversampling ratio of four. The IF output data may be demodulated by multiplying both the output of the third in-phase ISI subfilter and the output of the fourth quadrature-phase ISI subfilter by negative one. The resulting baseband signal is effectively oversampled by a factor of two. The outputs from the parallel subfilters use a two's complement number representation, and thus, multiplication by negative one involves bitwise inversion and then addition with one. Bitwise inversion may be easily accomplished by using inverters. Although adding one to the inverted result may seem like a simple operation, actual implementation is hindered by the 64MHz data rate. For example, the output of one subfilter consists of ten 64MHz data bits. In the worst case, adding one to the least significant bit requires "rippling" of the carry across ten bits under 16ns. A critical delay specification of 16ns is difficult to meet when using only commercially available discrete components. This problem may be circumvented simply by not performing the addition operation. However, this hardware simplification comes at the expense of a slight error in the bitwise inverted result. For example, the proposed solution calculates the negative of -512 as 511 instead of 512. For a ten-bit two's complement number system, which represents 2^{10}=1024 values, e.g., integer values from -512 to 511, the proposed solution results in a 0.098% error relative to the total dynamic range. This slight error is very well justified by the resulting hardware savings. Finally, discrete CMOS inverters may be used for the downsampling operation, since typical values of t_{PLH} and t_{PHL} are 4.0ns and 3.5ns, respectively [National93].

Next, the two 64MHz subfilter data streams for the in-phase data are combined to form one 128MHz data stream using discrete CMOS 2-input multiplexers, which have typical delay values of 5.0ns [National93]. The two 64MHz subfilter data streams for the quadrature-phase data are combined to form one 128MHz data stream in a similar way.

Since the high performance digital-to-analog converter requires ECL compatible inputs, a TTL-to-ECL translator is required. Such translators are available as discrete components with a maximum propagation delay of 3.2ns [Motorola93].

The two ECL digital-to-analog converters operate at 128MHz. The two lowpass filters which follow are identical and must have a single-sided passband from DC to 41.6MHz

and at least 40dB of attenuation after 86.4MHz. Lowpass filters with these specifications are commercially available [Mini-Circuits92].

Finally, two mixers are used to directly modulate the baseband in-phase and quadrature-phase signals to an RF center frequency of 1.088GHz. The in-phase data is multiplied by $\cos[2\pi(1.088\text{GHz})t]$ and the quadrature-phase data is multiplied by $\sin[2\pi(1.088\text{GHz})t]$. The two signals are then combined using an RF power combiner before transmission. A power amplifier is not required since only a couple milliwatts of output power is required for transmission in an indoor environment. For matching purposes, it is desirable to use a single chip which incorporates both mixers, the power combiner, and a quadrature generator. Such single chip implementations are available commercially and are called I&Q modulators. One type of I&Q modulator uses Schottky-barrier diodes for mixing. Unfortunately, these I&Q modulators cannot be used since their in-phase and quadrature-phase input frequencies are limited to a range DC to 5MHz [Mini-Circuits92]. A second type of I&Q modulators use Gilbert cell multipliers for mixing and offer much wider bandwidths for in-phase and quadrature-phase input frequencies [Hewlett-Packard93]. Although some modulators incorporate on-chip 90° phase shifters for the LO, these modulators operate correctly for only a specific range of LO frequencies, none of which include the desired RF center frequency. Fortunately, quadrature generation for a small range of frequencies around 1.088GHz may be accomplished using the analog Hilbert transform techniques described in Chapter 3. These techniques are applicable to quadrature LO generation since the input now consists of a single frequency rather than a range of frequencies. Constant phase response is not critical as long as the phase difference between the two outputs for any input frequency is 90°.

4.1. Implementation Procedure

The transmitter is implemented as a printed circuit board consisting of the custom baseband modulator chip and commercially available components. The design process consists of several stages which include schematic entry, component selection, design simulation and verification, as well printed circuit board layout.

4.1.1. Schematic Entry and Component Selection

ViewDraw was used for schematic entry. The schematic with major components annotated is illustrated in Figure 4-2. The schematic is divided into three major sections: digital;

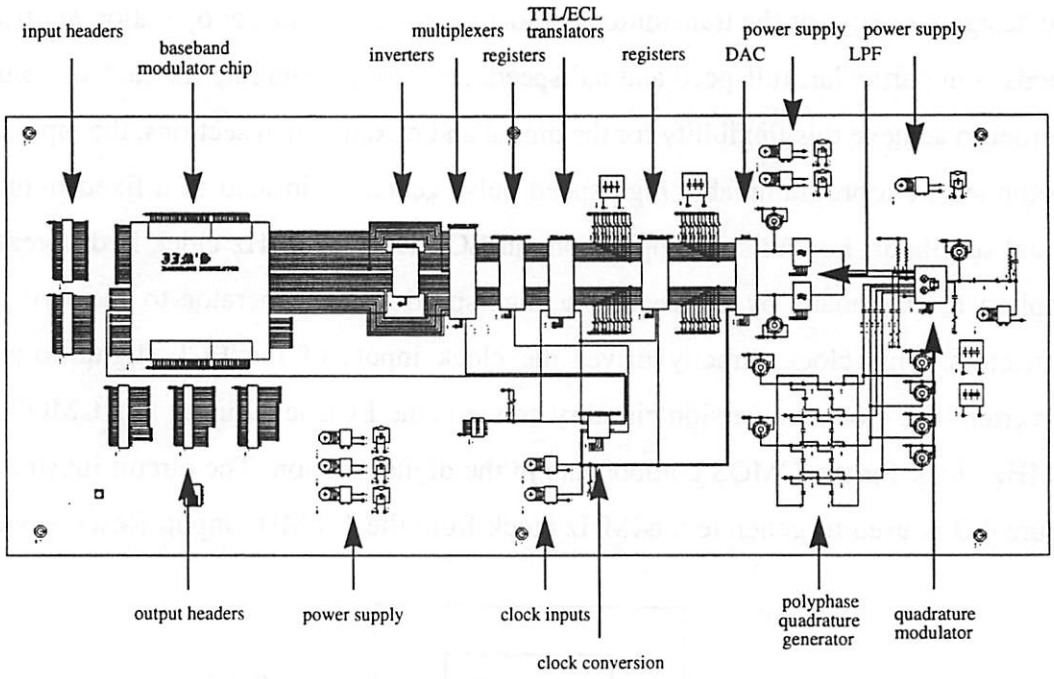


Figure 4-2. *ViewDraw* Schematic of Transmitter

mixed-signal; and analog. The digital section consists of the baseband modulator, inverters, multiplexers, registers, TTL-to-ECL translators, and the clock conversion circuitry. The mixed-signal section consists of the digital-to-analog converter and associated biasing circuitry, and the analog section consists of the lowpass filters and the quadrature modulator. In order to provide clean power supplies to the different sections of the board, each section includes a set of power supply inputs. The digital section has a 5V supply voltage for the CMOS components, and -5V and -2V supply voltages for the ECL components. The mixed-signal section has 5V and -5V supply voltages, and the analog section has one 3V supply voltage.

The input headers allow the baseband modulator to be programmed using a data generation module. In addition, the output of the baseband modulator can be monitored by connecting data acquisition probes to the output headers. The pinout of the input and output headers is

documented in Appendix A and programming of the baseband modulator chip is described in detail in [Peroulas95].

4.1.1.1. System Clocks

The design strategy for the transmitter testboard is to accommodate operation at different speeds -- in particular, fullspeed and halfspeed, i.e., 1Mbps data rate for each of 15 users. In order to achieve this flexibility for the digital and mixed-signal sections, the input clock is supplied by a programmable high-speed pulse generator instead of a fixed-frequency crystal oscillator. For fullspeed operation, an ECL level 128MHz clock is differentially supplied to the board by connecting a high-speed pulse generator to the two SMA connectors. This clock directly drives the clock inputs of the ECL digital-to-analog converter. The clock conversion circuitry converts the ECL level input to a CMOS level 64MHz clock for the CMOS components in the digital section. The circuit illustrated in Figure 4-3 is used to generate a 64MHz clock from the 128MHz input. Reset as well as

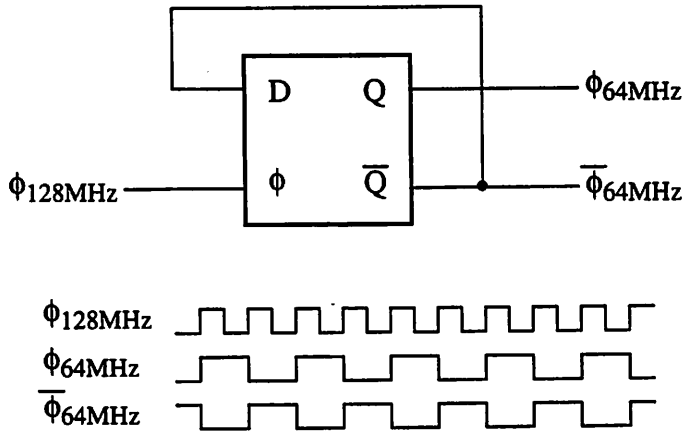


Figure 4-3. Generation of 64MHz Clock

selection of ϕ_{64MHz} or $\overline{\phi}_{64MHz}$ are provided by two dip switches.

4.1.1.2. Digital-to-Analog Converter

The input coding used by the digital-to-analog converter (AD9720) is offset binary. However, the output data from the baseband modulator chip uses a two's complement number representation. The mapping between offset binary and two's complement is

two's complement	offset binary
0111111111	1111111111
0111111110	1111111110
⋮	⋮
1000000001	0000000001
1000000000	0000000000

Figure 4-4. Conversion from Two's Complement to Offset Binary

illustrated in Figure 4-4. Conversion from two's complement to offset binary simply requires complementing the MSB. This operation is combined with the downsampling operation and uses the same set of inverters at the output of the baseband modulator chip.

The current output of the digital-to-analog converter must be converted to a voltage for subsequent stages. The desired voltage output swing is about 2V, centered at ground. The conversion technique uses the AD9617 operational amplifier in a current feedback mode is illustrated in Figure 4-5 [Analog Devices94]. The following equation relates V_o to I_{DAC}

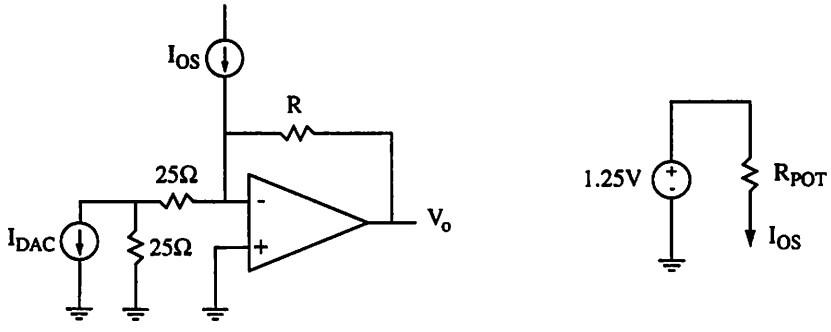


Figure 4-5. Current-to-Voltage Conversion

and I_{OS}:

$$V_o = \frac{I_{DAC}}{2}R - I_{OS}R$$

The first term represents the output swing and the second term represents the offset voltage. I_{DAC} varies between 0mA and 20.48mA and the desired voltage output swing is 2V. Solving for R in the first term of the above equation results in R=195Ω. Selecting

R=200Ω results in a voltage output swing of 2.048V. In order to determine I_{OS} for the output voltage to be centered at ground, the second term is equated to 1.024V. The corresponding offset current is 5.12mA. This offset current is generated using the DAC reference voltage of 1.25V and a resistor. Ideally, without the presence of offset voltages, the value of this resistor is 244Ω. As mentioned earlier, DC offsets and LO feedthrough must be carefully controlled when implementing the up-down Weaver method. The ability to adjust the bias voltages of the in-phase and quadrature-phase data is crucial for two reasons:

1. Tuning out the input offset voltage of the AD9617 operational amplifier, and
2. Improving the LO rejection of the quadrature modulator [Hewlett-Packard93].

For R=200Ω,

$$V_o = 100I_{DAC} - 200I_{OS} + 5V_{OS}$$

where V_{OS} is the input offset voltage off the AD9617 operational amplifier. Also,

$$I_{OS} = \frac{1.25 - V_{OS}}{R_{POT}}$$

where R_{POT} is a variable resistance. Thus,

$$V_o = 100I_{DAC} - \frac{250}{R_{POT}} + V_{OS}\left(5 + \frac{200}{R_{POT}}\right)$$

In the above equation, the first term represents the voltage swing and the two subsequent terms represent the bias voltage. In order to determine the range of R_{POT} for tuning out the

input offset voltage of the amplifier as well as for minimizing the LO leakage in the quadrature modulator, the following equation must be considered:

$$\frac{250}{R_{POT}} - V_{OS}\left(5 + \frac{200}{R_{POT}}\right) = 1.024V + V_{MOD}$$

where V_{MOD} is the DC imbalance at the mixer inputs of the quadrature modulator. The input offset voltage of the AD9617 operational amplifier ranges from -1.1mV to 2.2mV and values of V_{MOD} range from -56mV to 56mV. The calculated range of R_{POT} is 228Ω to 260Ω. In the final design, R_{POT} consists of one 100Ω fixed resistor in series with a multiturn 200Ω trimmer potentiometer for increased resolution.

4.1.1.3. Lowpass Filter

As mentioned earlier, it is desirable to design the transmitter testboard to accommodate various speeds. Unfortunately, the lowpass filters following the digital-to-analog converters are fixed-tuned to a particular operating frequency. Thus it is important to select a component model which offers several different frequency responses in packages with the same footprint and the same pin connections.

4.1.1.4. Quadrature Modulator

The HPMX-2001 QPSK modulator [Hewlett-Packard93] provides the greatest flexibility for upconversion. The modulator includes two Gilbert cell mixers and a power combiner. The typical I/Q bandwidth is DC to 700MHz and the typical LO operating frequency range is DC to 2000MHz. Unfortunately, the modulator does not provide an on-chip 90° phase shifter. The HPMX-2001 modulator is specified to operate at a 5V supply voltage and requires the in-phase and quadrature-phase inputs to be DC biased at 2.5V. However, the output voltages from the digital-to-analog converters are centered at ground. There are three possible solutions:

1. AC couple the input signals and provide the 2.5V DC bias directly,

2. Set the DC bias of the output voltages from the digital-to-analog converters at 2.5V and DC couple the input signals, or
3. Operate the HPMX-2001 modulator at a supply voltage of 2.5V instead of 5V and at a reference voltage of -2.5V instead of ground, set the DC bias of the output voltages from the analog-to-digital converters at 0V, and DC couple the input signals.

One disadvantage of the first alternative is that it requires another tuning circuit for the 2.5V bias voltage so that the input voltages may be adjusted to improve LO rejection. However, the major disadvantage of this method is that the capacitive coupling compromises the integrity of the input signals. A large coupling capacitor is desirable to minimize the loss of spectral energy near DC. However, a large coupling capacitor also has a low self-resonance frequency which may be problematic for passing high frequency components of the spread-spectrum signal. A small coupling capacitor, on the other hand, eliminates the spectral energy near DC.

The second method also requires a tuning circuit to adjust the 2.5V DC bias of the input signals. However, the circuit used to tune out the input offset voltage of the AD9617 operational amplifier can be modified to generate the 2.5V DC bias as well as provide tuning capability to improve LO rejection. The problem with this method is the limited output voltage range of the AD9617 amplifier. The in-phase and quadrature-phase data must swing ±1.024 V centered at 2.5V + V_{MOD}. Since V_{MOD} is between -56mV and 56mV, the maximum voltage which may appear at the output of the AD9617 amplifier is 3.58V. However, the worst-case output voltage range of the AD9617 amplifier is ±3.4 V for ±5 V supply voltages. One solution is to use a larger absolute supply voltage for the AD9617 amplifier, which is specified to have a maximum supply voltage rating of ±7 V, to increase the output voltage swing capability. Although the second method is a viable solution, nevertheless, the third method is slightly easier to implement.

For the third method, the tuning network used to tune out the input offset voltage of the AD9617 amplifier can also be used without modification to adjust the offset voltage of the quadrature mixers. Since the voltage output swing is centered at 0V, the quadrature modulator must operate at a supply voltage of 2.5V instead of 5V and at a reference voltage of -2.5V instead of ground. One disadvantage to this method is the need to generate two

additional bias voltages. However, only one additional supply voltage of 3V is necessary if the -2V supply from the digital ECL section is used as the reference voltage for the quadrature modulator chip. For this case, the input voltages must be centered at 0.5V instead of ground. The bias configuration for the HPMX-2001 is illustrated in Figure 4-6.

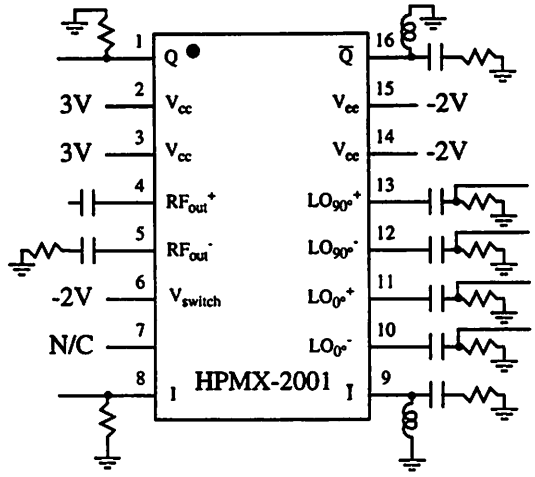


Figure 4-6. Current-to-Voltage Conversion

All capacitors are 200nF and all resistors are 50Ω. Single-ended configurations are used for the in-phase and quadrature-phase input signals as well as the RF output signal. The in-phase and quadrature-phase input signals are DC coupled to I^+ and Q^+, respectively. The inductors at I and Q are air-coil inductors. At DC, these inductors appear as low impedances and the capacitors appear as high impedances, thus providing a 0V DC bias to the I and Q input ports. At high frequencies, the inductors appear as high impedances and the capacitors appear as low impedances, thus providing the necessary 50Ω termination. The clock inputs are AC coupled and terminated to 50Ω. The clock inputs are configured for both differential and single-ended operation. Single-ended operation is achieved by using only $LO_{0°}{}^+$ and $LO_{90°}{}^+$. The RF output is configured for single-ended operation. $RF_{out}{}^-$ is terminated to 50Ω and $RF_{out}{}^+$ is AC coupled to a 50Ω load such as the input to a spectrum analyzer or an antenna.

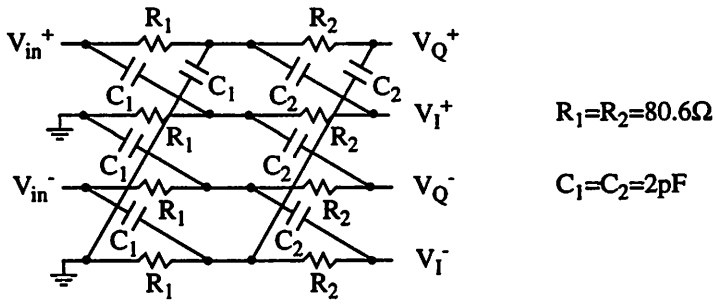
4.1.1.5. Quadrature Clock Generation

The RF LO is provided by a high frequency sinusoidal wave generator. This input LO is programmable in order to accommodate operation of the transmitter at different data rates. For example, at fullspeed the carrier frequency is 1.088GHz and at halfspeed the carrier frequency is 1.056GHz. The carrier frequency must be selected in order to satisfy the sampling-demodulation requirement at the receiver [Sheng96]. Differential quadrature clock generation is accomplished by using a two-stage asymmetric polyphase network as illustrated in Figure 4-7. SPICE plots of the amplitude and phase differences between in-phase and quadrature-phase LO outputs are also illustrated for $C_1=C_2=2pF$ and $R_1=R_2=80.6\Omega$. Between 800MHz and 1.2GHz, the amplitude imbalance is less than 23mV and the phase mismatch from 90° is less than 1.7°. However, in order to verify correct operation of the quadrature clock generator, component parasitics as well as tolerances must be accounted for in the SPICE simulation. The capacitor has a ±12.5 % tolerance and the resistor has a ±1 % tolerance. The circuit used to model the parasitics associated with discrete capacitors and resistors is shown in Figure 4-8. SPICE simulations indicate a worst-case 50mV amplitude mismatch and a worst-case 2.35° phase mismatch from 90°.

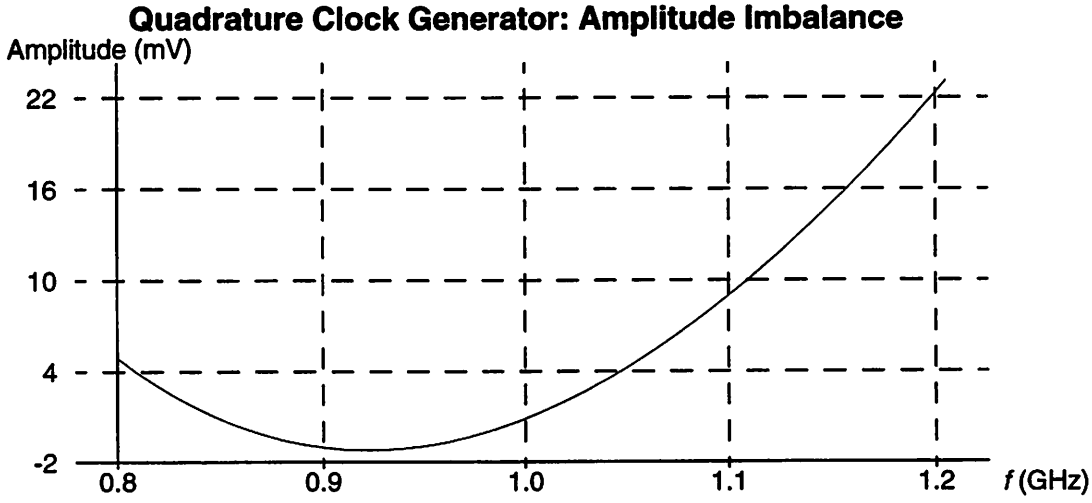
Finally, an additional set of OSMT connectors are provided for both signal observation and injection. These connectors may be used to observe the outputs of the asymmetric polyphase network. An external quadrature clock generator may also be injected at this point as long as the polyphase network is disabled.

4.1.1.6. Emission Masking

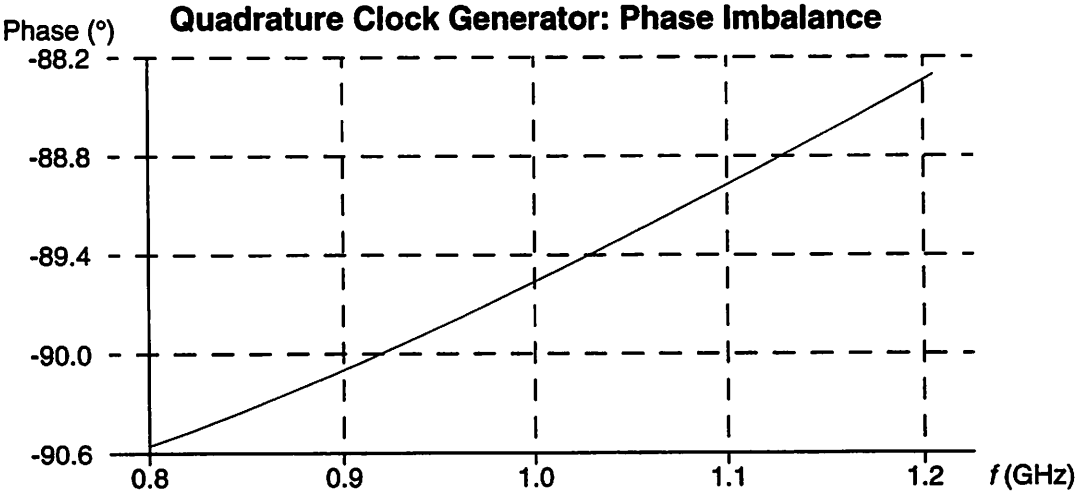
Before transmission, the modulator output must be bandpass filtered to eliminate out-of-band frequency components. These components arise from nonlinearities in the mixers. A standard RLC bandpass filter as depicted in Figure 4-9 is sufficient for emission masking. Alternatively, an external bandpass filter may be inserted at the OSMT probe point directly following the modulator output.



(a)



(b)



(c)

Figure 4-7. Differential Quadrature Clock Generator

(a) Asymmetric Polyphase Network; (b) Amplitude Imbalance; (c) Phase Imbalance

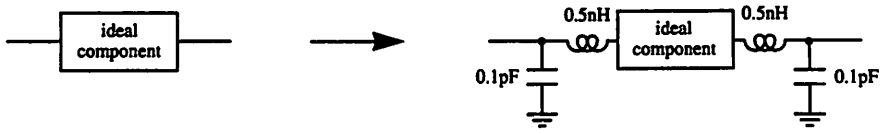
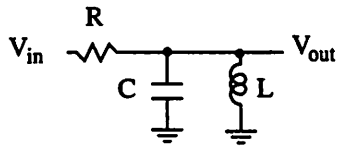


Figure 4-8. Modeling Parasitics in Discrete Components



$$\frac{V_{out}}{V_{in}} = \frac{s\left(\frac{1}{RC}\right)}{s^2 + s\left(\frac{1}{RC}\right) + \frac{1}{LC}}$$

Figure 4-9. RLC Bandpass Filter

4.1.1.7. Surface Mount Components

Surface mount components are used in preference to through-hole components. First, surface mount packages have significantly lower values of resistance, capacitance and inductance compared to dual in-line packages (DIP). Minimizing package parasitics is crucial for high speed designs. In addition, surface mount components are significantly smaller than their corresponding through-hole components.

Finally, type 0603 surface mount resistors and capacitors are used for efficient area utilization. However, for the ECL components, type 0805 resistors are used for the 50Ω output termination to -2V. Type 0805 resistors have a higher power rating which is required to sink the output current from the ECL components.

4.1.2. Design Simulation and Verification

Design simulation and verification of correct functionality are important for efficient implementation of the transmitter testboard. Using *ViewDraw* for schematic entry allows the digital section of the design to be simulated using *ViewSim*. Unfortunately, the analog section cannot be simulated so easily.

VHDL models which include behavioral as well as timing information were used to simulate the functionality of the digital section, excluding the baseband modulator chip.

Table 4-1 summarizes the expected results appearing at the input to the digital-to-analog converter for the following baseband modulator output data: *I1OUT*=0x2B3, *I2OUT*=0x06A, *Q1OUT*=0x32B, and *Q2OUT*=0x2B2. Simulation results for an input

Table 4-1. Expected Simulation Results

data	I1OUT=0x2B3	I2OUT=0x06A	Q1OUT=0x32B	Q2OUT=0x2B2
binary	1010110011	0001101010	1100101011	1010110010
bit inverse	N/A	1110010101	0011010100	N/A
MSB toggle	0010110011	0110010101	1011010100	0010110010
output	0x0B3	0x195	0x2D4	0x0B2

clock rate of 128MHz are plotted in Figure 4-10. The *ViewSim* simulation verifies that the

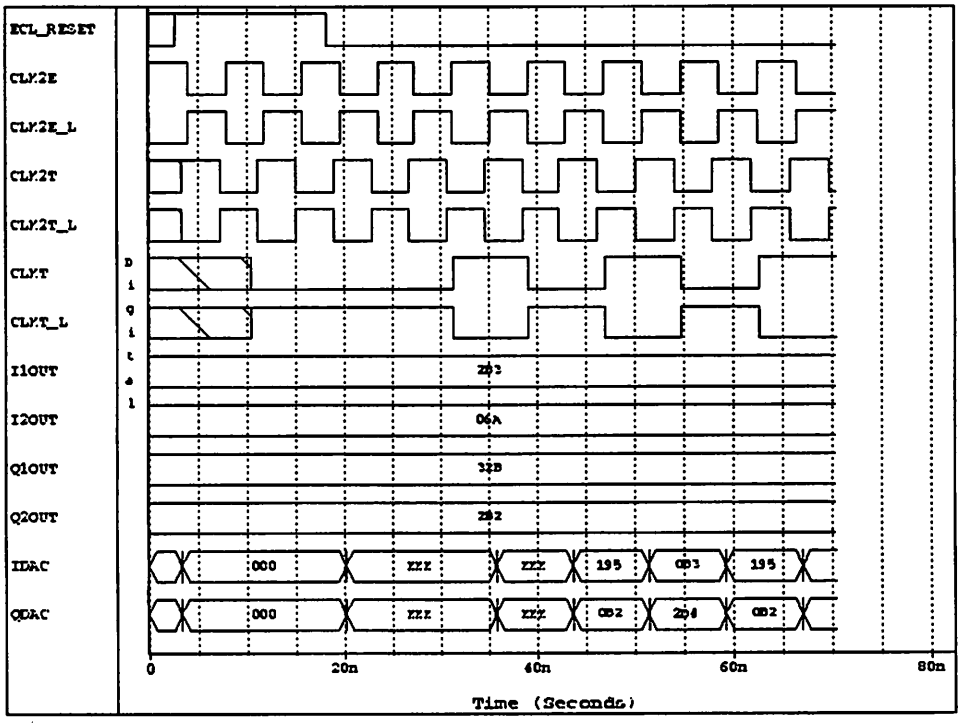


Figure 4-10. *ViewSim* Simulation of Digital Section

digital section of the transmitter testboard is indeed functioning as intended. The data appearing at the input to the digital-to-analog converter are labeled *IDAC* and *QDAC*.

4.1.3. Printed Circuit Board Layout

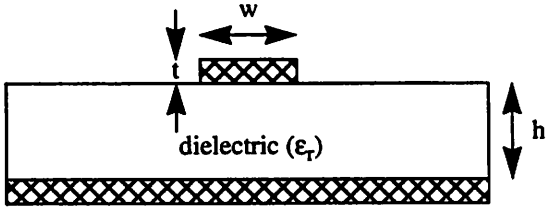
After completing the design in *ViewDraw* and verifying correct functionality using *ViewSim*, the next step was to create a printed circuit board using a layout editor called *Racal*. Designing the printed circuit board in *Racal* involves three major steps:

1. Placement of circuit components,
2. Creating interconnections between components, and
3. Replacing interconnections with physical routes.

Since the circuit components as well as their interconnections have already be entered into *ViewDraw*, it would be highly inefficient for the process to be repeated in *Racal*, especially since correct functionality has already been verified. Placement information as well as component package types were annotated on the *ViewDraw* schematic and the *OCT* tools were used to generate a *Racal* input file which preserves information about placement of components as well as the interconnections between them. Thus, the process required to create the printed circuit board was tremendously simplified.

4.1.3.1. Routing

The symbolic interconnections between components must be replaced with physical routes. All ECL and RF components are interconnected using 50Ω traces in order to minimize signal reflection. Only the component and solder sides are used for these traces so that all traces appear as microstrip lines. A microstrip line is illustrated in Figure 4-11.



$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

Figure 4-11. Characteristic Impedance of a Microstrip Line

The equation for the characteristic impedance of a microstrip line is accurate for $0.1 \le \frac{w}{l} \le 3.0$ and for $1 \le \varepsilon_r \le 15$. The testboard is fabricated with an interlayer spacing

of h=0.008". Routing on the component side and solder side layers consists of 1/2oz. copper with a thickness t=0.0007". All other layers use 1oz. copper with a thickness of 0.0012". The insulating material has a relative dielectric constant of ε_r=4.3. In order to achieve a characteristic impedance of 50Ω for routes on the component side and solder side layers, a trace width of 0.015" is required. All interconnections for ECL and RF components, including analog and digital clock lines, were manually routed. These signal lines were kept as short as possible in order to minimize propagation delay as well as ringing and overshoot. Interconnections for the digital components were routed using *Racal*'s auto-router with 0.008" trace widths.

4.1.3.2. Other Issues

Split power and ground planes are used in order to minimize cross talk between the three sections of the testboard. Power supply noise is minimized using 1000μF electrolytic bypass capacitors. In addition, surface mount bypass capacitors are generously placed throughout the testboard. The digital and mixed-signal sections use 1nF bypass capacitors whereas the analog section uses 10nF bypass capacitors.

The final layer specification is given in Table 4-2. A balanced layer specification is used

Table 4-2. Final Layer Specification

layer 1	component
layer 2	power plane (GND)
layer 3	power plane (VTT)
layer 4	route1
layer 5	route2
layer 6	power plane (VEE)
layer 7	power plane (VDD)
layer 8	solder

to minimize the possibility of warping after construction. The two routing layers are placed at the center with the power planes symmetrically placed on the surrounding layers. The actual layer ordering is specified during fabrication and does not need to be explicitly entered into *Racal*. The final testboard has dimensions 14120mils x 4660 mils. The layout is illustrated in Figure 4-12.

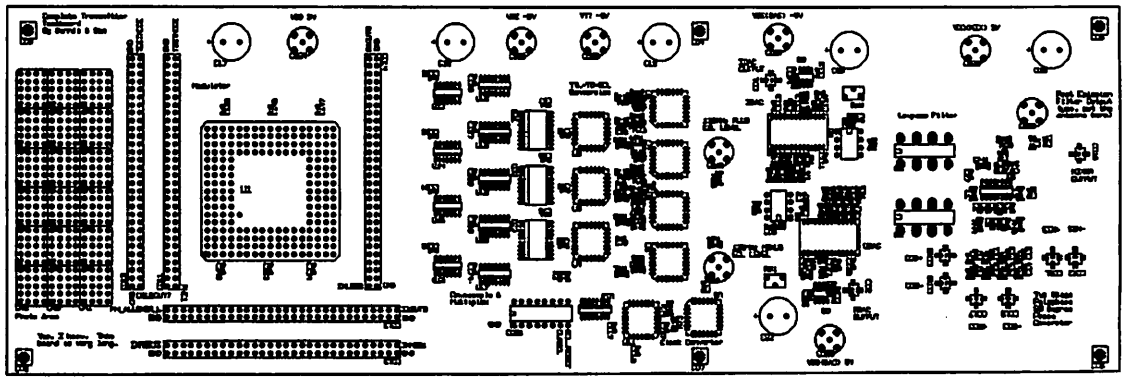


Figure 4-12. Transmitter Testboard Layout

5 Testing and Measurements

Initial functional testing was performed at halfspeed with an input clock rate of 64MHz for the digital-to-analog converter and 32MHz for the baseband modulator chip. Tektronix's Digital Analysis System was used to program the baseband modulator chip as well as acquire output data from the ISI filters. A 64MHz ECL level (-2V to 0V) input clock is generated using Hewlett-Packard's high speed pulse generator, HP8131A. The spectral outputs at baseband and at RF were observed on a spectrum analyzer. Although a few bugs were discovered, they were all amendable, and the baseband modulator chip and the transmitter testboard were found to be fully functional.

5.1. Verification of Correct Functionality

Several measurements were made in order to verify that the transmitter is operating correctly. All measurements presented in this section were performed at halfspeed.

5.1.1. Eye Diagram

An eye diagram graphically illustrates all possible intersymbol interference waveforms [Lee94]. The theoretical eye diagram corresponding to a 37-tap raised-cosine filter with 30% excess bandwidth is illustrated in Figure 5-1. A closed eye diagram indicates the presence of intersymbol interference. Since all traces pass through +1 or -1 at the center of the eye, the condition of no intersymbol interference is satisfied. In particular, a larger vertical opening indicates a greater immunity to noise. Thus, the ideal sampling instant is at time T, when the vertical eye opening is maximum. However, due to phase offsets between the clocks used in the transmitter and the receiver, the signal can never be sampled precisely at T. Thus, a larger horizontal eye opening is desirable for increased immunity to errors in timing phase.

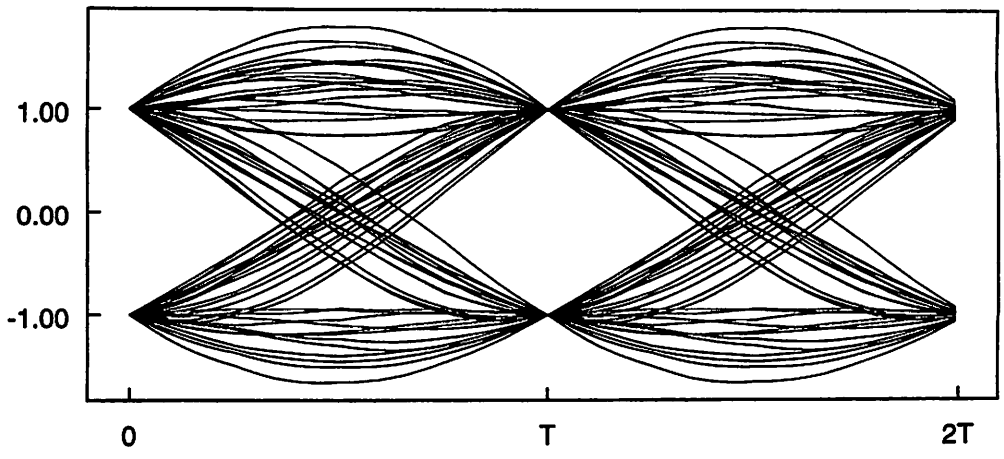
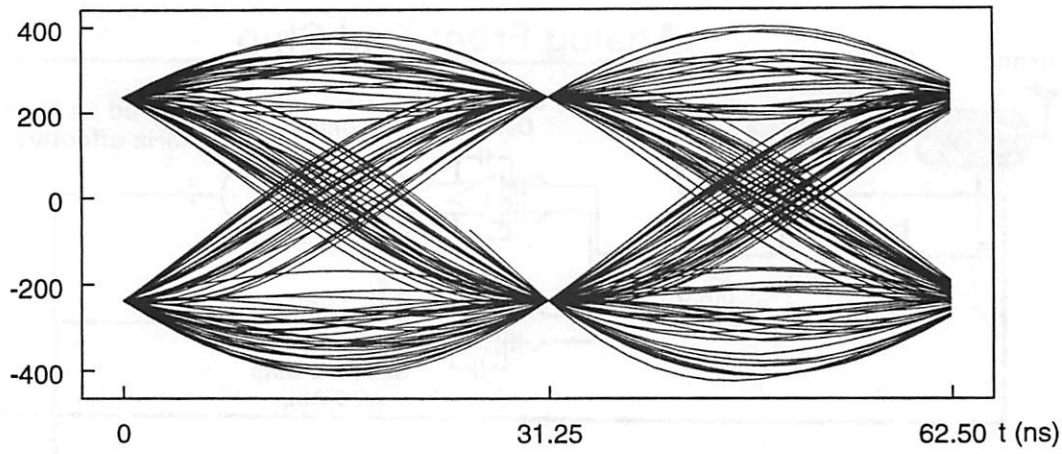


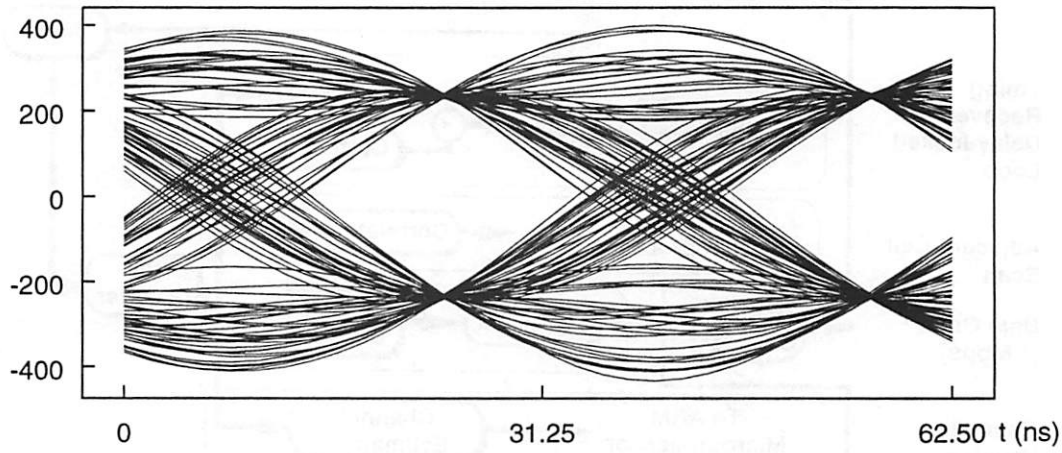
Figure 5-1. Theoretical Eye Diagram for 37-Tap 30% Excess Bandwidth Raised-Cosine Filter

The digital output from the baseband modulator chip was acquired and processed in *Ptolemy* to generate eye diagrams for both the in-phase and quadrature-phase data streams. The results are illustrated in Figure 5-2. The output data streams from the baseband modulator chip satisfy the zero intersymbol interference condition. The eye diagrams for the in-phase and quadrature-phase data streams are similar except for a phase shift of 7.8125ns, which corresponds to exactly T/4. Recall that the baseband modulator chip digitally modulates the in-phase and quadrature-phase data streams by $\sin[2\pi n/4]$ and $\cos[2\pi n/4]$, respectively. Hence the two output data streams are offset by exactly T/4, as evident in the measured eye diagrams.

In order to verify correct transmission and demodulation of the RF signal, an eye diagram is generated from the analog-to-digital converter output of the analog front-end receiver chip. A block diagram of the receiver is illustrated in Figure 5-3. All clocks in the system were synchronized in order to perform this measurement without using the baseband receiver chip for clock recovery. The result is illustrated in Figure 5-4. The analog-to-digital converter quantizes the demodulated signal to four bits using a sign-magnitude number representation. Since all traces pass through +7 or -7 at the center of the eye, the condition of no intersymbol interference is satisfied. This eye diagram verifies that the transmitter output signal is indeed correct.



(a)



(b)

Figure 5-2. Measured Eye Diagrams at the Transmitter

(a) In-Phase Data; (b) Quadrature-Phase Data

5.1.2. Spectral Outputs

At halfspeed, the theoretical spectral response of an ideal 30% excess bandwidth raised-cosine filter with an oversampling ratio of two is illustrated in Figure 5-5. Quantization of tap values as well as internal filter values are not accounted for in this filter response.

The spectral outputs of the in-phase and quadrature-phase data are obtained by applying the fast Fourier transform to the baseband modulator output data. The measured frequency responses are illustrated in Figure 5-6. The measured frequency responses of both in-phase and quadrature-phase data streams satisfy the 40dB out-of-band rejection requirement. The

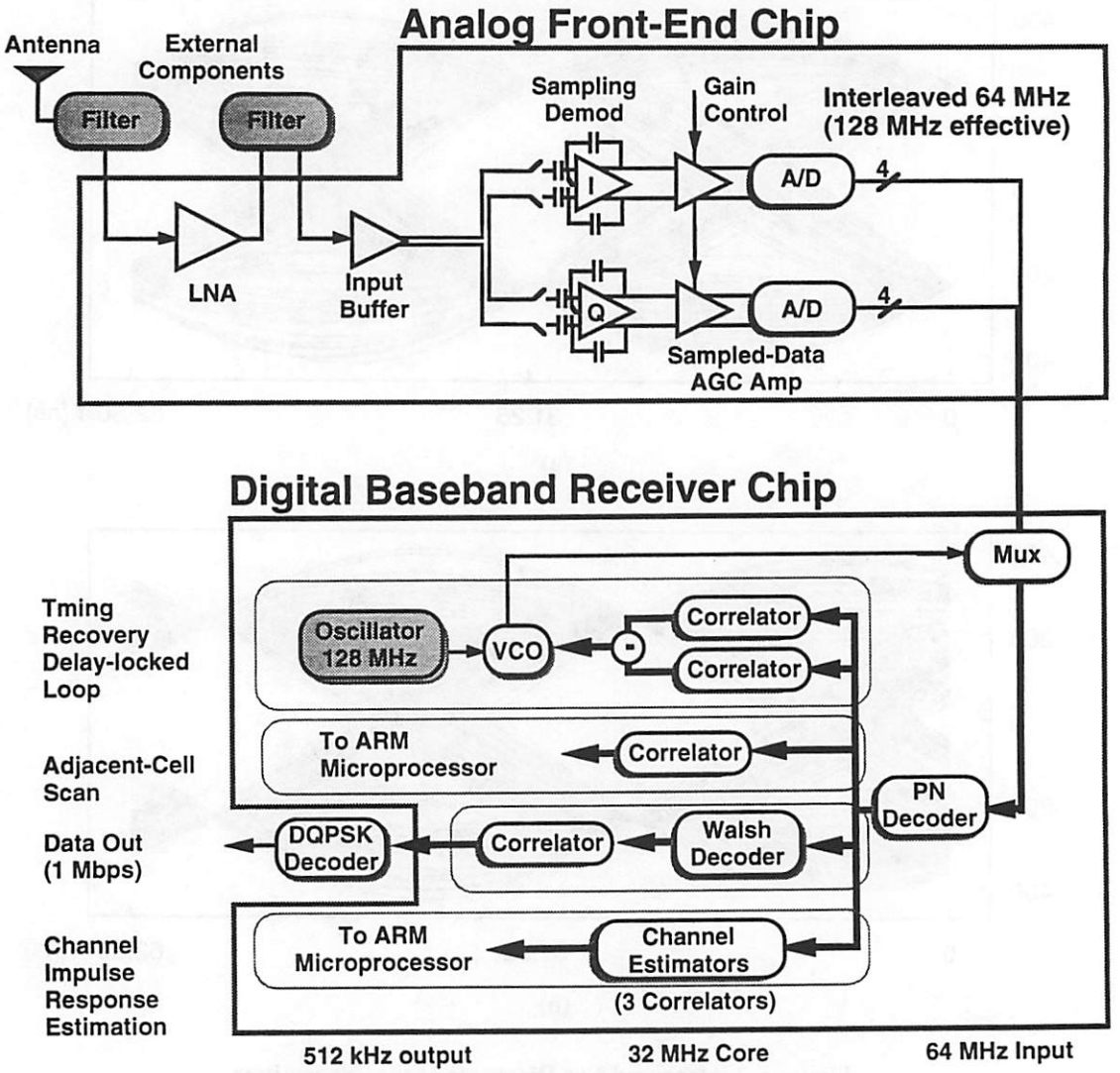


Figure 5-3. Receiver Architecture

spectral outputs are not exactly identical to the one illustrated in Figure 5-5 due to numerical quantization in practical implementations.

Both spectral outputs have a single-sided bandwidth of about 21MHz, and thus, satisfy the 30% excess bandwidth specification. At halfspeed, a 0% excess bandwidth filter results in a single-sided bandwidth of 16MHz. Correspondingly, a 30% excess bandwidth filter results in a single-sided bandwidth of 20.8MHz. In addition, both filter outputs are spectrally white as required for spread-spectrum communications.

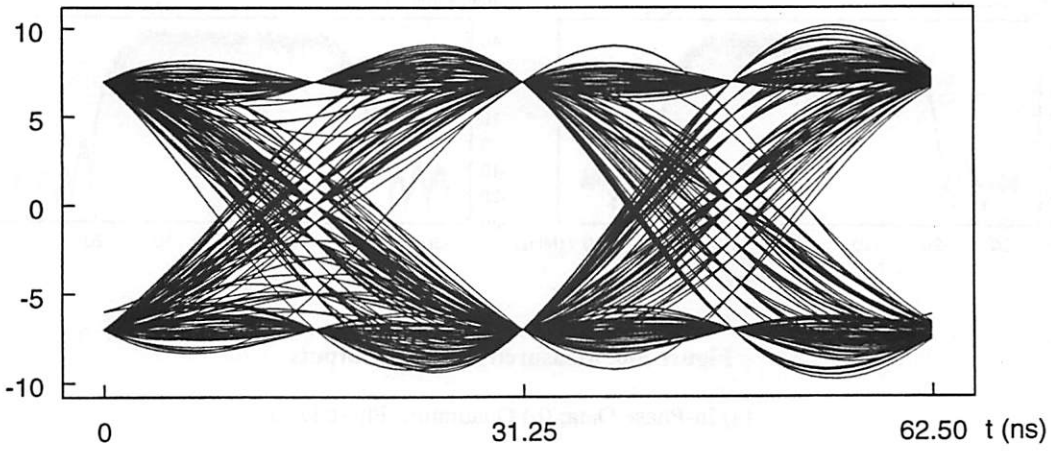


Figure 5-4. Measured Eye Diagram at the Receiver

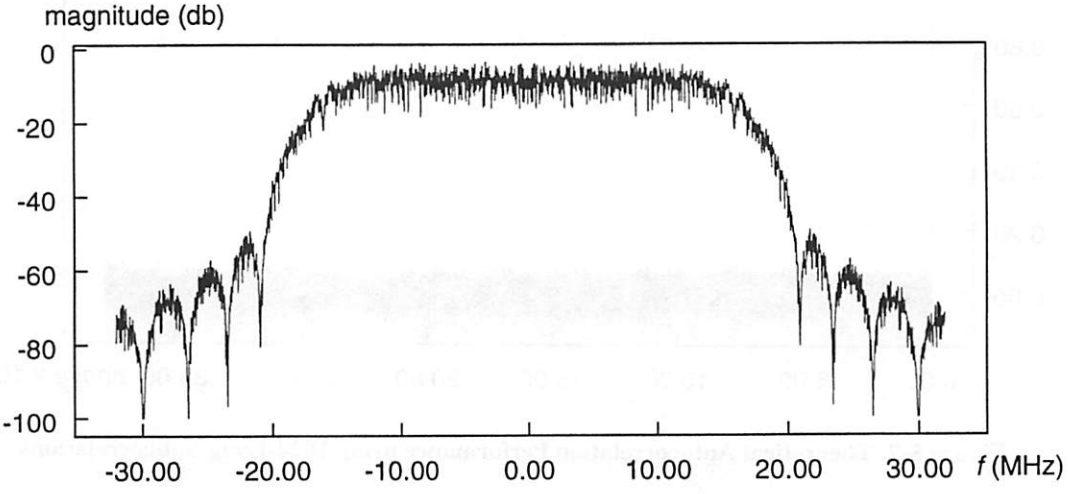


Figure 5-5. Theoretical Frequency Response for 37-Tap 30% Excess Bandwidth Raised-Cosine Filter without Quantization

5.1.3. Autocorrelation Performance

A 32768-long PN sequence is used for spectral whitening. This sequence is generated using a 32768-long subsequence of a 16-bit maximal-length shift register (MSLR) sequence. The MLSR is initialized with the seed 0x1154 and terminates with 0xFFFF. The receiver synchronizes the received data with an identical 32768-long PN sequence by correlating over 1024-long subsequences. The autocorrelation performance using 1024-long subcorrelations is illustrated in Figure 5-7. When the PN sequences are perfectly

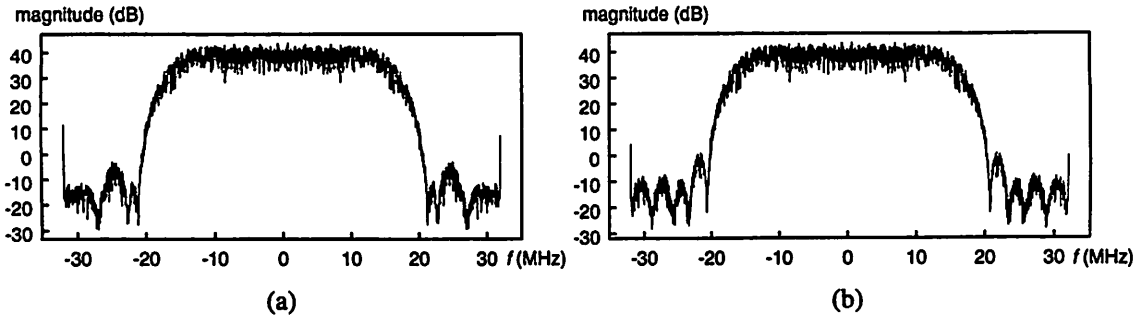


Figure 5-6. Measured Spectral Outputs

(a) In-Phase Data; (b) Quadrature-Phase Data

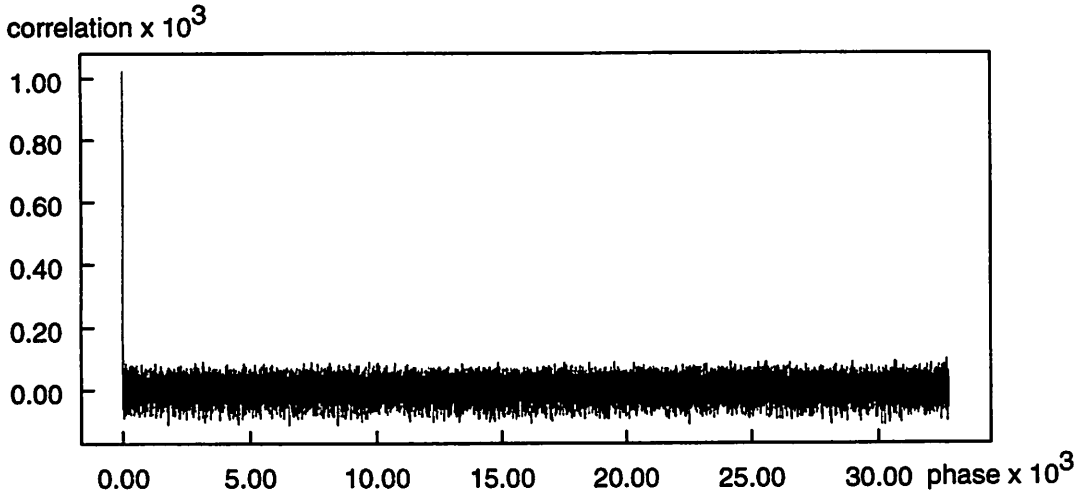


Figure 5-7. Theoretical Autocorrelation Performance using 1024-Long Subcorrelations

aligned, the correlation value is 1024 as expected. For all other phase offsets of the PN sequences, the correlation values are at least 20dB below the correlation peak.

The transmitter uses a 30% excess bandwidth 37-tap raised-cosine filter with an oversampling factor of four. As previously mentioned, this raised-cosine filter may be divided into four separate subfilters with tap coefficients as illustrated in Figure 5-8. Correlation with the output data from the third subfilter results in the autocorrelation performance illustrated in Figure 5-7. The single correlation peak corresponds to the maximum point of the raised-cosine pulse. Theoretical autocorrelation performance curves for the other three subfilters are illustrated in Figure 5-9. The region around the correlation

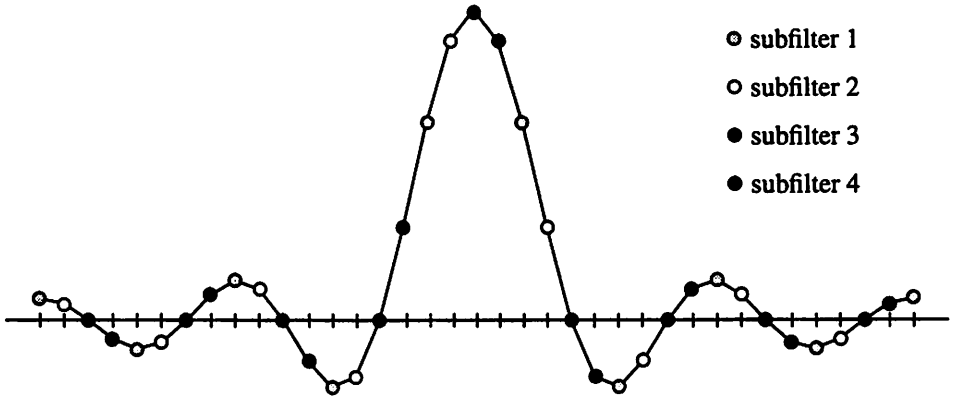


Figure 5-8. Truncated Raised-Cosine Pulse

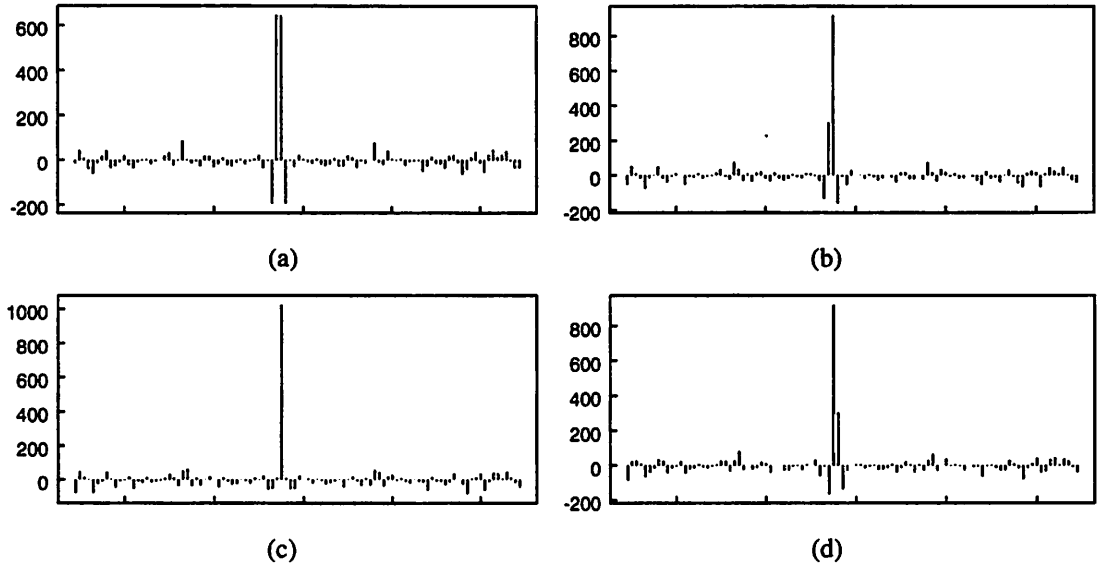


Figure 5-9. Theoretical Autocorrelation Performance using 1024-Long Subcorrelations

(a) Subfilter 1; (b) Subfilter2; (c) Subfilter 3; (d) Subfilter 4

peaks is enlarged for each curve. As expected, the four subfilters all have correlation peaks corresponding to the sampling instances illustrated in Figure 5-8.

The measured autocorrelation performance of the output data from the baseband modulator chip is illustrated in Figure 5-10. The raised-cosine filters for the in-phase and quadrature-phase data each consists of only two subfilters resulting from digital modulation by $\cos[2\pi n/4]$ and $\sin[2\pi n/4]$, respectively. The measured autocorrelation performance of the output data agrees well with the theoretical performance.

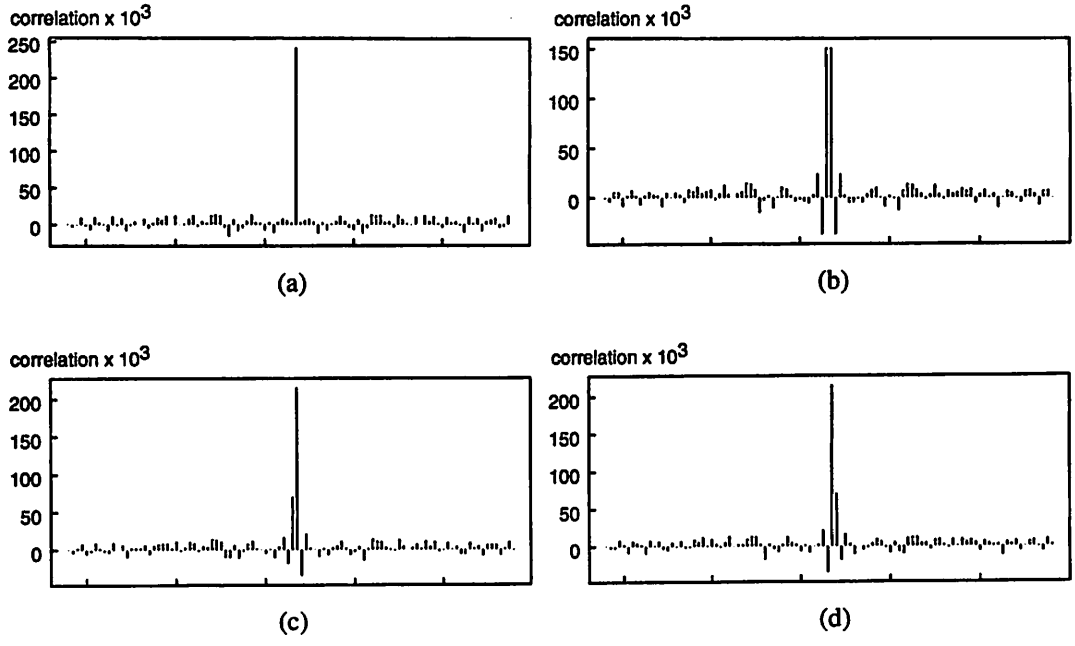


Figure 5-10. Measured Autocorrelation Performance at the Baseband Modulator Output using 1024-Long Subcorrelations

(a) In-Phase Data Subfilter 1; (b) In-Phase Data Subfilter 2; (c) Quadrature-Phase Data Subfilter 1; (d) Quadrature-Phase Data Subfilter 2

Figure 5-11 illustrates the measured autocorrelation performance of the data at the output of the analog receiver chip. The correlation peak occurs at a PN phase offset of 18464 and

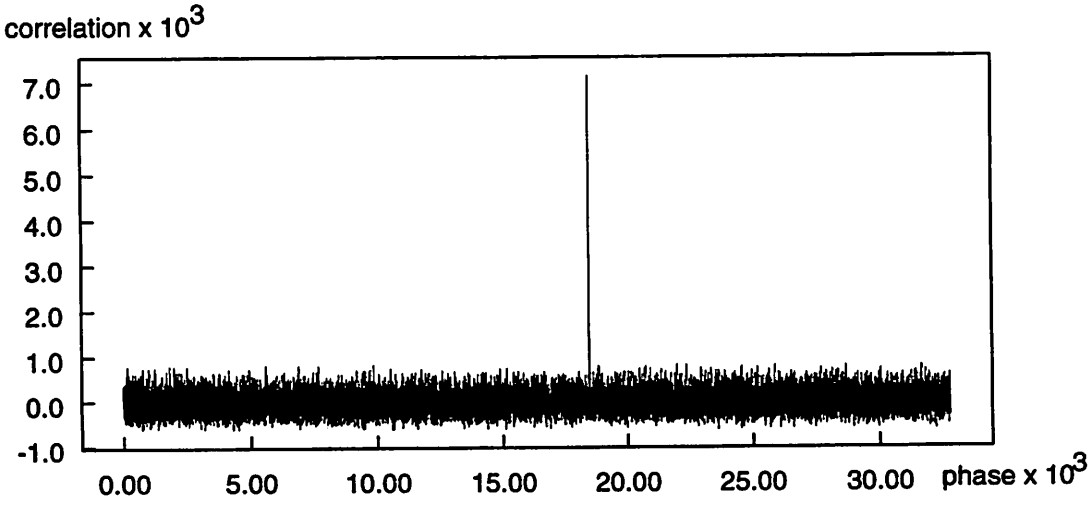


Figure 5-11. Measured Autocorrelation Performance at the Analog Receiver Output using 1024-Long Subcorrelations

has magnitude 7157. All other correlation values are at least 20dB below the correlation peak as desired.

5.1.4. Quadrature LO Generator

The quadrature LO generator is functional within the frequency range, 900MHz to 990 MHz. First, the amplitude imbalance of the two output signals was observed on a spectrum analyzer. Next, the following equation was used to determine the 90° phase accuracy of the clock generator:

$$A\sin(\omega t+\phi)\times B\cos(\omega t) = \frac{1}{2}AB\sin(2\omega t+\phi)+\frac{1}{2}AB\sin(\phi)$$

The in-phase and quadrature-phase outputs were fed into a mixer and the DC component as well as the signal amplitudes were used to determine the phase offset from quadrature. Care was taken to ensure that all wires were equal in length in order to minimize the phase difference due to different cable lengths. Table 5-1 summarizes the values of amplitude imbalance and phase offset from quadrature between the two output signals for various input frequencies. As expected from simulations, the two output clocks do not deviate

Table 5-1. Performance Summary of Quadrature LO Generator

f_{in}(MHz)	A_{out}(mV)	B_{out}(mV)	Δ_{out}(mV)	V_{offset}(mV)	ϕ
800	377	222	155	0.7	0.96°
850	377	252	125	1.8	2.17°
900	317	277	40	0.4	0.52°
910	272	252	20	0.3	0.50°
920	287	257	30	0.2	0.31°
930	297	272	25	0.3	0.43°
940	297	292	5	0.3	0.40°
950	272	272	0	0.2	0.31°
960	247	287	40	0.1	0.16°
970	247	292	45	0.2	0.32°
980	262	322	60	0.2	0.27°
990	242	332	90	0.2	0.29°
1000	169	302	133	0.1	0.22°
1050	222	302	80	0.1	0.17°
1100	182	262	80	0.2	0.48°

Table 5-1. Performance Summary of Quadrature LO Generator

f_{in}(MHz)	A_{out}(mV)	B_{out}(mV)	Δ_{out}(mV)	V_{offset}(mV)	ϕ
1150	162	252	90	0.2	0.56°
1200	182	307	125	0.2	0.41°

significantly from quadrature across the entire band of interest. The main limitation, however, is the amplitude mismatch between the two output clocks. The amplitudes of the two output clocks are identical at 950MHz but they rapidly deviate for both lower and higher frequencies. Future implementations should include output buffers which may be used to tune the two output clock amplitudes for better matching.

5.2. Speed and Power Measurements

All of the above performance measurements were performed at halfspeed with the baseband modulator chip operating with a 5V power supply. Performance measurements on the baseband modulator chip alone have confirmed correct operation at halfspeed down to a supply voltage of 3.3V with a power dissipation of 165mW.

The baseband operating frequency of the transmitter is limited by the maximum operating frequency of the baseband modulator. At 5V, the baseband modulator chip functions correctly at frequencies up to 41MHz, corresponding to an operating frequency of 82MHz for the digital-to-analog converter. This limit is due to the use of undersized clock buffers in the modulator chip.

The maximum carrier frequency is 990MHz which is limited by the on-board quadrature LO generator. The testboard was designed with the option of using an off-board quadrature LO generator. If an off-board quadrature generator is used, the maximum carrier frequency is limited by the LO frequency range (DC to 2.0GHz) of the HPMX-2001 quadrature modulator.

The total power consumption is 12.66W for the following conditions: halfspeed operation; 5V baseband modulator chip supply voltage; and 1.056GHz carrier frequency. The

breakdown of total power consumption by supply voltagles is listed in Table 5-2. The

Table 5-2. Power Consumption Breakdown by Supply Voltages

Supply	Current	Power
V_{DD} (5V)	500mA	2.5W
V_{EE} (-5V)	700mA	3.5W
V_{TT} (-2V)	750mA	1.5W
$V_{DD,DAC}$ (5V)	100mA	0.5W
$V_{EE,DAC}$ (-5V)	500mA	2.5W
$V_{DD,MIX}$ (3V)	20mA	0.06W
$V_{DD,VGA}$ (15V)	140mA	2.1W
	Total:	12.66W

additional power supply, $V_{DD,VGA}$, is used for a variable gain amplifier following the quadrature modulator. This amplifier is required to increase the RF output power level to 0dBm for transmission as described in Section 5.3.2. The breakdown of total power consumption by components is tabulated inTable 5-3. The components responsible for a

Table 5-3. Power Consumption Breakdown by Components

Component	Quantity	Description	Power
baseband modulator	1	custom modulator chip	0.5W
74AC04	4	inverter	0.22W
74AC157	6	multiplexer	0.32W
74AC574	3	register	0.16W
MC10E151	4	ECL register	2.0W
MC10E452	1	ECL register	0.43W
MC10H600	3	TTL-to-ECL converter	3.08W
MC10H601	1	ECL-to-TTL converter	0.75W
AD706	2	op amp	0.02W
AD9617	2	op amp	0.98W
AD9720	2	D/A converter	2.0W
HPMX-2001	1	quadrature modulator	0.1W
ZFL-1000GH	1	VGA	2.1W
		Total:	12.66W

significant portion of the total power consumption are the ECL components, the digital-to-analog converters, and the variable gain amplifier. The custom baseband modulator chip is responsible for only a very small percentage (4%) of the total power consumption.

5.3. Bugs

While testing the CDMA testboard, several bugs were discovered. Fortunately, none of the bugs are fatal. These bugs as well as the modifications used to correct them are described in this section.

5.3.1. Baseband Modulator Chip

As described in [Peroulas95], the registers used for power control values, Walsh codes and the multiplication constant are all double buffered. The appropriate values are initially written to the first level of registers followed by a write to the *loadREQ* register. The values are loaded to the second level of registers when the PN generator rolls over. Both levels of registers consist of TSPC registers. Due to the dynamic nature of these registers, a periodic refresh of the values is required, which may be accomplished simply by using cross-coupled inverters at the register outputs. The second level of TSPC registers used for storing the power control values are lacking the necessary feedback for refresh. Consequently, the power control values at the outputs of the second level of TSPC registers are not the same as the programmed values. For example, for all users set to zero power control, the output data is initially all zero. However, after a random period of time, the output data becomes nonzero due to the lack of refresh.

The most obvious solution is to include the feedback latches at the outputs of the TSPC registers. However, this solution is both time-consuming and costly since it requires a re-fabrication of the entire chip. Another solution is to continuously write to the *loadREQ* register, which strobes the *loadPCw* signal when the PN generator rolls over. Since the PN sequence has length 32768, when the baseband modulator chip is clocked at halfspeed, continuously writing to the *loadREQ* register results in a strobe rate of about 1kHz for the *loadPCw* signal. However, this rate may be insufficient for refreshing the output values of the TSPC registers since discharge times are typically in the range of hundreds of microseconds to tens of milliseconds. Fortunately, the baseband modulator chip includes several features which allow the *loadPCw* signal to be continuously strobed by an external clock, which can be set to a period less than the worst case discharge time. The modulator chip includes several input test signals as well as the ability to select the gating control of

the *loadPCw* signal. The TSPC registers in the first level of power control registers all have the feedback necessary for refresh, as evidenced by the ability to correctly read back the programmed values. By selecting no gating for the *loadPCw* signal and strobing the *testloadPCw* signal with an external clock, the TSPC registers in the second level of power control registers are continuously loaded with the correct values from the registers in the first level. Correct functionality was observed using a 5MHz external clock to strobe the *testloadPCw* signal. Although this method provides an interim solution to the lack of refresh in the second level of power control registers, two potential problems exist. First, the *testloadPCw* signal strobes both the power control and the Walsh registers. Since the feedback latch is present in the Walsh registers, strobing these registers is unnecessary. A more serious problem involves updating or changing the power control values. Simultaneous loading of the power control values to the second level of TSPC registers is no longer initiated by asserting the *loadREQ* signal. Instead the values are now loaded every time the *testloadPCw* signal is asserted. Since it is desirable to change the power control values for the various users simultaneously, the new power control values must be written to the first level of registers within a time equal to the clock period of the *testloadPCw* signal. In order to allow for enough time to update the first level of power control registers, a longer clock period is desired. However, a shorter clock period is desirable in order to refresh the register output values before charge leakage results in the loss of signal integrity.

5.3.2. Testboard

Several problems were discovered on the transmitter testboard. After these problems were rectified, the transmitter testboard was fully functional. First, the input clock to the bank of multiplexors is incorrect. Since the input clock to the baseband modulator chip is ϕ_{32MHz}, the input clock to the multiplexors should also be ϕ_{32MHz}. Instead $\overline{\phi}_{32MHz}$was mistakenly used as the input clock to the multiplexors. This problem was corrected by rewiring the correct clock signal to the multiplexors. Careful inspection of the simulation results of the digital section in Figure 4-10 reveals this mistake, which should have been avoided.

Next, both in-phase and quadrature-phase lowpass filters both lack 50Ω output termination resistors. A 50Ω trace at each output is not sufficient for proper termination. This problem was corrected by soldering a 50Ω resistor from the output to ground for each of the lowpass filters. Note, however, that the input of each lowpass filter does not require an additional 50Ω series termination resistor, despite the low output impedance of the shunt-shunt feedback amplifier used to convert the current output of the digital-to-analog converter to a voltage. After consulting with a Mini-Circuits Applications Engineer, it was determined that a 50Ω trace is sufficient for termination at the lowpass filter input.

Measurements at the ground pins of the lowpass filters exhibit excessive ground bounce. The ground bounce compromises the integrity of the signals by increasing the noise floor of the input signals to the quadrature mixer. Placing a slotted ground plane below each lowpass filter would provide better isolation and minimize the effect of ground bounce.

Observation of the spectral content of the output from the digital-to-analog converter reveals significant clock feedthrough at a frequency equal to half of the input clock frequency to the digital-to-analog converter. This feedthrough is not a significant concern as long as it is filtered out by the lowpass filter following the digital-to-analog converter.

The HPMX-2001 quadrature modulator lacks 50Ω termination resistors at the LO inputs. This problem was corrected by soldering a 50Ω resistor from each LO input to ground. Finally, the output power of the quadrature modulator is insufficient. The saturated output power of the modulator is only -5.5dBm. An additional power amplifier is required to increase the signal power before transmission. Currently an off-board Mini-Circuits variable gain amplifier (P/N ZFL-1000GH) is being used for this purpose.

6 Conclusion

6.1. Summary

Society's increasing demands for information exchange anticipate the need for transceivers which can support many users at very high data rates. [Sheng96] presents the system-level architecture of a CDMA direct sequence spread-spectrum transceiver which is capable of supporting up to 50 users each with a 2Mbps data rate. This report describes the architectural trade-offs and implementation details of designing the transmitter for the digital communications system presented in [Sheng96].

The transmitter presented in this report is a semi-custom solution consisting of commercially available components as well as a custom baseband modulator chip [Peroulas95] fabricated in a 0.8μm digital CMOS process. The transmitter testboard can support up to 15 users each with a 1.28Mbps maximum data rate. In addition, the testboard can support carrier frequencies in excess of 1GHz. The total power consumption of the testboard is 12.66W. Since the transmitter resides in the basestation, minimizing power consumption is not critical.

6.2. Future Directions

As discussed in Section 3.1.2.2.2, incorporation of the digital Hilbert transform within the baseband modulator chip is the most attractive method for single-sideband upconversion. This method has two major benefits. First, since the baseband signal is modulated to an intermediate frequency, the resulting signal is less susceptible to DC offsets and low frequency noise. Second, LO feedthrough in the mixers does not appear in the RF signal band. This method requires the inclusion of four additional subfilters within the baseband modulator chip which contributes to the already large area utilization of the modulator

chip. However, redesigning the baseband modulator chip using a process with a smaller minimum line-width mitigates this concern.

Although the transmitter testboard is fully functional at halfspeed, it fails to meet the original specification of 2Mbps data rate for each user. Achieving the desired data rate may be accomplished by resizing the clock buffers in the baseband modulator chip. In addition, with access to CMOS processes with continually decreasing line-widths, the 2Mbps data rate specification becomes a secondary design consideration. In fact, integration of the high-speed data combining circuitry becomes viable, thus reducing the total testboard area.

Commercially available digital-to-analog converters which operate at 256MHz offer up to only ten bits of resolution. As detailed in [Peroulas95], at least twelve bits of resolution is required in order to meet the worst case user power level combination. If this worst case is encountered frequently, then the current digital-to-analog converters are inadequate and an alternative solution must be determined.

As enumerated in Section 5.3.2, several errors were discovered on the transmitter testboard. The most critical error is the lack of a slotted ground plane below each lowpass filter. Placing a slotted ground plane below each lowpass filter would provide better isolation and minimize the effect of ground bounce.

Finally, the current transmitter testboard supports up to only 15 users. In order to support more than 15 users, several baseband modulator chips must be operated in parallel. The architectural description of a strategy to operate several modulator chips in parallel is presented in [Sheng96].

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Appendix A

A.1. Description of Transmitter Testboard Input and Output Signals

A.1.1. Power Supply Inputs

Table A-1. Power Supply Definitions

Connector	Name	Description
CO24	V_{DD}	5V supply for the digital section
CO25	V_{EE}	-5V supply for the digital section
CO26	V_{TT}	-2V supply
CO27	$V_{EE,DAC}$	-5V supply for the mixed-signal section
CO28	$V_{DD,DAC}$	5V supply for the mixed-signal section
CO23	$V_{DD,MIX}$	3V supply for the analog section

A.1.2. Clock Inputs

Table A-2. Input and Output Clock Definitions

Connector	Name	Description
CO10	f_{CLK2E}	ECL compatible input clock to the digital-to-analog converter; for halfspeed operation, f_{CLK2E} = 64MHz
CO9	$\bar{f}_{CLK2E}$	complementary input signal of f_{CLK2E}
CO19	$f_{LO=0°}$	in-phase sinusoidal output clock from the quadrature LO generator and/or input clock to the quadrature modulator
CO20	$\bar{f}_{LO=0°}$	complementary signal of $f_{LO=0°}$
CO21	$f_{LO=90°}$	quadrature phase sinusoidal output clock from the quadrature LO generator and/or input clock to the quadrature modulator
CO22	$\bar{f}_{LO=90°}$	complementary signal of $f_{LO=90°}$
CO17	f_{LO}	sinusoidal input clock to the quadrature LO generator
CO18	$\bar{f}_{LO}$	complementary input signal of f_{LO}

Table A-3. Clock Control Signals (Connector CO31)

Switch	Name	Description
1	not used	
2	not used	
3	not used	
4	not used	
5	not used	
6	not used	
7	CLKSEL	0: selects CLKPHI for the digital section 1: selects CLKPHI_L for the digital section
8	ECL_RESET	0: normal operation 1: resets the digital section

A.1.3. Baseband Modulator Chip Signals

Table A-4. Baseband Modulator Chip Inputs and Outputs

Inputs are tabulated in columns one and two, and outputs are tabulated in columns three, four and five. For detailed descriptions of the input and output signals, please refer to [Peroulas95].

CO11	CO12	CO13	CO14	CO15
01:	01: inmsb1	01: i1out0	01: q1out0	01: dbusout7
02: phi1	02: inlsb1	02: i1out1	02: q1out1	02: dbusout6
03: reset	03: inmsb2	03: i1out2	03: q1out2	03: dbusout5
04: abusin6	04: inlsb2	04: i1out3	04: q1out3	04: dbusout4
05: abusin5	05: inmsb3	05: i1out4	05: q1out4	05: dbusout3
06: abusin4	06: inlsb3	06: i1out5	06: q1out5	06: dbusout2
07: abusin3	07: inmsb4	07: i1out6	07: q1out6	07: dbusout1
08: abusin2	08: inlsb4	08: i1out7	08: q1out7	08: dbusout0
09: abusin1	09: inmsb5	09: i1out8	09: q1out8	09: abusin6
10: abusin0	10: inlsb5	10: i1out9	10: q1out9	10: abusin5
11: dbusin7	11: inmsb6	11:	11: q2out0	11: abusin4
12: dbusin6	12: inlsb6	12: i2out0	12: q2out1	12: abusin3
13: dbusin5	13: inmsb7	13: i2out1	13: q2out2	13: abusin2
14: dbusin4	14: inlsb7	14: i2out2	14: q2out3	14: abusin1
15: dbusin3	15: inmsb8	15: i2out3	15: q2out4	15: abusin0
16: dbusin2	16: inlsb8	16: i2out4	16: q2out5	16: read
17: dbusin1	17: inmsb9	17: i2out5	17: q2out6	17: write
18: dbusin0	18: inlsb9	18: i2out6	18: q2out7	18: cs_l
19: read	19: inmsb10	19: i2out7	19: q2out8	19: db_write_en
20: write	20: inlsb10	20: i2out8	20: q2out9	20: pnreset_l
21: cs_l	21: inmsb11	21:	21: inmsb1	21: load_pn
22: db_write_en	22: inlsb11	22: loadmult	22: inlsb1	22: stoppn_l
23: pnreset_l	23: inmsb12	23: loadpcw	23: inmsb2	23: stopwalsh_l
24: load_pn	24: inlsb12	24: dataclock	24: inlsb2	24: testloadmult
25: stoppn_l	25: inmsb13	25:	25: inmsb3	25: testloadpcw
26: stopwalsh_l	26: inlsb13	26: pnsig	26: inlsb3	26: testdcpulse
27: testloadmult	27: inmsb14	27: pn_allones_l	27: inmsb4	27: testmode
28: testloadpcw	28: inlsb14	28:	28: inlsb4	28:
29: testdcpulse	29: inmsb15	29:	29: inmsb5	29:
30: testmode	30: inlsb15	30:	30: inlsb5	30:

A.1.4. Miscellaneous Inputs and Outputs

Table A-5. Miscellaneous Input and Output Signal Definitions

Connector	Name	Description
CO1	V_{IDAC}	voltage output of the in-phase digital-to-analog converter and/or voltage input to the in-phase lowpass filter
CO2	V_{QDAC}	voltage output of the quadrature-phase digital-to-analog converter and/or voltage input to the quadrature-phase lowpass filter
CO16	V_{MOD}	voltage output of the quadrature modulator
CO29	V_{ANT}	antenna output
R70	R_{IPOT}	potentiometer used to tune the DC level of the digital-to-analog converter output for the in-phase data
R60	R_{QPOT}	potentiometer used to tune the DC level of the digital-to-analog converter output for the quadrature-phase data

A.2. Description of Files/Directories

A.2.1. *ViewDraw* Files

Table A-6. Description of *ViewDraw* Files

All *ViewDraw* files/directories are located in /users/dyee/research/transmitter/view-logic/.

File/Directory	Description
viewdraw.ini	*ViewDraw* initialization file which references the necessary design directories
newboard/	directory containing the transmitter testboard schematics and symbols; the toplevel schematic is named "toplevel"
boardparts/	directory containing the schematics and symbols of components used for the transmitter testboard

A.2.2. *ViewSim* Files

Table A-7. Description of *ViewSim* Files

All *ViewSim* files/directories are located in /users/dyee/research/transmitter/simulation/.

File/Directory	Description
newboard/	directory containing the transmitter testboard schematics and symbols; the mixed-signal and analog sections are removed since only the digital section can be simulated
toplevel.vsm	input file to *ViewSim*
toplevel.cmd	command file used to simulate the transmitter testboard
libcell.pl	*perl* script used to assign the correct simulation models to testboard components (courtesy S. Sheng)

A.2.3. *Racal* Files

Table A-8. Description of *Racal* Files

All *Racal* files/directories are located in /users/dyee/Racal/work/xboardyee/.

File/Directory	Description
pcb/xboardyee.pcb	*Racal* file for the transmitter testboard
report/paramit.lst	complete listing of transmitter testboard components
rinf/xboardyee.frp	*Racal* input file generated by *oct2rinf*

A.2.4. Quadrature LO Generator Simulation Files

Table A-9. Description of Quadrature LO Generator Simulation Files

All quadrature LO generator simulation files/directories are located in /users/dyee/research/transmitter/spice/.

File/Directory	Description
ire/	directory containing *HSPICE* simulation files for various RLC phase-splitter circuits
polyphase/	directory containing *HSPICE* simulation files for various asymmetric polyphase networks

A.2.5. Miscellaneous Files

Table A-10. Description of Miscellaneous Files

File/Directory	Description
/users/dyee/research/transmitter/oct/	directory containing *vb2oct* and *dmoct* output files; these files were generated in order to convert the *View-Draw* schematics to a *Racal* input file
/users/dyee/research/baseband/output/	directory containing output data acquired from the baseband modulator chip
/users/dyee/research/receiver/das/	directory containing output data acquired from the receiver
/users/dyee/research/receiver/ptolemy/	directory containing *Ptolemy* facets for generating spectral outputs and eye diagrams
baseiqnew (on haagendas)	DAS generation/acquisition program used to setup and acquire data from the baseband modulator chip