DESIGN AND OPTIMIZATION TECHNIQUES FOR MONOLITHIC RF DOWNCONVERSION MIXERS

by

Keng Leong Fong

Memorandum No. UCB/ERL M97/56

8 August 1997

DESIGN AND OPTIMIZATION TECHNIQUES FOR MONOLITHIC RF DOWNCONVERSION MIXERS

by

Keng Leong Fong

Memorandum No. UCB/ERL M97/56

8 August 1997

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

Abstract

Design and Optimization Techniques for Monolithic RF Downconversion Mixers

by

Keng Leong Fong

Doctor of Philosophy in Engineering-Electrical Engineering and Computer Science

University of California, Berkeley

Professor Robert G. Meyer, Chair

Design and optimization techniques for monolithic radio-frequency (RF) downconversion mixers are presented. Equations describing the high-frequency nonlinear behavior of common-emitter and differential-pair transconductance stages are derived. The equations show that the transconductance stages using inductive degeneration are more linear than those using capacitive or resistive degeneration, and that the common-emitter transconductance stages are more linear than the differential-pair transconductance stages with the same bias current and transconductance.

The class AB behavior of common-emitter transconductance stage with inductive degeneration is studied, and the techniques to exploit this behavior are presented. The class AB behavior reduces the bias current requirement and improves the power efficiency. Noise optimization issues and noise mixing phenomenon of downconversion mixers are explored. The desensitization mechanisms by a blocker are investigated. A strong blocker desensitizes a mixer with three mechanisms, namely compressing the gain of the small desired signal, mixing low-frequency noise from bias circuit up to the RF, and mixing phase noise of local oscillator to the intermediate frequency (IF).

The design and optimization techniques are demonstrated in two monolithic RF downconversion mixers. A downconversion mixer for 900 MHz applications is implemented in a 25 GHz f_T bipolar process. The design consumes 10.2 mA total current from a 3V supply. It has a power gain of 7.5 dB, a single-sideband noise figure of 7.5 dB and an input 1 dB compression point -1.5 dBm. A downconversion mixer for 2.4 GHz wireless LAN applications is implemented in a 1μm BiCMOS process with 13 GHz f_T bipolar transistor. The design has a power gain of 4.5 dB, a single-sideband noise figure of 10 dB, an input third-order intercept point of 1 dBm, and an input 1 dB compression point of -7.5 dBm. Applications of the techniques to other analog building blocks, such as low-noise amplifiers and power amplifiers, are also presented.

Approved by: Robert Gray

Committee Chairman

Table of Contents

Acknowledgments

I would like thank Professor Robert G. Meyer for supervising this thesis project. His guidance and supervision style allowed me to exercise my full potential and creativity in research. I would also like to thank Professor Paul R. Gray for being a second reader of this thesis and spending time with me within his busy schedule. I am also grateful to Professor Philip B. Stark who reviewed this thesis.

I am deeply grateful to the help provided by Dr. Christopher D. Hull. Besides supervising my summer internships with Rockwell International Corporation, he has been both a mentor and a friend since I have known him. His technical insight and experience provide a great source of information.

The 900 MHz mixer was designed during my summer internship with Rockwell. Financial and technical support provided by Rockwell are greatly appreciated. I would like to thank the employees of Rockwell, especially Joo Leong Tham, Frank Intveld, Loan Volt, Tom Little and Ronald Hlavac, for their help with design, layout and testing of this mixer.

Fabrication of the 2.4 GHz mixer by Philips Semiconductors is appreciated. I would like to thank the employees of Philips, especially William D. Mack, Sheng H. Lee, Kelvin McAdams, Frank Fang and Yvonne Peng, for their help on this project. Inductor simulation program from Ali M. Niknejad is used for the design.

Lastly, I would like to thank my family, especially my parents, Mr. Fong Chung and Madam Mak Kat Yan, for their love and emotional support during my quest for the highest

academic achievement. I would like to acknowledge the support of my fellow graduate students who share the fun and learning experience.

This work is supported in part by the U.S. Army Research Office under Grant Number DAAH04-93-F-0200.

CHAPTER 1

Introduction

The rapid growth of portable wireless communication systems, such as wireless (cordless and cellular) phones, global positioning satellites (GPS), wireless local area networks (LAN) and etc., have increased the demand for low-cost and high-performance front-end receivers. This presents a challenge to radio-frequency (RF) circuit designers to find optimal solutions for the realization of high-frequency (900 MHz to 3 GHz) receivers using low-cost plastic package and high-volume silicon technologies.

Fig. 1.1 shows a typical RF receiver front-end architecture. The downconversion

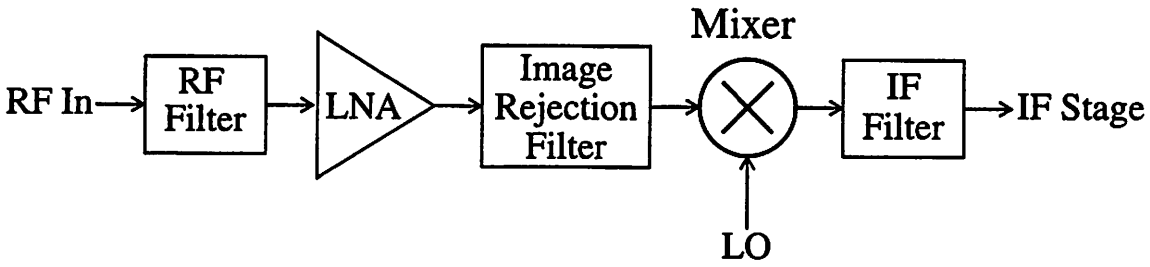

Fig. 1.1 RF Receiver Front-End

mixer is used to convert the RF signal down to an intermediate frequency (IF) by mixing the RF signal from the low-noise amplifier (LNA) with the local oscillator (LO) signal. This allows channel selection and gain control at lower frequencies where high quality-factor (Q) filters and variable-gain amplifiers can be constructed economically. Instead of using an IF filter with tunable passband frequency, an IF filter with fixed passband frequency is used, and the LO frequency is tuned to select the desired channel. The LNA is

used to amplify the RF signal to reduce the noise contribution from the mixer. The RF and image-rejection filters are used to reject undesired out-of-band signals.

The downconversion mixer, which is the focus of this thesis project, is a very important building block within the receiver front-end because its performance affects the system performance and the performance requirements of adjacent building blocks. For instance, a mixer with low noise reduces the gain requirement from the LNA. A mixer with high conversion gain reduces the noise contribution from the IF stages. A mixer which requires low LO input power reduce the power consumption of the LO.

Downconversion mixers perform frequency conversion by using nonlinear elements in time-varying circuits. The nonlinear operation is difficult to describe analytically, and hence optimization becomes very difficult. In addition to amplitude changes and phase shifts as in a linear system, signals and noise also undergo frequency shifts in a time-varying nonlinear system. As a result, many active mixers realized in silicon technologies are not optimized, and have poor performance (high noise and poor linearity). It is the objective of this thesis project to improve the performance of active mixers by understanding the nonlinear operations, simplifying the optimization procedures, and investigating new circuit techniques.

1.1 Manifestation of Nonlinear Behavior

In this section, some of the common nonlinear effects [1] are described. Understanding these effects helps in optimizing nonlinear circuits. The simplified nonlinear transfer function (in Volterra Series [2][3]) of a circuit shown below is used to explain the nonlinear effects.

$$V_o = \alpha_1 \circ V_s + \alpha_2 \circ V_s^2 + \alpha_3 \circ V_s^3 + \ldots + \alpha_n \circ V_s^n + \ldots \quad (1.1)$$

where V_s and V_o are the input and output signals respectively. The operator '$\circ$' indicates multiplying each frequency component in V_s^n by the magnitude of α_n and shifting each frequency component in V_s^n by the phase of α_n.

The n'th harmonic of V_s is generated by the n'th power of V_s in equation (1.1). For instance, if V_s is a single-tone signal represented by (Acos ωt), where A is the amplitude and ω is the fundamental frequency. The square of V_s generates the second harmonic (cos 2ωt) as follow

$$V_s^2 = (A\cos\omega t)^2 = \frac{A^2}{2}(1 + \cos 2\omega t)$$

If the index 'n' is an even number, the n'th power of V_s also generates other even-order harmonics (including the DC component) with lower order than 'n'. If the index 'n' is an odd number, the n'th power of V_s generates other odd-order harmonics (including the fundamental harmonic) with lower order than n. For instance, the cube of V_s generates the fundamental (cos ωt) and third-order (cos 3ωt) harmonics as follow

$$V_s^3 = (A\cos\omega t)^3 = \frac{3}{4}A^3\cos\omega t + \frac{1}{4}A^3\cos 3\omega t$$

All the even-power terms in equation (1.1) generate DC component. For instance, if V_s is a single-tone signal represented by (Acos ωt), the square of V_s generates the DC component $\left(\frac{1}{2}A^2\right)$. Similarly, the forth power of V_s generates the DC component $\left(\frac{3}{8}A^4\right)$. In general, the DC component generated by all even-power terms is given by

$$\frac{\alpha_2}{2}A^2 + \frac{3\alpha_4}{8}A^4 + \ldots + \binom{n}{n/2}\frac{\alpha_n}{2^n}A^n + \ldots$$

where

$$\binom{x}{y} = \frac{x!}{(x-y)!y!},$$

and n is even.

All the odd-power terms in equation (1.1) cause gain compression or expansion. For instance, if V_s is a single-tone signal represented by Acos ωt, the cube of V_s generates $\left(\frac{3}{4}A^3\cos\omega t\right)$, which is added directly to fundamental harmonic generated by the first-power term in equation (1.1). As a result, the fundamental harmonic in the output signal is given by

$$\alpha_1 \circ A\cos\omega t + \frac{3}{4}\alpha_3 \circ A^3\cos\omega t$$

If α_3 has opposite phase from α_1, the $(\alpha_3 \circ V_s^3)$ term causes gain compression. On the other hand, if α_3 has the same phase as α_1, the $(\alpha_3 \circ V_s^3)$ term causes gain expansion. Similarly, the fifth power of V_s generates $\left(\frac{5}{8}A^5\cos\omega t\right)$. This term can cause gain compression or expansion, depending on the phase of α_5. In general, the fundamental harmonic generated by all odd-power terms is given by

$$\alpha_1 \circ A\cos\omega t + \frac{3}{4}\alpha_3 \circ A^3\cos\omega t + \ldots + \binom{n}{(n-1)/2}\frac{\alpha_n}{2^{n-1}} \circ A^n\cos\omega t + \ldots \qquad (1.2)$$

where n is odd.

Expression (1.2) can also be used to explain the amplitude modulation (AM) to phase modulation (PM) conversion phenomenon. Since α_n (where n is larger than 1) has different phase from α_1, the odd-power term causes phase shift to the fundamental harmonic in the output signal. As shown in expression (1.2), the amount of phase shift is a function of amplitude (A). As a result, modulation in amplitude induces modulation in phase.

The odd-power terms in equation (1.1) cause gain compression or expansion to a small signal in the presence of a large signal. For instance, if V_s is the sum of a small signal ($A_a \cos \omega_a t$) and a large signal ($A_b \cos \omega_b t$), the small output signal at frequency ω_a is given by

$$\alpha_1 \circ A_a \cos \omega t + \frac{3}{2} \alpha_3 \circ A_a A_b^2 \cos \omega t + \ldots$$

where the first and second terms are generated by the first-power and the third-power terms in equation (1.1) respectively. The first term represents the desired output signal where the magnitude of α_1 is the linear gain under small-signal conditions. If α_3 has different phase from α_1, the large signal causes gain compression to the small signal. This phenomenon is known as desensitization by the large signal. The amount of gain compression depends on the amplitude of the large signal and the third-order coefficient α_3. In the extreme case, the small signal is reduced to a level so small that it is no longer detectable. In this case, the small signal is said to be blocked out by the large signal. On the other hand, if α_3 has the same phase as α_1, the third-power term in equation (1.1) causes gain expansion to the small signal. Typically, gain expansion of the small signal is harmless. It is important to note that the gain compression and expansion are independent of the ampli-

tude of the small signal, if the amplitude of the small signal is small enough that it does not activate higher-power terms in equation (1.1).

The nonlinear terms in equation (1.1) generates frequency-mixing products if V_s comprises more than one signals with different frequencies. This phenomenon is known as intermodulation. For instance, if V_s is the sum of two signals ($A_a\cos\omega_a t$ and $A_b\cos\omega_b t$) of different frequencies ω_a and ω_b, the square of V_s generates

$$V_s^2 = (A_a\cos\omega_a t + A_b\cos\omega_b t)^2$$
$$= \frac{A_a}{2}(1+\cos 2\omega_a t) + \frac{A_b}{2}(1+\cos 2\omega_b t) + A_1A_2[\cos(\omega_a+\omega_b)t + \cos(\omega_a-\omega_b)t]$$

where the ($\cos 2\omega_a t$) and ($\cos 2\omega_b t$) terms are the second harmonics of the two signals respectively. In addition, the $[\cos(\omega_a + \omega_b)t]$ and $[\cos(\omega_a - \omega_b)t]$ terms are the second-order intermodulation products which are located at the sum and difference frequencies of ω_a and ω_b respectively.

Similarly, the cube of V_s generates intermodulation products at frequencies $(2\omega_a \pm \omega_b)$ and $(2\omega_b \pm \omega_a)$ where the second harmonic of one signal mixes with the fundamental harmonic of the other signal. This phenomenon is known as third-order intermodulation. Unlike the second-order intermodulation products, the third-order intermodulation products at frequencies $(2\omega_a - \omega_b)$ and $(2\omega_a - \omega_b)$ are located close to the fundamental signals. This may result in undesirable consequence (more detail in section 2.4). If V_s is the sum of the three signals at different frequencies ω_a, ω_b and ω_c, the cube of V_s generates intermodulation products at frequencies $(\pm\omega_a \pm \omega_b \pm \omega_c)$. Those located at frequencies $(\omega_a + \omega_b - \omega_c)$, $(-\omega_a + \omega_b + \omega_c)$ and $(+\omega_a - \omega_b + \omega_c)$ are close to the fundamental signals.

In general, the n'th power of V_s generates intermodulation products at frequencies $(\pm\omega_1 \pm \omega_2 \pm \ldots \pm \omega_n)$. These frequency-mixing phenomena are not limited to mixing among signals. Signals can mix with noise and move noise from one frequency to another.

The odd-power terms in equation (1.1) can cause amplitude modulation of one signal to be transferred to another signal. This phenomenon is known as cross modulation. For instance, if V_s is the sum of the two signals, where the first one is a single-tone signal $(A_a \cos \omega_a t)$ without modulation. The second one is an amplitude-modulated signal represented by $\{[1 + m(t)]\, A_b \cos \omega_b t\}$, where [m(t)] is the modulation waveform and ω_b is the carrier frequency. The cube of V_s produces the following term at frequency ω_a.

$$\frac{3}{2} A_a A_b^2 [1 + m(t)]^2 \cos \omega_a t$$

This term is added to the fundamental signal $(\alpha_{1o} \cos \omega_a t)$ generated by the first-power term in equation (1.1). Hence, the modulation signal on the ω_b carrier is transferred to the signal at frequency ω_a.

The even-power terms in equation (1.1) can demodulate an amplitude-modulated signal. For instance, if V_s is an amplitude-modulated signal represented by $\{[1 + m(t)]\, A \cos \omega t\}$, where m(t) is the modulation waveform and ω is the carrier frequency. The square of V_s produces

$$V_s^2 = \frac{A^2}{2}[1 + m(t)]^2 + \frac{A^2}{2}[1 + m(t)]^2 \cos 2\omega t \,,$$

where the term $\left\{\frac{A^2}{2}[1+m(t)]^2\right\}$ can be expanded into $\left\{\frac{A^2}{2}+A^2m(t)+\frac{A^2}{2}m^2(t)\right\}$.

Thus, the second-power term extracts the modulation waveform m(t) from V_s.

1.2 Mixer Topologies

In terms of conversion gain, downconversion mixers can be categorized into passive and active mixers. Although passive mixers, such as diode mixers [1][4] and passive field effect transistor (FET) mixers [5][6] are very linear and can operate at very high frequency (> 10 GHz), they have no conversion gain. On the other hand, active mixers provide conversion gain to reduce the noise contribution from the IF stages. The single-balanced and double-balanced active mixers shown in Fig. 1.2 and Fig. 1.3 are common kinds of active

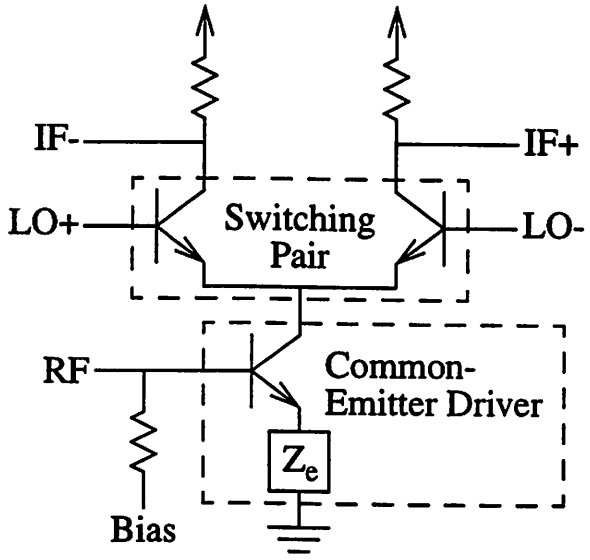

Fig. 1.2 Single-Balanced Active Mixer

mixers. Each mixer comprises a driver stage and a differential switching stage (switching pair in single-balanced mixer and switching quad in double-balanced mixer). The driver stage amplifies the RF signal to compensate for the attenuation caused by the switching

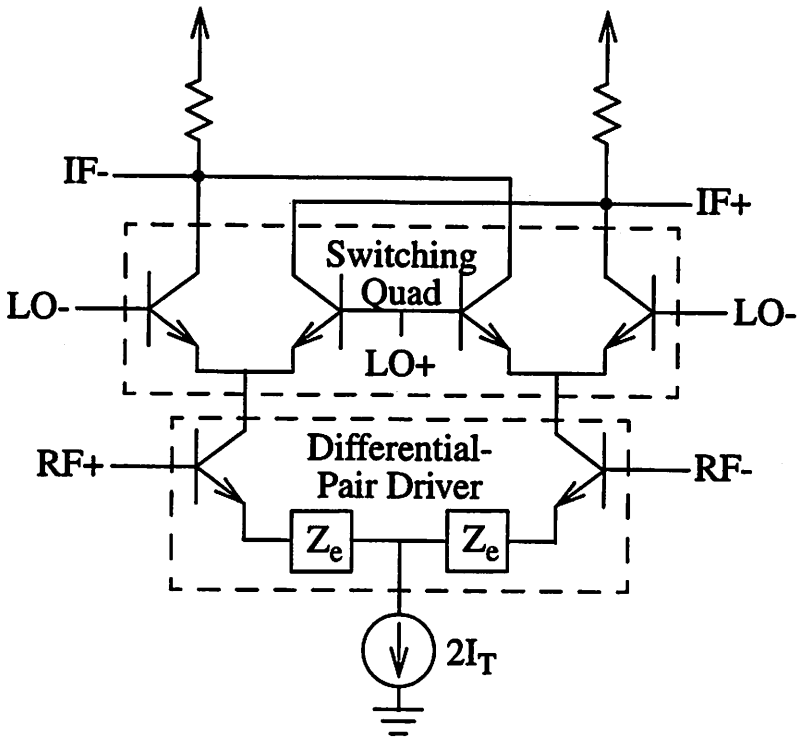

Fig. 1.3 Double-Balanced Active Mixer

operation, and to reduce the noise contribution from the switching stage (pair or quad). A common-emitter transconductance stage and a differential-pair transconductance stage (where $2I_T$ is the tail current source) are used as the driver stages for the single-balanced and double-balanced mixers respectively. The degeneration components (Z_e), which is used to increase the linearity of the driver stage, can be implemented by either resistors, inductors or capacitors. If the RF input signal is single-ended, one side of the differential-pair driver stage in the double-balanced mixer can be AC grounded.

The switching stages perform the mixing operation (multiplying with square wave) which converts the RF signal down to the IF. In the double-balanced mixer, the mixing operation can be described by the following equation.

$$I_O = V_{RF}\cos\omega_{RF}t \times G_M \times \left(\frac{2}{\pi}\cos\omega_{LO}t - \frac{2}{3\pi}\cos 3\omega_{LO}t + \ldots\right)$$

$$= \frac{1}{\pi}G_M V_{RF}\cos(\omega_{LO} - \omega_{RF})t + \frac{1}{\pi}G_M V_{RF}\cos(\omega_{LO} + \omega_{RF})t + \ldots, \qquad (1.3)$$

where I_O is the differential output signal (across differential load resistor), ω_{RF} and ω_{LO} are the RF and LO frequencies respectively, V_{RF} is the RF input signal, and G_M is the transconductance of the driver stage. This equation assumes instantaneous switching (multiplying RF signal with square wave) of the switching quad. In the high-side mixing case (LO frequency is higher RF), the (ω_{LO} - ω_{RF}) term is the desired IF signal, while the (ω_{LO} + ω_{RF}) term is the unwanted signal. The $\frac{1}{\pi}$ factor is caused by the power lost in the (ω_{LO} + ω_{RF}) term and other higher-frequency terms. In the low-side mixing case (LO frequency is lower than RF), the (ω_{RF} - ω_{LO}) and (ω_{LO} + ω_{RF}) terms are the desired and unwanted signals respectively.

Equation (1.3) , only applies to the case where differential IF output is taken. In this case, there are no LO or RF feedthrough signal at the IF output port of the mixer. If single-ended output is taken, the mixing operation can be represented by the following equation.

$$I_O = \left(I_T + V_{RF}\frac{G_M}{2}\cos\omega_{RF}t\right) \times \left(\frac{1}{2} + \frac{2}{\pi}\cos\omega_{LO}t - \frac{2}{3\pi}\cos 3\omega_{LO}t + \ldots\right) +$$

$$\left(I_T - V_{RF}\frac{G_M}{2}\cos\omega_{RF}t\right) \times \left(\frac{1}{2} - \frac{2}{\pi}\cos\omega_{LO}t + \frac{2}{3\pi}\cos 3\omega_{LO}t + \ldots\right)$$

$$= I_T + \frac{1}{\pi}G_M V_{RF}\cos(\omega_{LO} - \omega_{RF})t + \frac{1}{\pi}G_M V_{RF}\cos(\omega_{LO} + \omega_{RF})t + \ldots \qquad (1.4)$$

The LO and RF feedthrough signals are cancelled at the IF output port, but the DC component I_T remains. On the other hand, there are LO and RF feedthrough signals (due to DC components in both RF and LO signals) at the IF output port of the single-balanced mixer

if single-ended output is taken. In this case, the mixing operation can be represented by the following equation.

$$\begin{aligned} I_O &= (I_Q + V_{RF}G_M\cos\omega_{RF}t)\times\left(\frac{1}{2}+\frac{2}{\pi}\cos\omega_{LO}t-\frac{2}{3\pi}\cos 3\omega_{LO}t+\ldots\right) \\ &= \frac{I_Q}{2}+\frac{1}{2}V_{RF}G_M\cos\omega_{RF}t+\frac{2}{\pi}I_Q\cos\omega_{LO}t \\ &\quad +\frac{1}{\pi}G_MV_{RF}\cos(\omega_{LO}-\omega_{RF})t+\frac{1}{\pi}G_MV_{RF}\cos((\omega_{LO}+\omega_{RF})t+\ldots \end{aligned} \quad , (1.5)$$

where I_Q is the bias current of the driver stage. The $\left(\frac{1}{2}V_{RF}G_M\cos\omega_{RF}t\right)$ and $\left(\frac{2}{\pi}I_Q\cos\omega_{LO}t\right)$ terms represent the RF and LO feedthrough signals respectively. Therefore, a single-balanced mixer does not reject LO and RF feedthrough at the IF output port if single-ended output is taken. If the IF output of the single-balanced mixer is taken differentially, there is no RF feedthrough signal at the IF output port since the LO signal has no DC component. In this case, the mixing operation can be represented by following equation.

$$\begin{aligned} I_O &= (I_Q + V_{RF}G_M\cos\omega_{RF}t)\times\left(\frac{2}{\pi}\cos\omega_{LO}t-\frac{2}{3\pi}\cos 3\omega_{LO}t+\ldots\right) \\ &= \frac{2}{\pi}I_Q\cos\omega_{LO}t+\frac{1}{\pi}G_MV_{RF}\cos(\omega_{LO}-\omega_{RF})t+\frac{1}{\pi}G_MV_{RF}\cos(\omega_{LO}+\omega_{RF})t+\ldots \end{aligned} \quad (1.6)$$

However, there is still LO feedthrough signal at the IF output port.

Besides single-balanced and double-balanced mixers, there is a third group of active mixers, namely the unbalanced mixers. Fig. 1.4 and Fig. 1.5 show two different circuit topologies of unbalanced mixers. In both topologies, the mixing operation is performed by modulating transconductances of the driver stages with the LO signals. In the single-tran-

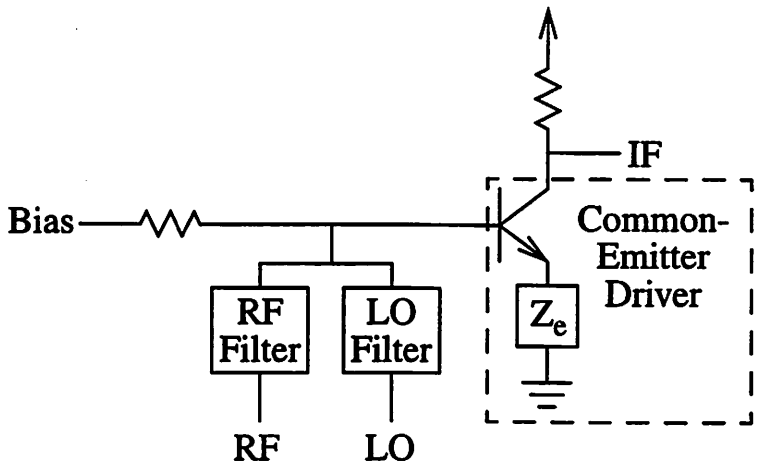

Fig. 1.4 Single-Transistor Active Mixer

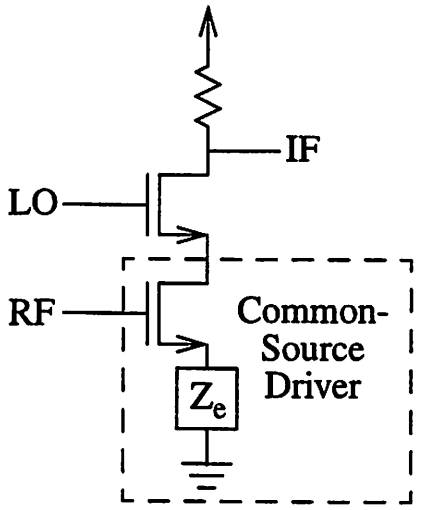

Fig. 1.5 Dual-Gate FET Mixer

sistor active mixer shown in Fig. 1.4, the LO signal modulates the transconductance of the common-emitter driver stage by varying the base-emitter voltage (V_{BE}) of the bipolar transistor. In the dual-gate FET mixer shown in Fig. 1.5, the LO signal modulates the transconductance of the common-source driver stage by varying the drain-source voltage

(V_{DS}) of the lower transistor. Since there are DC components in both RF and LO signals, unbalanced mixers do not reject LO-to-IF and RF-to-IF feedthrough signals.

The four active mixer topologies (Fig. 1.2, Fig. 1.3, Fig. 1.5 and Fig. 1.5) shown above can be implemented in both bipolar and FET technologies, except the dual-gate FET mixer shown in Fig. 1.5. The dual-gate FET mixer cannot be implemented in bipolar technology because the frequency response of bipolar transistors is greatly degraded in saturation.

Both single-balanced and double-balanced mixers reject LO-to-RF feedthrough if the differential switching stages are driven differentially. However, in the unbalanced mixer, LO-to-RF feedthrough is not rejected because the LO signal is unbalanced. In the single-transistor active mixer shown in Fig. 1.4, the LO signal is injected into the RF port through the RF filter. In the dual-gate FET mixer shown in Fig. 1.5, the LO signal is injected into the RF port through the gate-to-drain (C_{GD}) capacitance of the lower transistor.

The unbalanced mixers have best noise performance due to the simplicity of their circuits. In other words, there are fewer noise contributors, compared to both single-balanced and double-balanced designs. However, the unbalanced mixers are the most difficult to design due to their unbalanced properties. For instance, the RF and LO feedthrough problems have to be tolerated. The single-balanced design is a compromise between unbalanced and double-balanced designs. Single-balanced mixers are easier to design than unbalanced mixers, but have better noise performance than double-balanced mixers.

1.3 Thesis Outline

The objective of this thesis project is to investigate design and optimization techniques for improving the performance of monolithic RF downconversion mixers, and to apply them in actual designs to demonstrate their feasibility. The thesis is divided into three main chapters.

Chapter 2 discusses the performance parameters that characterize RF downconversion mixers, and their impacts on the overall system performance and the performance requirements of adjacent building blocks. The performance parameters discussed are noise figure, conversion gain, gain compression, third-order intermodulation distortion, power consumption, port return loss, and port isolation.

Chapter 3 presents the design and optimization techniques investigated in this thesis project. This chapter has four sections. Section 3.1 studies the third-order intermodulation distortion. The third-order intermodulation equations (in Volterra Series) for both common-emitter and differential-pair transconductance stages are derived. The equations can be used for linearity optimization. Section 3.2 discusses class AB behavior and how it can be exploited to reduce the power consumption. Section 3.3 concentrates on optimization techniques for noise performance. Section 3.4 discusses the desensitization mechanisms by a blocker and ways to mitigate the effects.

Chapter 4 presents two design examples to demonstrate the techniques discussed in chapter 3. The first example is a 900 MHz class AB mixer fabricated in a 25 GHz f_T bipolar process. The second example is a 2.4 GHz mixer fabricated in a 1μm BiCMOS process (with 13 GHz f_T bipolar transistor) for wireless LAN applications. The major difference

between the two designs is the ratio of device f_T to signal frequencies. Application of the techniques to other RF building blocks, such as LNAs and power amplifiers, are also discussed.

CHAPTER 2

Performance Parameters

The parameters that affect the receiver performance can be divided into four categories, namely sensitivity, selectivity, overloading and power consumption. Sensitivity measures the smallest signal the receiver needs to achieve the specified bit error rate (BER). It depends on the system noise figure of the receiver and the demodulation scheme used. Selectivity, which includes adjacent channel selectivity, image rejection, and out-of-band blocker rejection, measures the ability to detect the desired signal and to reject the undesired signals. Adjacent channel selectivity depends on the third-order intermodulation performance of the LNA and downconversion mixer, the selectivities of the IF and baseband filters, and the LO phase noise. Image rejection depends on the selectivities of the RF and image-rejection filters. Out-of-band blocker rejection depends on the selectivities of the RF and image-rejection filters, the LO phase noise, and the desensitization effects [7][8] on the LNA and downconversion mixer by the blocker. Overloading measures the largest desired signal the receiver can handle while maintaining a specific BER. It depends on the 1 dB compression point of the receiver system. Power consumption determines the usage time of a portable receiver. Although the overall performance of a receiver depends on the performance parameters of all building blocks, this chapter concentrates on the performance parameters of downconversion mixers only, and how they affect the system performance and the performance requirements of adjacent building blocks.

2.1 Noise Figure

Noise figure (NF) is commonly used in communication systems to specify the noise performance of a circuit. It measures the signal-to-noise ratio (SNR) degradation caused by the circuit [4]. In communication systems where the source impedance is well defined, NF is defined as

$$NF = \frac{N_s + N_i}{N_s} = 1 + \frac{N_i}{N_s} . \tag{2.1}$$

where N_s and N_i are the noise power of the source impedance and the input-referred noise power of the circuit respectively. The value of NF is meaningless if the source impedance is not specified. Typically, NF is expressed in decibel (dB) scale.

The system noise figure (in linear scale) for the downconverter shown in Fig. 1.1 is

$$\begin{aligned} NF &= \frac{1}{L_{RF}} + \frac{NF_{LNA} - 1}{L_{RF}} + \frac{1}{L_{RF}G_{LNA}}\left(\frac{1}{L_{IM}} - 1\right) + \frac{NF_{MIX} - 1}{L_{RF}G_{LNA}L_{IM}} \\ &= \frac{1}{L_{RF}}\left(NF_{LNA} + \frac{NF_{MIX} - L_{IM}}{G_{LNA}L_{IM}}\right), \end{aligned} \tag{2.2}$$

where L_{RF} and L_{IM} are the insertion losses of the RF filter and the image-rejection filter respectively, NF_{LNA} and NF_{MIX} are the noise figures of the LNA and the mixer respectively, and G_{LNA} is the power gain of the LNA. This equation assumes that the noise figures of the filters are the same as their insertion losses. Noise contribution from the IF stage is not included in this equation. As shown in equation (2.2), the LNA needs to have sufficient power gain to reduce the noise contribution from the mixer. Hence, a mixer with low noise figure (NF) is highly desirable in order to relax the gain requirement of the LNA. Most of the low-noise active downconversion mixers (in silicon technologies) currently available have a single-sideband noise figure greater than 10 dB. One of the goals of

this thesis project is to construct a mixer with significantly lower noise figure, without sacrificing linearity.

There are two types of noise figure measures for downconversion mixers, namely single-sideband (SSB) noise figure and double-sideband (DSB) noise figure. The single-sideband noise figure is applicable to the heterodyne architecture where the RF signal is converted to an IF which is higher than half the image-rejection filter bandwidth. Fig. 2.1

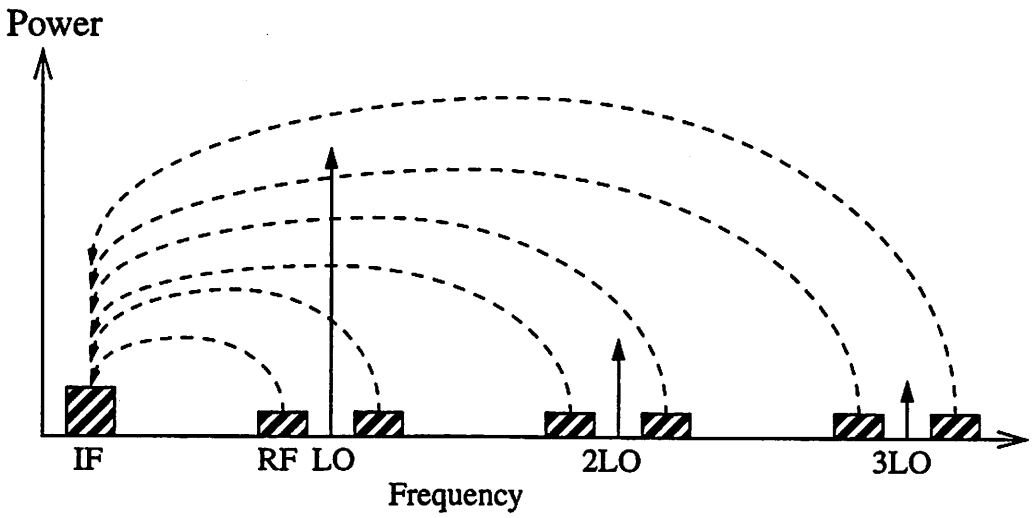

Fig. 2.1. LO Mixes Noise to the IF

shows how the LO signal and its harmonics mix noise at various frequencies to the IF. The term "single-sideband" is derived from the fact that only one of the sideband (the RF band) of the LO signal is converted to the IF (the image band is rejected). On the other hand, the double-sideband noise figure is applicable to the homodyne (direct conversion) architecture [9] where the RF signal is converted to the baseband directly. Fig. 2.2 shows how the LO and its harmonics mix noise at various frequencies to the baseband. The term "double-sideband" is derived from the fact that two sidebands of the LO signals are con-

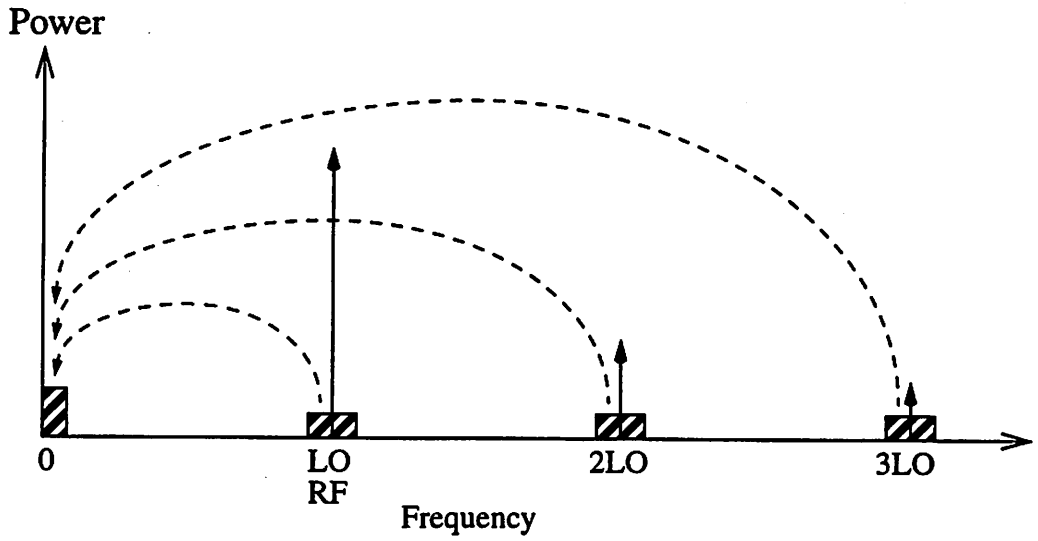

Fig. 2.2. LO Mixes Noise to the Baseband

verted to the baseband (LO frequency is in the middle of the RF band). Comparing Fig. 2.1 and Fig. 2.2, it is obvious that the mixer in the heterodyne architecture has twice as many noise contributors as that in the homodyne architecture. Hence, the single-sideband noise power is about 2 times (3 dB) higher than the double-sideband noise power. It is important to notice that a factor of 2 difference in noise power does not translate to 3 dB difference in noise figure because

$$\left(1+\frac{2N_{DSB}}{N_s}\right)<2\left(1+\frac{N_{DSB}}{N_s}\right)$$

$$\Rightarrow NF_{SSB}<2NF_{DSB}\ ,$$

where N_{DSB} is the input-referred double-sideband noise power of the mixer, NF_{SSB} and NF_{DSB} are the single-sideband and double-sideband noise figures of the mixer respectively. However, if NF_{DSB} is much larger than N_s, NF_{SSB} is about 3 dB higher than NF_{DSB}.

2.2 Conversion Gain

A downconversion mixer should provide sufficient power gain to compensate for the IF filter loss, and to reduce the noise contribution from the IF stages. However, this gain should not be too large, as a strong signal may saturate the output of the mixer. Typically, power gain, instead of voltage or current gains, is specified. The reason is that NF is a power quantity, and hence it is easier to translate the NF of the IF stages to the system NF using power gain. Power gain (G) is related to voltage and current gains by

$$G = \left(\frac{V_O}{V_I}\right)^2 \frac{R_S}{R_L} = \left(\frac{I_O}{I_I}\right)^2 \frac{R_L}{R_S} \tag{2.3}$$

where V_O and V_I are output and input voltages respectively, I_O and I_I are output and input currents respectively, R_L and R_S are load and source resistance respectively. Although increasing the load resistance by a factor of 2 can increase the voltage gain of the mixer by 6 dB, the power gain is increased by only 3 dB.

2.3 Gain Compression

A strong signal can saturate a mixer and reduce its gain. The input 1 dB compression point (P_{-1dB}) measures the input power level that causes the mixer to deviate from its linear magnitude response by 1 dB. Fig. 2.3 shows the magnitude response of a mixer as a function of input signal power. The dotted line shows the linear magnitude response of an ideal mixer. Due to odd-order nonlinearities and limiting (current limiting and/or voltage headroom limiting), the conversion gain of an actual mixer is compressed at high input power level, as shown by the solid line. The conversion gain of the mixer is the ratio of output power to input power. The point where the large-signal gain is 1 dB below the

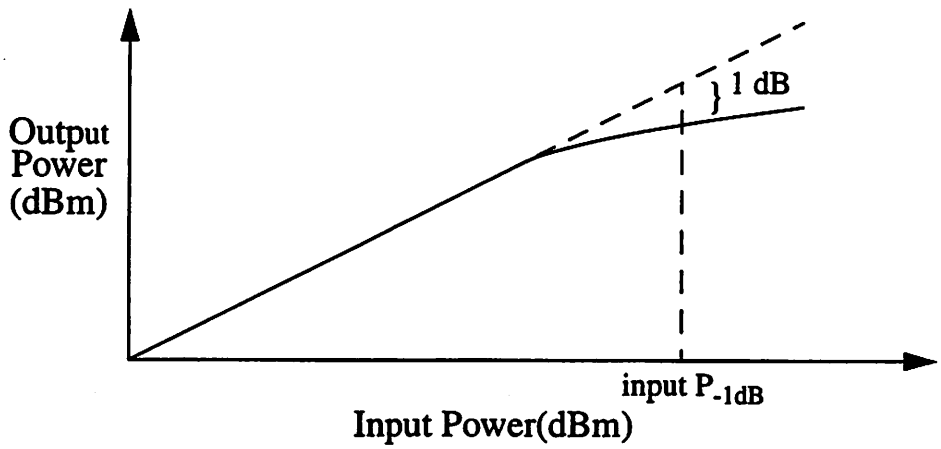

Fig. 2.3 Amplitude Response of Mixer

small-signal gain is the P_{-1dB}. In the case where gain compression is caused by limiting, the gain drops abruptly and the output power stays constant as the input power exceeds the input P_{-1dB}. In the case where the gain compression is caused by the odd-order nonlinearities in the transfer functions of the devices used, the gain decreases more gradually as the input power exceeds the input P_{-1dB}. At medium input power levels, gain compression is dominated by the third-order nonlinearity. As the input power increases, higher-order nonlinearities become significant.

If the input power of the desired signal is larger than the input P_{-1dB}, the desired signal can be distorted at the output of the mixer. This distortion causes amplitude modulation (AM) to phase modulation (PM) conversion. No information is lost if the desired signal is frequency modulated. On the other hand, if the signal is phase modulated, the unwanted phase shift caused by AM-to-PM conversion may result in detection errors, which increase the BER. On the other hand, if the input power of an undesired signal exceeds the input P_{-1dB}, distortion of the undesired signal does not affect the system per-

formance. However, a strong undesired signal (known as a blocker or interferer) can overload a mixer and cause gain compression of the small desired signal if the mixer does not have sufficiently high input P_{-1dB} [7][8]. This phenomenon is one of the desensitization effects caused by a strong blocker (more detail in section 3.4).

The blocker should not reduce the gain of the small desired signal by more than 1 dB to avoid increasing the noise contribution from the IF stages significantly. In many applications, especially those around the crowded 900 MHz bands, there are many strong adjacent out-of-band blockers which can desensitize the mixer. Unfortunately, there is no simple relationship between the gain compression of the small desired signal and that of the large undesired signal. The relationship derived in [7] assumes a weakly nonlinear condition where the gain compression is caused solely by the third-order term in the transfer function of the mixer. If this were case, the input blocker power that causes 1 dB gain compression to the small desired signal would be 3.1 dB less than input P_{-1dB} of the mixer. This describes many practical mixers, but higher-order terms can also be important in the presence of large signals. The small desired signal can be viewed as amplitude modulation on top of the blocker which functions like a carrier. Typically, the modulation signal (the small desired signal) is compressed more than the carrier (the large blocker). In actual designs, SPICE simulation should be used to verify that the gain compression of the small desired signal is less than 1 dB. The actual value of input P_{-1dB} is not the true design criterion in many receiver systems. Alternatively, a new performance parameter, the blocking P_{-1dB}, can be defined as the input power of the blocker that causes 1 dB gain compression to the small desired signal.

2.4 Third-Order Intermodulation Distortion

Due to the odd-order nonlinearities in the transfer function of the mixer, two undesired signals in the adjacent channels generate third-order intermodulation (IM_3) products at the output of mixer. As illustrated in Fig. 2.4, one of the IM_3 products can corrupt the

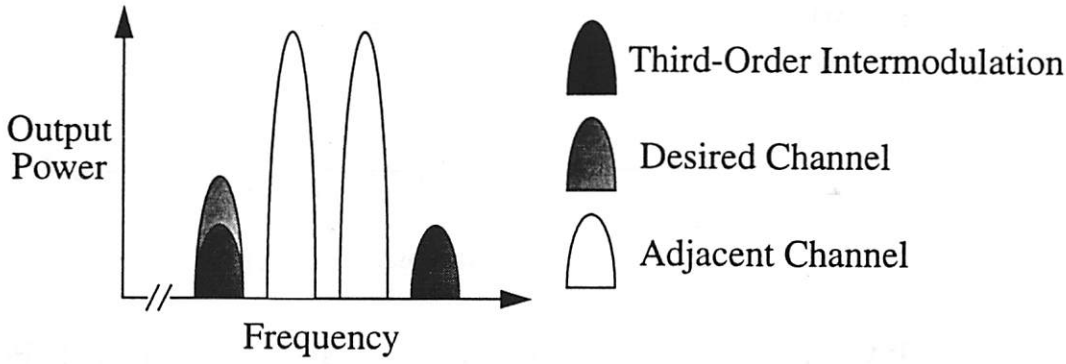

Fig. 2.4 Third-Order Intermodulation Corrupts Desired Channel

desired signal if it falls within the desired channel. If the two adjacent channel frequencies are ω_a and ω_b respectively, IM_3 products are generated at frequencies $(2\omega_a - \omega_b)$ and $(2\omega_b - \omega_a)$. At low input power level, the IM_3 product is dominated by the third-order nonlinearity. As the input power increases, higher-order nonlinearities become significant.

However, the third-order intercept point (IP_3) measures only the third-order nonlinearity. Fig. 2.5 shows the magnitude responses of the desired signal and the IM_3 product. The solid lines are the actual responses. At low input power level, the output power of the desired signal increases linearly with the input power, and the power of the IM_3 product increases with the cube of the input power. At high input power levels, the gain of the desired signal is compressed, and the IM_3 is no longer dominated by the third-order nonlinearity. The dotted lines are the linear extrapolations of the small-signal magnitude

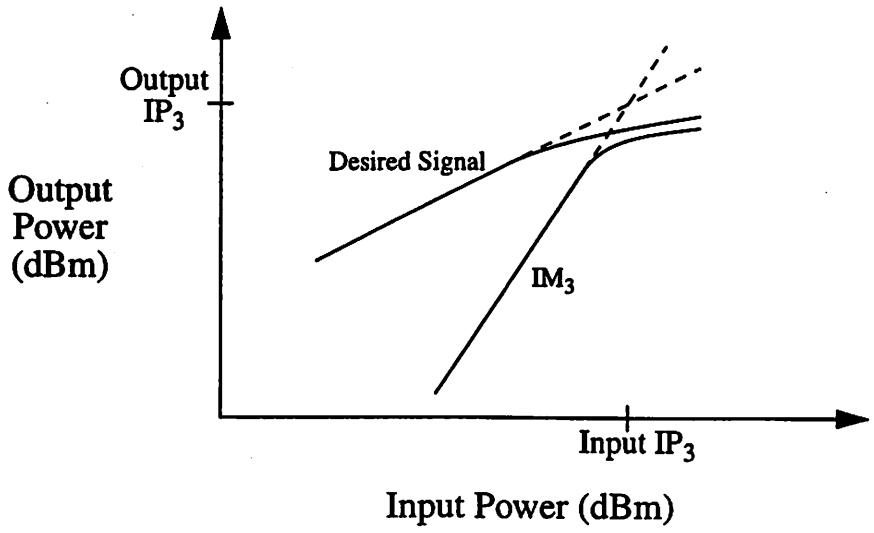

Fig. 2.5 Amplitude Responses of Desired Signal and IM_3 Product

responses of the desired signal and the IM_3 product respectively. The point where the two extrapolation curves meet is the IP_3. Given the input signal power at the adjacent channels, the power of the IM_3 product generated can be calculated by using the IP_3 value. However, the calculated value only applies to the small-signal IM_3 product since the IP_3 value is the result of extrapolation from the small-signal condition. Typically, input IP_3 is specified in receiver systems whereas output IP_3 is specified in transmitter systems. IP_3 is normally specified in dBm unit.

The system input IP_3 (in linear scale) for the downconverter shown in Fig. 1.1 is

$$IP_3 = L_{RF}\left[\frac{1}{IP_{3(LNA)}} + \frac{1}{IP_{3(MIX)}/(G_{LNA}L_{IM})}\right]^{-1}, \qquad (2.4)$$

where $IP_{3(LNA)}$ and $IP_{3(MIX)}$ are the input IP_3 (in power unit) of the LNA and downconversion mixer respectively. This equation assumes that the IM_3 contributions from the fil-

ters are negligible since they are passive components, and that the IM_3 products from the LNA and the mixer add coherently (in phase). On the other hand, if their IM_3 products add incoherently (out-of-phase), the system input IP_3 becomes

$$IP_3 = L_{RF}\left[\frac{1}{IP_{3(LNA)}^2} + \frac{1}{IP_{3(MIX)}^2/(G_{LNA}^2 L_{MIX}^2)}\right]^{-\frac{1}{2}}. \tag{2.5}$$

As shown in equations (2.4) and (2.5), increasing the gain of the LNA decreases the system input IP_3.

The numerical value of the input IP_3 is not directly related to that of the input P_{-1dB} because IP_3 measures the small-signal nonlinear condition which is dominated by the third-order nonlinearity, whereas P_{-1dB} measures the large-signal nonlinear condition which includes contributions from all odd-order nonlinearities. Furthermore, IP_3 depends on the magnitude of the third-order nonlinearity only, but P_{-1dB} depends on both the magnitude and phase of the third-order nonlinearity [2][10]. If both IP_3 and P_{-1dB} were dominated by the third-order nonlinearity, the numerical value of input IP_3 would be 9.6 dB (true for low-frequency case only) higher than that of input P_{-1dB}. In many practical designs (except the class AB mixer described in [8]), the difference between the numerical values of IP_3 and P_{-1dB} is more than 9.6 dB.

2.5 Power Consumption

The power consumption of other building blocks within a receiver system is as important as that of the downconversion mixer. While optimizing the power consumption of the mixer, care has to be taken to avoid increasing the power consumption of other

building blocks. For instance, a downconversion mixer with high NF increases the gain requirement from the LNA. This increases the power consumption of the LNA. As shown in equations (2.4) and (2.5), increasing the gain of the LNA also increases the input IP_3 requirement of the mixer in order to meet the system input IP_3 specification. This in turn increases the power consumption of the mixer (shown later in section 3.1). A mixer which requires high LO power drive increases the power consumption of the LO. It may take up to 10 mA of bias current in a LO output buffer to supply 0 dBm of LO power into the 50Ω LO port of the mixer. Reducing the conversion gain of the mixer may reduce the power consumption of the mixer, but increase the noise performance requirement of the IF stages. This may increase the power consumption of the IF stages.

2.6 Port Return Loss

The impedances of the RF and LO input ports are typically matched to 50Ω, while the impedance of the IF output port is matched to that of the IF filter. Impedance matching at the RF and IF ports is necessary to avoid signal reflection and excessive passband ripple in the frequency responses of the filters. Typically, return losses of less than -10 dB (voltage wave standing ratio of less than 2) are required. On the other hand, the return loss specification on the LO port can be more relaxed. However, excessive return loss requires the LO to deliver high power to the mixer. This would increase the power consumption of the overall system.

Any arbitrary port resistance R_p can be matched to the source resistance R_s (for input port) or load resistance R_L (for output port) using a two-element impedance-matching network. If R_p is larger than R_s (or R_L), the impedance-matching network shown in Fig. 2.6

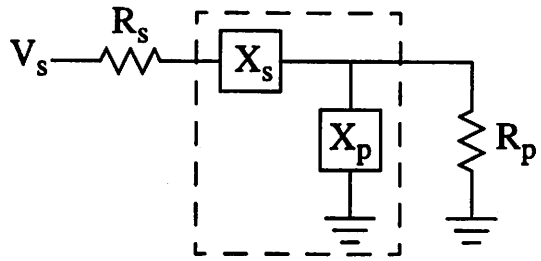

Fig. 2.6 Matching Network for R_p larger than R_s

can be used. The reactive elements X_s and X_p are used for impedance transformation. The quality factor (Q) of the network is given by

$$Q_N = \sqrt{\frac{R_p}{R_s} - 1} \ . \tag{2.6}$$

The value of Q_N specifies the Q of X_p in parallel with R_p and the Q of X_s in series with R_s. In other words,

$$Q_N = \frac{R_p}{|X_p|} = \frac{|X_s|}{R_s} \ .$$

The reactive elements X_s and X_p can be implemented by either inductors or capacitors. However, if X_s is capacitive, X_p has to be inductive. Similarly, if X_s is inductive, X_p has to be capacitive. The difference between these two configurations is that one is a lowpass network while the other one is a highpass network. If the port impedance is not purely resistive, the reactive part of the port impedance can be tuned out by a reactive element, or absorbed into the matching network.

The sensitivity of the network to component variations depends on the Q of the network, but not the Q of the reactive elements (X_s and X_p). Hence, if the resistance differ-

ence between R_p and R_s is very large (Q_N is large), the network is very sensitive to component variations. In this case, a two-stage matching network shown in Fig. 2.7 can be

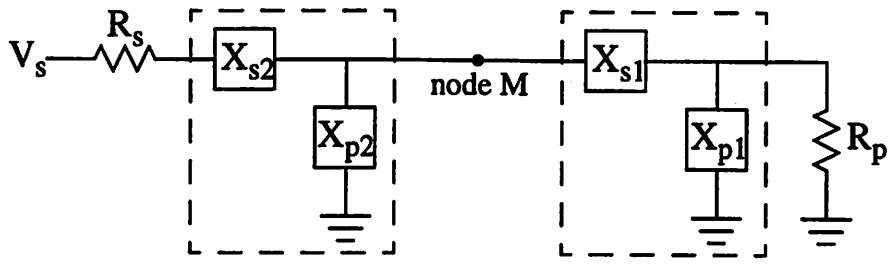

Fig. 2.7 Two-Stage Matching Network for R_p larger than R_s

used to transform the impedance of R_p to an intermediate value at node M before it is transformed to match the value of R_s. To minimize the sensitivity, the optimal equivalent resistance at node M should be equal to the geometric mean of R_s and R_p. The same concept can be extended to multi-stage impedance-matching network.

The reactive elements (X_s and X_p) of the impedance-matching network can be implemented by either on-chip or external components. However, the Q of the reactive elements determines the power loss across the network. Typically, on-chip reactive components have lower Q (due to parasitic series resistance and substrate loss) than external components.

If the R_p is smaller than the R_s (or R_L), the impedance-matching network shown in Fig. 2.8 can be used. In this case, the quality factor (Q) of the network is given by

$$Q_N = \sqrt{\frac{R_s}{R_p} - 1} \tag{2.7}$$

The value of Q_N specifies the Q of X_p in series with R_p and the Q of X_s in parallel with R_s.

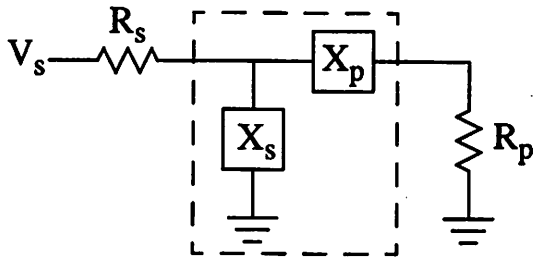

Fig. 2.8 Matching Network for R_p smaller than R_s

2.7 Port Isolation

If the downconversion mixer is in a different package from the LNA, the isolation between LO and RF ports of the mixer is important, as LO-to-RF feedthrough results in LO signal leaking through the antenna. The amount of feedthrough signal that is allowed depends on the reverse isolation of the LNA, and the stopband attenuation of the RF and image-rejection filters at the LO frequency. If the LNA is in the same package as the mixer, the LO feedthrough to RF input port of the LNA becomes more important. LO-to-IF and RF-to-IF isolations are not important because the high-frequency feedthrough signals can be rejected easily by the high-Q IF filter. However, large LO and RF feedthrough signals at the IF output port may saturate the IF output port, and decrease the P_{-1dB} of the mixer.

CHAPTER 3

Design and Optimization Techniques

3.1 Third-Order Intermodulation Distortion

As shown in Fig. 1.2 and Fig. 1.3, the downconversion mixer is composed of a driver stage and a differential switching stage. Both the driver stage and the differential switching stage (switching pair in single-balanced mixer and switching quad in double-balanced mixer) contribute third-order intermodulation (IM_3) products to the IF output of the mixer. A common-emitter transconductance stage and a differential-pair transconductance stage are used as the driver stages for the single-balanced (Fig. 1.2) and double-balanced (Fig. 1.3) mixers respectively. In this section, analytical equations (in Volterra Series [2][3]) describing the high-frequency IM_3 performance of both common-emitter and differential-pair transconductance stages are derived [10], and their implications are discussed. Using these equations, design and optimization techniques to improve the linearity of the driver stages can be formulated. On the other hand, the IM_3 distortion of the switching stage is difficult to describe analytically. Instead, design and optimization techniques for improving the linearity of the switching stage is discussed in a qualitative way using the materials from Hull's thesis [11].

The bipolar-transistor common-emitter and differential-pair transconductance stages shown in Fig. 3.1 and Fig. 3.2 respectively are commonly used in many RF building blocks, such as low-noise amplifiers (LNA) and mixers. To improve the linearity, the

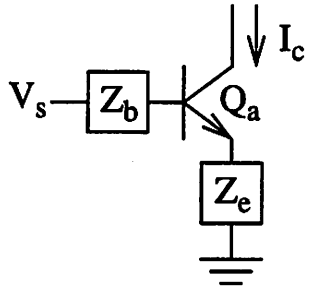

Fig. 3.1. Common-Emitter Transconductance Stage

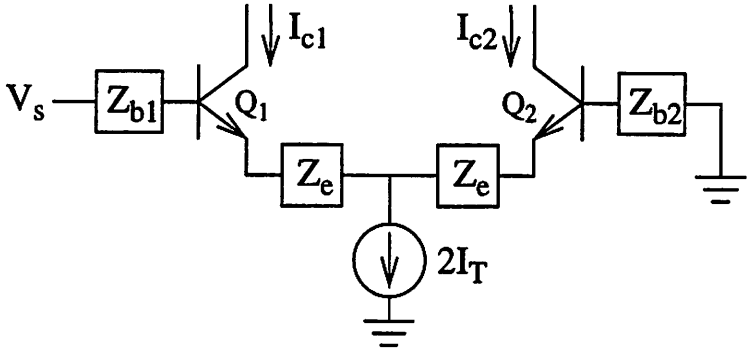

Fig. 3.2. Differential-Pair Transconductance Stage

transconductance stages are usually degenerated by an impedance Z_e, which can be implemented by using either resistors, capacitors or inductors.

Fig. 3.3 shows the large-signal model used to derive the nonlinearity equations for

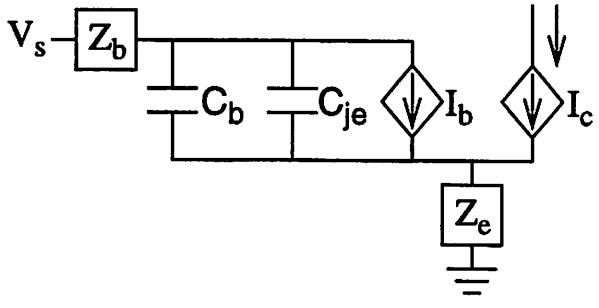

Fig. 3.3. Model of Common-Emitter Transconductance Stage

the common-emitter transconductance stage shown in Fig. 3.1. This model ignores the effect of base-collector junction capacitance (C_μ) of Q_a. Inclusion of C_μ greatly complicates the analysis without adding significant accuracy to the results in typical situations. V_s is the voltage signal source. Z_b is the impedance at the base of Q_a which includes source resistance (R_s), base resistance (r_b) of Q_a, shunt impedance of bias circuit and impedance of impedance-matching network. Z_e is the impedance at the emitter of Q_a which includes the parasitic emitter resistance (r_e) of Q_a and the impedance of the degeneration elements (resistor, capacitor and/or inductor). C_b is the base-charging capacitance of Q_a, which is linearly proportional to the collector current (I_c) and the forward transit time (τ_F) of Q_a. C_{je} is the base-emitter junction capacitance which is assumed to be constant in this model. I_b is the base current, which is equal to $\frac{I_c}{\beta_0}$, where β_0 is the small-signal low-frequency current gain of Q_a. I_b cannot be ignored, since the high-frequency nonlinearity also depends on the low-frequency characteristics of Q_a (this will become obvious later).

Using the model in Fig. 3.3, a Kirchhoff's Voltage Law equation can be written as

$$V_s = (sC_{je}V_\pi + s\tau_F I_c + I_c/\beta_0)(Z_b + Z_e) + I_c Z_e + V_\pi \ , \qquad (3.1)$$

where I_c is the collector signal current (collector current minus bias current), V_π is the base-emitter signal voltage drop across C_b and C_{je}, and s (= $j\omega$) is the Laplace Transform Variable. Solving this equation (derivation is shown in Appendix A) results in the following Volterra Series expression

$$I_c = A_1(s) \circ V_s + A_2(s_1, s_2) \circ V_s^2 + A_3(s_1, s_2, s_3) \circ V_s^3 + \dots \ , \qquad (3.2)$$

where V_s^n is the n'th power of the voltage source signal, and $A_n()$ is the Volterra Series Coefficient, which is a linear function of 'n' number of frequencies. The operator 'o' indicates multiplying each frequency component in V_s^n by the magnitude of $A_n()$ and shifting each frequency component in V_s^n by the phase of $A_n()$. The first three Volterra Series Coefficients are

$$A_1(s) = \frac{g_m}{[sC_{je}Z(s) + s\tau_F g_m Z(s) + g_m Z(s)/\beta_0 + 1 + g_m Z_e(s)]} , \tag{3.3}$$

$$A_2(s_1, s_2) = A_1(s_1 + s_2)A_1(s_1)A_1(s_2)\frac{V_T}{2I_Q^2}[1 + (s_1 + s_2)C_{je}Z(s_1 + s_2)] , \text{ and} \tag{3.4}$$

$$\begin{aligned} A_3(s_1, s_2, s_3) = {} & A_1(s_1 + s_2 + s_3)\frac{V_T}{3I_Q^3}[-A_1(s_1)A_1(s_2)A_1(s_3) + 3I_Q\overline{A_1A_2}] \\ & \times [1 + (s_1 + s_2 + s_3)C_{je}Z(s_1 + s_2 + s_3)] , \end{aligned} \tag{3.5}$$

where

$$Z(s) = Z_b(s) + Z_e(s) ,$$

$$\overline{A_1A_2} = \frac{A_1(s_1)A_2(s_2, s_3) + A_1(s_2)A_2(s_1, s_3) + A_1(s_3)A_2(s_1, s_2)}{3} ,$$

$$g_m = \frac{I_Q}{V_T} ,$$

I_Q is the bias current of Q_a, and V_T is the thermal voltage. The coefficient $A_1(s)$ is the small-signal transconductance of the transconductance stage.

The IM_3 product at frequency $(2\omega_a - \omega_b)$ can calculated by using the Volterra Series Coefficient $A_3(s_1,s_2,s_3)$, and letting $s_1 = s_a$, $s_2 = s_a$ and $s_3 = -s_b$. Similarly, the IM_3 product

at frequency $(2\omega_b - \omega_a)$ can calculated by letting $s_1 = s_b$, $s_2 = s_b$ and $s_3 = -s_a$. Typically, the frequency difference between ω_a and ω_b is so small that $s \approx s_a \approx s_b$ can be assumed. Using two input signals of the same amplitude V_s, the magnitude ($|IM_3|$) of the input-referred IM_3 products (the two IM_3 products have about the same magnitude) of the common-emitter transconductance stage is given by

$$
\begin{aligned}
|IM_3| &= \left|\frac{3}{4}\frac{A_3(s_a, s_a, -s_b)}{A_1(2s_a - s_b)}\right| |V_s|^2 \\
&\approx \left|\frac{A_1(s)}{I_Q}\right|^3 \left|\frac{V_T}{4}[1 + sC_{je}Z(s)]\left\{-1 + \frac{A_1(\Delta s)}{g_m}[1 + \Delta s C_{je} Z(\Delta s)]\right.\right. \\
&\quad \left.\left. + \frac{A_1(2s)}{2g_m}[1 + 2sC_{je}Z(2s)]\right\}\right| |V_s|^2
\end{aligned}
\tag{3.6}
$$

where $\Delta s = (s_a - s_b) << s$.

The $|IM_3|$ depends on the magnitude of

$$[1 + sC_{je}Z_b(s) + sC_{je}Z_e(s)] \; . \tag{3.7}$$

With inductive degeneration, the $[sC_{je}Z_e(s)]$ term is a negative real number which cancels the '1' term in (3.7) . partially. There is no such cancellation with resistive degeneration, since the $[sC_{je}Z_e(s)]$ term is a positive imaginary number, which adds to the imaginary part of the $[sC_{je}Z_b(s)]$ term in (3.7) .. For the same reason, capacitive degeneration would increase the $|IM_3|$ because the $[sC_{je}Z_e(s)]$ term is a positive real number, which adds to the '1' term in (3.7) ..

The $|IM_3|$ also depends on the magnitude of

$$\left\{-1+\frac{A_1(\Delta s)}{g_m}[1+\Delta sC_{je}Z(\Delta s)]+\frac{A_1(2s)}{2g_m}[1+2sC_{je}Z(2s)]\right\}, \tag{3.8}$$

where the '-1' and $\left\{\frac{A_1(\Delta s)}{g_m}[1+\Delta sC_{je}Z(\Delta s)]+\frac{A_1(2s)}{2g_m}[1+2sC_{je}Z(2s)]\right\}$ terms come from the third-order nonlinearity ($A_1A_1A_1$) and the second-order interaction ($\overline{A_1A_2}$) respectively. Using the approximation (for practical design values),

$$[1+\Delta sC_{je}Z(\Delta s)]\approx 1\ ,$$

equation (3.6) can be simplified to

$$|IM_3|\approx\left|\frac{A_1(s)}{I_Q}\right|^3\left|\frac{V_T}{4}[1+sC_{je}Z(s)]\left[-1+\frac{A_1(\Delta s)}{g_m}+\frac{A_1(2s)}{2g_m}[1+2sC_{je}Z(2s)]\right]\right||V_s|^2 \tag{3.9}$$

where the value of the $\left\{\frac{A_1(2s)}{2g_m}[1+2sC_{je}Z(2s)]\right\}$ term is typically small, compared to the value of the $\left[\frac{A_1(\Delta s)}{g_m}\right]$ term. However, it is not so small that it can be ignored.

As shown in equation (3.9), the $|IM_3|$ is independent of τ_F if the small-signal transconductance $[A_1(s)]$ is kept constant. On the other hand, it increases with C_{je} for the resistive and capacitive degeneration cases because the $[sC_{je}Z_e(s)]$ term is a positive imaginary number and a positive real number respectively, but decreases with C_{je} for the inductive degeneration case because the $[sC_{je}Z_e(s)]$ term is a negative real number. Furthermore, the $|IM_3|$ is proportional to the cube of the ratio of small-signal transconductance $[A_1(s)]$ to bias current (I_Q).

The $|IM_3|$ can be lowered by increasing the $[A_1(\Delta s)]$ term. This increases the second-order interaction to cancel the third-order nonlinearity. Since the degeneration inductor has low impedance at low frequency, the $[A_1(\Delta s)]$ term in the inductive degeneration case is much larger than those in the resistive and capacitive degeneration cases. Similarly, the capacitor has high impedance at low frequency, and hence the $[A_1(\Delta s)]$ term in the capacitive degeneration case is much smaller than that in the resistive degeneration case. This is the second reason why the inductively degenerated transconductance stage is more linear than the resistively degenerated transconductance stage, which in turn is more linear than the capacitive degenerated transconductance stage with the same transconductance and bias current.

Fig. 3.4 shows the basic topology of a typical common-emitter transconductance

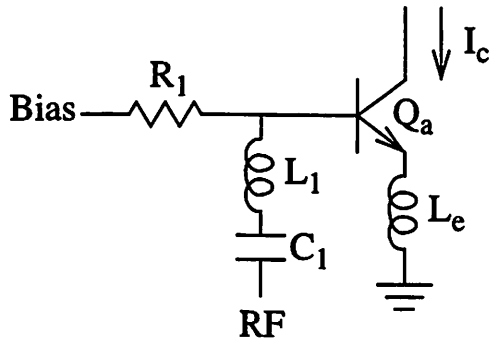

Fig. 3.4 Common-Emitter Transconductance Stage with Inductive Degeneration

stage with inductive degeneration. The degeneration inductor L_e is typically implemented by bond wires in series with package pins. C_1 serves as a DC blocking capacitor. It is also used to tune out the bond wire inductance L_1. R_1 is a bias resistor used to isolate the bias circuit from the RF port. At low frequency (Δs), the impedance of $[Z_e(\Delta s)]$ ($\approx \Delta s L_e$) is

negligible. The impedance of $[Z_b(\Delta s)]$ is dominated by the bias resistor R_1 since the blocking capacitor C_1 has high impedance at low frequency. In this case, the $\left[\frac{A_1(\Delta s)}{g_m}\right]$ term in equation can be simplified to

$$\frac{A_1(\Delta s)}{g_m} \approx \frac{r_\pi}{r_\pi + R_1}, \tag{3.10}$$

where r_π is the small-signal base-emitter resistance of Q_a. Therefore, in order to increase the linearity (reduce $|IM_3|$), R_1 should be kept small (relative to r_π) to increase the second-order interaction. However, R_1 has to be large enough avoid significant loading on the RF input port, which would cause impedance mismatch and noise figure degradation.

Fig. 3.5 shows the simulated (using HSPICE) and analytical [using equation (3.6)]

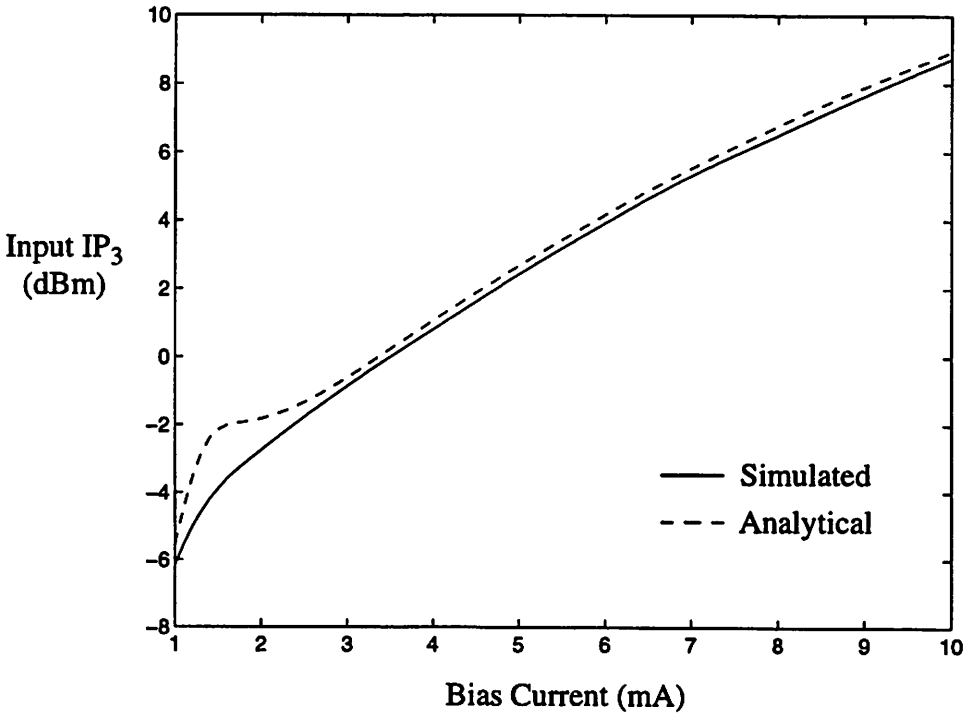

Fig. 3.5 Input Third-Order Intercept Point versus Bias Current

input IP_3 of the common-emitter transconductance stage shown in Fig. 3.4 as a function of bias current (I_Q). The simulation results include the nonlinear effects of C_μ and C_{je} of Q_a. Neglecting these effects does not seem to introduce significant errors in the analytical equation. The two RF sinusoidal signals used are at 900 MHz and 910 MHz respectively. The component values used are: τ_F=10.5 pF, C_{je}=1.17 pF, β=73, L_e=2.4 nH, L_1=3.5 nH C_1=20 pF, R_1=150Ω.

Similarly, the model shown in Fig. 3.6 is used to derive the nonlinearity equations

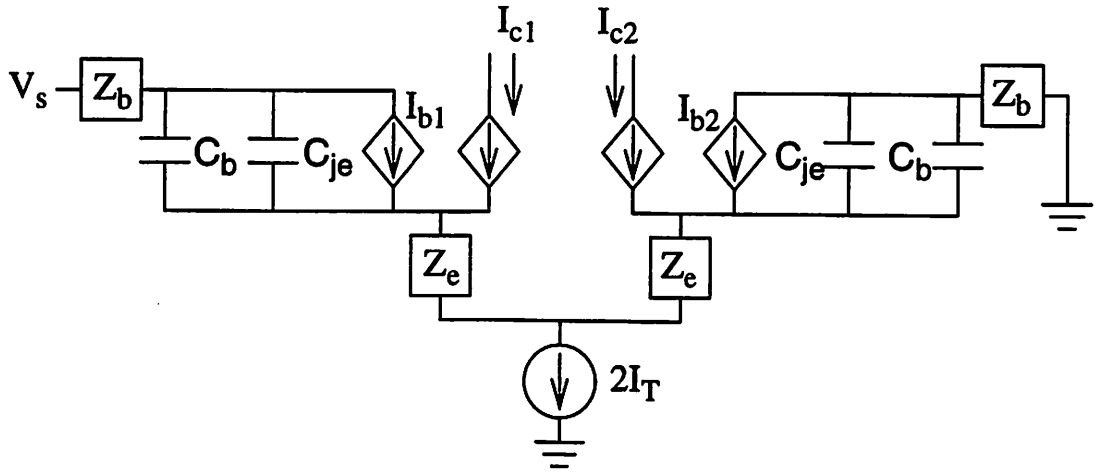

Fig. 3.6 Model of Differential-Pair Transconductance Stage

for the differential-pair transconductance stage shown in Fig. 3.2. This model ignores the effect of the base-collector junction capacitance (C_μ) of Q_1 and Q_2. The base impedance ($Z_{b1} + Z_{b2}$) in Fig. 3.2 is split into two Z_b's in Fig. 3.6 to simplify the derivation by exploiting symmetry. There is no loss of generality in this manipulation if the tail current source ($2I_T$) has infinite output impedance. Using the model in Fig. 3.6, Kirchhoff's Voltage Law and Kirchhoff's Current Law equations can be written as

$$V_s = (sC_{je}V_{\pi 1} + s\tau_F I_{c1} + I_{c1}/\beta_0)(Z_b + Z_e) + I_{c1}Z_e + V_{\pi 1}$$
$$- (sC_{je}V_{\pi 2} + s\tau_F I_{c2} + I_{c2}/\beta_0)(Z_b + Z_e) - I_{c2}Z_e - V_{\pi 2} \ , \qquad (3.11)$$

$$0 = sC_{je}V_{\pi 1} + s\tau_F I_{c1} + I_{c1}/\beta_0 + I_{c1} + sC_{je}V_{\pi 2} + s\tau_F I_{c2} + I_{c2}/\beta_0 + I_{c2} \qquad (3.12)$$

respectively, where I_{c1} and I_{c2} are collector signal currents of Q_1 and Q_2 respectively, $V_{\pi 1}$ and $V_{\pi 2}$ are signal voltage drops across the base-emitter junctions of Q_1 and Q_2 respectively. Solving the simultaneous equations (3.11) and (3.12) results in the following Volterra Series expressions (derivation is shown in Appendix A).

$$I_{c1} = B_1(s) \circ V_s + B_2(s_1, s_2) \circ V_s^2 + B_3(s_1, s_2, s_3) \circ V_s^3 + \ldots \ , \text{and} \qquad (3.13)$$

$$I_{c2} = -B_1(s) \circ V_s + B_2(s_1, s_2) \circ V_s^2 - B_3(s_1, s_2, s_3) \circ V_s^3 + \ldots \ , \qquad (3.14)$$

where

$$B_1(s) = \frac{g_m}{2[sC_{je}Z(s) + s\tau_F g_m Z(s) + g_m Z(s)/\beta_0 + 1 + g_m Z_e(s)]} \ , \qquad (3.15)$$

$$B_2(s_1, s_2) = B_1(s_1)B_1(s_2)\frac{(s_1 + s_2)C_{je}}{2I_T[(s_1 + s_2)C_{je} + (s_1 + s_2)g_m\tau_F + g_m/\beta_0 + g_m]} \ , \qquad (3.16)$$

$$B_3(s_1, s_2, s_3) = 2B_1(s_1 + s_2 + s_3)\frac{V_T}{3I_T^3}[-B_1(s_1)B_1(s_2)B_1(s_3) + 3I_Q\overline{B_1B_2}]$$
$$\times [1 + (s_1 + s_2 + s_3)C_{je}Z(s_1 + s_2 + s_3)] \ , \qquad (3.17)$$

$$Z(s) = Z_b(s) + Z_e(s) \ , \text{and}$$

$$g_m = \frac{I_T}{V_T} \ .$$

The $|IM_3|$ (by taking either single-ended or differential output) is given by

$$|IM_3| = \left|\frac{B_1(s)}{I_T}\right|^3 \left|\frac{V_T}{2}[1 + sC_{je}Z(s)]\left[-1 + \frac{\Delta sC_{je}}{\Delta sC_{je} + \Delta sg_m\tau_F + g_m/\beta_0 + g_m}\right.\right. \quad (3.18)$$
$$\left.\left. + \frac{sC_{je}}{2sC_{je} + 2sg_m\tau_F + g_m/\beta_0 + g_m}\right]\right| |V_s|^2$$

The $|IM_3|$ depends on the magnitude of

$$[1 + sC_{je}Z_b(s) + sC_{je}Z_e(s)] ,$$

and hence the differential-pair transconductance stage with inductive degeneration is more linear than that with resistive degeneration, which in turn is more linear than that with capacitive degeneration. The $|IM_3|$ also depends on the magnitude of

$$\left[-1 + \frac{\Delta sC_{je}}{\Delta sC_{je} + \Delta sg_m\tau_F + g_m/\beta_0 + g_m} + \frac{sC_{je}}{2sC_{je} + 2sg_m\tau_F + g_m/\beta_0 + g_m}\right] \quad (3.19)$$

where the $\left\{\frac{\Delta sC_{je}}{\Delta sC_{je} + \Delta sg_m\tau_F + g_m/\beta_0 + g_m} + \frac{sC_{je}}{2sC_{je} + 2sg_m\tau_F + g_m/\beta_0 + g_m}\right\}$ and '-1' terms come from the second-order interaction ($\overline{B_1B_2}$) and the third-order nonlinearity ($B_1B_1B_1$) respectively. The term (3.19) is independent of the degeneration impedance used, and typically dominated by the third-order nonlinearity. Hence, equation (3.18) can be simplified to

$$|IM_3| \approx \left|B_1^3(s)\frac{V_T}{2I_T^3}[1 + sC_{je}Z(s)]\right| |V_s|^2 . \quad (3.20)$$

Comparing equation (3.20) with equation (3.9) of the common-emitter transconductance stage, we notice that the $|IM_3|$ of the differential-pair transconductance stage is at least twice as large as that of the common-emitter transconductance stage with the same

bias current and transconductance (in this case, $\left|\frac{A_1(s)}{I_Q}\right| = \left|\frac{B_1(s)}{I_T}\right|$). This condition can only be satisfied when degeneration is used. Without degeneration, common-emitter and differential-pair transconductance stages cannot have the same bias current and transconductance simultaneously. Without degeneration, we have $\frac{1}{2}\left|\frac{A_1(s)}{I_Q}\right| = \left|\frac{B_1(s)}{I_T}\right|$, and hence the $|IM_3|$ of the common-emitter transconductance stage is twice as large as that of the differential-pair transconductance stage without degeneration.

Besides the driver stage, the differential switching stage (switching pair in single-balanced mixer and switching quad in double-balanced mixer) of a mixer also contributes IM_3 products to the output of the mixer. Generally, the linearity of the switching stage increases with the LO signal amplitude driving the switching stage because large LO signal amplitudes reduce the duration when both sides of the switching stage are active. When one side of the switching stage is active, the mixer is similar to a cascode amplifier, and the cascode transistors contribute little nonlinearity. However, switching the base-emitter junction capacitors (C_{je}) of the switching stage results in excessive current being pumped into the common-emitter points of the switching stage through the C_{je} [11][12]. This phenomenon generates additional IM_3 products. Therefore, the linearity of the switching stage decreases with LO signal amplitude at very large LO signal amplitude levels.

Similarly, increasing the device size results in increased C_{je}, which decreases the linearity of the switching stage. However, if the device sizes are too small (r_b is large), exces-

sive voltage drop across r_b reduces the effective LO signal amplitude driving the switching stage. Therefore, the size of the devices in the switching stage should be small enough to reduce C_{je}, but large enough to reduce r_b.

Both the driver stage and the differential switching stage contribute IM_3 products to the IF output of the mixer. When the device f_T is much higher (more than 10 times) than the LO frequency and reasonably large LO signal amplitude (> 0.1V) is used to drive the switching stage, the IM_3 distortion of the mixer is dominated by the nonlinearity contribution from the driver stage because the switching stage can be switched very rapidly and the C_{je} can be kept small. On the other hand, the IM_3 distortion of the mixer is typically dominated by the nonlinearity contribution from the switching stage when the device f_T is low, relative to the LO frequency. These two different cases are demonstrated in the two design examples presented in CHAPTER 4.

3.2 Class AB Behavior

Without resistive or DC feedback, the common-emitter transconductance stage shown in Fig. 3.4 also exhibits a class AB behavior [8][13]. This phenomenon is caused by the nonlinear characteristics of the active device (Q_a shown in Fig. 3.4) used, which is can be either bipolar or field effect transistor. If the output current of the driver stage is represented as

$$I_{out} = I_0 + I_1\cos\omega t + I_2\cos 2\omega t + I_3\cos 3\omega t + \dots , \qquad (3.21)$$

where I_n is the amplitude of the n'th harmonic, I_0 is the average current and $I_1\cos\omega t$ is the desired signal current. In a class A design (such as differential-pair transconductance stage

with a constant tail current source shown in Fig. 3.2), the average current (I_0) is the same as the bias current used in the design, and the signal current amplitude (I_1) has be smaller than the bias current. As a result, the input 1 dB compression point (P_{-1dB}) and gain requirements set a lower limit on the bias current. On the other hand, the signal current amplitude (I_1) in a class AB design can increase beyond the bias current.

Fig. 3.7 shows the simulated (using HSPICE) signal current amplitude (I_1) and the

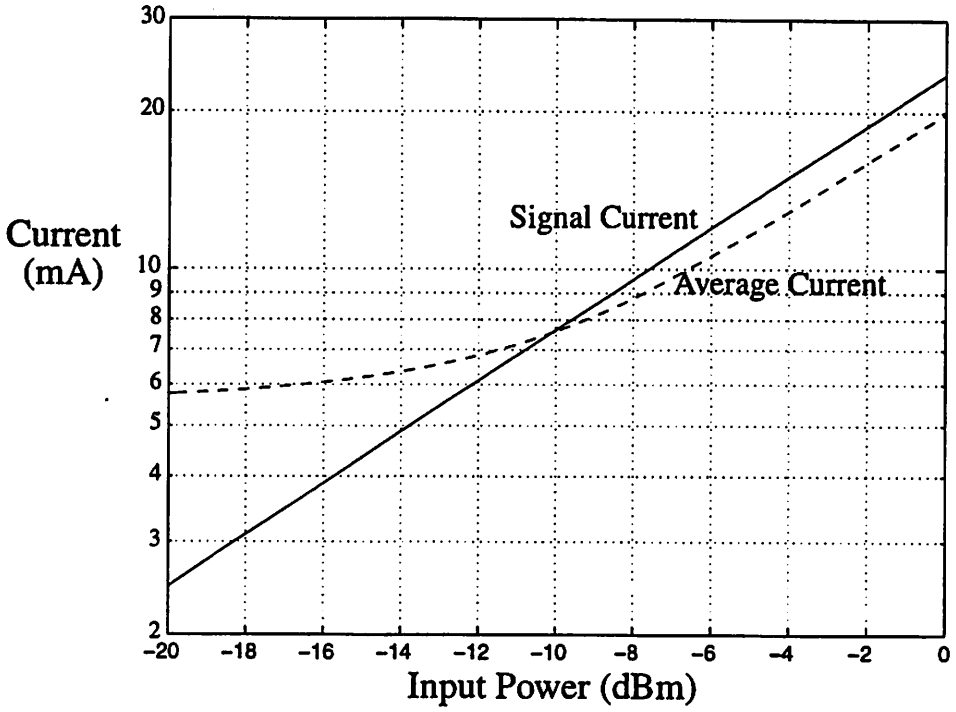

Fig. 3.7. Simulated Output Currents of Class AB Transconductance Stage versus Input Power

average current (I_0) of a the class AB transconductance stage (biased at a collector current of 5.6 mA) shown in Fig. 3.4 as a function of RF input power. The RF input signal is a sinusoidal waveform at 900 MHz. The increase of signal current amplitude and average current beyond the bias current is caused by the nonlinearities of the active device used.

Fig. 3.8 shows the simulated output current waveform of the transconductance stage with

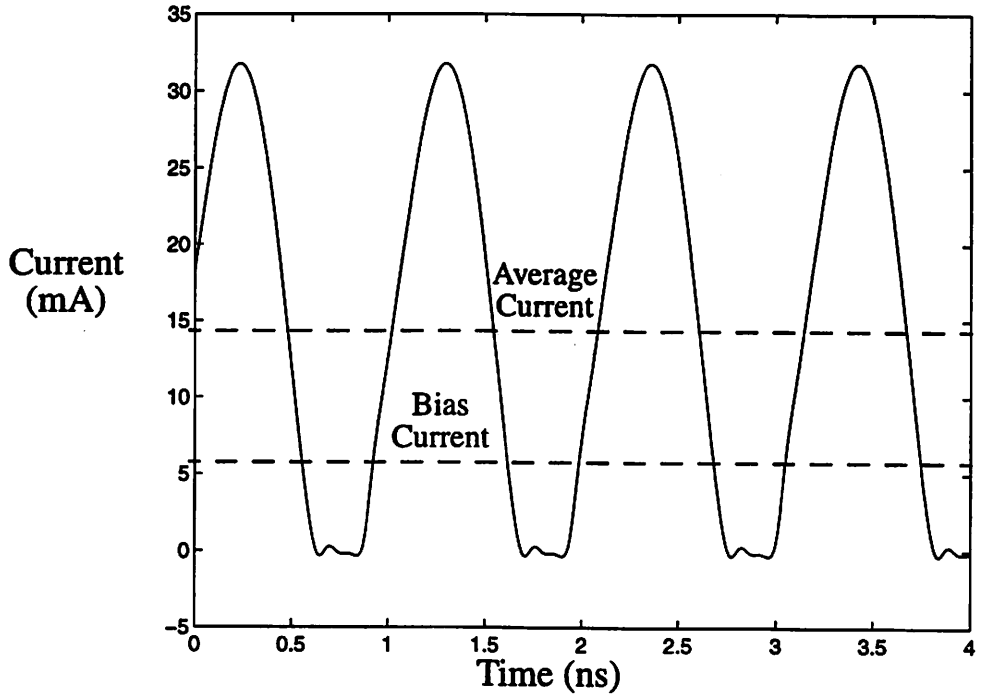

Fig. 3.8. Simulated Output Current of Class AB Transconductance Stage

a -3 dBm input signal applied to its RF input. Due to the class AB phenomenon, the signal current amplitude (I1) and the average current increase to 16.7 mA and 14.4 mA respectively.

Unlike a class A design, which has to be biased with large current to handle large input signal power, class AB design can be biased with smaller current because the signal current amplitude (I_1) can increase beyond the bias current when the input signal power is large. Thus, power is conserved in a class AB design when the input signal power is small. At large input signal power levels, the signal current amplitude (I_1) in a class AB design is larger than the average current (I_0). Therefore, class AB design is more power efficient than class A design at both small and large input power levels.

Fig. 3.9 shows simulated normalized transconductance (normalized to small-signal

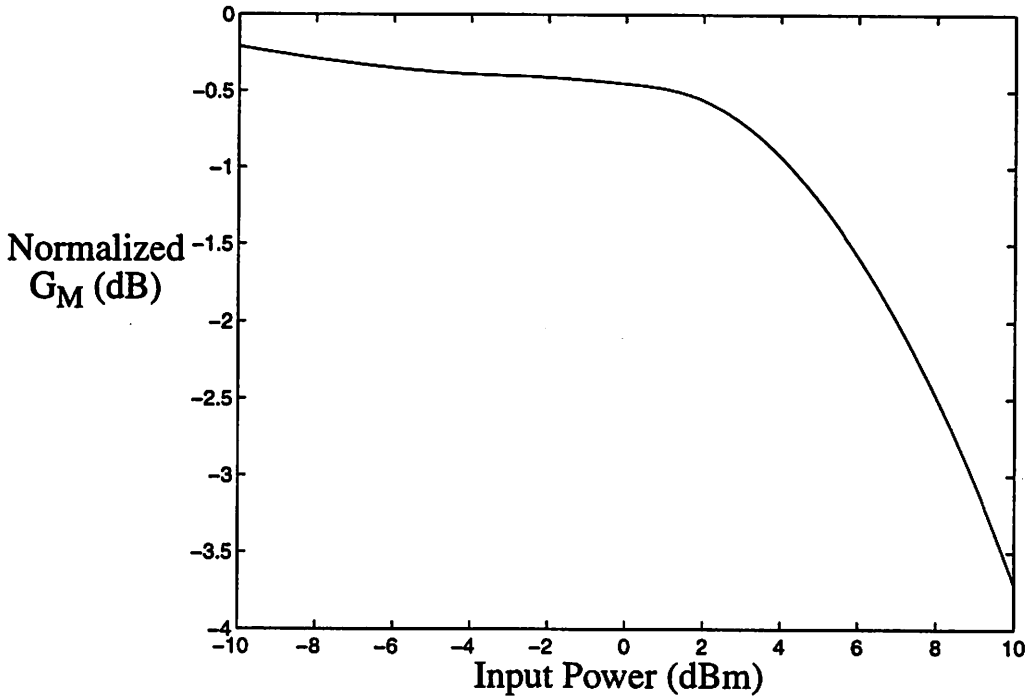

Fig. 3.9. Normalized Transconductance of Class AB Transconductance Stage versus Input Power

transconductance) of the class AB transconductance stage as a function of RF input power. Simulation shows that the driver stage has an input P_{-1dB} of 4 dBm. For a class A design biased at the same collector current, the input P_{-1dB} would be less than -12 dBm because the signal current amplitude (I_1) has to be smaller than the bias current. Similarly, a class A design with the same transconductance and input P_{-1dB} would require a bias current of more than 40 mA.

Due to the increase in average (DC) current as input signal power increases, the presence of DC (resistive) feedback in the common-emitter transconductance stage can suppress the class AB behavior. Without any DC feedback components, the transconductance

of the class AB transconductance stage is not compressed, even at very high input power levels (> 10 dBm). To avoid gain compression caused by the DC feedback, the bias resistors R_1 and the parasitic resistor at the emitter of Q_a should be minimized. However, R_1 should be large enough to avoid significant loading at the RF input port, which would cause impedance mismatch and noise figure degradation.

The nonlinearity equations derived in section 3.1 can be used to explain the class AB behavior [10]. The Volterra Series method is effective in predicting distortion in weakly nonlinear condition such as the small-signal IM_3 distortion (measured by third-order intercept point) which is dominated by the first three Volterra Series terms. When larger signals are applied, more terms are needed in the series, and the derivation becomes cumbersome. Nevertheless, the analysis of the weakly nonlinear condition, described in the previous section, can provide insights into class AB behavior.

Gain compression under large-signal conditions is caused by all the odd-order terms in the Volterra Series. Assuming that gain compression is dominated by the third-order terms, the large-signal transconductance of the common-emitter transconductance stage shown in Fig. 3.1 can be calculated by using the Volterra Series Coefficient $A_3(s_1,s_2,s_3)$ from equation (3.5) and letting $s_1 = s$, $s_2 = s$, $s_3 = -s$, where s is the signal frequency. Hence, the normalized transconductance (normalized to small-signal transconductance) of a common-emitter transconductance stage is given by

$$
\begin{aligned}
|G_M| &= \left|\frac{A_1(s)V_s + \frac{3}{4}A_3(s,s,-s)V_s^3}{A_1(s)V_s}\right| \\
&= \left|1 + \frac{3}{4}\frac{A_3(s,s,-s)}{A_1(s)}V_s^2\right| \\
&\approx \left|1 + A_1^2(s)A_1(-s)\frac{V_T}{4I_Q^3}[1 + sC_{je}Z(s)]\left\{-1 + \frac{A_1(0)}{g_m}\right.\right. \\
&\quad \left.\left. + \frac{A_1(2s)}{2g_m}[1 + 2sC_{je}Z(2s)]\right\}V_s^2\right|
\end{aligned}
\quad . \qquad (3.22)
$$

Gain compression is caused by

$$
A_1^2(s)A_1(-s)\frac{V_T}{4I_Q^3}[1 + sC_{je}Z(s)]\left\{-1 + \frac{A_1(0)}{g_m} + \frac{A_1(2s)}{2g_m}[1 + 2sC_{je}Z(2s)]\right\}V_s^2 \ , \qquad (3.23)
$$

within which $\left\{-1 + \frac{A_1(0)}{g_m} + \frac{A_1(2s)}{2g_m}[1 + 2sC_{je}Z(2s)]\right\}$ has a negative sign because $\left\{\frac{A_1(0)}{g_m} + \frac{A_1(2s)}{2g_m}[1 + 2sC_{je}Z(2s)]\right\}$ is typically less than 1. With resistive degeneration, $A_1(s)$ is mostly real, and hence the term (3.23) is mostly a negative real number, which causes gain compression. On the other hand, the term (3.23) for the inductive degeneration case is a complex number of which the imaginary part is not negligible. As a result, the real part causes gain compression, but the imaginary part causes gain expansion (with phase shift). Although both $|IM_3|$ and gain compression depend on $\left[\frac{A_3(s,s,-s)}{A_1(s)}\right]$, the

$|IM_3|$ depends on the magnitude of $\left[\frac{A_3(s, s, -s)}{A_1(s)}\right]$ whereas the gain compression depends on both amplitude and phase of $\left[\frac{A_3(s, s, -s)}{A_1(s)}\right]$.

Furthermore, the second-order interaction can be increased to cancel the third-order nonlinearity partially in the inductive degeneration case by increasing the $\left[\frac{A_1(0)}{g_m}\right]$ term. Since this term depends on R_1 as shown in equation (3.10), R_1 should be kept smaller than r_π of Q_a in order to increase the second-order interaction (to reduce gain compression). In other words, R_1 should be small enough to avoid suppressing the class AB behavior.

Increasing the $\left[\frac{A_1(0)}{g_m}\right]$ term also increases the average current. The increase in average current under large signal condition is caused by all the even-order terms in the Volterra Series. Assuming that the increase in average current is dominated by the second-order term, the average current can be calculated by using the Volterra Series Coefficient $A_2(s_1,s_2)$ from equation (3.4) and letting $s_1 = s$, $s_2 = -s$. The magnitude of the average current is given by

$$|I_{ave}| = \left| I_Q + \left[\frac{1}{2}A_1(0)A_1(s)A_1(-s)\frac{V_T}{2I_Q^2}\right]V_s^2 \right| , \qquad (3.24)$$

which depends on the $[A_1(0)]$ term. Fig. 3.10 shows the simulated (using HSPICE) and analytical [using equation (3.24)] average current of the common-emitter transconductance stage shown in Fig. 3.4 as a function of RF input power. As expected, the deviation between the analytical and simulated results increases as the RF input power increases

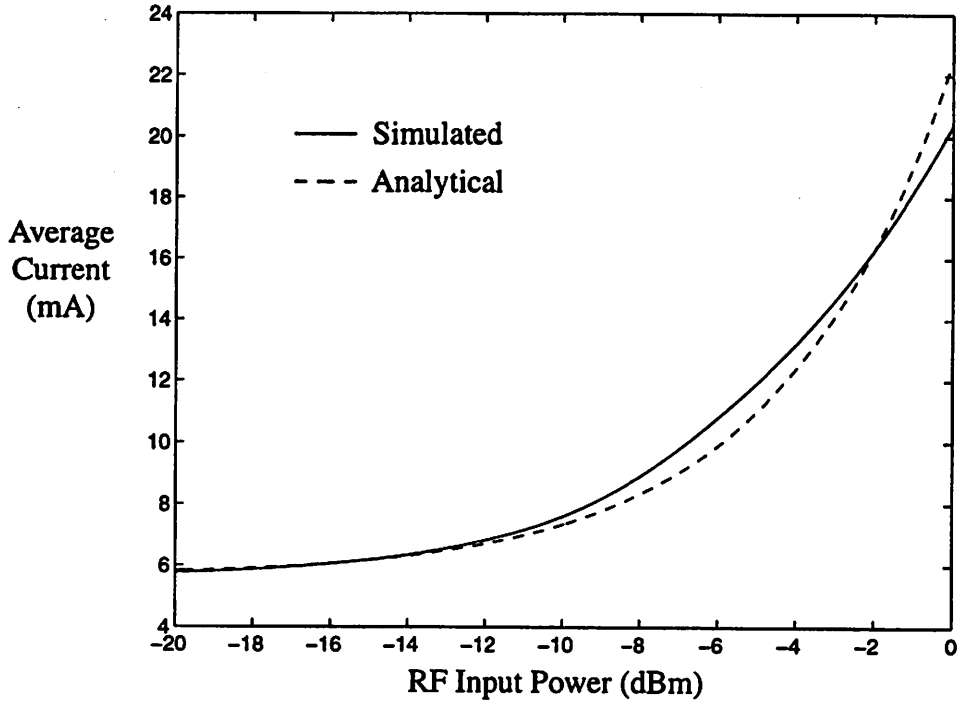

Fig. 3.10. Average Current of Class AB Transconductance Stage versus Input Power

because higher even-order terms in the Volterra Series expression become more significant.

3.3 Noise Performance

Both the driver stage and the differential switching stage (switching pair in single-balanced mixer and switching quad in double-balanced mixer) contribute noise to the IF output of the mixer. In this section, the analytical noise figure equations for common-emitter and differential-pair transconductance stages are derived. The noise contribution from the differential switching stage is discussed in a qualitative way. In a nonlinear circuit such as mixer, noise at various frequencies can be mixed to the IF and increase the noise figure of the circuit.

Fig. 3.11 shows the model used to derive the noise figure equation for a common-

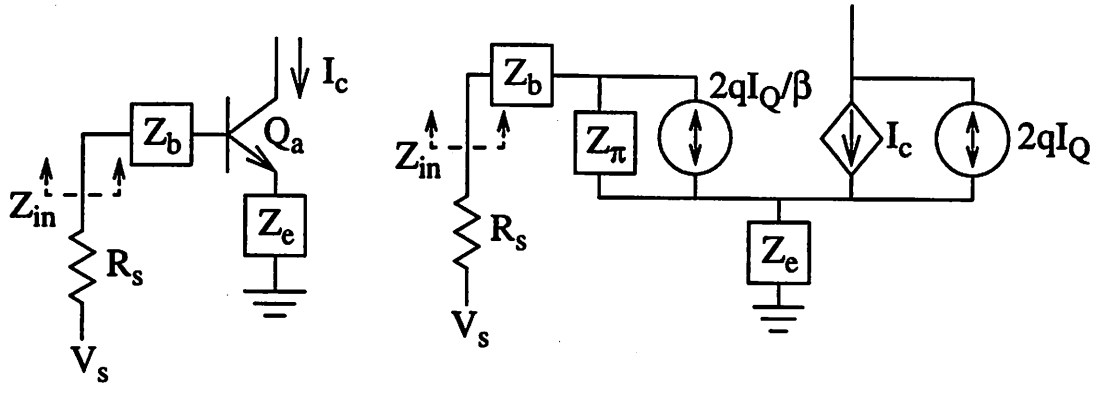

Fig. 3.11. Model of Common-Emitter Transconductance Stage

emitter transconductance stage which is biased at a collector current of I_Q. The terms $(2qI_Q/\beta)$ and $(2qI_Q)$ in Fig. 3.11 represent of base and collector shot noise generators respectively. R_s is the source resistor. Z_π is the base-emitter impedance, which includes C_b, C_{je} and r_π. The base impedance Z_b includes r_b and the impedance of input matching network. Z_{in} is the input impedance of the transconductance stage. To avoid dealing with correlation between the equivalent input noise voltage and current generators, the method described in [11][14] is not used to derive the noise figure equation. Instead, the output noise contribution from each noise generator is calculated, and the output noise power is divided by the transconductance to obtain the input-referred noise power which is compared to thermal noise power generated by R_s. The noise figure (in linear scale) of the common-emitter transconductance stage is given by

$$NF = 1 + N_c + N_b + N_t \,, \tag{3.25}$$

where

$$N_c = \frac{|R_s + Z_b + Z_e + Z_\pi|^2}{2g_m Z_\pi^2 R_s}, \tag{3.26}$$

$$N_b = \frac{g_m |R_s + Z_b + Z_e|^2}{2\beta R_s}, \tag{3.27}$$

$$N_t = \frac{\text{Real}(Z_b + Z_e)}{R_s}, \text{ and} \tag{3.28}$$

$$g_m = \frac{I_Q}{V_T},$$

where N_c, N_b and N_t are collector shot noise, base shot noise and thermal noise contributions respectively. This equation neglects the effect of C_μ of Q_a.

The collector shot noise contribution can be decreased by increasing g_m (or bias current). On the other hand, the base shot noise contribution increases with g_m (or bias current). Therefore, there exists an optimal bias current where the sum of collector and base shot noise contributions is minimum. When R_s is small, both the collector and base shot noise contributions can be decreased by increasing R_s. As R_s becomes sufficiently large and dominates the numerators of equations (3.26) and (3.27), both the collector and base shot noise contributions increase with R_s since the numerators increase with the square of R_s but the denominators increase linearly with R_s. Therefore, there exists an optimal R_s to minimize the sum of collector and base shot noise contributions.

On the other hand, the thermal noise contribution decreases when R_s increases. To reduce the thermal noise contribution from Q_a, large device size is needed to reduce r_b and parasitic emitter resistance. However, the increase in C_μ decreases the linearity of the

transconductance stage, and increases feedback from collector to base (this decreases gain and make impedance matching difficult). The degeneration impedance Z_e can be implemented by either resistors, inductors or capacitors. In contrast to resistive degeneration, reactive (inductive or capacitive) degeneration does not introduce an additional source of thermal noise.

The input impedance Z_{in} of the common-emitter transconductance stage (Fig. 3.11) is given by

$$Z_{in} = Z_b + Z_e + Z_\pi + g_m Z_\pi Z_e \ . \tag{3.29}$$

This equation neglects the effect of C_μ of Q_a, which depends on the output load impedance. With inductive degeneration, the real part of Z_{in} is supplied by [real(Z_b) + $g_m Z_\pi Z_e$], where $g_m Z_\pi$ is approximately equal to $\omega_T L_e$ (r_π can be ignored at high frequency). Impedance matching networks (discussed in section 2.6) may be needed to match the real part of Z_{in} to the source resistance R_s. The imaginary part of Z_{in} can be cancelled by setting [imag(Z_b) + Z_e + Z_π)] to zero. For stability reason, capacitive degeneration is typically avoided since the ($g_m Z_\pi Z_e$) term is a negative real number if Z_e is capacitive, and the real part of Z_{in} may be negative (negative resistance may cause oscillation). If the noise figure of the common-emitter transconductance stage is dominated by the collector shot noise contribution, the same condition for impedance matching minimizes the noise figure. Thus, simultaneous noise and impedance matching can be achieved. This situation is not possible when the device f_T is much higher (more than a factor of 10) than the input signal frequency as the base shot noise contribution becomes significant. In the case of a common-source FET transconductance stage where the noise figure is dominated by the ther-

mal noise (similar to collector shot noise in terms of the noise source location), simultaneous noise and impedance matching is possible (if intrinsic gate resistance R_i caused by distributed channel effect can be ignored).

The gain of the transconductance stage should be maximized (by minimizing the degeneration impedance Z_e) to reduce the noise contribution from the switching stage. However, linearity (IP_3 and P_{-1dB}), current consumption and impedance matching requirements set a lower limit on the degeneration impedance. If an input impedance-matching network is used, high-Q components should be used to construct the matching network because power loss through the matching network can degrade the NF of the transconductance stage, and the loss resistance introduces an additional source of thermal noise.

For a differential-pair transconductance stage (Fig. 3.12) biased with a tail current of

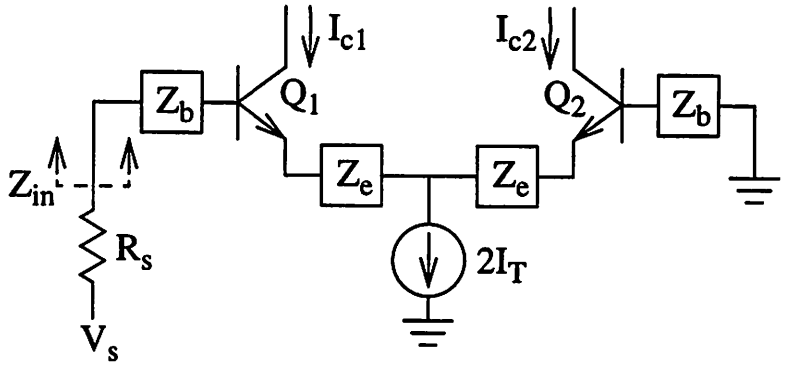

Fig. 3.12. Model of Differential-Pair Transconductance Stage

$2I_T$, the noise figure (in linear scale) and the input impedance are

$$NF = 1 + 2(N_c + N_b + N_t) \text{ , and} \tag{3.30}$$

$$Z_{in} = 2(Z_b + Z_e + Z_\pi + g_m Z_\pi Z_e) \tag{3.31}$$

respectively, where N_c, N_b and N_t are the same as those in equations (3.26), (3.27) and (3.28) respectively, and $g_m = \frac{I_T}{V_T}$. As shown in equation (3.30), a differential-pair transconductance stage has higher noise figure than a common-emitter transconductance stage, since the former has more noise generators. Furthermore, the g_m of each device in the differential-pair transconductance stage is lower than that in the common-emitter transconductance stage with the same bias current because each device in the differential-pair transconductance stage is biased with only half of the tail current.

Fig. 3.13 shows a common-emitter transconductance stage using inductive degenera-

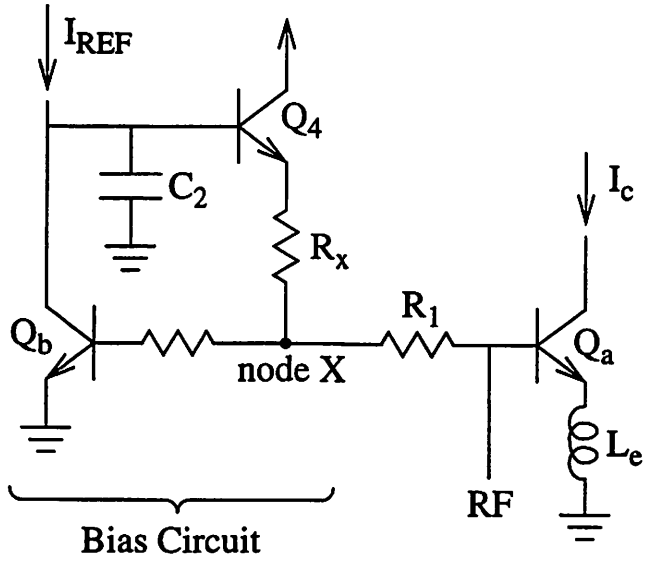

Fig. 3.13. Common-Emitter Transconductance Stage with Bias Circuit

tion. The bias transistor Q_b forms a current mirror with the driver transistor Q_a. By scaling device sizes, Q_a can be biased with a collector current which is a multiple of I_{REF}. The helper transistor Q_4 is used to supply base current to Q_a to reduce the sensitivity of bias

current with respect to β_0 variation (due to process variation) of Q_a. Noise from the bias circuit and reference current source (I_{REF}) can be injected into the base of Q_a, and increases the noise figure of the transconductance stage. Capacitor C_2 is used to attenuate this noise from the bias circuit. It also helps to stabilize the bias circuit, which has a feedback configuration. Although C_2 does not filter the noise from Q_4, the noise contribution from Q_4 is small since it is attenuated by the impedance-divider network formed by the resistor R_x, R_1, and the impedance looking into the base of Q_1 in parallel with the source resistance R_s of the RF input source.

To exploit the class AB behavior discussed in section 3.1, the bias resistor R_1 needs to be kept small. However, the current noise from R_1 can be injected into the base of Q_a, and degrades the noise performance of the transconductance stage if a bypass capacitor is placed at node X. Without a bypass capacitor at node X, the high-frequency impedance at node X is large. Hence, the current noise from R_1 is not injected into the base of Q_a. Instead, the current noise is circulated within R_1. Therefore, it is undesirable to place a bypass capacitor at node X. In this configuration. R_1 should be large enough to attenuate the noise contribution from the bias circuit, but small enough to avoid suppressing the class AB behavior.

The differential switching stage (switching pair in single-balanced mixer and switching quad in double-balanced mixer) contributes noise to the mixer output when both sides of the switching stage are active [11]. When one side of the switching pair is active, the mixer is similar to a cascode amplifier, and the cascode transistors contribute little noise. Hence, a large LO signal amplitude is needed to reduce the duration when both sides of

the switching stage are active. At large LO signal amplitude levels, when the LO signal amplitude is increased by a factor of 2 (6 dB), this transition duration is reduced by a factor of 2 and hence the output noise power is reduced by a factor of 2 (3 dB). However, a very large LO signal amplitude may decrease the linearity of the switching stage (discussed in section 3.1). Large LO signal amplitudes also decrease the voltage headroom at the mixer output. Another disadvantage of using large LO signal amplitudes is increased power consumption.

In bipolar transistor technologies, differential LO signal amplitudes larger than 300 mV are typically used to achieve a low mixer noise figure [8][13]. If the switching stage is driven directly by an external LO, 300 mV of LO signal amplitude is equivalent to 0 dBm of LO signal power. It might take up to 10 mA of bias current in an external LO driver to supply this LO signal power. A LO buffer can be used to reduce the LO input power requirement of the mixer [8][13]. If the LO is on the same die as the mixer, an LO buffer is also needed to isolate the sensitive output nodes of the LO from the mixer (to avoid LO pulling phenomenon). If the differential switching stage is implemented in FET technologies, the switching stage needs to be driven by a large LO signal amplitude to minimize its noise contribution. The reason is that large LO signal swing is needed to turn off one side of the FET switching stage.

Reasonably large devices should be used to reduce the r_b noise contribution from the switching stage. Small r_b also reduces the AC voltage drop across r_b, which would decrease the effective LO signal amplitude driving the switching devices. However, if the C_{je} is too large (if large devices are used), the switching of C_{je} would decrease the linearity

of the mixer (discussed in section 3.1).

If the transconductance of the driver stage and its output noise power were constant across all frequencies, the instantaneous-switching operation (multiplying the output noise from the driver stage with square wave at LO frequency) would increase the input-referred noise contribution from the driver stage by a factor of $\left(\frac{\pi}{2}\right)^2$ (or 3.9 dB) as illustrated in Fig. 3.14 [11]. The LO and its harmonics (a square wave has no even harmonics) mix

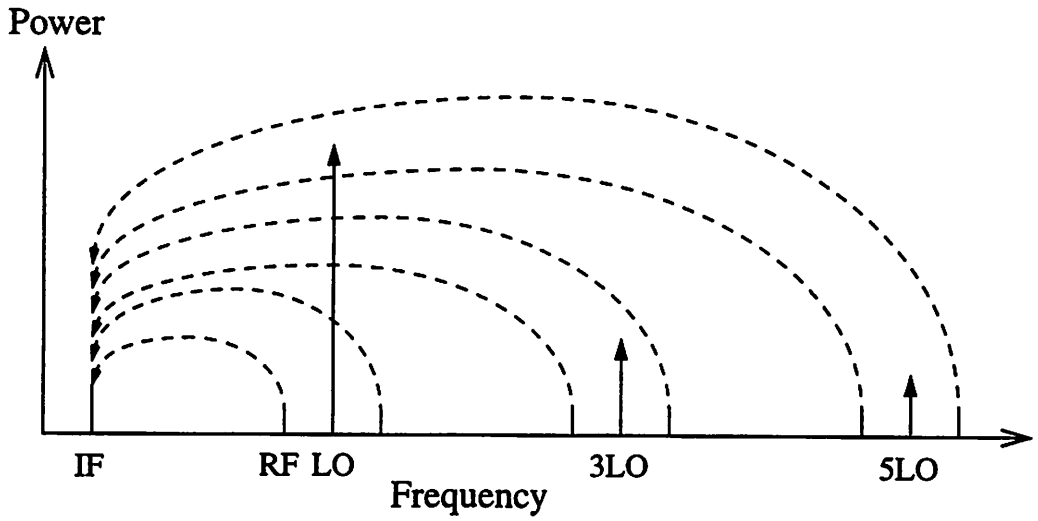

Fig. 3.14. LO Mixes Noise to the IF

noise at various frequencies down to the IF. On the other hand, if the switching operation is a sine wave, the input-referred noise contribution from the driver stage would be increased by a factor of 2 (3 dB) due to mixing of the noise at the image frequency down to the IF (an ideal sine wave has no harmonics). For practical switching operation (neither square nor sine wave), noise contribution from the driver stage is increased by a factor between 2 and $\left(\frac{\pi}{2}\right)^2$. In this case, the overall input-referred noise power (in linear scale) of

the mixer is given by

input-referred noise of driver stage × k + noise contribution from switching stage , (3.32)

where k is the noise mixing factor, which is between 2 and $\left(\frac{\pi}{2}\right)^2$.

With inductive degeneration, the transconductance and output noise floor of the driver stage decrease with frequency [15]. If high-side mixing (LO frequency higher than RF) is used, the RF signal (and the associated noise) has higher gain than the noise at the image frequency. Also, noise at higher frequencies is attenuated by the degeneration inductance. In this case, the mixing operation increases the input-referred noise power of the driver stage by a factor of less than $\left(\frac{\pi}{2}\right)^2$. On the other hand, if low-side mixing (LO frequency is lower than RF) is used, the mixing process increases the input-referred noise power of the driver stage by a factor of more than $\left(\frac{\pi}{2}\right)^2$, since noise at the image frequency has higher gain than the RF signal. The amount of reduction in the factor k of equation (3.32) depends on the frequency difference between the RF and image frequencies. The larger the difference, the smaller the k factor becomes. Therefore, high-side mixing is suitable for the inductively degenerated driver stage. Furthermore, high IF helps to reduce the noise figure of the mixer. For the same reason, low-side mixing is suitable for the capacitively degenerated driver stage.

In both single-balanced and double-balanced mixers, the IF output can be taken either single-endedly or differentially. Taking the output differentially increases the output signal power and conversion gain of the mixers. Furthermore, taking the output differen-

tially helps to reject the common-mode noise. In a double-balanced mixer, noise from the tail current source ($2I_T$) at the IF can feedthrough to the IF output ports. This noise would increase the IF output noise power of the mixer significantly if single-ended output is taken. Since this noise is common-mode, it can be cancelled by taking the IF output differentially. If a differential IF filter is available, both of the IF output ports can be connected directly to the input ports of the filter. On other hand, if the IF filter is single-ended, differential-to-single-ended conversion is needed. This can be achieved by using either a transformer or some kinds of narrow-band current-combining networks [16][17]. Alternatively, a IF output buffer with differential inputs can be used.

In a single-balanced mixer, taking the IF output single-endedly would increase the input-referred noise contribution from the driver stage by a factor of $\left[2\left(\frac{\pi}{2}\right)^2\right]$ (or 6.9 dB) if the output noise power of the driver stage were constant across all frequencies. Since there is a DC component in the LO signal, noise from the driver stage at the IF can mix with this DC component and increase the noise power at the IF output ports. If the driver stage is inductively degenerated, it has high transconductance and noise power at the IF. In this case, taking the IF output single-endedly would increase the noise figure of the mixer significantly. Therefore, the IF output of the single-balanced mixer has to be taken differentially (in this case, LO signal has no DC component) in order to minimize its noise figure [8][13].

Since the RF signal has a DC component in a single-balanced mixer, noise from the LO at the IF can mix with this DC component and increase the noise power at the IF output port. Taking the mixer output differentially does not help to reduce this noise. There-

fore, the LO signal should have low noise power at the IF. If a LO buffer is used, bandpass or highpass load can be used at the output of the LO buffer to reduce its noise at the IF [8][13]. On the other hand, double-balanced mixers reject noise from the LO at the IF, since the RF signal has no DC component.

Using large LO signal amplitudes (> 300 mV or -10 dBV) and a driver stage with high transconductance, the driver stage typically contributes more noise than the switching stage because the switching stage can be switched very rapidly (the duration when both sides of the switching stage are active is reduced). This is particularly true when a high f_T (relative to LO frequency) process is used. On the other hand, the noise contribution from the switching stage becomes significant in a low f_T process because the $r_b C_\pi$ time constant of the switching devices reduces the switching speed (increase the duration of the switching transition). These two different cases are demonstrated in the design examples presented in CHAPTER 4.

3.4 Desensitization Mechanisms by a Blocker

A blocker with large amplitude can desensitize a mixer via a number of mechanisms. Firstly, a large blocker can reduce the conversion gain of a mixer with respect to the small desired signal (discussed in section 2.3), and thus increase the noise contribution from the IF stages. This gain-compression problem can be alleviated by improving the linearity and overload performance (P_{-1dB}) of the mixer. Further desensitization may occur due to the increased output noise power in the presence of a large blocking signal [7][8]. A blocker at 10 MHz away from the RF is used below to illustrate this phenomenon.

In the common-emitter transconductance stage shown in Fig. 3.4, the blocker can be

viewed as functioning as a second LO signal (besides the desired LO signal for downconversion) which mixes (due to even-order nonlinearities of Q_a) low-frequency noise from the bias circuit up to the RF [7]. For instance, the blocker at 10 MHz away from the RF mixes with the noise from the bias circuit at 10 MHz and shifts it to the RF. As a result, the output noise power of the transconductance stage is increased by the blocker. This is the second desensitization mechanism by the blocker.

There are two commonly used methods to remove this low-frequency noise from bias circuit. The first method is shown in Fig. 3.15. An RC filter is used to filter the low-

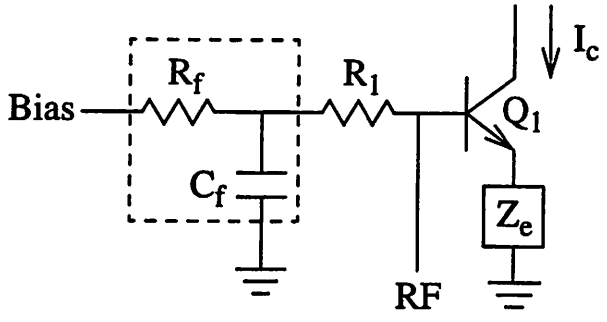

Fig. 3.15 Common-Emitter Transconductance Stage with RC Filter

frequency noise from the bias circuit. The filter cutoff frequency (reciprocal of the RC time constant) needs to be much lower than 10 MHz if the blocker is 10 MHz away from the RF. However, the bias resistors (R_f and R_1) need to be kept small to exploit the class AB behavior of the transconductance stage. Hence, the capacitor C_f needs to have large capacitance. Large capacitance can only be implemented by using an external component. However, the RC filter does not reject the low-frequency current noise from the bias resistor R_1.

A better method using a low-frequency trap is shown in Fig. 3.16. The trap has low

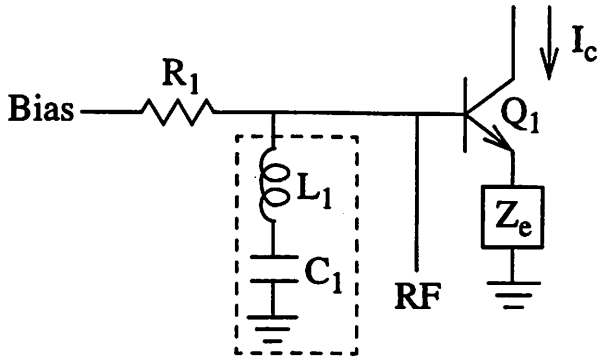

Fig. 3.16 Common-Emitter Transconductance Stage with Low-Frequency Trap

impedance at low frequency (10 MHz) to filter out the low-frequency noise from the bias circuit. At low frequencies, the inductor L_1 appears to be short. Hence, capacitor C_1 can filter out the low-frequency noise from the bias circuit if it has low enough impedance. At RF, the trap appears open (due to L_1) and does not affect the impedance matching. The disadvantage of this method is that two external components are needed (instead of one external component in the previous method).

The blocker can also mix with the internal noise (base and collector shot noise, and r_b thermal noise) sources of Q_a and shift this low-frequency noise to the RF. Currently, there is no known technique to filter this noise, since it is caused by the internal noise generators.

In the differential-pair transconductance stage shown in Fig. 3.17, the low-frequency noise from the bias circuit is common-mode. Hence, it can be suppressed by taking the output differentially. On the other hand, noise from the tail current source ($2I_T$) at low fre-

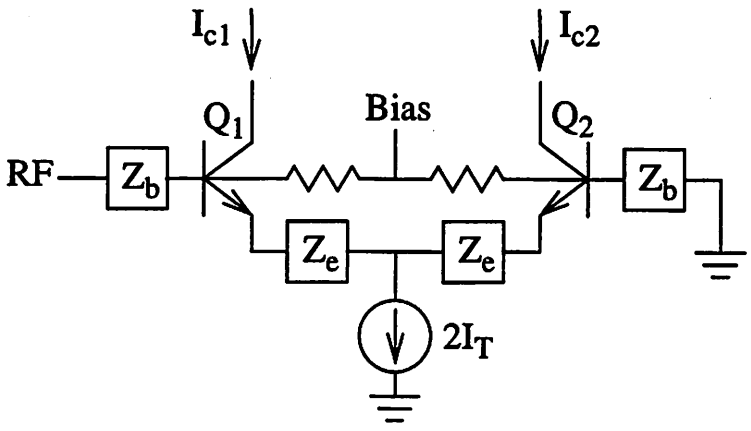

Fig. 3.17 Differential-Pair Transconductance Stage with Bias Circuit

quency can mix with the blocker, and move to the RF. The blocker can be viewed as a second LO signal driving the differential pair in a way similar to the way the desired LO signal drives the switching stage of the mixer. To alleviate this problem, the tail current source needs to have low noise at low frequency.

Fig. 3.18 shows the circuit topology of a typical current source. The low-frequency

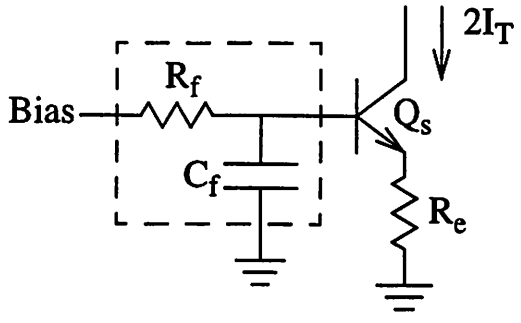

Fig. 3.18 A Typical Current Source

noise from the bias circuit can be suppressed by using a RC filter with low enough cutoff frequency. To suppress the low-frequency noise at 10 MHz, the cutoff frequency of the RC filter should be much lower than 10 MHz. However, the internal noise sources (base and

collector shot noise, and r_b thermal noise) of Q_s cannot be filtered by the RC filter, but can be attenuated by increasing the degeneration resistor R_e. Therefore, the degeneration resistor R_e should be maximized, subjected to voltage headroom limitation.

The third desensitization mechanism by a blocker is known as the reciprocal mixing phenomenon [18]. Once amplified by the driver stage of the mixer, the blocker mixes with the LO phase noise, and shifts it to the IF. For instance, the blocker at 10 MHz away from the RF mixes with LO phase noise at 10 MHz offset from the LO carrier. The input-referred noise power of the mixer caused by this reciprocal mixing phenomenon is given by

$$\text{Input-Referred Noise Power} = \text{Input Blocker Power} + \text{LO Phase Noise}, \quad (3.33)$$

where the LO phase Noise is in (dBc/Hz) unit. The equation is independent of the mixer topologies. Hence, the only way to reduce this noise is to reduce the blocker power and the LO phase noise. For out-of-band blockers, the blocker power can be reduced by using RF and image-rejection filters with greater stopband attenuation. Alternatively, the LO phase noise can be reduced. However, if the blockers are in-band, the RF and image rejection filters do not attenuate these blockers. In this case, the LO needs to have very low phase noise. In many wireless applications which have to handle strong blockers, off-chip LO may be needed for its superior phase-noise performance. If an LO buffer is included in the mixer design, the LO buffer needs to have low noise to avoid increasing the phase noise of the LO signal at the output of the buffer.

CHAPTER 4

Design Examples

The design and optimization techniques discussed in CHAPTER 3 are demonstrated in two mixer design examples in this chapter. Two monolithic RF downconversion mixers have been fabricated, packaged and characterized. Section 4.1 presents a class AB monolithic mixer for 900 MHz applications [8]. The design is implemented in a 25 GHz f_T bipolar process. Section 4.2 presents a 2.4 GHz monolithic mixer for wireless LAN applications [13]. The design is implemented in a 1μm BiCMOS process with 13 GHz bipolar transistors. The major difference between the two designs is the ratio of device f_T to signal frequency. Sections 4.3, 4.4 and 4.5 discuss how the techniques can be applied to other RF building blocks, such as the low-noise amplifiers (LNA) and power amplifiers (PA).

4.1 A Monolithic Mixer for 900 MHz Applications

In this section, a class AB downconversion mixer for 900 MHz applications is presented [8]. The mixer is designed to operate with a differential IF filter with input resistance of 1kΩ. The single-balanced topology shown in Fig. 1.2 is used in the design for its superior noise performance. The driver stage is inductively degenerated to exploit the class AB behavior discussed in section 3.2.

As shown in equation (2.2), the LNA needs to have sufficient power gain to reduce the noise contribution from the mixer. Hence, a mixer with low noise figure (NF) is highly desirable in order to relax the gain requirement of the LNA. Most of the low-noise active

mixers (in silicon technologies) currently available have a single-sideband noise figure greater than 10 dB. The goal of this design is to obtain a mixer with significantly lower noise figure, without sacrificing linearity. Furthermore, the downconversion mixer should provide sufficient power gain to compensate for the IF filter loss, and to reduce the noise contribution from the IF stages. Typically, a power gain greater than 5 dB is desirable. However, this gain should not be too large, since saturation at the IF output port may limit the 1 dB compression point (P_{-1dB}).

As discussed in section 2.3, a strong blocker can overload a mixer and cause gain compression of the small desired signal if the mixer does not have sufficiently high input P_{-1dB}. In some applications, a blocker as strong as -5 dBm can appear at the input of the mixer. In order to avoid increasing the noise contribution from the IF stages significantly, this blocker should not reduce the gain of the mixer with respect to the small desired signal by more than 1 dB. Hence, an input P_{-1dB} specification greater than -5 dBm (-3 dBm is used in this design to provide 2 dB margin) for the mixer is used as a starting point for this design. In the actual design, SPICE simulation is used to verify that the gain compression of the small desired signal in the presence of a -5 dBm blocker is less than 1 dB. The actual value of P_{-1dB} is not the true design criterion.

The basic topology of the class AB mixer is shown in Fig. 4.1. It comprises a common-emitter driver stage (Q_1) and a differential switching pair (Q_2 and Q_3). To improve the linearity of the common-emitter driver stage, it is degenerated by bond wires in series with package pins (modeled as a high-Q inductor L_e), instead of a resistor. As discussed in sections 3.1, inductive degeneration is more power efficient than both resistive and capaci-

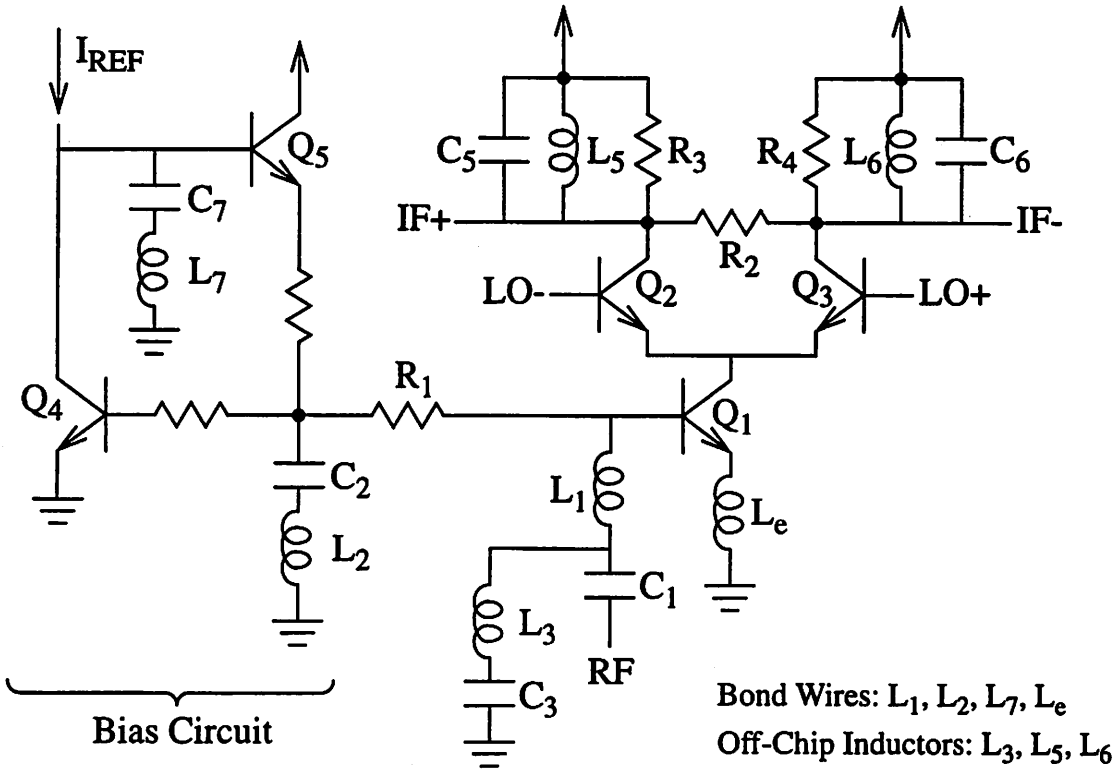

Fig. 4.1. Class AB Mixer

tive degeneration (with the same transconductance and linearity). As discussed in section 3.3, inductive degeneration has better noise performance than resistive degeneration since the degeneration inductor does not introduce an additional source of noise. To reduce the noise contribution from Q_1, a large device with small base resistance ($r_b \sim 3\Omega$) is used. The bias current is also optimized to reduce the sum of base and collector shot noise contributions. Ideally, the gain of the driver stage should be maximized (by minimizing the degeneration inductance L_e) to minimize the noise contribution from the switching pair. However, linearity (third-order intermodulation and spurious response) and head room (which affects P_{-1dB}) considerations set the lower limit on the degeneration inductance.

The bias transistor Q_4 forms a current mirror with the driver transistor Q_1. The reference current I_{REF} (0.6 mA) is supplied by a PTAT (proportional to absolute temperature) current source from an on-chip bias-current generator. The total emitter size of Q_1 is a factor of 9 larger than that of Q_4. This allows transistor Q_1 to be biased at a collector current of 5.6 mA ($\approx 9 \times 0.6$mA). The helper transistor Q_5 is used to supply base current to Q_1 to reduce the sensitivity of bias current with respect to β_0 variation (due to process variation) of Q_1.

Capacitor C_2 is a bypass capacitor used to prevent bias-circuit noise from entering the base of Q_1 (this is a mistake as discussed in section 3.3). Series tuning between C_2 and a bond wire (L_2) provides an AC ground at the RF (900 MHz). The impedance looking into the base of Q_1 [from equation (3.29)] is given by

$$2\pi f_T L_e + r_b + sL_e + \frac{1}{sC_\pi}, \tag{4.1}$$

where f_T is the unity current-gain frequency of Q_1, and C_π is the total base-emitter capacitance of Q_1. This equation neglects the effect of collector-base junction capacitance (C_μ) and the base-emitter resistance (r_π) of Q_1. The parallel combination between the real part of this equation and the resistance of R_1 (150Ω) provides 50Ω for impedance matching. The imaginary part of this equation is cancelled by the reactance of the bond wire L_1 in series with the external DC blocking capacitor C_1.

Capacitor C_7 is used to stabilize the bias circuit, which uses a feedback configuration. It also helps to filter noise from the reference current I_{REF}. The external capacitor C_3

and inductor L_3 form a low-frequency trap used to suppress the low-frequency noise from the bias circuit. This is to alleviate the desensitization effect by a strong blocker (discussed in section 3.4). The input resistance of the differential IF filter is modeled by R_2 (1kΩ). Resistors R_5 and R_6 ($R_5 + R_6 = R_2$) are used to match the input impedance of the IF filter.

The common-emitter driver stage with inductive degeneration exhibits the class AB behavior described in section 3.2. To avoid gain compression caused by DC feedback, resistor R_1 and parasitic resistance at the emitter of Q_1 (r_e) should be minimized. However, R_1 should be large enough to avoid significant loading at the RF input port, which would cause impedance mismatch and noise-figure degradation. Considering the trade-offs between P_{-1dB} and noise figure, the resistance value of R_1 is chosen to be 150Ω .

For a mixer with 5 dB of power gain, a -3 dBm RF input signal produces 2 dBm of IF output power. The signal current amplitude required to drive 2 dBm of power into the 1kΩ IF filter resistor (R_2) is 1.78 mA. In a class A design (as in the case of a differential-pair driver stage with constant tail current source), the bias current required is

$$1.78\text{mA} \times \pi \times 2 = 11.2\text{mA} . \qquad (4.2)$$

The π factor is caused by the current lost in the switching (mixing) operation. The factor of 2 is caused by half of the current being lost in the filter-matching resistor (R_3 and R_4). On the other hand, a class AB mixer can be biased at a much lower quiescent current level. In this design, Q_1 is biased at a collector current of 5.6 mA. Fig. 3.7 shows the simulated signal current amplitude and average current of the driver stage as a function of RF input power. Simulation shows that, due to the class AB behavior, the signal current amplitude and average current of Q_1 increase to 16.8 mA and 14.4 mA respectively when a -3 dBm

sinusoidal signal is applied to its input. Fig. 3.8 shows the simulated output current waveform of the driver stage.

To further investigate the effect of class AB behavior on gain compression under blocking conditions, a small signal and a large blocker are applied to the input of the driver stage. Fig. 4.2 shows the normalized transconductances G_M (normalized to the small-sig-

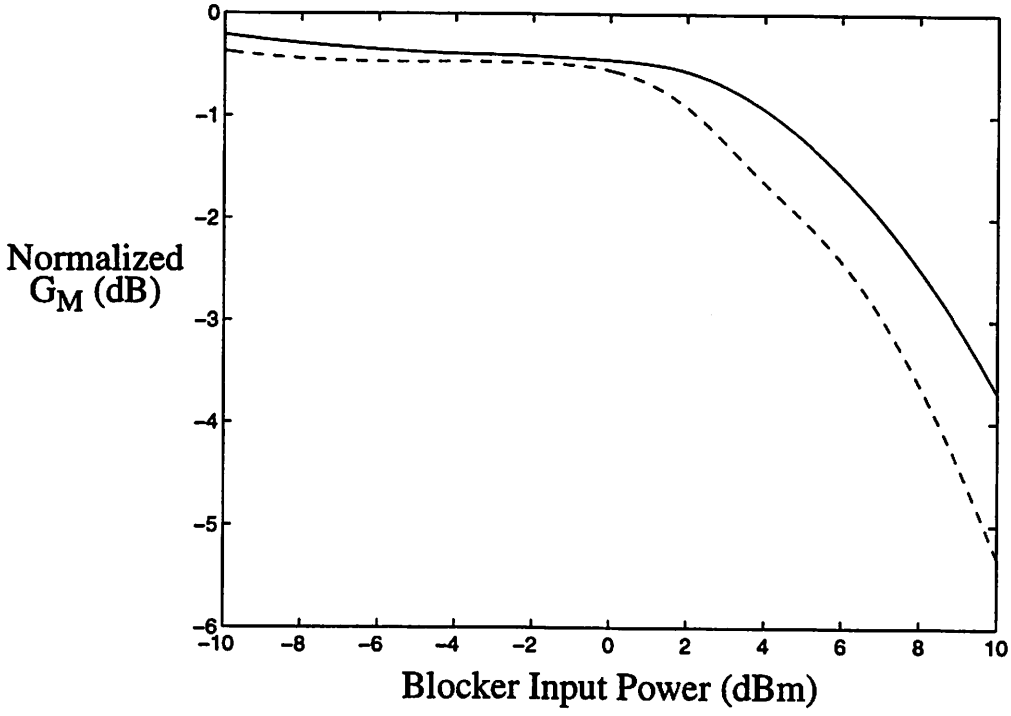

Fig. 4.2. Normalized Transconductance versus Blocker Input Power

nal transconductance) of these two signals, as a function of the blocker input power. Due to the class AB behavior, the driver stage has an input P_{-1dB} of about 4 dBm. With a -5 dBm blocker, the transconductance of the small desired signal is compressed by only 0.5 dB.

In this mixer design, gain compression is not dominated by the nonlinearities in the

transfer function of the driver stage, but dominated by saturation of Q_2 and Q_3 caused by large signal swings at the IF output port. With 2 dBm of IF output power across the 1kΩ differential load resistor R_2, the resulting differential output signal amplitude is 1.78V (0.89V at each IF output terminal). Hence, sufficient head room is required at the collectors of Q_2 and Q_3 to avoid limiting the IF output swings. In this design, inductors L_5 and L_6 are used to bias the collectors of Q_2 and Q_3 to the power supply voltage. The bases of Q_2 and Q_3 are biased at 1.1V below the power supply voltage. Assuming that bipolar transistors saturate at a base-collector voltage of about 0.4V (conservative estimate), this allows a 0.6V (=1.1V+0.4V-0.9V) head room for LO swing to drive the bases of Q_2 and Q_3, and high-frequency feedthrough signals at the IF output terminals, as well as bias voltage shift caused by component variations.

Single-balanced mixers do not reject LO and RF feedthrough at the IF output port. Normally, this is not a problem, since the IF filter has high enough stopband attenuation to filter out unwanted signals at both LO and RF frequencies (and their harmonics). However, this high-frequency feedthrough signals can produce large signal swings at the IF output port of the mixer, and degrade the P_{-1dB} and the spurious performance of the mixer. Capacitors C_5 and C_6 are used to attenuate the LO and RF feedthrough signals without affecting the desired IF signal. The LC tanks, L_5C_5 and L_6C_6, are tuned at the IF.

High-side mixing (LO frequency is higher than the RF) is used to convert the RF signal down to the IF. As discussed in section 3.3, high-side mixing (as opposed to low-side mixing) reduces the noise contribution from the driver stage, since it is inductively degen-

erated. Taking the IF output differentially (using a differential IF filter) helps to cancel the common-mode IF noise (discussed in section 3.3) from the driver stage.

The differential switching pair should be driven by a large LO signal to minimize its noise contribution (discussed in section 3.3). Fig. 4.3 shows the simulated noise figure

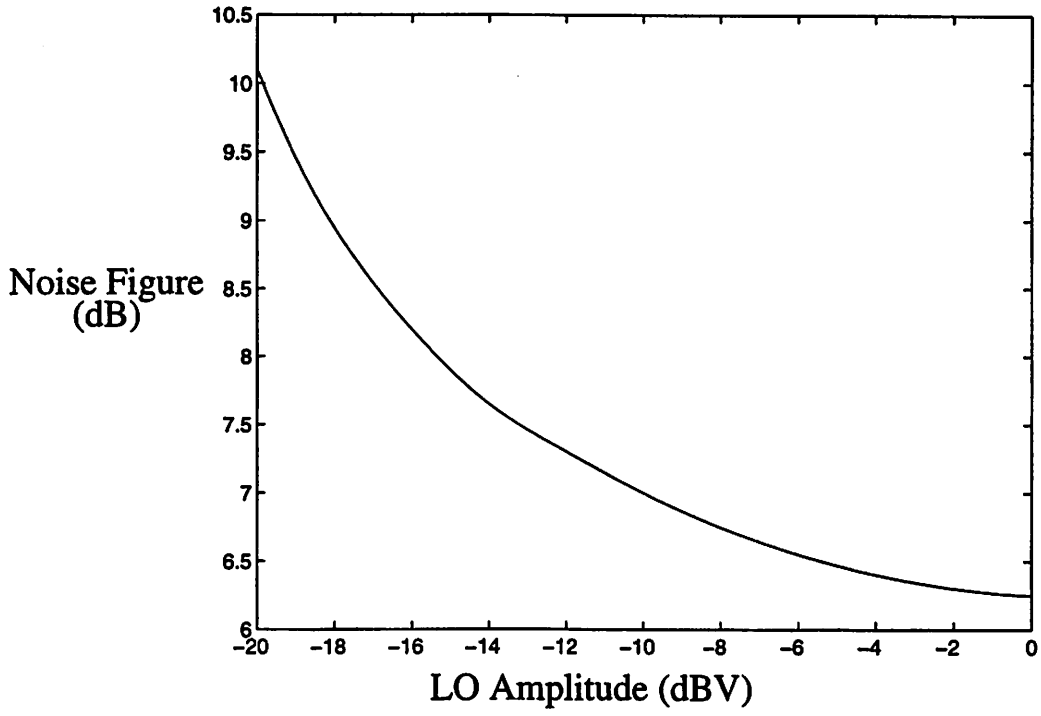

Fig. 4.3. Mixer Noise Figure versus LO Signal Amplitude

(NF) of the mixer (LO buffer is not included) as function of differential LO signal amplitude. For LO signal amplitudes above or 0.3V or -10 dBV (1V = 0 dBV), the noise figure of the mixer decreases slowly as the LO signal amplitude increases because the overall input-referred noise power is dominated by the noise contribution from the driver stage. Linearity, head room, LO feedthrough and power consumption considerations set the upper limit on the LO signal amplitude. A very large LO signal amplitude decreases the linearity (discussed in section 3.1), reduces the head room at the collectors of Q_2 and Q_3,

and increases the LO feedthrough to the RF input port (through C_μ of Q_1). Another disadvantage of using a large LO signal amplitude is that large power consumption is required.

Considering the trade-offs between noise figure and other performance parameters mentioned above, a differential LO signal amplitude of -10 dBV (630 mV peak-to-peak) is used in this design to drive the differential switching pair. Using this LO signal amplitude and devices with high f_T (~ 20 GHz), the switching pair is switched very rapidly, and thus generates relatively little noise and IM_3 distortion at the mixer output port [11][12]. Reasonably large devices for the switching pair are used to reduce the r_b noise contribution. However, if the base-emitter junction capacitance (C_{je}) is too large, the switching of C_{je} can degrade the linearity (discussed in section 3.1). With proper choices of LO signal amplitude and device sizes in this design, the noise and nonlinearity contributions from the switching pair are small relative to those from the driver stage. In other words, noise and linearity performance of this design is dominated by that of the driver stage.

If the differential switching pair were driven directly by an external LO, 0 dBm of LO signal power would be required. In the absence of an on-chip LO buffer, it might take up to 10 mA of bias current in an external LO driver to supply this LO signal power. Hence, a LO buffer with a voltage gain of 10 dB is included in this design to reduce the LO input power requirement to -10 dBm. Fig. 4.4 shows the basic topology of the LO buffer. One side of the differential switching pair (Q_{11} and Q_{12}) accepts the LO input signal, while the other side is AC grounded by series tuning between capacitor C_9 and a bond wire (L_9). Resistor R_5 is used for impedance matching. The output terminals (LO+ and LO-) of the LO buffer are connected directly (without coupling capacitors or level-shifting

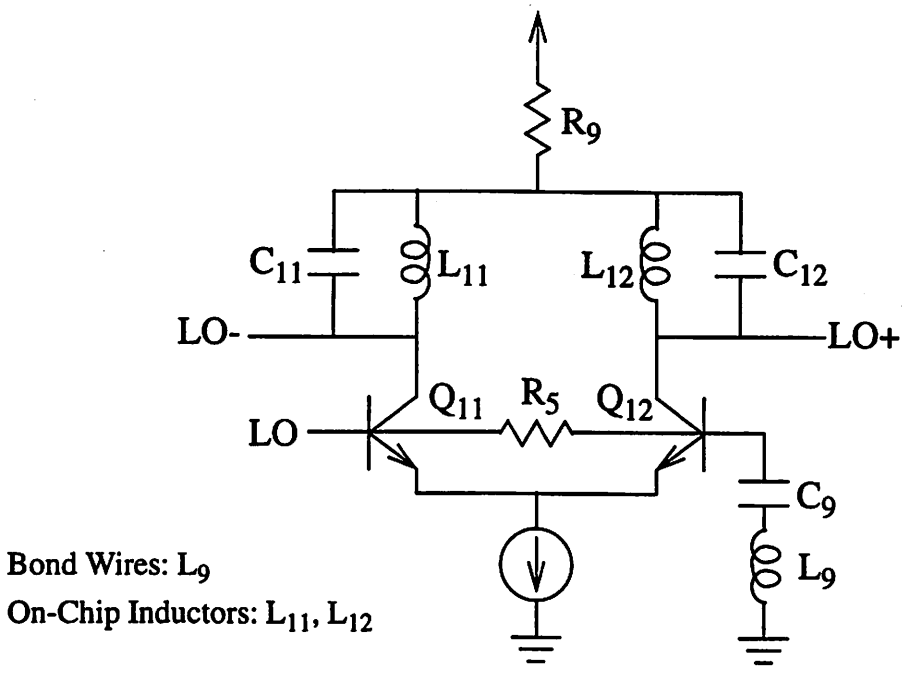

Fig. 4.4. LO Buffer

circuitries) to bases of the differential switching pair (Q_2 and Q_3) of the mixer. Resistor R_9 is used for level shifting to match the DC level of the buffer output terminals to the bases of the switching pair (Q_2 and Q_3). The noise contribution from the LO buffer is minimized by using large devices (small r_b) for the differential pair (Q_{11} and Q_{12}), and using a low-noise current source (discussed in section 3.4). Further reduction of the LO input power requirement (by increasing the gain of the LO buffer) is not desirable because the LO buffer would become very noisy. Like the switching pair (Q_2 and Q_3) in the mixer, the differential pair (Q_{11} and Q_{12}) contributes noise to the output of the LO buffer when both transistors are active.

For a single-balanced design, the noise from the LO buffer at the IF can feed through to the IF output port (discussed in section 3.3). Hence, on-chip spiral inductors L_{11} and

L_{12} (low impedance at the IF) are used at the output of the LO buffer to remove this noise. Capacitors C_{11} and C_{12} are used for parallel tuning with the inductors at the LO frequency in order to increase the load impedance at the output terminals of the LO buffer. This increases LO signal amplitude at the buffer output without consuming additional bias current.

The class AB mixer is implemented in a bipolar process with peak npn f_T of 25 GHz. Fig. 4.5 shows the die micrograph. The bonding pads are electrostatic discharge (ESD)

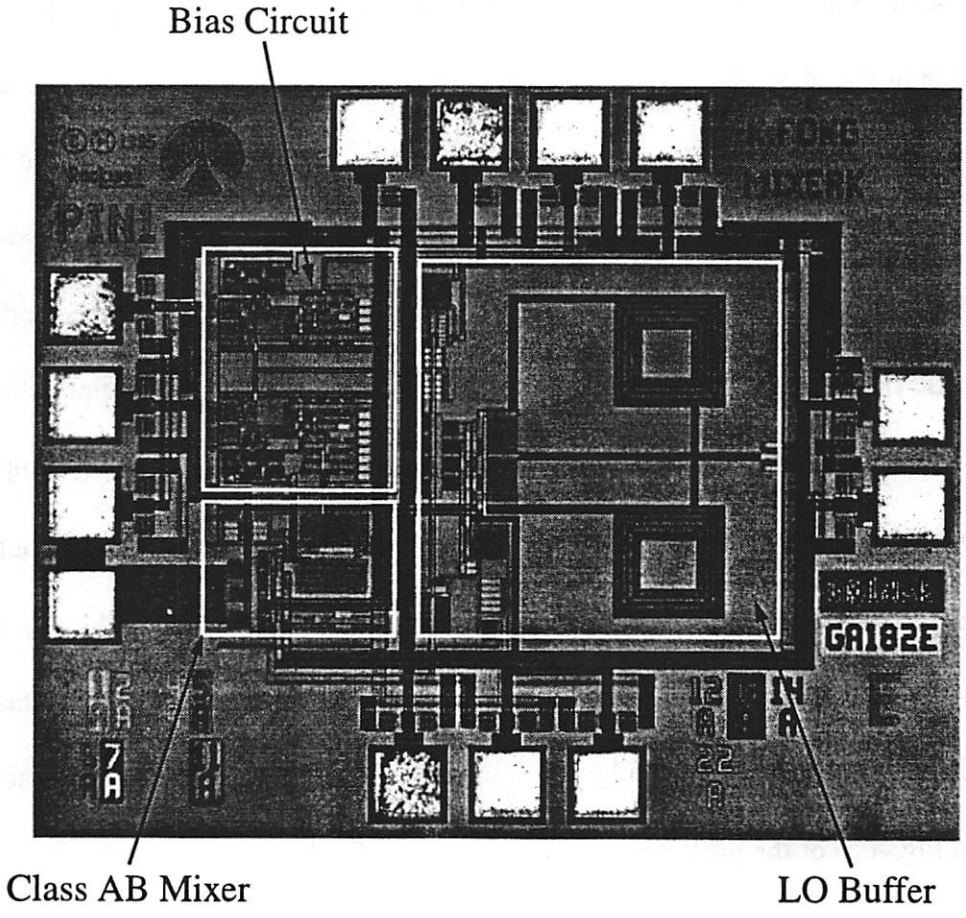

Fig. 4.5. Chip Micrograph

protected and the die is housed in a 32-pin plastic Thin Quad Flat Package (TQFP) for

prototyping. Transistor Q_1 is placed close to the bonding pads to which the bond wires used for degeneration are connected. This is to minimize the parasitic capacitance and resistance at the emitter of Q_1. The two inductors (L_{11} and L_{12}) at the output of the LO buffer are implemented by on-chip spiral inductors as shown in Fig. 4.5. Substrate contacts are placed far away from the spiral inductors to reduce subtract loss in the inductors.

The degeneration inductor L_e (~ 2.4nH) is implemented by using two adjacent pins and bond wires in parallel. The LO input pin and the AC ground pin (L_9) of the LO buffer (located on the lower side in Fig. 4.5) is perpendicular to the RF pin (located on the left side in Fig. 4.5) and IF pins (located on the right side in Fig. 4.5) to reduce the inductive coupling of the LO signal to the RF and IF ports. The LO input pin and the AC ground pin (L_9) of the LO buffer are placed next to each other to minimize the cross-sectional area of the resulting current loop. This technique minimizes the pin inductance and reduces magnetic radiation from the current loop. The same technique is also applied to the RF input pin (L_1) and the ground pin (L_2) for the bypass capacitor C_2. The RF input pin (L_1) is placed far away from the emitter pin (L_e) of the driver stage. Mutual coupling between these two pins affects impedance matching of the RF input port. The two IF output pins are placed next to each other on the opposite side of the package from the RF input pin (L_1). The supply and ground pins for the bias circuit are placed on the fourth side (top side in Fig. 4.5) of the package.

Table 4.1 summarizes the simulation (using TekSpice) and measurement results. The noise figure is simulated (using harmonic balance simulator in MDS from HP) without ESD and package models. The measurements were performed at 25°C with a 3V supply.

Table 4.1 Performance Summary

Parameters	Simulations	Measurements
Power Supply	2.7 V to 5V	2.7V to 5V
Current Consumption	11.4 mA	10.1 mA
LO Input Power	-10 dBm	-10 dBm
Conversion Gain (Power)	7.7 dB	7.5 dB
Gain Variation (@-10 dBm Blocker)	-0.4 dB	-0.25 dB
Gain Variation (@-5 dBm Blocker)	-0.6 dB	-0.2 dB
Gain Variation (+/- 20 MHz)	+/- 0.2 dB	+/- 0.25 dB
Input Third-Order Intercept Point	4.5 dBm	2.5 dBm
Input 1dB compression point	-0.5 dBm	-1.5 dBm
Single-Sideband (SSB) Noise Figure	6.9 dB	7.5 dB
SSB Noise Figure (@-10 dBm blocker)	12.3 dB	12.1 dB
SSB Noise Figure (@-5 dBm blocker)	16.6 dB	16.7 dB
LO-to-RF Feedthrough	-44.8 dBm	-47.5 dBm

The RF, LO and IF frequencies used are 900 MHz, 1150 MHz, and 250 MHz respectively. The LO input signal power used is -10 dBm. The input return loss of the RF port is less than -14 dB (600 MHz to 1.5 GHz), using only one off-chip blocking capacitor (C_1) for impedance matching. The design achieves an input IP_3 of 2.5 dBm. Simulation (using HSPICE) predicts an input IP_3 of 3.3 dBm (the result from HSPICE seems to be more accurate than that from TekSpice). Ignoring the IM_3 contribution from the switching pair, equation (3.6) predicts an input IP_3 of 3.6 dBm. Ignoring C_μ of Q_1 in the analysis does not introduce significant error.

With -5 dBm and -10 dBm blockers (at 890 MHz) applied to the RF input port, the current consumption of the whole mixer (including LO buffer) increases to 14.6 mA and 11.4 mA respectively. Equation (3.24) predicts average currents of 15.6 mA and 11.8 mA respectively. Due to the class AB behavior of Q_1, the input 1dB compression point (P_{-1dB})

and the input third-order intercept point (IP_3) differ by less than the theoretical value (weak nonlinear condition) of 9.6 dB. To achieve a comparable P_{-1dB} in a conventional class A mixer would require much higher current consumption.

A single-sideband noise figure of 7.5 dB is achieved in this design. When the LO input signal power is increased to -5 dBm, the noise figure is improved to 6.9 dB. As discussed in the section 3.4, a strong blocker can desensitize a mixer and increase its noise figure. With -5 dBm and -10 dBm blockers (at 890 MHz) applied in the RF input port, the noise figures increase to 16.7 dB and 12.1 dB respectively. However, the blockers compress the gain of the mixer with respect to small signal by less than 0.25 dB.

Fig. 4.6 shows the experimental setup used to measure the mixer noise figure under

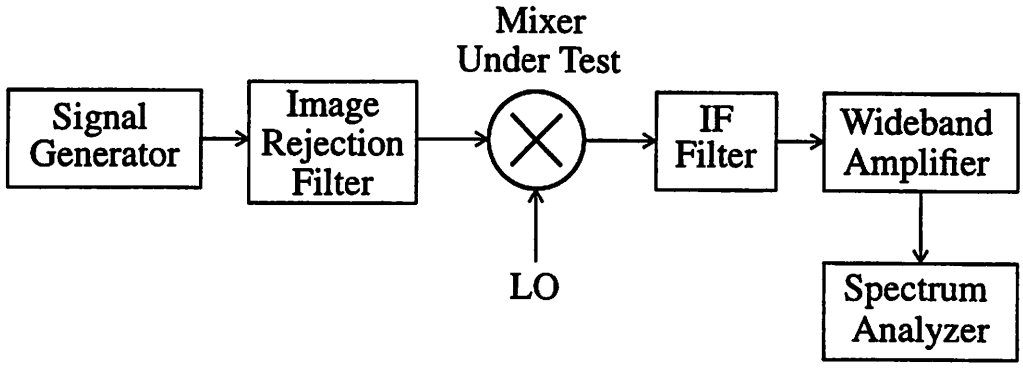

Fig. 4.6. Noise Measurement under Blocking Condition

the blocking conditions. The signal generator is used to apply the blocker at 890 MHz. The image-rejection filter is needed for single-sideband noise figure measurement. The IF filter is used to filter out the blocker (at 260 MHz after being mixed down) to prevent it from desensitizing the wideband amplifier and spectrum analyzer. The wideband amplifier (which has 24 dB gain) is used to increase the sensitivity of the spectrum analyzer. A good

spectrum analyzer has a noise floor of about -150 dBm/Hz. The output noise power from this setup should be much larger than that of the spectrum analyzer so that it can be displayed on the spectrum analyzer. To calculate the noise figure of the mixer under the blocking conditions, the noise contributions from the image rejection filter, the IF filter, the wideband amplifier and the spectrum analyzer have to be subtracted.

To obtain the noise figure under each blocker condition, three measurements are needed. The first measurement measures the output noise power (N_1) of the experimental setup without the downconversion mixer. The second measurement measures the output noise power (N_2) of the experimental setup with the downconversion mixer. The third measurement measures the output noise power (N_3) of the experimental setup with downconversion mixer under the blocking condition. Combining these three measurement values, the blocker is found to increase the output noise power of the mixer by a factor of $\left(\frac{N_3 - N_1}{N_2 - N_1}\right)$. Knowing the small-signal noise figure (from noise-figure meter measurement) of the mixer, the noise figure (NF_B) under the blocking condition is given by

$$NF_B = 1 + (NF - 1) \times \left(\frac{N_3 - N_1}{N_2 - N_1}\right) / G_C \tag{4.3}$$

where is NF_B and NF are in linear scale, and G_c is the gain compression of small signal (e.g.: 0.955 with -5 dBm blocker) under the blocking condition.

4.2 A Monolithic Mixer for Wireless LAN Applications

The rapid growth of wireless communication services has now been extended to higher frequencies, such as the 2.4 GHz band. Together with the demand for low cost and

low power, this increase in frequency presents a challenge to RF circuit designers to find low-cost solutions for the realization of high-frequency receivers using plastic packages and high-volume silicon technologies. In this section, a 2.4 GHz monolithic mixer for wireless LAN applications is presented [13]. Single-balanced topology (Fig. 1.2) is used to exploit the class AB behavior and to reduce the number of noise sources.

The downconversion mixer is required to have low noise figure to reduce the gain requirement of the LNA. This design is implemented in a 1μm BiCMOS process with peak npn f_T of 13 GHz and CMOS effective channel length (L_{eff}) of 0.8 μm. It is very difficult to obtain high gain in one-stage LNA design in this process. Since the LNA cannot provide high gain, the downconversion mixer needs to provide some conversion gain to reduce the noise contribution from the IF stages.

The basic topology of the mixer is shown in Fig. 4.7. It comprises a common-emitter driver stage (Q_1) and a differential switching pair (Q_2 and Q_3). The linearity of the common-emitter driver stage is increased by the use of degeneration provided by the inductor L_e (implemented by bond wires in series with package pins). As discussed in sections 3.1 and 3.3, inductive degeneration is superior in linearity to both resistive and capacitive degeneration, and in noise performance to resistive degeneration. To reduce the noise contribution from Q_1, a large device with small base resistance (r_b) is used. However, the increase in base-collector junction capacitor (C_μ) of Q_1 decreases linearity, and increases feedback from collector to base (this reduces gain and makes impedance matching difficult). The gain of the driver stage should be maximized (by minimizing the bond-wire inductance of L_e) to reduce the noise contribution from the switching pair. However, the

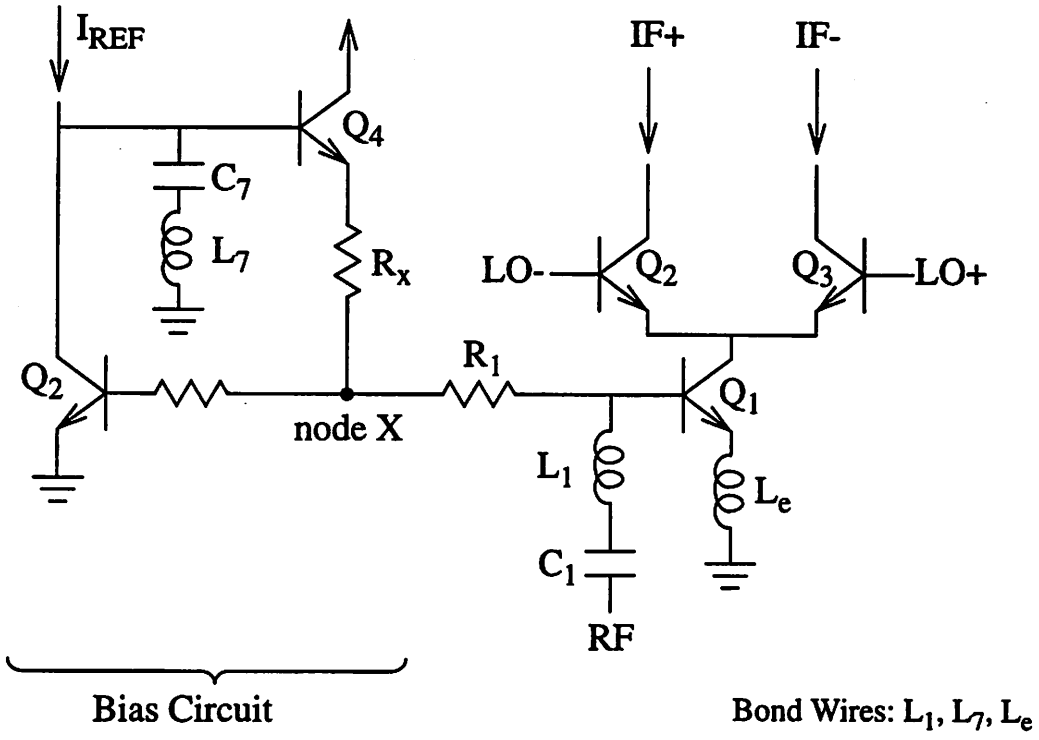

Fig. 4.7. Class AB Mixer

impedance-matching requirement sets a lower limit on the value of the degeneration inductance. The impedance looking into the base of Q_1 [from equation (3.29)] is

$$2\pi f_T L_e + r_b + sL_e + \frac{1}{sC_\pi}, \tag{4.4}$$

where f_T is the unity current-gain frequency of Q_1, and C_π is the total base-emitter capacitance. This equation neglects the effect of C_μ. The $(2\pi f_T L_e + r_b)$ term should be made large enough for impedance matching. The imaginary part of this equation is cancelled by the bond wire L_1 in series with the external blocking capacitor C_1.

Capacitor C_7 is a bypass capacitor used to prevent noise of the bias circuit from entering the base of Q_1. It also helps to stabilize the bias circuit. As discussed in section

3.3, it is undesirable to place a bypass capacitor at node X. Although placing a bypass capacitor at node X can help to filter noise from the bias circuit, the noise contribution from R_1 (which needs to be small to exploit the class AB behavior discussed in section 3.2) becomes significant (increase NF of driver stage by 0.8 dB and NF of the mixer by 1.2 dB), as a result of low impedance at node X. Since node X has high impedance at the RF, small R_1 does not affect impedance matching at the RF input port.

This common-emitter driver stage with inductive degeneration exhibits a class AB behavior as described in section 3.2. Fig. 4.8 shows the simulated signal current amplitude

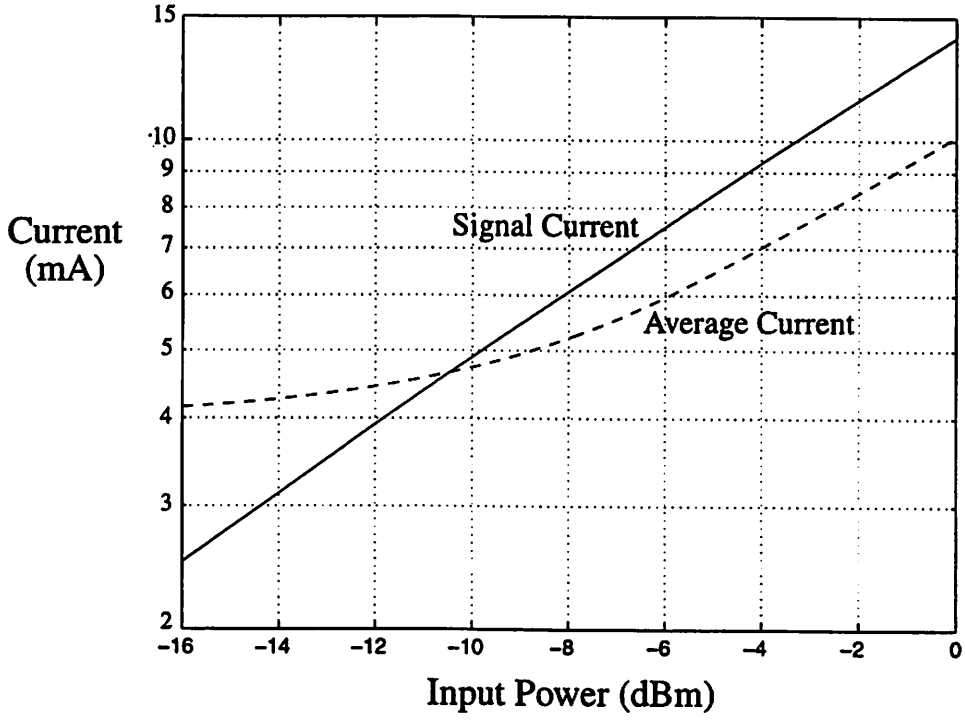

Fig. 4.8. Simulated Output Currents of Class AB Transconductance Stage versus Input Power

and average current of the class AB driver stage as a function of RF input power. Simulation shows that the driver stage biased at a collector current of 4 mA has an input P_{-1dB} of

0 dBm. As discussed in section 3.2, the presence of DC (resistive) feedback in the common-emitter driver stage can suppresses the class AB behavior. To avoid gain compression caused by the DC feedback, resistors R_1 (node X has low impedance at low-frequency) and the resistance at the emitter of Q_1 should be minimized. However, R_1 should be large enough to attenuate the noise contribution from the bias circuit. A resistance value of 200Ω is used for R_1 as a compromise between noise figure and P_{-1dB}.

The nonlinear behavior of this mixer is dominated by that of the differential switching pair (Q_2 and Q_3) caused by the large C_{je} of the switching devices used. The f_T of the switching devices (Q_2 and Q_3) is less than a factor of 4 higher than the LO frequency. On the other hand, the linearity of the common-emitter driver stage is very good at high frequency because the degeneration impedance ($j\omega L_e$) increases with frequency.

The differential switching pair (Q_2 and Q_3) should be driven by a large LO signal to minimize its noise contribution (discussed in section 3.3). Fig. 4.9 shows the simulated noise figure (NF) of the mixer (LO buffer not included) as a function of differential LO signal amplitude. However, a very large LO signal amplitude would decrease the linearity of the mixer as discussed in section 3.1. Fig. 4.10 shows the simulated input third-order intercept point (IP_3) of the mixer as a function of differential LO signal amplitude. When the LO signal amplitude is small, the input IP_3 increases with LO signal amplitude. However, when the LO signal amplitude exceeds -6 dBV, the input IP_3 decreases with LO signal amplitude. For the same reason, the device sizes should be kept small to reduce the C_{je}. On the other hand, reasonably large devices should be used to reduce the r_b noise contribu-

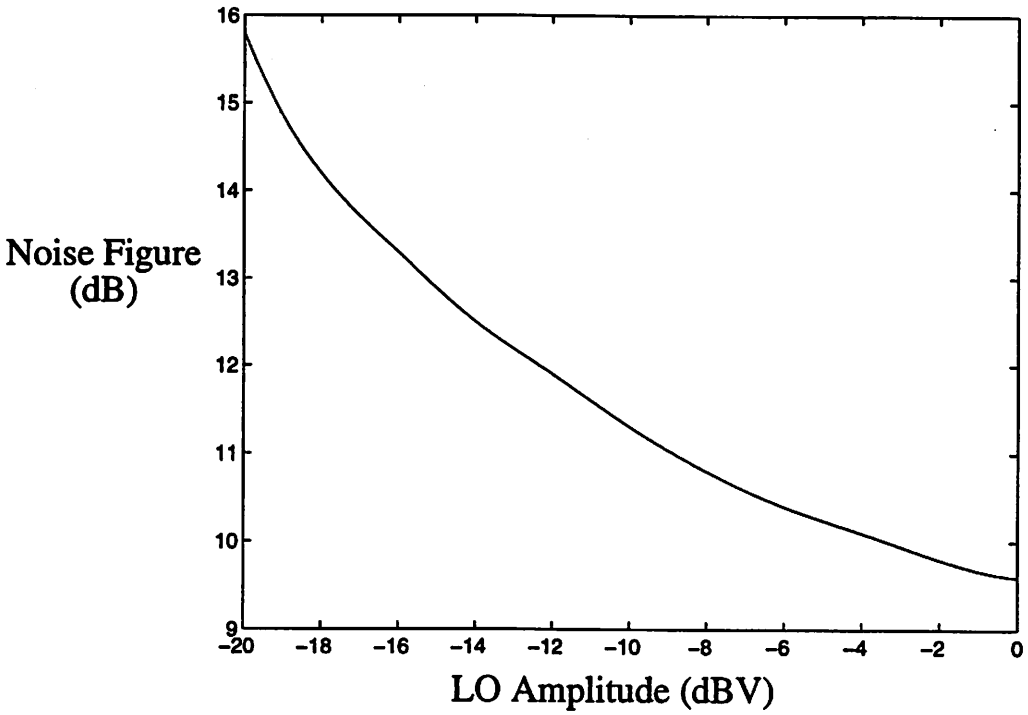

Fig. 4.9. Simulated Mixer Noise Figure versus LO Signal Amplitude

tion and the voltage drop across r_b (reduce the effective LO signal amplitude driving the switching pair). Large LO amplitudes also increase power consumption and LO feedthrough, as well as decreasing head room at the collectors of Q_2 and Q_3. Considering the trade-off among noise figure, linearity and power consumption, a differential LO amplitude of 0.4V or -8 dBV is used in this design.

As discussed in section 3.3, single-balanced mixers do not reject noise from the driver stage at the IF. Since the driver stage has high gain at the IF (due to the inductive degeneration), the output noise power of the mixer would increase significantly if single-ended output were taken. This common-mode noise can be suppressed by either taking the IF outputs differentially or performing differential to single-ended conversion. Since most

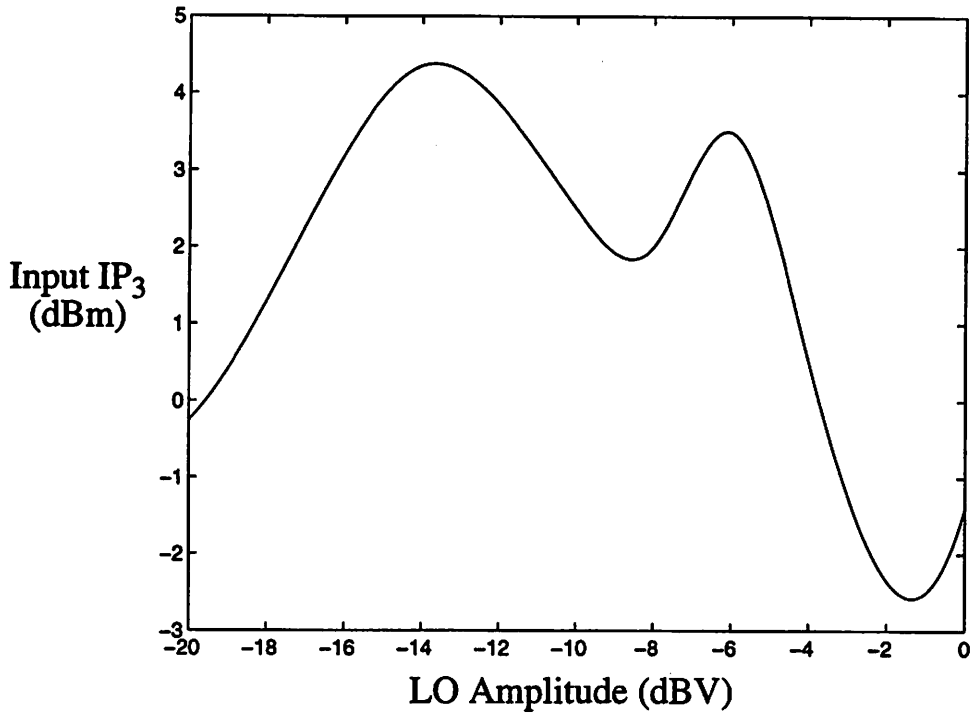

Fig. 4.10. Simulated Mixer Input IP_3 versus LO Signal Amplitude

IF filters are single-ended, the current combiner network [16] shown in Fig. 4.11 is used to

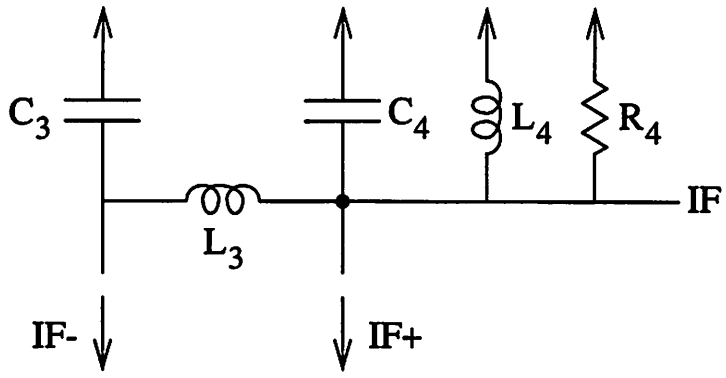

Fig. 4.11. Current Combiner Network

perform the differential to single-ended conversion. Capacitor C_3 and inductor L_3 resonate

partially $\left(\frac{1}{2\pi\sqrt{2L_3C_3}} = IF\right)$ and reverse the phase of signal current IF- so that it can added in phase to the signal current IF+. Capacitor C_4 (= C_3) is used to cancel the residual reactance caused by partial resonance between C_3 and L_3. C_3 and C_4 are implemented by monolithic MOS capacitors. Due to the large inductance, L_3 is implemented externally. L_4 is an external AC choke used to bias the collectors of Q_2 and Q_3 to the power supply voltage, while R_4 defines the output resistance at the IF port. This implementation is lower in cost than a transformer. The dual of this network (C_3 and C_4 are replaced by inductors, and L_3 is replaced by a capacitor) is not suitable for this design because a single-balanced mixer does not reject LO and RF feedthrough at the IF output port, and hence the capacitors C_3 and C_4 are needed to attenuate these high-frequency feedthrough signals.

If the switching pair were driven directly by an external LO, 2 dBm of LO signal power would be required. To reduce the power consumption of the external LO, a LO buffer with a voltage gain of 12 dB is included in the design. Fig. 4.12 shows the basic circuit topology of the LO buffer. The output terminals (LO+ and LO-) of the LO buffer are connected directly to the bases of the differential switching pair (Q_2 and Q_3) of the mixer. Resistor R_9 is used for level shifting to match the DC level of the output terminals of the buffer to the bases of the switching pair. One side of the differential pair (Q_{11} and Q_{12}) accepts the LO input signal, while the other side is AC grounded by series tuning between capacitor C_9 (external capacitor for good AC ground) and a bond wire L_9. Since the differential pair (Q_{11} and Q_{12}) is not degenerated, the impedance looking into the base of Q_5 (due to large C_π) is too low for impedance matching. The f_T of the devices (Q_{11} and Q_{12})

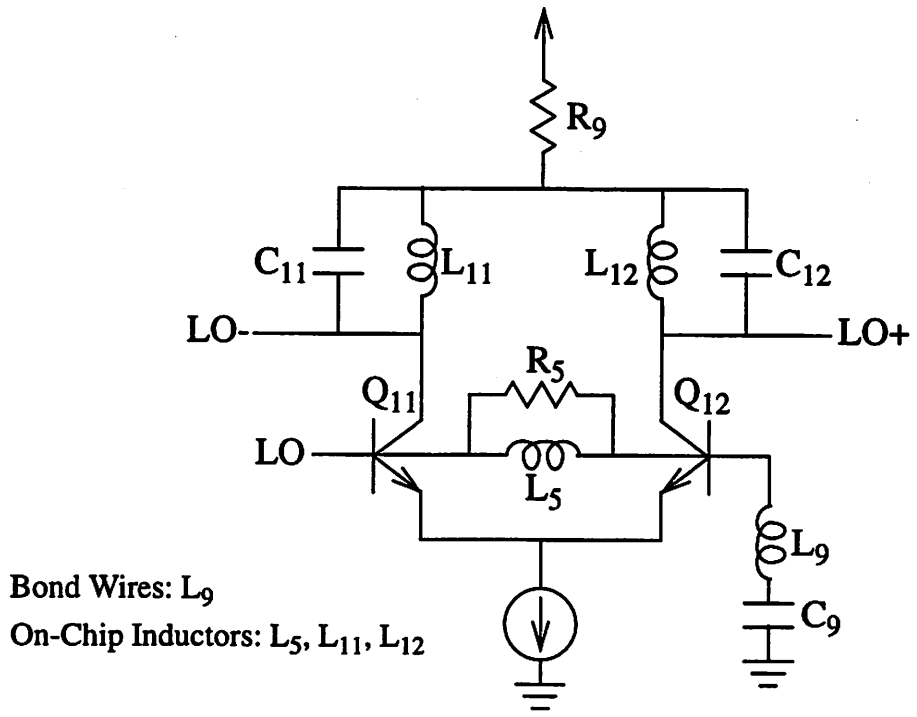

Fig. 4.12. LO Buffer

is only a factor of 3 higher than the LO frequency. An integrated spiral inductor L_5 is needed to provide tuning with the C_π of Q_5 and Q_6. Resistor R_5 is used to define the input resistance at the LO input port for impedance matching.

For a single-balanced design, the noise from the LO buffer at the IF can feedthrough to the IF output port (discussed in section 3.3). Hence, integrated spiral inductors L_{11} and L_{12} (low impedance at the IF) are used at the output of the LO buffer to remove this noise. The inductors also provide tuning with the input capacitance of the differential switching pair (Q_2 and Q_3) to reduce the bias current requirement of the LO buffer. Since the capacitance at the bases of Q_2 and Q_3 is nonlinear, the LO signal at the output of the LO buffer becomes highly distorted without the linear capacitors C_{11} and C_{12}. This LO signal distor-

tion tends to decrease the linearity of the mixer. Charges stored in the linear capacitors smooth out the LO waveform transition at the buffer output. The value of C_{11} and C_{12} should be much larger than C_π of Q_2 and Q_3 to reduce this LO signal distortion. The upper limit is set by current consumption and the Q of L_{11} and L_{12}.

The mixer is implemented in a 1μm BiCMOS process with peak npn f_T of 13 GHz and CMOS L_{eff} of 0.8 μm. The CMOS devices are not used in the active circuits. PMOS devices, instead of pnp bipolar devices, are used to implement the upper current mirrors. Fig. 4.13 shows the die micrograph. The bonding pads are electrostatic discharge (ESD) protected and the die is housed in a 20-pin plastic Shrink Small Outline Package (SSOP). The ESD buses are routed at the perimeter (outside bonding pads) of the die to avoid crossing with the signal lines. This reduces the lengths of the signal buses connecting the active circuits to the bonding pads, and the mutual coupling among the signal buses through the ESD buses. Transistor Q_1 is placed close to the bonding pads to which the bond wires used for degeneration are connected. This is to minimize parasitic capacitance and resistance at the emitter of Q_1. To further minimize the routing distance of high-frequency signals, the mixer and LO buffer are placed next to their corresponding bonding pads. The differential LO signal buses from the output terminals of the LO buffer are routed next to each other to reduce coupling of LO signal to other circuits. This technique is also applied to the differential IF buses at the output of the mixer.

The degeneration inductor L_e is implemented by three adjacent bond wires and pins in parallel. The LO pin and the AC ground pin (L_9) of the LO buffer are placed next to each other (on the bottom side in Fig. 4.13) to minimize the cross-sectional area of the

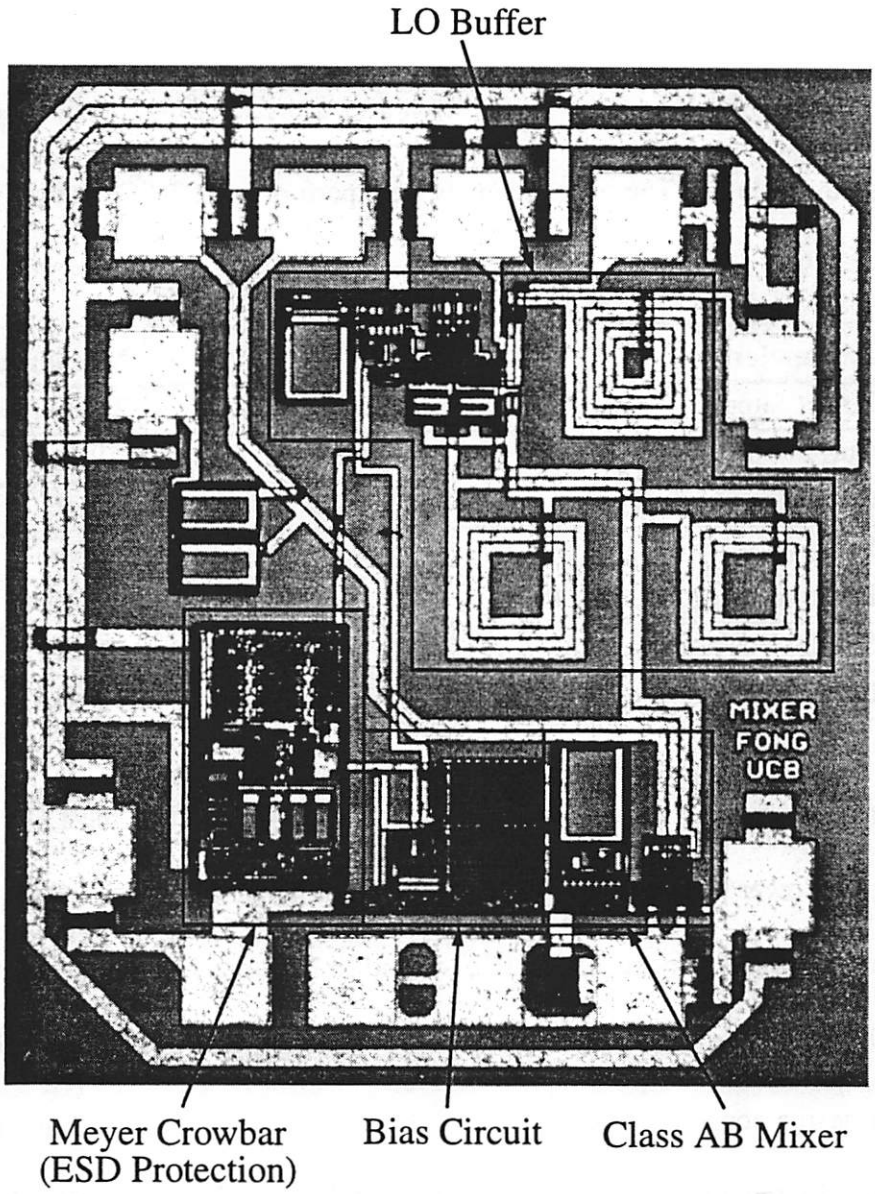

Fig. 4.13. Chip Micrograph

resulting current loop. The two LO buffer pins and the two IF pins are placed on the opposite side (top side in Fig. 4.13) of the package from the RF pin and the emitter-degeneration pins (bottom side in Fig. 4.13) to minimize coupling. This helps to reduce LO-to-RF feedthrough. On the other, LO-to-IF feedthrough does not cause major problem since

there are capacitors at the IF output port to attenuate the high-frequency feedthrough signals.

The simulated (using HSPICE) and measured performance of the mixer is summarized in Table 4.1. The measurements were performed at 25°C with a 3V supply, using LO

Table 4.1 Performance Summary

Parameters	Simulations	Measurements
Power Supply	2.7V to 5.5V	2.7V to 5.5V
Current Consumption	8 mA	7.9 mA
Conversion Gain (Power)	4 dB	4.5 dB
Input Third-Order Intercept Point	2.5 dBm	1 dBm
Input 1dB Compression Point	-5 dBm	-7.5 dBm
Single-Sideband Noise Figure	10.8 dB	10 dB
LO-to-RF Feedthrough	-30 dBc	-28 dBc

signal power of -8 dBm. Since the LC tank at the output of the LO buffer is tuned to a slightly lower frequency (due to parasitic capacitance), a higher LO signal power than the simulated value is needed. The RF, LO and IF frequencies used are 2.4 GHz, 2.6 GHz and 200 MHz respectively. The input IP_3 was measured with two RF tones of 1 MHz spacing. The design consumes total current of about 8 mA, where 4 mA, 3 mA and 1 mA are consumed by the mixer core, the LO buffer and the bias circuit respectively. The average current of the whole design increases to 10.3 mA when -7.5 dBm of signal power is applied to the RF input port. If this were a class A design, the mixer core would require 6 mA of bias current to have -8 dBm of input P_{-1dB}.

The difference in linearity performance (IP_3 and P_{-1dB}) between simulation and measurement is mainly caused by the imperfect device models used in the simulation. For

instance, bipolar device characteristics in the saturation region (or at the edge of saturation region) is not simulated well by the device models. Furthermore, the bipolar devices are characterized at low frequency using lump circuit models. Distributed RC effects (distributed r_b, C_π, and C_μ) within the devices are not simulated. Substrate-coupling effects, which is difficult to model, increase the gap between simulation and measurement results.

4.3 Low-Noise Amplifier

The applications of the design and optimization techniques presented in CHAPTER 3 have been demonstrated in the two mixer examples presented in the previous sections. The techniques can also be applied to many other RF building blocks, such as the low-noise amplifiers and power amplifiers.

Fig. 4.14 shows the typical circuit topology of a low-noise amplifier (LNA). The gain stage (Q_1) of the LNA is similar to the driver stage of the single-balanced mixer, and hence similar design and optimization techniques can be used. The gain stage uses inductive degeneration to increase its linearity. Class AB behavior can be exploited to reduce the bias current requirement, and to increase the power efficiency. To exploit the class AB behavior, DC feedback caused by the parasitic emitter resistance and the bias resistor R_1 needs to be minimized (discussed in section 3.2). To reduce the noise contribution from r_b, a large device is used for Q_1. The bias current is optimized to reduce the sum of base and collector shot noise contributions (discussed in section 3.3). A bypass capacitor should not be placed at node X, as it would increase the noise figure (discussed in section 3.3).

The linearity requirement for LNA can be met easily with small amount of degeneration since the RF input power level is low. On the other hand, the noise performance is

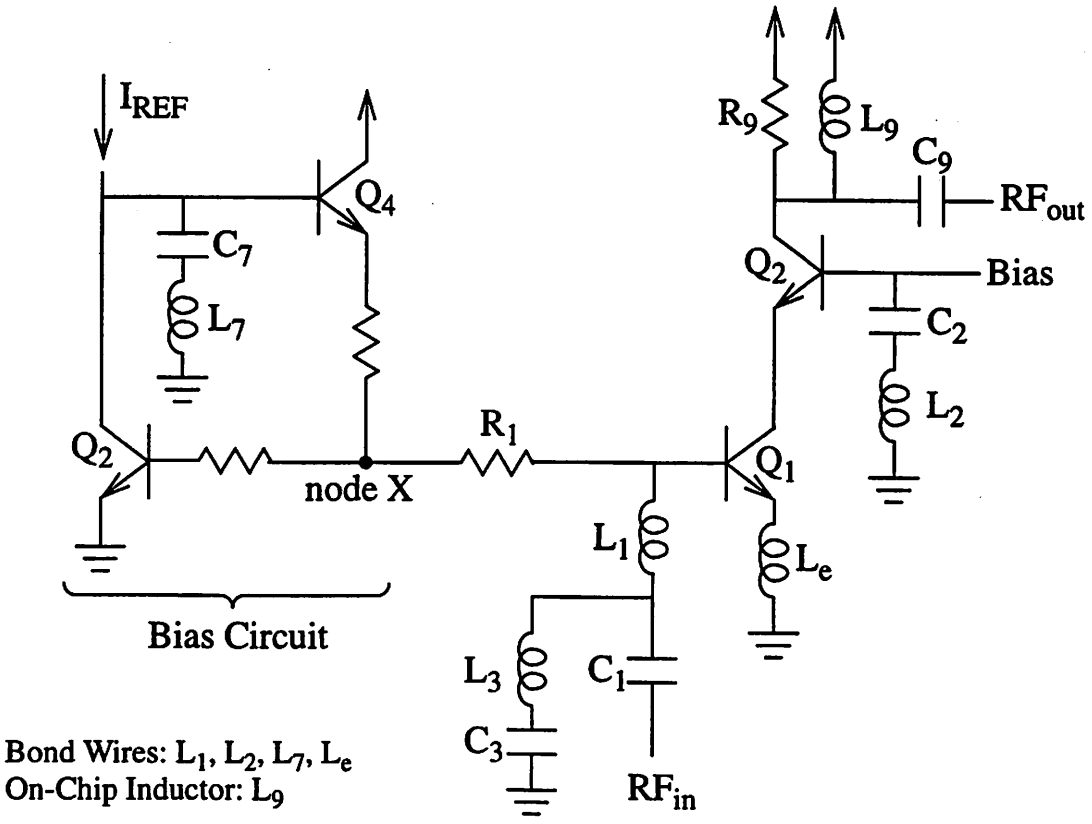

Fig. 4.14. Low-Noise Amplifier

extremely important since there is no gain stage before the LNA (unlike a mixer) to reduce its noise contribution. Therefore, the degeneration inductor (L_e) is minimized to reduce the noise figure. The lower limit is set by the number of bond wires available and the maximum gain allowed without overloading the downconversion mixer. In some applications, the noise performance is so important that an external impedance-matching network is used to translate the source resistance (R_s) to some optimal value (different from 50Ω). In such cases, the impedance-matching network shown in Fig. 2.6 or Fig. 2.8 can be used. On the other hand, such a matching network is typically omitted in a mixer design in order to reduce the number of external components. In some applications where there is a strong

blocker, a low-frequency trap (L_3, C_3) is needed to attenuate the low-frequency noise from the bias circuit.

Transistor Q_2 is a cascode transistor used to increase the power gain of the LNA. It can be viewed as a common-base amplifier. It also helps to isolate the RF input port from the output port. Without the cascode transistor, the Miller Effect caused by C_μ of Q_1 can reduce the power gain and cause impedance mismatch at the RF input port. Series tuning between C_2 and L_2 provides an AC ground for the base of Q_2 at the RF. To increase the power gain, load resistor R_9 is typically designed to be larger than 50Ω. It is matched to 50Ω by using the impedance-matching network formed by L_9 and C_9.

In contrast to a downconversion mixer of which the input frequency is different from the output frequency, a LNA can run into stability problems (oscillation) easily. The unconditional stability criteria shown below have to be checked to make sure that the LNA does not oscillate (at all frequencies) at any input and output loading conditions.

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} > 1 \text{ , and} \tag{4.5}$$

$$|S_{11}S_{22} - S_{12}S_{21}| < 1 \text{ .} \tag{4.6}$$

Mutual couplings between L_2 and L_e, and between L_9 and L_e need to be minimized. These coupling mechanisms form positive feedback loops which may cause oscillation.

4.4 Power Amplifier

Fig. 4.15 shows the block diagram of a typical three-stage power amplifier. Multiple gain stages are used to increase the power gain (some lower-gain designs use only two

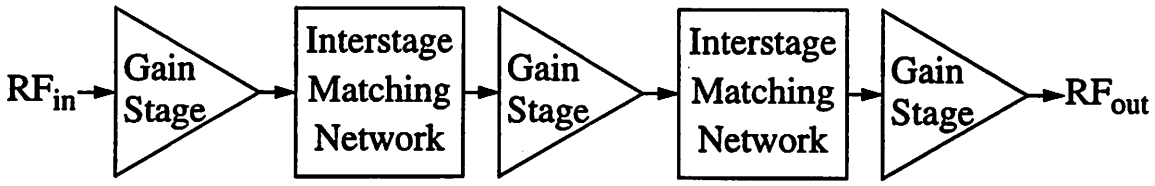

Fig. 4.15. Block Diagram of Power Amplifier

gain stages). An output matching network (not shown in Fig. 4.15) is used to match the load resistance (50Ω) to the optimal impedance needed at the output terminal of the output gain stage for maximum power efficiency. Similarly, the last interstage matching network is used to match the input impedance of the output gain stage to the optimal impedance needed at the output terminal of the driver stage (before the output gain stage). High-Q components are used in the matching networks to minimize the power loss, and to maximize the power efficiency. For power efficiency reasons, the output matching network is implemented by off-chip components (higher Q than on-chip components), since the power consumption of the PA is dominated by the output gain stage. The interstage matching networks are implemented by monolithic components to reduce the number of external components and to achieve a high level of integration.

The circuit topology of each gain stage is similar to that of a LNA except that the transistor size is much larger (to be able to handle large currents), and that there is no cascode device (to increase the voltage headroom for power efficiency reasons). Unlike the LNA and the downconversion mixer, the RF input signal power (from the upconversion mixer) to the PA is much higher than the noise floor, and hence noise performance is not an important design criterion. Therefore, the active devices are typically biased for the maximum power efficiency, instead of the lowest noise figure. In a class A design, the

active device of the gain stage is normally biased close to the corner of Kirk Effect.

Class AB behavior, discussed in section 3.2, can be exploited to reduce the bias current requirement, and to improve the power efficiency at both low and high output power levels. Typically, a power amplifier has to be able to output a range of power. In a class A design, the gain stages have to be biased with sufficient collector current to be able to output the maximum power required. However, the power amplifier only needs to deliver medium output power most of the time. Hence, the extra bias current is wasted. On the other hand, a class AB design can be biased at a much lower quiescent current level. As shown in Fig. 3.7, the average current (power consumption) depends on the output power (input power). Furthermore, at large output power level (input power level), the signal current amplitude becomes larger than the average current. This makes the class AB design more power efficient that a class A design, even at the maximum output power level.

Unlike a LNA (low power) which has no thermal runaway problem, a small amount of resistive degeneration (realized using ballasting resistors) has to be introduced at the emitters of the gain stages in a power amplifier to prevent thermal runaway. Thermal runaway is positive feedback phenomenon where the bias current of a bipolar transistor increases due to an increase in temperature. The increase in bias current increases the temperature further. If this positive feedback phenomenon is not checked, the device can be destroyed. Hence, resistive degeneration is needed to reduce the loop gain of this positive thermal feedback loop. However, this degeneration resistor can also suppress the class AB behavior. A trade-off between power efficiency (exploiting class AB behavior) and circuit robustness has to be considered carefully in the design. As shown in section 3.1, the bal-

lasting resistor also reduces the linearity (IP_3) of the gain stage. If the active devices in the gain stages are implemented by FETs, ballasting resistors are not needed because the bias current decreases with temperature.

4.5 Discussion

Besides the examples given above, the design and optimization techniques discussed in CHAPTER 3 can be applied to many other analog building blocks. For instance, the class AB design can be used for any common-emitter amplifier or gain stage. It is also applicable to common-source amplifier or gain stage using FET as the active device. Since the FET has no DC gate current, the gate bias resistor does not have to be minimized to exploit the class AB behavior. However, the main disadvantage of using the class AB behavior is that a fully differential design cannot be used. The IM_3 equations derived in section 3.1 are very general, and can be used to optimize the linearity of common-emitter and differential pair transconductance stages with arbitrary degeneration. The concepts behind noise performance optimization and noise mixing phenomenon discussed as section 3.3 can be used in many linear and nonlinear analog building blocks.

The desensitization mechanisms by a blocker discussed in section 3.4 concentrate on the downconversion mixer. However, the noise mixing phenomenon is very similar to those in the upconversion mixers and power amplifiers. In these applications, the large signal is the desired signal (instead of the undesired blocker), which mixes the low-frequency noise from the bias circuit and the LO phase noise to the sidebands of the desired signal and raises the sideband noise floor.

CHAPTER 5

Conclusions

In this thesis, design and optimization techniques for monolithic RF downconversion mixers have been presented. The class AB behavior of the common-emitter transconductance stage with inductive degeneration has been studied. It can be exploited to improve the 1 dB compression point, the blocking performance, and the power efficiency. To exploit the class AB behavior, resistive (DC) feedback at the emitter and base of the driver transistor has to be minimized. This class AB concept is also applicable to the common-source FET transconductance stage.

Third-order intermodulation equations in Volterra Series for both common-emitter and differential-pair transconductance stages were derived. The equations can be applied to transconductance stages with arbitrary emitter degeneration and source impedances. The equations show that common-emitter transconductance stages are more linear than differential- pair transconductance stages with the same gain and bias current. The equations also show that inductive degeneration is more linear than both resistive and capacitive degeneration. Also, design guidelines to improve the linearity of the differential switching stage were presented.

Noise figure equations for both common-emitter and differential-pair driver stages were derived. The equations show that the collector shot noise contribution decreases with bias current, whereas the base shot noise contribution increases with bias current. Unlike an FET driver stage, it is not possible to achieve simultaneous noise and impedance

matching at the input of the bipolar implementation unless the noise figure is dominated by the collector shot noise contribution. In addition, methods to minimize the noise contribution from the differential switching stage have been presented. With inductive degeneration, high-side mixing has better noise performance than low-side mixing. Methods to handle the IF noise feedthrough problems (from both driver stage and LO buffer) in a single-balanced design were presented.

The desensitization mechanisms by a blocker were discussed. A strong blocker can increase the noise figure of a mixer by causing gain compression and increasing the output noise power. The blocker increases the output noise power by mixing the low-frequency noise from the bias circuit up to the RF, and by mixing the LO phase noise to the IF (reciprocal mixing). The low-frequency noise from the bias circuit can be suppressed by using a low-frequency RC filter or a low-frequency trap network. The reciprocal mixing problem can only be alleviated by reducing the blocker power or the LO phase noise.

Two design examples using the design and optimization techniques were presented. The 900 MHz mixer, implemented in a 25 GHz f_T bipolar process, consumes 10.2 mA total current from a 3V power supply. The design has a power gain of 7.5 dB, and operates with supply voltages from 2.7V to 5V. The single-sideband noise figure and the input 1 dB compression point are 7.5 dB and -1.5 dBm respectively. The 2.4 GHz mixer, implemented in a 13 GHz f_T BiCMOS process, consumes 7.9 mA total current from a 3V power supply. The design has a power gain of 4.5 dB, a single-sideband noise figure of 10 dB, an input third-order intercept point of 1 dBm, and an input 1 dB compression point of -7.5 dBm. Applications of the techniques to other RF building blocks, such as low noise amplifiers and power amplifiers, were discussed.

Appendix A

Derivation of Nonlinearity Equations

A.1 Common-Emitter Transconductance Stage

The Kirchhoff's Voltage Law equation for the common-emitter transconductance stage is

$$V_s = (sC_{je}V_\pi + s\tau_F I_c + I_c/\beta_0)(Z_b + Z_e) + I_c Z_e + V_\pi \ . \tag{A.1}$$

Substituting

$$\begin{aligned} I_c &= I_Q \exp\left(\frac{V_\pi}{V_T}\right) \\ &= I_Q\left[\left(\frac{V_\pi}{V_T}\right) + \frac{1}{2}\left(\frac{V_\pi}{V_T}\right)^2 + \frac{1}{6}\left(\frac{V_\pi}{V_T}\right)^3 + \ldots\right] \ , \text{and} \end{aligned} \tag{A.2}$$

$$V_\pi = C_1(s_1) \circ V_s + C_2(s_1, s_2) \circ V_s^2 + C_3(s_1, s_2, s_3) \circ V_s^3 + \ldots \tag{A.3}$$

into equation (A.1), and solving for $C_1(s_1)$, $C_2(s_1,s_2)$ and $C_3(s_1,s_2,s_3)$ results in

$$C_1(s) = \frac{1}{[sC_{je}Z(s) + s\tau_F g_m Z(s) + g_m Z(s)/\beta_0 + 1 + g_m Z_e(s)]} \ , \tag{A.4}$$

$$\begin{aligned} C_2(s_1, s_2) = -C_1(s_1 + s_2)C_1(s_1)C_1(s_2)\frac{I_Q}{2V_T^2}\Bigg[&(s_1 + s_2)\tau_F Z(s_1 + s_2) \\ &+ \frac{Z(s_1 + s_2)}{\beta_0} + Z_e(s_1 + s_2)\Bigg] \end{aligned} \quad , \text{and} \tag{A.5}$$

$$C_3(s_1, s_2, s_3) = -\frac{A_1(s_1+s_2+s_3)I_Q}{6V_T^3}[A_1(s_1)A_1(s_2)A_1(s_3) + 6V_T\overline{A_1A_2}] \quad . \quad (A.6)$$
$$\times\left[(s_1+s_2+s_3)\tau_F Z(s_1+s_2+s_3)\right.$$
$$\left.+\frac{Z(s_1+s_2+s_3)}{\beta_0} + Z_e(s_1+s_2+s_3)\right]$$

Substituting equation (A.3) into equation (A.2) results in

$$A_1(s) = g_m C_1(s) \ , \quad (A.7)$$

$$A_2(s_1, s_2) = g_m C_2(s_1, s_2) + \frac{I_Q}{2V_T^2} C_1(s_1)C_1(s_2) \ , \text{and} \quad (A.8)$$

$$A_3(s_1, s_2, s_3) = g_m C_3(s_1, s_2, s_3) + \frac{I_Q}{6V_T^3} C_1(s_1)C_1(s_2)C_1(s_3) + \frac{I_Q}{V_T^2}\overline{C_1C_2} \ . \quad (A.9)$$

Equations (3.3), (3.4) and (3.5) can be obtained by expanding equations (A.7), (A.8) and (A.9) respectively.

A.2 Differential-Pair Transconductance Stage

The Kirchhoff's Voltage and Current Law equations for the differential-pair transconductance stage are

$$V_s = (sC_{je}V_{\pi 1} + s\tau_F I_{c1} + I_{c1}/\beta_0)(Z_b + Z_e) + I_{c1}Z_e + V_{\pi 1}$$
$$-(sC_{je}V_{\pi 2} + s\tau_F I_{c2} + I_{c2}/\beta_0)(Z_b + Z_e) - I_{c2}Z_e - V_{\pi 2} \ , \text{and} \quad (A.10)$$

$$0 = sC_{je}V_{\pi 1} + s\tau_F I_{c1} + I_{c1}/\beta_0 + I_{c1} + sC_{je}V_{\pi 2} + s\tau_F I_{c2} + I_{c2}/\beta_0 + I_{c2} \ . \quad (A.11)$$

Substituting

$$I_{c1} = I_T\left[\left(\frac{V_{\pi 1}}{V_T}\right) + \frac{1}{2}\left(\frac{V_{\pi 1}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{V_{\pi 1}}{V_T}\right)^3 + \ldots\right] \ , \quad (A.12)$$

$$I_{c2} = I_T\left[\left(\frac{V_{\pi 2}}{V_T}\right) + \frac{1}{2}\left(\frac{V_{\pi 2}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{V_{\pi 2}}{V_T}\right)^3 + \ldots\right] , \tag{A.13}$$

$$V_{\pi 1} = D_1(s_1) \circ V_s + D_2(s_1, s_2) \circ V_s^2 + D_3(s_1, s_2, s_3) \circ V_s^3 + \ldots \text{ , and} \tag{A.14}$$

$$V_{\pi 2} = -D_1(s_1) \circ V_s + D_2(s_1, s_2) \circ V_s^2 - D_3(s_1, s_2, s_3) \circ V_s^3 + \ldots \tag{A.15}$$

into equations (A.10) and (A.11), and solving for $D_1(s_1)$, $D_2(s_1,s_2)$ and $D_3(s_1,s_2,s_3)$ results in

$$D_1(s) = \frac{1}{2[sC_{je}Z(s) + s\tau_F g_m Z(s) + g_m Z(s)/\beta_0 + 1 + g_m Z_e(s)]} , \tag{A.16}$$

$$D_2(s_1, s_2) = -D_1(s_1)D_1(s_2)\frac{I_T[(s_1 + s_2)\tau_F + 1/\beta_0 + 1]}{2V_T^2[(s_1 + s_2)C_{je} + (s_1 + s_2)\tau_F g_m + g_m/\beta_0 + g_m]} , \tag{A.17}$$

$$\begin{aligned} D_3(s_1, s_2, s_3) = -\frac{D_1(s_1 + s_2 + s_3)I_T}{3V_T^3}[D_1(s_1)D_1(s_2)D_1(s_3) + 6V_T\overline{D_1 D_2}] \\ \times\left[(s_1 + s_2 + s_3)\tau_F Z(s_1 + s_2 + s_3)\right. \\ \left. + \frac{Z(s_1 + s_2 + s_3)}{\beta_0} + Z_e(s_1 + s_2 + s_3)\right] \end{aligned} . \tag{A.18}$$

Substituting equations (A.14) and (A.15) into equations (A.12) and (A.13) respectively results in

$$B_1(s) = g_m D_1(s) , \tag{A.19}$$

$$B_2(s_1, s_2) = g_m D_2(s_1, s_2) + \frac{I_T}{2V_T^2} D_1(s_1)D_1(s_2) \text{ , and} \tag{A.20}$$

$$B_3(s_1, s_2, s_3) = g_m D_3(s_1, s_2, s_3) + \frac{I_T}{6V_T^3} D_1(s_1)D_1(s_2)D_1(s_3) + \frac{I_T}{V_T^2}\overline{D_1 D_2} . \tag{A.21}$$

Equations (3.15), (3.16) and (3.17) can be obtained by expanding equations (A.19), (A.20) and (A.21) respectively.

References

[1] S. A. Mass, *Microwave Mixers*, Artech House, Inc., 1986.

[2] D. D. Weiner and J. F. Spina, *Sinusoidal Analysis and Modeling of Weakly Nonlinear Circuits*, Van Nostrand Reinhold Company, 1980.

[3] S. A. Mass, *Nonlinear Microwave Circuits*, Artech House, Inc., 1988.

[4] G. D. Vendelin, A. M. Pavio, and U. L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*, John Wiley & Sons, Inc., 1990.

[5] S. Weiner, D. Neuf, and S. Spohrer, "2 To 8 GHz Double Balanced MESFET Mixer with +30 dBm Input 3rd Order Intercept", IEEE MTT-S International Microwave Symposium Digest, vol. 11, pp. 1097-1100, 1988.

[6] S. A. Maas, "A Low Distortion GaAs MESFET Resistive Mixer", Microwave Journal, vol. 31, no. 3, pp. 213-220, March 1988.

[7] R. G. Meyer, A. K. Wong, "Blocking and Desensitization in RF Amplifiers", IEEE Journal of Solid-State Circuits, vol. 30, no. 8, pp. 944-946, August 1995.

[8] K. L. Fong, C. D. Hull, R. G. Meyer, "A Class AB Monolithic Mixer for 900 MHz Applications", IEEE Journal of Solid-State Circuits, vol. 32, no. 8, pp. 1166-1172, August 1997.

[9] C. D. Hull, J. L. Tham, and R. R. Chu, "A Direct-Conversion Receiver for 900 MHz (ISM Band) Spread-Spectrum Digital Cordless Telephone", IEEE Journal of Solid-State Circuits, vol. 31, no. 12, pp. 1955-1963, December 1996.

[10] K. L. Fong and R. G. Meyer, "High-Frequency Nonlinearity Analysis of Common-Emitter and Differential-Pair Transconductance Stages", IEEE Journal of Solid-State Circuit, accepted for publication.

[11] C. D. Hull, "Analysis and Optimization of Monolithic RF Downconversion Receivers", Ph.D. dissertation, University of California, Berkeley, California, 1992.

[12] R. G. Meyer, "Intermodulation in High-Frequency Bipolar Transistor Integrated-Circuit Mixers", IEEE Journal of Solid-State Circuit, vol. sc-21, no. 4, pp. 534-537, August 1986.

[13] K. L. Fong, R. G. Meyer, "A 2.4 GHz Monolithic Mixer for Wireless LAN Applications", IEEE Custom Integrated Circuits Conference, pp. 9.4.1-9.4.4, May 1997.

[14] P. R. Gray, R. G. Meyer, *Analysis and Design of Analog Integrated Circuit*, 3rd edition, John Wiley & Sons, Inc., 1993.

[15] R. G. Meyer, W. D. Mack, "A 1-GHz BiCMOS RF Front-End", IEEE Journal of Solid-State Circuits, vol. 29, no. 3, pp. 350-355, March 1994.

[16] S. H. Lee, "Resonance Balun with Arbitrary Impedance", US Patent No. 5412355.

[17] L. E. Larson, *RF and Microwave Circuit Design for Wireless Communications*, Artech House, Inc., 1996.

[18] J. Smith, *Modern Communication Circuits*, McGraw-Hill Book Company, 1986.

[19] D. O. Pederson and K. Mayaram, *Analog Integrated Circuits for Communication*, Kluwer, 1991.

[20] D. M. Pozar, *Microwave Engineering*, Addison-Wesley Publishing Company, 1990.

[21] K. L. Fong, R. G. Meyer, "Monolithic RF Active Mixer Design", 1997, IEEE Transactions on Circuits and Systems-Part II, submitted for publication.