HIGH-SPEED, LOW-POWER SIGMA-DELTA MODULATORS FOR RF BASEBAND CHANNEL APPLICATIONS

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
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94720

Abstract

High-Speed, Low-Power Sigma-Delta Modulators for RF Baseband Channel Applications

by
Arnold R. Feldman

Doctor of Philosophy in Engineering-Electrical Engineering and Computer Sciences

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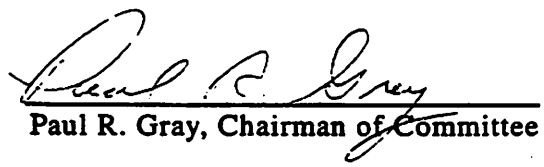
Professor Paul R. Gray, Chair

Recent efforts in the design of integrated circuits for RF communication transceivers have focussed on achieving higher levels of integration as well as adaptability to multiple RF communication standards. Direct conversion and wideband IF double conversion receiver architectures increase integration because channel select filtering may be performed on chip at baseband. To achieve adaptability to multiple communication standards, programmable channel select filtering can be more easily performed in the digital domain. A sigma-delta modulator can achieve the wide dynamic range required to detect a desired channel in the presence of strong adjacent channel interferers. A digital decimation filter can then remove both the interferers and the quantization noise which fall out in the same frequency band

This thesis describes architectural and circuit techniques for high-speed sigma-delta modulators. A new 2-2-2 cascade sigma-delta architecture which can achieve 14 bit resolution at only 16 X oversampling ratio is introduced. Power reduction strategies are developed at both the sigma-delta architecture and circuit design levels. An experimental prototype was designed and fabricated in a 0.72 μm CMOS process to test

the new architecture and verify the effectiveness of the power reduction strategies. The modulator achieves 71 dB of peak SNDR and 77 dB of dynamic range. The chip dissipates 81 mW from a 3.3 V supply at 1.4 MS/s Nyquist rate and 16 X oversampling ratio.



Paul R. Gray, Chairman of Committee

Acknowledgments

First, I would like to acknowledge my advisor, Professor Paul Gray, for his guidance and support during my stay at Berkeley. His insight into circuit design and ability to keep me focussed on the big picture was critical to the project's success. I also want to thank Professor Bernhard Boser for his invaluable help and especially for sharing his sigma-delta architecture and circuit design expertise. Along with Professors Gray and Boser, I would like to thank Professor Jan Rabaey and Professor Philip Stark for serving on my qualifying exam committee. I would also like to thank Professors Gray, Boser and Stark for reading this thesis.

Fabrication of silicon is a complicated problem. Keith Onodera deserves special thanks for all of the work he did to help get my chips fabbed at National Semiconductor. Without Keith's efforts, I might still be waiting for working silicon. Other people at National I'd like to thank for their fab help are Pat Tucci, Robert Eddy, Gabriel Li and Mike Sampogna. I'd also like to thank everyone at Rockwell Semiconductor Systems, especially S.V. Kishore, Chris Hull and Frank Intveld for their help with my second tapeout.

I'd like to thank my colleagues in Professor Gray's group for their friendship and all of their help over years. Thomas Cho and Dave Cline helped me get up to speed and were incredibly patient with questions at the start of this project. My cubicle mates for much of my time in Berkeley, Chris Rudell, Todd Weigandt and Jeff Weldon helped make 550 Cory a fun place to work. Andy Abo, Sekhar Narayanaswami, Jeff Ou, Srenik Mehta, George Chien and Keith Onodera are good friends and were great people to bounce ideas off of. Best of luck to all of the newer students in the group, especially Carol Barrett, Danelle Au, and Kelvin Khoo who I've had the opportunity to work closely with in the past year. Also, thanks to Andy Abo and Jeff Weldon for their comments on parts of this thesis.

Outside of work, there were the numerous cubicle conversations, coffee breaks, lunches, the RSF and Cal basketball games. Arthur Abnous, Tom Burd, Lisa Guerra, Dave Lidsky, Tony Stratakos and Dennis Yee among other people I have probably missed come to mind. I'd also like to thank Howard Sweed for giving me a reason to visit Australia and Vanessa Tanaka for her countless emails.

Special thanks to my parents Melvin and Sandra Feldman and my sisters Ellen and Amy for their love and support. I couldn't have completed this thesis without it.

This work was supported by the Semiconductor Research Corporation. CMOS fabrication was donated by National Semiconductor and Rockwell Semiconductor Systems.

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Chapter 1

Introduction

1.1 Motivation

The market for digital radio frequency personal communication devices is rapidly expanding with the development of new services and applications. Devices such as cordless telephones, cellular telephones, and wireless LANs, utilize spectrum in the regions from 800 MHz to 2.5 GHz. This variety of applications and devices has led to a proliferation of communications standards with different modulation schemes, channel bandwidths, dynamic range requirements and so forth. In addition, consumers are demanding low-cost, low-power, and small form factor devices to satisfy these communication requirements. As a result, recent efforts in the design of integrated circuits for personal communication transceivers have focussed on increased integration in a low cost technology (e.g. CMOS) as well as adaptability to multiple RF communication standards. This requires research into new architectures and circuit techniques that enable both integration and programmability in RF transceivers [1], [2].

Increased integration by eliminating external components such as SAW filters will reduce transceiver cost, reduce the power dissipation required to drive high frequency signals off chip and shrink the form factor. However, traditional

superheterodyne receivers which require external bandpass filters for image-rejection and channel selection as well as external local oscillators are not amenable to integration. In addition to eliminating the other external components described above, suitable receiver architectures such as direct-conversion or wideband IF double-conversion will eliminate the IF channel select filter by performing channel selection on chip at baseband.

In wireless systems, a weak desired channel must be selected in the presence of strong adjacent channel interferers. Moving channel selection to baseband results in increased dynamic range requirements as compared to the conventional approach. These requirements range from greater than 80 dB for DECT (Digital European Cordless Telephone) to greater than 100 dB for GSM (a European cellular standard) [3],[4]. This wide dynamic range must be achieved at minimum power dissipation.

To achieve multi-standard capability, channel selection should be moved into the digital domain where it is easier to implement programmable filters This requires a wideband A/D converter that can digitize both the desired channel and adjacent channel interferers. Oversampled sigma-delta modulators are uniquely suited to this application because the adjacent channel interferers fall into the same band as the high-pass shaped quantization noise. Both the quantization noise and interferers can be removed by the same digital decimation filter.

1.2 Research Goals

This research seeks to address issues of integration and programmability in RF receivers by investigating the use of a high-speed sigma-delta modulator to perform channel select filtering and digitization at baseband. A more general goal of this research, which is critical for the RF application, is to develop techniques at both the architecture and circuit design levels to minimize power dissipation in high-speed

sigma-delta modulators. In the context of these goals, some key research results are summarized below:

- Demonstrated that a sigma-delta modulator can meet the baseband processing requirements for a wideband RF standard such as DECT at reasonable power dissipation. An experimental prototype implemented in a 0.72μm double-poly, double-metal CMOS process achieved 77 dB of dynamic range and dissipated 81 mW at 1.4 MS/s Nyquist rate.
- Developed a new 2-2-2 cascade sigma-delta architecture oversampling at 16 X to minimize modulator power dissipation.
- Showed that scaling integrator sampling capacitors to the minimum value required by kT/C noise at each stage in the cascade is an effective technique for reducing power dissipation.
- Developed a digital calibration scheme using an LMS adaptive filter to compensate for the effects of interstage gain mismatch in cascaded sigma-delta modulators.
- Designed a new two-stage operational amplifier with an all NMOS signal path and capacitive level-shift between the stages and optimized this amplifier to minimize power dissipation.

1.3 Thesis Organization

Chapter 2 provides a brief overview of RF receiver architectures and discusses various approaches to channel select filtering for highly integrated RF receivers. Sigma-delta modulators are introduced in Chapter 3 including a discussion of performance metrics, tradeoffs between various architectures, and fundamental limits on power dissipation. Chapter 4 describes various low-power design techniques at the sigma-delta architecture level. The effects of mismatch and calibration techniques are discussed in Chapter 5. Chapter 6 focuses on the design and power optimization of switched-capacitor integrators, the key circuit building block in a sigma-delta modulator. An experimental prototype and test results are discussed in Chapter 7. Chapter 8 contains concluding remarks and recommendations for future work.

Chapter 2
Baseband Processing for RF Applications

2.1 Introduction

RF receivers are characterized by their sensitivity and selectivity. Sensitivity refers to the ability of a receiver to demodulate a small desired signal in the presence of thermal noise at acceptable bit error rate (BER). Selectivity is a measure the ability of a receiver to demodulate a small desired signal in the presence of much stronger signals in adjacent frequency bands at acceptable BER. Sensitivity is primarily determined by the RF front-end, while selectivity is determined by the channel select filtering. Selectivity is the relevant specification for this RF baseband processing application. This chapter will start with a review of receiver architectures, paying special attention to how they achieve selectivity. Then, the discussion will focus in more detail on both analog and digital schemes for performing channel selection on chip. Finally, the requirements a variety of RF specifications place on baseband channel select filtering will be discussed.

2.2 Receiver Architecture Overview

Figure 2.1 shows an idealized implementation of an integrated multi-standard capable RF transceiver. In this approach, the RF signal coming in at the antenna would be directly digitized by the A/D converter. Channel selection and all other processing would be handled in the digital domain by the DSP. This digital approach can be made multi-standard capable merely by programming the DSP. Unfortunately, an RF A/D converter is unrealizable; it would require 14 to 18 bit resolution and a sampling rate in the range of 900 MHz to 2.5 GHz depending on the carrier frequency.

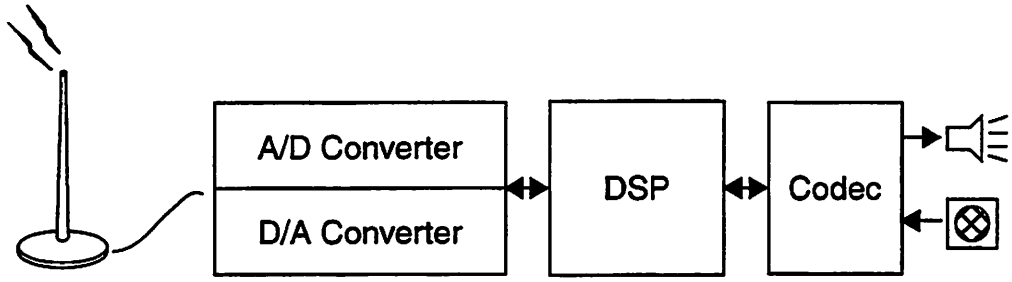

Fig. 2.1: Ideal integrated multi-standard RF transceiver block diagram.

Since an RF A/D converter is unrealizable, a practical transceiver will take the form of Fig. 2.2.The analog signal processing block will include frequency translation, amplification, and filtering. There are several basic forms this analog signal processing function in the receive path can take: superheterodyne, direct-conversion, low-IF, and wideband IF double-conversion. The discussion will focus on how these receiver architectures impact selectivity, integration, and multi-standard capability.

2.2.1 Superheterodyne Receiver

The superheterodyne shown in Fig. 2.3 is the conventional approach to RF receiver architecture. Recent examples of superheterodyne designs are described in

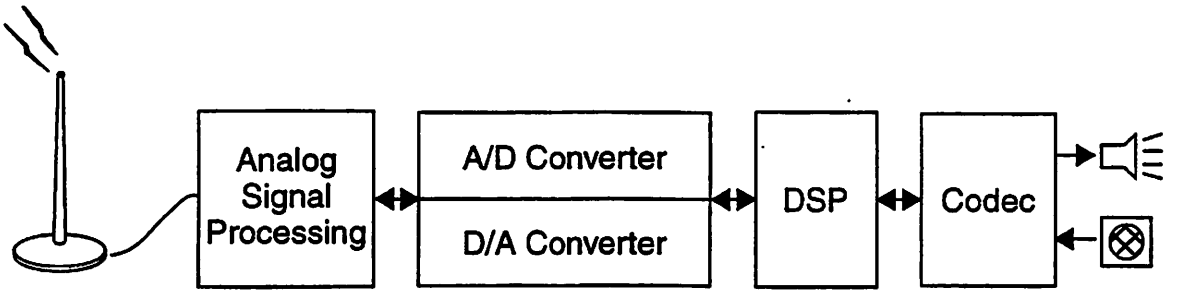

Fig. 2.2: Conceptual view of a practical RF transceiver.

[5],[6],[7],[8]. With high Q off-chip bandpass filters (shaded in Fig. 2.3), this conventional architecture is not amenable to a highly integrated solution. The off-chip filters also must be specific to a particular communications standard implying that this architecture cannot be made multi-standard capable. However, a description of the frequency planning and functionality of this receiver will illustrate some of the basic requirements of RF receivers in more detail.

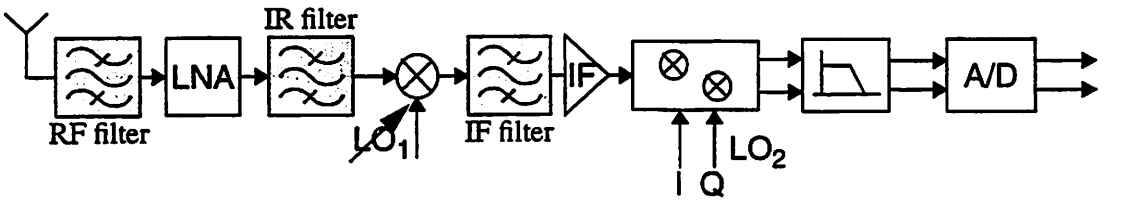

Fig. 2.3: Conventional superheterodyne receiver.

Consider the propagation of a desired signal through the receive path as shown in the frequency plan in Fig. 2.4 [9]. The RF spectrum at the antenna passes through an off-chip RF filter and is amplified by the low-noise amplifier (LNA). Amplification of the RF signal is required to achieve adequate sensitivity by reducing the noise contributions of later blocks in the receive path. After the LNA, the signal goes off-chip through the image-reject (IR) filter. The combination of the RF and IR filters rejects signals in the image band that must be attenuated prior to mixing. Otherwise, the signals in the image band will corrupt the desired signal by

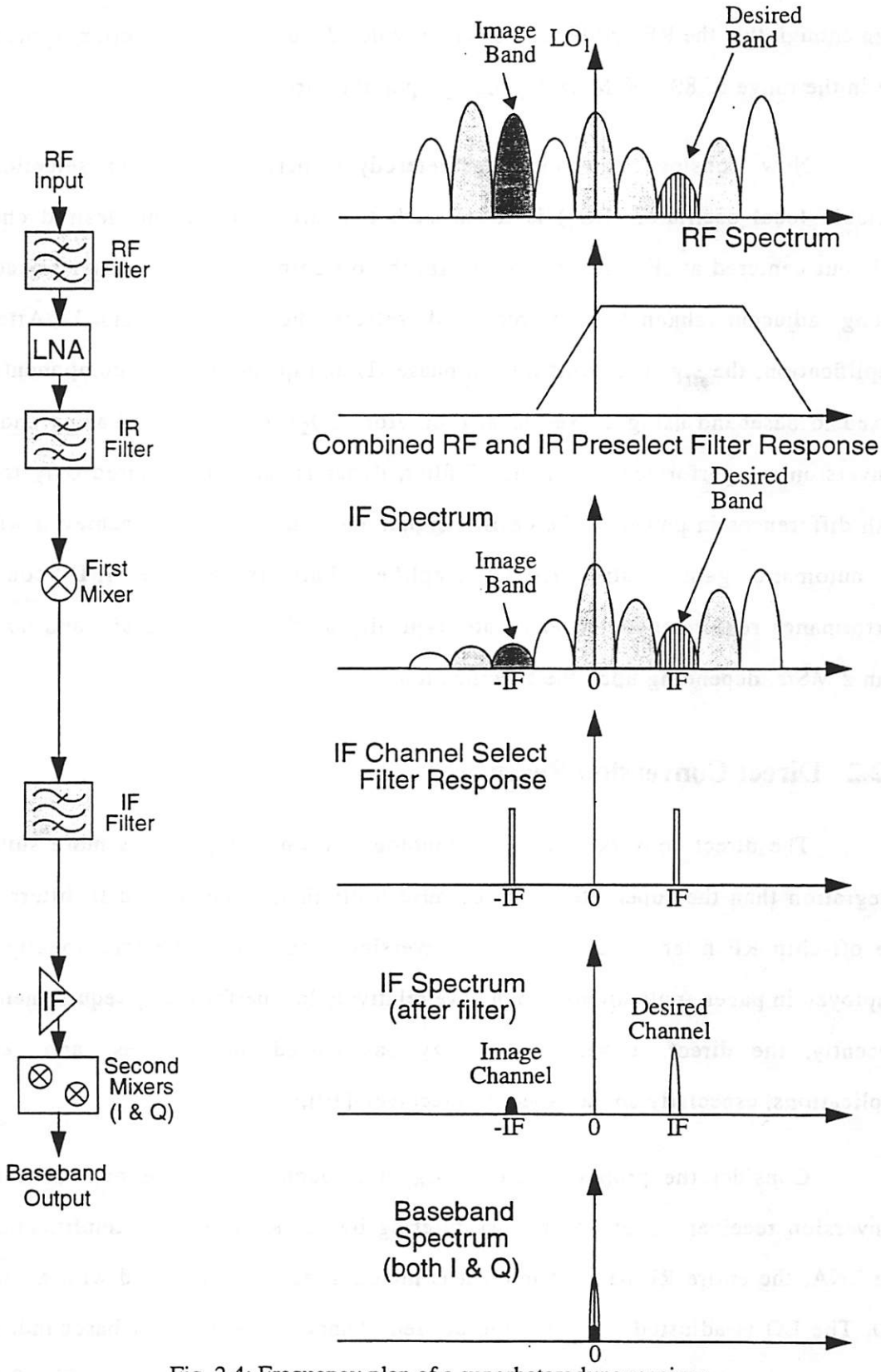

Fig. 2.4: Frequency plan of a superheterodyne receiver.

mixing into the same frequency band. Note that the intermediate frequency (IF) must be high enough that the RF and IR filters can provide adequate image rejection; typical IFs are in the range of 80-300 MHz depending upon the carrier frequency.

Now consider how the superheterodyne performs channel selection. A variable local oscillator (LO_1) is tuned such that after mixing the desired channel falls out centered at IF. After mixing to IF, the off-chip IF bandpass filter rejects the strong adjacent channel interferers and selects the desired channel. After IF amplification, the signal is split into in-phase (I) and quadrature (Q) components and mixed to baseband using a fixed local oscillator (LO_2). Finally, antialiasing and A/D conversion are performed. After the IF filter, dynamic range is required only to deal with differences in power of the desired signal and can therefore be achieved with an IF automatic gain control (AGC) amplifier. Furthermore, the A/D converter performance requirements are moderate: typically on the order of 8 bits and no more than 2 MS/s, depending upon the specification.

2.2.2 Direct Conversion Receiver

The direct conversion receiver topology shown in Fig. 2.5 is more suited to integration than the superheterodyne because it eliminates the IR and IF filters; only the off-chip RF filter remains. Direct conversion topologies have traditionally been employed in pager applications which have relatively low performance requirements[2]. Recently, the direct conversion topology has moved into cordless and cellular applications, especially spread-spectrum receivers[10],[11].

Consider the propagation of a signal through the receive path of a direct conversion receiver. After preliminary filtering by the RF filter and amplification by the LNA, the entire RF band of interest is mixed directly to baseband with a variable LO. The LO is adjusted such that the desired channel is centered at baseband. Since the mix is direct to baseband, there is no image component as shown in Fig. 2.6 [9].

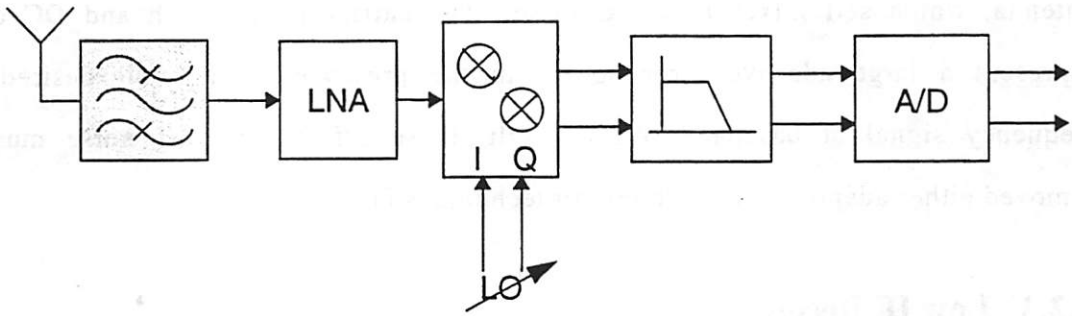

Fig. 2.5: Direct conversion receiver block diagram.

Finally, an on-chip low pass filter selects the desired channel and the result is digitized for further processing. Depending upon the partition between analog and digital, lowpass filtering and A/D dynamic range and bandwidth, the lowpass filter may be made programmable to satisfy multiple communications standards.

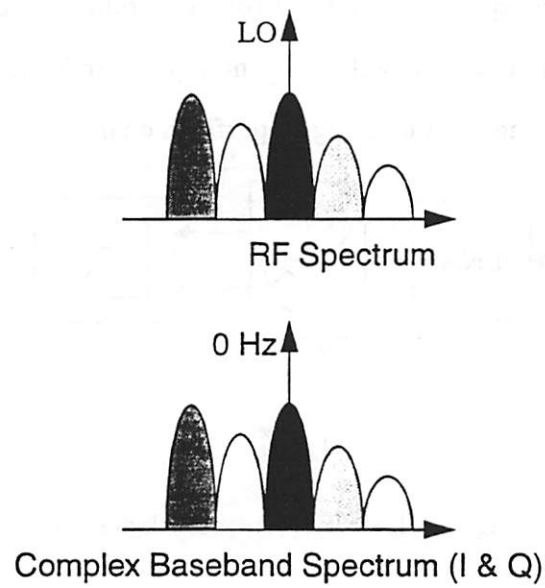

Fig. 2.6: Direct conversion frequency translation.

While the direct conversion approach is amenable to integration and can be made multi-standard capable, several system level problems need to be overcome. The DC offset and 1/f noise from the mixer and baseband processing circuits may be larger than the desired signal. Furthermore, there can be LO leakage back to the

antenna, which self mixes as a DC offset. The carrier feedthrough and DC offset represent a large additive error source in the presence of a small desired low frequency signal at baseband. As a result, these offsets and 1/f noise must be removed either adaptively or with circuit techniques [1].

2.2.3 Low IF Receiver

The low IF receiver shown in Fig. 2.7 mixes to a low enough IF that on chip bandpass filtering can be used to perform channel selection. This architecture eliminates the problems of DC offset and 1/f noise associated with direct conversion receivers while maintaining the same level of integration. However, the low IF receiver introduces a new problem: rejecting a nearby image component. Active image reject mixer techniques are required for this architecture to be utilized [12]. In many instances, this architecture will also employ a bandpass sigma-delta modulator and digital bandpass decimation filtering to perform channel selection[13].

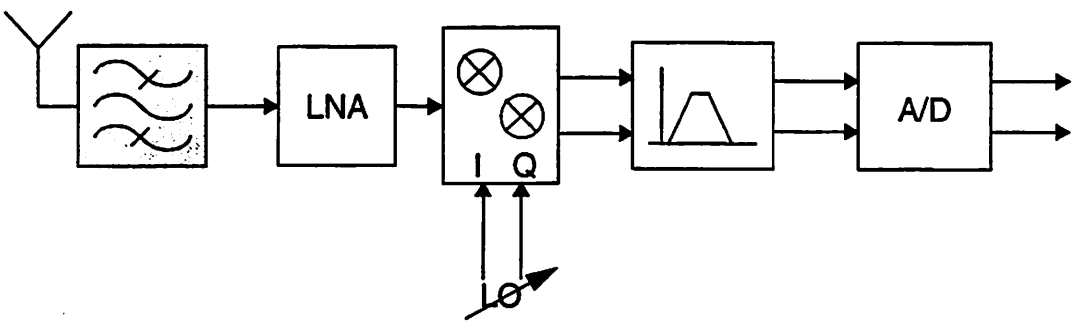

Fig. 2.7: Low IF receiver block diagram.

While low IF receivers can be integrated, the bandpass filtering is not suitable for standards like DECT, which have wide channel bandwidths. This occurs because a bandpass filter or sigma-delta modulator of a given specification requires twice the number of poles and zeros as compared to its lowpass counterpart; the power dissipation required to achieve this wide bandwidth becomes prohibitive even if it is possible to meet the performance requirements. As a result, low IF receivers can only

address a subset of communications standards and cannot be viewed as truly multi-standard capable.

2.2.4 Wideband IF Double-Conversion Receiver

The wideband IF double-conversion receiver shown in Fig. 2.8 is a combination of the superheterodyne and direct conversion receivers. The architecture employs a two-stage mix similar to the superheterodyne; however, the off-chip IF and IR filters are eliminated as in direct conversion. Thus, this architecture is suitable for integration [1],[14].

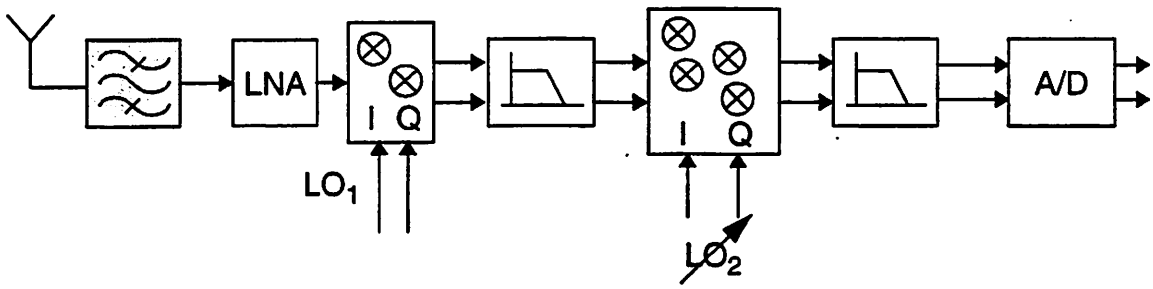

Fig. 2.8: Wideband IF double-conversion receiver.

Consider the propagation of a signal through the receive path in Fig. 2.8. An RF signal is filtered by an off-chip RF filter and amplified by the low-noise amplifier as in the superheterodyne case. Then, a fixed LO mixes the entire RF spectrum to IF, where a simple lowpass filter removes harmonics and high frequency noise. A variable LO mixes the entire spectrum to baseband, centering the desired channel at DC. The fixed high-frequency LO and variable low-frequency LO make it easier to meet phase noise requirements. As in a direct conversion receiver, channel select filtering is lowpass at baseband implying that this receiver can be made multi-standard capable. Since the IR filter is eliminated, this architecture requires active image reject mixers to suppress undesired signals in the image band. However, the DC offset problem of direct conversion receivers is eliminated by the two-stage mix [14].

2.3 Channel Select Filtering

Both the direct conversion and wideband IF double-conversion architectures are suitable for integration and can be made multi-standard capable because they perform lowpass channel select filtering on chip at baseband. This section focuses in detail on the baseband channel select filtering problem, including various methods to perform channel selection.

In order to achieve adequate selectivity, a RF receiver must select a weak desired channel in the presence of strong adjacent channel interferers as shown in Fig. 2.9. For baseband channel selection, a lowpass filter with adequate stopband rejection in the region of the strong adjacent channel interferers is required. In addition to filtering, an A/D converter is required so that bits can be recovered in the digital domain. As will be discussed in more detail below, the channel selection can be performed in the analog domain using either continuous-time or switched-capacitor filters or in the digital domain. While the filter requirements are the same for either the analog or digital methods, the choice of analog or digital selection impacts the dynamic range requirements of the A/D converter and the programmability of the receiver.

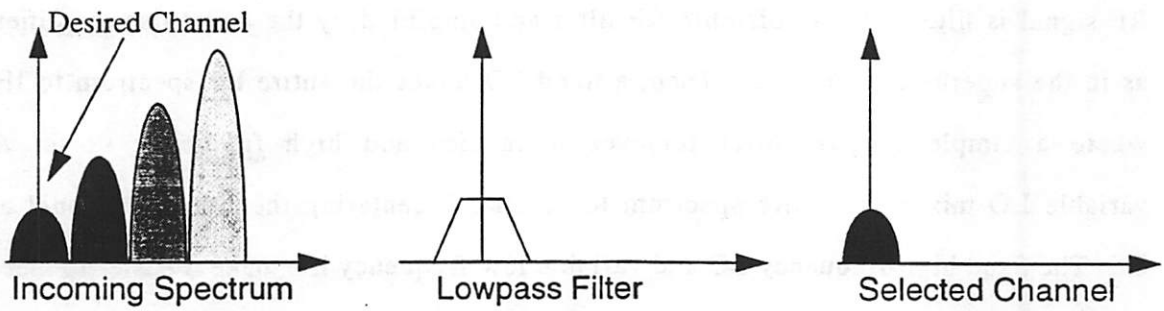

Fig. 2.9: The baseband channel select filtering problem.

An alternative (A/D converter design) view of the baseband channel selection process can be developed from antialiasing considerations. Irrespective of whether the channel selection is performed in the analog or digital domain, the

strong adjacent channel interferers must not be allowed to alias into the desired frequency band as part of the sampling process. This implies that either (1) an analog filter in front of the A/D converter must band-limit the incoming signal with enough stopband rejection to remove the strong adjacent channel interferers prior to sampling by the A/D converter, or (2) the A/D converter must oversample enough so that the adjacent channel interferers do not alias into the desired frequency band and can be removed by a subsequent digital filter. Thus, from the A/D converter design view, the channel selection process reduces to providing adequate antialiasing in either the analog or digital domain.

2.3.1 Analog

Channel selection can be performed in the analog domain with a lowpass filter prior to the A/D converter. This is illustrated with the generic analog baseband processing block consisting of a lowpass filter and A/D converter shown in Fig. 2.10. The analog filter must have enough dynamic range and linearity to select the desired channel in the presence of strong adjacent channel interferers. Since all channel select filtering is performed prior to the A/D, only a low resolution A/D converter (typically 8 bits or less) with enough bandwidth to digitize the desired channel is required.

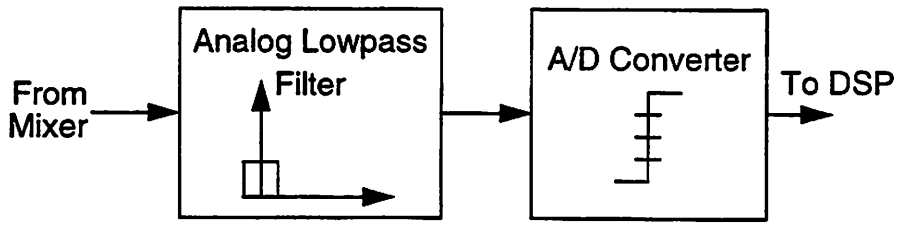

Fig. 2.10: Baseband processing with analog channel select filtering.

One implementation of the baseband processing block in Fig. 2.10 would employ a continuous time lowpass analog filter in front of the A/D converter[7],[15],[16],[17]. This would be the typical approach in a bipolar or BiCMOS technology using transconductance-C filters. Continuous-time channel select filtering

has also been implemented in CMOS [17]. This particular filter is implemented as an active RC filter. One key issue in the design of continuous-time filters is compensating for component variations since the filter frequency response depends on the absolute value of capacitors and conductances; this usually requires some form of on-chip tuning circuitry. In addition, linearity is a key design requirement as the strong adjacent channel interferers set the out-of-band third-order intercept point. Linearity considerations dictate the signal-handling capability of the first integrator in the filter.

The channel select filtering can be performed using analog CMOS switched-capacitor filters as shown in Fig. 2.11 [18],[19],[20]. Following a relatively simple continuous-time antialias filter, the switched-capacitor filter samples the input signal and rejects the adjacent channels. One advantage of this approach is that the continuous-time antialias filter does not require precision pole locations; tuning is not required. The poles in the switched-capacitor filter depend solely on the sampling frequency and capacitor ratios which are well controlled in CMOS technology. Furthermore, switched-capacitor filters exhibit good linearity.

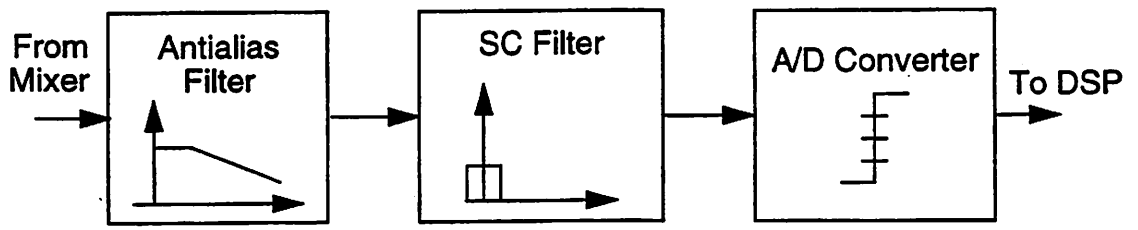

Fig. 2.11: Baseband channel selection with an analog switched-capacitor filter.

To further illustrate channel selection using a switched-capacitor filter, a sample frequency plan for such a filter is shown in Fig. 2.12 [21]. This filter implements channel selection for the DECT standard. The filter consists of a second-order Sallen-Key stage with a 1.5 MHz bandwidth to perform antialiasing. Voltage gain of 6 dB in the Sallen-Key helps attenuate the noise contribution of the switched-capacitor filter thereby improving receiver sensitivity. The switched-capacitor filter

consists of a cascade of four biquads sampling at 31.1 MS/s: a sixth order lowpass filter with 700 kHz bandwidth followed by a second order allpass filter to maintain constant group delay. The filter also includes 42 dB of programmable gain to improve dynamic range. A 10 bit pipelined ADC operating at 10.3 MS/s digitizes the filtered result.

2.3.2 Digital

Channel selection can be performed in the digital domain using an oversampled sigma-delta modulator followed by a digital decimation filter as shown in Fig. 2.13. The continuous time antialias filter in front provides adequate rejection about the sampling rate of the sigma-delta modulator. For system level purposes, a sigma-delta modulator can be considered as an A/D converter which samples at a rate M times larger than required by aliasing considerations. The modulator has the additional property that its quantization noise is shaped with a highpass transfer function into the frequency region above the baseband where the desired signal lies. The strong adjacent channel interferers fall into the same band as the quantization noise. This allows the same digital lowpass filter to remove both the quantization noise and adjacent channel interferers. Since this digital filter reduces the sample rate from the oversampled rate to Nyquist rate, it is referred to as a decimation filter.

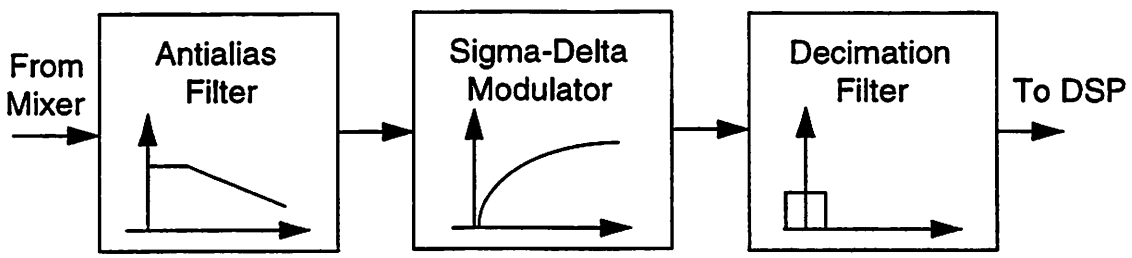

Fig. 2.13: Baseband channel selection with a sigma-delta modulator and digital filter

To further illustrate digital channel selection, the frequency planning for the sigma-delta modulator and decimation filter is shown in Fig. 2.14 for the DECT case.

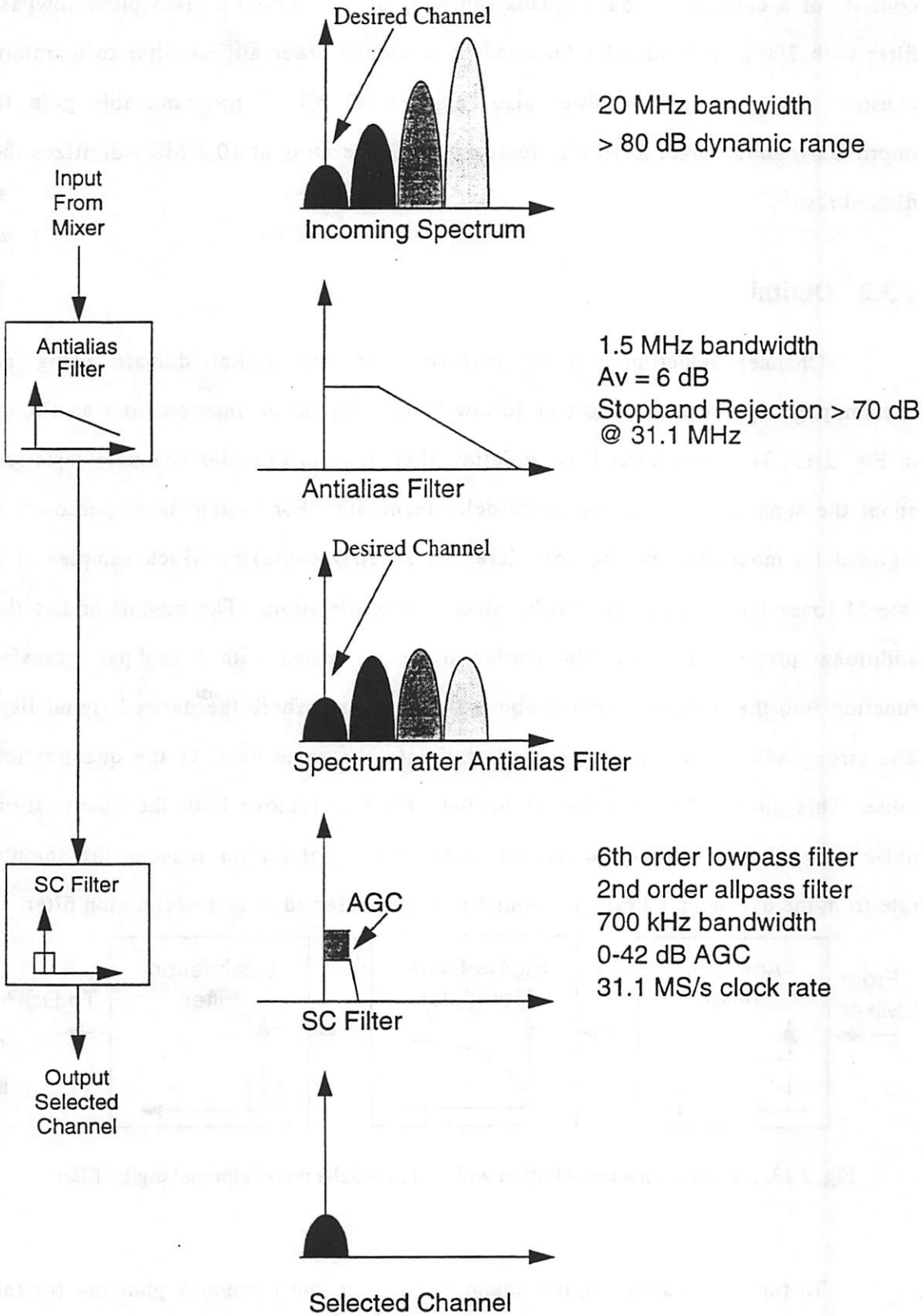

Fig. 2.12: Frequency planning for a switched-capacitor channel select filter

Note that the continuous time antialiasing filter has basically the same characteristics as in the analog case although it requires a slightly sharper roll-off. The sigma-delta modulator needs to achieve more than 80 dB of dynamic range in an 800 kHz baseband. It samples at 25.6 MS/s at 16 X oversampling ratio. After the sigma-delta modulator, the lowpass digital decimation filter rejects the quantization noise and adjacent channel interferers with a 700 kHz passband and transition bandwidth from 700 to 800 kHz. After decimation, the results are sent for further digital signal processing.

2.3.3 Mixed-Signal

Digital communication receivers are inherently mixed-signal systems. As a result channel select filtering may be partitioned between the analog and digital domains as shown in Fig. 2.15. From a power dissipation and area perspective, some combination of analog and digital filtering will be optimal for a communications standard which requires a given dynamic range and bandwidth in the baseband processing circuitry[22]. In a practical receiver employing analog channel selection as shown in Fig. 2.10, it is likely that some form of subsequent digital filtering after the A/D converter will be performed to achieve a sharper cutoff lowpass filter. Similarly, the digital channel selection scheme in Fig. 2.13 is actually a mixed-signal scheme with the antialias filter serving as an analog lowpass filter. As a result, all practical channel select schemes are actually mixed-signal. However, to maintain clarity in the discussion, channel select filtering which is predominantly analog will be referred to as analog channel selection and channel select filtering which is predominantly digital will be referred to as digital channel selection. Mixed-signal channel selection will refer to schemes which divide the filtering requirements close to equally between the analog and digital domains.

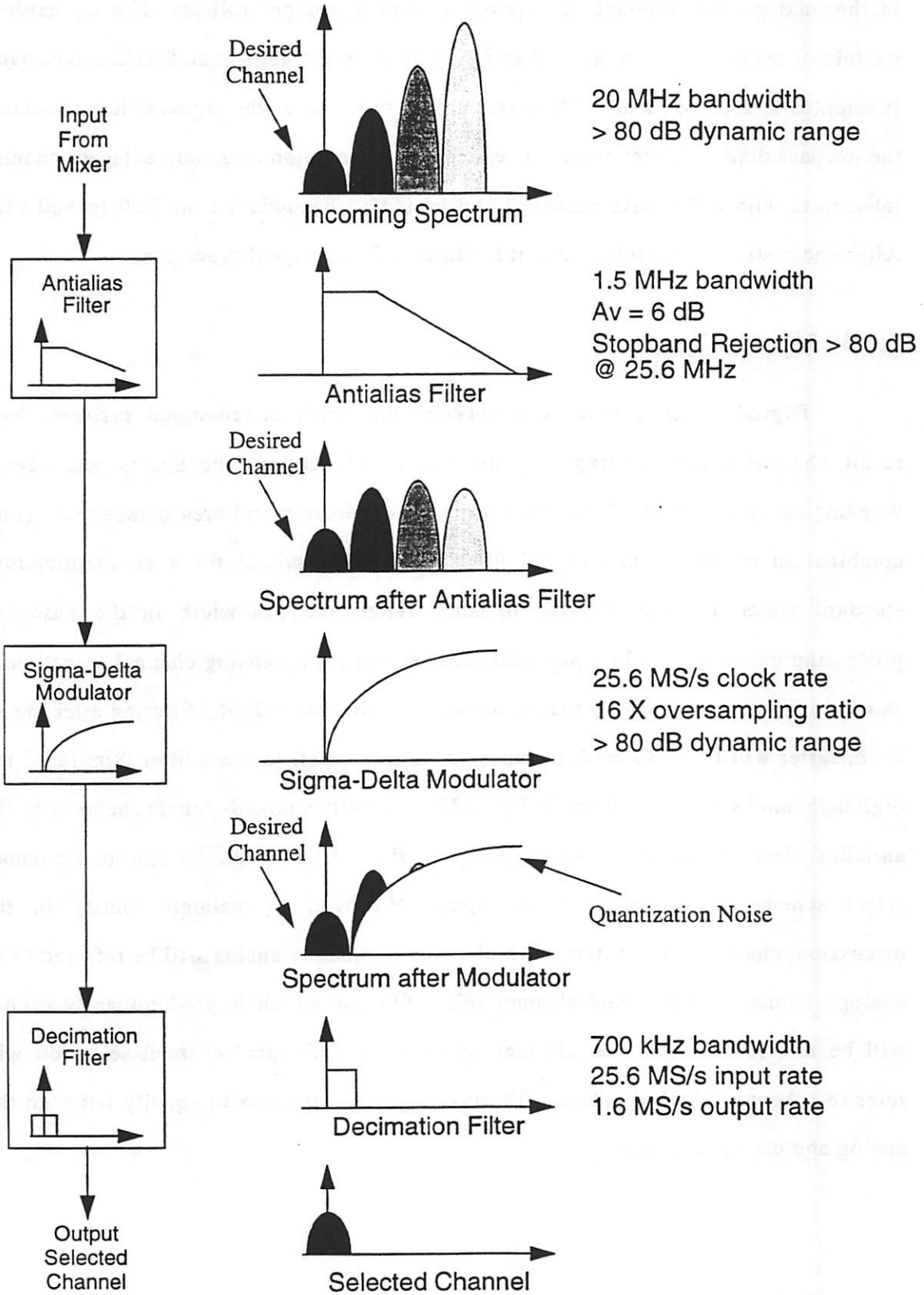

Fig. 2.14: Frequency planning for a digital channel select filter

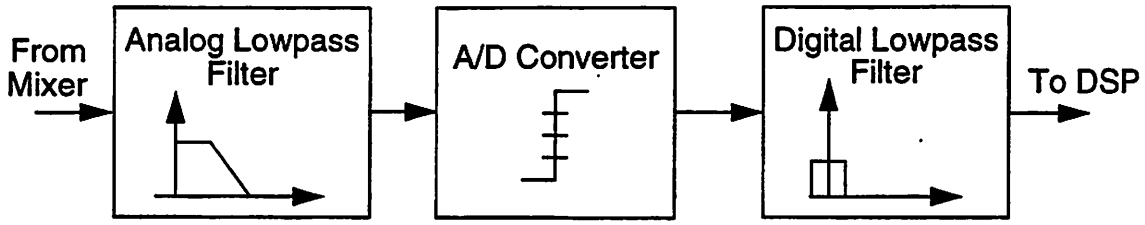

Fig. 2.15: Baseband processing with mixed-signal channel select filtering.

2.3.4 System-Level Tradeoffs

The various tradeoffs among analog, digital and mixed-signal channel select filtering schemes at the system level are of key concern to the designer. Such tradeoffs include the bandwidth and dynamic range requirements of the A/D converter, AGC requirements, programmability, power dissipation and circuit area. Any discussion of these tradeoffs at the system level is qualitative by nature since metrics such as power dissipation and area can vary widely depending on the choice of architecture and circuit techniques.

For direct conversion and wideband IF double-conversion receivers, the overall requirements on the baseband processing circuits are set by the RF specifications. As will be described in Section 2.4, the various RF specifications give the channel bandwidth, number of channels, worst case signal power, relative strengths of adjacent channel interferers and required SNR. Since the entire RF spectrum is mixed to baseband in these receivers, the signal at the input to the baseband processing block will have its dynamic range and bandwidth requirements set by the RF specifications. As a result, the design space is constrained to be fixed dynamic range and bandwidth independent of choice of channel select filtering scheme.

Consider the dynamic range and speed requirements of the A/D converter for analog, digital and mixed-signal channel select filtering. In the analog case, filtering prior to the A/D converter eliminates the adjacent channel interferers. As a

result, the required A/D converter resolution is moderate ranging from 4 bits for CDMA systems to a maximum of about 10 bits [17], [19]. This resolution depends on the modulation scheme which sets the required SNR at the slicer for a given BER and the amount of AGC in front of the A/D converter. For analog filtering, the A/D converter must satisfy the Nyquist criterion, sampling at twice the channel bandwidth. In practice, the A/D converter must oversample by at least 2 X to perform timing recovery [23]. For digital channel select filtering, the A/D converter resolution is set by the RF blocking and noise requirements which can be as high as 14 to 16 bits [3],[4]. Since the A/D converter will typically be a sigma-delta modulator, its bandwidth is only twice the desired channel bandwidth; the interferers fall into the same band as the quantization noise as described previously. Since the A/D converter is already oversampling, timing recovery can be performed without an additional speed increase. For mixed-signal channel select filtering, the ADC resolution requirements fall somewhere between the analog and digital cases.

Automatic gain control (AGC) amplifiers may be used to increase the dynamic range of the baseband processing in certain cases. The power received at the antenna in the desired channel can vary widely depending on the distance from the base station and channel characteristics such as multipath fading [24]. If only the desired channel were present, the dynamic range requirements are set by this power variation. This implies that a feedback (AGC) loop based on the received signal power can be used to vary the gain in the receive path to meet the dynamic range specification. Note that if the interfering channels are present AGC amplifiers will not improve the dynamic range because both the desired and undesired channels will be amplified by the same amount.

Consider the use of AGC amplifiers in the various channel select filtering schemes. In the analog case, analog AGC amplifiers are usually combined with the filtering to ease the requirements on the A/D converter. Typical values of gain

control range are from 42 dB to 70 dB depending on the application and choice of A/D converter [10],[19]. Analog AGC amplifiers cannot be used in the digital channel select filtering case because the interferers are removed after A/D conversion. As a result, the overall system design in the digital case will be simpler than in the analog case due to the elimination of the AGC loop, especially the requirement of generating the feedback signals to update the gain.

Programmable channel select filtering is required to make a RF receiver multi-standard capable. As will be discussed in Section 2.4, the RF specifications are set up so that higher dynamic range is required for narrower bandwidth specifications and lower dynamic range is required for wider bandwidth specifications. As a result, programmable baseband processing should be able to trade off bandwidth and dynamic range. Unfortunately, there is no obvious way to perform this tradeoff when analog channel select filtering is employed; the approach to programmability in a switched-capacitor filter will be to meet the worst case dynamic range and change the clock frequency to change the bandwidth. Since power dissipation increases with dynamic range and bandwidth, this will yield a suboptimal solution. Digital channel select filtering can be made easily programmable merely by changing the filter coefficients in the decimation filter; a good example of this approach for audio rate applications is described in [25]. However, the dynamic range of the A/D converter must also be made programmable to fit the RF specification. Fortunately, as will be described in Chapter 3, sigma-delta modulators allow the designer to trade off bandwidth and dynamic range which makes them uniquely suited to performing the A/D conversion function in a multi-standard capable RF transceiver. Thus, programmability is a clear advantage of the digital channel select filtering approach.

Power and area tradeoffs between analog (switched-capacitor) and digital implementations of signal processing functions were examined in detail by Nishimura [22]. His results shown in Fig. 2.16 are applicable for the case of RF

baseband processing applications. In all cases, the dynamic range and bandwidths are such that both analog and digital solutions are possible. Wideband RF specifications such as DECT [3] with dynamic range requirements of 13 to 14 bits and bandwidths on the order of 1 MHz fall into the area-power equivalency zone defined by Nishimura. Narrowband RF specifications such as GSM [4] with bandwidths on the order of 100 to 200 kHz and dynamic range on the order of 15-16 bits favor digital solutions. While Nishimura's results show the general power and area trends, both power and area are greatly impacted by implementation details such as A/D and filter architectures, circuit techniques and fabrication process.

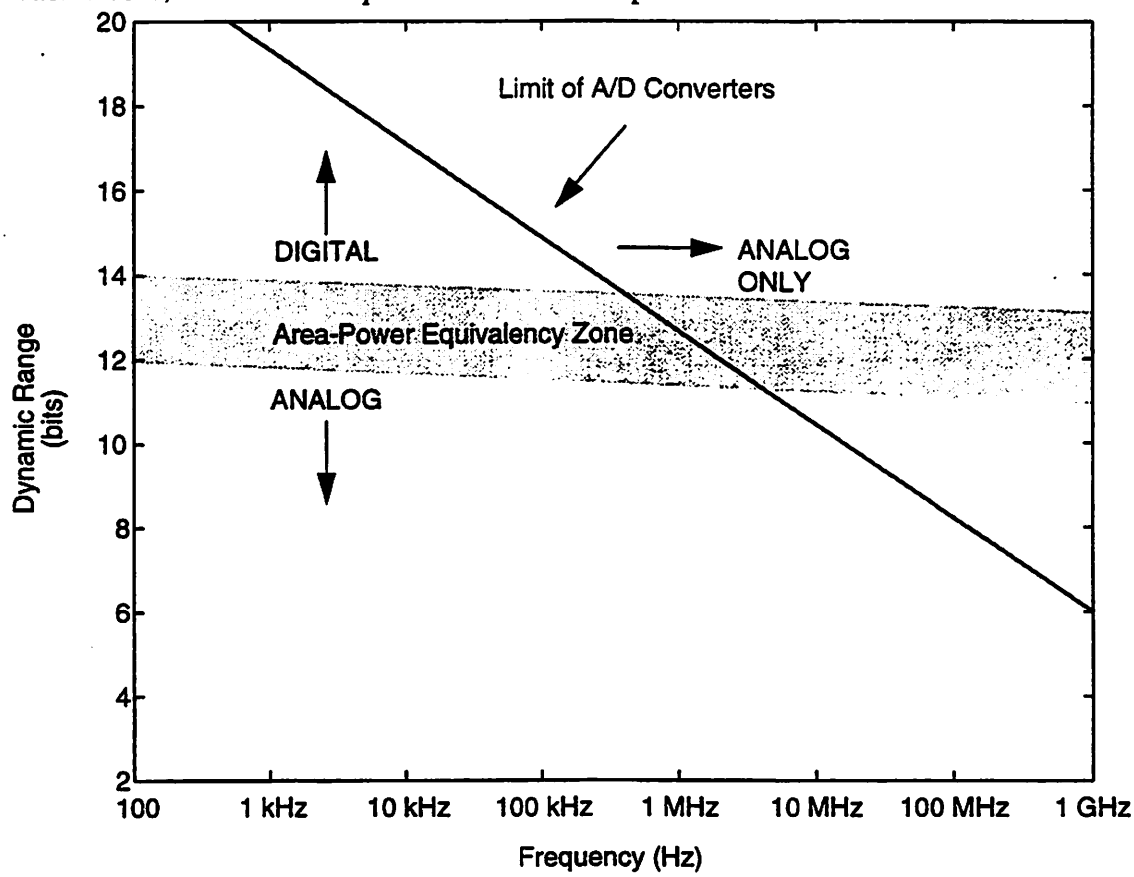

Fig. 2.16: Preferred areas of operation for analog and digital signal processors

The above discussion of system level tradeoffs suggests that both analog an digital approaches are suitable for integrated baseband channel select filtering. Analog approaches will relax the A/D converter requirements while digital

approaches eliminate AGC loops. Power and area are likely to be comparable for analog and digital approaches for wideband specifications while narrowband specifications favor digital approaches. However, multi-standard capability requires programmability in the baseband channel select filtering and programmability is the clear advantage of a more digital solution.

2.4 Requirements

This section seeks to summarize the requirements a variety of RF specifications place on the baseband processing circuitry. Examining these requirements is important to understanding the appropriate way to make the system level tradeoffs between analog and digital processing described in the previous section. These requirements are especially important in understanding how to implement multi-standard capable baseband processing systems. The specifications discussed include dynamic range, bandwidth, antialiasing, and distortion considerations. RF specifications to be covered include: DECT, GSM (900 MHz), PCS-1900, and 802.11. The results summarized come from the specifications themselves as well as from several implementations and secondary sources [3], [4], [26], [27], [28], [29]. The calculations serve as an example of how to specify dynamic range and linearity requirements of a baseband circuit given an RF specification. Under different assumptions about gain and baseband contributions to overall receiver noise and distortion, the requirements placed on baseband processing circuits in actual implementations will differ.

Dynamic range is the difference in power between the maximum signal level that must be handled and the noise floor. Since no channel select filtering is performed prior to the baseband in integrated receivers, the maximum signal level is set primarily by blocking requirements. Typically, a LNA bypass mode will be provided in the case of a large desired signal. The noise floor is set by the system

reference sensitivity (minimum desired signal level) and the SNR (E_b/N_o) required at the slicer to detect a signal at acceptable BER. An additional constraint is that the baseband processing must have minimal impact on the overall receiver noise figure. Finally, extra dynamic range must allocated to provide adequate margins for variations in the gain of the RF front-end due to process. Table 2.1 summarizes the results with a sample calculation for DECT shown in Appendix 1.

Table 2.1: Dynamic Range Requirements

	DECT	GSM	PCS-1900	802.11
Reference Sensitivity	-83 dBm	-102 dBm	-102 dBm	-80 dBm
Worst Case Blocker	-33 dBm	-23 dBm	-26 dBm	-20 dBm
SNR (E_b/N_o)	14.6 dB	11 dB	11 dB	19 dB
Bandwidth (Bit Rate)	1.152 MHz	200 kHz	200 kHz	1 MHz
Input Noise Power	-113.2 dBm	-120.8 dBm	-120.8 dBm	-113.8 dBm
Noise Figure	15.6 dB	7.8 dB	7.8 dB	14.8 dB
Baseband Dynamic Range	85 dB	110 dB	107 dB	89 dB

The bandwidth requirements on the baseband processing are set by the channel spacing and the modulation scheme which determines how much of that bandwidth is occupied by information. The bandwidth specifications summarized in Table 2.2 assume that the signal has been split into I and Q components and mixed directly to baseband. Additionally, there are a number of available RF channels; this sets the total RF bandwidth which is simply the number of channels multiplied by the channel spacing. Since integrated receivers mix the entire RF band to baseband, the total RF bandwidth will impact antialiasing requirements. The RF filter at the front-end of the receiver must allow the entire RF bandwidth to pass through to baseband. As a result, blockers at or above the sampling frequency of either the

sigma-delta modulator, switched-capacitor filter or ADC depending upon the choice of channel select filter must be rejected by a continuous time antialiasing filter.

Table 2.2: Bandwidth Requirements

	DECT	GSM	PCS-1900	802.11
Channel Spacing	1.728 MHz	200 kHz	200 kHz	1 MHz
Filter Bandwidth	700 kHz	100 kHz	100 kHz	500 kHz
Total RF Bandwidth	20 MHz	25 MHz	60 MHz	80 MHz

Linearity is an important specification of a RF receiver because third-order intermodulation of the large adjacent channel blockers will fall into the same frequency band as the desired signal. Third-order distortion is usually specified in terms of the out-of-band input referred third-order intercept point IIP_3. IIP_3 as shown in Fig. 2.17 is the input power level in dBm where the third-order intermodulation distortion (IM_3) line crosses the out-of-band input line. The RF requirements specify power levels for the out-of band signals and desired signal. From these requirements, IIP_3 can be calculated for the overall receiver. Similar to the noise requirements, the baseband processing must not significantly degrade the overall receiver IIP_3. Results for the various specifications are summarized in Table 2.3 with a sample calculation for DECT shown in Appendix 1.

Table 2.3: Linearity Requirements

	DECT	GSM	PCS-1900	802.11
Desired Signal Power	-80 dBm	-99 dBm	-99 dBm	-79 dBm
Blocker Power	-46 dBm	-49 dBm	-49 dBm	-34 dBm
Receiver IIP_3	-16.7 dBm	-13.5 dBm	-13.5 dBm	3 dBm
Gain	41 dB	34 dB	37 dB	28 dB
Baseband IIP_3	31.1 dBm	27.4 dBm	30.4 dBm	37.9 dBm

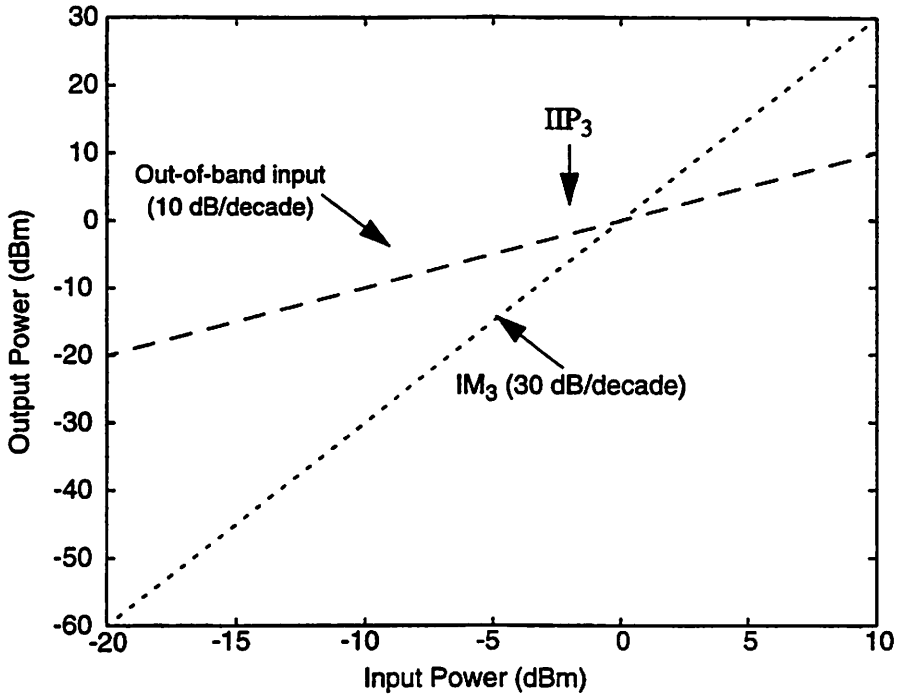

Fig. 2.17: Out-of-band IIP_3 definition

2.5 Summary

This chapter sought provide an overview of RF receiver architectures with an emphasis on integration and multi-standard capability. Direct-conversion and wideband IF double conversion architectures are suitable for highly integrated, multi-standard capable solutions because they perform channel select filtering on-chip at baseband. Next, channel select filtering in both the digital and the analog domains was discussed. It was shown that digital channel select filtering utilizing a sigma-delta modulator and decimation filter achieves a more programmable solution than an analog approach thereby allowing for multi-standard capable receivers. Finally, a variety of RF specifications were discussed in the context of the dynamic range, bandwidth, and linearity requirements placed on the baseband processing circuits.

Chapter 3
Sigma-Delta Modulator Fundamentals

3.1 Introduction

This chapter reviews some of the fundamental issues in the design of sigma-delta modulators. The discussion begins with a variety metrics used to evaluate modulator performance with emphasis on those which are important for RF applications. Then, the basic concept of how a sigma-delta modulator works is described, and the basic linearized models are reviewed and related to performance issues. Following this basic introduction, tradeoffs among a variety of sigma-delta architectures suitable for high-speed applications are explored. Finally, the fundamental power limits for sigma-delta modulators implemented using switched-capacitor circuits are derived.

3.2 Performance Metrics

This section defines the metrics used to evaluate sigma-delta modulator performance. For the RF application described in Chapter 2, the key requirements for a sigma-delta modulator are dynamic range, out-of-band input referred third-order

intercept point, Nyquist rate and power dissipation. In addition, sigma-delta designers usually specify peak SNR (signal-to-noise ratio) and peak SNDR (signal-to-noise-and-distortion ratio), which measure the degradation of the signal due to noise alone, and due to a combination of noise and distortion, respectively.

3.2.1 Peak SNR/SNDR and Dynamic Range

Peak SNR, SNDR and dynamic range are related specifications and will be defined together. Dynamic range is the ratio in power between the maximum input signal level that the modulator can handle and the minimum detectable input signal. SNR is the ratio of the signal power at the output of the modulator to the noise power. SNR includes all noise sources in the modulator, both thermal and quantization. SNDR is the ratio of the signal power at the output of the modulator to the sum of the noise and harmonic distortion powers. Peak SNDR is a useful metric for evaluating the capability of a sigma-delta modulator for handing large in band signals at acceptable linearity and is especially important for applications such as digital audio. Note that peak SNDR is frequency dependent and can be used to measure the degradation of modulator performance as the input signal increases in frequency.

Peak SNR, SNDR and dynamic range are typically reported using the type of plot shown in Fig. 3.1. The plot shows SNR and SNDR as a function of input signal power in dB relative to the full scale of the modulator. For small signal levels, distortion is not important implying that the SNR and SNDR are approximately equal. As the signal level increases, distortion degrades the modulator performance, and the SNDR will be less than the SNR. Dynamic range on the plot is the difference between the input level where the SNDR drops 3 dB beyond the peak and the x-intercept of the SNDR curve.

A closely related specification to dynamic range is the resolution of the modulator expressed in bits. The resolution in bits (N) is defined in (Eq 3-1) where DR

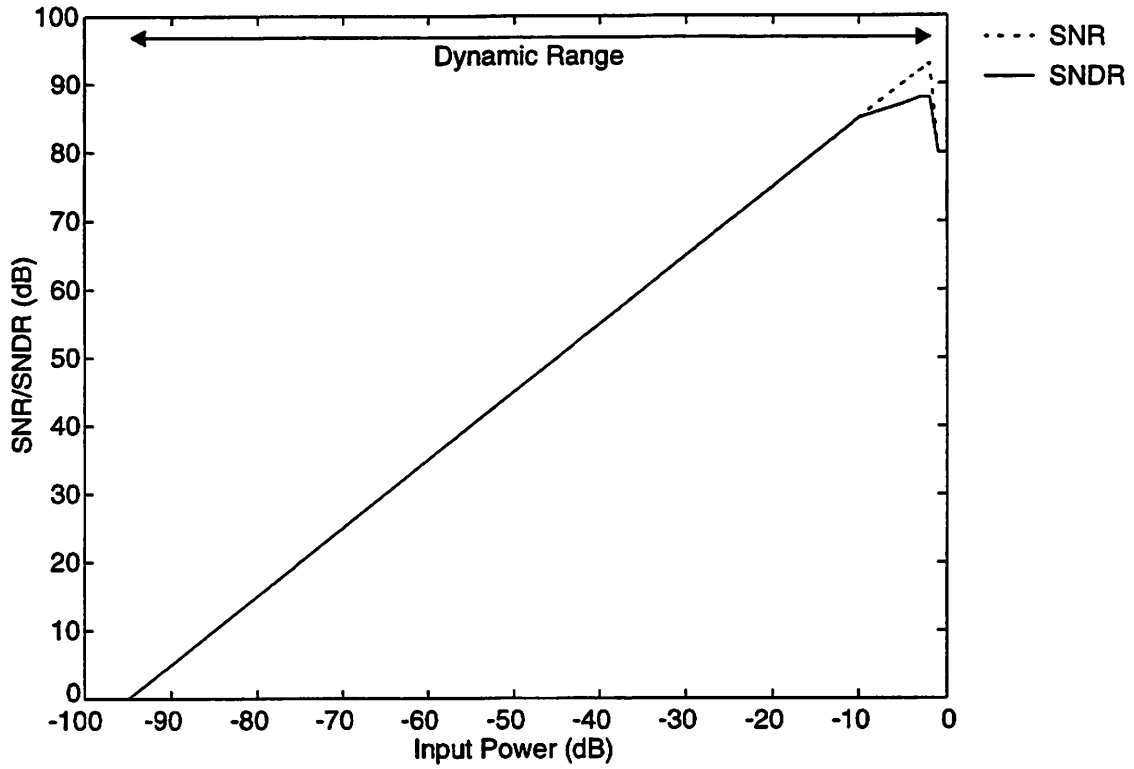

Fig. 3.1: SNR and SNDR curves

is the dynamic range of the modulator expressed in dB. The correspondence is such that each bit of resolution is equivalent to 6 dB of dynamic range.

$$N = \frac{DR - 2}{6} \qquad \text{(Eq 3-1)}$$

3.2.2 Nyquist Rate

The Nyquist rate is a measure of the speed of a sigma-delta modulator. The Nyquist sampling theorem states that to avoid aliasing, a lowpass signal must be sampled at a rate that is twice its bandwidth. As a result, specifying the Nyquist rate is equivalent to specifying the modulator input bandwidth.

3.2.3 Power Dissipation

Power dissipation is the key design constraint for battery operated applications such as RF receivers. The designer must meet the other performance constraints such as dynamic range, Nyquist rate and linearity while minimizing power dissipation. Power dissipation will be discussed in further detail in Section 3.5 and Chapter 4.

3.3 Basic Concepts

The forward path of a sigma-delta modulator consists of a series of integrators, and a quantizer in a feedback loop as shown in Fig. 3.2. Each integrator input is the difference between the previous integrator output and the D/A converter output. The effect of the feedback loop is to bring the average value at the first integrator input to zero. This implies that the output of the D/A converter is on average equal to the input signal X(z). Since the output of the D/A converter is merely an analog representation of the digital output Y(z) of the quantizer, it follows that Y(z) is on average equal to X(z). If the modulator samples the input signal at a higher rate than required by the Nyquist sampling criterion and multiple samples are averaged to produce a digital output Y(z), the sigma-delta modulator can then be used as an oversampled A/D converter.

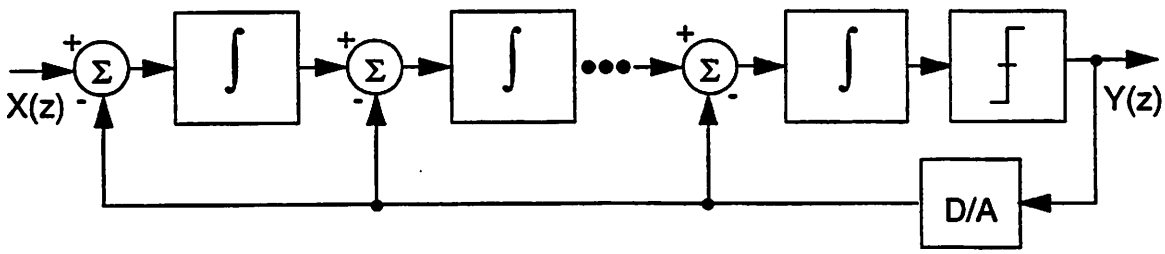

Fig. 3.2: Sigma-delta modulator block diagram

To describe the functionality of a sigma-delta modulator in greater detail, it is first necessary to define a few terms. The order (L) of a sigma-delta modulator is the number of integrators in the forward path. The oversampling ratio (M) is defined as the ratio of the modulator sampling rate to its Nyquist rate. The quantizer and D/A converter provide B bits of resolution.

Suppose that each integrator has the transfer function shown in (Eq 3-2), the quantizer can be modeled as an additive error source E(z) and that errors in the D/A converter can be modeled as an additive error source $E_{DAC}(z)$. Then, a linearized

$$I(z) = \frac{az^{-1}}{1-z^{-1}} \qquad \text{(Eq 3-2)}$$

transfer function of an Lth order sigma-delta modulator neglecting delays can be expressed as in (Eq 3-3), where G is the overall gain in the forward path from the input to the quantizer [30].

$$Y(z) = X(z) + \frac{(1-z^{-1})^L}{G} E(z) - E_{DAC}(z) \qquad \text{(Eq 3-3)}$$

(Eq 3-3) indicates that errors in the D/A converter add directly at the input of the sigma-delta loop. This implies that the D/A converter must be linear to the full resolution of the sigma-delta modulator to avoid degrading the overall modulator performance. One way to ensure that this linearity constraint is met is to use a single bit quantizer and two-level D/A converter. A two-level D/A converter is inherently linear; it can only result in a DC offset at the input of the modulator [30]. Multi-bit D/A converters require some kind of calibration to meet this linearity constraint [31].

Consider the overall quantization noise power in the baseband ($-f_b$, f_b) which can be found by integrating the quantization error term in (Eq 3-3) evaluated on

the unit circle[30]. Note that the oversampling ratio (M) in (Eq 3-4) will be $f_s/(2f_b)$

$$S_{qe} \approx \frac{\sigma_e^2}{f_s}\int_{-f_b}^{f_b}\left|\frac{(1-e^{-j2\pi f/f_s})}{G}\right|^2 df \approx \frac{\sigma_e^2}{G^2}\frac{\pi^{2L}}{2L+1}\frac{1}{M^{2L+1}} \qquad \text{(Eq 3-4)}$$

because f_b is the signal bandwidth not the Nyquist rate.

σ_e^2 in (Eq 3-4) is the variance of the quantization error which must now be calculated. Consider a quantizer that can be modeled by a linear input range $\left(-\frac{\Delta}{2},\frac{\Delta}{2}\right)$ and B bits of resolution. It follows that one least significant bit (LSB) will have the value in (Eq 3-5). Assume that the quantization error can be modeled as white and

$$\delta = \frac{\Delta}{2^B - 1} \qquad \text{(Eq 3-5)}$$

uniformly distributed between $[-\frac{\delta}{2},\frac{\delta}{2}]$. Then it follows from a statistical analysis that the quantization noise power can be expressed as in (Eq 3-6) [30].

$$\sigma_e^2 = \frac{\delta^2}{12} \qquad \text{(Eq 3-6)}$$

It is now possible to combine the results of (Eq 3-4), (Eq 3-5), and (Eq 3-6) to calculate the dynamic range of a sigma-delta modulator. Dynamic range is the ratio in power of a full scale sinusoidal signal ($\Delta^2/8$) to the power of the signal that yields a SNR of 0 dB. This results in the following expression for the dynamic range (DR) of sigma-delta modulator:

$$DR = \frac{3}{2}\frac{2L+1}{\pi^{2L}}G^2M^{2L+1}(2^B-1)^2 \qquad \text{(Eq 3-7)}$$

The dynamic range of a sigma-delta modulator is a strong function of the oversampling ratio and order of the loop. This implies that the designer can tradeoff between order and oversampling ratio to meet a given dynamic range requirement.

As described above, single bit quantizers and D/A converters are preferable from the standpoint that they are inherently linear. However, the modeling behind the statistical analysis of the quantization error which results in (Eq 3-7) is not particularly accurate for single bit quantizers. As a result, (Eq 3-7) should be viewed as an upper bound on the dynamic range.

The discussion has so far neglected stability issues. Modulators of order (L > 2) are only conditionally stable [31]. Stabilizing a higher-order loop requires the use of more complicated transfer functions than just a cascade of integrators in the forward path of the modulator and possibly the use of circuits that reset the state variables in the integrators when instability is detected. Unfortunately, the methods required to stabilize a higher-order loop reduce the modulator dynamic range well below the upper bound in (Eq 3-7).

3.4 Architecture Tradeoffs

This section explores architecture issues related to the implementation of high-speed sigma-delta modulators. Traditional sigma-delta modulators have operated at relatively low speeds for audio applications, with Nyquist rates on the order of 40 kS/s. At such rates, highly oversampled solutions, from 64 X to 256 X tend to be most attractive. However, at higher speeds with Nyquist rates above 1 MS/s, highly oversampled solutions cannot be implemented in current integrated circuit technologies. As a result, the sigma-delta architect must come up with solutions that can meet a dynamic range requirement at oversampling ratios of 32 X or less. Given the tradeoff between oversampling ratio and order in (Eq 3-7), this suggests that higher-order architectures and possibly multi-bit DACs will be required.

Sigma-delta architectures may be classified as either single-loop, which use one A/D converter and D/A converter along with a series of integrators, or multi-stage

(MASH), which consist of a cascade of single-loop sigma-delta modulators. Both single-loop and cascade architectures may employ either single bit or multi-bit A/D and D/A converters. This section reviews various single-loop architectures. Then, cascade architectures are discussed, followed by a comparison of cascade and single-loop architectures for high-speed applications.

3.4.1 Single Loop

The second-order sigma-delta modulator shown in Fig. 3.3 is widely used because it is simple to implement and insensitive to component mismatch [32]. The modulator consists of two integrators with transfer functions as in (Eq 3-2) (a=0.5 for the case in [32]) and a single bit A/D and D/A converter. The problem with a second-order modulator is the high oversampling ratio required to meet a dynamic range requirement According to the upper bound in (Eq 3-7), M=56 is required for 12 bit dynamic range, M=97 is required for 14 bit dynamic range and M=169 is required for 16 bit dynamic range. As a result, a single second-order modulator is impractical for high-speed applications.

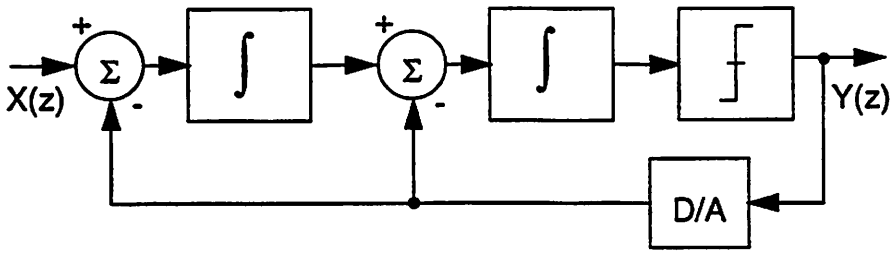

Fig. 3.3: Second-order sigma-delta modulator

To increase beyond a second-order loop, the designer must pay significant attention to stability. One approach to achieving a stable fourth-order single-loop design is shown in Fig. 3.4 [33]. The designers scale the integrator gains and place clippers on the outputs of each of the integrators to assure that the modulator remains stable when overloaded and during power up. This architecture achieves 14

bit resolution at 64 X oversampling ratio. The implementation in [33] achieves a 500 kS/s Nyquist rate which suggests that this architecture might be pushed into the 1MS/s range as technologies improve.

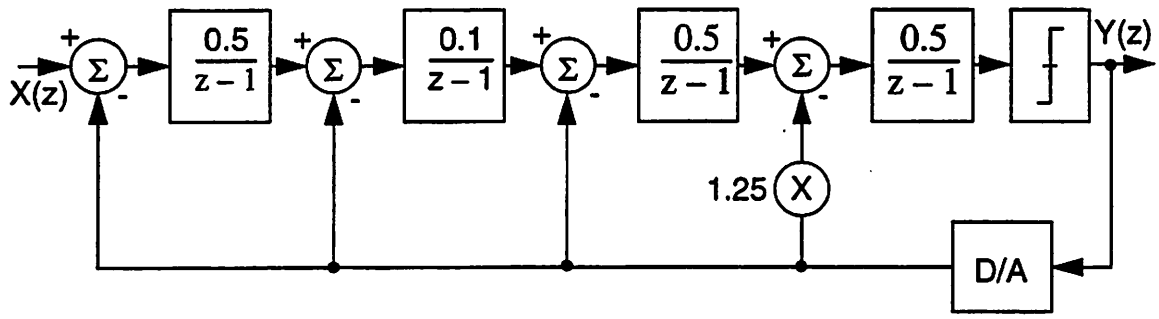

Fig. 3.4: Single-loop fourth-order modulator

One obvious extension to the architecture in Fig. 3.4 is to add a multi-bit D/A converter to improve the modulator dynamic range as shown in Fig. 3.5 [34]. This fourth-order modulator achieves 14 bit resolution at only 16 X oversampling ratio by using a 4 bit D/A converter. The integrators in this architecture have a delay-free transfer function to stabilize the loop and the integrator gains are selected as a compromise between stability and dynamic range. The obvious drawback to this approach is the need to calibrate the 4 bit D/A converter to 14 bit linearity.

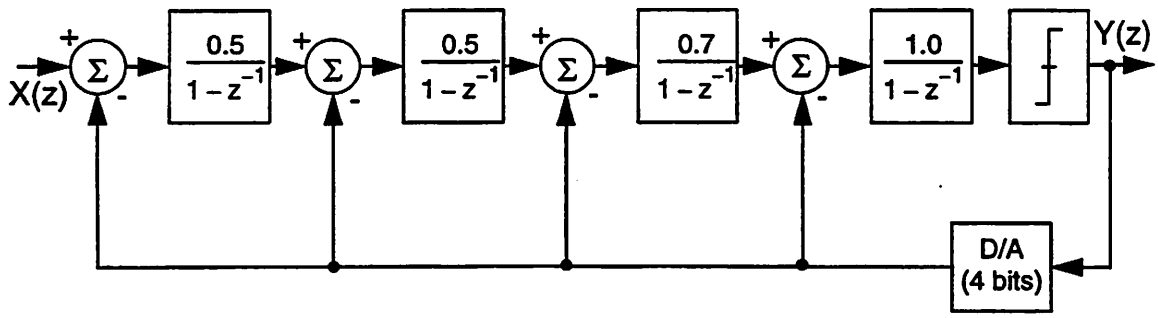

Fig. 3.5: Single-loop fourth-order modulator with a 4 bit D/A converter

An alternative approach to higher-order modulators distributes zeros in the noise across the signal band rather than just at DC. If done properly, this may more

efficiently shape the quantization noise out of the band of interest [35]. Generally referred to as interpolative architectures, these modulators use standard switched-capacitor filter design techniques to realize the desired noise-shaping. For example, the fourth-order modulator in Fig. 3.6 achieves 16 bit resolution at 64 X oversampling ratio with proper choice of coefficients [36].

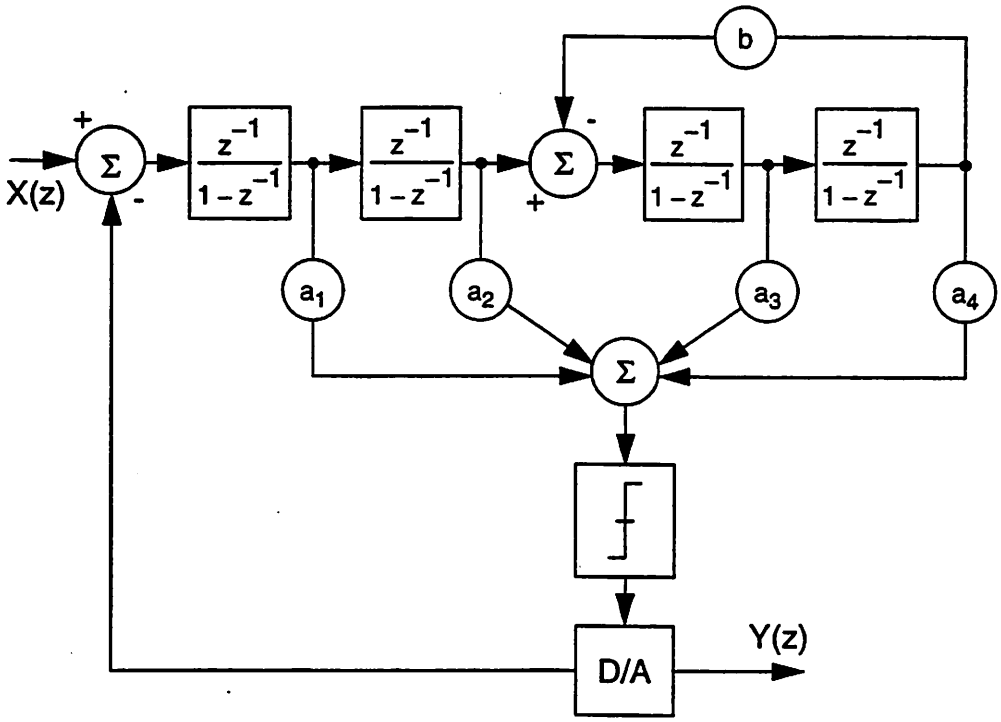

Fig. 3.6: Interpolative fourth-order modulator architecture

The interpolative architecture in Fig. 3.6 can be extended to higher orders. For example, a seventh-order modulator with a three-level D/A converter achieves 19 bit performance at 64 X oversampling ratio [37]. This performance is only three bits better than the fourth-order modulator at the same oversampling ratio which suggests that there are diminishing returns with increased order for this type of architectures. This problem of diminishing returns with increased order occurs because the choice of attenuating coefficients required to stabilize the loop offsets the increase in dynamic range from an additional integrator. This points to a general problem of higher-order

single loop modulators where the dynamic range is significantly below the upper bound in (Eq 3-7) due to the attenuation in the signal path required to stabilize the loop.

3.4.2 Cascade

Cascade architectures use combinations of inherently stable first and second-order sigma-delta modulators to achieve higher-order noise-shaping. Since stability criteria are relaxed as compared to the higher-order loops, the cascade modulators approach the dynamic range bound in (Eq 3-7) more closely than higher-order single loop implementations. An example of a 2-2 cascade architecture is shown in Fig. 3.7. In this architecture, the second modulator estimates the quantization error of the first modulator with an overall result obtained by an appropriate digital combination of the outputs. If the digital combination is done correctly, this results in fourth-order noise-shaping.

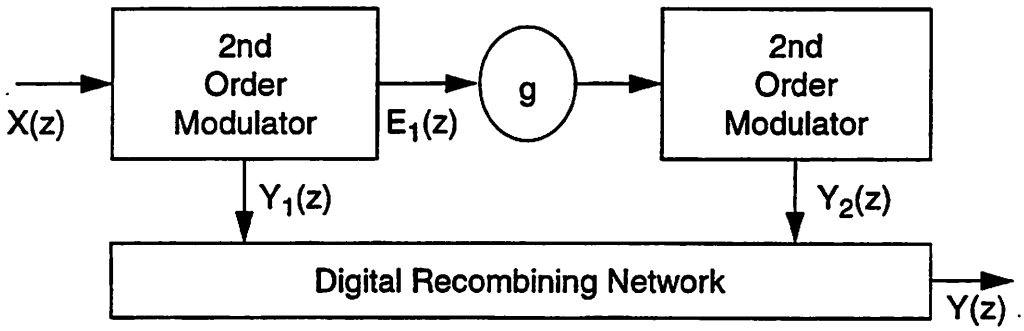

Fig. 3.7: 2-2 cascade architecture

Consider the transfer function of a second-order modulator with integrators as in (Eq 3-2). Then, including delays in the loop and neglecting any D/A converter linearity errors, the transfer function of the first second-order loop can be written as

in (Eq 3-8) and the transfer function of the second loop as in (Eq 3-9). It follows that

$$Y_1(z) = z^{-2}X(z) + (1-z^{-1})^2 E_1(z) \qquad \text{(Eq 3-8)}$$

$$Y_2(z) = z^{-2}[gE_1(z)] + (1-z^{-1})^2 E_2(z) \qquad \text{(Eq 3-9)}$$

the appropriate digital recombining network to cancel the first stage quantization error is defined in (Eq 3-10). Combining the results of (Eq 3-8), (Eq 3-9), and (Eq 3-10)

$$Y(z) = z^{-2}Y_1(z) - \frac{1}{g}(1-z^{-1})^2 Y_2(z) \qquad \text{(Eq 3-10)}$$

yields the overall fourth-order noise-shaping transfer function of the 2-2 cascade architecture in (Eq 3-11). Simulations suggest that this architecture can achieve 14 bit

$$Y(z) = z^{-4}X(z) - \frac{1}{g}(1-z^{-1})^4 E_2(z) \qquad \text{(Eq 3-11)}$$

performance at only 32 X oversampling ratio with single bit quantizers.

The cascade architecture can be combined with multi-bit D/A converters to improve dynamic range further. For example, a 2-1 cascade with a 3 bit D/A converter in the second stage achieves 12 bit resolution at 24 X oversampling ratio and 2.1 MS/s Nyquist rate [38]. Since the 3 bit D/A converter is at the input of the second loop rather than at the overall modulator input, the D/A converter linearity constraint is relaxed to only 6 bits. This easing of the linearity requirements occurs because the second stage D/A converter errors are attenuated by second-order noise-shaping when referred to the overall modulator input. Note that since the quantization error of the first stage does not appear directly at the output of the modulator, the use of a multi-bit D/A converter in the first stage will not improve the dynamic range of the cascaded modulator.

The cascade approach can also be extended to higher-orders simply by adding more first or second-order stages. The approach in [39] employs a cascade of three second-order modulators with three-level D/A converters to achieve 15 bit resolution at only 16 X oversampling ratio. Three-level quantizers can be realized with adequate linearity since one of the levels is zero. However, the quantizer is inactive most of the time at small input signal levels suggesting that an out-of-band dither signal needs to be added to keep it active when dealing with small signals.

The limit on the increase in order of cascaded modulators is set by matching requirements. If the gain in the analog and digital paths does not match, first stage quantization noise will leak through to the output. This can be seen for the 2-2 cascade example by modifying (Eq 3-10) where the mismatch is modeled by changing the gain term to $\hat{g}$ as shown in (Eq 3-12). With the mismatch included, the overall

$$Y(z) = z^{-2}Y_1(z) - \frac{1}{\hat{g}}(1-z^{-1})^2 Y_2(z) \qquad \text{(Eq 3-12)}$$

modulator transfer function in (Eq 3-11) will have an additional second-order noise-shaped term at the output as in (Eq 3-13). When this second-order noise-shaped term

$$Y(z) = z^{-4}X(z) + z^{-2}\left(1-\frac{g}{\hat{g}}\right)(1-z^{-1})^2 E_1(z) - \frac{1}{\hat{g}}(1-z^{-1})^4 E_2(z) \qquad \text{(Eq 3-13)}$$

becomes comparable to the quantization error, it will limit the dynamic range. As the order of the noise-shaping in the cascade is increased, the constraints on this mismatch term become more severe because the second-order noise-shaped term will be relatively larger compared to the desired noise-shaping of the overall modulator.

3.4.3 Comparison

The key issue in designing high-speed sigma-delta modulators is to lower the oversampling ratio to the point that it can be implemented in current integrated circuit technology. In most technologies, this suggests oversampling ratios of 32 X or below. The best single-loop architecture in the literature without a difficult to calibrate multi-bit D/A converter is seventh-order at 64 X oversampling ratio [37]. Ideally, this modulator achieves 140 dB of signal to quantization noise using a three-level D/A converter. Since the quantization noise of a seventh-order modulator decreases at a rate of 45 dB/octave with decreasing oversampling ratio according to (Eq 3-7), this modulator will achieve 95 dB of signal to quantization noise at 32 X oversampling ratio. In contrast at 32 X oversampling ratio, a 2-2 cascade architecture achieves approximately the same performance with three fewer integrators. To further improve the performance of a single-loop modulator will require a multi-bit D/A converter since there are diminishing returns and a difficult stability problem when trying to increase the order beyond seventh. This discussion suggests that the cascade architectures are favored at low oversampling ratios because they can achieve the same dynamic range at lower order than the single-loop modulators and therefore dissipate less power

The reason single-loop architectures have been favored for higher oversampling ratio applications is that they are relatively insensitive to mismatch in circuit components. For example, a fourth-order interpolative topology can tolerate up to 5% mismatch in its coefficients [40]. In contrast, the 2-2 cascade will require about 1% mismatch between the analog and digital interstage gains to achieve 14 bit performance. However, if the matching properties of the integrated circuit process are not adequate to meet the requirements, some form of calibration as described in Chapter 5 can be used to alleviate the problem. It will be shown that this calibration

problem is less severe than calibrating a multi-bit D/A converter at the input of a single-loop modulator.

3.5 Fundamental Power Limits

The discussion of sigma-delta modulators so far has focussed on how to achieve high-speed performance without taking into account the requirement to minimize power dissipation for the RF baseband processing application. While Chapter 4 will focus on a variety of low-power design techniques which can be applied to sigma-delta architectures, it is first necessary to understand where the power is going in sigma-delta modulators and what are the fundamental power limits.

The key circuit building block in a sigma-delta modulator is the integrator. Typically implemented using switched-capacitor techniques, the integrators will dominate the power dissipation of the modulator. The minimum achievable power dissipation is set by the need to charge and discharge capacitors of a given size at a given speed. This will be referred to as the dynamic power limit. In practice, switched-capacitor circuits are implemented using class A amplifiers which have static bias currents and burn significantly more power than the dynamic limit. In this section, both the dynamic and static power limits for switched-capacitor integrators are derived in the context of an oversampled system.

3.5.1 Dynamic Power Limit

The dynamic limit assumes that the only power dissipated in a switched-capacitor integrator is that which is required to charge and discharge the sampling capacitor. This is the absolute lower bound on the achievable power dissipation in a switched-capacitor circuit. Suppose the amplifier in Fig. 3.8 delivers just the required charge for the sampling capacitor, dissipates no static power and introduces no

additional noise into the circuit. Let the system Nyquist rate be f_N and oversampling ratio be M. The maximum voltage swing will be limited by the power supply V_{dd}. Then, it follows that the integrator power will obey the relationship in (Eq 3-14).

$$P \propto C_S V_{dd}^2 f_N M \qquad \text{(Eq 3-14)}$$

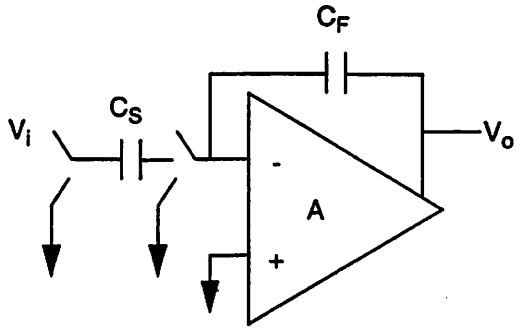

Fig. 3.8: Switched-capacitor integrator

Now consider the noise introduced by the sampling process. The circuit in Fig. 3.9 models a switched-capacitor MOS sample and hold circuit. When the switch is on, the voltage across the capacitor tracks the input voltage. At the instant the switch opens, a sample of both the input signal and the noise due to the switch is held on the capacitor. Since the switch is in the triode region, the single-sided power spectral density of the noise in (Eq 3-15) models the switch by its effective on resistance R_{on} [41]. The quantity of interest is not the power spectral density but the total inband noise

$$\bar{v}^2 = 4kTR_{on}\Delta f \qquad \text{(Eq 3-15)}$$

power which can be found by integrating the power spectral density accounting for the bandwidth of the switch and capacitor as in (Eq 3-16). Note that $P_{N,TOT}$ represents the

$$P_{N,TOT} = \int_0^\infty \frac{\bar{v}^2}{\Delta f} \frac{1}{|1 + j2\pi R_{on} C_S f|^2} df = \int_0^\infty \frac{4kTR_{on}}{1 + (2\pi R_{on} C_S f)^2} df = \frac{kT}{C_S} \qquad \text{(Eq 3-16)}$$

total sampled noise in the interval $(\frac{-f_s}{2},\frac{f_s}{2})$ where f_s is the sampling frequency. Since the sampling process causes uncorrelated noise from higher frequencies to alias into this frequency region, the noise may be modeled as white with the two-sided power spectral density in (Eq 3-17). Since this is an oversampled system, only noise in the region

$$S_N = \frac{kT}{f_s C_S} \qquad \text{(Eq 3-17)}$$

$(-f_b,f_b)$ corrupts the desired signal. The noise power in the region of interest (P_N) is simply the integral of the power spectral density over the bandwidth in (Eq 3-18). Note

$$P_N = \int_{-f_b}^{f_b} \frac{kT}{f_s C_S} df = \frac{2f_b kT}{f_s C_S} = \frac{kT}{MC_S} \qquad \text{(Eq 3-18)}$$

that the overall noise is independent of the switch resistance and inversely proportional to the sampling capacitance. In addition, the noise is inversely proportional to the oversampling ratio which implies that oversampling ratio and capacitor size trade off for a fixed noise specification.

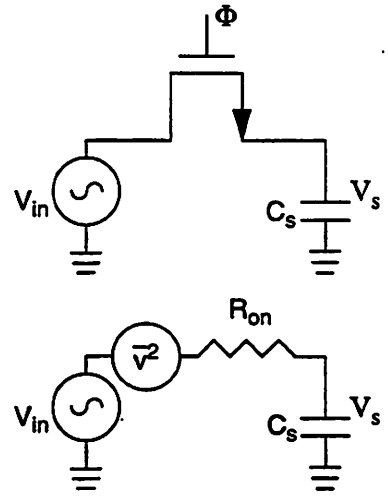

Fig. 3.9: MOS sample and hold and noise model

The next step is to relate the thermal noise to the dynamic range requirement for a switched-capacitor integrator. Assume that the maximum signal

power is limited by the power supply voltage V_{dd}. Then, it follows that the dynamic range obeys the relationship in (Eq 3-19). Note that the dynamic range is proportional

$$DR \propto \frac{MC_S V_{dd}^2}{kT} \qquad \text{(Eq 3-19)}$$

to the capacitor size, the oversampling ratio and the square of the power supply voltage. This dynamic range expression does not include quantization noise, but for this analysis it is assumed that the modulator is thermal noise limited.

Observe that the power dissipation can now be related to the dynamic range by combining (Eq 3-14) and (Eq 3-19). As indicated in (Eq 3-20), the dynamic power

$$P \propto kT(DR)f_N \qquad \text{(Eq 3-20)}$$

limit for an oversampled switched-capacitor circuit is independent of the oversampling ratio and the power supply voltage. Power and speed trade off since power is directly proportional to the Nyquist rate f_N. In addition, power and noise trade off since power is directly proportional to dynamic range.

3.5.2 Static Power Limit

While the dynamic limit sets the absolute lower bound on power dissipation in switched-capacitor circuits, it is not achievable because practical implementations employ class A operational amplifiers which dissipate static power. The simplest model of a class A operational amplifier is a single transistor driving a series of capacitors as shown in Fig. 3.10 [42]. The amplifier is biased at a current (I) and therefore dissipates static power given by (Eq 3-21).

$$P = V_{dd}I \qquad \text{(Eq 3-21)}$$

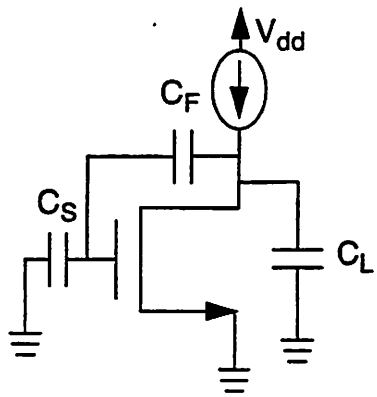

Fig. 3.10: Single transistor op amp model of a switched-capacitor integrator

With a series of simplifying assumptions, it is possible to relate the static power to fundamental parameters of the system.

1) Assume the device is biased at fixed V_{GS}-V_T which implies that the device transconductance (g_m) is directly proportional to the bias current (I).

2) Assume that the feedback factor (f) given by (Eq 3-22) is fixed. This is equivalent to assuming that the gate capacitance C_{GS} of the transistor is small compared to the sampling capacitance.

$$f = \frac{C_F}{C_F + C_S + C_{GS}} \approx \frac{C_F}{C_F + C_S} \qquad \text{(Eq 3-22)}$$

3) Assume that the total capacitive loading ($C_{L,TOT}$) on the operational amplifier given by (Eq 3-23) is dominated by the sampling network. Note that the device parasitics and any external load capacitance has been lumped into C_L.

$$C_{L,TOT} = \frac{C_F(C_S + C_{GS})}{C_F + C_S + C_{GS}} + C_L \approx \frac{C_F C_S}{C_F + C_S} \qquad \text{(Eq 3-23)}$$

A single transistor amplifier has a single pole settling characteristic with time constant given by (Eq 3-24). At a given sampling rate and for a given dynamic

$$\tau = \frac{C_{L,TOT}}{fg_m} \approx \frac{C_S}{g_m} \qquad \text{(Eq 3-24)}$$

range the amplifier must settle to a certain accuracy which can be defined by a number of single pole time constants. This implies that the time constant can be related to the sampling frequency though the proportionality in(Eq 3-25).

$$\tau \propto \frac{1}{Mf_N} \qquad \text{(Eq 3-25)}$$

Using assumption one above and substituting with the result from (Eq 3-24), (Eq 3-21) can be rewritten as the proportionality in (Eq 3-26). Substituting the results

$$P \propto V_{dd}g_m = \frac{V_{dd}C_S}{\tau} \qquad \text{(Eq 3-26)}$$

from (Eq 3-19) and (Eq 3-25) into (Eq 3-26) yields the static power limit in (Eq 3-27).

$$P \propto \frac{(DR)kTf_N}{V_{dd}} \qquad \text{(Eq 3-27)}$$

Like the dynamic limit, the static power limit is independent of oversampling ratio. In addition, dynamic range and power trade off as do speed and power. However, the static limit is inversely proportional to the power supply voltage which suggests that the trend toward lower supplies favored by digital circuits and required by deep submicron CMOS processes will have an adverse effect on power dissipation.

3.6 Summary

Sigma-delta modulators were introduced in this chapter. Beginning with a discussion of the metrics used to evaluate modulator performance, the fundamental concept of how a modulator works was described. Then, a variety of single-loop and cascade sigma-delta architectures were evaluated, and it was determined that cascade architectures were more suitable for high-speed applications. Finally, the fundamental dynamic and static power limits for switched-capacitor integrators in oversampled systems were derived. The limits suggest that power trades off with dynamic range and speed and is inversely related to supply voltage.

Chapter 4
Design Techniques for Low-Power Sigma-Delta Modulators

4.1 Introduction

This chapter describes various design techniques that can be used at the architecture level to reduce power dissipation in high-speed sigma-delta modulators. The discussion extends the analysis of fundamental power limits in Chapter 3 to include a variety of second-order effects and shows the appropriate choice of oversampling ratio to minimize power dissipation. Then, a 2-2-2 cascade architecture oversampling at 16 X is introduced based upon the oversampling ratio analysis. Signal-scaling to maximize modulator overload level is discussed. Finally, scaling capacitors to the minimum value required by kT/C noise considerations is shown to be an effective power reduction strategy.

4.2 Oversampling Ratio Selection

The analysis in Section 3.5 showed that power dissipation is to first order independent of oversampling ratio for systems implemented with switched-capacitor circuits. However, this analysis was oversimplified because it neglected such second-

order effects as parasitic capacitances due to the transistors used to implement the operational amplifiers and clock rise, fall and nonoverlap times. Furthermore, the analysis did not account for the changes in the order of a sigma-delta modulator with fixed dynamic range as the oversampling ratio is changed and the use of such power reduction techniques as capacitor scaling which will be described in Section 4.5. In this section, the design example of a 14 bit 2 MS/s modulator implemented in a 0.72 μm CMOS process is used to illustrate how oversampling ratio affects power dissipation including all second-order effects. In addition, the power limit analysis for a single integrator is modified to include second-order effects.

4.2.1 Power vs. Oversampling Ratio

Consider implementing the 14 bit 2 MS/s sigma-delta modulator using a cascade architecture which is suitable for high-speed operation. System level simulations suggest that any of four possible cascade architectures can meet the specifications: 1) eighth order at 12 X oversampling ratio, 2) sixth order at 16 X oversampling ratio, 3) fifth order at 24 X oversampling ratio, and 4) fourth order at 32 X oversampling ratio. It is impossible to meet the operational amplifier settling requirements in a 0.72 μm technology at sampling rates above 64 MHz (32 X oversampling ratio). Below 12 X oversampling ratio, the required order of the sigma-delta loop for 14 bit performance increases rapidly which does not allow for a low-power implementation.

Additional constraints are required to make the problem tractable. Only the static bias currents in the operational amplifiers are assumed to contribute significant power dissipation. The operational amplifier is implemented using the two-stage topology with cascoded compensation and dynamic level-shift between the stages as will be described in Section 6.3. Capacitors in the switched-capacitor

integrators are scaled to the minimum value required by kT/C noise at each stage in the cascade using the method in Section 4.5.

Given the above constraints, the settling time, slew rate, and thermal noise requirements are specified for each integrator in each of the cascade architectures. The operational amplifiers are designed and simulated using SPICE to verify that the specifications are met. The results of these simulations in Fig. 4.1 show that a sixth order architecture oversampling at 16 X minimizes power dissipation. As shown in Fig. 4.2, the first integrator in the cascade dominates the power dissipation for each architecture because it is strongly kT/C limited and must settle to the full 14 bit accuracy of the modulator. Increasing the order of the modulator by adding more integrators at the end of the cascade is relatively cheap because later integrators do not contribute significant thermal noise at the modulator input and can use minimum sized capacitors. However, as the oversampling ratio is reduced to 12 X, the increase in order becomes large enough that the power dissipation increases as compared to the 16 X case. This increase in modulator order sets the lower bound on oversampling ratio to minimize power dissipation.

The results in Fig. 4.1 and Fig. 4.2 contradict the fundamental power limit in (Eq 3-27) which suggests that power is independent of oversampling ratio. However, the derivation of this limit did not account for several second-order effects which cost power in actual implementations. The achievable clock rise, fall, and non-overlap times for switched-capacitor circuits are fixed by a given technology. This implies that rise, fall and non-overlap times occupy a larger fraction of the clock period as the sampling frequency is increased. As a result, the available settling time for the operational amplifier is fractionally reduced. Despite the decrease in sampling capacitance as the oversampling ratio is increased, this fractional reduction in available settling time results in increased power dissipation, This occurs because increased device transconductance is necessary to meet the settling constraints.

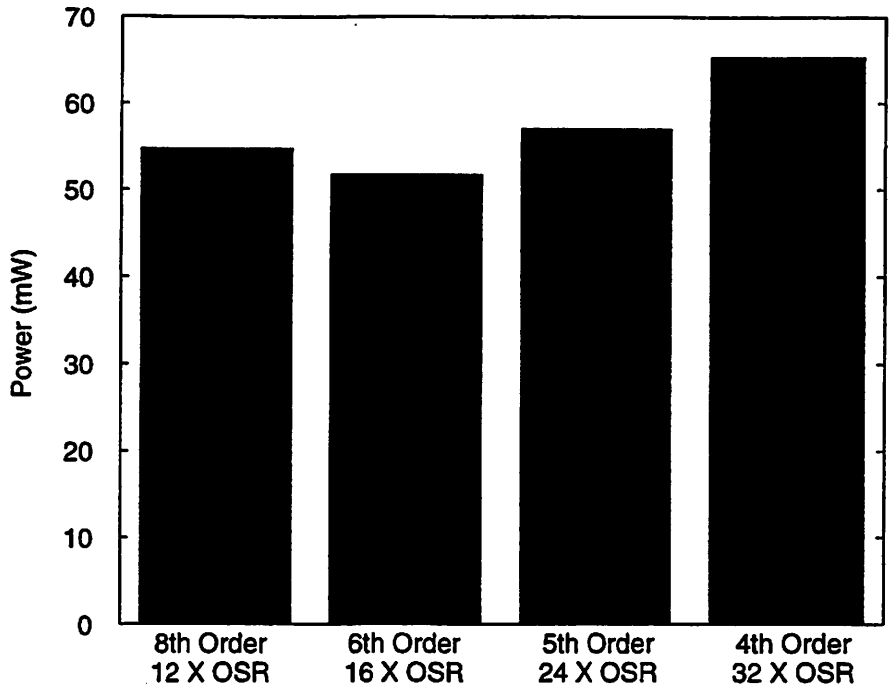

Fig. 4.1: Power vs. oversampling ratio

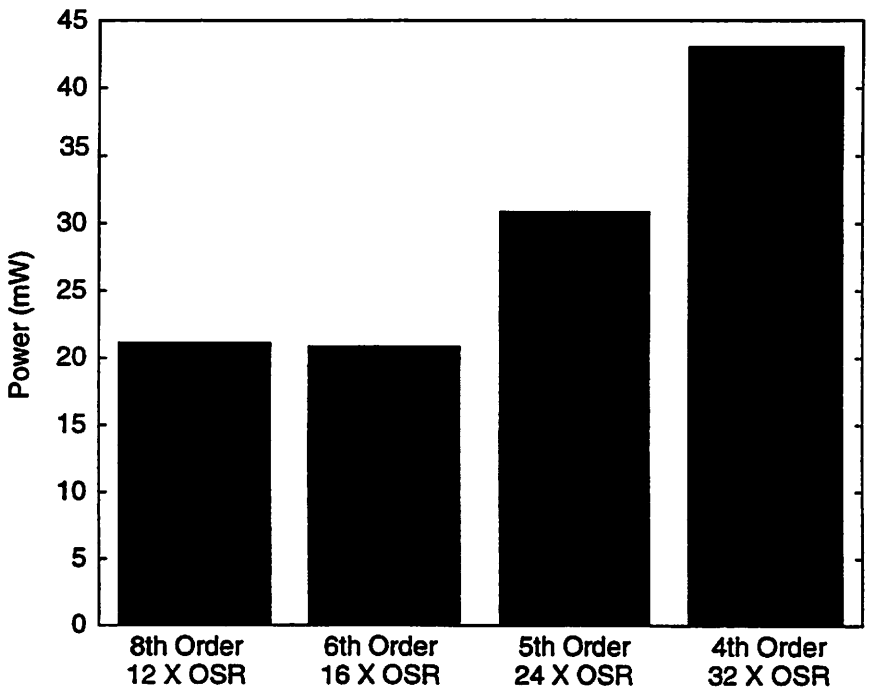

Fig. 4.2: First integrator power vs. oversampling ratio

The fundamental power limit only accounted for power dissipated in driving the sampling capacitance but not device parasitic capacitances. As the oversampling ratio is increased, the sampling capacitance is proportionally reduced while the parasitics are fixed for fixed transconductance. This implies that the parasitic capacitances become proportionally larger compared to the sampling capacitance and additional power will need to be expended to drive the parasitics.

Since the power dissipation is dominated by the first switched-capacitor integrator in each of the architectures, it is instructive to revisit the fundamental power limits accounting for second-order effects associated with the clocking and parasitic capacitances. The portion of the clock cycle wasted by clock nonoverlap, rise and fall times may be modeled by modifying (Eq 3-25) which describes the settling time constant of a single transistor amplifier. This portion of the clock cycle is denoted by t_{clk} in (Eq 4-1).

$$\tau \propto \frac{1}{Mf_N} - t_{clk} \qquad \text{(Eq 4-1)}$$

Amplifier input parasitic capacitance C_{GS} and output parasitic and external load capacitances which are lumped together as C_L cannot be neglected. This implies that the feedback factor f at the input of the amplifier in (Eq 3-22) must include C_{GS} as in (Eq 4-2) and the total amplifier loading $C_{L,TOT}$ in (Eq 3-23) must include both C_{GS}

$$f = \frac{C_F}{C_F + C_S + C_{GS}} \qquad \text{(Eq 4-2)}$$

and C_L as in (Eq 4-3).

$$\begin{aligned} C_{L,TOT} &= \frac{C_F(C_S + C_{GS})}{C_F + C_S + C_{GS}} + C_L \\ &= \frac{C_F C_S}{C_F + C_S + C_{GS}} + \frac{C_{GS}}{C_F + C_S + C_{GS}} + C_L \end{aligned} \qquad \text{(Eq 4-3)}$$

With the addition of the device parasitic capacitances, the single pole time constant of the amplifier in (Eq 3-24) can be modified as in (Eq 4-4). This equation

$$\tau = \frac{C_{L,TOT}}{fg_m} = \frac{C_S}{g_m} + \frac{C_{GS}}{C_F g_m} + \frac{C_L(C_F + C_S + C_{GS})}{C_F g_m} = \frac{C_S + C_P}{g_m} \qquad \text{(Eq 4-4)}$$

shows that the time constant depends on the device transconductance and sampling capacitance as well as the parasitic capacitances which have been lumped together as C_P to include the effects of C_L and C_{GS}.

It is now possible to relate the settling to power consumption by modifying (Eq 3-26) to account for parasitic capacitances. If it is still assumed that the transistor is biased at fixed V_{GS}-V_T, this results in (Eq 4-5). Now, combine (Eq 4-1),(Eq 4-5) and

$$P \propto V_{dd} g_m = \frac{V_{dd}(C_S + C_P)}{\tau} \qquad \text{(Eq 4-5)}$$

the kT/C noise limit from (Eq 3-19) to find power as a function of fundamental parameters in (Eq 4-6). The second-order effects modeled in (Eq 4-6) suggest that there

$$P \propto \left[\frac{(DR)kTf_N}{V_{dd}} + V_{dd}C_P M f_N\right]\frac{1}{1 - Mf_N t_{CLK}} \qquad \text{(Eq 4-6)}$$

is a portion of power which is independent of oversampling ratio. In addition, parasitic capacitances create an additive term which is directly proportional to oversampling ratio and there is a fixed multiplicative term which is related to clocking effects. The above analysis explains why power dissipation increases dramatically in the first integrator in a cascaded sigma-delta modulator as the oversampling ratio increases above 16 X. At 12 X and 16 X oversampling ratios, the power dissipation in the first integrator is independent of oversampling ratio which suggests that these second-order effects are small at low oversampling ratios. The power increase in the first integrator above 16 X oversampling ratio is not completely offset by decreasing modulator orders

or relaxed requirements on subsequent integrators. As shown in Fig. 4.1, this suggests that the sixth-order modulator at 16 X oversampling ratio is the minimum power solution for a 14 bit, 2MS/s specification.

4.2.2 Antialiasing Requirements

The sigma-delta modulator must be considered in the context of a larger system taking into account the requirements placed on the continuous time antialiasing filter. Fig. 4.3 shows an RF baseband channel using a sigma-delta modulator to perform digital channel selection. To avoid the aliasing of out-of-band blockers into the desired single band, the antialiasing filter must provide adequate attenuation at the sigma-delta sampling frequency. Given a desired channel bandwidth, worst case desired signal power, and worst case out-of-band blocker levels, the designer can calculate the number of poles required in the antialiasing filter as a function of the sigma-delta oversampling ratio. The power dissipation in the antialiasing filter is directly related to the number of poles. As a result, if the number of poles in the filter can be decreased by increasing the oversampling ratio, the overall power dissipation in the baseband channel may decrease even though the sigma-delta modulator power will increase.

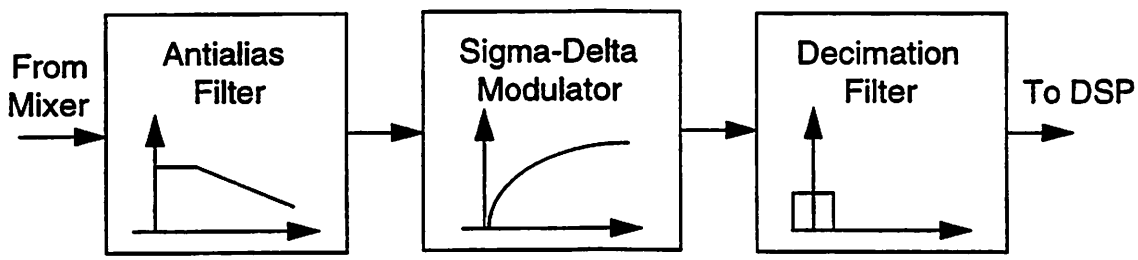

Fig. 4.3: RF baseband channel using a sigma-delta modulator

4.2.3 Area

Die area is an important consideration in the cost of an integrated circuit. Increasing the oversampling ratio of a sigma-delta modulator will reduce the overall capacitance required which in turn reduces the die area. While this area reduction could cost some power dissipation, it may be required if the sigma-delta modulator takes up a significant fraction of the total die area. This is especially true in the RF baseband channel application where two modulators are required, one for the in-phase component and one for the quadrature component.

4.3 2-2-2 Cascade Architecture

A sixth-order modulator oversampling at 16 X achieves 14 bits, 2 MS/s at minimum power dissipation. The modulator is implemented as a cascade of three second-order loops with feedback coefficients (b_i) coupled by two interstage coefficient networks g_1, λ_1, g_2, λ_2 as shown in Fig. 4.4. Each integrator has a full delay between its input and output to create a fully pipelined structure. Single bit quantizers and D/A converters are used in the first two stages while a three-level quantizer and D/A converter is used in the final stage to improve dynamic range. The ideal simulated dynamic range of this architecture is 96 dB as shown in Fig. 4.5. The simulated dynamic range includes only quantization noise; the rest of the error budget for the modulator will be allocated to thermal noise and various nonidealities such as mismatch, amplifier settling and slew rate.

The interstage coefficients should be selected to achieve the best possible overload characteristics for the modulator [43]. The overload level is defined as the maximum input signal level relative to full scale that the modulator can handle. This level corresponds to an input signal which produces SNDR 3 dB below the peak on the downward sloping part of a characteristic like that in Fig. 4.5. When a larger

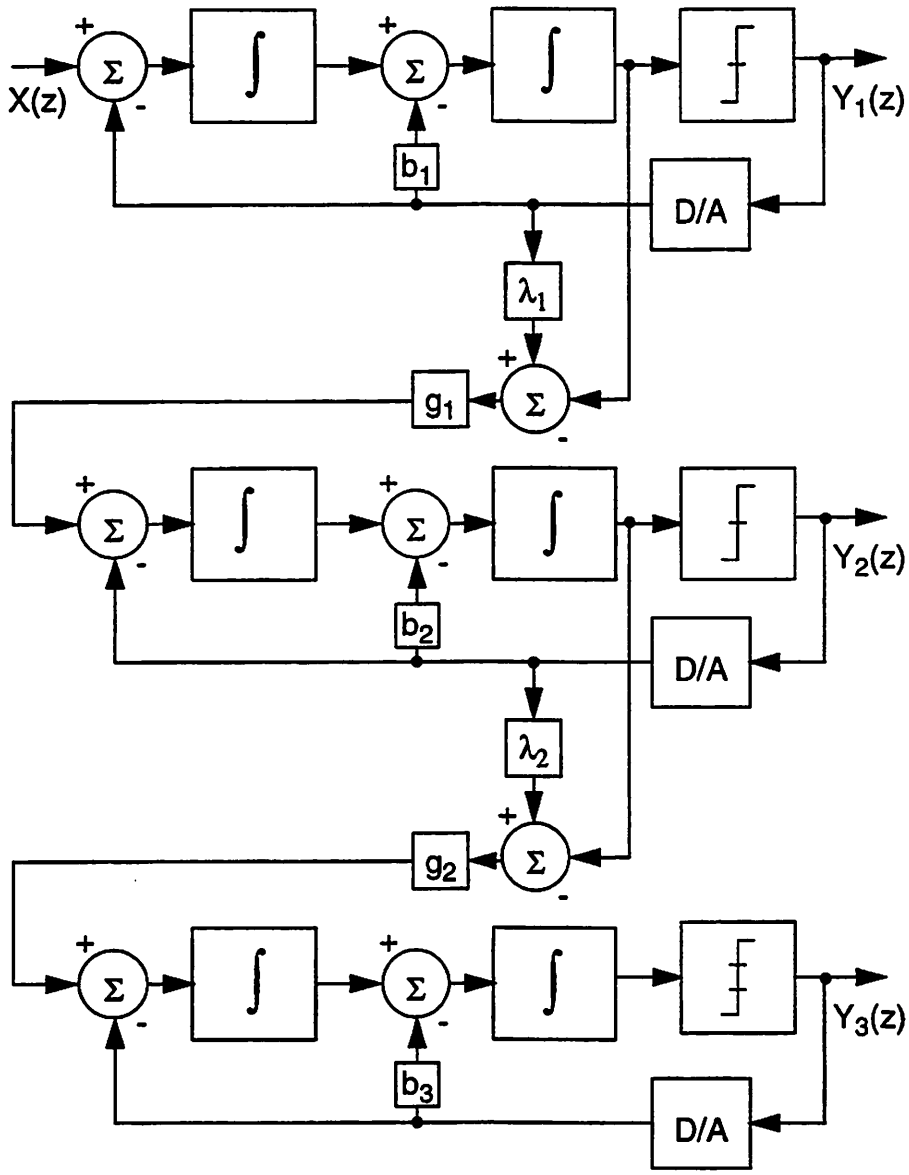

Fig. 4.4: 2-2-2 cascade architecture

maximum signal can be handled, the thermal noise requirements are relaxed for a modulator of fixed dynamic range. This implies that smaller capacitors and correspondingly smaller bias currents can be used in a kT/C limited design. As a result, achieving good overload performance can be viewed as a power reduction strategy. In addition, the interstage coefficients should be selected to simplify the processing in the digital recombination network by assuring that all multiplies are by a power of two which can be implemented as a simple bit shift.

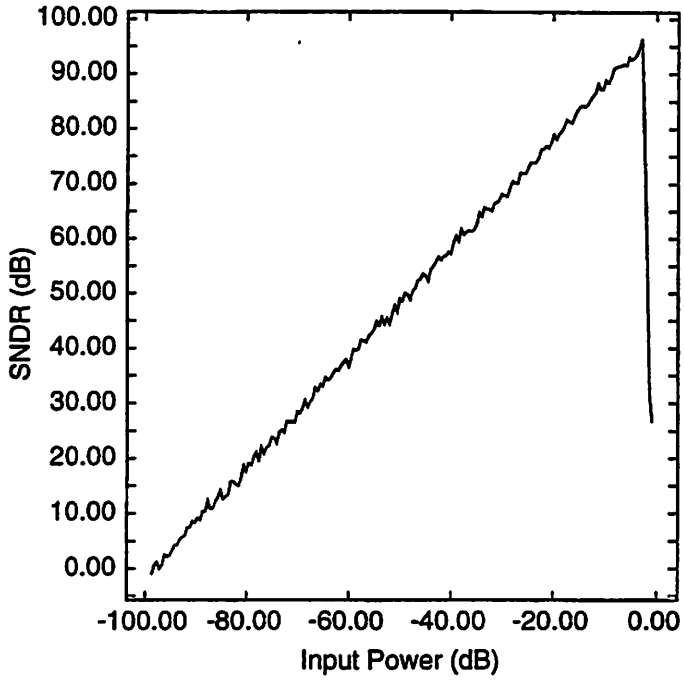

Fig. 4.5: Simulated SNDR vs. input power for a 2-2-2 cascade modulator at 16 X OSR

For the 2-2-2 cascade architecture in Fig. 4.4, the recombining network equations can be written as in (Eq 4-7) - (Eq 4-10).The constraint of simple bit shifts in

$$Y(z) = H_1(z)Y_1(z) - H_2(z)Y_2(z) + H_3(z)Y_3(z) \qquad \text{(Eq 4-7)}$$

$$H_1(z) = \lambda_1 z^{-4} - 2(\lambda_1 - 1)z^{-5} + (\lambda_1 - 1)z^{-6} \qquad \text{(Eq 4-8)}$$

$$H_2(z) = \frac{1}{g_1}(1 - 2z^{-1} + z^{-2})[\lambda_2 z^{-2} - 2(\lambda_2 - 1)z^{-3} + (\lambda_2 - 1)z^{-4}] \qquad \text{(Eq 4-9)}$$

$$H_3(z) = \frac{1}{g_1 g_2}(1 - 2z^{-1} + z^{-2})^2 \qquad \text{(Eq 4-10)}$$

the digital multiplies can be met with g_1 and g_2 which are any power of two and λ_1 and λ_2 which are 0, 1, or 2. Each second-order loop produces an output given by (Eq 4-11) where the first loop has input $X_1(z) = X(z)$ and subsequent loops have inputs given by

(Eq 4-12). The output of the overall modulator assuming perfect matching between the

$$Y_i(z) = z^{-2}X_i(z) + (1-z^{-1})^2 E_i(z) \qquad \text{(Eq 4-11)}$$

$$X_i(z) = g_{i-1}[(\lambda_{i-1} - 1)Y_{i-1}(z) + E_{i-1}(z)] \qquad \text{(Eq 4-12)}$$

analog path and digital recombining network is expressed in (Eq 4-13) where $E_3(z)$ denotes the quantization error from the third loop in the cascade. This equation

$$Y(z) = z^{-6}X(z) + \frac{1}{g_1 g_2}(1-z^{-1})^6 E_3(z) \qquad \text{(Eq 4-13)}$$

suggests that the g_1 and g_2 should be maximized to reduce the size of the quantization error term while λ_1 and λ_2 should be selected solely on the basis of overload performance. Table 4.1 shows the values of the coefficients for the 2-2-2 cascade architecture which were obtained from simulation.

Table 4.1:Interstage coefficients

Coefficient	Value
g_1	0.25
g_2	0.5
λ_1	2
λ_2	2

Like any cascade architecture, the 2-2-2 cascade is sensitive to the effects of component mismatch at the interstage nodes. Mismatch requirements and calibration techniques will be described in Chapter 5.

4.4 Signal Scaling

To avoid clipping for large input signals, it is necessary to place appropriate attenuation factors in front of each integrator in the 2-2-2 cascade sigma-delta modulator. The goal of this signal scaling process is to maximize the overload level of the entire modulator by using all of the available signal swing at the output of each integrator without clipping. To begin the scaling process, the 2-2-2 cascade architecture in Fig. 4.4 must be mapped into an equivalent structure that can be implemented using switched-capacitor circuits as shown in Fig. 4.6. To maintain equivalence, the coefficients are constrained to satisfy the following equations:[30].

$$x = \frac{a_{i1}}{a_{f1}} v_i \qquad \text{(Eq 4-14)}$$

$$b_1 = \frac{a_{f2}}{a_{f1} a_{i2}} \qquad \text{(Eq 4-15)}$$

$$g_1 = \frac{a_{f1} a_{i2} a_{u3}}{a_{f3}} \qquad \text{(Eq 4-16)}$$

$$\lambda_1 = \frac{a_{i3}}{a_{f1} a_{i2} a_{u3}} \qquad \text{(Eq 4-17)}$$

$$b_2 = \frac{a_{f4}}{a_{f3} a_{i4}} \qquad \text{(Eq 4-18)}$$

$$g_2 = \frac{a_{f3} a_{i4} a_{u5}}{a_{f5}} \qquad \text{(Eq 4-19)}$$

$$\lambda_2 = \frac{a_{i5}}{a_{f3} a_{i4} a_{u5}} \qquad \text{(Eq 4-20)}$$

$$b_3 = \frac{a_{f6}}{a_{f5} a_{i6}} \qquad \text{(Eq 4-21)}$$

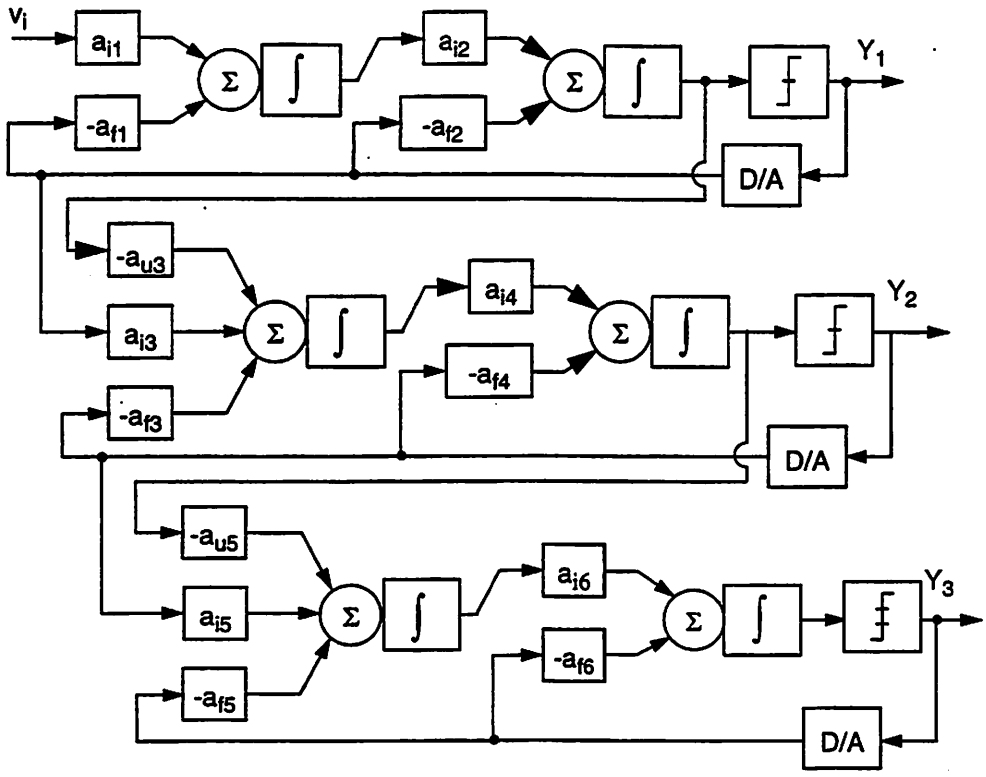

Fig. 4.6: 2-2-2 cascade architecture implementation

Since (Eq 4-14) - (Eq 4-21) are only eight equations while there are 14 coefficients to fully specify the modulator, the remaining six degrees of freedom can be used to maximize the modulator overload characteristics. Following a simulation procedure like that in [30], bounds on each integrator feedback coefficient (a_{fi}) may be found. Fig. 4.7 shows the normalized maximum swing at the output of each integrator as a function of input signal power. Prior to overload, each of the curves is relatively

flat; the value at the knee of each curve sets the constant in the following inequalities which denormalize the simulation results:

$$3.5a_{f1} < 1 \quad \text{(Eq 4-22)}$$

$$3.5a_{f2} < 1 \quad \text{(Eq 4-23)}$$

$$3.5a_{f3} < 1 \quad \text{(Eq 4-24)}$$

$$3a_{f4} < 1 \quad \text{(Eq 4-25)}$$

$$5a_{f5} < 1 \quad \text{(Eq 4-26)}$$

$$5a_{f6} < 1 \quad \text{(Eq 4-27)}$$

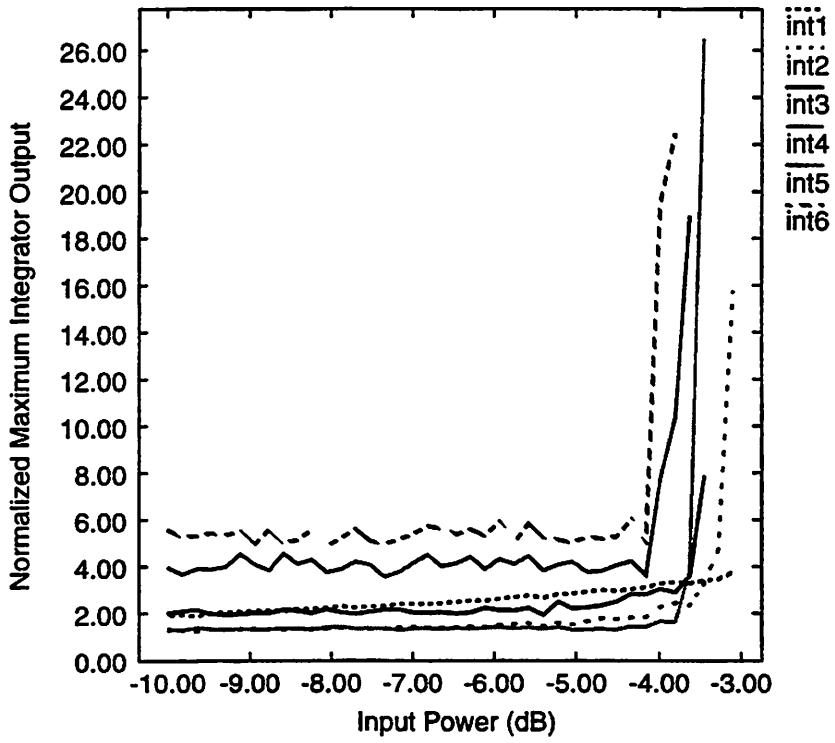

Fig. 4.7: Maximum integrator output swings as a function of input power

If inequalities (Eq 4-22) - (Eq 4-27) are satisfied, then the modulator will achieve good overload performance. An additional constraint is to select the

coefficients at the input of each integrator in ratios which facilitate capacitor sharing between its forward and feedback path. Given the values of g_i and λ_i from Table 4.1 and $b_i = 2.5$ (for reduced tones in the quantization noise [30]), the coefficients for the 2-2-2 cascade modulator can now be fully specified as shown in Table 4.2. With this choice of coefficients, the modulator input overload level is approximately 2.0 dB below the reference level.

Table 4.2:Coefficient values

Coefficient	Value
a_{i1}	0.2
a_{f1}	0.2
a_{i2}	0.5
a_{f2}	0.25
a_{u3}	0.5
a_{i3}	0.1
a_{f3}	0.2
a_{i4}	0.5
a_{f4}	0.25
a_{u5}	1.0
a_{i5}	0.2
a_{f5}	0.2
a_{i6}	0.4
a_{f6}	0.2

4.5 Capacitor Scaling

A key approach to reducing power dissipation in switched-capacitor circuits is to use the minimum sized capacitor required by kT/C noise considerations. A capacitor scaling technique similar to that in [50] for a pipelined A/D converter can be

used to take advantage of relaxed noise requirements for later stages in the cascade of switched-capacitor integrators. Using a noise-shaping argument, the total input referred thermal noise of the 2-2-2 cascade sigma-delta modulator can be derived. (Eq 4-28) shows that the total input referred thermal noise of the modulator ($S_{N,TH}$) is a function of the input referred noise of each integrator (S_{Ni}), the oversampling ratio (M) and the gain between the modulator input and each integrator input (A_i)

$$S_{N,TH} = \frac{S_{N1}}{M} + \frac{\pi^2}{3A_2^2M^3}S_{N2} + \frac{\pi^4}{5A_3^2M^5}S_{N3} + \frac{\pi^6}{7A_4^2M^7}S_{N4} + \frac{\pi^8}{9A_5^2M^9}S_{N5} + \frac{\pi^{10}}{11A_6^2M^{11}}S_{N6} \qquad \text{(Eq 4-28)}$$

For highly oversampled solutions, the input referred noise is such a strong function of the oversampling ratio that only the first stage in the cascade contributes significant thermal noise; the sampling capacitors of subsequent stages will be selected based on parasitic considerations rather than noise. However, in the high-speed scenario at moderate oversampling ratio, more than one stage will contribute thermal noise at the modulator input. Still, sampling capacitor sizes of later stages may be scaled as compared to the first stage to reduce power.

The noise shaping argument in (Eq 4-28) also applies to other error sources entering the modulator at the inputs of later integrators in the cascade. Errors due to the finite settling time and slew rate of operational amplifiers will be less significant for later integrators in the cascade because they are attenuated by the noise-shaping of the overall modulator when referred to the input. Relaxed settling requirements can be met with lower amplifier transconductance which translates directly into lower power dissipation.

Now consider the 2-2-2 cascade architecture with integrator scaling coefficients from Table 4.2 and 16 X oversampling ratio. The input referred thermal

noise of each integrator can be modeled as a constant γ_i multiplied by kT/C as in (Eq 4-29). If the operational amplifier used to implement the integrator is noiseless, γ_i will be four for a fully differential topology; in practical cases γ_i will be larger due to the amplifier noise contribution. With the noise model in (Eq 4-29), the input referred noise

$$S_{Ni} = \frac{\gamma_i kT}{C_{Si}} \qquad \text{(Eq 4-29)}$$

of the 2-2-2 cascade modulator may be found as a function of the sampling capacitances. (Eq 4-30) shows the relative noise contributions of each stage in the cascade. The numerical values of the constants suggest that the last three stages will be limited mainly by parasitic capacitances while the first three stages will be limited mainly by thermal noise.

$$\begin{aligned} S_{N,TH} = {} & 0.0625\gamma_1\frac{kT}{C_{s1}} + 0.02\gamma_2\frac{kT}{C_{s2}} + 1.85\times10^{-3}\gamma_3\frac{kT}{C_{s3}} \\ & + 2.05\times10^{-4}\gamma_4\frac{kT}{C_{s4}} + 2.46\times10^{-5}\gamma_5\frac{kT}{C_{s5}} + 4.84\times10^{-6}\gamma_6\frac{kT}{C_{s6}} \end{aligned} \qquad \text{(Eq 4-30)}$$

Using (Eq 4-30), it is possible to optimize the power dissipation of the modulator by selecting the capacitances in the first three stages to minimize power dissipation in the amplifiers. The optimization procedure is iterative in nature since the input referred noise is a nonlinear function of the integrator sampling capacitances. Fig. 4.8 shows the normalized power dissipation for each of the stages in the cascade for the experimental prototype. Power dissipation is reduced by more than 2 X when compared to the use of identical amplifiers for all stages in the cascade.

4.6 Summary

This chapter described a number of techniques which can be employed to reduce power dissipation in a high-speed sigma-delta modulator. At the system level,

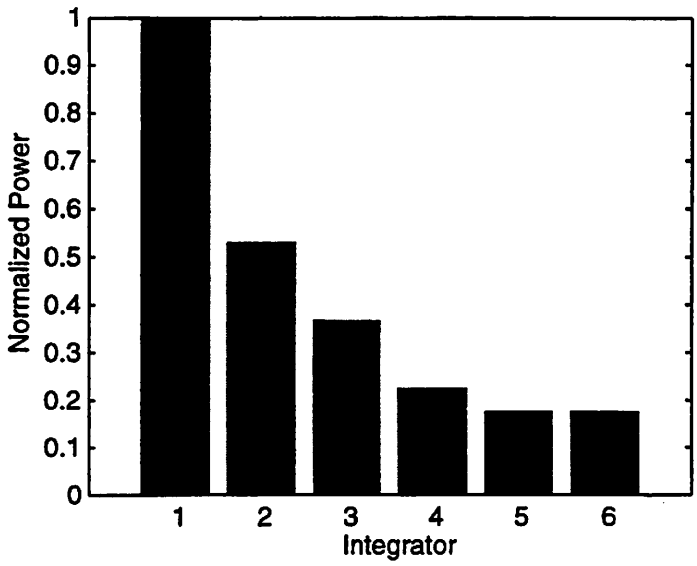

Fig. 4.8: Normalized power dissipation of each integrator with capacitor scaling

it was shown that power dissipation in a sigma-delta modulator depends fundamentally on meeting kT/C noise requirements. However, second-order effects such as parasitic capacitances in the amplifiers and finite clock rise, fall and nonoverlap times increase the power dissipation of high-speed sigma-delta modulators as the oversampling ratio is increased. As a result, the oversampling ratio and loop order should be selected such that the kT/C limited sampling capacitance of the first integrator dominates the power dissipation. For a 14 bit, 2 MS/s modulator implemented in a 0.72 μm CMOS process, this minimum power point occurs for a sixth-order modulator at 16 X oversampling ratio. Once an oversampling ratio and loop order is selected, a particularly effective method of reducing power dissipation is to scale the sampling capacitance of each integrator in the cascade to the minimum value required by kT/C noise. This capacitor scaling technique reduces power dissipation by 2.5 X in the prototype implementation.

Chapter 5
Calibration of Mismatch in Cascaded Sigma-Delta Modulators

5.1 Introduction

This chapter explores both analog and digital techniques to calibrate out the effects of mismatch in the interstage gain coefficients of a cascaded sigma-delta modulator. Mismatch is analyzed in detail for the example of the 2-2-2 cascade architecture described in Chapter 4. Then, analog trim and digital calibration using least-mean-square (LMS) adaptive filters are described for the 2-2-2 cascade example and the efficacy of these calibration techniques is compared.

5.2 Mismatch in the 2-2-2 Cascade Architecture

Like any cascade architecture, the 2-2-2 cascade is sensitive to component mismatch at the interstage nodes. Following a similar method to that in [43], the effects of mismatch in the interstage coefficients can be analyzed for the 2-2-2 cascade. To simplify the mathematics, it is assumed that the second interstage coupling network is perfect. With mismatch, (Eq 4-12) is modified for the first interstage node as shown in

(Eq 5-1), where δg_1 and $\delta\lambda_1$ represent mismatch in the interstage coefficients. It is then

$$X_2(z) = g_1(1+\delta g_1)\{[\lambda_1(1+\delta\lambda_1)-1]Y_1(z)+E_1(z)\} \qquad \text{(Eq 5-1)}$$

possible to combine the recombining network equations, modulator output equations, mismatch effects in (Eq 5-1) to calculate the overall modulator output. Neglecting higher-order differences, it follows that the modulator output Y(z) can be approximated as in (Eq 5-2). The key result from (Eq 5-2) is that a second-order noise-shaped term

$$Y(z) \approx z^{-6}X(z) + \frac{1}{g_1 g_2}(1-z^{-1})^6 E_3(z) - \delta g_1 (1-z^{-1})^2 z^{-4} E_1(z) \qquad \text{(Eq 5-2)}$$

related to the first stage quantization error leaks through to the output. Mismatch in λ_1 only appears in higher-order terms and is not as significant as mismatch in g_1.

Since the result in (Eq 5-2) is only approximate, system level simulations are required to accurately determine the degradation in dynamic range due to interstage coefficient mismatch in the 2-2-2 cascade architecture. For a target dynamic range of 92 dB, the simulations include all sources of error which degrade the quantization noise such as amplifier settling and slew rate which are discussed in Section 6.2. Table 5.1 summarizes the results. As expected, the dominant mismatch term is related to the first interstage gain coefficient g_1. Since g_1 depends on the product of three independent capacitor ratios as shown in Section 4.4, the constraint on g_1 is severe enough that it cannot be met by component matching in an integrated circuit fabrication process. Calibration as described in Section 5.3 will be required. Tolerances on the mismatch in λ_1 and λ_2 are large enough that errors in these coefficients will not cause significant

degradation in the overall modulator dynamic range. The tolerance on g_2 is such that careful layout should provide adequate matching.

Table 5.1:Interstage coefficient mismatch

Coefficient	Allowable Mismatch
g_1	0.25%
g_2	2.8%
λ_1	5%
λ_2	10%

5.3 Calibration Strategies

Calibration of the first interstage gain coefficient g_1 will be required since matching constraints are beyond the capabilities of integrated circuit fabrication processes. Calibration may be performed in either the analog domain with capacitor trim or in the digital domain with post-processing depending upon the architecture, application and calibration requirements. Calibration techniques for sigma-delta modulators have focussed almost exclusively on errors due to nonlinear multi-bit D/A converters. Techniques employed include least-mean-square (LMS) adaptive filters [44], dynamic element matching [45] auxiliary A/D converters and digital post-processing [46], and a combination of dynamic element matching and analog trim [47]. Analog trim has also been used to calibrate out interstage gain errors in a pipelined ADC [48]. Both analog trim and LMS digital filters are suitable for calibration of the interstage gain error in cascaded sigma-delta modulators. This section will describe the calibration techniques in the context of the 2-2-2 cascade example; however, the calibration strategies are applicable to interstage gain mismatch in any cascaded sigma-delta modulator.

5.3.1 Analog Trim

Analog trim simply adds small capacitors in parallel with the unit capacitor to calibrate out the effects of capacitor mismatch. As shown in Section 4.4, the first interstage gain coefficient depends on the product of three independent capacitor ratios. For example, assuming 1% matching between capacitors, the worst case mismatch in g_1 will be 3%. This implies that four bits of trim will be required for each capacitor to achieve 0.25% accuracy in g_1. Fig. 5.1 shows a generalized capacitive divider trim array based on a T network to achieve small trim capacitors [48]. In a calibration cycle, the trim bits could be adjusted with zero input to the modulator and the combination which minimizes the variance of the noise at the output of the decimation filter selected as the appropriate value. This will require a similar approach to the algorithm in [47]. In the RF baseband processing application for a cellular or cordless phone, calibration could be performed at call setup. If drift is a concern, recalibration could be performed during unused time slots in TDMA systems such as DECT or GSM.

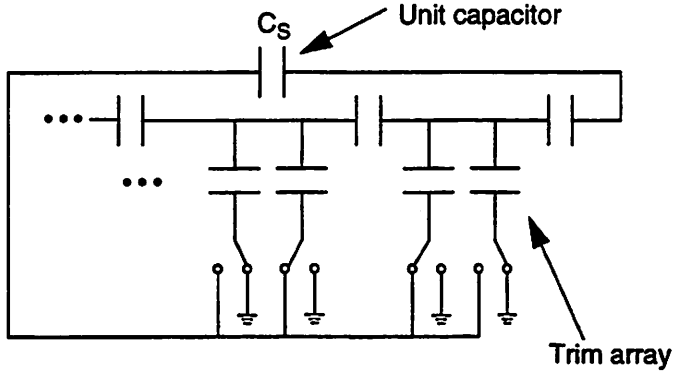

Fig. 5.1: Capacitive divider trim array

5.3.2 LMS Digital Calibration

Calibration of the interstage gain may be performed in the digital domain using an LMS adaptive filter as shown in Fig. 5.2. The combined outputs of the second and third stages of the modulator represent an estimate of the quantization error of the

first stage. A single tap LMS adaptive digital filter can find the minimum mean square error between the output of the first stage and the combined outputs of the second and third stages. The value of this tap that minimizes the mean square error will be the correct value to fully cancel the quantization error of the first stage of the modulator. Initial calibration can be performed by shorting the inputs of the modulator together and letting the filter adapt to the correct value. Calibration can be performed continuously during conversion by allowing the filter to adapt at a smaller step size or shut off if drift requirements allow.

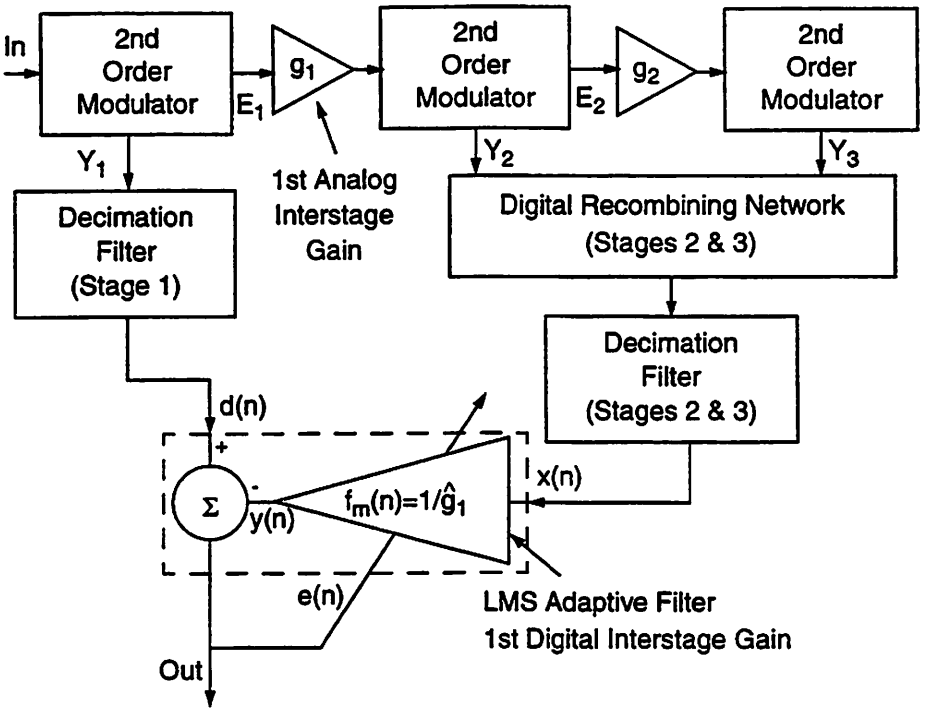

Fig. 5.2: Digital calibration using an LMS adaptive filter

To explain the calibration scheme in greater detail, it is necessary to describe the LMS algorithm for a single tap. Let $f_m(n)$ denote the single tap of an LMS adaptive filter at time m, d(n) denote the desired signal to be matched (output of the first stage in this case), x(n) denote the input to the filter (recombined output of the second and third stages) and y(n) denote the filter output as shown in Fig. 5.2. It

follows from a simple convolution that the output of the filter y(n) is given by (Eq 5-3).

$$y(n) = f_m(n)x(n) \qquad \text{(Eq 5-3)}$$

The error signal e(n) which is fed back to update the taps is the difference between the desired signal d(n) and the filter output y(n). The filter seeks to minimize $E[e^2(n)]$, the mean squared error of e(n). It can be shown that the mean square error will be minimized when (Eq 5-4) is satisfied. This makes sense at an intuitive level; when the

$$E[x(m-n)e(m)] = 0 \qquad \text{(Eq 5-4)}$$

filter adapts properly, all correlation is removed between the filter input representing the recombined outputs of the second and third stages of the modulator and the error signal which in this case represents the overall modulator output [49].

Now consider the LMS algorithm for updating the filter tap. The tap $f_m(n)$ is updated according to the algorithm in (Eq 5-5). β which represents an update step size

$$f_{m+1}(n) = f_m(n) + \beta x(m-n)e(m) \qquad \text{(Eq 5-5)}$$

must be small enough to keep the algorithm stable; the maximum allowable β depends on the statistics of the input signal. The second term in (Eq 5-5) will go to zero when the algorithm converges because it represents an estimate of the expression in (Eq 5-4). If the algorithm converges with appropriate choice of β, it can also be shown that there exists a single minimum value [49].

5.3.3 Comparison

Analog trim and digital calibration using an LMS adaptive filter need to be compared to see which is the appropriate technique for the RF baseband processing application. Analog trim has the disadvantage of changing the analog structure of the modulator which complicates routing of capacitor arrays in switched capacitor

integrators. Moreover careful attention must be paid to the layout of trim capacitor arrays. In addition, analog calibration cannot be performed while the sigma-delta is converting actual data; this is not a problem in TDMA systems as described above but could be a problem in direct sequence CDMA systems which are continuously receiving. Digital calibration with an LMS adaptive filter leaves the analog portions of the modulator unchanged and can be performed while the sigma-delta is converting actual data at a reduced step size. The big disadvantage is the use of parallel paths in the decimation filter which is estimated to increase the filter complexity by 1.5 X to 1.7 X depending on the particular filtering algorithm. This increase in complexity is accompanied by a corresponding increase in decimation filter power. If the decimation filter power is significantly smaller than the analog power in the modulator which should be the case for high-speed applications, then the overhead for digital calibration has little impact on the overall system. As a result, digital calibration using an LMS adaptive filter is the more attractive approach to meet the 14 bit 2 MS/s specification.

5.4 Summary

This chapter analyzed mismatch effects for the 2-2-2 cascade sigma-delta architecture. It was shown that the matching requirements at the first interstage gain node were beyond the capabilities of integrated circuit fabrication processes. This implied that calibration was required. Both analog trim and digital calibration using an LMS adaptive filter were proposed as possible techniques to compensate for mismatch. Furthermore, digital calibration using an LMS adaptive filter was shown to be the preferred technique because it may be performed in the background while the modulator is converting actual data and because it does not complicate critical analog portions of the modulator.

Chapter 6

Switched-Capacitor Integrator Design and Optimization

6.1 Introduction

Switched-capacitor integrators are the key circuit building block in a sigma-delta modulator. This chapter explores design tradeoffs and power optimization strategies for switched-capacitor integrators in the context of a high-speed sigma-delta modulator. The discussion begins with a review of how system level requirements such as dynamic range and sampling rate can be translated into a set of circuit level performance specifications for each integrator in the modulator. Given these circuit level specifications, choice of operational amplifier topology is investigated for the 2-2-2 cascade architecture described in Chapter 4. Once the amplifier topology is fixed, quantities such as dc gain, settling time, thermal noise and slew rate may be analyzed. The emphasis of this analysis is on design tradeoffs, power minimization, and robust implementation.

6.2 Integrator Specifications for Sigma-Delta Modulators

In a sigma-delta modulator, integrator performance is specified in terms of nonidealities which limit the overall modulator dynamic range and speed of operation. Parameters such as finite dc gain, linear settling and slew rate can raise the quantization noise floor or introduce distortion depending on the circumstances. The available swing at the output of the integrators sets the modulator overload level (peak input signal handling capability). Thermal noise introduced by the sampling process (kT/C) as well as by the amplifiers adds directly to the quantization noise to set the minimum detectable signal. The effect of each of these nonidealities on the overall modulator will be investigated and procedures will be described to specify integrator performance. The 2-2-2 cascade architecture from Chapter 4 will be used as an example to illustrate the limits of integrator nonidealities in more detail.

6.2.1 DC Gain

Finite amplifier dc gain can degrade both the distortion and noise performance of a sigma-delta modulator. Depending upon modulator architecture, either distortion or quantization noise enhancement will set a more severe constraint on amplifier dc gain. Third-order distortion due to nonlinearities in the amplifier dc transfer function over its output range sets one dc gain requirement on the first integrator in a sigma-delta converter. The noise-shaping of the loop relaxes this dc gain requirement for subsequent integrators. Since these nonlinearities are inversely related to the amplifier dc gain, the gain must be increased to the point that the overall modulator performance is not degraded. This dc gain specification is not particularly severe; a moderate dc gain of 60 dB is more than adequate for 16 bit performance [51]. It is also important to note that the distortion specification is relatively independent of architecture for a fixed dynamic range.

A second effect of finite amplifier dc gain is to change the positions of the poles in a switched-capacitor integrator. The block diagram of a switched-capacitor integrator with an amplifier of dc gain A is shown in Fig. 6.1. The diagram is single-ended for convenience but the results apply to fully-differential implementations. Charge conservation analysis in the z domain yields the integrator transfer function H(z) in (Eq 6-1).The effect of finite amplifier dc gain is to shift the pole H(z) slightly

$$H(z) = \frac{V_o(z)}{V_i(z)} = \frac{(C_S/C_F)z^{-1}}{1-(1-\varepsilon)z^{-1}} \qquad \text{(Eq 6-1)}$$

where

$$(1-\varepsilon) = \frac{1}{1+C_S/(AC_F)}$$

off of the unit circle. This pole shift known as leak will increase the quantization noise floor at baseband. In a single-loop modulator, this effect is less severe than distortion; a dc gain on the order of the oversampling ratio will make it negligible [32].

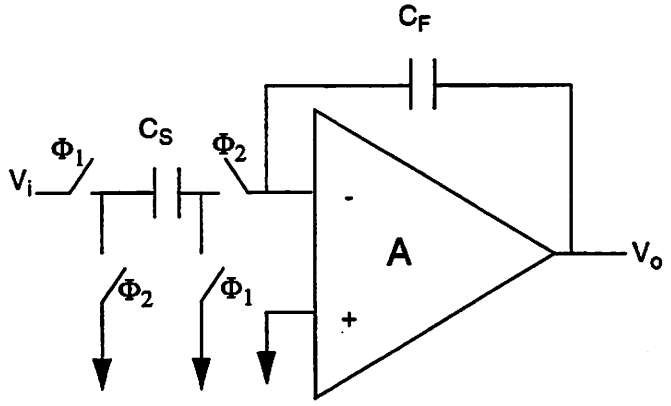

Fig. 6.1: Switched-capacitor integrator with finite amplifier dc gain

The effect of the integrator leak due to finite amplifier dc gain can be severe in cascaded sigma-delta modulators. Complete digital error cancellation requires that the integrator poles be at z=1; a shift in these poles will cause quantization noise from the first stage of the cascade to leak through to the output of the modulator. To

quantify this effect, consider the 2-2-2 cascade architecture described in Chapter 4 with the transfer function of the first modulator modified to include the effects of leak in (Eq 6-2) [30]. The symbols ε_1 and ε_2 in (Eq 6-2) refer to the dc gain error of the first and

$$Y_1(z) = z^{-2}X(z) + \left\{1 - [(1-\varepsilon_1) + (1-\varepsilon_2)]z^{-1} + (1-\varepsilon_1)(1-\varepsilon_2)z^{-2}\right\}E_1(z) \qquad \text{(Eq 6-2)}$$

second integrators in the cascade respectively and can be related to the dc gain by (Eq 6-1). If it is assumed that the second and third modulators in the cascade are ideal, then the overall transfer function of the 2-2-2 cascade will be as defined in (Eq 6-3). The key

$$\begin{aligned} Y(z) = {} & z^{-6}X(z) + [z^{-5}(1-z^{-1})(\varepsilon_1+\varepsilon_2) + z^{-6}\varepsilon_1\varepsilon_2]E_1(z) \\ & + \frac{1}{g_1 g_2}(1-z^{-1})^6 E_3(z) \end{aligned} \qquad \text{(Eq 6-3)}$$

result from (Eq 6-3) is that a first-order noise-shaped term related to the leak in the first two integrators $z^{-5}(1-z^{-1})(\varepsilon_1+\varepsilon_2)$ will appear at the output of the overall modulator. The other leak term in (Eq 6-3) is related to ε^2 which will be negligible compared to the first-order noise-shaped term. Unlike other specifications, the leak requirements are identical for the first and second integrators in the cascade.

The leak specification on dc gain will have an impact on the choice of operational amplifier topology in practical designs. Since ε_1 and ε_2 are very small for reasonable dc gains, it is difficult to calibrate out the leak effect. For a dc gain of 1000 and an integrator gain of 0.5, ε will be 5×10^{-4}. As a result, the solution is to design amplifiers with large enough dc gains that leak will have a negligible effect on the overall modulator performance. For the 2-2-2 cascade architecture with scaling in Section 4.4, system level simulations show that ε_1 of 7.69×10^{-5} and ε_2 of 1.92×10^{-4} are required to make the effect of integrator leak negligible (<1 dB) decrease in modulator dynamic range). This corresponds to equal dc gains of 2600 for the first two amplifiers in the cascade according to (Eq 6-1). The dc gain specification

of 2600 is large enough that a two-stage amplifier with dc gain related to $(g_m r_o)^3$ will be required. It is also important to note that the leak specification is more stringent than the distortion specification for the 2-2-2 cascade architecture.

6.2.2 Linear Settling and Slew Rate

Linear settling and slew rate specify the small signal and large signal speed performance of an integrator respectively. In a sigma-delta modulator, a linear settling error results in an integrator gain error while slew rate results in harmonic distortion [51]. In a cascade modulator, this gain error has the same effect as capacitor mismatch but can be made small enough to have negligible effect on the modulator quantization noise. Harmonic distortion due to amplifier slew rate can directly degrade the large signal performance of the modulator. The slew rate in each amplifier must be made large enough that the distortion introduced falls below the noise floor of the modulator. Due to the low g_m/I ratio of short channel CMOS devices and the required high speed operation, this distortion constraint will be satisfied if the amplifier slews for a small fraction of the settling period and spends the majority of its time in a linear settling regime.

To quantify the effect of slew rate and linear settling on a sigma-delta modulator requires system level simulation. The simulations assume a single pole operational amplifier characteristic with slew rate and employ the method described in [30]. This amplifier model is a significant oversimplification for a design which employs more complicated two-stage amplifiers; actual designs will have to leave significant margin from these results to ensure good performance. The plot in Fig. 6.2 shows peak SNDR as a function of various combinations of slew rate and linear settling accuracy for the first integrator for the 2-2-2 cascade modulator. Robust designs will operate in the flat area to the right of the characteristic where performance is independent of small shifts in the amplifier settling accuracy. In this region, the first

integrator settles to an accuracy of ten single pole time constants for a peak SNDR of 92 dB.

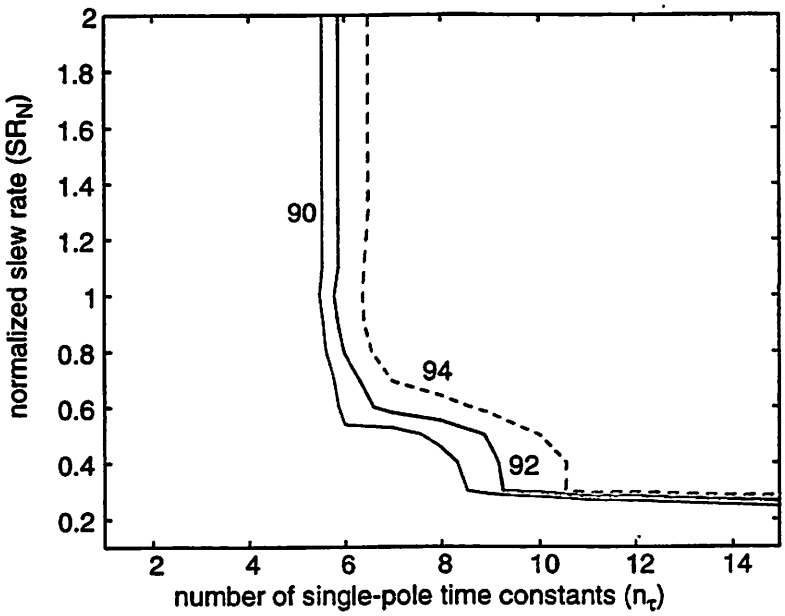

Fig. 6.2: Contours of peak SNDR as a function of slew rate and settling time (1st integrator)

It is necessary to convert the normalized simulation quantities in Fig. 6.2 to actual specifications on an amplifier. The settling error is denoted by ε_s in (Eq 6-4) and is usually specified as a percentage. This settling error is the deviation of the integrator output from the value it would achieve if the amplifier had an infinite amount of time to settle. The quantity n_τ in (Eq 6-4) is the required number of single pole time constants which is shown on the x-axis in Fig. 6.2 For implementations utilizing two-stage

$$\varepsilon_s = e^{-n_\tau} \qquad \text{(Eq 6-4)}$$

amplifiers, the constraint on ε_s should be satisfied by the more complicated multi-pole settling. The normalized slew rate (SR_N) on the y-axis in Fig. 6.2 may be converted to a physical slew rate specification by (Eq 6-5) where SR denotes the denormalized slew

rate, V_{MAX} the differential DAC reference levels, and T_S the available settling time. For

$$SR = \frac{2SR_N V_{MAX}}{T_S} \qquad \text{(Eq 6-5)}$$

the normalized results in Fig. 6.2 and a 92 dB peak SNDR, the first integrator should settle to ten single pole time constants with a normalized slew rate of 0.35. This corresponds to ε_s of 0.0045% or 14 bit accuracy according to (Eq 6-4). Denormalizing the slew rate for V_{MAX} = 1.8 V and a 32 MHz clock (T_s=15.625 ns per half cycle) yields a slew rate of 81 V/μs. Significant margins are required on the slew rate specification for designs employing two-stage compensated amplifiers because the slew rate is not accurately modeled at the behavioral level for this type of amplifier.

The simulations shown in Fig. 6.2 must be repeated for each integrator in the cascade. Requirements will be relaxed for subsequent integrators by the noise-shaping of the modulator as discussed in Section 4.5.

6.2.3 Output Swing

Output swing defines the maximum signal handling capability of an operational amplifier and is directly related to the modulator input overload level. Maximizing the output swing will increase the maximum signal handling capability of the modulator. For a kT/C noise limited design, this will minimize the required sampling capacitance and power dissipation as described in Chapter 4.

Output swing is ultimately limited by the power supply voltage, but in practical designs the swing will be lower due to the requirement that the output devices remain in saturation. The circuits in Fig. 6.3 represent the output stages of a two-stage amplifier. For an amplifier with cascoded devices at the output shown in Fig. 6.3(a), the output swing will be given by (Eq 6-6) while for the common source

configuration shown in Fig. 6.3(b), the output swing will be given by (Eq 6-7). In

$$V_{SWING} = V_{dd} - 2V_{dsat,n} - 2V_{dsat,p} \quad \text{(Eq 6-6)}$$

$$V_{SWING} = V_{dd} - V_{dsat,n} - V_{dsat,p} \quad \text{(Eq 6-7)}$$

traditional 5 V designs, output swing was not as critical as it is in designs using a 3.3 V or lower supply. Maximizing output swing favors the common source configuration if a two-stage amplifier is required. (Eq 6-7) suggests that $V_{dsat,n}$ and $V_{dsat,p}$ should be minimized. In practice, $V_{dsat,n}$ will need to be large enough to bias the NMOS device at sufficient f_t that settling requirements can be met. $V_{dsat,p}$ will need to be large enough that the device parasitics do not appreciably load the amplifier output. As a result, output swing will trade-off with amplifier settling requirements.

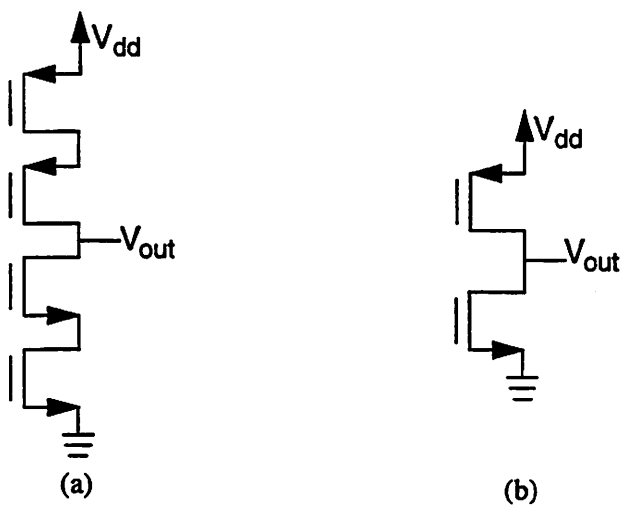

Fig. 6.3: Operational amplifier output configurations (a) cascoded and (b) common source

Output swing will have a significant impact on the 2-2-2 cascade modulator. For the scaling in Section 4.4, the amplifier output swing will be equal to the DAC reference levels which set the full-scale voltage of the sigma-delta modulator. Since the modulator input overload level is approximately 2 dB below the full scale, output swing

will directly set the modulator peak input signal handling capability. To maximize this peak signal handling capability especially given the 3.3 V power supply, an amplifier with common source output configuration should be employed.

6.2.4 Thermal Noise

Thermal noise places fundamental limits on the power dissipation and dynamic range of a switched-capacitor integrator as described in Section 3.5. While capacitor scaling discussed in Section 4.5 can reduce the effect of thermal noise on power dissipation of later integrators in the cascade, reducing the thermal noise contribution at the integrator design level can result in significant power savings. To meet a given dynamic range specification, a sigma-delta modulator must satisfy (Eq 6-8), where $S_{N,TH}$ denotes the total inband input referred thermal noise from (Eq 4-30), $S_{N,Q}$ denotes the quantization noise and $S_{N,1/f}$ denotes the input referred 1/f noise.

$$DR = \frac{V_{in,max}^2}{2(S_{N,TH} + S_{N,Q} + S_{N,1/f})} \qquad \text{(Eq 6-8)}$$

The 2-2-2 cascade architecture is required to achieve 14 bit resolution at 2 MS/s Nyquist rate and 16 X oversampling ratio. The wide input bandwidth relaxes the 1/f noise constraints as compared to lower frequency modulators. With careful circuit design, 1/f noise can be made low enough that it does not significantly degrade the modulator performance. As a result, the designer should trade off quantization and thermal noise to minimize power dissipation. If more thermal noise can be tolerated, smaller integrator sampling capacitors can be used. This in turn reduces the power dissipation in the integrator for a fixed settling requirement. Therefore, the sigma-delta architecture should place the quantization noise including all error sources below the thermal noise to achieve a low-power solution. A good rule of thumb is to make the dynamic range of the modulator excluding thermal noise to be at least one bit (6 dB) larger than the overall dynamic range specification. This makes the thermal noise contribution at least 3 X the contribution of the quantization noise.

Once the total thermal noise requirements are calculated, the capacitor scaling in (Eq 4-30) specifies the required sampling capacitance at each integrator input. To reduce the size of this capacitance, the designer needs to minimize the effect of thermal noise coming from devices in the amplifier rather than kT/C. This amounts to selecting an operational amplifier topology with the minimum number of devices contributing thermal noise as will be described in Section 6.3 and selecting device bias points and the compensation capacitor appropriately as will be described in Section 6.4.

6.3 Operational Amplifier Topology Selection

The integrator nonidealities and specifications discussed in Section 6.2 can be used to select an appropriate circuit topology for the operational amplifiers used in the 2-2-2 cascade modulator. The overriding goal is to select a topology which can meet the integrator performance requirements at minimum power dissipation. The discussion in this section will summarize the required characteristics of an operational amplifier for the 2-2-2 cascade architecture and propose various candidate topologies which could meet the requirements. Then, the desired characteristics to reduce power dissipation in the operational amplifier are reviewed which leads to the choice of an appropriate topology from the candidates.

6.3.1 Operational Amplifier Requirements

The operational amplifier requirements are most stringent for the first integrator in the cascade. Leak of first stage quantization noise demands an operational amplifier topology with dc gain of greater than 2600. This corresponds to a gain on the order of $(g_m r_o)^3$ and requires the use of a two-stage or three-stage nested-Miller amplifier. The amplifier must be able to settle to 0.0045% accuracy when clocked at 32 MHz. This precludes the use of nested-Miller topologies which are significantly slower

than two-stage amplifiers [52]. Amplifier thermal noise and kT/C noise must be small enough to achieve 14 bit resolution. The amplifier must also have adequate output swing and headroom in the first stage for 3.3 V operation. Output swing favors topologies with a common source second stage.

6.3.2 Candidate Operational Amplifier Topologies

Any two-stage amplifier with common source second stage and cascoded first stage can meet the specifications discussed in the previous section. Four candidate topologies are shown in Fig. 6.4 - Fig. 6.7. The topologies differ in the type of compensation employed either standard Miller [41] or cascode compensation [53], [54], [55]. The topologies also differ in whether the first stage of the amplifier is a folded-cascode or telescopic topology. If the first stage is a telescopic topology, then the common-mode voltage at the output of the first stage is not the same as the dc bias point required at the second stage input. As a result, a switched-capacitor dynamic level-shift is provided between the two stages of the amplifiers in Fig. 6.5 and Fig. 6.7 to independently set the first stage output common-mode level and second stage input dc bias. The level-shift is biased in identical manner to a switched-capacitor common-mode feedback circuit.

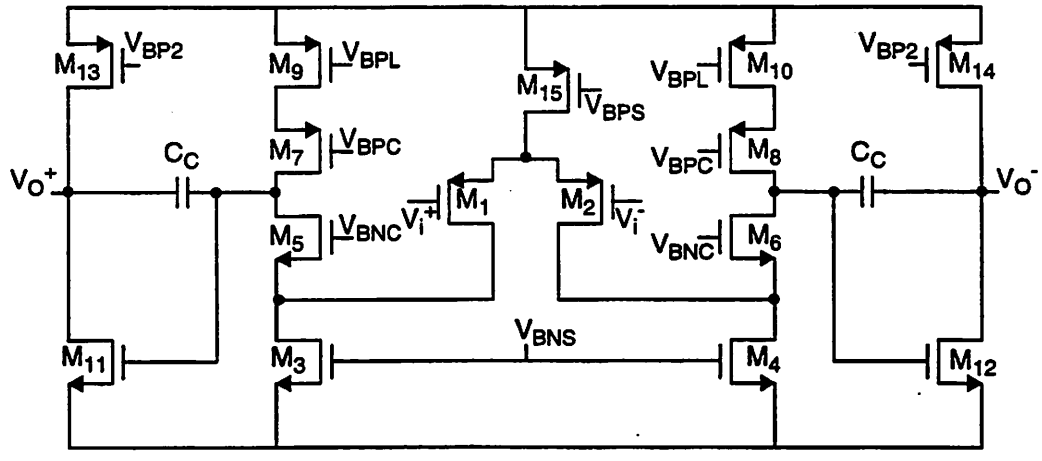

Fig. 6.4: Two-stage Miller compensated operational amplifier with folded first-stage

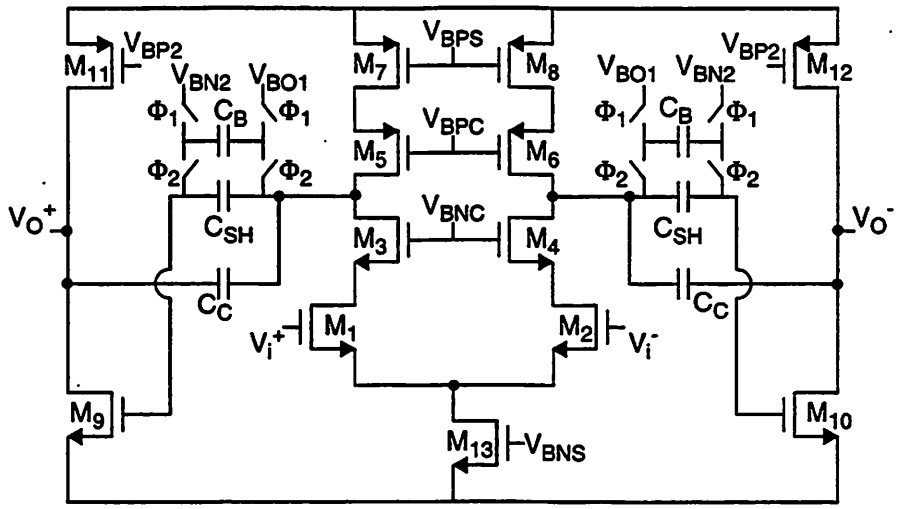

Fig. 6.5: Two-stage Miller compensated operational amplifier with dynamic level-shift

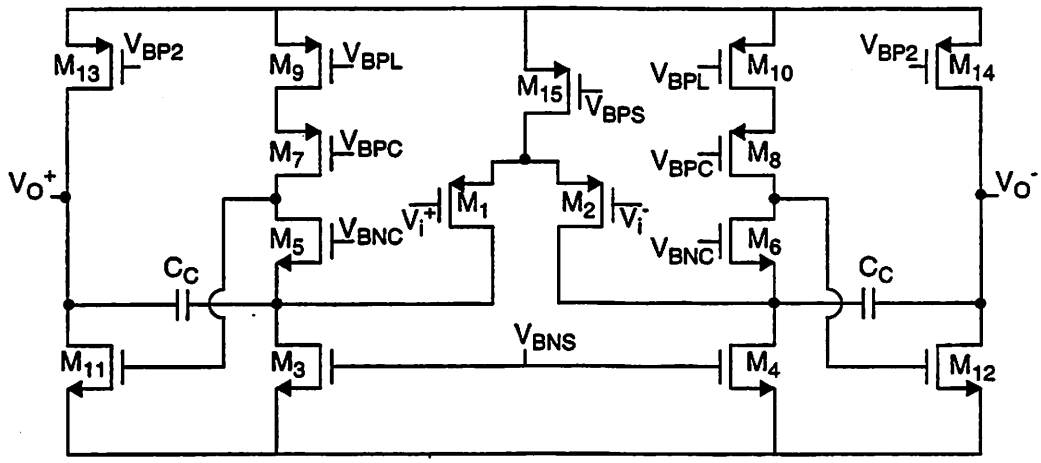

Fig. 6.6: Two-stage cascode compensated operational amplifier with folded first-stage

6.3.3 Low-Power Operational Amplifier Characteristics

The objective is to select the lowest power operational amplifier topology from the candidates in Fig. 6.4 - Fig. 6.7 by investigating desirable characteristic for low-power operation. Such desirable characteristics are: 1) minimum number of current legs, 2) minimum number of devices which contribute significant thermal noise, 3) all NMOS signal path for maximum speed, and 4) a maximum bandwidth compensation loop.

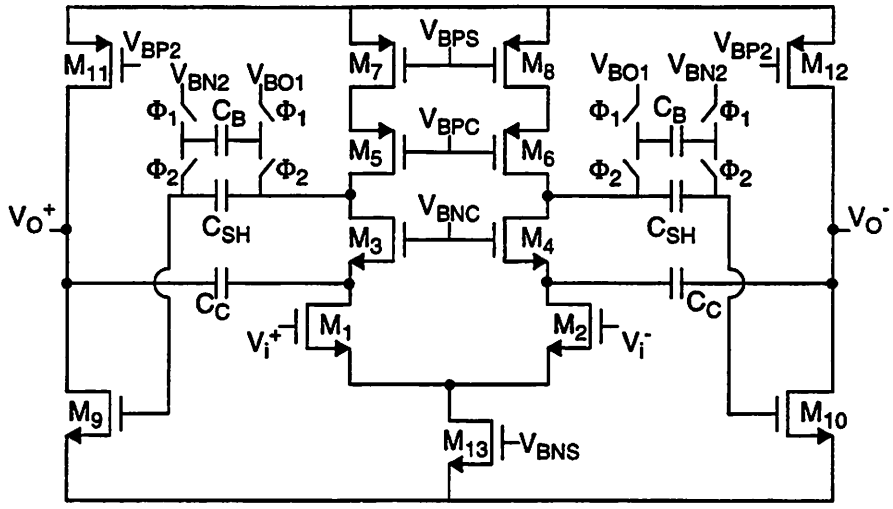

Fig. 6.7: Two-stage cascode compensated operational amplifier with dynamic level-shift

Since minimizing power dissipation amounts to minimizing the static bias current, one obvious approach is to minimize the number of current legs in an amplifier. For a fixed settling constraint and compensation scheme in the candidate two-stage amplifiers, an amplifier with fewer current legs will be lower power than an amplifier with more current legs. For a fully-differential two-stage amplifier, the minimum number of current legs is four. The amplifiers in Fig. 6.5 and Fig. 6.7 with telescopic first stage and dynamic level-shift meet this constraint. Folding the first stage of the amplifier as in Fig. 6.4 and Fig. 6.6 increases the number of current legs to six. Thus, minimizing the number of current legs favors topologies with a telescopic front-end and dynamic level-shift.

Since power and noise directly trade off, minimizing the number of devices in the amplifier which contribute thermal noise will reduce power dissipation. In a properly designed two-stage amplifier, thermal noise will be dominated by the first stage of the amplifier since the second stage noise will be attenuated by the first stage gain when referred to the input. For the dynamic-level shift amplifiers in Fig. 6.5 and Fig. 6.7, four devices (M_1, M_2, M_7 and M_8) contribute significant amplifier thermal

noise. This corresponds to an input device and active load device for each side of the fully-differential amplifier, the minimum number of devices for such a topology. The folded-cascode input stage topologies in Fig. 6.4 and Fig. 6.6 have six devices (M_1, M_2, M_3, M_4, M_9 and M_{10}) which contribute significant amplifier thermal noise. As a result, the topologies with telescopic first stage and dynamic level-shift minimize the number of devices which contribute significant amplifier thermal noise.

NMOS devices are approximately 3 X faster than PMOS devices due to the difference between the mobilities of electrons and holes. As a result, amplifiers with all NMOS signal paths will be higher speed than amplifiers with PMOS devices in the signal path. Since speed and power directly trade off, a higher speed amplifier will dissipate less power for a fixed settling constraint. The dynamic level-shift amplifiers in Fig. 6.5 and Fig. 6.7 have all NMOS devices (M_1, M_2, M_3, M_4, M_9 and M_{10}) in their signal paths while the folded-cascode input stage amplifiers in Fig. 6.4 and Fig. 6.6 have PMOS input devices. Note that the amplifiers with PMOS inputs will have the advantage of reduced 1/f noise which is especially important for low-frequency applications. However, the relaxed 1/f noise constraints due to the 1 MHz bandwidth of the 2-2-2 cascade modulator can be met with NMOS input amplifiers. Thus, the higher-speed of the dynamic level-shift amplifiers will result in a lower power solution.

Some form of compensation is required to maintain stability in a two-stage amplifier placed inside the feedback loop of a switched-capacitor integrator. The standard Miller compensation scheme places a pole-splitting capacitor between the output of the overall amplifier and the output of the first stage of the amplifier as shown in Fig. 6.4 and Fig. 6.5. This has the effect of creating a dominant low frequency pole and moving the second pole to a higher frequency which will ensure amplifier stability when it is placed in a feedback loop. On the other hand, the cascode compensation scheme shown in Fig. 6.6 and Fig. 6.7 creates a dominant pole and two

complex poles at higher frequency by placing a compensation capacitor between the amplifier output and first stage cascode node. This will also ensure amplifier stability when it is placed in a feedback loop. While both compensation schemes ensure stability, the cascode compensation scheme increases the speed of the amplifier as compared to the conventional Miller compensation scheme [52], [56]. Since higher speed amplifier topologies will achieve lower power dissipation under a fixed settling constraint, the cascode compensation scheme is preferred.

6.3.4 Operational Amplifier for the 2-2-2 Cascade Sigma-Delta Modulator

The amplifier topology in Fig. 6.7 with telescopic front-end, dynamic switched-capacitor level-shift and cascode compensation is the best of the candidate topologies in Section 6.3.3 from a power dissipation perspective. This topology satisfies the four desirable characteristics for low-power operation: minimum number of current legs, minimum number of noise contributing devices, all NMOS signal path, and maximum bandwidth compensation loop. As a result, the operational amplifier in Fig. 6.7 was selected for use in the 2-2-2 cascade sigma-delta modulator.

6.4 Amplifier Design and Power Optimization

This section develops design procedures and power-optimization strategies for the operational amplifier topology in Fig. 6.7. The approach is to provide design equations which illustrate trade-offs when picking device sizes and bias points with emphasis on minimizing power dissipation and providing robust implementations. Design equations for dc gain, small-signal frequency response, step-response, thermal noise and slew rate are derived. Since the cascode compensation scheme creates an amplifier with three closed-loop poles, the design equations become significantly more

complicated than for a single-stage or conventional Miller compensated two-stage amplifier. This implies that for practical designs some form of computer optimization constrained by the trade-offs illustrated in the design equations will be necessary. Such procedures are explored in detail in [52] and a similar procedure will be outlined in Section 6.4.6.

6.4.1 DC Gain

A small-signal half circuit model which can be used to calculate the amplifier dc gain is shown in Fig. 6.8. The model neglects all capacitances which only affect the amplifier frequency response; a capacitive divider between the level-shift capacitor and gate capacitor at the input of the second stage will reduce the dc gain and must be included. From small-signal analysis, it can be shown that the dc gain of the amplifier is given by (Eq 6-9). As expected, the gain is on the order of $(g_m r_o)^3$.

$$A_{dc} = g_{m1}g_{m9}[r_{o1}(1+g_{m3}r_{o3}) \parallel r_{o5}(1+g_{m5}r_{o7})](r_{o9} \parallel r_{o11})\left(\frac{C_{sh}}{C_{sh}+C_{g9}}\right) \quad \text{(Eq 6-9)}$$

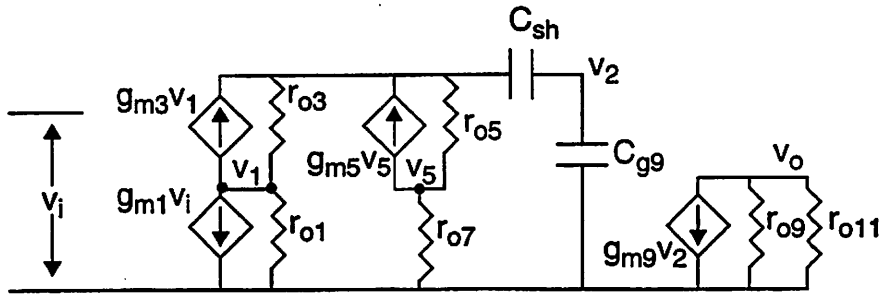

Fig. 6.8: Small-signal model for dc gain calculations

The dc gain in (Eq 6-9) provides a starting point for sizing certain devices in the amplifier. The capacitive divider between C_{sh} and C_{g9} implies that C_{sh} must be much larger than C_{g9} to avoid significant reduction in dc gain. For a ten percent gain reduction, which should be acceptable in most cases, C_{sh} needs to be nine times as large as C_{g9}.

To provide adequate margin for process variations and assure that the leak specification is met, it is desirable to maximize the amplifier dc gain. Dc gain is maximized when it is limited by the NMOS devices in the signal path. In the first stage of the amplifier, this implies that the output resistance of the PMOS active load should be made much larger than the output resistance of the NMOS input and cascode device as given in (Eq 6-10). Since M_7 and M_8 in Fig. 6.7 do not capacitively

$$r_{o5}(1 + g_{m5}r_{o7}) \gg r_{o1}(1 + g_{m3}r_{o3}) \qquad \text{(Eq 6-10)}$$

load the signal path, these devices can be made long channel to maximize r_{o7} in dc gain equation (Eq 6-10). If this is still not sufficient to satisfy (Eq 6-10), M_5 and M_6, the PMOS cascode devices, in Fig. 6.7 can be increased in channel length. Since the output capacitance of these devices loads the output of the first stage of the amplifier, speed and dc gain will trade off through the channel length of the cascode devices.

Dc gain of the second stage of the amplifier is maximized when it is limited by the NMOS devices M_9 and M_{10} in Fig. 6.7. An additional constraint is that the second stage gain needs to be large enough that the first stage devices will remain in saturation for the worst case output swing and process corner. Practically, this implies that the PMOS current source loads M_{11} and M_{12} in Fig. 6.7 will need to be increased from the minimum channel length. Since the output capacitance of M_{11} and M_{12} directly loads the output of the amplifier, speed and dc gain will also trade off through the channel length of these PMOS devices.

6.4.2 Frequency Response

The small-signal closed-loop frequency response is a measure of amplifier speed capability. This frequency response may be calculated using the half-circuit model in Fig. 6.9. Note that device output resistances are assumed to be infinite to

simplify the analysis. The effect of finite resistance is to move the amplifier poles slightly to the left which will slightly increase the bandwidth of the amplifier [52].

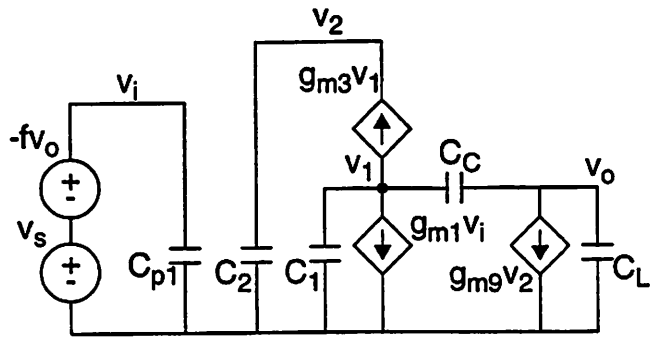

Fig. 6.9: Small-signal model for frequency response calculation

To begin the analysis both the feedback factor (f) and the various capacitances in Fig. 6.9 need to be defined in terms of physical device parameters. The amplifier feedback factor is the same as defined in (Eq 3-22) and is restated here as (Eq 6-11) for the notation used in this section. The model of transistors assumes that the

$$f = \frac{C_F}{C_F + C_S + C_{p1}} \qquad \text{(Eq 6-11)}$$

source and drain capacitances are proportional to the gate capacitance through a process specific constant α which differs for NMOS and PMOS devices. Capacitors must include the parasitic bottom-plate capacitance to ground which is related to the physical capacitance through a constant α_c. Given these definitions, the capacitances in

Fig. 6.9 are as shown in (Eq 6-12) - (Eq 6-15). The quantity C_{psw} in (Eq 6-12) refers to

$$C_{p1} = C_{g1} + C_{psw} \tag{Eq 6-12}$$

$$C_1 = \alpha_N C_{g1} + C_{g3} + \alpha_N C_{g3} \tag{Eq 6-13}$$

$$C_2 = \alpha_N C_{g3} + \alpha_P C_{g5} + \alpha_C (C_{sh} + C_b) + C_{g9} \tag{Eq 6-14}$$

$$C_L = \alpha_N C_{g9} + \alpha_P C_{g11} + \alpha_C (C_F + C_C) + C_{LE} + C_F (1 - f) \tag{Eq 6-15}$$

the parasitic capacitance due to the transfer switches at the summing node of the amplifier. The quantity C_{LE} in (Eq 6-15) refers to any external load capacitance which includes the parasitics due to the next stage switches, the capacitance used for sensing in the common-mode feedback loop and possibly comparator input capacitance depending upon which integrator is being analyzed.

From an analysis of the small-signal model in Fig. 6.9, it can be shown that the amplifier transfer function denoted by H(s) is given by (Eq 6-16) where C_T^2 is given by (Eq 6-17) [52]. The transfer function includes two zeros and three poles as shown in

$$H(s) = \frac{\frac{g_{m1}}{C_2 C_T^2}(g_{m3}g_{m9} - C_2 C_C s^2)}{s^3 + \left[\frac{g_{m3}(C_L + C_C) - f g_{m1} C_C}{C_T^2}\right] s^2 + \frac{g_{m3}g_{m9}C_C}{C_2 C_T^2} s + \frac{f g_{m1} g_{m3} g_{m9}}{C_2 C_T^2}} \tag{Eq 6-16}$$

$$C_T^2 = C_1 C_L + C_1 C_C + C_L C_C \tag{Eq 6-17}$$

Fig. 6.10. There are two off-axis complex poles with natural frequency ω_n and damping factor ζ. The damping factor ζ sets the stability of the amplifier; ζ falls between zero and one with zero being poles on the imaginary axis and one being poles on the real axis. The location of the on-axis pole is normalized through a constant α to the real part

of the complex poles. Depending on the choice of device parameters, the on-axis pole may either be closer to the jω axis ($\alpha < 1$) or further from the jω axis ($\alpha > 1$) than the complex poles. Since there are both left and right half-plane zeros at equal frequencies given by (Eq 6-18), the zeros do not degrade the amplifier phase margin. In practical

$$z = \pm\sqrt{\frac{g_{m3}g_{m9}}{C_2C_C}} \qquad \text{(Eq 6-18)}$$

designs, the zeros will also be at significantly higher frequencies than the poles and can be neglected in most analysis of the amplifier.

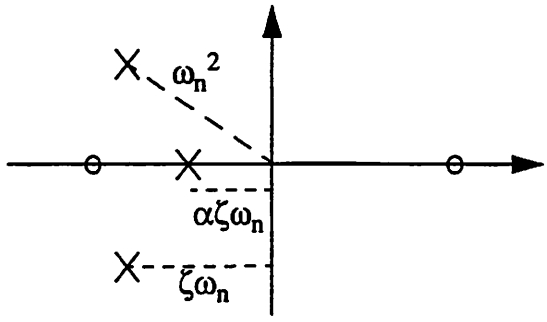

Fig. 6.10: Closed-loop pole-zero plot

The poles in Fig. 6.10 follow the characteristic polynomial D(s) in (Eq 6-19) with the normalization of the on-axis pole location in the second form. By equating

$$\begin{aligned} D(s) &= (s+\omega_{cl})(s^2+2\zeta\omega_n s+\omega_n^2) \\ &= (s+\alpha\zeta\omega_n)(s^2+2\zeta\omega_n s+\omega_n^2) \end{aligned} \qquad \text{(Eq 6-19)}$$

terms in s of the characteristic polynomial in (Eq 6-19) with the denominator of the transfer function in (Eq 6-16), the pole parameters such as natural frequency and

damping factor can be related to the physical device parameters as shown in (Eq 6-20) - (Eq 6-22) [52].

$$(2+\alpha)\zeta\omega_n = \frac{g_{m3}(C_L + C_C) - fg_{m1}C_C}{C_T^2} \quad \text{(Eq 6-20)}$$

$$\omega_n^2(1+2\alpha\zeta^2) = \frac{g_{m3}g_{m9}C_C}{C_2C_T^2} \quad \text{(Eq 6-21)}$$

$$\alpha\zeta\omega_n^3 = \frac{fg_{m1}g_{m3}g_{m9}}{C_2C_T^2} \quad \text{(Eq 6-22)}$$

The relationships expressed in (Eq 6-20) - (Eq 6-22) serve as the basic small signal design equations for the amplifier. These equations show that both amplifier stability and bandwidth are complicated functions of capacitances and transconductances in the circuit. However, some rules of thumb about relative values of the device parameters can be obtained. If the product $\zeta\omega_n$ is maximized, an amplifier with good stability and bandwidth can be obtained. Looking more carefully at (Eq 6-20), $\zeta\omega_n$ will be maximized if (Eq 6-23) is satisfied.

$$g_{m3} \gg fg_{m1} \quad \text{(Eq 6-23)}$$

Since the cascode devices (M_3 and M_4) in Fig. 6.7 run at the same current as the input devices (M_1 and M_2) and g_m obeys the relationship in (Eq 6-24), the cascode devices must be biased at significantly lower V_{GS}-V_T than the input devices to satisfy (Eq 6-23). Note that as the V_{GS}-V_T of the cascode devices is reduced, these devices will

$$g_m = \frac{2I_d}{V_{GS} - V_T} \quad \text{(Eq 6-24)}$$

contribute more parasitic capacitance which will reduce the amplifier bandwidth. This implies that there will be an optimal value of V_{GS}-V_T for the cascode devices which

satisfies (Eq 6-23) without contributing excessive capacitance; this value can be found through the computer optimization procedure that will be described in Section 6.4.6.

Maximizing the transconductance of the cascode devices is consistent with the open loop stability analysis of this type of amplifier in [55]. The open loop analysis shows that there will be a dominant low frequency on-axis pole and two high frequency complex poles. The complex poles are characterized by a natural frequency ω_{ol} and a quality factor Q_{ol} which can be approximated as in (Eq 6-25) and (Eq 6-26) respectively [55]. If these open loop poles have too high of Q, there will be peaking in the amplifier

$$\omega_{ol} \approx \sqrt{\frac{g_{m3}g_{m9}}{C_2C_L}} \qquad \text{(Eq 6-25)}$$

$$Q_{ol} \approx \frac{C_C}{C_L + C_C}\sqrt{\frac{g_{m9}C_L}{g_{m3}C_2}} \qquad \text{(Eq 6-26)}$$

open loop gain response beyond the amplifier unity gain bandwidth. This corresponds to an amplifier with inadequate gain margin and results in an inadequate closed-loop damping factor ζ [55]. Since Q_{ol} is inversely related to the transconductance of the cascode devices (g_{m3}) while ω_{ol} is directly related to this transconductance, a design approach which achieves good stability without sacrificing bandwidth will maximize the transconductance of the cascode devices.

6.4.3 Linear Settling

In a switched-capacitor integrator, the step response determines the amplifier linear settling performance in the time domain. In Section 6.2.2, settling error was one of the parameters used to relate integrator performance to the modulator system-level performance. Since the settling error is a measure of the deviation of the step response from the value it would attain if there were infinite time to settle, the step response must be derived first. A detailed derivation is shown in Appendix 2 with the resulting

step response s(t) in (Eq 6-27). As expected, the step response consists of an

$$s(t) = A_{cl}\left\{1 - \frac{1}{(1-2\alpha\zeta^2+\alpha^2\zeta^2)}e^{-\alpha\zeta\omega_n t} - \frac{\alpha\zeta e^{-\zeta\omega_n t}}{(1-2\alpha\zeta^2+\alpha^2\zeta^2)}\left[(-2\zeta+\alpha\zeta)\cos\left(\omega_n t\sqrt{1-\zeta^2}\right) + \frac{(1-2\zeta^2+\alpha\zeta^2)}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right]\right\} \quad \text{(Eq 6-27)}$$

exponentially decaying term related to the on-axis pole and a damped oscillatory term related to the complex poles. If an infinite amount of time were available for settling, the integrator output would simply be the closed loop gain A_{CL} multiplied by the input step.

The settling error in percentage form at a particular time t_s may be derived from the step response by (Eq 6-28). The resulting settling error ε_s in (Eq 6-29) is a

$$\varepsilon_s = \frac{s(\infty) - s(t_s)}{s(\infty)} \quad \text{(Eq 6-28)}$$

complicated function of the integrator closed-loop pole position parameters (α, ζ, ω_n).

$$\varepsilon_s = \frac{1}{(1-2\alpha\zeta^2+\alpha^2\zeta^2)}e^{-\alpha\zeta\omega_n t_s} + \frac{\alpha\zeta e^{-\zeta\omega_n t_s}}{(1-2\alpha\zeta^2+\alpha^2\zeta^2)}\left[(-2\zeta+\alpha\zeta)\cos\left(\omega_n t_s\sqrt{1-\zeta^2}\right) + \frac{(1-2\zeta^2+\alpha\zeta^2)}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t_s\sqrt{1-\zeta^2}\right)\right] \quad \text{(Eq 6-29)}$$

As a result, it is not immediately obvious how these parameters should be selected to optimize the settling error.

To get a clearer idea of how to place the integrator closed-loop poles, a graphical approach is employed. To begin, note that t_s in (Eq 6-29) is fixed at the system level; it will equal one half clock period less the time required for clock

nonoverlap, rise, and fall times. Since ω_n is a measure of the overall bandwidth, the normalized quantity $\omega_n t_s$ may be used to derive pole positions which are independent of the clock frequency. The plot in Fig. 6.11 shows settling error as a function of $\omega_n t_s$ for varying damping factor ζ and fixed on-axis pole location $\alpha = 1$ (real parts of the poles lined up).

For a given error level, the optimal value of ζ will be the one which minimizes $\omega_n t_s$ resulting in the narrowest required bandwidth. An optimal ζ exists because the oscillatory term in (Eq 6-29) will speed up settling in regions where it is of the same sign as the exponential term and slow down settling in regions where it is of opposite sign. Since the frequency of the oscillatory term is inversely related to ζ, ζ will directly control the sign of the oscillatory term. This is seen in Fig. 6.11 where a region of fast settling (high slope) is followed by a region of slow settling (an inflection point). Note that in the high slope region, the slope is inversely related to ζ and that the amplifier will not overshoot for $\alpha \leq 1$. Since settling in the high slope region is faster, this implies that the optimal ζ is selected such that the inflection point is placed at the desired settling error level and that ζ should be made smaller as settling constraints are relaxed. For example, according to Fig. 6.11, the optimal value of ζ for 14 bit settling ($\varepsilon_s = 6 \times 10^{-5}$) is 0.85 while the optimal value for 12 bit settling ($\varepsilon_s = 2.4 \times 10^{-4}$) is 0.8.

The plot in Fig. 6.12 shows settling error as a function of $\omega_n t_s$ for varying on-axis pole location α and fixed damping factor ζ=0.85. Decreasing α moves the on-axis pole closer to the origin than the complex poles which results in settling error that looks more like a single-pole response. On the other hand, by the time α reaches 1.1, the step response includes significant overshoot which is evident in the notches in the settling error in Fig. 6.12. For the 14 bit settling example, α=1 minimizes $\omega_n t_s$ according to Fig. 6.12.

In a robust design, the integrator settling performance must be insensitive to shifts in the amplifier pole positions. These pole positions are not well controlled

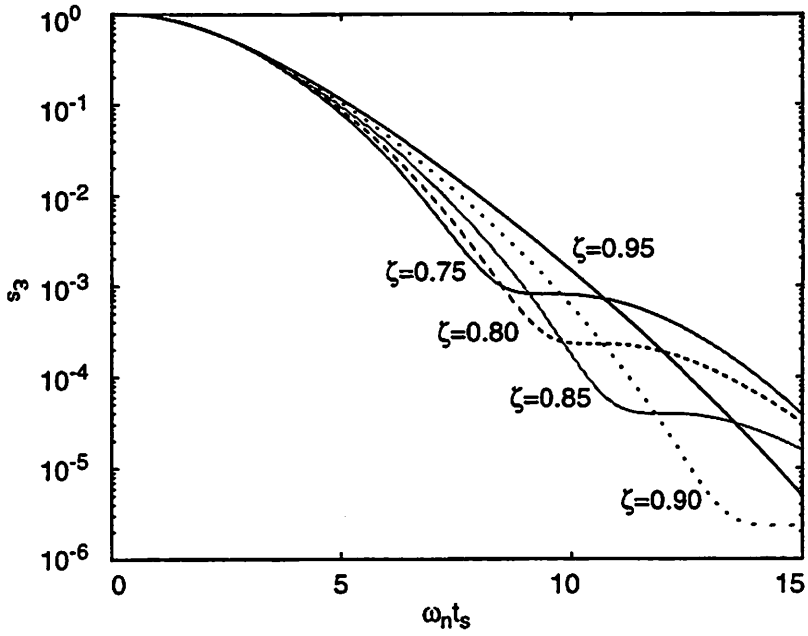

Fig. 6.11: Settling error as a function of $\omega_n t_s$ (varying ζ, α =1)

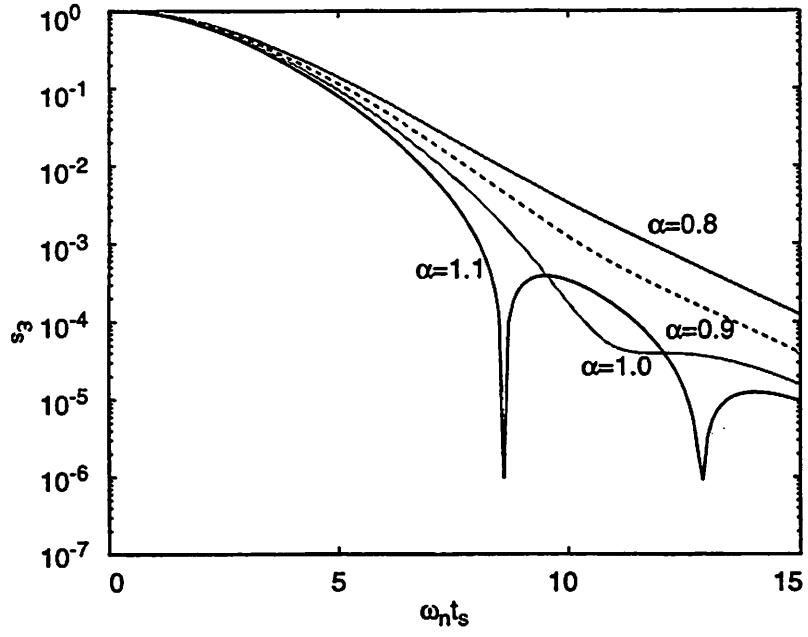

Fig. 6.12: Settling error as a function of $\omega_n t_s$ (varying α, ζ = 0.85)

due to process variations in capacitances and device transconductances. For the α=1 case, the settling error is fairly sensitive to shifts in ζ as can be seen in Fig. 6.11 and is

also somewhat sensitive to shifts in α as can be seen in Fig. 6.12. These plots also show that the sensitivity to pole shifts increases as the settling requirements become more stringent. If α is reduced to 0.9, the sensitivity to changes in ζ is greatly reduced as can be seen in Fig. 6.13. The sensitivity to variations in α is also reduced for α=0.9 as can be seen in Fig. 6.12.

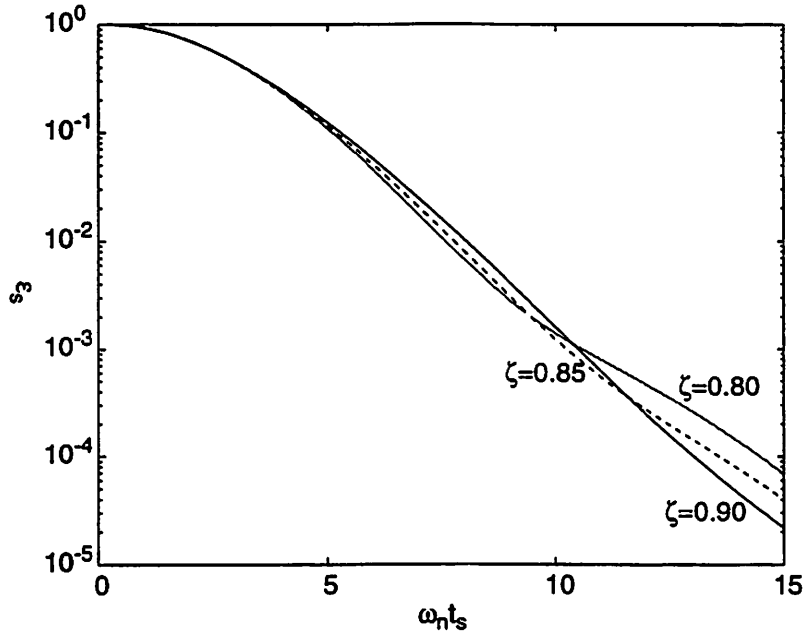

Fig. 6.13: Settling error as a function of $\omega_n t_s$ (varying ζ, α= 0.9)

It makes intuitive sense that the amplifier would be less sensitive to changes in the pole positions as α is decreased because the step response becomes more like a single pole response. This represents a trade-off between optimal linear settling which minimizes $\omega_n t_s$ and robust design because decreasing α increases the required $\omega_n t_s$. A good compromise is to set α in the range of 0.8 to 0.9 which results in less sensitivity to the pole positions but does not excessively increase the amplifier bandwidth and cost too much power.

6.4.4 Thermal Noise

Thermal noise adds directly to quantization noise to set the noise floor for a sigma-delta modulator as described in Section 6.2.4. The total input referred thermal noise of the overall modulator is set by the capacitor scaling equation (Eq 4-30) which specifies the input referred noise of the i-th integrator as per (Eq 4-29) (restated here as (Eq 6-30)). The goals of this section are to show how to calculate the constants γ_i given

$$S_{Ni} = \frac{\gamma_i kT}{C_{Si}} \qquad \text{(Eq 6-30)}$$

the amplifier topology in Fig. 6.7 and how to design the amplifier to minimize its noise contribution.

The analysis begins by considering the idealized case of a fully-differential switched-capacitor integrator with a noiseless infinite bandwidth operational amplifier in Fig. 6.14. On the sampling phase, the switches labeled Φ_1 are closed and the amplifier is out of the circuit. If the input is an ideal voltage source, a noise sample with variance $2kT/C_S$ (kT/C_S on each of the differential sampling capacitors) will be taken when the Φ_1 switches open. On the transfer phase, the switches labeled Φ_2 are closed and charge is moved from the sampling capacitors (C_S) to the feedback capacitors (C_F). Since the amplifier is assumed to be ideal, another input referred $2kT/C_S$ noise sample is taken when the transfer switches open [57]. As a result, the input referred thermal noise of a switched-capacitor integrator under these idealized conditions is $4kT/C_S$. Practical amplifiers usually yield an increase in noise from this idealized case; the design goal is to keep γ_i for a practical fully-differential switched-capacitor integrator as close to four as possible.

The next step is to analyze the output noise which results from the operational amplifier in Fig. 6.7 to illustrate design trade-offs. The small-signal model in Fig. 6.15 may be used to calculate the total output noise of the operational amplifier.

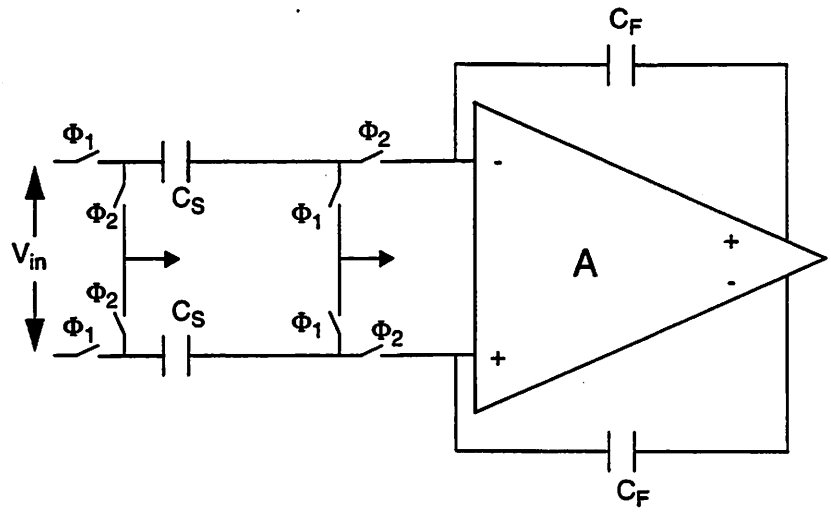

Fig. 6.14: Fully-differential switched-capacitor integrator with noiseless amplifier

The model considers the noise from the first stage of the amplifier only because it will contribute significantly more noise than the second stage. Since the noise calculation is rather long, it is performed in Appendix 3. The resulting total output thermal noise of the amplifier for the fully-differential case is given by (Eq 6-31).

$$S_{N,OUT} = \frac{2kT}{3fC_C}\left(1+\frac{g_{m7}}{g_{m1}}\right)\left[\frac{(2+\alpha)(1+2\alpha\zeta^2)}{1+2\alpha\zeta^2+\alpha^2\zeta^2}\right] \qquad \text{(Eq 6-31)}$$

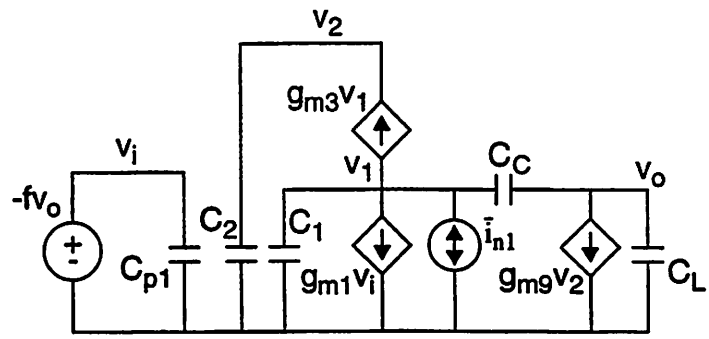

Fig. 6.15: Small-signal model for amplifier output noise calculation

Several means can be employed to reduce the operational amplifier output noise in (Eq 6-31). Since the noise is inversely related to the compensation capacitor, (Eq 6-31) suggests increasing the size of this capacitor will reduce the amplifier noise

contribution. Increasing the compensation capacitor will reduce the amplifier bandwidth which conflicts with the settling constraints. Another approach to reducing the amplifier noise is to minimize the ratio of g_{m7}/g_{m1} in (Eq 6-31). According to (Eq 6-24), this amounts to allocating as large of V_{GS}-V_T as headroom constraints allow to the active load PMOS current devices M_7 and M_8 in Fig. 6.7. The other important observation is that the noise is a weak a function of the relative amplifier pole positions. This implies that the pole positions may be selected on the basis of settling alone.

The complete integrator noise model must include the amplifier with all noise sources as well as the switch modeled as R_{ON} and its noise source. The complete small-signal half-circuit noise model for the integrator in transfer mode (phase 2 in Fig. 6.14) is shown in Fig. 6.16. The input referred thermal noise is calculated at node X. The noise sources in the amplifier are defined in (Eq 6-32) - (Eq 6-34). The model may be employed by calculating the noise transfer function from each

$$\overline{i_{n1}}^2 = 4kT\frac{2}{3}(g_{m1} + g_{m7})\Delta f \qquad \text{(Eq 6-32)}$$

$$\overline{i_{n2}}^2 = 4kT\frac{2}{3}(g_{m9} + g_{m11})\Delta f \qquad \text{(Eq 6-33)}$$

$$\overline{v_n}^2 = 4kTR_{ON}\Delta f \qquad \text{(Eq 6-34)}$$

source to node X. When an integrator is designed, the model can then be used numerically to calculate the total input referred thermal noise on phase 2.

In sampling mode (phase 1), excess noise can come from one amplifier driving the next stage sampling capacitor through a switch as shown in Fig. 6.17. For the first integrator in the cascade, the noise reduces to the ideal $2kT/C_S$ if the input is coming from an ideal source off-chip. Otherwise, the noise transfer function from each noise source to the next stage sampling capacitor C_{Sn} should be calculated at

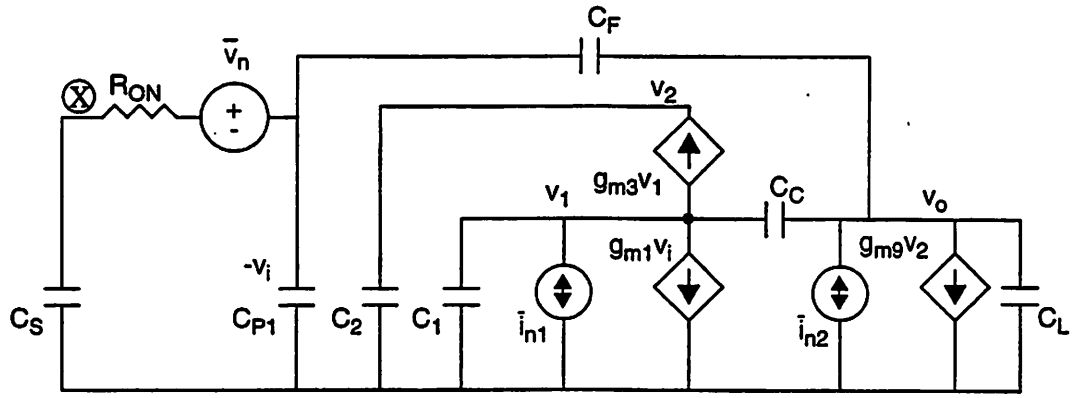

Fig. 6.16: Complete integrator noise model for phase 2

node X in Fig. 6.17. For a particular design, the noise power can then be calculated numerically.

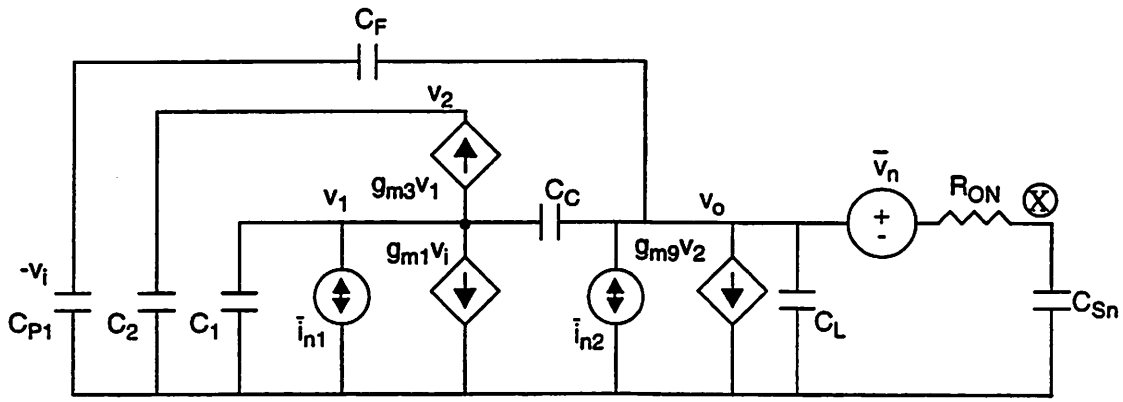

Fig. 6.17: Complete integrator noise model for phase 1

The overall input referred thermal noise for an integrator will be the sum of the previous stage driving its sampling capacitance on phase 1 and the noise from the transfer mode on phase 2. This sum can be used to calculate the noise constant γ_i. It may require several iterations to minimize the noise constant and design integrators which meet the overall noise specifications of the sigma-delta modulator.

6.4.5 Slew Rate

Slew rate refers to the nonlinear response of an amplifier to a large input step. This nonlinear response occurs because the amplifier can only deliver a maximum amount of differential current due to its class A biasing. As a result, the amplifier output cannot track the large rate of change at the amplifier input. To analyze the effect of slew rate on a two-stage cascode compensated amplifier, consider the diagram in Fig. 6.18. The amplifier may reach a slew limit in either the first or second stage depending on the available bias current and capacitance values. The first stage slew limit is set by the need to keep a fixed voltage on the compensation capacitor at the source of cascode devices M_3 and M_4. The second-stage slew limit is set by the need to charge the load and compensation capacitors through the PMOS current sources M_{11} and M_{12}. The overall amplifier slew rate may be approximated to first order by (Eq 6-35) with C_L given by (Eq 6-15).

$$SR = \min\left(\frac{I_1}{C_C}, \frac{I_2}{C_C + C_L}\right) \qquad \text{(Eq 6-35)}$$

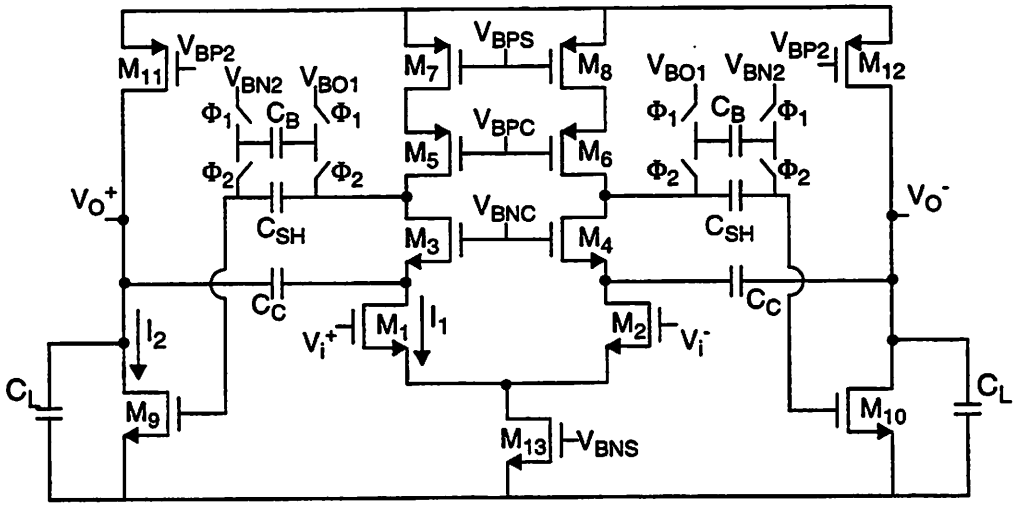

Fig. 6.18: Amplifier diagram for slew rate calculations

Since slew rate depends on the available bias current and the capacitance, it may be improved by increasing the current or decreasing the capacitance. For a fixed settling specification, both of these results can be accomplished by biasing the input (M_1 and M_2) and second stage NMOS devices (M_9 and M_{10}) at high V_{GS}-V_T. This increases both the device f_t and I/g_m ratio which implies better slew rate performance. However, headroom in the first stage and output swing in the second stage will set a maximum V_{GS}-V_T on both sets of devices. Another way to attack the slew rate problem is to reduce the size of the compensation capacitor. However, this will increase the amplifier thermal noise according to (Eq 6-31) and will degrade the settling performance by reducing the damping factor ζ. The last approach is to design an amplifier which settles in a shorter period of time than required by linear settling criteria alone. This can be accomplished by increasing device W/L ratios at fixed V_{GS}-V_T bias points. If the amplifier is limited by the sampling and compensation capacitances, this will increase the current relative to the capacitance thereby improving the slew rate. This approach costs some power dissipation but may be the only way to assure that the slew rate specification is satisfied in combination with all of the other requirements placed on the amplifier.

6.4.6 Computer Optimization Procedures

The previous sections have developed a series of equations to illustrate trade-offs in the design of a three-pole cascode compensated amplifier. To search the design space for the minimum power solution requires the use of computer optimization. Detailed amplifier computer optimization procedures are described in [52] for a variety of topologies. This section will sketch a different optimization procedure for a noise limited three pole cascode compensated amplifier.

1). Select the amplifier pole position parameters (α,ζ,ω_n) from the settling error constraint in (Eq 6-29). Keep in mind the discussion in Section 6.4.3 and select parameters which yield good sensitivities to shifts in the pole positions.

2). Select the PMOS device channel lengths for adequate dc gain following the discussion in Section 6.4.1.

3). Estimate the noise constant γ for this integrator using the complete noise model in Section 6.4.4.

4). Loop through device V_{GS}-V_T bias points keeping in mind the various recommended constraints which come out of the design equation discussions in previous sections. For each V_{GS}-V_T combination, calculate the output swing and then size the sampling capacitor to meet the thermal noise requirements.

5). Given information about the process and the pole position parameters, solve the small-signal frequency response equations (Eq 6-20) - (Eq 6-22) for device sizes (W/L) and the value of compensation capacitor C_C.

6). Check both the dc gain and slew rate specifications and throw out any solutions which do not satisfy both constraints.

7). Select the minimum power solution from those that are left.

8). Double check the thermal noise estimate for the amplifier now that it is designed and iterate through the optimization procedure if necessary.

The above optimization procedure provides a means for obtaining a low-power design for a three-pole cascode compensated operational amplifier. As with any optimization procedure, it is important to note that a variety of second-order effects including common-mode settling, charge injection, and clock feedthrough are not modeled. To see these second-order effects requires transient circuit simulation

across all process corners. If the second-order effects degrade the integrator performance or the integrator is not robust across process, then some design iteration will be required at the circuit simulation level.

6.5 Summary

This chapter investigated the design and power optimization of switched-capacitor integrators. The discussion began by relating sigma-delta modulator system-level specifications to integrator requirements such as settling time, slew rate, output swing, thermal noise and dc gain. Given these system-level specifications, the choice of amplifier topology was critical to minimizing power dissipation. To minimize power, an amplifier topology should have an all NMOS signal path, wideband cascode compensation, the minimum number of current legs, the minimum number of noise contributing devices and rail-to-rail output swing. The two-stage amplifier in Fig. 6.7 with a telescopic first stage, common source second stage and capacitive level-shift between the stages was the amplifier topology that satisfies system-level constraints while possessing the above desirable characteristics for minimum power dissipation. Once the topology was selected, design equations were developed to pick device sizes and bias points subject to constraints on noise, settling error, dc gain, slew rate and robustness. These design equations and computer optimization procedures provide a methodology for exploring the amplifier design space to minimize power dissipation.

Chapter 7
Experimental Prototype and Test Results

7.1 Introduction

This chapter will describe an experimental prototype 2-2-2 cascade sigma-delta modulator implemented in a 0.72 μm double-poly, double-metal CMOS process at 3.3 V supply. The discussion will begin by exploring the design of various circuit blocks on the chip in more detail. Then, experimental results will be presented.

7.2 Circuit Blocks

This section will examine the circuit blocks on the experimental prototype chip. The specifications for each of the six integrators will be reviewed. Details of the operational amplifier design such as common-mode feedback and biasing will be discussed. Various auxiliary circuits such as comparators, a clock generator, output buffers and charge pumps will be described.

7.2.1 Integrators

The specifications for each of the six integrators on the prototype chip will be described in this section. In addition, issues such as integrator timing and the sharing of capacitors between the forward and feedback paths will be discussed.

Using the methods from Chapter 6 and including margins for robust implementation, the settling accuracy, slew rate and thermal noise requirements were specified for each integrator. Table 7.1 shows the specifications for a 1.8 V differential DAC reference level and 1.45 V maximum sinusoidal input signal. The integrators must settle to the required accuracy when clocked at 32 MHz. The sampling capacitors are selected using the scaling procedure in Section 4.5 with a minimum unit capacitor of 100 fF for the parasitic limited integrators at the end of the cascade. The overall simulated integrator power dissipation is 51.8 mW with 40 percent of the power dissipated in the first integrator.

Table 7.1: Integrator Specifications

Integrator	Total Sampling Capacitance	Thermal Noise Contribution	Settling Accuracy	Slew Rate	Simulated Power Dissipation
1	2.45 pF	60.6%	0.0045%	160 V/μs	20.9mW
2	2.2 pF	33.6%	0.012%	160 V/μs	11.1mW
3	1.5 pF	4.6%	0.034%	140 V/ms	7.7mW
4	0.6 pF	1.2%	0.25%	120 V/μs	4.7mW
5	0.5 pF	negligible	0.25%	120 V/μs	3.7mW
6	0.2 pF	negligible	0.25%	80 V/μs	3.7mW

The switched-capacitor integrator diagram in Fig. 7.1 illustrates the basic timing using two-phase non-overlapping clocks. The modulator employs integrators with full delays in the forward path to achieve a pipelined structure. The integrator samples on phase one when the switches labeled Φ_1 and Φ_{1d} are closed. The integrator

transfers charge from the sampling capacitor to the feedback capacitor on phase two when the switches labeled Φ_2 are closed. The appropriate DAC reference level is also applied on phase two by closing either the switches labeled Φ_{2d1} or Φ_{2d2}. Delayed clocks denoted by Φ_{1d}, Φ_{2d1}, and Φ_{2d2} are used to reduce signal-dependent charge injection [58].

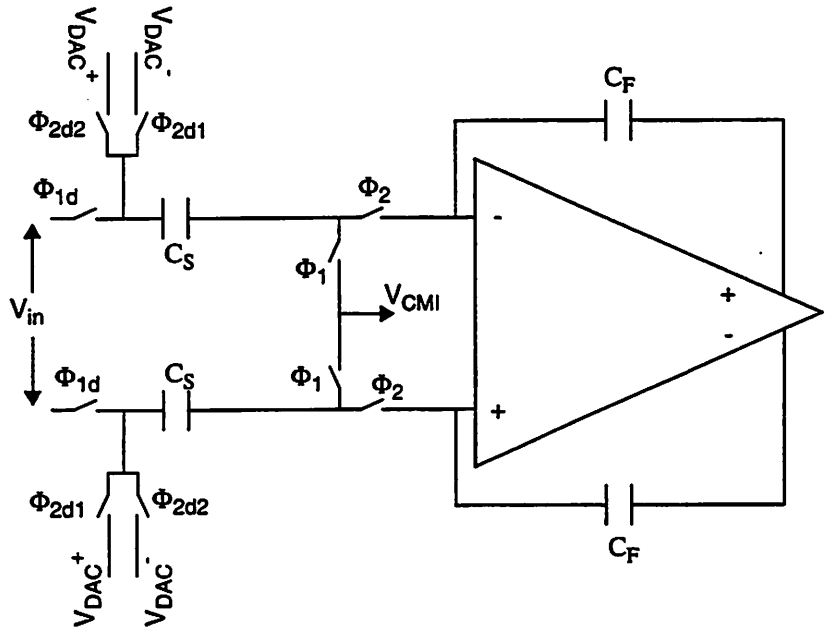

Fig. 7.1: Switched-capacitor integrator

The integrator in Fig. 7.1 shares capacitors between its forward and feedback paths. This implies that the DAC level is applied to the same physical capacitor which is used to sample the input signal. This sharing of capacitors reduces power dissipation because it minimizes the loading on the amplifier summing node as compared to the use of separate capacitors in the forward and feedback paths.

7.2.2 Operational Amplifiers

This section explores the operational amplifier design in more detail focussing on the common-mode feedback loop and internal biasing of the NMOS cascode devices.

In a fully-differential amplifier, common-mode feedback is required to define the voltages at high impedance nodes in the circuit. The operational amplifier including common-mode feedback is shown in Fig. 7.2. The amplifier employs switched-capacitor common-mode feedback using capacitors C_{CM} to sense the output common-mode voltage. Since the integrator is active on both clock phases, switched capacitors C_M are used to define the appropriate dc voltage on the sense capacitors. Because a two-stage amplifier is utilized, an inversion circuit is required to achieve negative common-mode feedback; inversion is performed by the PMOS differential pair formed by M_{C2} and M_{C3}. The common-mode loop works by steering current from current source M_{13} between M_{C2} and the first stage of the amplifier. The loop is compensated using the same capacitors C_C employed in the differential-mode. References V_{REF} and V_{REFB} which are at the same nominal voltage are separated to maintain a stable bias on the gate of M_{C2} while the capacitors C_M are switched onto V_{REFB}. The nominal output common-mode voltage V_{CMO} is 1.7 V for this implementation.

The diagram in Fig. 7.3 shows the operational amplifier with internal biasing of the first stage NMOS cascode devices M_3 and M_4 via a stack of nine transistors M_{ST} [59]. The cascode node is biased internally so that the cascode bias will track changes in the amplifier input common-mode voltage. In addition, the cascode devices are in the signal path; internal biasing will prevent crosstalk of signals between amplifiers. Note that the cascode bias will require decoupling capacitance internal to each amplifier which is not shown in Fig. 7.3.

7.2.3 Bias

Fig. 7.4 shows the biasing scheme for the prototype chip. An external master bias current source is brought onto the chip through a diode-connected PMOS device. This device is decoupled on chip to V_{dd} through a 20 pF capacitor (not shown). A variety of master bias currents are then generated by mirroring the current from the

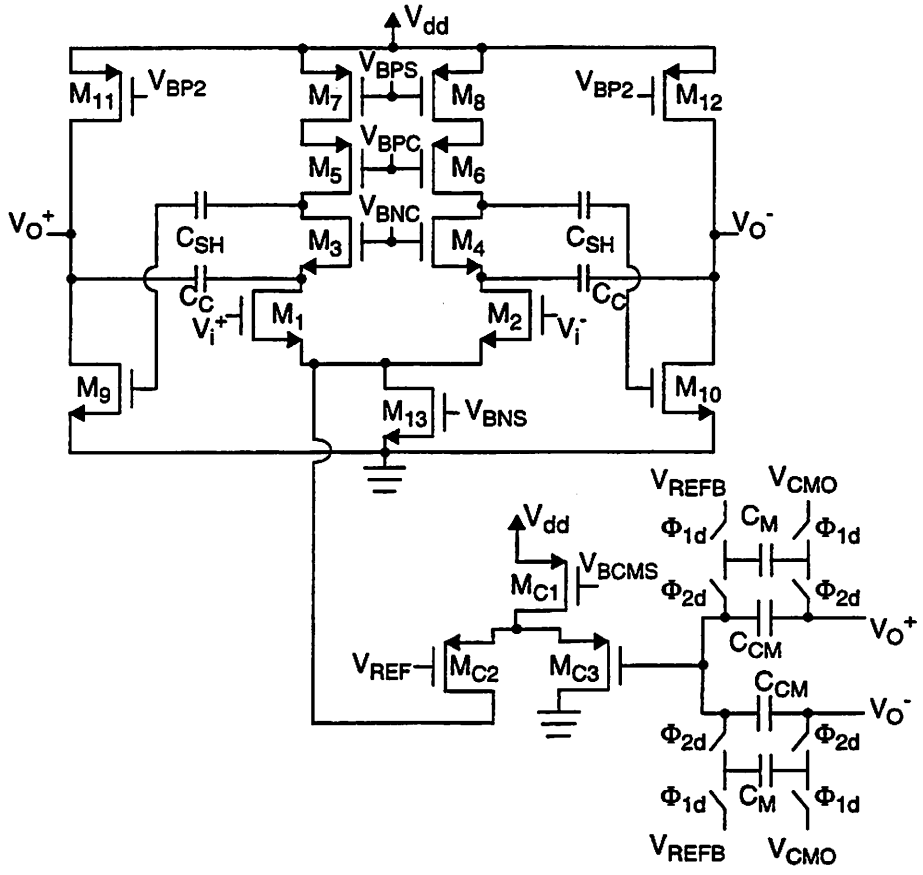

Fig. 7.2: Operational amplifier with switched-capacitor common-mode feedback

diode-connected device. To provide good isolation between circuits on the chip, individual bias circuits are used for each of the three second-order modulators. The master bias is distributed to the local modulator biases as a current so that IR drops due to routing do not affect the bias [42]. When distributing currents, care must be taken in the layout to avoid coupling any noise from the substrate into the bias. This implies that the bias currents should be routed on top-level metal which has the minimum capacitance to substrate and if possible a clean ground shield should be placed between the metal routing and the substrate.

The bias circuit for the first modulator is shown in Fig. 7.5. High-swing cascode biases are generated by the stacks of triode region devices. The PMOS side of the biasing is slaved off the NMOS side for good current matching and to be more

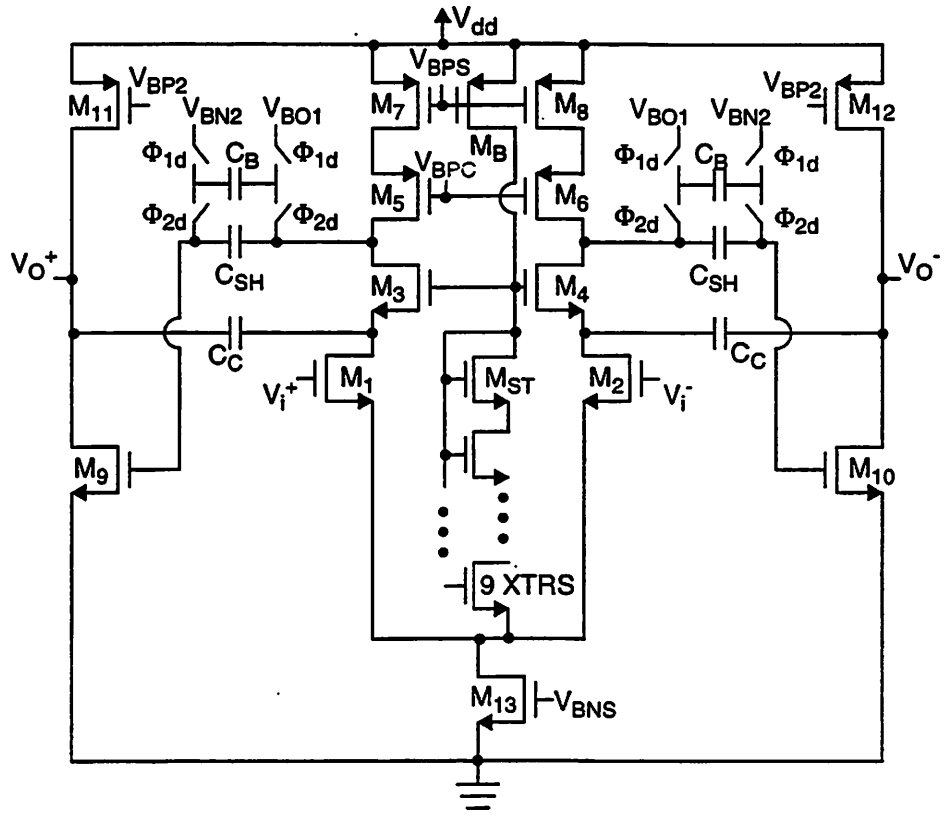

Fig. 7.3: Operational amplifier including internal cascode bias

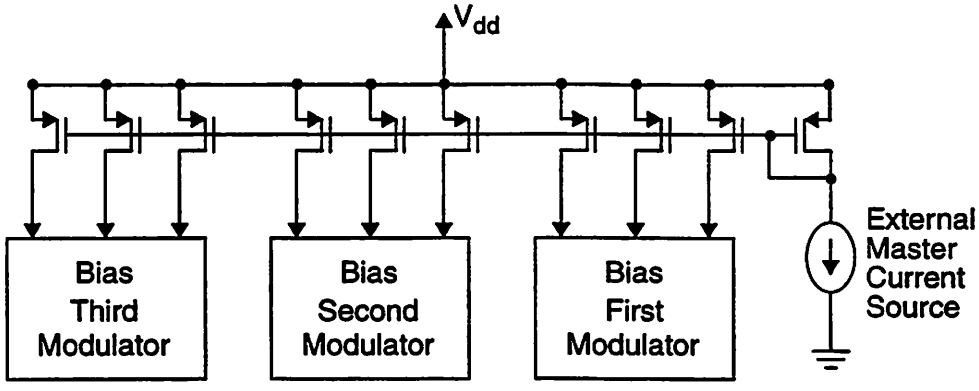

Fig. 7.4: Master Bias Circuit

robust to process shifts. The output common-mode voltage (V_{CMO}) and the first stage output level-shift voltage (V_{BOI}) are generated off-chip and buffered by source followers to provide a low impedance bias. One set of source followers is used for the entire chip. The input common-mode voltage is buffered using a differential pair

because there is not adequate headroom for a source follower at 3.3 V supply. A separate buffer is used for the first integrator to keep the input common-mode as clean as possible since this voltage is used for bottom-plate sampling of the continuous time signal. All nodes which do not require low impedance due to switching of capacitors are decoupled on chip to V_{dd} or ground as appropriate. The bias circuits for the second and third modulators are similar except that only one input common-mode buffer is required.

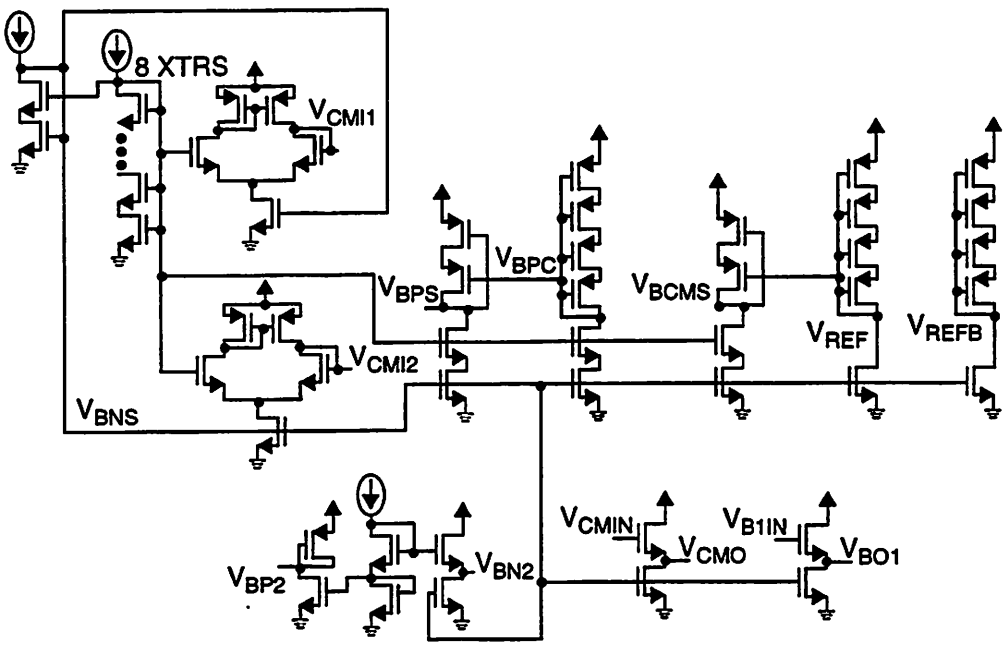

Fig. 7.5: First modulator bias circuit

7.2.4 Comparators

Two types of comparators are employed in the sigma-delta modulator. In the first two stages, a simple dynamic comparator shown in Fig. 7.6 is used to perform a single bit conversion. In the third stage, two static comparators like the one shown in Fig. 7.7 are used to perform a three-level conversion at low offset.

The dynamic comparator in Fig. 7.6 is similar to the one in [50] but simplified to perform a comparison with zero. The differential signal varies the resistance of triode region devices M_1 and M_2. When the latch signal is low, the comparator output is precharged to V_{dd} by devices M_7 and M_{10}. On the rising edge of the latch signal, the outputs of the cross-coupled inverters formed by M_3, M_4, M_7 and M_8 flip in the appropriate direction based on the differential resistance of the triode region input devices.

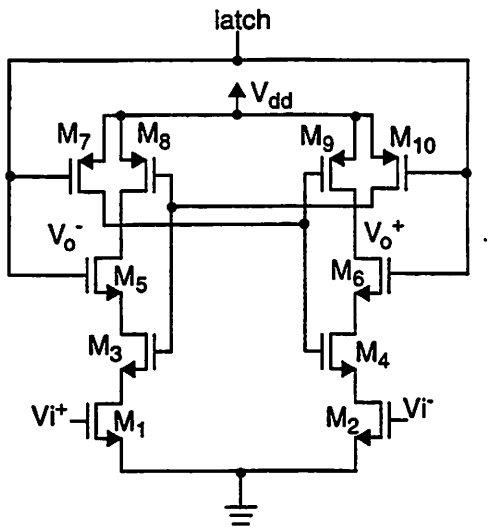

Fig. 7.6: Dynamic comparator

In the last stage of the sigma-delta modulator, the differential comparator references are set 100 mV apart. A comparator offset of less than 25 mV is required to achieve the full dynamic range of the modulator. This offset requirement is beyond the capabilities of a simple dynamic latch, and a static comparator is employed. The comparator in Fig. 7.7 is similar to the one in [60]. A switched-capacitor network is used to set the references for the comparator on phase one and apply the input signal on phase two. On phase two when the input is applied, M_2 is on, M_3 is off and the comparator is in amplification mode. Amplification is performed by the input differential pair M_4 and M_5 in combination with triode region PMOS devices M_9 and

M_{10}. The input differential pair is cascoded to reduce the Miller effect and provide better input-output isolation for the comparator. On phase one, M_3 is on, M_2 is off, comparison is performed and the result is latched by cross-coupled devices M_{12} and M_{13}. Output source followers M_{B1} and M_{B3} provide a level-shift so that the result may be brought to full digital levels by a subsequent inverter. Diode-connected devices M_8 and M_{11} clamp the comparator output for large input signals to improve the overload recovery. It is also important to note that M_2 and M_3 are operated on the inverted clock phases to achieve clock overlap which keeps the current source device M_1 active for the entire cycle with a well defined V_{ds}.

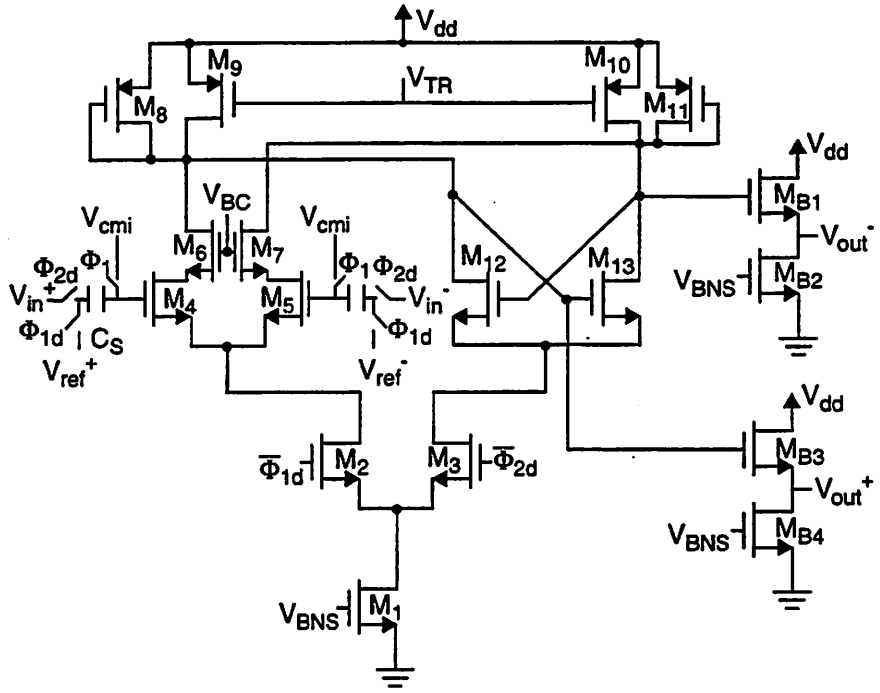

Fig. 7.7: Static comparator

7.2.5 Clock Generator

Switched-capacitor circuits require the generation of two-phase non-overlapping clocks with delayed clocks to reduce signal-dependent charge injection. The circuit in Fig. 7.8 performs this clock generation [42]. The dynamic inverter

circuits formed by M_1 - M_3 and M_4 - M_6 allow the rising edges of the delayed clocks to be lined up with the rising edge of the non-delayed clocks as shown in Fig. 7.9. Lining up these edges gives the amplifier additional time to settle as compared to the case where the rising edge of the delayed clock is delayed by the same amount as its falling edge.

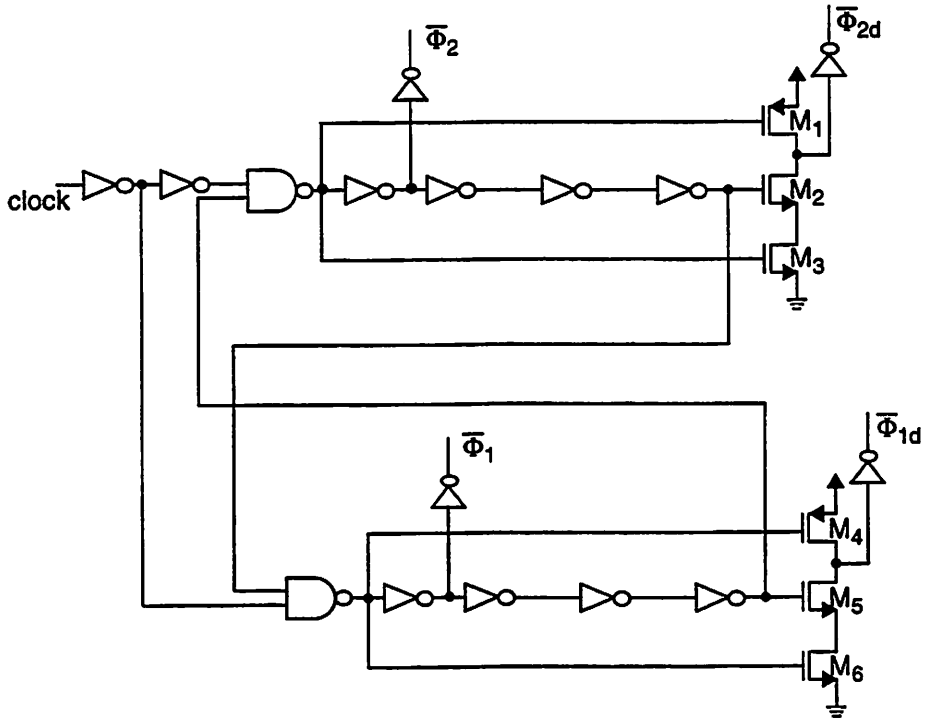

Fig. 7.8: Clock generator

7.2.6 Output Buffers

Output buffers must be designed to minimize digital noise-coupling into the substrate as well as through the bond wires. The circuit in Fig. 7.10 uses an open drain differential pair (M_2 and M_3) to drive digital signals off chip to a 500 ohm load resistor on the test board. This circuit maintains a constant current into the substrate through transistor M_1 independent of the digital output. Coming off chip as a differential signal provides first-order cancellation of the L(dI/dt) induced in the bond wires. The

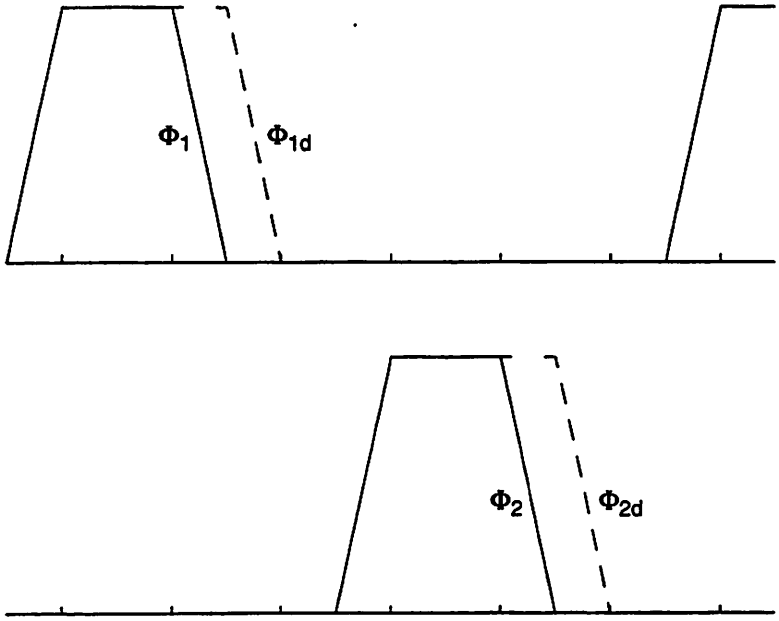

Fig. 7.9: Clock waveforms

differential digital input controls the differential pair by switching reference voltages appropriately through NMOS switches M_4-M_7.

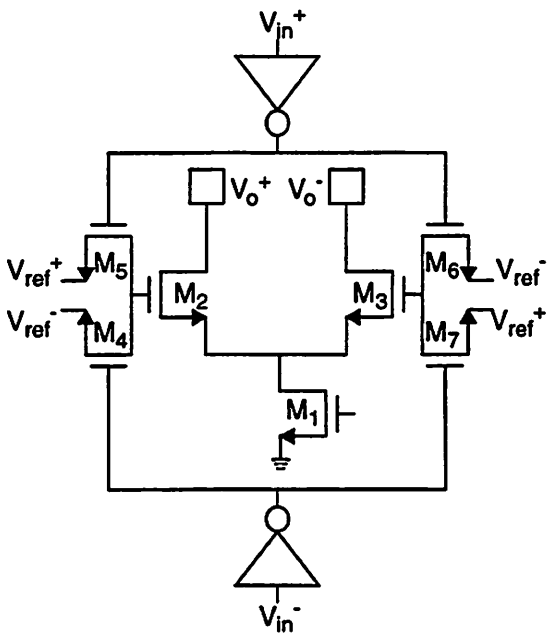

Fig. 7.10: Output buffer

7.2.7 Charge Pumps

Since the 0.72μm process is 5 V capable, charge pumps are used to boast the gate voltage on the switches. This allows only NMOS switches to be used in the switched-capacitor integrators which reduces the parasitic loading on the amplifiers as compared to the use of full CMOS transmission gates. While digital power dissipation increases with the use of charge pumped switches, the reduced capacitive loading on the amplifiers results in a net power savings due to decreased amplifier bias current requirements.

The charge pump circuit employed is shown in Fig. 7.11 [42]. A 0 to 3.3 V clock at the input is dynamically boasted to an inverted 0 to 5 V clock at node clk in Fig. 7.11 through the action of cross-coupled NMOS transistors M_1 and M_2 and capacitors C_1 and C_2. The boasted clocks are generated locally on a per switch basis to prevent crosstalk between sensitive nodes and allow for adequate estimation of the parasitic capacitances which the charge pumps must drive. Accurate estimation of these parasitics is important because the voltage at node clk is given by (Eq 7-1). To achieve

$$V_{clk} = 2V_{dd}\frac{C_2}{C_{gate,\,Msw} + C_{parasitic} + C_2} \qquad \text{(Eq 7-1)}$$

a 5 V clock from a 3.3 V supply, C_2 needs to be sized approximately 5 X the switch gate capacitances while C_1 should be approximately the same size as this gate capacitance. A similar circuit is used to generate a high voltage well-bias (V_{subhi}) for PMOS transistor M_4 in Fig. 7.11.

7.3 Experimental Results

A die photo of the prototype modulator implemented in a 0.72 μm double-poly, double-metal CMOS process is shown in Fig. 7.12. The chip active area is 1.3 mm x 2.7

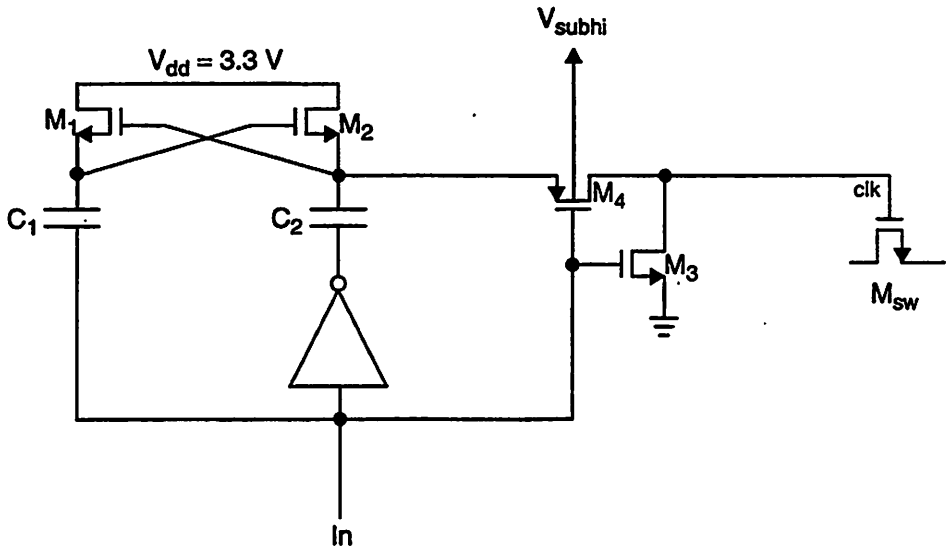

Fig. 7.11: Charge pump

mm. The chip is bonded directly to a custom printed circuit board using chip-on-board technology to minimize the effect bondwire inductance.

Fig. 7.13 shows the measured SNR and SNDR as a function of input power for a 100 kHz sinusoidal input at 2MS/s Nyquist rate and 16 X oversampling ratio. The modulator achieves 71 dB dynamic range, 65 dB peak SNR and 63 dB peak SNDR. At this speed, the modulator dissipates 98 mW from a 3.3 V supply. The performance is limited by amplifier settling due to a 13% increase in nominal capacitance density of the process between layout and fabrication.

At 1.4 MS/s Nyquist rate, the modulator achieves 77 dB dynamic range, 72 dB peak SNR and 71dB peak SNDR as shown in Fig. 7.14. At this speed, the modulator dissipates 81 mW. Performance is noise limited in this regime as shown by the FFT for a -27 dBFS, 100 kHz input in Fig. 7.15. The slight rise in noise toward the band edge is consistent with thermal noise from the second integrator which is shaped by a first-order difference when referred to the input. The noise floor is about 6 dB higher than the designed value. Possible explanations for the noise increase include substrate

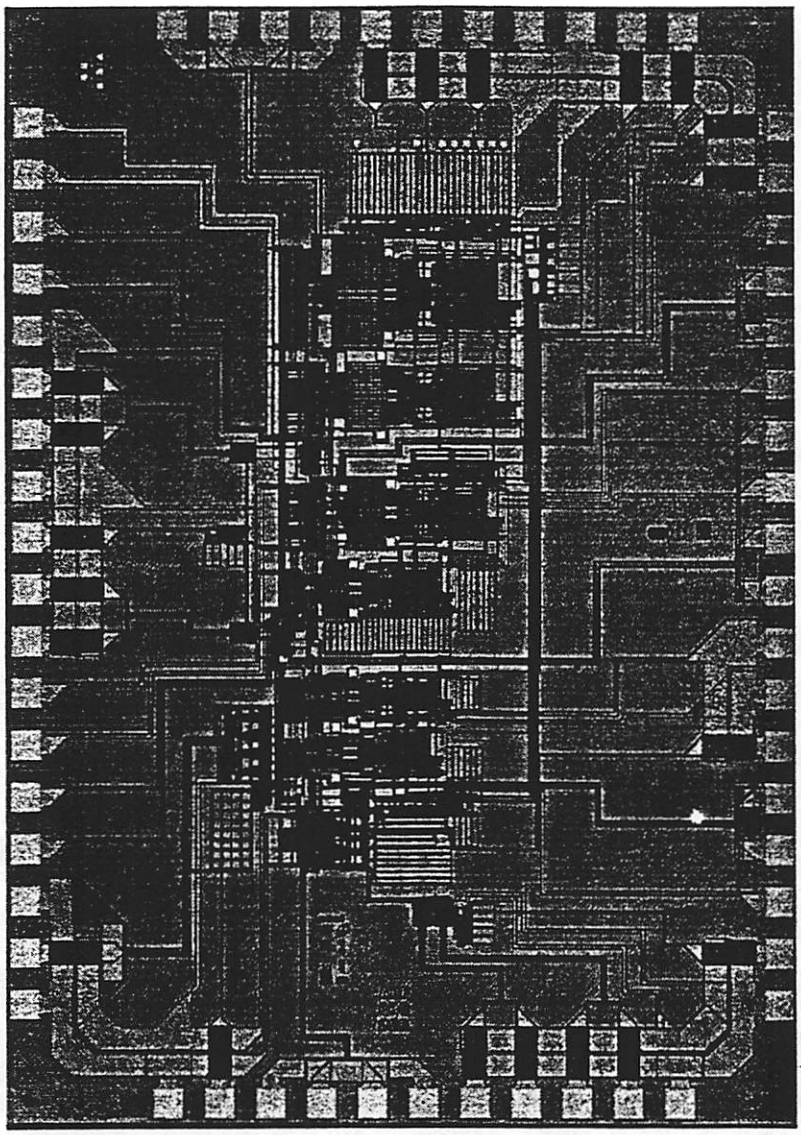

Fig. 7.12: Die photo

coupling, supply noise, reference noise and short channel device noise [61]. As shown in Fig. 7.14, the modulator overload point is -2.9 dBFS. LMS digital calibration provides 0.5 dB improvement suggesting that the performance is not limited by capacitor matching at this dynamic range.

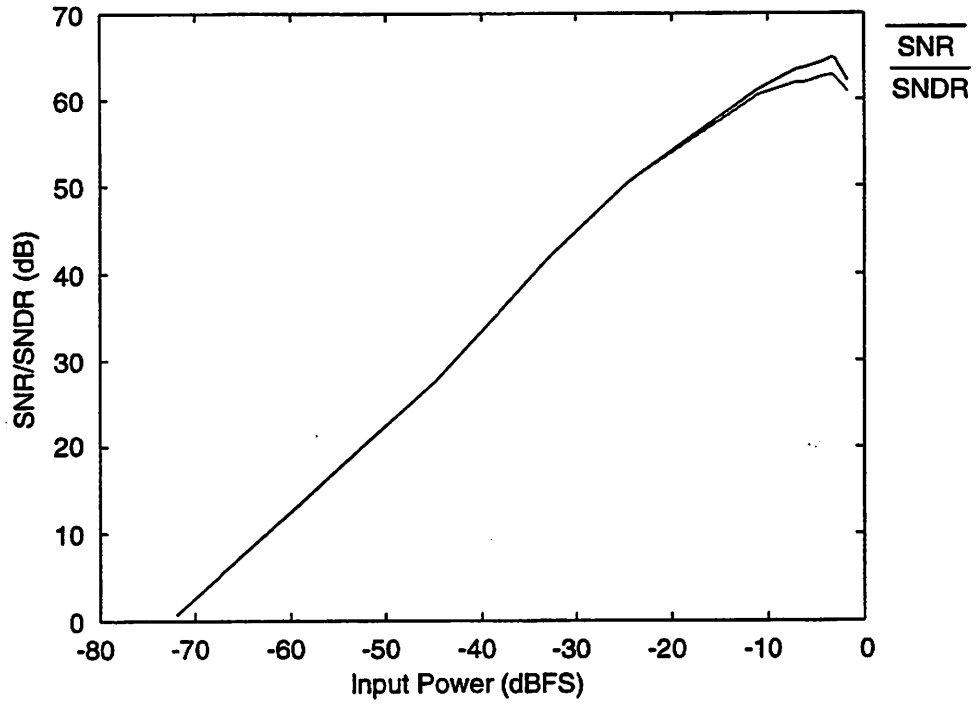

Fig. 7.13: Measured SNR/SNDR versus input power at 2 MS/s

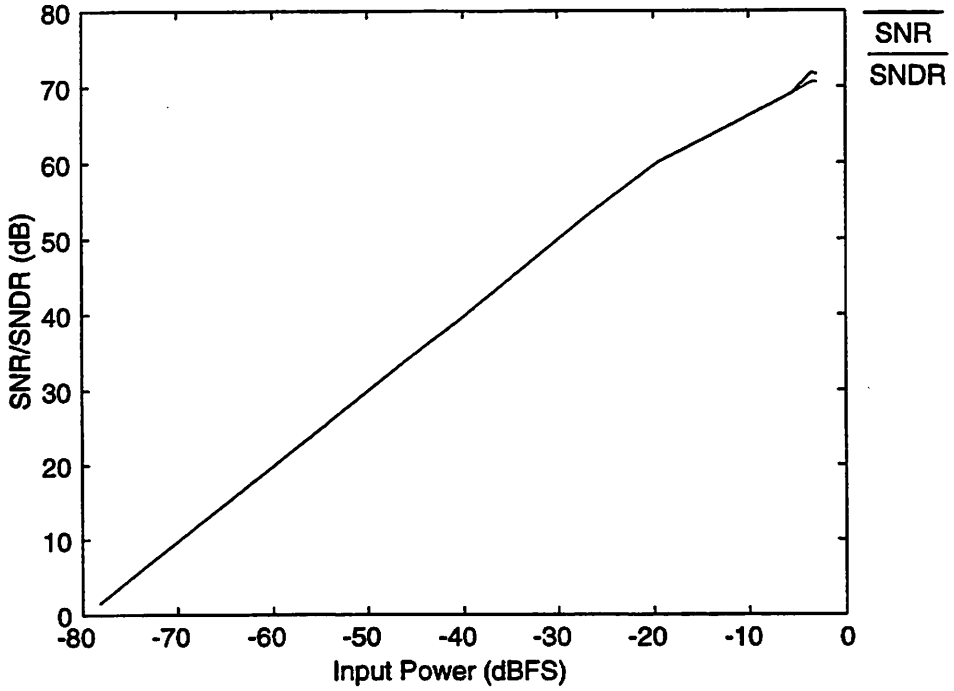

Fig. 7.14: Measured SNR/SNDR versus input power at 1.4 MS/s

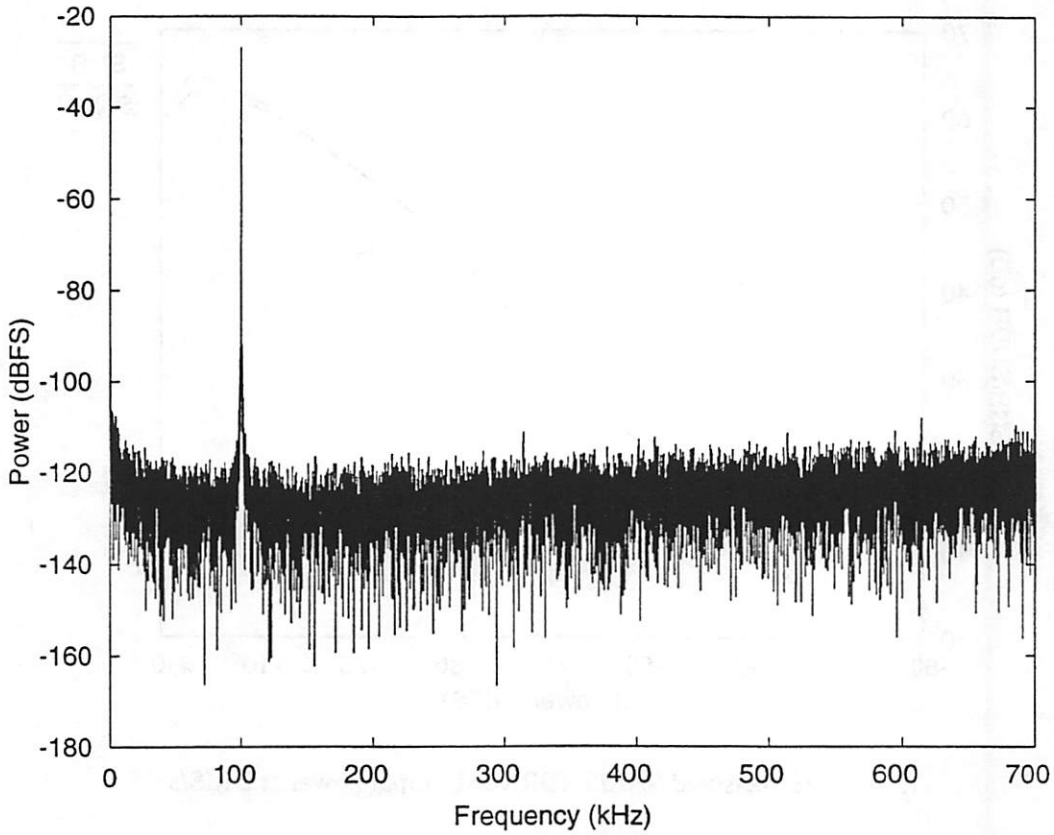

Fig. 7.15: FFT for -27 dBFS, 100 kHz input at 1.4 MS/s

7.4 Summary

This chapter described in more detail the experimental prototype 2-2-2 cascade sigma-delta modulator and showed measured results of an implementation in a 0.72 µm CMOS process. The modulator achieved 77 dB of dynamic range, 72 dB peak SNR and 71 dB of dynamic at 1.4 MS/s Nyquist rate. The modulator dissipated 81 mW from a 3.3 V supply.

Chapter 8
Conclusions and Future Work

8.1 Introduction

This chapter summarizes key research contributions and results, and provides some recommendations for future work. There were two general thrusts of this research: 1) Issues of integration and programmability in RF receivers were explored with particular emphasis on baseband processing. 2) Techniques for minimizing the power dissipation of high-speed sigma-delta modulators were investigated. Integration is an important issue in reducing the cost, power dissipation and form factor of RF transceivers. Programmability will allow future RF transceivers to adapt to multiple communications standards with varying bandwidth and dynamic range requirements. While the RF application was emphasized, techniques for minimizing power dissipation in sigma-delta modulators are important to extend battery life in any portable application.

8.2 Key Research Contributions and Results

This research explored the use of a high-speed, low-power sigma-delta modulator in concert with a digital decimation filter to perform channel select filtering and digitization in the baseband path of a highly-integrated, multi-standard capable RF receiver. Key research contributions and results are summarized below:

- Demonstrated that a sigma-delta modulator can meet the baseband processing requirements for a wideband RF standard at reasonable power dissipation. An experimental prototype achieved 77 dB of dynamic range and dissipated 81 mW at 1.4 MS/s Nyquist rate which is suitable for a DECT application.
- Developed a new 2-2-2 cascade sigma-delta architecture oversampling at 16 X. This architecture minimizes power dissipation by allowing the kT/C noise limited sampling capacitance to dominate the loading on the switched-capacitor integrators.
- Showed that scaling integrator sampling capacitors to the minimum value required by kT/C noise at each stage in the cascade is an effective technique for reducing power dissipation. This techniques reduce the power dissipation by 2.5 X in the prototype design.
- Developed a digital calibration scheme using an LMS adaptive filter to compensate for the effects of interstage gain mismatch in cascaded sigma-delta modulators.
- Designed a new two-stage operational amplifier with an all NMOS signal path and capacitive level-shift between the stages which has desirable properties for minimizing power dissipation. Developed a methodology to pick bias points and device sizes in this amplifier to satisfy design constraints while minimizing power dissipation.

8.3 Recommended Future Work

This project served primarily as a proof of concept that a sigma-delta modulator could meet the specifications of a wideband RF system without excessive power dissipation. The next step would be to integrate the modulator with the other blocks in the receive path to demonstrate an overall system. Issues such as substrate noise and other coupling mechanisms will need to be addressed carefully as part of this integration effort.

Multi-standard capability is another area that requires further investigation. A demonstration of a modulator as part of a larger system that can meet standards of varying dynamic range and bandwidth (e.g. DECT and GSM) would be a good next step in this area. In addition, the design of low-power programmable decimation filters will be a critical part of demonstrating multi-standard capability.

The power optimization of the baseband processing block as a whole is another area where further research is required. Power trade-offs when the requirements on the continuous-time antialiasing filter are considered along with those of the sigma-delta modulator should be explored. This work could lead to a more power efficient baseband block as compared to optimizing the modulator alone.

Appendix 1

Sample Baseband Dynamic Range and Linearity Calculations

This appendix shows the dynamic range (Table 2.1) and distortion (Table 2.3) calculations for the DECT standard. Calculations for the other standards follow an identical procedure with the different numbers.

The RF specifications provide the reference sensitivity, worst case blocker, either SNR (E_b/N_o) or BER which corresponds directly to an SNR, and bandwidth or bit rate. First calculate the noise power at the input of the LNA assuming a 50 ohm source resistance which will be denoted S_{Nin} and expressed in dBm:

$$S_{Nin} = 10\log(kTRB) + 13(dBm)/(dBV) \qquad \text{(Eq A1-1)}$$

where k is Boltzmann's constant, T is 300 K, R is 50 ohms and B is the receiver bit rate (1.152 MS/s for DECT) [3]. This results in S_{Nin} of -113.2 dBm.

Next calculate the maximum allowable receiver noise figure denoted by NF:

$$NF = S_{REF} - S_{Nin} - \frac{E_b}{N_o} \qquad \text{(Eq A1-2)}$$

For DECT, the reference sensitivity (S_{REF}) is -83 dBm and the required E_b/N_o is 14.6 dB for 10^{-3} BER using a frequency discriminator type of demodulator [3], [28]. This implies from (Eq A1-2) that the maximum allowable receiver noise figure is 15.6 dB.

Next, calculate the noise level of the baseband processing circuit in dBm referred to the LNA input such that the baseband processing contributes negligibly to the overall receiver noise figure. This noise level depends upon the input noise at the front-end of the LNA, the receiver noise figure and a margin to make sure that the baseband noise is negligible. In this case the margin is set to 10 dB. In (Eq A1-3), S_{NBBin} represents the input referred noise level of the baseband processing circuits.

$$S_{NBBin} = S_{Nin} + NF - 10dB \qquad \text{(Eq A1-3)}$$

For the calculated input noise from (Eq A1-1) and the noise figure from (Eq A1-2), this yields an input referred baseband noise contribution of -107.6 dBm.

Now, calculate the allowable gain in the receive chain. It is assumed that the baseband circuit can swing 1 V and is fully differential. This yields a peak signal handling capability (S_{peak}) of 0 dBV or 13 dBm for the baseband circuitry. Allow a 5 dB margin in case the receiver gain is larger than expected and choose the gain (G) such that the worst case blocker (S_B) is amplified to this maximum allowable level

$$G = S_{peak} - S_B - 5dB \qquad \text{(Eq A1-4)}$$

For DECT, the worst case blocker is -33 dBm [3]. This results in an allowable receiver gain of 41 dB.

Now, take the baseband noise contribution at the input of the LNA and refer it to the input of the baseband processing circuit by using (Eq A1-5) with S_{NBBin} in dBm and G in dB.

$$S_{NBB} = S_{NBBin} + G \qquad \text{(Eq A1-5)}$$

This results in noise referred to the input of the baseband processing circuit (S_{NBB}) of -66.6 dBm or -79.6 dBV. An additional 5 dB of margin is required on this noise floor in case the gain of the receiver is lower than expected. This yields a final noise floor of -84.6 dBV and overall dynamic range of 84.6 dB assuming a peak signal handling capability of 0 dBV.

Next consider the linearity requirements of the baseband processing circuitry for DECT. The DECT specification requires the receiver to handle a -80 dBm desired signal in the presence of a -46 dBm out-of-band blocker [3]. First calculate, the power of the third-order intermodulation component (IM_{3in}) at the receiver input which is dependent on the desired signal power (S_{DES}) and the required SNR (E_b/N_o) at the slicer as shown in (Eq A1-6).

$$IM_{3in} = S_{DES} - \frac{E_b}{N_o} - 10dB \qquad \text{(Eq A1-6)}$$

The 10 dB margin in (Eq A1-6) is required to make sure that noise rather than distortion limits the overall receiver performance. Given a desired signal level of -80 dBm and E_b/N_o of 14.6 dB yields IM_{3in} of -104.6 dBm.

It is now possible to calculate the overall receiver out-of-band input third-order intercept point (IIP_{3R}) by using the definition in Fig. 2.17.

$$IIP_{3R} = 1.5S_{BLK} - 0.5IM_{3in} \qquad \text{(Eq A1-7)}$$

This results in an overall receiver out-of-band input third-order intercept point of -16.7 dBm for DECT according to (Eq A1-7).

Finally calculate the baseband processing input third-order intercept point (IIP_{3BB}). The baseband processing circuit is assumed to contribute 1dBm to the IIP_{3R} of -16.7 dBm. This implies that the everything else in the receiver has an input third-order intercept point (IIP_{3EE}) of -15.7 dBm. Given the gain (G) of 41 dB from (Eq A1-4), (Eq A1-8) with all terms expressed on a linear scale specifies the baseband processing input third-order intercept point.

$$IIP_{3BB} = \frac{G}{\frac{1}{IIP_{3R}} - \frac{1}{IIP_{3EE}}} \qquad \text{(Eq A1-8)}$$

(Eq A1-8) results in an baseband processing out-of-band input third-order intercept point of 31.1 dBm for DECT.

Appendix 2

Step Response of a Cascode Compensated Operational Amplifier

This appendix includes a detailed derivation of the closed-loop step response of a three-pole cascode compensated operational amplifier. The amplifier has the following closed-loop transfer function which is of the same form as the transfer function in (Eq 6-16):

$$H(s) = \frac{k(z^2 - s^2)}{(s + \omega_{cl})(s^2 + 2\zeta\omega_n s + \omega_n^2)} \qquad \text{(Eq A2-1)}$$

The first step in calculating the step response is to convolve h(t) with a unit step function. This is equivalent to multiplying the frequency domain result H(s) by 1/s which is the Laplace transform of the unit step. The result is:

$$S(s) = \frac{k(z^2 - s^2)}{s(s + \omega_{cl})(s^2 + 2\zeta\omega_n s + \omega_n^2)} \qquad \text{(Eq A2-2)}$$

Next factor the denominator so that a partial fraction expansion can be performed:

$$S(s) = \frac{k(z^2 - s^2)}{s(s + \omega_{cl})(s + a + jb)(s + a - jb)} \qquad \text{(Eq A2-3)}$$

where

$$a = \zeta\omega_n \qquad \text{(Eq A2-4)}$$

$$b = \omega_n\sqrt{1-\zeta^2} \qquad \text{(Eq A2-5)}$$

Perform a partial fraction expansion on S(s):

$$\begin{aligned} S(s) = {} & \frac{kz^2}{s\omega_{cl}(a+jb)(a-jb)} - \frac{k(z^2-\omega_{cl}^2)}{(s+\omega_{cl})\omega_{cl}(-\omega_{cl}+a+jb)(-\omega_{cl}+a-jb)} \\ & + \frac{k(z^2-a^2-2jab+b^2)}{(s+a+jb)(-2jb)(-a-jb)(\omega_{cl}-a-jb)} \\ & + \frac{k(z^2-a^2+2jab+b^2)}{(s+a-jb)(2jb)(-a+jb)(\omega_{cl}-a+jb)} \end{aligned} \qquad \text{(Eq A2-6)}$$

Now, inverse Laplace transform S(s) to find the closed-loop step response s(t)

$$\begin{aligned} s(t) = {} & \frac{kz^2}{\omega_{cl}(a+jb)(a-jb)} - \frac{k(z^2-\omega_{cl}^2)}{\omega_{cl}(-\omega_{cl}+a+jb)(-\omega_{cl}+a-jb)}e^{-\omega_{cl}t} \\ & + \frac{k(z^2-a^2-2jab+b^2)}{(-2jb)(-a-jb)(\omega_{cl}-a-jb)}e^{-(a+jb)t} \\ & + \frac{k(z^2-a^2+2jab+b^2)}{(2jb)(-a+jb)(\omega_{cl}-a+jb)}e^{-(a-jb)t} \end{aligned} \qquad \text{(Eq A2-7)}$$

Simplify terms:

$$\begin{aligned} s(t) = {} & \frac{kz^2}{\omega_{cl}(a^2+b^2)} - \frac{k(z^2-\omega_{cl}^2)}{\omega_{cl}(\omega_{cl}^2-2a\omega_{cl}+a^2+b^2)}e^{-\omega_{cl}t} \\ & + \frac{ke^{-at}}{2jb}\left(\frac{(z^2-a^2-2jab+b^2)}{(a+jb)(\omega_{cl}-a-jb)}e^{-jbt} + \frac{(z^2-a^2+2jab+b^2)}{(-a+jb)(\omega_{cl}-a+jb)}e^{jbt}\right) \end{aligned} \qquad \text{(Eq A2-8)}$$

Place last two terms over a common denominator:

$$s(t) = \frac{kz^2}{\omega_{cl}(a^2+b^2)} - \frac{k(z^2-\omega_{cl}^2)}{\omega_{cl}(\omega_{cl}^2-2a\omega_{cl}+a^2+b^2)}e^{-\omega_{cl}t}$$
$$-\left(\frac{ke^{-at}}{2jb(a^2+b^2)(\omega_{cl}^2-2a\omega_{cl}+a^2+b^2)}\right) \qquad \text{(Eq A2-9)}$$
$$[j(a^2b\omega_{cl}+b^3\omega_{cl}-2abz^2+b\omega_{cl}z^2)(e^{-jbt}+e^{jbt})$$
$$+(a^4+2a^2b^2+b^4-a^3\omega_{cl}-ab^2\omega_{cl}-a^2z^2+b^2z^2+a\omega_{cl}z^2)(e^{jbt}-e^{-jbt})]$$

Put last term into trigonometric format:

$$s(t) = \frac{kz^2}{\omega_{cl}(a^2+b^2)} - \frac{k(z^2-\omega_{cl}^2)}{\omega_{cl}(\omega_{cl}^2-2a\omega_{cl}+a^2+b^2)}e^{-\omega_{cl}t}$$
$$-\left(\frac{ke^{-at}}{b(a^2+b^2)(\omega_{cl}^2-2a\omega_{cl}+a^2+b^2)}\right) \qquad \text{(Eq A2-10)}$$
$$[(a^2b\omega_{cl}+b^3\omega_{cl}-2abz^2+b\omega_{cl}z^2)\cos(bt)$$
$$+(a^4+2a^2b^2+b^4-a^3\omega_{cl}-ab^2\omega_{cl}-a^2z^2+b^2z^2+a\omega_{cl}z^2)\sin(bt)]$$

Substitute back expressions for a and b from (Eq A2-4) and (Eq A2-5) and simplify:

$$s(t) = \frac{kz^2}{\omega_{cl}\omega_n^2} - \frac{k(z^2-\omega_{cl}^2)}{\omega_{cl}(\omega_{cl}^2-2\zeta\omega_n\omega_{cl}+\omega_n^2)}e^{-\omega_{cl}t} - \frac{ke^{-\zeta\omega_n t}}{\omega_n^3(\sqrt{1-\zeta^2})(\omega_{cl}^2-2\zeta\omega_n\omega_{cl}+\omega_n^2)}$$
$$\left[(\omega_n^2\omega_{cl}-2\zeta\omega_n z^2+\omega_{cl}z^2)\left(\omega_n\sqrt{1-\zeta^2}\right)\cos\left(\omega_n t\sqrt{1-\zeta^2}\right)+ \right. \qquad \text{(Eq A2-11)}$$
$$\left.(\omega_n^4-\zeta\omega_n^3\omega_{cl}+\zeta\omega_n\omega_{cl}z^2-2\zeta^2\omega_n^2z^2+\omega_n^2z^2)\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right]$$

Perform final simplification and factoring:

$$s(t) = \frac{kz^2}{\omega_{cl}\omega_n^2}\left\{1 - \frac{\omega_n^2(z^2-\omega_{cl}^2)}{z^2(\omega_{cl}^2 - 2\zeta\omega_n\omega_{cl} + \omega_n^2)}e^{-\omega_{cl}t} - \frac{\omega_{cl}e^{-\zeta\omega_n t}}{z^2(\omega_{cl}^2 - 2\zeta\omega_n\omega_{cl} + \omega_n^2)}\right.$$

(Eq A2-12)

$$\left[(\omega_n^2\omega_{cl} - 2\zeta\omega_n z^2 + \omega_{cl}z^2)\cos\left(\left(\omega_n t\sqrt{1-\zeta^2}\right)\right.\right.$$

$$\left.\left. + \frac{1}{\sqrt{1-\zeta^2}}(\omega_n^3 - \zeta\omega_n^2\omega_{cl} + \zeta\omega_{cl}z^2 - 2\zeta^2\omega_n z^2 + \omega_n z^2)\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right)\right]\right\}$$

Note that the factor to the left of the expression is the closed loop gain of the amplifier A_{cl}.

$$s(t) = A_{cl}\left\{1 - \frac{\omega_n^2(z^2-\omega_{cl}^2)}{z^2(\omega_{cl}^2 - 2\zeta\omega_n\omega_{cl} + \omega_n^2)}e^{-\omega_{cl}t} - \frac{\omega_{cl}e^{-\zeta\omega_n t}}{z^2(\omega_{cl}^2 - 2\zeta\omega_n\omega_{cl} + \omega_n^2)}\right.$$

(Eq A2-13)

$$\left[(\omega_n^2\omega_{cl} - 2\zeta\omega_n z^2 + \omega_{cl}z^2)\cos\left(\left(\omega_n t\sqrt{1-\zeta^2}\right)\right.\right.$$

$$\left.\left. + \frac{1}{\sqrt{1-\zeta^2}}(\omega_n^3 - \zeta\omega_n^2\omega_{cl} + \zeta\omega_{cl}z^2 - 2\zeta^2\omega_n z^2 + \omega_n z^2)\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right)\right]\right\}$$

It is useful in the design process to work with relative values of the pole and zero positions rather than the absolute values. To do this define the following relationships which normalize the pole and zero positions to the real part of the complex closed-loop poles:

$$z = \gamma\zeta\omega_n \qquad \text{(Eq A2-14)}$$

$$\omega_{cl} = \alpha\zeta\omega_n \qquad \text{(Eq A2-15)}$$

The normalized step response becomes:

$$s(t) = A_{cl}\left\{1 - \frac{(\gamma^2 - \alpha^2)}{\gamma^2(1 - 2\alpha\zeta^2 + \alpha^2\zeta^2)}e^{-\alpha\zeta\omega_n t} - \frac{\alpha e^{-\zeta\omega_n t}}{\gamma^2(1 - 2\alpha\zeta^2 + \alpha^2\zeta^2)}\right.$$
$$\left[(\alpha + -2\zeta^2\gamma^2 + \alpha\zeta^2\gamma^2)\cos\left(\omega_n t\sqrt{1-\zeta^2}\right) + \right. \qquad \text{(Eq A2-16)}$$
$$\left.\left.\frac{(1 - \alpha\zeta^2 + \zeta^2\gamma^2 - 2\zeta^4\gamma^2 + \alpha\zeta^4\gamma^2)}{\zeta\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right]\right\}$$

While (Eq A2-16) is the complete step response of a three pole cascode compensated op amp, it is not particularly useful for design. In practical cases, the right and left plane zeroes in the closed loop transfer function will be at much higher frequency than the poles. This corresponds to $\gamma \to \infty$ in (Eq A2-16). With this simplification, the step response becomes:

$$s(t) = A_{cl}\left\{1 - \frac{1}{(1 - 2\alpha\zeta^2 + \alpha^2\zeta^2)}e^{-\alpha\zeta\omega_n t} - \right.$$
$$\frac{\alpha\zeta e^{-\zeta\omega_n t}}{(1 - 2\alpha\zeta^2 + \alpha^2\zeta^2)}\left[(-2\zeta + \alpha\zeta)\cos\left(\omega_n t\sqrt{1-\zeta^2}\right) + \right. \qquad \text{(Eq A2-17)}$$
$$\left.\left.\frac{(1 - 2\zeta^2 + \alpha\zeta^2)}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right]\right\}$$

Appendix 3

Thermal Noise in a Cascode Compensated Operational Amplifier

This appendix shows the derivation of the total output thermal noise of the cascode compensated amplifier in Fig. 6.7 using the small-signal half-circuit in Fig. 6.15. The derivation begins by calculating the noise transfer function in (Eq A3-1).

$$\frac{v_o}{i_{n1}}(s) = \frac{\dfrac{g_{m1}g_{m3}g_{m9}}{C_2C_T^2}\left(1-\dfrac{C_2C_C}{g_{m3}g_{m9}}s^2\right)}{s^3+\left[\dfrac{g_{m3}(C_L+C_C)-fg_{m1}C_C}{C_T^2}\right]s^2+\dfrac{g_{m3}g_{m9}C_C}{C_2C_T^2}s+\dfrac{fg_{m1}g_{m3}g_{m9}}{C_2C_T^2}} \qquad \text{(Eq A3-1)}$$

This noise transfer function is of the form in (Eq A3-2) noting that this applies the characteristic polynomial in (Eq 6-19) and that the pole and zero locations of the noise transfer function are identical to those in the amplifier input-output transfer function H(s) in (Eq 6-18).

$$\frac{v_o}{i_{n1}}(s) = \frac{k\left(1-\dfrac{s^2}{z^2}\right)}{(s+\omega_{cl})(s^2+2\zeta\omega_n s+\omega_n^2)} \qquad \text{(Eq A3-2)}$$

The pole and zero relationships obtained by equating terms in s of (Eq A3-1) and (Eq A3-2) and the constant k are given by (Eq A3-3) - (Eq A3-7).

$$z = \pm\sqrt{\frac{g_{m3}g_{m9}}{C_2C_C}} \qquad \text{(Eq A3-3)}$$

$$\omega_{cl} + 2\zeta\omega_n = \frac{g_{m3}(C_L + C_C) - fg_{m1}C_C}{C_2C_T^2} \qquad \text{(Eq A3-4)}$$

$$\omega_n^2 + 2\zeta\omega_n\omega_{cl} = \frac{g_{m3}g_{m9}C_C}{C_2C_T^2} \qquad \text{(Eq A3-5)}$$

$$\omega_{cl}\omega_n^2 = \frac{fg_{m1}g_{m3}g_{m9}}{C_2C_T^2} \qquad \text{(Eq A3-6)}$$

$$k = \frac{g_{m1}g_{m3}g_{m9}}{C_2C_T^2} \qquad \text{(Eq A3-7)}$$

Note also that the single-sided power spectral density of an MOS device is defined by (Eq A3-8) [41]. This implies that $\overline{i_{n1}^2}$ in the small-signal circuit diagram Fig. 6.15 is

$$\overline{i_n^2} = 4kT\frac{2}{3}g_m\Delta f \qquad \text{(Eq A3-8)}$$

given by (Eq A3-9).

$$\overline{i_{n1}^2} = 4kT\frac{2}{3}(g_{m1} + g_{m7})\Delta f \qquad \text{(Eq A3-9)}$$

Now evaluate the noise transfer function in (Eq A3-2) at $s = j\omega$.

$$\frac{v_o}{i_{n1}}(j\omega) = \frac{k\left(1 + \frac{\omega^2}{z^2}\right)}{(j\omega + \omega_{cl})(-\omega^2 + j\omega 2\zeta\omega_n + \omega_n^2)} \qquad \text{(Eq A3-10)}$$

The two-sided noise power spectral density at the output of the amplifier is given by (Eq A3-11). Note that $\overline{i_{n1}^2}$ is a single-sided power spectral density which accounts for the factor of two.

$$S_N(\omega) = \frac{1}{2}\left(\frac{v_o}{i_{n1}}(j\omega)\right)\left(\frac{v_o}{i_{n1}}(j\omega)\right)^* \overline{i_{n1}^2} \qquad \text{(Eq A3-11)}$$

Now plug the noise transfer function from (Eq A3-10) into (Eq A3-11) to derive the amplifier output noise power spectral density in (Eq A3-12).

$$S_N(\omega) = \frac{\frac{1}{2}k^2\overline{i_{n1}^2}\left(1+\frac{\omega^2}{z^2}\right)^2}{(\omega^2+\omega_{cl}^2)[\omega^4+2\omega^2\omega_n^2(2\zeta^2-1)+\omega_n^4]} \qquad \text{(Eq A3-12)}$$

The next step is to calculate the total amplifier noise denoted by $S_{N,OUT}$ in (Eq A3-13).

$$S_{N,OUT} = \int_{-\infty}^{\infty} S_N(2\pi f)df \qquad \text{(Eq A3-13)}$$

Note that (Eq A3-13) cannot be evaluated by direct integration for the power spectral density in (Eq A3-12). However, the integral can be evaluated by noting that the power spectral density $S_N(\omega)$ for a wide-sense stationary random process is the Fourier transform of an autocorrelation function $R_x(\tau)$ given by (Eq A3-14) [49].

$$R_x(\tau) = \int_{-\infty}^{\infty} S_N(2\pi f)e^{j2\pi f\tau}df \qquad \text{(Eq A3-14)}$$

The inverse Fourier transform of $S_N(\omega)$ can be calculated by performing a partial fraction expansion. Then, the integral may be evaluated by noting the result in (Eq A3-15) which equates (Eq A3-13) and (Eq A3-14).

$$R_x(0) = S_{N,OUT} = \int_{-\infty}^{\infty} S_N(2\pi f)df \qquad \text{(Eq A3-15)}$$

Begin by performing a partial fraction expansion of $S_N(\omega)$

$$S_N(\omega) = \frac{1}{2}k^2\overline{i_{n1}^2}\left[\frac{A}{j\omega+\omega_{cl}} + \frac{B}{-j\omega+\omega_{cl}}\right.$$
$$+\frac{C}{j\omega+\zeta\omega_n+j\omega_n\sqrt{1-\zeta^2}} + \frac{D}{j\omega+\zeta\omega_n-j\omega_n\sqrt{1-\zeta^2}} \qquad \text{(Eq A3-16)}$$
$$\left.+\frac{E}{-j\omega+\zeta\omega_n+j\omega_n\sqrt{1-\zeta^2}} + \frac{F}{-j\omega+\zeta\omega_n-j\omega_n\sqrt{1-\zeta^2}}\right]$$

Since there are symmetry relationships which can be exploited in the autocorrelation function, first compute $R_x(\tau)$ before evaluating the constants in the partial fraction expansion.

$$R_x(\tau) = \frac{1}{2}k^2\overline{i_{n1}^2}\left[Ae^{-\omega_{cl}\tau}u(\tau) + Be^{\omega_{cl}\tau}u(-\tau)\right.$$
$$+Ce^{-\zeta\omega_n\tau-j\omega_n\tau\sqrt{1-\zeta^2}}u(\tau) + De^{-\zeta\omega_n\tau+j\omega_n\tau\sqrt{1-\zeta^2}}u(\tau) \qquad \text{(Eq A3-17)}$$
$$\left.+Ee^{\zeta\omega_n\tau+j\omega_n\tau\sqrt{1-\zeta^2}}u(-\tau) + Fe^{\zeta\omega_n\tau-j\omega_n\tau\sqrt{1-\zeta^2}}u(-\tau)\right]$$

Note the symmetry relationship in (Eq A3-18) [49].

$$R_x(\tau) = R_x^*(-\tau) \qquad \text{(Eq A3-18)}$$

The symmetry relationship in (Eq A3-18) implies the following relationships between the constants in the autocorrelation function.

$$B = A^* \qquad \text{(Eq A3-19)}$$

$$F = C^* \qquad \text{(Eq A3-20)}$$

$$D = E^* \qquad \text{(Eq A3-21)}$$

Substitute the results from (Eq A3-19) - (Eq A3-21) into the autocorrelation function from (Eq A3-17) and split the constants into real and imaginary parts.

$$\begin{aligned} R_x(\tau) = \frac{1}{2}k^2\overline{i_{n1}^2}\Big[&(A_R + jA_I)e^{-\omega_{c1}\tau}u(\tau) \\ &+ (A_R - jA_I)e^{\omega_{c1}\tau}u(-\tau) \\ &+ (C_R + jC_I)e^{-\zeta\omega_n\tau - j\omega_n\tau\sqrt{1-\zeta^2}}u(\tau) \\ &+ (D_R + jD_I)e^{-\zeta\omega_n\tau + j\omega_n\tau\sqrt{1-\zeta^2}}u(\tau) \\ &+ (D_R - jD_I)e^{\zeta\omega_n\tau + j\omega_n\tau\sqrt{1-\zeta^2}}u(-\tau) \\ &+ (C_R - jC_I)e^{\zeta\omega_n\tau - j\omega_n\tau\sqrt{1-\zeta^2}}u(-\tau)\Big] \end{aligned} \qquad \text{(Eq A3-22)}$$

Place the autocorrelation function into trigonometric form.

$$\begin{aligned} R_x(\tau) = \frac{1}{2}k^2\overline{i_{n1}^2}\Big\{&(A_R + jA_I)e^{-\omega_{c1}\tau}u(\tau) \\ &+ (A_R - jA_I)e^{\omega_{c1}\tau}u(-\tau) \\ &+ (C_R + jC_I)e^{-\zeta\omega_n\tau}\Big[\cos\left(\omega_n\tau\sqrt{1-\zeta^2}\right) - j\sin\left(\omega_n\tau\sqrt{1-\zeta^2}\right)\Big]u(\tau) \\ &+ (D_R + jD_I)e^{-\zeta\omega_n\tau}\Big[\cos\left(\omega_n\tau\sqrt{1-\zeta^2}\right) + j\sin\left(\omega_n\tau\sqrt{1-\zeta^2}\right)\Big]u(\tau) \\ &+ (D_R - jD_I)e^{\zeta\omega_n\tau}\Big[\cos\left(\omega_n\tau\sqrt{1-\zeta^2}\right) + j\sin\left(\omega_n\tau\sqrt{1-\zeta^2}\right)\Big]u(-\tau) \\ &+ (C_R - jC_I)e^{\zeta\omega_n\tau}\Big[\cos\left(\omega_n\tau\sqrt{1-\zeta^2}\right) - j\sin\left(\omega_n\tau\sqrt{1-\zeta^2}\right)\Big]u(-\tau)\Big\} \end{aligned} \qquad \text{(Eq A3-23)}$$

Since the noise of an amplifier is a real-valued random process, it must have a real valued autocorrelation function $R_x(\tau)$ [49]. This further constrains the constants in the partial fraction expansion.

$$A_I = 0 \tag{Eq A3-24}$$

$$\begin{aligned} &jC_I\cos\left(\omega_n\tau\sqrt{1-\zeta^2}\right) - jC_R\sin\left(\omega_n\tau\sqrt{1-\zeta^2}\right) \\ &+ jD_I\cos\left(\omega_n\tau\sqrt{1-\zeta^2}\right) + jD_R\sin\left(\omega_n\tau\sqrt{1-\zeta^2}\right) = 0 \end{aligned} \tag{Eq A3-25}$$

Satisfying (Eq A3-25) is equivalent to satisfying the following relationships.

$$D_R = C_R \tag{Eq A3-26}$$

$$D_I = -C_I \tag{Eq A3-27}$$

Substitute (Eq A3-24), (Eq A3-26) and (Eq A3-27) back into the autocorrelation function and simplify the result.

$$\begin{aligned} R_x(\tau) = \frac{1}{2}k^2\overline{i_{n1}^2}\Big\{ & A_R e^{-\omega_{c1}\tau}u(\tau) + A_R e^{\omega_{c1}\tau}u(-\tau) \\ & + 2C_R e^{-\zeta\omega_n\tau}\cos\left(\omega_n\tau\sqrt{1-\zeta^2}\right)u(\tau) \\ & + 2C_I e^{-\zeta\omega_n\tau}\sin\left(\omega_n\tau\sqrt{1-\zeta^2}\right)u(\tau) \\ & + 2C_R e^{\zeta\omega_n\tau}\cos\left(\omega_n\tau\sqrt{1-\zeta^2}\right)u(-\tau) \\ & - 2C_I e^{\zeta\omega_n\tau}\sin\left(\omega_n\tau\sqrt{1-\zeta^2}\right)u(-\tau)\Big\} \end{aligned} \tag{Eq A3-28}$$

Note that the autocorrelation function should be continuous at $\tau=0$.

$$R_x(\tau) = \frac{1}{2}k^2\overline{i_{n1}^2}\Big[A_R e^{-\omega_{cl}|\tau|} + 2C_R e^{-\zeta\omega_n|\tau|}\cos\left(\omega_n|\tau|\sqrt{1-\zeta^2}\right) + 2C_I e^{-\zeta\omega_n|\tau|}\sin\left(\omega_n|\tau|\sqrt{1-\zeta^2}\right)\Big] \qquad \text{(Eq A3-29)}$$

The constants A_R, C_R, and C_I can be calculated by equating terms in ω between (Eq A3-12) and (Eq A3-16) and noting the symmetry relationships that have been developed throughout this appendix. Since this procedure requires extensive algebraic manipulations, a symbolic manipulation program was employed and the results are shown in (Eq A3-30) - (Eq A3-32).

$$A_R = \frac{(-\omega_{cl}^2 + z^2)^2}{2\omega_{cl}z^4(\omega_{cl}^4 + 2\omega_{cl}^2\omega_n^2 - 4\zeta^2\omega_{cl}^2\omega_n^2 + \omega_n^4)} \qquad \text{(Eq A3-30)}$$

$$C_R = \frac{\omega_{cl}^2\omega_n^4(1-4\zeta^2) + \omega_n^6 + 2\omega_{cl}^2\omega_n^2z^2 + 2\omega_n^4z^2 + \omega_{cl}^2z^4 + \omega_n^2z^4(1-4\zeta^2)}{8\zeta\omega_n^3z^4(\omega_{cl}^4 + 2\omega_{cl}^2\omega_n^2 - 4\zeta^2\omega_{cl}^2\omega_n^2 + \omega_n^4)} \qquad \text{(Eq A3-31)}$$

$$C_I = \frac{\omega_{cl}^2\omega_n^4(3-4\zeta^2) + \omega_n^6 + 2\omega_{cl}^2\omega_n^2z^2 - 2\omega_n^4z^2 - \omega_{cl}^2z^4 - \omega_n^2z^4(3-4\zeta^2)}{-8\omega_n^3z^4\sqrt{1-\zeta^2}(\omega_{cl}^4 + 2\omega_{cl}^2\omega_n^2 - 4\zeta^2\omega_{cl}^2\omega_n^2 + \omega_n^4)} \qquad \text{(Eq A3-32)}$$

It is now possible to calculate the total amplifier output noise power from (Eq A3-29).

$$S_{N,OUT} = R_x(0) = \frac{1}{2}k^2\overline{i_{n1}^2}(A_R + 2C_R) \qquad \text{(Eq A3-33)}$$

Plug the appropriate constants into (Eq A3-33) and multiply by a factor of two for the case of a fully-differential amplifier.

$$S_{N,OUT} = \left(\frac{g_{m1}g_{m3}g_{m9}}{C_2C_T^2}\right)^2 \frac{8kT}{3}(g_{m1}+g_{m7}) \left[\frac{2\zeta\omega_{cl}^2\omega_n^3 + \omega_{cl}\omega_n^4 + 2\omega_{cl}\omega_n^2 z^2 + \omega_{cl}z^4 + 2\zeta\omega_n z^4}{4\zeta\omega_{cl}\omega_n^3 z^4(\omega_{cl}^2 + 2\zeta\omega_{cl}\omega_n + \omega_n^2)}\right] \quad \text{(Eq A3-34)}$$

Note the result from (Eq A3-6) which can be used for further simplification of (Eq A3-34).

$$\frac{\omega_{cl}^2\omega_n^4}{f^2} = \left(\frac{g_{m1}g_{m3}g_{m9}}{C_2C_T^2}\right)^2 \quad \text{(Eq A3-35)}$$

Now perform further simplification of (Eq A3-34).

$$S_{N,OUT} = \frac{2kT}{3f^2 g_{m1}}\left(1+\frac{g_{m7}}{g_{m1}}\right) \left[\frac{\omega_{cl}\omega_n(2\zeta\omega_{cl}^2\omega_n^3 + \omega_{cl}\omega_n^4 + 2\omega_{cl}\omega_n^2 z^2 + \omega_{cl}z^4 + 2\zeta\omega_n z^4)}{\zeta z^4(\omega_{cl}^2 + 2\zeta\omega_{cl}\omega_n + \omega_n^2)}\right] \quad \text{(Eq A3-36)}$$

Combine (Eq A3-5) and (Eq A3-6) to obtain a result which can be used to further simplify (Eq A3-36).

$$fg_{m1} = \frac{\omega_{cl}\omega_n}{2\zeta\omega_{cl}+\omega_n}C_C \quad \text{(Eq A3-37)}$$

Perform simplification of (Eq A3-36).

$$S_{N,OUT} = \frac{2kT}{3fC_C}\left(1+\frac{g_{m7}}{g_{m1}}\right) \left[\frac{(2\zeta\omega_{cl}^2\omega_n^3+\omega_{cl}\omega_n^4+2\omega_{cl}\omega_n^2z^2+\omega_{cl}z^4+2\zeta\omega_nz^4)(2\zeta\omega_{cl}+\omega_n)}{\zeta z^4(\omega_{cl}^2+2\zeta\omega_{cl}\omega_n+\omega_n^2)}\right] \quad \text{(Eq A3-38)}$$

Redefine the normalized quantities for the pole and zero positions.

$$z = \gamma\zeta\omega_n \quad \text{(Eq A3-39)}$$

$$\omega_{cl} = \alpha\zeta\omega_n \quad \text{(Eq A3-40)}$$

Apply the normalization to (Eq A3-38) to finish calculating the total output referred noise.

$$S_{N,OUT} = \frac{2kT}{3fC_C}\left(1+\frac{g_{m7}}{g_{m1}}\right) \left[\frac{(\alpha+2\alpha\zeta^2+2\alpha\zeta^2\gamma^2+2\zeta^4\gamma^4+\alpha\zeta^4\gamma^4)(1+2\alpha\zeta^2)}{\zeta^4\gamma^4(1+2\alpha\zeta^2+\alpha^2\zeta^2)}\right] \quad \text{(Eq A3-41)}$$

Note that in most practical designs the zeros are at significantly higher frequencies than the poles. This corresponds to $\gamma \to \infty$ in (Eq A3-41) which results in the following output noise equation:

$$S_{N,OUT} = \frac{2kT}{3fC_C}\left(1+\frac{g_{m7}}{g_{m1}}\right)\left[\frac{(2+\alpha)(1+2\alpha\zeta^2)}{(1+2\alpha\zeta^2+\alpha^2\zeta^2)}\right] \quad \text{(Eq A3-42)}$$

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