PROGRAMMABLE, HIGH-DYNAMIC RANGE SIGMA-DELTA A/D CONVERTER FOR MULTISTANDARD, FULLY-INTEGRATED CMOS RF RECEIVER

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Memorandum No. UCB/ERL M98/75

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
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by
Kelvin Boo-Huat Khoo

Master of Science in Electrical Engineering
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Professor Paul R. Gray, Advisor

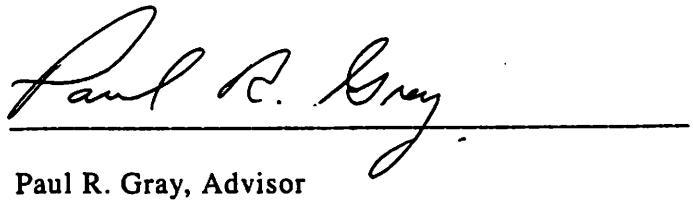
Abstract

A major focus of recent RF transceiver IC designs has been to increase both the integration and adaptability to multiple RF communication standards. Performing channel selection on chip at baseband allows the use of high-integration receiver architectures, and enhances programmability to different channel bandwidths and dynamic range requirements of multiple RF standards. A wideband, high-dynamic range sigma-delta modulator can be used to digitize both the desired signal and potentially stronger adjacent-channel interferers. In the digital domain, the decimation filter following the ADC can be easily made programmable.

A 4th-order sigma-delta ADC which is capable of adapting to GSM (cellular) and DECT (cordless) communication standards is described. The ADC achieves 14 bits of resolution at 128x oversampling ratio (200kS/s Nyquist rate) for GSM, and 12 bits of

resolution at 32x oversampling ratio (1.4MS/s Nyquist rate) for DECT. Power reduction strategies are developed at both the sigma-delta architecture and circuit design levels. The experimental prototype, fabricated in a 0.35μm CMOS process, dissipates 70mW from a 3.3V supply.

Approved by:



Paul R. Gray, Advisor

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Chapter 1

Introduction

1.1 Motivation

The explosive growth in the wireless communications industry has fueled recent research efforts to increase both integration and adaptability/programmability in radio-frequency (RF) transceiver design [1][2][3][4][5][6][7][8][9][10][11].

The circuitry of a current cellular telephone is shown in Figure 1.1. It comprises multiple chips and discrete components which are fabricated in different technologies (GaAs, Bipolar and CMOS). One of the goals of this research is to integrate these components onto a single chip in standard CMOS technology, exploiting the performance of modern deep submicron processes. Such a fully-integrated, single-chip solution results in personal communications devices with lower cost and smaller form factor.

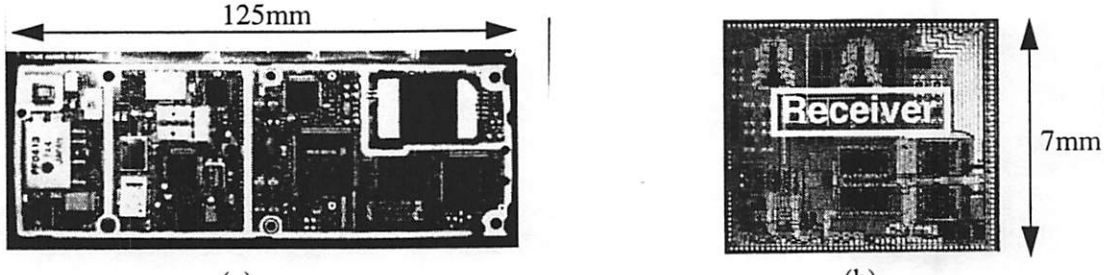


Fig. 1.1: RF Receiver Integration. (a) Commercially-implemented multi-chip approach (including DSP) (b) Single-chip solution (without RF filter and DSP)

Wireless Applications/Services	RF Standards
Cellular Telephony	GSM, E-GSM PCS 1900, DCS 1800 CDMA, Wideband CDMA AMPS
Cordless Telephony	DECT, etc.
Wireless LAN	IEEE 802.11 Bluetooth, HomeRF
Satellite	GPS, Iridium, GlobalStar

Table 1.1: Major wireless applications and RF standards associated with each application

The increasing variety of wireless applications, coupled with the proliferation of communications standards for these applications--each with its own set of signal bandwidth, blocking profile, and dynamic range and intermodulation requirements--motivate the second goal of this research. Implementing two or more wireless standards in a transceiver design enhances the functionality and flexibility of the personal communications device.

New architectures and circuit techniques need to be explored in the design of fully-integrated, multistandard RF transceivers. One of the more notable challenges lies in the design of low-power, high dynamic range baseband blocks which will coexist on the same substrate as the RF front-end components. The wide dynamic range is necessitated by the elimination of discrete high-Q SAW filters in traditional receivers. In addition, baseband circuits need to adapt to the different dynamic range, linearity and signal bandwidth requirements of multiple communications standards. This programmability can be easily achieved by performing channel selection in the digital domain.

In moving channel selection to the digital domain, a high dynamic range, wideband analog-to-digital converter (ADC) is needed to quantize a small desired signal in the presence of stronger adjacent-channel blockers and interferers. Sigma-delta ($\Sigma\Delta$) modulators are

uniquely suited to this application because the high-pass-shaped quantization noise falls into the same band as the blockers [12]. This implies that a single programmable digital decimation filter following the ADC can attenuate both the quantization noise and blockers.

1.2 Research Goals

The primary aim of this project is to design a programmable, high speed, high dynamic-range sigma-delta ADC for a fully-integrated, multistandard CMOS RF receiver. In particular, the ADC is designed to meet the requirements for (cellular) GSM, PCS 1900, DCS 1800, E-GSM and (cordless) DECT communications standards.

The results of this project are summarized below:

- Designed a sigma-delta modulator which meets the requirements for both cellular (GSM, PCS 1900, DCS 1800, E-GSM) and cordless (DECT) standards. An experimental prototype using a cascade of 2 second-order ΣΔ loops in a MASH configuration. is being fabricated in a 0.35μm double-poly, five-metal CMOS process. The ADC is realized on the same die as the other transceiver blocks (LNA, LO/VCO, mixers, power amplifier, continuous-time filter and DAC). The simulated dynamic range is 95dB and 85dB for GSM/PCS/DCS and DECT, respectively. The modulator dissipates 70mW at Nyquist rates of 200kS/s (GSM/PCS/DCS) and 1.4MS/s (DECT).

- Demonstrated that the same ΣΔ architecture, differing only in oversampling ratio, can be used to adapt to multiple communications standards.

- Developed a power-saving technique which permits the optimization of the first integrator for each of the standards.

- Designed a new fully-differential two-stage transconductance amplifier with an all-NMOS signal path and cascode compensation. This amplifier configuration eliminates the need for a level-shift between the two stages, and allows for the use of a low-power dynamic common-mode feedback.

- Showed that the ADC contributes less than 3% toward the receiver noise figure

1.3 Thesis Organization

Following this chapter, Chapter 2 provides an overview of RF system architectures and requirements. It will briefly review the fundamental operation of a conventional superheterodyne receiver, followed by a discussion on receiver architectures which emphasizes high-integration and multi-standard capability. Key receiver specifications and their impact on baseband circuits will be presented. The chapter concludes with motivations for utilizing a ΣΔ modulator in fully-integrated, multistandard receivers.

Chapter 3 introduces the fundamentals of oversampled sigma-delta modulator design. System-level trade-offs including single-loop versus cascade architectures, and continuous-time versus sampled-data modulators are discussed here.

System-level architecture design of the ADC is presented in Chapter 4. Issues such as the oversampling ratio selection, integrator gain factor, interstage gain mismatch and capacitor scaling are discussed. This is followed by simulated performance of the 2-2 MASH modulator.

Chapter 5 focuses the circuit implementation of the ΣΔ ADC, with an emphasis on low power optimization. Key trade-offs and challenges in the design of the transconductance amplifier, common-mode feedback network, sampling switches, biasing and digital circuits are discussed.

The simulated results of an experimental prototype of the 4th-order ADC is finally presented in Chapter 6.

Conclusions from this work are given in Chapter 7.

Chapter 2

System Architecture

2.1 Introduction

This chapter will review fundamental challenges and trade-offs in fully-integrated, multistandard receiver design. A discussion of the conventional Super-Heterodyne receiver architecture will be presented in the next section, followed by a discussion of alternative receiver architectures which are more amenable to single-chip integration and adaptability. The chapter concludes with a summary of receiver specifications and their impact on the baseband sections.

As mentioned in the previous chapter, each communications standard has its own set of requirements. The key figures of merit for wireless receivers are selectivity and sensitivity. Selectivity is a measure of the receiver's ability to select a weak desired channel in the presence of strong adjacent interferers. Sensitivity on the other hand refers to the minimum detectable signal in the presence of electronic noise. Both selectivity and sensitivity are measured at acceptable bit error rate (BER).

A receiver's sensitivity is determined by the RF front-end components while its selectivity by the channel-select blocks. Because channel selection in this project is performed

at baseband, the discussions in subsequent sections will emphasize the effect of the ADC's performance on the receiver selectivity.

2.2 Receiver Architectures

2.2.1 Super-Heterodyne

The conventional Super-Heterodyne architecture, shown in Figure 2.1, is widely implemented in existing commercial designs today. It benefits from the superior performance of external image-reject (IR) and intermediate-frequency (IF) channel-select filters. Because these filters perform channel selection at IF, only low to medium dynamic-range circuits are required at baseband. These discrete components, however, do not make the Super-Heterodyne architecture particularly amenable to higher levels of integration. In addition, the high-Q and low-phase noise associated with discrete inductors and varactor diodes used in the Voltage Controlled Oscillator (VCO) are difficult to realize in an integrated solution [2].

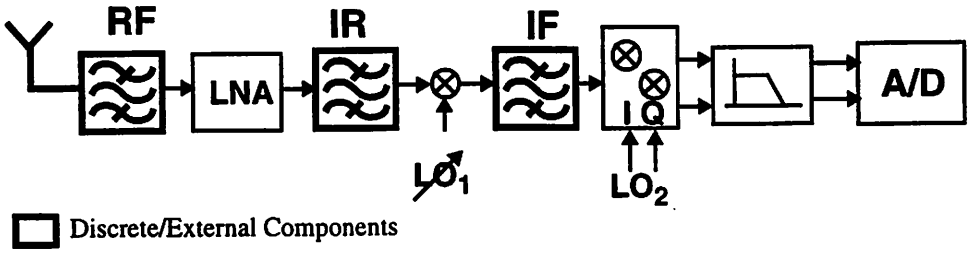


Fig. 2.1: Conventional Super-Heterodyne Receiver Architecture

2.2.2 Direct Conversion

An example of a receiver architecture which achieves high levels of integration is Direct Conversion [11]. The virtue of the Direct Conversion architecture is the elimination of discrete IR and IF filters. The incoming RF signal is directly translated down to baseband,

where channel selection is performed. Because no external components (with the exception of the RF filter) are needed in this architecture, and because channel-selection is performed at baseband, Direct Conversion receivers are more amenable to both high-integration and multi-standard capabilities.

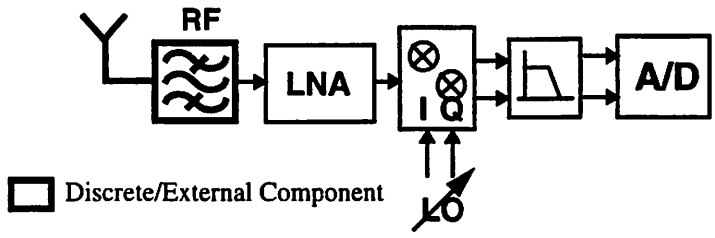


Fig. 2.2: Direct Conversion (Homodyne) Receiver Architecture

The Direct Conversion architecture has its share of disadvantages. Because the LO is tuned to the same frequency as the incoming RF frequency, there may be LO leakage back to the antenna. This unintentional transmission of the LO signal may reflect off nearby objects and be "re-received." This undesired LO signal then self-mixes with the local oscillator, causing a time-varying or wandering DC offset at the mixer output [2].

Additional DC offsets can be caused by second-order intermodulation of the adjacent-channel blockers. These offsets, coupled with low-frequency 1/f noise, degrade the dynamic range of the receiver. Moreover, a high-frequency, low phase-noise, channel-select frequency synthesizer is difficult to implement with the relatively low-Q elements which are available on-chip.

2.2.3 Low-IF Single-Conversion

The Low-IF architecture [5] alleviates many of the DC offset and low-frequency noise problems of Direct Conversion receivers, while preserving many of the high-integration and multi-mode characteristics. Instead of translating the desired channel down to DC, the Low-IF

architecture mixes the desired band to a low intermediate frequency--typically one or two channel bandwidths away from DC--to avoid the said DC offset and 1/f noise problems.

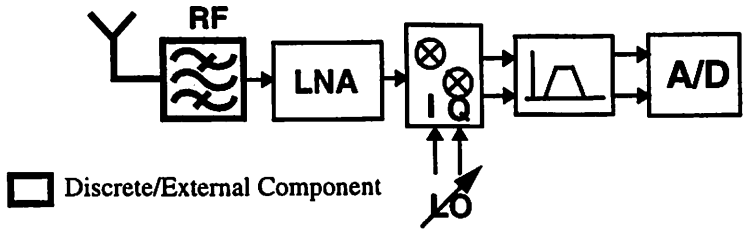


Fig. 2.3: Low-IF Single-Conversion Architecture

The Low-IF architecture sets a number of constraints on the performance of baseband blocks. Alternate channel blockers are folded in closer to the desired carrier, making it more difficult to filter out the out-of-channel energies. Since the desired signal is a channel or two away from DC, a wider bandwidth ADC is needed to digitize the signal. A higher-order filter and a wider bandwidth ADC result in higher power consumption for the receiver, which is contrary to the goals of this research.

2.2.4 Wideband IF with Double Conversion

The Wideband IF with Double Conversion (WIFDC) architecture [3] used in this research is another example of a receiver which is amenable to high integration and adaptability. Like the conventional Super-Heterodyne architecture, WIFDC employs a two-step conversion from RF to IF and from IF to DC. WIFDC differs from the Super-Heterodyne receiver in that the second, lower frequency LO is made programmable to select the desired band. This somewhat relaxes the phase noise requirements of the local oscillators. At the same time, this architecture mitigates the DC offset errors caused by LO self mixing. This relaxes the offset requirements of the A/D converter at baseband.

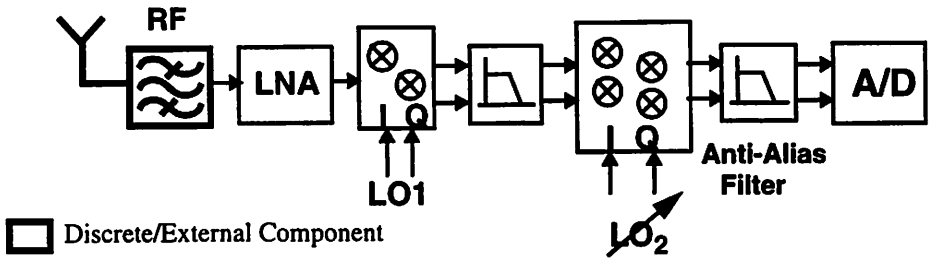


Fig. 2.4: Wideband IF with Double Conversion Architecture

	Super-Heterodyne	Direct Conversion	Low-IF Single-Conversion	Wideband IF Double Conversion
Integration	LOW	HIGH	HIGH	HIGH
Multi-Standard Capability	LOW	HIGH	MEDIUM	HIGH

Table 2.1: Comparison of Receiver Architectures from a standpoint of Integration and Multi-Standard Capability

Table 2.1 above summarizes the four architectures described earlier in terms of their potential for high-integration and multi-standard capability.

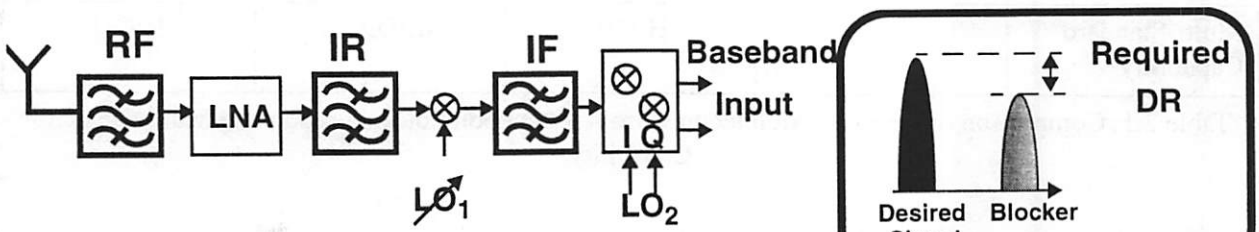
2.3 Baseband Processing

Now that suitable RF receiver architectures have been presented, a discussion on the functionality and trade-offs in the design of baseband components will follow. The discussions in this section are generic toward any of the high-integration architectures presented in the previous section.

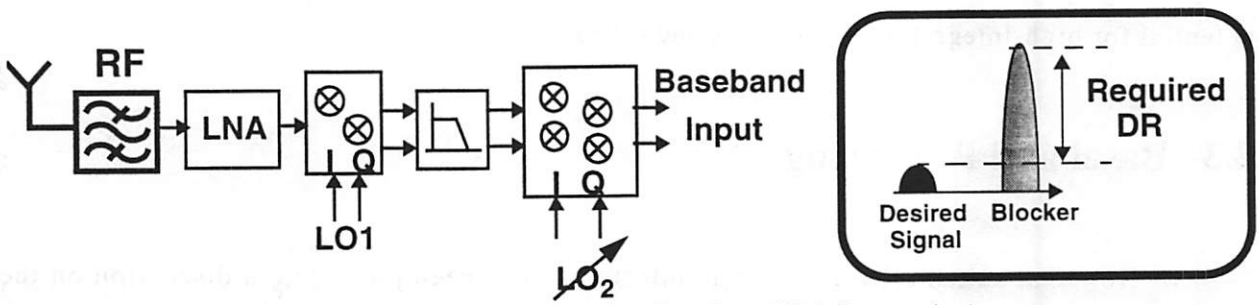
To enhance receiver adaptability, channel selection should be performed at baseband. This indicates that, unlike traditional receivers, both the desired channel and strong adjacent channels will be present at the input to baseband. As a result, the dynamic range required at

baseband is significantly higher than would have otherwise been required in traditional receivers.

Figure 2.5 illustrates this increased dynamic range requirement for baseband blocks in highly-integrated receivers. In a conventional Super-Heterodyne receiver, the combination of discrete high-Q filters performs channel selection at intermediate frequency (IF) and therefore significantly reduces the required dynamic range of baseband circuits. The elimination of such filters in high-integration architectures like Direct Conversion, Low-IF or WIFDC imposes a more challenging requirement at baseband, where channel selection is performed. The ADC needs to quantize a small desired signal in the presence of strong adjacent blockers.



(a) Super-Heterodyne Receiver (Low-Integration)



(b) Wideband IF with Double Conversion Receiver (High-Integration)

Fig. 2.5: Increased Baseband Dynamic Range Requirement in Highly-Integrated Receivers

Several options exist for performing channel selection at baseband. The following sections will explore the advantages and disadvantages of the options, with emphasis on low-power, multi-standard design.

2.3.1 Analog Channel Selection

Channel-select filtering can be done in the analog domain with the use of a high-order, high dynamic range switched-capacitor filter [19]. This filter serves to attenuate adjacent-channel energies while providing some automatic gain control (AGC) on the desired channel in order to further reduce the dynamic range requirement of subsequent stages. Typically, the ADC following the switched-capacitor filter is required to have only 7-8 bits of resolution. A frequency plan of analog channel select is given in Figure 2.6.

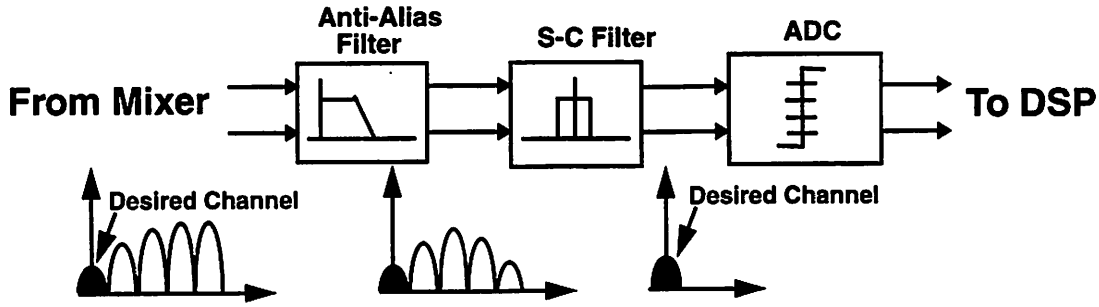


Fig. 2.6: Frequency Plan for Analog Channel Selection at Baseband of a Fully-Integrated Receiver

2.3.2 Digital Channel Selection

Alternatively, baseband channel selection can be performed in the digital domain using a digital finite-impulse-response (FIR) filter following the ADC. Because there will be minimal filtering of the RF spectrum prior to the digital filter, we need a wideband ADC which can quantize both the desired signal and the adjacent-channel blockers. In addition, the ADC needs to have a wide dynamic range to accommodate the large blockers described earlier. The advantage of digital channel selection is the increased multi-standard adaptability afforded by the ease of programming the filter in the digital domain.

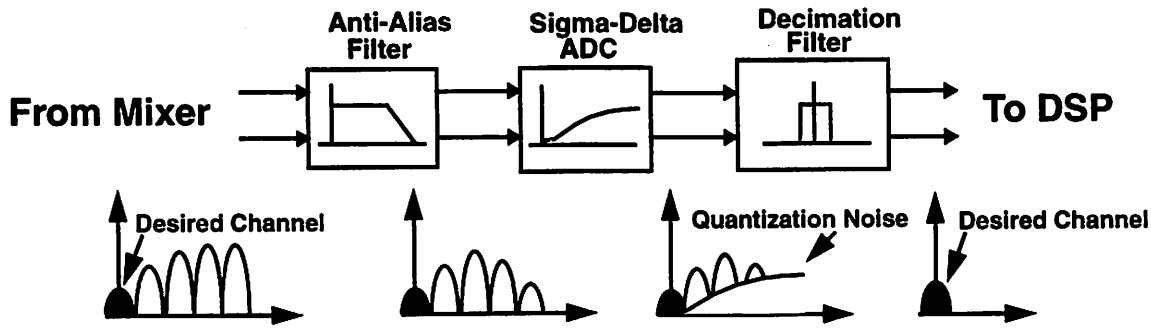


Fig. 2.7: Frequency Plan for Digital Channel Selection at Baseband of a Fully-Integrated Receiver

2.3.3 Mixed-Signal Channel Selection

A combination of analog and digital filtering may be used to achieve an acceptable compromise between programmability and relaxed ADC requirements. A low- to moderate-dynamic range switched-capacitor filter is typically used to relax the noise and intermodulation requirements of the ADC. This is then followed by a digital programmable filter..

An obvious question is the optimum amount of analog and/or digital filtering for any particular system in order to minimize power dissipation and silicon area. Power and area trade-offs between analog (switched-capacitor) and digital implementations of signal processing functions were examined in detail by Nishimura [20]. His results, shown in Figure 2.8, are applicable for the case of RF baseband processing applications. It should be noted, however, that the graph shows a very generalized trend, and that both power and area are significantly impacted by implementation details such as filter and A/D architectures, circuit techniques and technology.

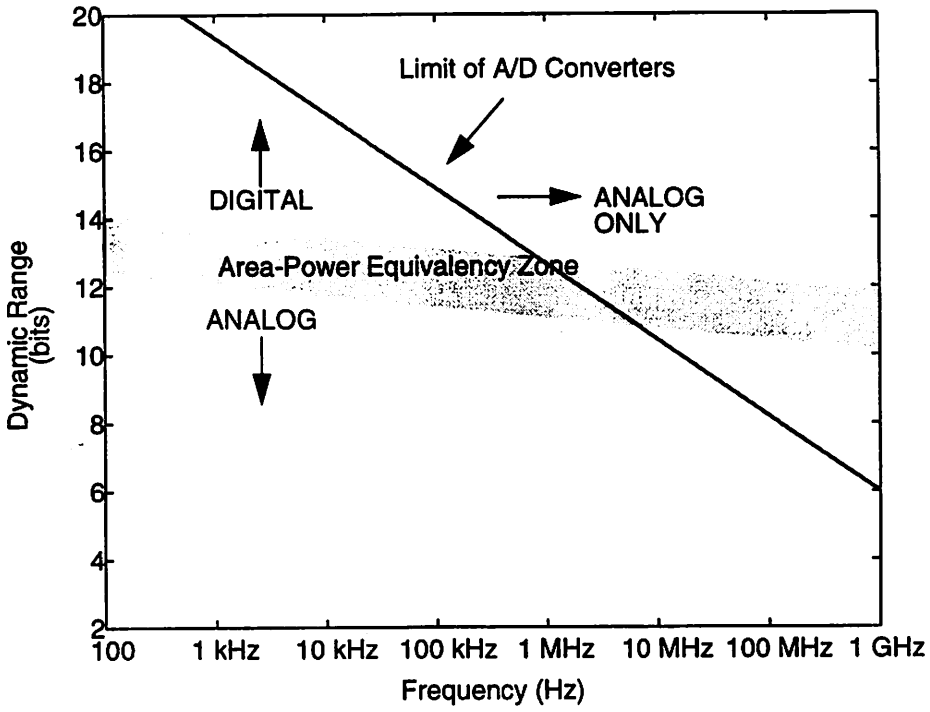


Fig. 2.8: Preferred Areas of Operation for Analog and Digital Signal Processors

It can be observed that baseband channel selection for GSM, where the signal bandwidth is 100kHz and the required resolution is 14 bits, favors a digital solution. For a wider bandwidth system with lower dynamic range requirements like DECT (12-bit resolution and 700kHz bandwidth), a mixed-signal approach is favorable.

2.4 Receiver and ADC Specifications

The system specifications for various RF communications standards used today are given in Table 2.3 [13]. Based on the noise, intermodulation, and blocking performance requirements of the receiver, the specifications for each individual block in the receiver chain can be derived [13].

The requirements for the ADC at baseband of the Wideband IF Double Conversion receiver can be determined in a similar fashion by charting out the various signal and blocker

levels going down the receiver chain. Figure 2.9 illustrates this for cellular GSM/DCS/PCS standards. The required dynamic range, for example, is the difference between the largest signal at the ADC input and the allowable noise floor. The noise floor is dictated by the receiver noise figure and the desired ADC noise contribution toward this noise figure. For GSM/DCS/PCS, a receiver noise figure of 3.9dB (from the LNA input to the ADC output) is targeted, and it is desirable that the ADC contribution to the noise figure is minimal.

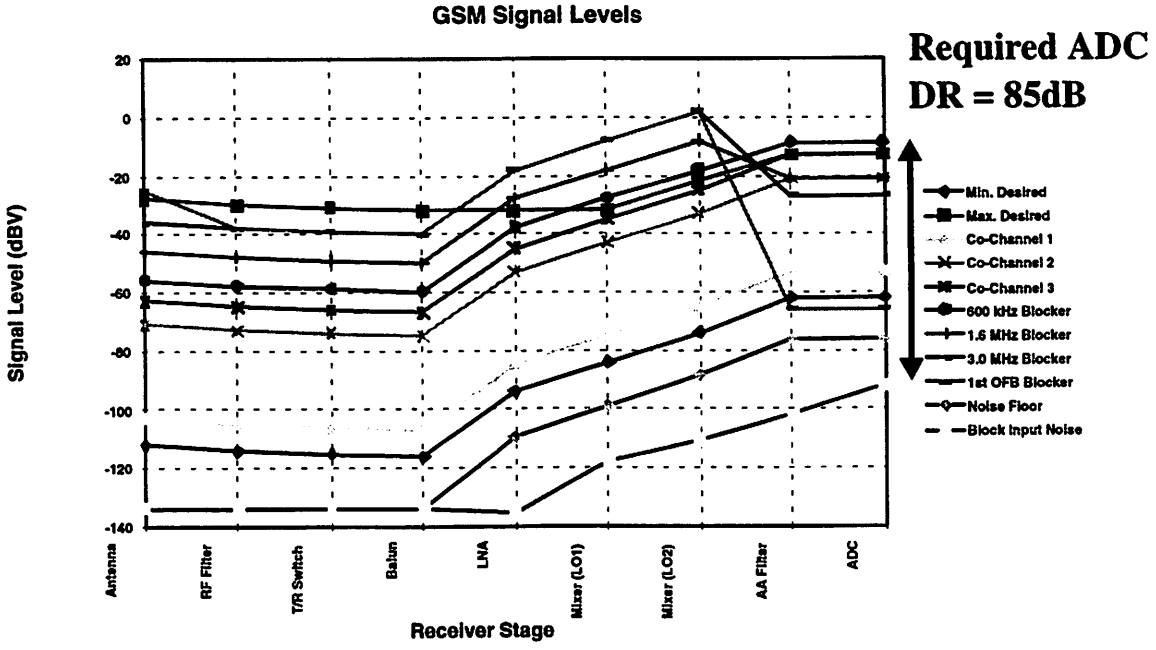


Fig. 2.9: All possible GSM signal levels at Various Stages of the Receiver Chain

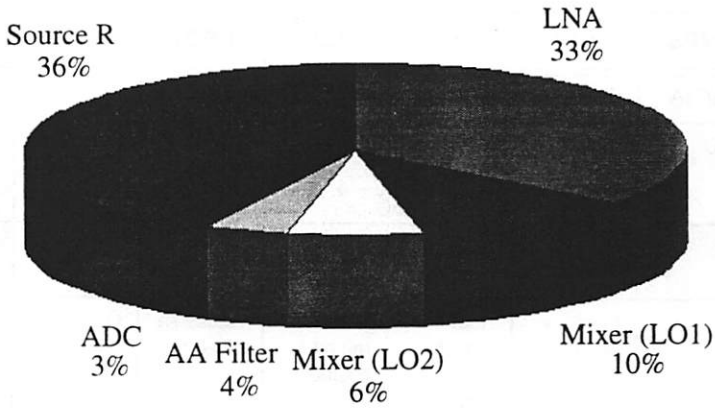


Fig. 2.10: Receiver Noise Contribution

The ADC design specifications for both cellular GSM/DCS1800/PCS1900 and cordless DECT standards at baseband of the WIFDC receiver are given in Table 2.2 below. It can be observed that the dynamic range and intermodulation requirements for the ADC in fully-integrated receivers are significantly higher than those for the conventional Super-Heterodyne receiver.

	GSM/DCS1800/PCS1900	DECT
Signal Bandwidth	100kHz	700kHz
Dynamic Range	86dB	72dB
Intermodulation: Input-Referred 3rd-Order Intercept Point (IIP3)	22V	
Power	Minimize	Minimize

Table 2.2: Summary of ADC Design Specifications

Parameter	AMPS	IS54	GSM	JCP	DECT	CT2	PHP	802.11FH
Origin	EIA/TIA	EIA/TIA	ETSI		ETSI	UK	Japan	IEEE
Access	FDD	FDM/ FDD/ TDM	FDM/ FDD/ TDM		FDM/ TDM/ TDD	FDM/ TDD	TDM/TDD	FH/FDM
Modulation	FM	pi/ 4QPSK	GMSK, diff	pi/ 4DQPSK	GFSK	GFSK	pi/4DQPSK	(G)FSK
Baseband filter		Root raised cosine	Root raised cos. beta=0.3	Root raised cosine	Gaussian BT=0.5	Gaussian BT=0.5	Root Nyquist alpha=0.5	500khz LP
Data rate per RF channel	NA	48kb/sec (2bits/ symbol)	270.8 kb/sec	42kb/sec (2bits/ symbol)	1.152 Mb/sec	72kb/sec	384kb/sec	1Mb/sec/ 2Mb/sec
FM Deviation	3kHz	NA	NA	NA	288kHz	14.4-25.2kHz	NA	~150kHz
RF Channel frequencies	824.04-848.97 (Tx) 869.04-893.97 (Rx)	824.04-848.97 (Tx) 869.04-893.97 (Rx)	890-915 (Tx) 935-960 (Rx)		0:1897.344Mhz, 9:1881.792Mhz	1:864.15 Mhz 40:868.05Mhz	1895-1911MHz	2.4-2.5GHz
No of RF Channels	833	833	124	1600	10	40	52	75
Channel Spacing	30kHz	30kHz	200kHz		1.728 MHz	10kHz	300kHz	1MHz
Synthesizer switching speed	slow	slow			30us(BS) 450us (HS)	1ms (ch-ch) 2ms	30us(BS) 1.5ms(HS)	several us
Frequency Accuracy	2.5ppm	200hz			50kHz	10kHz	3ppm	
Speech channels/RF channel	1	3	8/16 (full/half rt)	3/6 (full/half rt)	12/24 (full/half rt)	1/1 (full/half rt)	4/8 (full/half rt)	NA
Speech coding	Analog com-panded	VCELP 8kb/s	RELP-LTP 13kb/sec	VCELP 8kb/sec	32kb/s ADPCM	32kb/s ADPCM	32kb/s ADPCM	NA
Frame Length	NA	40ms			10ms(12 Tx+12Rx)	2ms (1Tx+1Rx)	5ms (4Tx+4Rx)	
Peak Power :	3W (6max)	3W (6max)	3W (20max)		250mW	10mW	100mW	1 watt?
Power Control rqmt	7 steps	7 steps			no	no		no

Table 2.3: Comparison of Wireless RF Standards

2.5 Motivations for ΣΔ ADCs

Sigma-delta modulators are uniquely suited to fully-integrated RF baseband applications for a couple of reasons. First, because their quantization noise is shaped with a high-pass characteristic, most of the noise energies fall in the same band as the undesired blockers. The same digital decimation filter can therefore be used to attenuate both the quantization noise and the blockers [18]. Second, the same ΣΔ modulator architecture, differing only in oversampling ratio, can be used to adapt to the different dynamic range and bandwidth requirements of multiple RF standards. Chapter 3 reviews the fundamental concepts in sigma-delta modulators.

Chapter 3

Sigma-Delta Modulators

3.1 Introduction

This chapter will present a brief overview of key sigma-delta modulator concepts. ΣΔ modulators trade resolution in time for resolution in amplitude such that the use of imprecise analog circuits can be tolerated. Although commercial sigma-delta A/D and D/A converters have been in existence for more than a decade now, the primary application of such converters has been in digital audio. The narrow bandwidths in digital audio applications have made oversampled converters particularly appealing. It is only recently, as we benefit from the increased speed of submicron devices, that sigma-delta modulators are exploited for wider band systems such as wireless RF communications [12].

The first part of this chapter reviews quantization noise in data converters, and compares the noise spectrum for Nyquist-rate, oversampled, and sigma-delta converters. Different sigma-delta modulator structures are then described, with emphasis on dynamic-range improvement. Finally, trade-offs between single-loop and cascaded (MASH) architectures will be discussed. Readers are referred to [14][15][16][17][18] for a more comprehensive and in-depth review of oversampled ΣΔ design concepts and issues.

3.2 Quantization Noise

3.2.1 Nyquist-Rate Converters

Quantization of amplitude refers to the "mapping" of a continuous amplitude signal to a finite number of discrete levels, is at the heart of all digital modulators. The difference between the original continuous amplitude and the new "mapped" value represents the quantization error. Figure 3.1 illustrates the quantization process. Qualitatively, it can be observed that the quantization error gets smaller as the number of discrete levels increases. The number of levels is in turn proportional to the resolution of the quantizer used in the ADC. Increasing the quantizer resolution will decrease the quantization error.

The error is a strong function of the input; however, if the input changes randomly between samples by amounts comparable to or greater than the spacing of the levels, then the error is largely uncorrelated from sample to sample and has equal probability of lying anywhere in the range of $\pm\Delta/2$ [15]. Further, if it is assumed that the error has statistical properties which are independent of the signal, the error can then be represented by a noise.

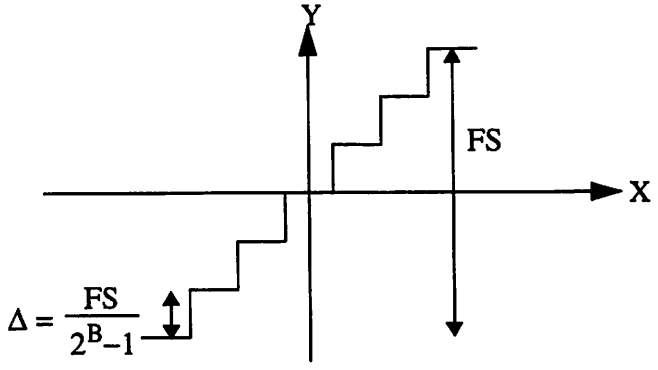


Fig. 3.1: Quantization Process

The quantization noise is given by the mean-square value of the quantization error described above. Using a double-sided spectrum, the quantization noise is given by

$$P_{Q,\,Nyquist} = \frac{1}{\Delta} \cdot \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} q^2 dq = \frac{\Delta^2}{12} \qquad \text{(Eq 3-1)}$$

and is assumed to fall between $-f_s/2$ and $+f_s/2$, where f_s is the sampling frequency. In Nyquist-rate converters, the sampling frequency is usually twice the signal bandwidth.

3.2.2 Oversampled Converters

Oversampled converters run at sampling frequencies greater than twice the signal bandwidth. From (Eq 3-1), the quantization noise power is independent of the sampling rate. As such, the quantization noise power in oversampled converters is the same as that for Nyquist-rate converters, but is now distributed over a wider band, as shown in Figure 3.2. The in-band quantization noise is shown by the shaded region, and is given by

$$P_{Q,\,Oversampled} = \int_{-f_{BW}}^{f_{BW}} \frac{\Delta^2}{12} \cdot \frac{1}{f_s} \cdot df = \frac{P_{Q,\,Nyquist}}{\left(\frac{f_s}{2f_{BW}}\right)} = \frac{P_{Q,\,Nyquist}}{M} \qquad \text{(Eq 3-2)}$$

where oversampling ratio, $M = f_s / 2f_{BW}$

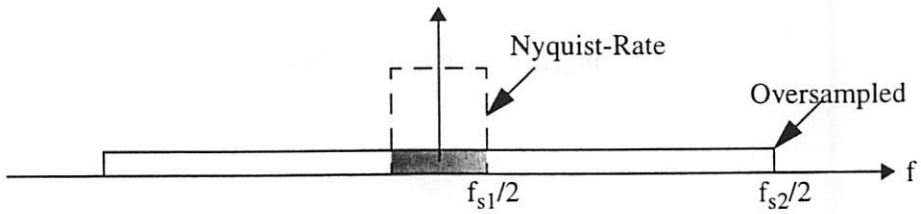


Fig. 3.2: Quantization Noise Spectrum in Nyquist-Rate and Oversampled Converters

Increasing the sampling rate therefore reduces the quantization noise power by a fraction M, which is equal to the oversampling ratio. The above analysis assumes that the quantization noise spectrum is white; however, this is not the case in practical systems. A complete modeling of the quantization noise as an additive white-noise source was performed by Bennett [23].

3.2.3 Sigma-Delta Converters

Sigma-delta modulators employs negative feedback in addition to oversampling to further reduce the in-band quantization noise. Figure 3.3 (a) shows a basic first-order sigma-delta modulator. Due to the negative feedback, the output Y will, on average, be force to equal the input signal X. By oversampling the input and then averaging the output, we can very accurately predict the input signal without the need for a high resolution quantizer.

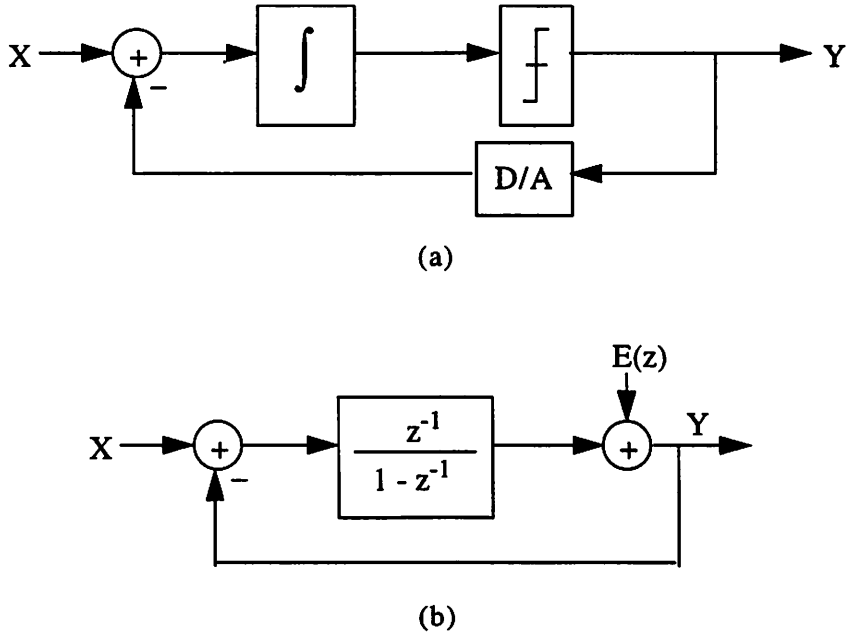


Fig. 3.3: 1st-Order Sigma-Delta Modulator: (a) Simplified Block Diagram (b) Linearized Model

The first-order sigma-delta modulator can be represented by the linearized model shown in Figure 3.3 (b). Since the transfer function from the quantization error source to the

output is given by $(1-z^{-1})$ the noise is shaped by a high-pass characteristic. This suppresses the in-band noise, as quantified by

$$P_{Q,\Sigma\Delta} = \int_{-f_{BW}}^{f_{BW}} \frac{P_{Q,Nyquist}}{M} \cdot (1-z^{-1})df \approx \frac{P_{Q,Nyquist}}{M^3} \cdot \frac{\pi^2}{3} \qquad \text{(Eq 3-3)}$$

for $M >> 1$

The feedback loop at the heart of sigma-delta modulators is clearly a noise-shaping filter which attempts to cancel the in-band quantization noise by predicting the value of the noise. Higher-order modulators can better predict (and therefore cancel) the in-band quantization noise. A simple feedback theory analysis will show that the transfer function from the quantization noise source to the output is given by $(1-z^{-1})^L$, where L is the order of the sigma-delta modulator. This is given by the equation below.

$$P_{Q,\Sigma\Delta} = \int_{-f_{BW}}^{f_{BW}} \frac{P_{Q,Nyquist}}{M} \cdot (1-z^{-1})^L df \approx \frac{P_{Q,Nyquist}}{M^{2L+1}} \cdot \frac{\pi^{2L}}{2L+1} \qquad \text{(Eq 3-4)}$$

for $M >> 1$

Below is a generalized equation for the in-band quantization in a L-order sigma-delta modulator. The dynamic range (with quantization noise being the only noise source) can be easily derived and is shown below.

$$DR_{\Sigma\Delta} = 10 \cdot \log\left[\frac{3}{2} \cdot (2^B - 1)^2 \cdot \frac{2L+1}{\pi^{2L}} \cdot M^{2L+1}\right] \qquad \text{(Eq 3-5)}$$

where B = resolution of quantizer
L = modulator order
M = oversampling ratio

It can be observed that the dynamic range can be increased by increasing the modulator order, the oversampling ratio, or the quantizer resolution. For every doubling of the oversampling ratio, the dynamic range increases by 3(2L+1) dB or (L+0.5) bits.

The disadvantage of using higher-order modulators (3rd-order or higher) is that the modulators may experience limit-cycle oscillations or instability. Techniques to overcome this problem are discussed in [15].

3.3 Loop Filter Topologies

This section aims to review the fundamentals of sigma-delta loop filter design; the topologies presented here are not intended to be an exhaustive in nature; rather, they only represent a cross-section of common commercially-implemented filter designs today. The modulator order is determined by the number of integrator stages in the forward path. In each of the filter topology below, the transfer function from the quantization-noise source to the output will be presented.

Figure 3.4 illustrates the distributed feedback filter topology for a 4th-order modulator. The output Y(z) is fed back to each of the four integrators through gain stages, a_1-a_4. The quantization noise transfer function, $H_e(z)$, to the output is given by

$$H_e(z) = \frac{(z-1)^4}{(z-1)^4 + a_4(z-1)^3 + a_3(z-1)^2 + a_2(z-1) + a_1} \qquad \text{(Eq 3-6)}$$

Note that all the zeros are at z = 1. In the frequency domain, this means the zeros are all at DC. The poles can be implemented using a Butterworth high-pass response for a maximally flat quantization noise spectrum at high frequency.

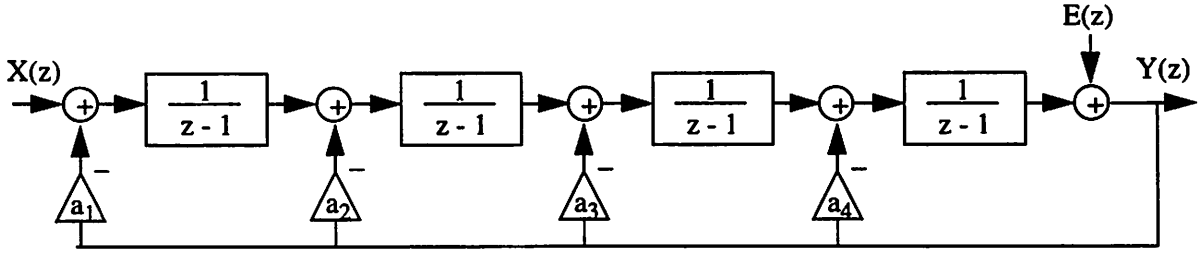


Fig. 3.4: Distributed Feedback Filter Topology

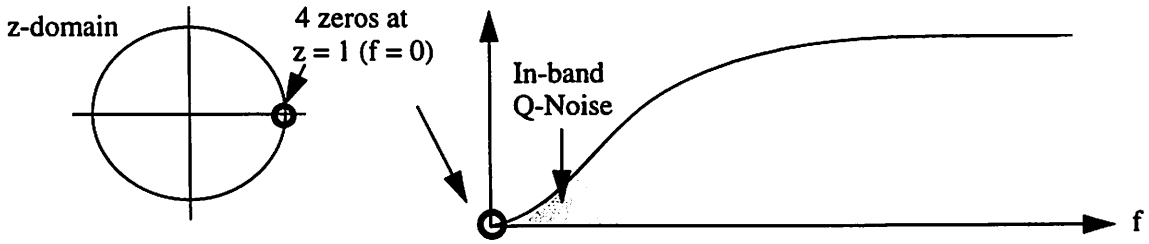


Fig. 3.5: Frequency Response of Distributed Feedback, Feedforward Summation Topologies

An "inverted" form to the previous topology is shown in Figure 3.6. The output of each integrator is gained and then summed together before feeding into the quantizer. It can be easily shown that the quantization noise transfer function is identical to that for the Distributed Feedback structure, and is given by (Eq 3-6).

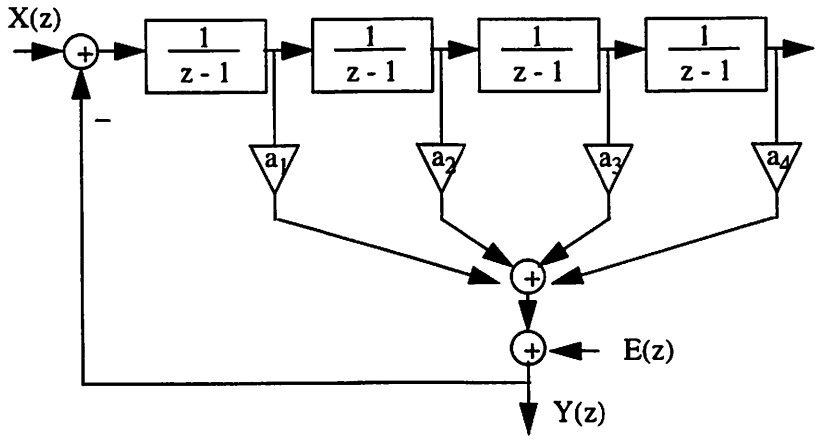


Fig. 3.6: Feedforward Summation Topology

An effective way of suppressing the in-band quantization noise is to spread the zeros over the signal bandwidth instead of placing them all at DC. This can be accomplished by adding local resonator feedback loops in either the distributed feedback or feedforward

summation topologies. The resonators create pairs of complex zeros which allow the use of an Inverse Chebychev response.

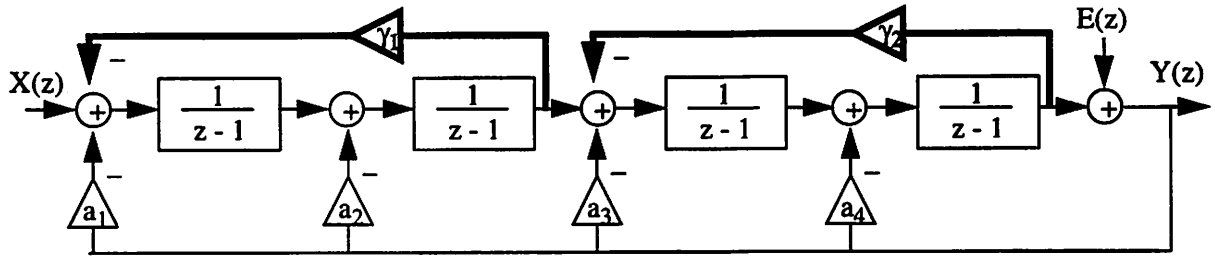


Fig. 3.7: Distributed Feedback with Local Resonator Feedback Topology

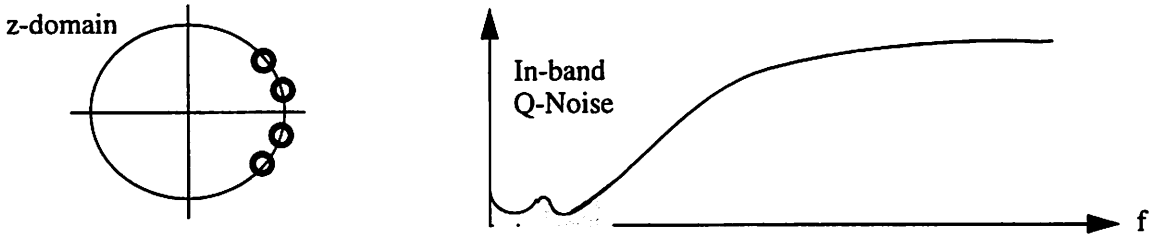


Fig. 3.8: Frequency Response for Distributed Feedback Topology with Local Resonator Feedbacks

3.4 Sampled-Data vs. Continuous-Time

Sigma-delta modulators can be implemented either as a sampled-data system or in the continuous-time domain. The primary difference is that sampled-data sigma-delta systems employ switched-capacitor integrators while continuous-time systems use active-RC integrators in the modulators. There are a number of advantages and disadvantages associated with each option, as will be discussed below.

Switched-capacitor integrators take advantage of fine-line VLSI capabilities by eliminating the need for physical resistors. On-chip resistors with very high linearity are difficult to achieve in standard CMOS process. In addition, resistors in continuous-time integrators need to be kept small to minimize thermal noise. For the same time-constant,

reducing the resistors implies that the feedback capacitors need to be increased. This may make the area prohibitively large and the capacitors impractical to realize on-chip.

The frequency response of switched-capacitor integrators can be more accurately predicted because the time-constant is a function of capacitor ratios (C_S/C_I) and of the sampling frequency [22]. The time-constant of continuous-time integrators, on the other hand, is a product of the resistor and the capacitor, and suffers severely from process variations. The absolute value of on-chip poly resistors typically vary by 30% from the nominal/desired value, whereas capacitor ratios are usually more well controlled (typical variation is only 1%).

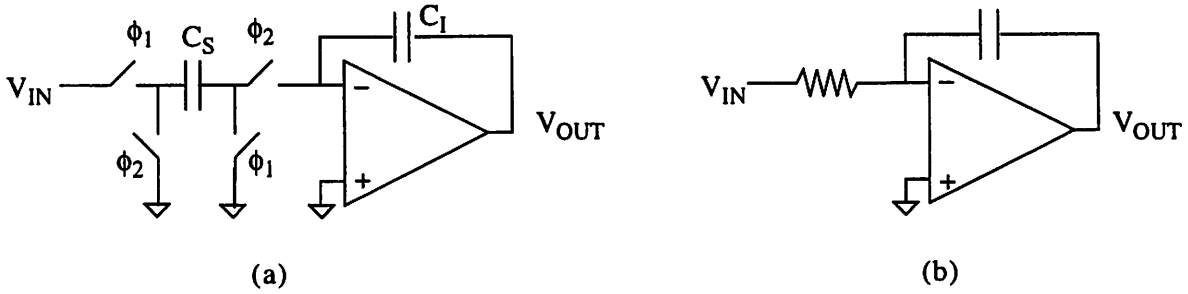


Fig. 3.9: (a) Switched-Capacitor Integrator (b) Continuous-Time Integrator

Another advantage of switched-capacitor sigma-delta systems is that they are less sensitive to clock jitter and to the manner in which the opamp settles [15]. As long as the opamp settles to the required accuracy, it does not matter whether the opamp slews or linearly settles. Continuous-time integrators, however, must be linear at all times.

Continuous-time systems have their share of advantages over sampled-data systems. Because the opamp in an active-RC integrator does not have to settle to full accuracy every half clock period, a very high oversampling ratio is achievable [21]. The oversampling ratio in switched-capacitor integrators is limited by the achievable bandwidths of the opamps. This makes continuous-time sigma-delta modulators very appealing for high-speed applications.

Finally, continuous-time systems eliminate the need for an anti-alias filter prior to the sigma-delta ADC. The anti-alias filter is needed in sampled-data systems to attenuate energies at multiples of the sampling frequency which may potentially fold down to baseband. The elimination of this filter results in significant power savings for the receiver.

3.5 Cascaded (MASH) Architecture

One of the solutions to the instability in high-order modulators is to cascade two or more low-order (1st- or 2nd-order) modulator stages. Stability is guaranteed as long as each individual loops is made stable. Figure 3.10 shows an example of a 2-2 architecture. The cascade of two 2nd-order loops effectively gives a 4th-order noise-shaping performance. With the exception of the first loop, the input to each loop is the quantization error from the preceding loop.

The outputs, Y_1 and Y_2, are fed into a digital cancellation network prior to the decimation filter. This cancellation network, based on a prediction of the analog interstage gain

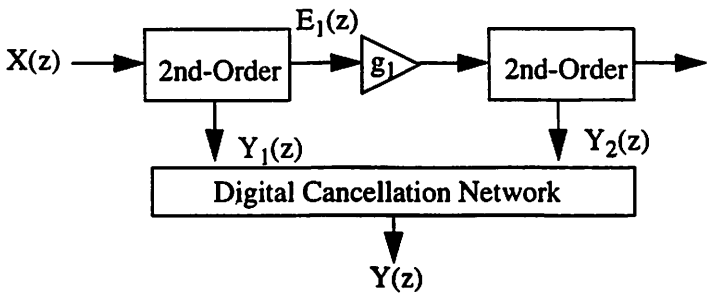


Fig. 3.10: Example of a 4th-order (2-2) MASH architecture

g_1, aims to cancel the quantization error from all but the last stage. The transfer functions from the input and the quantization-noise sources to the output are derived in the equations below.

$$Y_1(z) = z^{-2} \cdot X(z) + (1 - z^{-1})^2 \cdot E_1(z)$$

$$Y_2(z) = z^{-2} g_1 \cdot E_1(z) + (1 - z^{-1})^2 \cdot E_2(z)$$

$$\begin{aligned} Y(z) &= H_1(z) \cdot Y_1(z) + H_2(z) \cdot Y_2(z) \\ &= z^{-4} \cdot X(z) + z^{-2} \cdot (1 - z^{-1})^2 \cdot \left(1 - \frac{g_1}{\bar{g}_1}\right) \cdot E_1(z) - \frac{(1 - z^{-1})^4}{\bar{g}_1} \cdot E_2(z) \end{aligned} \quad \text{(Eq 3-7)}$$

where $H_1(z) = z^{-2}$

$$H_2(z) = -\frac{(1 - z^{-1})^2}{\bar{g}_1}$$

$H_1(z)$ and $H_2(z)$ are the coefficients of the digital cancellation network which will cancel out the quantization noise from the first modulator loop, $E_1(z)$. As can be observed in (Eq 3-7) above, the second term (E_1) will be effectively cancelled out if the analog gain g_1 matches the digital prediction of the gain $\bar{g}_1$.

The following sections will discuss sources of circuit nonidealities which cause the modulator to deviate from the ideal performance given by (Eq 3-5) and (Eq 3-7).

3.5.1 Interstage Gain Mismatch

The variation in the analog interstage gain, g_1, from its nominal (or digital) value, $\bar{g}_1$, is by far the most detrimental source of nonideality in MASH or cascaded modulator structures. From (Eq 3-7), it is clear that any mismatch between g_1 and $\bar{g}_1$ will not result in a complete cancellation of the quantization noise from the first loop, $E_1(z)$. In other words, interstage gain mismatch causes a leakage in quantization noise from the first loop to the output. For a 4th-order modulator, a 2-3% mismatch can result in 20-30dB increase in the in-band quantization

noise. In switched-capacitor circuits, this mismatch is determined by variations in capacitor ratios--and not the absolute values of resistors and capacitors as would be the case for continuous-time implementations.

3.5.2 Finite Opamp DC Gain

The analyses in Section 3.2 assume the use of perfect integrators in the modulator loop(s). The finite DC gain of operational amplifiers, however, causes the integrators to be leaky since the poles are shifted inside the unit circle, as shown in Figure 3.11. This effect can be quantified by

$$\frac{V_{OUT}}{V_{IN}}(z) = \frac{C_S}{C_I} \cdot \frac{z^{-1}}{1-(1-\varepsilon)\cdot z^{-1}} \qquad \text{(Eq 3-8)}$$

$$\text{where} \quad (1-\varepsilon) = \frac{1}{1+\frac{C_S}{C_I}\cdot\frac{1}{A_{DC}}}$$

From the standpoint of sigma-delta modulators, this translates into the leakage of quantization noise to the output. In addition, insufficient DC gain also degrades the linearity of the system. It should be noted that noise-shaping relaxes the DC gain requirements of the 2nd and subsequent opamps.

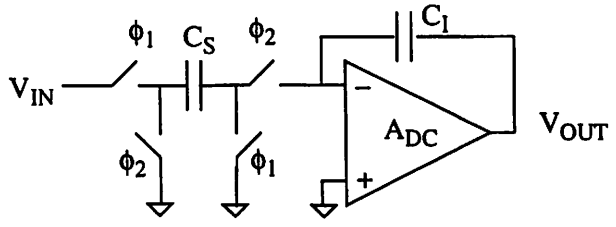


Fig. 3.11: Effect of Finite DC OpAmp Gain on Integrator Transfer Function

In a MASH or cascaded architecture, the shift in pole locations results in incomplete cancellation of the quantization noise from the first loop--similar to the effects of interstage

gain mismatch. This can be described by the equations below, where ε_1, ε_2, ε_3, and ε_4 are respectively the errors due to the finite DC gain of opamps 1, 2, 3 and 4.

$$Y_1(z) = z^{-2} \cdot X(z) + [1-(1-\varepsilon_1)z^{-1}] \cdot [1-(1-\varepsilon_2)z^{-1}] \cdot E_1(z)$$

$$Y_2(z) = z^{-2} \cdot g_1 \cdot E_1(z) + [1-(1-\varepsilon_3)z^{-1}] \cdot [1-(1-\varepsilon_4)z^{-1}] \cdot E_2(z)$$

$$\begin{aligned} Y(z) &= H_1(z) \cdot Y_1(z) + H_2(z) \cdot Y_2(z) \\ &= z^{-4} \cdot X(z) + \left\{ z^{-3}(1-z^{-1})(\varepsilon_1+\varepsilon_2) + z^{-4}(\varepsilon_1 \cdot \varepsilon_2) \right\} \cdot E_1(z) - \\ &\quad \left\{ \frac{(1-z^{-1})^2}{\hat{g}_1} [(1-z^{-1})^2 + z^{-1}(1-z^{-1})(\varepsilon_3+\varepsilon_4) + z^{-2}\varepsilon_3\varepsilon_4] \right\} E_2(z) \end{aligned} \qquad \text{(Eq 3-9)}$$

3.5.3 Incomplete Linear Settling and Slew Rate Limitation

The finite bandwidth of operational amplifiers translates into incomplete linear settling in the time domain when the amplifiers are used in switched-capacitor integrators (Figure 3.11). This causes an integrator gain error as shown below.

$$\frac{V_{OUT}}{V_{IN}}(z) \approx \frac{C_S}{C_I} \cdot \frac{z^{-1}}{1-z^{-1}} (1-\varepsilon_s) \qquad \text{(Eq 3-10)}$$

Ideal Gain — Integrator Xfer Funct. — Gain Error

where $\varepsilon_s = e^{-n_\tau} = 2^{-N}$ (Settling Error)

$n_\tau = -\ln(2^{-N})$ (Number of Time Constants)

$f_{FB} = \dfrac{C_I}{C_S + C_I}$ (Feedback Factor)

(Eq 3-10) above suggests that the higher the required resolution (N) of the ADC, the smaller the tolerable settling error will be. As will be shown in later chapters, this means that a higher bias current is needed in the amplifiers.

The gain error due to incomplete linear settling applies not only to the opamp bandwidth but also to the finite bandwidth of the switching network in the integrator, described below.

$$\frac{V_{OUT}}{V_{IN}}(z) = \frac{C_S}{C_I} \cdot \frac{z^{-1}}{1-z^{-1}} \cdot \left(1 - 2e^{-\frac{T_s}{4R_{ON}C_s}}\right) \qquad \text{(Eq 3-11)}$$

Ideal Gain — Integrator Xfer Funct. — Gain Error

where T_s = Sampling Period

R_{ON} = "On" Resistance of MOS Switch

C_S = Sampling Capacitor

This implies that we need a small switch on-resistance R_{ON} to minimize the gain error due to incomplete linear settling.

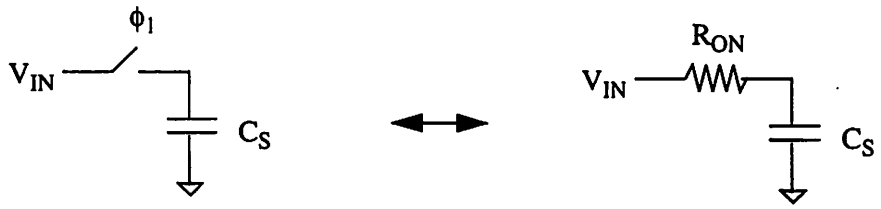


Fig. 3.12: Finite Bandwidth of Integrator Switching Network

Slew rate, on the other hand, results in harmonic distortion. Note that because the closed-loop unity-gain bandwidth of the amplifier is given by $(g_m/C_L)f_{FB}$ and its slew rate is given by I/C_L, and because the g_m/I ratio is relatively low in short-channel CMOS devices, linear settling requirements usually dictate the required opamp power dissipation.

3.6 Summary

This chapter reviewed important concepts in the design of sigma-delta modulators. The benefits of sigma-delta modulators as data converters were first presented, and were contrasted with conventional Nyquist-rate converters. The concept of noise-shaping was discussed. Next, various options for loop filter design were investigated, with emphasis on strategies to suppress the in-band quantization noise by spreading the zeros over the signal bandwidth. This was followed by a discussion on sampled-data versus continuous-time implementations. The chapter concluded with the MASH or cascaded architecture, and the circuit nonidealities which affect its performance. The implications and severity of the nonidealities will be presented in the next chapter.

Chapter 4

Modulator Design

4.1 Introduction

This chapter describes the architecture techniques which can be employed to enhance the system-level modulator performance. The 2-2 MASH architecture used in this design is then presented, along with a discussion on adaptability to both GSM/DCS and DECT standards. This is followed by a discussion on the selection of oversampling ratio and integrator gain factors. Simulation results which show noise shaping, SQNR and dynamic range of the modulator are then presented.

4.2 2-2 MASH (Cascaded) Architecture

A fourth-order modulator was selected because it was sufficient to achieve 14 bits of resolution for a 200kS/s Nyquist rate (GSM) and 12 bits of resolution for a 1.4MS/s Nyquist rate. The MASH architecture was selected over a single-loop 4th-order modulator because of its inherent stability. It must be noted, however, that the MASH architecture has its share of disadvantages, most notably its sensitivity to gain mismatch as discussed in Section 3.5.1.

A basic block diagram for the 2-2 architecture was shown in Figure 3.10. This is repeated in greater detail in Figure 4.1 below. Each integrator has a full clock delay between its

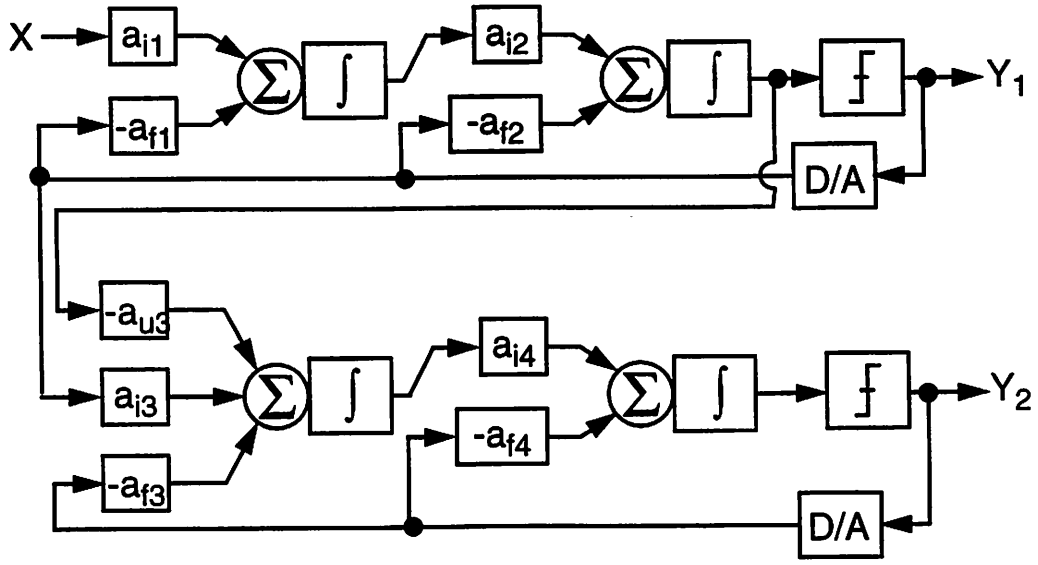


Fig. 4.1: 2-2 Cascaded Architecture Implementation

input and output to create a fully pipelined structure. Single-bit quantizers are used in each of the two cascaded loops because of their inherent linearity.

4.3 Signal Scaling

This section will describe strategies for selecting the gain factors in front of each integrator in the modulator. It is necessary to place appropriate attenuation factors to avoid clipping for large input signals. The goal of this signal scaling process is to maximize the overload level of the modulator by using all of the available swing at the output of each integrator without clipping [17].

Coefficient	Value
a_{i1}	0.2
a_{f1}	0.2
a_{i2}	0.5
a_{f2}	0.25
a_{u3}	0.5
a_{i3}	0.1
a_{f3}	0.2
a_{i4}	0.5
a_{f4}	0.25

Table 4.1: Integrator Gain Coefficients

The gain coefficients selected for the 2-2 cascaded modulator is summarized in Table 4.1 [18]. For this set of gain factors, it can be observed that all four integrators have approximately the same output overload level.

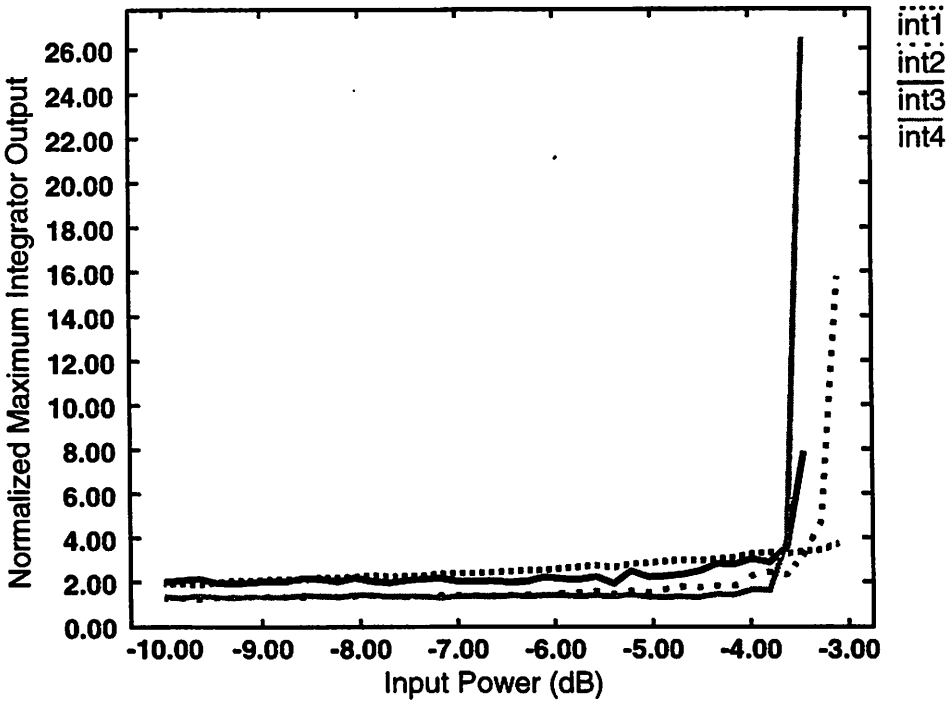


Fig. 4.2: Maximum Integrator Output Levels as a function of Input Power

4.4 Oversampling Ratio Selection

As mentioned in Chapter 3, increasing the oversampling ratio improves the dynamic range of the modulator. In switched-capacitor circuits, however, increasing the oversampling ratio also implies that the amplifier bandwidth needs to increase since the available time for settling ($T_s/2$ minus rise, fall, and 2-phase nonoverlap time) is reduced. The maximum achievable amplifier bandwidth is finite and is determined by the process technology.

The key is to therefore select the minimum oversampling ratio which yields the required performance. Circuit nonidealities which degrade the modulator performance should be included in any simulations to determine the required oversampling ratio. In addition, sufficient margins should be allocated for thermal and flicker noise if the system-level simulations account for quantization noise only. It is also worth mentioning that the oversampling ratio should be an integer which is a power of two, i.e. OSR = 2^x, to minimize power dissipation in the decimation filter following the ADC.

From system-level simulations, the required oversampling ratio to achieve 86dB of dynamic range for GSM is 128x, while that for DECT (72dB dynamic range) is 32x. The clock frequencies for GSM and DECT are 25.6MHz and 44.8MHz, respectively.

4.5 Power Optimization

One of the goals of any portable electronics systems is to minimize power dissipation. It is therefore important to identify the factors which affect the power budget in a sigma-delta

modulator. Most practical implementations employ the class A operational transconductance amplifier, the simplest form of which is the common-source amplifier shown in Figure 4.3.

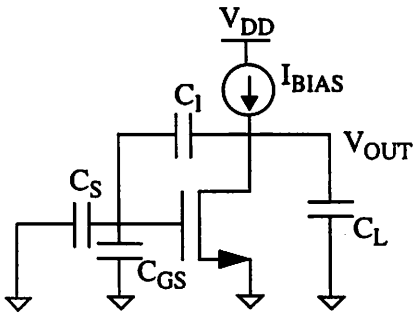


Fig. 4.3: Simplified Class A Amplifier Model

The static power dissipated in the amplifier is proportional to the supply voltage and the bias current.

$$P \propto V_{DD} \cdot I_{BIAS} \qquad \text{(Eq 4-1)}$$

Assuming that the device is biased at a fixed V_{GS}-V_{TH}, the bias current I_{BIAS} is therefore proportional to the device transconductance, g_m, as shown by the equation below.

$$P \propto V_{DD} \cdot g_m \qquad \text{(Eq 4-2)}$$

The closed-loop unity-gain bandwidth, ω_{UT}, of the amplifier is given by

$$\omega_{UT} = \frac{g_m}{C_{OUT}} \cdot f_{FB} \qquad \text{(Eq 4-3)}$$

where C_{OUT} is the total capacitance at the output of the amplifier, and f_{FB} is the feedback factor of the integrator.

$$C_{OUT} = \frac{C_I(C_S + C_{GS})}{C_I + C_S + C_{GS}} + C_L \approx \frac{C_I C_S}{C_I + C_S} \qquad \text{(Eq 4-4)}$$

$$f_{FB} = \frac{C_I}{C_I + C_S} \qquad \text{(Eq 4-5)}$$

Substituting (Eq 4-4) and (Eq 4-5) into (Eq 4-3) yields

$$\omega_{UT} = \frac{g_m}{C_S + C_{GS}} \approx \frac{g_m}{C_S} \qquad \text{(Eq 4-6)}$$

Substituting (Eq 4-6) back into (Eq 4-2) allows us to rewrite the power dissipated in the amplifier as a function of the unity-gain bandwidth and the sampling capacitor, as shown below.

$$P \propto V_{DD} \cdot \omega_{UT} \cdot C_S \qquad \text{(Eq 4-7)}$$

The dynamic range of the integrator is the ratio of the input signal power to the noise power. Assuming that the input can swing from ground to V_{DD}, and that the noise floor is dominated by thermal noise, the dynamic range can be approximated by

$$DR = \frac{P_{IN}}{P_{NOISE}} \approx \frac{\left(\frac{V_{DD}^2}{8}\right)}{\left(\frac{kT}{M \cdot C_S}\right)} \qquad \text{(Eq 4-8)}$$

where M, the oversampling ratio, is the ratio of the sampling frequency to the Nyquist frequency (f_s/f_N).

The unity-gain bandwidth, ω_{UT}, can be rewritten in terms of the sampling frequency as shown below.

$$\omega_{UT} = \frac{1}{\tau} = \frac{1}{\left(\frac{T_s}{2n_\tau}\right)} = 2n_\tau f_s = 2[-\ln(2^{-N})]f_s \qquad \text{(Eq 4-9)}$$

By reorganizing terms and substituting (Eq 4-8) and (Eq 4-9) back into (Eq 4-7), the static power limit can be written in the form

$$P \propto \frac{DR \cdot f_N}{V_{DD}} \qquad \text{(Eq 4-10)}$$

The static power is proportional to the required dynamic range and the Nyquist frequency, and is inversely proportional to the supply voltage. It is interesting to consider the different requirements for GSM and DECT standards, and their implications on the power consumption. The required dynamic range for GSM is approximately four times (12dB) greater than that for DECT, but the Nyquist rate for DECT signals is seven times greater than that for GSM. (Eq 4-10) suggests that, using the same ADC for the two standards, the power dissipation in the ADC will be limited by the DECT standard due to its wider bandwidth.

The latter suggests that the trend toward lower supplies favored by digital circuits and required by deep submicron CMOS process will have an adverse effect on power dissipation of the modulator [18]. It is interesting to note that the power is independent of the sampling frequency and oversampling ratio, assuming the devices operate in the forward active region.

4.6 Noise-Shaping and Capacitor Scaling

One strategy to minimize power dissipation is to take advantage of noise-shaping in sigma-delta modulators to scale down the capacitors (and bias currents) in later integrators in the modulator chain. The thermal and flicker noise of the 2nd integrator, when referred to the ADC input, is shaped with a 1st-order high-pass characteristic; the noise from the 3rd integrator has a 2nd-order shaping, and so on. In general, the minimum sampling capacitors is determined by the required kT/C noise, without being limited by parasitic capacitors.

The total input-referred thermal noise as a function of the input-referred thermal noise of each integrator is given by

$$P_{N,tot} = P_{N1}\left(\frac{1}{M}\right) + P_{N2}\left(\frac{\pi^2}{3A_2^2M^3}\right) + P_{N3}\left(\frac{\pi^4}{5A_3^2M^5}\right) + P_{N4}\left(\frac{\pi^6}{7A_4^2M^7}\right) \qquad \text{(Eq 4-11)}$$

where P_{Ni} = Input-referred noise of i-th integrator
A_i = DC gain from ADC input to input of i-th integrator

The integrator input-referred thermal noise will be discussed later in Section 5.2.2.

Increasing the oversampling ratio M significantly relaxes the noise requirement of subsequent stages. In a system like GSM where the low bandwidth permits a high oversampling ratio of 128x, only the first stage in the cascade contributes significantly to the total thermal noise of the ADC. Wider bandwidth systems like DECT do not allow the luxury of a high oversampling ratio. As such, more than one integrator will contribute to the ADC input-referred thermal noise.

Besides thermal noise, noise shaping in sigma-delta modulators also relaxes flicker noise and settling requirements of later integrators in the cascade. This further permits the scaling of capacitors, transistor sizes and bias currents in the 2nd, 3rd and 4th integrators. Figure 4.4 shows that the capacitor scaling technique results in a net power savings of 250%.

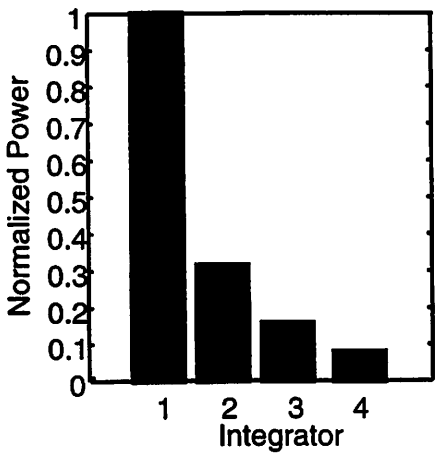


Fig. 4.4: Power Savings afforded by Noise Shaping

In the next section, the relaxed settling requirements in sigma-delta modulators will be illustrated.

4.7 Linear Settling and Slew Rate

The linear settling and slew rate requirements of each of the integrators in the cascade can be quantified by system level simulations [17]. For simplicity, a single-pole model of the

opamp is used for the simulations; actual designs which employ more complicated 2-stage amplifiers must leave significant margins from these results. Figure 4.5 shows the peak SNDR

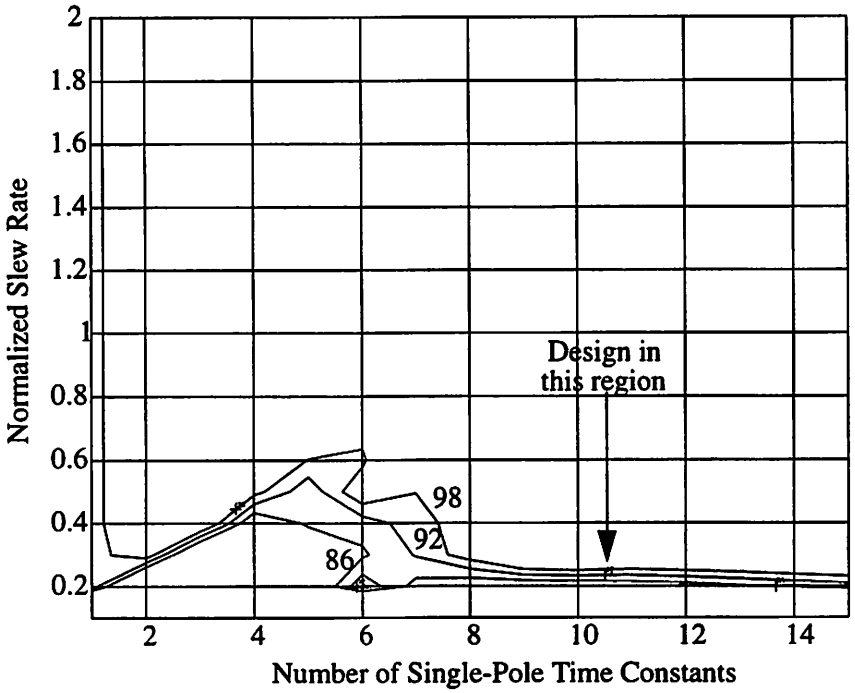


Fig. 4.5: Contours of Peak SNDR as a function of Slew Rate and Settling Time for 1st Integrator

of the first integrator as a function of various combinations of slew rate and linear settling accuracy for an oversampling ratio of 128x. It is desirable for the integrator to be designed for the flat region where performance is independent of small shifts in amplifier settling accuracy.

The settling error is defined to be the departure of the output from the value it would achieve with an infinite amount of time for settling. From (Eq 3-10), this settling error is given by

$$\varepsilon_s = e^{-n_\tau} \qquad \text{(Eq 4-12)}$$

The slew rate shown in Figure 4.5 can be denormalized to a physical slew rate specification for the amplifier by

$$SR = 2(SR_N)V_{DAC}f_s \qquad \text{(Eq 4-13)}$$

V_{DAC} denotes the differential DAC reference levels and f_s the sampling frequency.

A summary of the required slew rate and the tolerable settling error for each of the integrators are summarized in Table 4.2 for both GSM and DECT.

	GSM Standard		DECT Standard	
	Slew Rate	Settling Error	Slew Rate	Settling Error
OpAmp 1	150V/μs	0.0061%	260V/μs	0.0244%
OpAmp 2	150V/μs	1.83%	260V/μs	0.248%
OpAmp 3	135V/μs	Negligible	230V/μs	1.83%
OpAmp4	120V/μs	Negligible	200V/μs	Negligible

Table 4.2: Summary of Slew Rate and Linear Settling Specifications

4.8 Simulated Results

The simulated performance of the 2-2 MASH or cascaded architecture will now be presented. Recall that the required oversampling ratio for GSM is 128x and that for DECT is 32x. The left curve in Figure 4.6 illustrates the signal-to-quantization-noise (SQNR) as a function of input power for an ideal 4th-order modulator. The peak SQNR is approximately 145dB while the simulated dynamic range is 140dB.

As discussed in Section 3.5, a number of circuit imperfections cause the modulator performance to deviate from this ideal prediction. The right curve on the same figure takes into account such circuit imperfections. It assumes a finite opamp DC gain of 66dB, a settling error of 0.003% in the first opamp, a slew rate of 150V/μs and an interstage gain mismatch of 2.5%.

This results in a degradation of about 35dB in dynamic range. It should be noted that the dominant cause of dynamic range degradation is the interstage gain mismatch. With a dynamic range of 110dB, the quantization noise floor is still ensured to be at least 20dB below the thermal noise floor. This margin will accommodate any possible in-band "tones" in the quantization noise spectrum.

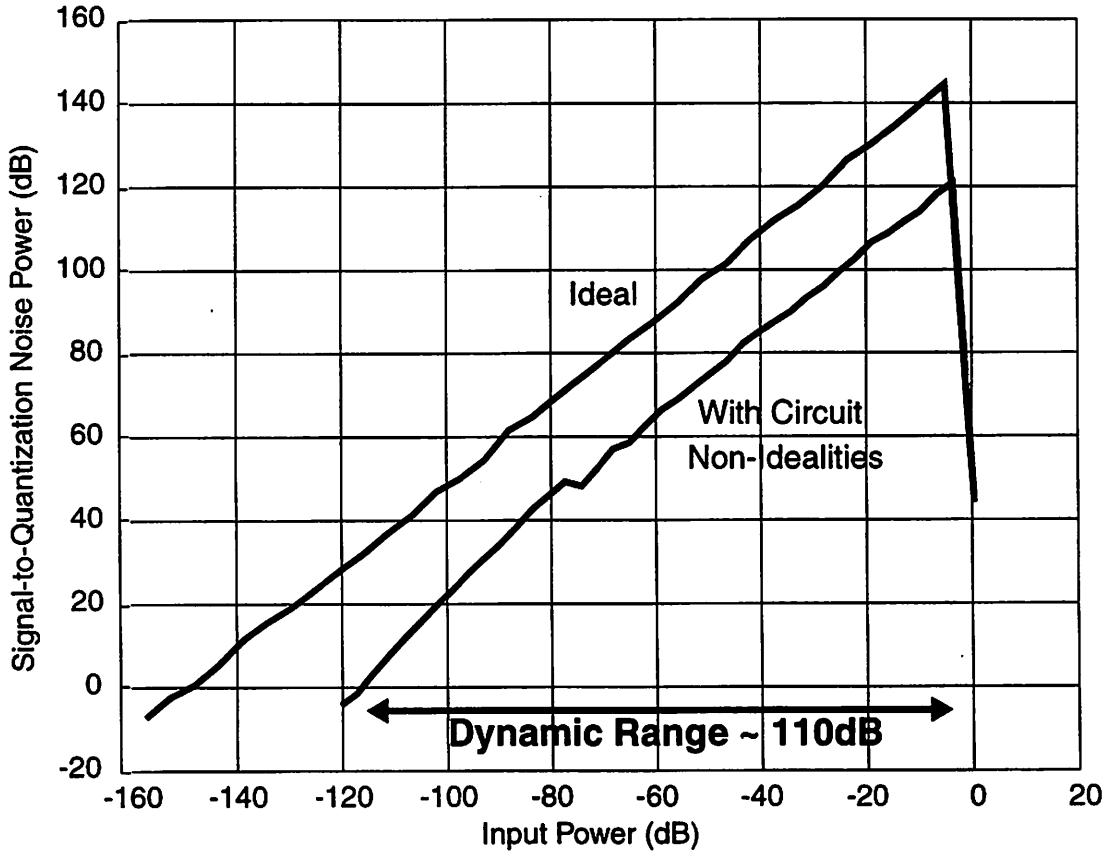


Fig. 4.6: Simulated Signal-to-Quantization Noise of 2-2 MASH Architecture for GSM (OSR = 128x)

A similar plot of SQNR for the DECT standard is shown in Figure 4.7. The left curve illustrates the ideal performance of the 2-2 cascade modulator with an oversampling ratio of 32x. The same nonidealities as those described in the previous paragraph were then included in

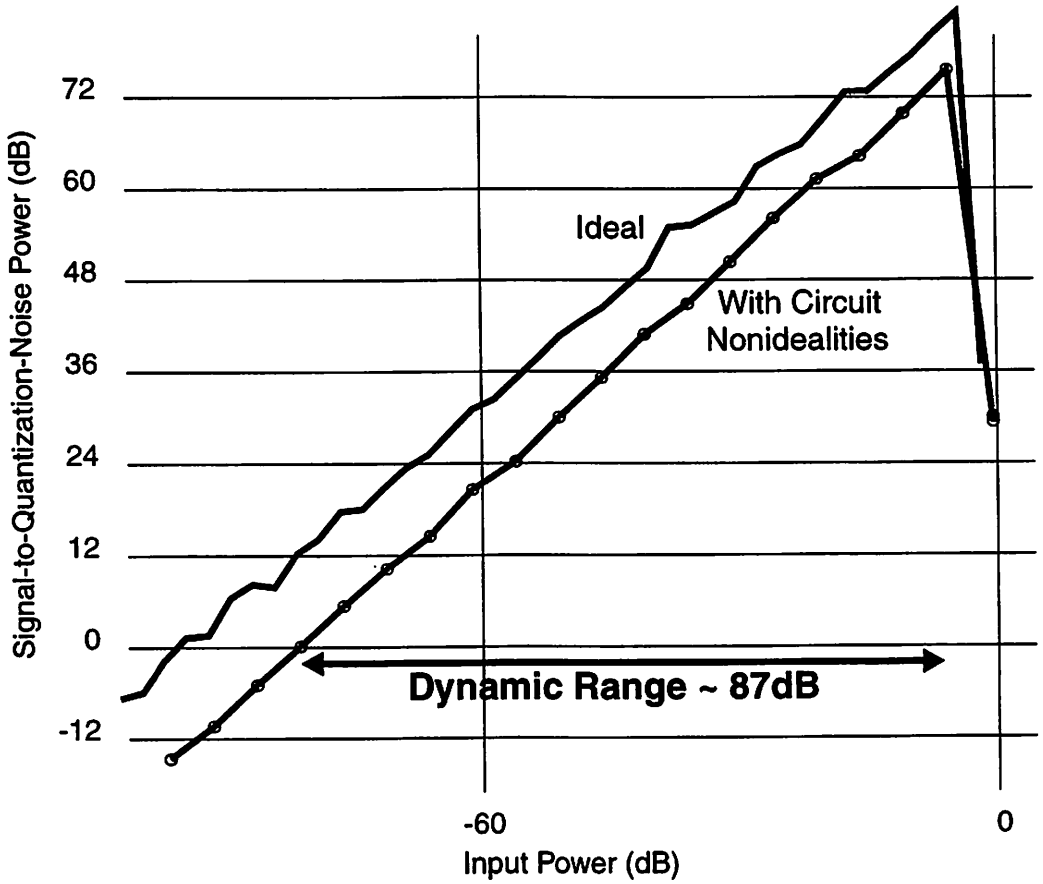


Fig. 4.7: Simulated Signal-to-Quantization Noise of 2-2 MASH Architecture for DECT (OSR = 32x)

the simulations. The nonideal modulator performance is shown on the right curve. The quantization noise floor is kept about 15dB below the required thermal noise floor.

Finally, the FFT plot for the modulator with a 100kHz-input is shown in Figure 4.8.

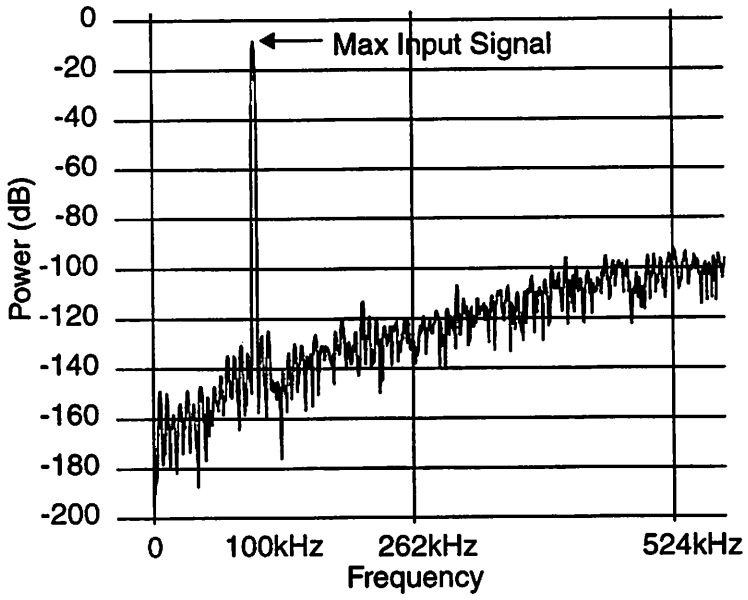


Fig. 4.8: FFT Output Plot of the 2-2 Cascade Architecture for GSM (M = 128)

Chapter 5

Integrator and Amplifier Design

5.1 Introduction

This chapter explores design tradeoffs and power-optimization strategies for key circuit blocks which are at the heart of the sigma-delta modulator. These include switched-capacitor integrators, operational transconductance amplifiers (OTA), bias networks, comparators, digital output buffers, and two-phase clock generation circuitry. An experimental prototype of the 2-2 MASH ΣΔ modulator implemented in a 0.35μm double-poly, five-metal 3.3V CMOS process will be described.

5.2 Integrator Design

The experimental prototype comprises four switched-capacitor integrators. Figure 5.1 illustrates the first integrator in the cascade. The integrator is implemented in a fully-differential configuration and employs a two-phase nonoverlapping clock, the latter of which is shown in Figure 5.2. The input is sampled during phase 1 (ϕ_1 and ϕ_{1d}). During phase 2, the charge is transferred from the sampling capacitor (C_S) to the integrating capacitor (C_I). At the same time, depending on the output value, the appropriate DAC reference level is applied by closing either switches labeled ϕ_{2d1} or ϕ_{2d2}.

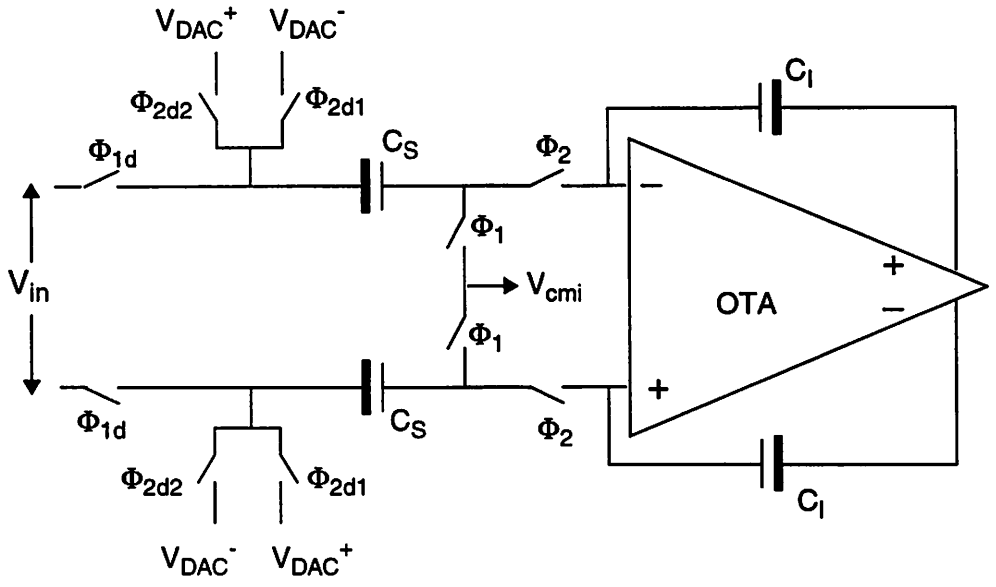


Fig. 5.1: Fully-differential switched-capacitor integrator

The integrator employs the bottom-plate sampling technique to minimize signal-dependent charge-injection [22]. This is achieved through delayed clocks: ϕ_{1d}, ϕ_{2d1} and ϕ_{2d2}. When switches labeled ϕ_1 are first turned off, the charge injection from those switches remains, to a first order, independent of the input signal. Because one of plates is now floating, turning off switches labeled ϕ_{1d} shortly after does not introduce charge-injection errors.

Recall from Figure 4.1 and Table 4.1 that the feedforward and feedback gains of the first integrator are respectively 0.2 and -0.2. This allows the sharing of the sampling capacitors for the feedforward and feedback paths in order to minimize the loading on the amplifier summing node and maximize the feedback factor. This reduces power dissipation in the amplifier.

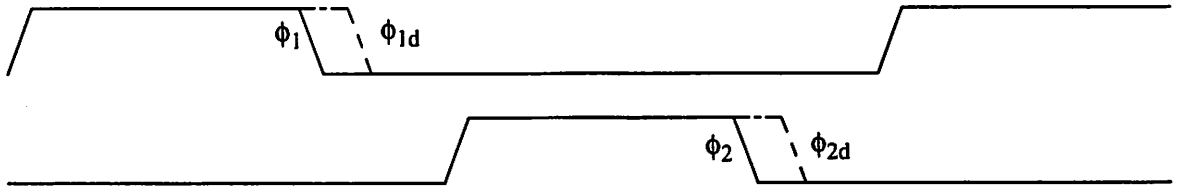


Fig. 5.2: 2-Phase Nonoverlap Clock

5.2.1 Switches

Linearity is an important factor in the design of the switches. From Figure 5.3, it is desirable to operate in a region where the on resistance of the switch is independent of the input voltage. The switches used in the integrator are implemented with complementary MOS devices because the DC voltages are biased at mid-supply. Alternatively, gate boasting

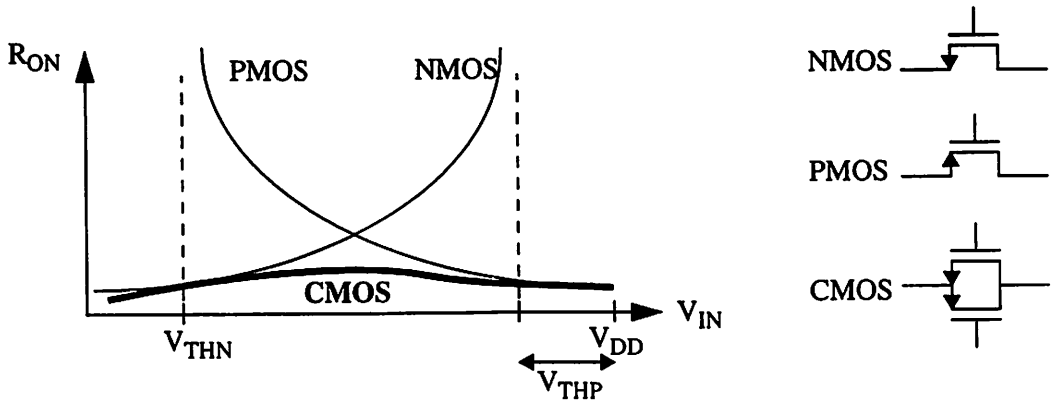


Fig. 5.3: Switch On-Resistance as a Function of the Input Voltage

techniques using charge pumps may be employed to keep a constant on resistance [18]; however the process for which this experimental prototype is designed does not permit voltages above V_{DD}.

In CMOS switches, the sizing of the NMOS and PMOS devices is critical. The parallel combination of the NMOS and PMOS devices yields an effective resistance given by

$$R_{ON,\,CMOS} = \left[\mu_N C_{ox}\left(\frac{W}{L}\right)_N (V_{GSN} - V_{THN}) + \mu_P C_{ox}\left(\frac{W}{L}\right)_P (V_{SGP} - |V_{THP}|)\right]^{-1} \quad \text{(Eq 5-1)}$$

For linearity reasons, the input switches, labeled ϕ_{1d}, ϕ_{2d1} and ϕ_{2d2} in Figure 5.1, should be designed for equal impedances. This means the PMOS should be made larger than the NMOS by a factor equal to the ratio μ_N/μ_P, as shown below.

$$\frac{\left(\frac{W}{L}\right)_P}{\left(\frac{W}{L}\right)_N} = \frac{\mu_N}{\mu_P} \qquad \text{(Eq 5-2)}$$

The bottom-plate switches, labeled ϕ_1 and ϕ_2 in Figure 5.1, should be designed for a first-order cancellation of charge-injection errors. The error is given by

$$\Delta V_{OUT} = -\frac{1}{2}\cdot\frac{(Q_{chan})_N}{C_S} + \frac{1}{2}\cdot\frac{(Q_{chan})_P}{C_S}$$

$$= -\frac{1}{2}\cdot\frac{C_{ox}}{C_S}\cdot\{W_N L_N(V_{DD} - V_{IN} - V_{THN}) - W_P L_P(V_{IN} - V_{THP})\} \qquad \text{(Eq 5-3)}$$

For a partial cancellation of charge-injection error, the NMOS and PMOS devices should be designed to have equal sizes.

$$W_N L_N = W_P L_P \qquad \text{(Eq 5-4)}$$

The fully-differential configuration of the integrator further mitigates the effects of signal-dependent charge injection.

In addition to sizing the switches for linearity and charge-injection reasons, the sampling network also needs to be designed for sufficient bandwidth. Increasing the switch sizes decreases the resistance but increases the parasitic capacitance of the network. An optimum value of the switch size which yields a minimum R-C time constant can be determined.

5.2.2 Sampling and Integrating Capacitors

The sizes of the sampling and integrating capacitors are dictated by the noise requirements. The ideal input-referred thermal noise of the integrator is given by

$$P_{Ni} = 4 \cdot \frac{kT}{C_S} \qquad \text{(Eq 5-5)}$$

Ideally, during phase 1, a noise sample with variance $2kT/C_S$ (kT/C_S on each of the differential path) is captured across the sampling capacitors when the switches labeled ϕ_1 are open. Another $2kT/C_S$ is sampled across the sampling capacitors during phase 2. However, because of nonideal effects described below, the total input-referred noise will be larger than that predicted by (Eq 5-5).

The switches labeled ϕ_1 are not driven by an ideal input voltage source; rather, it is driven by a buffer stage in the preceding baseband filter, as shown in Figure 5.4(a). The simplified noise model is shown in Figure 5.4(b). The noise sampled across C_S during ϕ_1 is therefore given by

$$P_{Ni,\phi 1} = 4kT(R_N + R_{on})\Delta f \cdot \left| \frac{1}{1 + s(R_{out} + R_{on})C_S} \right|^2 \qquad \text{(Eq 5-6)}$$

where $$R_N \approx \frac{2}{3} \cdot \frac{1}{g_{m,\,buffer}} \cdot n_{sc}$$

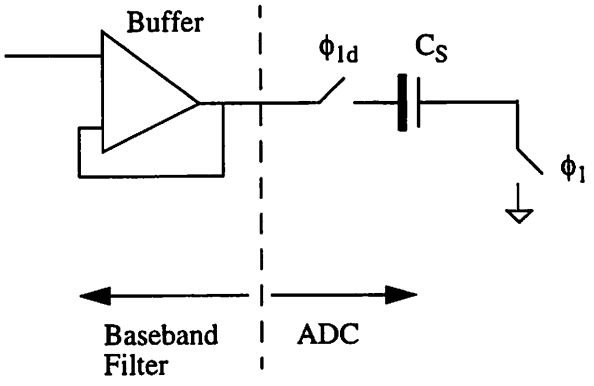
$$R_{out} \approx \frac{1}{g_{m,\,buffer}}$$

The factor n_{sc} refers to additional noise in short-channel devices. Because the noise resistance and output resistance of the buffer driving the sampling network are not the same,

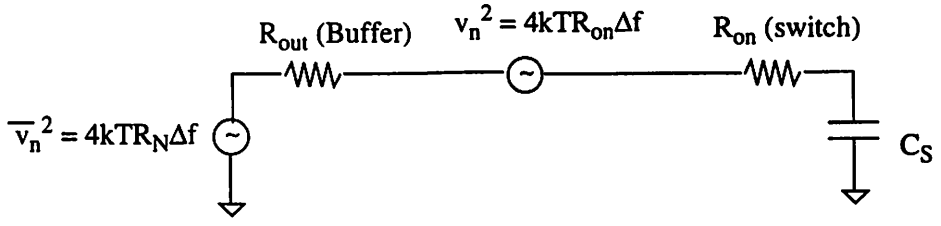
the result does not yield a simple kT/C value. Reorganizing (Eq 5-6), the total input-referred noise power can be written as

$$P_{Ni,\phi 1} = \frac{R_N + R_{on}}{R_{out} + R_{on}} \cdot 4kT(R_{out} + R_{on})\Delta f \cdot \left| \frac{1}{1 + s(R_{out} + R_{on})C_S} \right|^2 \qquad \text{(Eq 5-7)}$$

$$= \frac{R_N + R_{on}}{R_{out} + R_{on}} \cdot \frac{kT}{C_S}$$



(a)



(b)

Fig. 5.4: (a) Filter-to-ADC Interface (Single-Sided Representation) (b) Noise Model during Phase 1

During phase 2, due to thermal noise from the operational transconductance amplifier (OTA), the noise captured across C_S when the switches labeled ϕ_2 open can be greater than

$2kT/C_S$. The OTA in-band flicker noise, when referred to the input of the integrator, simply adds on to the total input-referred noise power.

It is interesting to note that although the noise power is doubled in differential architectures, the input signal power is quadrupled. This results in a net gain of 3dB in dynamic range. Moreover, fully-differential integrators are more immune toward power-supply, common-mode and substrate-coupled noise.

$$DR = \frac{P_{IN}}{P_{NOISE}} \qquad \text{(Eq 5-8)}$$

Because of noise shaping, later integrators will have relaxed noise requirements. This suggests that the capacitors in later integrators in the cascade will be selected based on parasitic considerations rather than noise.

5.2.3 Multi-Standard Adaptability

One of the requirements of this ADC design is the adaptability to multiple RF standards. This experimental prototype was designed for cellular GSM/DCS1800/PCS1900 and cordless DECT standards. At the architecture level, the sampling frequency has been selected to be 25.6MHz and 44.8MHz for GSM and DECT, respectively. Recall that the required dynamic range is 86dB for GSM and 72dB for DECT.

This multi-standard adaptability is achieved by switching to different values of sampling and integrating capacitors. Because the cellular GSM standard has a more stringent dynamic range requirement and because settling requirements are somewhat more relaxed (compared to the DECT standard), a higher value of sampling and integrating capacitors can be used to reduce the kT/C noise.

On the other hand, the settling requirements for the DECT standard are more difficult to meet. Reducing the sampling and integrating capacitors helps increase the bandwidth of the

OTA, but results in a higher kT/C noise. The lower dynamic range requirements for DECT permit a higher kT/C noise.

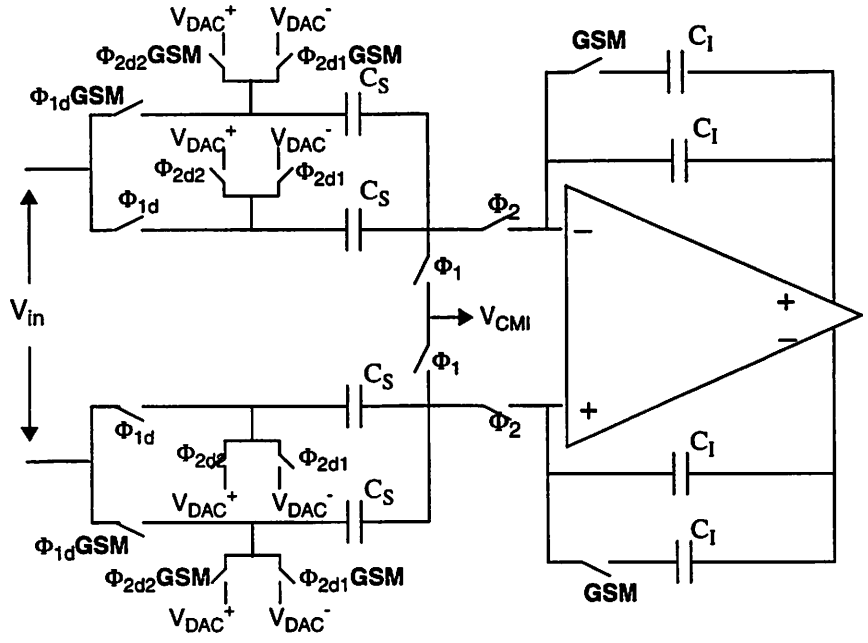


Fig. 5.5: Multi-Standard Adaptability in 1st Integrator

The values of the sampling capacitors in the first integrator have been selected to be 5pF and 1.5pF for GSM and DECT, respectively. Because the desired closed-loop gain is 0.2, the integrating capacitors are 25pF and 7.5pF, respectively, for GSM and DECT.

5.3 Operational Transconductance Amplifier

The DC gain and output swing requirements necessitate the use of a 2-stage amplifier. Figure 5.6 shows the fully-differential OTA used in this experimental prototype. The first stage is a telescopic amplifier, and this is followed by differential pair in the second stage. The telescopic topology has a number of advantages over its folded-cascode counterpart. It has fewer noise-contributing devices, fewer current legs, and a wider bandwidth for a given current level.

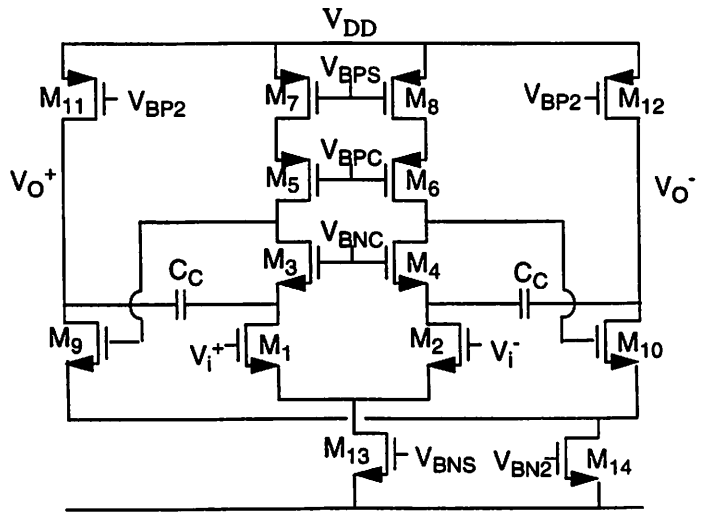


Fig. 5.6: Fully-Differential 2-Stage OTA

The amplifier has an all-NMOS signal path. NMOS devices are approximately three times faster than PMOS devices because of the difference between the electron and hole mobilities. Since speed and power directly trade off, a higher speed amplifier will dissipate less power for a fixed settling constraint. The disadvantage with NMOS input devices is the higher 1/f (or flicker) noise which can be particularly damaging in narrowband applications.

The second stage is made fully differential instead of a quasi-differential common-source stage for a number of reasons. Having a tail-current device eliminates the need for a power-hungry inversion stage for the common-mode feedback amplifier. It has been shown that for the common-mode feedback circuit to have the same bandwidth as the differential amplifier path, the common-mode feedback amplifier needs to dissipate about 40% of the total power consumption in the differential amplifier shown above [25]. This allows the use of dynamic switched-capacitor common-mode feedback circuits (detailed in Section 5.4) which does not dissipate any static power.

The fully-differential second stage amplifier also eliminates the need for a dynamic level shift between the output of the first stage and the input of the second stage [18]. In

addition, this fully-differential topology improves the power-supply rejection ratio (PSRR) and the common-mode rejection ratio (CMRR).

Some form of compensation is needed to maintain stability in a 2-stage amplifier. The standard Miller compensation has a pole-splitting effect which moves one pole to a lower frequency and another to a higher frequency. The 2-stage amplifier in Figure 5.6 employs the cascode compensation scheme [26][27][28], which creates a dominant pole and two complex poles at a higher frequency. It has been shown [30] the cascode compensation scheme yields a higher amplifier bandwidth compared to the conventional Miller compensation.

The following sections will investigate the various noise, speed and power tradeoffs in the design of the OTA.

5.3.1 Thermal Noise

The input-referred thermal noise of a single common-source transistor, shown in Figure 5.7 can be approximated by

$$\overline{v_{n,in}^2} \approx \overline{i_{ds}^2} \cdot g_m^2 = 4kT \cdot \frac{2}{3} \cdot \frac{1}{g_m} \cdot n_{sc} \Delta f \qquad \text{(Eq 5-9)}$$

The factor n_{sc} takes into consideration the additional noise in short-channel devices

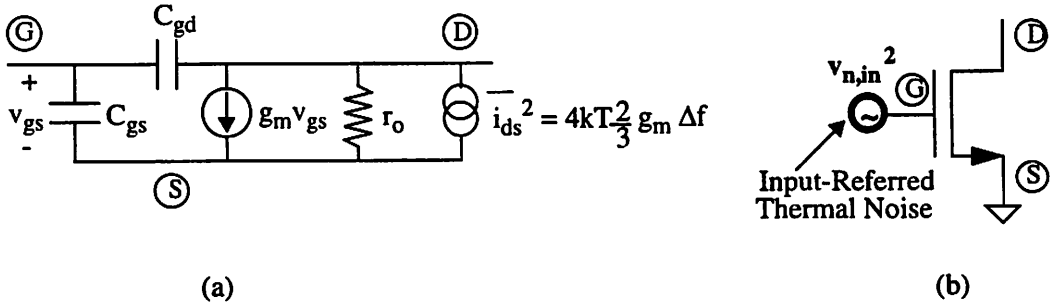


Fig. 5.7: Thermal Noise in a Single Common-Source Transistor: (a) Small-Signal Model (b) Input-Referred Noise Voltage

($L \leq 1\mu m$), and is bias dependent. The results of (Eq 5-9) can be applied to determine the input-referred thermal noise of the OTA. A simple analysis of the small-signal model will show that

the noise contribution from the cascode devices is negligible. Moreover, the noise of the devices in the second stage, when referred to the input of the OTA, is attenuated by the square of the gain of the first stage. As such, the input-referred thermal noise is dominated by the input devices (M_1, M_2) and the load devices (M_7, M_8), as shown below.

$$P_{n,\,OTA} = 2 \cdot \left\{ v_{n1,\,in}^2 + \left(\frac{G_{m3}}{g_{m1}}\right)^2 v_{n3,\,in}^2 + \left(\frac{G_{m5}}{g_{m1}}\right)^2 v_{n5,\,in}^2 + \left(\frac{g_{m7}}{g_{m1}}\right)^2 v_{n7,\,in}^2 + \left(\frac{1}{A_{dc1}}\right)^2 \left[v_{n9,\,in}^2 + \left(\frac{g_{m11}}{g_{m9}}\right)^2 v_{n(11,\,in)}^2 \right] \right\} \quad \text{(Eq 5-10)}$$

$$\approx 2 \cdot \left\{ 4kT \cdot \frac{2}{3} \cdot \frac{1}{g_{m1}} \left[1 + \left(\frac{g_{m7}}{g_{m1}}\right) \right] \right\} \Delta f \quad \text{(Eq 5-11)}$$

When the amplifier is placed in the switched-capacitor integrator, the total noise power is evaluated by integrating the noise spectrum to infinity. This is because the sampling process causes the noise spectrum at high frequencies to fold down to baseband, as illustrated in Figure 5.8. The Δf term in (Eq 5-11) should therefore be the bandwidth of the integrator. The

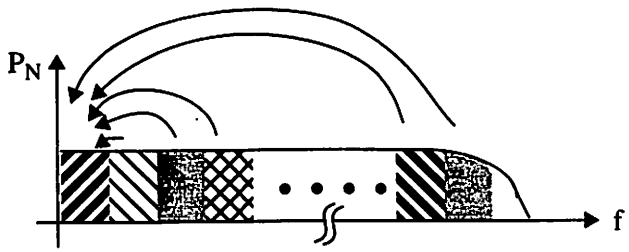


Fig. 5.8: Noise Folding in Sampled-Data Systems

thermal noise of the OTA, when referred to the output of the integrator, is shown below [29].

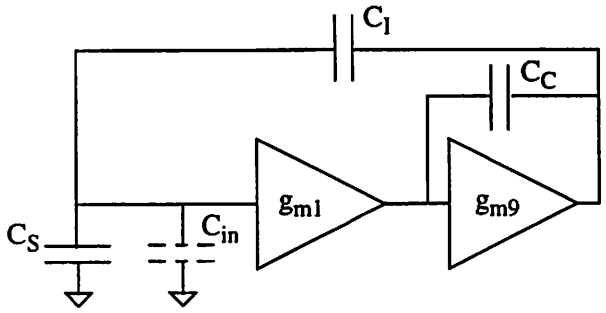


Fig. 5.9: 2-Stage OTA in the Integrator during Phase 2 (Integrating)

$$P_{OTA,\,out} = \int_0^\infty P_{n,\,OTA} \cdot \frac{1}{f_{FB}^2} \cdot \left| \frac{1}{1 + \frac{sC_C}{g_{m1} \cdot f_{FB}}} \right|^2 df = \int_0^\infty 4kT \cdot \frac{2}{3} \cdot \frac{1}{g_{m1}} \left(1 + \frac{g_{m7}}{g_{m1}}\right) \cdot \frac{1}{f_{FB}^2} \cdot \left| \frac{1}{1 + \frac{sC_C}{g_{m1} \cdot f_{FB}}} \right|^2 df$$

$$= \frac{2}{3} \cdot \frac{kT}{C_C} \cdot \frac{\left(1 + \frac{g_{m7}}{g_{m1}}\right)}{f_{FB}} \quad \text{(Eq 5-12)}$$

where feedback factor, $f_{FB} = \dfrac{C_I}{C_I + C_S + C_{in}}$

(Eq 5-12) suggests that decreasing the ratio (g_{m7}/g_{m1}), will minimize the OTA thermal noise. Because the transconductance g_m is given by

$$g_m \approx \frac{2I_{DS}}{V_{DS}^{sat}} \quad \text{(Eq 5-13)}$$

it is desirable to minimize of the ratio $V_{DS1}{}^{sat}/V_{DS7}{}^{sat}$. In addition, the compensation capacitor needs to be sufficiently large to keep the OTA noise contribution minimal.

5.3.2 Flicker Noise

Flicker noise is due to the random trapping and detrapping of minority carriers in the channel of MOS devices. Because the fluctuations in the channel charge carrier density have a relatively large time constant, the noise power density is inversely proportional to frequency. This is why flicker noise is also commonly referred to as 1/f noise.

The input-referred flicker noise of a single common-source transistor is given by

$$v_{fl,\,in} = \frac{K_F}{WLC_{ox}f} \cdot \Delta f \qquad \text{(Eq 5-14)}$$

The constant K_F is an fitting parameter which differs from process to process. NMOS devices demonstrate a higher flicker noise characteristic compared to their PMOS counterparts.

A straightforward strategy to reduce the flicker noise is to increase gate area, i.e. width and length, of the device. There are circuit techniques at the integrator level which can be employed to provide a first-order cancellation of the 1/f noise. Two such techniques are correlated double sampling and chopper stabilization [22][24].

For design simplicity, the OTA flicker noise contribution is reduced by increasing the sizes of the input (M_1, M_2) and load (M_7, M_8) devices. By increasing both the width and length by the same factor, the gate area is increased without changing the W/L ratio. For a fixed current, this keeps a constant transconductance (g_m) and saturation voltage V_{DS}^{sat}.

Increasing the input device sizes, however, increases the input parasitic capacitances, which in turn degrades the feedback factor. This is tolerable in this system because of the relatively large sampling and integrating capacitors.

5.3.3 DC Gain

The low-frequency gain of the amplifier in Figure 5.6 is the product of the gain in the first stage and the gain in the second stage.

$$A_{dc} = \{g_{m1} \cdot (g_{m3}r_{o3}r_{o1} \parallel g_{m5}r_{o5}r_{o7})\}\{g_{m9} \cdot (r_{o9} \parallel r_{o11})\} \qquad \text{(Eq 5-15)}$$

The transistor output resistance, r_o, is proportional to the channel length of the device. Since M_7, M_8, M_{11} and M_{12} do not capacitively load the signal path, they can be made long channel to maximize r_{o7} and r_{o11} in the DC gain equation.

5.3.4 Linear Settling

The OTA needs to have a sufficient bandwidth for the signal to linearly settle to the desired accuracy within half a clock period, as shown below.

$$\omega_{uT} = \frac{1}{\tau} \geq 2f_s \cdot n_\tau \qquad \text{(Eq 5-16)}$$

The sampling frequency f_s is determined by the signal bandwidth and the required oversampling ratio, and the number of time constants n_τ can be determined from the technique described in Section 4.7.

The frequency response of the amplifier will now be analyzed to provide an understanding of how circuit parameters affect the unity-gain bandwidth. Shown in Figure 5.10

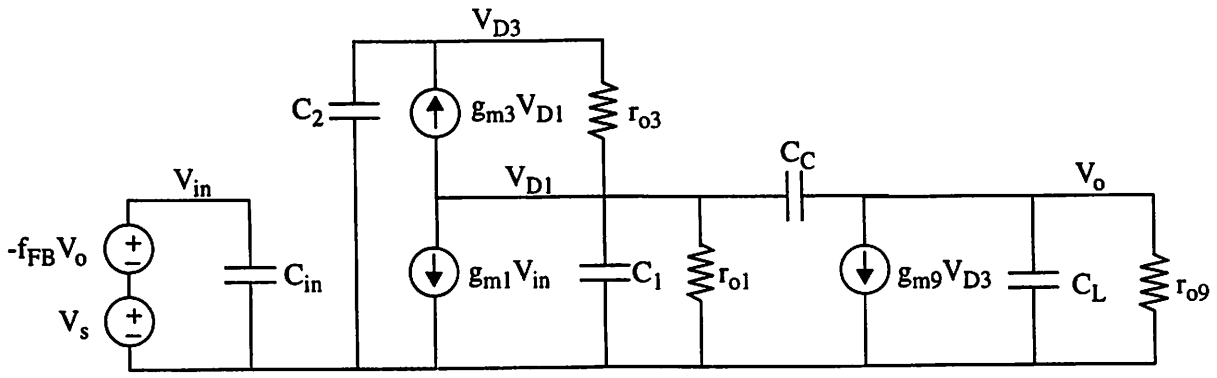


Fig. 5.10: Small-Signal Model of 2-Stage Amplifier for Frequency Response Calculations

is the small-signal model of the amplifier. The capacitors in the figure are defined below.

$$C_{in} = C_{gs1} + C_{p,\,switch} \qquad \text{(Eq 5-17)}$$

$$C_1 = C_{gd1} + C_{gs3} \qquad \text{(Eq 5-18)}$$

$$C_2 = C_{gd3} + C_{gd5} + C_{gs9} \qquad \text{(Eq 5-19)}$$

$$C_L = C_{gd9} + C_{gd11} + C_1(1 - f_{FB}) + C_{1,\,bottom} + C_{C,\,bottom} + C_{next} \qquad \text{(Eq 5-20)}$$

The quantities $C_{1,bottom}$ and $C_{C,bottom}$ are respectively the bottom-plate parasitic capacitances for the integrating and compensation capacitors. $C_{p,switch}$ refers to the parasitic capacitance due to the transfer switch at the summing node, while C_{next} is the parasitic capacitance due to the sampling switches in the next stage.

Assuming infinite device output resistance, r_o, it can be shown that the amplifier transfer function is given by (Eq 5-21) [30].

$$H(s) = \frac{\frac{g_{m1}}{C_2C_T^2}(g_{m3}g_{m9} - C_2C_Cs^2)}{s^3 + \left[\frac{g_{m3}(C_L + C_C) - fg_{m1}C_C}{C_T^2}\right]s^2 + \frac{g_{m3}g_{m9}C_C}{C_2C_T^2}s + \frac{fg_{m1}g_{m3}g_{m9}}{C_2C_T^2}} \qquad \text{(Eq 5-21)}$$

$$\text{where} \qquad C_T^2 = C_1C_L + C_1C_C + C_LC_C$$

Although (Eq 5-21) provides a complete quantitative solution, it is too complicated for hand calculations. Many simplifying assumptions can be made to allow the designer to approximate the pole locations.

The closed-loop unity-gain bandwidth in (Eq 5-16) can be rewritten in terms of circuit parameters. Since the feedback factor f_{FB} is constant for a fixed gain, and because the

$$\omega_{uT} \approx \frac{g_{m1}}{C_C} \cdot f_{FB} \qquad \text{(Eq 5-22)}$$

compensation capacitor C_C is determined by thermal noise considerations, the minimum transconductance of the input devices g_{m1} can be calculated from (Eq 5-16) and (Eq 5-22).

The two open-loop non-dominant poles can be approximated by

$$|p_2| \approx \frac{g_{m9}}{C_1(1 - f_{FB}) + C_{gd11} + C_L} \qquad \text{(Eq 5-23)}$$

$$|p_3| \approx \frac{g_{m3}}{C_C + C_{gs3} + C_{sb3} + C_{gd1}} \qquad \text{(Eq 5-24)}$$

For the amplifier to remain stable, the non-dominant poles should be made much larger than the unity-gain bandwidth. From (Eq 5-22) and (Eq 5-23), it is obvious that

$$g_{m9} \gg g_{m1} \cdot f_{FB} \cdot \frac{C_1(1 - f_{FB})}{C_C} \qquad \text{(Eq 5-25)}$$

From (Eq 5-22) and (Eq 5-24), the transconductance of the NMOS cascode devices (M_3, M_4) should be made larger than the transconductance of the input devices (M_1, M_2).

$$g_{m3} \gg g_{m1} \cdot f_{FB} \qquad \text{(Eq 5-26)}$$

5.3.5 Slew Rate

When a large input step is applied to the amplifier, its output is unable to track the large rate of change in its input. This is due to the limit in the differential current which the class A amplifier can deliver. This nonlinear response is known as the amplifier's slew rate. The amplifier may approach a slew limit in either the first or second stage. The slew limit in the first stage is determined by the need to charge the compensation capacitor at the source of M_3 and M_4, while the slew limit in the second stage is set by the need to charge the load and compensation capacitors. This suggests that for a fixed settling specification, the slew rate can

$$SR = \min\left(\frac{2I_1}{C_C}, \frac{2I_9}{C_C + C_L}\right) \qquad \text{(Eq 5-27)}$$

be improved by increasing the V_{GS}-V_{TH} of the input devices (M_1, M_2, M_9 and M_{10}). This requires increasing bias current, as suggested by (Eq 5-27).

5.4 Common-Mode Feedback

Common-mode feedback is required in fully-differential amplifiers to define the voltages at the high-impedance output nodes. The amplifier employs dynamic or switched-

capacitor common-mode feedback. The fully-differential second stage eliminates the need for an inversion stage in the common-mode feedback loop. Figure 5.11 shows the common-mode feedback loop for the first stage of the amplifier. Capacitors C_M are used to sense the output common-mode voltage. During ϕ_{2d}, switched capacitors C_{CM} define the appropriate DC voltage on the sense capacitors. The loop works by steering current from current source M_{13cm}. The total tail current source has been split into M_{13} and M_{13cm} for improved stability. A similar loop is designed for the second stage of the amplifier.

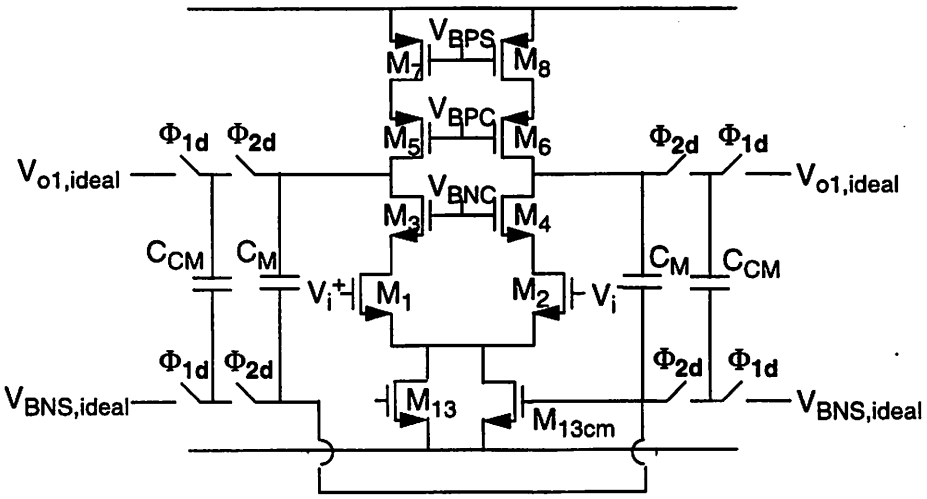


Fig. 5.11: Common-Mode Feedback in the 1st Stage of the OTA

5.5 Bias

Figure 5.12 shows the biasing scheme for the prototype chip. High-swing cascode biasing are generated by stacking a number of triode-region devices. The PMOS portion of the biasing is slaved off the NMOS portion for better matching and tolerance toward process shifts. Internal biasing is used for the NMOS cascode devices (V_{BNC}) in the first stage, as shown in Figure 5.13. To provide good isolation between circuits on the chip, the first OTA (where performance is the most critical) has its own bias network while the other three amplifiers

share another bias network. The master bias currents shown in Figure 5.12 are generated on chip by mirroring the current from an external master current source, as shown in Figure 5.14. The master bias is distributed to local bias networks as a current so that IR drops in routing do not affect the biasing [31].

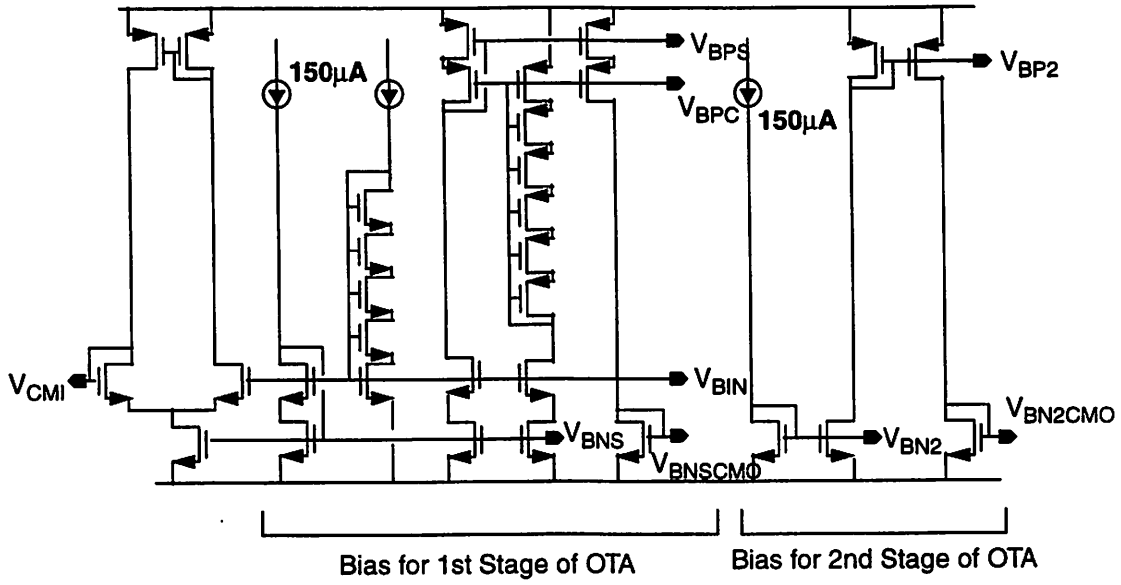


Fig. 5.12: Bias Network for Operational Transconductance Amplifier

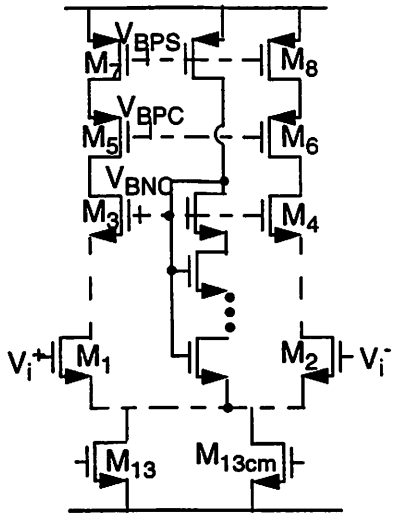


Fig. 5.13: Internal Cascode Biasing for the OTA

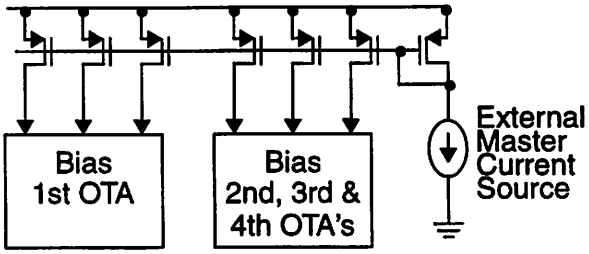
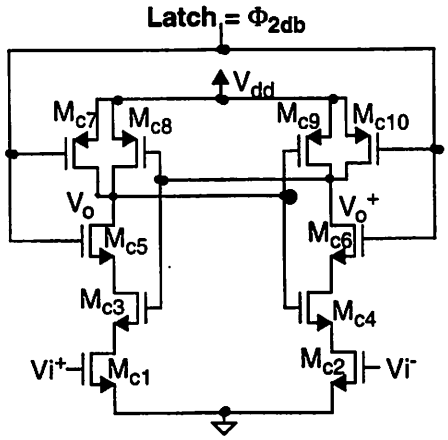


Fig. 5.14: Master Bias Circuit

5.6 Comparator

A simple dynamic comparator, similar to the one in [18], is used to perform a single-bit conversion. During phase 2, when the latch signal is low, the differential outputs are reset to



V_{DD}. As the latch signal turns high, the differential inputs control the resistance of the triode devices, M_1 and M_2. Based on this differential resistance, the outputs of the cross-coupled inverters (M_3, M_4, M_7 and M_8) flip in the appropriate direction.

5.7 Two-Phase Clock Generator

As discussed in Section 5.2, the integrators need a 2-phase nonoverlapping clock (with delays) to minimize signal-dependent charge-injection errors. Shown in Figure 5.15 is the waveform of the 2-phase clock. ϕ_{1d} and ϕ_{2d} are the delayed versions of ϕ_1 and ϕ_2. The rising edges of the delayed clocks should be lined up with the rising edges of the non-delayed versions to increase the amount of available settling time for the OTA, which is given by

$$t_{settle,\,available} = \frac{T_s}{2} - t_{nol} - t_r - t_f \qquad \text{(Eq 5-28)}$$

where T_s = Sampling Period
t_{nol} = Nonoverlap Time
t_r = Rise Time
t_f = Fall Time

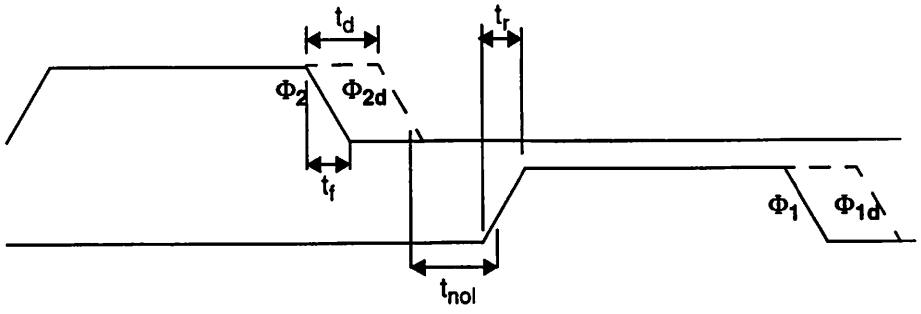


Fig. 5.15: Timing Waveforms of 2-Phase Nonoverlap Clocks

The circuit formed by M_1-M_3 and M_4-M_6 in Figure 5.16 line up the rising edges of the delayed and nondelayed clocks. The delay and nonoverlap times are affected by the delays in the inverter chain and the NAND gates.

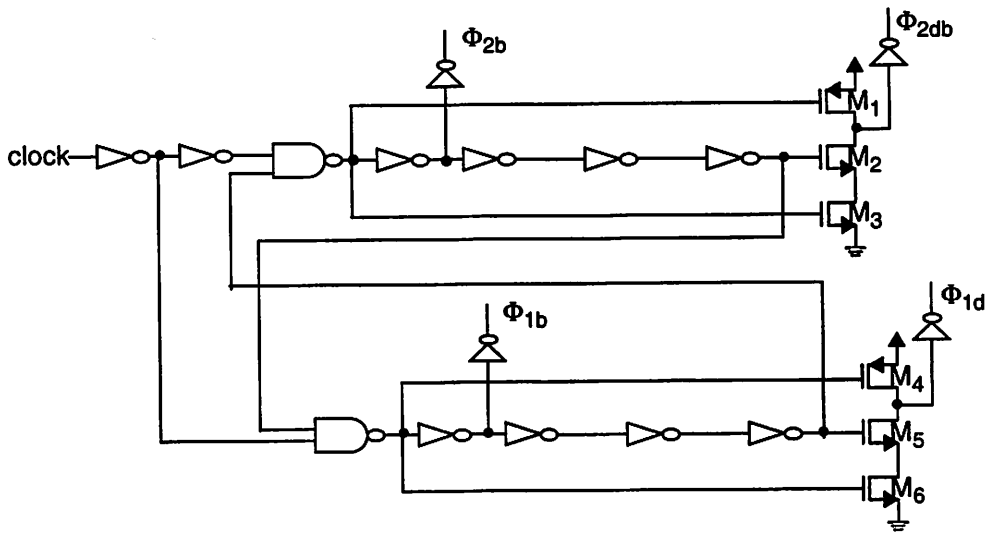


Fig. 5.16: 2-Phase Clock Generator

5.8 Output Buffer

One of the key goals of any mixed-signal design is to minimize the coupling of digital noise through the substrate of bond wires back into the analog circuits. Because the ADC's output digital bits can swing between V_{DD} and ground each clock cycle, they can inject substantial noise into the substrate. The output buffer shown in Figure 5.17 minimizes the

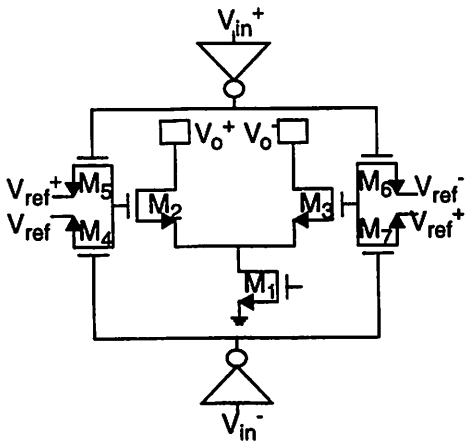


Fig. 5.17: Output Buffer

substrate noise-coupling by maintaining a constant current into the substrate through M_1, regardless of the digital output bits.

In addition, the circuit employs an open-drain differential pair to drive the digital signals off chip to load resistors on the test board. By going off chip differentially, the L(dI/dt) bond-wire coupling is cancelled to a first order.

5.9 Layout Considerations

A number of layout strategies are adopted for the experimental prototype chip. There should be a clear separation between the analog and digital blocks. Digital blocks include the comparators, clock generators and output buffers. The analog circuits should have a different set of supplies from the noisy digital circuits. In addition, critical analog devices and signals (especially in the first integrator) should be placed far away from the digital circuits.

Because the ADC is part of a transceiver chip, it does not enjoy the luxury of being surrounded with pads. Nevertheless, precautions can be taken in pad assignments to improve the ADC performance. One such example is to take advantage of the orthogonal sides of the die which are available for ADC pads. By placing the pads for noisy digital signals at a 90^{o} angle from the pads for sensitive analog pads, the inductive coupling through the bond wires can be significantly minimized.

The coupling of digital noise through the substrate causes great concern among mixed-signal designers, especially when an epi-substrate is being used. To minimize the injection of digital noise into the substrate, the bulk of NMOS transistors in digital circuits should not be tied to digital ground. In a standard CMOS inverter, for example, the NMOS transistor can deliver current spikes of several amperes to the ground (source) node. The bulk connection for digital circuits can be tied to a separate clean signal to hold the substrate constant. On the analog side, the bulk should be tied to analog ground for better threshold control on the bias current mirrors.

Another strategy to minimize differential substrate noise is to route differential paths in close proximity. Maintaining symmetry on the layout of the amplifiers and integrators preserves the many virtues of fully-differential circuits, as discussed earlier in this chapter.

Since capacitor mismatch is an issue for cascaded sigma-delta architectures, a brief discussion on strategies to improve matching is pertinent. It should be noted that it is the matching of the capacitor ratios and not the absolute values of the capacitors which is critical. As such, the sampling and integrating capacitors can be implemented using an array of unit capacitors. For example, if the sampling capacitor is 1pF and the integrating capacitor 5pF, the unit capacitor can be made 250fF. The sampling capacitor will then be made up of 4 unit capacitors and the integrating capacitor will comprise 20 unit capacitors. This ensures that any process variation will affect both the sampling and integrating capacitors by a same factor. Moreover, the integrating capacitors can be wrapped around the smaller sampling capacitor in a common centroid configuration, as shown below.

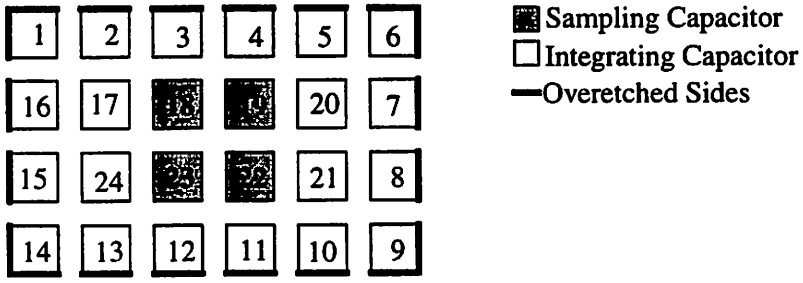


Fig. 5.18: Common-Centroid Layout of Sampling and Integrating Capacitors

The unit capacitors on the periphery of the structure shown above (1-16) suffer from possible overetching on the outer sides, compared to the other unit capacitors. To mitigate this effect, dummy unit capacitors can be placed around the actual unit capacitors. This is illustrated in Figure 5.19.

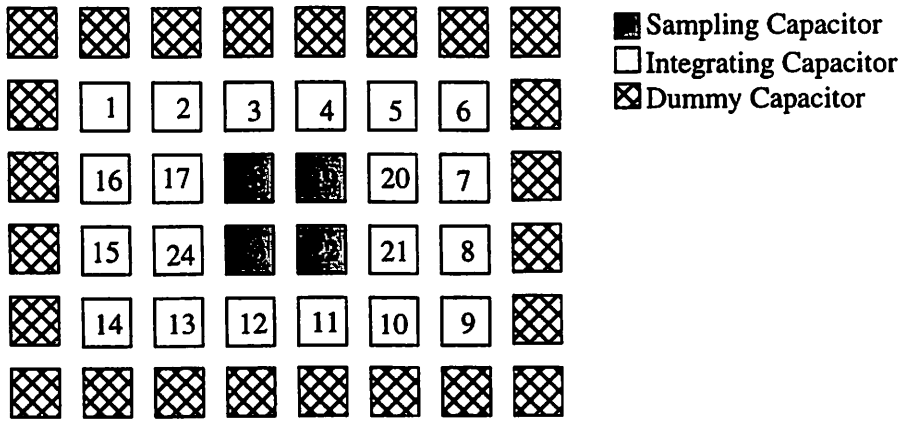


Fig. 5.19: Dummy Unit Capacitors to Improve Matching

On a final note, the transistors in the OTA are fingered to share the drains of the devices. This reduces the parasitic drain capacitances which in turn improves the settling performance of the amplifier.

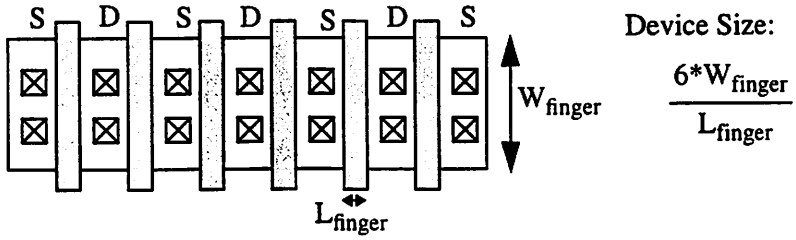


Fig. 5.20: Fingered Device to Reduce Parasitic Drain Capacitance

5.10 Summary

This chapter presented fundamental issues and tradeoffs in the design of the key circuit blocks: integrators, amplifiers, comparators, 2-phase clock generators, and output buffers. Power optimization techniques for the operational transconductance amplifier were investigated. The chapter concluded with a brief discussion of layout considerations.

Chapter 6

Simulated Results

6.1 Introduction

This chapter describes an experimental 2-2 cascade sigma-delta modulator implemented in a 0.35μm double-poly, five-metal CMOS process at 3.3V supply. The simulated performance of the modulator will be presented.

6.2 Capacitor and Current Values

This section will present the values selected for the capacitors and current levels in the integrators. The tradeoffs and optimization for the design of the integrators and amplifiers were discussed in Chapter 5.

Recall that the first integrator switches to different values of capacitors to adapt to multiple standards. Because of the lower oversampling ratio for the DECT standard, the noise from the second and third integrators can be significant. The capacitors in integrators 2 and 3 are therefore selected based on the thermal noise requirements of the DECT standard. The noise contribution from the last integrator is negligible, and the capacitor values are parasitic

limited. Table 6.1 summarizes the values of the sampling and integrating capacitors used in this design.

	C_S	C_I
Integrator 1 (GSM) .(DECT)	5pF 1.5pF	25pF 7.5pF
Integrator 2	1pF	2pF
Integrator 3	0.5pF	1pF
Integrator 4	0.2pF	0.4pF

Table 6.1: Summary of Sampling and Integrating Capacitor Values

The bias currents in the operational transconductance amplifier are determined by settling constraints, slew rate considerations and required thermal noise floor. The 2-stage OTA used in this prototype design was shown in Section 5.3, and is repeated here in Figure 6.1.

	Required Settling Accuracy	Required Slew Rate	I_{DS1}	I_{DS9}	C_C
Integrator 1	0.0061% in 15ns (GSM) 0.0244% in 7ns (DECT)	150 V/µs 260V/µs	2.56 mA	2.95 mA	9.45 pF
Integrator 2	1.83% (GSM) 0.248% (DECT)	150 V/µs 260V/µs	796 µA	977 µA	1.6 pF
Integrator 3	Negligible (GSM) 1.83% (DECT)	135 V/µs 230V/µs	402 µA	517 µA	0.7 pF
Integrator 4	Negligible (GSM) Negligible (DECT)	120 V/µs 200V/µs	230 µA	280 µA	0.2 pF

Table 6.2: Summary of Bias Currents and Compensation Capacitors in OTA's

Table 6.2 summarizes the settling and slew rate requirements of the four amplifiers in the modulator cascade, and presents the selected values of the bias currents and compensation capacitors.

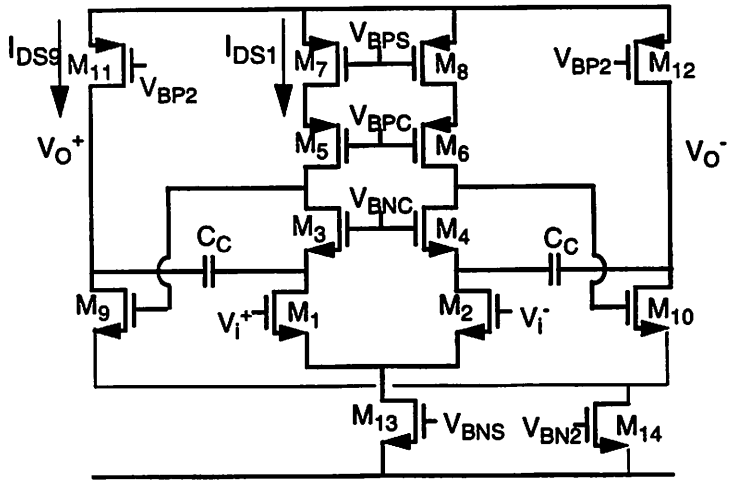


Fig. 6.1: Two-Stage Operational Transconductance Amplifier

As described in Section 5.3, the values of the device V_{DS}^{sat}'s affect the input-referred noise and frequency response of the amplifier. Table 6.3 shows the V_{DS}^{sat} values for the transistors shown in the figure above.

Device	$V_{DS}^{sat} = V_{GS}-V_{TH}$
M_1, M_2	0.5 V
M_3, M_4	0.1 V
M_5, M_6	0.3 V
M_7, M_8	0.7 V
M_9, M_{10}	0.5 V
M_{11}, M_{12}	0.5 V
M_{13}	0.1 V
M_{14}	0.1 V

Table 6.3: Summary of V_{DS}^{sat} values for the OTA

For a fixed current, the transconductance (g_m) of the cascode M3 device is made larger than that for the input device to satisfy (Eq 5-26). Additionally, the V_{DS}^{sat} of the PMOS load devices (M_7 and M_8) are made larger than that of the input devices to reduce the noise contribution from the load devices.

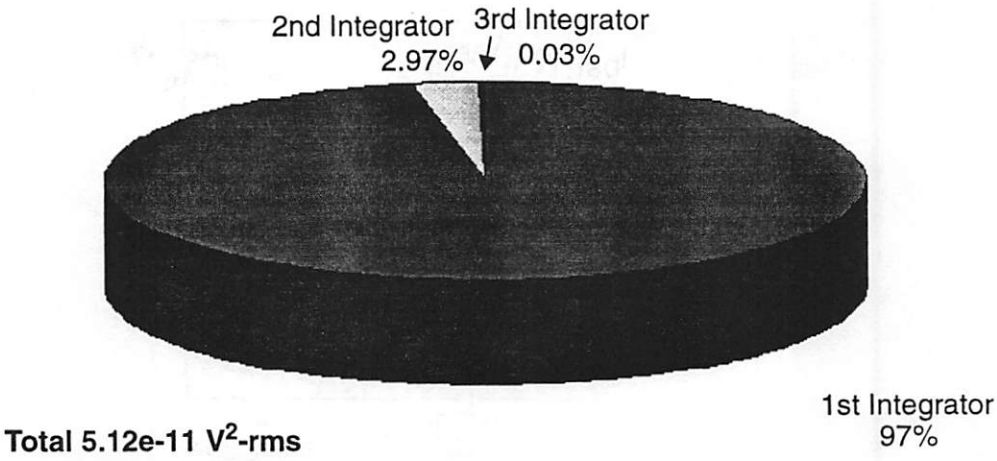


Fig. 6.2: Breakdown of Noise Contribution for the ADC (GSM Standard)

6.3 Dynamic Range

The required dynamic range for the ADC is 86dB for GSM and 72dB for DECT. Robust designs require that the ADC be overdesigned to leave sufficient margins for noise sources which cannot be simulated using existing softwares and for the effects of process variations. The equation for calculating the dynamic range is given by

$$DR = \frac{P_{IN}}{P_{NOISE}} = \frac{\left(\frac{\hat{V}_{IN}}{\sqrt{2}}\right)^2}{P_{N,\,thermal} + P_{N,\,flicker} + P_{N,\,quantization}} \qquad \text{(Eq 6-1)}$$

The breakdown of ADC noise for GSM is illustrated in Figure 6.2. The high oversampling ratio (128x) makes the input-referred noise dominated by the noise from the 1st integrator. The noise contribution of the 3rd and 4th integrators, and the quantization noise are negligible. It is interesting to investigate the breakdown of the noise in the first integrator.

A similar breakdown chart for DECT is shown in Figure 6.3. Because of the lower oversampling ratio (32x), the quantization noise becomes as significant as the thermal and flicker noise from the first integrator. In addition, noise from the 2nd, 3rd and 4th integrators are not negligible.

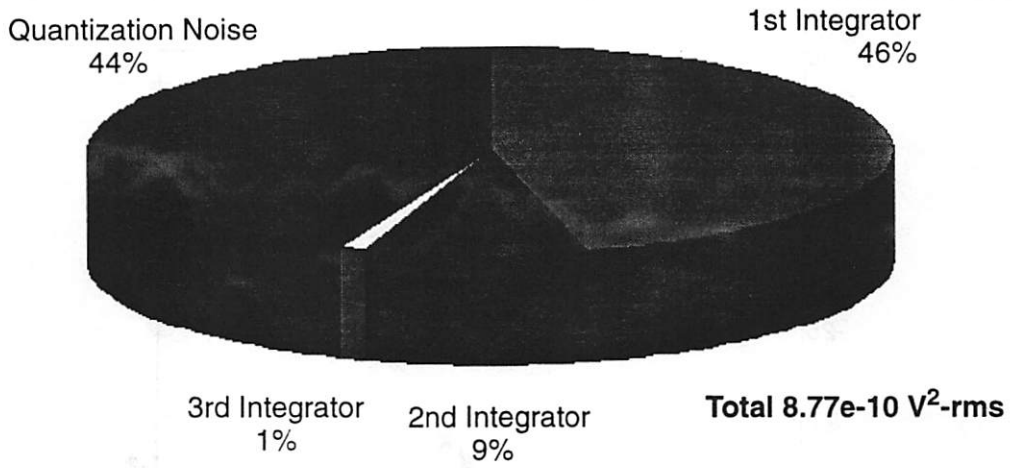


Fig. 6.3: Breakdown of Noise Contribution for the ADC (DECT Standard)

6.4 Intermodulation

The intermodulation performance of the ADC is important in RF receivers. For GSM, two blockers at 900kHz and 1.7MHz may modulate through the nonlinearities of the ADC down to baseband. Due to noise shaping and the relatively high gain of the amplifiers, the

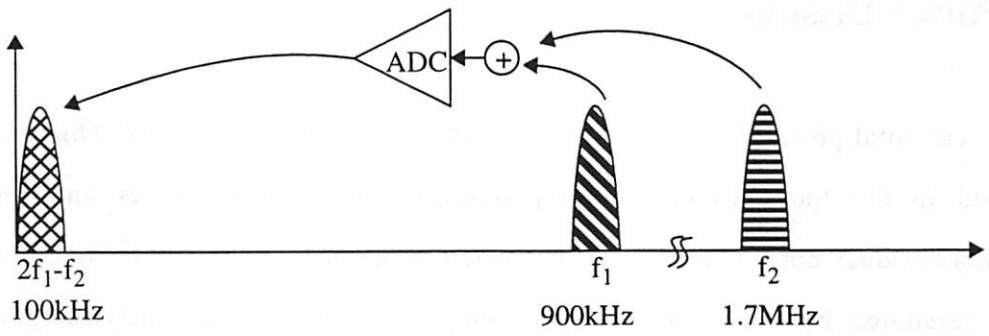


Fig. 6.4: Intermodulation Test Requirement for GSM

dominant source of nonlinearity in the ADC is the switching network in the first integrator. To check the intermodulation performance, the ADC is simulated together with the continuous-time filter preceding it. A minimum of three points is needed to generate the plot shown in Figure 6.5.

The fundamental and the absolute 3rd-order intermodulation terms are plotted and

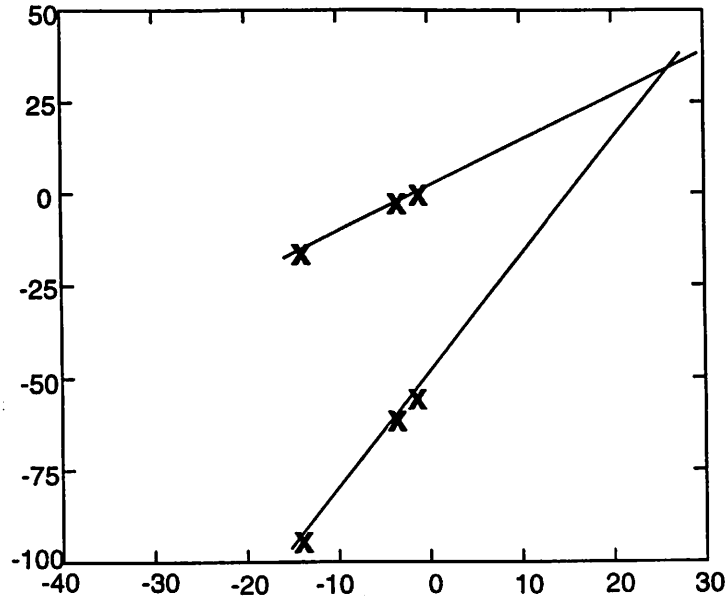


Fig. 6.5: Input-Referred 3rd-Order Intercept Point

extrapolated. The crossover point is known as the input-referred 3rd-order intercept point. From the figure above, the simulated IIP_3 at the input of baseband circuits is 26dBV. This exceeds the IIP_3 specification of 12dBV for GSM.

6.5 Power Dissipation

The total power dissipation in the 4th-order modulator is 70mW. This includes power dissipated in the local digital circuitry (comparators, output buffers and 2-phase clock generator) but does not include power dissipated in the decimation filter. This power level has been necessitated by the higher dynamic range requirements for fully-integrated receiver applications.

Figure 6.6 shows a breakdown of power dissipation in the various blocks of the ADC. More than 50% of the power is consumed by the 1st amplifier. Noise shaping in sigma-delta modulators permit the scaling of bias currents and capacitors in later amplifiers.

However, since there are two ADC's on the transceiver chip (I and Q channels), the

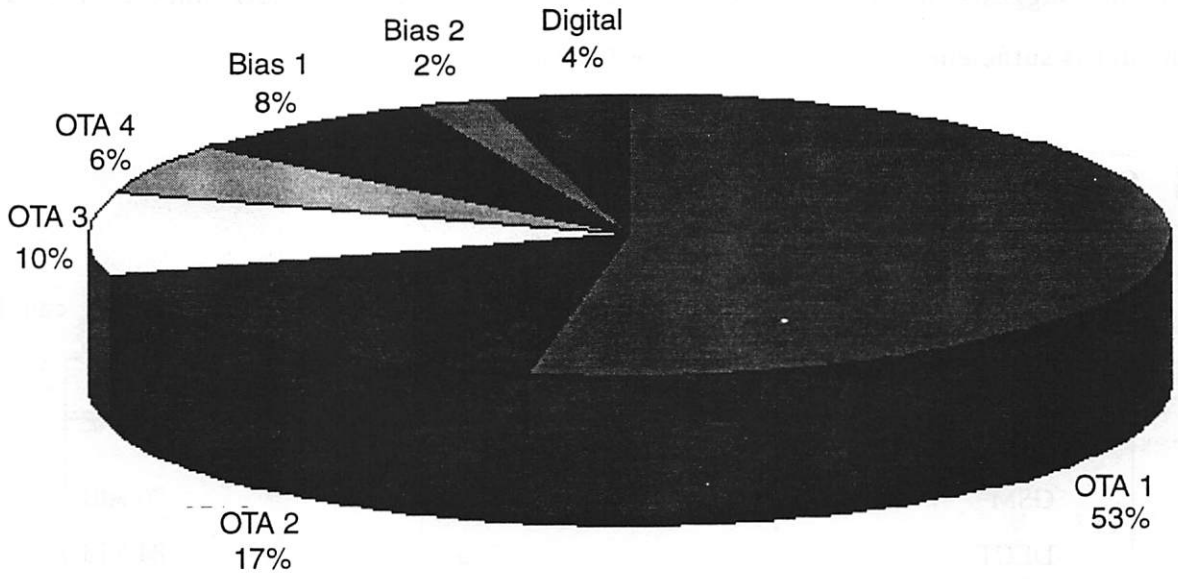


Fig. 6.6: Breakdown of Power Dissipation in ADC

relatively high power consumption (compared to an 8- to 10-bit ADC's in conventional Super-Heterodyne receivers) works against the goals of portable electronics.

Detailed discussions of power-optimization strategies in fully-integrated receivers are presented in [2]. One such strategy with respect to the ADC design is to have a dual power mode adaptability. Because the scenario of having a weak desired signal in the presence of strong adjacent-channel blockers is quite rare, the high dynamic range required of baseband circuits may be needed only for brief periods of time. For the majority of the time, a low-power ADC with 6-8 bits of resolution may be sufficient [32]. From (Eq 4-10), this implies a power savings of several orders of magnitude.

A number of options exist for implementing the power-adaptive ADC. A straightforward approach is to have two versions of the ADC on the same chip: one targeting 12-14 bits of resolution and another targeting 6-8 bits. Depending on the blocking profile, the appropriate ADC will be switched in. This solution, however, is not area-efficient. A more efficient option involves the scaling down of the bias current in the amplifiers under nominal

conditions, and the scaling up of the current under strong blocking conditions. Additionally, Figure 6.6 suggests that the first integrator can be bypassed completely since a 3rd-order modulator is sufficient to provide a 6-8 bit performance.

6.6 Summary of Simulated Performance

The performance of the entire modulator is summarized in Table 6.4. As can be

	Specifications	Simulated Results
Dynamic Range		
GSM	86dB	96.8dB
DECT	72dB	84.5dB
IIP_3 (AA Filter & ADC)	12.7dBV	26dBV
Power	Minimize	70mW

Table 6.4: Summary of Simulated Performance

observed, the ADC is overdesigned to leave sufficient margins for modeling errors and potential substrate coupling from other blocks in the receiver chain. With the shown results, the total ADC noise contribution to the overall receiver is only 3%.

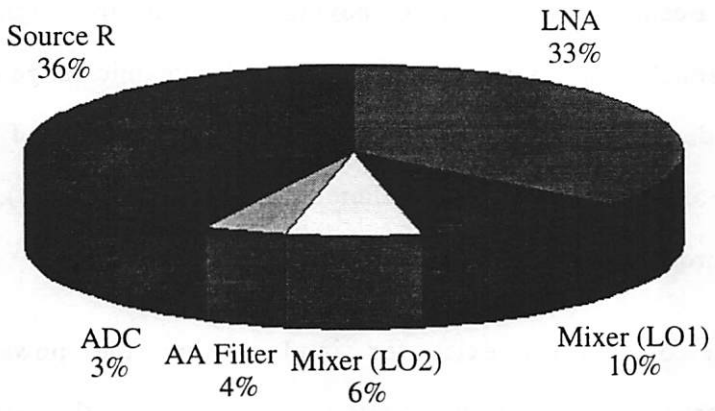


Fig. 6.7: Receiver Noise Contribution

6.7 Layout

The layout of the full-chip ADC is shown in Figure 6.8, and the layout of the first integrator in shown in Figure 6.9. The strategies adopted for the layout were presented in Chapter 5.

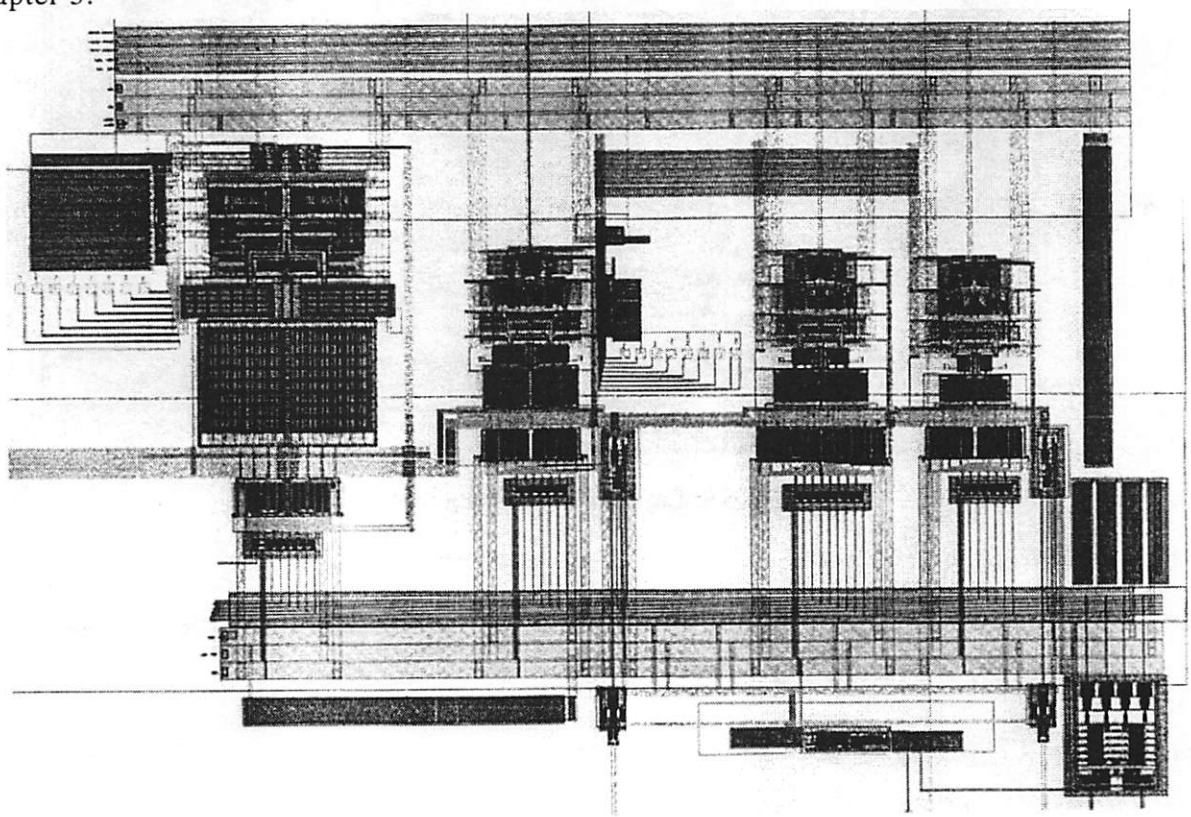


Fig. 6.8: Layout of ADC

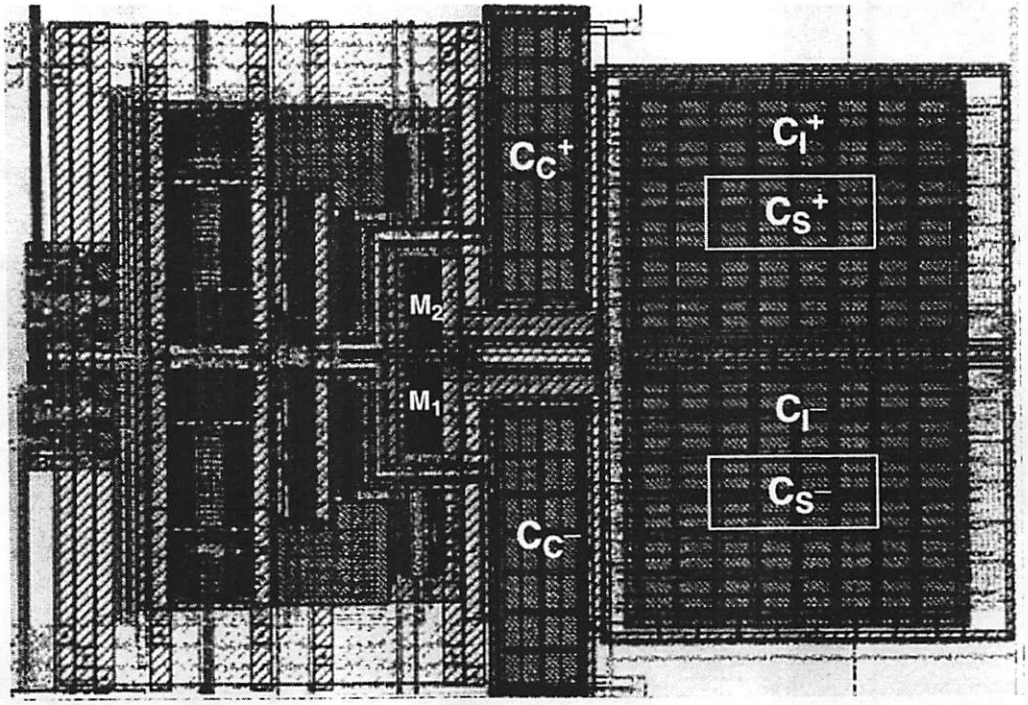


Fig. 6.9: Layout of First Integrator

Chapter 7

Conclusions

7.1 Introduction

This chapter summarizes the key contributions in the design of the multistandard-capable ADC for a fully-integrated CMOS RF receiver. The experimental prototype is designed for cellular GSM/DCS1800/PCS1900 and cordless DECT standards. System-level architecture design of the 2-2 cascade modulator was presented in Chapter 4, and the circuit design issues and tradeoffs were discussed in Chapter 5. Chapter 6 then summarized the simulated performance of the ADC.

The next section will provide recommendations for future work.

7.2 Future Work

This project primarily aims to demonstrate the feasibility of using a single sigma-delta modulator to adapt to multiple communications standards, and to integrate the ADC with the other blocks in the receive path.

One area which will be of interest is power-reduction strategies for the high dynamic-range baseband circuits. An automatic scheme to detect whether a nominal or strong blocking

condition is present will aid the use of the power-adaptive technique discussed in the previous chapter. In addition, optimizing the power distribution among the various baseband blocks: (1) continuous-time analog filter preceding the ADC, (2) the ADC, and (3) the digital filter following the ADC should be explored.

Another possible future work is to investigate the feasibility of making the ADC adaptable to a very wideband standard like spread-spectrum CDMA and W-CDMA without excessive power dissipation. Achieving 8-10 bits of resolution with a Nyquist rate of 10MS/s or greater involves a somewhat different set of design tradeoffs and optimization than those for GSM and DECT.

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