PROGRAMMABLE, LOW-NOISE, HIGH-LINEARITY BASEBAND FILTER FOR A FULLY-INTEGRATED, MULTI-STANDARD, CMOS RF RECEIVER

by

Tai-Ling Danelle Au

Memorandum No. UCB/ERL M98/76

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
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94720

Programmable, Low-noise, High-linearity Baseband Filter for a Fully-Integrated, Multi-Standard, CMOS RF Receiver

by
Tai-Ling Danelle Au

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Abstract

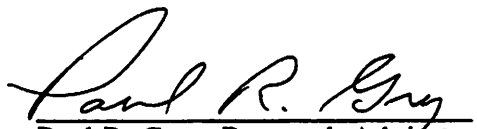
The expanding market for radio-frequency personal communication devices has led to the proliferation of different communication standards and a high consumer demand for low cost, low power, small form factor devices. As a result, present research focuses on the design of a monolithic receiver that can adapt to the various communications standards in a cost-effective CMOS technology. A fully integrated receiver architecture necessitates the elimination of discrete high-Q image-rejection and IF filters. The received signal spectrum is typically downconverted to baseband or low-IF in its entirety. Because there is no channel filtering before the baseband blocks, both the desired signal and strong adjacent channel blockers may be present. A high-dynamic range baseband filter is needed at the input of the baseband blocks to attenuate these blockers.

This work focuses on the baseband filter that precedes the sampled data circuits or analog-to-digital converters in the baseband of an integrated receiver. The same filter can be used to perform anti-aliasing, accomodate for gain variation in the RF front-end and reduce dynamic range requirements of subsequent baseband blocks. The baseband filter incorporates a

variable gain stage, a 3-rd order filter and a buffer that drives the sigma-delta converters. The 3-rd order filter is designed by combining an RC network and a second-order Sallen-and-Key configuration.

This baseband filter will be used in the wideband IF with double conversion receiver architecture and is designed to meet the baseband signal conditions required of both the Digital Enhanced Cordless Telecommunications (DECT) and cellular (GSM,PCS-1900,DCS-1800) standards. The baseband filter is designed in a 0.35 um double-poly CMOS process, runs off a 3.3 V supply and dissipates 75 mW. The simulated dynamic range is 90dB for GSM and 80dB for DECT.

Approved by:



Paul R. Gray, Research Advisor

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Chapter 1

Introduction

1.1 Motivation

The expanding market for radio-frequency (RF) personal communication devices has led to the proliferation of different communication standards as shown in Table 1.1. To take advantage of the services provided by these communication standards, it is desirable to have a receiver system that can adapt to these different RF communication standards. However, existing hardware solutions are inefficient. Numerous discrete components and chips limit the form factor, and increases cost and power dissipation.

Wireless Services	RF Standards
Cellular	GSM E-GSM PCS 1900 DCS 1800 AMPS
Cordless	DECT
Wireless LAN	802.11 Bluetooth Home RF
Satellite	GPS Iridium

Table 1.1: Multiple RF standards for multiple wireless services

A highly integrated receiver system provides the functionality and flexibility for multi-standard operation [1][2][3][4]. The integrated receiver system can be implemented in a low-cost, VLSI-capable technology like CMOS, with a small form factor and low power operation for added portability. However, in a fully-integrated receiver architecture, discrete high-Q image-rejection and IF filters are eliminated. Therefore, the entire received RF spectrum is typically downconverted to baseband or low-IF. Because there is no channel filtering before the baseband blocks, both the desired signal and strong adjacent channel blockers may be present.

Consequently, the challenge of designing baseband circuits for integrated receivers is to realize the required analog functions for a variety of signal conditions, like linearity, dynamic range and blocking profile. At the input of the baseband blocks, a baseband filter is needed to attenuates blockers. The same filter can be used to perform anti-aliasing, accommodate for gain variation in the RF front-end and reduce noise requirements of subsequent baseband blocks. A high-dynamic range, oversampled sigma-delta modulator can then be used after the filter to digitize the signal.

1.2 Research Goals

The focus of this project is to design an analog programmable, low noise, high-linearity, continuous-time baseband filter for the GSM (cellular) and DECT (cordless) communication standards. The baseband filter incorporates a variable gain amplifier, a 3rd order filter and a buffer. The results of this work are summarized below.

- Designed a baseband filter that meets the GSM and DECT specifications. Estimated power consumption is 75mW.
- Developed a filter with a programmable bandwidth to adapt to the different signal bandwidths for GSM and DECT
- Developed a high-linearity variable gain amplifier with discrete gain control that accommodates for gain variation in the RF front-end. This maximizes the input to the ADC without overloading.

1.3 Thesis Organization

In Chapter 2, three different receiver architectures are discussed, and the ones most amenable to higher integration and multi-standard capability are identified. The chapter concludes by introducing the receiver specifications developed for the Wideband IF with Double-Conversion Receiver architecture. Chapter 3 focuses on the baseband blocks of integrated receivers. The challenges in baseband design are addressed. A description of possible ways to perform channel selection are also discussed. The baseband specifications are also presented along with how they pertain to the design of the baseband filter. The baseband filter blocks and system level issues are discussed.

Chapter 4 discusses circuit related design issues related to the design of the first block of the baseband filter--the Variable Gain Amplifier. Issues such as opamp-topology selection, compensation, common-mode feedback circuits are investigated. At the end of the chapter, a summary of the simulation results is presented. Chapter 5 describes the design of the 3rd order filter. The filter specifications are discussed, along with how they can be implemented. The selection of filter order, pole location, and magnitude and phase response is discussed. Three possible filter implementations are given. The chapter concludes with the design of the filter type selected--the Sallen-Key filter, and a summary of simulation results.

Chapter 6 begins with the motivation behind implementing a buffer to drive the sigma delta modulator. The buffer settling response, opamp-topology selection and noise and power dissipation are also discussed. Chapter 7 presents the baseband filter simulation results, including a breakdown of the noise and power contribution from each block. Conclusions from this work are given in Chapter 8 along with suggestions for future work.

Chapter 2

System Architectures

2.1 Introduction

Most radio communication standards today outline a set of specific test conditions which determine the noise, intermodulation and blocking requirements of receivers. To implement multiple communication standards, a receiver system must address the different performance requirements of each standards, including different carrier frequencies, channel bandwidths, sensitivity and selectivity. A highly integrated receiver system has the increased functionality and flexibility for multimodal operation. In addition, the elimination of the number of discrete components reduces cost and form factor.

This chapter starts with a review of receiver architectures, with particular emphasis on the issues related to integration and multi-standard operation. A discussion of the receiver specifications based on the Wideband-IF double conversion architecture follows.

2.2 Receiver Architectures

In an ideal receiver architecture, also known as a software radio, as shown in Figure 2.1, the RF signal at the antenna is digitized by an analog-to-digital converter before being

processed in the digital domain. By programming the digital signal processing for multiple RF standards, this receiver architecture is amenable to multi-standard operation.

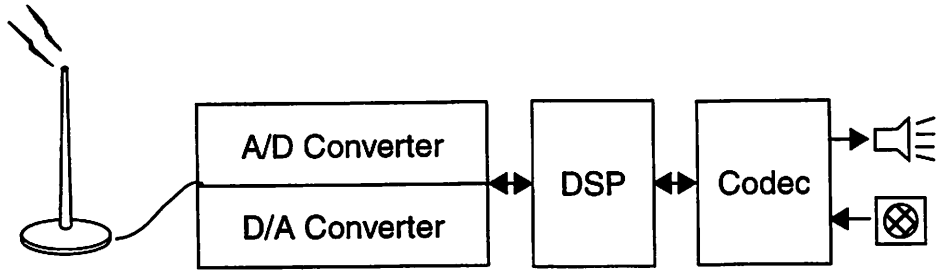


Fig. 2.1: Ideal Receiver

However, the design and implementation of an RF A/D converter is difficult because it would require an extremely high resolution and a sampling frequency in the GHz range. Some analog signal processing would be required before the A/D conversion. The next section will focus on the different architectures--superheterodyne, direct conversion, wideband IF double conversion--that are more practical for actual implementations.

2.2.1 Superheterodyne Receiver Architecture

Most commercial RF communication receivers today use the superheterodyne receiver architecture. Examples of superheterodyne designs are featured in [5][6][7][8]. As shown in Figure 2.2, the receiver uses a collection of discrete components of various technologies such as galium arsenide for the RF blocks, silicon bipolar for the IF blocks and CMOS for the baseband circuits. The RF spectrum first passes through a discrete RF filter that removes out-of-band energy and performs rejection of image-band signals. The LNA amplifies the signal before another image rejection filter further attenuates the undesired signals present at the image frequencies.

An RF channel-select frequency synthesizer then tunes the desired band to a fixed IF where alternate channel energy is removed by a discrete high-Q IF filter. Because the desired signal is now isolated, a variable gain amplifier can adjust the amplitude of signal to reduce the dynamic range of subsequent blocks. The signal is then mixed to baseband, where a low to moderate performance anti-aliasing and A/D conversion is used to digitize the signal.

The superior performance of this receiver architecture is achieved by using high-Q, high-performance, off-chip discrete components. However, these discrete components are not amenable to the highly-integrated solution required by modern, portable communication systems. In addition, the IF filter that performs channel selection typically has a frequency response specific to a specific standard, and is therefore not multi-standard capable.

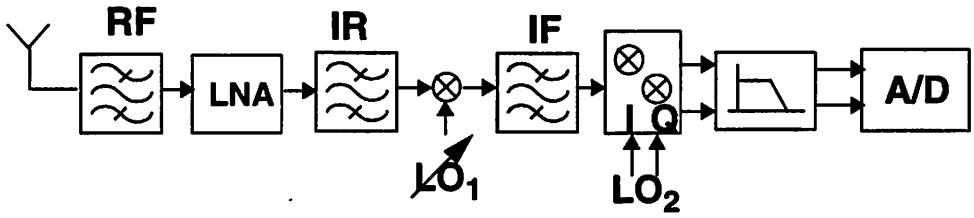


Fig. 2.2: Superheterodyne Receiver Architecture

2.2.2 Direct Conversion Receiver Architecture

One architecture that is more amenable to integration is the Direct Conversion or

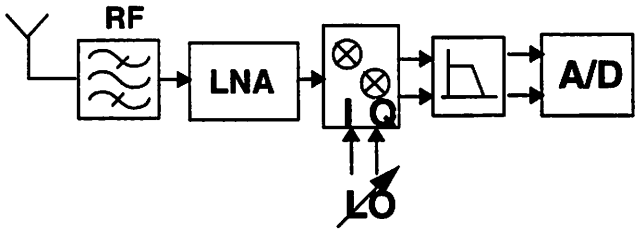


Fig. 2.3: Direct-Conversion Homodyne Receiver

Homodyne Receiver Architecture [9][10]. In this architecture, both the IR and IF filters are eliminated. The entire RF spectrum is translated directly to baseband. Multi-standard operation

can then be achieved by programming for variable-bandwidth channel selection in the digital domain.

However, because the LO is at the same frequency as the RF carrier, this architecture suffers from LO leakage to the antenna. This may result in a time-varying DC offset from self-mixing. Additional DC offset components also arise from LO leakage to the mixer input, second order intermodulation and flicker noise. In addition, this architecture requires a low-phase noise frequency synthesizer which is difficult to implement with low Q on chip oscillators.

2.2.3 Wideband IF with Double Conversion Receiver Architecture

Another architecture that is also amenable to integration is the wideband IF with double conversion receiver [11]. As shown in Figure 2.4, this architecture also eliminates the

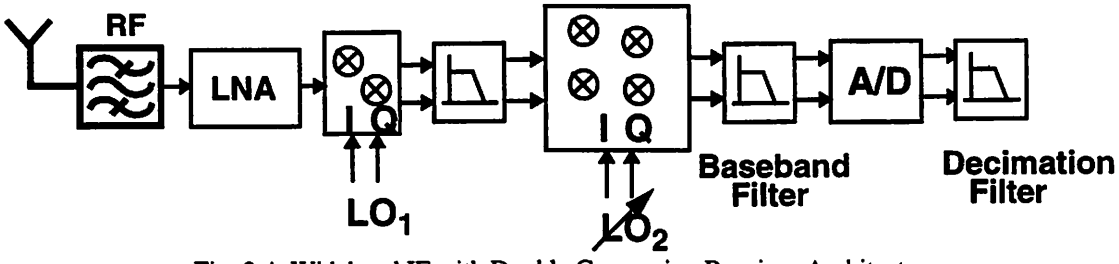


Fig. 2.4: Wideband IF with Double Conversion Receiver Architecture

IR and IF filters. The entire RF spectrum is translated to IF using a fixed LO. This local oscillator is at a higher frequency and can be implemented with a low phase noise and wide phase-locked loop bandwidth. The upconverted components from the mixer are then removed using a simple low-pass filter before the spectrum is translated to baseband using a tunable frequency synthesizer. Similar to the direct conversion receiver architecture, a programmable decimation filter can then be used in the digital domain to perform channel selection.

Because the entire RF spectrum is translated directly to baseband without any filtering, a very weak desired signal next to large adjacent blockers may be present at the input

of the baseband filter. This results in very high linearity and dynamic range requirements for the baseband circuits.

The wideband IF with double conversion receiver architecture also suffers from DC offset problems resulting from LO leakage to the mixer output, second order intermodulation and flicker noise. However, the DC offset in this architecture is relatively constant compared to that of the direct conversion receiver architecture and a current DAC can be used at the input of the baseband filter to cancel the offset.

2.2.4 Comparison of Receiver Architectures

From an analysis of the different receiver architectures above, the challenges in an integrated receiver design, as summarized in Table 2.1 are higher linearity and dynamic range requirements. In addition, for multi-standard capability, the receiver should be able to adapt to the different channel bandwidths and blocking profile of different RF standards.

	Discrete Component Receivers	Fully-Integrated Receivers
Multi-Standard Capability	Lower	Higher
Linearity Requirements	Lower	Higher
Dynamic Range Requirements	Lower	Higher

Table 2.1: Receiver Comparison

2.3 Receiver Specifications

The receiver was designed for the wideband IF with double conversion architecture for the DCS 1800 and DECT standards. DCS 1800 has more stringent linearity and dynamic specifications and is therefore the more challenging standard to meet. The receiver specifications are summarized in Table 2.2 [12].

SPECIFICATIONS	DCS 1800	DECT
Sensitivity (dBm)	-100	-83
Input Noise (dBm)	-120.8	-112.3
Input SNR (dB)	20.8	29.3
Input IP3 (dB)	-18	-26
Required CNR (dB)	9	10.3
Required NF (dB)	11.9	19

Table 2.2: Summary of Receiver Specifications

The sensitivity of a receiver is the minimum detectable signal at the input of the receiver that translates to a sufficient signal to noise ratio at the output of the receiver. This is usually determined by the RF front-end of a receiver. The input noise is the total noise at the antenna multiplied by the channel bandwidths. The input SNR is the ratio of the signal input to the input noise.

The intermodulation requirement is a method to calculate the distortion performance of a receiver block. Two blockers which intermodulate can create a 3rd order component. The Input IP3 is the intercept point of the fundamental and 3rd order intermodulation component. The CNR is the ratio of the carrier to noise at the receiver output to meet the minimum BER requirements of an RF standard. The noise figure of the receiver is the ratio of the SNR input to the SNR output.

2.3.1 DCS 1800 Standard

The DCS 1800 standard is an upbanded version of the GSM standard in the 1800 MHz band [12]. The blocking profile at the receiver input is shown in Figure 2.5. The biggest blocker in this standard is the 3 MHz blocker that is 71 dB above the carrier.

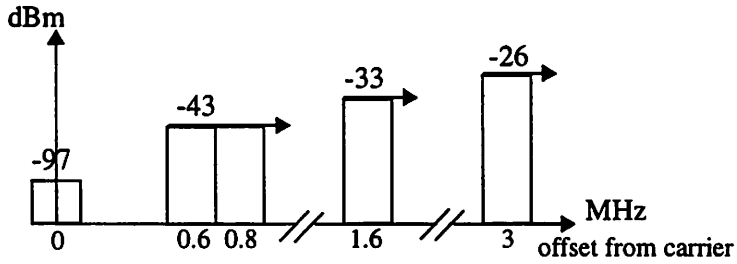


Fig. 2.5: GSM Blocking Profile

Blockers are large undesired signals within the same transmit range of a specific cellular base station.

2.3.2 DECT Standard

The blocking profile for the DECT or Digital Enhanced Cordless Telephone standard is shown in Figure 2.6. Compared with DCS 1800, the DECT standard has more relaxed

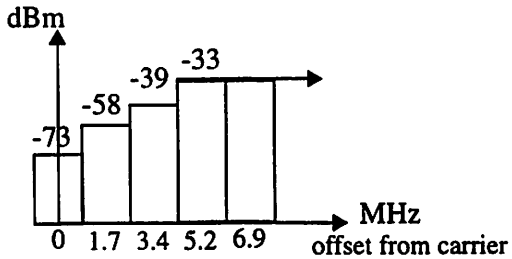


Fig. 2.6: DECT Blocking Profile

blocking requirements [12].

2.4 Summary

Three different receiver architectures were discussed in this chapter. Both the direct conversion and the wideband IF with double conversion receiver architecture were found to have ideal properties for integration and multi-standard operation. The wideband IF with double conversion receiver architecture was eventually selected because of several advantages over the direct conversion receiver. The receiver specifications were described, and a brief explanation on each of the specifications were provided.

Chapter 3

Baseband Design

3.1 Introduction

In integrated receivers, on-chip discrete filters are eliminated. The lack of front-end filtering may lead to a weak desired signal being present next to large blockers at the input of the baseband circuits. This places a more challenging set of requirements on the baseband circuits of integrated receivers. The baseband blocks determine the sensitivity of a receiver, the ability to demodulate a desired signal in the presence of large blockers.

This chapter provides a more detailed discussion of the challenge of designing baseband circuits for integrated receivers and the wideband IF with double conversion receiver architecture in particular. Two types of baseband channel selection are compared. The baseband requirements are also described, with particular emphasis on how they affect the implementation of multi-standard baseband circuits and the baseband filter. Finally, the baseband filter blocks are described in detail.

3.2 Baseband Channel Selection

Performing channel selection at the baseband of receivers allows for more flexibility in integration and multimodal operation. The baseband blocks of the wideband IF double conversion receiver must meet the specifications of the DCS 1800 and the DECT standards and must be programmable to meet the variable bandwidths of 100 kHz and 700 kHz for the two standards respectively.

Three kinds of baseband channel selection are possible: analog, digital and mixed signal. The choice of the type of channel selection impacts the baseband circuits from a dynamic range, programmability, linearity, power dissipation and area perspective.

3.2.1 Analog Channel Selection

Analog channel selection takes the form of Figure 3.1. A simple low-pass filter [13] performs anti-aliasing and is followed by an analog switched-capacitor filter [14] that performs channel selection. Following the switched-capacitor filter, an A/D converter is used to digitize the signal.

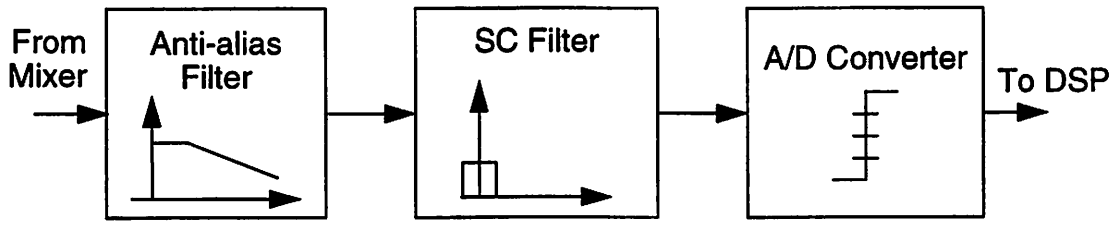


Fig. 3.1: Analog Channel Selection

The anti-alias filter in this configuration can be a simple, continuous time low-pass filter. Process variation is typically not an important issue in this anti-alias filter because the switched-capacitor filter following it has a sharp cut-off. The switched-capacitor filter must have high dynamic range and linearity to select a weak desired signal in the presence of large,

adjacent blokers. Since the switched-capacitor filter has filtered out large adjacent blockers, only a low resolution A/D converter is required to digitized the desired signal.

The disadvantage of analog channel selection with respect to multi-standard operation is the programmability in a switched-capacitor filter. There are two ways to accomplish this. The filter can be designed meet the highest dynamic range requirements and the clock frequency can be modified to change the bandwidth. The other way would be to switch to different capacitor values to change the bandwidth.

3.2.2 Digital Channel Selection

Channel selection can be also be performed digitally, as shown in Figure 3.2. A simple low pass filter performs anti-aliasing and is followed by a high dynamic range A/D converter that digitizes the signal. A sigma-delta modulator [15] is well-suited for this application because the oversampling properties relaxes the requirements of the filter preceding it. In addition, the quantization noise of the modulator is shaped with a high-pass transfer function. The decimation filter [16] following the sigma-delta modulator can therefore remove both the quantization noise and adjacent channel interferers.

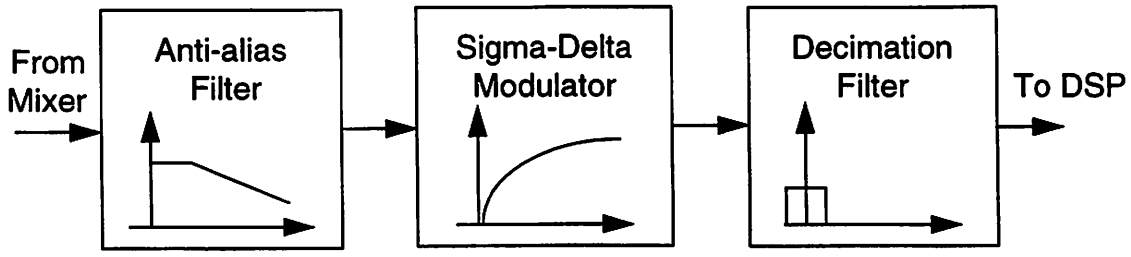


Fig. 3.2: Digital Channel Selection

Programmability is easier to implement with digital channel selection because the same sigma-delta modulator, differing only in oversampling ratio, can be used to meet the

specifications of multiple RF standards. The digital decimation filter which performs channel selection can also be easily made programmable for different channel bandwidths.

3.2.3 Mixed-Signal Channel Selection

In mixed-signal channel selection, channel select filtering is partitioned optimally between the analog and digital domains. As shown in Figure 3.3, the analog low-pass filter performs some analog channel selection. Following an A/D converter, a digital low-pass filter performs digital channel selection. The dynamic range of the A/D converter will depend on the breakdown of the filtering requirements of the analog and digital filter.

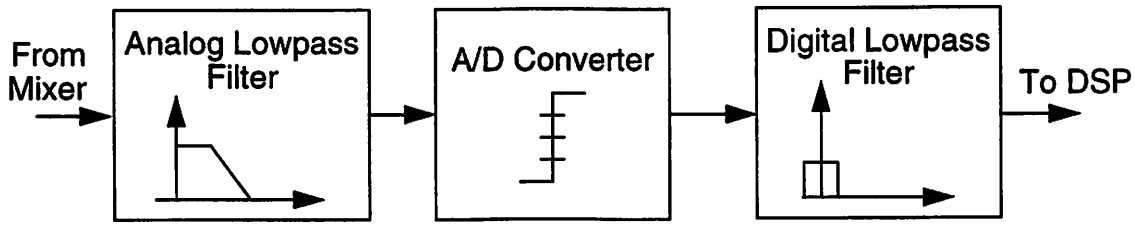


Fig. 3.3: Mixed-Signal Channel Selection

3.2.4 Summary

From the review of the types of channel selection, digital channel selection appears to be most suitable for fully-integrated, multi-standard receiver applications. A high dynamic range, sigma-delta modulator is more easily made programmable than a switched capacitor filter in the analog channel selection case. The modulator can trade off bandwidth and dynamic range to perform A/D conversion. Using a sigma-delta modulator also reduces the anti-aliasing requirements of the filter that precedes it. In addition, programmable channel selection using a digital decimation filter can be realized easily by changing the filter coefficients.

3.3 Baseband Filter for the WBIFDC Receiver

The baseband blocks for the wideband IF with double conversion receiver (WIFDC) performs channel selection digitally. The first block at the baseband of the receiver is the baseband filter. It will be discussed in the following section.

3.3.1 Design Specifications

The overall baseband filter specifications are summarized in Table 3.1 [12]. The function of the filter is to attenuate large adjacent blockers and to perform anti-aliasing. The baseband filter also has a variable gain requirement to accommodate for any gain variation in the RF front-end and to reduce the noise requirements of subsequent stages.

The noise figure of the receiver is targeted at 3.6 dB, and the baseband filter should contribute as little noise as possible. The noise performance of the filter is particularly challenging because of flicker noise in the 100 kHz GSM bandwidth. The linearity of the filter

Noise Resistance	35kΩ (7.62μVrms)
Input Referred IP3	> 7V
$V_{o\text{-}pmax}$	600 mV
A_v	12 dB (+/- 6dB)
Anti-Aliasing Requirements	> 90dB at 25.5MHz (GSM) > 70dB at 44.1 MHz (DECT)
DR	92 dB
Power	minimize
Programmability	DECT, GSM
Bandwidth GSM DECT	 100 kHz 700 kHz

Table 3.1: Baseband Filter Specifications

is also important because a weak desired signal next to large adjacent blockers may be present.

The linearity must meet a 3rd order input intercept point (IIP3) requirement. Again, the GSM standard is the more challenging specification to meet. The filter must be programmable for the DECT and GSM standards as shown in Figure 3.4.

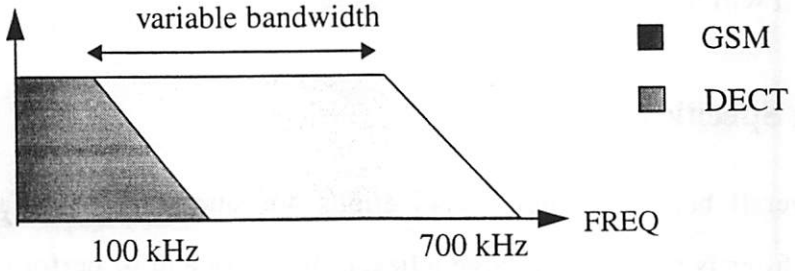


Fig. 3.4: Variable bandwidth for Baseband Filter

3.3.2 Baseband Filter Architecture

The basic structure of the baseband filter is shown in Figure 3.5 [12]. The variable gain requirements of the filter is accomplished with a variable gain amplifier (VGA) with a variable gain of 6-18 dB. This VGA differs from VGAs in superheterodyne receivers. In integrated receivers like the WIFDC, only a moderate amount of gain can be used because both the blockers and the desired signal are gained up. The 6-18 dB of variable gain accommodates for any gain variation in the RF front-end of the receiver to maximize the signal levels at the input of the ADC without overload. In addition, the input-referred noise contribution of subsequent stages are reduced.

The anti-aliasing requirements of the baseband filter is accomplished with a 3rd order filter; one pole at the output of the mixer and a 2nd order Sallen-Key filter following the variable gain amplifier. The pole at the output of the mixer is important to reduce the second order intermodulation requirements of the baseband blocks. The required IP2 requirements of the baseband blocks is a function of the magnitude of the blockers which are present. Because the biggest blocker at the output of the mixer is the 3 MHz blocker, the pole at the output of the

mixer is chosen to be 300 kHz to reduce the 3 MHz blocker by 20 dB. Following the Sallen-Key filter, a buffer is used to drive the sampling network of the sigma-delta modulator.

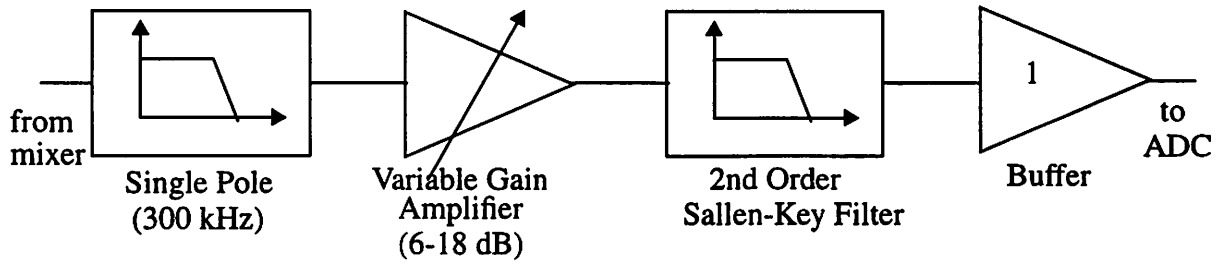


Fig. 3.5: Baseband Filter Architecture

3.3.3 Signal Levels and Slew Rate Requirements

Figure 3.6 best illustrates the signal levels including the desired signal, adjacent channel blockers and out-of band blockers at the output of each block of the baseband filter. Note that the biggest blocker at the output of the mixer is the 3 MHz blocker, but the biggest blocker after filtering by the Sallen-Key is the 600 kHz blocker.

These signal levels are important to calculate the slew rate and current we need in each block of the baseband filter. The slew rate equation is given by

$$SR = \frac{I}{C} = \frac{dV}{dt} \qquad \text{(Eq 3-1)}$$

where $V = \hat{V} \cdot \sin\omega t$

$$\frac{dV}{dt} = \hat{V} \cdot \omega \cdot \cos\omega t$$

where I is the available current and C the load or compensating capacitor driven by the block. The maximum slew rate is then

$$SR_{max} = \hat{V} \cdot \omega \qquad \text{(Eq 3-2)}$$

which is the product of the maximum output step and the frequency of interest. In this design, the maximum output step is the biggest desired signal or blocker seen at the output of each block.

Because we design for the worst case blocking conditions, the maximum slew rate can be calculated for each of the blockers in Figure 3.6. For example, at the output of the variable gain amplifier, the 600 kHz blocker has a magnitude of -12 dBV which translates to 251 mV. The maximum slew rate at 600 kHz is thus

$$\begin{aligned} SR_{max} &= \hat{V} \cdot \omega \\ &= 251\text{m} \cdot (2 \cdot \pi \cdot 600\text{k}) \\ &= 0.95(\text{V}/(\mu\text{s})) \end{aligned} \qquad \text{(Eq 3-3)}$$

The maximum slew rate for the rest of the blockers is shown in Table 3.2. Note that slew rate

Blocker	VGA Slew Rate (V/μs)	Sallen-Key Filter Slew Rate (V/μs)	Buffer Slew Rate (V/μs)
600 kHz	0.95	1.34	1.34
1.6 MHz	2.83	0.89	0.89
3.0 MHz	9.44	0.85	0.85

Table 3.2: Slew Rate Required for Each Baseband Filter Block (GSM)

requirements for the Sallen-Key filter and the buffer is the same because the magnitude of the blockers at the output of their respective blocks are the same.

From the slew rate values given in Table 3.2, we can find the minimum current needed in each block to slew correctly because

$$I_{SR} = SR_{max} \cdot C \qquad \text{(Eq 3-4)}$$

The capacitor C values will differ from block to block depending on the size of the load or compensation capacitors.

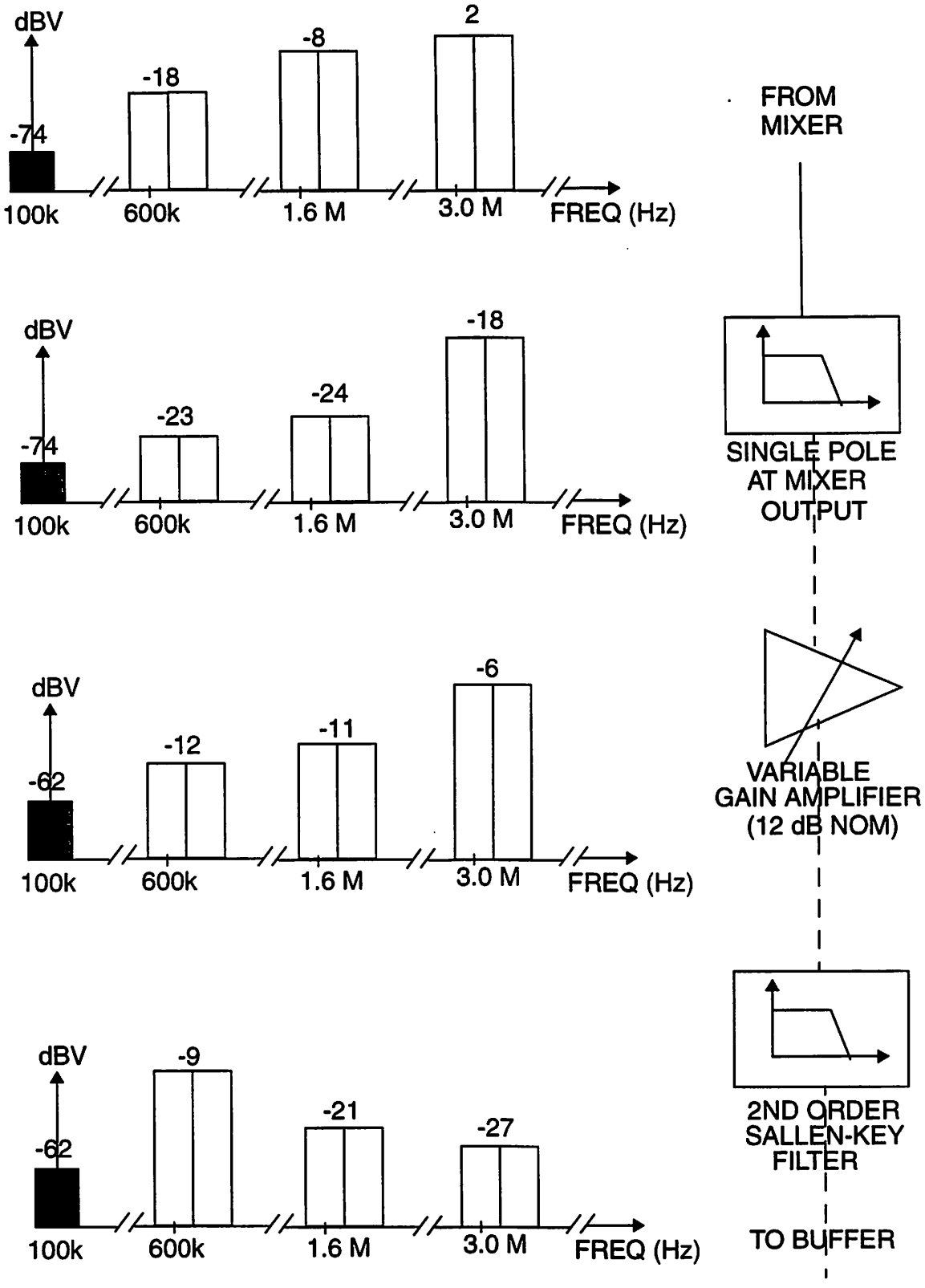


Fig. 3.6: GSM Signal Levels At the Output of Each Baseband Filter Block

3.3.4 Filtering Requirements

3.3.4.1 Anti-Aliasing Requirements

Whenever a signal is sampled, any blocker at multiples of the sampling frequency, f_s will fall into the desired band. The purpose of an anti-aliasing filter is to attenuate all signals which could eventually alias into the desired band [20]. This is shown in Figure 3.7.

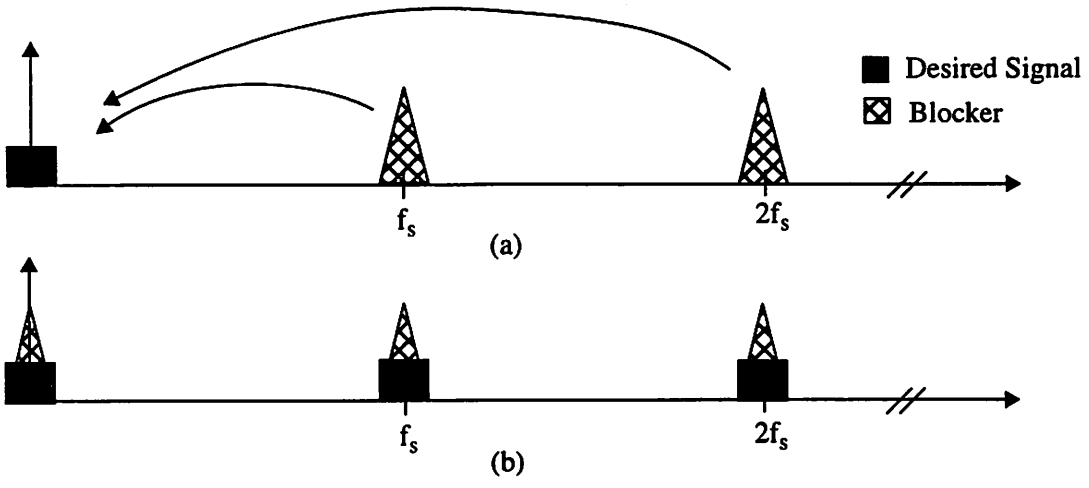


Fig 3.7: (a) Before Sampling (b) After Sampling, blockers fall into desired band

The required anti-aliasing requirements for the filter is then the difference between the magnitude of the blockers at f_s and the minimum desired signal, added to the carrier-to interference (C/I) ratio of 12 dB. From the GSM blocking profile, we see that the minimum desired signal is at -97 dBm and the blocker at f_s is at -26 dBm. The required attenuation for GSM is then

$$\text{Attenuation at } f_s > (-26) - (-97) + 12 = 83\text{dB} \qquad \text{(Eq 3-5)}$$

Similar calculations for the DECT blocking profile yield attenuation requirements of greater than 70 dB.

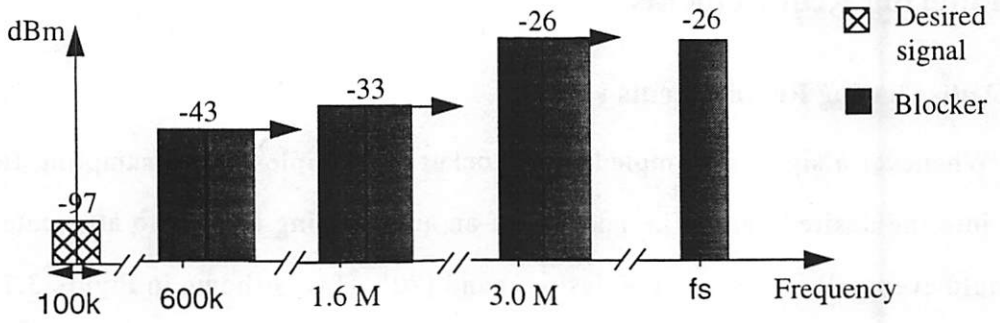
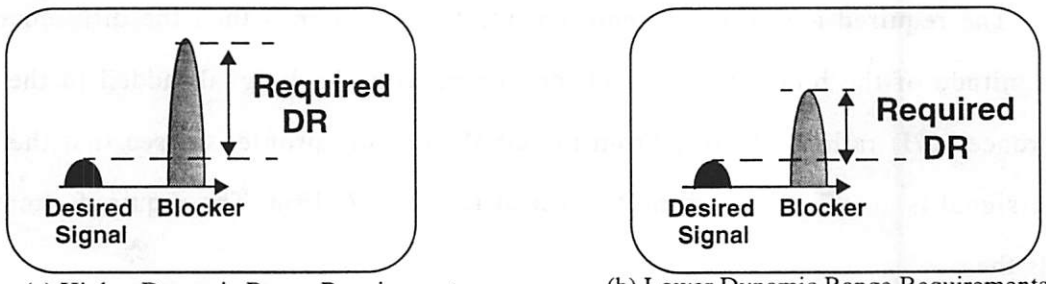


Fig 3.8: GSM Blocking Profile

3.3.4.2 Blocker-Attenuation Requirements

The required dynamic range is the difference between the blocker and the desired signal as shown in Figure 3.9. The more the blocker is attenuated, the lower the requirements of the ADC block.

The GSM standard is the determing standard and it has tougher blocker-attenuation requirements. The key blockers are at 600 kHz, 1.6 MHz and at 3.0 MHz. The DECT standard has blocker-attenuation requirements at 3.56 MHz and at 5.34 MHz.



(a) Higher Dynamic Range Requirements (b) Lower Dynamic Range Requirements

Fig 3.9: Dynamic Range Comparison with different Blocker Attenuation

A summary of both the anti-aliasing and blocker attenuation requirements is given in Table 3.3 [12].

Filter Specifications	GSM	DECT
Passband	100 kHz	700 kHz
Anti-aliasing Requirements	>90 dB at 25.6 MHz	>70 dB at 44.1 MHz
Attenuation at 600 kHz	>3 dB	N/A
Attenuation at 1.6 MHz	>25 dB	N/A
Attenuation of 3.0 MHz	>40 dB at 3.0 MHz	N/A
Attenuation of 3.56 MHz	N/A	>6 dB at 3.56 MHz
Attenuation of 5.34 MHz	N/A	>12 dB at 5.34 MHz

Table 3.3: Filtering Requirements

3.4 Sigma-Delta Modulator

The baseband filter drives the sampling network of the sigma-delta modulator. The sampling frequency and sampling capacitor of the modulator determine the settling requirements of the baseband filter block that precedes the modulator.

A sigma-delta modulator trades resolution in time for resolution in amplitude. It employs oversampling and feedback to shape the quantization noise with a high-pass function [17]. The oversampling ratio, the quantizer resolution and the order of the modulator determines the dynamic range of the modulator. In this work, a 4th order sigma-delta modulator using a 2-2 MASH architecture was used. The specifications of the modulator are summarized in Table 3.4[18].

SPECIFICATIONS	GSM	DECT
Modulator Order	4	4
Oversampling Ratio	128	32
Sampling Frequency (MHz)	25.6	44.8
Dynamic Range (dB)	86	74
Sampling Capacitor (pF)	5	1.5

Table 3.4: Sigma-Delta Modulator Specifications

3.5 Summary

The goal of this chapter was to convey the challenges of designing baseband circuits for fully-integrated, multi-standard RF receivers. Digital channel selection was selected because it allows for more programmability in the sigma-delta modulator and the decimation filter. Using a sigma-delta modulator eases the anti-aliasing requirements of the baseband filter that precedes it.

The baseband filter requires high linearity and dynamic range to meet the specifications of the GSM and DECT standards. The filter includes a variable gain amplifier that accommodates for any frequency variation in the RF front-end and maximizes the input to sigma-delta modulator. The VGA also reduces noise requirements of subsequent stages. The baseband filter architecture and design must be tailored to the worst-case blocking conditions for GSM.

Chapter 4

Variable Gain Amplifier Design

4.1 Introduction

The variable gain amplifier design will be presented in this chapter. The variable gain amplifier precedes the 2nd order Sallen-Key filter in the overall baseband filter architecture. It functions to accommodate for any gain variation in the RF front-end to maximize the input to the sigma-delta modulator without overload. Recall that the VGA gain varies from 6-18 dB with a nominal gain of 12 dB.

There are many ways to implement a variable gain amplifier but the design must satisfy the high linearity requirements of the GSM standard. This limits the variable gain realization to linear poly-poly or metal capacitors and poly resistors. In addition, having the amplifier in feedback topology also improves the linearity of the VGA.

The opamp design is discussed in detail, along with the breakdown of the noise and power dissipation. Simulation results are also presented.

4.2 Variable Gain Amplifier Architecture

Shown in Figure 4.1 are two possible architectures to implement the variable gain. In case (a), the gain is a ratio of the capacitors, as described below.

$$A_{dc} = \frac{C_x}{C_y} \qquad \text{(Eq 4-1)}$$

In case (b), the gain is a ratio of resistors, as described below

$$A_{dc} = \frac{R_y}{R_x} \qquad \text{(Eq 4-2)}$$

By switching to different capacitors or resistors, a wide range of variable gain can be achieved.

There are certain tradeoffs with each configuration. The resistive VGA is noisier than the capacitive VGA case because of thermal noise from the resistors which is given by

$$V_R^2 = 4kTR\Delta f \qquad \text{(Eq 4-3)}$$

In the capacitive VGA (a) case, the dc voltages at V_x are not defined. This can be resolved with a very large resistor across C_y. However, this creates a high-pass transfer function which will fall into the desired bandwidth. The dc voltages can also be defined by

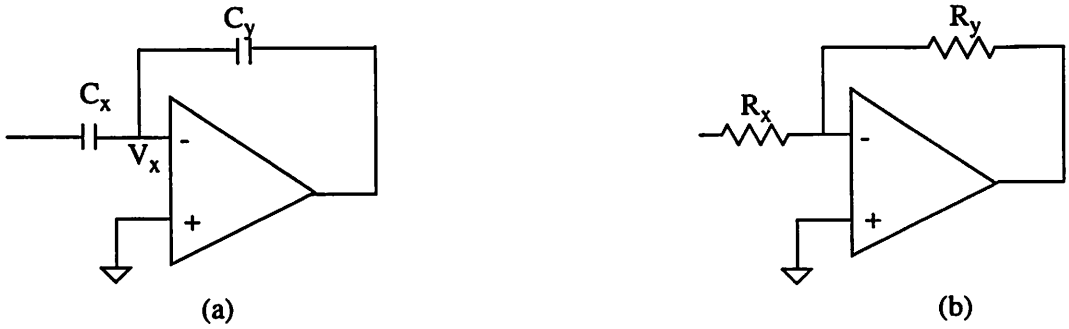


Fig. 4.1: (a)Capacitive Variable Gain Amplifier (b)Resistive Variable Gain Amplifier

using a switched-capacitor feedback circuit that refreshes the input and output nodes. The refresh rate must be at least the sampling rate of the sigma-delta modulator to ensure that the V_x node will have correct voltages when the sigma delta modulator is sampling. However, a capacitive feedback circuit creates glitches at the harmonics of the sampling frequency. For these reasons, the resistive variable gain amplifier was selected.

The final architecture for the variable gain amplifier is shown in Figure 4.2. A fully-differential configuration holds several advantages. Differential circuits have been shown to effectively attenuate even-order harmonic distortion, substrate noise and other common-mode disturbances. In addition, in differential circuits, noise power is doubled while the signal power increases by four times. This results in a net gain of 3dB in dynamic range. The only drawback in adopting a fully-differential VGA is the need for a common-mode feedback circuit.

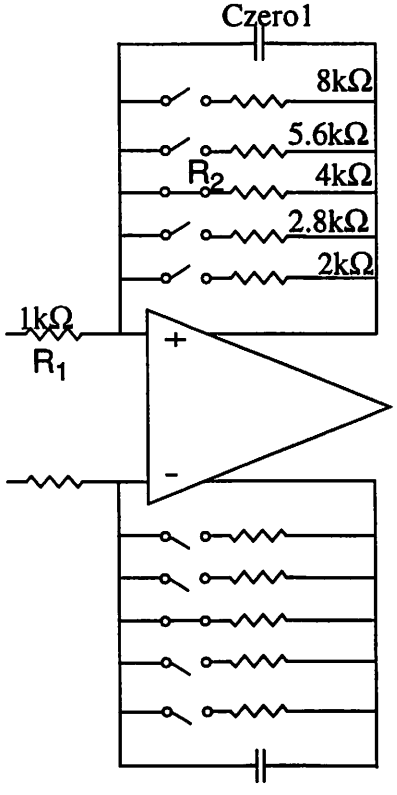


Fig. 4.2: Variable Gain Amplifier Architecture with nominal gain of 12 dB

The nominal gain of 12 dB is achieved by switching in the feedback resistors with a value of 4 kΩ. Similarly, the gains of 6 dB, 9 dB, 15 dB and 18 dB are achieved by switching in the feedback resistors with values of 2 kΩ, 2.8 kΩ, 5.6 kΩ and 8kΩ respectively. This range of gain is chosen from the worst and best case gain variation from the RF blocks. The discrete 3 dB steps is chosen to be small enough to minimize the amout of dynamic range by which the ADC needs to be overdesigned to acommodate the RF front-end gain variation.

The resistor values must be chosen to minimize the thermal noise. A value of 1kΩ is chosen for R_1 to meet the noise specifications. This is also the minimum value that will not degrade the gain of the stage that precedes the variable gain amplifier. The gain and noise specifications will then determine the values of the feedback resistors R_2. CMOS switches are used to switch to different values of resistor R_2 and will be described in more detail in the next section.

4.2.1 Switches for the Variable Gain Amplifier

As shown in Figure 4.3, PMOS switches conduct very well for large values of V_{in}. NMOS switches conduct very well for small values of V_{in} [19][20][21]. Because the common-mode output voltage of V_{in} is in mid-supply, complementary (CMOS) switches are selected for this VGA. The on resistances of the CMOS switches are given by

$$R_{on} = \frac{1}{\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_n \cdot (V_{GSn} - V_{THn}) + \mu_p \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_p \cdot (V_{GSp} - V_{THp})} \qquad \text{(Eq 4-4)}$$

$$= \frac{1}{\mu_n \cdot C_{ox} \cdot \left(\frac{W}{L}\right)_n \cdot (V_{dd} - V_{THn} - V_{THp})} \qquad \text{if } \boxed{\mu_n \cdot \left(\frac{W}{L}\right)_n = \mu_p \cdot \left(\frac{W}{L}\right)_p}$$

The device sizes for the NMOS and the PMOS transistors are selected for equal impedances. This implies that the W/L ratio is a ratio of their respective mobilities so that the equivalent CMOS resistance is not a function of the input voltage.

To minimize distortion, the switches are placed at the input instead of the output nodes of the opamp.

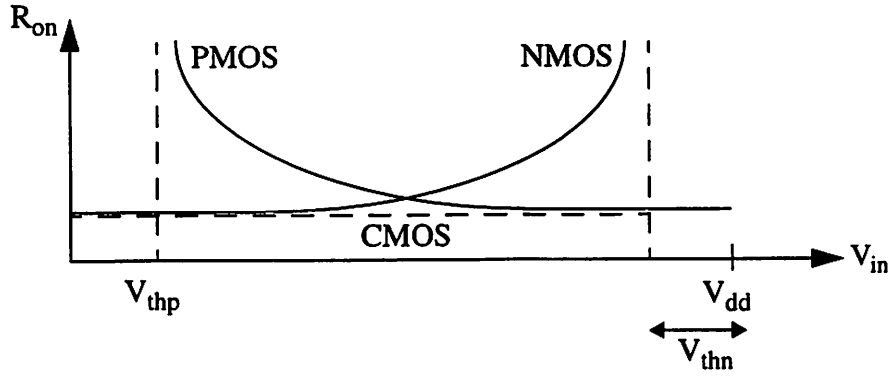


Fig. 4.3: Switch Nonlinear On Resistance

4.3 VGA Operational Transconductance Amplifier

Several fundamental issues and trade-offs exist when selecting an optimal architecture for the operational transconductance amplifier (OTA). Firstly, the gain of the OTA must be high enough so that the 3rd order intermodulation is kept sufficiently small. The basic equation for the 3rd order intermodulation is given by

$$IM_3 = \frac{3}{4} \cdot \frac{a_3}{a_1} \cdot \frac{S_1^2}{(1 + a_1 \cdot f)} \qquad \text{(Eq 4-5)}$$

where S_1 is the input signal, a_1 is the gain of the fundamental or in this case the open-loop gain of the OTA, a_3 is the gain of the 3rd order component and f is the feedback factor. The higher the open-loop gain of the OTA, the lower the 3rd order intermodulation.

The number of gain stages in the OTA is determined from the low-frequency gain requirement. A single-stage OTA cannot achieve a high gain because the 3.3 V supply limits the number of cascodes. Therefore, a 2-stage amplifier is selected for this design.

The first stage of the amplifier can be designed using either a telescopic or folded-cascode topology, shown in Figure 4.4. The topology with lower power consumption and lower noise should be chosen for this design. There are four current legs between Vdd and ground in the folded cascode topology while there are only two current legs in the telescopic amplifier. This implies that the telescopic amplifier consumes less static power.

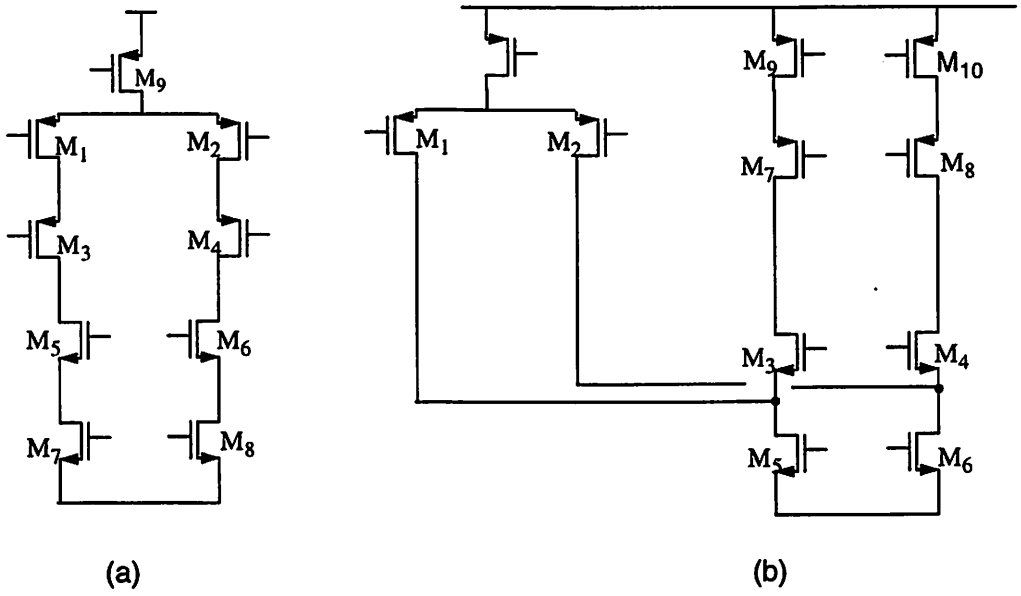


Fig. 4.4: (a) Telescopic (b) Folded-Cascode

From a noise perspective, the folded-cascode amplifier has six noise contributing devices--M_1, M_2, M_5, M_6, M_9, M_{10}. It can be shown that the cascode devices (M_3, M_4, M_7, M_8) contribute negligible noise to the amplifiers. In the telescopic amplifier, only four transistors--M_1, M_2, M_7, M_8 contribute significant noise [25]. Because the telescopic amplifier has fewer current legs and fewer noise-contributing devices, it was selected for this design.

Flicker noise is also an important design consideration. Caused by the charge and discharge of oxide traps at the silicon-silicon dioxide surface, the flicker noise from PMOS

devices is about three times lower than NMOS devices because of speed of the PMOS carriers. The input devices of both the telescopic and folded-cascode amplifier are thus chosen to be PMOS to lower flicker noise.

The OTA is designed to be fully differential. This doubles the effective output swing. Because the signal power quadruples while the noise power only doubles, the dynamic range is also doubled.

The complete 2-stage differential OTA used for the variable gain amplifier is shown in Figure 4.5. The first stage is telescopic while the second stage is a common source stage. Cascode compensation is used in this OTA because it has been shown to provide a higher bandwidth than Miller compensation. Cascode compensation creates a dominant pole and two complex poles at a higher frequency [22][23][24]. This compensation method will be described

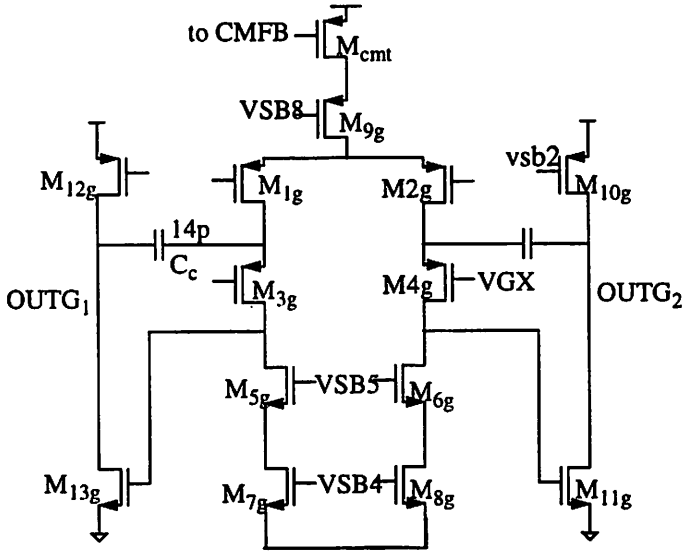


Fig. 4.5: 2-Stage OTA with Cascode Compensation

in more detail in Section 4.3.4.

Note that the gate of the current source is connected to a common-mode feedback circuit that will be described later.

4.3.1 Thermal Noise

The input-referred thermal noise of a transistor is given by

$$\overline{V_n^2} = 4kT\frac{2}{3}\cdot\frac{1}{g_m}\Delta f \qquad \text{(Eq 4-6)}$$

The input-referred thermal noise of the amplifier in Figure 4.5 is contributed mainly by the input devices and the load devices. The cascode devices contribute negligible noise when referred to the input.

The input-referred thermal noise power is given by

$$\begin{aligned} P_{noise} &= P_{thermal} \\ &= 2\cdot\left[4kT\cdot\frac{2}{3}\cdot\frac{1}{gm_1}\left(1+\frac{gm_7}{gm_1}\right)\right]\Delta f \end{aligned} \qquad \text{(Eq 4-7)}$$

To reduce the thermal noise in the amplifier, the noise factor of the amplifier should be minimized. The noise factor is $(1 + g_{m7}/g_{m1})$. The ratio of the transconductance g_{m7}/g_{m1} should thus be minimized. However, the transconductance of a device is inversely proportional to its V_D^{sat}, as given by

$$g_m = \frac{2I_D}{V_D^{sat}} \qquad \text{(Eq 4-8)}$$

For a fixed current, this is equivalent to minimizing $V_{D1}^{sat}/V_{D7}^{sat}$. Designing for a noise factor of 1.6, V_{D1}^{sat} is chosen to be 350mV and V_{D7}^{sat} to be 600 mV.

An important consideration in choosing the V_D^{sat} values is the output swing. To achieve an output swing of 700 mV (single ended) at the output of the second stage, the required headroom at the output of the first stage is only 70 mV assuming that the gain in the

second stage is 10 or greater. Leaving a margin of 200 mV on each $V_D{}^{sat}$, the sum of all the $V_D{}^{sat}$s in the first stage must be less than about 2 V. Because $V_{D9}{}^{sat}$ and $V_{Dcmt}{}^{sat}$ are each chosen to be 100 mV, and because $V_{D3}{}^{sat}$ and $V_{D5}{}^{sat}$ will be shown later to be small (100-200mV), there is sufficient headroom in the first stage to achieve the noise factor of 1.6.

To leave sufficient margin for flicker noise, the thermal noise floor needs to be lowered. This is achieved by increasing the current in each of the opamp stages.

4.3.2 Flicker Noise

Flicker noise is caused by the charging and discharging of oxide traps near the Si-SiO_2 interface. The oxide trapping time constant is inversely proportional to frequency and because of this, flicker noise is sometimes known as 1/f noise. PMOS devices have a slower oxide trapping time constant compared to NMOS devices and thus contribute flicker noise that is three times lower for this process. The input referred flicker noise for a PMOS device is given by

$$V_f^2 = \frac{K_{fp}}{fWLC_{ox}}\Delta f \qquad \text{(Eq 4-9)}$$

The flicker noise contributing devices are the input and load devices, as given by

$$P_{flicker} = 2 \cdot \left[\frac{K_{fp}}{W_1 \cdot L_1 \cdot C_{ox}} \left(1 + \frac{K_{fn} \cdot L_1^2 \cdot \mu_n}{K_{fp} \cdot L_7^2 \cdot \mu_p} \right) \Delta f \right] \qquad \text{(Eq 4-10)}$$

The cascode devices contribute negligible flicker noise. To reduce the flicker noise contribution, the input devices should be made bigger. Increasing the input device sizes however increases C_{gs1}, which in turn increases the non-dominant pole caused by the combination of C_{gs1} and the resistors R_1 and R_2. This is compensated by Czero, which cancels out the pole with a phase lead, according to the following equation

$$\frac{1}{C_{gs1} \cdot (R_1 \| R_2)} = \frac{g_{m1}}{C_{zero}}$$

A value of 10 pF was used in this design for a C_{gs1} of 2.5 pF, and was simulated across process and for the 6-18 dB of variable gain to ensure adequate phase margin.

From (Eq 4-10), the flicker noise is also proportional to the ratio of the channel length of the input and load devices. The lengths of the load devices are made longer than the input devices to reduce the flicker noise contribution.

4.3.3 DC Gain

The low frequency gain of the OTA in Figure 4.5 is shown below as

$$A_{DC} = g_{m1} \cdot (g_{m3} \cdot r_{o3} \cdot r_{o1} \| g_{m5} \cdot r_{o5} \cdot r_{o7}) \cdot g_{m13} \cdot (r_{o13} \| r_{o12} \| [R_1 + R_2]) \quad \text{(Eq 4-11)}$$

The output resistance, r_o is proportional to the channel length, is given by

$$r_o = \frac{1}{\lambda I_{DS}} \propto L \quad \text{(Eq 4-12)}$$

Therefore, to increase the low-frequency gain of the OTA, the load devices of the first stage (M_7-M_8) are made long channel devices. Because these devices do not capacitively load the signal path, increasing the channel lengths of these devices does not slow down the amplifier. In the second stage, increasing the lengths of the load devices will capacitively load the outputs. In addition, the output resistance of the second stage is limited by the loading of R_1 and R_2. For example, the parallel combination of r_{o13} and r_{o12} gives approximately 8kΩ while the $(R_1 + R_2)_{min}$ combination gives 3kΩ.

4.3.4 Frequency Response

The half-circuit small-signal model for the amplifier is shown in Figure 4.6. For simplicity, the output resistances are assumed to be infinite.

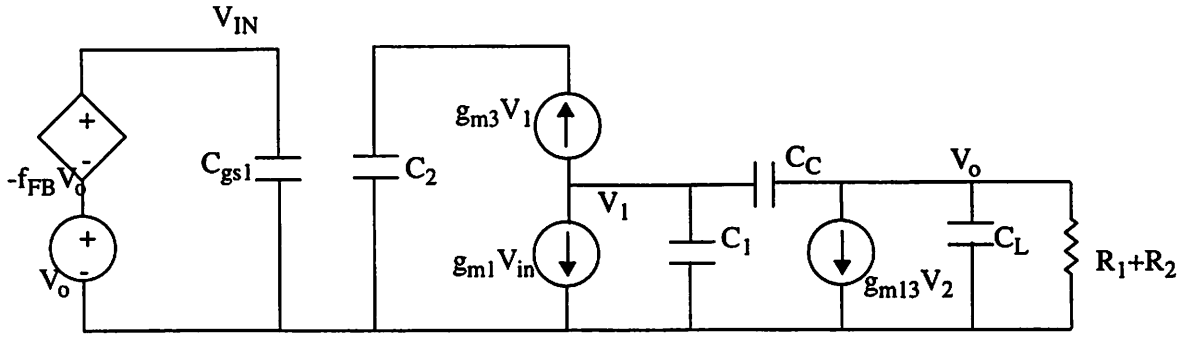


Fig. 4.6: Simplified Small-Signal Model

C_1 is the total capacitance at the drain of M_1. C_2 is the total capacitance at the drain of M_3. C_C is the compensation capacitor and C_L is the total load capacitance. The parameter f_{FB} is the feedback factor when the OTA is used in a feedback loop with the VGA resistors and is given by

$$f_{FB} = \frac{R_1}{R_1 + R_2} \qquad \text{(Eq 4-13)}$$

The complete transfer function for the amplifier is given by

$$H(s) = \frac{\frac{g_{m1}}{C_2 C_T^2}(g_{m3}g_{m9} - C_2 C_C s^2)}{s^3 + \left[\frac{g_{m3}(C_L + C_C) - f g_{m1} C_C}{C_T^2}\right]s^2 + \frac{g_{m3}g_{m9}C_C}{C_2 C_T^2}s + \frac{f g_{m1} g_{m3} g_{m9}}{C_2 C_T^2}} \qquad \text{(Eq 4-14)}$$

where
$$C_T^2 = C_1 C_L + C_1 C_C + C_L C_C$$
$$C_1 = C_{gd1} + C_{gs3}$$
$$C_2 = C_{gd3} + C_{gd5} + C_{gs13}$$
$$C_L = C_{gd12} + C_{gd13} + C_{C,bottom} + C_{zero,bottom} + C_{zero}(1 - f_{FB})$$

The non-dominant poles in the circuit can be approximated by

$$p_2 \cong \frac{g_{m13}}{C_L} \qquad \text{(Eq 4-15)}$$

and

$$p_3 \cong \frac{g_{m3}}{C_C + C_{gs3} + C_{gd1}} \qquad \text{(Eq 4-16)}$$

Since there are two non-dominant poles chose together, they should be made at least 4x the closed loop unity-gain frequency (ω_{uT}) below

$$\omega_{uT} = \frac{g_{m1}}{C_C} \cdot f_{FB} \qquad \text{(Eq 4-17)}$$

to ensure sufficient phase margin. This suggests that $g_{m3} >> f_{FB}\, g_{m1}$ and $g_{m13} >> f_{FB}\, g_{m1}\, C_L/C_C$.

Since the current through M1 and M3 is the same, we need $V_{D3}^{sat} << V_{D1}^{sat}/f_{FB}$. For this design, V_{D3}^{sat} is chosen to be 100 mV and V_{D1}^{sat} to be 350 mV. To satisfy $g_{m13} >> f_{FB}\, g_{m1}\, C_L/C_C$, the V_D^{sat} of M13 must satisfy

$$V_{D13}^{sat} \ll \frac{I_{SS,12}}{I_{SS,9}} \cdot \frac{1}{f_{FB}} \cdot \frac{C_C}{C_L} \cdot V_{D1}^{sat} \qquad \text{(Eq 4-18)}$$

For this design, V_{D13}^{sat} is chosen to be 800 mV.

Since the cascode compensation produces two zeros at approximately equal frequencies in both the left and right half planes, the zeros do not degrade the phase margin of the OTA.

4.3.5 Summary of Opamp Device Sizes

The device sizes for the opamp are presented in Table 4.1 below.

Devices	V_D^{sat}	Length
M_{1g}, M_{2g}	350 mV	6 µ
M_{3g}, M_{4g}	100 mV	0.35 µ
M_{5g}, M_{6g}	200 mV	0.35 µ
M_{7g}, M_{8g}	600 mV	10 µ
M_{9g}	100 mV	0.7 µ
M_{10g}	450 mV	0.7 µ
M_{11g}	830 mV	0.35 µ
M_{cmt}	100 mV	0.7 µ

Table 4.1: VGA Opamp Device Sizes

4.3.6 Biasing

Figure 4.7 shows the biasing network for the OTA. One master current source is used and a variety of bias currents are generated using current mirrors. High-swing biasing is

adopted for both PMOS and NMOS cascode devices. An internal cascode bias is used for M_3 and M_4 and this is shown in (b).

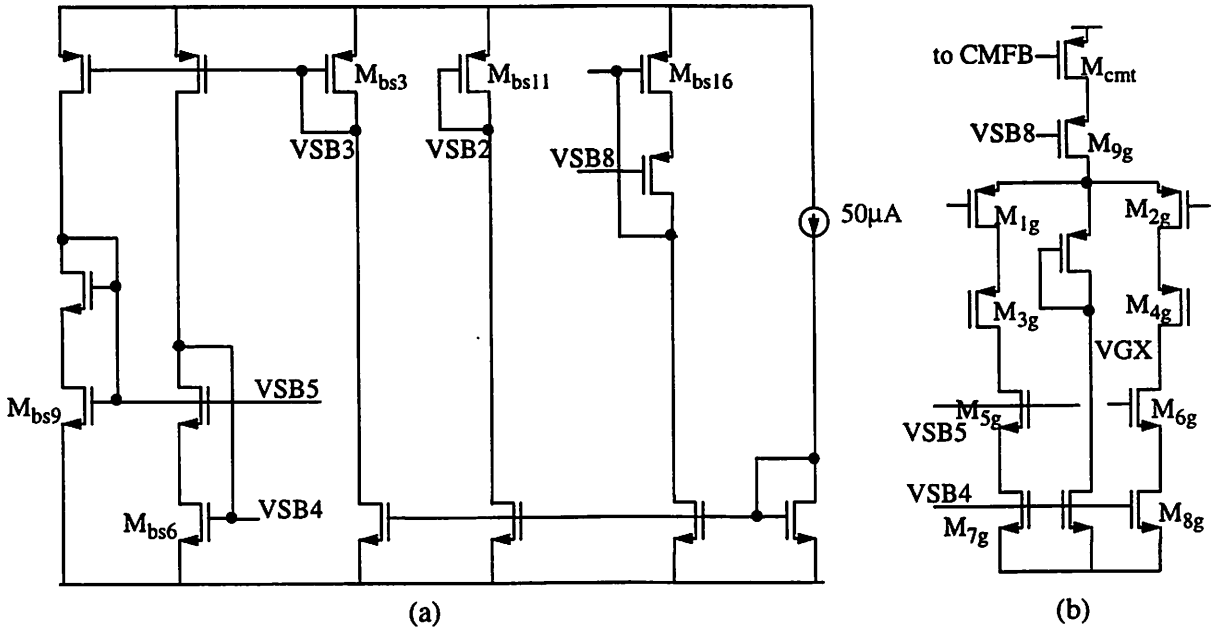


Fig. 4.7: (a) Biasing Circuits (b) Internal Biasing

The $V_D{}^{sat}$s of the biasing devices are chosen to be identical to those in the OTA to ensure good matching. The VDS of the OTA is biased to be 200 mV greater than their respective $V_D{}^{sat}$s. Device M_{bs6} is also made the same channel length as M_{7g} to improve matching. Decoupling capacitors to Vdd for PMOS bias devices and ground for NMOS bias devices are used at all biasing nodes to keep the DC bias voltages stable. Power dissipation can be reduced by decreasing the currents in the biasing stage.

4.3.7 Common-mode feedback

In a fully-differential amplifier, common-mode feedback is needed to define the DC voltages at the high-impedance output nodes. A continuous-time common-mode feedback circuit is used here, as shown in Figure 4.8.

The continuous-time common-mode feedback circuit is designed using a simple differential pair. The gate of M_{cm2} is tied to the desired output voltage, $V_{o,desired}$. The resistors R_{cm1} and R_{cm2} sense and average the output voltages of the OTA. The diode connection of Mcm3 is tied to the current source of the OTA and completes the feedback loop. The loop operates by steering current in or out of the current source device, M_{cmt}.

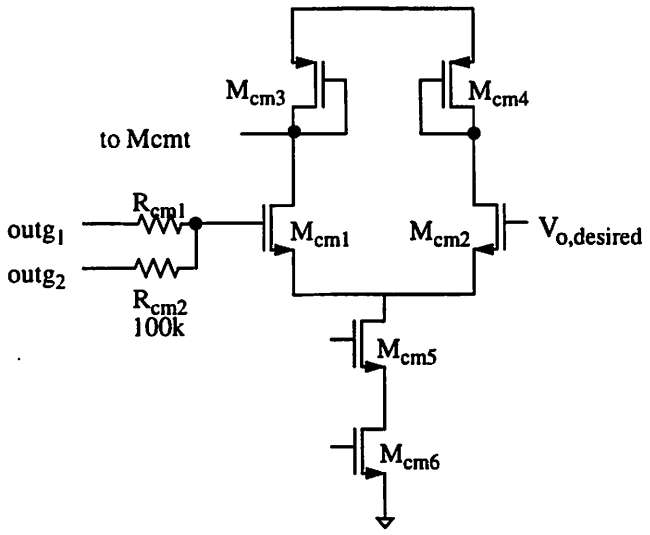


Fig. 4.8: Continuous-time Common-Mode Feedback

The unity-gain bandwidth of the common-mode feedback circuit is approximated by

$$\omega_{uT,\,CMFB} = \left(\frac{g_{m,\,cmt}}{C_C}\right)\cdot f$$

$$= \frac{g_{m,\,cmt}}{C_C}\cdot\left(\frac{1}{2}\cdot\frac{g_{m,\,cm1}}{g_{m,\,cm3}}\right) \qquad \text{(Eq 4-19)}$$

The unity-gain bandwidth of the common-mode feedback circuit should be the same or higher than that of the OTA so that it does not slow down the amplifier. This can be achieved by making $g_{m,cm1} >> g_{m,mcm3}$. In other words, the $V_D{}^{sat}$ of M_{cm3} should be bigger than M_{cm1}.

4.4 Simulation Results

The input-referred noise of the variable gain amplifier for GSM and DECT is shown in Table 4.2 and Table 4.3. The noise was analysed using SPICE for different VGA gain settings.

Gain (dB)	Input Referred Noise (μV)
6	2.9
9	2.84
12	2.68
15	2.57
18	2.48

Table 4.2: VGA Noise breakdown for different gain settings (GSM)

Gain (dB)	Input Referred Noise (μV)
6	7.13
9	6.7
12	6.3
15	5.85
18	5.57

Table 4.3: VGA Noise breakdown for different gain settings (DECT)

The minimum gain setting gives the highest input-referred noise because the total output noise is divided by a much lower gain.

The noise breakdown for the minimum gain setting (GSM) is shown in Figure 4.9. As can be seen, the dominant source of noise is resistor R_1 which contributes about 38% of the noise. The rest of the noise is divided fairly equally among the resistor R_2, the opamp thermal noise and the opamp flicker noise. When resistor R_2 changes to accommodate a higher gain, the output noise contribution from R_2 increases. However, the total input referred noise decreases

because it is divided by the higher gain. Therefore, the additional noise from R_2 is insignificant.

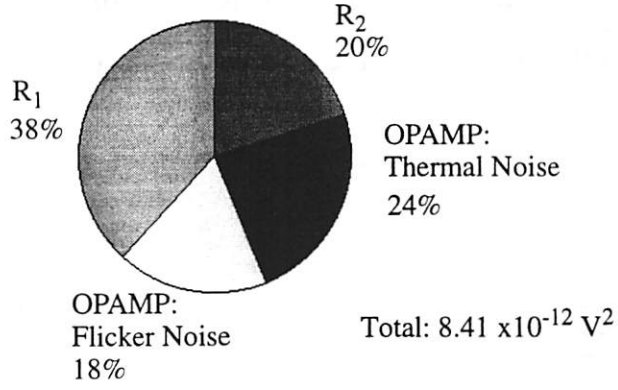


Fig. 4.9: Noise Breakdown of Variable Gain Amplifier (GSM)

The dynamic range of the VGA is defined by the ratio of the signal to the total noise in the circuit, as given below

$$DR_{in} = \frac{P_{signal,in}}{P_{noise,in}} \qquad \text{(Eq 4-20)}$$

$$\text{where } P_{signal,in} = \frac{\hat{V}_{in}^2}{2} = \frac{(200mV)^2}{2} = (0.02)$$

$$P_{noise,in} = 2\left[4kTR_1 \cdot \left(1 + \frac{R_1}{R_2}\right) + \frac{P_{OTA,in}}{\left(\frac{R_2}{R_1 + R_2}\right)^2}\right]\Delta f$$

$P_{noise,in}$ is the input-referred VGA noise from Table 4.2 above. The dynamic range for GSM for the minimum gain setting is then

$$DR = 10 \cdot \log\left(\frac{0.02}{8.4x10^{-12}}\right) = 93.7dB \qquad \text{(Eq 4-21)}$$

Recalculating the dynamic range for DECT using (Eq 4-20) and the input-referred noise from Table 4.3 for the minimum gain setting gives 86 dB.

The magnified plot of the magnitude response of the VGA circuit is shown below. The nominal gain is 12dB. The VGA gain can be programmed up to 18 dB or down to 6 dB in steps of 3 dB.

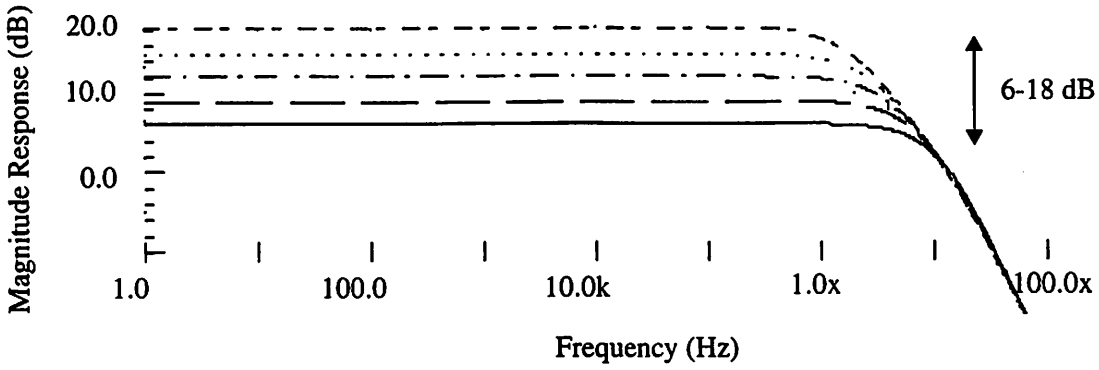


Fig. 4.10: VGA Magnitude Response

4.5 Summary

This chapter investigated the design of a variable gain amplifier. The chapter began with a comparison of different system-level implementations of variable gain. CMOS switches were used to switch to different gains because the common-mode voltage of the VGA was in mid-supply. Following that, an opamp topology was selected that had the minimum number of current legs and minimum number of noise contributing devices to reduce the power dissipation. The opamp was designed with PMOS inputs to lower flicker noise. The first stage was a telescopic amplifier and the second stage was a common source stage. Design requirements like DC gain, noise and slew rate determined the device sizes. Finally, simulation results for the variable gain amplifier were presented.

Chapter 5

Sallen-Key Filter Design

5.1 Filter Specifications

Recall that the architecture of the baseband filter was selected in Chapter 3, and it was decided that for linearity reasons, the filtering specifications would be accomplished with one pole at the output of the mixer, followed by a second order filter after the variable gain amplifier. In this chapter, the design of the 2nd-order filter will be discussed.

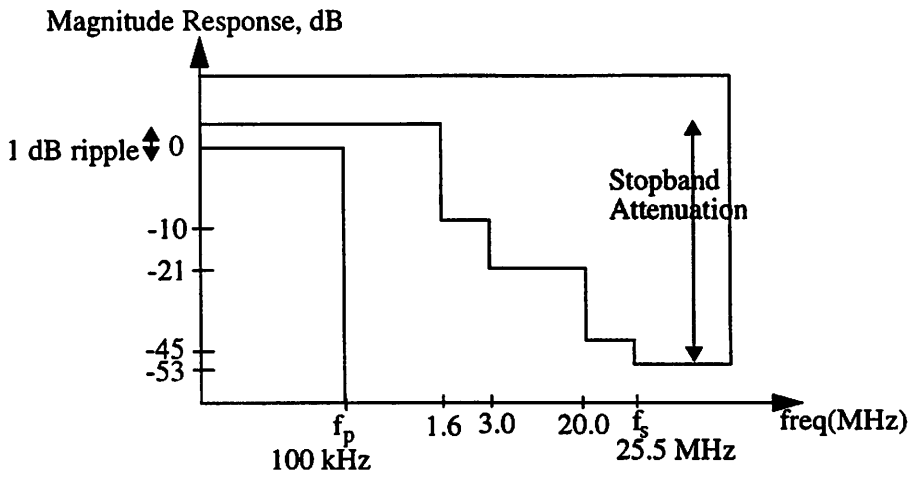


Fig. 5.1: Specification of the transmission characteristics for GSM

Based on the attenuation requirements for the baseband filter given in Chapter 3, the attenuation requirements for the Sallen-Key filter alone can be calculated. This assumes that the first pole at the output of the mixer is at 300 kHz. A plot of the transmission characteristics for both GSM and DECT is shown in Figure 5.1 and Figure 5.2. The parameter f_p is the passband frequency and the parameter f_s is the stopband frequency.

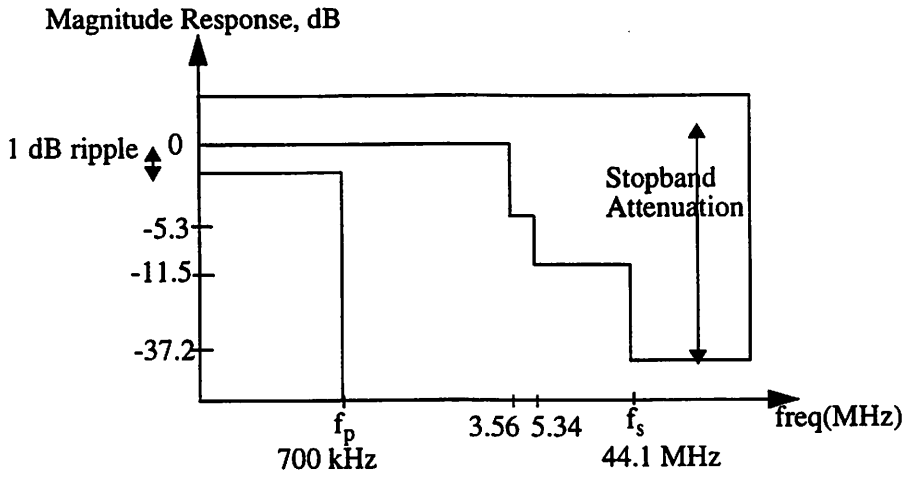


Fig. 5.2: Specification of the transmission characteristics for DECT

5.1.1 Linearity

The linearity of the anti-alias filter is just as important as that of the variable gain amplifier. In fact, the requirements are more challenging because at the input of the filter, both the desired signal and the blockers have been gained up. Both the 2nd and 3rd order intermodulation performance are analyzed in this section.

If we assume a nonlinear relationship in a system, the transfer function can be approximated by

$$S_o(t) = a_1 \cdot S_i(t) + a_2 \cdot S_i^2(t) + a_3 \cdot S_i^3(t)... \qquad \text{(Eq 5-1)}$$

S_o is the output signal and $S_i=(S_1\cos\omega_1 t + S_2\cos\omega_2 t)$ is the input signal. The parameter a_1 is the gain of the fundamental, a_2 is the gain of the second order component and

a_3 is the gain of the third order component. By expanding the 2nd order nonlinearity equation as shown below

$$a_2 \cdot (S_1 \cos\omega_1 t + S_2 \cos\omega_2 t)^2 = a_2[(S_1 \cos\omega_1 t)^2 + (S_2 \cos\omega_2 t)^2 + 2S_1 S_2 \cos\omega_1 t \cdot \cos\omega_2 t] \quad \text{(Eq 5-2)}$$

we find that the relationship between the 2nd order intermodulation becomes [26]

$$IM_2 = \frac{a_2}{a_1} \cdot S_1 \quad \text{(Eq 5-3)}$$

This means that when a weak desired signal is translated down to baseband in the presence of large adjacent blockers, the large blockers will pass through the 2nd order nonlinearities and create a component in the desired band. Because the 2nd order intermodulation is a function of the magnitude of the blockers which are present, it is limited by the attenuation 3 MHz blocker. Depending on the filtering at the output of the mixer, the attenuation of the 3 MHz blocker can relax the intermodulation requirement of the baseband circuits. This is the reason for the first pole at the output of the mixer.

If we expand the 3rd order nonlinearity in (Eq 5-1), we can find the 3rd order intermodulation given by

$$IM_3 = \frac{3}{4} \cdot \frac{a_3}{a_1} \cdot S_1^2 \quad \text{(Eq 5-4)}$$

Two blockers which intermodulate will pass through the 3rd order nonlinearities and create a component in the desired band [26]. The GSM specifications are more aggressive than the DECT standards. An example of two blockers at 900 kHz and 1.7 MHz which can potentially intermodulate to create a component at 100 kHz is illustrated in Figure 5.3. Similar to the variable gain amplifier, we know that to improve the linearity of the filter, we want a_1, the gain of the opamp to be high. In addition, linear poly capacitors and resistors should be used in the filter. Having the amplifier in feedback topology also improves the linearity of the filter [26].

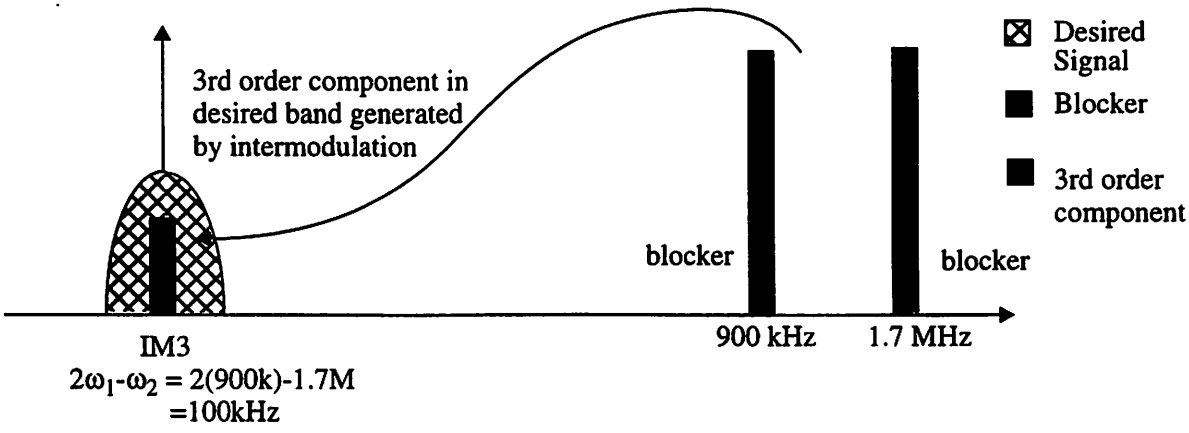


Fig. 5.3: 3rd order intermodulation

5.2 Filter Design

This section explores the different design procedures and strategies in designing a filter. Three different kinds of filter are presented. Based on the tradeoffs among them, one type of filter will be selected for the receiver application. Following this, we discuss the different properties to be considered in the filter. This includes the filter order selection, the magnitude and phase response, the pole and zero placement and the sensitivity of a filter.

5.2.1 Comparison of Filters

There exists many classes of filters. Some examples are switched capacitor filters, LC filters, MOSFET-C filters, G_m/C filters and active-RC filters. Switched capacitor filters are sampled-data filters and are will not be considered for continuous-time anti-aliasing applications. In LC filters, the poles lie only on the $j\omega$ axis. Inductors can suffer from nonlinearities due to saturation or wiring and core losses. In addition, high-Q inductors are difficult to realize on-chip in a standard CMOS process.

A G_m/C filter is illustrated in Figure 5.4 (a). The unity-gain bandwidth of the filter is

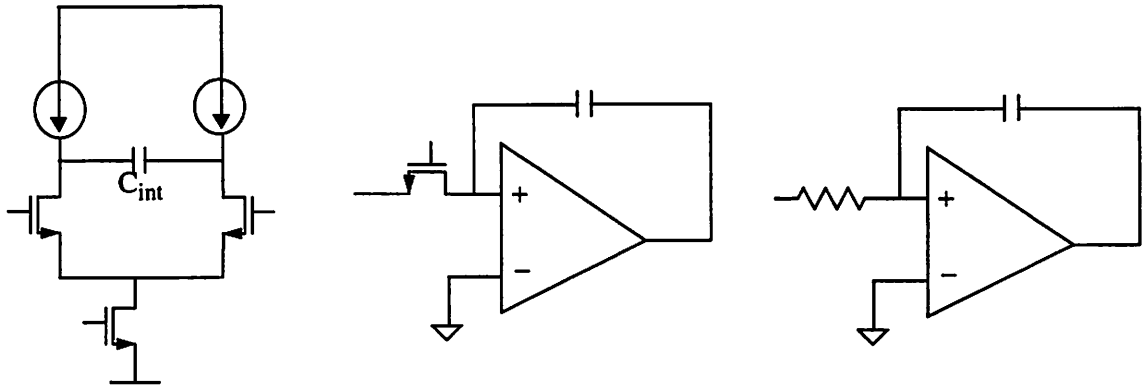


Fig. 5.4: (a) Gm/C Filter (b) Mos-C Filter (c) Active-RC Filter

given by

$$\omega_u = \frac{G_m}{2C_{int}} \qquad \text{(Eq 5-5)}$$

A G_m/C filter eliminates the problem of excess phase from high-frequency non-dominant poles that can cause large errors in the filter response [27]. However, the G_m/C filter is very sensitive to parasitic capacitance that may load down the integrating capacitor. This has the effect of increasing the unity gain bandwidth. In addition, the transconductance for the G_m/C filter is nonlinear, as shown in Figure 5.5.

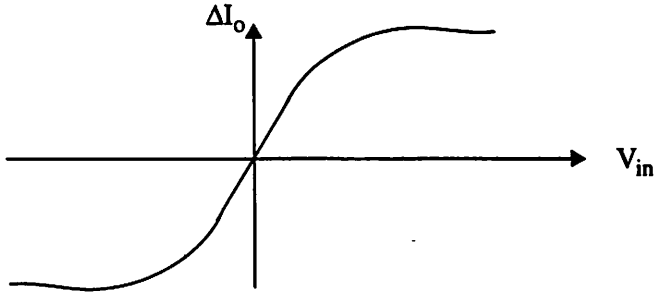


Fig. 5.5: G_m/C Transconductor Nonlinearity.

The active-RC filter in Figure 5.4 (c) by contrast is very linear because only passive poly-poly capacitors and poly resistors are used. The opamp in the active-RC filter can be designed to maximize the performance of the filter. However, the capacitive and resistive elements in the filter suffers from process variations. The absolute value of Rs and Cs typically can vary by 30% and 15% respectively. This can lead to a filter cut-off frequency spread of 2 to 1. In addition, resistors are noisy.

The MOS C filter in Figure 5.4 (b) is similar to the active-RC filter except the resistor is replaced by an active transistor in triode. The MOSFET in triode is not as linear as the passive poly resistors in the active-RC filter.

A summary of the properties of these filters are shown in Table 5.1. The bandwidth of

Filter	Bandwidth	S/(N+D)	Tolerance
Active-RC	10 MHz	90 dB	30-50 %
MOS C	5-10 MHz	50-60 dB	2-5 %
g_m/C	40-50 MHz	40-50 dB	2-5 %

Table 5.1: Performance Comparison

the three filters are wide enough to accommodate the GSM and DECT bandwidths of 100 kHz and 700 kHz respectively. The active filter has the higher signal to noise and distortion ratio. For these reasons, the active-RC filter is determined to be favorable for this application. The filter will be designed so that the worst case process variation meets the attenuation requirements and the lower limit does not cut into the bandwidth of interest.

5.2.2 Filter Order Selection

In Chapter 3, we determined the filter attenuation at the sampling frequency was 90dB for GSM and 70 dB for DECT. From this attenuation, we can find the minimum order for the filter. As an example, the attenuation for GSM would be

$$20 \cdot N \cdot \log\frac{f_s}{f_{BW}} > 90dB \qquad \text{(Eq 5-7)}$$

where f_s=sampling frequency
f_{BW}=signal bandwidth
N=filter order

where f_s=25.6 MHz and the bandwidth is 100 kHz. This gives a minimum filter order of

$$N_{min} = 2 \qquad \text{(Eq 5-8)}$$

A filter order of three was selected because placing a capacitor at the output of the mixer provides a free pole. In addition, the pole is important to attenuate the biggest blocker, the 3 MHz blocker.

5.2.3 Magnitude and Phase Response

An ideal low pass magnitude response is that of the brick wall characteristic. The plot, in Figure 5.6 shows the low-frequency signal components are transmitted, while high-frequency components are blocked. The range of low frequencies which are passed is called the passband or bandwidth of the filter. The range of high frequencies which are stopped is known as the stopband. The value of the highest frequency transmitted is known as the cut-off frequency or ω_c. In practice, the sharp transition bandwidth of the ideal brick wall response is

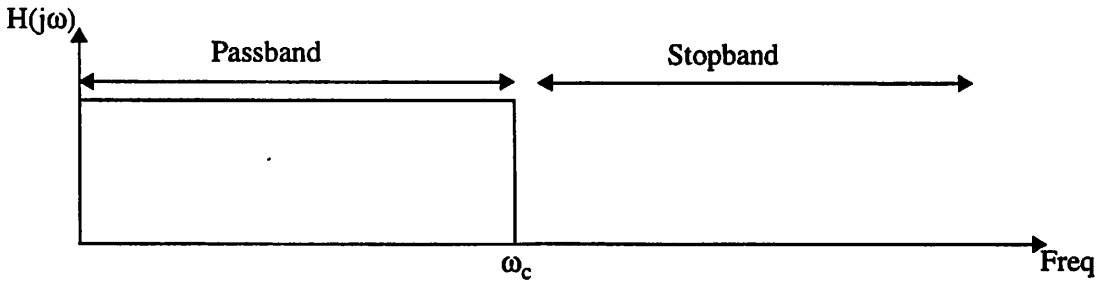


Fig. 5.6: Ideal Magnitude Response

difficult to realize. The response thus, can only be approximated [28].

One approximation is shown in Figure 5.7. This is known as the Butterworth response.

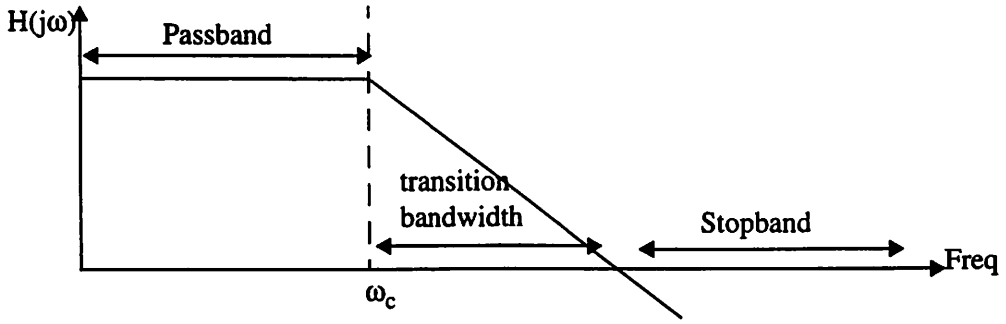


Fig. 5.7: Butterworth Magnitude Response

The Butterworth response is monotonic, i.e the derivative of the magnitude does not change sign over a given range of frequencies. In addition, the passband is maximally flat. All poles

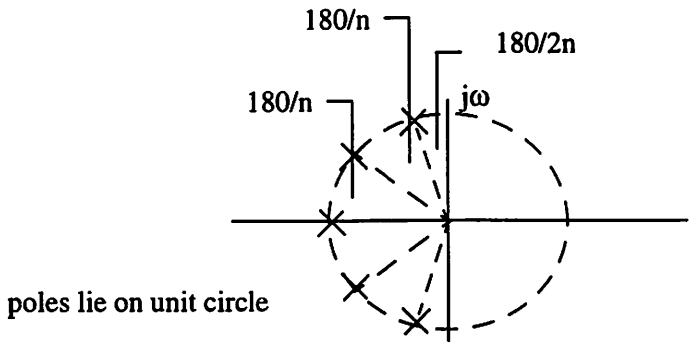


Fig. 5.8: Pole Zero Plot of Butterworth Response

for this response lies on a unit circle while all the zero lies at infinite frequencies. Figure 5.8 is a pole zero plot for a 5th order Butterworth Response. Note that the Butterworth has a very wide transition bandwidth. Because of this, the stopband attenuation is poor for filters of low orders.

A better approximation is the Chebychev Response, shown in Figure 5.9. A characteristic of the magnitude response is ripples in the passband. The stopband attenuation for the Chebychev Response is higher than that of the Butterworth Response for filters of the same order. Because of the ripples, the transition bandwidth of the Chebychev Response is also sharper than that of the Butterworth Response. The pole of the Chebychev Response is on an

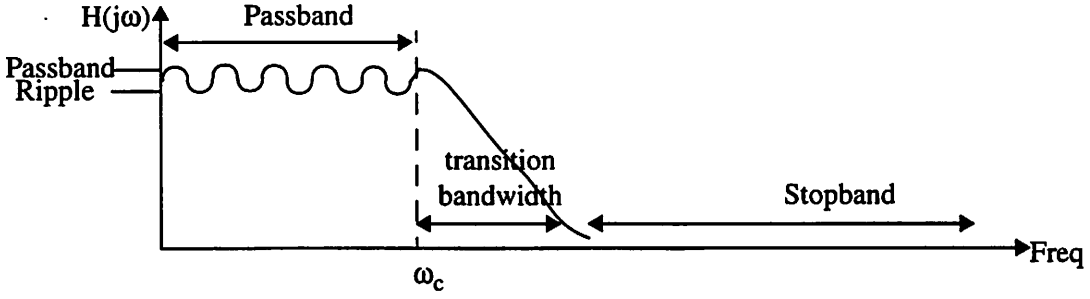


Fig. 5.9: Chebychev Magnitude Response

ellipse and the zeros are all at infinite frequencies. A 5th order Chebychev Response pole zero plot is shown in Figure 5.10.

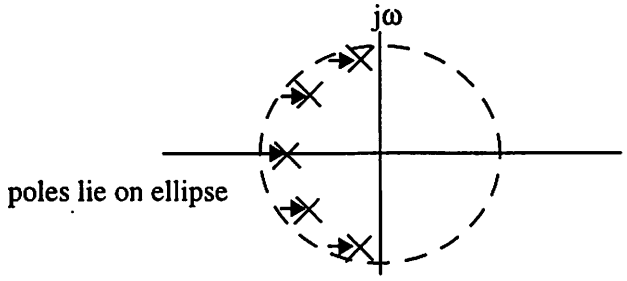


Fig. 5.10: Pole Zero Plot of Chebychev Response

Another approximation that has ripples in both the passband and the stopband is known as the Elliptic Response in Figure 5.11. For the same order filter as the Butterworth and the Chebychev, this response provides the smallest transition bandwidth and the largest stopband attenuation. The poles in the Elliptic Response lie on an ellipse, and the zeros are on

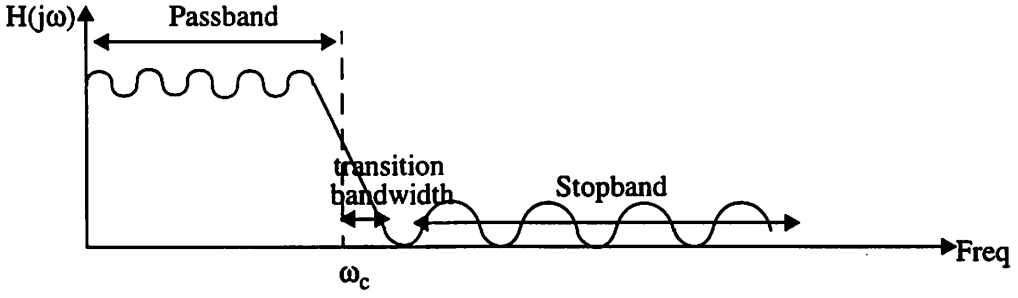


Fig. 5.11: Elliptic Magnitude Response

the imaginary axis, as shown in Figure 5.12. The zeros provide the ripples in the stopband.

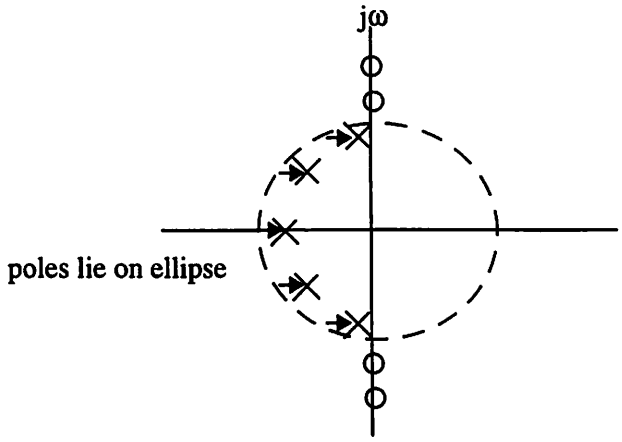


Fig. 5.12: Pole Zero Plot of Elliptic Response

We have previously been discussing the magnitude characteristics of the three types of responses. However, the phase characteristics is also important. In an ideal transmission, we would like the output response signal to have the same information content as the input excitation signal. This means that in an ideal filter response, the phase should be linearly proportional to frequency.

The Butterworth, Chebychev and Elliptic Responses all have phase characteristics that deviate from the ideal. The Butterworth has the most linear phase among the three, followed by the Chebychev, and the Elliptic Response.

The characteristics of the three responses is summarized in Table 5.2. The Elliptic

	Butterworth	Chebychev	Elliptic
Pole Location	on unit circle	on ellipse	on ellipse
Magnitude Response	maximally flat	ripples in passband	ripples in passband ripples in stopband
Phase Response	linear	less linear	poor
Filter Order for Same Stopband Attenuation	high	medium	low

Table 5.2: Comparison of Filter Response

provides the sharpest cutoff between the passband and stopband for a given order. However,

the Butterworth provides the most linear phase. The Chebychev appears to be a good compromise between the three responses. It provides better stopband attenuation than the Butterworth, and the phase response is not as poor as the Elliptic. For these reasons, the Chebychev Response is selected.

5.2.4 Poles Selection

Now that the stopband attenuation, filter order and response have been selected, the poles for the filter can be defined. There are two ways to accomplish this. The first is to refer to design tables for filter function approximations that provides values of the coefficients for functions [29]. The second is to use a software program like Matlab that calculates the coefficients based on the values entered for the stopband attenuation, filter order and type of response.

The nominal poles for the filter are summarized in Table 5.3. Because it is a 3rd order filter, there are two complex poles and one real pole. The zeros are at infinite frequencies. The real pole will be implemented at the output of the mixer while the two complex poles will be implemented with a Sallen-Key filter described in the next section.

The poles were selected with the resistor and capacitor process variation in mind. The

Nominal Poles (Mrad/s)	GSM	DECT
p1	-1.08	-3.73
p2	-0.53 + 2.12j	-1.86 + 7.28j
p3	-0.53 - 2.12j	-1.86 - 7.28j

Table 5.3: Poles Selection

higher limit of the variation will provide enough attenuation, particularly the 3 MHz blocker for GSM, and the lower limit will not cut into the bandwidths of interest.

5.3 Sallen-Key Design

Sallen and Key introduced a number of active filters in 1954. Many are still being used today. The Sallen-Key filter is popular because of it is easy to analyze and design [30]. The low-pass Sallen-Key filter is shown in Figure 5.13.

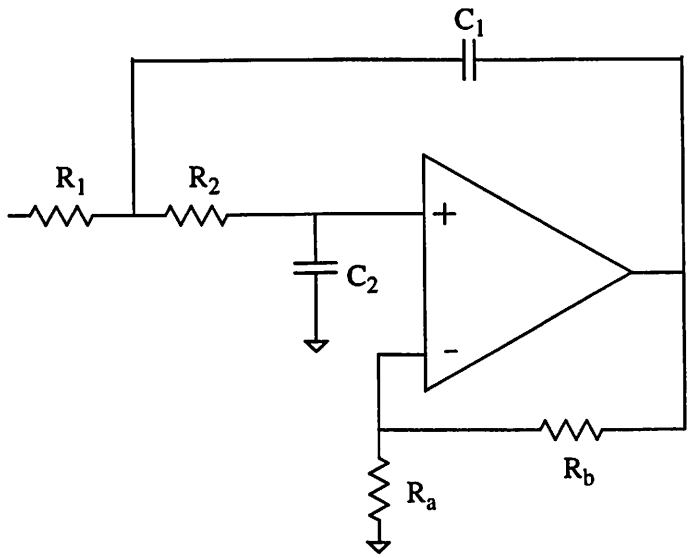


Fig. 5.13: Sallen-Key Filter

The general form of the transfer function can be written as

$$H(s) = \frac{G \cdot \omega_o^2}{s^2 + \left(\frac{\omega_o}{Q}\right)^2 + \omega_o^2} \qquad \text{(Eq 5-8)}$$

where G is the DC gain, ω_o is the undamped natural frequency, and Q is the quality factor. The quality factor Q is the relative sharpness at which the peak of the magnitude response occurs. By analyzing the Sallen-Key circuit, we can find G, ω_o and Q in terms of the element values. These are given by [30][25]

$$\omega_o = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \qquad \text{(Eq 5-9)}$$

$$Q = \frac{\omega_o}{\frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1-G}{R_2 C_2}} \qquad \text{(Eq 5-10)}$$

$$G = 1 + \frac{R_b}{R_a} \qquad \text{(Eq 5-11)}$$

5.3.1 Sensitivity

One of the challenges of designing a filter is the evaluation of a design, in comparison with other possible realizations which meet the same specifications. Sensitivity is a useful tool of comparison. Sensitivity is the measure of the change in a performance characteristic when there is a change in the nominal value of one or more elements [30][25]. A design which is attractive from a theoretical standpoint but has high sensitivities may be useless in practice.

The symbol S is used to denote sensitivity. The characteristic that is being evaluated is denoted by the superscript character while the element that is changed is denoted by the subscript character. For example, if y is the performance characteristic and x is the element, the sensitivity is defined by

$$S_x^y = \frac{\delta y}{\delta x} \cdot \frac{x}{y} = \frac{\delta y / y}{\delta x / x} \qquad \text{(Eq 5-12)}$$

The sensitivity of the Sallen-Key filter depends on the choice of the element values in the circuit. Three kinds of designs are evaluated in the next sections, and their sensitivities will be compared.

In the first design, all the capacitances are set to the same value and all the resistances are set to the same value, as given below

$$C_1 = C_2 = C \qquad \text{(Eq 5-13)}$$

$$R_1 = R_2 = R \qquad \text{(Eq 5-14)}$$

This design is easiest to implement, and because the elements are set to the same values, good matching is achievable. By inserting (Eq 5-13) and (Eq 5-14) into (Eq 5-9), (Eq 5-10) and (Eq 5-11), we compute the following:

$$RC = \frac{1}{\omega_o} \qquad \text{(Eq 5-15)}$$

$$G = 3 - \frac{1}{Q} \qquad \text{(Eq 5-16)}$$

The second design has equal capacitance values, and the feedback resistors are set to the same value. The feedback resistors are thus easy to match and the gain is fixed at two. This is shown by

$$C_1 = C_2 = C \qquad \text{(Eq 5-17)}$$

$$R_a = R_b = R \qquad \text{(Eq 5-18)}$$

With some computation, we find that the following conditions must be true.

$$R_1 = \frac{Q}{\omega_o C} \qquad \text{(Eq 5-19)}$$

$$R_2 = \frac{1}{R_1 \omega_o^2 C^2} \qquad \text{(Eq 5-20)}$$

The final design to be considered is when the gain is set to be 1. The opamp is now reduced to a voltage follower. The gain is now insensitive, and there is no noise contribution

from the feedback resistors which have been set to 0. Again, the equations below must hold true:

$$C_1 > C_2 \cdot (4Q^2) \qquad \text{(Eq 5-21)}$$

By using the element values from the three designs above, we find that their sensitivities differ. As shown in Table 5.4, Design 1 is the simplest to implement but it has the

	Design 1	Design 2	Design 3
G	3-1/Q	2	1
$S_{R_1}^{Q}$	-1/2 + Q	-1/2 + Q	0
$S_{R_2}^{Q}$	1/2 - Q	1/2 - Q	0
$S_{C_1}^{Q}$	-1/2 + 2Q	1/2 + Q	1/2
$S_{C_2}^{Q}$	1/2 - 2Q	-1/2 - Q	-1/2
$S_{R_a}^{Q}$	1 - 2Q	-1	0
$S_{R_b}^{Q}$	2Q - 1	1	0

Table 5.4: Sensitivity Comparison

	Design 1	Design 2	Design 3
$S^{G}_{R_a}$	$-\frac{2Q-1}{3Q-1}$	-1/2	0

Table 5.4: Sensitivity Comparison

highest sensitivities. Design 2 is not as sensitive as Design 1, but this is at the expense of a wide resistance spread between R_1 and R_2. Design 3 is the least sensitive but this is at the expense of a great capacitor spread between C_1 and C_2. For minimum sensitivity reasons, Design 3, the unity-gain configuration was selected.

5.3.2 Element Value Selection

This section will describe the tradeoffs in selecting resistance and capacitance values for the unity-gain Sallen-Key filter. Because the resistors R_1 and R_2 in the filter will generate noise, according to

$$V_R^2 = 4kTR \cdot \Delta f \qquad \text{(Eq 5-22)}$$

we would like to minimize the resistance. However, for the same cut-off frequency, if we decrease the resistance the capacitances C_1 and C_2 will increase.

There are a number of disadvantages in increasing the capacitances. First, the area will increase. Second, the capacitance C_1 will load down the amplifier. This increases the slew rate of the amplifier, and the increased current to drive the capacitor will increase the power dissipation. More importantly, a large value of C_1 will create a left-half-plane zero in the transfer function which will reduce the attenuation of the filter. The resistance and capacitance values must be chosen to optimize the noise and power dissipation, while preserving the functions of the filter.

Another factor to consider is that the filter will be programmable for the GSM and DECT standards. Because both these standards have differing bandwidths, the element values must be changed. The same resistors can be used while the capacitor values are changed, or vice versa.

We first design for the GSM standard because the noise specification is more stringent. For the DECT standard, the element values can be decreased because the cut-off frequency is higher. As shown in Figure 5.14, C_{1d} and C_{2d} are the capacitances for DECT. The

	GSM	DECT
R_1 kΩ	12	12
R_2 kΩ	12	12
C_1 pF	44.7	44.7
C_{1d} pF	108	N/A
C_2 pF	2.75	2.75
C_{2d} pF	6.65	N/A
f_c	350 kHz	1.2 MHz

Table 5.5: Sallen-Key Element Values

capacitances for GSM are (C_1+C_{1d}) and (C_2+C_{2d}). The additional capacitors C_{1d} and C_{2d} are turned on with a GSM switch.

A CMOS switch is used to turn on C_1 because the output common mode of 1.8 V is close to the middle of the supply. An NMOS switch is used to turn on C_2 because the switch is connected to ground. For more detailed analysis of switches, please refer to Chapter 4, Section 4.2.1.

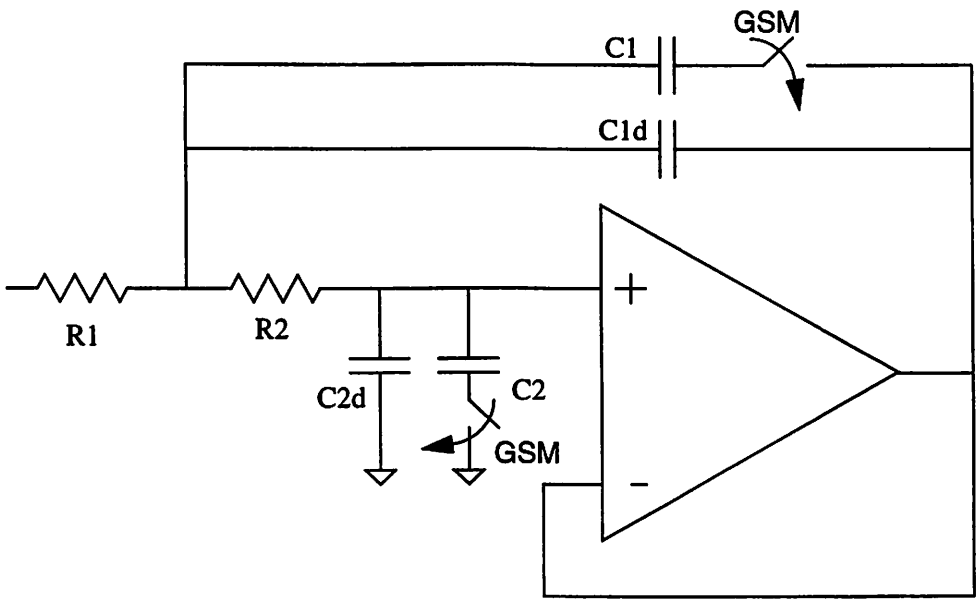


Fig. 5.14: Programmable Sallen-Key Filter

5.3.3 Operational Transconductance Amplifier Design

The operational transconductance amplifier (OTA) used in the Sallen-Key filter is similar to the one used in the variable gain amplifier. The only difference is this OTA is single-ended. Because the Sallen-Key filter has a single-ended output, using a single-ended amplifier instead of a differential amplifier helps to save power. The differential to single ended conversion is achieved by tying the gate of the load devices to one output of the first stage, as shown in Figure 5.15.

The choice of the device sizes is the same as the VGA opamp. The load devices have much larger Vdsats than the input devices to reduce thermal noise. The load devices are also much longer than the input devices to reduce flicker noise. The input devices are PMOS devices and are made large to reduce flicker noise. The cascode devices have minimum channel lengths and small Vdsats. In addition, a margin of 200 mV is left on all devices to ensure that they are in saturation mode.

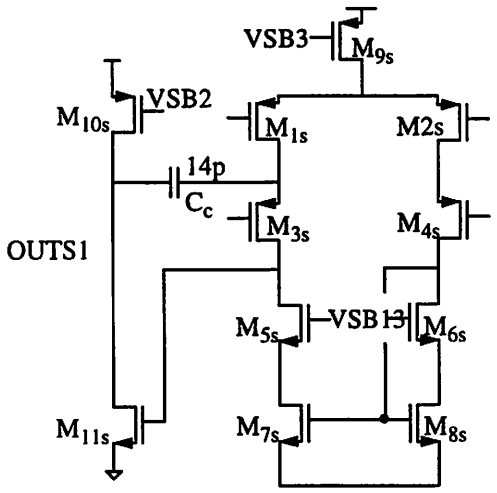


Fig. 5.15: OTA for Sallen-Key

Cascode compensation is used to maintain stability in this opamp because it is faster than the regular Miller compensation. For a more complete description on this form of compensation, please refer to Chapter 4, Section 4.3.4.

One very important consideration for this opamp is the input swing. Because the opamp is used in the unity-gain configuration, one of the inputs is connected directly to the output. Both inputs must therefore be able to swing the required swing specification of 700 mV.

A summary of the V_D^{sat}s of the devices and their lengths are presented in Table 5.6.

Devices	V_D^{sat}	Length
M_{1s}, M_{2s}	300 mV	1.5 µ
M_{3s}, M_{4s}	100 mV	0.35 µ
M_{5s}, M_{6s}	200 mV	0.35 µ
M_{7s}, M_{8s}	700 mV	8 µ
M_{9s}	110 mV	0.7 µ
M_{10s}	450 mV	0.7 µ

Table 5.6: Summary of Device Vdsats

Devices	V_D^{sat}	Length
M_{11s}	800 mV	0.35 μ

Table 5.6: Summary of Device Vdsats

5.3.4 Slew Rate

When an input step is applied at the input of an amplifier, the rate that the output tracks the input is known as slew rate. Slew rate is an important consideration when designing an opamp. The slew rate is especially important for the Sallen-Key filter because the opamp may see large adjacent blockers next to a weak desired signal. In addition, the capacitor C_1 is large and will load down the output of the opamp. Any errors from amplifier slew rate will create harmonic distortion and degrade the performance of the Sallen-Key filter.

Previously, in Section 3.3.3, we defined the slew rate requirement for each of the blocker in the GSM blocking profile. The highest slew rate requirement is defined by the 600 kHz blocker. We also defined the slew rate equation as

$$SR = \frac{2I_{SR}}{C} \qquad \text{(Eq 5-23)}$$

where I_{SR} is the current in the opamp, and C is the capacitor that is driven by the opamp. In the first stage of the opamp, the capacitance that must be driven by the opamp is approximately equal to the compensation capacitor. In the second stage of the opamp, the opamp must drive the compensation capacitor and the feedback capacitor C_1. From these slew rate requirements, we calculate the minimum current in each leg of the opamp.

For the first stage of the opamp that drives a compensation capacitor of 15 pF, the minimum current required is 20μA. The second stage of the opamp drives the compensation capacitor and the feedback capacitor of 152.7 pF, and the minimum current required is 225μA.

5.3.5 Stability

The Sallen-Key filter has two feedback loops. The first loop is the unity-gain feedback that is a negative feedback loop. The second loop is the global feedback loop. To ensure stability, both loops must be stable or the negative feedback loop must dominate.

To ensure stability of the unity-gain bandwidth loop, the Sallen-Key filter is simulated

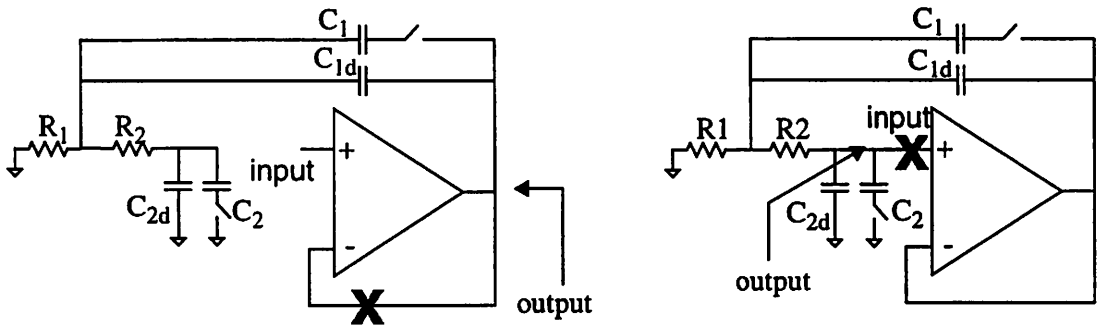


Fig. 5.16: (a) Unity Gain Feedback Stability (b) Global Feedback Stability

using configuration (a) of Figure 5.16. The loop is broken at "X" and the loop gain evaluated. For the global feedback stability simulation as shown in configuration (b) of Figure 5.16, the loop is broken at "X" and the parasitic gate-source capacitance of the opamp is added to the capacitors C_2 or C_{2d} before the loop gain is again evaluated.

5.3.6 Simulation Results

The magnitude response of the Sallen-Key filter for the GSM standard is presented in Figure 5.17. The shaded area denotes the key required attenuation at the sampling frequency and at the frequency of the blockers. Because of process variation, the cut-off bandwidth varies from 250-870 kHz. The filter is designed so that the high limit still meets the attenuation requirements, and the lower limit does not cut into the bandwidth of interest.

The magnitude response of the DECT standard is shown in Figure 5.18. Again, the shaded area is the key required attenuation at the sampling frequency for DECT and at the

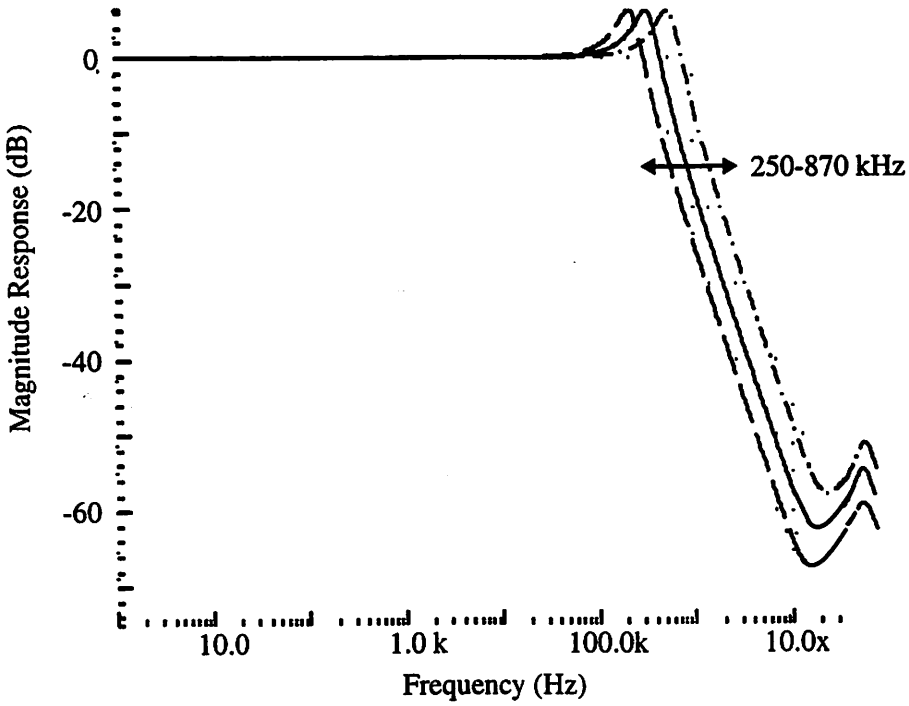


Fig. 5.17: GSM Magnitude Response

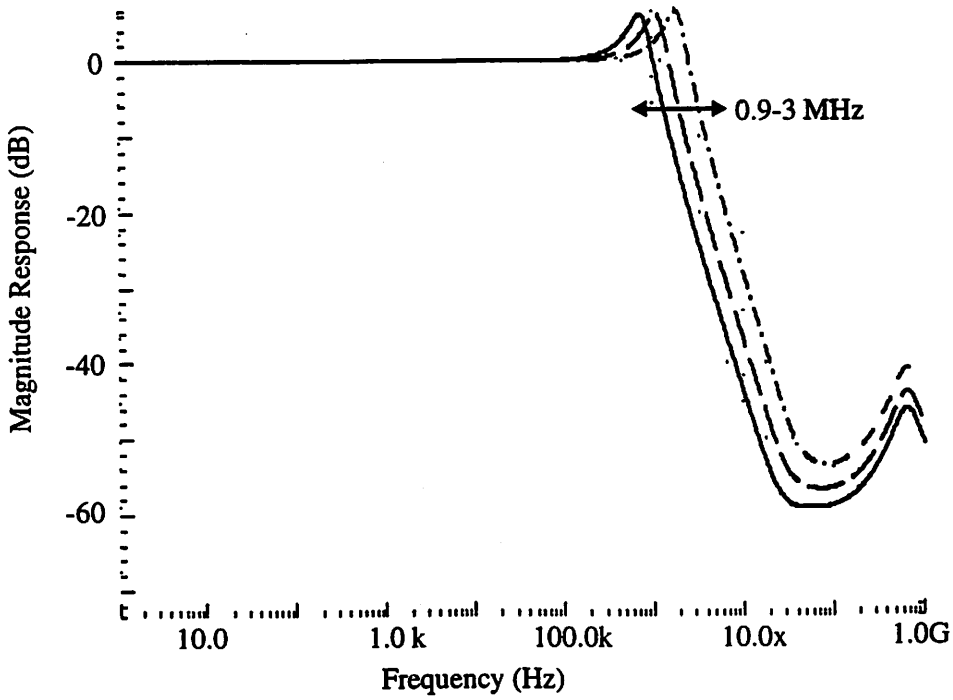


Fig. 5.18: DECT Magnitude Response

frequencies of the blockers. Note that the blocking requirements are more easily met in this standard. The cut-off frequency varies from 0.9-3 MHz. As explained in earlier sections, switching between standards is accomplished by just switching to different capacitors C_1 and C_2.

From Figure 5.17 and Figure 5.18, we see that the magnitude response peaks almost 6 dB. This is due to the high Q factor of the filter. The parameter Q is a measure of the distance of the poles from the $j\omega$ axis. Therefore, the higher the Q, the more selective the filter response becomes. However, a disadvantage of a high-Q response is the additional noise caused by the peaking. The filter response was designed so that the peaking occurs outside the bandwidth of interest, and thus does not contribute additional in-band noise.

During the slow process, both the GSM and DECT magnitude responses show in-band peaking. It can be argued that because of the GMSK and GFSK modulation schemes for GSM and DECT, the signal band edge is actually less than 100 kHz and 700 kHz respectively and any peaking close to the bandwidth is thus tolerated [8][31]. There are also ways to mitigate any phase, magnitude or group delay errors resulting from in-band peaking, such as using a digital adaptive equalizer after the sigma-delta modulator.

At higher frequencies, the output impedance of the Sallen-Key filter begins to increase from its ideal value and a feedforward path is created from capacitor C_1 in the Sallen-Key circuit. The magnitude response starts to exhibit a zero that reduces the attenuation of the filter. A number of strategies may be employed to mitigate the effect of the feedforward zero. These include using a source follower to cancel the feedforward path, using a very high unity-gain bandwidth opamp, or using an RC circuit after the Sallen-Key filter to cancel the zero. However, because the filter still meets the attenuation requirements inspite of the zero, none of the procedures were needed.

Noise analysis was performed on the Sallen-Key circuit using SPICE. The input-referred noise for GSM and DECT is presented in Table 5.7.

	GSM	DECT
Total Input Referred Noise	11.2 μV-rms	43.1 μV-rms

Table 5.7: Input Referred Noise for GSM and DECT

The in-band noise breakdown of the Sallen-Key filter for GSM is presented in Figure 5.19. The dominant source of noise is from the resistors in the filter, R_1 and R_2. Note that there are four of these resistors, which contribute significant thermal noise that total 85%. If the resistors are decreased to lower the noise contribution, the feedback capacitors C_1 will have to be increased to maintain the same cut-off frequency. Recall that a large value of C_1 will create a left-half plane zero that reduces the attenuation of the filter.

The in-band noise breakdown for DECT is presented in Figure 5.20. The opamp flicker noise is now a smaller percentage of the total noise. This is because the bandwidth for DECT is much larger than GSM, and flicker noise is not dominant at higher frequencies. Note that the same noise percentages hold for the opamp thermal noise, resistor R_1 and resistor R_2. This is because thermal noise is white and the noise spectral density is independent of frequency.

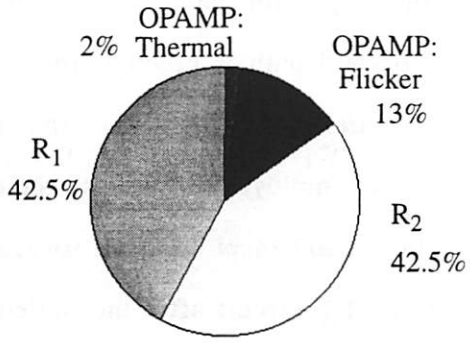


Fig. 5.19: Noise Breakdown of Sallen-Key filter for GSM

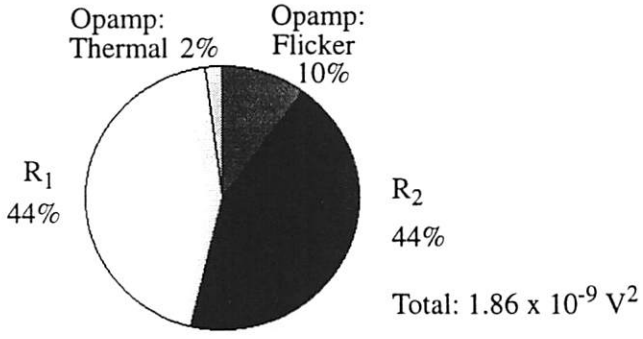


Fig. 5.20: Noise Breakdown of Sallen-Key Filter for DECT

The dynamic range of the Sallen-Key filter, is calculated using the equation below

$$DR_{in} = \frac{P_{signal,in}}{P_{noise,in}} = \begin{cases} 91.6\text{dB} & \text{GSM} \\ 80\text{dB} & \text{DECT} \end{cases} \qquad \text{(Eq 5-24)}$$

$$\text{where} \quad P_{signal,in} = \frac{\hat{V}_{in}^2}{2} = \frac{(600\text{mV})^2}{2} = (0.18)$$

The input-referred noise power, $P_{noise,in}$ is given in Table 5.7. The dynamic range is 91.6 dB for GSM and 80 dB for DECT.

5.4 Summary

This chapter presented the design and simulations results of the Sallen-Key filter. The discussion began with a review of important system-level specifications such as anti-aliasing requirements, linearity requirements and programmability. Given these specifications, a number of filters were compared. The active-RC filter was found to be the filter of choice and a Sallen-Key filter was selected to implement the requirements. The Sallen-Key filter was designed with unity-gain for minimum sensitivity. The design of the filter followed, along with

a detailed analysis of the order, magnitude response, phase response and pole location of the filter. The amplifier topology that was similar to that used in the variable gain amplifier was used in the Sallen-Key filter. Finally, simulation results were presented.

Chapter 6

Buffer Design

6.1 Introduction

This chapter will first review the motivations for having the buffer prior to the sampling network in the ADC. Design issues and tradeoffs will be investigated. This is followed by a brief discussion of optimization techniques for the buffer design. The tradeoffs in the amplifier used in the buffer will be discussed. Simulation results will be presented.

6.2 Motivations for a Buffer

The baseband filter drives the sampling network of the sigma-delta modulator. The ADC is sampling at 44.8 MHz for DECT and 25.6 MHz for GSM. As can be seen from Figure 6.1(a), when the switch is closed during Φ_1, the modulator is sampling. Similarly, during Φ_2, the switch is open and the modulator is holding its previous sampling value. Now assume an input signal that is a sine wave, as shown in Figure 6.1(b). During Φ_2, the modulator is holding its previous value. During Φ_1, the filter-ADC interface must charge up to the magnitude of the sinusoid before the start of the next clock phase of Φ_2. This means that the last stage of the baseband filter must settle to the same accuracy as the sigma-delta modulator.

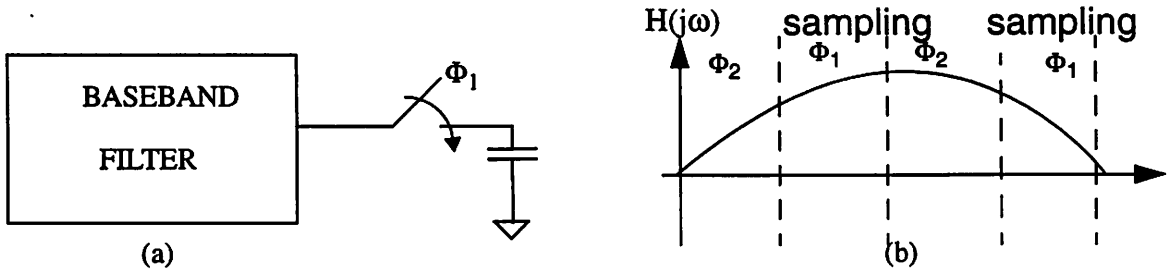


Fig. 6.1: (a)Baseband Filter-ADC Interface (b)Sinusoidal Input Signal

There are certain advantages in using a buffer to drive the sigma-delta modulator, as shown in Figure 6.2. Firstly, the buffer helps by preventing any perturbation from the sampling network from reaching the input of the Sallen-Key filter. Any large perturbation may lead to distortion in the filter. In addition, it is easier to design the buffer to settle to the ADC sampling accuracy because the buffer just drives the sampling capacitor of 5pF. In contrast, without the buffer, the Sallen-Key has to fulfill the settling requirements while driving the feedback capacitors, C_1, C_{1d} and the sampling capacitor C_s. The buffer also isolates the Sallen-Key filter from the nonlinearities of the sampling network during slewing.

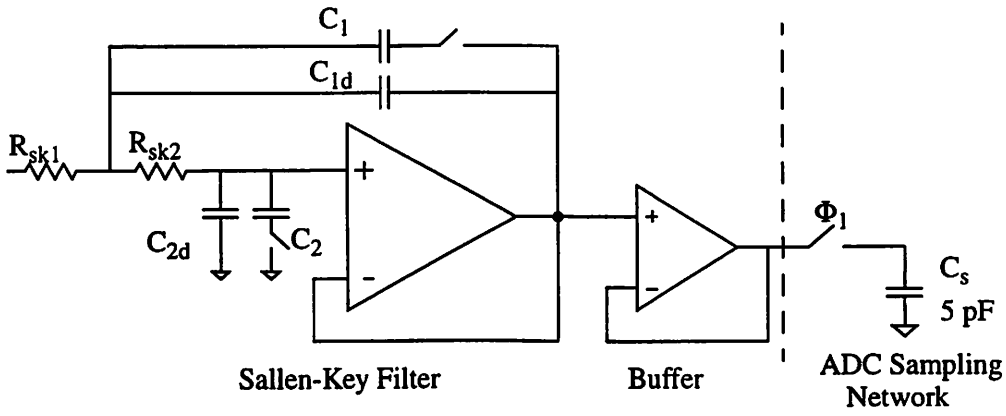


Fig. 6.2: Buffer drives Sigma-Delta Modulator

6.3 Buffer Comparison

Two types of buffers were compared, and they are shown in Figure 6.3 (a) and (b). In case (a), the gain is implemented with resistors R_2 and R_1 of equal size. In case (b), the opamp has a unity-gain feedback loop.

The fully-differential resistive buffer has good power supply rejection ratio. The

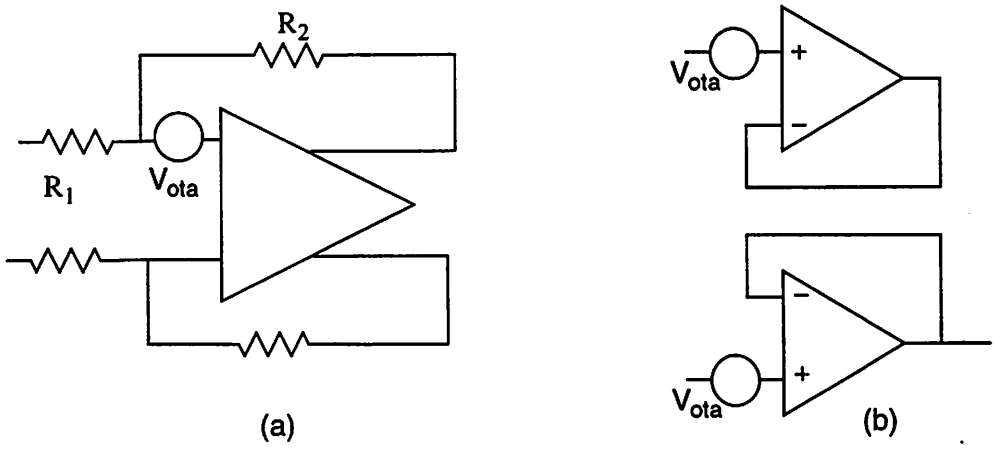


Fig. 6.3: (a)Resistive Fully-Differential Buffer (b)Quasi-Differential Buffer

disadvantage of this buffer is the thermal noise from the resistors. In addition, the noise from the opamp when referred to the input of the buffer is multiplied by a factor of four, as given by (Eq 6-1).

$$\overline{V_{in}^2} = 4kTR_1\left(1+\frac{R_1}{R_2}\right)\Delta f + \frac{\overline{V_{OTA}^2}}{\left(\frac{R_2}{R_1+R_2}\right)^2}\Delta f$$

$$= 4kTR_1(2)\Delta f + \overline{V_{OTA}^2}\cdot 4\Delta f \qquad \text{(Eq 6-1)}$$

The quasi-differential buffer in (b) does not have any noise contributing resistors. The input referred noise is the noise from the opamp, as given by

$$V_{in}^2 = 2V_{OTA}^2 \cdot \Delta f \qquad \text{(Eq 6-2)}$$

Compared to the buffer in (a), this buffer contributes less noise. However, this quasi-differential buffer dissipates more power because there are two opamps.

The buffer in (b) was selected to drive the sigma-delta modulator because the stringent noise specifications for GSM have to be met. While power dissipation should be minimized, there is no specific power dissipation requirement.

6.4 Operational Amplifier

The operational amplifier used in the buffer must be designed to optimize the performance of the buffer. The opamp should have a wide bandwidth so that the signal can settle to the desired accuracy within half a clock period. The higher the number of stages in the opamp, the smaller the bandwidth. This is because the opamp will need to be compensated and this will decrease the bandwidth.

In previous sections, specifically Section 5.1.1, we discussed that a high-gain opamp was needed for better linearity. In this design, having the opamp in unity feedback topology greatly improves the linearity performance of the amplifier. In addition, the linearity requirements of the buffer stage are reduced because most of the large adjacent blockers have been filtered out by the first pole at the input of the VGA and the 2nd-order Sallen-Key filter.

From [26], the 3rd order input intercept point (IIP_3) equation is

$$IIP_3 = \sqrt{\frac{3}{4} \cdot \left|\frac{b_1}{b_3}\right|} \qquad \text{(Eq 6-3)}$$

where $$b_1 = \frac{g_m \cdot R_o}{1 + g_m \cdot R_o}$$

$$b_3 = \frac{-\frac{1}{8} \cdot \frac{g_m}{(V_d^{sat})^2}}{(1 + g_m \cdot R_o)^4}$$

The IIP3 for the buffer alone is approximately 22 V, calculated using the method described in [12]. Reorganizing the terms in (Eq 6-3) and assuming a constant V_d^{sat} of 0.35 V, we get

$$(1 + g_m \cdot R_o)^3 > \left((22)^2 \cdot \frac{3}{32} \cdot \frac{1}{(0.35)^2}\right)$$

$$(g_m \cdot R_o) > 10 \qquad \text{(Eq 6-4)}$$

Based on the DC gain requirements, a simple differential pair was selected for this design, as shown in Figure 6.4.

The unity gain was accomplished with a diode connection at M_2. The inputs of the opamp were selected to be NMOS for speed reasons. NMOS devices are faster than PMOS devices because the mobilities of electrons are greater than that of holes.

The unity-gain bandwidth of the opamp is given as

$$\omega_{u,T} = \frac{1}{\tau}$$

$$= 2f_s \cdot n_\tau \qquad \text{(Eq 6-5)}$$

where f_s is the sampling frequency of the sigma-delta modulator, and n_τ is the required number of time constants. The required number of time constants is determined from the resolution of the modulator.

The unity-gain bandwidth requirement of the opamp determines the minimum current

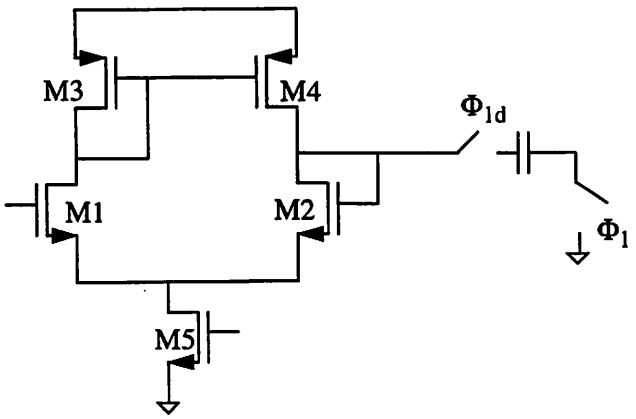


Fig. 6.4: Buffer

we need in the opamp, as given by

$$\omega_{u,T} = \frac{G_{m1}}{C_L} = \frac{\sqrt{2I_{DS}\mu C_{ox}\frac{W}{L}}}{C_L} \qquad \text{(Eq 6-6)}$$

G_{m1} is the transconductance of the amplifier and C_L is the load capacitance. The transconductance of the amplifier is proportional to the square root of the current.

6.5 Thermal Noise

The input referred thermal noise of the amplifier in Figure 6.4 is given by

$$\overline{V_{in}^2} = 2\left\{4kT \cdot \frac{2}{3} \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{g_{m3}}{g_{m1}}\right)\Delta f\right\} \qquad \text{(Eq 6-7)}$$

Because the buffer drives a sampled data network, the total noise power is evaluated by integrating the noise spectrum to infinity [25]. This is because of the noise folding phenomena where all the noise at high frequencies is folded back into the bandwidth of interest after sampling. This is illustrated in Figure 6.5, where it can be observed that the thermal noise power rolls off at the bandwidth of the sampling network. The paramater Δf in (Eq 6-7) should therefore be the bandwidth of the sampling network.

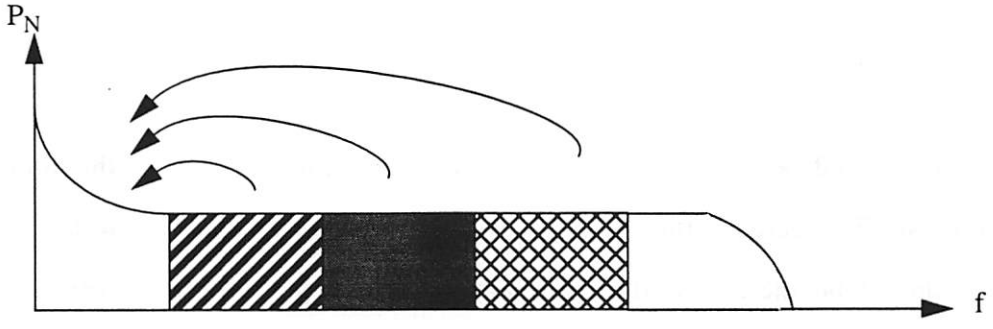


Fig. 6.5: Noise Folding in Buffer

Recall from Chapter 3, Section 3.4 that the sigma-delta modulator will be oversampled by an oversampling ratio, M. The oversampling ratio is 128 for GSM and 32 for DECT. The total in-band thermal noise should therefore be divided by the oversampling ratio. A more accurate equation for the opamp thermal noise is then

$$\overline{V_{in}^2} = \frac{2\left\{4kT \cdot \frac{2}{3} \cdot \frac{1}{g_{m1}} \cdot \left(1 + \frac{g_{m3}}{g_{m1}}\right)\Delta f\right\}}{M} \qquad \text{(Eq 6-8)}$$

6.6 Flicker Noise

Flicker noise is caused by the charging and discharging of oxide traps near the Si-SiO_2 interface. The oxide trapping time constant is inversely proportional to frequency and because of this, flicker noise is sometimes known as 1/f noise. PMOS devices have a slower oxide trapping time constant compared to NMOS devices and thus contribute flicker noise that is three times lower. The flicker noise equation for the buffer is shown as

$$P_{flicker} = 2 \cdot \left[\frac{K_{fp}}{W_1 \cdot L_1 \cdot C_{ox}} \left(1 + \frac{K_{fn} \cdot L_1^2 \cdot \mu_n}{K_{fp} \cdot L_3^2 \cdot \mu_p} \right) \Delta f \right] \qquad \text{(Eq 6-9)}$$

For speed reasons, the buffer has NMOS input devices and is the dominant source of flicker noise. To decrease the flicker noise, the gate area, i.e. the width and length of the devices should be increased. However, increasing the input device sizes also increases the input parasitic capacitances. This will degrade the settling performance of the buffer. Therefore, the devices sizes are optimized for speed and flicker noise.

6.7 Simulation Results

The dynamic settling response of the buffer across process is presented for GSM and DECT in Table 6.1. Recall that the settling requirements is 15 ns for GSM and 7 ns for DECT.

	Typical	Fast	Slow
GSM	8.2 ns	10.1 ns	11.5 ns
DECT	5.8 ns	4.9 ns	6.5 ns

Table 6.1: Settling time for GSM and DECT

The DC gain across process was also simulated and is shown in Table 6.2. The DC gain varies from 78 to 97 V/V. Because the static error is inversely proportional to the DC gain,

	Slow	Typical	Fast
DC Gain	78 (V/V)	85 (V/V)	97 (V/V)

Table 6.2: DC Gain across process

the static error varies by approximately 2.5 mV across process.

SPICE was used to perform noise analysis for the buffer. The input-referred noise breakdown for GSM and DECT is presented in Table 6.3. For the GSM standard, flicker noise

	Thermal Noise	Flicker Noise	Total Input-Referred Noise
GSM	3.3 μV-rms	6.3 μV-rms	7.12 μV-rms
DECT	17.2 μV-rms	7.3 μV-rms	18.7 μV-rms

Table 6.3: Input Referred Noise for GSM and DECT

is almost 78% of the total noise. Flicker noise dominates because NMOS input devices were used. The input devices sizes cannot be made too large to reduce flicker noise because the input capacitance will load down the buffer. For the DECT standard, flicker noise is only 15 % of the total noise. This is due to the fact that flicker noise not dominant at higher frequencies.

6.8 Summary

The design of the buffer is presented in this chapter. The buffer is the final block of the baseband filter. The chapter began with a discussion of the motivations for having a buffer drive the sampling network of the sigma-delta modulator. A buffer is important to prevent any perturbation from the sampling network from reaching the input of the Sallen-Key. In addition, it is easier for the buffer to settle to the ADC sampling accuracy because the buffer just drives

a 5pF sampling capacitor. The opamp in the buffer is a simple differential pair because the fewer the number of stages in the opamp, the wider the bandwidth. The unity-gain bandwidth of the buffer determines the current in the opamp, and the power dissipation of the buffer. This chapter concludes with simulation results.

Chapter 7

Conclusions and Future Work

7.1 Introduction

This chapter summarizes the results of the baseband filter and provides recommendations for future work. The baseband filter explores two research goals. The first involves the issues of integration in an RF receiver. Integration in receivers can help reduce the cost, power dissipation and form factor. The second goal is the issue of programmability. Programmability allows an RF receiver to adapt to multiple RF standards.

7.2 Baseband Filter

The baseband filter is the first stage in the baseband of an RF receiver, between the mixer and the sigma-delta modulator. The continuous-time baseband filter has several functions. It attenuates large adjacent blockers, performs anti-aliasing, accommodates for gain variation in the RF front-end and reduces noise requirements of subsequent stages.

A complete circuit diagram of the baseband filter is illustrated in Figure 7.1. The first pole at the output of the mixer attenuates the biggest blocker for GSM, at 3 MHz. Following that, a fully-differential variable gain amplifier gains up the signal. The nominal gain is 12 dB,

maximum gain is 18 dB and minimum gain is 6 dB. The gain changes in discrete steps of 3 dB.

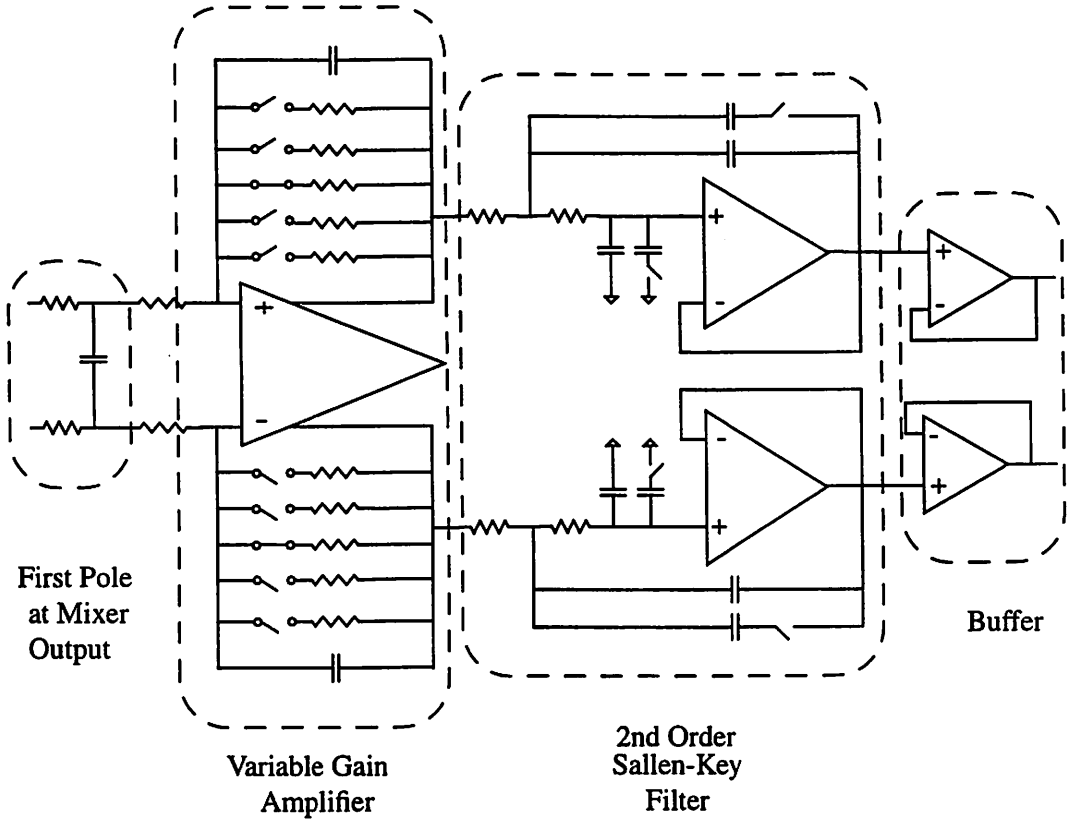


Fig. 7.1: Baseband Filter Circuit Diagram

After the variable gain amplifier, two 2nd order Sallen-Key filters provide more filtering and anti-aliasing. The last stage of the baseband filter is a buffer that drives the sampling network of the sigma-delta modulator.

7.2.1 Noise and Power Dissipation Tradeoffs

This section discusses the noise breakdown and the power dissipation breakdown in each block of the baseband filter. From Figure 7.1, we can see that the two Sallen-Key filters have four input resistors of 12kΩ each which will contribute significant thermal noise. Also, recall from Section 6.7 that the two buffers have large flicker noise contributions from their NMOS inputs. Therefore, a large percentage of the noise specification was allocated to the

Sallen-Key filters and the buffers. The variable gain amplifier was designed to have lower noise, to leave more room for the noise contributed by the Sallen-Key filters and the buffers.

The noise breakdown of the baseband filter for GSM with different VGA gain settings is shown in Table 7.1. The noise power for all the different blocks are referred to the input of the variable gain amplifier and then added together to give the total noise. When referred to the input of the variable gain amplifier, the noise is maximum for the minimum gain setting. This is because the noise is dominated by the Sallen-Key filters and the buffer blocks. When the VGA gain increases, the input-referred noise from those blocks is divided by a higher gain factor. For the minimum gain setting, the variable gain amplifier contributes 16% of the noise,

Variable Gain	VGA Contribution	Sallen-Key Contribution	Buffer Contribution	Total Input-Referred Noise
6 dB	$8.41 \times 10^{-12}\ V^2$	$31.4 \times 10^{-12}\ V^2$	$12.60 \times 10^{-12}\ V^2$	$52.41 \times 10^{-12}\ V^2$
9 dB	$8.07 \times 10^{-12}\ V^2$	$16.0 \times 10^{-12}\ V^2$	$6.43 \times 10^{-12}\ V^2$	$30.50 \times 10^{-12}\ V^2$
12 dB	$7.18 \times 10^{-12}\ V^2$	$7.84 \times 10^{-12}\ V^2$	$3.15 \times 10^{-12}\ V^2$	$18.17 \times 10^{-12}\ V^2$
15 dB	$6.60 \times 10^{-12}\ V^2$	$4.00 \times 10^{-12}\ V^2$	$1.61 \times 10^{-12}\ V^2$	$12.21 \times 10^{-12}\ V^2$
18 dB	$6.15 \times 10^{-12}\ V^2$	$1.96 \times 10^{-12}\ V^2$	$0.79 \times 10^{-12}\ V^2$	$8.90 \times 10^{-12}\ V^2$

Table 7.1: Tabulated breakdown of input-referred noise at VGA input (GSM)

the two Sallen-Key filters contribute more than 50% of the total noise and the buffers are also a dominant source of noise, contributing 24% of the noise.

The noise breakdown for the DECT standard is shown in Table 7.2. Again, the total noise is the highest for the minimum gain setting. The variable gain amplifier contributes only 8% of the total noise. The Sallen-Key filters and the buffers contribute 77% and 14.5% of the total noise respectively.

Variable Gain	VGA Contribution	Sallen-Key Contribution	Buffer Contribution	Total Input-Referred Noise
6 dB	50.8×10^{-12} V^2	464.4×10^{-12} V^2	87.4×10^{-12} V^2	602.6×10^{-12} V^2
9 dB	44.9×10^{-12} V^2	236.9×10^{-12} V^2	44.6×10^{-12} V^2	326.4×10^{-12} V^2
12 dB	39.7×10^{-12} V^2	116.1×10^{-12} V^2	21.9×10^{-12} V^2	177.7×10^{-12} V^2
15 dB	35.4×10^{-12} V^2	59.2×10^{-12} V^2	11.2×10^{-12} V^2	105.8×10^{-12} V^2
18 dB	31.0×10^{-12} V^2	29.0×10^{-12} V^2	5.46×10^{-12} V^2	65.46×10^{-12} V^2

Table 7.2: Tabulated breakdown of input-referred noise at VGA input (DECT)

The breakdown of the power dissipation for the baseband filter blocks is presented in Figure 7.2. The Sallen-Key filters and the buffers dissipate the most power and this is neccessitated by their specifications. For example, recall that the Sallen-Key filters have two

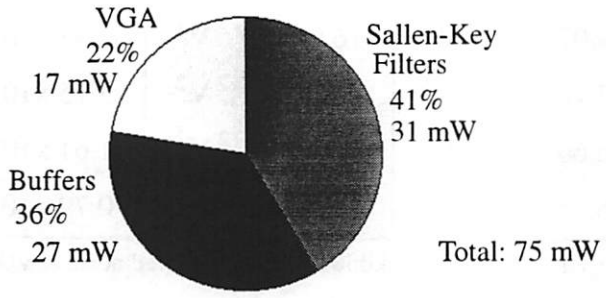


Fig. 7.2: Power Breakdown of Baseband Filter

opamps in each filter which must charge up the large feedback capacitors to meet the slew rate requirements. The power dissipation in the buffers is high because a wide unity-gain bandwidth is required to meet the ADC settling requirements. The total power dissipation of the baseband filter is 75 mW.

7.2.2 Intermodulation Performance

The intermodulation performance of the filter is important to ensure that any non-linearities do not degrade the performance of the entire receiver. The baseband filter was simulated together with the sigma-delta modulator following it to check the 3rd order input intercept point (IIP_3) for the baseband circuits. The IIP_3 requirement for the baseband circuits is 12 dBV.

Two tones to represent the blockers, are applied at 900kHz and 1.7MHz. The fundamental and the absolute 3rd order intermodulation terms are plotted and extrapolated. This is shown in Figure 7.3. The cross-over point is the IIP_3. The simulated IIP_3 is 26 dBV.

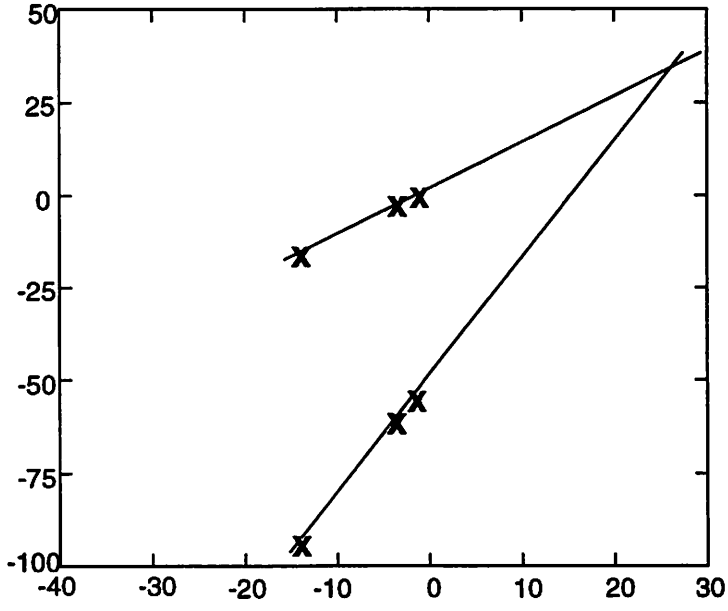


Fig. 7.3: Input Referred 3rd Order Intercept Point

7.2.3 Summary of Simulated Performance

A summary of the simulated performance of the baseband filter is shown in Table 7.3.

	SPECIFICATIONS	SIMULATED RESULTS
Dynamic Range GSM DECT	 85 dB 75 dB	 90 dB 80 dB
IIP_3	12 dBV	26 dBV
Power	minimize	75 mW

Table 7.3: Simulated Performance of Baseband FIlter

The key results of this project is summarized below:

- Designed a baseband filter that meets the GSM and DECT specifications. Estimated power consumption is 75mW.
- Developed a filter with a programmable bandwidth to adapt to the different signal bandwidths for GSM and DECT
- Developed a high-linearity variable gain amplifier with discrete gain control that accommodates for gain variation in the RF front-end. This maximizes the input to the ADC without overloading.

7.3 Future Work

An area which will be of interest for future work is power reduction strategies for the baseband filter. This may include implementing the variable gain and the filtering in one block. In addition, the implementation of fully-differential Sallen-Key filters and buffers can be explored to save power dissipation. Optimizing the power distribution among the baseband filter, the sigma-delta modulator and the digital blocks should be investigated. One way would be to use a power-adaptive technique where high dynamic baseband circuits are used when large adjacent blockers are present and low dynamic baseband circuits are used to conserve power when only moderate blockers are present [31].

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