THE DESIGN AND IMPLEMENTATION OF A DOWNCONVERSION MIXER FOR A WIDEBAND CDMA RECEIVER

by

Brian Limketkai

Memorandum No. UCB/ERL M99/66

16 December 1999

COVER

THE DESIGN AND IMPLEMENTATION OF A DOWNCONVERSION MIXER FOR A WIDEBAND CDMA RECEIVER

by

Brian Limketkai

Memorandum No. UCB/ERL M99/66

16 December 1999

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

THE DESIGN AND IMPLEMENTATION OF A DOWNCONVERSION MIXER FOR A WIDEBAND CDMA RECEIVER

by

Brian Limketkai

16 December 1999

College of Engineering

University of California, Berkeley

94720

The Design and Implementation of a Downconversion Mixer for a Wideband CDMA Receiver

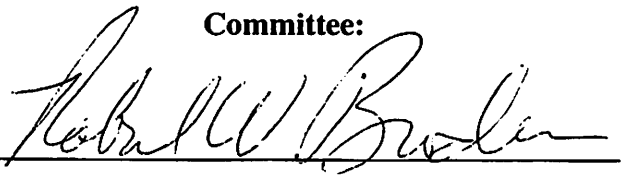
by Brian Limketkai

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II.**

Approval for the Report and Comprehensive Examination:

Committee:



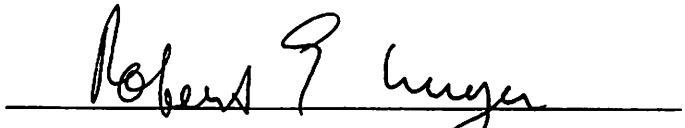
Robert W. Brodersen

Research Advisor

12/13/99

Date

* * * * * *



Robert G. Meyer

Second Reader

12/15/99

Date

Acknowledgments

As with any endeavor, this research project could not have been completed without the help and support of others. Foremost, I wish to thank my research advisor Professor Robert Brodersen. Your guidance throughout the course of this project is greatly appreciated. I would also like to thank Professor Robert Meyer for reviewing this thesis and providing helpful comments.

I am greatly indebted to Dennis Yee for his friendship and his selflessness in teaching me everything I know about RF design. The success of this project would not have been possible without your guidance. Thanks Dennis!

I am also very grateful to all the members of my group who have helped me get through the hardships of this project. My thanks go out to Sayf Alalusi, Chinh Doan, Dennis Yee, Johan Vanderhaegen, David Sobel, and Sam Blackman for helping me during those times. Special thanks to Dennis for proofreading this report, and providing me with the template for this acknowledgment. Chinh has always been there whenever I needed to play pool. Thanks to Sayf for the hours of fun in Unreal. I would also like to thank Johan for all the Belgian jokes he sends me.

Finally, I would like to thank my family and friends for their support and encouragement. I am very lucky to have wonderful friends who have helped me throughout my college years like Payam, Vito, Bret and Varun.

Berkeley, you are always there for me, even when you are in the other room. Thanks big bro!

I would also like to thank my other brothers, Benson, Benjie, and Benhan for their love and support. Thanks Benson for taking the bus in the morning, and understanding when I need to go home really late. Thanks Benjie for being yourself.

Your weirdness has always been a source of amusement. Thanks hopper for all the times you've made me laugh, and for being there when I needed someone to pick on.

Mommy and Daddy, your continual love and encouragement have been a source of strength for the past 22 years. I dedicate this work to you will all my love.

Contents

Figures

Tables

Chapter 1

Introduction

Communication is an essential component to the advancement of technology. From the scribbles inside cave walls of a hundred thousand years ago to the vast internet database of today, the exchange of information has always been vital to our society's growth. The transfer of information lets us learn from the work of others, allowing us to build our foundation of knowledge faster than otherwise possible. One of the first modern communications system, the telephone, was partly responsible for the phenomenal growth of the 20th century. The telephone gave us a means to exchange information very quickly across the continental United States, which before 1876 meant sending mail through the Pony Express. With an almost instantaneous transfer of information, society boomed as scientific, as well as non-scientific, discoveries were shared between people thousands of miles apart.

Today's communications system have come a long way since Bell's days. High speed communications systems are now commonplace and can provide quick and reliable connections to worldwide databases. Many different methods of communication are also now feasible through different media. But whether it is the wired cable mo-

dem providing many channels of high speed video connections to the home or the wireless cellular phone being used to connect two friends for an impromptu conversation, most modern communications systems still need to convert the signal to a form suitable for transmission. This usually entails translating the signal frequency into a band suitable for transmission. For the case of the cable modem, frequency translation is used to selectively choose different frequency bands representing different television channels. On the wireless device, translation into the higher frequencies makes the design of antennas practical, in addition to providing channels for communication between multiple users. Frequency translating blocks have even found some esoteric uses such as in the chopper stabilizer.[1] These examples show the importance of frequency translation in modern communications systems. As a consequence, the design of the frequency translating block, the mixer, requires special attention in any communications system design.

This report focuses on the design of a monolithic downconversion mixer implemented in a standard 0.25 μm CMOS process. Chapter 2 gives a brief overview of receiver architectures amenable to monolithic integration in CMOS, along with some applications to indoor wireless systems. Chapter 3 then focuses on the system-level operation of a downconversion mixer. Figures of merit for a downconversion mixer are also introduced, as well as second-order effects that a mixer designer should consider when implementing a design. Tradeoffs between different parameters will also be touched upon lightly. Chapter 4 describes in detail two different types of mixers, the passive and the active. One example of each type will be presented in more detail with the tradeoffs in implementing each design. The chapter finishes with a comparison between the two types of mixers. Chapter 5 is a case study of the design of a downconversion mixer for an indoor wireless system. The final mixer design will be presented. Important considerations in implementing the mixer will also be discussed. Finally, concluding thoughts are summarized in Chapter 6.

[1] A chopper stabilizer translates signals into the higher frequencies, where there is less flicker noise, before amplification, then back down to lower frequencies after amplification.

Chapter 2

Receiver Architectures

The design of the mixer depends a lot on the receiver architecture used for the communications system. The choice of architecture imposes certain requirements on the mixer, with different mixer design specifications associated with different architectures. Obviously, a host of different possible receiver architectures exist, making the understanding of the particular application important to ensuring a sensible choice of architecture. In this report, we will consider mixers in an indoor picocellular wireless environment, though most of the mixer theory is equally applicable to other communications systems, such as outdoor cellular or wired systems.

The indoor wireless environment is a relatively new field of wireless research. The first wireless systems were installed outdoors to try to provide communications to areas where installing cables was expensive or prohibitive. Unlike in the outdoor environment, there was no great need to install wireless systems inside buildings where wiring was cheap and easily available. The goal in the indoor wireless environment is to outperform current indoor wiring technologies, mainly cables, in areas such as cost, convenience, and perhaps even data rate. In order to be competitive in this

environment, the indoor system has to be portable, consume little power, and support the data rates that current cables already provide. With these objectives in mind, we will see that the monolithic integration of the receiver makes sense.

2.1 Single-Chip Implementations

Combining the analog and digital sections of the receiver greatly reduces cost as the need for a separate fabrication process is removed. In addition, by integrating the whole system on a single chip, the assembly cost of the final product is reduced as there is no longer a need to install external components after circuit fabrication.

But does this integration affect the power consumption of the circuit? Obviously, the parasitic losses due to packaging is detrimental to the performance of the system if high-frequency signals have to go off-chip. One solution would be to leave the high-frequency signals on-chip, and only go off chip at lower frequencies. However, with the higher data rates being achieved by modern wireless systems, all signals are considered high-frequency signals. Another possibility would be to implement two chips in the same package, but on separate dies. This minimizes the parasitic losses, but leads to very costly packaging which will probably prevent this technique from being widely-used. So, monolithic integration of the whole system seems to be the most favorable choice for mainstream technology. But then, which technology should we use to implement this single-chip system?

Today, most digital circuits are implemented in CMOS, and high-frequency analog circuitry in bipolar technologies. Clearly, the monolithic integration of the system requires choosing one process for both sections. By implementing both analog and digital sections in bipolar technologies, we increase power consumption of the digital section due to the static power consumption of bipolar logic gates. With the large number of digital logic required on most of today's systems, even a slight increase in the power consumption of a single gate could be significant. On the other hand, implementing the analog front-end in CMOS increases power consumption due to the MOSFET's smaller transconductance. The smaller transconductance leads to more noise, which means CMOS analog circuits must consume more power to achieve noise

levels equivalent to those of bipolar circuits. This means that the increase in power consumption due to the small analog section may be comparable to the increase in power consumption due to the large digital section. From this argument, we cannot make a choice of technology simply based on the power consumption of the analog or digital sections of the chip. How then will we choose our process?

Because of the high energy efficiency of CMOS for digital circuits, and the higher performance that CMOS digital circuitry provides over bipolar, CMOS is probably the better technology of the two. With the rapid pace at which CMOS technology is advancing, the advantage that bipolar technologies offer for analog circuit design is quickly diminishing. With transition frequencies, f_T, of CMOS processes up in the GHz range, it is now easily possible to realize high-speed wireless devices in CMOS.

A monolithic CMOS[1] implementation of an indoor wireless system would feature low cost, portability, faster development and assembly time, and the newest technologies of today. Thus, for these reasons, we will only consider receiver architectures that lend themselves to monolithic integration in a CMOS process.

2.2 Heterodyne Receivers

We will begin with an explanation of the conventional heterodyne receiver architecture, shown in Fig. 2.1. Though we will later see that the heterodyne architecture may not be the best choice for an indoor wireless communications system, we can use this section to explain the basic concepts of receiver architectures.

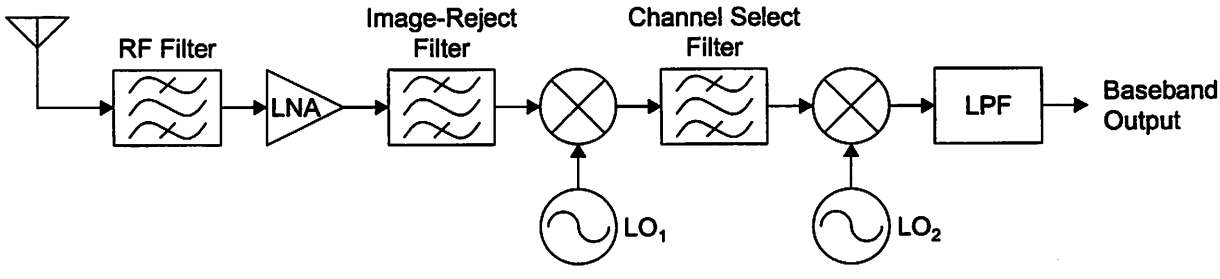


Figure 2.1 Heterodyne receiver architecture.

[1] Because of the higher cost, we will not consider Gallium-Arsenide or other exotic technologies.

The basic premise behind the heterodyne receiver is the translation of the radio-frequency (RF) signal to a lower frequency, called the intermediate frequency (IF), in order to relax the design requirements of the channel select filter. In systems that distinguish users by their frequency bands, the channel select filter is a band pass filter that passes select frequency bands allocated to a desired *channel*, while attenuating all other frequencies. This selective filtering of channels would be very difficult without an IF since variable-frequency band pass filters are not easily designed. Instead, the IF is fixed as the RF signal is shifted down by different amounts to center the desired channel at the IF.

The RF filter is a fixed-frequency filter that attenuates signals coming from other radio systems, termed out-of-band signals. The low-noise amplifier (LNA) then provides primary gain for the receiver front-end. As the first block in the whole chain, the noise it contributes will add directly on top of the still weak received signal. As a result, the LNA's noise will have the most significant effect on the signal-to-noise ratio (SNR) of the system. Thus, the primary objective in the LNA's design is to provide large gain with minimal noise.

On most heterodyne systems, the image-reject (IR) filter and mixer follow the LNA. The mixer, which is essentially an analog multiplier, performs the frequency translation through multiplication of the local oscillator (LO) waveform with the RF signal. The image-reject filter, as its name implies, provides attenuation for the image of the RF signal. The image of a signal is defined as the frequency component which will be superposed on the desired signal after frequency translation. This concept can be seen in Fig. 2.2.

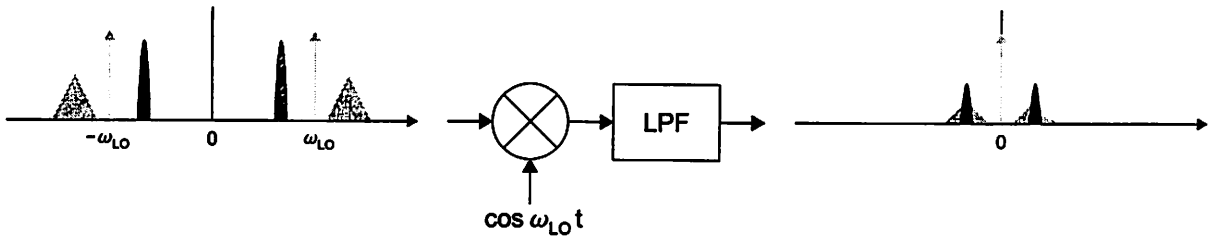


Figure 2.2 Superposition of image and signal.

The frequency plot of any real signal will be conjugate symmetric about the zero-frequency axis as shown in [1]. Multiplication of the RF signal with the LO waveform superimposes a negative-shifted and a positive-shifted copy of the frequency plot on top of each other, with the amount of shift equal to the frequency of the LO waveform. It follows that the presence of a large out-of-band signal at the image frequency could possibly corrupt detection of the desired signal. Thus, image-reject filters are usually placed to provide attenuation.

The astute reader may notice that the image-reject filter and the RF filter seem to perform the same function. So why bother putting an image-reject filter? Image-reject filters are used to filter out the out-of-band signals due to the LNA, such as noise and nonlinearities. Since we want the mixer to see the smallest image possible, the IR filter is usually placed right before the mixer. LNAs designed with tuned loads incorporate the IR filter into the load, thus some designs may not show a separate IR filter block.

The variable frequency channel select filter selectively passes the frequency band of interest, for systems with frequency-multiplexed channels, such as FDMA [2]. The second mixer then downconverts the signal from the intermediate frequency to base-band.

As can be seen, the heterodyne architecture is somewhat complicated. It contains many blocks, each of which consumes power. The filters attenuate the signal, and usually must be compensated for by power-consuming gain blocks. In addition, achieving high attenuation in the IR filter is difficult to do on-chip due to the low Q's of on-chip inductors. Hence, external passive filters are usually used. Clearly, our goal of a single-chip implementation cannot be achieved if we have to go off-chip. Thus, we may want to consider other architectures that do not pose as difficult a design requirement for the filters.

2.3 Homodyne Receivers

By mixing down the RF signal directly to DC, through matching of the LO frequency with the center frequency of the RF passband, a zero IF is achieved. Hence, the

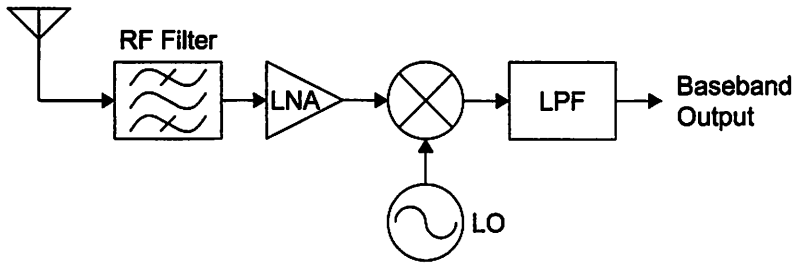


Figure 2.3 Homodyne receiver architecture.

homodyne architecture, shown in Fig. 2.3, is also referred to as zero-IF or direct-conversion. Unlike the heterodyne receiver, the homodyne receiver does not have an image problem as shown in Fig. 2.4. Thus, an image-reject filter is not needed, making this architecture more amenable to monolithic integration.

The direct-conversion system, however, does have other problems not present in heterodyne systems. Because the signal bandwidth now extends directly to DC, any DC offset sits inside the signal bandwidth and corrupts the received signal. In addition, the DC offsets pass unfiltered through the system and may possibly saturate stages down the receiver chain. Circuit techniques to reduce DC offsets, such as offset cancellation or AC coupling, may remove some of the desired signal if used after downconversion. DC offsets can be a big problem in direct-conversion systems, and must be handled appropriately. Techniques to reduce the DC content of a signal, through coding or redefinition of the baseband signal, can be used to mitigate this problem.

With the signal bandwidth centered at zero, the channel select filter is now a low pass filter. Passive implementations of low pass filters with low cutoff frequencies

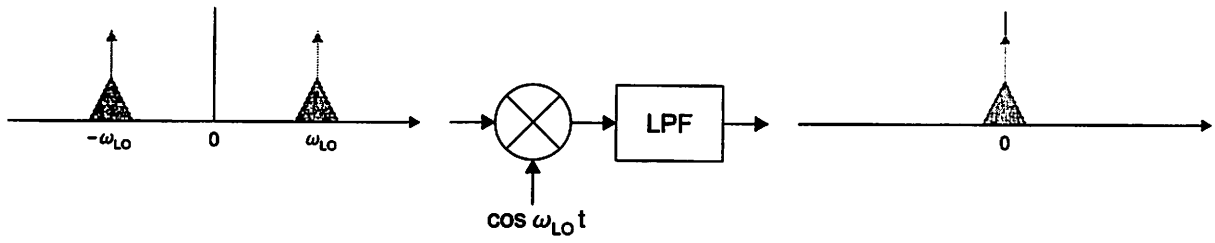


Figure 2.4 Homodyne downconversion without image.

require large capacitors which are impractical for on-chip solutions. To circumvent this problem, we can use active filters. However, care must be taken in designing the active filter so as not to introduce too much noise or nonlinearities. At the lower frequencies, the flicker noise of the MOSFET may be a problem.

Despite the problems with the homodyne architecture, its simplicity is a big advantage over the heterodyne system. The homodyne system also lends itself to monolithic integration with the removal of external filtering. However, the right choice of architecture depends on the application, and perhaps, a variant of these two receivers may be the better choice.

2.4 Image-Reject Receivers

To cope with the image problem present in the heterodyne receiver, several systems have been proposed which cancel the image. These architectures are referred to as image-reject architectures. Two of the more common ones will be presented here, the Hartley and Weaver image-reject receivers. A more complete description and analysis of these architecture can be found in [7].

2.4.1 Hartley Architecture

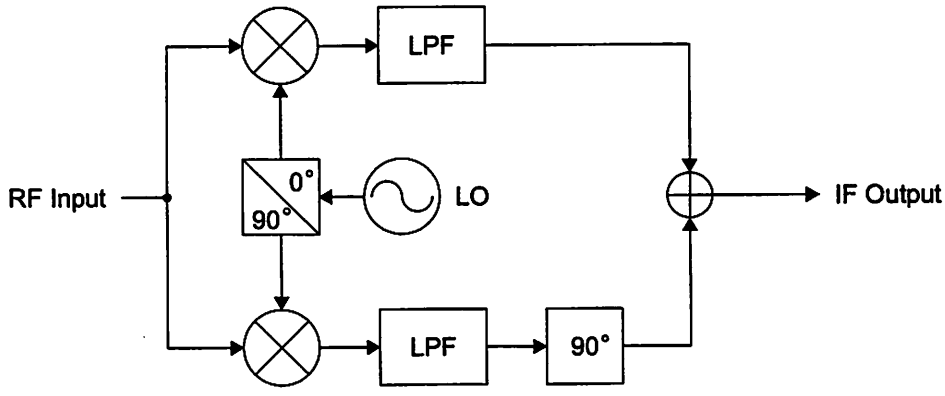


Figure 2.5 Hartley image-reject architecture.

The Hartley architecture shown in Fig. 2.5 performs image-rejection through a phase-shifting method. The 90° phase-shifting block is simply the Hilbert transformer, with

the transfer function

$$H(j\omega) = -j\,\mathrm{sgn}(\omega) \tag{2.1}$$

The multiplication of the RF signal with the 90° phase-shifted LO followed by a phase-shift inverts the signals on one side of the LO, hence distinguishing the signal from the image. Adding this to the signal downconverted with the nonphase-shifted LO leads to image-rejection. A disadvantage of the Hartley architecture is the need for a wideband phase shifter. The Hilbert transformer shown must provide 90° phase shift over the whole RF signal bandwidth.

2.4.2 Weaver Architecture

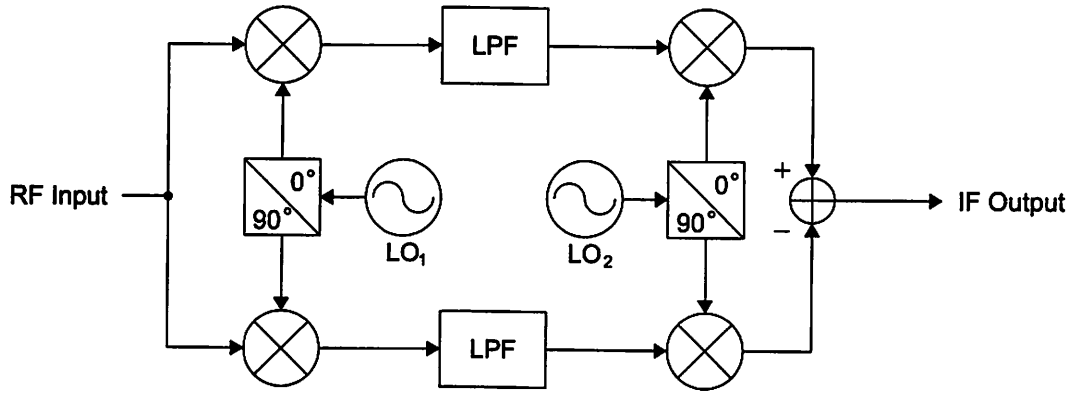


Figure 2.6 Weaver image-reject architecture.

The main difference between the Weaver architecture and the Hartley architecture is the removal of the phase shifter at RF. Instead, two additional mixers are placed after the LPFs to perform the phase-shifting. Rather than achieving image-rejection with only one downconverting step as in the Hartley architecture, the Weaver architecture first downconverts the signal to a "temporary" intermediate frequency. After the first downconversion, one path is multiplied by a sine wave, which is simply a phase-shifted cosine wave, equivalently downconverting the signal to the output frequency and phase-shifting by 90° at the same time. The other path, which is multiplied by the cosine wave, is downconverted without the phase-shift. Like in the Hartley architecture, image-rejection can then be achieved.

Frequently, the Weaver architecture is used to convert the RF signal directly to baseband. Lumping all four mixers into one super mixer block, the internal IF can be viewed as a temporary IF used to perform the phase-shifting, hence this architecture is sometimes referred to as quasi-IF.

The Weaver architecture does have a 90° phase shifter to create the quadrature signals, but this is narrowband and only needs to provide a 90° phase shift at one frequency, and hence should be easier to design.

Chapter 3

Downconversion Mixers

Unless the received signal's frequency can readily be digitized then processed by the digital hardware, some frequency translation is needed to downconvert to a lower frequency more suitable for processing. With the exception of digital radios, most radios need to downconvert the received signal. Hence, the downconversion mixer is one of the more important blocks of the receiver chain. This chapter will present a system-level analysis of the downconversion mixer which is suitable for making architectural decisions when designing the receiver.

3.1 General Mixer Theory

From basic linear systems theory, we know that the frequencies of an output of a linear block can only consist of frequencies present at the input. Hence, to achieve frequency translation, mixers have to be nonlinear.

3.1.1 Conversion Gain

Multiplication is one of the most basic nonlinearities. In fact, most mixers are basically analog multipliers. To see how mixers translate signal frequencies, we first

represent signals as a sum of sinusoids. Then, the multiplication of two sinusoids gives

$$\cos\omega_1 t \cos\omega_2 t = \frac{1}{2}\cos(\omega_1 - \omega_2)t + \frac{1}{2}\cos(\omega_1 + \omega_2)t \tag{3.1}$$

which is the sum of two signals at the sum and difference frequencies.

For this analysis, we will assume that the mixer input coming from the previous block, such as the LNA, is small and doesn't affect the gain of the mixer. In other words, only the LO overdrives the mixer. We also assume the gain of the mixer affects the input signal linearly. We represent the input to the mixer by

$$S_i = a_0 + a_1\cos\omega_i t + a_2\cos 2\omega_i t + \ldots \tag{3.2}$$

However, for simplicity, we will only consider a single tone input,

$$S_i = a_1\cos\omega_i t \tag{3.3}$$

and the time-varying gain of the mixer driven by an oscillator with frequency ω_0,

$$G = g_0 + g_1\cos\omega_0 t + g_2\cos 2\omega_0 t + \ldots \tag{3.4}$$

Hence, the output of the mixer is then expressed as

$$S_o = GS_i \tag{3.5}$$

$$= a_1 g_0\cos\omega_i t + \frac{a_1 g_1}{2}\cos\left(\omega_i - \omega_0\right)t + \frac{a_1 g_1}{2}\cos\left(\omega_i + \omega_0\right)t + \ldots \tag{3.6}$$

The second and third terms are the signals of interest. We see that this nonlinear circuit downconverts the RF signal to $\omega_i - \omega_0$ as well as upconverts it to $\omega_i + \omega_0$. For both downconversion and upconversion mixers, the conversion gain is $\frac{1}{2}g_1$. Note that for an input tone at frequency $2\omega_0 - \omega_i$, we would get a downconverted term at $\omega_i - \omega_0$. This, as introduced in the previous chapter, is the image that corrupts the downconverted signal.

What happens if the oscillator is not synchronized with the incoming RF signal? We can represent the timing offset by t_0. Then, the RF signal becomes

$$S_i = a_1\cos(\omega_i t + \phi) \tag{3.7}$$

$$= a_1\cos\phi\cos\omega_i t - a_1\sin\phi\sin\omega_i t \tag{3.8}$$

where

$$\phi = \omega_i t_0 \tag{3.9}$$

Then,

$$\begin{aligned} S_o = {} & a_1 g_0 \cos\phi \cos\omega_i t - a_1 g_0 \sin\phi \sin\omega_i t \\ & + \frac{a_1 g_1}{2} \cos\phi \cos\left(\omega_i - \omega_0\right) t + \frac{a_1 g_1}{2} \cos\phi \cos\left(\omega_i + \omega_0\right) t \\ & - \frac{a_1 g_1}{2} \sin\phi \sin\left(\omega_i - \omega_0\right) t - \frac{a_1 g_1}{2} \sin\phi \sin\left(\omega_i + \omega_0\right) t + \ldots \end{aligned} \tag{3.10}$$

Because of the offset, some of the signal energy of the cosine term leaks into the sine term. Quadrature[1] systems will experience some corruption of signal as the in-phase data is leaked into the quadrature channel. For a direct-conversion receiver with $\omega_i = \omega_0$, the sine term is not present, and the conversion gain is reduced to $\frac{1}{2} g_1 \cos(\phi)$.

We will now consider the conversion gain of a mixer with a square mixing function. The Fourier series of a square wave is

$$\frac{4}{\pi}\left(\cos\omega_0 t - \frac{1}{3}\cos 3\omega_0 t + \frac{1}{5}\cos 5\omega_0 t - \ldots\right) \tag{3.11}$$

So the conversion gain for a synchronized signal is

$$G_{square} = \frac{2}{\pi} \tag{3.12}$$

For a non-ideal square wave with finite rise and fall times, t_r, the conversion gain is

$$G_{ramp} = \frac{2}{\pi} \frac{\sin\left(\omega_0 \frac{t_r}{2}\right)}{\omega_0 \frac{t_r}{2}} \tag{3.13}$$

(see Appendix for derivation).

However, note that this is the conversion gain for a memoryless mixer, since the output can be determined completely by the inputs at the same point in time. A more complicated analysis using Volterra series may be used to include memory effects. A good explanation of Volterra series can be found in [20].

[1] Quadrature systems modulate data on a cosine wave and sine wave, called the in-phase and quadrature-phase components, respectively.

3.1.2 Linearity

Despite the apparent irony of designing a "linear" mixer, mixer designers often use the term "linearity" to describe mixer performance. Ideally, the only nonlinearity in a mixer should be the one that translates the input signal's frequency. In the previous section, we assumed that the mixer affected the RF signal in a linear way. However, most mixers will affect the RF signal nonlinearly, such that (3.5) becomes

$$S_o = G_1 S_i + G_2 S_i^2 + G_3 S_i^3 + \ldots \tag{3.14}$$

A basic measure of distortion is harmonic distortion, defined by

$$HD_n = \frac{\text{amplitude of } nth \text{ harmonic}}{\text{amplitude of fundamental}} \tag{3.15}.$$

In mixers, the fundamental refers to the downconverted signal, at frequency $\omega_i - \omega_0$, since this is the desired signal. Any signal at frequency ω_i which appears at the output is referred to as RF-IF feedthrough, and is undesirable in most mixers.

For the sinusoid input (3.3),

$$S_i^2 = \frac{a_1^2}{2} + \frac{a_1^2}{2}\cos 2\omega_i t \tag{3.16}$$

$$S_i^3 = \frac{3a_1^3}{4}\cos \omega_i t + \frac{a_1^3}{4}\cos 3\omega_i t \tag{3.17}$$

The tone at frequency $2\omega_i$ will be downconverted to $2\omega_i - 2\omega_0$ by the second harmonic of the LO. This is the second harmonic of the downconverted signal. The same principle applies for higher orders.

Intermodulation distortion, more commonly referred to as "intermod," measures the amount of spurious signals generated by two input signals. In communications systems, this metric is often used more than harmonic distortion to measure the nonlinearities of a block. Intermodulation distortion is defined as

$$IM_n = \frac{\text{amplitude of } nth\text{-order IM product}}{\text{amplitude of fundamental}} \tag{3.18}$$

For two equal amplitude input signals at frequencies ω_1 and ω_2, the nth-order IM product is any tone at frequency $p\omega_1 + q\omega_2$ where $|p| + |q| = n$.

Consider two tones at the input of the mixer,

$$S_i = a_1 \cos \omega_1 t + a_2 \cos \omega_2 t \tag{3.19}$$

The third order intermodulation terms, at frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$, are of particular concern since they appear in the vicinity of ω_1 and ω_2 for ω_1 close to ω_2. The downconverted third order intermodulation product is then simply $2\omega_1 - \omega_2 - \omega_0$ and $2\omega_2 - \omega_1 - \omega_0$.

Intermodulation distortion can also be specified in terms of the amplitude of the signals when the *nth*-order intermodulation product equals the fundamental. This is called the intercept point. From [20], we know that the third order intermodulation product grows like the cube of the input amplitude, while the fundamental grows linearly as shown in Fig. 3.1.

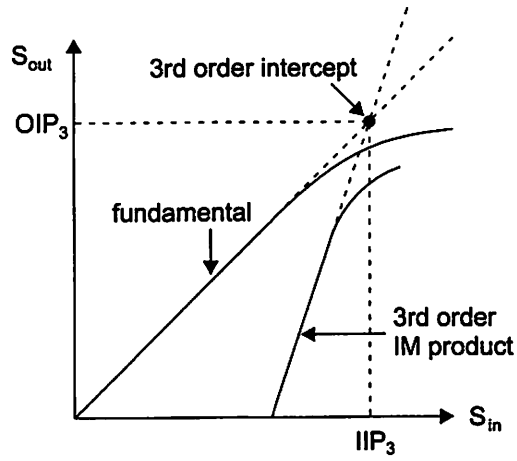


Figure 3.1 Third-order intercept.

The intersection of the extrapolated fundamental and third-order IM curves is called the intercept point. The corresponding input and output amplitudes are called the input and output intercept (IIP and OIP), respectively. We have to take the extrapolated curves because most circuits suffer from a form of gain degradation, called gain expansion or gain compression, as the input amplitude is increased. Gain compression or expansion is caused by the nonlinearities of the circuit. From (3.17), we see that the first term, $\frac{3}{4}a_1^3 \cos \omega_i t$ is multiplied with G_3 in (3.14), to give a downconverted

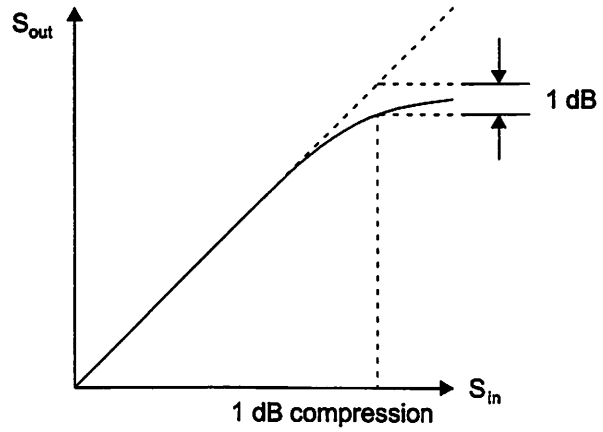


Figure 3.2 1-dB compression point.

term at frequency $\omega_i - \omega_0$. This term either adds or subtracts from the gain of the mixer, giving gain expansion or compression. The gain compression of a system is usually specified with the 1-dB compression point, which occurs when the gain of the circuit decreases by 1 dB from the ideal linear gain curve as depicted in Fig. 3.2.

Other forms of distortion, such as cross-modulation distortion and triple-beat distortion are covered in [19] and [20]. Cross-modulation, which measures the transfer of modulation from one frequency to another, is important when large amplitude-modulated signals pass through a nonlinear block along with a weak signal.

3.1.3 Linearity of the Short-Channel MOSFET

Because of the importance of the differential pair in analog design, we will now examine its distortion characteristics. We will find the distortion in the output current of the differential pair with the voltage across the gates as the input signal. With matched devices, the differential pair is symmetric and there is no second order distortion. From [19] and [20], we get

$$HD_3 = \frac{1}{32}\frac{V_i^2}{(V_{gs} - V_t)^2} \tag{3.20}$$

where V_i is the amplitude of the input signal. This is true for the ideal square-law MOSFET. However, in modern analog circuit design, we usually design with short-

channel transistors that do not always follow the square law description

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_t)^2 \tag{3.21}$$

The equation for the drain current in the short-channel MOSFET is

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_t)^2 \frac{1}{1 + \frac{(V_{gs} - V_t)}{E_{sat}L}} \tag{3.22}$$

where E_{sat} is the critical field which marks the onset of velocity saturation. Obviously, (3.22) is a lot more complicated than (3.21), hence a simple closed-formed expression for HD_3 may not be practical. Instead, we will try to find a computer model for the distortion of the differential pair. By solving for HD_3 in *Mathematica* using (3.22), we can find a closed-form expression for the third order distortion. Unfortunately, this expression is three pages long and will not be useful to the circuit designer.

However, with this model, we can qualitatively understand the behavior of the short-channel differential pair. As shown in Fig. 3.3, we observe that when the tail

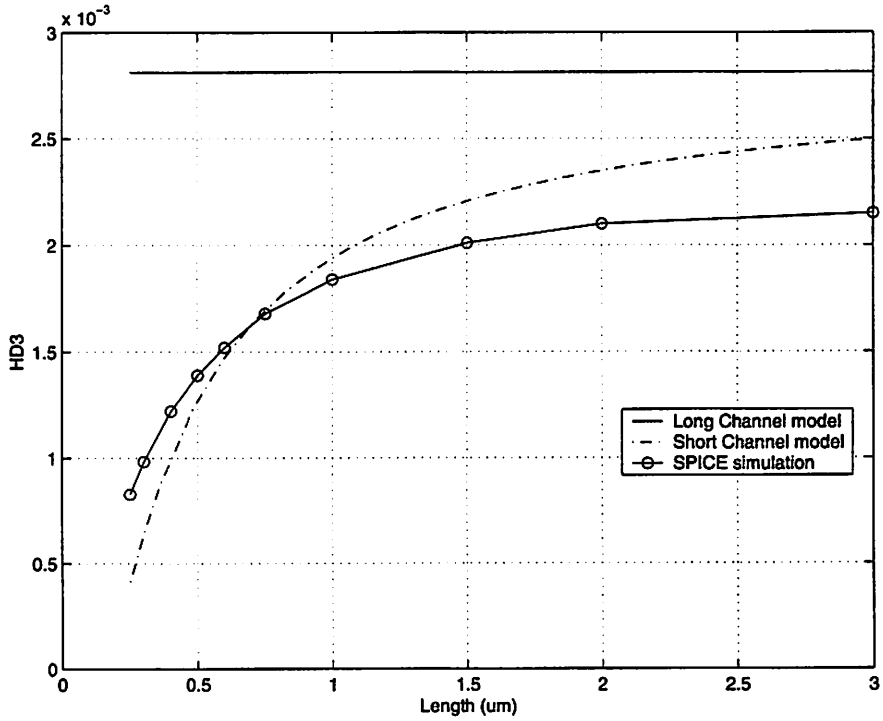


Figure 3.3 HD_3 of the differential pair.

current and the W/L ratio are kept constant, HD_3 decreases as channel length decreases in the same technology. This can be explained by noting that the short-channel MOSFET approaches the velocity saturation region as channel lengths are decreased. The velocity-saturated model for current is

$$I_{ds} = C_{ox} v_{sat} W \left(V_{gs} - V_t\right) \tag{3.23}$$

where v_{sat} is the saturation velocity of the carriers. This equation for current has a linear relationship to the controlling voltage, hence in the limit as channel lengths tend to zero, harmonic distortion should be completely eliminated. From [19], harmonic distortion and intermodulation distortion are related by

$$IM_2 = 2HD_2 \tag{3.24}$$

$$IM_3 = 3HD_3 \tag{3.25}$$

Active mixers, such as the Gilbert commutating mixer, often use the differential pair as the input pair. The qualitative conclusion from this analysis is that channel lengths should be kept as small as possible to decrease third order distortion. Unfortunately, decreasing channel lengths increase the amount of mismatch between the input devices, increasing second order distortion. Choosing an optimal channel length could also possibly depend on the system specifications on distortion—IM_3 may be more important than IM_2 in some systems.

The MOS transistor is also often used in the linear region as a load, or as a variable resistance in a feedback loop. In the linear or triode region, the long-channel current equation is

$$I_{ds} = \mu C_{ox} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) V_{ds} \tag{3.26}$$

In the short-channel regime,

$$I_{ds} = \mu C_{ox} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) \frac{V_{ds}}{1 + \dfrac{V_{ds}}{E_{sat} L}} \tag{3.27}$$

Again, plugging in (3.27) into *Mathematica* and solving for HD_2 and HD_3, we see that decreasing channel lengths within a certain technology increases distortion as shown in Fig. 3.4 and Fig. 3.5.

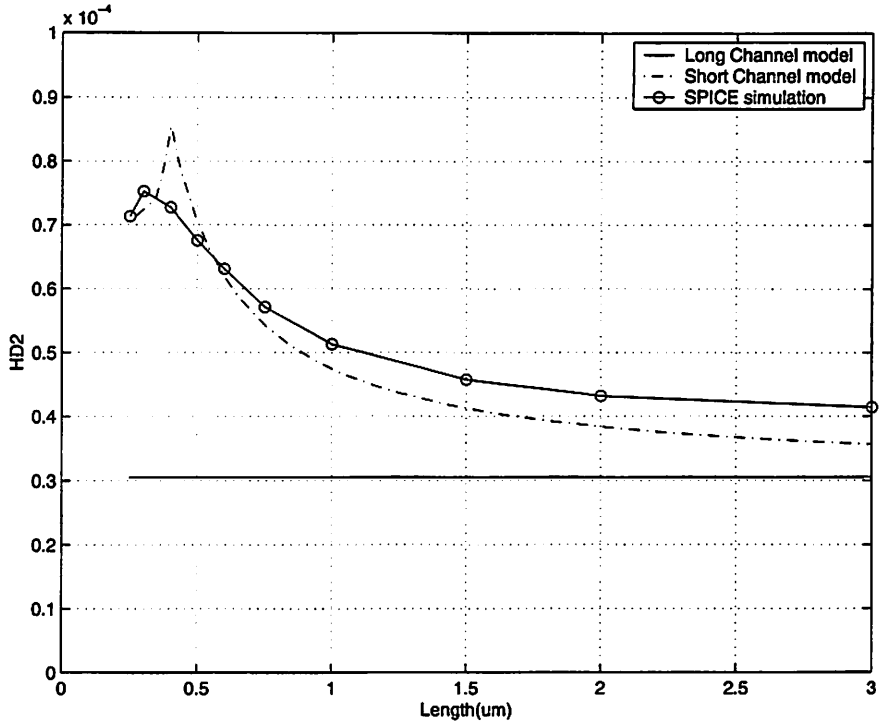


Figure 3.4 HD_2 of the MOSFET in triode region.

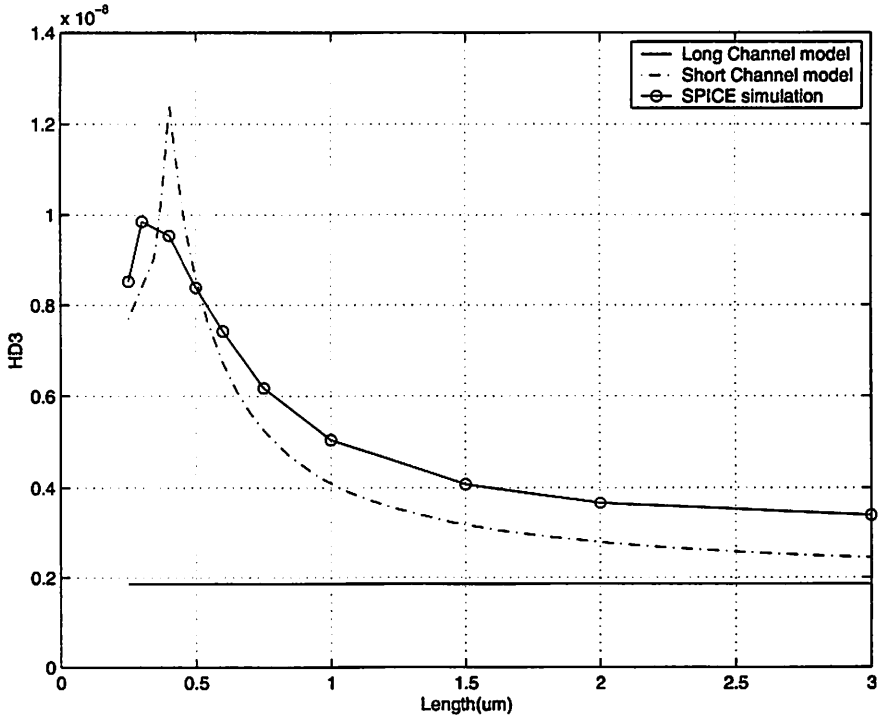


Figure 3.5 HD_3 of the MOSFET in triode region.

As channel lengths decrease, V_{dsat} decreases, and the transition from the triode region to the saturation region becomes more abrupt, thus increasing distortion. The little dip at very small channel lengths is due to V_t rolloff. The lowering of V_t increases V_{dsat} which decreases distortion.

A more complete description of the distortion analysis presented here can be found in [18].

3.1.4 Noise

The noise factor of a block is defined to be

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{3.28}$$

The noise factor expressed in dB is called the noise figure (NF). There are two types of noise figures defined for mixers, single-sideband (SSB) and double-sideband (DSB).

The single-sideband noise figure is used when the signal is present on only one side of the LO, unlike noise which is present at all frequencies as in Fig. 3.6. The mixing process folds the noise over, doubling the total noise power at the downconverted frequency while the signal power remains fixed. Heterodyne systems commonly use single-sideband noise figures.

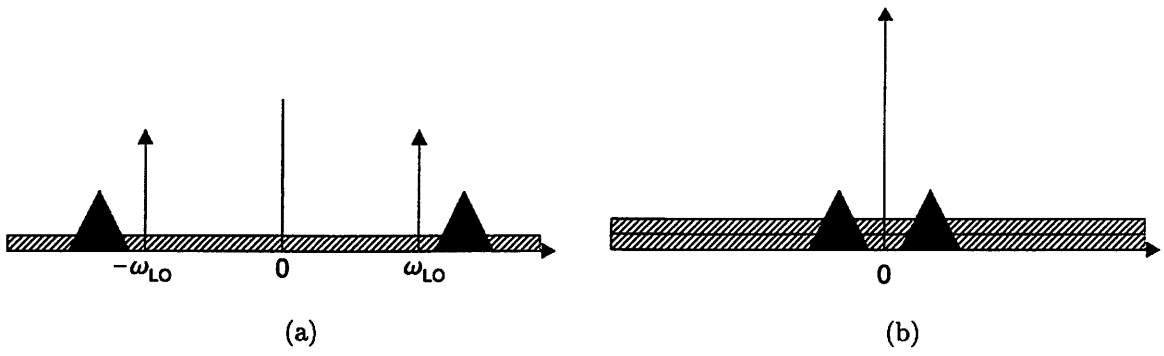


Figure 3.6 SSB noise during downconversion (a) before folding. (b) after folding.

The double-sideband noise figure is used when the signal is present on both sides of the LO as shown in Fig. 3.7. The downconverted signal doubles in power along with the noise. Double-sideband noise figures are used for homodyne systems.

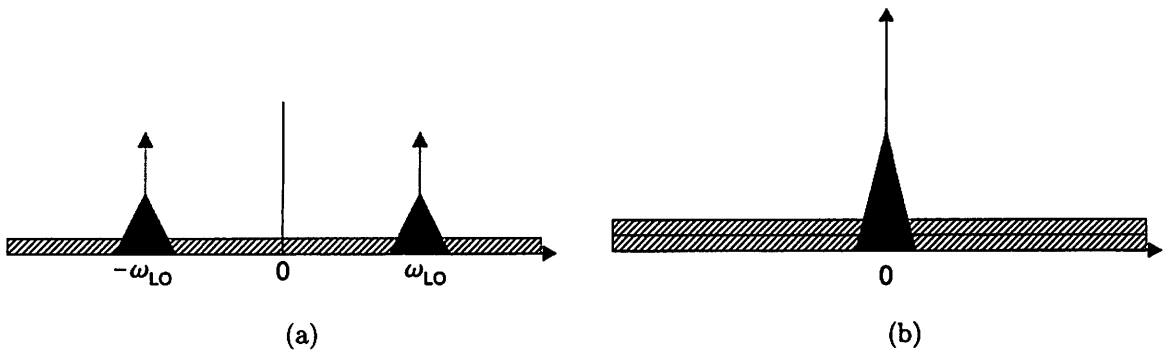


Figure 3.7 DSB noise during downconversion (a) before folding. (b) after folding.

As can be seen, the SSB noise-figure is 3 dB higher than the DSB noise-figure. Hence, care must be taken in interpreting a quoted noise figure. The correct noise figure measurement to use depends on the system. For a heterodyne system with good filtering around the signal band, noise folding might not be present and DSB noise figures might be the more appropriate measure.

3.1.5 Noise of the Short-Channel MOSFET

The noise spectral density for the long-channel MOS transistor in saturation can be found in [5],

$$S_{I_d}(f) = 4kT\frac{2}{3}g_m \tag{3.29}$$

However, since this result was derived using the square law current equation (3.21), it may not hold for short-channel transistors. An analysis of the noise of short-channel MOS devices in the saturation region is given in [14]. For short-channel devices, the thermal noise spectral density is given by

$$S_{I_d}(f) = \frac{4kT\mu C_{ox}\frac{W}{L}(V_{gs}-V_t)}{\left[(V_{gs}-V_t)+E_{sat}L\right]^2} \times \left[\frac{2}{3}(E_{sat}L)^2 + 2(V_{gs}-V_t)E_{sat}L + 2(V_{gs}-V_t)^2\right] \tag{3.30}$$

This predicts the noise of short-channel devices to be larger than long-channel devices. As explained in [14], this increase in thermal noise is due to hot electron effects, and the temperature increase of the carriers above the lattice temperature. In addition,

there is a further increase in the noise spectral density at higher drain voltages due to substrate current leakage as shown in Fig. 3.8. Substrate current causes shot noise and can be described by

$$S_{I_{sub}}(f) = 2qI_{sub} \tag{3.31}$$

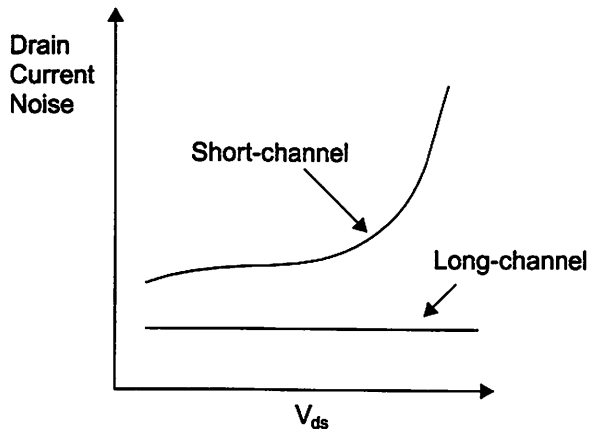


Figure 3.8 Noise spectral density of the MOSFET.

3.1.6 Port Isolation

As shown in Fig. 3.9a, LO-RF feedthrough is the leakage of the LO signal into the RF port. This feedthrough has several consequences. First, the presence of a tone at the LO frequency at the RF port results in a DC offset at the IF port. This offset may be large enough to saturate the blocks following the mixer, thereby disturbing

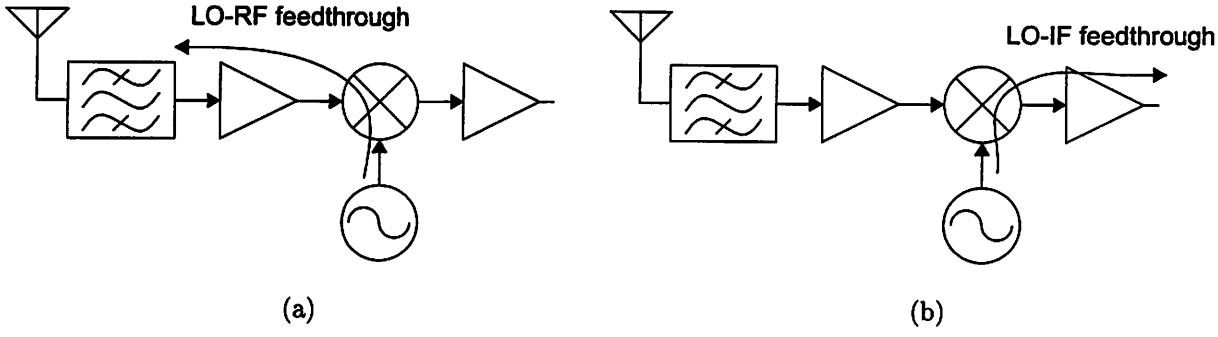


Figure 3.9 (a) LO-RF feedthrough. (b) LO-IF feedthrough.

proper operation of the receiver. This process of downconverting LO-RF feedthrough is usually called self-mixing. Secondly, some of the LO leakage signal may propagrate through the mixer, LNA, and filter, into the antenna and radiate. This reradiation could possibly reflect off objects, resulting in a tone at the LO frequency at the input of any receiver that picks it up. This tone, in turn, becomes a DC offset. However, this has a lesser effect than the self-mixing due to the small reverse gain of the LNA, along with the large loss incurred when reflecting off objects. Lastly, there are standards set by the Federal Communications Commission (FCC) for the amount of radiation electronic devices may emit. Reradiation might jeopardize the marketability of the receiver if it were designed to be a product.

LO-IF feedthrough, as shown in Fig. 3.9b, is usually not that problematic because the gain of the mixer will boost the RF signal to levels comparable, if not higher, than the LO leakage. In addition, filtering after the mixer should be sufficient to attenuate most of the LO leakage. Note however that passive mixers, which will be discussed in greater detail in the next chapter, do not have gain and rely solely on the filtering to attenuate LO leakage.

Finally, RF-IF feedthrough is the leakage of the RF signal to the IF port of the mixer. Since the RF signal is typically small, this type of feedthrough is usually negligible. Even for the case of passive mixers where the IF component may be less than the RF component, the high-frequency RF should be outside the passband of any filter that follows the mixer.

APPENDIX

A.3.1 FOURIER SERIES EXPANSION OF A SQUARE WAVE

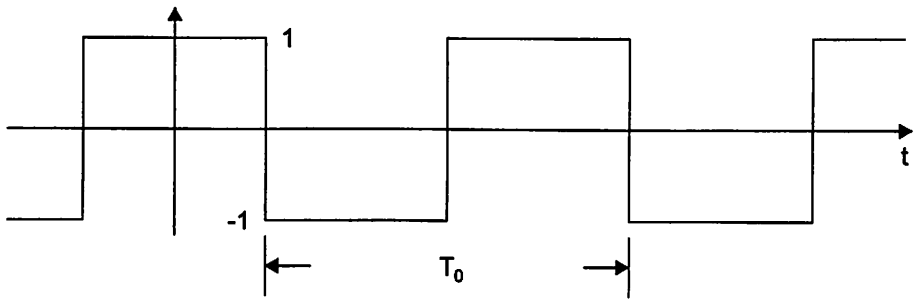


Figure 3.10 Ideal square wave.

We will consider the zero-mean square wave shown in Fig. 3.10. Since this is an even function, we can express this periodic function, $f(t)$, as a sum of cosine terms.

$$f(t) = \sum_{n=1}^{\infty} a_n \cos n\omega_0 t \tag{3.32}$$

The coefficients of the Fourier cosine series are found by,

$$a_n = \frac{2}{T_0}\int_0^{T_0} f(t)\cos n\omega_0 t\, dt, \quad \text{for } n \neq 0 \tag{3.33}$$

$$= \frac{2}{T_0}\left(\int_0^{T_0/4} \cos n\omega_0 t\, dt - \int_{T_0/4}^{3T_0/4} \cos n\omega_0 t\, dt + \int_{3T_0/4}^{T_0} \cos n\omega_0 t\, dt\right) \tag{3.34}$$

$$= \frac{2}{T_0}\left(\frac{\sin n\omega_0 t}{n\omega_0}\bigg|_0^{T_0/4} - \frac{\sin n\omega_0 t}{n\omega_0}\bigg|_{T_0/4}^{3T_0/4} + \frac{\sin n\omega_0 t}{n\omega_0}\bigg|_{3T_0/4}^{T_0}\right) \tag{3.35}$$

$$= \frac{2}{n\pi}\left(\sin\frac{n\pi}{2} - \sin\frac{3n\pi}{2}\right) \tag{3.36}$$

$$= \begin{cases} \dfrac{4}{n\pi}, & \dfrac{n+1}{2} \text{ odd} \\ -\dfrac{4}{n\pi}, & \dfrac{n+1}{2} \text{ even} \\ 0, & n \text{ even} \end{cases} \tag{3.37}$$

Therefore, the Fourier series expansion of the even square wave is

$$\frac{4}{\pi}\left(\cos\omega_0 t - \frac{1}{3}\cos 3\omega_0 t + \frac{1}{5}\cos 5\omega_0 t - \ldots\right) \tag{3.38}$$

Shifting this result by $T_0/4$ will result in the Fourier sine series of the odd square wave,

$$\frac{4}{\pi}\left(\sin\omega_0 t + \frac{1}{3}\sin 3\omega_0 t + \frac{1}{5}\sin 5\omega_0 t + \ldots\right) \tag{3.39}$$

A.3.2 FOURIER SERIES EXPANSION OF A NON-IDEAL SQUARE WAVE

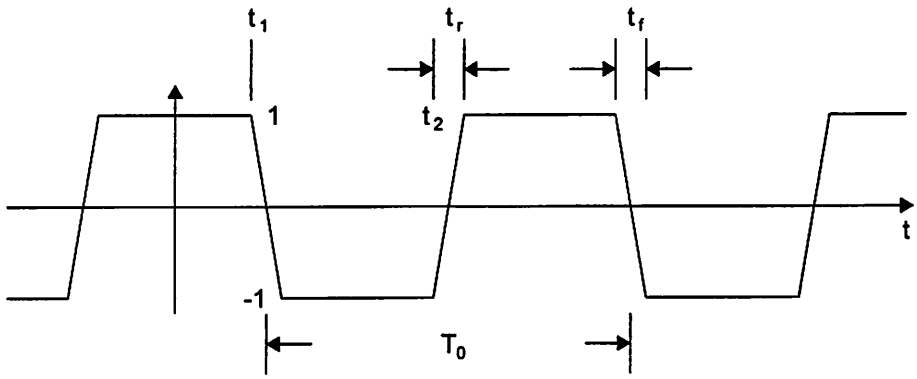


Figure 3.11 Nonideal square wave.

Now consider the nonideal square wave shown in Fig. 3.11. The Fourier series expansion of this periodic function will not be a simple sine or cosine series since it is neither an even nor odd function. Instead, we write the Fourier expansion,

$$f(t) = \sum_{n=-\infty}^{\infty} a_n e^{jn\omega_0 t} \tag{3.40}$$

For $f(t)$ real, a_{-n} is simply the complex conjugate of a_n. This is proved in [1]. Then combining positive and negative terms, we get

$$f(t) = a_0 + \sum_{n=1}^{\infty} 2\mathrm{Re}\left[a_n e^{jn\omega_0 t}\right] \tag{3.41}$$

$$= a_0 + \sum_{n=1}^{\infty} \left(2\mathrm{Re}\left[a_n\right]\cos n\omega_0 t - 2\mathrm{Im}\left[a_n\right]\sin n\omega_0 t\right) \tag{3.42}$$

indicating that calculating the coefficients of the complex Fourier case will give us real coefficients for a sum of sines and cosines. The complex coefficients are defined

by

$$a_n = \frac{1}{T_0}\int_0^{T_0} f(t)e^{-jn\omega_0 t}\,dt \tag{3.43}$$

$$\begin{aligned}
&= \frac{1}{T_0}\left(\int_0^{t_1} e^{-jn\omega_0 t}\,dt + \int_{t_1}^{t_1+t_f}\left(1+2\frac{t_1}{t_f}-2\frac{t}{t_f}\right)e^{-jn\omega_0 t}\,dt\right.\\
&- \int_{t_1+t_f}^{t_2} e^{-jn\omega_0 t}\,dt\\
&\left.+ \int_{t_2}^{t_2+t_r}\left(-1-2\frac{t_2}{t_r}+2\frac{t}{t_r}\right)e^{-jn\omega_0 t}\,dt + \int_{t_2+t_r}^{T_0} e^{-jn\omega_0 t}\,dt\right)
\end{aligned} \tag{3.44}$$

$$\begin{aligned}
&= \frac{1}{T_0}\left[\frac{1-e^{-jn\omega_0 t_1}+e^{-jn\omega_0 t_2}-e^{-jn\omega_0(t_1+t_f)}+e^{-jn\omega_0(t_2+t_r)}-1}{jn\omega_0}\right.\\
&+ \frac{\left(1+2\frac{t_2}{t_r}\right)\left(e^{-jn\omega_0(t_2+t_r)}-e^{-jn\omega_0 t_2}\right)+\left(1+2\frac{t_1}{t_f}\right)\left(e^{-jn\omega_0 t_1}-e^{-jn\omega_0(t_1+t_f)}\right)}{jn\omega_0}\\
&+ \frac{2}{t_f}\left(\frac{(t_1+t_f)e^{-jn\omega_0(t_1+t_f)}-t_1e^{-jn\omega_0 t_1}}{jn\omega_0}\right)+\frac{2}{t_f}\left(\frac{e^{-jn\omega_0 t_1}-e^{-jn\omega_0(t_1+t_f)}}{n^2\omega_0^2}\right)\\
&\left.+ \frac{2}{t_r}\left(\frac{t_2e^{-jn\omega_0 t_2}-(t_2+t_r)e^{-jn\omega_0(t_2+t_r)}}{jn\omega_0}\right)+\frac{2}{t_r}\left(\frac{e^{-jn\omega_0(t_2+t_r)}-e^{-jn\omega_0 t_2}}{n^2\omega_0^2}\right)\right]
\end{aligned} \tag{3.45}$$

Taking the real and imaginary parts, we get

$$\begin{aligned}
\mathrm{Re}\,[a_n] = \frac{1}{T_0}&\left[\frac{\sin n\omega_0 t_1-\sin n\omega_0 t_2+\sin n\omega_0(t_1+t_f)-\sin n\omega_0(t_2+t_r)}{n\omega_0}\right.\\
&+\frac{\left(1+2\frac{t_2}{t_r}\right)\left(\sin n\omega_0 t_2-\sin n\omega_0(t_2+t_r)\right)}{n\omega_0}\\
&+\frac{\left(1+2\frac{t_1}{t_f}\right)\left(\sin n\omega_0(t_1+t_f)-\sin n\omega_0 t_1\right)}{n\omega_0}\\
&+\frac{2}{t_f}\left(\frac{t_1\sin n\omega_0 t_1-(t_1+t_f)\sin n\omega_0(t_1+t_f)}{n\omega_0}\right)\\
&+\frac{2}{t_r}\left(\frac{(t_2+t_r)\sin n\omega_0(t_2+t_r)-t_2\sin n\omega_0 t_2}{n\omega_0}\right)\\
&+\frac{2}{t_f}\left(\frac{\cos n\omega_0 t_1-\cos n\omega_0(t_1+t_f)}{n^2\omega_0^2}\right)\\
&\left.+\frac{2}{t_r}\left(\frac{\cos n\omega_0(t_2+t_r)-\cos n\omega_0 t_2}{n^2\omega_0^2}\right)\right]
\end{aligned} \tag{3.46}$$

$$\mathrm{Im}\,[a_n] = \frac{1}{T_0}\left[\frac{\cos n\omega_0 t_1+\cos n\omega_0(t_1+t_f)-\cos n\omega_0 t_2-\cos n\omega_0(t_2+t_r)}{n\omega_0}\right.$$

$$+\frac{\left(1+2\frac{t_2}{t_r}\right)(\cos n\omega_0 t_2-\cos n\omega_0(t_2+t_r))}{n\omega_0}$$
$$+\frac{\left(1+2\frac{t_1}{t_f}\right)(\cos n\omega_0(t_1+t_f)-\cos n\omega_0 t_1)}{n\omega_0}$$
$$+\frac{2}{t_f}\left(\frac{t_1\cos n\omega_0 t_1-(t_1+t_f)\cos n\omega_0(t_1+t_f)}{n\omega_0}\right)$$
$$+\frac{2}{t_r}\left(\frac{(t_2+t_r)\cos n\omega_0(t_2+t_r)-t_2\cos n\omega_0 t_2}{n\omega_0}\right)$$
$$+\frac{2}{t_f}\left(\frac{\sin n\omega_0 t_1-\sin n\omega_0(t_1+t_f)}{n^2\omega_0^2}\right)$$
$$+\frac{2}{t_r}\left(\frac{\sin n\omega_0(t_2+t_r)-\sin n\omega_0 t_2}{n^2\omega_0^2}\right)\Bigg] \tag{3.47}$$

For $n=0$, we find the mean and get a_0. Despite the unwieldiness of these expressions, we can use (3.46) and (3.47) to find the Fourier series expansions of various types of waves without having to find the Fourier series expansion for each one.

For a triangle wave, we set $t_r=t_f=t_2=T_0/2$ and $t_1=0$. This gives

$$\mathrm{Re}\,[a_n]=\begin{cases}\frac{4T_0}{n^2\pi^2}, & n \text{ odd}\\ 0, & \text{otherwise}\end{cases} \tag{3.48}$$

$$\mathrm{Im}\,[a_n]=0 \tag{3.49}$$

For a 50 % duty cycle square wave with equal rise and fall times, we set $t_r=t_f$ with the times $t_1=T_0/4-t_r/2$ and $t_2=3T_0/4-t_r/2$. Plugging these conditions into (3.46) and (3.47), we get

$$\mathrm{Re}\,[a_n]=\begin{cases}\left(\frac{2}{n\pi}\right)(-1)^{\frac{n-1}{2}}\frac{\sin\left(\frac{n\pi t_r}{T_0}\right)}{\frac{n\pi t_r}{T_0}}, & n \text{ odd}\\ 0, & \text{otherwise}\end{cases} \tag{3.50}$$

$$\mathrm{Im}\,[a_n]=0 \tag{3.51}$$

To get the ideal square wave, simply set $t_r=t_f=0$ with $t_1=T_0/4$ and $t_2=3T_0/4$.

This results in

$$\mathrm{Re}\,[a_n] = \begin{cases} \left(\frac{2}{n\pi}\right)(-1)^{\frac{n-1}{2}}, & n \text{ odd} \\ 0, & \text{otherwise} \end{cases} \tag{3.52}$$

$$\mathrm{Im}\,[a_n] = 0 \tag{3.53}$$

This analysis was carried out in [17].

Chapter 4

Mixer Topologies

Designing a downconversion mixer, like any other block of the system, requires the careful examination and analysis of the wide range of existing circuit topologies. Part of the design phase entails understanding the choices made by other designers. As mixer designers, we must then create a circuit schematic based on our creativity and our ability to consolidate the benefits of other circuits into one working circuit that meets our design specifications. In this chapter, we will focus on introducing a few different CMOS downconversion mixer circuits which have been proposed in the past. Tradeoffs between the circuits will be explained with bias towards their application to indoor wireless receivers. A detailed analysis of two particular mixers will also be presented.

4.1 Passive Mixers

Passive mixers are mixers that cannot provide power gain by virtue of their circuit topology. Whereas a poor design of an active mixer may provide loss, no good passive design can ever have conversion gain. Hence, a more appropriate metric used for passive mixers is conversion loss.

4.1.1 Passive Switching Mixers

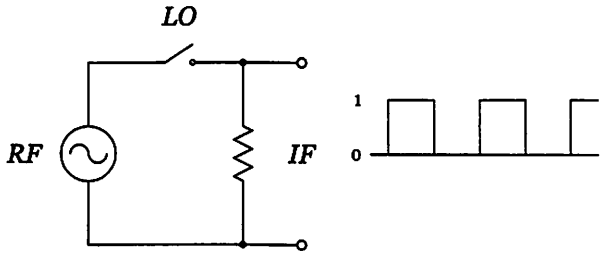


Figure 4.1 Basic switching mixer.

As mentioned in previous chapters, mixers are basically multipliers. The RF input is multiplied with a periodic signal of the same frequency as the LO. Hence, a switch toggling at the LO frequency, as shown in Fig. 4.1, can be a mixer. The RF input is multiplied by a square wave to get the IF output. The square wave is unity for the conducting half of the period, and zero otherwise. Another version of the switching mixer multiplies the RF signal with a bipolar square wave as shown in Fig. 4.2. These mixers are called balanced, or single-balanced, because of the differential nature of one of the ports, in this case the RF port.[1] Similarly, balancing both RF and LO ports will make a mixer double-balanced.

It can easily be seen that any electronically controlled switch, such as a diode, could be used in place of a mechanical switch to make a switching mixer. An example of a double-balanced diode mixer is shown in Fig. 4.3.

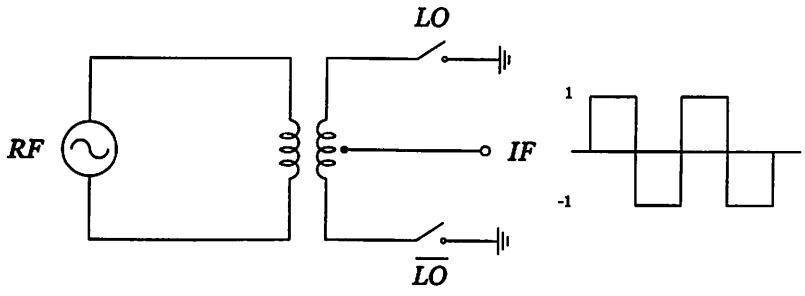


Figure 4.2 Balanced switching mixer.

[1] The LO port is unbalanced since we assume that the switch toggles at some trigger voltage.

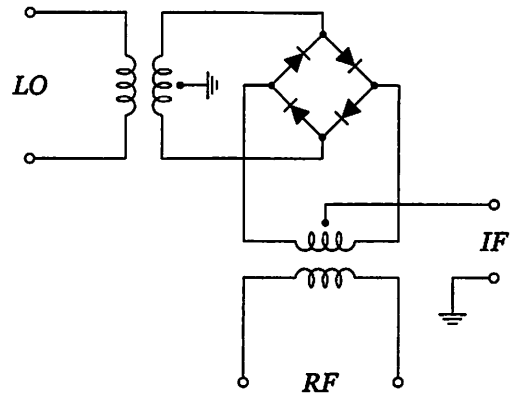


Figure 4.3 Double-balanced diode ring mixer.

Of all the switching topologies, the double-balanced mixer appears most desirable for a monolithic implementation because of its immunity to common-mode variations. Mixer operation depends only on the differential signals on both ports, thus preventing "digital noise," coupled through the substrate, from affecting the integrity of the mixer's output. The higher component count in the double-balanced mixer is not an issue for on-chip mixers because the fabrication cost is fixed, and independent of the number of devices used.

However, the transformers used in the diode ring mixer of Fig. 4.3 may be problematic in single-chip implementations. Monolithic transformers, like inductors, are difficult to design with because of the high resistive losses in the windings. Poor coupling between windings also result in larger losses from the primary to secondary sections. A CMOS version of the double-balanced mixer is needed. By realizing the

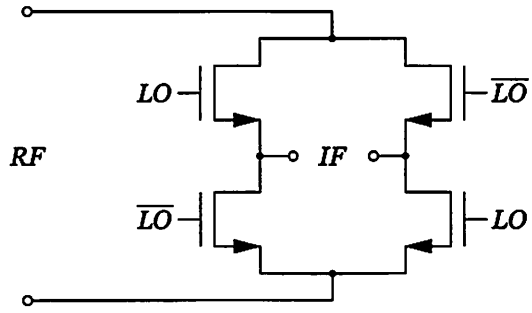


Figure 4.4 CMOS double-balanced mixer.

switches with gated MOSFETs, we can derive a CMOS version of the double-balanced diode mixer as shown in Fig. 4.4. Further analysis of this switching mixer will follow in a future section.

4.1.2 Passive Linear Mixers

Another type of passive mixer based on a slightly different technique to achieve mixing is the linear mixer shown in Fig. 4.5. Instead of operating the MOS transistor as a switch in either the "on" or "off" state, the MOSFETs are operated in the linear region. The RF signal modulates the gate of the input transistors, thus varying the channel resistance, which essentially multiplies the RF signal with the drain-source voltage. Since the input transistors operate in the linear region, the linearity performance of this mixer significantly outperforms that of switching mixers.

Noise performance, however, suffers due to the active gain block needed to compensate for the large conversion loss of the first half of the mixer. In addition, the

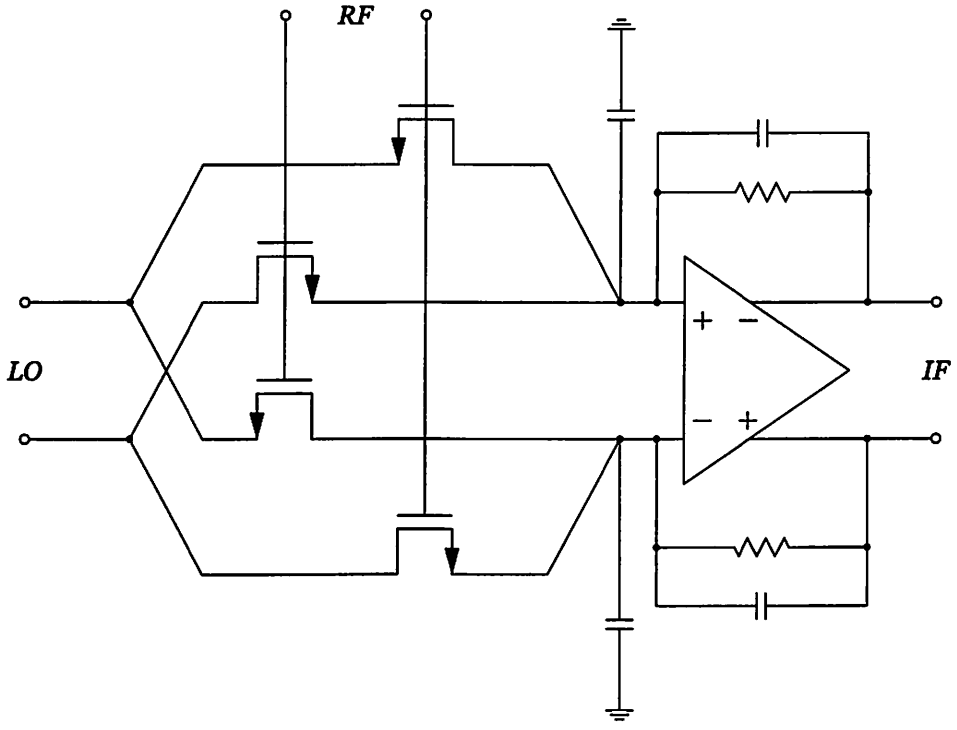


Figure 4.5 Super linear passive mixer.

input transistors used to perform the mixing also contribute significant noise to the mixer's output. Since noise is proportional to resistance in the triode region, reducing noise would require increasing the size of the transistors or driving the transistors with a larger gate voltage. Unfortunately, the RF signal is usually small, and increasing device sizes would only increase the LO power consumption, as the LO signal now needs to drive a larger input capacitance. A more detailed analysis of this mixer is presented in [15].

To fully understand the tradeoffs in implementing a certain mixer topology, we would have to analyze them in great detail. However, analyzing every existing topology would be very prohibitive, hence only one will be considered.

4.2 Analysis of the CMOS Passive Switching Mixer

We will consider the CMOS double-balanced switching mixer, or commutating mixer as it is sometimes called. The basic elements that perform the mixing are shown in Fig. 4.6. Two different analyses of the conversion gain of this mixer will be presented in the following sections.

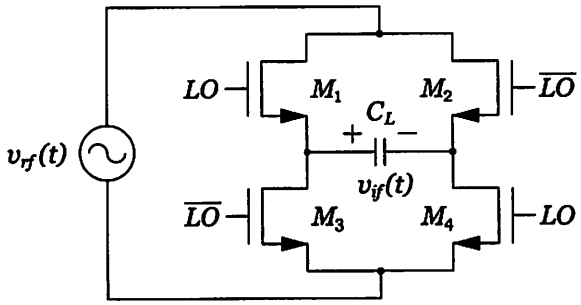


Figure 4.6 Passive CMOS mixer.

4.2.1 Conversion Gain Using the Method of Time-Varying Conductances

Modeling the transistors as time-varying conductances, we simplify the schematic as shown in Fig. 4.7a. Then we can find the Thevenin equivalent circuit as shown in Fig. 4.7b.

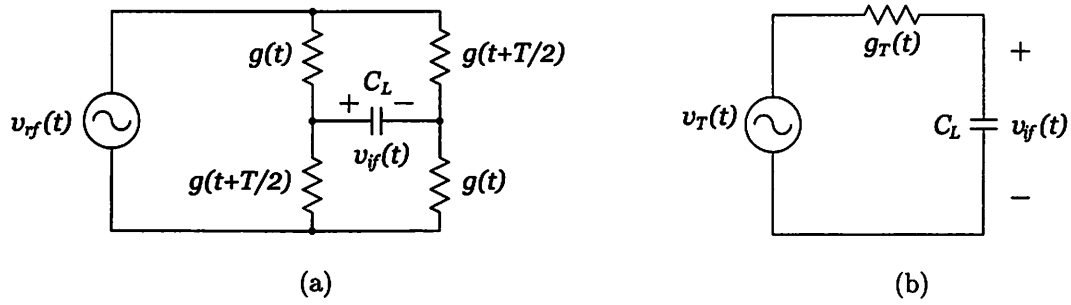


Figure 4.7 (a) Equivalent circuit with time-varying resistors. (b) Thevenin equivalent with mixing source.

In Fig. 4.7b, v_T and g_T are defined by

$$v_T(t) = m(t)v_{rf}(t) \tag{4.1}$$

where

$$m(t) = \frac{g(t) - g(t+T/2)}{g(t) + g(t+T/2)} \tag{4.2}$$

and

$$g_T(t) = \frac{g(t) + g(t+T/2)}{2} \tag{4.3}$$

The current through the capacitor is

$$C_L v_{if}(t)' = g_T(t)\left(v_T(t) - v_{if}(t)\right) \tag{4.4}$$

Rearranging (4.4) gives

$$v_{if}(t)' + \frac{g_T(t)}{C_L} v_{if}(t) = \frac{g_T(t)}{C_L} v_T(t) \tag{4.5}$$

Now, we define

$$P(t) \triangleq \int_{-\infty}^{t} \frac{g_T(x)}{C_L}\, dx \tag{4.6}$$

$$P'(t) = \frac{g_T(t)}{C_L} \tag{4.7}$$

These definitions facilitate the solution of the differential equation by allowing us to define an integrating factor. Multiplying (4.5) by the integrating factor, we get

$$e^P v_{if}' + e^P P' v_{if} = \left(e^P v_{if}\right)' = e^P \frac{g_T}{C_L} v_T \tag{4.8}$$

Then,

$$e^P v_{if}\Big|_{-\infty}^{t} = \int_{-\infty}^{t} \frac{g_T(\tau)}{C_L} e^{P(\tau)} v_T(\tau)\, d\tau \tag{4.9}$$

so, for $v_{if}(-\infty) = 0$,

$$v_{if}(t) = \int_{-\infty}^{t} \frac{g_T(\tau)}{C_L} e^{-\int_{\tau}^{t} \frac{g_T(s)}{C_L} ds} v_T(\tau)\, d\tau \tag{4.10}$$

Since $g_T(t)$ is periodic, we can try to write it down as a Fourier series. We note from (4.3) that $g_T(t)$ has period $T/2$, hence $g_T(t)$ can be expanded as

$$g_T(t) = \overline{g_T} + \sum_{n=1}^{\infty} (a_n \cos 2n\omega_0 t + b_n \sin 2n\omega_0 t) \tag{4.11}$$

Then,

$$\int_{\tau}^{t} \frac{g_T(s)}{C_L} ds = \frac{\overline{g_T}(t-\tau)}{C_L} + \frac{\overline{g_T}}{2\omega_0 C_L} \left[\sum_{n=1}^{\infty} \frac{1}{n\overline{g_T}} (a_n \sin 2n\omega_0 t - b_n \cos 2n\omega_0 t) \right]_{\tau}^{t} \tag{4.12}$$

The second term in (4.12) contains a prefactor of $\overline{g_T}/2\omega_0 C_L$ multiplied by a normalized series of sines and cosines.

When $\overline{g_T} \ll 2\omega_0 C_L$, the second term of (4.12) may be neglected, permitting the approximation,

$$v_{if}(t) \approx \int_{-\infty}^{t} \frac{g_T(\tau)}{C_L} e^{-\frac{\overline{g_T}(t-\tau)}{C_L}} v_T(\tau)\, d\tau \tag{4.13}$$

$$= \int_{-\infty}^{t} \frac{\overline{g_T}}{C_L} e^{-\frac{\overline{g_T}(t-\tau)}{C_L}} \frac{g_{Tmax}}{\overline{g_T}} \frac{g_T(\tau)}{g_{Tmax}} m(\tau) v_{rf}(\tau)\, d\tau \tag{4.14}$$

where the terms in (4.14) were rearranged to highlight the equivalent block diagram of Fig. 4.8. We now assume the conductance is proportional to $V_{gs} - V_t$ when the transistor is "on," and zero when the transistor is "off." From (4.2) and (4.3), LO waveforms biased about the threshold voltage, V_t, will result in normalized mixing functions, $m(t)g_T(t)/g_{Tmax}$, of the same waveform but with unit amplitude.

From Fig. 4.8, the conversion gain of the switching CMOS mixer with sinusoidal LO waveform is

$$A_{sine} = \frac{1}{2} \frac{g_{Tmax}}{\overline{g_T}} \tag{4.15}$$

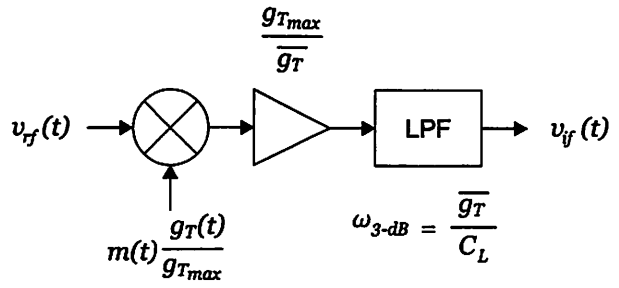


Figure 4.8 Equivalent block diagram of the passive CMOS commutating mixer.

Using the simple square law model for the MOSFET, the conductance is

$$g(V) = \mu C_{ox} \frac{W}{L} (V - V_t) \tag{4.16}$$

From (4.3), we get

$$g_{Tmax} = \frac{\mu C_{ox}}{2} \frac{W}{L} V_{LO} \tag{4.17}$$

$$\overline{g_T} = \frac{\mu C_{ox}}{2} \frac{W}{L} \frac{2}{\pi} V_{LO} \tag{4.18}$$

where V_{LO} is the amplitude of the LO waveform. Therefore,

$$A_{sine} = \frac{\pi}{4} \tag{4.19}$$

Similarly, for a square wave, the conversion gain is given by

$$A_{square} = \frac{2}{\pi} \frac{g_{Tmax}}{\overline{g_T}} = \frac{2}{\pi} \tag{4.20}$$

where

$$g_{Tmax} = \overline{g_T} = \frac{\mu C_{ox}}{2} \frac{W}{L} V_{LO} \tag{4.21}$$

When $\overline{g_T} \gg 2\omega_0 C_L$, the circuit degenerates to the switching mixer with open-circuited load. This results in the conversion gain

$$A = \frac{2}{\pi} \tag{4.22}$$

for all possible LO waveforms biased about V_t. This result was derived in (3.12).

When $\overline{g_T}$ is comparable to $2\omega_0 C_L$, the integral (4.10) cannot easily be evaluated. Hence, this analysis does not apply to this case.

This analysis of the CMOS passive switching mixer can be found in [12].

4.2.2 Conversion Gain Using the EKV Model

Despite the fact that we used the square-law model to calculate the time-varying conductances in the previous section, the analysis is still valid for any MOS model, provided we can find an expression for the conductance which is independent of $v_{if}(t)$. Unfortunately, the more advanced MOS models usually depend strongly of the terminal voltages of the device, making it seem unlikely that we can find an expression for $g(t)$ which is independent of $v_{if}(t)$. Also, finding the time-varying conductance of the MOS transistor when the gate voltage is below the threshold may be tricky due to the highly nonlinear nature of the MOSFET in the subthreshold region. Are we then stuck with the results given by the square-law model?

Fortunately, a simpler solution to analyzing the complicated MOS transistor in several different regions exists. We can get relatively simple expressions for the current through the MOSFET without sacrificing too much accuracy if we use interpolation models. Interpolation models are equations formulated to match certain data while maintaining simplicity in the overall expression. They are not entirely derived from physical laws, but may consist of several physical equations pieced together. Interpolation models were created to provide accurate models for design, hence are a tradeoff between the simplicity of basic models for a large increase in accuracy.

One interpolation model described in [21] which seems appropriate to use for the double-balanced CMOS mixer is the EKV model. The large-signal current equation for the EKV model is

$$I_{ds} = \mu C_{ox}\frac{W}{L}(2n)\phi_t^2\left(\ln^2\left(1+e^{\frac{V_P-V_{SB}}{2\phi_t}}\right)-\ln^2\left(1+e^{\frac{V_P-V_{DB}}{2\phi_t}}\right)\right) \tag{4.23}$$

where

$$V_P = \frac{V_{GB}-V_t}{n} \tag{4.24}$$

$$n = 1+\chi \tag{4.25}$$

and ϕ_t is the thermal voltage, χ the body-effect factor. Notice from (4.23) that the source and drain of the MOS transistor are interchangeable (up to a sign). Thus, this

equation is of particular interest to the double-balanced CMOS mixer since current flowing through the switches is changing directions frequently. In addition, this model is valid in the strong, moderate, and weak inversion regions.

Using (4.23), we can analyze the CMOS double-balanced mixer once more, this time including the effects of entering and exiting the subthreshold region as the LO signal swings. Rather than take the approach of a time-varying conductance, we use the EKV model and KCL to formulate a differential equation. This ODE will be nonlinear and difficult to solve, but we can make some approximations to recast it into the form of (4.14). After that, we can find the equivalent block diagram shown in Fig. 4.9. This derivation is carried out in the appendix.

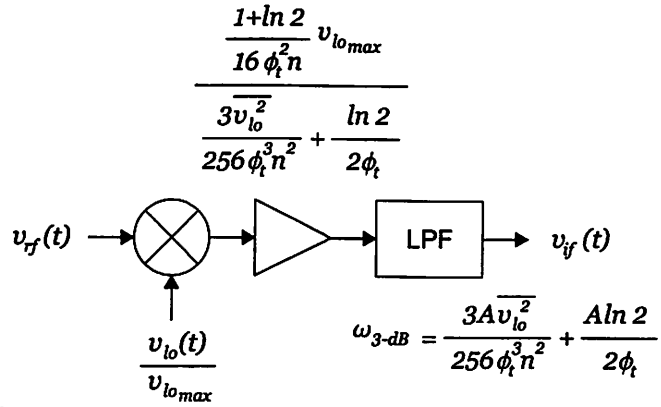


Figure 4.9 Equivalent block diagram of the CMOS double-balanced switching mixer derived using the EKV model.

Immediately, we see how the complexity of the expressions have increased from Fig. 4.8. We also notice that the conversion gain predicted by this model depends on the amplitude of the LO signal, unlike what was found in (4.19) and (4.20). However, as will be explained in the appendix, Fig. 4.9 is valid only for LO amplitudes of about 250 mV. This makes it useful for low-power applications which restrict the amplitudes of the LO signal to minimize power consumption.

4.2.3 Linearity, Noise, Port Isolation

The linearity performance of this double-balanced mixer depends strongly on how large the LO signal drives the MOS switches. Larger LO signals drive the switches

out of the highly nonlinear subthreshold region into the linear region much quicker than smaller LO signals. In addition, increasing switch sizes also increase the linearity of the mixer.

The noise in this passive mixer is dominated by thermal noise. Because of the alternating current flowing through the switches, no flicker noise is generated. However, note that with mismatch, a steady current might flow if the switches are not completely turned "off," resulting in some flicker noise.

Port-to-port isolation however is poor for the passive mixer. The LO signal couples in to both the RF and IF port through the gate capacitance of each switch. Larger switches lead to larger capacitances, which in turn increase the amount of feedthrough from the LO port to the other ports. Similarly, larger LO switches increase the amount of charge injected into the signal path. Hence, this mixer is prone to self-mixing and large DC offsets. Other offset reducing techniques must be employed if this mixer is to be used in a homodyne system.

With a direct path between RF and IF ports, the high-frequency RF signal can also feed straight through to the IF output if the mixer is not balanced properly. Any mismatch could result in some common-mode term in the mixing function, $m(t)$, permitting feedthrough. However, as mentioned in a previous chapter, this may not be a problem because of the filtering at the IF port. This mixer topology has a built-in single-pole lowpass filter at the output as shown in Fig. 4.8 and Fig. 4.9.

4.3 Active Mixers

Unlike passive mixers, active mixers have the ability to provide gain. As a result, most receivers use active mixers. The gain provided by the active mixer lessens the gain requirements of other blocks in the receiver chain. Passive mixers, on the other hand, have loss which increases the gain requirements of the other blocks. Hence, the use of passive mixers has been minimized in aggressive designs, and has been limited to really high frequency systems where the active devices can no longer provide gain. However, as will be discussed later, passive mixers are making a comeback in receiver design because of their zero power consumption.

4.3.1 FET Mixers

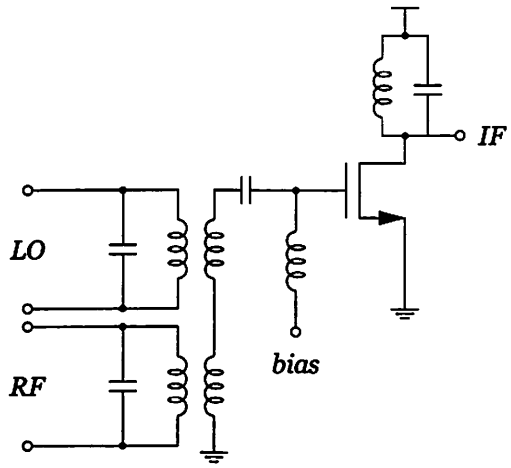


Figure 4.10 CMOS FET mixer.

One type of active mixer is the FET mixer. As described in [19], this circuit is first driven by the large LO signal to set up the natural frequency of the circuit. The small RF signal then acts linearly on the forced circuit to produce sum and difference frequency terms, hence mixing down to IF as in (3.6). A problem with these mixers in monolithic implementations is their need for on-chip transformers.

4.3.2 Gilbert Mixers

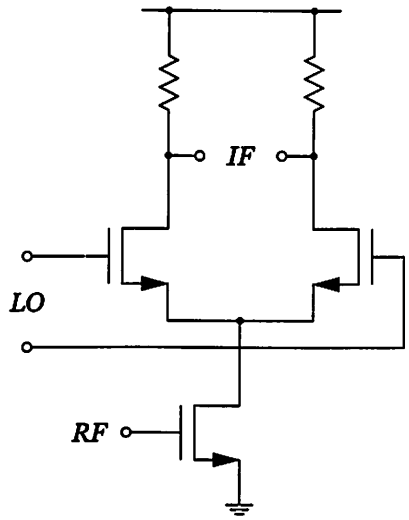


Figure 4.11 Single-balanced Gilbert mixer.

Another type of active mixer is the Gilbert mixer. This is probably the most common mixer circuit used in receivers. The basic Gilbert mixer consists of a differential pair controlled by the LO which switches its tail current back and forth between two loads. The tail current is modulated by the RF signal, thus multiplying the RF signal by the mixing function as in Fig. 4.1. Therefore, the Gilbert mixer is a switching mixer, or sometimes referred to as a commutating mixer or Gilbert quad. Like the passive switching mixer, there are balanced Gilbert mixers. A differential-output single-balanced Gilbert mixer is shown in Fig. 4.11. The double-balanced version is shown in Fig. 4.12.

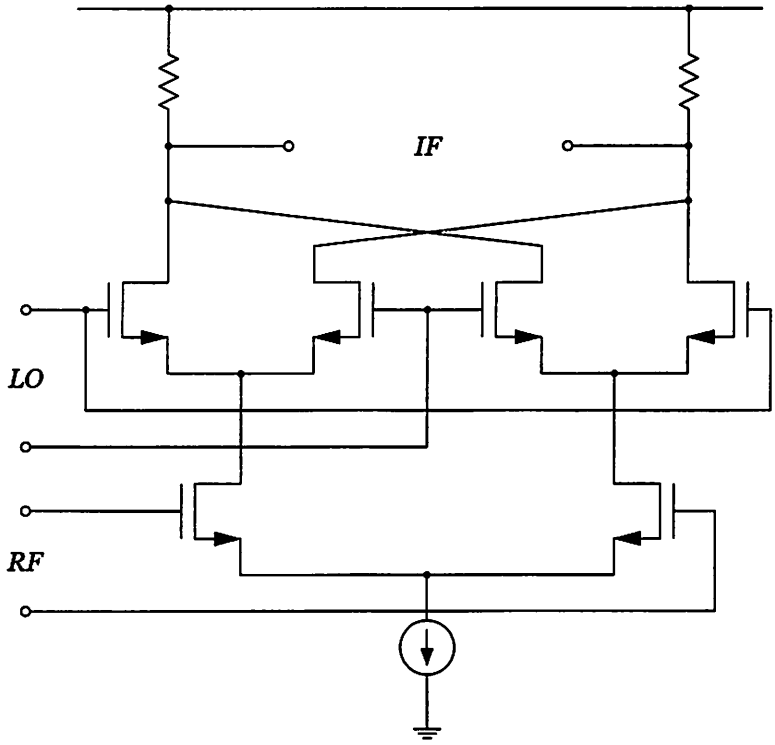


Figure 4.12 Double-balanced Gilbert mixer.

There is, however, one difference between the operations of the Gilbert mixer and the passive switching mixer. The transistors in the switching differential pair of the Gilbert mixer do not have to be driven fully to the hard "on" or "off" states. Because these transistors are connected in the differential configuration, the amount of current switched from one leg to the other depends only on the difference between

the voltages on the gates. From [5], we find that over 90% of the current switches when the LO signal is greater than $\sqrt{2}\,V_{dsat3}$.

4.4 Analysis of the CMOS Gilbert Mixer

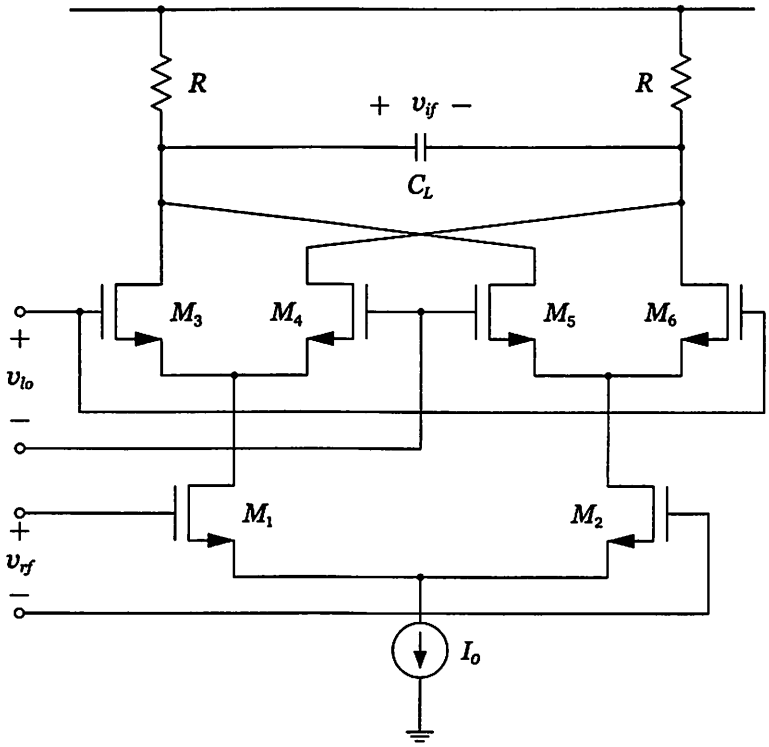


Figure 4.13 Gilbert quad.

In this section, we will focus on the analysis of the CMOS Gilbert switching mixer. This particular mixer has great applicability in low-power wireless research since it can easily be implemented in an integrated environment where analog and digital circuits coexist on the same chip. The circuit is fully differential allowing a greater level of insensitivity to common-mode noise coming from the digital domain. Moreover, no inductors or transformers are needed to perform mixing, relaxing area requirements.

4.4.1 Conversion Gain

The small-signal tail current for the upper differential pair is $g_{m1}v_{rf}$. If the differential LO amplitude is larger than $\sqrt{2}\,V_{dsat3}$, this tail current will be switched back and forth

between the two resistors with a bipolar square wave mixing function. Hence, the conversion gain for the double-balanced Gilbert mixer is

$$A_v = \frac{2}{\pi} \frac{g_{m1} R}{1 + 2sRC_L} \tag{4.26}$$

However, the current through the LO diff-pair does not switch from one branch to the other instantaneously. Instead, the current in one branch slowly decreases as the current in the other branch increases. Both branches conduct equal amounts of current when the differential LO voltage is zero. Assuming the long-channel model for the MOS transistors, the differential current can be found in [19] and is described by

$$I_3 - I_4 = \frac{\mu C_{ox}}{2} \frac{W}{L} v_{lo} \sqrt{\frac{2I_0}{\frac{\mu C_{ox}}{2} \frac{W}{L}} - v_{lo}^2} \tag{4.27}$$

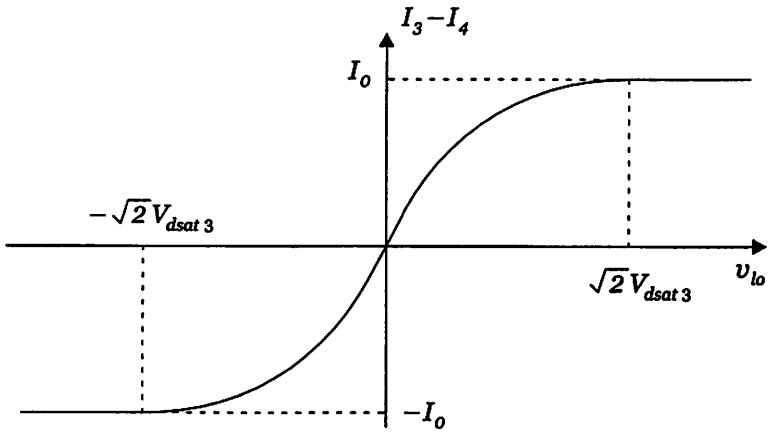


Figure 4.14 Transfer characteristic of a MOS differential pair.

Hence, from Fig. 4.14, we see that if the amplitude of v_{lo} is much larger than $\sqrt{2}V_{dsat3}$, the differential pair will switch very quickly and $|I_3 - I_4| < I_0$ only for a short period of time. We can then represent the mixing function as a "square" wave with finite rise and fall times. Then from (3.13), we get

$$A_v = \frac{2}{\pi} \frac{\sin\left(w_0 \frac{t_s}{2}\right)}{w_0 \frac{t_s}{2}} \frac{g_{m1} R}{1 + 2sRC_L} \tag{4.28}$$

where t_s is the rise/fall time of the mixing function, and w_0 is the LO frequency.

When the amplitude of v_{lo} is large compared to $\sqrt{2}V_{dsat3}$, we can make the additional approximation for sinusoidal LO drives,

$$v_{lo}(t) = A_{LO}\sin(w_0 t) \approx A_{LO}w_0 t \tag{4.29}$$

Then finding t_s becomes

$$\sqrt{2}V_{dsat3} = A_{LO}w_0\frac{t_s}{2} \tag{4.30}$$

which gives

$$t_s = \frac{2\sqrt{2}V_{dsat3}}{A_{LO}w_0} \tag{4.31}$$

Using sine instead of cosine in the above approximation is fine since we are only after the value of t_s. Plugging (4.31) into (4.28), we get

$$A_v = \frac{2}{\pi}\left(1 - \frac{1}{3}\left(\frac{V_{dsat3}}{A_{LO}}\right)^2\right)\frac{g_{m1}R}{1+2sRC_L} \tag{4.32}$$

From (4.32), we see that increasing the LO amplitude increases the conversion gain, as does decreasing V_{dsat3}. There is a built-in first-order lowpass filter with corner frequency $\omega_{3\text{-}dB} = 1/2RC_L$. A similar analysis is presented in [13].

Notice that square wave LO waveforms switch instantaneously leading to the conversion gain given in (4.26).

For short-channel MOS transistors, the short-channel g_m should be used, as derived in the appendix.

4.4.2 Linearity

To minimize distortion in the input differential pair of the Gilbert mixer, we should decrease the channel lengths of the transistors. As explained in the previous chapter, as the channel length of the MOS transistor decreases, it approaches the velocity saturation region at lower drain voltages, hence lower currents. Thus, the input differential pair will behave more linearly than the square-law model. This result was simulated and confirmed for a 0.25 μm process, as shown in Fig. 3.3.

Another possible source of nonlinearity is the load. Again, the previous chapter showed that larger channel lengths decrease distortion. This is due to the more abrupt transition from the linear to saturation region in shorter-channel transistors. As a result, we should design our MOSFET loads with larger lengths.

Wireless communications systems usually specify the linearity requirements in terms of the 1-dB compression point. This can be related to the other distortion measurements [7].

Another form of nonlinearity which is occasionally overlooked is the maximum signal level that can be handled before clipping. To maximize this level, amplifier and mixer outputs are usually biased at the point which allows the maximum signal swing. However, this is not always possible if the mixer or amplifier is designed to DC couple into a previous block. In the Gilbert mixer, it is obvious that the larger we make the bias on the LO switches, the smaller the swing we will get at the output. The tradeoff here is between a smaller signal level and the overhead of adding some interconnect circuitry between the frequency synthesizer and the mixer.

4.4.3 Noise

We see that there are two main types of noise in a CMOS Gilbert mixer. These are the flicker noise at low frequencies and the white thermal noise. The three main sources of noise are the input differential pair, the LO switches, and the load.

The contribution to the output noise spectral density due to the input differential pair is

$$S_{o12}(f) = 4 \times 4kT\gamma \left(\frac{1}{g_{m1}} \left(\frac{g_{m1}}{1 + g_{m1}/g_{m2}} \right)^2 + \frac{1}{g_{m2}} \left(\frac{g_{m2}}{1 + g_{m2}/g_{m1}} \right)^2 \right) \quad (4.33)$$

$$= 16kT\gamma \left(\frac{g_{m1}g_{m2}}{g_{m1} + g_{m2}} \right) \quad (4.34)$$

$$= 8kT\gamma g_{m1} \quad (4.35)$$

where γ is 2/3 for long-channel devices, and greater than 1 for shorter-channel transistors because of noise enhancement, as shown in (3.30). The factor of 4 in (4.33) is due to the correlation of one source's noise in both branches. We get (4.35) if

the input devices are matched, which is how they are usually designed. We neglect the flicker noise due to the input differential pair since it will be upconverted at the output.

Similarly, when both switches in each of the upper differential pairs is conducting (when current is switching from one branch to the other), the LO switches contribute thermal noise like a differential pair, which is given by

$$S_{osw,th}(f) = 2 \times 8kT\gamma g_{m3} \tag{4.36}$$

$$= 16kT\gamma g_{m3} \tag{4.37}$$

The factor of 2 appears since there are two pairs of switches. In addition to thermal noise, the LO switches also add flicker noise directly to the output.

$$S_{osw,fl}(f) = 4 \times \frac{K_f}{WLC_{ox}f} g_{m3}^2 \tag{4.38}$$

The total output noise spectral density due to the LO switches is then

$$S_{osw}(f) = S_{osw,th}(f) + S_{osw,fl}(f) \tag{4.39}$$

This noise is added directly to the output when the switches are commutating current. However, when the switches are fully conducting current in one direction, as is the case when $v_{lo} > \sqrt{2}\,V_{dsat3}$, the LO switches behave like cascode transistors, and their noise may be neglected. To take this into account, some averaging over the period of the LO may be done. Hence, we see that larger LO swings are better for the noise performance since it minimizes the amount of noise the LO switches contribute to the overall noise of the system.

The load's noise adds directly to the output, and is simply given by

$$S_{oload}(f) = 2 \times 4kTR \tag{4.40}$$

A more complete analysis of the noise in a CMOS commutating mixer can be found in [16].

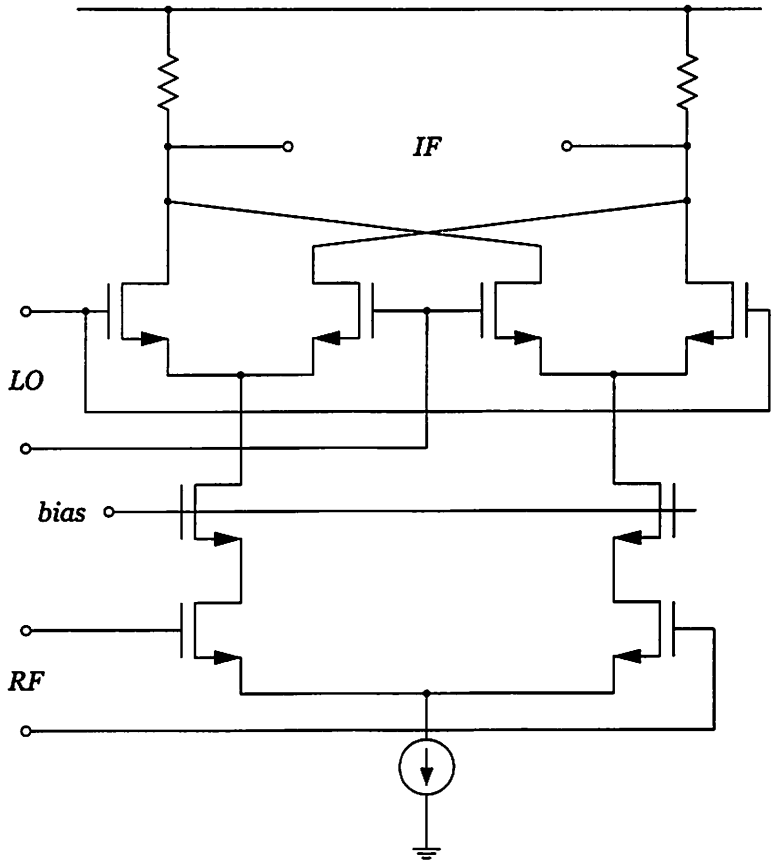


Figure 4.15 Gilbert mixer with cascode.

4.4.4 Port Isolation

The LO-IF feedthrough is determined by the gate-drain capacitance, and is given by

$$A_{LO\text{-}IF} \approx A_{LO}\frac{C_{gd_3}}{C_{gd_3} + 2C_L} \tag{4.41}$$

which is just the capacitive voltage divider equation. This expression is only an approximation since there is some resistance in parallel with the load capacitance. From (4.41), we see that increasing the load capacitance helps in reducing the amount of LO-IF feedthrough at the expense of lowering the pole of the filter at the output. A good strategy, in this case, would be to maximize the capacitance to push the single pole close to the band edge of the signal.

The LO-RF feedthrough is limited somewhat by the "distance" that the LO signal has to travel to get to the RF ports, through C_{gs_3} then C_{gd_1}. This isolation is much

better than that provided by the passive double-balanced mixer. However, because LO-RF rejection is important for self-mixing reasons, we may wish to further reduce this feedthrough. This can be accomplished by inserting a cascode transistor as in Fig. 4.15.

4.5 Choosing a Mixer

In this chapter, we presented several different mixer topologies to illustrate the design process that a mixer designer might go through. Various performance metrics were addressed in several short analyses in an attempt to understand the elements that determine the performance in a mixer.

Other types of mixers could have been considered. In order to reduce power, mixing could have been achieved with a higher harmonic of the LO, leading to the design of subharmonic mixers. Higher harmonics, however, are usually smaller than the fundamental, hence might not be a benefit in terms of power.

As mentioned before, choosing a mixer topology depends strongly on the application and the environment in which the mixer will reside. For indoor wireless applications using a CMOS process, we decided on the use of a double-balanced mixer. The double-balanced mixer provides a significant increase in insensitivity to common-mode variations, such as the unwanted noise coupling through the substrate. Of all the double-balanced CMOS mixers, we considered the passive switching mixer, and the Gilbert commutating mixer. Despite the loss of the passive mixer, its advantage is the absence of flicker noise and the zero power consumption. The Gilbert mixer, on the other hand, provides gain along with better rejection.

Another widely viewed advantage of passive mixers is their higher linearity compared to active mixers. However, an open research topic questions whether overdriving the LO switches in active mixers or increasing switch sizes would result in the linearity of active mixers being comparable to those of passive mixers. Similarly, would reducing the switch sizes in a passive mixer lead to acceptable distortion levels while providing less of a load to the LO buffer (or frequency synthesizer), in hopes of reducing power?

APPENDIX

A.4.1 CONVERSION GAIN USING THE EKV MODEL

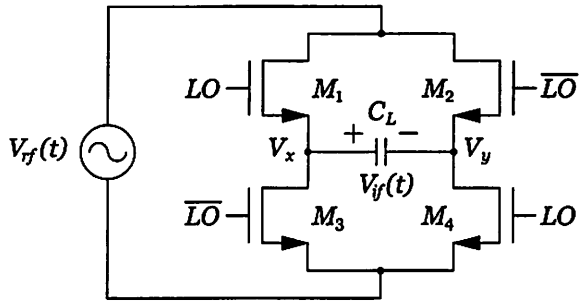


Figure 4.16 CMOS passive switching mixer.

The passive switching mixer is shown in Fig. 4.16. For convenience, the curve-fitted current equation described by the EKV model is repeated here.

$$I_{ds} = \mu C_{ox}\frac{W}{L}(2n)\phi_t^2\left(\ln^2\left(1+e^{\frac{V_P - V_{SB}}{2\phi_t}}\right) - \ln^2\left(1+e^{\frac{V_P - V_{DB}}{2\phi_t}}\right)\right) \tag{4.42}$$

where

$$V_P = \frac{V_{GB} - V_t}{n} \tag{4.43}$$

$$n = 1 + \chi \tag{4.44}$$

Following the analysis of the simplified model which used the square-law current equation, we write

$$\begin{aligned} C_L v_{if}{}' = {} & \mu C_{ox}\frac{W}{L}(2n)\phi_t^2 \\ & \times \left(\ln^2\left(1+e^{\frac{V_{lo} - nV_x - V_t}{2n\phi_t}}\right) - \ln^2\left(1+e^{\frac{V_{lo} - nV_{rf} - V_t}{2n\phi_t}}\right)\right. \\ & \left. + \ln^2\left(1+e^{\frac{V_{\overline{lo}} - nV_x - V_t}{2n\phi_t}}\right) - \ln^2\left(1+e^{\frac{V_{\overline{lo}} - nV_{\overline{rf}} - V_t}{2n\phi_t}}\right)\right) \end{aligned} \tag{4.45}$$

where

$$V_{lo} = V_{LO} + \frac{v_{lo}}{2} \tag{4.46}$$

$$V_{\overline{lo}} = V_{LO} - \frac{v_{lo}}{2} \tag{4.47}$$

$$V_{rf} = V_{RF} + \frac{v_{rf}}{2} \tag{4.48}$$

$$V_{\overline{rf}} = V_{RF} - \frac{v_{rf}}{2} \tag{4.49}$$

$$V_x = V_{IF} + \frac{v_{if}}{2} \tag{4.50}$$

$$V_y = V_{IF} - \frac{v_{if}}{2} \tag{4.51}$$

Now we define

$$\frac{V_C}{2} = V_{LO} - nV_{RF} - V_t \tag{4.52}$$

We now note that the voltage swing of V_{if} lies inside the voltage swing of V_{rf}. In addition, since the RF signal is assumed small, we can safely assume that the IF signal will also be small and

$$V_{IF} \approx V_{RF} \tag{4.53}$$

Hence, rewriting (4.45), we get

$$\begin{aligned} I_{if} \approx\ & \mu C_{ox} \frac{W}{L} (2n) \phi_t^2 \\ & \times \left(\ln^2 \left(1 + e^{\frac{v_{lo} - nv_{if} + V_C}{4n\phi_t}} \right) - \ln^2 \left(1 + e^{\frac{v_{lo} - nv_{rf} + V_C}{4n\phi_t}} \right) \right. \\ & \left. + \ln^2 \left(1 + e^{\frac{-v_{lo} - nv_{if} + V_C}{4n\phi_t}} \right) - \ln^2 \left(1 + e^{\frac{-v_{lo} + nv_{rf} + V_C}{4n\phi_t}} \right) \right) \end{aligned} \tag{4.54}$$

This nonlinear ODE looks daunting and may not even have a simple closed form solution. Rather than strain our brains with the perhaps impossible task of finding a closed form solution, we will attempt to make some reasonable approximations which might lead to a qualitative solution to the circuit.

The problematic factor in (4.54) is the square of the natural log term. By finding a Taylor series expansion for $\ln^2(1 + e^x)$, we can convert this nonlinear ODE with transcendental terms into an ODE containing only algebraic terms.

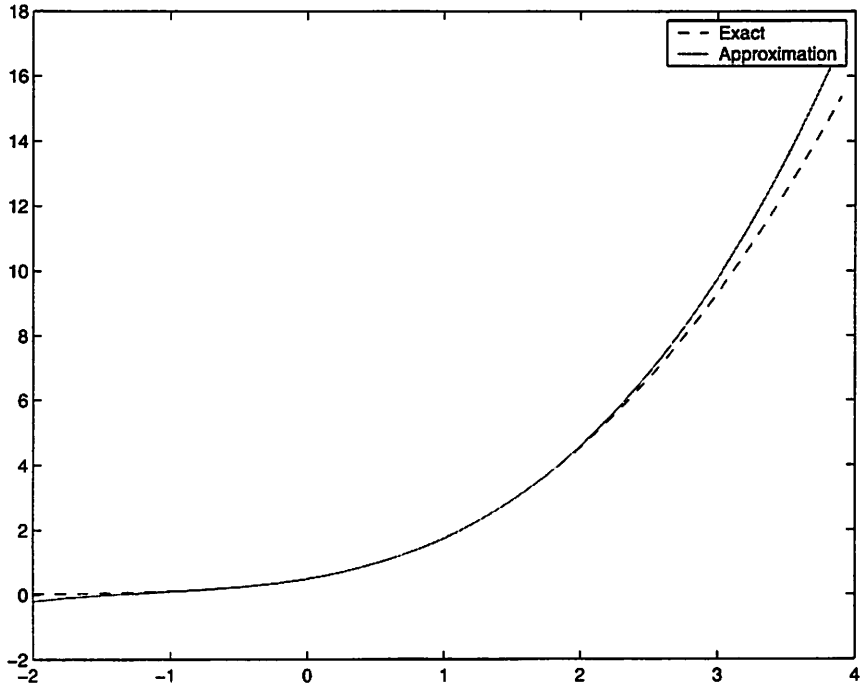


Figure 4.17 Third-order Taylor series to $\ln^2(1+e^x)$.

The Taylor series expansion of $\ln^2(1+e^x)$ is

$$\ln^2(1+e^x) = \ln^2 2 + x\ln 2 + \frac{x^2}{4}(1+\ln 2) + \frac{x^3}{8} - \frac{x^4}{192} + \ldots \qquad (4.55)$$

A comparison between (4.55) and $\ln^2(1+e^x)$ is shown in Fig. 4.17. From Fig. 4.17, we see that the fit matches well in the interval $[-2,3]$. By changing V_C, we can center our circuit's operation anywhere on the curve. Thus, choosing V_C somewhere between $V_C = 0$ and $V_C = 1$ maximizes the region where the approximate solution is valid. Remember that x in the Taylor series expansion is related to gate-source voltages added to V_C. At "hot" room temperature (300 K), $\phi_t = 25.85$ mV and $4n\phi_t$ is somewhere between 100 mV and 150 mV. Hence, the range of x from -2 to $+3$ is valid for an LO swing of about 250 mV.

This limited range of the LO swing implies that this approximate solution is not valid for large LO signals that drive the MOS transistors into both hard "on" and "off" regions. Instead, this analysis is appropriate for small LO swings, which is of particular interest to low-power research. As will be explained in the next chapter,

one of the techniques to reduce power is the removal of the hidden power consumers, such as LO buffers and other inter-block patchwork circuitry. This removal of inter-block buffers, however, does not come without a consequence. Without buffers, the gates of the LO switches load down the LO, hence must be reduced in size, in addition to the LO signal remaining small. This analysis applies to these situations.

Plugging (4.55) into (4.54), we get

$$v_{if}' + A\left(\frac{3v_{lo}^2}{256\phi_t^3 n^2} + \frac{\ln 2}{2\phi_t} + \ldots\right) v_{if} = A\left(\frac{v_{lo}v_{rf}}{16\phi_t^2 n}(1+\ln 2) + \ldots\right) \tag{4.56}$$

where

$$A = \mu\frac{C_{ox}}{C_L}\frac{W}{L}(2n)\phi_t^2 \tag{4.57}$$

Neglecting higher-order terms, we linearize the problem and get a simple first-order linear ODE. Noticing the similar forms of both (4.5) and (4.56), we follow the analysis of the simplified model to transform (4.56) into an equivalent block diagram, as shown in Fig. 4.18.

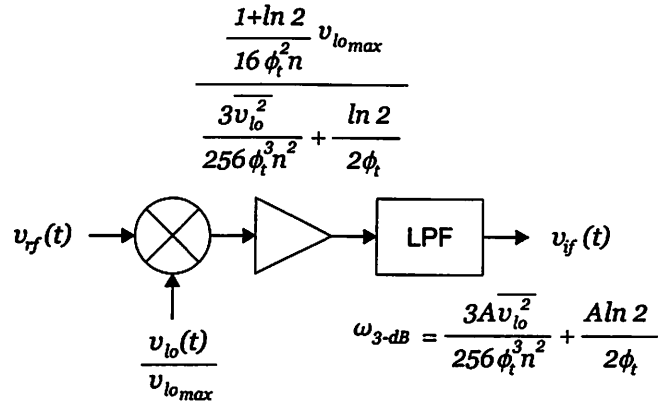


Figure 4.18 Equivalent block diagram of the CMOS double-balanced switching mixer derived using the EKV model.

TABLE 4.1

Passive mixer conversion gain when driven by a sinusoidal LO

LO amplitude	Square-Law	EKV	Spectre
0.6	0.7854	0.7994	0.8516
0.5	0.7854	0.8347	0.8554
0.4	0.7854	0.8561	0.8542
0.3	0.7854	0.8418	0.8300
0.2	0.7854	0.7556	0.7480

TABLE 4.2

Output pole of the passive mixer when driven by a sinusoidal LO

LO amplitude	Square-Law	EKV	Spectre
0.6	163 MHz	130 MHz	110 MHz
0.5	136 MHz	100 MHz	66.3 MHz
0.4	109 MHz	78 MHz	32 MHz
0.3	82 MHz	60 MHz	13 MHz
0.2	54 MHz	47 MHz	4 MHz

From Table 4.1 and Table 4.2, we see that when we use the EKV model in our analysis, our results are closer to simulated values than when using the square-law model. This is because the EKV model is specifically curve-fitted to the actual simulation models used. However, when the LO waveform takes on the shape of a square wave, using the EKV model returns results for the conversion gain which are farther than $2/\pi$. This is probably due to the linearization of the expression in (4.56). Also, the poles found from the more complicated analysis are only slightly closer than those found using the square-law model.

We see that this analysis is useful when analyzing the passive mixer with small LO amplitudes.

A.4.2 SHORT-CHANNEL TRANSCONDUCTANCE

We repeat the equation for the short-channel MOS transistor (3.22) for convenience.

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs}-V_t)^2\frac{1}{1+\dfrac{(V_{gs}-V_t)}{E_{sat}L}} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs}-V_t)\,V_{dsat} \qquad (4.58)$$

where V_{dsat} is the short-channel saturation voltage which includes the effects of velocity saturation, E_{sat} is the saturation field which marks the onset of velocity saturation, L is the effective channel length, and μ is the effective mobility.

$$V_{dsat} = (V_{gs}-V_t) \parallel E_{sat}L = \frac{(V_{gs}-V_t)\,E_{sat}L}{(V_{gs}-V_t)+E_{sat}L} \qquad (4.59)$$

The transconductance is the derivative of the current with respect to the gate voltage, hence

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \tag{4.60}$$

$$= \mu C_{ox} \frac{W}{L} (V_{gs} - V_t) \frac{1}{1 + \frac{(V_{gs} - V_t)}{E_{sat} L}}$$

$$- \frac{1}{2} \mu C_{ox} \frac{W}{L} \frac{(V_{gs} - V_t)^2}{\left(1 + \frac{(V_{gs} - V_t)}{E_{sat} L}\right)^2} \frac{1}{E_{sat} L} \tag{4.61}$$

$$= \sqrt{\frac{2 I_{ds} \mu C_{ox} \frac{W}{L}}{1 + \frac{(V_{gs} - V_t)}{E_{sat} L}}} - \frac{I_{ds}}{(V_{gs} - V_t) + E_{sat} L} \tag{4.62}$$

$$= \sqrt{\frac{2 I_{ds} \mu C_{ox} E_{sat} W}{(V_{gs} - V_t) + E_{sat} L}} - \frac{I_{ds}}{(V_{gs} - V_t) + E_{sat} L} \tag{4.63}$$

Chapter 5

A Mixer Design for Indoor Wireless Applications

A downconversion mixer has been designed for the receiver of an indoor wireless communications system in a 0.25 μm CMOS process. This chapter addresses the issues involved in its implementation.

5.1 The Indoor Wireless Environment

Designing an indoor wireless communications system entails solving a host of new problems not present in conventional outdoor systems. One problem is the addition of multiple signal paths which exist between the transmitter and the receiver. Termed multipath, the presence of several pathways for the signal to take is due to the many indoor reflections off objects, such as walls, furniture, and people. Signals which traverse different path lengths arrive at the receiver at different times, resulting in time-shifted copies of the same signal. If not properly handled, this could lead to corruption of the signal as delayed pulses interfere with later transmissions.

Indoor systems also face the problem of dealing with spurious electromagnetic radiation coming from many indoor appliances. Electronic devices, such as microwaves

and cordless phones, could be radiating close to the band of interest resulting in large interference for the indoor system. While their relatively low radiated power is negligibly small to high-powered outdoor systems, low-power indoor systems may find the spurious radiation to be nonnegligible.

On the other hand, indoor wireless systems do have their advantages. For picocellular applications, the presence of walls naturally define the boundaries of a cell. The barriers present large attenuation to penetrating signals, effectively limiting the amount of intercell interference. In addition, indoor systems do not have to face the wrath of the elements, such as rain, snow, or other meteorological hindrances to electromagnetic radiation.

Thus, designing a working indoor wireless system requires careful consideration of these problems and advantages. Choosing the right specifications based on the application and environment is currently an open field of research. The receiver we fabricated was based on specifications outlined in [22].

5.2 An Indoor Wireless System

Through more sophisticated algorithms which can recover the received signal with lower SNR, the specifications for the analog front-end can be relaxed, essentially trading high-power analog processing for low-power digital computation and flexibility. Part of the reasons for this, as mentioned in Chapter 2, is the increased noise tolerance of digital circuitry.

The indoor wireless system chosen depends on an adaptive demodulation scheme, based on code division multiple-access (CDMA) [2], to achieve a *processing gain* which boosts the received SNR. But more importantly, CDMA spreads the signal energy uniformly over a large bandwidth, thus reducing the dependency of transmission on any narrow band of frequencies. This makes the system more immune to frequency fading effects when compared to other schemes, such as FDMA. Frequency fading can arise from shifts in time, such as is encountered in the multipath problem.

By careful choice of modulation schemes, much of the signal power close to DC can also be reduced, opening up the possibility of using a homodyne system. This,

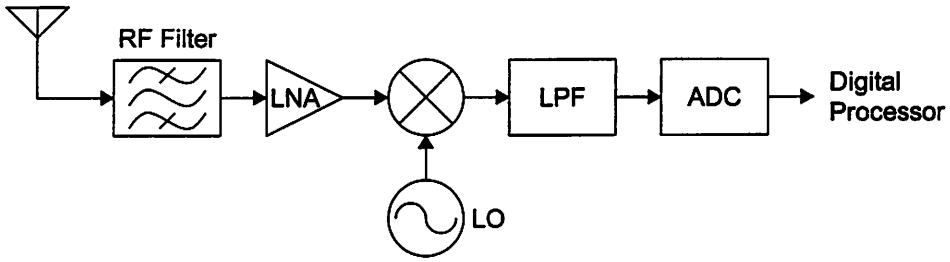


Figure 5.1 Direct-conversion receiver.

in turn, could lead to greater savings in power and simplicity. The overall receiver chain is shown in Fig. 5.1.

The receiver uses a fully-differential architecture, immediately converting the single-ended output of the RF filter[1] into a differential input to the LNA with a balun. All the blocks following the filter are fully-differential structures.

The LNA is implemented with a differential pair using a tuned-load at the output. As in most LNA designs, the main goal is to achieve maximum gain with the minimum noise output. This minimizes the noise contributions of the following blocks as shown by the Friis equation [7]. For this system, power consumption is also an issue. Slightly higher noise levels can be tolerated if they come with great savings in power.

Following the LNA, the downconverting mixer is based on the double-balanced Gilbert commutating cell. The active mixer uses linear PMOS loads which are biased by an external network which allows for the possibility of variable gain. Being the second block in the receiver chain, the noise contributions of the mixer is still somewhat significant. A compromise between power consumption and added noise was made which resulted in a low-power design.

The frequency synthesizer is a ring oscillator based phased-locked loop (PLL) operating at 2 GHz. Again, with the relaxed specifications of the analog front-end, higher phase noise can be tolerated in exchange for greater savings in power. The PLL also provides the clock signal for the digital portion of the receiver. This block is described in great detail in [23].

[1] The analog front-end for this implementation requires an external RF filter. Future versions will make use of on-board microstrip filters, baluns, and antennas.

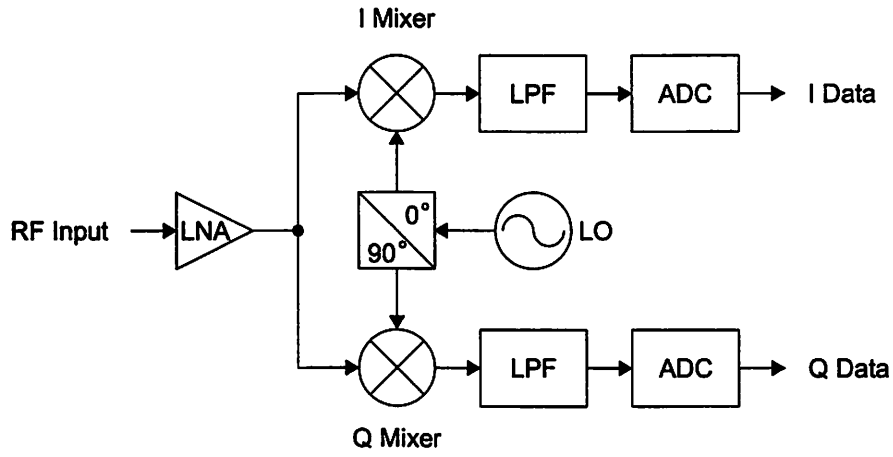


Figure 5.2 IQ downconversion.

Following the mixer is a Sallen-Key active Butterworth filter. This lowpass filter provides additional filtering and gain after the mixer. Being the third block in the received signal path, its noise contribution may be negligible.

The analog-digital converter (ADC) is a 7-bit 2-1-1 delta-sigma modulator. This complicated block is much better explained in [24].

5.3 The Mixer

The double-balanced active switching mixer was chosen for several reasons. As mentioned before, the double-balanced configuration provides some immunity to common-mode noise in the LO and RF signal paths. The differential output at the IF port keeps the mixer fully-differential.

The active mixer was chosen since some gain was needed. The other option considered was a passive mixer followed (or preceded) by a gain stage. By adding another gain stage, power consumption is increased, and the argument of a zero power consumption passive mixer can no longer be used when comparing against the active mixer. Hence, a comparison based on overall gain, noise, and total power consumption would have to be made. We found that by designing a relaxed active mixer, it was possible to achieve very low power consumption. In addition, the active mixer has much better port isolation properties, which can be further improved by

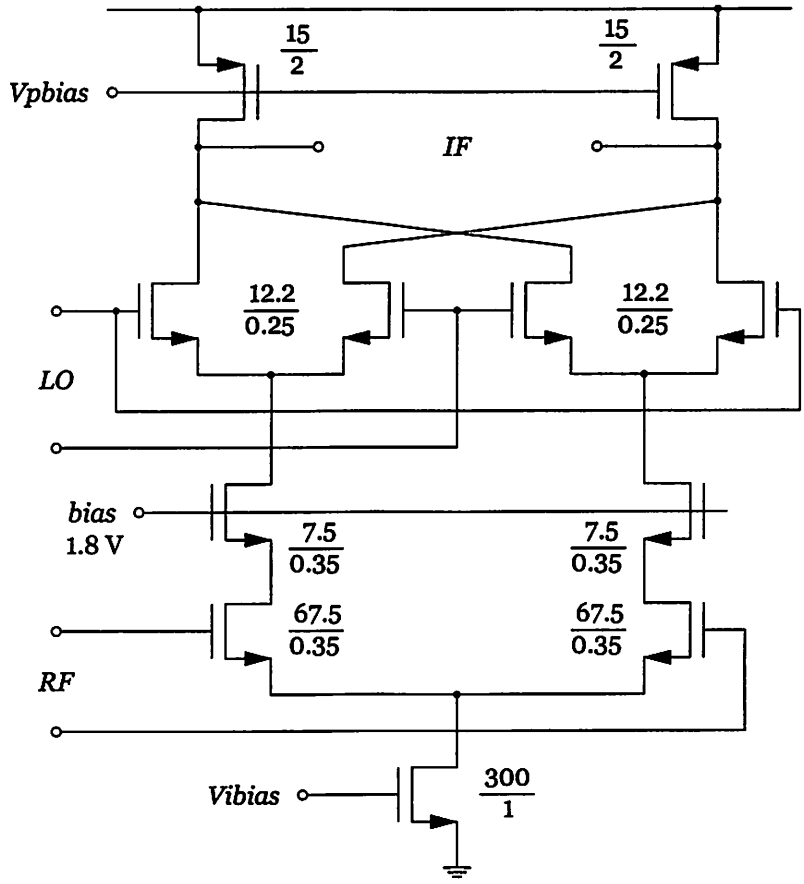


Figure 5.3 CMOS Gilbert mixer.

adding cascode transistors.

A final reason for designing the active mixer is the ease of the design compared to the passive mixer. Designing for the different performance metrics of an active mixer is somewhat uncoupled. Whereas changing the size of the switches in the passive mixer may change gain,[2] the load presented to the PLL, and the pole of the output filter, the LO switches do not affect the gain or the pole on the active mixer, to a first-order approximation. The mixer implemented is shown in Fig. 5.3.

5.3.1 Mixer Load

A linear PMOS load was used for this mixer because of the variable resistance they can provide through changing the gate voltage. Other possible loads include an NMOS

[2] Changing the switch resistance may invalidate the approximations made in Chapter 3.

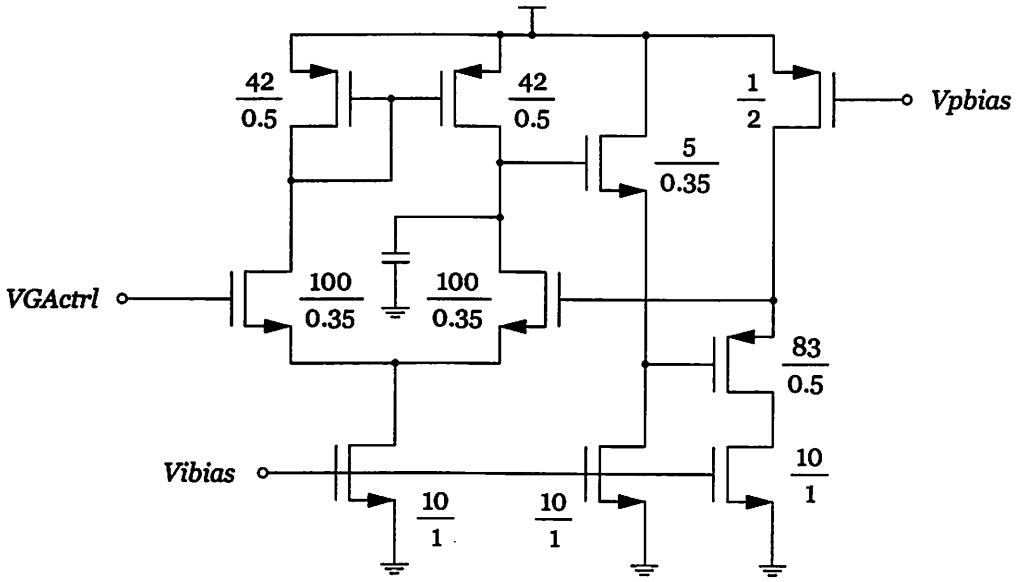


Figure 5.4 Bias network that generates bias voltage for mixer load.

load, as implemented in [13]. The NMOS load was not chosen because of its need for common-mode feedback. The circuitry used to control the gate voltage of the PMOS load is shown in Fig. 5.4.

5.3.2 Coupling with the LNA

Because of the different DC bias voltages at the output of the LNA and the input of the mixer, voltage-shifting was necessary. A bias string was used to provide the

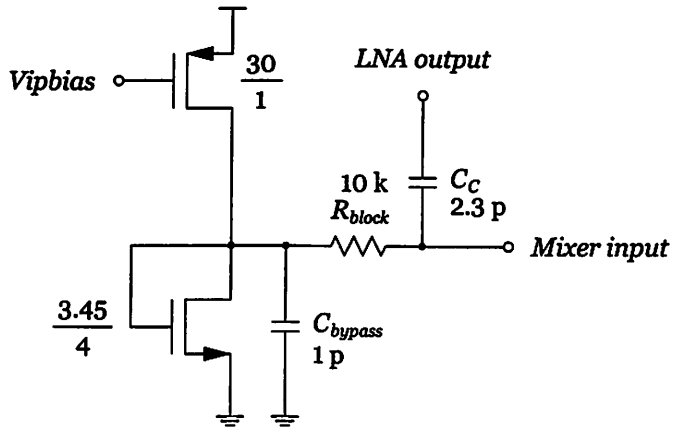


Figure 5.5 AC coupling circuitry between the LNA output and the mixer input.

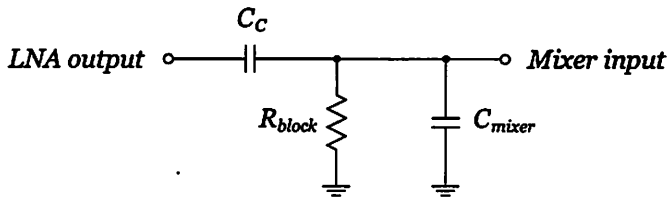


Figure 5.6 Equivalent small-signal circuit of the AC coupling circuitry.

input DC voltage for the mixer, while a metal-metal sandwich capacitor was used for AC coupling between the LNA output and the mixer input. DC coupling was not used because of the large difference between the LNA output bias and the mixer input bias. The AC coupling circuitry is shown in Fig. 5.5. R_{block} acts as a choke for high-frequency signals (in place of on-chip inductors). For analysis, the equivalent circuit, shown in Fig. 5.6, was used to calculate the transfer function of the coupling circuitry,

$$\frac{V_{out}}{V_{in}} = \frac{sR_{block}C_C}{1 + sR_{block}(C_C + C_{mixer})} \tag{5.1}$$

which, for large R_{block} or large C_C, reduces to the capacitive voltage divider,

$$\frac{V_{out}}{V_{in}} = \frac{C_C}{C_C + C_{mixer}} \tag{5.2}$$

Notice that we can go from (5.1) to (5.2) if we set C_{mixer} large, but this would only degrade the transfer function (5.2). Hence, we should design for large R_{block} and large C_C. In the final implementation, R_{block} was 10 kΩ and C_C was 2.3 pF. The bottom plate parasitic capacitance of the metal-metal sandwich capacitor was placed on the LNA side. This way, the transfer function (5.2) would not be degraded through the increase of C_{mixer}. The bottom plate capacitance is simply added as a capacitance in the tuned load of the LNA.

5.3.3 Coupling with the PLL

We chose to DC couple the PLL with the LO port of the mixer to remove the need for the LO buffer. Consequently, the LO switches of the mixer would have to be made smaller to keep the PLL lightly loaded and thus preventing an increase in power consumption. This leads to an increase in flicker noise generated by the switches. Lower

total noise was essentially traded for lower total power consumption. AC coupling could not be achieved easily with passive structures, as was done for the coupling with the LNA, because of the large parasitic capacitances which would have ended up loading the PLL. These large parasitic capacitances would have increased the PLL's total power consumption, thus nullifying the savings in mixer power consumption.

5.3.4 Coupling with the Filter

The IF port of the mixer was DC coupled to the filter. By setting the resistance of the mixer load to set the common-mode output of the mixer, a suitable input bias level for the filter was achieved.

5.3.5 Bias

The bias voltages used for the LNA input, cascode transistors, and load control network, are all referenced to one current source. On the current test-chip, the current source was provided off-chip, but future versions of the receiver will provide an on-chip reference.

Careful layout techniques were used to ensure matching between mirrored transistors that were designed to provide the same current. In addition, large bypass capacitors were placed along the gates of the current sources to maximize cleanliness of the sources.

5.4 Simulated Results

The mixer design was simulated extensively in Cadence's *Spectre* simulator, making use of the SpectreRF package. SpectreRF is one of few simulators capable of simulating time-varying circuits, such as mixers and oscillators.

5.4.1 Conversion Gain

A plot of the conversion gain of the mixer is shown in Fig. 5.7. As can be seen, the conversion gain from 2 GHz to DC is 7.33 (17 dB) for frequencies close to the

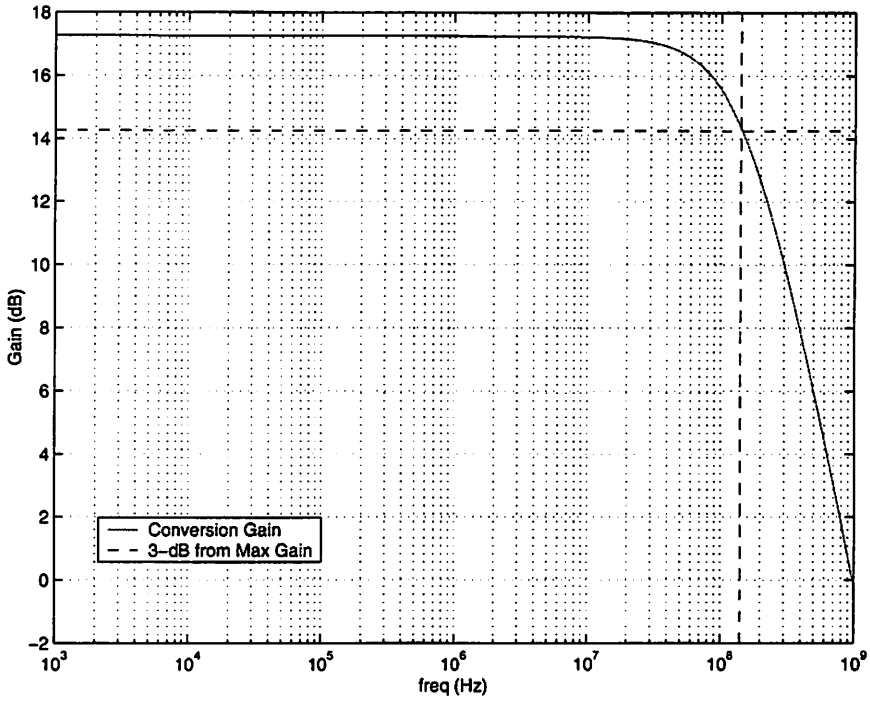


Figure 5.7 Mixer conversion gain.

carrier. The 3-dB rolloff is at 142 MHz from the carrier. There is a 0.05 dB drop from the maximum gain at 16 MHz, and at most 0.2 dB drop at 32 MHz. This plot was generated in Spectre using the periodic steady-state analysis (PSS) which linearizes the system over a time-varying operating point.

5.4.2 Linearity

A plot of the conversion gain over increasing input signal power is shown in Fig. 5.8. We see that the 1-dB compression point, which was introduced in Chapter 3 as a good metric for linearity, is -10 dBm. The 1-dB compression was determined by the input amplitude which caused the small-signal gain to drop by 1 dB, hence compression is not relative to the peak. Plotting the output powers of the fundamental and the third harmonic together in Fig. 5.9, we see that the input-referred third-order intercept point (IIP_3) is 4 dBm. Similarly, the output-referred third-order intercept point (OIP_3) is 32 dBm.

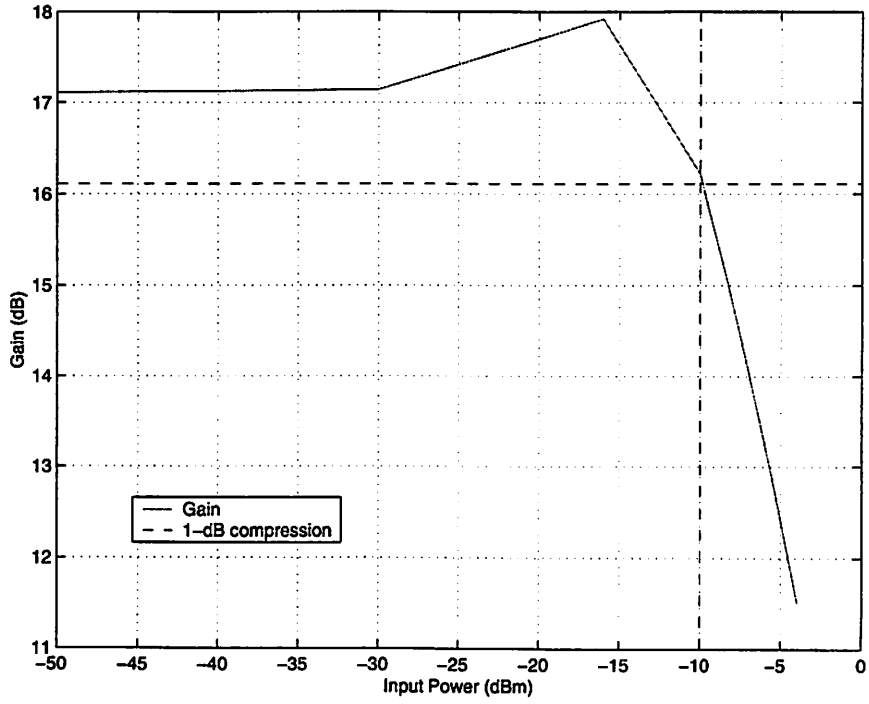


Figure 5.8 Gain plot showing 1-dB compression.

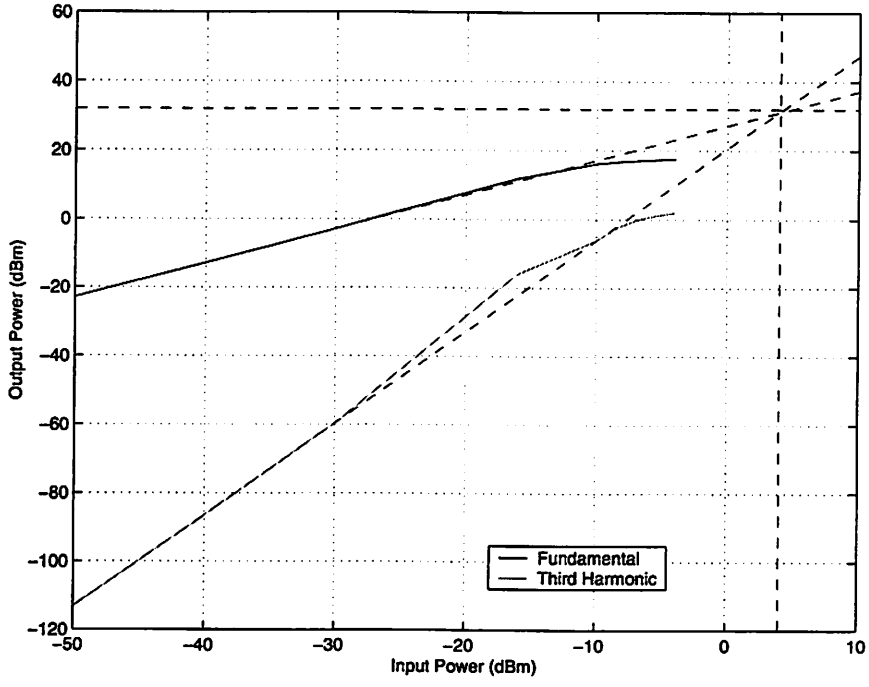


Figure 5.9 Third-order intercept point.

5.4.3 Noise

The output noise spectral density is plotted in Fig. 5.10. The increase in noise for lower frequencies is due to the flicker noise, which is particularly high for this mixer due to the small LO switches. This can be reduced through the use of larger LO switches, or LO waveforms with faster rise times, as explained in Chapter 4. The flicker noise corner is at about 1.8 MHz, after which thermal noise dominates.

One caveat in interpreting the noise output returned by SpectreRF is the difference between SSB and DSB noise, as explained in Chapter 3. Spectre calculates the SSB noise, hence must be compensated for in homodyne systems which use DSB.

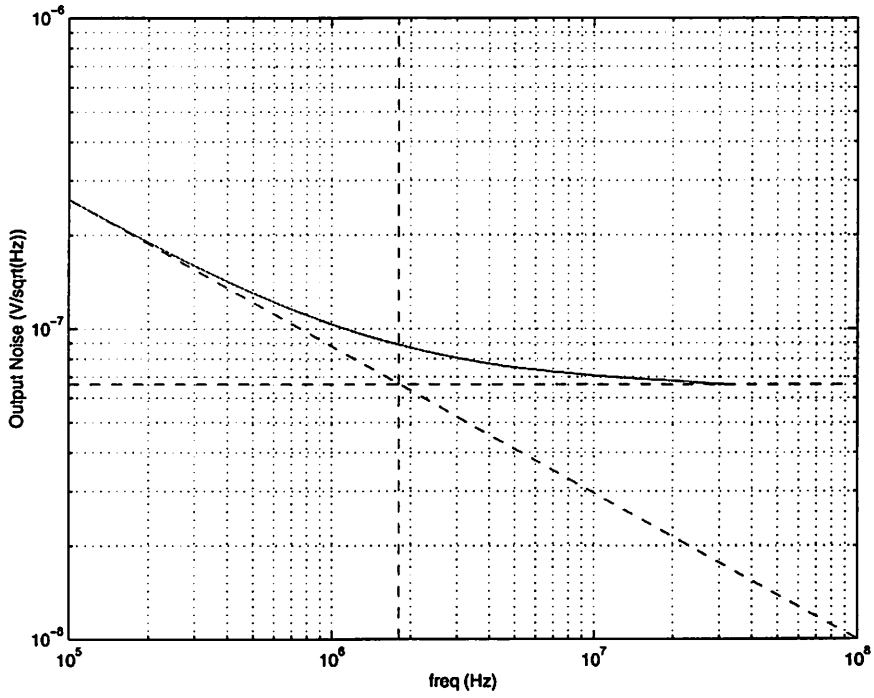


Figure 5.10 Output noise.

5.4.4 Summary

A summary of the simulated results for this mixer is shown in Table 5.1. Since this system is not normalized to 50 Ω, we have included other metrics for noise not normally provided in the mixer literature. The output-referred total integrated

TABLE 5.1

Summary of results

Supply Voltage	2.5 V
Current Consumption (I and Q mixers)	900 μA
Total Power Consumption	2.25 mW
Conversion Gain	17 dB
IIP3	4 dBm
OIP3	32 dBm
3-dB rolloff	142 MHz
Output-Referred Noise (Integrated over 32 MHz)	87.122×10^{-9} V^2
Input-Referred Noise (Integrated over 32 MHz)	1.664×10^{-9} V^2
Noise Figure (DSB)	18.0 dB

noise and the input-referred total integrated noise is a much more useful metric for determining noise performance in a fully integrated system. The noise figure reported, however, is normalized to 50 Ω, as specified by the IEEE definition.

5.4.5 Layout

Images of the layout are plotted in the following pages. The first image contains the layout of the stand-alone mixer, shown in Fig. 5.11. A close-up view of the Gilbert mixer core is shown in Fig. 5.12. The necessary bias strings and load control bias circuitry are shown in Fig. 5.13 and Fig. 5.14, respectively. The AC coupling circuitry between the LNA and the mixer is shown in Fig. 5.15. Details of the layout used to minimize parasitic capacitances between the PLL and the mixer can be seen in Fig. 5.16. A plot of the complete test-chip is shown in Fig. 5.17, while Fig. 5.19 shows the receiver implementation with the ADC.

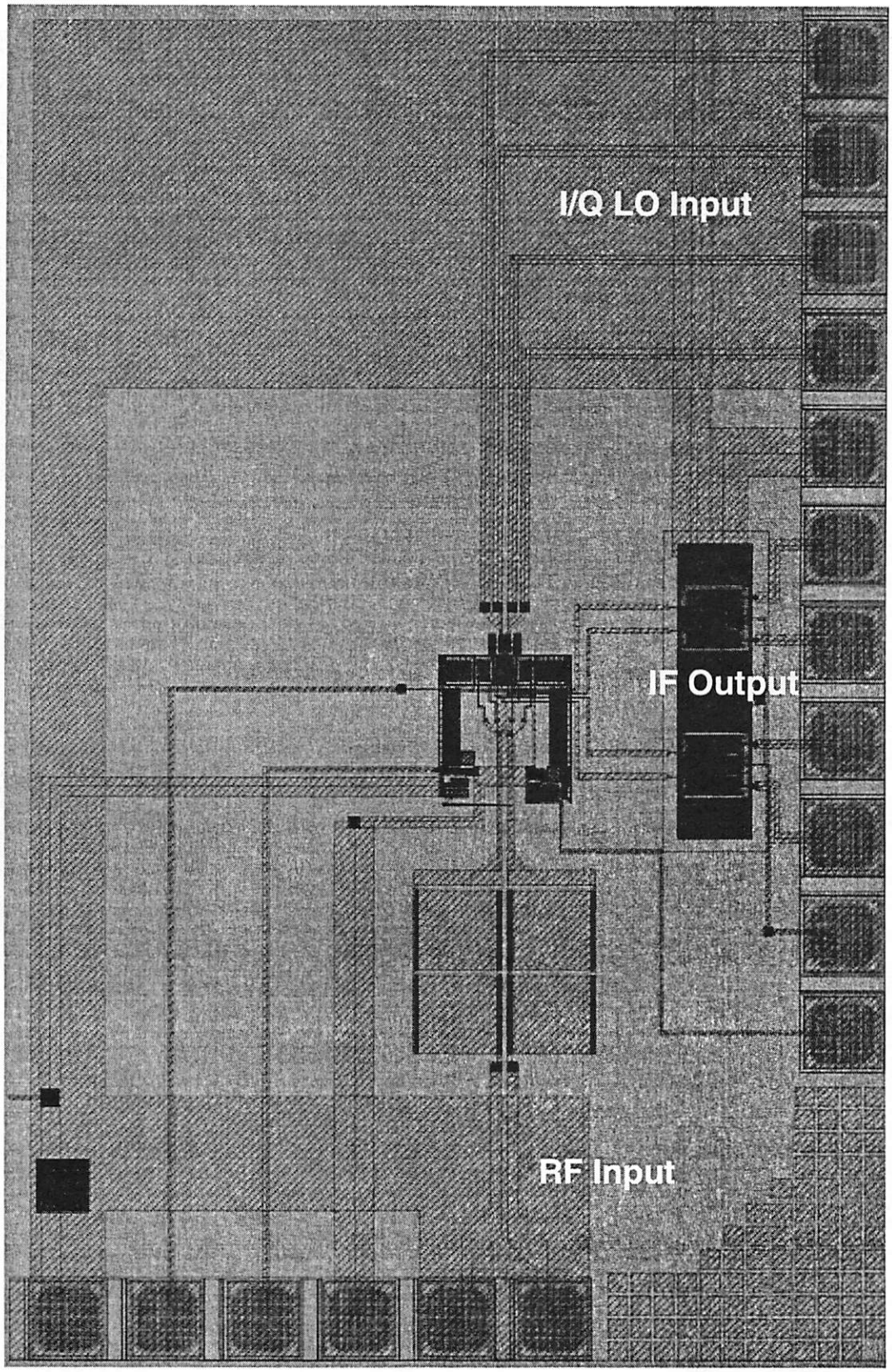


Figure 5.11 Layout of mixer.

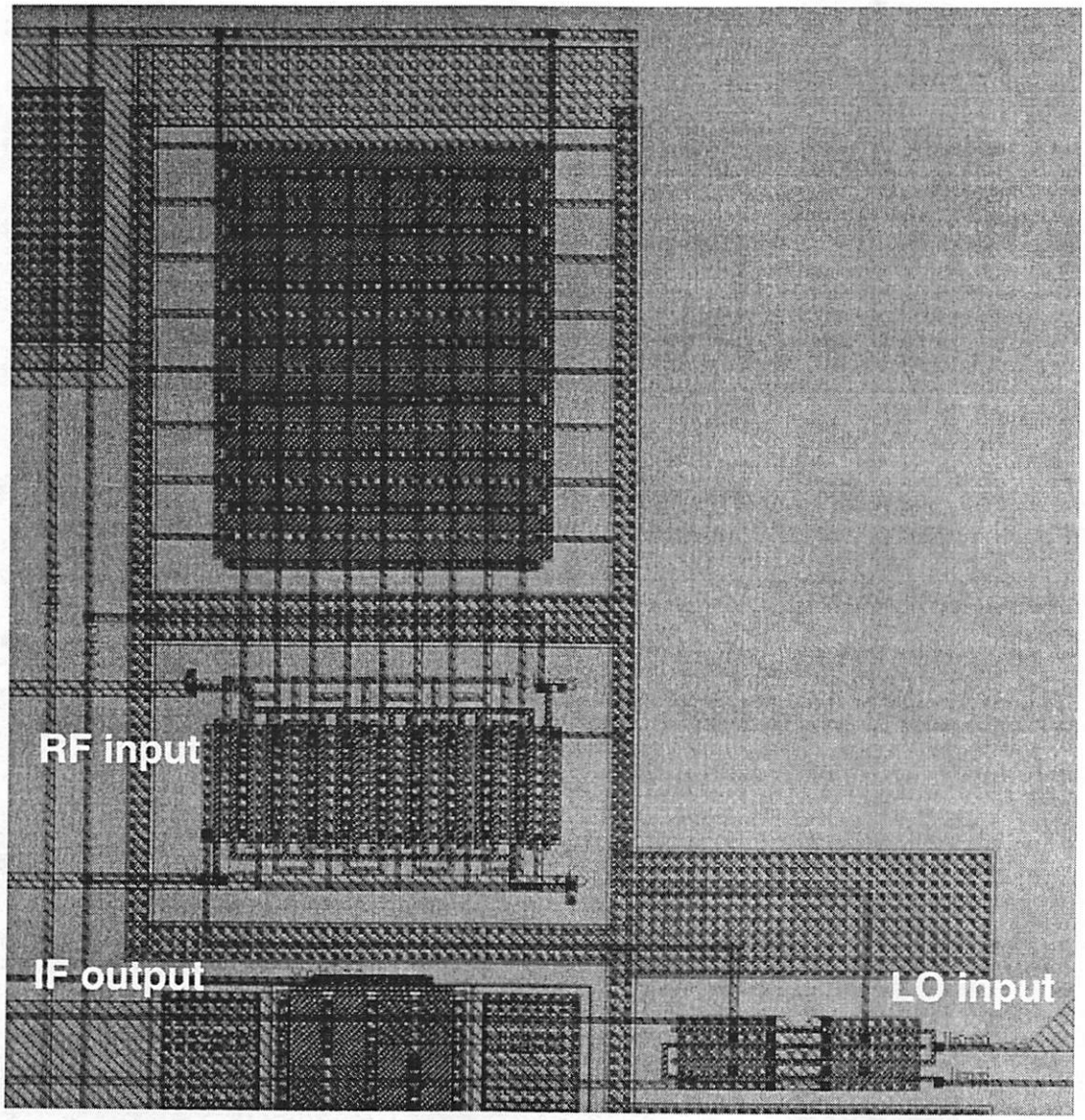


Figure 5.12 Layout of mixer core.

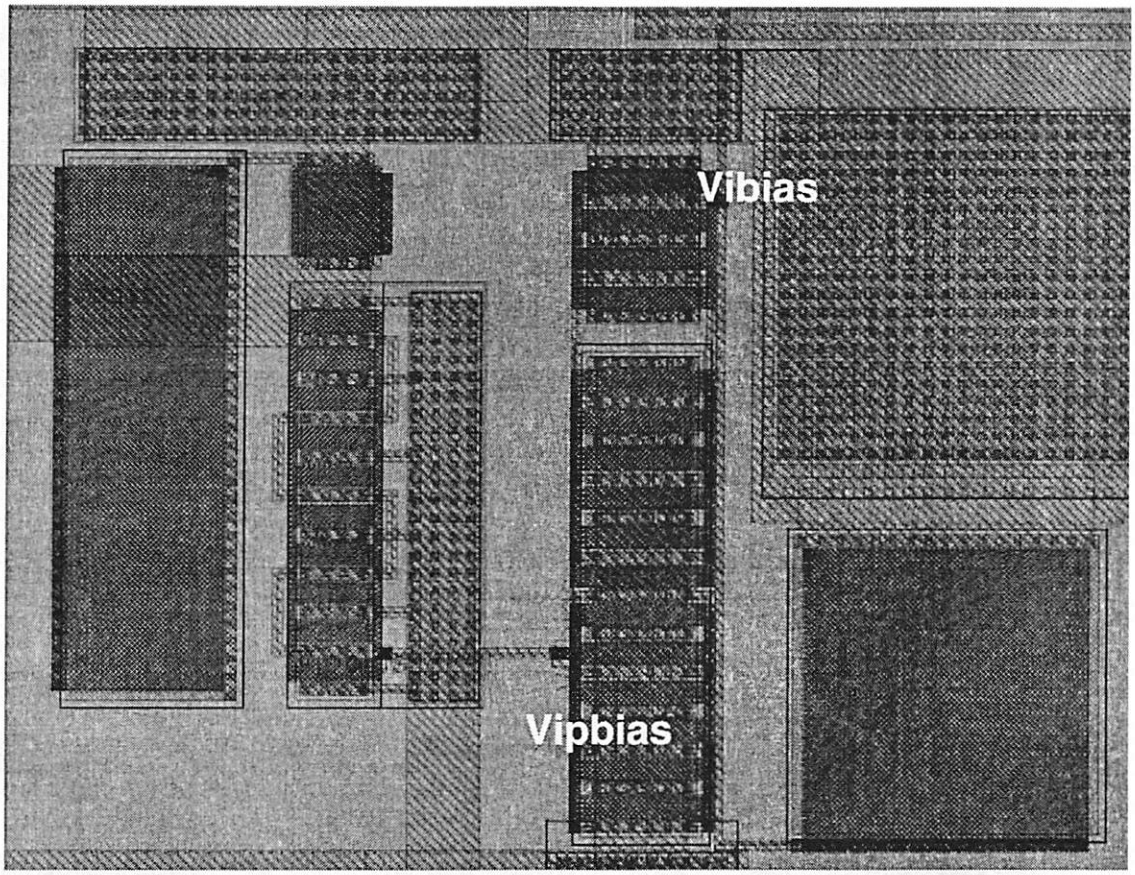


Figure 5.13 Layout of bias circuitry.

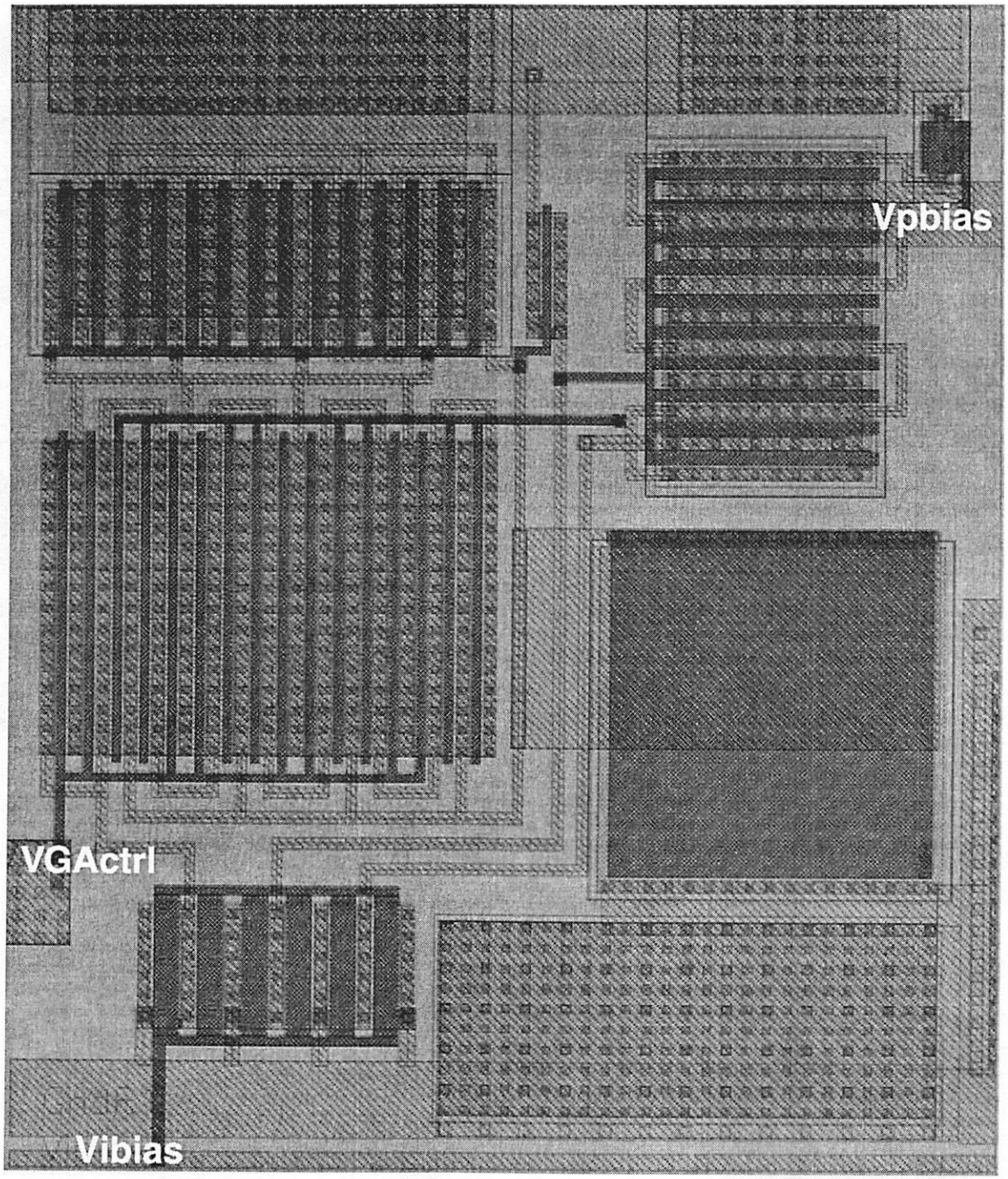


Figure 5.14 Layout of load bias network.

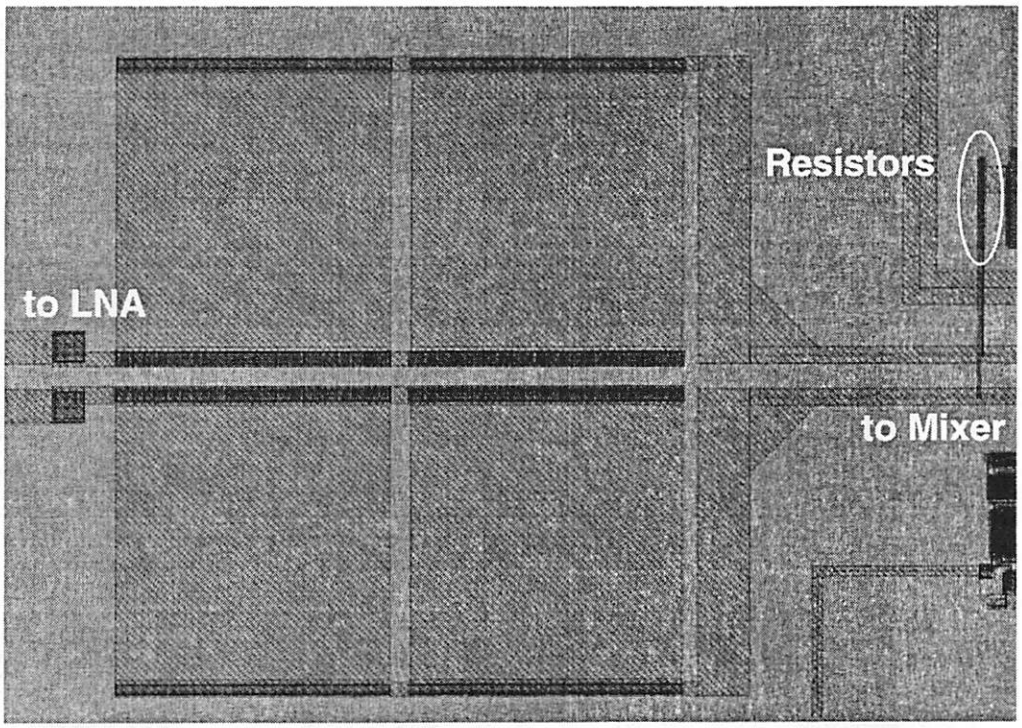


Figure 5.15 Layout of AC coupling circuitry used in LNA to mixer interface.

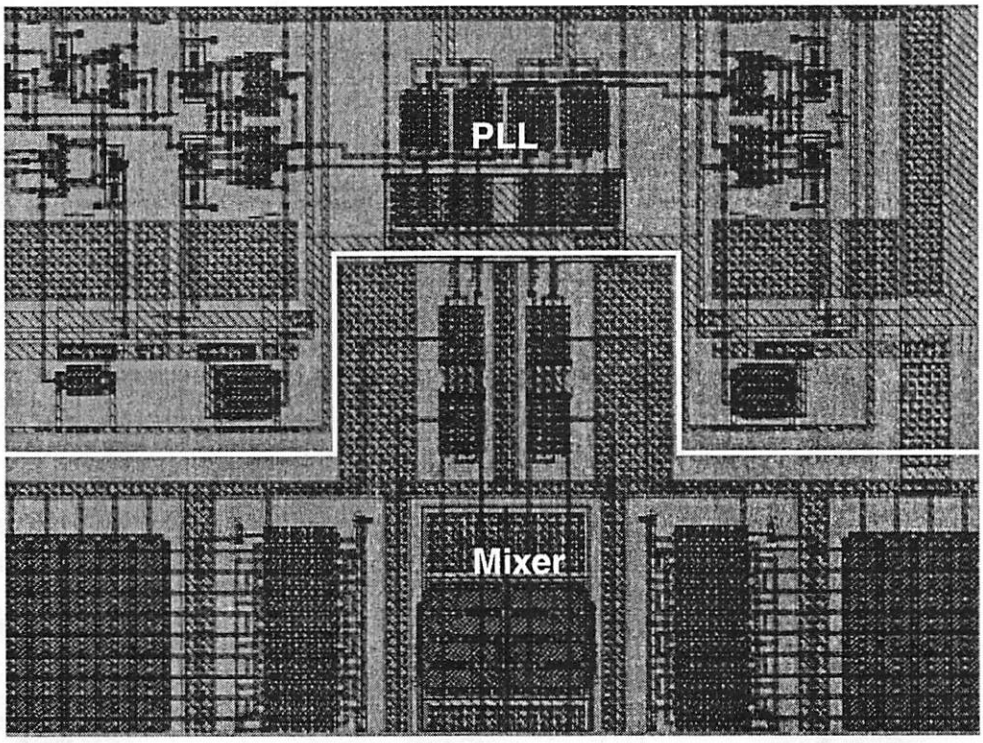


Figure 5.16 Layout of mixer/PLL interface.

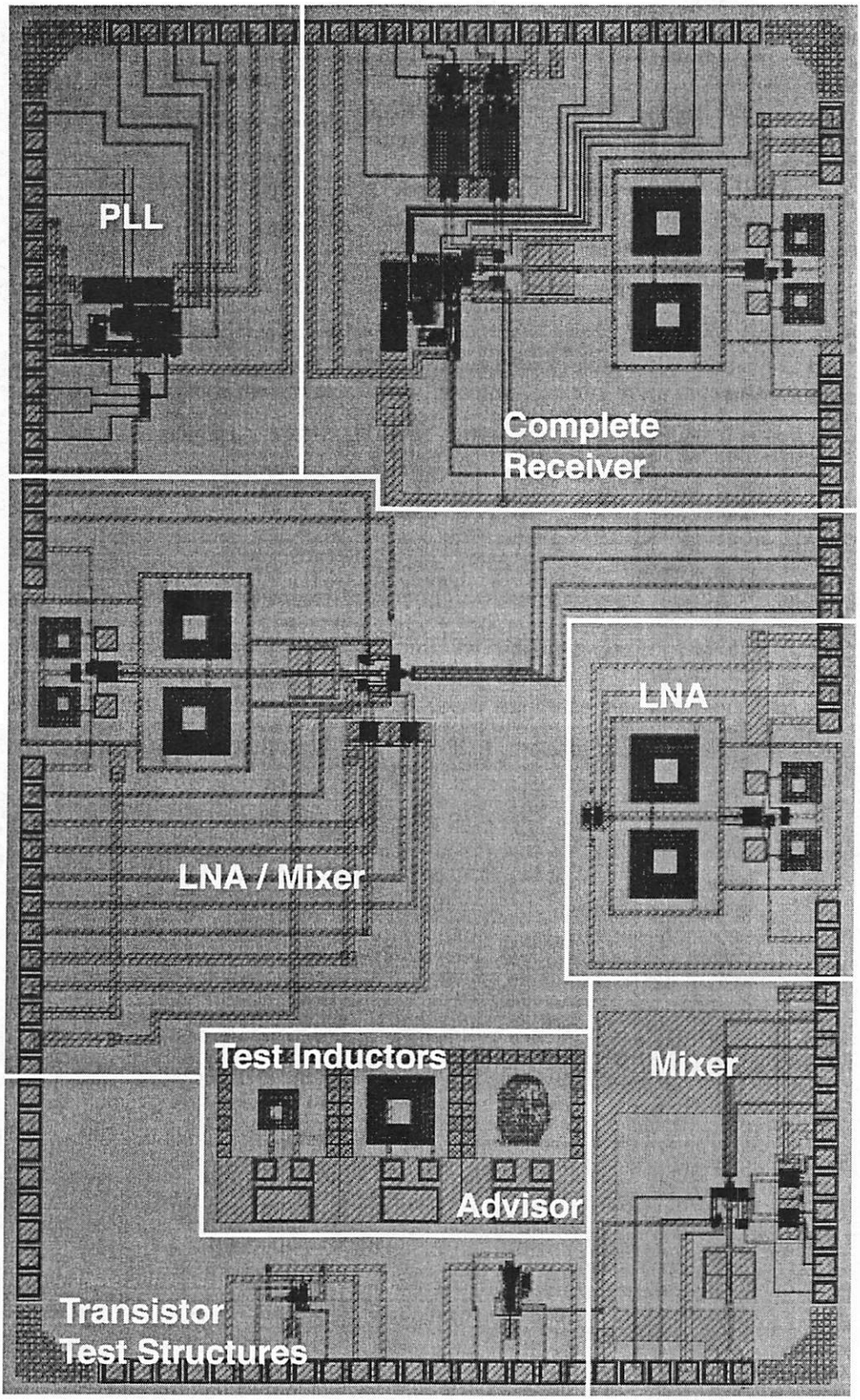


Figure 5.17 Layout of test chip.

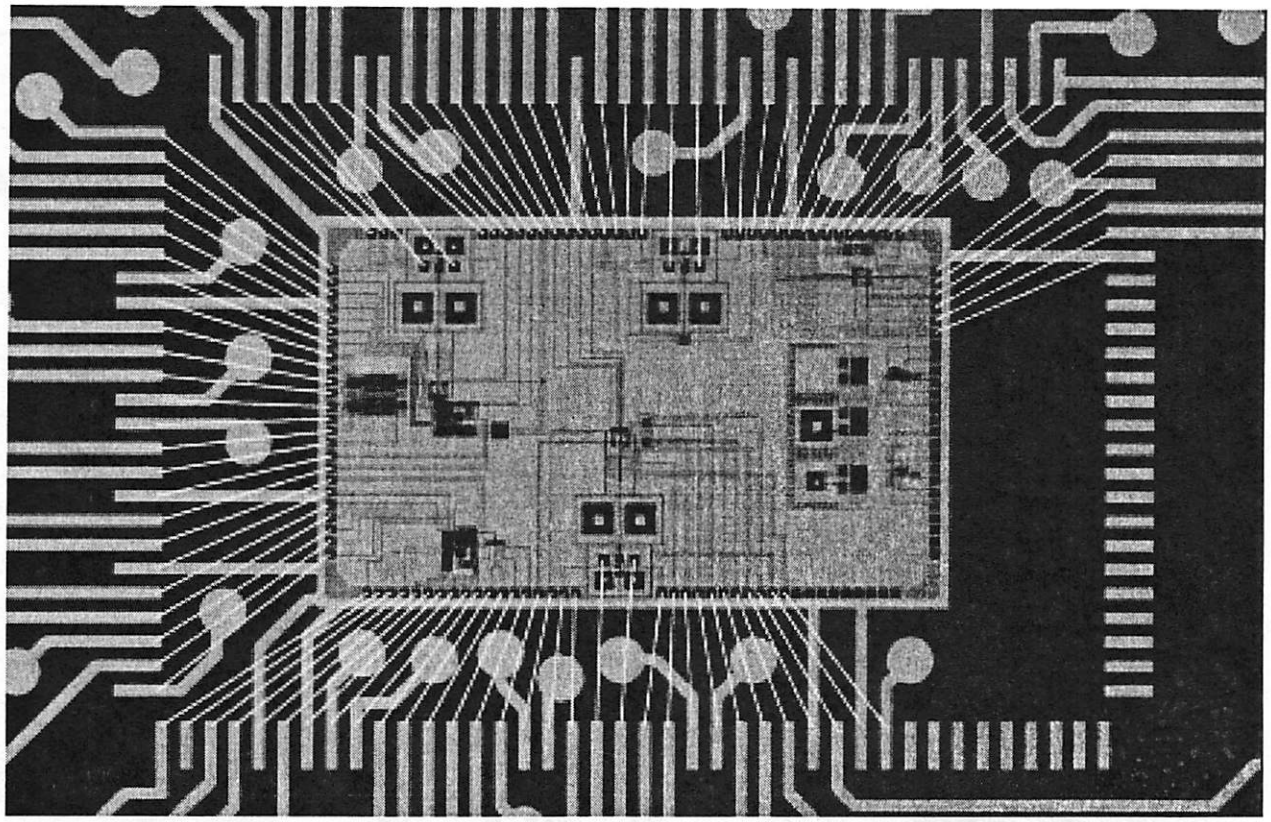


Figure 5.18 Diagram of bonding of test chip.

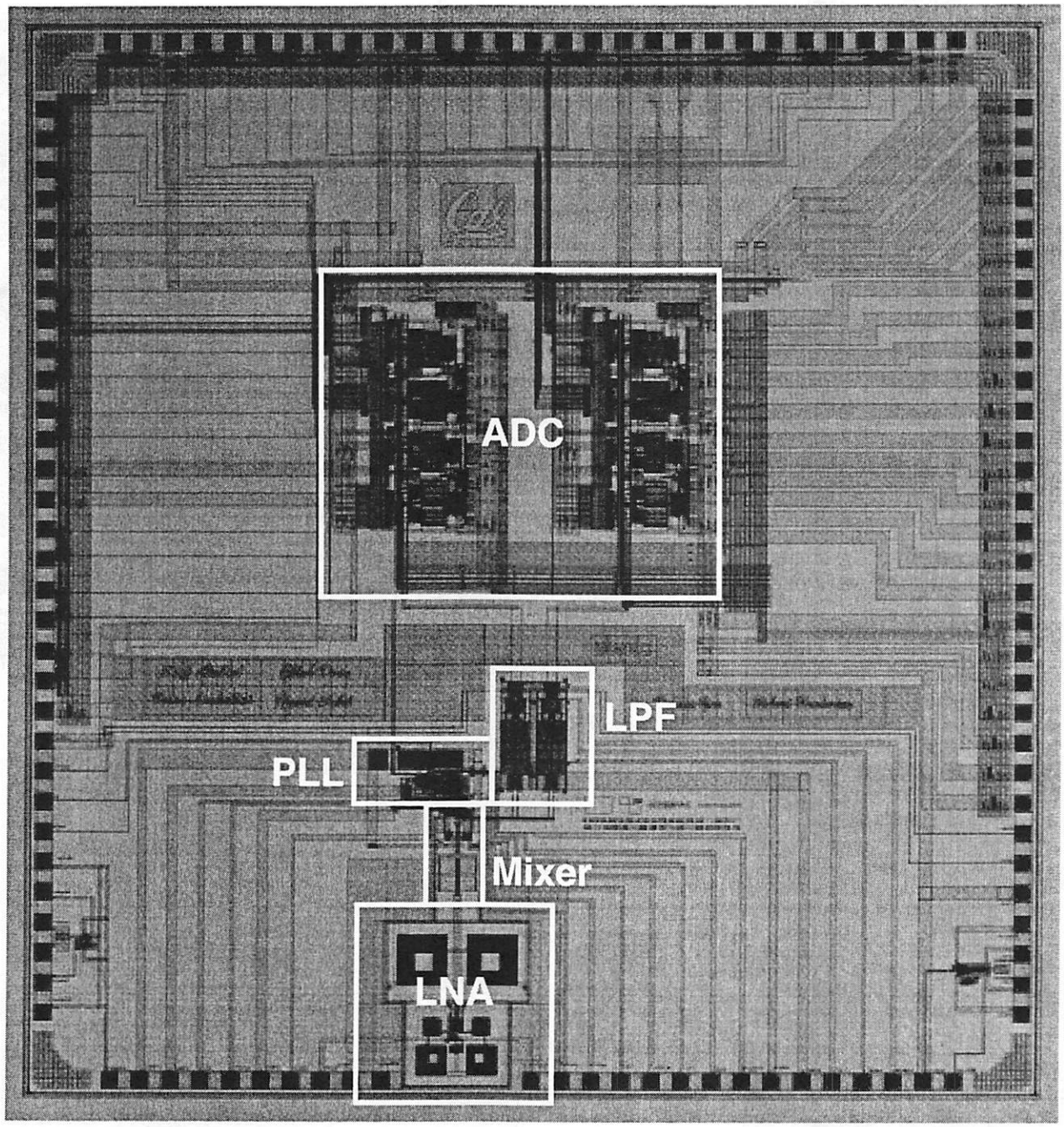


Figure 5.19 Layout of completed receiver.

Chapter 6

Conclusion

Although mixers have been around since the early half of this century, research in mixer design has not been completely exhausted beyond the need for innovation. As wireless, or wireline, devices emerge with varying requirements, the techniques used to design mixers change. With the current trend towards analog CMOS design, passive mixers are making a comeback in non-microwave frequency systems. As mentioned in the previous chapters, there are a lot of possibilities in analyzing performance tradeoffs between passive mixers and active mixers. The type of mixer that will ultimately be chosen depends on the particular application.

The mixer designed for this indoor wireless system was an active mixer. After weighing the differences between the passive and the active mixer, we chose the active mixer due to several reasons.

The active Gilbert mixer can provide gain, which for the indoor system we implemented, allows us to reduce the number of additional gain stages needed, thus saving power. Without a second gain stage after the LNA, the noise levels can also be kept at a minimum as the additional noise added by a second gain stage would

not be present. The passive design, on the other hand, would require the second gain stage, thus increasing total power consumption, noise, and the size of the signal level present at the input of the mixer. Here, the tradeoff is between noise and linearity. The additional second gain stage increases the noise at the input of the mixer, but reduces the amount of noise contribution from the mixer in the overall SNR because of the gain appearing before the mixer. However, the size of the signal going into the mixer is now increased, leading to greater linearity requirements for the mixer.

From the noise perspective, the passive design appears to be better off because of the absence of flicker noise. This, however, is nullified by the conversion loss which ends up magnifying the thermal noise contributed by the devices in the mixer.

However, the active mixer provides much greater isolation properties over the passive design. For reasons of reradiation, the active mixer is a much better design from this perspective.

With the uncoupling of several performance metrics, designing the active mixer also provides greater flexibility. This flexibility was very convenient to have during the design process since the specifications of the block were not fixed. Unlike conventional mixer design, the specifications of this mixer were changing throughout the design as we traded power consumption between the blocks in order to achieve a global optimal power consumption.

Thus, because of the gain and isolation properties, the active mixer was found to be the better design for our system.

As systems design couples in closer to individual block design, the need for a thorough understanding of the various types of mixers, and other blocks, becomes ever more important. This report tries to underline the basic elements that determine the performance of CMOS mixers. An actual design is also presented. Hopefully, this report will prove useful to future engineers when faced with the task of designing mixers.

References

[1] A. V. Oppenheim and A. S. Willsky. *Signals and Systems.* Prentice Hall, New Jersey, 1996.

[2] S. Verdu. *Multiuser Detection.* Cambridge University Press, Cambridge, 1998.

[3] R. F. Pierret. *Semiconductor Device Fundamentals.* Addison-Wesley, Reading, Massachusetts, 1996.

[4] S. Wolf. *Silicon Processing for the VLSI Era Vol. 3.* Lattice Press, Sunset Beach, California, 1995.

[5] P. R. Gray and R. G. Meyer. *Analysis and Design of Analog Integrated Circuits.* Wiley, New York, 1993.

[6] J. M. Rabaey. *Digital Integrated Circuits.* Prentice Hall, New Jersey, 1996.

[7] B. Razavi. *RF Microelectronics.* Prentice Hall, New Jersey, 1998.

[8] T. H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits.* Cambridge University Press, Cambridge, 1998.

[9] S. A. Maas. *Microwave Mixers.* Artech House, Massachusetts, 1993.

[10] J. R. Pierce and E. C. Posner. *Introduction to Communication Science and Systems.* Plenum Press, New York, 1980.

[11] A. van der Ziel. *Noise in Solid-State Devices and Circuits.* Wiley, New York, 1986.

[12] A. R. Shahani, D. K. Shaeffer and T. H. Lee. "A 12-mW Wide Dynamic Range CMOS Front-End for a Portable GPS Receiver," *IEEE Journal of Solid-State Circuits*, Vol. 32, pp. 2061–2069, December 1997.

[13] J. C. Rudell, J. J. Ou, T. B. Cho, G. Chien, F. Brianti, J. A. Weldon and P. R. Gray. "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for

Cordless Telephone Applications," *IEEE Journal of Solid-State Circuits*, Vol. 32, pp. 2071–2088, December 1997.

[14] R. S. Narayanaswami and D. G. Yee. "Noise Models for MOSFETs in Saturation," *EECS 231 Term Project*, Spring 1997.

[15] J. Crols and S. J. Steyaert. "A 1.5 GHz Highly Linear CMOS Downconversion Mixer," *IEEE Journal of Solid-State Circuits*, Vol. 30, pp. 736–742, July 1995.

[16] M. T. Terrovitis and R. G. Meyer. "Noise in Current-Commutating CMOS Mixers," *IEEE Journal of Solid-State Circuits*, Vol. 34, pp. 772–782, June 1999.

[17] B. N. Limketkai. *The Design and Implementation of a Downconversion Mixer for a Wideband CDMA Receiver.* Berkeley, December 1999.

[18] B. N. Limketkai and D. A. Sobel. "An Investigation of the Effects of Scaling on the Linearity of RF Gain Stages," *EECS 231 Term Project*, Spring 1999.

[19] R. G. Meyer. *EECS 142 Notes.* Copy Central, Berkeley, 1998.

[20] R. G. Meyer. *EECS 242 Notes.* Copy Central, Berkeley, 1998.

[21] Tsividis. *Operation and Modeling of the MOS Transistor.* Wiley, New York, 1998.

[22] D. G. Yee. *Ph.D. Dissertation.* Berkeley, To be published.

[23] C. H. Doan. *MS Project Report.* Berkeley, To be published.

[24] D. A. Sobel. *MS Project Report.* Berkeley, To be published.

[25] J. P. Vanderhaegen. *The Design and Implementation of a Wideband CDMA Basestation Transmitter.* Berkeley, December 1999.

Colophon

This document was typeset using Plain TEX and a "thesis" macro package created by the author on a Windows NT workstation running the bash shell. Text editing was done in Lemmy, a vi port to the Windows environment. Paragraphs were typeset using the included Computer Modern Roman fonts (CMR) at 12 point with 1.5 line spacing. Chapter, section, subsection headings were typset using Georgia font (converted from the Windows Truetype font collection). Figures were created using AutoCAD 2000. Text in the figures used both Georgia and Arial fonts. Plots were generated in MATLAB. Simulation data taken from Cadence/Spectre were exported as text then imported into MATLAB for plotting.