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THE IMPACT OF LINE EDGE ROUGHNESS ON 100nm MOSFET DEVICES

by

Tho Truong Nguyen

Memorandum No. UCB/ERL M00/27

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ELECTRONICS RESEARCH LABORATORY

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The Impact of Line Edge Roughness on 100nm MOSFET Devices

By Tho Truong Nguyen

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements of the degree of **Master of Science, Plan II**.

Approval for the Report and Comprehensive Examination:

Committee:

Professor Jeffrey Bokor
Research Advisor

5/16/00

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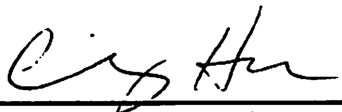

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Table of Contents

1.0 Introduction 1

2.0 Line Edge Roughness in Resist Patterns 3

2.01 Experimental Evidence of LER in sub-0.25-μm Resist Patterns.. 3

2.02 Factors Contributing to Line Edge Roughness 5
2.02.1 Effects of Polymer Aggregates on LER 6
2.02.2 Effects of Aerial Image Contrast on LER 7
2.02.3 Effects of Mask Defects on LER 8

2.03 Transfer of LER from Resist Pattern to Etched Pattern 10

2.04 Metrology Methods for Measuring and Quantifying LER 11
2.04.1 Scanning Electron Microscope (SEM) Method 11
2.04.2 Atomic Force Microscope (AFM) Method 12
2.04.3 SEM and AFM Method Comparisons 13

3.0 Effects of LER on Device Performance Simulations 14
3.01 Simulation Plans 14
3.02 Base Device Design 14
3.03 Short Channel Effects (SCE) Considerations in FDSOI Design .. 16

4.0 Single Defect Simulations, Results and Discussion 22

5.0 Line Edge Roughness Simulation Setup 27
5.01 Line Edge Roughness Construction 27
5.02 Device Structure by 3-D Processing 29

6.0 LER Device Simulations, Results and Discussion 31

7.0 Conclusion 41

8.0 References 43

1. Introduction

With the explosion of the high-speed digital circuitry in the past decades, MOSFET devices have been the most often used as basic devices. The continuous demand for faster speed, higher package density and more cost effective methods has forced chip makers to reduce transistor size down to the nanometer regime. According to the International Technology Roadmap for Semiconductors, MOSFET transistors with gate length of 100 nm will be on the production line by the year 2005.

During the course of device fabrication, a device undergoes multiple processes that cause it to be subject to deviation far from an ideal model. Namely, the geometry of the device will be very different from the original design. In the nanometer regime, the critical dimension of a device plays a very important role in the device electrical characteristics. Most importantly as the device dimensions continue to scale down, the channel length of a MOSFET transistor plays a major role in determining the device performance. Short channel devices are subject to several effects that are not normally seen in long channel devices; in some cases these short channel effects can severely impact the device. Therefore any changes in the gate definition will ultimately lead to changes in the device channel length and thus its electrical behavior. Most device simulations treat the gate as if it were perfectly smooth along the width of the device. However, experiments have shown that linewidth fluctuation occurred in all resist patterns due to reticles, the aerial image quality, the etch mask quality, polymer molecular properties of resists and etch process. These linewidth fluctuations are line edge roughness (LER) that is transferred from the resist pattern onto the gate with some further variation during gate etching and formation. As the critical dimensions (CDs)

shrink to below 130 nm, LER consumes a major part of CD tolerance budget. Therefore, it is important to address the cause of such gate LER and the effects on the device performance. To answer the question of how LER affects the device behavior and what maximum tolerable LER is allowed, device modeling in 3D structure must be carried out. The benefit of device simulation is the flexibility of producing roughness variations for different devices without having to do time consuming and costly fabrication. The models give more insight about the effects of the device so that we can define better experimental direction. The daunting challenge of simulating device with random roughness is to construct the geometry, doping profile, and the grid file such that they represent a realistic device and still meet convergence criteria. Furthermore the computation capability in terms of CPU and Memory set some limitation due to the nature of 3-D structures. This project investigates the impact of LER on 100 nm MOSFET devices through extensive 3-D model simulations. The report contains three major parts. Part one of the report will discuss experimental evidence and causes of LER and metrology methods of measuring LER. Part 2 of the report presents the experimental approach and plans for creating devices with random rough gates for simulations. The final simulation results will be presented in part 3 of the report.

2.0 Line Edge Roughness in resist patterns

2.01 Experimental Evidence of LER in sub-0.25-μm Resist Patterns

Line edge roughness on resist patterns ranging from 5 to 20nm has been observed in a number of experimental studies. For feature length in the order of 100nm, post-optical lithography such as EUV lithography will be the used for pattern transfer. One that has been considered for EUV lithography is top-surface-imaging silylation resist, which unfortunately exhibits high LER. An experiment done at Lincoln Laboratory has focused on this TSI resist LER led by Susan Palmeteer[1]. The group used MX-P7, from Microlithography Chemical Company (MCC), which is a single component resist composed of poly(4-hydroxysterene) (PHOST). The samples were exposed on either a 193-nm SVGL Micrascan prototype 0.5-NA step-and-scan lithography tool. More resist processing details are referred to reference 1. Table 1 summarizes the results found from top down SEM measurements of LER.

		Exposure			LER Result (Top Down SEM)	
Process	Resist	Tools	Development	sigma(nm)	Indicated Range(nm)	Period (nm)
TSI	MX-P7	193	Dry (O2)	5	25	<90
TSI	MX-P7	193	Dry(C2F6+O2)	2	9	>100
TSI	NEK 304	193	Dry(CF4+O2)	4	15	>100

Table 1 (reproduced from Reference 1) - Line edge roughness measured for three different resist schemes. Measurement taken on a 175-nm isolated line at best dose and best focus.

Details of the metrology tools used for measurement of line edge roughness will be discussed later. The numbers in table 1 were obtained at best dose and best focus and represent minimum LER measured. The results show that resists without breakthrough etch (Dry O_2) contains very high LER. Breakthrough etch is a proposed method, through wet- or dry-developed means, to improve LER. For example the dry-developed breakthrough often uses a low selectivity (~ 1:1 silylated-to-unsilylated) plasma etch

prior to the oxygen-plasma-based transfer. More details on this proposed method are found in reference 1. Top down SEM images and plots of LER fluctuations are shown in Figure 1 and 2 below.

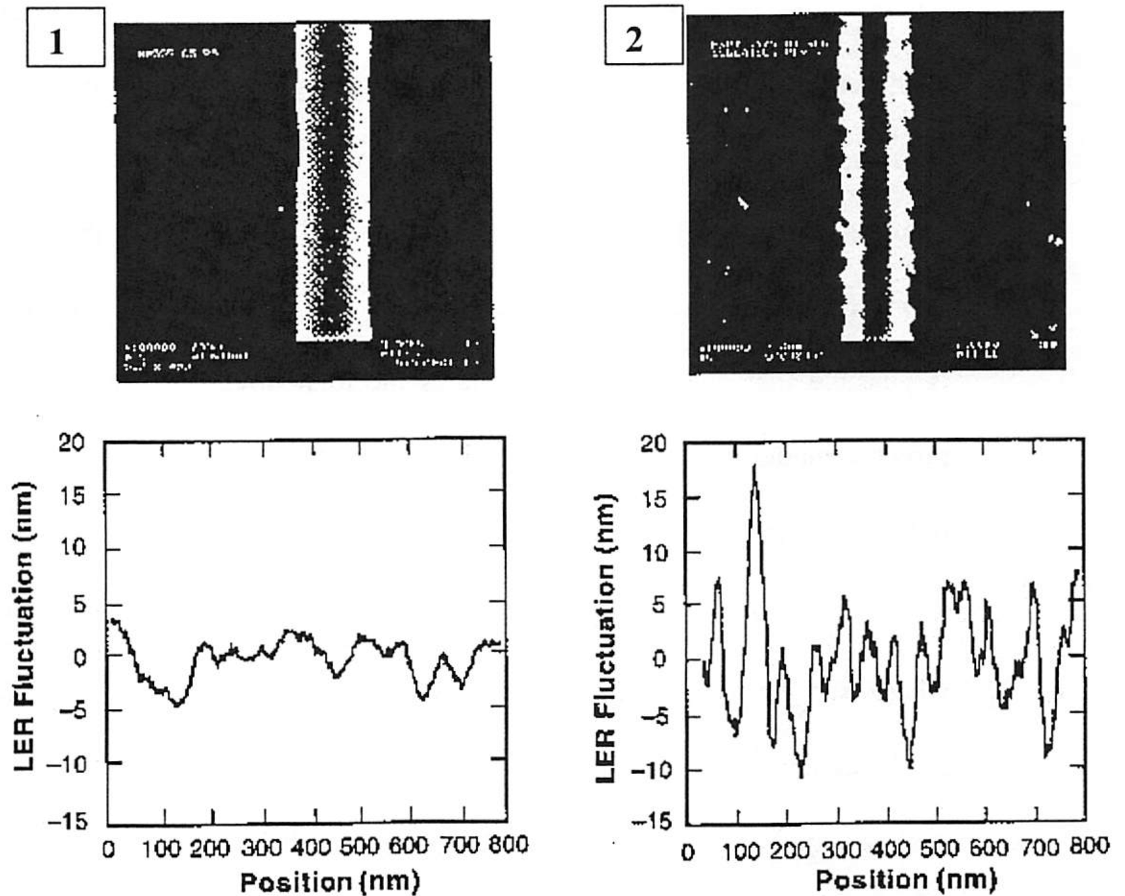


Figure 1&2 (reproduced from Reference 1) - Top-down SEM images and plots of LER fluctuations for nominal 175-nm isolated line in (1) TSI (MX-P7) with a C_2F_6+O2 breakthrough etch and (2) TSI (MX-P7) without a breakthrough etch

One can see from Figure 2 that LER with Indicated Range of 25nm with RMS value of 5nm is possible unless some improved methods limit the range of LER smaller as seen in Figure 1. More evidences of LER will be presented in the next section as we introduce

the causes and methods of measuring LER in order to further convince the readers that LER takes a significant portion of the total gate length.

2.02 Factors Contributing to Line Edge Roughness:

There are many contributing factors to the line edge roughness of the gate. Among those, the most important factors include: the roughness transferred from the mask features to the resist via aerial image, aggregation of polymers during development process, non-uniform diffusion and reaction of photo-generated acid at the boundary between the exposed and unexposed regions, and the statistical shot noise effects in the exposure process. Although each of the above factors contributes at a different degree, it is possible that one of them dominates the total effects. Reynold et. al.[2] suggested a possible model describing the contributions of the various factors that contribute to the overall roughness, σ_{total}, as followed.

$$\sigma^2_{total} = \sigma^2_{mask} + \sigma^2_{shotnoise} + \sigma^2_{diffusion} + \sigma^2_{development} + \sigma^2_{aerial} \quad (1)$$

where σ is the roughness due to each component assuming they add statistically. This model assumes that each factor contributes independently. However, it may not be the case in actual process because some of them may be coupled. For example the mask and aerial image effects are coupled and acid diffusion and shot-noise effects could be coupled also[2]. To understand the contribution to LER of each factor, it is necessary to investigate them separately.

2.02.1 Effects of Polymer Aggregates on LER:

Recently, granular structures in resist films have appeared to cause LER. Yamaguchi et. al. had found that granules are made up of polymer aggregates[2]. Granular morphology was observed in the pattern sidewall[4]. Granular structures more than 30 nm in the diameter had been observed on the surface. These structures are polymer aggregates. When resist films containing such aggregates are developed, the development rate becomes uneven. The polymer surrounding the aggregates dissolves faster, because the developer molecules diffuse faster in area around the aggregates than in the aggregates due to polymer density difference. As a result these polymer aggregates, which are not dissolved, are separated from the surrounding polymers by dissolution and extracted into the developer as shown in Figure 3.

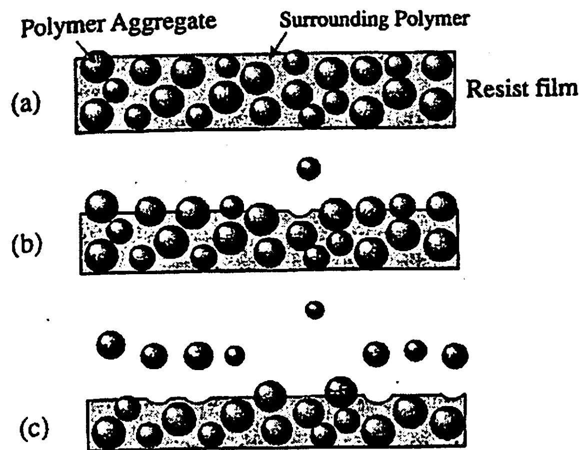


Figure 3 (reproduced from Reference 5) – Schematic diagram of aggregate extraction development

When resist film containing these aggregates are developed, many aggregates remain trapped in the pattern sidewall or edges. That means part of the aggregate shapes appear in the pattern edge or sidewall and cause some LER. Polymer aggregates had been confirmed in both positive and negative resists[4].

2.02.2 Effects of Aerial Image Contrast on LER

Another cause of LER links to aerial image contrast (AIC). Varying AIC on the imaging properties of a single-layer photoresist showed that LER increased with decreasing AIC[3]. A deep-UV interferometric lithography (IL) was used to study AIC effects at the sub-100 nm scale. The readers are referred to reference 3 for IL experimental set up. The technique allows independent control of the dose, pitch and AIC during exposure. The IL tool provides the imaging interference pattern by splitting and recombining a continuous-wave beam at 257 nm. By using a dual exposure sequence the modulation of the IL image can be varied in a controlled manner. Each site is first exposed with a two-beam imaging exposure, followed with a flood exposure using a single beam. Thus any desired image contrast can be achieved by appropriate selection of the two doses. Below is some of the results showing that LER increases with decreasing contrast for different resist materials and different development conditions[3].

PHOTORESIST	ARC	PAB (°C/time)	DOSE (mJ/cm²)	PEB (°C/time)	Developer/ time
Positive-tone CA					
Shipley UVII-HS	BARL-900	130/60 sec.	2.5	140/90 sec.	Shipley CD-26/30 sec.
UV5	BARL-900	130/60 sec.	2.86	140/90 sec.	Shipley CD-26/30 sec.
UV6	BARL-900	130/60 sec.	2.6	140/90 sec.	Shipley CD-26/30 sec.
Negative-tone/Aqueous base developed CA					
CGR2205	AR3-600	95/60 sec.	1.9	95/60 sec.	0.14N Shipley CD-26/60 sec
Shipley UVN30	AR3-600	110/60 sec.	2.5	95/60 sec.	Shipley CD-26/30 sec
[a] CGR (2.5K MW)	AR3-600	95/60 sec.	1.43	95/60 sec.	0.10N Shipley CD-26/60 sec
[a] CGR (8K MW)	AR3-600	95/60 sec.	1.1	95/60 sec.	0.13N Shipley CD-26/60 sec
[a] CGR (15K MW)	AR3-600	95/60 sec.	1.25	95/60 sec.	0.19N Shipley CD-26/60 sec
Negative-tone/Organic solvent developed CA					
SU8		85/3 min.	0.8	90/3 min.	[b] PGMEA/45 sec.
Non-Acid Catalyzed					
[c] Clariant AZ7905	XHRi-16	110/2 min.	136	135/90 sec.	1:4 AZ400K:H_2O/60 sec.

[a] prepared from monodisperse polyhydroxystyrene (pHOST)
[b] Propylene glycol methyl ether acetate
[c] exposed at 364 nm wavelength

Table 2 (reproduced from Reference 3) – Resist materials and their processing conditions

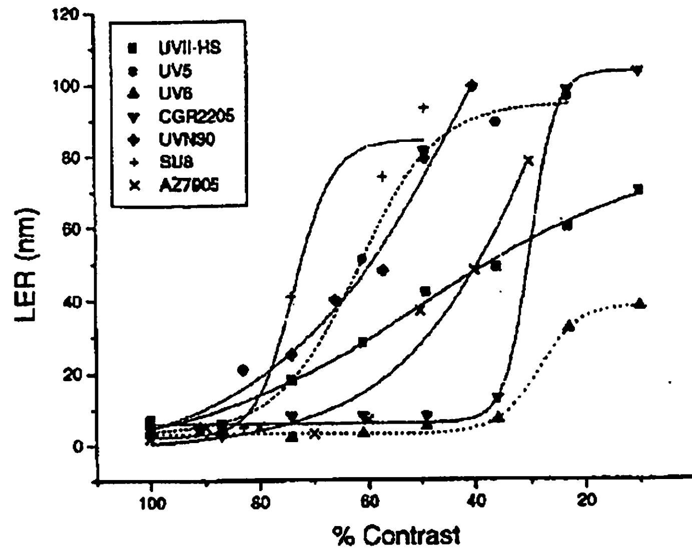


Figure 4 (reproduced from Reference 3) – Line Edge Roughness decreases as function of image contrast

At maximum aerial image contrast (100% intensity modulation of the aerial image), all materials display very low LER (~2% of the linewidth). As the aerial image contrast decreases, the magnitude of LER increase. At certain threshold % contrast value, LER jump from a very small value to a significant value. Different materials display different threshold percent contrast value. This suggests that resist composition play a significant factor in the relationship between AIC and LER, although no specific class of resist under study offers a distinct advantage.

2.02.3 Effect of Mask Defects on LER:

Mask pattern is used to define the images. It is likely that any mask roughness or defect will influence the overall roughness in the resist. Small mask defects or roughness show perturbations to the linewidth[2]. Reynold et. al. found that large defect bumps in the mask are transferred as grooves or columns onto the resist sidewall. If the roughness does not depend on the mask, changing the mask should not significantly change the characteristics of the resist roughness. Reynold did an experiment with different mask

with different roughness. The study found that the average RMS roughness increases with the roughness of the mask as shown in the following figures.

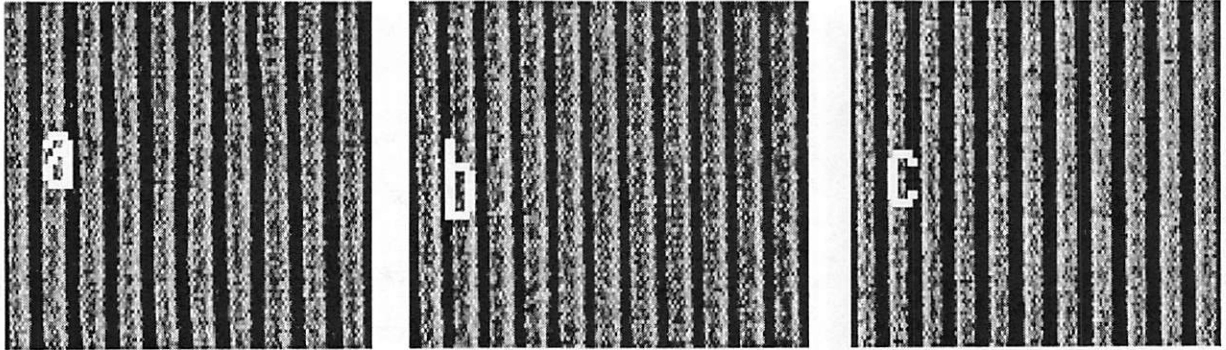


Figure 5b (reproduced from Reference 3)- SEM images of mask grating patters. (a) Poorly formed grating pattern on replicamask. (b) Better grating pattern on replica mask. (c) Original grating pattern on IBM mask.

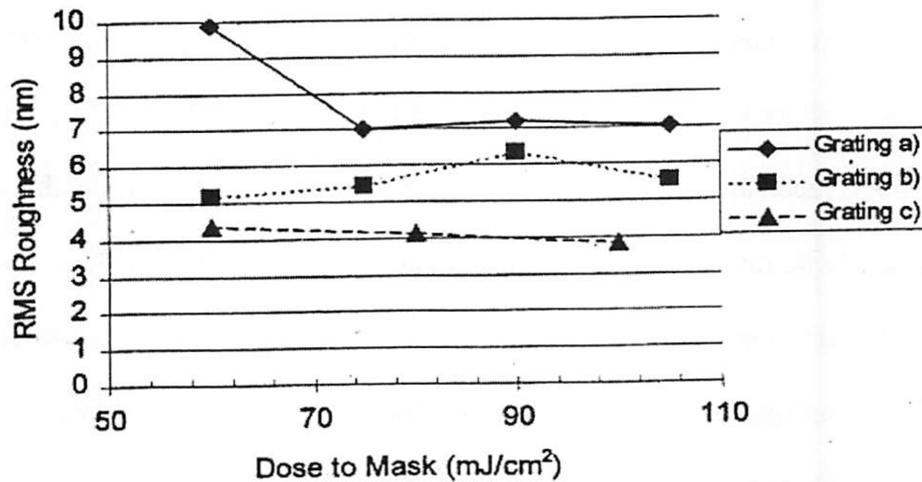


Figure 6 (reproduced from Ref. 3) - LER for samples exposed through grating (a), (b), and (c) as shown in Figure 4.

Figure 5 shows that LER is substantially larger for resist sidewall exposed through the (a) grating than the other two. RMS roughness for (b) grating is also larger on average than that of the original mask pattern (c). Thus it is plausible to conclude that roughness and defects on the mask do transfer onto the resist patterns and contribute to the overall roughness.

2.03 Transfer of LER from Resist Pattern to Etched Pattern:

In the process of gate formation, photoresist is used as etch mask. We have seen that mask defects and roughness contribute to resist LER. Undoubtedly, LER observed for photoresist would also be transferred onto the etched pattern with some variations. Namatsu[5] measured LER of Si patterns etched using the resist patterns as an etching mask to examine how resist LER are transferred to the etched patterns. Using two different resist materials, Figure 7 and 8 show how resist LER is faithfully transferred into the etched Si pattern[5].

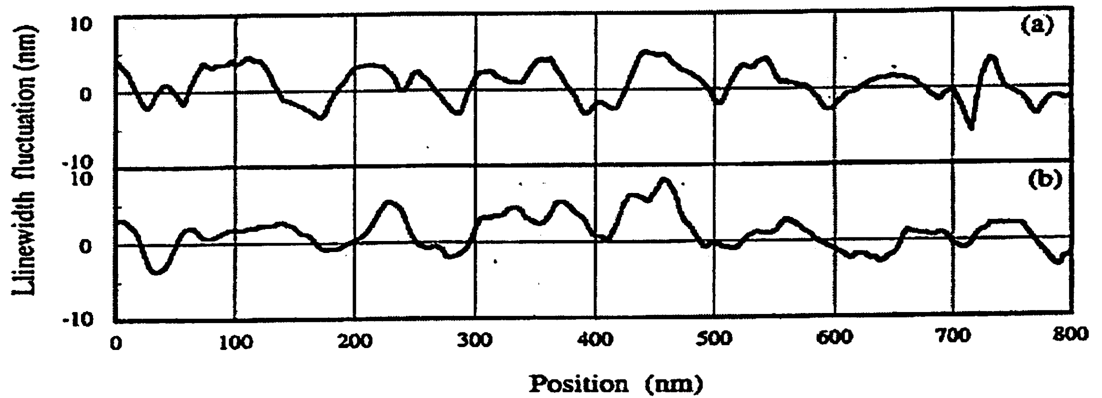


Figure 7 (reproduced from Ref. 5) – Linewidth fluctuation in a (a) SAL-601 (from Shipley) resist pattern and (b) Si line pattern etched using SAL-601 resist as mask

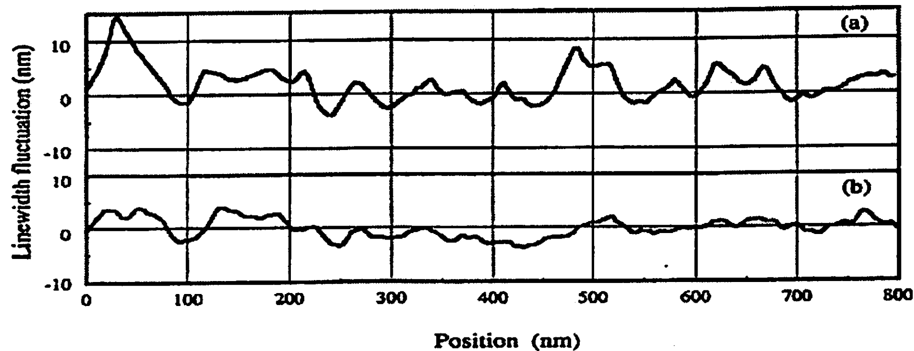


Figure 8 (reproduced from Ref. 5) - Linewidth fluctuation in a (a) ZEP-520 (from Nippon Zeon) resist pattern and (b) Si line pattern etched using ZEP-520 resist as mask

Figure 7 and 8 show that the Si etched pattern inherits LER characteristics from resist LER.

2.04 Metrology Methods for Measuring and Quantifying LER:

This section will discuss the metrology methods for measuring and quantifying line edge roughness. Scanning Electron Microscope (SEM) and Atomic Force Microscopes(AFM) are the two major technologies that are used to measure line edge roughness. Each method has been evaluated by Nelson from SEMATECH and Palmateer from Lincoln Laboratory, MIT. We will present their findings in the following sections.

2.04.1 Scanning Electron Microscope (SEM) method:

Line edge roughness was measured by taking top-down SEM images of isolated lines. The SEM images were then imported into the CD (critical dimension) measurement module software developed by SIS, Inc. In the software, there were several algorithms and parameters that the users could pick to determine the edge of a feature from the magnitude of the secondary electron signal. First, a frame was selected by the user to determine the area in which the computer was allowed to search for the feature edge. Then the computer used the chosen algorithm and threshold % value to find the feature edge. After the feature edge data was found, those that lie more than 2 σ from the mean were removed using a noise filtering option. The points that lie more than 2 σ from the means usually are measurement algorithm error and have values of zero. The data was then exported to spreadsheet and normalized. The single-sided LER was then reported as the standard deviation (1σ) and total indicated range (TIR) of the values. All LER values were visually verified against tilted SEM images in the high resolution SEM of the same feature edge[6]. SEM technique for LER measurement is more sensitive to

parameters that affect the SEM resolution than for software parameters. In one study Nelson et. al. varied the stigmation of the SEM to significantly decrease the resolution of the SEM as shown in Figure 9.

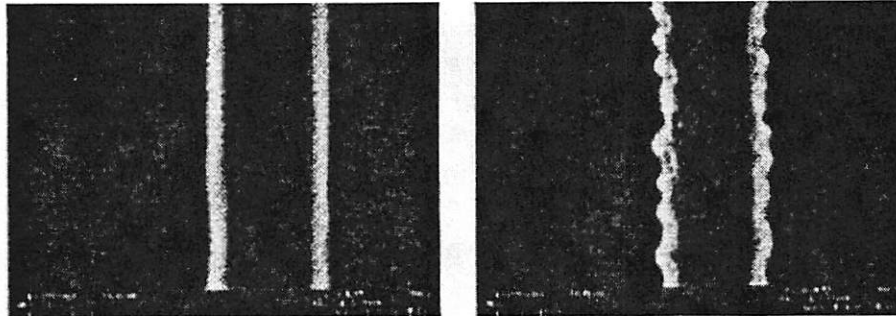


Figure 9 (reproduced from Ref. 6) – SEM images of the same feature with different stigmation settings.

The roughness measured for the image taken with incorrect stigmation setting was 3nm (1σ) and 13nm (TIR). However, the roughness of image with correct stigmation setting was 23nm (1σ) and 67nm (TIR)[6].

2.04.2 Atomic Force Microscope (AFM) Method:

Whereas SEM method can not be used to measure the edge roughness below the top surface, AFM method allows the user to measure roughness at certain level of the sidewall. Using AFM for measuring and calculating the edge roughness, features were scanned with a conical shape probe tip. The features were scanned perpendicular to the feature so that the tip rode up and over the feature. The scan was run in the non-contact tapping mode where the tapping was in the vertical direction. The sample needed to be carefully checked to make sure that the non-contact tapping mode always operated so that the sample surface was not damaged. The check was done by scanning an area where ten previous scans were run. If no change or dimpling of the surface occurs, the check is done[6].

A typical probe has a tip radius of 5-10 nm, a scan length of 1-2 μm with 512 samples, and a scan rate of 1 Hz. The AFM resolution depends on the tip radius of the probe, the cone angle of the probe, the surface relief, the scanning rate, and the scanning resolution. If the surface is flat, the measurement is limited by the tip radius and the scanning resolution. However, if the surface slope is larger than the cone angle of the probe, then the measurements is limited by the sidewall of the probe. The feature line edge was determined as the height value of the specified threshold % value. Then the distance from the edge of the scan to the feature edge was calculated. Similar to SEM data, all distance values were checked for any error (larger than 2 σ) and removed before being exported into spreadsheet and normalized. The edge roughness was reported as the standard deviation (1σ) or TIR. LER values were visually verified against the tilted high resolution SEM images of the same feature edge[6].

2.04.3 SEM and AFM Comparisons:

SEM measurement had been found to have lower 1σ edge-roughness value than AFM measurement, although both methods were able to follow the general changes in the edge roughness. The difference was attributed to different calibrations and underestimation of the edge roughness by the SEM. SEM underestimates the edge roughness because it represents the edge roughness by only one dimension with its top-down SEM image. The top down image does not provide any changes in the edge roughness from the top to the bottom of the feature without taking additional SEM images where the sample is tilted and rotated. However, AFM measures the sidewall which contains two dimension information. Although SEM may underestimate the edge

roughness, SEM can still measure the relative changes in edge roughness and is highly recommended over AFM because of it high throughput[6].

3.0 Effects of LER on Device Characteristics Simulations

3.01 Simulation Plans:

The simulation can be divided into three major phases. The first phase is to design a good device. Our target device is 100-nm NMOS, which is subject to short channel effects that are not seen in long channel devices. Therefore, we need a device whose parameters are well controlled and resemble a real working device. This device will be used as the reference device for comparisons between the rough gate and smooth gate device. The second phase is to simulate a device with single, rectangular or square defects. This single defect simulation allows us to gain more insights into the trend of roughness effect so that we can focus on what is dominant factor affecting the device performance. The third phase is the most challenging and most exciting phase, which we actually simulate the device with random roughness.

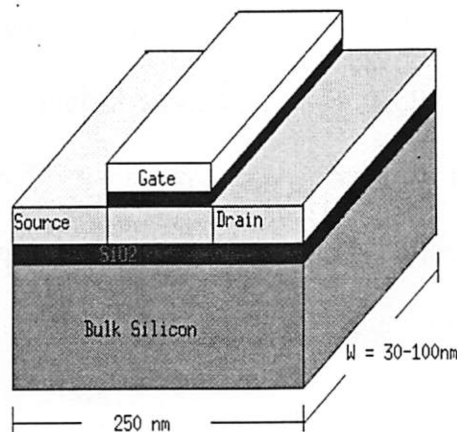
3.02 Base Device Design:

The selected device is an NMOS, fully depleted silicon-on-insulator (FDSOI) with nominal channel length of 100 nm. The main reason we chose the SOI device is the ease of device structure design. SOI device offers superior short channel effect tolerance over bulk devices. Nonetheless, there are several important issues in designing the base design, which will be addressed.

The work was first simulated by Silvaco-ATLAS device simulator. ATLAS offers very good and fast 2-D and 3-D simulation time. However, the simulator lacks

several important short channel models such as velocity overshoot and energy balance models. Furthermore, the simulator does not offer a solution to construct a gate with random roughness and doping roughness which are the heart of this project. The Integrated System Engineering (ISE) simulation tools offer what the project needed. It includes a good 3-D simulation tool (DESSIS) with advanced models for short channel devices. It allows us to work with the input deck such that we could construct the random gate roughness with the same rough doping profile for our simulations.

The schematic structure of the SOI device structure is provided in Figure 10 shown below.



- Total Device Length = 250 n
- Nominal Channel Length = 100 nm
- Channel Width = 30-100 nm
- Buried Oxide = 100 nm
- Si Film Thickness = 25 nm
- Gate Oxide = 30 Å

Figure 10 – Schematicstructure of the base SOI device

The nominal channel length was 100 nm. The effective channel length after implantation and diffusion was 85 nm. The substrate doping was selected at ~ $1E18/cm^3$ with Boron so that the threshold voltage was about 0.3-0.4 Volts. The source and drain was doped with Arsenic at $2E20/cm^3$. The polysilicon gate was heavily doped with arsenic at around $7E19/cm^3$. Since the channel length is very short, the gate needs to have a very good control of the channel. Thinning gate oxide and shallowing source/drain layers are known to be very effective ways of preventing short channel

effects[8]. Therefore, the oxide thickness was reduced to 30-Å and the film thickness was 25 nm to give a good sub-threshold swing.

3.02 Short Channel Effects(SCE) Considerations in FDSOI Design:

Although fully depleted SOI device has shown to have highly suppressed short channel effects over bulk devices, drain induced barrier lowering (DIBL) effect, which ties to Vt roll-off is not negligible and needs to be addressed in more details. As the channel length decreases, the barrier height for channel carriers at the edge of the source near the surface is lowered by the drain electric field. The barrier height for the channel carrier should ideally be controlled by the gate voltage for maximum transconductance. However, the barrier height for channel carriers is affected by the drain voltage in addition to the gate voltage. Therefore such interference from the drain voltage degrades the controllability of the gate voltage to drain current[8]. The physical mechanisms behind DIBL effect can be illustrated in Figure 11.

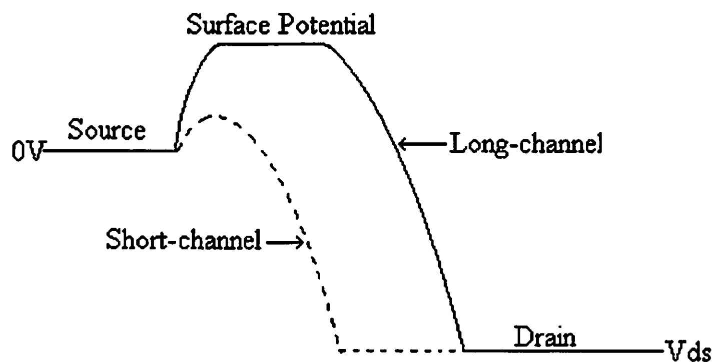


Figure 11 – Barrier Height and Potential along the channel for a short and a long L device

The barrier heights for the electrons (in NMOS) are compared for a long channel and short channel device. In long channel device the barrier height is relatively insensitive to the drain voltage. However the barrier height is substantially reduced by the drain voltage for short channel devices. Even when the drain bias is 0 volt, the barrier

height in the short channel is lower because the built-in potential of the S/D junctions becomes a significant contribution for short channel devices. Reducing the barrier height will lower the threshold voltage[9].

The Quasi-2D model has been developed by Liu by applying Gauss's law to a rectangular box (Gaussian Box) of height X_{dep} and length Δy in the channel depletion region as shown in Figure 12.[10]

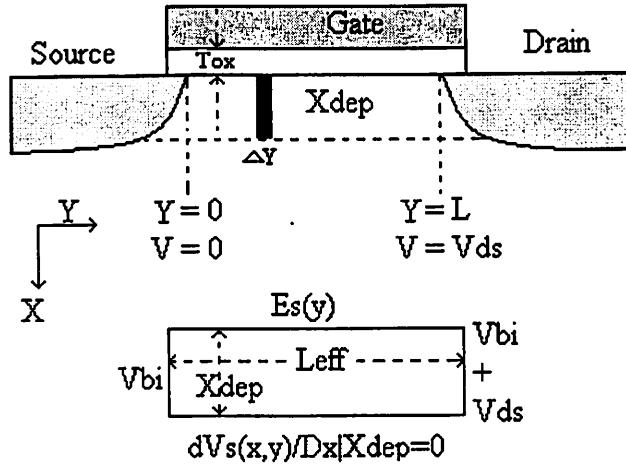


Figure 12 – The Gaussian box used in Quasi-2D analysis and boundary conditions

The threshold voltage shift can be derived from the following equation:

$$\varepsilon_{Si}\frac{X_{dep}}{\eta}\frac{dE_s(y)}{dy}+\varepsilon_{OX}\frac{V_{GS}-V_{FB}-V_s(y)}{T_{OX}}=qN_{SUB}X_{dep} \quad (2)$$

Where $E_s(y)$ is the lateral surface electric field, $V_s(y)$ is the channel potential at the Si-SiO_2 interface, V_{GS} is the gate-source voltage, V_{FB} is the flatband voltage, N_{SUB} is the channel doping, T_{OX} is the gate-oxide thickness, and ε_{si} and ε_{ox} are permittivity of Si and SiO_2 respectively and η is the fitting parameter. X_{dep} is the depletion width and is defined as: $X_{dep}=\sqrt{2\varepsilon_{Si}(\phi_s-V_{BS})/(qN_{SUB})}$, where V_{BS} is the substrate bias, $\phi_s = 2\phi_B$ is the surface potential at the onset of strong inversion. The first term on the left-hand side

of equation 2 represents the net electric flux entering the Gaussian box along the y direction; the second term is the electric flux entering the top surface of the Gaussian box. No net electric flux passes through the bottom of the Gaussian box. Further analysis and derivation of the threshold voltage shift, ΔV_{th}, can be found in reference 10. ΔV_{th} can be expressed as:

$$\Delta V_{th} = [2(V_{bi} - 2\phi_B) + V_{DS}](e^{-L/2l} + 2e^{-L/l}) \quad (3)$$

However, equation (3) is only valid for small value of V_{DS}. When V_{DS} is not small, for $l \ll L$, ΔV_{th} has been derived as[10]:

$$\Delta V_{th} = [3(V_{bi} - \phi_s) + V_{DS}]e^{-L/l} + 2\sqrt{(V_{bi} - \phi_s)(V_{bi} - \phi_s + V_{DS})}e^{-L/2l} \quad (4)$$

Equation (4) reduces to (3) for small V_{DS} and large L/l as expected. Equation (3) & (4) predict that the threshold voltage reduces rapidly as L decreases; a higher channel doping level, a lower S/D doping level, or a thinner Tox, all of which reduce l, will help to suppress large threshold voltage shift, V_{th} roll-off.

While designing for the base device, all of the above SCE was carefully considered such as reducing the oxide thickness, increasing substrate doping, reducing the film thickness within the acceptable standard set by the SIA roadmap. However, pocket implant was also needed to further reduce the SCE in our device. Pocket or Halo implant is a popular technique for improving SCE. While substrate doping increases the doping level throughout the entire device, causing device degradations, pocket implants can locally place the implanted ions near the location where it is needed the most around the drain and source. Since our device film is very thin, the pocket implant is almost a step implant profile. For a step implant profile, the threshold voltage shift, ΔV_{th}, has been modeled as[11]:

$$\Delta V_{th} \approx -(V_{DS}+2)e^{-L/l} + 1.8(\kappa-1)\sqrt{V_{DS}+0.8}e^{-L/2l} \quad (5a)$$

$$\kappa \approx \sqrt{\frac{V_{th}\ln\frac{N_p}{N_{SUB}}}{V_{DS}}\frac{L_p}{l}} \quad (5b)$$

where N_p is the pocket implant concentration, L_p is the pocket implant length from the source/drain to the background channel doping. From equation (5) we see that one can vary the value of κ to adjust V_{th} shift to an acceptable level down to some length below the target channel length. Each κ has many combinations of N_p and L_p; one can select an optimal L_p and N_p combination in the design.

Halo implant was incorporated to our device model. N_p was selected to be twice the background doping (~2e18/cm^3), and L_p was about 13 nm. The device show significant V_{th} roll-off improvement as shown in Figure 14. Figure 13 shows the I_{DS} – V_{GS} of the base device.

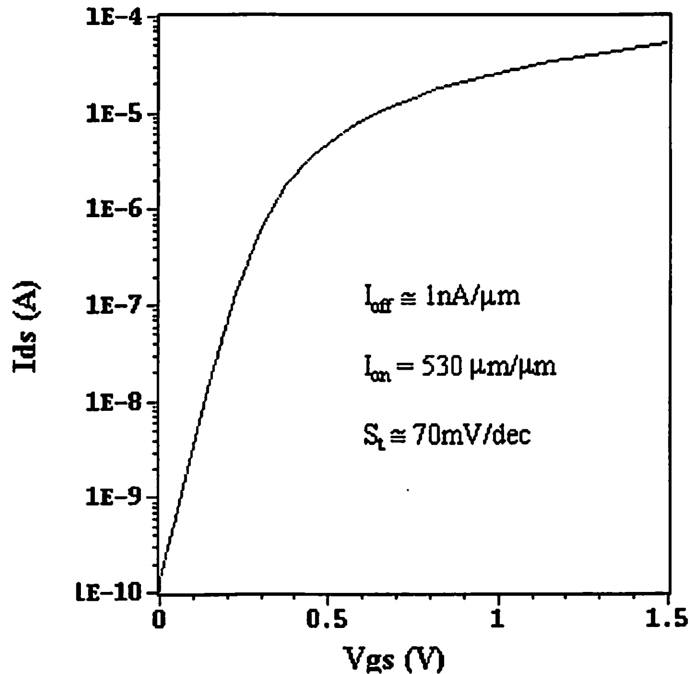


Figure 13 – Drain Current Vs. gate voltage @ Vds =1.1V for 100 nm channel width

The base device shows very good subthreshold swing for a FDSOI with 70mV/dec. Ioff is defined as Ids at Vds =1.1V and Vgs = 0V; Ion is defined as Ids at Vds =1.1V and Vgs = 1.5V

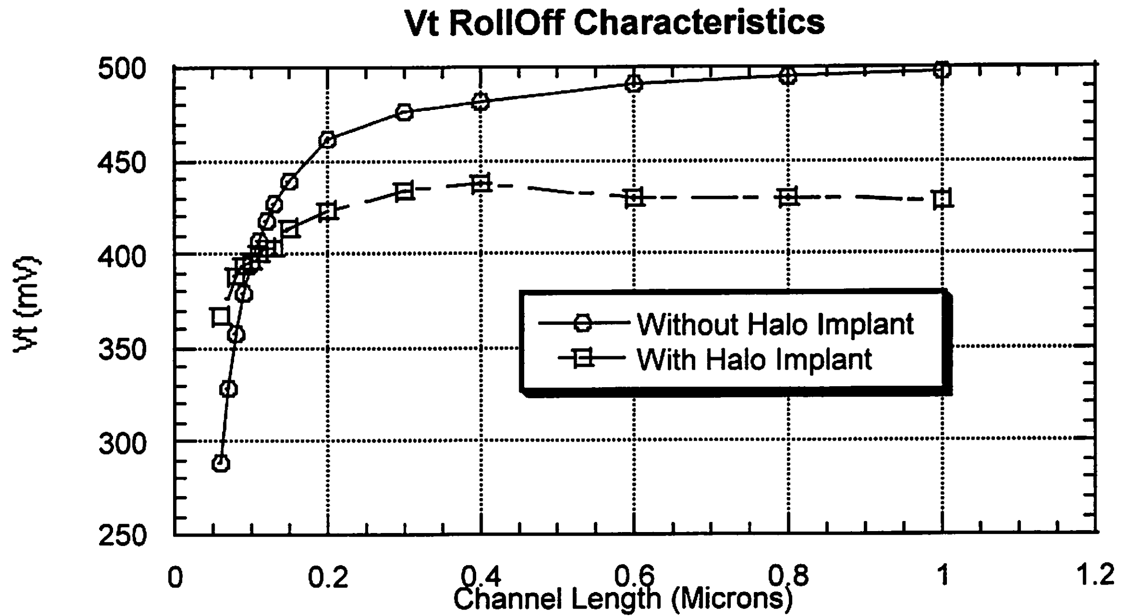


Figure 14 – V_{th} roll-off characteristics for the base devie with and without halo implant

Figure 14 shows that without pocket implant V_{th} starts to roll off at 0.2 μm. With the pocket implant, V_{th} roll off is suppressed down to about 0.07 μm.

4.0 Single Defect Simulations, Results and Discussions:

Before simulating complicated, random rough-gate devices, simulations of simple rectangular gate defects provide very good physical insights into the effect of the roughness. The results help explain the effects observed on real rough-gate devices.

Single rectangular defects placed at the center of one side of the gate edges as shown in Figure 15. Defect length and width were systematically varied. Defect length follows the direction of the channel length, and defect width follows the direction of the channel width.

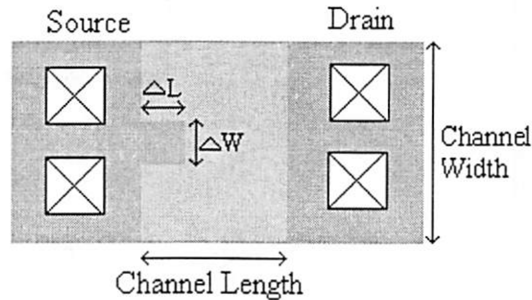


Figure 15 – Top view schematic of single defect simulation

First, defects of 20-nm width were varied in length. Plots of Ioff and Ion for different defect lengths are shown in Figure 16. The doping profile is abrupt (no S/D diffusion).

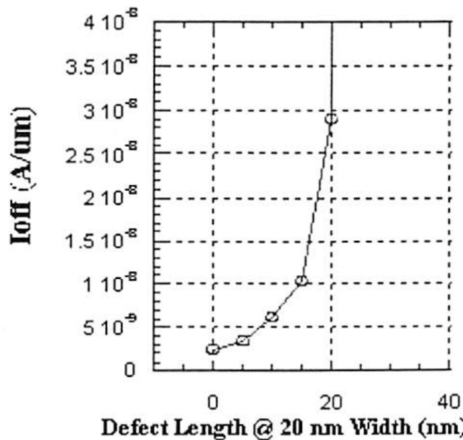


Figure 16a – I_{off} increases with defect length

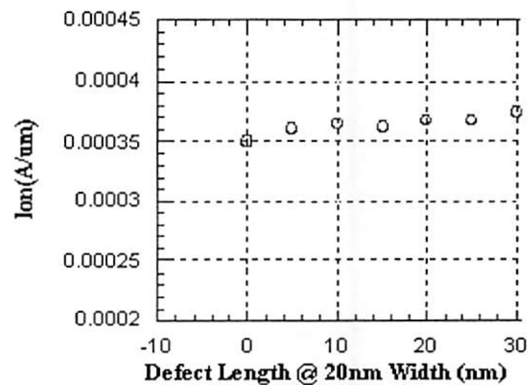


Figure 16b – I_{on} slightly increases with defect length

The off-state current was very sensitive to increases in the length of the defect. Figure 16a shows that Ioff increases non-linearly with defect length while Ion only marginally increases. The cause of such a non-linear increase in I_{off} will be explained later. The sub-threshold swing was observed to increase very fast when the defect length was longer than 15 nm and also the threshold voltage rolled off extremely fast. This occurs because the short part of the device with L_{short}, due to the increase of defect length, passes the minimum allowable effective length, L_{min}, that was designed for the base design.

Next, the width of the defect was varied while keeping the defect length at 20 nm. The simulation result showed that I_{off} increased linearly with width variation; I_{on} also increased marginally and linearly as shown in Figure 17. The reasons will also be explained in the next section. Nevertheless, as one might have anticipated, the drain current especially the off-state current was extremely sensitive to defect length increment. This is very true with decreasing channel length of a device in deep sub-micron region. The effect of the defect width on I_{off} and I_{on} contributed in a predictable, linear fashion.

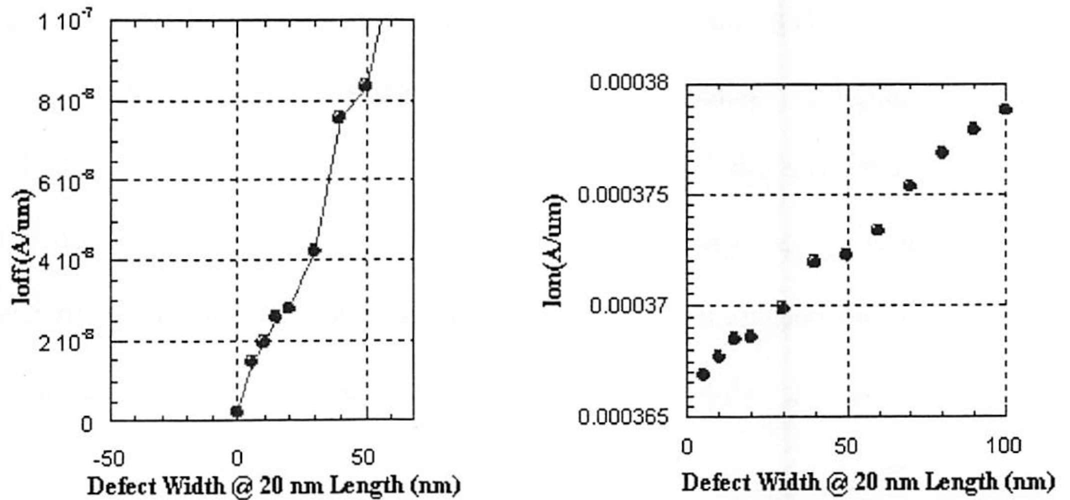


Figure 17 – Linear increase of I_{off} and (b) I_{on} with defect width

To help explain such large increase in leakage current observed above, a 20nm by 20 nm defect placed at the center on one side of the gate as in Figure 15 was simulated. In one simulation, the total drain current was obtained from a single device with the 20nm-by-20nm defect simulation. In another simulation, the 20nm-by-20nm gate defected device was broken into three devices: one with 80-nm gate length and two with 100-nm gate length as illustrated in Figure 18.

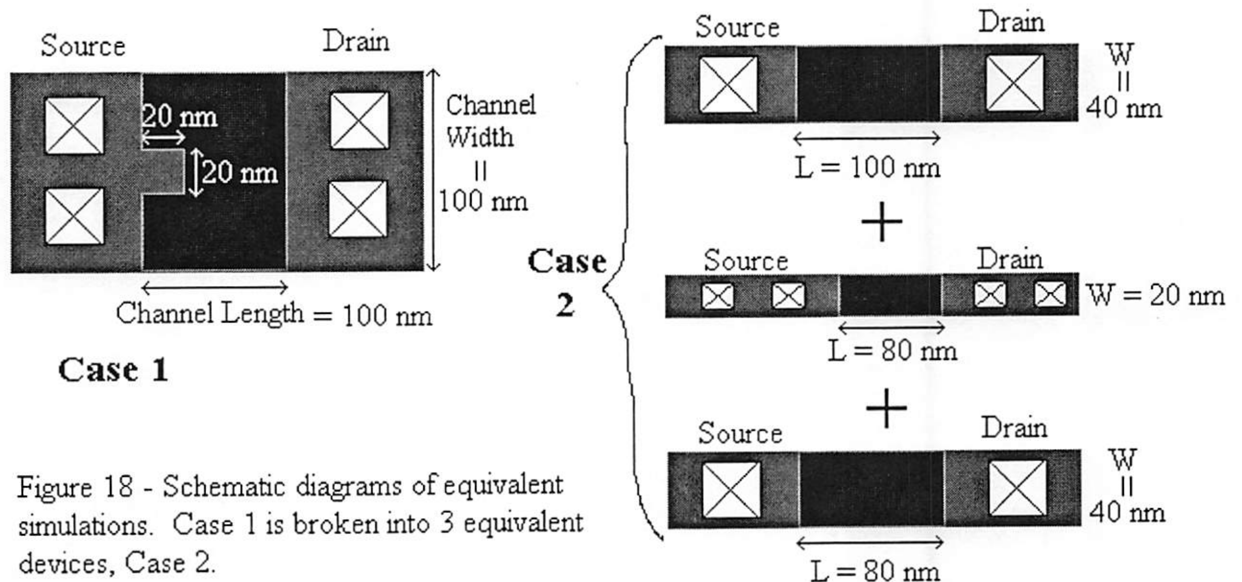


Figure 18 - Schematic diagrams of equivalent simulations. Case 1 is broken into 3 equivalent devices, Case 2.

The simulation result from Case 1 in Figure 18 should be equals to the result from Case 2 if there is no 3-D interactions going on because of the defect. The simulation result showed that I_{off} from Case 1 was 126% higher than Case 2; I_{on} from Case 1 is 19.2% higher than Case 2. The reason for such higher leakage increase observed in Case 1 is because of the high electric field at the two corners of the defect. The field at the corners are enhanced by the drain voltage surrounding the corner. Therefore, the field at the corners is much higher, more band bending at zero gate voltage, and thus higher leakage current. Similarly, at the on state, the electric field at the sharp corner is enhanced by the nearby gate voltage, causing the on state current, I_{on}, to be slightly higher. However this enhanced etch field effect disappeared when we introduced lateral diffusion into our model. Real devices all have lateral strangle from ion implantation and lateral diffusion due to high temperature processes.

The abrupt junction (or non-lateral diffusion) simulation showed strong enhanced E-field effect when there were sharp corners. Next we introduced lateral diffusion parameters into the device model with a lateral diffusion length of 8 nm. Again, the two simulations similar to Case 1 and Case 2 shown in Figure 18 were run. Lateral diffusion clearly smoothed out the sharp corners as shown in Figure 19. Therefore the impact of high field at the corner would be greatly reduced. However, the current result simulated for Case 1 and 2 this time still showed that I_{off} in Case 1 is 115% higher than in Case 2; I_{on} in Case 1 is 17% higher than in Case 2. Although there was no enhanced corner field, another effect, namely 2-D lateral diffusion, emerged. Since implanted ion diffused in all directions, the defect size became larger after diffusion as shown in Figure 19, therefore

increasing the severity of the defect's effects on the device current. This effect will be shown to be the dominant contributor to the total LER effect on device performance.

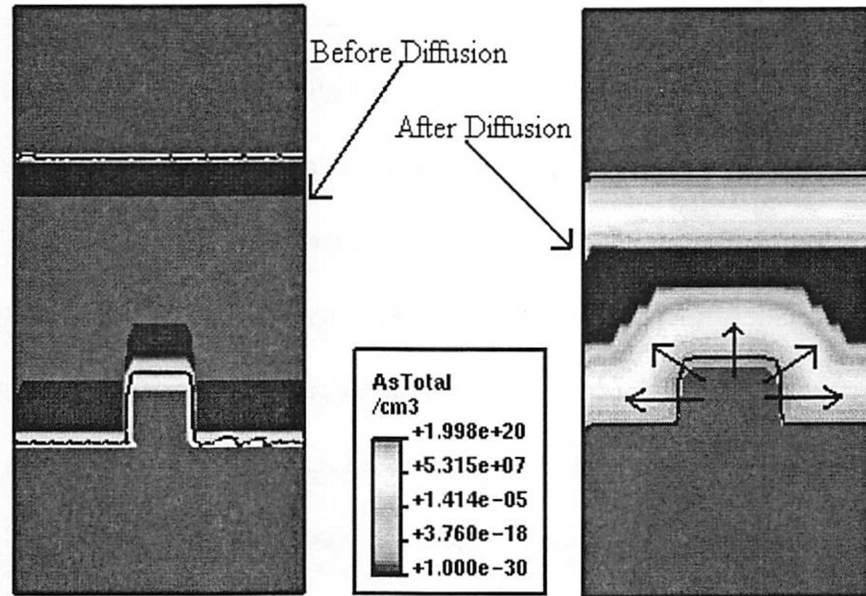


Figure 19- Top-view cross section of defects showing the square defect being smoothed out and enlarged by 2_D lateral diffusion. The arrows indicate the directions of 2-D lateral diffusion.

5.0 Line Edge Roughness Simulation Setup:

5.01 Line Edge Roughness Construction:

One of the difficulties in this project was to be able to create the waviness of the gate and input that into the simulator in such away that the simulator could read and create the device geometry and doping profiles. Since ISE simulators allowed direct editing of the input deck for the boundary and doping command files, it was possible to automate a device with random rough gate. By following the format of the input decks, one could figure out which part of the input decks were used for device geometry definition. We used Matlab's white noise function to generate a band-limited white noise with a gaussian (normal) distribution. The white noise was then filtered to exclude the high frequency noise at some cut-off frequency, ω_c. Figure 20 shows a filtered band limited white noise and its power density function (PDF).

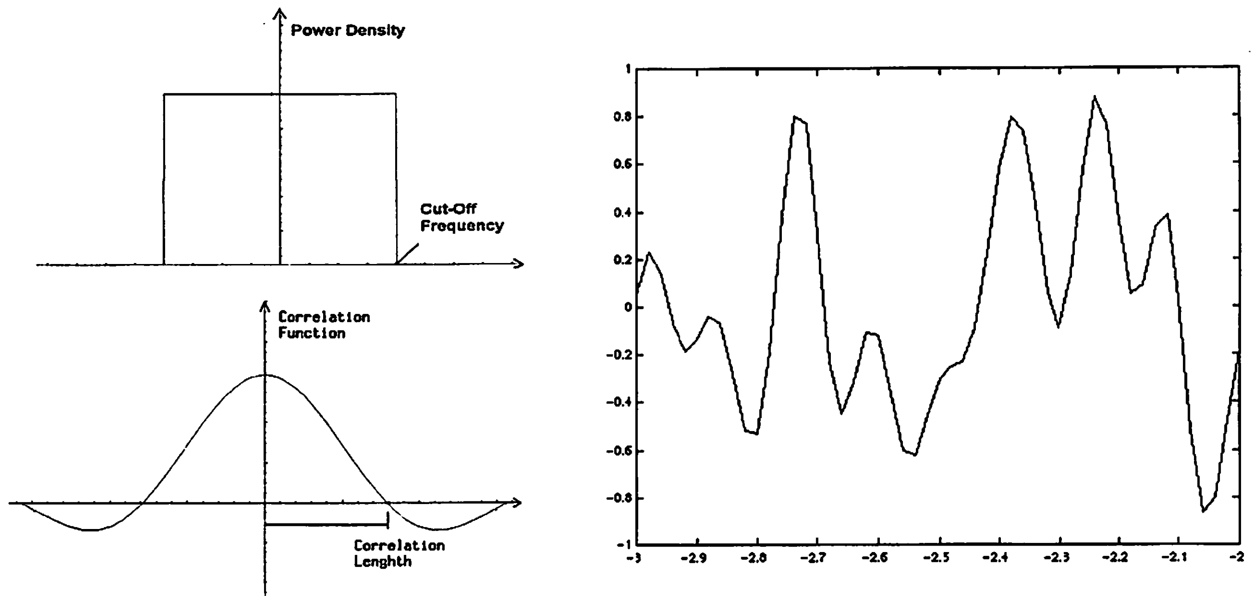


Figure 20 – The PDF of a filtered white noise at cut off frequency, ω_c and its corresponding correlation function and waveform.

The LER created in Matlab was controlled by two input variables: the correlative length, l_c and the square root standard deviation, RMS. The correlative length is related to the cut-off frequency as followed.

$$l_c = \frac{\pi}{\omega_c} \qquad (6)$$

Thus by varying the correlative length, one can decide which frequency for LER to operate at. The RMS roughness is defined as $\sqrt{\frac{\sum(x-\bar{x})^2}{n}}$

Since the simulator can only accept discreet points for the roughness, the output waveform was then sampled and digitized into step increment waveform as shown in Figure 21. The smallest increment step in Figure 21 10 Å.

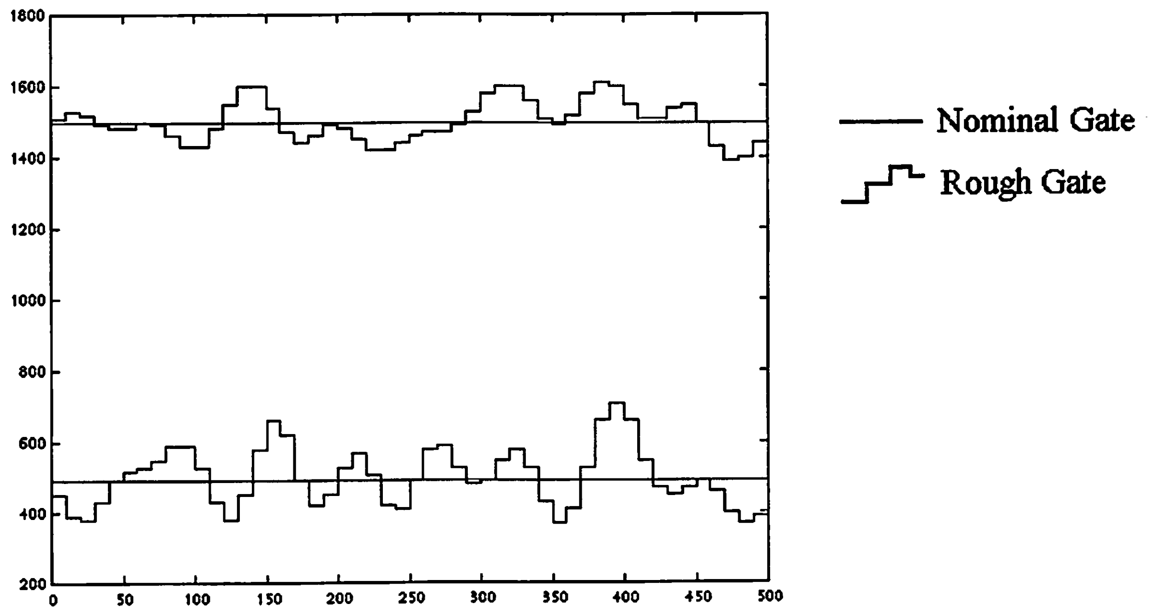


Figure 21 – An example of a discreet step in crease waveform.

5.02 Device Structure by 3-D Processing:

Construction of 3-D device with rough gate would not have been possible without the 3-D processing simulator, PROSIT. We used the waveform output generated by Matlab as input gate mask to PROSIT. The processing simulator would use the rough mask to develop the gate; it also used the mask for self-aligned source/drain and halo implantation as shown in Figure 22. Therefore the doping profile underneath the gate was automatically constructed.

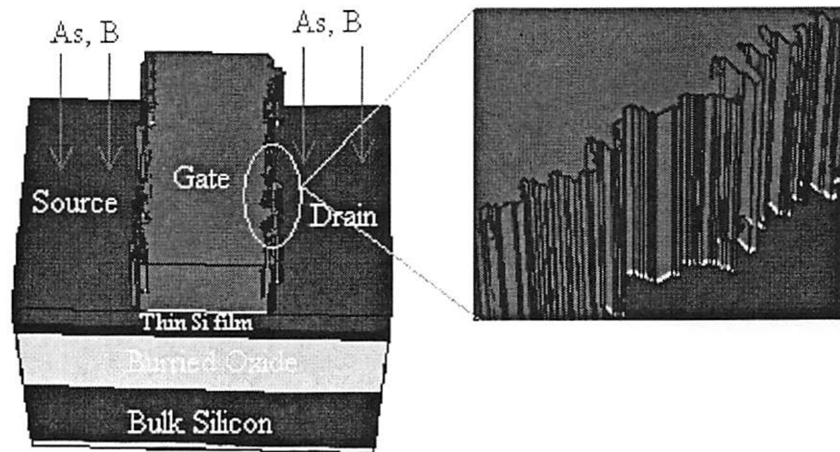


Figure 22 – 3-D view of a rough gate device fabricated using PROSIT with self-aligned As (for S/D) and B (for pocket implant) implantation.

PROSIT could only read in tens of nanometer. That means the smallest length and width is 10 nm. This was not good enough to create roughness that had spatial frequencies less than 10 nm. To resolve this difficulty, we constructed the device with smallest unit length and width of 100 nm. After the simulator fabricated the device, we scaled down the device dimensions 100 times smaller. Thus the scaled down device would have a smallest unit length and width of 1nm. We could have scaled down our device's unit length and width further but that would tremendously increase the grid size beyond the computation capability at our facility. Once we finished construction the

boundary profile and the channel doping profile, we proceeded with creating the mesh by using the simulator MESH. Since the device geometry contained a very rough gate boundary and a very rough doping profile underneath the gate edge, convergence error is extremely sensitive. Therefore we needed very small grid size in the region around the gate edge. The minimum grid size was 5 Å, which was half of the smallest unit length of our device. It is very important to have the same mesh for all simulations to have consistent results. Thus, we worked out the most critical device, which was most likely to have convergence instability first. Then we used such mesh file for all of the devices to keep our results consistent.

6.0 LER Device Simulations, Results and Discussion:

The simulation results for LER devices were obtained from the device simulator DESSIS from the Integrated System Engineering, Inc. The model used the drift diffusion current equations with most short channel effect models. Due to the complexity of the mesh structure and convergence sensitivity, the minority carriers (holes) were turned off; minority carriers contributed small current contribution and should not affect the relative change in current when we compared smooth-gate device and rough-gate device. First we simulated devices with different RMS roughness values while keeping the same correlative length. The roughness was only introduced on one side of the gate (source side) only because excessively large mesh file, long computation time (~10 hours each simulation), and large memory required (~1Gbytes). Without lateral diffusion, the junction was very abrupt. The source and drain doping follows the shape of the gate. Figure 23 shows the S/D doping for the rough-gate device.

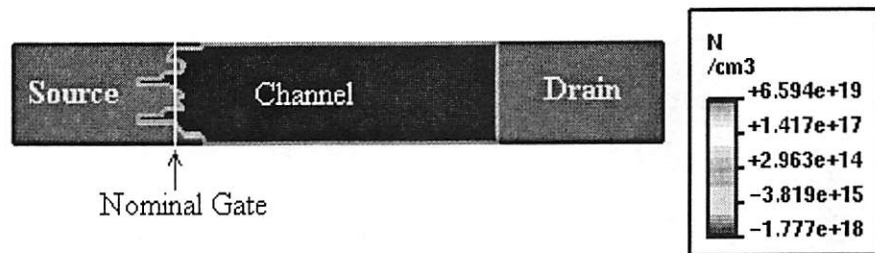


Figure 23 – Top-view cross section of a rough source device.

As expected, the off-state leakage current increased rapidly with increasing RMS roughness value, while the on-state drive current only increased nominally. Such large increases in I_{off} was attributed to the sharp corners whose electric field was enhanced by the surrounding drain voltage similar the single defect simulation results. The effect is

significant only when the S/D junction was very abrupt. The on-state current however was not affected as much because at large Vgs the device has been saturated. Therefore the enhanced field does not help increase drain current as much as in the leakage increase. The results were plotted on Figure 24

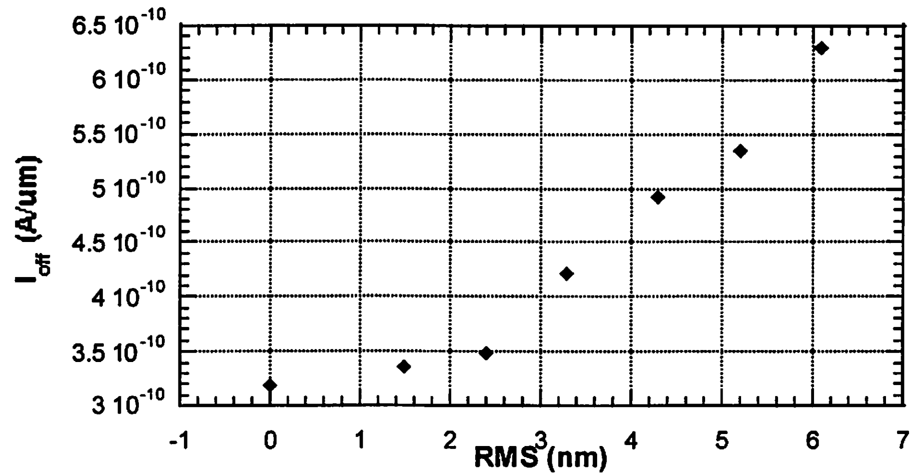


Figure 24a – Large increase in I_{off} with RMS roughness due to high corner field effect.

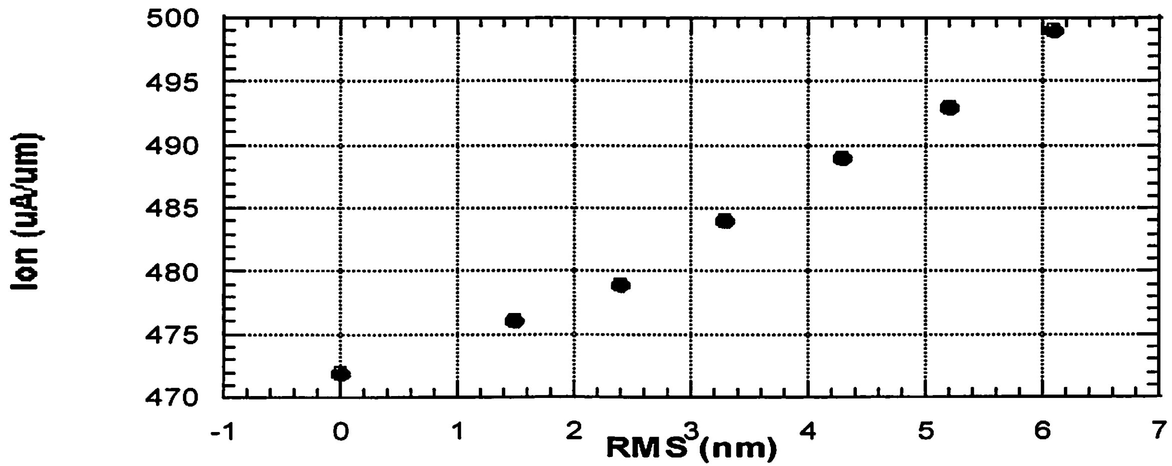


Figure 24b – Small increases in I_{on} with RMS roughness

It was noted from Figure 24 that for RMS value of 6.1 nm, I_{off} increased by about 100% while I_{on} increased by about 6%. Abrupt junction presented a possible effect of LER on device performance. It helped to single out the effect of the high field around a sharp corner sometimes occured in rough devices. However, to study a more realistic device, one needs to introduce lateral diffusion to the source, drain, and pocket implant doping. Thus we simulated device with different RMS roughness and introduced lateral diffusion into our devices. The problem here was that PROSIT did not offer a true 3-D diffusion model. However, to the first order approximation, it offered a very good physical insight into what happened to the source and drain doping. The plots of I_{off} and I_{on} increase with RMS roughness is shown in Figure 25.

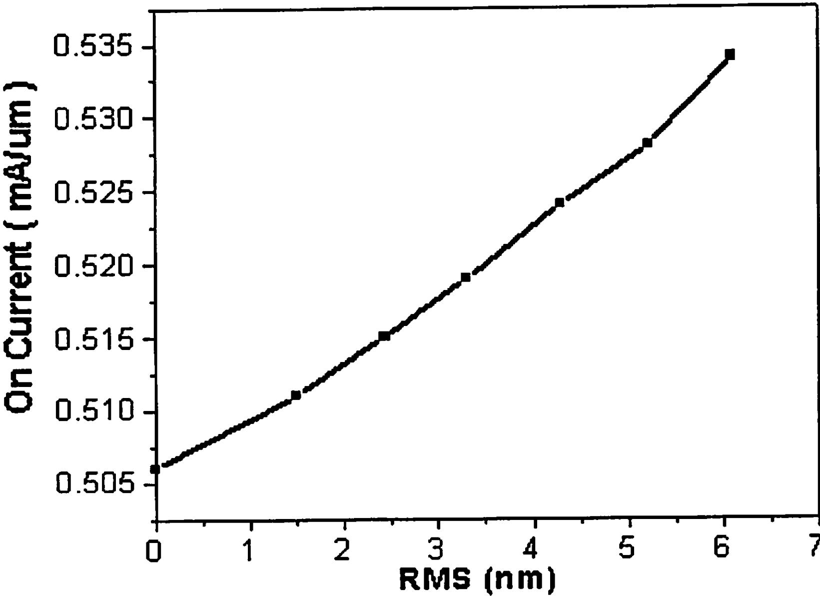


Figure 25a – I_{on} increases with RMS roughness

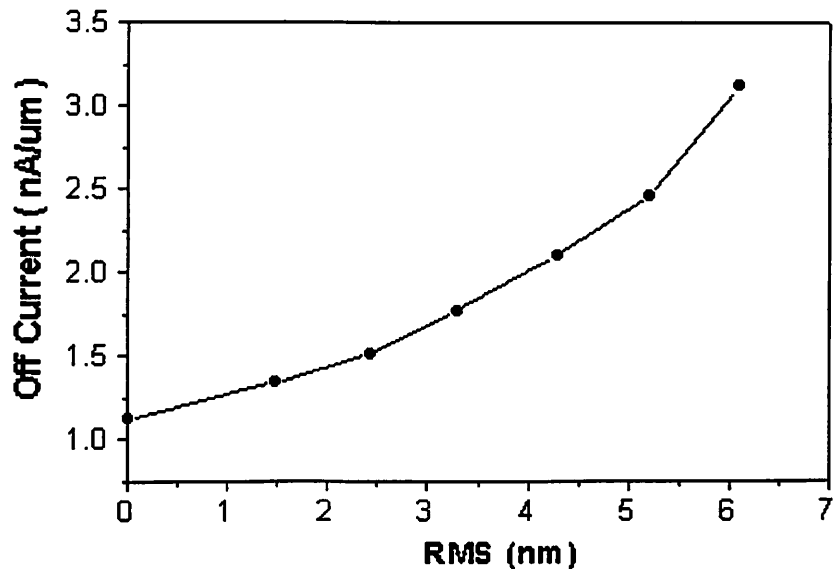


Figure 25b – I_{off} increase with increasing RMS roughness

The results indicated that off-state current increase very fast with increasing RMS roughness beyond 5 nm. The leakage current could have increased beyond acceptable values especially required in low power circuits and DRAM. At RMS roughness of 6.1 nm, I_{off} increased by 178% while Ion increased by 5.5%. A similar study done by Linton found similar results. Linton simulated a modulated square wave roughness and found that the leakage increase significantly[12]. However, there was no clear explanation as to what mechanism was responsible for such large leakage increase.

We have found from single defect simulation that the defect corners were smoothed out and further enlarged by lateral diffusion. It was no surprise that LER doping was also smoothed out by lateral diffusion. Furthermore, 2-D diffusion of LER doping caused the source/drain doping to extend further into the channel, thus shortening the average effective channel length of the device. Since LER device on average had a much smaller effective channel length than its nominal device; the leakage current was significantly higher. We also know that decreasing channel length does not dramatically

boost up the on-state current; this was the reason why I_{on} in LER device only increased a few percent.

To confirm that lateral diffusion smoothed out the doping, we performed diffusion and cut a top-down view, cross section. Figure 26 clearly shows that the same roughness as in Figure 23 has been smoothed out. Figure 26(a) shows the average position of the metallurgical junction for a rough gate device without diffusion; Figure 26(b) shows the average junction position for an identical rough-gate device with diffusion. Besides showing the roughness being smoothed out by 2-D lateral diffusion, Figure 26 shows that lateral diffusion causes the junction in (b) to be longer by, Δl.

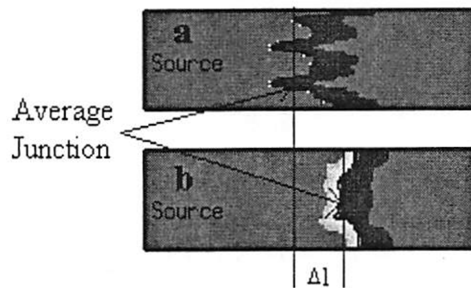
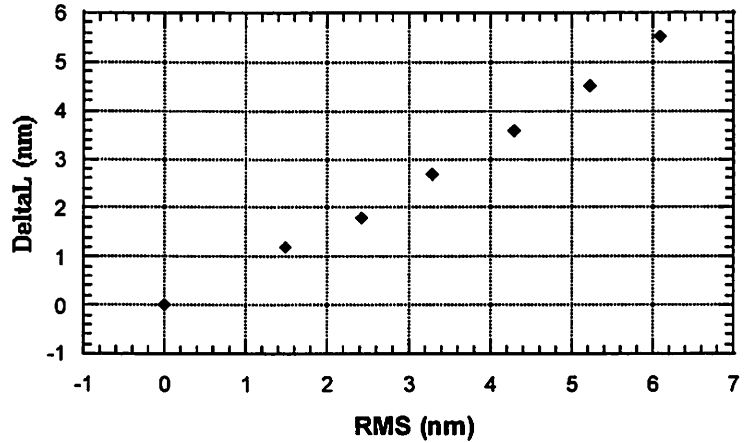


Figure 26 – Top down image cut of an LER doping smoothed out by diffusion

For different RMS values of LER, we extracted the average positions of the metallurgical junction. The position of the metallurgical junction was determined at the location where doping change from negative sign (Arsenic) to positive sign (Boron). Therefore we could determine how much longer was the junction extended into the channel. The junction length difference, Δl, was plotted against increasing RMS value in Figure 27. Δl increased linearly with RMS roughness. At RMS roughness of 6.1nm, Δl was 5.5 nm on each side of the gate. Therefore the total average effective channel could be shortened by approximately 11 nm.

Figure 27- S/D junction length difference increase with RMS roughness value



To reinforce the effect of lateral diffusion combined with LER causing shorter effective channel length, Shiying Xiong had used a mathematical model to confirm the result from the simulator. Xiong used a sinusoidal wave to represent the LER of the gate and the standard 2-D diffusion model as followed.

$$\begin{cases} \frac{\partial C(x,y,t)}{\partial t} - D\left[\frac{\partial^2 C(x,y,t)}{\partial x^2} + \frac{\partial^2 C(x,y,t)}{\partial y^2}\right] = 0 \\ C(x,y,0) = \varphi(x,y) \end{cases}$$

$$C(x,y,t) = \frac{1}{4\pi Dt}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\varphi(\xi,\eta)\exp\left[-\frac{(x-\xi)^2+(y-\eta)^2}{4Dt}\right]d\xi\, d\eta$$

With the following initial boundary conditions:

$$\varphi(x,y) = \begin{cases} C_p, & \text{for } y \le A\cos\left(\frac{2\pi x}{\lambda}\right) \\ 0, & \text{for } y > A\cos\left(\frac{2\pi x}{\lambda}\right) \end{cases}$$

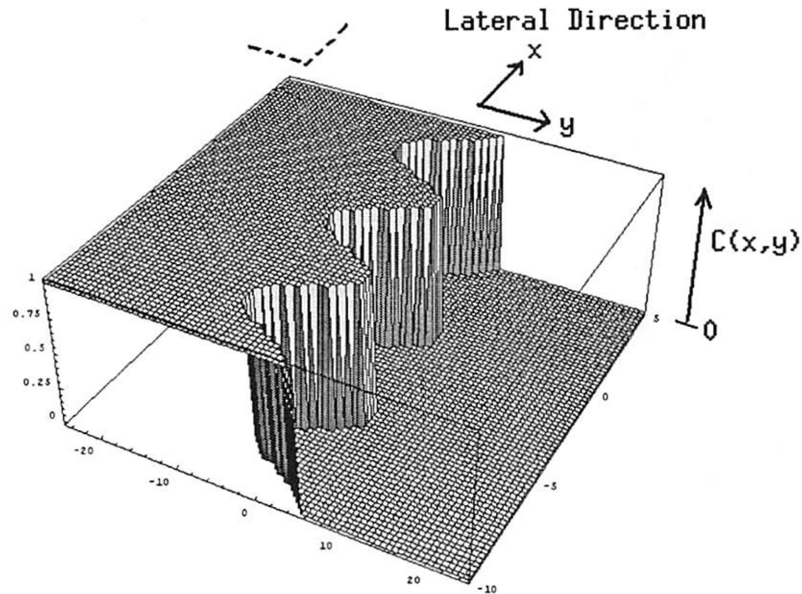


Figure 28 – 3-D Image of the cosine wave roughness used for calculating LER diffusion effect

The Cosine wave roughness as shown in Figure 28 was calculated for its lateral diffusion distance by Mathematica. The results are shown on Figure 29 and 30. Figure 29 shows (a) normalized 3-D image of the doping concentration after diffusion of a smooth gate device, (b) contours of doping concentration at different length and (c) the average junction position. Similarly, Figure 30 shows the 3-D image of the doping concentration, doping contours and the average junction position for a sinusoidal LER. This work has been done by Shiying Xiong, who may report this finding elsewhere later. Comparing Figure 29c and 30c, there is no doubt that the average junction position of rough gate was extended deeper into the channel than that of the smooth gate device.

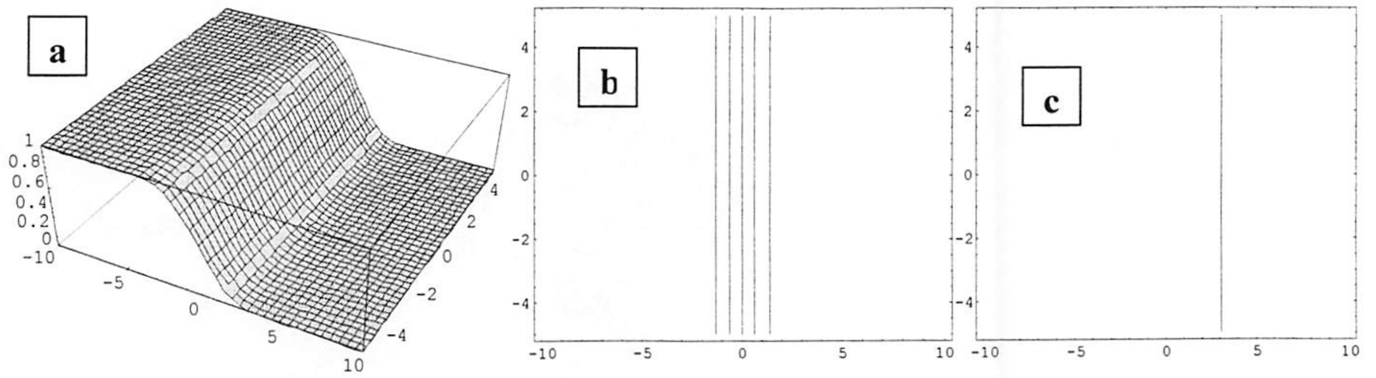


Figure 29- (a) 3-D Doping Concentration Profile (b) Doping Concentration Contours (c) junction position of a smooth gate

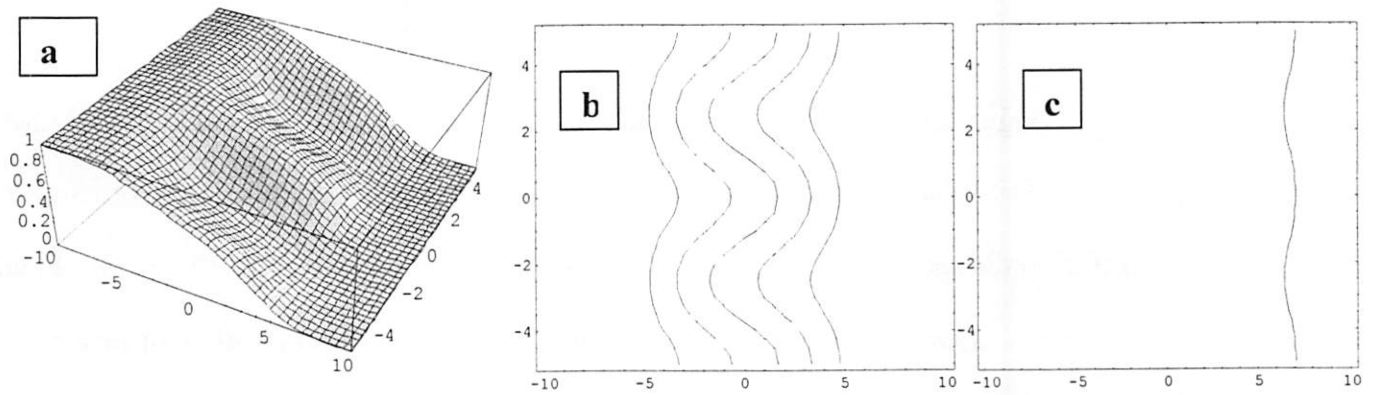


Figure 30- (a) 3-D Doping Concentration profile (b) Doping Concentration Contours (c) junction position of a sinusoidal rough gate.

To confirm that LER enhanced lateral diffusion effect, which shortens the device channel length, was the dominant contributor to LER effect on device performance, we simulated the following four devices. Device 1 had a rough gate with smooth doping (no LER effect on doping). Device 2 was a smooth gate, but the doping was rough. Device 3 had rough gate and rough doping. Device 4 was a smooth gate and smooth doping (normal device) but its source side average junction was adjusted to be the same as that of Device 3. The same LER mask was used in all four devices wherever the roughness was applied. The result showed that Device 1 (rough gate, smooth doping) behaved almost identical to a normal device as shown in Figure 31. This indicates that the shape of the gate has very little effect on device peformance. As long as we have identical channel doping, the devices work almost the same.

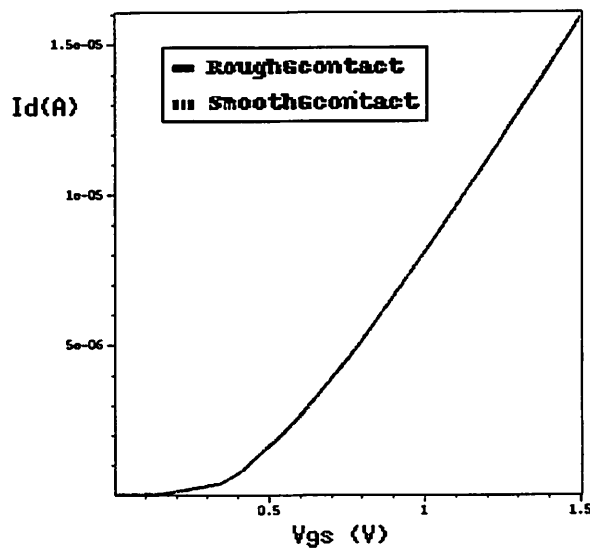


Figure 31 – Id-Vg of smooth gate and rough gate (Device 1) devices with smooth doping

Device 2 (smooth gate, rough doping) and Device 3 (rough gate, rough doping) showed nearly identical I-V curve as shown in Figure 32. This again reaffirms that the shape of the gate does not affect the device; the doping the profile underneath the gate is the dominant factor.

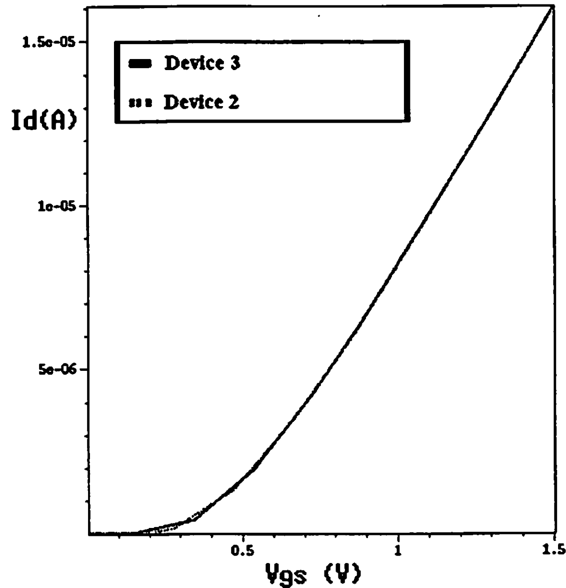


Figure 32 – The same I-V characteristic for Device 2 and 3 with the same doping roughness but different gate shape

Since Device 2 and 3 had rough doping and their effective channel lengths were thus shortened, they showed a 180% increase in I_{off} and 5.5% increase in I_{on} compared to a normal device. However, Device 4 (normal device with effective channel length adjusted to be the same as Device 2 and 3) shows a 23% difference in I_{off} and 0.75% difference in I_{on} compared to Device 2 and 3. This result clearly shows that the effect of LER enhanced lateral diffusion causing effective length shortened dominates. The 23% difference in I_{off} could have been attributed to simulation errors or residual high field effect around sharp corners.

Another effect that results from smoothing out of LER and increase the junction length further into the channel is that the overlap capacitance increases. Since the source and drain diffuse further into the channel due to gate LER, the overlap area between the gate and the soure/drain diffusion region would be larger. The significance of this increase has not been investigated. To reduce this effect, on obvious solution is to tightly control LER. However, the trade off would be the increase in production cost. One needs to evaluate the trade-offs to make processing decisions.

From the leakage current point of view, the effect of LER could be minimized by adjusting the nominal length of the device to offset for the shortening of channel length by LER. This solution had been suggested by Linton[12]. Since the dominant LER effect comes from channel length shortening, it is plausible to adjust the channel length to so that the average channel length would be approximately the same as the non-LER devices. However, adjusting the channel length would reduce I_{on} by a few percent. This is a tolerable loss of I_{on}. Another side effect of adjusting the channel length is an increase in overlap capacitance. Again, it is left to designers to optimize the adjustment so that an acceptable I_{off} is obtained without sacrificing drive current and overlap capacitance.

7.0 Conclusion:

Line edge roughness has shown to increase with reducing feature lengths. In the sub-100nm channel length, LER can be in the order of 5-10 % of gate length. Thus, device simulations for LER impact on device performance have been the goal of this project. The single defect study revealed two important effects of LER: the effect of enhanced electric field at sharp corners only in abrupt junction devices, and the lateral diffusion smoothing out of sharp corners and enlarging the defect size. These two effects were carried on to LER. The dominant contributor had been identified as the LER enhanced diffusion, which extended the S/D doping further into the channel and thus shortened the effective channel length and increased the overlap capacitance. Although the shape of the gate had very little direct effect on the device characteristics, it determined the doping profile underneath the gate which was found to be the critical factor of LER effect.

Since LER shortens the average effective length, it tends to reduce the threshold voltage and increase the subthreshold swing. These effects resulted in increasing the off-state leakage current, which needs very tight control especially in dynamic logic. Higher leakage requires higher refresh frequency and thus higher power consumption. The result suggests that devices with well-controlled short channel effects are necessary to minimize the impact of LER; a device needs to have very good threshold voltage roll-off characteristics well below the nominal gate length, very good sub-threshold swing, and low leakage current. However, the trade-off is increasing production cost. Another way

of offsetting LER effect is to adjust the channel length to account for the reduction in channel length by LER.

Since SOI device has highly suppressed short channel effects over the bulk technology, it is plausible to believe that the impact of LER on bulk technology would be greater, especially since bulk devices show worse V_t roll-off. The work of LER on bulk technology would be an interesting subject for continuing work.

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