

Copyright © 2000, by the author(s).
All rights reserved.

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission.

**A 25 Ms/s NYQUIST-RATE
SIGMA-DELTA MODULATOR FOR
A WIDEBAND CDMA RECEIVER**

by

David A. Sobel

Memorandum No. UCB/ERL M00/32

1 May 2000

**A 25 Ms/s NYQUIST-RATE
SIGMA-DELTA MODULATOR FOR
A WIDEBAND CDMA RECEIVER**

by

David A. Sobel

Memorandum No. UCB/ERL M00/32

1 May 2000

ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

A 25 Ms/s Nyquist-Rate Sigma-Delta Modulator for a Wideband CDMA Receiver

by David A. Sobel

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

Approval for the Report and Comprehensive Examination:

Committee:

Professor Robert W. Brodersen
Research Advisor

(Date)

Professor Bernhard E. Boser
Second Reader

(Date)

There are stars whose radiance is visible on Earth
even though they have long been extinct.

There are people whose brilliance continues to
light the world though they are no longer
among the living.

These lights are particularly bright
when the night is dark.

They light the way for us all.

—Hannah Senesh

Acknowledgments

As with any endeavor, this research project could not have been completed without the help and support of others. Foremost, I would like to thank my research advisor Professor Robert Brodersen. Your guidance throughout the course of this project is greatly appreciated. I would also like to thank Professor Bernhard Boser for teaching the coursework that formed the foundation of this work and for reviewing this thesis.

Over the past three years, I have had the unique honor of working with an extremely talented, dedicated, and fun group of people. Major thanks are due to Craig Teuscher and Dennis Yee for teaching me everything I know (and some stuff that I'm sure I've forgotten) about communication theory and RF design, respectively. My thanks also go out to the fellow members of the BARF group: Sayf Alalusi, Chinh Doan, Brian Limketkai, Dennis Yee, Johan Vanderhaegen, and Sam Blackman. Our discussions—technical and otherwise—have been a highlight of my years in the BWRC. Additionally, I want to single out my current and former cubicle mates for making the countless hours spent at my desk a little bit more fun. Even though Sam eventually sheared off his flowing locks in an effort to sell-out to Corporate America, his presence at the center made it a far more entertaining place. Andy did an admirable job as the resident financial advisor, even if I (regretfully) never heeded his advice. And Johan was an invaluable source of three crucial items: intellect, Belgian beer, and Belgian chocolate.

Berkeley has been an incredible place to live for the past three years, and this is due in no small part to the wonderful and fascinating people that I've spent time with when I haven't been swamped with work. I would like to thank all the people—far too many to name—who have enriched my life so much over these past years.

Finally, and most importantly, I would like to express my sincere appreciation and love to my family. Their unfailing love and support has been a source of strength over the past 24 years. There have been good times, and there have been bad times, but throughout it all, my family has been my rock. I dedicate this work to you with all my love.

Contents

Figures	vii
Tables	ix
CHAPTER 1 INTRODUCTION	1
1.1 Motivation	1
1.2 Research Goals	2
1.3 Thesis Organization	3
CHAPTER 2 SYSTEM ARCHITECTURES FOR INDOOR WIRELESS COMMUNICATIONS	5
2.1 Introduction	5
2.2 CDMA Receiver with Multi-User Detection	6
2.2.1 Introduction of Direct-Sequence Code-Division Multiple Access	6
2.2.2 Advantages of a CDMA System for Indoor Portable Wireless Applications	7
2.2.3 ADC Requirements for a Wideband CDMA Indoor Wireless Downlink	10
2.3 Receiver Front-End Architectures	10
2.3.1 Super-Heterodyne Receiver	10
2.3.2 Wideband IF with Double Conversion Receiver	11
2.3.3 Direct-Conversion Receiver	11
2.4 Baseband Processing	12
2.4.1 Analog Channel Selection	13
2.4.2 Digital Channel Selection	14
2.5 Motivation for Sigma-Delta Conversion	14
2.5.1 Process-Oriented and Circuit-Oriented Arguments	15
2.5.2 System-Oriented Arguments	16
2.6 Summary	19
CHAPTER 3 SIGMA-DELTA MODULATION	21
3.1 Introduction	21
3.2 Quantization Noise	21
3.2.1 Nyquist-Rate Converters	23
3.2.2 Sigma-Delta Converters	24
3.3 Constraints of High-Bandwidth Sigma-Deltas	27
3.3.1 Loop Filter Topologies	28
3.3.2 Discrete-Time vs. Continuous-Time	31
3.3.3 Single-Bit vs. Multi-Bit Quantization	33

3.4	Fundamental Power Limits	38
3.4.1	Dynamic Power	39
3.4.2	Static Power with Negligible Parasitics	40
3.4.3	Static Power with Capacitive Parasitics	42
3.5	Summary	44
CHAPTER 4	MODULATOR DESIGN	45
4.1	Introduction	45
4.2	2-1-1 Cascade Architecture	45
4.3	Signal Scaling	47
4.4	Capacitor Scaling	49
4.5	Analog/Digital Mismatch	50
4.6	Finite DC Gain	51
4.7	Settling Constraints	52
4.8	Simulation Environment	53
4.8.1	SIMULINK Simulation Environment	54
4.8.2	Simulation Results	55
CHAPTER 5	SWITCHED-CAPACITOR INTEGRATOR DESIGN	59
5.1	Introduction	59
5.2	Integrator Specifications and Design	59
5.3	OTA Design	61
5.3.1	Thermal Noise	62
5.3.2	Flicker Noise	64
5.3.3	Linear Settling	65
5.3.4	Slew Rate	67
5.3.5	DC Gain	68
5.4	Common-Mode Feedback	69
5.5	Bias	70
5.6	Comparator	70
5.7	Clock Generation	71
5.7.1	Duty Cycle Adjust	72
5.8	Output Buffer	73
5.9	Summary	74
CHAPTER 6	RESULTS	75
6.1	Introduction	75
6.2	Simulated Results	75
6.2.1	Capacitor and Bias Values	75
6.2.2	Transient Performance	76
6.2.3	Dynamic Range	77
6.3	Measured Results	78
6.4	Summary	83

CHAPTER 7 CONCLUSIONS	85
7.1 Introduction	85
7.2 Summary of Research Results	85
7.3 Future Work	86
REFERENCES	88

Figures

Figure 2.1	Generic multi-access link	6
Figure 2.2	Aggregate received spectrum of (a) FDMA and (b) CDMA	7
Figure 2.3	CDMA receiver block diagram	8
Figure 2.4	(a) Example indoor channel impulse response (b) and the channel transfer function	9
Figure 2.5	Superheterodyne Receiver	11
Figure 2.6	WIFDC Receiver	11
Figure 2.7	Direct-conversion receiver	12
Figure 2.8	Frequency Plan for Analog Channel Selection at Baseband Frequencies	13
Figure 2.9	Frequency Plan for Digital Channel Selection at Baseband Frequencies	14
Figure 2.10	Example DS-SS pulse train and oversampled data stream	17
Figure 2.11	Standard CDMA timing recovery scheme	17
Figure 2.12	$\Sigma\Delta$ -assisted Timing Recovery Scheme	18
Figure 2.13	(a) Standard $\Sigma\Delta$ /CDMA system and (b) new $\Sigma\Delta$ /CDMA	19
Figure 3.1	Possible analog and digital values between -2 and 2 .	22
Figure 3.2	Quantization transfer function	23
Figure 3.3	Quantization error for figure 3.2	23
Figure 3.4	1st-Order Sigma-Delta Modulator: (a) Block diagram (b) Linearized model	25
Figure 3.5	Noise-shaped spectrum and LPF	26
Figure 3.6	Third-order single-loop $\Sigma\Delta$ with distributed feedback	28
Figure 3.7	Generic 2-1 cascade $\Sigma\Delta$ modulator	30
Figure 3.8	Discrete-time and continuous-time integrator implementations	32
Figure 3.9	DAC impairments in a multi-bit $\Sigma\Delta$	35
Figure 3.10	Leslie-Singh dual-quantizer architecture	36
Figure 3.11	Multi-bit cascade $\Sigma\Delta$	36
Figure 3.12	Simplified CMOS integrator schematic	40
Figure 3.13	Normalized static power dissipation vs. $\omega_{UT,req}$	44
Figure 4.1	Maximum Achievable Dynamic Range for Various Cascade Modulators	46
Figure 4.2	2-1-1 block diagram	47
Figure 4.3	Maximum Integrator Output as a Function of Input Power	49
Figure 4.4	Switched-capacitor Integrator with Finite DC Gain OpAmp	52
Figure 4.5	Model of typical switched-capacitor voltage transient	53
Figure 4.6	SIMULINK structural model of $\Sigma\Delta$ modulator	55
Figure 4.7	SIMULINK Dynamic Range Performance Curve	56
Figure 4.8	System-level simulated SNR	57
Figure 5.1	Fully-differential switched-capacitor integrator	60
Figure 5.2	Two-phase non-overlap clock for bottomplate sampling	60
Figure 5.3	Fully-differential folded-cascode OTA	62
Figure 5.4	Small-signal model of switched-cap integrator with folded-cascode OTA	65
Figure 5.5	Dynamic common-mode feedback circuitry	69
Figure 5.6	Bias circuitry for folded cascode OTA	70

Figure 5.7	Dynamic comparator	71
Figure 5.8	Comparator with R-S latch	71
Figure 5.9	Two-phase non-overlap clock waveforms	72
Figure 5.10	Two-phase non-overlap clock generator	72
Figure 5.11	Clock duty-cycle adjust circuitry	73
Figure 5.12	Output Buffer	74
Figure 6.1	Folded-cascode OTA	76
Figure 6.2	(a) Simulated settling transient and (b) zoomed-in version	77
Figure 6.3	Dynamic range as simulated by SPICE	78
Figure 6.4	(a) Die photo of direct-conversion receiver. (b) Close up of $\Sigma\Delta$ modulator.	79
Figure 6.5	Dynamic range measurements at $f_{\text{NYQ}} = 25 \text{ Ms/s}$	80
Figure 6.6	Undecimated output spectrum of $\Sigma\Delta$ modulator	81
Figure 6.7	Dynamic Range as a function of f_{NYQ}	81
Figure 6.8	Undecimated output spectrum of $\Sigma\Delta$ modulator	82
Figure 6.9	(a) Charge residue (b) Resulting corruption of input signal	83

Tables

Table 2.1	ADC requirements	10
Table 4.1	Gain Coefficients for 2-1-1 Cascade Modulator	48
Table 4.2	Circuit performance requirements for first integrator	56
Table 6.1	Capacitor sizes and bias conditions for the OTAs	76

Introduction

1.1 Motivation

In recent years, there has been explosive growth in the demand for wireless communications capabilities. Cordless and cellular phones have practically replaced traditional wired telephony for traditional voice communications applications as the idea of mobile access has become the de facto standard for business professionals and residential consumers alike. This demand for mobile access has spread beyond mere voice-band applications; with the emergence of high data-rate wireless standards—such as Bluetooth, 802.11, HomeRF, and many others—the possibility of mobile wireless data access has become a reality.

The design of mobile wireless communications devices is fraught with several research challenges. First, as the mobile device is powered by a portable battery, low-power operation is of utmost concern. Additionally, the device must have a small form factor and be relatively low-cost in order to meet the demands of a consumer market. All of these challenges motivate research into the design of highly integrated receivers implemented in a low-cost technology (e.g. CMOS).

With the continual scaling of CMOS technology, it becomes desirable to leverage off of the exponential growth of digital computation capability for two reasons: first, scaling allows us to implement more computations in a given area of silicon and to perform those computations at lower power levels. This increase in computational capacity opens the door to innovative and complex communications algorithms. Second, while the scaling of CMOS technology results in more complex digital circuits and analog circuits with faster transient performance, it also tends to degrade many of the other typical analog performance metrics, (e.g. gain, voltage swing, linearity, et al.) Therefore, it becomes necessary to compensate for these shortcomings—or avoid some of them altogether—through the increased use of digital computation.

A sigma-delta ($\Sigma\Delta$) modulator is a converter architecture that takes advantage of this increased digital computation capacity by moving more of the channel selection operation into the digital domain. By doing so, a $\Sigma\Delta$ modulator does not suffer as greatly from the analog performance degradation that comes with scaled CMOS technologies. Additionally, as the channel selection is performed in the digital domain, opportunities arise to employ flexibility and intelligence in this operation. By co-designing the analog circuits of the modulator along with the back-end digital circuits used for signal processing, it becomes possible to co-optimize across this boundary and create circuit topologies and algorithms that are uniquely suited to high-performance, low-power operation. A $\Sigma\Delta$ modulator is an appropriate vehicle for such a co-design exercise, as it can be viewed as a “mostly digital” converter.

1.2 Research Goals

The primary goal of this research is to design a very high-speed, low-power sigma-delta ADC for a highly-integrated, CMOS direct-conversion receiver front-end of a wideband CDMA wireless link. A secondary goal is to further understand the area of system and circuit co-design, so that the interaction between the analog circuits of the sigma-delta modulator and the back-end algorithms can be understood and exploited.

The results of the project are summarized below:

- Designed a switched-capacitor, CMOS sigma-delta modulator and demonstrated that this circuit could meet the specifications of a wideband

CDMA indoor wireless link at a reasonable power dissipation. An experimental prototype achieved a dynamic range of 42 dB at a Nyquist rate of 25 Ms/s and dissipated 26 mW.

- Examined and developed several areas of circuit and system co-design. Implemented a $\Sigma\Delta$ -assisted timing recovery scheme where the intrinsic oversampling of the modulator is used to greatly ease timing recovery with minimal additional complexity. Identified a code-based noise-shaping scheme where the quantization noise is shaped relative to the CDMA spreading code rather than relative to frequency.
- Designed a high-speed, low-power operational transconductance amplifier suitable for 2.5 V CMOS processes.
- Developed a methodology to identify key performance constraints of the switched-capacitor integrators and minimize power consumption in the integrators around those constraints.

1.3 Thesis Organization

Chapter 2 provides an overview of system architectures for indoor wireless communications systems. It briefly reviews system and circuit architectures suitable for highly-integrated, low-power operation, followed by motivations for using a sigma-delta modulator. The fundamentals of sigma-delta modulation are introduced in Chapter 3. Key constraints and techniques for high-speed $\Sigma\Delta$ modulation are presented, and fundamental power dissipation limits of switched-capacitor implementations are investigated. Chapter 4 presents the system-level design of a $\Sigma\Delta$ modulator. Issues such as architecture selection, oversampling ratio and capacitor scaling are discussed. Circuit-level specifications are derived via structural simulations. Chapter 5 focuses on the design of the key circuit blocks of the $\Sigma\Delta$ modulator. Test results are presented in Chapter 6, and conclusions from this work are presented in Chapter 7.

System Architectures for Indoor Wireless Communications

2.1 Introduction

This chapter will introduce the system architecture used for an indoor, high data-rate, multi-user wireless link [1]. First, the multi-access scheme of code-division multiple access (CDMA) will be introduced, and comparisons to the more familiar frequency-division multiple access (FDMA) scheme will be made. System requirements for the analog front end of a CDMA receiver will be considered.

The primary goal of the larger receiver project is to design a low-power, fully integrated receiver that meets the specifications for the system mentioned above. Therefore, several architectures for the analog front-end are considered in section 2.3; trade-offs in design complexity, ease of integration, and power consumption are considered. It is shown that a direct conversion receiver architecture is most suitable for the targeted application.

Section 2.4 addresses the issue of signal processing at baseband frequencies. Different techniques are compared for suitability in design of the wideband-CDMA

system described. Finally, section 2.5 discusses the challenges and promise of designing a $\Sigma\Delta$ converter architecture for the system in question.

2.2 CDMA Receiver with Multi-User Detection

2.2.1 Introduction of Direct-Sequence Code-Division Multiple Access

Direct-Sequence Code-Division Multiple Access (DS-CDMA or CDMA) is a technique that allows simultaneous access multiple users to a common communication channel. CDMA allows for multiple users much in the same way that Orthogonal Frequency-Division Multiple Access (OFDMA) schemes do: by multiplying each user's data signal by a signature signal that is orthogonal (or nearly orthogonal) to the other users' signature (Figure 2.1). At the receiver side, an analogous demodulating process is performed.

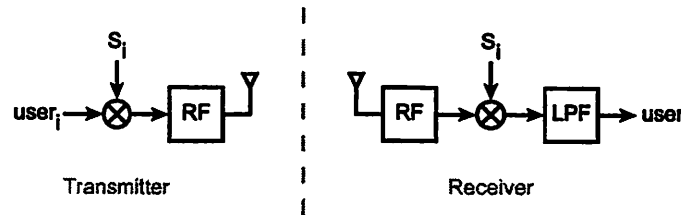


Figure 2.1 Generic multi-access link

In the case of OFDMA, the modulating signal is a sinusoid of fixed frequency. Because two sinusoids of different frequency are orthogonal in the DC sense, the demodulation process is able to isolate the desired user's signal.

$$\overline{\int \sin(\omega_1 t) \sin(\omega_2 t)} = 0 \quad \omega_1 \neq \omega_2 \quad (2.1)$$

The aggregate transmit spectrum of an OFDMA system is similar to that shown in figure 2.2a. Furthermore in OFDMA, the orthogonalization process is typically performed in the analog domain.

In contrast, the orthogonal signature sequences used in CDMA signals are typically pseudo-noise sequences of finite length, N , that possess an approximately white spectrum. The process of multiplying the user's data signal is termed *spreading*, because

the output spectrum of this process is *spread* out by the factor N .¹ Therefore, the individual users' data signals overlay in frequency space, as shown in figure 2.2b. Each user's signature sequence, s_k , is chosen such that it is orthogonal (or nearly orthogonal) to every other user's signature sequence:

$$\langle s_k, s_j \rangle = 0 \quad k \neq j \quad (2.2)$$



Figure 2.2 Aggregate received spectrum of (a) FDMA and (b) CDMA

Therefore, the receiver can isolate the desired signal by demodulating with the identical signature sequence, as in figure 2.1. For this system, the ideal low-pass filter in figure 2.1 is an N -tap accumulator (also known as a “comb filter”). The process of accumulate-and-dump in the low pass filter brings the data rate down to that of a single user. Since this operation is the dual of the spreading process, it is commonly referred to as *despreading*.

Hence, one can observe that—at the basic mathematical level—FDMA systems and CDMA systems are fundamentally the same. They both partition the available signal space into N mutually orthogonal subsets. The key difference is one of implementation: OFDMA systems use sinusoids as their orthogonal signatures, whereas CDMA systems employ pseudo-random noise (PN) sequences for the orthogonalization process. This choice involves trade-offs at both the circuit and system levels. These trade-offs are analyzed below in brief below. For a complete analysis of the multiple-access scheme used in this system, see [2]. For a theoretical analysis of CDMA algorithms, see [3] [4].

2.2.2 Advantages of a CDMA System for Indoor Portable Wireless Applications

Figure 2.3 shows a more detailed description of a CDMA receiver, assuming a single user bandwidth of f_U and a spreading factor of N . While the despreading process can be performed in the analog domain [5], such an implementation is not considered

¹ N is commonly referred to as the “spreading gain” or “spreading factor”.

here. One of the drawbacks of a CDMA receiver can be immediately discerned from Figure 2.3: the analog-to-digital converter (ADC) and significant portions of the baseband digital section must operate at N times the individual user data rate. This speed requirement is ameliorated by the fact that the despreading process increases the SNR of the data signal, as noise that is orthogonal to the desired signature sequence is suppressed, as in (2.2). Therefore, the N -fold increase in required speed comes along with an N -fold reduction in required pre-despreading dynamic range. As a result, DS-SS-CDMA systems tend to require high-speed, reduced dynamic range circuits. The ever-increasing speed of CMOS devices allows for this high-speed operation.

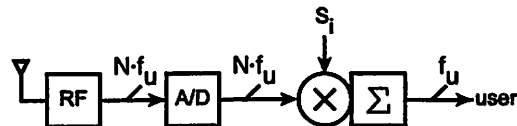


Figure 2.3 CDMA receiver block diagram

Operating at this higher rate (by the factor N) affords certain benefits, however. The first, and most important, benefit is specific to the indoor channel. Indoor (i.e. office, home) channels are characterized by having several relatively strong, closely spaced reflective paths in addition to the primary line-of-sight (LOS) path. This is due to the fact that the confines of an indoor environment tends to have many closely spaced walls and obstacles that allow for multiple reflective paths. In an indoor environment, the differences in reflected path lengths creates an impulse response with a finite delay-spread, T_d (fig 2.4a). This can be contrasted to outdoor communications, where the direct LOS path is likely to be the only one of significance, and any reflections are likely to be weak and be more spaced out in time.

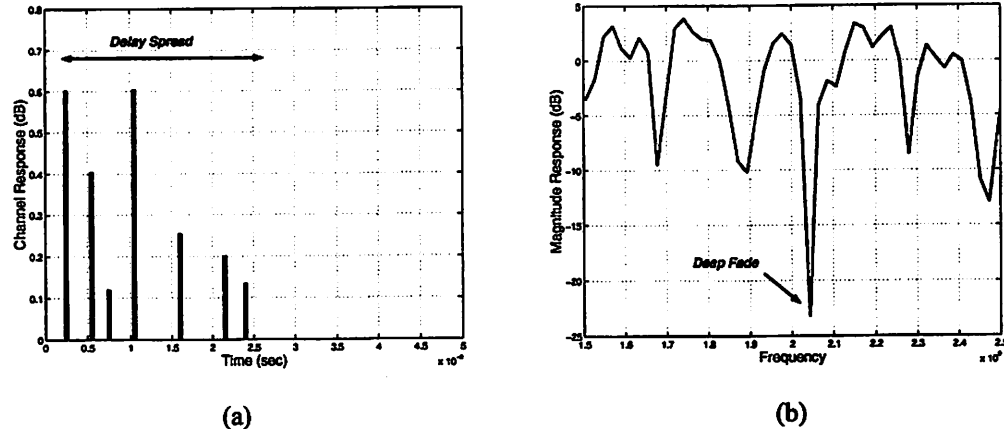


Figure 2.4 (a) Example indoor channel impulse response (b) and the channel transfer function

The Fourier transform of the impulse response in figure 2.4a gives figure 2.4b. Here we can observe that the multi-path reflections create frequency-selective fades with a width roughly equal to the inverse of T_d [2]. If a narrowband FDMA approach is used, there is a possibility that the entire desired signal could fall within one of these nulls, resulting in a great deterioration in performance. If a wideband² CDMA signal is instead employed, the channel null only affects a small portion of the desired signal, resulting in far less performance degradation. Furthermore, due to its robustness to interference, CDMA systems are more robust in electrically “noisy” environments [3]. For these reasons, spread-spectrum techniques such as CDMA are preferred for indoor, high-performance systems [6] [7].

Another advantage of this CDMA approach is its amenability to a “mostly digital” approach. In fact, the spreading and despreading processes map directly to digital architectures, which allows us to leverage off of the tremendous achievements in low-power digital circuit design. Furthermore, through a process of circuit and system co-design, it has been shown that the front-ends for these high performance systems can be constructed from low-performance analog components [8]. Viewed another way, high-performance systems can be constructed using analog circuits that consume very little power. For these reasons, a CDMA approach is very attractive for a portable wireless application.

² Here, “wideband” implies that the spread-spectrum bandwidth is significantly larger than the null bandwidth.

2.2.3 ADC Requirements for a Wideband CDMA Indoor Wireless Downlink

The system design of a wideband CDMA wireless downlink is presented in [2]. The system is based on a 1.6 Msymbol/s QPSK constellation, spread by a length-15 MLSR pseudo-noise sequence; hence, the chip rate is 25 Mchip/s. The system is based on an indoor picocellular model, where each room acts as an individual cell and office walls provide natural isolation between cells.

As discussed in the previous section, the use of spread-spectrum techniques requires high-speed baseband circuits with moderate dynamic range. As the chip rate of this system is 25 Mchips/s, the minimum acceptable Nyquist rate is 25 Ms/s. Analysis and simulations in [2] have shown that the system requires an ADC with at least 6 bit resolution. The requirements of the ADC are summarized in Table 2.1.

	WCDMA Indoor Wireless Link[2]
Signal Bandwidth	> 25 MHz
Dynamic Range	>5.9 bits
Power	Minimize

Table 2.1 ADC requirements

2.3 Receiver Front-End Architectures

2.3.1 Super-Heterodyne Receiver

The block diagram for a super-heterodyne receiver is shown in figure 2.5. This architecture has been widely implemented in commercial systems [9], as the high-Q off-chip filters (shaded in Figure 2.5) provide superior noise and selectivity performance. The speed and dynamic range requirements on the ADC are reduced, as unwanted blockers are greatly attenuated by the high-selectivity filters. This is a high-cost solution, however, as the high-Q components required for the filters cannot be integrated with the active circuitry.

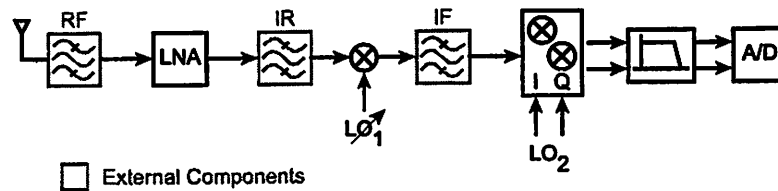


Figure 2.5 Superheterodyne Receiver

2.3.2 Wideband IF with Double Conversion Receiver

The Wideband IF with Double Conversion (WIFDC) architecture shown in 2.6 is far more amenable to integration [10]. This architecture uses a two-step downconversion process, but high-Q filters are no longer needed. Instead, the second mixing stage utilizes an image-rejection architecture which exploits the properties of quadrature signals to mathematically cancel out unwanted image signals. The image cancellation is limited by circuit mismatch in the I- and Q-paths to about 25-30 dB [11]. Hence, the image problem is not entirely resolved. Furthermore, the added complexity and power consumption needed for 6 mixers and 2 LO signals makes this architecture attractive only for systems that require multi-standard capabilities [12]. As this architecture performs a block-downconvert, the baseband analog circuitry must have a higher dynamic range and operating speed in order to accommodate the entire inband spectrum.

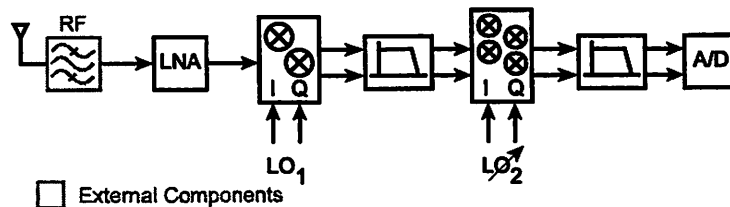


Figure 2.6 WIFDC Receiver

2.3.3 Direct-Conversion Receiver

Figure 2.7 shows a direct-conversion (homodyne) receiver. This architecture is the easiest to understand. There is a single mixing stage with (for DS-CDMA applications) a fixed-frequency LO that brings the entire RF signal to baseband for

subsequent processing. As there is only a single downconversion, there is no image problem, and high-Q IF filters are not required. Hence, this architecture is very appropriate for high levels of integration. This architecture also performs a block-downconvert, so the speed and dynamic range requirements are similar to that of the WIFDC architecture discussed above.

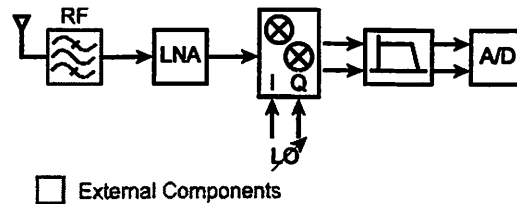


Figure 2.7 Direct-conversion receiver

Potential problems with this architecture arise from the fact that the desired signal is brought to directly DC at an early point in the receiver chain. The LO signal is at the same frequency as the incoming signal, so any leakage of the LO to the RF port can cause self-mixing. This can create a large DC offset that could saturate later stages. Additionally, the gain from the antenna through the mixer is relatively low, so the flicker noise from baseband stages could be significant. Both of these deleterious effects can be minimized by inserting a high-pass characteristic in the form of a coupling capacitor prior to the ADC. On-chip capacitors can be made large enough to realize a 100-kHz notch frequency [11]. While this notch does attenuate the signal energy, the attenuation is over a small portion of a wideband CDMA signal. Hence, resulting signal degradation is kept small. Additional DC offsets can be caused by second-order distortion of nearby blocker signals. This effect can be minimized by careful layout of fully-differential circuitry. Thus, the critical problems of a direct conversion receiver can be overcome with system and circuit co-design, and this architecture becomes very attractive for indoor spread-spectrum applications.

2.4 Baseband Processing

The previous section discussed receiver front-end architectures for an indoor CDMA system. This section will discuss the trade-offs involved in the design of the

baseband components. The discussions that follow assume a CDMA system that performs the despreading process in the digital domain, as in [13]. As such, the entire CDMA band must be converted by the ADC, and user-channel selection is performed during the digital despreading. Therefore, each CDMA band of N users can be viewed as a single “channel” for the purposes of baseband processing. Adjacent channels are CDMA bands that are transmitted from nearby cells and are centered at adjacent carrier frequencies.

In this light, there are several options for performing channel selection at baseband. Discussion of the design considerations and trade-offs will be explored in the following sections.

2.4.1 Analog Channel Selection

Channel selection can be performed in the analog domain with the use of an anti-alias filter and a low-pass switched-capacitor circuit [14]. These filters attenuate adjacent channels. The achievable selectivity of these filters is determined by the filter order, and in the case of the switched-capacitor filter, its oversampling as well [15]. Also, these filters can also provide additional gain to the desired channel in order to reduce dynamic range requirements of later stages. As a result, the ADC in this system has relatively moderate speed and resolution requirements. Figure 2.8 shows a frequency plan for an analog channel select baseband architecture.

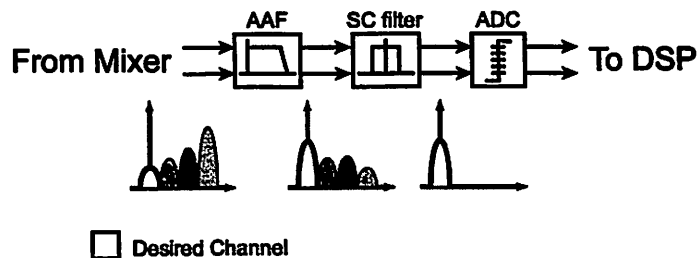


Figure 2.8 Frequency Plan for Analog Channel Selection at Baseband Frequencies

2.4.2 Digital Channel Selection

Channel selection can be performed in the digital domain with a low-pass FIR filter. The ADC must be oversampled in order to quantize both the desired signal and the adjacent channels and prevent aliasing. Furthermore, the ADC must have increased dynamic range in order to quantize the desired signal in the presence of these adjacent channels. Figure 2.9 shows a frequency plan for an digital channel select baseband architecture.

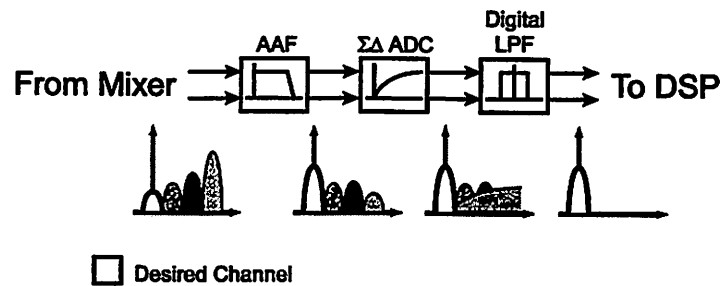


Figure 2.9 Frequency Plan for Digital Channel Selection at Baseband Frequencies

The ADC in a digital channel selection architecture is typically a $\Sigma\Delta$ modulator. The quantization noise is then shaped outside of the band of interest; it primarily lies in the same band as the adjacent channels and can be removed by the digital FIR filter [16].

2.5 Motivation for Sigma-Delta Conversion

The previous section discussed analog and digital channel selection techniques. The primary difference between analog and digital channel selection techniques is the trade-off between resolution and bandwidth; analog techniques are more appropriate for low-resolution, high-speed applications, while digital techniques have historically been employed in higher-resolution, lower-speed applications. The bandwidth-resolution trade-off has been thoroughly analyzed in the context of baseband processing systems in [17].

Previous CMOS implementations have demonstrated that an analog channel-selection topology can meet the specification discussed in Section 2.2.3 [14]. The purpose of this study, however, is examine the applicability of a digital channel selection

topology this system. There are several factors on both the circuit- and system-level that motivate such an exploration. They are discussed in the following sections.

2.5.1 Process-Oriented and Circuit-Oriented Arguments

It should first be noted that the circuit requirements for analog and digital channel selection blocks are strikingly similar. In particular, the switched-capacitor filter in the analog channel selection architecture and the $\Sigma\Delta$ modulator in the digital channel selection architecture have almost identical circuit requirements; they must both have sufficient dynamic range to handle a small desired signal in the presence of adjacent blockers and be sufficiently oversampled to prevent aliasing. As a result, it has been shown that the required order and OSR of these two blocks are typically very similar, and to first order, the power and complexity of these blocks should be similar as well [18].

$\Sigma\Delta$ modulators were first employed in audio-band converters, as the slow speed of the silicon technology greatly limited sampling speeds [31]. In the intervening 12 years, high-resolution $\Sigma\Delta$ modulators have been demonstrated with conversion bandwidths of 2.2 MHz [19] and sampling rates up to 4 GHz [33]. This increase in bandwidth is in no small part due to the drastic increase in transistor f_T that has occurred since 1988. Research on technology scaling predicts that f_T will continue to increase an additional 40-100x over the next decade [20]. Hence, from a standpoint of sheer transistor speeds, an examination of high-bandwidth $\Sigma\Delta$ modulators is attractive.

Furthermore, it has been shown that high-resolution $\Sigma\Delta$ modulators can be constructed from relatively low-resolution circuit components [28] [31]. While the extent to which this observation can be exploited lessens with complicated modulator structures, this trade-off of speed for resolution is attractive in deep-submicron technologies: the transistors will continue to demonstrate high operating speeds, but this will come at the expense of other performance metrics, such as gain, matching, or linearity [21]. $\Sigma\Delta$ modulators therefore map well onto high-speed, low-precision CMOS processes.

2.5.2 System-Oriented Arguments

The original impetus for the exploration of high-speed $\Sigma\Delta$ modulators stems from earlier research on the wireless link for the InfoPad system [22]. This research aimed to develop a high-performance wireless link with the lowest possible power consumption. A key finding of this research was that power consumption could be reduced by “pushing” as much complexity as possible out of the analog front-end and into the digital portion of the receiver [2]. $\Sigma\Delta$ analog-to-digital conversion is a step in the direction of a “mostly digital” radio. The channel selection filter is now implemented in the digital domain. As a result, low-power digital circuit techniques can be utilized to realize highly efficient structures [23]. Furthermore, as digital filters do not have the mismatch problems associated with analog filters, they are greatly preferred in applications where a high degree of selectivity is required.

An oversampled approach lessens the requirements on the anti-alias filter (AAF) preceding it. As the frequencies which alias to baseband are integral multiples of the sampling frequency, an oversampled approach provides a larger bandwidth for the continuous-time AAF to roll-off. This enlarged roll-off bandwidth can be of crucial importance, as process variation can shift the AAF poles by as much as 30% [15].

The most interesting arguments for a digital channel select architecture stem from the opportunities for system/circuit co-design it allows. As demonstrated in [35], a single $\Sigma\Delta$ modulator can be made multi-standard capable by changing the oversampling rate and decimation filters. Two other potential applications of $\Sigma\Delta$ /CDMA co-design, outlined below.

$\Sigma\Delta$ -assisted Timing Recovery In any communication system, proper synchronization with the incoming signal is a necessary condition for data reception. This problem is exacerbated with DS-CDMA signals, as the pulse trains that comprise these signals tend to have sharp peaks that need to be captured. Figure 2.10 shows an example DS-CDMA pulse train. The chip time is labeled as T_c . In order to provide adequate timing recovery granularity, the input stream is typically oversampled by a factor of 4 [24], resulting in a data stream with sampling time T_{TR} , shown in figure 2.10. The digital circuitry of the timing recovery block decimates the high-speed sequence on the appropriate phase to create the chip-rate sequence for data detection (figure 2.11) [25].

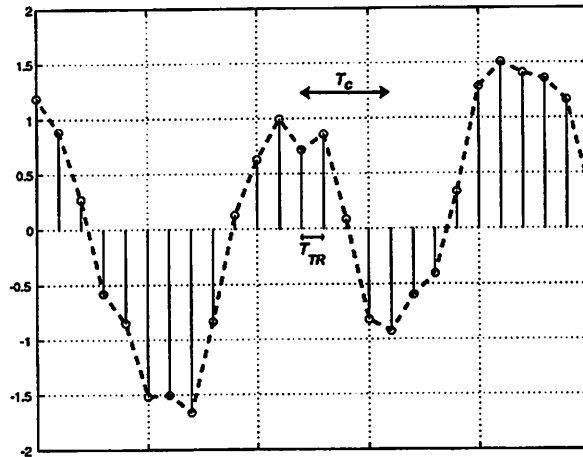


Figure 2.10 Example DS-CDMA pulse train and oversampled data stream

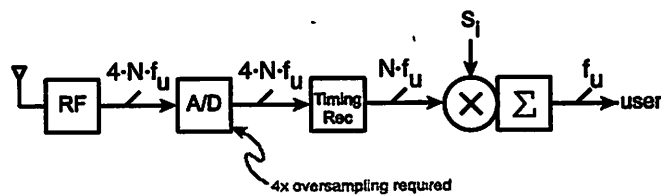


Figure 2.11 Standard CDMA timing recovery scheme

In a system employing a standard analog-to-digital converter, the ADC must operate at a speed of 4 times greater than required by the Nyquist. This increased operation speed of the ADC results in wasted power, as 75% of the ADC output data values are wasted through decimation. In such a scheme, one may also need to control the phasing of the sampling clock in order to provide adequate granularity for the timing recovery blocks [25].

It can be observed that a $\Sigma\Delta$ already samples the input stream at the higher data rate needed for timing recovery; in fact, the pre-decimated output of the modulator is a lower resolution of the stream shown in figure 2.10. Therefore, as shown in figure 2.12, timing recovery can be accomplished with minimal changes to the analog circuitry. Instead, one can control the phasing of the decimating digital LPF. By including a variable-length delay line right before the LPF, the timing recovery block can fully control the effective phase of the sampling instant. This approach allows for a fully-

digital timing recovery block without having to increase the complexity of the analog circuitry. This scheme is implemented in [26], and is quite similar to the system proposed in [27].

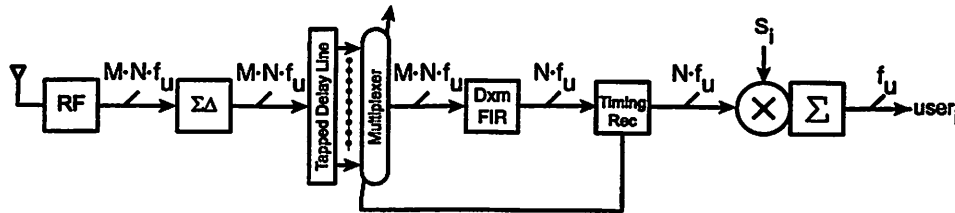


Figure 2.12 $\Sigma\Delta$ -assisted Timing Recovery Scheme

Code-based Noise-Shaping DS-CDMA systems are intentionally oversampled in relation to their symbol rates in order to create wideband signals that are robust to channel impairments. This wideband property hinders oversampled analog-to-digital conversion of DS-CDMA signals, as the overall sampling rate is limited by process technology. Yet it should be observed that the desired signal converted by the ADC contains *all* of the users' data streams. If only one user stream is required, it can be observed that some of the converted bandwidth is extraneous.

Section 2.2 demonstrated that OFDMA systems and CDMA system are mathematically equivalent in that they divide a range of bandwidth into several distinct subsets. The only difference between the two systems is that FDMA forms its subsets with a frequency basis and CDMA forms its subsets with a code basis.

A conventional $\Sigma\Delta$ modulator is appropriate for FDMA systems, as its noise-shaping property is based on frequency; quantization noise is suppressed in the frequency subset of interest and is pushed into the extraneous frequency subsets. Based on the mathematical equivalence between FDMA and CDMA systems, it seems reasonable to hypothesize that an analogous CDMA $\Sigma\Delta$ modulator can be constructed. In essence, it seems feasible that the structure of a standard sigma-delta modulator can be altered, such that the additive quantization noise is shaped in a manner orthogonal to the desired user's *spreading code*, (hence the name *code-based noise shaping*). A standard $\Sigma\Delta$ modulator in a CDMA system is shown in figure 2.13a, and a rudimentary version of a modified $\Sigma\Delta$ -CDMA system that enables code-based noise-shaping is shown in figure 2.13b.

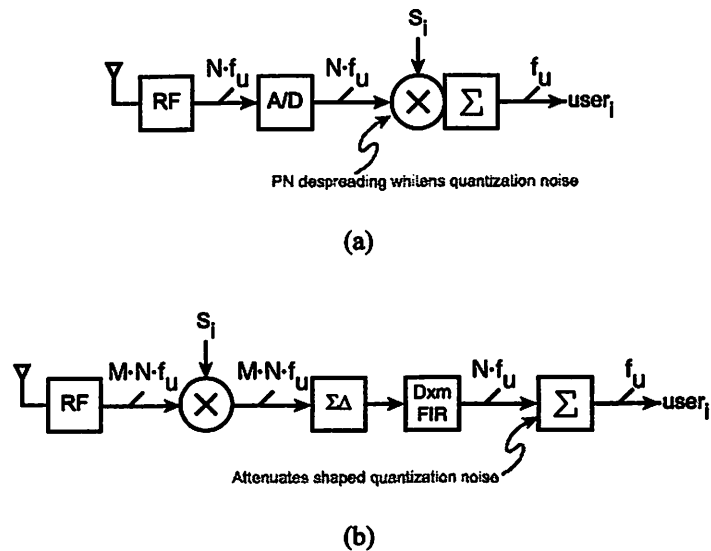


Figure 2.13 (a) Standard $\Sigma\Delta$ /CDMA system and (b) new $\Sigma\Delta$ /CDMA

In figure 2.13a, the despreading by the PN-sequence following the $\Sigma\Delta$ modulator whitens the quantization noise spectrum. Therefore, the accumulator LPF only reduces the quantization noise by 3 dB/octave. In contrast, multiplication by the PN-sequence is performed before the $\Sigma\Delta$ modulator in figure 2.13b. Therefore, the quantization noise added by the $\Sigma\Delta$ retains its shaped characteristic at the input to the accumulator. Therefore, the decimation by the accumulator attenuates the quantization noise by much more than 3 dB/octave.³ If this architecture is used, the multiplication by the PN-sequence is done in the analog domain. This can be easily accomplished by a polarity reversal in switched-capacitor differential circuits, provided that the PN-sequence is comprised solely of ± 1 's.

2.6 Summary

This chapter introduced the system architecture used for an indoor, high data-rate, multi-user wireless link. The CDMA protocol was discussed, and reasons for selecting a direct-conversion receiver were reviewed. In this context, the issue of baseband

³ One could argue that the accumulator attenuates the quantization noise by as much as $(6L+3)$ dB, where L is the $\Sigma\Delta$ order. It should be noted that an accumulator does not exhibit a "brick-wall" LPF characteristic, so the actual attenuation will be less than the theoretical limit.

processing was discussed, and motivations for a digital channel selection architecture comprising of a $\Sigma\Delta$ modulator and digital FIR filters were presented. Fundamental issues in $\Sigma\Delta$ modulation will be presented in the next chapter.

Sigma-Delta Modulation

3.1 Introduction

This chapter reviews some of the fundamental issues of analog-to-digital conversion and sigma-delta modulation. The chapter begins with a discussion of the quantization noise inherent to all analog-to-digital converters. A comparison between the quantization noise of Nyquist-rate converters and $\Sigma\Delta$ converters is made. Due to their oversampled nature, sigma-delta converters have historically been used for low data-rate applications. The next section of this chapter addresses various $\Sigma\Delta$ design choices with an emphasis on topologies and techniques that enable high data-rate applications. Finally, dynamic and static power limits for discrete-time $\Sigma\Delta$ modulators are derived, again taking into account factors applicable to high-speed operation. Readers are referred to [28], [29], [30], [31], [32], [33] for further reading on issues related to $\Sigma\Delta$ design.

3.2 Quantization Noise

An analog signal can, by definition, take on any value within a continuous range. A digital signal, on the other hand, can only take on a discrete set of values. The

resolution of a digital signal is ultimately limited by the number of bits used to represent it. This difference is demonstrated in Figure 3.1. (For the purpose of convention, the resolution of the digital value is set to 1.)

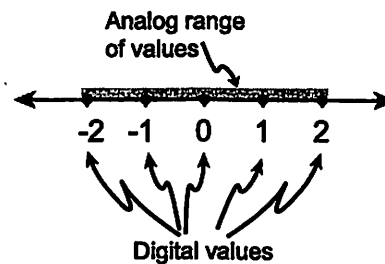


Figure 3.1 Possible analog and digital values between -2 and 2 .

All real, physical signals (e.g. acoustic waves, electromagnetic waves, etc.) are analog in nature. Yet with the rapid advances of the technology and algorithms associated with digital signal processing, it often becomes desirable to process the signal in the digital domain. Before this can be accomplished, a faithful representation of the analog signal must be constructed in the digital domain. This is done through the process of amplitude quantization, where a continuous range of analog amplitudes is mapped to a set of several discrete, or digital, amplitudes. Figure 3.2 shows the input/output transfer function of a typical quantization process. It is clear that the quantization process introduces error to the digital representation of the analog signal; the quantization error is merely the difference between the original analog amplitude and the quantized digital amplitude. One of the primary goals of analog-to-digital converters (ADC's) is to minimize this error.

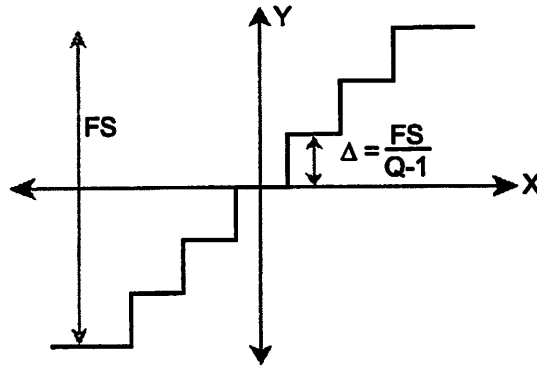


Figure 3.2 Quantization transfer function

3.2.1 Nyquist-Rate Converters

The term “Nyquist-rate converters” refers to the class of ADC’s where the output rate of the quantizer is equal to the ADC output rate. In this class of converters, the input/output transfer function of the ADC is typically identical to that of the quantizer itself. Thus, in order to analyze the quantization error of a Nyquist-rate converter, it is sufficient to only analyze the quantization error introduced by the quantization process. The error introduced by the quantization process, e_n , is simply:

$$e_n = y(x_n) - x_n \quad (3.1)$$

where x_n is the n th input and y_n is the corresponding output of the quantizer. Figure 3.3 shows the quantization error transfer function for the quantization transfer function shown in figure 3.2.

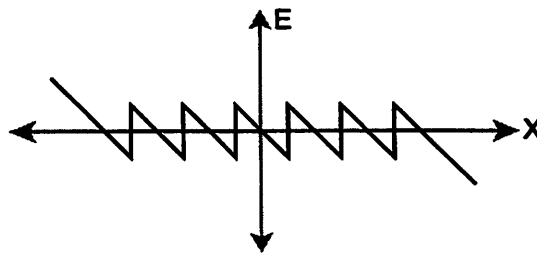


Figure 3.3 Quantization error for figure 3.2

Figure 3.3 demonstrates that the error is strongly correlated to the input. Under certain assumptions about the input spectrum and the operating conditions of the quantizer, Bennett proved in [34] that the quantization error can be approximated as an additive white noise source. Furthermore, the error can be approximated with a boxcar pdf between the bounds of $\pm \Delta/2$. The total in-band quantization noise for a Nyquist-rate converter can then be calculated as the mean-square-value of the quantization error: [35]

$$P_{Q,Nyq} = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} q^2 dq = \frac{\Delta^2}{12} \quad (3.2)$$

The quantization noise is proportional to the square of the quantizer step-size, Δ , (relative to full scale). Hence, as the step size is decreased by adding additional quantization levels, the overall quantization noise power decreases. Stated more succinctly, a quantizer with a finer bit resolution adds less quantization noise.

3.2.2 Sigma-Delta Converters

Sigma-delta converters use feedback and oversampling to suppress the in-band quantization noise. This is done by shaping the spectrum of the quantization noise with a high-pass transfer function. The noise is shaped to lie primarily outside the signal band of interest and can be removed with subsequent digital low-pass filters. Hence, by shaping the quantization noise spectrum out of the signal band, $\Sigma\Delta$ modulators are able to attain high signal-to-noise ratios with low resolution quantizers. Figure 3.4(a) shows the block diagram for a first-order sigma-delta. Figure 3.4(b) shows a linearized equivalent block diagram; the integrator block is replaced by its discrete time equivalent, and the quantizer is replaced by its equivalent additive white noise source, as explained in the previous section.

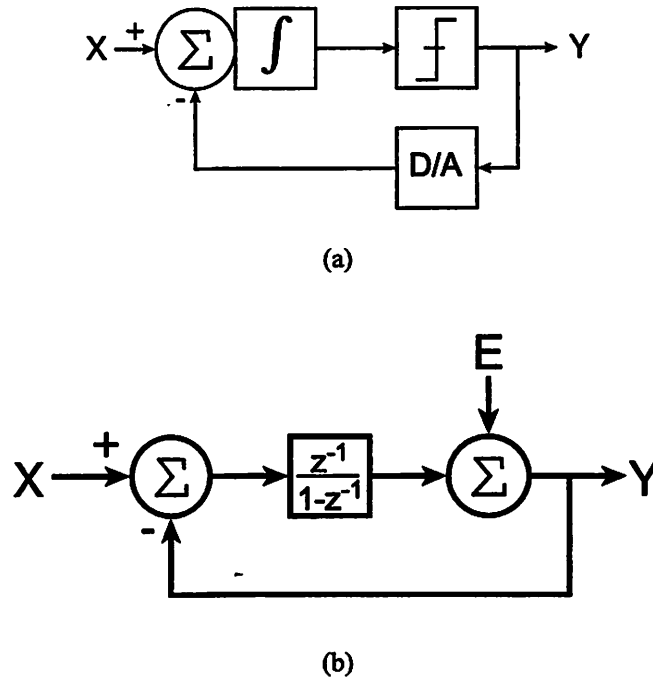


Figure 3.4 1st-Order Sigma-Delta Modulator: (a) Block diagram (b) Linearized model

There are two important transfer functions that can be determined from figure 3.4(b): the signal transfer function (*STF*) and the noise transfer function (*NTF*). Using simple feedback analysis, they are given by

$$STF \equiv \frac{Y(z)}{X(z)} = \frac{\frac{z^{-1}}{1-z^{-1}}}{1 + \frac{z^{-1}}{1-z^{-1}}} = z^{-1} \quad (3.3)$$

$$NTF \equiv \frac{Y(z)}{E(z)} = \frac{1}{1 + \frac{z^{-1}}{1-z^{-1}}} = 1 - z^{-1} \quad (3.4)$$

Therefore, the *STF* is simply a unit delay. A signal that is input to the $\Sigma\Delta$ is passed through without any frequency distortion. The *NTF*, however, has a frequency-selective characteristic, shaping the additive white noise source, $E(z)$, with a high-pass characteristic.

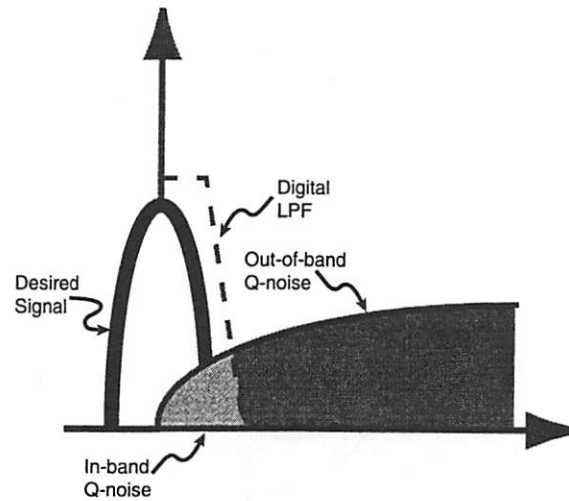


Figure 3.5 Noise-shaped spectrum and LPF

If the $\Sigma\Delta$ converter is oversampled, the shaped quantization noise is spread over the entire sampling bandwidth. The signal bandwidth becomes a small fraction of the entire sampling bandwidth. Subsequent digital filters can low-pass filter the modulator output and remove the quantization noise without altering the signal bandwidth, as demonstrated in figure 3.5. The power of the in-band quantization noise can be calculated as

$$P_{Q,\Sigma\Delta} = \int_{-f_{BW}}^{f_{BW}} \frac{P_{Q,Nyq}}{M} (1 - z^{-1}) \Big|_{z=e^{2\pi jf}} df = \frac{P_{Q,Nyq}}{M^3} \cdot \frac{\pi^2}{3} \quad (3.5)$$

Feedback analysis can be used to qualitatively explain the high-pass noise shaping phenomenon. From figure 3.4(b), the feedforward portion of the NTF is a unity gain; its feedback path is comprised of the discrete-time integrator. From feedback analysis, the overall NTF should have a characteristic opposite to its feedback transfer function. Therefore, we expect the NTF to possess the high-pass characteristic of a differentiator.

The qualitative analysis above motivates the understanding that a sharper low-pass characteristic in the $\Sigma\Delta$ feedforward path will result in a sharper high-pass NTF. It can be shown that a L -th order modulator will give an NTF of $(1 - z^{-1})^L$. Therefore, equation (3.5) can be generalized for higher-order $\Sigma\Delta$ modulators:

$$P_{Q,\Sigma\Delta} = \int_{-f_{BW}}^{f_{BW}} \frac{P_{Q,Nyq}}{M} (1-z^{-1})^L df = \frac{P_{Q,Nyq}}{M^{2L+1}} \cdot \frac{\pi^{2L}}{2L+1} \quad (3.6)$$

The dynamic range of an ideal sigma-delta modulator can then be expressed in decibels as:

$$DR_{\Sigma\Delta} = 10 \cdot \log_{10} \left[\frac{3}{2} (Q-1)^2 \cdot \frac{2L+1}{\pi^{2L}} \cdot M^{2L+1} \right] \quad (3.7)$$

Q = number of levels in quantizer

L = modulator order

M = oversampling ratio

It can be seen that there are three mechanisms which can be used to increase the dynamic range of a $\Sigma\Delta$. For each doubling of the number of quantization levels in the quantizer, the dynamic range is increased by roughly 6 dB. For each doubling of the oversampling ratio, the dynamic range increases by $(6L + 3)$ dB. Alternatively stated, increasing the order of the modulator by one increases the dynamic range by $20 \log_{10}(M/\pi)$ dB. It is important to note the synergistic effect of increasing the oversampling ratio and the modulator order; increasing both of these parameters gives far greater increase in DR than increasing one at the expense of the other. There are several limitations to the expression given in (3.7), and these will be discussed in the following section.

3.3 Constraints of High-Bandwidth Sigma-Deltas

$\Sigma\Delta$'s are uniquely suited to low-bandwidth, high-resolution applications. High resolution $\Sigma\Delta$ modulators can be implemented by using a simple modulator structure and greatly oversampling a relatively low bandwidth. For instance, a second-order modulator is able to achieve a dynamic range of 89 db when the oversampling ratio is 256 [31]. This approach is suitable for audio applications, where a Nyquist bandwidth of 16 kHz corresponds to a sampling frequency of 4 MHz. For applications where the signal bandwidths are in the MHz range, this approach can no longer be used as current CMOS technology cannot support the sampling rates required by such a simple topology.

Referring back to (3.7), there are three parameters of a $\Sigma\Delta$ modulator that can be increased in order to obtain higher DR: modulator order (L), oversampling ratio (M), and quantizer resolution (Q). Architecture techniques that allow each of these three parameters to be increased are examined below. Before continuing this discussion, it is important to note that the approaches detailed below are effective methods to reduce quantization noise. Other noise sources, such as thermal noise or digital noise coupling, must be suppressed by other methods.

3.3.1 Loop Filter Topologies

The loop filters used in sigma-delta modulators can be classified into two broad groups: single-loop or multi-stage⁴ modulators. A single-loop architecture employs a given number of integrators and only one quantizer/DAC pair. The output of the DAC is fed back to some or all of the integrators, and the digital output stream is taken from the single quantizer. A generic third-order single-loop $\Sigma\Delta$ is shown in Figure 3.6. A multi-stage $\Sigma\Delta$ consists of several single-loop $\Sigma\Delta$'s cascaded, where each subsequent stage quantizes the error from the previous stage. The several digital bit-streams are recombined in the digital domain in order to cancel out the quantization errors from all stages except the last. A 2-1 cascade is shown in Figure 3.7. This section will compare single-loop and multi-stage modulators in order to determine their suitability for high-speed data conversion.

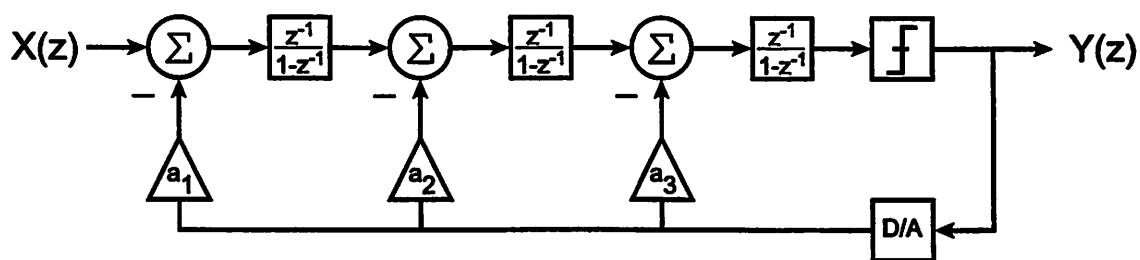


Figure 3.6 Third-order single-loop $\Sigma\Delta$ with distributed feedback

⁴ Also known as “cascade” or “MASH” $\Sigma\Delta$ modulators.

Single-loop $\Sigma\Delta$ Figure 3.6 shows a generic third-order single-loop $\Sigma\Delta$. Using the feedback analysis presented in section 3.2.2, its NTF is calculated in (3.8).

$$NTF(z) = \frac{(1-z^{-1})^3}{(1-z^{-1})^3 + a_3 z^{-1}(1-z^{-1})^2 + a_2 z^{-2}(1-z^{-1}) + a_1 z^{-3}} \quad (3.8)$$

It can be observed that the NTF above has three zeros at DC. The integrators can be transformed into resonators if local feedback is added around the integrator pairs. In this way, the NTF zeros are spread across the signal band, improving quantization noise suppression in the band of interest [36].

Single-loop $\Sigma\Delta$ modulators are attractive to design because of their relative simplicity and insensitivity to circuit imperfections such as component mismatch or finite gain. Analysis and simulation of a second-order $\Sigma\Delta$ show that it is able to achieve 89 dB resolution with an OSR of 256, even with circuits that have an open-loop gain on the order of the OSR and a unity-gain bandwidth on the order of $f_s/2$ [31]. The use of second- (or first-) order $\Sigma\Delta$ modulators is limited to low-bandwidth applications, as they require a very high oversampling ratio in order to attain high resolution. Additionally, low-order single-loop $\Sigma\Delta$'s tend to have significant tonal content in their output [28]. Therefore, higher-order loops are required.

Problems arise with the single-loop approach when the modulator order is higher than two. In particular, these types of modulators display a tendency towards instability; in order to guarantee stability, the designer must make the overall NTF of the $\Sigma\Delta$ loop sub-optimal [28]. For instance, the study in [36] has shown that the optimal DR for a stable 4th-order single-loop $\Sigma\Delta$ is roughly 38 dB below that predicted by ideal DR equation in (3.7). This severely limits the applicability of single-loop, single-bit $\Sigma\Delta$'s, as these types of modulators cannot achieve a stable dynamic range above 45dB at an OSR of 16, regardless of the modulator order [36].

Multi-stage (Cascade) $\Sigma\Delta$ An alternative approach to attaining high modulator order while maintaining modulator stability is to implement the $\Sigma\Delta$ as a cascade of stable low-order loops. The first stage performs rough quantization on the input signal, and all subsequent stages quantize the error from the stage preceding it. The numerous digital bit

streams are recombined in the digital domain, (ideally) canceling out all quantization noise except that from the last stage. In this manner, the overall noise shaping characteristic is identical to that of a single-loop modulator whose order is equal to the sum of the order of the cascaded loops. Figure 3.7 shows a generic cascade of a second-order loop followed by a first-order loop, termed a 2-1 cascade. The quantization error from the first stage, E_1 , is passed through an inter-stage gain, g_1 , and then applied to the second stage. Equation (3.9) below shows a calculation of the output spectrum.

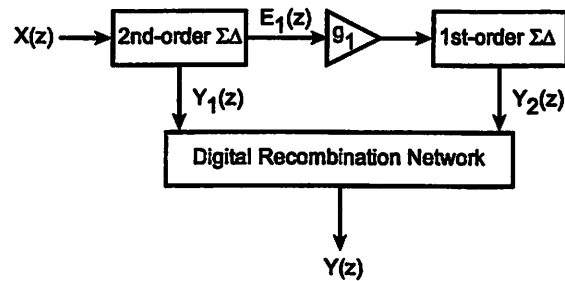


Figure 3.7 Generic 2-1 cascade $\Sigma\Delta$ modulator

$$\begin{aligned}
 Y_1(z) &= z^{-2}X(z) + (1 - z^{-1})^2 E_1(z) \\
 Y_2(z) &= z^{-1} \cdot g_1 \cdot E_1(z) + (1 - z^{-1})E_2(z) \\
 Y(z) &= H_1(z)Y_1(z) + H_2(z)Y_2(z) \\
 &= z^{-3}X(z) + z^{-1} \left(1 - \frac{g_1}{g_{1d}} \right) (1 - z^{-1})^2 E_1(z) - \frac{(1 - z^{-1})^3}{g_{1d}} E_2(z) \quad (3.9)
 \end{aligned}$$

where

$$\begin{aligned}
 H_1(z) &= z^{-1} \\
 H_2(z) &= -\frac{(1 - z^{-1})^2}{g_{1d}}
 \end{aligned}$$

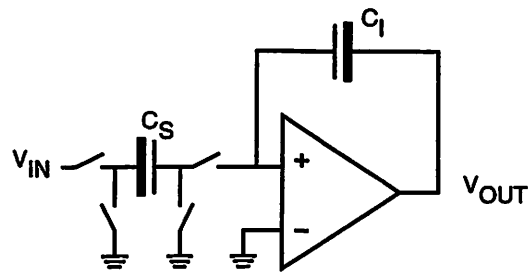
The digital recombination filter cancels out approximately all of the quantization error from the first stage, leaving the error from the second stage and a delayed version of the input in the output spectrum

Examination of the terms in (3.9) reveals two primary limitations on the performance of multi-stage $\Sigma\Delta$ modulators. The error term related to E_1 is identically zero if and only if the inter-stage gain, g_1 , is equal to its digital approximation, g_{1d} . For reasons that will be further explained in Section 4.5, this condition cannot be guaranteed. Hence,

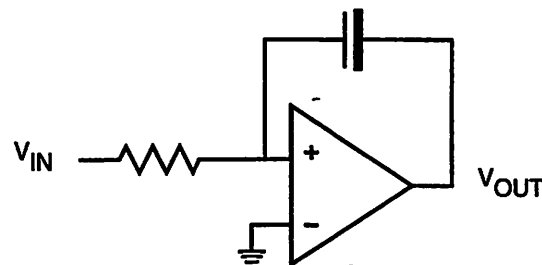
there will typically be leakage of the first-stage quantization error, which is only suppressed by second-order noise shaping. The designer must take care not to have the $\Sigma\Delta$ performance limited by this noise leakage. Additionally, the error term related to E_2 is amplified by $1/g_{1d}$. This factor is typically less than or equal to one, so an ideal cascade architecture of a given order will tend to have a higher quantization noise level than that of a comparable, ideal single-loop modulator. On the other hand, a high-order cascade $\Sigma\Delta$ does not have the same instability concerns as a high-order, single-loop $\Sigma\Delta$. Hence, a cascade can have a significantly more aggressive NTF than its single-loop counterpart.

3.3.2 Discrete-Time vs. Continuous-Time

$\Sigma\Delta$ modulators can be implemented in discrete-time or continuous-time form. The primary difference between these two implementations resides in the structure of the integrator in the feedforward path: discrete-time $\Sigma\Delta$'s typically employ switched-capacitor integrators (figure 3.8a), whereas continuous-time $\Sigma\Delta$'s utilize either RC (figure 3.8b) or G_M/C integrators (figure 3.8c).



(a) Switched-capacitor integrator



(b) RC integrator

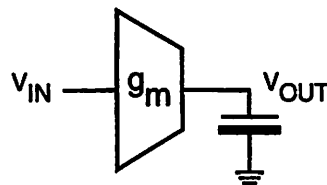
(c) G_M/C integrator

Figure 3.8 Discrete-time and continuous-time integrator implementations

The primary advantages of using a switched-capacitor $\Sigma\Delta$ ($SC\Sigma\Delta$) stem from the fact that this approach is well-suited to current CMOS technology. The capacitors can be fabricated as a “sandwiched” stack of metal and/or poly. These capacitor stacks tend to be fairly linear, and the VLSI processing capabilities of CMOS technology allow for control of the capacitive ratio (C_S/C_I) to within about 1%. This capacitive ratio determines the pole location of the integrator, so accurate control is crucial for noise suppression. Furthermore, as all loads in a switched-cap $\Sigma\Delta$ are capacitive, the amplifiers do not need a power-hungry output stage.

The main advantage of continuous-time $\Sigma\Delta$ ($CT\Sigma\Delta$) is that, for a given technology, a $CT\Sigma\Delta$ is typically able to achieve a higher OSR than a $SC\Sigma\Delta$ [33].

Furthermore, CT $\Sigma\Delta$ systems provide implicit anti-alias filtering, thus reducing the need for explicit anti-alias filtering prior to the modulator. In a CT $\Sigma\Delta$, the sampling instant occurs at the quantizer; at that point in the modulator, the loop filter of the CT $\Sigma\Delta$ has already attenuated signal energy that might otherwise fold down to baseband.

There are serious drawbacks to using a CT $\Sigma\Delta$ modulator. Depending on the actual circuit implementation, a CT $\Sigma\Delta$ requires a highly linear resistor or transconductor; modern CMOS processes are not particularly well-suited to implementing these devices. Additionally, the pole location of these integrators are set by the RC (or C/G_M) time constants of these devices. As the time constant is set by a product of two dissimilar device parameters (rather than as a ratio of similar device parameters), the accuracy of these pole locations is limited to about $\pm 30\%$. This large mismatch greatly limits the efficacy of multi-stage CT $\Sigma\Delta$ architectures without adding elaborate tuning mechanisms. CT $\Sigma\Delta$'s are also more sensitive to clock jitter and quantizer metastability. Both these phenomena cause random pulse width modulation in the feedback DAC, which in turn causes high-frequency quantization noise to fold into the signal bandwidth [33]. Additionally, design methodologies for and circuit requirements of CT $\Sigma\Delta$ modulators are still not fully understood at this current time, although there is much ongoing research in this field [33] [37].

3.3.3 Single-Bit vs. Multi-Bit Quantization

The previous two sections have discussed techniques to increasing the order and oversampling ratio of $\Sigma\Delta$ modulators. This section discusses the trade-offs involved with changing the number of levels in the quantizer of an $\Sigma\Delta$ modulator. While $\Sigma\Delta$ modulators have traditionally employed single-bit quantizers, there is nothing fundamental which prevents $\Sigma\Delta$ loops from using multi-bit quantizers. The advantages and challenges of both approaches are outlined below.

The primary advantage of utilizing a multi-bit quantizer is that the total power level of the quantization noise is decreased with an increased number of quantization levels. As explained in section 3.2, total quantization noise power is directly proportional to the square of the quantizer step size. Hence, doubling the number of levels (halving the

step size) in the quantizer decreases the noise power (increases the resolution) by 6 dB, or one bit.

Multi-bit quantizer/DAC pairs also have another advantage when used in high-order single-loop $\Sigma\Delta$'s. As explained in section 3.3.1, single-loop $\Sigma\Delta$'s must employ non-optimal noise-shaping filters in order to guarantee stability. The instability of single-loop $\Sigma\Delta$ modulators is due to the hard non-linearity of the quantizer embedded within the feedback loop [28]. With multi-level quantization, the hard non-linearity of the quantizer becomes less pronounced; the de-emphasis of the quantizer's hard non-linearity makes the $\Sigma\Delta$ loop more stable and allows the $\Sigma\Delta$ designer to utilize a much more aggressive NTF. As an example, [38] presents a third-order 4-bit SD modulator that achieves 95dB dynamic range with an oversampling ratio of 24. This represents an NTF that has roughly 19 dB more noise suppression than the optimal stable NTF of a comparable single-bit topology [28]

There are several limitations to the applicability of multi-level quantization within $\Sigma\Delta$ modulators. One such limitation stems from the fact that the $\Sigma\Delta$ loop requires the quantizer/DAC pair to quantize the input and feedback an output at the oversampled rate with a latency of only one clock cycle. This requirement necessitates the use of a flash ADC as the quantizer. The flash architecture can be very area- and power-hungry for high resolutions, as the amount of circuitry required is directly proportional to the number of quantization levels desired.

The primary limitation of multi-level $\Sigma\Delta$ modulation, however, lies within the implementation of the feedback DAC. In order to have a multi-level $\Sigma\Delta$ loop, the feedback DAC must also be multi-level. While a single-bit feedback DAC is linear by construction, the linearity of a multi-level DAC is limited by the component matching of its individual elements. Furthermore, the output of the feedback DAC is fed into the same point of the $\Sigma\Delta$ loop as the input signal; thus, the transfer function from the DAC to the output (*DACTF*) will be the same as the *STF*. As Figure 3.9 and equation (3.10) demonstrate, "noise" generated by DAC non-linearity will not be suppressed by the $\Sigma\Delta$ noise-shaping. Therefore, while the DAC requires a *resolution* only equal to that of the quantizer, it requires an *accuracy* equal or greater than the resolution of the entire

converter. Achieving such DAC performance in compact chip areas and at low-power levels is a very difficult task.

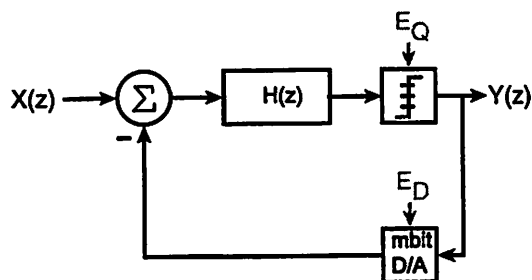


Figure 3.9 DAC impairments in a multi-bit $\Sigma\Delta$

$$Y(z) = z^{-L}X(z) + (1 - z^{-1})^L E_Q(z) - E_D(z) \quad (3.10)$$

Previously published results have suggested several improvements to the basic $\Sigma\Delta$ architecture in order to alleviate the problems associated with the implementation of a multi-level quantizer and feedback DAC. The Leslie-Singh architecture, also known as the dual-quantization technique, uses a multi-stage cascade strategy in order to implement multi-bit quantization [39]. A generic 1st-order Leslie-Singh architecture is shown in figure 3.10. The core $\Sigma\Delta$ loop remains a single-bit structure, thus removing the need for a linear multi-level DAC. This loop is followed by a multi-bit quantizer to quantize the error in the $\Sigma\Delta$ loop output. After proper digital recombination, the overall noise-spectrum is similar to that of a typical multi-bit $\Sigma\Delta$. Another side benefit of this approach is the removal of the requirement that the multi-level quantizer has only a single cycle latency. As the multi-level quantizer is no longer embedded in a feedback loop, it can be replaced by more efficient structures that tradeoff increased latency for reduced power and area [28]. However, like all cascade modulators, the Leslie-Singh structure is susceptible to analog/digital mismatch. As shown in (3.11), mismatch in the effective gain coefficient of the multi-bit converter results in noise-leakage from the single-bit quantizer.

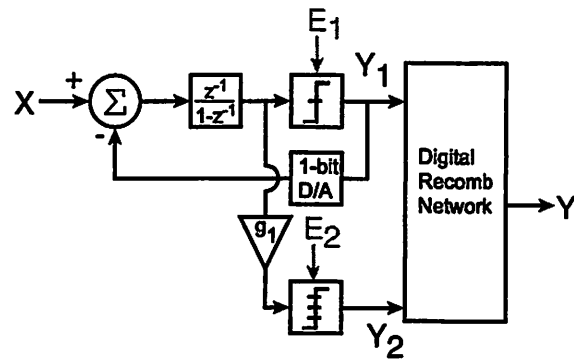


Figure 3.10 Leslie-Singh dual-quantizer architecture

$$\begin{aligned}
 Y_1(z) &= z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E_1(z) \\
 Y_2(z) &= g_1 \cdot (z^{-1} \cdot X(z) - z^{-1} \cdot E_1(z)) + E_2(z) \\
 Y(z) &= H_1(z) \cdot Y_1(z) + H_2(z) \cdot Y_2(z) \\
 &\approx z^{-1} \cdot X(z) + \left(1 - \frac{g_1}{g_{1d}}\right) \cdot z^{-1} \cdot (1 - z^{-1}) \cdot E_1(z) + \frac{1}{g_{1d}} \cdot (1 - z^{-1}) E_2(z) \quad (3.11)
 \end{aligned}$$

where

$$\begin{aligned}
 H_1(z) &= z^{-1} \\
 H_2(z) &= \frac{1}{g_{1d}} (1 - z^{-1})
 \end{aligned}$$

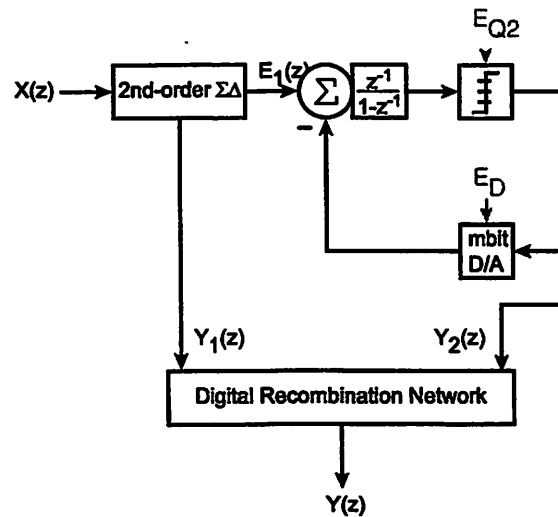


Figure 3.11 Multi-bit cascade $\Sigma\Delta$

An alternative method to suppressing the effects of a non-linear multi-level DAC is presented in [40]. This approach utilizes a cascaded $\Sigma\Delta$ with a multi-bit quantizer/DAC

in only the last stage, shown in figure 3.11. Under ideal conditions, the recombined output spectrum will be

$$Y(z) = z^{-3}X(z) + (1 - z^{-1})^3 E_{Q2}(z) \quad (3.12)$$

where $E_{Q2}(z)$ is the approximate additive white noise from an ideal multi-level quantizer. It is argued in [40] that the output of the second stage of the modulator in figure 3.11 is approximately white. As the output of the second stage is also the input to the multi-level DAC, it is argued that the DAC signal is sufficiently “busy” that its non-linearity can be represented as an additive noise, $E_D(z)$. Including this effect, and again solving for the recombined output spectrum:

$$Y(z) = z^{-3}X(z) + (1 - z^{-1})^3 E_{Q2}(z) + (1 - z^{-1})^2 E_D(z) \quad (3.13)$$

It can be observed that the “noise” from the DAC non-linearity has been suppressed by second-order noise-shaping. Intuitively, this can be understood by observing that the output of the multi-bit DAC is fed back into the circuit after the second-order loop. Hence, this noise can be referred back to the input only after it is shaped by that second-order loop. More generally, the noise from a non-linear DAC in the L^{th} stage of a multi-stage modulator is shaped by N^{th} order noise shaping at the output, where N is the total number of integrators in stages 1 to $L-1$.

A third technique to suppress the nonlinear DAC “noise” uses digital scrambling techniques to either whiten [41] or shape [42][43][44] the effective noise from the nonlinear DAC. If the DAC is composed of N unit-weighted elements, each unit element can be represented as

$$\begin{aligned} d_i &= d_{AVG} + e_i & i &= 1, \dots, N \\ \sum_{i=1}^N e_i &= 0 \end{aligned} \quad (3.14)$$

where d_{AVG} is the average analog unit output value and e_i is the error of the i^{th} unit element. In order to represent an analog value of $m \cdot d_{AVG}$, m unit elements must be activated. If the DAC element selection algorithm for simply to activate the first m unit elements out of the set of N , the actual output will be

$$V_{out} = m \cdot d_{AVG} + \sum_{i=1}^m e_i \quad (3.15)$$

While this selection method is the most intuitive approach, it should be observed that there exists $\binom{N}{m}$ different ways representing the desired analog value. Furthermore, it should be noted that if all $\binom{N}{m}$ different combinations are used equally, the long-term average of the error goes to zero.

This observation forms the basis of the technique called dynamic element matching [28]. By employing a DAC element selection algorithm that digitally scrambles DAC element utilization, dynamic element matching is able to either whiten or shape the noise from a nonlinear DAC. Shaping the DAC noise is particularly attractive, as it pushes much of the noise outside of the signal bandwidth in highly oversampled systems. Many circuits have been demonstrated that exhibit first-order noise-shaping of the DAC non-linearity [43][44], and algorithms to extend this shaping characteristic to higher-order suppression have been developed [42]. A problem with this approach is the large amount of digital circuitry needed to implement high-order shaping [45]. Additionally, a unit-element DAC may not be the most efficient implementation in switched-capacitor circuits [40]. Nonetheless, dynamic element matching is a good technique for creating multi-bit $\Sigma\Delta$ modulators without high-precision DAC elements.

One serious drawback of multi-bit $\Sigma\Delta$ modulation, however, stems from the fact that a multi-bit quantizer/DAC pair has a fixed equivalent gain associated with it, whereas a single-bit quantizer/DAC pair can have an arbitrary equivalent gain. The fixed gain associated with a multi-bit quantizer tends to force very high forward-gain coefficients in the integrators of cascade modulators. As will be shown in Section 3.4.3, integrators with high forward gain-coefficients are not amenable to low-power operation at high-speeds.

3.4 Fundamental Power Limits

The previous sections in this chapter have discussed the fundamentals of $\Sigma\Delta$ modulation and some of the techniques useful for maximizing the achievable resolution of high-bandwidth $\Sigma\Delta$ systems. This section addresses the issue of power consumption in

$\Sigma\Delta$ modulators. While Chapter 5 discusses practical methods for minimizing power consumption through circuit design techniques, it is instructive to first examine the fundamental limits on low-power design of $\Sigma\Delta$ modulators.

This section assumes that the $\Sigma\Delta$ modulator is built using switched-capacitor techniques. While section 3.3.2 demonstrated that there are some advantages to a continuous-time approach, it was deemed that the limitations presented in that section, specifically those preventing high-order modulator design, limited the applicability of the continuous-time approach to this application. In a switched-capacitor implementation, there are two fundamental contributors to power dissipation. The first is dynamic power; this is the power required to charge and discharge capacitors that function as signal-charge storage devices in the integrator. The other source of power dissipation is the static power dissipated by the active devices within the integrator amplifier. The fundamental limits for the dynamic and static power dissipation of a $\Sigma\Delta$ modulator will be examined below. This first part of this section consists of a review of the results derived in [16]. Further derivations are then performed to better understand practical power limits at fast conversion rates, where capacitive parasitics are typically no longer negligible.

3.4.1 Dynamic Power

Figure 3.8(a) on page 32 shows the configuration of a typical switched-capacitor integrator. Dynamic power refers to the power dissipated through the charging and discharging of the charge-storing capacitors in the integrator and represents an absolute lower bound on the power dissipation; in reality, total power dissipation will be several orders of magnitude higher than this limit. A complete derivation of the dynamic power limit can be found in the [16], and only the result will be stated here:

$$P_{DYN} \propto kT(DR)f_N \quad (3.16)$$

where DR is the required dynamic range and f_N is the Nyquist rate. This derivation ignores quantization noise and assumes that the circuit dynamic range is solely limited by thermal noise. It is worth noting that the dynamic power limitation is independent of the power supply voltage (V_{dd}) or oversampling ratio (M).

3.4.2 Static Power with Negligible Parasitics

Circuits that employ class A amplifiers typically have a power consumption significantly higher than the limit shown in (3.16). This is due to the fact that the static power dissipated by the active devices comprising the amplifier is far greater than the dynamic power required to charge and discharge the signal capacitors. A simple class A amplifier is a single-transistor amplifier, shown in 3.12 [16].

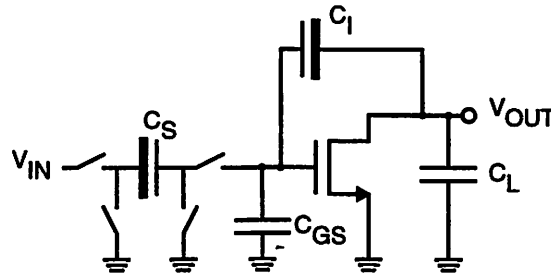


Figure 3.12 Simplified CMOS integrator schematic

The static power dissipated by the amplifier is

$$P_{STAT} = V_{DD} I_{BIAS} \quad (3.17)$$

If the active device is biased at a constant current density (I_{BIAS} / W_N is held constant), then the device transconductance (g_m) is also proportional to bias current, so:

$$P_{STAT} \propto V_{DD} g_m \quad (3.18)$$

The total effective capacitance at the output node is

$$C_{L,TOT} = C_L + \frac{C_I (C_S + C_{GS})}{C_I + C_S + C_{GS}} \quad (3.19)$$

and the feedback factor is

$$f = \frac{C_I}{C_I + C_S + C_{GS}} \quad (3.20)$$

If the conversion bandwidth is significantly smaller than the process f_T , C_{GS} will be small and can be ignored. If it is further assumed that C_L is negligibly small compared to C_S and C_I , then the following approximations can be made:

$$C_{L,TOT} \approx \frac{C_I \cdot C_S}{C_I + C_S} \quad (3.21)$$

$$f \approx \frac{C_I}{C_I + C_S} \quad (3.22)$$

The closed-loop settling time constant, τ , is given by

$$\tau = \frac{C_{L,TOT}}{f \cdot g_m} \approx \frac{C_S}{g_m} \quad (3.23)$$

If it is assumed that the circuit requires χ time constants to adequately settle during its settling phase, then

$$\tau_{req'd} = \frac{1}{\chi \cdot M \cdot f_N} \quad (3.24)$$

$$g_m = \chi \cdot M \cdot f_N \cdot C_S \quad (3.25)$$

where χ is a system constraint determined by behavioral simulations.

The dynamic range of the integrator is the ratio of the input signal power to the thermal noise power. Assuming that the input peak-to-peak signal swing is equal to some fraction, β , of V_{DD} , the maximum signal power is

$$P_{sig,MAX} = \frac{(\beta \cdot V_{DD})^2}{8} \quad (3.26)$$

The total in-band thermal noise is proportional to the kT/C noise divided by the oversampling ratio [16].

$$P_{N,inband} \propto \frac{kT}{M \cdot C_S} \quad (3.27)$$

The dynamic range is then proportional to:

$$DR \propto \frac{(\beta \cdot V_{DD})^2 M \cdot C_S}{8kT} \quad (3.28)$$

Plugging (3.25) and (3.28) into (3.17), the static power dissipation can be derived

$$P_{STAT} \propto \frac{8kT(DR)\chi \cdot f_N}{\beta^2 V_{DD}} \quad (3.29)$$

(3.25) shows that the static power dissipation is proportional to the product of the dynamic range and the Nyquist rate. Also, the static power dissipation has a strong inverse relationship to available swing. This bodes poorly for power dissipation in deep-submicron low-voltage CMOS processes; not only because power dissipation is inversely

proportional to V_{DD} , but also because β will tend to decrease with decreasing supply voltage [46].

3.4.3 Static Power with Capacitive Parasitics

(3.29) shows a derivation of the static power limit under the assumption that capacitive parasitics are negligibly small in comparison the primary charge-storage capacitors. This assumption does not hold when high-speed conversion is performed. In order to support high-speed performance, the transconductance of the amplifier has to be made large. Due to the finite process ω_T , this will cause the amplifier input capacitance to become comparable in size to the primary capacitors. Additionally, in processes where high-density capacitors are not available, the bottom-plate parasitics also become appreciable. This section rederives the results from the previous section when the assumption of negligible parasitics no longer holds. The derivation will be similar to that in Section 3.4.2, with changes made as needed.

The ratio of C_S to C_I is the forward gain of the integrator, A , and is usually fixed during system design. For integrators, usually $A < 1$.

$$C_S = A \cdot C_I \quad (3.30)$$

C_{GS} is no longer negligible. It is equal to g_m/ω_T . Also, as C_L is the load presented by the next integrator plus associated parasitics, it is assumed to be proportional to C_S , with the proportionality constant η fixed by process parameters.

$$C_{GS} = g_m / \omega_T \quad (3.31)$$

$$C_L = \eta \cdot C_S \quad (3.32)$$

Therefore, (3.21) and (3.22) can be expressed as

$$C_{L,TOT} = \eta \cdot C_S + \frac{\frac{C_S}{A} (C_S + g_m/\omega_T)}{\frac{C_S}{A} + C_S + g_m/\omega_T} \quad (3.33)$$

$$f = \frac{\frac{C_S}{A}}{\frac{C_S}{A} + C_S + g_m/\omega_T} \quad (3.34)$$

Substituting the above equations into (3.23) and (3.24) and solving for g_m :

$$g_m = \frac{C_S \cdot f_N \cdot \chi \cdot M(1 + \eta + A\eta)}{1 - \frac{f_N \cdot \chi \cdot M(1 + A\eta)}{\omega_T}} \quad (3.35)$$

Using (3.28) to complete the derivation, static power is found to be

$$P_{STAT} \propto \frac{8kT(DR)\chi \cdot f_N}{\beta^2 V_{DD}} \cdot \frac{(1 + \eta + A\eta)}{\left(1 - \frac{f_N \cdot \chi \cdot M(1 + A\eta)}{\omega_T}\right)} \quad (3.36)$$

The first factor in (3.36) is the same as in (3.29); hence all the proportionalities regard dynamic range and voltage swing still hold. The second factor of (3.36) indicates excess power consumption due to parasitic considerations and deserves further examination.

The numerator of the second factor in (3.36) is independent of operating frequency and is only dependent on the effective parasitic loading presented at the output. It should be noted, however, the effective loading is dependent on the forward-gain, A , of the integrator. The numerator shows that integrators with low forward-gain factors are more amenable to low-power implementation than those with high forward gain factors. This observation should be coupled into the block-level design of a $\Sigma\Delta$ modulator in order to design a power-optimized system.

The denominator of (3.36) demonstrates that the power consumption increases dramatically as the required circuit speed approaches the device ω_T . Recalling from (3.24) that the required closed-loop time constant is equal to $(f_N \cdot \chi \cdot M)^{-1}$ and that the closed-loop dominant pole, $\omega_{UT,req}$ is equal to $(\tau_{req})^{-1}$, the required static power becomes unbounded as

$$\omega_{UT,req} \rightarrow \frac{\omega_T}{1 + A \cdot \eta} \quad (3.37)$$

Again, it is worth noting that the upper achievable bound on $\omega_{UT,req}$ is not only determined by device ω_T and parasitic loading, but is also affected by the integrator forward gain. As the denominator of (3.36) puts an absolute upper bound on the frequency of operation, it is crucial that the block-level design accommodates for this limitation by keeping the integrator gain, A , as small as possible. Figure 3.13 shows normalized plots of static power dissipation versus $\omega_{UT,req}$ for various A , η configurations.

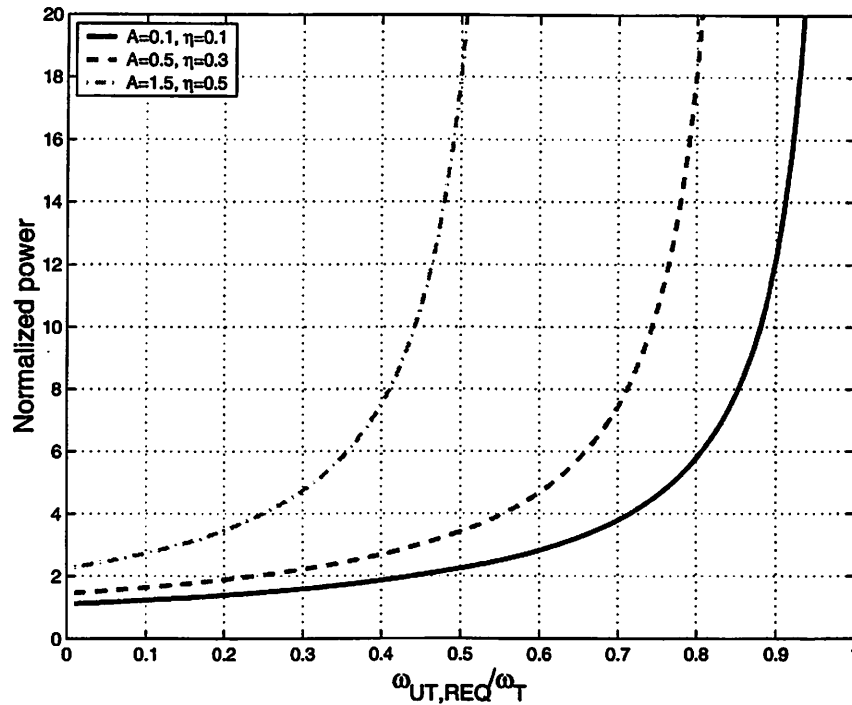


Figure 3.13 Normalized static power dissipation vs. $\omega_{UT,req}$. A is the integrator forward gain, η the parasitic loading parameter.

3.5 Summary

This chapter began with a review of the process of quantization in analog-to-digital converters. Next, sigma-delta conversion was introduced. The concept of noise-shaping was discussed, and techniques to increase the resolution of $\Sigma\Delta$ converters were reviewed. The chapter focused on high-speed applications, and the efficacy of these techniques were evaluated in the context of high-speed operation. Finally, the fundamental dynamic and static power limits for switched-capacitor $\Sigma\Delta$ integrators were derived. Limitations due to high-speed operation were analyzed, and system-level considerations to combat these limitations were discussed.

Modulator Design

4.1 Introduction

This chapter describes the architecture techniques used to design a $\Sigma\Delta$ modulator that meets the required specifications. Emphasis is placed on achieving the required performance at a low oversampling ratio due to the wideband nature of the incoming signal. A 2-1-1 cascade $\Sigma\Delta$ architecture is presented. Internal signal scaling is performed in order to maximize the overload level of the modulator and minimize power dissipation. Capacitor scaling is also shown to be an effective method to reduce power dissipation. Simulation results which determine circuit block requirements are presented, and a simulation environment for rapid evaluation of analog impairments in a communications channel is introduced.

4.2 2-1-1 Cascade Architecture

As discussed in Section 3.3, the wideband nature of the desired signal requires a modulator architecture that can achieve the required performance at a low oversampling ratio (OSR). Additionally, it is desirable to have an OSR that is a power of two in order to

facilitate the decimation process. SPICE simulations of test circuits determined that a $0.25\ \mu\text{m}$ CMOS process could support an oversampling ratio of 8 ($f_{\text{NYQ}} = 25\ \text{MHz}$, $f_s = 200\ \text{MHz}$).

As discussed in Section 3.3.1, a cascade architecture is preferable at low oversampling ratios, as the instability problems associated with single-loop architectures greatly limit achievable dynamic range. In keeping with the discussion on low-power implementation in Section 3.4.3, it was decided that single-bit quantization was to be used throughout. Additionally, single-bit quantization will enhance the linearity performance of the $\Sigma\Delta$ modulator, as a single-bit quantizer is intrinsically linear.

Figure 4.1 shows the maximum achievable dynamic range of a single-bit $\Sigma\Delta$ modulator as a function of its oversampling ratio and modulator order. This figure was generated using equation (3.7). This figure also included the effect of noise enhancement due to small interstage gain coefficients of each particular architecture, as discussed in Section 3.3.1.

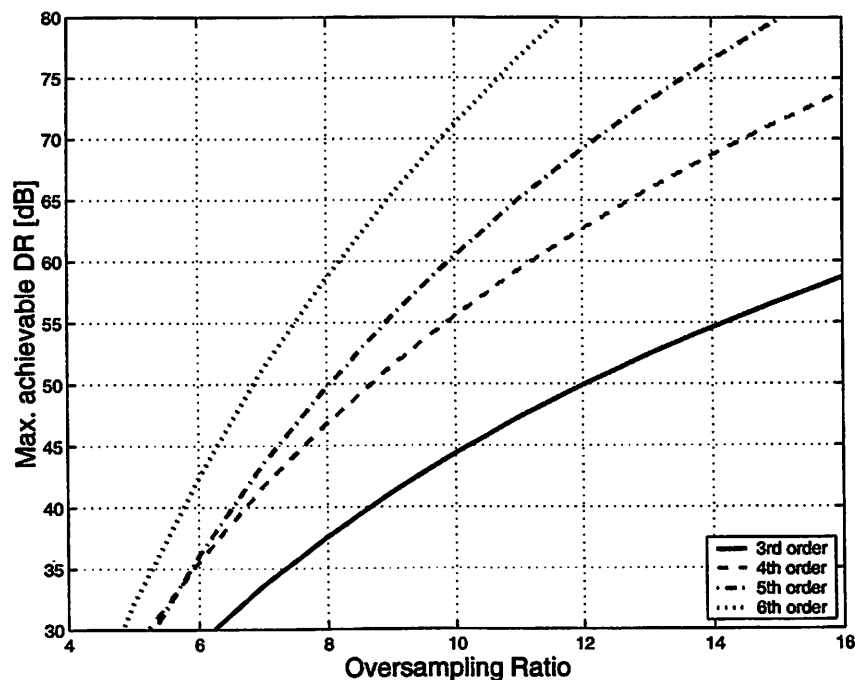


Figure 4.1 Maximum Achievable Dynamic Range for Various Cascade Modulators

A fourth-order modulator was selected, as it can achieve over 46 dB of dynamic range with an OSR of 8. A 2-1-1 cascade architecture was chosen, because it has been empirically shown in [47] that this has much better overload performance than a comparable 2-2 architecture. Single-bit quantizers were utilized in all three loops because of their intrinsic linearity and their amenability to low-power implementation, as mentioned above.

A basic block diagram of the 2-1-1 architecture is shown in Figure 4.2. Each integrator has a full clock delay between its input and output to create a fully pipelined structure.

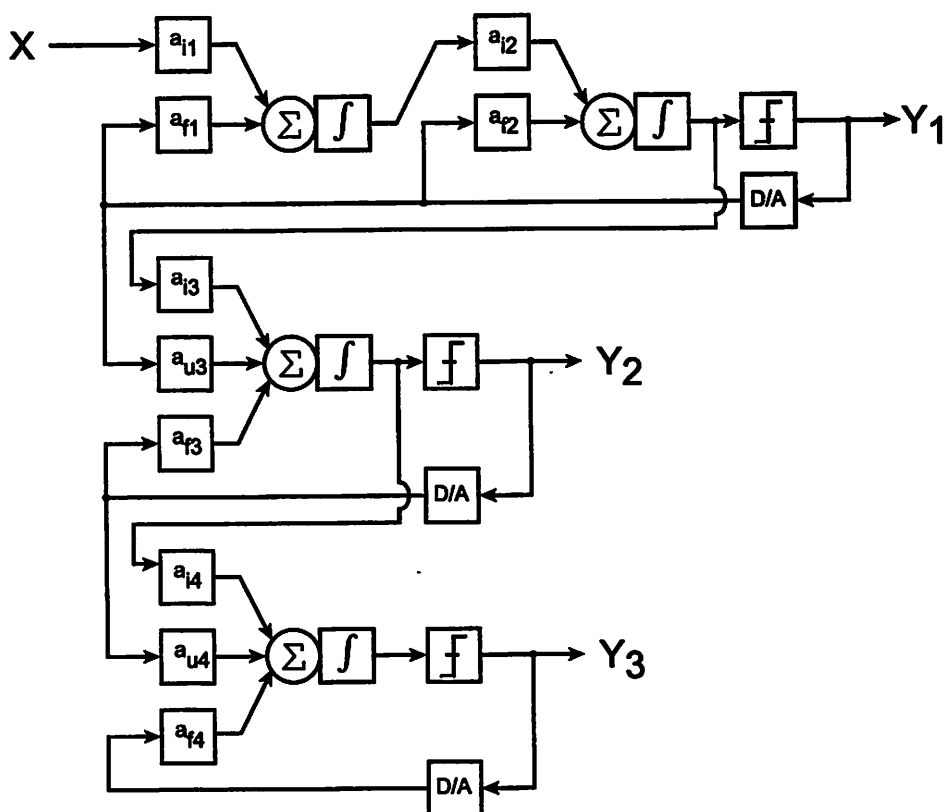


Figure 4.2 2-1-1 block diagram

4.3 Signal Scaling

In order to maximize the dynamic range of the $\Sigma\Delta$ modulator, it is important to maximize its input overload level. This is the input level at which clipping occurs at the

internal nodes. It is desirable to scale the internal signal levels such that they utilize the entire signal swing at the output of each integrator without clipping [32].

The gain coefficients for the 2-1-1 single-bit architecture are shown in Table 4.1 [30]. It should be noted that the gain coefficients are all similar values. As demonstrated in Section 3.4.3, a high forward gain coefficient is not amenable to low-power design. By spreading out the gain between the stages, individual gain coefficients can remain small and power consumption can be minimized on the system-level.

Coefficient	Value
a_{i1}	$1/3$
a_{f1}	$-1/3$
a_{i2}	$3/5$
a_{f2}	$-2/5$
a_{u3}	$5/6$
a_{i3}	$-1/2$
a_{f3}	$-1/3$
a_{u4}	$1/2$
a_{i4}	$-1/6$
a_{f4}	$-1/6$

Table 4.1 Gain Coefficients for 2-1-1 Cascade Modulator

Figure 4.3 shows the maximum integrator outputs for a given input power level. The modulator can accommodate a maximum input signal of -1.7 dB relative to the full-scale input before significant clipping occurs.

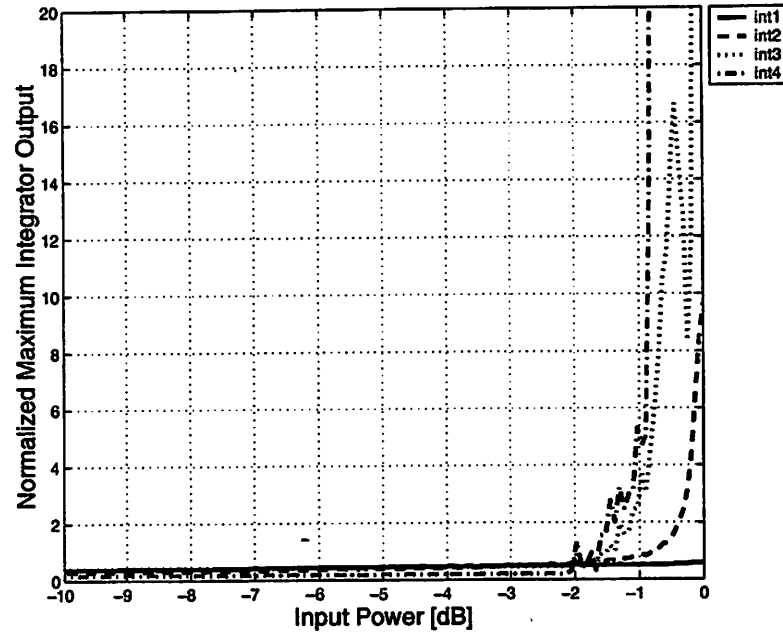


Figure 4.3 Maximum Integrator Output as a Function of Input Power

4.4 Capacitor Scaling

The power dissipation of the $\Sigma\Delta$ modulator can be reduced by utilizing a capacitor scaling approach similar to that employed in [16]. Noise shaping within the modulator reduces the effective input-referred thermal and flicker noise from later stages in the cascade of switched-capacitor integrators. As a result, the capacitor sizes of later stages can be reduced while still meeting overall noise requirements. This allows for reduced bias currents in later stages, thus reducing overall power dissipation. This approach is limited by the presence of parasitic capacitors, however.

The total in-band, input-referred thermal noise can be expressed as a weighted sum of each integrator's input-referred thermal noise, as in (4.1). A similar expression can be derived for input-referred flicker noise.

$$P_{N,tot} = P_{N1} \left(\frac{1}{M} \right) + P_{N2} \left(\frac{\pi^2}{3A_2^2 M^3} \right) + P_{N3} \left(\frac{\pi^4}{5A_3^2 M^5} \right) + P_{N4} \left(\frac{\pi^6}{7A_4^2 M^7} \right) \quad (4.1)$$

P_{Ni} = Input - referred noise of i - th integrator

$$A_k = \prod_{j=1}^k a_{ij}$$

It can be observed that increasing the oversampling ratio greatly decreases the noise contribution of later integrators in the cascade. With the small OSR of this architecture, however, the applicability of capacitor scaling is somewhat limited. Still, a power savings of roughly 15% can be achieved with this approach. The input-referred noise of each integrator will be derived in Section 5.3.

4.5 Analog/Digital Mismatch

Section 3.3.1 demonstrated that variation of the analog interstage gain coefficient from its nominal value can lead to noise leakage and performance degradation. Variation in the analog interstage gain coefficient arises from mismatch in the capacitor ratios in the modulator. Ignoring higher order terms, mismatch in a 2-1-1 cascade results in an output spectrum of:

$$Y(z) = z^{-3} X(z) + z^{-1} \left(1 - \frac{g_1}{g_{1d}} \right) (1 - z^{-1})^2 E_1(z) - \frac{(1 - z^{-1})^4}{g_{1d} \cdot g_{2d}} E_3(z) \quad (4.2)$$

The second term in (4.2) is the result of interstage gain mismatch. The amount of noise leakage is directly proportional to the mismatch between the actual interstage gain, g_1 , and its nominal (digital) value, g_{1d} . The noise leakage is also suppressed by second-order shaping; therefore, precise capacitor matching is not required.

For a 2-1-1 $\Sigma\Delta$ modulator, g_1 is a product of 3 independent capacitor ratios, where each capacitor ratio is determined by two independent capacitors. Therefore, g_1 is a function of six independent capacitors. Assuming each capacitor takes on the value of

$$C_i = C_{i,des} \cdot (1 + \delta_i) \quad i = 1, \dots, 6 \quad (4.3)$$

where C_i is the actual capacitor value, $C_{i,des}$ is the desired capacitor value. δ_i is the fractional mismatch, which is assumed to be a zero-mean Gaussian random variable with standard deviation, σ_c . Therefore, g_I can be expressed as:

$$g_I = \frac{\prod_{i=1}^3 C_i}{\prod_{j=4}^6 C_j} \quad (4.4)$$

For $\sigma_c \ll 1$, g_I can be shown to be a Gaussian random variable with mean of g_{Id} and standard deviation of $\sqrt{6}\sigma_c$.

4.6 Finite DC Gain

The noise-shaping action of a $\Sigma\Delta$ modulator is governed by the closed-loop transfer function of its filter. In particular, the efficacy of the noise-shaping is dependent on the assumption that the integrators have an infinite Q. Finite amplifier DC gain, however, will degrade the integrator Q, and in turn degrade the noise-shaping performance of a $\Sigma\Delta$ modulator. A block diagram of a switched-capacitor integrator with finite DC gain is shown in Figure 4.4. Solving the z-domain transfer function for this topology yields (4.5).

$$H(z) = \frac{C_s}{C_I} \cdot \beta \cdot \frac{z^{-1}}{1 - (1 - \varepsilon) \cdot z^{-1}} \quad (4.5)$$

where $\beta = \left(\frac{1}{1 + \frac{C_s + C_I}{A \cdot C_I}} \right)$, $\varepsilon = \frac{1}{1 + \frac{C_s}{C_I \cdot A}}$

Equation (4.5) shows that finite amplifier gain causes two deleterious effects in the integrator transfer function. First, the forward gain coefficient is reduced by the factor β . This results in the same sort of interstage gain mismatch as described in the previous section. Furthermore, finite amplifier gain shifts the pole of $H(z)$ inside the unit circle, reducing the Q of the integrator. The shift in pole locations results in increased noise leakage at low frequencies relative to the sample rate. Noise-leakage is dominated by non-idealities in the first stage of a cascade $\Sigma\Delta$ modulator. The effect of finite DC gain in the first stage of a 2-1-1 cascade can be described by the equation below. The second

term in (4.6) shows that noise leakage from the first stage will occur for values of $\epsilon > 0$ or $\beta < 1$. These conditions occur for finite OTA gain, as described in (4.5).

$$Y(z) = z^{-4} \cdot X(z) + \left\{ z^{-2}(1 - z^{-2})(1 - \beta_1 \cdot \beta_2) + z^{-3}(1 - z^{-1})(\epsilon_1 + \epsilon_2) + z^{-4}(\epsilon_1 \cdot \epsilon_2) \right\} \cdot E_1(z) + \frac{(1 - z^{-1})^4}{g_{1d} \cdot g_{2d}} \cdot E_3(z) \quad (4.6)$$

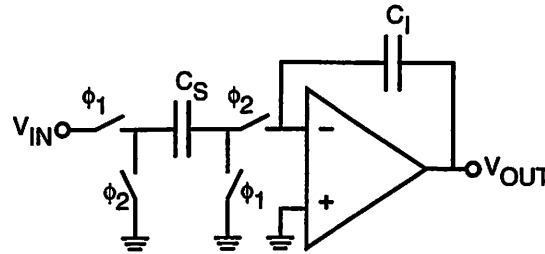


Figure 4.4 Switched-capacitor Integrator with Finite DC Gain OpAmp

4.7 Settling Constraints

The imperfect settling performance of operational amplifiers causes additional non-idealities in $\Sigma\Delta$ modulator performance. A model of a typical switched-capacitor voltage transient is shown in Figure 4.5. Three distinct characteristics of this transient can be observed: first, charge feedthrough through C_f causes an initial voltage deviation in the incorrect direction. Then, the output voltage may show some slew-rate limitations. Finally, assuming that the slew-rate limitations are overcome, the integrator settles linearly.

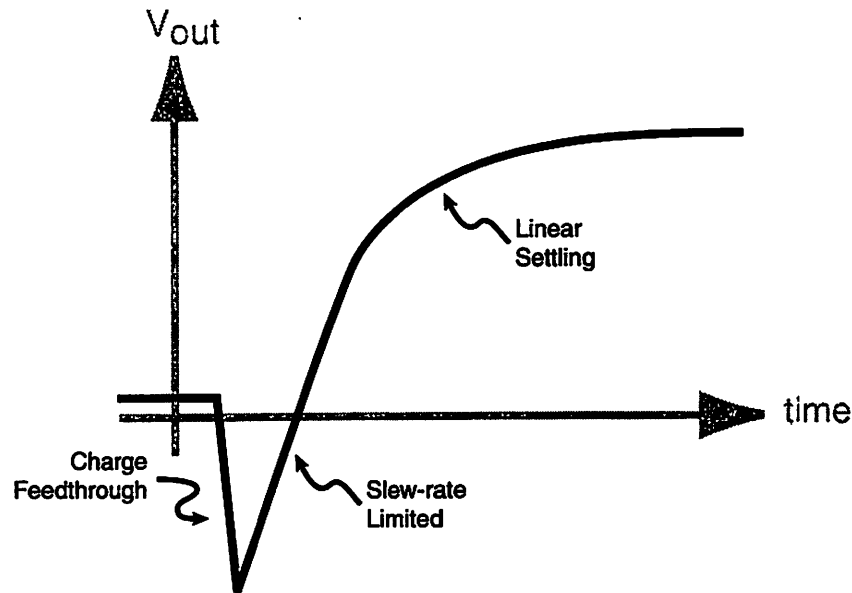


Figure 4.5 Model of typical switched-capacitor voltage transient

These three effects taken together results in a non-linear integrator transfer function. Therefore, it is not possible to use the linear, “white-noise” assumption to derive an analytic result of the modulator noise performance. Instead, a nonlinear input-output transfer function can be derived for use in simulation. If one assumes that the linear settling portion of the transient is determined by a single dominant pole, one can express the input-output relationship as in (4.7). These equations are an extension of those utilized by the MIDAS $\Sigma\Delta$ simulation tool [32].

$$v_o(v_i) = \begin{cases} -K \cdot v_i + (K+1) \cdot v_i \cdot (1 - e^{-n_r}) & |v_i \cdot (K+1)| \leq SRN/n_r \\ v_i - \text{sgn}(v_i) \cdot \frac{1}{n_r} \cdot SRN \cdot e^{\left(\frac{|v_i \cdot (K+1)| \cdot n_r}{SRN} - n_r - 1\right)}, & SRN/n_r < |v_i \cdot (K+1)| \leq SRN \cdot \left(\frac{1}{n_r} - 1\right) \\ -K \cdot v_i + \text{sgn}(v_i) \cdot SRN & SRN \cdot \left(\frac{1}{n_r} - 1\right) < |v_i \cdot (K+1)| \end{cases} \quad (4.7)$$

4.8 Simulation Environment

This section will begin with a description of the simulation environment developed for design and verification of the block-level performance of the $\Sigma\Delta$

modulator. Also, simulation results—in the form of modulator performance and circuit requirements—will be presented.

4.8.1 SIMULINK Simulation Environment

A block-level structural description of the $\Sigma\Delta$ modulator was built in the SIMULINK environment. Figure 4.6 shows a screen capture of the structural model of the $\Sigma\Delta$ modulator. The non-idealities described in the previous section were encapsulated in SIMULINK blocks and the block parameters were swept in order to determine modulator performance and circuit requirements. These results are presented below.

SIMULINK is a time-step simulation tool that offers a great deal of flexibility in creating user-defined systems. As a result, it was possible to create a SIMULINK model of the complete wireless downlink. The SIMULINK model of the $\Sigma\Delta$ modulator was integrated within this larger model for system-level verification. For more information about the SIMULINK model of the direct conversion receiver, refer to [48].

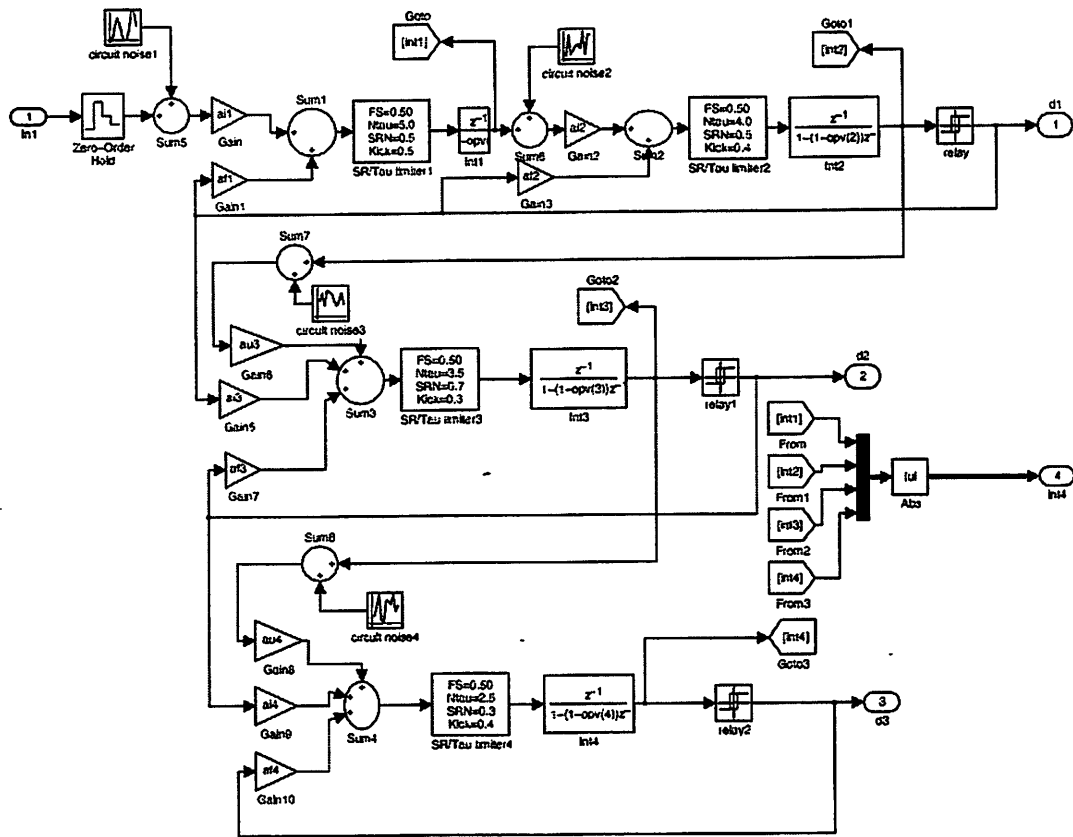


Figure 4.6 SIMULINK structural model of $\Sigma\Delta$ modulator

4.8.2 Simulation Results

The simulated performance and circuit requirements of the 2-1-1 cascade architecture will now be presented. The Nyquist rate of this system is 25 Ms/s and the oversampling ratio is 8; therefore the sampling rate is 200 Ms/s. Figure 4.7 shows the signal-to-noise-and-distortion-ratio (SNDR) with all the non-idealities outlined above included. The peak SNDR is 42.5 dB and the dynamic range is 46 dB.

By sweeping through a parameterized simulation of the $\Sigma\Delta$ modulator, individual circuit block requirements can be determined. Performance requirements for the first integrator are shown in Table 4.2.

As mentioned above, the SIMULINK environment allows for the integration of the $\Sigma\Delta$ modulator model into the entire wireless downlink model for verification purposes. The SNR required at the output of the digital despreading process is 15 dB is

order to provide a BER of 10^{-4} [2]. The entire downlink model was simulated, and Figure 4.8 demonstrates that the system level requirement of 15 dB post-correlation SNR is met with the $\Sigma\Delta$ modulator designed.

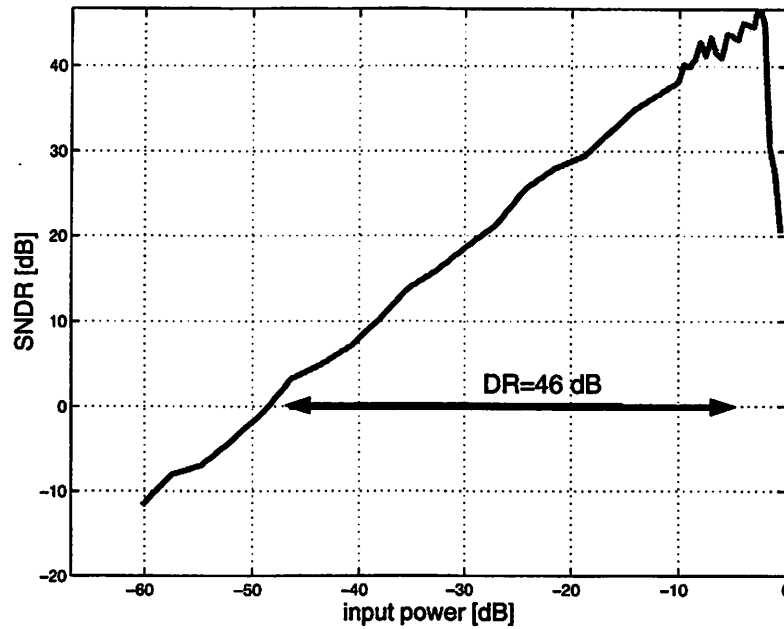


Figure 4.7 SIMULINK Dynamic Range Performance Curve

Specification	Value
DC gain	>100
Unit capacitor mismatch (σ_{ACC})	< 5%
Comparator offset	< 120 mV
Closed-loop settling frequency ($\omega_{L,T}$)	> 530 MHz
Phase margin	> 60 deg
Differential Slew Rate	> 670 V/ μ s

Table 4.2 Circuit performance requirements for first integrator

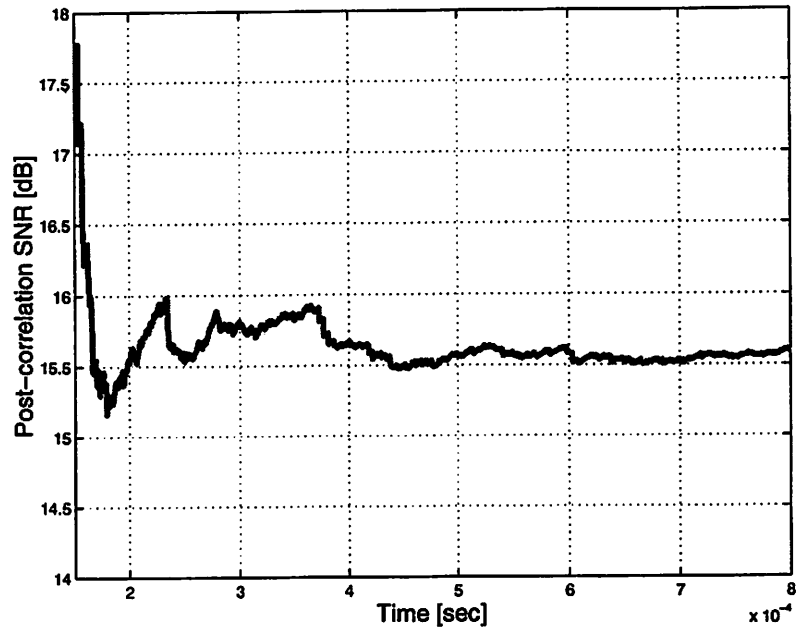


Figure 4.8 System-level simulated SNR

Switched-Capacitor Integrator Design

5.1 Introduction

The previous chapter examined potential architectures for high-speed $\Sigma\Delta$ analog-to-digital conversion. In that chapter, a 2-1-1 multi-stage, switched-capacitor $\Sigma\Delta$ modulator was introduced, and the required circuit performance metrics were determined. This chapter will focus on the necessary circuit design needed to implement the crucial circuit blocks of the $\Sigma\Delta$ modulator. These circuits include switched-capacitor integrators, operational transconductance amplifiers, bias circuitry, comparators, and other related circuitry. Analysis of these circuits for high-speed, low-power operation will be presented. An experimental 2-1-1 multi-stage $\Sigma\Delta$ modulator implemented in a 0.25 μm , 2.5V, single-poly, six-level metal, CMOS process will then be described.

5.2 Integrator Specifications and Design

The prototype $\Sigma\Delta$ modulator consists of four switched-capacitor integrators. The relevant requirements for the first of these integrators, as determined in Section 4.8, are shown in Table 4.2. Figure 5.1 shows the first integrator in the modulator. It is

implemented using the standard switched-capacitor network that ideally gives the integrator transfer function shown in (5.1):

$$\frac{V_{OUT}}{V_{IN}}(z) = \frac{C_S}{C_I} \cdot \frac{z^{-1}}{1 - z^{-1}} \quad (5.1)$$

The integrator is implemented using fully-differential circuits in order to minimize non-idealities such as PSRR, device matching, and noise coupling. Additionally, a two-phase bottom-plate sampling clocking technique is used to minimize signal-dependent charge injection [49]. The clock waveforms used are shown in figure 5.2.

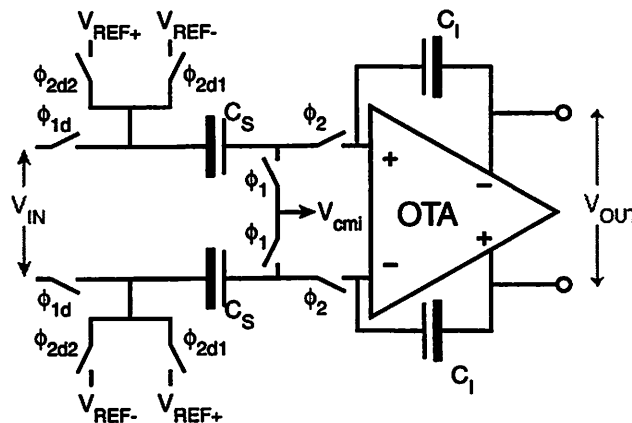


Figure 5.1 Fully-differential switched-capacitor integrator

The DAC feedback path is created by the switches connected to V_{REF+} and V_{REF-} . These reference voltages create 800 mV differential DAC reference levels, and their switch control signals (ϕ_{2d1} and ϕ_{2d2}) are cross-coupled in order to appropriately sample the differential DAC signal across C_S . As derived in the simulations described in Section 4.3, the $\Sigma\Delta$ modulator can accommodate 660 mV (-1.7 dBFS) input sinusoid signal before significant clipping occurs.

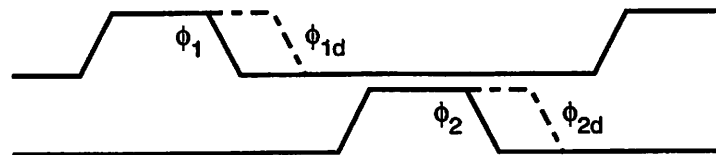


Figure 5.2 Two-phase non-overlap clock for bottomplate sampling

5.3 OTA Design

As shown in Table 4.2, the dominant circuit performance requirements relate to the transient performance of the switched-capacitor integrators. This is expected, as the oversampled approach of a $\Sigma\Delta$ modulator tends to intensify speed-related circuit requirements while easing other circuit performance metrics. Considering that the gain requirement is particularly modest, a circuit topology that provides the fastest possible settling response is preferred.

A single-stage, folded-cascode OTA is chosen as it meets all the required specifications with minimum complexity. A telescopic cascode OTA is not used, as that topology would reduce the signal swing too much due to the extra tail current device. Also, a folded cascode topology effectively decouples the input common-mode voltage from the output swing, allowing for much easier biasing and less concern about common-mode excursions.

NMOS input devices are chosen in order to maximize the settling speed of the amplifier. An NMOS device has roughly three times the transconductance of a PMOS device for a given gate overdrive due to the difference in electron and hole mobility. Therefore, for a given speed requirement, an OTA with NMOS input devices will consume far less power than one with PMOS inputs. While the stability of an NMOS-input folded cascode OTA is inferior to that of its PMOS counterpart, it will be shown in 5.3.3 that the PMOS cascode devices of such a topology does not significantly degrade the phase margin of the OTA. A schematic of the OTA used is shown in Figure 5.3.

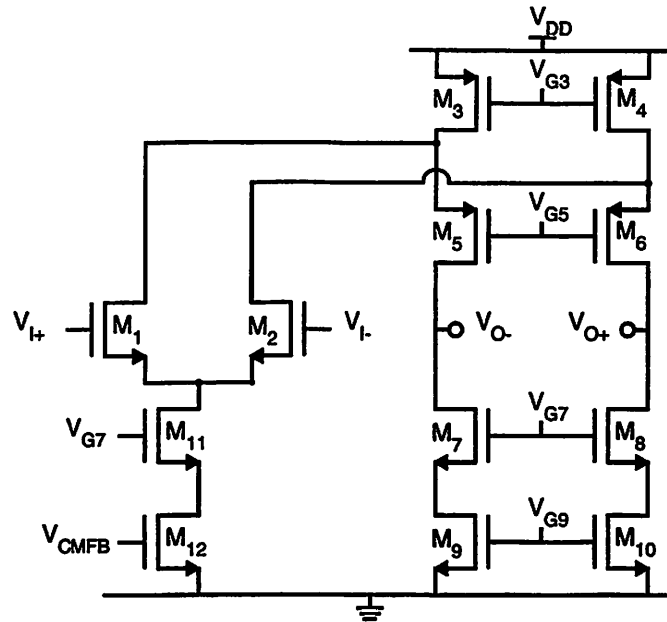


Figure 5.3 Fully-differential folded-cascode OTA

5.3.1 Thermal Noise

Thermal noise degrades $\Sigma\Delta$ performance in much the same manner as quantization noise. There are two primary sources of thermal noise in a switched-capacitor circuit. First, the CMOS switches have a finite resistance (R_{ON}), and therefore contribute thermal noise which is directly sampled onto the sampling capacitors. The thermal noise contribution of the switches is given by:

$$P_{N,SW} = 4 \frac{kT}{C_s} \quad (5.2)$$

The factor of 4 in (5.2) is due to the fact that a noise with variance $2kT/C_s$ (2x due to the differential implementation) is injected during phase 1 and then again during phase 2; since the noise samples in phase 1 and phase 2 are uncorrelated, their powers add.

The second source of thermal noise is the OTA itself. The input referred noise density of a common-source connected transistor is:

$$\frac{\overline{v_{n,in}^2}}{\Delta f} = 4kT \cdot \gamma \cdot \frac{1}{g_m} \quad (5.3)$$

where γ is the MOS noise factor. In long channel devices, γ is 2/3, but values of γ are significantly larger for short-channel devices [50]. For the folded-cascode OTA in figure 5.3, it can be shown that the input-referred noise power is:

$$\frac{P_{N,OTA}}{\Delta f} = 2 \cdot \left\{ \overline{v^2_{n1,in}} + \left(\frac{g_{m3}}{g_{m1}} \right)^2 \overline{v^2_{n3,in}} + \left(\frac{G_{m5}}{g_{m1}} \right)^2 \overline{v^2_{n5,in}} + \left(\frac{G_{m7}}{g_{m1}} \right)^2 \overline{v^2_{n7,in}} + \left(\frac{g_{m9}}{g_{m1}} \right)^2 \overline{v^2_{n9,in}} \right\} \quad (5.4)$$

$$\text{where } G_m = \frac{g_m}{1 + g_m r_o}$$

Equation (5.4) can be understood by recognizing the fact that the input-referred voltage noise is a sum of all the output-referred current noises divided by transconductance of the input device. With this framework, it becomes clear that the noise contributions of the cascoded devices (M5 and M7) become negligible; as transistors M5 and M7 are degenerated by M3 and M9, respectively, the output-referred current noise from these devices become negligible. Therefore, (5.4) can be simplified to:

$$\frac{P_{N,OTA}}{\Delta f} \approx 2 \cdot \left\{ 4kT \cdot \gamma \cdot \frac{1}{g_{m1}} \left[1 + \left(\frac{g_{m3} + g_{m9}}{g_{m1}} \right) \right] \right\} \quad (5.5)$$

One can determine the total input noise of the integrator via a three-step process. First, the output noise density is calculated by multiplying (5.5) by square of its transfer function to the output⁵:

$$\frac{P_{N,OUT}}{\Delta f} = \frac{P_{N,OTA}}{\Delta f} \cdot \left| \frac{\frac{1}{f_{FB}}}{1 + \frac{s \cdot C_{L,TOT}}{g_{m1} \cdot f_{FB}}} \right|^2 \quad (5.6)$$

Then, the total integrated output noise is calculated by integrating (5.6) over all frequencies:

⁵ For simplified mathematics, the transfer function is assumed to be dominated by the low-frequency pole. The presence of a second, non-dominant pole may cause peaking in the transfer function, but this effect should be negligible if the OTA is designed with sufficient phase margin.

$$\begin{aligned}
P_{N,OUT} &= \int_0^{\infty} \frac{P_{N,OUT}}{\Delta f} df = \int_0^{\infty} 2 \cdot \left\{ 4kT \cdot \gamma \cdot \frac{1}{g_{m1}} \left[1 + \left(\frac{g_{m3} + g_{m9}}{g_{m1}} \right) \right] \right\} \cdot \left| \frac{\frac{1}{f_{FB}}}{1 + \frac{s \cdot C_{L,TOT}}{g_{m1} \cdot f_{FB}}} \right|^2 df \\
&= 2 \cdot \frac{kT}{C_{L,TOT}} \cdot \gamma \cdot \frac{1 + \frac{g_{m3} + g_{m9}}{g_{m1}}}{f_{FB}}
\end{aligned} \tag{5.7}$$

Finally, the total input-referred noise is found by relating (5.7) back to the input via the feedback factor, f_{FB} :

$$P_{N,IN} = P_{N,OUT} \cdot f_{FB}^2 = 2 \cdot \frac{kT}{C_{L,TOT}} \cdot \gamma \cdot \left(1 + \frac{g_{m3} + g_{m9}}{g_{m1}} \right) \cdot f_{FB} \tag{5.8}$$

Equation (5.8) shows that the total input-referred thermal noise can be made smaller by two mechanisms: either $C_{L,TOT}$ may be increased (by scaling up C_S and C_I) or the ratio in parentheses may be decreased by decreasing g_{m3} and g_{m9} . As the bias currents of M1, M3, and M9 are all related, the latter technique is equivalent to increasing V_{dsat3} and V_{dsat9} . This must be balanced against signal swing constraints, as these V_{dsat} 's directly subtract from available output voltage swing. Therefore, capacitor sizes and the bias conditions of M3 and M9 can be determined.

5.3.2 Flicker Noise

MOS flicker noise is caused the random interaction of the minority carriers with the interface trap states at the surface of the MOS channel. Flicker noise has a power spectral density that is inversely proportional to frequency. A simple model for the input-referred flicker noise of an MOS transistor is:

$$\frac{\overline{v_{f,in}^2}}{\Delta f} = \frac{K_f}{W \cdot L \cdot C_{ox}} \cdot \frac{1}{f} \tag{5.9}$$

Due to the very wide bandwidth of the $\Sigma\Delta$ modulator being designed, total integrated flicker noise is negligible when compared to the total integrated thermal noise.

5.3.3 Linear Settling

As described in section 4.7, the OTA must have sufficient bandwidth in order to settle adequately during half of a single clock period. The linear settling of the OTA may be derived by calculating its closed-loop frequency response. A small-signal model of the OTA is shown in Figure 5.4. The output resistances (r_o) of the transistors is assumed to be infinite for the purposes of this transient analysis. The capacitors in the figure are defined as follows:

$$\begin{aligned} C_1 &= C_{GS1} + C_{P,SW} \\ C_3 &= C_{GS5} + C_{D1} + C_{D3} \\ C_L &= C_{P,SW,N} + C_{BP,I} + C_{DS} + C_{D7} \end{aligned} \quad (5.10)$$

The capacitors $C_{P,SW}$ and $C_{P,SW,N}$ refer to the parasitic switch capacitors of this integrator and the next integrator, respectively. $C_{BP,I}$ refers to the bottom-plate parasitic capacitance of the integrating capacitor.

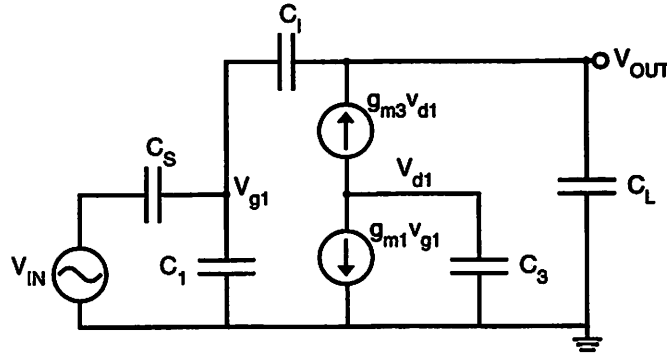


Figure 5.4 Small-signal model of switched-cap integrator with folded-cascode OTA

The closed-loop OTA transfer function can be calculated as:

$$H(s) = -\frac{C_S}{C_I} \cdot \frac{f_{FB} \cdot (g_{m1}g_{m3} - C_I g_{m3}s - C_3 C_I s^2)}{f_{FB} g_{m1}g_{m3} + C_{L,TOT} g_{m3}s + C_3 C_{L,TOT} s^2} \quad (5.11)$$

where

$$\begin{aligned} f_{FB} &= \frac{C_I}{C_I + C_S + C_1} \\ C_{L,TOT} &= C_L + \frac{C_I \cdot (C_S + C_1)}{C_I + C_S + C_1} \end{aligned} \quad (5.12)$$

While (5.11) is difficult to understand in its full form, relevant settling parameters can be extracted. In particular, assuming that the OTA has sufficient closed-loop phase margin⁶, the dominant pole location can be calculated, as in (5.13). From this equation, one can obtain a rough estimate for a minimum bound on the required transconductance for the input pair. It is important to note that a direct calculation for g_{m1} cannot be derived from (5.13) without further elaboration. This is due to the fact that $C_{L,TOT}$ and f_{FB} are also indirectly controlled by the bias conditions of M1, which has not yet been determined.

$$\omega_{u,T} \approx \frac{g_{m1} \cdot f_{FB}}{C_{L,TOT}} \quad (5.13)$$

Inserting full expressions for $C_{L,TOT}$ and f_{FB} into (5.13), $\omega_{u,T}$ is shown in (5.14).

$$\omega_{u,T} = \frac{g_{m1}}{C_S} \parallel \frac{g_{m1}}{C_L} \parallel \omega_{n1} \parallel \frac{g_{m1}}{A \cdot C_L} \parallel \frac{\omega_{n1} \cdot C_S}{A \cdot C_L}$$

where $a \parallel b \equiv \frac{1}{\frac{1}{a} + \frac{1}{b}}$

$$A \equiv \frac{C_S}{C_I}$$

$$\omega_{n1} \equiv \frac{g_{m1}}{C_1} \quad (5.14)$$

Equation (5.14) shows that $\omega_{u,T}$ is bounded by five terms. As $A \ll 1$ for discrete-time integrators, the latter two terms can be neglected. Therefore, (5.14) can be approximated as:

$$\omega_{u,T} \approx \frac{g_{m1}}{C_S + C_L + C_1} \quad (5.15)$$

C_S and C_L are determined by thermal noise considerations and the parasitics of the process, respectively. Therefore for a given settling requirement, an appropriate g_{m1} and C_1 can be determined. As C_1 is dominated by C_{GS1} , the device size and bias condition of transistor M1 can then be fully specified.

The PMOS cascode device causes a non-dominant pole to be present in the closed-loop OTA transfer function. Manipulating (5.11), one can approximate the non-dominant pole location:

⁶ This condition is satisfied if the non-dominant pole from the cascoded M3 transistor is sufficiently higher than the unity-gain frequency. This condition will be assumed here and verified in later paragraphs.

$$\omega_{nd} \approx \frac{g_{m3}}{C_3} \quad (5.16)$$

Therefore, sufficient phase margin can be ensured provided that ω_{nd} is roughly 2.5-3x greater than $\omega_{u,T}$. As shown in (5.10), the capacitor C_3 is dominated by the gate capacitance of M3; therefore ω_{nd} is slightly less than the natural ω_T of the device. Although M3 is a PMOS transistor, sizing the device with a short length and biasing it with a “healthy” V_{dsat} can provide a PMOS ω_T high enough so as not to overly degrade phase margin. These bias conditions force the $g_m r_o$ product of M3 to be relatively low. As will be discussed in 5.3.5, this can be tolerated due to the low DC gain requirement for the OTA.

The feedforward path in the closed-loop OTA through C_I creates a right half-plane zero at approximately:

$$\omega_z \approx \frac{g_{m1}}{C_I} \quad (5.17)$$

The effect of this zero is to create a “glitch” in the incorrect direction at the beginning of the settling transient, hence degrading settling performance. This effect is most prominent in integrators, where typically $C_S/C_I \ll 1$. For high-level simulation purposes, this effect is fully modeled by the K parameter in (4.7).

5.3.4 Slew Rate

As the folded-cascode amplifier is a Class A OTA, it will exhibit slew-rate limiting when large input steps are applied to the amplifier. Assuming a large positive input step is applied to the OTA in Figure 5.1, the node V_{O+} will slew in a positive direction at the rate:

$$|SR_{V+}| = \frac{I_3 - I_9}{C_{L,TOT}} \quad (5.18)$$

and the node V_{O-} will slew in a negative direction at the rate:

$$|SR_{V-}| = \frac{I_9}{C_{L,TOT}} \quad (5.19)$$

Hence, the differential slew rate is

$$|SR_{diff}| = \frac{I_3}{C_{L,TOT}} \quad (5.20)$$

and is therefore independent of the partition of I_3 between I_1 and I_9 . However, in order to minimize common-mode excursions during slew-rate limiting, it is desirable to equalize (5.19) and (5.20). Therefore, both I_1 and I_9 are set to $I_3/2$. As MOS devices tend to have a relatively low g_m/I ratio, the slew rate constraint is slightly less critical than the settling constraint outlined in the previous section.

5.3.5 DC Gain

Small-signal analysis shows that the DC gain of the OTA in (5.21) is:

$$A_{DC} = g_{m1} \cdot \{(g_{m5}r_{o5} \cdot (r_{o1} \parallel r_{o3}))\}(g_{m7}r_{o7}r_{o9}) \quad (5.21)$$

The gain is on the order of $(g_m r_o)^2$, which can easily provide the gain required by the block-level specifications. At moderate to long device lengths, transistor output resistance, r_o , is roughly proportional to the channel length. However, process limitations greatly reduce r_o for minimum length transistors [51]. In order to compensate for this effect, devices M5 and M1 are sized slightly longer than minimum length. Additionally, as M9 does not capacitively load the signal path, it is made longer to maximize r_{o9} in the DC gain equation.

5.4 Common-Mode Feedback

A schematic of the common-mode feedback circuitry is shown in figure 5.5. The CMFB circuitry used is dynamic in order to reduce power dissipation. The capacitors C_{sns} sense the output common-mode voltage and control the tail current of the input pair appropriately. The capacitors C_{dc} apply the correct DC voltage to C_{sns} .

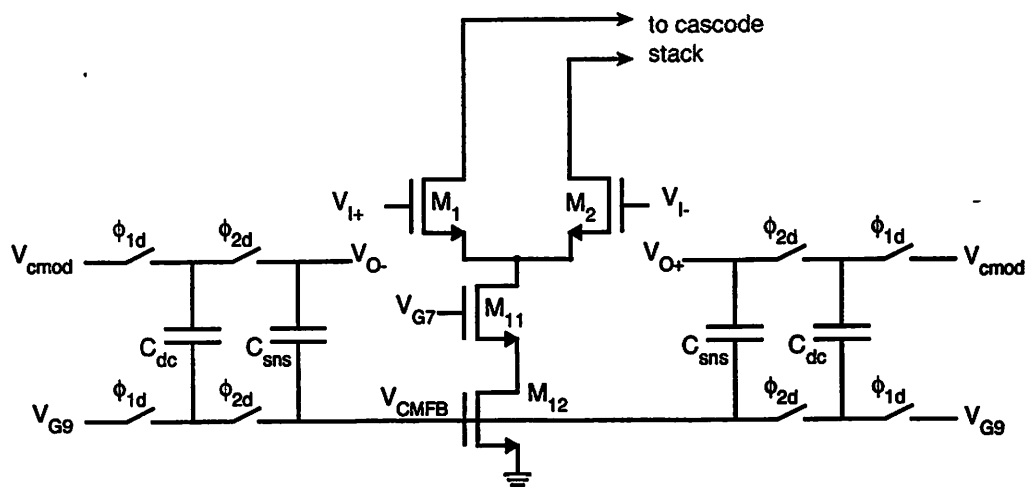


Figure 5.5 Dynamic common-mode feedback circuitry

5.5 Bias

Figure 5.6 shows the circuits used to bias the core analog $\Sigma\Delta$ circuitry. High-swing cascode biasing was implemented using stacked triode devices [52]. The $20\ \mu\text{A}$ bias currents shown in the figure are supplied by a master bias circuit, which is in turn supplied by a single off-chip bias current.

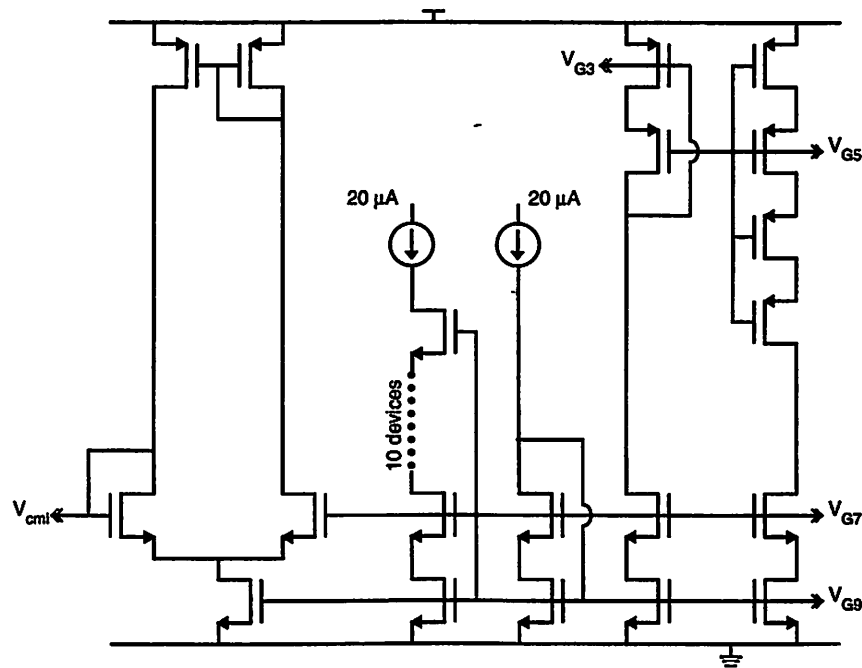


Figure 5.6 Bias circuitry for folded cascode OTA

5.6 Comparator

The single-bit comparator used is shown in figure 5.7 [35].). Due to the relaxed offset and hysteresis specifications, a low-power dynamic comparator is used. The comparator of figure 5.7 is followed by an active low R-S latch, as shown in figure 5.8. During phase 2, the enable signal is low, and the outputs of the comparator are reset to VDD; this causes the R-S latch to hold its previous state. When the enable signal is brought high, the differential input signal varies the resistance of the triode-region devices, M1 and M2. This differential resistance causes the cross-coupled inverters, consisting of devices M5, M6, M7, and M8, to toggle in the appropriate direction.

The fast, regenerative nature of the dynamic comparator, coupled with the memory inherent to the R-S latch, reduces the possibility of metastability to very low levels. Instead, if the comparator is unable to resolve the input signal in the allotted time, the R-S latch hold its previous state. Hence, metastability is converted to hysteresis, which is far less problematic for correct operation.

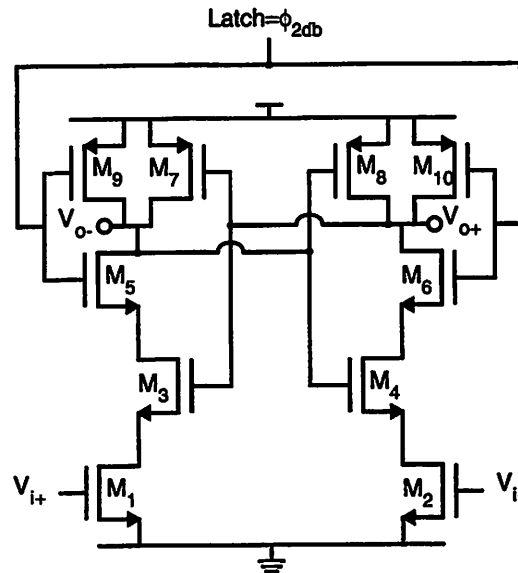


Figure 5.7 Dynamic comparator

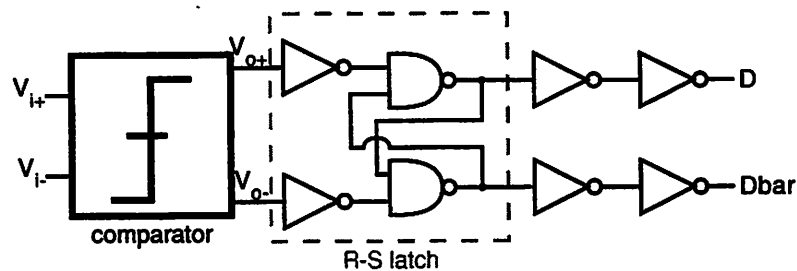


Figure 5.8 Comparator with R-S latch

5.7 Clock Generation

Figure 5.9 shows the clock waveforms required for switched-capacitor bottom-plate sampling techniques. The addition of phases ϕ_{1d} and ϕ_{2d} reduce signal-dependent charge injection.

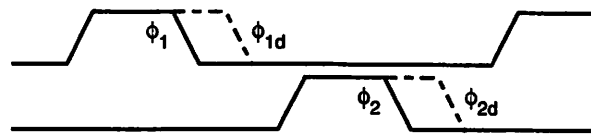


Figure 5.9 Two-phase non-overlap clock waveforms

The circuit in figure 5.10 generates these waveforms [53]. The dynamic inverters of M1-M3 and M4-M6 align the rising edges of the delayed and non-delayed clocks. The delay between the falling edges of the delayed and non-delayed clocks is controlled by the propagation delay of the inverter chain.

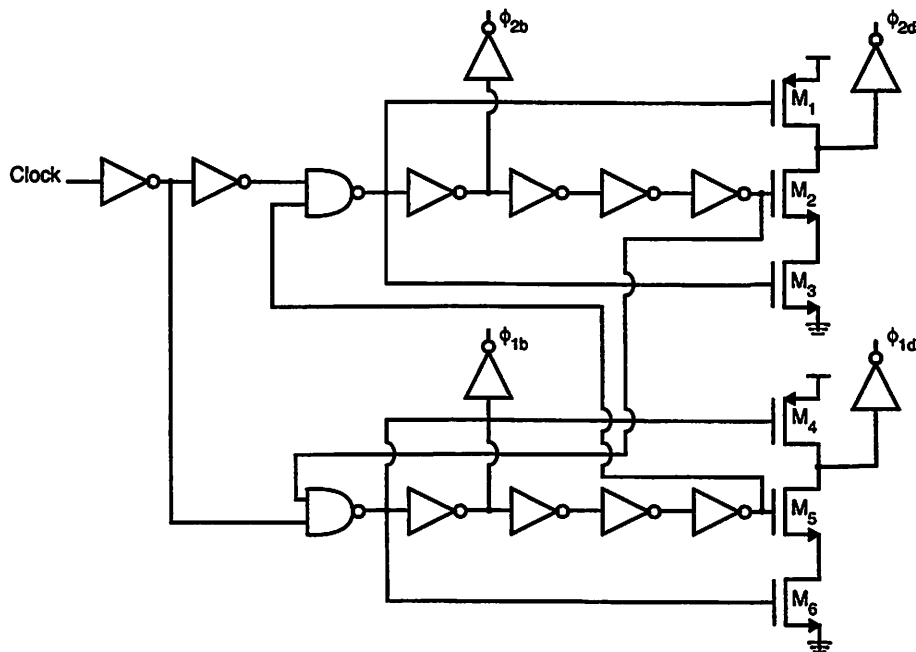


Figure 5.10 Two-phase non-overlap clock generator

5.7.1 Duty Cycle Adjust

As the $\Sigma\Delta$ modulator is to be integrated with an entire RF front-end [54], it is desirable to utilize as few external signals as necessary; a 200 MHz off-chip clock waveform is likely to introduce a substantial amount of switching noise into the substrate, thus degrading signal integrity. Instead, it is preferable to use a divided down version of the on-chip LO output. The on-chip frequency synthesizer generates a 2 GHz signal, and

the divider chain produces a 200 MHz signal [55]. The 200 MHz signal has a 60% duty cycle, and it is desirable to equalize this clock waveform to a 50% duty cycle. The circuit in figure 5.11 adjusts the duty cycle as necessary. Its operation is similar to that of the clock generation circuitry described above.

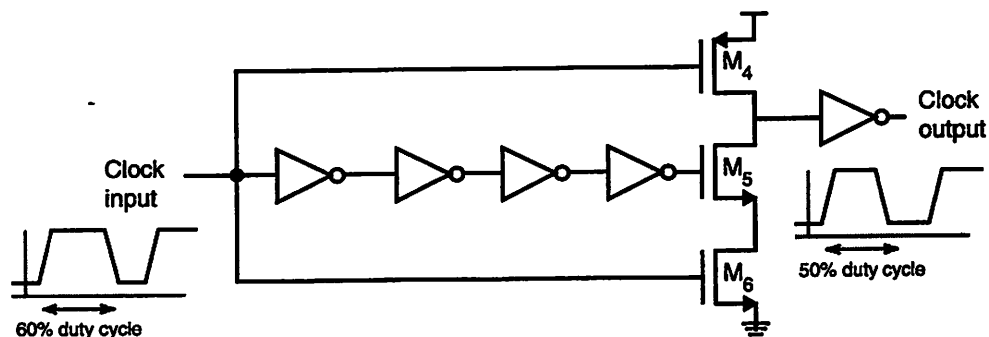


Figure 5.11 Clock duty-cycle adjust circuitry

5.8 Output Buffer

The output buffers, shown in figure 5.12, are used to minimize digital noise coupling into the substrate or through the bond wires. Transistors M1, M2, and M3 form a current-mode logic pair that drives an off-chip resistive load for I/V conversion. This circuit maintains a constant current regardless of output bit, thus keeping digital switching noise low. Additionally, the output signal comes off-chip in a differential manner, thus providing first-order cancellation of $L(di/dt)$ noise produced in the bond wires.

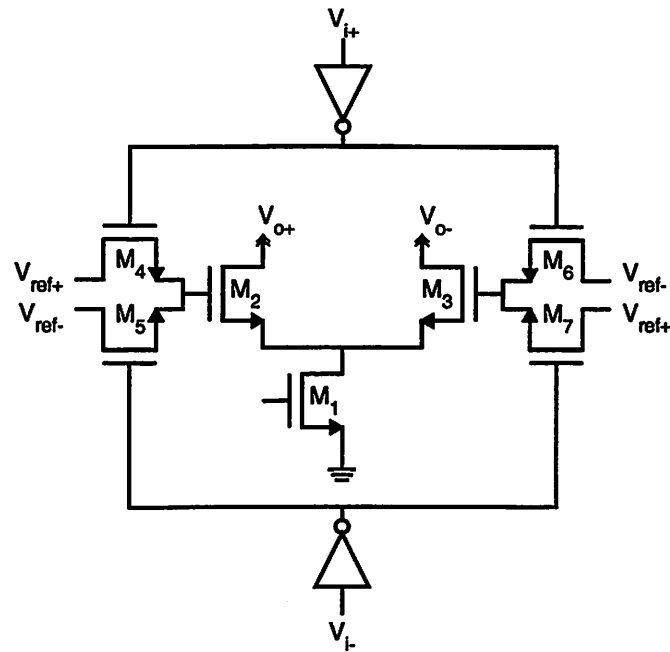


Figure 5.12 Output Buffer

5.9 Summary

This chapter presented the circuit design challenges in the design of the circuit blocks for a switched-capacitor $\Sigma\Delta$ modulator. These circuits include switched-capacitor integrators, operational transconductance amplifiers, bias circuitry, comparators, and other related circuitry. Low-power analysis and design techniques were presented. These circuits were used to implement a prototype 2-1-1 multi-stage $\Sigma\Delta$ modulator.

6

Results

6.1 Introduction

This chapter will discuss the simulated and measured results for a prototype 2-1-1 cascade $\Sigma\Delta$ modulator implemented in a 0.25 μm , single-poly, 2.5V CMOS process. Results will be presented and differences between simulated and measured results will be discussed.

6.2 Simulated Results

This section will discuss simulation results from the fully extracted layout of the $\Sigma\Delta$ modulator. Discussion of the design and optimization of the circuit blocks can be found in Chapter 5.

6.2.1 Capacitor and Bias Values

Table 6.1 shows the extracted capacitor sizes and the simulated bias conditions for the folded-cascode OTAs used in this design. As the design was parasitic limited, capacitor scaling was not heavily employed. The bias current in Table 6.1 are determined

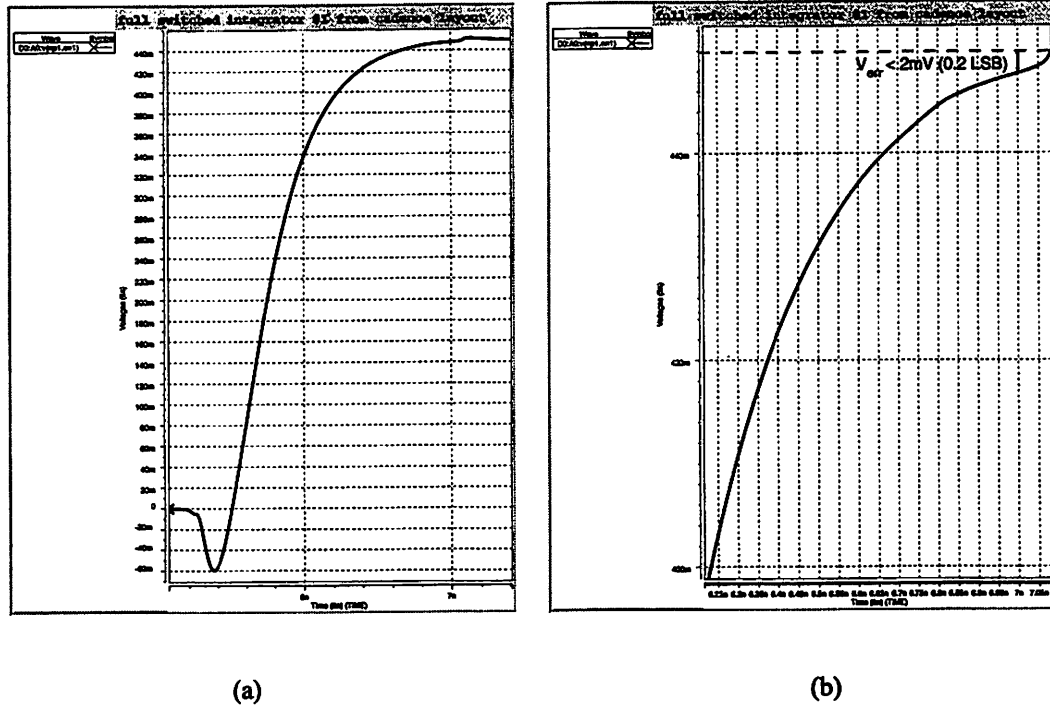


Figure 6.2 (a) Simulated settling transient and (b) zoomed-in version

6.2.3 Dynamic Range

Figure 6.3 shows dynamic range measurements as determined from a transient SPICE simulation of the fully extracted layout. The simulated dynamic range is approximately 46.4 dB and the peak SNDR is approximately 45 dB. Simulated power dissipation is 26 mW.

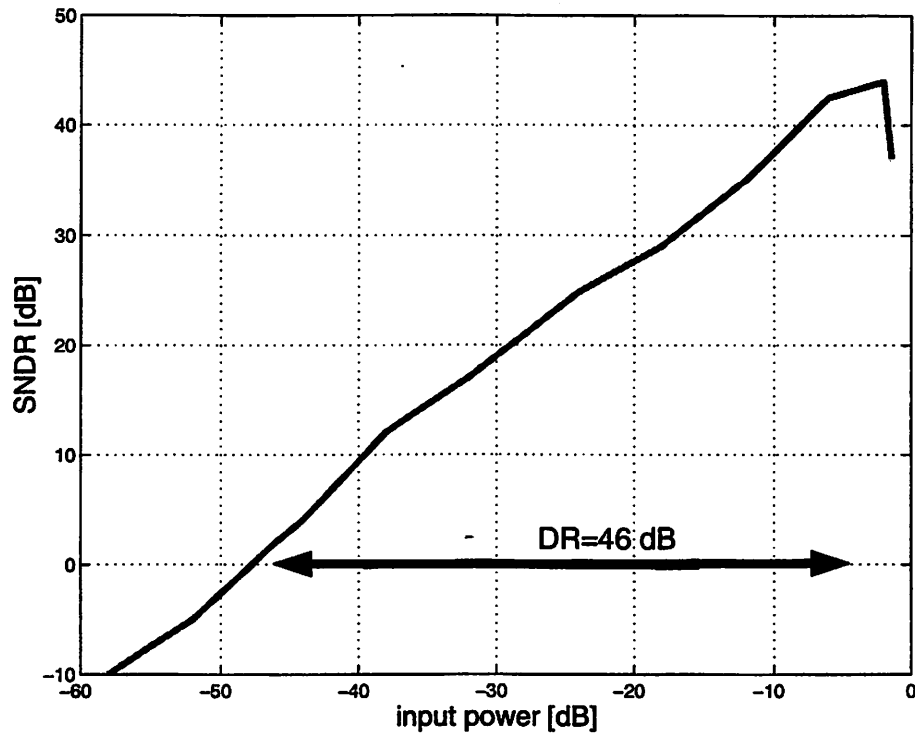
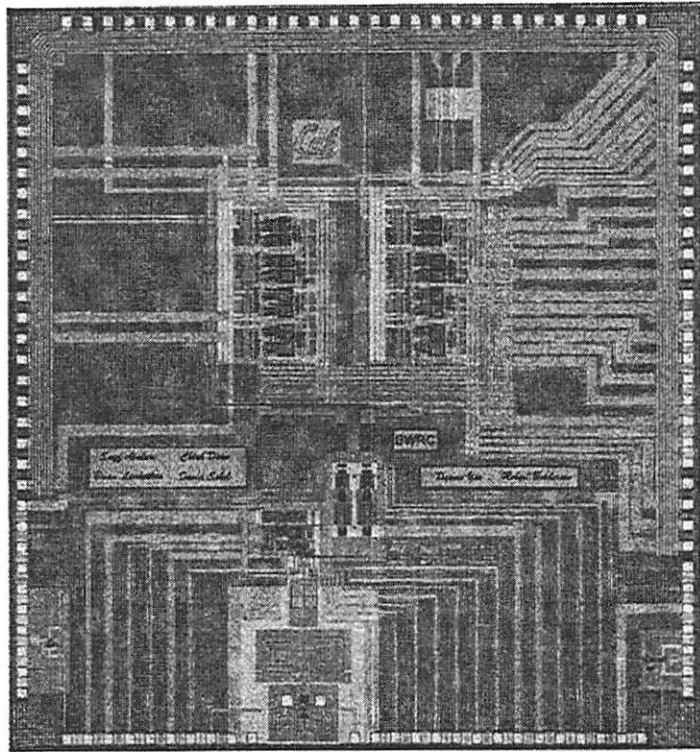


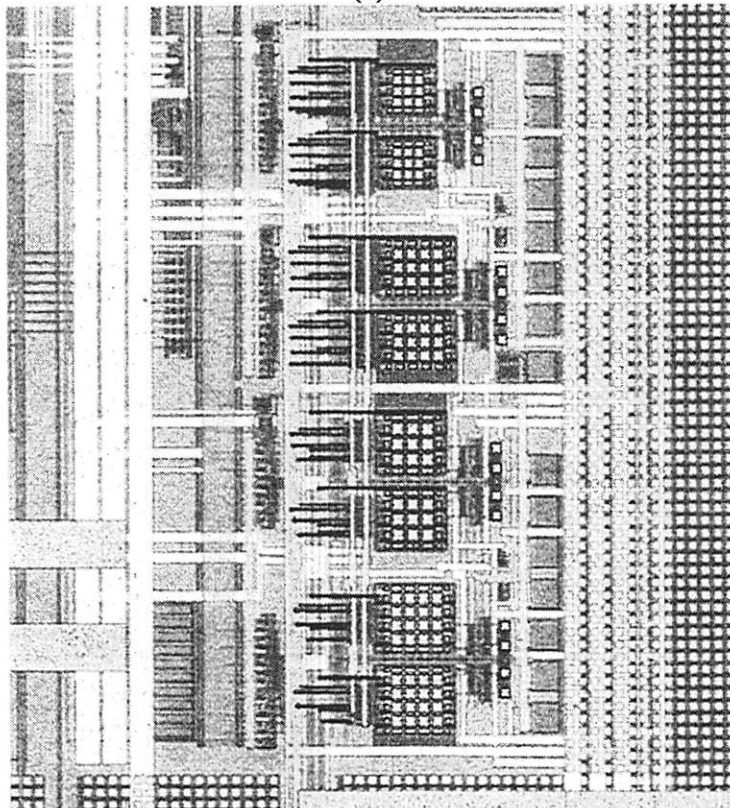
Figure 6.3 Dynamic range as simulated by SPICE

6.3 Measured Results

A die photo of the entire direct-conversion receiver is shown in Figure 6.4(a). Figure 6.4(b) shows the die photo zoomed in on one of the $\Sigma\Delta$ modulators. Active area for each modulator is approximately 1.2 mm x 0.8 mm. The chip is bonded directly to a custom printed circuit board using chip-on-board technology to minimize the effect of bond-wire inductance.



(a)



(b)

Figure 6.4 (a) Die photo of direct-conversion receiver. (b) Close up of $\Sigma\Delta$ modulator.

Figure 6.5 shows the measured SNDR as a function of input power for a 3.125 MHz sinusoidal input at 25 Ms/s Nyquist rate and 8 X oversampling ratio. The modulator achieves roughly 42 dB dynamic range and 40 dB peak SNDR, while dissipating 29 mW from a 2.5 V supply. When compared to simulated results, it can be noticed that these measurements are about 4 dB lower than expected. The increase in power dissipation is due to increased capacitive parasitics on the digital clock lines.

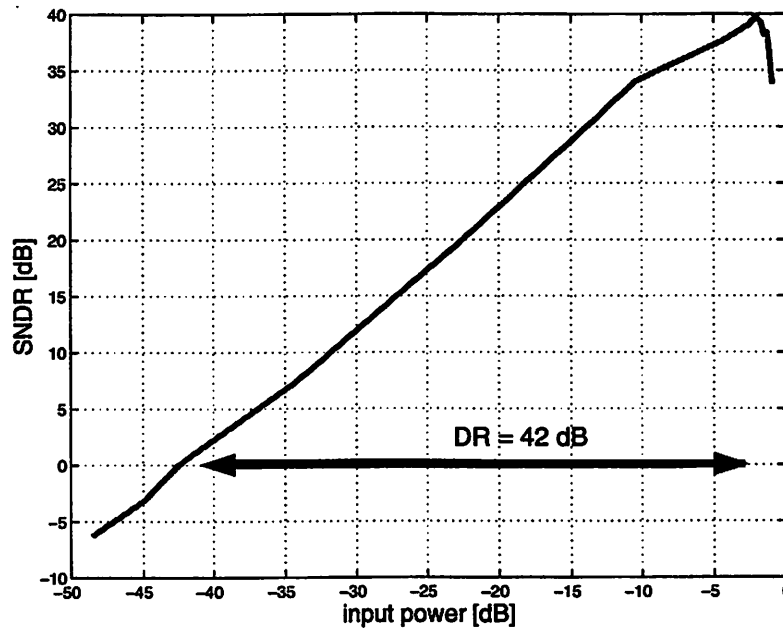


Figure 6.5 Dynamic range measurements at $f_{NYQ} = 25$ Ms/s

Figure 6.6(a) shows the undecimated spectrum for a -33 dBFS signal at 3.125 MHz; the fourth-order noise shaping is obvious. Figure 6.6(b) shows a zoomed-in version of the undecimated spectrum. It can be noticed that the fourth-order shaping does not exist all the way down to DC; second-order shaping dominates from DC to about 1.125 MHz ($0.045 \times f_{NYQ}$), resulting in the 4 dB degradation noted above.

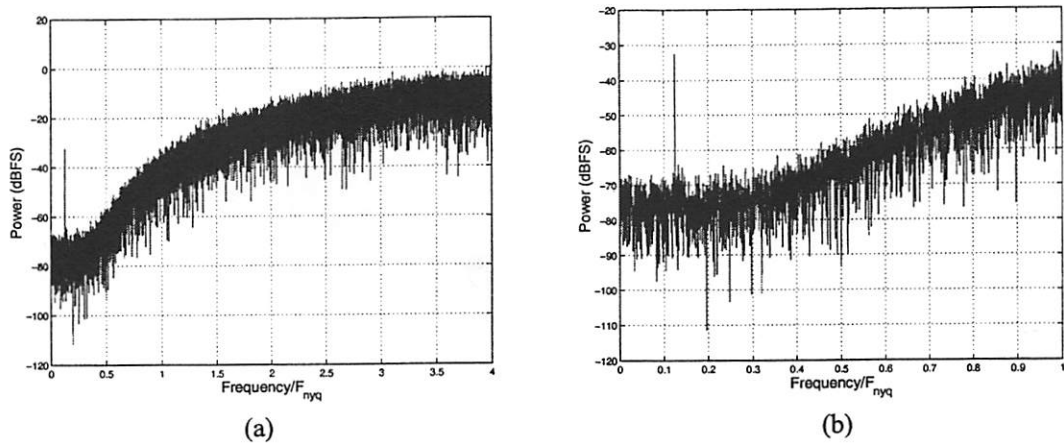


Figure 6.6 (a) Undecimated output spectrum of $\Sigma\Delta$ modulator, $f_{NYQ} = 25$ Ms/s. (b) Zoomed in near DC.

Dynamic range measurements of the modulator operating at an 8 X oversampling ratio were made for several different Nyquist rates. These measurements are shown in Figure 6.7. It can be observed that a Nyquist rate of 6.25 MHz the performance loss is only about 2 dB. Figure 6.8 shows the undecimated spectrum for this Nyquist rate, and it can be seen that fourth-order noise-shape exists all the way down to 125 kHz ($0.02 \times f_{NYQ}$). This measurement demonstrates that the performance is not limited by finite DC gain, as degradation from finite DC gain is independent of sampling frequency.

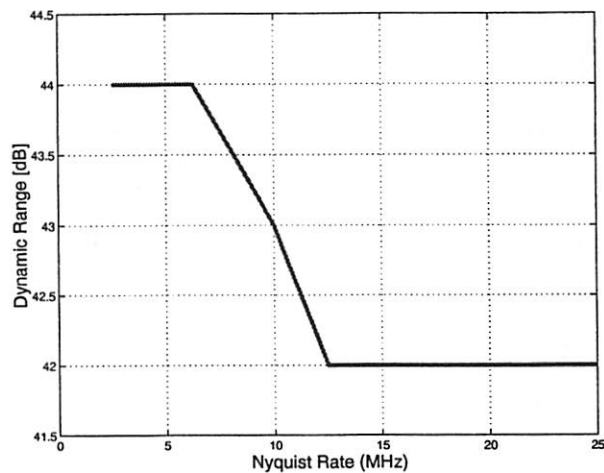


Figure 6.7 Dynamic Range as a function of f_{NYQ}

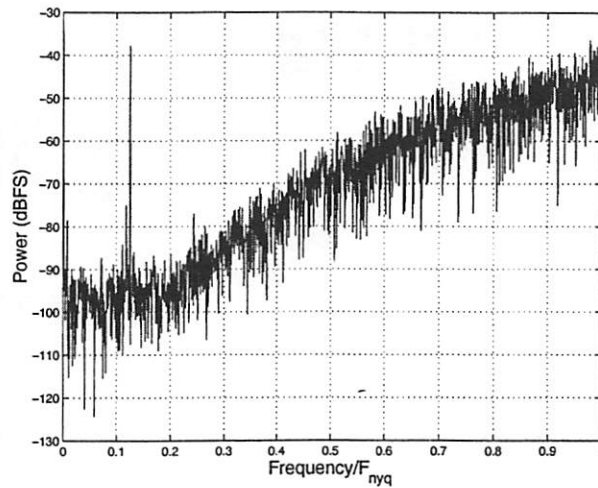


Figure 6.8 Undecimated output spectrum of $\Sigma\Delta$ modulator, $f_{NYQ} = 6.25$ Ms/s (zoomed in)

It also is unlikely that limited integrator settling is the cause of the performance degradation. Figure 6.7 shows that there is no performance degradation incurred when the Nyquist frequency is raised from 12.5 MHz to 25 MHz. (At 8 X OSR, the sampling frequency is raised from 100 MHz to 200 MHz.) In this case, the settling time is reduced from roughly 3.7ns to roughly 1.2ns, hence reducing settling time by a factor of three. If imperfect integrator settling were the performance limiter, such a reduction in settling time should result in a drastic reduction in dynamic range performance.

It is unclear what causes the performance degradation as the Nyquist frequency is raised from 50 MHz to 100 MHz. One possible explanation is as follows: the signal generator driving the input is unable to drive the input sampling capacitor sufficiently quickly. As shown in figure 6.9(a), when the sampling capacitor is switched to the input source at the beginning of phase 1, there exists a residual charge on the capacitor equal to $V_{DAC} \cdot C_S$. If the signal generator had infinite bandwidth, it would immediately discharge this residue and charge the sampling capacitor to the appropriate voltage.

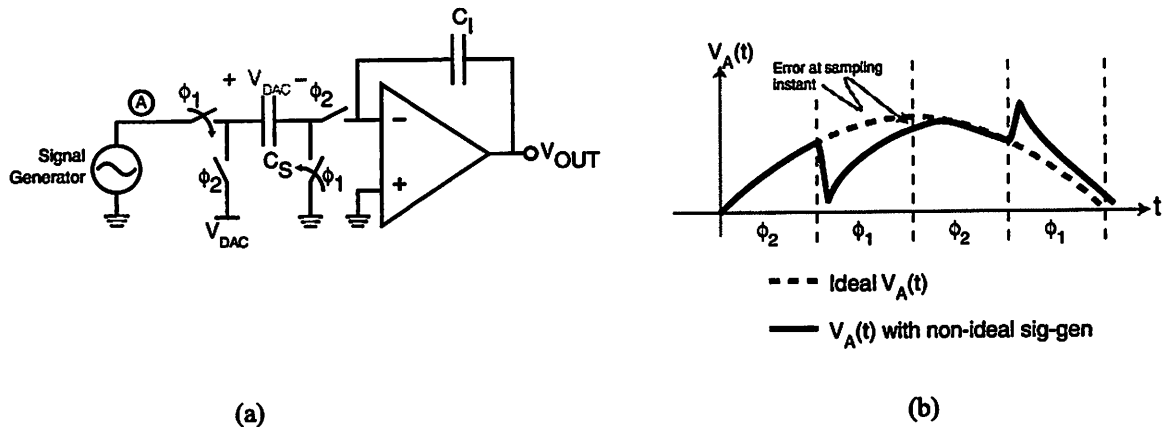


Figure 6.9 (a) Charge residue (b) Resulting corruption of input signal

Measurements made while the device was under test showed that the signal generator was not able to fully discharge this residue charge. Therefore, as shown in Figure 6.9(b), the input signal is somewhat corrupted by the DAC feedback signal. Viewed another way, the effective feedback coefficient, a_{f1} , from Figure 4.2, is modified from its nominal value due to the finite driving speed of the signal generator. As discussed in Section 4.5, changes in the modulator coefficients result in leakage of second-order shaped noise which is exactly what is observed in the modulator output spectrum of Figure 6.4. As the Nyquist rate is reduced below 6.25 MHz (Nyquist rate below 50 MHz), the signal generator is fast enough to discharge the residue charge to negligible levels.

6.4 Summary

This chapter described the test results of a prototype 2-1-1 cascade $\Sigma\Delta$ modulator implemented in a 0.25 μm CMOS process. The modulator exhibited 42 dB dynamic range and a peak SNDR of 40 dB, with a Nyquist rate of 25 Ms/s. The modulator operated at an 8 X oversampling ratio and dissipated 29 mW from a 2.5 V supply

Conclusions

7.1 Introduction

This chapter summarizes the primary research contributions and results, and provides some suggestions for future areas of research. A prototype 2-1-1 cascade $\Sigma\Delta$ modulator was designed for an indoor wideband CDMA wireless link. System-level design of the modulator was presented in Chapter 4, and the design of key circuit blocks was discussed in Chapter 5. Chapter 6 presented measured results.

7.2 Summary of Research Results

The research explored design issues of a very high-speed switched-capacitor $\Sigma\Delta$ modulator. Emphasis was placed on low-power design techniques that are amenable to highly integrated analog receivers. A secondary goal was to further understand the area of system and circuit co-design, so that the interaction between the analog circuits and back-end algorithms could be understood and exploited. Key results of this project are summarized below:

- Designed a switched-capacitor, CMOS sigma-delta modulator and demonstrated that this circuit could meet the specifications of a wideband CDMA indoor wireless link at a reasonable power dissipation. An experimental prototype achieved a dynamic range of 42 dB at a Nyquist rate of 25 Ms/s and dissipated 26 mW.
- Examined and developed several areas of circuit and system co-design. Implemented a $\Sigma\Delta$ -assisted timing recovery scheme where the intrinsic oversampling of the modulator is used to greatly ease timing recovery with minimal additional complexity. Identified a code-based noise-shaping scheme where the quantization noise is shaped relative to the CDMA spreading code rather than relative to frequency.
- Designed a high-speed, low-power operational transconductance amplifier suitable for 2.5 V CMOS processes.
- Developed a methodology to identify key performance constraints of the switched-capacitor integrators and minimize power consumption in the integrators around those constraints.

7.3 Future Work

This project aims to prove that a very high-speed $\Sigma\Delta$ modulator can meet the specifications of a wideband CDMA wireless downlink with moderate power dissipation, and that this modulator can be integrated with the entire analog front-end for a mobile receiver.

Technology scaling will continue to enable faster ADCs, but new circuit techniques will be necessary if very high-speed, high dynamic range $\Sigma\Delta$ modulators are desired. Continuous-time $\Sigma\Delta$ (CT $\Sigma\Delta$) modulators have demonstrated the potential to operate at significantly faster sampling rates than discrete-time, switched-capacitor implementations. Still, limited understanding of the design methodologies for CT $\Sigma\Delta$ modulators have curbed the design of high-order, multi-bit CT $\Sigma\Delta$'s. Further research in this area has the potential to allow high dynamic range CMOS $\Sigma\Delta$ modulators with Nyquist rates in the several to tens of MHz range.

As discussed in Chapter 3, the “mostly digital” nature of $\Sigma\Delta$ modulators allow for unique circuit-level and system-level co-design. The flexibility of having a highly oversampled digital signal stream enables new application-specific techniques that reside on the border between the analog circuits and the digital backend. Examples of such techniques include $\Sigma\Delta$ -assisted timing recovery and code-based noise-shaping, both described in Chapter 3. In order for more of these design opportunities to be discovered, however, the circuit designer must have a thorough understanding of both the application framework and the algorithms employed. It is this author’s strong belief that understanding and incorporating the behavior of the digital backend into the design of the ADC will enable higher performance complete systems.

References

- [1] C. Teuscher, D. Yee, N. Zhang, R. Brodersen, "Design of a Wideband Spread Spectrum Radio Using Adaptive Multiuser Detection," *Proceedings of the 1998 IEEE International Symposium on Circuits and Systems*, pp.595-599, May 1998.
- [2] C. Teuscher, *Low Power Receiver Design for Portable RF Applications: Design and Implementation of an Adaptive Multiuser Detector for an Indoor, Wideband CDMA Application*, PhD. Dissertation, University of California at Berkeley, 1998.
- [3] Andrew Viterbi, *CDMA : Principles of Spread Spectrum Communications*, Addison-Wesley, Sydney, 1995.
- [4] S. Verdu, *Multiuser Detection*, Cambridge University Press, Cambridge, 1998.
- [5] K. Onodera, P. Gray, "A 75-mW 128-MHz DS-SS Baseband Demodulator for High-Speed Wireless Applications," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, pp.753-761, May 1998.
- [6] S. Sheng, et al. "A Low-Power CMOS Chipset for Spread Spectrum Communications," *Digest of Technical Papers, International Solid-State Circuits Conference*, pp.346-347, February 1996.
- [7] *Specification of the Bluetooth System*, version 1.0B, Bluetooth Special Interest Group, December 1999.
- [8] Dennis Yee, *Ph.D. Qualifying Exam*, August 1998.
- [9] H. Sato, et al. "A 1.9 GHz Single-Chip IF Transceiver for Digital Cordless Phones," *Digest of Technical Papers, International Solid-State Circuits Conference*, pp. 342-343, February 1996.
- [10] J. Rudell, et al. "A 1.9 GHz Wide-Band IF Double Conversion CMOS Integrated Receiver for Cordless Telephone Applications," *Digest of Technical Papers, International Solid-State Circuits Conference*, pp.304-305, February 1997.
- [11] Dennis Yee, personal communications
- [12] J. Rudell, et al. "Recent Developments in High Integration, Multi-Standard CMOS Transceivers for Personal communication Systems," *Proceedings of the International Symposium on Low Power Electronics and Design*, pp.149-154, August 1998.
- [13] N. Zhang, *Implementation Issues in the Design of a CDMA Baseband Receiver*, M.S. Thesis, University of California at Berkeley, May 1998.

continuation separator

- [14] T. Cho et al, "A Power-Optimized CMOS Baseband Channel Filter and ADC for Cordless Applications," *1996 Symposium on VLSI Circuits (slides)*, June 1996.
- [15] B. Boser, EECS 247 Class Notes, University of California at Berkeley, Spring 1998.
- [16] A. Feldman, *High-Speed, Low-Power Sigma-Delta Modulators for RF Baseband Channel Applications*, PhD. Dissertation, University of California at Berkeley, September 1997.
- [17] K. Nishimura, *Optimal Partitioning of Analog and Digital Circuitry in Mixed-Signal Circuits for Signal Processing*, PhD. Dissertation, University of California at Berkeley, 1993.
- [18] D. Sobel and L. Zheng, "Baseband Filter and A/D Converter for Wideband RF Receiver," *EECS 247 midterm report*, University of California at Berkeley, Spring 1998.
- [19] Y. Geerts, et al. "A 3.3V 15-bit delta-sigma ADC with a signal bandwidth of 1.1 MHz for ADSL applications," *Proceedings of the 24th European Solid-State Circuits Conference*, pp.168-171, Sept 1998.
- [20] E. Morifuji, et al. "Future Perspective and Scaling Down Roadmap for RF CMOS," *Digest of Technical Papers, 1999 Symposium on VLSI Technology*, pp. 163-164.
- [21] A. Annema, "Analog Circuit Performance and Process Scaling," *IEEE Trans. on Circuits and Systems II*, vol. 46, no. 6, pp.711-725, June 1999.
- [22] <http://bwrc.eecs.berkeley.edu>
- [23] A. Chandrakasan, et al. "Low-Power CMOS Digital Design," *IEEE J. Solid-State Circuits*, vol. 27, no.4, pp.473-484, April 1992.
- [24] H. Meyr, et al. *Digital Communication Receivers*, Wiley and Sons, New York, 1998.
- [25] S. Sheng, R. Brodersen, *Low-Power CMOS Wireless Communications*, Kluwer Academic Press, Boston, 1998.
- [26] P. Husted, *Design and Implementation of Digital Timing Recovery and Carrier Synchronization for High Speed Wireless Communications*, M.S. Report, University of California at Berkeley, Decemeber 1999.
- [27] A. Gatherer, et al, "Method and System for Analog to Digital Conversion," *U.S. Patent Application*, Docket No TI-22227 (032350.A451)
- [28] S. Norsworthy, R. Schreier, G. Temes, ed., *Delta-Sigma Data Converters: Theory, Design and Simulation*, IEEE Press, New York, 1997.

continuation notice

continuation separator

- [29] P. Aziz, et al. "An Overview of Sigma-Delta Converter," *IEEE Signal Processing Magazine*, vol. 13, no. 1, pp.61-84, January 1996.
- [30] A. Marques, et al. "A 15-b Resolution 2-MHz Nyquist Rate Delta-Sigma ACD in a 1- μ m CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp.1065-1075, July 1998.
- [31] B. Boser, et al. "The Design of Sigma-Delta Modulation Analog-to-Digital Converters," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 6, pp. 1298-1308, December 1998.
- [32] L. Williams, *Modeling and Design of High-Resolution Sigma-Delta Modulators*, PhD. Dissertation, Stanford University, 1993.
- [33] J. Cherry, et al., *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion*, Kluwer Academic Press, Boston, 2000.
- [34] W.R. Bennet, "Spectra of Quantized Signals," *Bell Systems Technical Journal*, vol. 27, pp.446-472, July 1948.
- [35] K. Khoo, *Programmable, High-Dynamic Range Sigma-Delta A/D Converter for Multistandard, Fully-Integrated CMOS RF Receiver*, Masters Thesis, University of California at Berkeley, December 1998.
- [36] R. Schreier, "An Empirical Study of High-Order Single-Bit Delta-Sigma Modulators," *IEEE Trans. on Circuits and Systems II*, vol. 40, no. 8, pp.461-466, August 1993.
- [37] P. Benabes, et al. "A Methodology for Designing Continuous-Time Sigma-Delta Modulators," *Proceedings of the IEEE European Design and Test Conference*, pp.46-50, March 1997.
- [38] Y. Geerts, et al. "A 2.5 Msample/S Multi-Bit $\Delta\Sigma$ CMOS ADC with 95dB SNR," *Digest of Technical Papers, 2000 International Solid-State Circuits Conference*, pp.336-337, February 2000.
- [39] T. Leslie and B. Singh, "An Improved Sigma-Delta Modulator Architecture," *IEEE Proc. ISCAS '90*, pp.372-375, May 1990.
- [40] B. Brandt, et al. "A 50-MHz Multibit Sigma-Delta Modulator for 12-b 2-MHz A/D Conversion," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 12, pp.1746-1756, December 1991.
- [41] L. R. Carley, "A noise-shaping coder topology for 15+ bit converters," *IEEE J. Solid-State Circuits*, vol. SC-24, pp.267-273, April 1989.

continuation notice

continuation separator

- [42] E. Fogleman, et al. "A Dynamic Element Matching Technique for Reduced-Distortion Multibit Quantization in Delta-Sigma ADCs," *Proceedings of the 1999 IEEE International Symposium on Circuits and Systems*, pp.290-293, May 1999.
- [43] F. Chen et al, "A High Resolution Multibit Sigma-Delta Modulator with Individual Level Averaging," *IEEE J. Solid-State Circuits*, vol 30, no. 4, pp453-460, April 1995.
- [44] R. Baird, et al. "Linearity Enhancement of Multibit Delta-Sigma A/D and D/A Converters Using Data Weighted Averaging," *IEEE Trans. on Circuits and Systems II*, vol. 42, no. 12, pp.753-762, December 1995.
- [45] I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. on Circuits and Systems II*, vol. 44, no. 10, pp.808-817, Oct 1997.
- [46] K. Bult, "Analog Broadband Communications Circuits in Pure Digital Deep Sub-Micron CMOS," *Digest of Technical Papers, 199 International Solid-State Circuits Conference*, pp.76-77, February 1999.
- [47] A. Marques, et al. "Optimal Parameters for Cascade Delta-Sigma Modulators," *Proceedings of 1997 IEEE ISCAS*, pp.61-64, June 1997.
- [48] D. Yee, *Ph.D. Dissertation*, University of California at Berkeley, to be published.
- [49] K. Lee and R. Meyer, "Low-Distortion Switched-Capacitor Filter Design Techniques," *IEEE J. Solid-State Circuits*, vol 20, no. 6, pp.1103-1113, December 1985.
- [50] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, New York, 1998.
- [51] C. Hu, *EE231 lecture notes*, University of California at Berkeley, Spring 1999.
- [52] B. Boser, *EE240 lecture notes*, University of California at Berkeley, Fall 1997.
- [53] T. Cho, *Low-Power Low-Voltage Analog-to-Digital Conversion Techniques Using Pipelined Architectures*, PhD. Dissertation, University of California at Berkeley, 1995.
- [54] D. Yee, et al. "A 2-GHz Low-Power Single-Chip CMOS Receiver for WCDMA Applications," *ESSCIRC 2000*, to be published.
- [55] C. Doan, *Masters Report*, University of California at Berkeley, to be published