SEMICONDUCTOR WAFER BONDING AND ION-CUT LAYER TRANSFER

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Changhan Yun

Memorandum No. UCB/ERL M01/5

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
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Changhan Yun

B.S. (Seoul National University, Korea) 1995
M.S. (University of California, Berkeley) 1998
M.Eng. (University of California, Berkeley) 2000

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Nathan Cheung Dec. 6, 2000
Chair Date

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Semiconductor Wafer Bonding and Ion-Cut Layer Transfer

Abstract

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Doctor of Philosophy in Engineering

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Professor Nathan W. Cheung, Chair

This dissertation describes a semiconductor layer transfer process using wafer bonding and hydrogen-induced semiconductor cleavage. In this process, hydrogen is implanted into a wafer that has the layer to be transferred. The implanted hydrogen ions form a highly damaged region around the hydrogen stopping range. The implanted wafer is then bonded to another wafer using low-temperature direct bonding. With appropriate heat or mechanical treatment, the bonded wafer pair separates along the highly damaged region, resulting in the transfer of the layer from one substrate to the other.

With this technique, we have been able to fabricate silicon-on-insulator (SOI) structures by transferring single- and poly- crystalline silicon layers, especially using hydrogen plasma implantation, oxygen plasma-activated wafer bonding, and thermal cleavage and mechanical cleavage methods. We have also formed silicon, SOI, and oxide membranes on buried cavities and channels, which can be applied for use in pressure transducers, microfluidic systems, and radio frequency filters and resonators. In these demonstrations, we

have observed good thickness uniformity (<1 %) across a 100 mm wafer and surface micro-roughness (<10 nm) of the transferred layers.

For the transfer of pre-fabricated electronic device layers, gate oxide damage was first evaluated after high-dose and high-energy hydrogen implantation through metal-oxide-silicon (MOS) transistors. The results showed that stress-induced leakage current (SILC) through the gate oxide increased as hydrogen dose increased for the 5 nm-thick oxide. For the 1.8 nm-thick gate oxide, no SILC was observed, showing that the implantation damage is not significant for the ultra-thin (< 2 nm) oxides.

To protect the thicker (>3 nm) oxides from damage during the hydrogen implantation, we have proposed layer transfer with patterned implantation of hydrogen. In this process, active device regions were masked during the implantation. This experiment showed that the hydrogen induced silicon layer cleavage is feasible even without a continuous hydrogen implantation of the entire wafer, and that the silicon cleavage can propagate across at least 16 microns of non-implanted area from a 4 micron-wide implanted region each side. Furthermore, it has shown that the mechanical cleaving can overcome some non-implantation area limitations imposed by the thermal cleavage process.

Nathan Cheung

Professor Nathan W. Cheung
Chair, Dissertation Committee

To my parents

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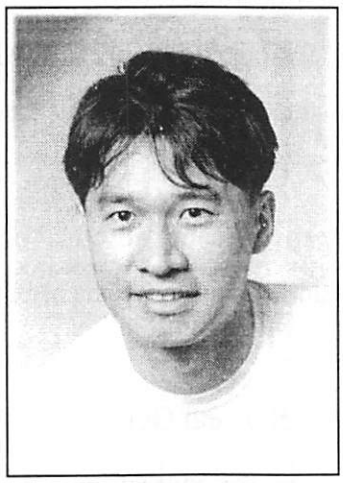
Berkeley, California CHANGHAN YUN
December 2000

ABOUT THE AUTHOR



CHANGHAN YUN was born in Korea on October 31, 1971. He earned his B.S. degree in nuclear engineering and physics at Seoul National University, Korea, where he studied between March 1991 and February 1995. He started his graduate studies in August 1995 at the University of California, Berkeley, where he received the M.S. degree in nuclear engineering in December 1998 and the M.Eng. degree in electrical engineering in May 2000. This dissertation is for his Ph.D. degree, and was filed on December 21, 2000. In addition, he has completed the Management of Technology program, a joint program between the College of Engineering and the Haas School of Business at the University of California, Berkeley. During his graduate studies in Berkeley, he taught an undergraduate course on "Microfabrication Technology" covering hands-on processing of integrated circuits and microelectromechanical devices. He also worked on logic device integration in Advanced Micro Devices, Inc. in Sunnyvale, California as a summer intern.

When not working, he spends his time with a snowboard and golf clubs, drinking with his friends, reading novels, and listening to music.

Chapter 1

INTRODUCTION

1.1 Integration of Microsystems

Through intimate integration of disparate (e.g., electronic, optical, piezoelectric, superconducting, magnetic, organic, etc.) materials in a single substrate, the functionality of integrated microsystems can be significantly enhanced beyond what is possible in a single material platform. Along with continuous scaling of individual devices such as transistors and micro-machines, this *multi-systems-on-a-chip* integration can shrink microsystems further by increasing the number of microelectronic circuits and machines on a single chip. A useful integrated microsystem must combine the materials that are individually suited for their specific functions; e.g., silicon for electronic circuits, III-V compounds for optical devices, and piezoelectric materials for electro-mechanical transducers. Furthermore, these materials must be able to integrated with virtually any substrate including silicon, glass, plastics, etc.

Figure 1.1 illustrates an example of an integrated microsystems being developed by inter-disciplinary research groups in the University of California, Berkeley [1]. The proposed device is designed to analyze DNA (deoxyribonucleic acids) with organic dye molecules. This *biology-lab-on-a-chip* endeavor necessitates a wide variety of materials components, including epitaxially-grown (In, Ga)N heterostructures for light emission, piezoelectric thin-film membranes for sensors and actuators, micro-machined Si and/or polymer for molecules and cells transport, and Si for signal processing.

These material combinations, however, cannot be realized with current planar technology without substantial performance degradation due to compromising the processing

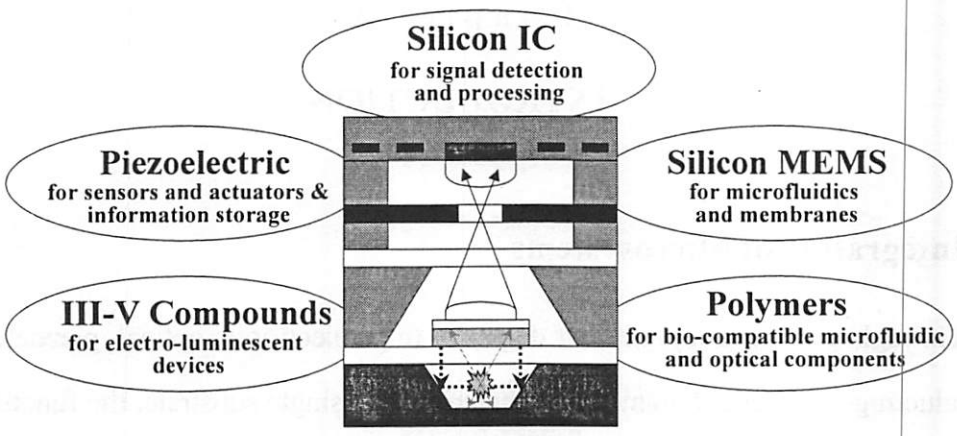


Figure 1.1 Materials and devices integration for optical microfluidic systems on a chip – a side view [1]

of the different materials. For example, group III – nitride heterostructures will decompose at temperatures higher than 900 °C, imposing constraints on silicon integrated circuit (IC) fabrication. In order to incorporate these materials with silicon transistors and/or polymer substrates, it is necessary to develop *paste-and-cut* integration processes, which can overcome the thermal, mechanical, and chemical mismatches between materials.

1.2 *Paste-and-Cut* Approach

Figure 1.2 illustrates the concept of the *paste-and-cut* technology, which allows each material or device to be separately synthesized and processed prior to assembly on a final handle wafer. This technology, as its nomenclature indicates, has two principal components – pasting and cutting.

Pasting is a method for bonding any material films and device structures to each other or to a *handle* wafer, including adhesive bonding, direct bonding (see chapter 2), anodic bonding [2], metallic bonding [3], etc.

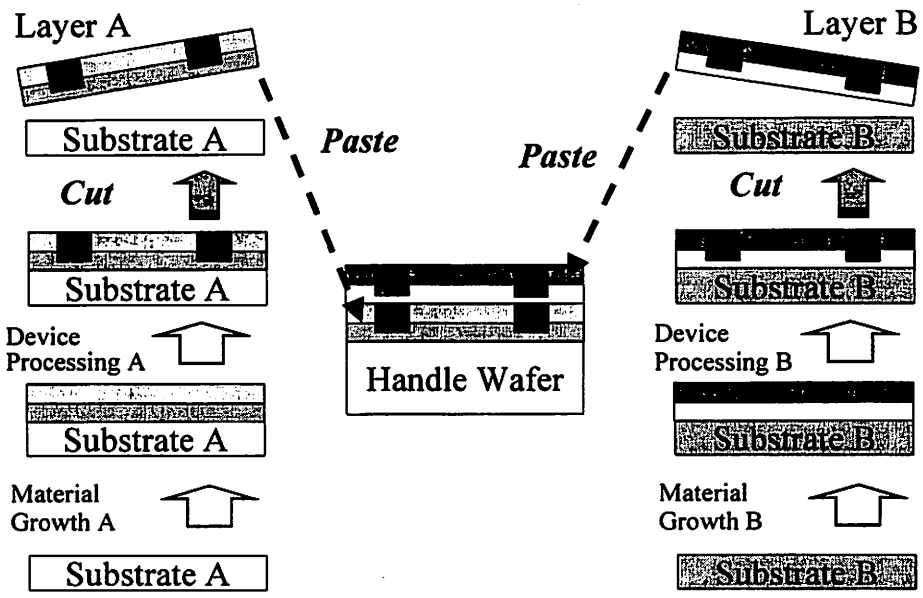


Figure 1.2 *Paste-and-cut* integration, which allows each material or device to be synthesized and processed separately prior to assembly on a final handle wafer.

Cutting is a method for separating a material film or device layer from its original substrate (*donor* wafer) to accomplish layer transfer from one (donor) wafer to another (handle) wafer. The cutting methods include chemical etching or lift-off, mechanical separation [4], ion-beam cutting (see chapter 4), laser lift-off [3], etc.

By combining these pasting and cutting tools, depending on the process conditions or constraints with materials and devices layers available, many complex microsystems integration can be achieved. This paste-and-cut integration allows a flexible process flow, bypassing materials and devices compatibility limitations.

1.3 Layer Transfer Using Wafer Bonding and Ion-Cut

Among the pasting and cutting tools, wafer direct bonding and ion-cutting are the most versatile methods for crystalline material layer transfer. Figure 1.3 illustrates the *ion-cut layer transfer* process. In this process, hydrogen and/or helium is implanted into a

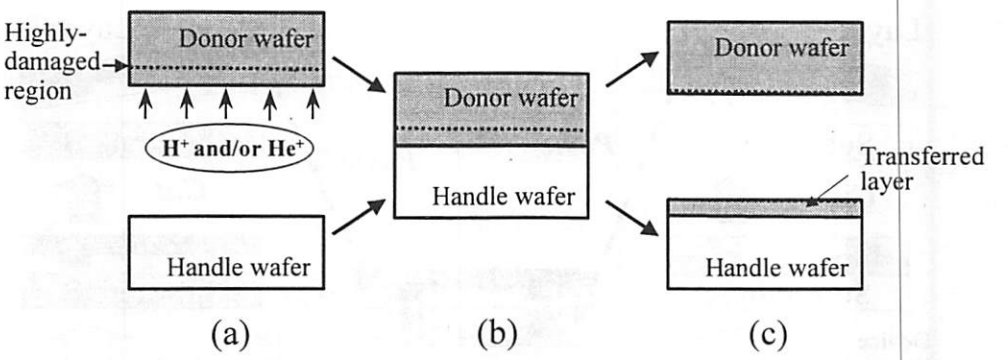


Figure 1.3 Layer transfer process using wafer bonding and ion-beam cutting. (a) Ion implantation. (b) Low-temperature wafer direct bonding. (c) Layer cleavage by thermal or mechanical means.

wafer that has the layer to be transferred. Due to the high dose implantation (~10^{17} ions / cm^2), a highly damaged region is formed around the ion stopping range in the substrate. The implanted wafer (donor wafer) is then bonded to another wafer (handle wafer) directly at low temperature (~200 °C). By an appropriate heat treatment or a mechanical separation method, the bonded wafer pair will completely separate along the highly damaged region, resulting in the transfer of the layer.

In this dissertation, an overview and recent accomplishments regarding the ion-cut layer transfer are presented. All chapters are organized in a self-contained fashion – wafer bonding, hydrogen-induced silicon blistering, layer transfer, gate oxide damage, patterned ion-cut, and micro-membrane fabrication. The goal of chapter 2 is to achieve an interfacial bonding strength larger than the fracture or yield strength of the bonded materials at low temperature by understanding bonding mechanisms with different surface treatments. Chapter 3 reviews the literature on the behavior of implanted hydrogen in silicon. In chapter 4, a comparison is made between transferred single- and poly- crystalline silicon layers, and ion-cut with plasma implantation of hydrogen is demonstrated as an effective alternative to the conventional beam-line implanter. For pre-fabricated metal-oxide-semi-

conductor transistor layer transfer applications, gate oxide damage due to hydrogen implantation is evaluated in chapter 5, and a novel process of patterned ion-cut is reported in chapter 6. In the patterned ion-cut process, even if hydrogen is implanted only in certain areas (e.g., non-active device regions) of a wafer, the hydrogen-induced cleavage can propagate through the non-implanted region, resulting in the layer transfer. Chapter 7 shows that sub-micron thick single crystalline silicon membranes can be fabricated using the ion-cut process with good thickness uniformity and micro-smoothness.

References

[1] T. Sands, N. W. Cheung, and L. P. Lee, *Integration of Dissimilar Materials by Bonding and Thin-film Transfer: Application to Integrated Optical Microfluidic Systems*, Proposal to the National Science Foundation: DMII-0088145, 2000.

[2] A. Gerlach, D. Maas, D. Seidel, H. Bartuch, S. Schundau, K. Kaschlik, "Low-temperature anodic bonding of silicon to silicon wafers by means of intermediate glass layers," *Microsystem Technologies*, vol.5, pp.144-149, 1999.

[3] W. Wong, T. Sands, N. Cheung, M. Kneissl, D. Bour, P. Mei, L. Romano, and N. Johnson, "Ubiquitous blue LEDs: the integration of GaN thin films with dissimilar substrate materials by wafer bonding and laser lift-off," *Compound Semiconductor*, vol. 5, no. 9, pp. 54-56, 1999.

[4] K. Sakaguchi, K. Yanagita, H. Kurisu, H. Suzuki, K. Ohmi, and T. Yonehara, "ELTRAN® by water-jet splitting in stress-controlled porous Si," in *1999 IEEE International SOI Conference Proceedings*, Rohnert Park, CA, 4-7 October 1999, pp. 110-111.

Chapter 2

SEMICONDUCTOR WAFER BONDING

Abstract- Low-temperature semiconductor wafer direct bonding is discussed. With oxygen plasma activation of wafer surfaces, it has been shown that the bonding strength can exceed the silicon lattice bonding energy. Poly-crystalline silicon wafers have been bonded successfully to other thermally oxidized wafers after chemical-mechanical polishing of the poly-silicon surface.

2.1 Introduction

Wafer direct bonding refers to joining two similar or dissimilar wafers together without any adhesives or glues. The wafers can be any materials: semiconductors (Si, GaAs, SiGe, etc.) or insulators (sapphire, quartz, glass, etc.). After the completion of bonding, however, the mechanical strength of the bonding interface should be comparable to that of the bonded material.

Even though wafer bonding was originally developed for glass-packaging of micro sensors [1], the motivation of wafer bonding is for homogeneous or heterogeneous materials integration and 3-dimensional structure fabrication. For example, III-V compounds such as GaN or GaAs are used for light emitting elements, while silicon is used for electronic circuits. If it is desired to integrate these two different materials into a single chip for more functionality, the wafer bonding technique can be applied. For most micro-electromechanical and micro-fluidic systems applications, e.g., mechanical resonators or micro-channels, wafer bonding is necessary for fabrication of flexible membranes or fluid-flowing ducts.

Low temperature wafer bonding is essential for bonding substrates with temperature limitations (e.g. GaAs, glass, etc.), and for bonding between materials with different thermal expansion characteristics. This chapter will focus on direct bonding between single or poly crystalline silicon wafers and silicon dioxide coated wafers. Room temperature or low temperature (~200 °C) wafer direct bonding is studied extensively, since it is crucial for the ion-cut layer transfer technology (discussed in chapter 4).

2.2 Wafer Direct Bonding

2.2.1 Requirements for Direct Bonding

The first step of wafer bonding is mating two wafer surfaces together directly. Since there is no adhesive involved in the direct bonding, the bonding is based on interactions between two solid surfaces. For a strong bond, the two surfaces should be close enough to attract each other by inter-molecular interactions. The main interaction between the two solid surfaces is van der Waals force or Coulomb force, depending on the existence of electric charge on the surfaces. If there are electric charges on the wafer surfaces, the electrostatic (Coulomb) interaction will be dominant. However, the electrostatic force becomes negligible in an ambient where water vapors are present, since the water vapors partly compensate the surface charges. Van der Waals force is a dipole interaction between polarizable atoms or molecules, and gets stronger as the distance between two molecules decreases [2]. For two flat surfaces, van der Waals attraction force is inversely proportional to the cube of the separation distance, and is very effective at distances within ~ 20 nm [3]. Therefore, any two solid surfaces may be bonded to each other in ambient as far as the two surfaces are flat, smooth, and clean.

Surface flatness (waviness) is a macroscopic parameter describing the thickness variations of the wafer surface with respect to an ideally flat surface. The flatness is often

measured in terms of the total thickness variation (TTV) and wavelength. TTV is the peak to valley height difference of the top wafer surface, and the wavelength is the period of the peak and valleys. In practice, even wafers from the same batch process have different TTV's and wavelengths. Upon wafer bonding of these two wafers, each of the wafers will be elastically deformed to achieve conformal bonding between the two surfaces [4]. For 10 cm diameter silicon wafers, since the wafers can be warped up to ~ 25 μm [5], TTV of up to 25 μm with a wavelength of 20 cm can be tolerable for bonding.

Surface smoothness (micro-roughness) is a microscopic parameter characterizing wafer surface quality. Figure 2.1 compares the concepts of the surface flatness and surface micro-roughness. Micro-roughness is usually measured in terms of root-mean-square (RMS) elevations obtained from a 1~2 μm × 1~2 μm surface by scanning probe microscopes such as scanning tunneling microscopes (STM) or atomic force microscopes (AFM). Empirically, RMS roughness of better than 10 Å is required for wafer bonding. Table 2.1 summarizes micro-roughness values of various surfaces prepared for wafer bonding and the ion-cut layer transfer process (which needs high dose implantation of hydrogen). Commercially available bare silicon wafers have RMS roughness around 2Å. Thermal oxidation and/or hydrogen implantation increased the RMS roughness up to around 4Å. All wafers showed good bonding characteristics, except for those wafers with poly-silicon or silicon nitride films deposited in a low-pressure chemical vapor deposition (CVD) chamber. The deposited films had RMS roughness of 1~10 nm depending on the film material and thickness.

A clean surface is free of particles and organic contamination. Particles cause imperfect gap closure, and leave voids behind after bonding. If two wafer surfaces are bonded without removing hydrocarbon residues on the surfaces, the hydrocarbons will be

Table 2.1 Micro-roughness after various wafer surface treatments. Data obtained from AFM scan over 2μm×2μm.

Wafer description	RMS roughness (nm)	Maximum roughness (nm)	Bonding possible?
Bare silicon (starting reference)	0.22	1.7	Yes
Thermal oxide: 60nm-thick	0.25	2.1	Yes
Thermal oxide: 200nm-thick	0.36	3.0	Yes
Bare silicon with H implant	0.25	1.9	Yes
Thermal oxide: 60nm-thick, H implant	0.27	2.6	Yes
After H implant through 60nm-thick thermal oxide, remove all oxide using HF	0.31	2.8	Yes
Thermal oxide: 200nm-thick, H implant	0.38	3.0	Yes
After H implant through 200nm-thick thermal oxide, remove all oxide using HF	0.35	2.7	Yes
CVD silicon nitride: 200 nm-thick	1.4	11	No
CVD poly-silicon: 2.2 μm-thick	10	76	No

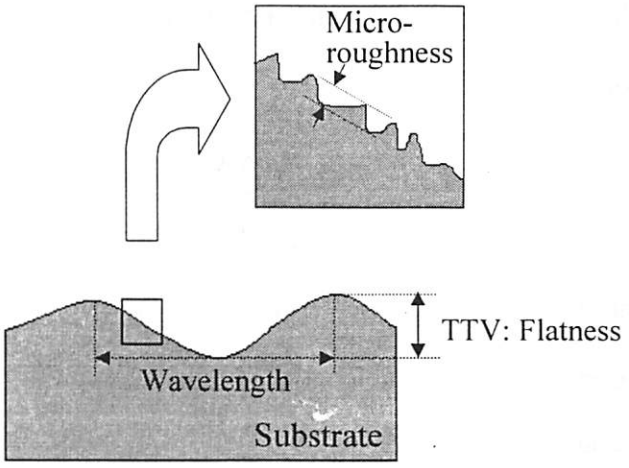


Figure 2.1 Surface flatness vs. smoothness. The flatness is a macroscopic parameter describing the thickness variations of the wafer surface, and is measured in terms of total thickness variation (TTV). The smoothness is a microscopic parameter characterizing wafer surface quality (roughness), and is measured in terms of RMS elevations from a micron-size surface.

out-gassed upon annealing or any heat treatments. The out-gassed hydrocarbons expand, de-bonding the bonding interface, and forming a void. In most cases, wafer cleaning is necessary to get rid of any particles and other contaminants from the wafer surface before bonding. The wafer surface preparation methods, including chemical cleaning and surface activation, are discussed in subsection 2.2.3.

2.2.2 Bonding Inspection

If there are any regions in a wafer that do not satisfy the bonding requirements described above, then unbonded area will be present, forming bubbles or voids inside a bonded pair. The voids can be detected using an optical interference method. Figure 2.2 (a) illustrates a typical setup for optical inspection using an infrared (IR) light source and camera. In order to transmit light, the photon energy should be lower than the band-gap energy of the wafer material, necessitating the use of IR for silicon imaging. At higher energies, the incident photons will be used to generate electrons and holes, and therefore will be absorbed almost entirely in the wafer. For light of wavelength λ to penetrate a material of band-gap energy E_g,

$$E_g > hc/\lambda \tag{2.1}$$

where h is the Planck constant and c is the speed of light. For silicon, with band-gap energy of 1.12 eV, light of a wavelength greater than 1.10 μm (IR) can penetrate the material. Table 2.2 summarizes minimum wavelengths of light required to penetrate various semiconductors and insulators [5], [6].

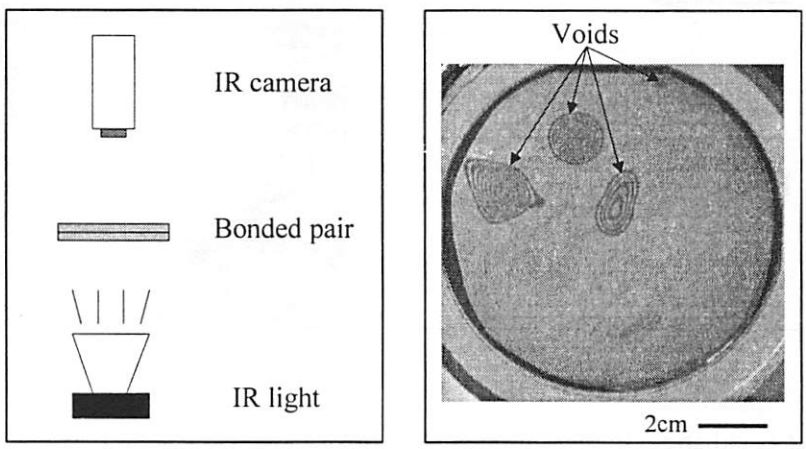
Figure 2.2(b) shows an IR image of a bonded pair of silicon wafers. The three interference patterns in the image indicate void regions. The gap of a void, d, can be estimated by counting the number of fringes, N, of the interference pattern [7]:

$$2d\sin\theta = N\lambda \tag{2.2}$$

Table 2.2 Minimum wavelengths for which the materials are transparent

Material	E_g (eV)	λ_{min} (μm)
Si	1.12	1.10
Ge	0.67	1.84
C (diamond)	5.48	0.22
GaAs	1.43	0.86
GaN	3.4	0.36
GaP	2.24	0.55
InP	1.35	0.91
AlN	6.2	0.20
SiO_2	~8	~0.15
Si_3N_4	4.7	0.26

where θ is the angle of the incident light, 90° in this case. At the minimum wavelength for silicon transparency, 1.1 μm, the minimum gap detectable will be one half of $\lambda/2$, or 0.28 μm, since one half of a fringe can be still detected using this method. The minimum lateral dimension of a void detectable in this method is limited by the camera resolution, which is about 1mm for the present setup.



(a) IR setup (b) IR image

Figure 2.2 IR wafer bonding inspection setup and image.

2.2.3 Bond Strength Measurement

In order to qualitatively measure the strength of a bonded pair, a crack opening method has been used [8]. Figure 2.3 shows the crack opening method with a solid wedge, in this case a razor blade. If a razor blade is inserted between two bonded wafers, the two wafers will be separated along the bonding interface until the wafer bending force and the wafer bonding force are balanced. The bond strength γ can be obtained in terms of the equilibrium crack length L, wafer thickness t, and the blade thickness y:

$$\gamma = \frac{3Et^3y^2}{32L^4} \tag{2.3}$$

where E is the modulus of elasticity of the wafer [8]. For example, in Figure 2.3(b), L = 13 mm, t = 528 μm, y = 102 μm. With silicon (100) wafers, E = 166 GPa, and the surface energy of the bonding can be calculated as γ = 0.84 J/ m^2. In this calculation, the presence

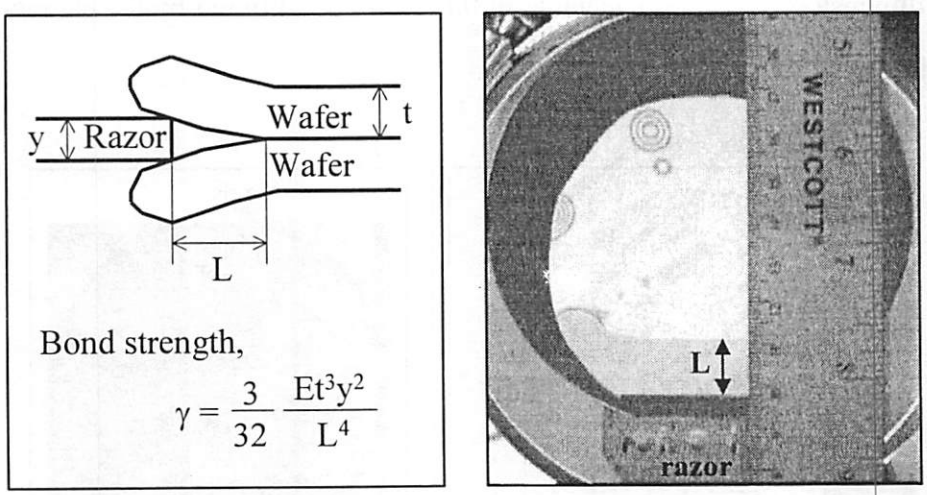


Figure 2.3 Bond strength measurement. If a razor blade is inserted between two bonded wafers, the two wafers will be separated along the bonding interface until the wafer bending force and the wafer bonding force are balanced. (a) Schematic side view. (b) IR top view.

of any oxide thin film on either wafer surface was neglected, since the oxide thickness is less than 0.1 % of the silicon wafer thickness.

2.3 Wafer Surface Treatments

2.3.1 Wafer Cleaning

Since bare silicon is highly reactive, a silicon wafer surface can attract particles and metallic and organic contaminants. Also, when silicon is exposed to air or to pure water, up to ~10 Å of native oxide can be grown even at room temperature [9], and this native oxide can be a trap-center for impurities and contaminants. The metals and organics can be removed by piranha solution, composed of 5 parts sulfuric acid (H_2SO_4) and 1 part hydrogen peroxide (H_2O_2) by volume, and self-heats up to ~120 °C upon mixing. Piranha removes metals by forming soluble complexes and organic contaminants by oxidizing (burning) them. The native oxide and by-product oxide from piranha cleaning can be removed using diluted hydrofluoric acid (HF). Since HF usually removes all native oxides and any left-over metals on a silicon surface, the silicon surface after HF cleaning will be terminated mostly by hydrogen and fluorine. Because the Si–H bond is known to be weakly polarized, having little attraction for water, the surface becomes hydrophobic [10]. After the HF cleaning, particles can be attracted to the highly reactive bare silicon surface, and these particles are effectively removed by RCA1 solution. RCA1 is a mixture of 1 part ammonia (NH_4OH), 1 part H_2O_2, and 5 parts water (H_2O) by volume, and is heated to ~80 °C. The H_2O_2 in the solution quickly oxidizes the silicon surface to form native oxide. This native oxide is cleaner than the native oxide found on the starting wafer or after the piranha cleaning, since most particles and contaminants are removed from the previous cleaning steps. During pure de-ionized (DI) water rinsing after the cleaning, the native oxide is known to form Si–OH (silanol) bonds through a reaction with water

[10]. Unlike the Si–H bond after an HF dip, the silanol bond is strongly polarized, so the surface becomes hydrophilic [10].

For both hydrophobic and hydrophilic surfaces, hydrogen bonding plays an important role. The hydrogen bonding is a strong dipole-dipole interaction. Normally hydrogen easily forms a covalent bond with any electronegative atoms such as F, O, N, Cl, Br, etc. These bonds are strongly polarized, making the hydrogen partially positive. This electrophilic hydrogen will attract another electronegative atom to form a hydrogen bond. Therefore the hydrogen bond is in the form of

$$X - H \cdots Y \tag{2.4}$$

where X and Y are electronegative atoms, and "– "and "···" indicate a covalent and a hydrogen bond, respectively [10].

For a hydrophobic surface terminated with –H or –F, two wafer surfaces may be bonded together by some chained residual HF (H–F) molecules linked by hydrogen bonds. The chemical formula can be expressed as

$$Si - F \cdots [H - F \cdots]_n H - Si \tag{2.5}$$

where n = 0, 1, 2, 3 …, the number of hydrogen bonded HF molecules bridging the two surfaces [10]. For a hydrophilic surface terminated with –OH, two wafer surfaces may be bonded together with some chained residual H_2O (H–O–H) molecules linked by hydrogen bonds, such as

$$Si - O \overset{H \cdots}{\diagup} \left[\begin{matrix} O - H \cdots \\ H \diagup \end{matrix} \right. \overset{H}{\diagdown} \left. O - Si \right]_n . \tag{2.6}$$

Again, n is the number of hydrogen bonded H_2O molecules bridging the two surfaces.

Since the Si–F group and the Si–OH group play important roles in hydrophobic and hydrophilic bonding, respectively, the strength of each bond depends on the density of ei-

ther Si–F or Si–OH. The surface density of Si–F is known to be ~1/nm^2 or less, while the Si–OH bond density can be ~5/nm^2, resulting in 5~10 times stronger bonding for hydrophilic surfaces (~100 mJ/m^2 vs. ~10 mJ/m^2) [10].

2.3.2 Plasma Surface Activation

A wafer exposed to some plasma (e.g., hydrogen, argon, oxygen, etc.) can activate the surface to increase bonding energy [10]-[15]. In hydrogen and/or argon plasmas, the ions sputter-etch any native oxide and hydrocarbons, resulting in highly reactive pure silicon surface [10], [11]. However, excessive plasma power or exposure time can also etch the silicon substrate, increasing micro-roughness of the surface [12].

With oxygen plasma treatment, thin (1~2 nm) oxide formation has been observed [13]-[15], and depending on the plasma condition, the surface micro-roughness can be improved [15]. Even if surface smoothing increases the wafer bonding energy, a more fundamental reason for increased bonding strength is believed to be the reduction of water content on the surface. For stronger bonding, the hydrogen bond between the two Si–OH (silanol) bonds in (2.6) should turn into a Si–O–Si (siloxane) bond by the following reaction:

$$\text{Si–OH} + \text{HO–Si} \rightarrow \text{Si–O–Si} + \text{H}_2\text{O} \,. \qquad (2.7)$$

Since water can break the stronger siloxane bonds to form the weaker silanol bonds by the reverse reaction of (2.7) [16], the reduction of water by oxygen plasma will improve the bonding strength significantly. There may be several mechanisms of water removal from the surface; one of which is through water consumption during the oxide growth [13], [17]:

$$\text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2 \,. \qquad (2.8)$$

Figure 2.4 compares the bond strengths between bonded pairs before and after oxygen plasma treatment. The oxygen plasma was generated between two parallel plates by applying 200 W radio-frequency (RF, 13.56 MHz) power. The chamber was sustained at the pressure of ~250 mTorr (~30 Pa) with 51 sccm (cm^3/min at standard temperature and pressure) of oxygen flow. Both RCA1-cleaned silicon and oxide-covered (200 nm-thick thermal) wafers were placed in the chamber for ~30 seconds, and were then bonded to each other right after being taken out of the chamber. The bonding strength was measured using the crack opening method described in subsection 2.2.3. As shown in Figure 2.4, the plasma treated pair was about 5 times stronger than just RCA1-treated one at room temperature (23 °C in this experiment).

The figure also shows the bond strength evolution after annealing at different temperatures. The annealing time was ~10 hours for all temperatures. The annealing made the bonding interface stronger with increased temperature, and with an anneal at ~200 °C,

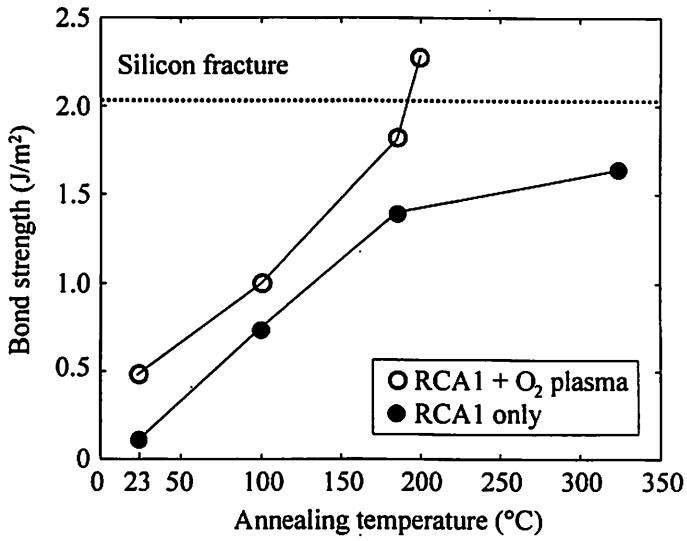


Figure 2.4 Plasma treatment and annealing temperature effects on bond strength. With O_2 plasma surface treatment and annealing at 200 °C for ~10 hours, bond strength exceeding the silicon fracture strength can be achieved.

the plasma-treated pair made the interface stronger than silicon fracture surface energy (2.1 J/m^2 for silicon (111) surface [18]). The bond strength improvement may be due to the out-diffusion and reduction of water from a bonding interface during annealing. For the rest of work in this dissertation, the RCA1 clean followed by oxygen plasma treatment was used for bonding, and annealing at 200 °C for ~10 hours was used for curing. In this way, it is ensured that the bonding interface is comparable to or stronger than the bulk silicon.

2.3.3 Chemical-Mechanical Polishing for Bonding

Most commercially available wafers are flat and smooth enough for direct bonding. However, a wafer surface which has gone through a typical series of device fabrication processing steps may not be flat or smooth any more. For example, chemical vapor deposited poly-silicon or silicon nitride films were not suitable for bonding due to the rough surfaces in our experiment (see Table 2.1).

For the bonding of non-flat or non-smooth surfaces, chemical mechanical planarization or polishing (CMP) technology has been adopted [19], [20]. In the CMP process, a wafer to be polished is mounted on a wafer carrier by vacuum, and an external downward force is applied for the wafer to contact a polishing pad (see Figure 2.5). The polishing pad is usually a poromeric synthetic material such as polyurethane. This micro-porous pad works effectively with abrasive slurry, which is a colloidal dispersion of 10 nm - 100 μm silica (SiO_2) particles in a potassium hydroxide (KOH) and DI water solution. By pressing the wafer and rotating both the wafer and polishing pad within the slurry, the wafer surface is polished by chemical (formation of $Si(OH)_4$ by Si from wafer and OH from KOH in slurry) and mechanical (frictional removal of $Si(OH)_4$ by silica particles) means [21].

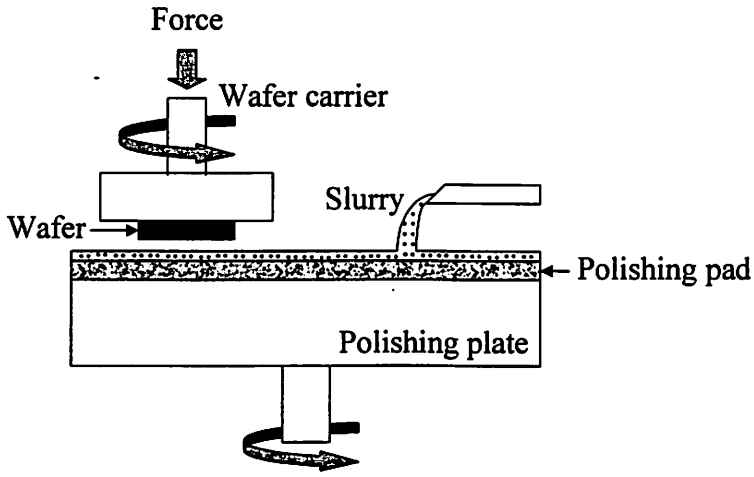


Figure 2.5 CMP schematic. A wafer is mounted on a wafer carrier, and external downward force is applied for the wafer to contact a polish pad. By pressing the wafer and rotating both the wafer and polishing pad within the slurry, the wafer surface is polished by chemical and mechanical means.

In this way, poly-silicon was polished and bonded directly to other thermally oxidized wafers. In an experiment, ~2.2 μm-thick undoped poly-silicon was deposited on a wafer surface in a ~600 °C silane (SiH_4) chamber. The poly-silicon wafer was polished using the CMP setup shown in Figure 2.5. The wafer and polishing pad contacting pressure was 6 psi (86 kPa) with rotational speeds of 10 and 100 rpm for the wafer and polishing pad, respectively. The wafer was polished for one minute, and ~680 nm of poly-silicon was removed. The micro-roughness before and after CMP was measured to be 10 nm and 0.93 nm, respectively (see Figure 2.6). The maximum roughness was also improved by 10 times during the CMP process. The polished wafer was then bonded to a thermally oxidized silicon wafer after piranha and RCA1 cleaning and oxygen plasma activation. The bonded pair was further annealed at 200 °C for ~10 hours. The bonding strength measured after the annealing was 2.4 J/m^2, which is about the same as achieved with a bare silicon wafer bonding to an oxidized wafer (see Figure 2.4).

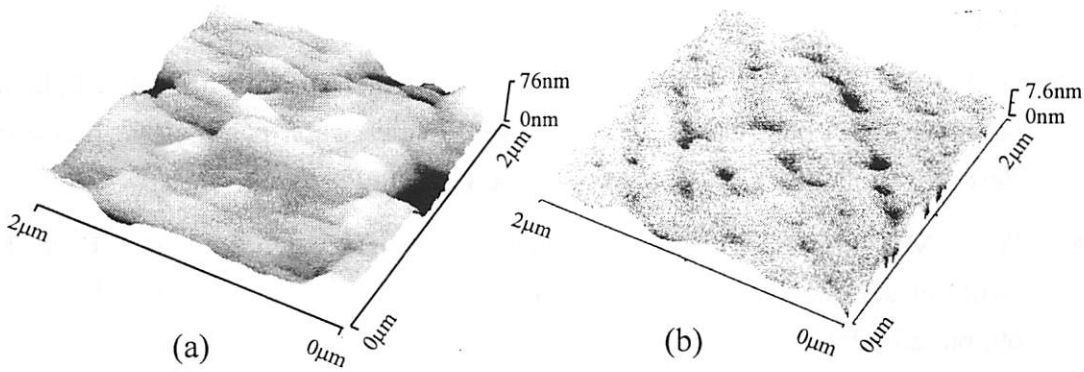


Figure 2.6 Poly-silicon surfaces (a) before and (b) after CMP. CMP made the surface ~10 times smoother (from 10nm to 0.93nm) and therefore bondable.

2.4 Summary

Low temperature wafer direct bonding was described with respect to surface requirements such as flatness, smoothness, and cleanness. In order to obtain a flat and smooth surface from a processed wafer, CMP has been adopted. CMP of CVD poly-silicon made the surface about 10 times smoother than as-deposited, and boding strength was comparable to a bare silicon wafer.

Various chemical cleaning effects on silicon wafer surfaces were reviewed. Plasma surface activation of wafer surfaces and annealing of bonded pairs has been shown to strengthen the bonding interface, and a bonding interface stronger than silicon fracture was achieved with oxygen plasma treatment and low-temperature (~200 °C) annealing.

References

[1] G. Wallis, "Field assisted glass sealing," *Electrocomponent Science and Technology*, vol. 2, pp. 45-53, 1975.

[2] C. Kittel, *Introduction to Solid State Physics*, 6th ed., New York: Wiley, pp. 54-60, 1986.

[3] G. A. C. M. Spierings, J. Haisma, and T. M. Michielsen, "Surface-related phenomena in the direct bonding of silicon and fused-silica wafer pairs," *Philips Journal of Research*, vol. 49, pp. 47-63, 1995.

[4] W. P. Maszara, B. L. Jiang, A. Yamada, G. A. Rozgonyi, and A. J. R. de Kock, "Role of surface morphology in wafer bonding," *Journal of Applied Physics*, vol. 69, pp. 257-260, 1991.

[5] Q. Y. Tong and U. Gösele, *Semiconductor Wafer Bonding: Science and Technology*, New York: Wiley, pp. 33-48, 1999.

[6] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd ed., New York: Wiley, pp. 54-55, 1986.

[7] M. Born and E. Wolf, *Principles of Optics*, New York: Pergamon, pp. 285-290, 1959.

[8] W. P. Maszara, G. Goetz, A. Caviglia, and J. B. McKitterick, "Bonding of silicon wafers for silicon-on-insulator," *Journal of Applied Physics*, vol. 64, pp. 4943-4950, 1988.

[9] M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, and M. Ohwada, "Growth of native oxide on a silicon surface," *Journal of Applied Physics*, vol. 68, pp. 1272-1281, 1990.

[10] Q. Y. Tong and U. Gösele, *Semiconductor Wafer Bonding: Science and Technology*, New York: Wiley, pp. 49-101, 1999.

[11] H. Takagi, K. Kikuchi, R. Maeda, T. R. Chung, and T. Suga, "Surface activated bonding of silicon wafers at room temperature," *Applied Physics Letters*, vol. 68, pp. 2222-2224, 1996.

[12] W. B. Choi, C. M. Ju, B. K. Ju, and M. Y. Sung, "Wafer to wafer direct bonding using surfaces activated by hydrogen plasma treatment," in *Twenty Fourth IEEE/CPMT International Electronics Manufacturing Technology Symposium*, Austin, TX, 18-19 October 1999, p. 148.

[13] S. N. Farrens, J. R. Dekker, J. K. Smith, and B. E. Roberds, "Chemical free room temperature wafer to wafer direct bonding," *Journal of the Electrochemical Society*, vol. 142, pp. 3949-3955, 1995.

[14] P. Amirfeiz, S. Bengtsson, M. Bergh, E. Zanghellini, and L. Börjesson, "Formation of silicon structures by plasma-activated wafer bonding," *Journal of the Electrochemical Society*, vol. 147, pp. 2693-2698, 2000.

[15] D. Pasquariello, M. Lindeberg, C. Hedlund, and K. Hjort, "Surface energy as a function of self-bias voltage in oxygen plasma wafer bonding," *Sensors and Actuators A*, vol. 82, pp. 239-244, 2000.

[16] T. A. Michalske and B. C. Bunker, "Slow fracture model based on strained silicate structures," *Journal of Applied Physics*, vol. 56, pp. 2686-2693, 1984.

[17] G. Kräuter, A. Schumacher, and U. Gösele, "Low temperature silicon direct bonding for applications in micromechanics: bonding energies for different combination of oxides," *Sensors and Actuators A*, vol. 70, pp. 271-275, 1998.

[18] C. P. Chen, M. H. Leipold, "Fracture toughness of silicon," *American Ceramic Society Bulletin*, vol. 59, pp. 469-472, 1980.

[19] Q. Y. Tong, T. H. Lee, W. J. Kim, T. Y. Tan, U. Gösele, H. M. You, W. Yun, and J. K. O. Sin, "Feasibility study of VLSI device layer transfer by CMP PETEOS direct bonding," in *1996 IEEE International SOI Conference Proceedings*, Sanibel Island, FL, 30 September - 3 October 1996, pp. 36-37.

[20] C. Gui, M. Elwenspoek, J. G. E. Gardeniers, and P. V. Lambeck, "Present and future role of chemical mechanical polishing in wafer bonding," *Journal of the Electrochemical Society*, vol. 145, pp. 2198-2204, 1998.

[21] G. J. Pietsch, G. S. Higashi, and Y. J. Chabal, "Chemomechanical polishing of silicon: surface termination mechanism of removal," *Applied Physics Letters*, vol. 64, pp. 3115-3117, 1994.

Chapter 3

HYDROGEN-INDUCED SILICON SURFACE BLISTERING

Abstract- High-dose hydrogen or helium-induced material surface blistering has been observed for decades. This chapter reviews crystalline silicon lattice damages due to high dose implantation of hydrogen, particularly hydrogen bubble formation in the lattice. It also describes hydrogen bubble growth and silicon blistering due to pressure build-up inside the bubbles.

3.1 Introduction

Material surface failure due to high dose ion bombardment has been reported since early 1970's in nuclear fusion research [1], [2]. When energetic hydrogen (including its isotopes) and/or helium ions strike the plasma confinement wall (usually metal alloys), they penetrate the wall and stop at a given depth. With the continuous ion flux into the wall, atom built up underneath the wall surface will occur. If the irradiation dose is high enough, atoms may be coalesced to form bubbles, and the pressure inside will cause stresses to the wall material. These pressures and stresses can cause blisters and flakes.

Among semiconductor materials, hydrogen-induced blistering was first observed in silicon in mid 1970's [3]. Since then, almost every crystalline material has been shown to blister with a high dose hydrogen implantation and subsequent annealing [4]-[6]. Figure 3.1 shows an example of a blistered silicon surface. In addition, surface ruptures (flakes) are also shown in the figure. With this blistering phenomenon and wafer bonding techniques described in chapter 2, large crystalline silicon layer separation has been demonstrated [7], where a bonded wafer exerts a restoring force for lateral bubble expansion, re-

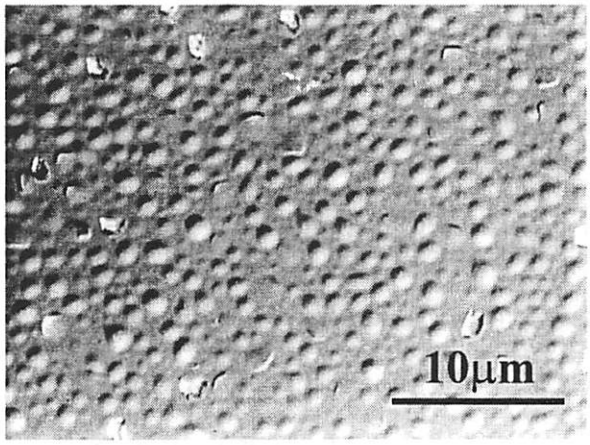


Figure 3.1 Blistered silicon surface with hydrogen implantation (8×10^{16} H^+/cm^2 at 40 keV) and subsequent annealing (450 °C for 20 seconds).

sulting in the whole silicon layer transfer from one wafer to another instead of local flaking.

This chapter reviews the mechanism of blistering in silicon by hydrogen implantation and thermal annealing. It includes defect generation in silicon lattice, hydrogen positions in the lattice, hydrogen-defect interaction, hydrogen gas evolution, bubble coalescence, as well as blistering and flaking models. Also, an attempt has been made to compare single- and poly- crystalline silicon blistering.

3.2 Hydrogen in Silicon

Hydrogen is a quite common (intentionally or unintentionally) impurity in silicon, which has been a discrete topic in solid-state physics and devices. Hydrogen in the environment may diffuse into silicon and passivates electrical activities of both donors and acceptors near the surface. Intentional hydrogenation of poly-silicon can passivate silicon dangling bonds at the grain boundaries, reducing trap states and lowering grain boundary potential barriers. Even though there are several ways of hydrogen incorporation in sili-

con, ion implantation is the most common method reported for silicon layer transfer or blistering experiments, because the hydrogen amount required for blistering is much higher than the solid solubility in silicon (~10^{21} cm^{-3} vs. ~10^{16} cm^{-3}). The ion implantation technique, by bombarding lattice atoms with energetic projectiles and recoiled atoms, creates point defects such as vacancies and interstitials. These vacancies, with hydrogen incorporation, are believed to be precursors for cavities and hydrogen bubble segregation. In this section, models of hydrogen-defect complexes and hydrogen bubble formation reported in the literature will be reviewed. We have also developed a simple model to describe the thermal blistering behavior.

3.2.1 Hydrogen-Related Complexes

Hydrogen atoms can be located in three most probable positions in the silicon lattice: bond center (BC), antibonding (AB), and tetrahedral interstitial (T) sites (see Figure 3.2) [8]. Among those sites, majority of hydrogen atoms are found in BC, while hydrogen molecules (if formed) are found in T. This BC majority implies that hydrogen atoms tend to break Si–Si bonds to form Si–H (silanic) bonds, and the silanic bonds are more stable than Si–Si bonds.

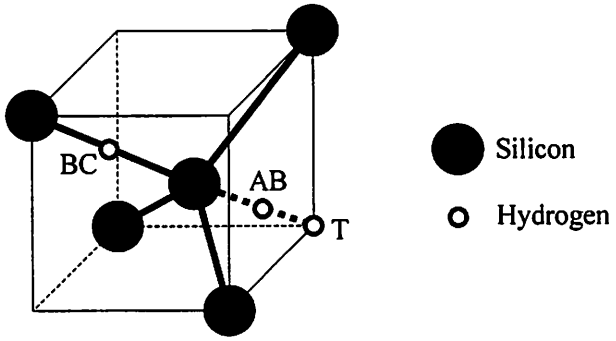
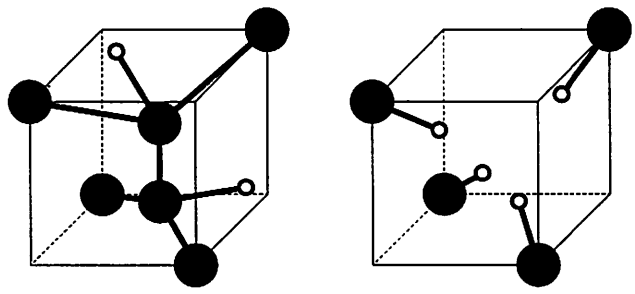


Figure 3.2 Possible hydrogen sites in the silicon lattice: bond center (BC), anti-bond (AB), and tetrahedral interstitial (T) sites.

The H^{BC} (hydrogen atom at BC) react with silicon vacancies and interstitials generated during implantation to form hydrogen-decorated complexes (vacancies or interstitials). These complexes have the form of IH_n or V_mH_n, where I, V, and H stand for silicon interstitial, vacancy, and hydrogen, respectively. m and n are natural numbers. Figure 3.3 illustrates possible structures of frequently observed IH_2 and VH_4 complexes in this study [9], [10]. Depending on the number of H attached to the two split interstitials in Figure 3.3(a) or to the dangling bonds in Figure 3.3(b), n can be 1, 2, 3, or 4 corresponding to an interstitial or a monovacancy (m=1).

3.2.2 Hydrogen-Defect Cluster Formation

For low dose hydrogen implantation, most of hydrogen is expected to be in a BC position, and most of hydrogen-related complexes will be formed after annealing enough for hydrogen to migrate. However, for high doses, when the hydrogen-hydrogen and hydrogen-defect distances are close, hydrogen-decorated vacancy (such as VH_n) clusters and hydrogen dimers will be formed [11]. There have been two identified hydrogen dimers: H_2^* and H_2^T. H_2^* is a close pair of H^{BC} and H^{AB}, and H_2^T is a molecular hydrogen in a T site.



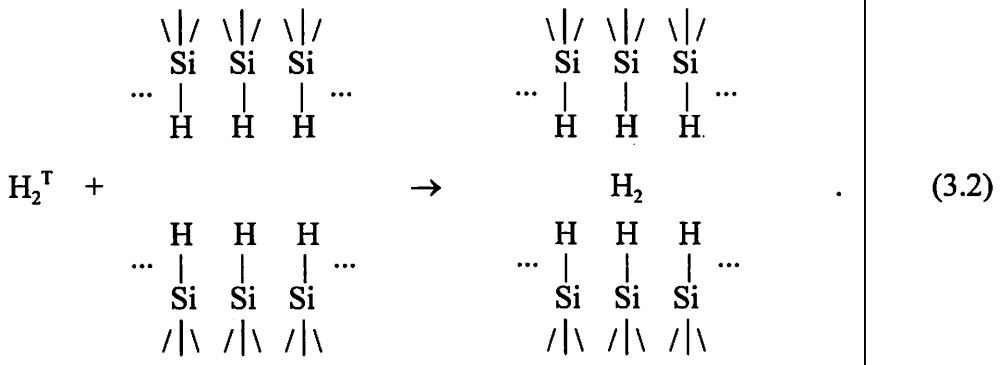
(a) IH_2 (b) VH_4

Figure 3.3 Examples of hydrogen-decorated defects. (a) Two hydrogen atoms are attached to two split interstitials. (b) Four hydrogen atoms are attached to the silicon dangling bonds.

At an elevated temperature between 200-400 °C, Si–H bonds are found to decrease from infrared transmission spectroscopy, while the total amount of hydrogen remains the same from forward recoil scattering [10]. It was assumed that the difference is the production of hydrogen dimers via reaction between Si–H bonds and silicon self-interstitials that can be mobile at the temperature interval [10], [11]:

$$VH_n + I \rightarrow (n/2)\ \{H_2^T \text{ or } H_2^*\}\ . \qquad (3.1)$$

The mobile H_2^T diffuses until it is trapped in large hydrogen-decorated vacancy clusters [11]:



(3.2)

With sufficient feeding of H_2 to the vacancy cluster such as (3.2), an internal surface will eventually form, gradually building up the H_2 pressure [11].

3.3 Silicon Surface Blistering

3.3.1 Blistering Mechanisms and Models

There have been some debates regarding blistering (inter-bubble fracture) mechanisms: gas pressure-driven [12] and lateral stress-driven [13]. The gas-driven model starts with gas pressure estimates inside a bubble using an empirical formula. The bubble grows by the pressure that exceeds the surface tension of the bubble and even the fracture strength of the hosting material. In the stress-driven model, implantation creates a large lateral stress (which is maximum at the ion range), and stress relaxation accounts for the

buckling of a top layer. Since then, more evidences have been observed to confirm the influence of gas pressure and large stress in the hydrogen implanted crystals [15]. For instance, ion-beam channeling showed that hydrogen migrating to the damage peak further distorted the silicon lattice (stress effect), and hydrogen profiling showed that ~50% of hydrogen was lost during flaking of a blister (gas pressure effect) [15]. These observations indicate that both gas pressure and stress can contribute to blistering mechanisms.

Most blistering models reported in literature are based on the hydrogen gas pressure [16]-[19]. These assume the blister as a crack cavity filled with gas [16], or a buckling of a thin film (blister lid) by the pressure inside [18]. Using the Griffith criterion (a necessary condition for crack growth [20]) for the crack cavity [16], or the thin film delamination (which leads to a growth of the blister size) for the blister lid [18], a calculated minimum hydrogen dose (Φ_{min}) for blistering has a form of

$$\Phi_{min} = C\frac{\gamma}{k_B T}, \tag{3.1}$$

where C is a constant between 2~20 depending on a model conditions, and γ is the surface energy required for creating a new surface (maybe 0.5~1 J/m^2 for hydrogen-implanted silicon). k_B and T are Boltzman's constant and the absolute temperature, respectively. The order of minimum dose required for blistering will be

$$O(\Phi_{min}) \approx 10\frac{1[J/m^2]}{10^{-23}[J/K]\cdot 1000[K]} = 10^{16}[cm^{-2}]\ . \tag{3.2}$$

This seems a reasonable estimate, since the minimum hydrogen dose for silicon surface blistering is around 3.5~4.0 × 10^{16} cm^{-2}.

3.3.2 Blister Rupture and Flaking

We attempt to explain the thermal blistering behavior with a simple model. The blister is approximated as a circular plate with a uniform pressure loading (see Figure 3.4). With a hydrogen gas pressure, p, the height of the blister (the maximum deflection of the plate), h, can be expressed as [21]

$$h = \frac{3}{16}\frac{p}{E}(1-\nu^2)\frac{a^4}{d^3}\ , \tag{3.3}$$

where E is the Young's modulus and ν is the Poisson's ratio of silicon. a is the radius of a blister and d is its thickness. The maximum stress occurs at the edge of the blister, and it is given by [21]

$$\sigma_{max} = \frac{3}{4}p\frac{a^2}{d^2}\ . \tag{3.4}$$

If σ_{max} exceeds the fracture strength of silicon, the blister will rupture.

Figure 3.5 shows optical micrographs of flaked surfaces. All three surfaces were hydrogen implanted with a dose of 8×10^{16} H^+/cm^2 at three different energies of 40, 80, and 180 keV, respectively, and annealed at 600 °C for 10 seconds. Comparing the measured dimension of flakes ($2a_{max}$) from the micrographs and the estimated thicknesses of the flakes (d) from the ion projection range in silicon (e.g., SRIM simulation [22]), $2a_{max}$ vs.

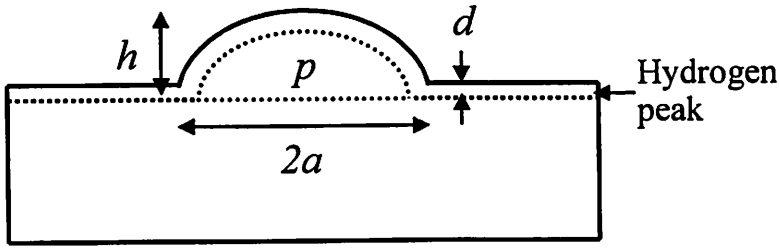
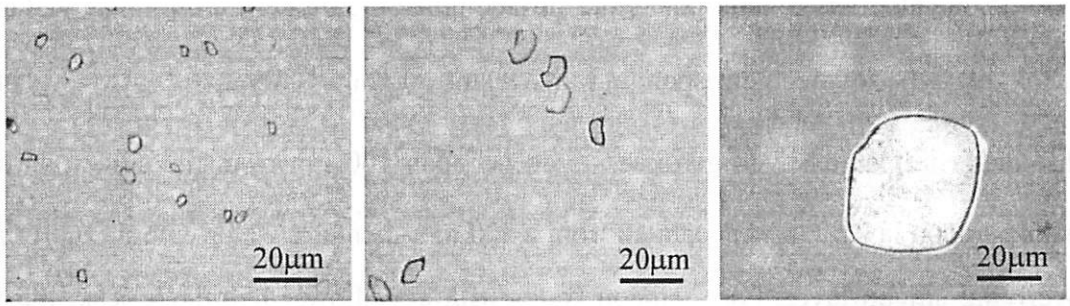


Figure 3.4 A blister model – a uniformly loaded (with pressure, p) circular plate of a diameter, $2a$. The thickness of the plate is d, which is the stopping range of implanted hydrogen.

d can be plotted as in Figure 3.6. $2a_{max}$ was roughly proportional to d^2, and this is consistent with the shearing force balance at the edge of a blister. Using the same geometry in Figure 3.4 and the same model as the uniformly loaded plate, the shearing force balance at the edge of the blister shell is expressed as [21]

$$\pi a^2 p = 2\pi a Q \tag{3.5}$$

where Q is the shear force per unit length of the cylindrical section of radius a. Solving (3.7) for p, and combining it with (3.6) yields



(a) d=0.4μm (b) d=0.7μm (c) d=1.5μm

Figure 3.5 Silicon flake size for three different blister lid thicknesses. All samples were 8× 10^{16} H/cm^2 implanted at (a) 40, (b) 80, and (c) 180 keV, respectively, and annealed at 600 °C for 10 seconds.

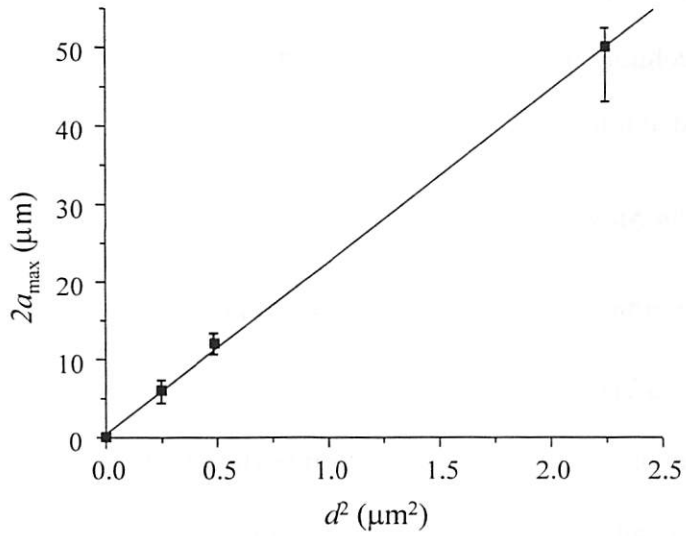


Figure 3.6 Silicon flake size ($2a_{max}$) vs. thickness (d). $2a_{max} \propto d^2$.

$$\sigma_{max} = \frac{3}{4} Q \frac{2a}{d^2} . \quad (3.6)$$

The critical shear force per unit length for bursting blisters (flaking) is then

$$Q_{crit} = \frac{4}{3} \sigma_F \frac{d^2}{2a_{max}} \quad (3.7)$$

where σ_F is the fracture strength of hydrogen implanted silicon. With constant values of Q_{crit} and σ_F in silicon, $2a_{max}$ is proportional to d^2.

If one attempts to extrapolate the surface blistering model for complete wafer layer exfoliation, the d value corresponding to $2a_{max}$ of 300 mm is about 100 μm. This implies that if the implanted hydrogen peak is deeper than 100 μm from the silicon surface, a whole silicon layer can be separated from a 300 mm-diameter wafer without rupturing the overlying silicon layer. For a silicon wafer with a shallower hydrogen peak, the whole layer can be still separated by increasing the top layer thickness by wafer bonding. In this way, the bonded wafer suppresses blister formations from the hydrogen-implanted substrate and lets the hydrogen bubbles grow parallel to the surface. This lateral crack propagation due to the bonded wafer allows layer transfer from one substrate to another. The layer transfer technology using hydrogen implantation and wafer bonding will be discussed more in detail in the next chapter.

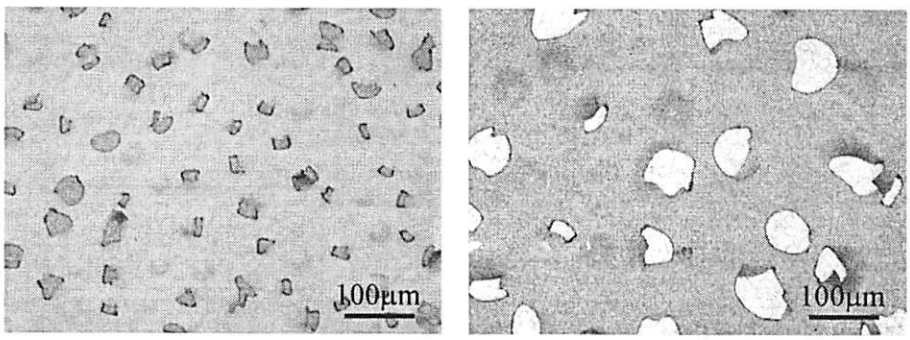
3.3.3 Poly-Silicon Surface Blistering

In this experiment, ~2.2 μm-thick undoped poly-silicon was deposited on two thermally oxidized wafers. Hydrogen was then implanted for both wafers with a dose of 8×10^{16} H^+/cm^2 at an energy of 180 keV. With this energy, the hydrogen peak will be placed at 1.5 μm underneath the wafer surface. After the implantation, one of the wafer surface

was thinned down to about 0.8 μm, re-locating the hydrogen peak at 0.7 μm underneath the new surface. The samples of two different hydrogen depths were then annealed at ~ 500 °C for 10 seconds.

Figure 3.7 shows the blistered poly-silicon surfaces with two different lid thicknesses. Compared with single-crystal silicon in Figure 3.5, the size of blisters and flakes were approximately 2-4 times bigger in poly-silicon (see Figure 3.8). In Figure 3.8, the slopes of the $2a_{\max}$ vs. d^2 plots for both poly- and single- crystalline silicon were approximately the same, implying the similar fracture parameters for both silicon, since the slope can be expressed as $4\sigma_F/3Q_{crit}$ in our blistering model. The discrepancy between the two curves may be attributed to the stress in the poly-silicon introduced possibly during the film deposition and the hydrogen implantation. With a lateral force per unit length, S, (3.7)-(3.9) can be rewritten by replacing Q with Q-S. The critical S for buckling of a circular plate, S_{crit}, can be expressed as [13], [23]

$$S_{crit} \sim \frac{KE}{1-\nu^2}\frac{d^3}{(2a_{\max})^2} \tag{3.8}$$



(a) d=0.7μm (b) d=1.5μm

Figure 3.7 Poly-silicon surface blistering for two different lid thicknesses. The flake sizes in poly-silicon were approximately 2-4 times bigger than single-crystal silicon (see Figure 3.8).

where K is a geometric factor ranging from 1.4 to 4.9 depending on the plate edge conditions such as simply supported or clamped. With this, (3.7) can be modified as

$$Q_{crit} - S_{crit} = Q_{crit} - \frac{KE}{1-\nu^2}\frac{d^3}{(2a_{\max})^2} = \frac{4}{3}\sigma_F \frac{d^2}{2a_{\max}}. \tag{3.9}$$

Solving for $2a_{\max}$ yields

$$2a_{\max} = \frac{2\sigma_F d^2}{3Q_{crit}} + \sqrt{\left(\frac{2\sigma_F d^2}{3Q_{crit}}\right)^2 + \frac{KEd^3}{(1-\nu^2)Q_{crit}}}\ . \tag{3.10}$$

The annealing conditions required for blistering was shorter in time and lower in temperature for poly-silicon. This also distinguishes the layer transfer time and temperature characteristics between poly- and single- crystalline silicon. For a quantitative discussion of this thermally activated process, refer to sections 4.2 and 4.3.

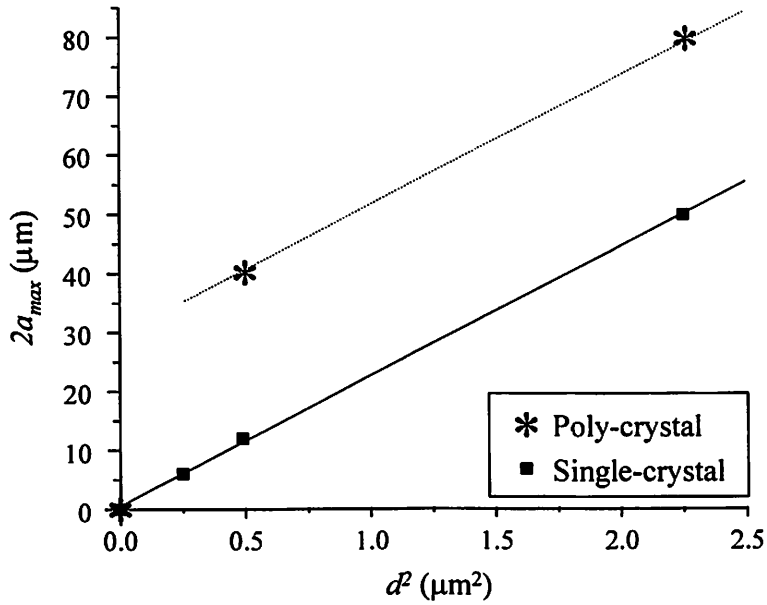


Figure 3.8 Flake size ($2a_{\max}$) vs. thickness (d) for poly-silicon.

3.4 Summary

Literature survey shows the following scenario for thermal blistering of hydrogen-implanted silicon: Due to the hydrogen implantation, silicon vacancies and vacancy clusters are formed. Hydrogen atoms break Si-Si bonds to form Si-H bonds, because they tend to be positioned at Si-Si bond centers. By the reaction between hydrogen and vacancies, hydrogen-decorated vacancies such as (Si-H) – (H-Si) structures are formed. At elevated temperatures, hydrogen molecules are generated through various reaction paths, and diffused into the hydrogen-decorated vacancies. For sufficient build-up of hydrogen molecules, hydrogen bubbles are formed. Due to the gas pressure in the bubble and the integrated lateral stress in the implanted layer, the inter-bubble fracture occurs, resulting in bubble growth.

By modeling blisters as uniformly loaded circular plates, the pressure inside a blister and bursting condition were reasonably estimated from the shape. The flake size was roughly proportional to the thickness squared, suggesting that a large area layer separation is possible with a bonded wafer on top.

Poly-silicon layer was also blistered with hydrogen implantation and subsequent annealing. The flake size was 2~4 times bigger than that of single-crystal silicon for the same lid thickness. Annealing time and temperature required for blistering were shorter and lower, respectively, compared with single-crystal silicon.

References

[1] T. J. Dolan, *Fusion Research*, New York: Pergamon, pp. 706-708, 1982.

[2] S. K. Das and M. Kaminsky, "Radiation blistering in metals and alloys," in *Radiation Effects on Solid Surfaces*, M. Kaminsky, Ed. Washington: American Chemical Society, pp. 112-170, 1976.

[3] E. Ligeon and A. Guivarc'h, "Hydrogen implantation in silicon between 1.5 and 60 keV," *Radiation Effects*, vol. 27, pp. 129-137, 1976.

[4] Q. Y. Tong, K. Gutjahr, S. Hopfe, U. Gösele, and T. H. Lee, "Layer splitting process in hydrogen-implanted Si, Ge, SiC, and diamond substrates," *Applied Physics Letters*, vol. 70, pp. 1390-1392, 1997.

[5] L. J. Huang, Q. Y. Tong, and U. Gösele, "Hydrogen-implantation induced blistering and layer transfer of $LaAlO_3$ and sapphire," *Electrochemical and Solid-State Letters*, vol. 2, pp. 238-239, 1999.

[6] Q. Y. Tong, L. J. Huang, Y. L. Chao, Q. Gang, and U. Goesele, "IOS–a new type of materials combination for system-on-a chip preparation," in *1999 IEEE International SOI Conference Proceedings*, Rohnert Park, CA, 4-7 October 1999, pp. 104-105.

[7] M. Bruel, "Silicon on insulator material technology," *Electronics Letters*, vol. 31, pp. 1201-1202, 1995.

[8] S. J. Pearton, J. W. Corbett, and M. Stavola, *Hydrogen in Crystalline Semiconductors*, Berlin: Springer, pp. 10-25, 1992.

[9] J. L. Hastings, M. Gharaibeh, S. K. Estreicher, and P. A. Fedders, "Hydrogen interactions with intrinsic defects in silicon," *Physica B*, vol. 273-274, pp. 216-219, 1999.

[10] M. K. Weldon, V. E. Marsico, Y. J. Chabal, A. Agarwal, D. J. Eaglesham, J. Sapjeta, W. L. Brown, D. C. Jacobson, Y. Caudano, S. B. Christman, and E. E. Chaban, "On the mechanism of the hydrogen-induced exfoliation of silicon," *Journal of Vacuum Science and Technology B*, vol. 15, pp. 1065-1073, 1997.

[11] G. F. Cerofolini, F. Corni, S. Frabboni, C. Nobili, G. Ottaviani, and R. Tonini, "Hydrogen and helium bubbles in silicon," *Materials Science and Engineering R*, vol. 27, pp. 1-52, 2000.

[12] J. H. Evans, "An interbubble fracture mechanism of blister formation of helium-irradiated metals," *Journal of Nuclear Materials*, vol. 68, pp. 129-140, 1977.

[13] E. P. EerNisse and S. T. Picraux, "Role of integrated lateral stress in surface deformation of He-implanted surfaces," *Journal of Applied Physics*, vol. 48, pp. 9-17, 1977.

[14] W. G. Wolfer, "The role of gas pressure and lateral stress on blistering," *Journal of Nuclear Materials*, vol. 93-94, pp. 713-720, 1980.

[15] S. W. Bedell, *Blistering and Layer Transfer of Hydrogen Implanted Crystals*, Ph.D. dissertation, State University of New York, Albany, NY, pp. 129-145, 2000.

[16] L. B. Freund, "A lower bound on implant density to induce wafer splitting in forming compliant substrate structure," *Applied Physics Letters*, vol. 70, pp. 3519-3521, 1997.

[17] C. M. Varma, "Hydrogen-implant induced exfoliation of silicon and other crystals," *Applied Physics Letters*, vol. 71, pp. 3519-3521, 1997.

[18] L. J. Huang, Q. Y. Tong, T. H. Lee, Y. L. Chao, and U. Gösele, "A model for blistering and splitting of hydrogen implanted silicon and its application to silicon-on-quartz," in *Proceedings of the Eighth International Symposium on Silicon Materials Science and Technology*, San Diego, CA, 4-8 May 1998, pp. 1373-1384.

[19] L. J. Huang, Q. Y. Tong, Y. L. Chao, T. H. Lee, T. Martini, and U. Gösele, "Onset of blistering in hydrogen-implanted silicon," *Applied Physics Letters*, vol. 74, pp. 982-984, 1999.

[20] T. L. Anderson, *Fracture Mechanics*, 2nd ed., Boca Raton, FL: CRC, 1995, pp. 36-46.

[21] S. Timoshenko and S. Woinowsky-Krieger, *Theory of Plates and Shells*, 2nd ed., New York: McGraw-Hill, 1959, pp. 54-58.

[22] J. F. Ziegler and J. P. Biersack, *SRIM (the Stopping and Range of Ions in Matter) – 2000 Program*, IBM Research, Yorktown, NY, 1999.

[23] S. Timoshenko and S. Woinowsky-Krieger, *Theory of Plates and Shells*, 2nd ed., New York: McGraw-Hill, 1959, pp. 391-393.

Chapter 4

ION-CUT SILICON LAYER TRANSFER

Abstract- In this chapter silicon-on-insulator (SOI) technology is introduced, and the ion-cut silicon layer transfer process is described for fabricating SOI structures. The layer transfer technology has been made possible by combining both wafer bonding and hydrogen-induced silicon layer cleavage. In this process, a hydrogen-implanted wafer was bonded to another non-implanted wafer. By appropriate heat treatment, the bonded wafer pair separates along the hydrogen peak, resulting in the transfer of a semiconductor layer from one wafer to another. The bonded wafer acted as a stiffener for the blisters, and made the hydrogen bubbles grow laterally and thus the crack propagates in the plane, instead of bulging up toward wafer surface. With this technique, we have been able to fabricate SOI wafers with good thickness uniformity (< 0.3%) and surface micro-roughness (< 10 nm RMS as-cut). Ion-cut layer transfer was also achieved using plasma immersion ion implantation (PIII) of hydrogen in place of a conventional beam-line implanter. In addition to the thermal cleavage process, mechanical cleavage methods were introduced for the potential use of the ion-cut layer transfer process to glass or plastic substrates where a low-temperature process is required.

4.1 Introduction

4.1.1 SOI Technology

An SOI wafer refers to a layered structure consisting of a relatively thin single-crystal silicon layer either atop an insulating substrate (e.g., quartz, sapphire, etc.), or isolated from a bulk silicon substrate by an insulating layer (typically, silicon dioxide). Figure 4.1 illustrates the cross-sections of the two SOI structures described above and a bulk silicon

wafer used in semiconductor industry currently. The top silicon layer is often called the silicon overlayer, and this is where electronic devices are built. Since there are thermal process limitations because of the different thermal expansion coefficients between two materials in the structure depicted in Figure 4.1(a), it has largely been replaced by the structure of Figure 4.1(b). The silicon dioxide layer between the silicon overlayer and the bulk silicon substrate is called buried oxide, or BOX [see Figure 4.1(b)].

In SOI, unlike bulk silicon [Figure 4.1(c)], and therefore the top silicon device layer is electrically isolated from the silicon substrate, there is a significant reduction of parasitic p-n junction capacitances and leakage currents through the substrate. This capacitance and leakage reduction directly contributes to a higher speed of operation and to lower power consumption, which are critical, particularly in mobile electronics. SOI is also well suited for space electronics, since photocurrents induced by ionizing radiation are reduced by substrate isolation. The isolation layer also eliminates latch-up (parasitic bipolar device formation with the substrate) and simplifies the process of isolating devices from one another, thus leading to smaller circuit sizes than in bulk silicon counterparts [1], [2]. Structurally, the BOX layer serves as an etch stop in the patterning of silicon waveguides [3] and the fabrication of sensor membranes or three-dimensional structures [4].

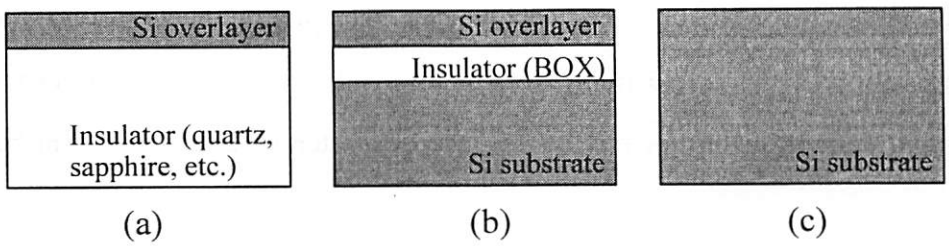


Figure 4.1 SOI structures and bulk silicon. (a) Silicon on insulating substrate. (b) Silicon on insulating layer. (c) Bulk silicon substrate.

4.1.2 SOI Fabrication

There are a variety of methods for the fabrication of SOI structures. Some are designed to produce a thicker (10~100 μm) silicon overlayer, others to produce a thinner (0.01~1 μm) one. For this thinner case, uniform thickness and high quality silicon are essential.

Separation by implantation of oxygen (SIMOX) has been the most widely used method for SOI fabrication. In this process, a high dose (~10^{18} cm^{-2}) of oxygen ions are implanted at energies on the order of 100 keV depending on the desired BOX depth. The wafer is then annealed at a temperature over 1300 °C for several hours to allow for the formation of silicon dioxide for BOX [5].

Silicon can be deposited and grown on a crystal such as sapphire to form a structure like Figure 4.1(a). In this technique, the lattice mismatch between sapphire and silicon crystals produces poor silicon quality [6]. This problem can be overcome with wafer bonding and etch-back or ion-cut layer transfer processes as explained below.

In the bonding and etch-back process [7], two silicon wafers with oxide surfaces are bonded together, face to face, at room temperature and annealed above 800 °C to strengthen the bond. One side of the bonded pair is then ground, etched, polished, and so forth to get a desired silicon overlayer thickness. This method is good for thick SOI that has applications in power electronics and micro-mechanics. For precise thickness control, wafers with doped layers for etch stops, or special etching chemistries can be used [8], [9].

By combining both wafer bonding and hydrogen-induced delamination as described in the previous chapters, a whole layer of silicon can be cleaved and transferred from one

wafer to another, forming SOI structures. This technique is called ion-cut layer transfer in general. Figure 4.2 shows the sequence of SOI fabrication using a thermal cleavage process. In this process, one of the two wafers is implanted with a high dose (~10^{17} cm^{-2}) of hydrogen before bonding. After the bonding, the bonded pair is heated until layer separation occurs, resulting in SOI structure formation [10]. Without the bonded wafer, the hydrogen bubbles will begin to bulge up when the pressure reaches a critical value to deform or fracture the silicon overlayer [Figurer 4.3(a)]. However when a bonded wafer is on top of the hydrogen implanted silicon wafer, the bonded wafer exerts vertical stiffening force to the bubbles forcing lateral expansion [Figure 4.3(b)].

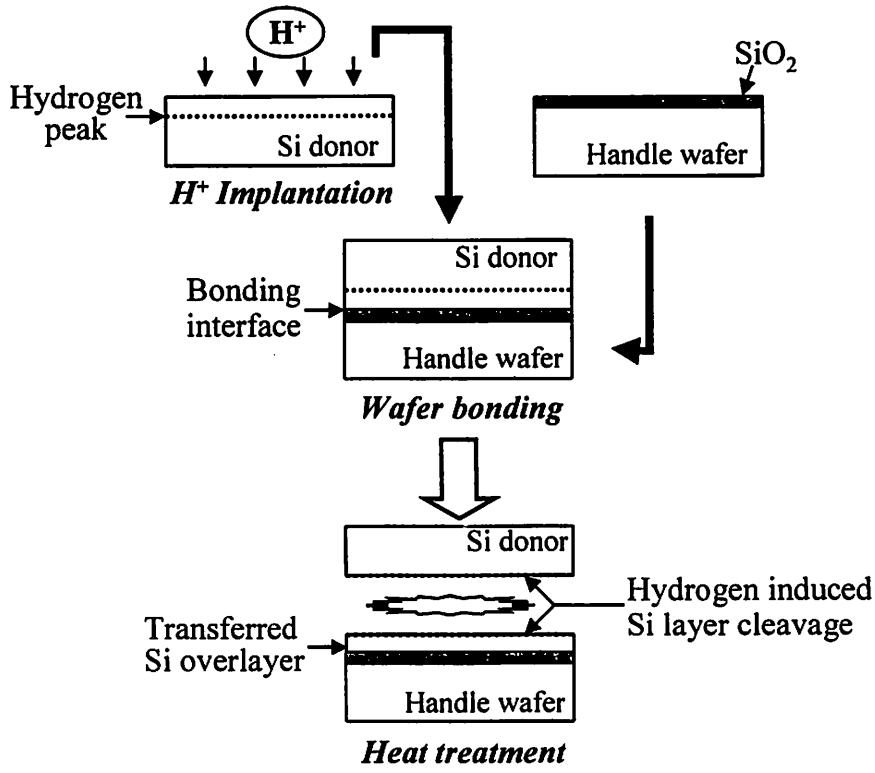


Figure 4.2 Ion-cut silicon layer transfer process with a thermal cleavage method.

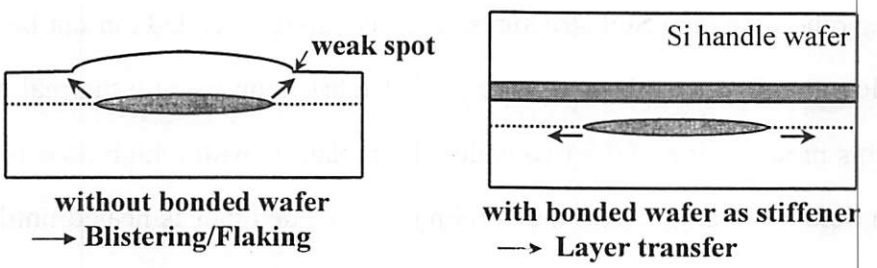


Figure 4.3 Comparison between blistering and layer transfer. (a) Without the bonded wafer, the hydrogen bubbles bulge up when the pressure reaches a critical value to deform or fracture the silicon overlayer. (b) When a bonded wafer is on top of the hydrogen implanted silicon wafer, the bonded wafer exerts vertical stiffening force to the bubbles forcing lateral expansion.

4.2 Thermal Cleavage for Ion-Cut Silicon Layer Transfer

In this study, CZ-grown, boron-doped p-type wafer with a resistivity of 30-60 Ω·cm, silicon (100) were used. The bare silicon wafers were implanted with two different doses of 5×10^{16} or 8×10^{16} H^+ ions/cm^2 at energies of 40 or 80 keV. For the silicon handle wafers, a 100 nm-thick SiO_2 layers were grown in a thermal oxidation furnace. The implanted donor and oxidized handle wafers were then bonded directly, face-to-face at room temperature after a standard RCA cleaning and an oxygen plasma surface treatment. The bonding interface was cured at 200 °C for ~10 hours. The bonded pair was then heated in a halogen lamp heater until the hydrogen induced silicon layer cleavage occurred. This ion-cut process enables the silicon layer transfer from the silicon donor wafer to the handle wafer (see Figure 4.2).

Figure 4.4 shows a scanning electron micrograph (SEM) and an atomic force micrograph (AFM) of the as-transferred silicon layer on top of the handle wafer. The transferred surface was a mirror-like finish as-cleaved, and the SEM also confirmed the smooth surface. The root-mean-squared (RMS) surface roughness was 5.1 nm, and peak-

to-valley was 38 nm over the 2 μm × 2 μm scanned region. The donor wafer in this case was implanted with a dose of 8×10^{16} H^+/cm^2 at 80 keV, and there was no noticeable difference in the surface morphology between the two different energies, but 10~20 % reduction in RMS roughness for the higher dose.

The thickness of the transferred layer was measured to be 667 nm average across a 100 mm wafer (see Figure 4.5), and the thickness uniformity across the wafer was better than 1% (within ±3 nm). Since the silicon layer cleavage is believed to occur at the depth corresponding to the peak concentration of the hydrogen implantation profile [10], and the hydrogen peak position is determined by the ion implantation energy, the silicon thickness can be predicted according to the hydrogen ion energy. The depth profile of hydrogen ions in silicon can be simulated with the aid of the SRIM 2000 program [11]. In general, the transferred layer thickness is closer to the silicon lattice damage (vacancy) peak rather than hydrogen concentration peak in the simulation. Table 4.1 compares the simulated hydrogen and damage peaks, and the actual thickness of the transferred layer from the 40, 80, and 180 keV H^+ implanted silicon donor wafers. The actual thickness was within 5% of the damage peak, and showed ~10% difference with respect to the hydrogen peak.

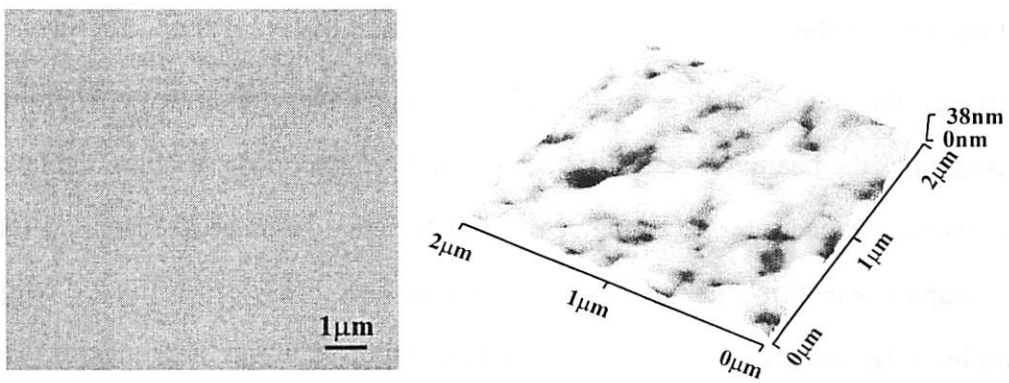


Figure 4.4 SEM and AFM of the transferred silicon layer surface. The surface was a mirror-like finish as-cleaved. The RMS surface roughness was 5.1nm.

Table 4.1 Comparison between simulated peaks and actual thickness

Energy	Hydrogen peak	Damage peak	Actual thickness
40 keV	0.48 μm	0.42 μm	0.44 μm
80 keV	0.77 μm	0.68 μm	0.67 μm
180 keV	1.58 μm	1.52 μm	1.53 μm

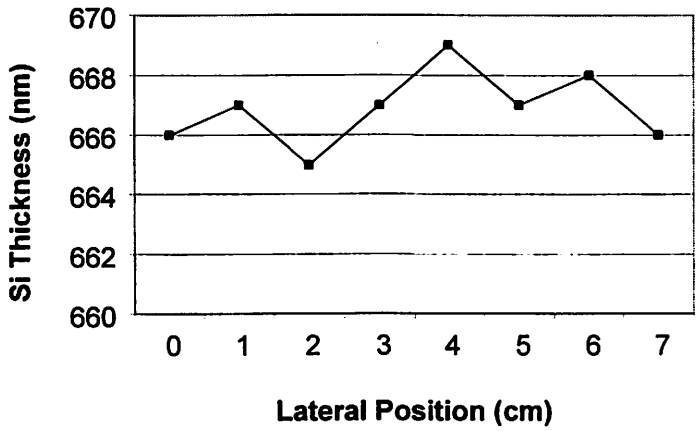


Figure 4.5 Transferred silicon layer thickness across a wafer. The average thickness is 667nm. The thickness uniformity of the wafer was better than 1%. The sample was implanted with 8×10^{16} H^+/cm^2 at 80 keV.

Figure 4.6 shows the Arrhenius plot of the silicon layer transfer time (t) vs. temperatures (T) for the two different doses of 5×10^{16} and 8×10^{16} H^+/cm^2. The layer transfer time means the annealing time required to split silicon layers at various temperatures, and it increased as the heating temperature decreased. For lower dose samples, the layer transfer times were longer at a given temperature. The activation energy decreased for higher dose samples, which means the layer transfer time becomes less sensitive to temperature for higher dose samples. The activation energies reported in the literature vary from 0.5-2.5 eV for different doses, temperature ranges, bonding recipes, etc. [12]-[14].

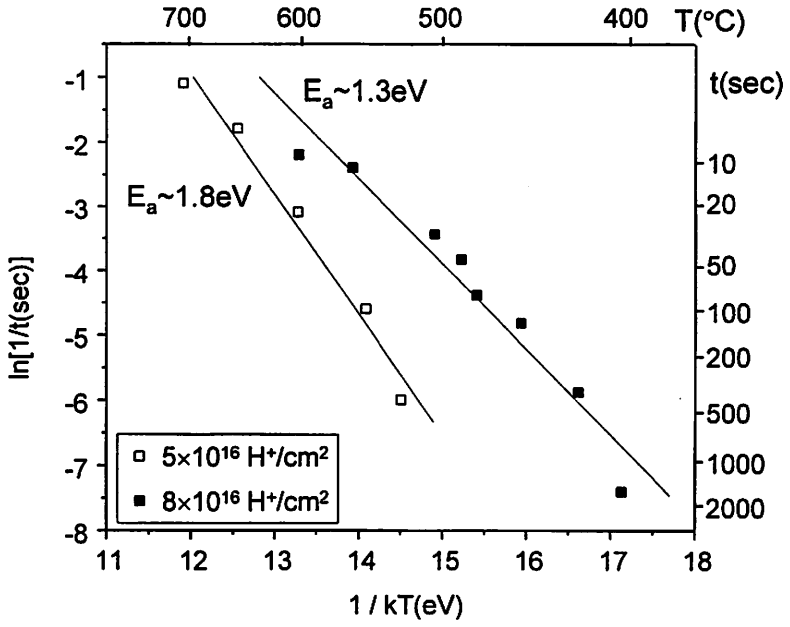


Figure 4.6 Arrhenius plot of silicon layer transfer time vs. temperature. The layer transfer times decreased as the heating temperature decreased. For lower dose samples, the layer transfer times were longer at a given temperature.

4.3 Thermal Cleavage for Polycrystalline-Silicon Layer Transfer

In subsection 2.3.3, a poly-silicon wafer was directly bonded to another substrate after chemical-mechanical polishing of the surface, and in subsection 3.3.3, hydrogen-implanted poly-silicon wafer surface blistered after high temperature annealing. The bonding ability and blistering phenomenon means a good chance for layer transfer. Motivated by these promising results, poly-silicon layer transfer was demonstrated and will be described in this section.

Figure 4.7 illustrates the process flow for poly-silicon layer transfer. After hydrogen implantation with 8×10^{16} H^+/cm^2 of dose at 180 keV of energy, the implanted poly-silicon layer was chemically-mechanically polished. The polished wafer was then bonded to an

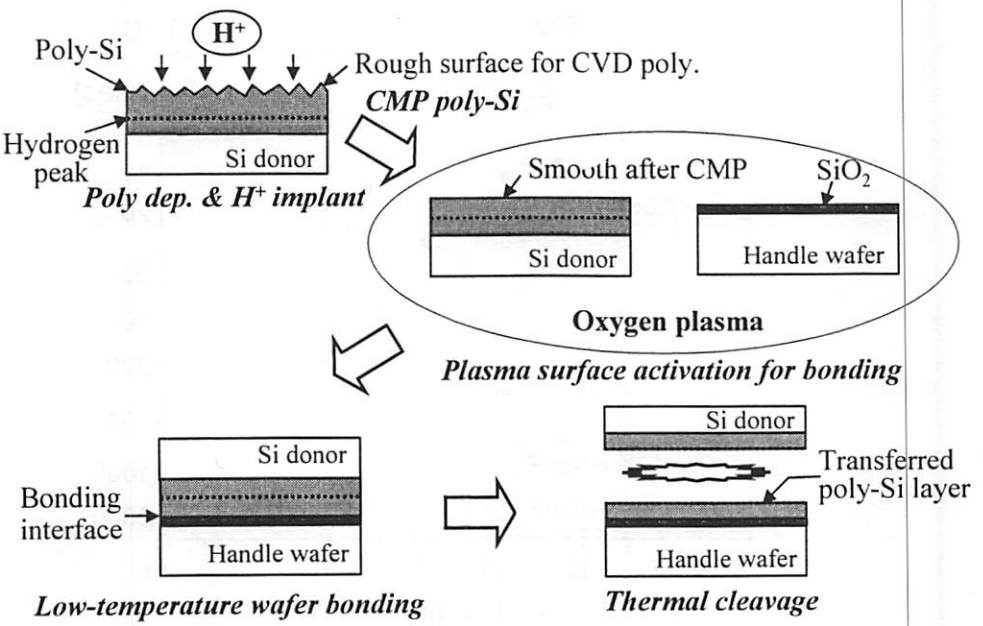


Figure 4.7 Poly-silicon layer transfer process. After hydrogen implantation to the CVD poly-Si, the wafer was CMP'ed. The polished wafer was then bonded to an oxidized wafer the same way as described in the previous section.

oxidized wafer the same way as described in the previous section. The bonded pair was then placed in a lamp heater (rapid thermal annealing) to cut across the poly-silicon layer.

The poly-silicon layer was successfully transferred to another substrate. Figure 4.8 shows an AFM scan over 2 μm × 2 μm area of the transferred poly-silicon layer surface. The root-mean-square (rms) roughness was 4.2 nm, and the peak-to-valley was 40 nm in the area. The values are about the same as the transferred single-crystalline silicon layer (see Figure 4.4).

Figure 4.9 shows the Arrhenius plot of the layer transfer time vs. annealing temperature. Comparing this with single-crystalline silicon, the cleavage time was significantly decreased. Moreover, the cracking activation energy was reduced by an order of magnitude. The extracted value of 0.17 eV is much lower than all reported activation energies for single-crystal silicon.

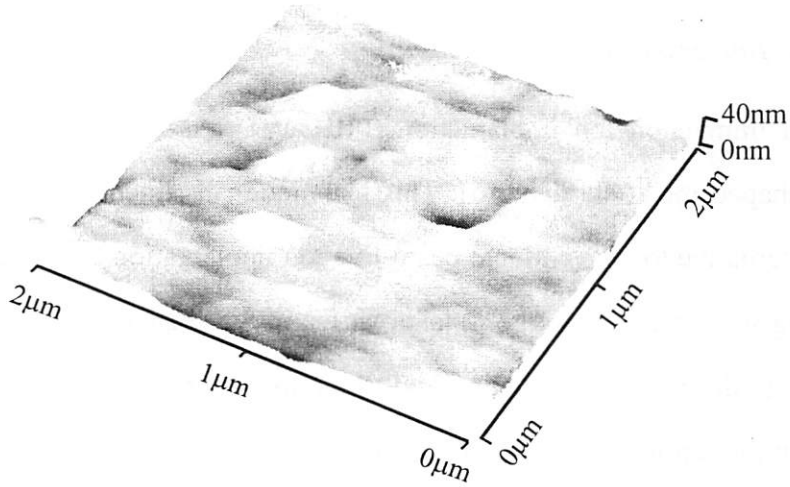


Figure 4.8 Transferred poly-silicon layer surface (AFM scan). The RMS roughness was 4.2 nm, which is about the same as the transferred single-crystal silicon.

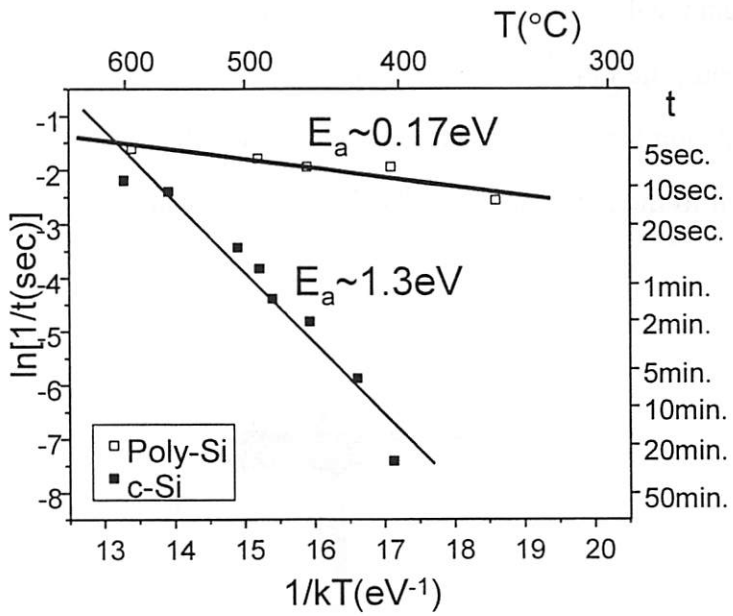


Figure 4.9 Poly-silicon layer transfer time vs. temperature. Comparing with single-crystal silicon, the cleavage time was significantly decreased. Moreover, the cleavage activation energy was reduced by an order of magnitude.

4.4 Ion-cut with Plasma Immersion Ion Implantation of Hydrogen

4.4.1 Plasma Immersion Ion Implantation

Plasma immersion ion implantation (PIII) was first introduced for nitridation of irregularly shaped metal surface [15]. This technique was intended as a high dose rate, large area alternative to conventional beam-line ion implantation as well as being capable of implanting work-pieces with non-planar surfaces. Subsequently, this method has been applied to high dose rate implantation and to the low-energy shallow junction-depth implantations in the semiconductor industry [16], [17].

Figure 4.10 illustrates the principle of PIII. In PIII, the target (wafer) is immersed in plasmas containing the desired ions to be implanted. By applying a negative bias to the target, electrons will be repelled away near the target surface and a region of positive ions called the sheath will be established [18]. Since almost all the applied voltage drops across the sheath, the ions in the sheath are accelerated and implanted into the target. If there is no collision between the species in the sheath, the ions will acquire the full kinetic energy equal to the potential drop. The bias voltage can be dc, ac, or pulsed. However

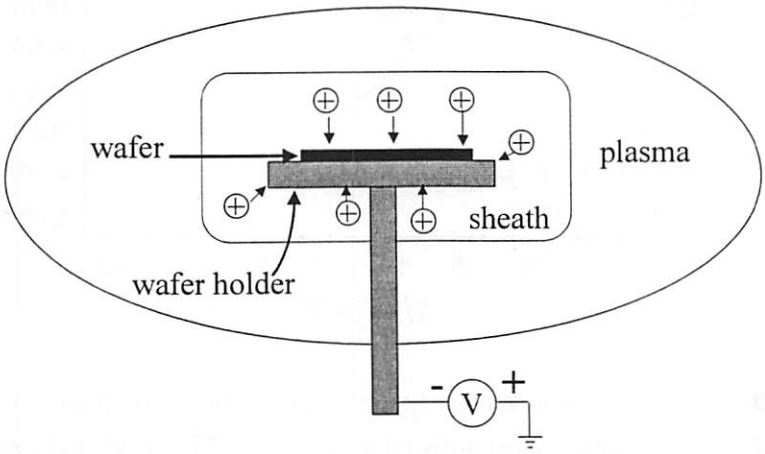


Figure 4.10 Principle of plasma immersion ion implantation. When a negative bias is applied to the target, the sheath is formed around the target. Ions are accelerated across the sheath, and implanted into the wafer.

for a dielectric substrate, pulsed operation is necessary to avoid dielectric breakdown or stressing. When the wafer bias is turned off, electrons from the plasma collapse the sheath region and neutralize the accumulated surface charge.

A main advantage of PIII is that the entire wafer surface is implanted simultaneously unlike ion-beam scanning in a conventional beam-line implanter. Hence, high wafer throughput is achieved independent of the wafer size. However, since there is no mass separation unit in the PIII system, all ion species in the plasma will be implanted into the target simultaneously during the negative bias. Also, precise dose control of the implanting species is a major challenge.

4.4.2 Hydrogen PIII

In the hydrogen plasma, three ions (H^+, H_2^+, and H_3^+) are present. In PIII, since there is no ion mass selection tool, all three ions will be implanted. These ion species have different projected depth profile in the target, creating a multiple peaked and broadened hydrogen distribution. For the ion-cut process application of the hydrogen PIII, the presence of multiple peaks of the hydrogen depth profile may initiate cracks at different depth, resulting in the non-uniformity of transferred film thickness and defective film quality.

In this experiment, the hydrogen plasma was generated by electron cyclotron resonance heating [19]. From the chamber base pressure of 1.0×10^{-6} Torr (1.3×10^{-4} Pa), the chamber pressure was sustained at 0.29 mTorr with the hydrogen flow rate of 7.7 sccm (cm^3/min at standard temperature and pressure). The net microwave power was 290 W (300 W forward and 10 W reflected) at a frequency of 2.45 GHz. The hydrogen plasma was confined in the source by a magnetic cusp configuration with a magnetic coil current of 260 A [20]. The target wafer was biased at -12 kV for implantation. The implantation time was 15 minutes and current into the target was monitored to be 60-120 mA.

With the similar condition to the above, the compositional ratio of H^+, H_2^+, and H_3^+ was measured to be around 21:70:8 [21]. If we approximate the hydrogen depth profile in silicon as a Gaussian, the hydrogen density, *n(x)*, at the depth *x* from the target surface will be expressed as the following [22]:

$$n(x) = \sum_{i=1}^{3} \frac{\Phi^i}{\sqrt{2\pi}\Delta R_p^i} \exp\left[-\frac{(x - R_p^i)^2}{2(\Delta R_p^i)^2}\right] \tag{4.1}$$

where the superscript *i* describes the three different ion species, H^+, H_2^+, and H_3^+. The projected range, R_p, is equal to the average distance an ion travels before it stops, and the straggle, ΔR_p, is the standard deviation characterizing the spread of the distribution. With 12 keV of implantation energy, the projected range and the straggle of each ion species can be obtained using TRIM simulation, and Table 4.2 summarizes the result [11]. Φ^i is the hydrogen dose contribution by *i*th ion, and it can be related to the implantation current monitored, *I*:

$$\Phi^i = \frac{NfIt}{eA(1+\gamma_i)} \tag{4.2}$$

where *N* is the average number of hydrogen atoms produced per implanted ion. For example, there will be three hydrogen atoms per H_3^+. *f* is the fraction of each implanted ion species, *t* is the implantation time, *e* is the unit charge, and *A* is the total wafer holder area exposed to plasma. γ_i represents the secondary electron emission coefficient, defined as the average number of electrons emitted per incident ion. In this experiment, the implantation current was 60 mA for 15 minutes. If γ_i is assumed to be 3.5 for all three species [23], [24], we can plot the distribution of each ion and the total hydrogen distribution. Figure 4.11 shows the simulated hydrogen distribution in a silicon target. The distribution is dominated by H_2^+ ions as expected, since H_2^+ is the most dominant species in the plasma condition described above.

Table 4.2 Simulated stopping ranges and straggles for three hydrogen ions at 12keV

Ion species	R_p (Å)	ΔR_p (Å)
H^+	1975	797
H_2^+	1066	584
H_3^+	729	472

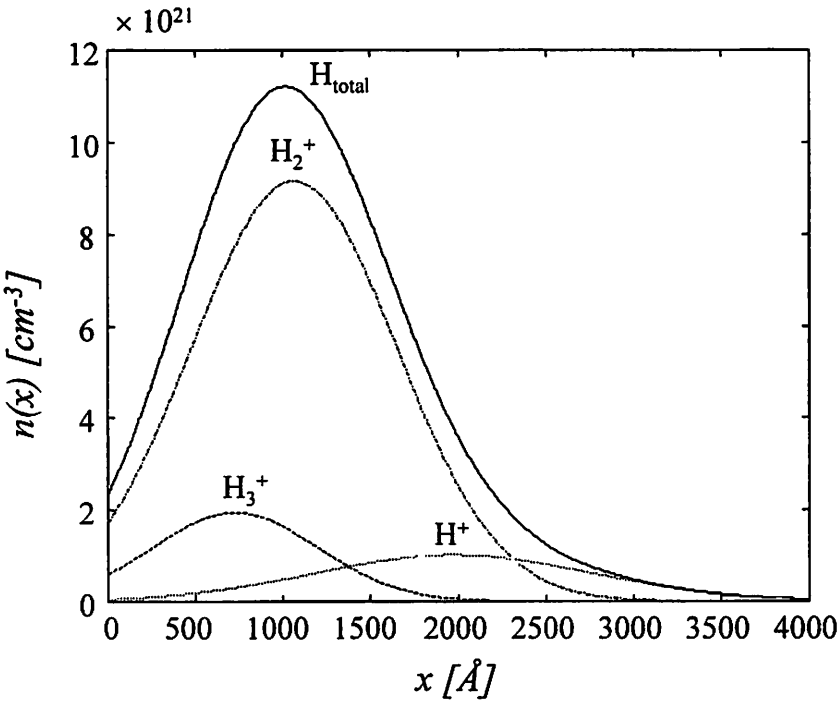


Figure 4.11 Simulated hydrogen profile in silicon. The profile was obtained from (4.1) with data from Table 4.2 and an estimated total dose of 1.4×10^{17} cm^{-2}.

4.4.3 Ion-Cut with Hydrogen PIII

The hydrogen plasma-implanted sample described in subsection 4.4.2 was bonded to an oxidized silicon handle wafer after cleaning in piranha (H_2SO_4 and H_2O_2 mixture) and RCA1 (NH_4OH, H_2O_2, and H_2O mixture) solutions. The bonding interface was further cured at 200 °C for ~10 hours. The bonded pair was then placed in a lamp heater un-

til hydrogen-induced silicon layer cleavage occurred. The layer transfer temperature was 550 °C in less than 10 seconds, from which the implantation dose can be empirically deduced as ~1 × 10^{17} H/cm^2. This experimental dose is lower than the simulation result of 1.4 × 10^{17} H/cm^2 as shown above, and it may be caused from the roughly estimated value of secondary electron emission coefficient, γ, in the calculation.

The transferred silicon layer thickness was ~110 nm, which was close to the simulated depth of the implanted hydrogen peak (see Figure 4.11). Figure 4.12 shows an AFM micrograph of the transferred silicon layer. The surface micro-roughness of the 2 μm × 2 μm scanned region was 4.1 nm rms, which is ~20 % smoother than the ion-cut surface with conventionally implanted silicon samples described in section 4.2. This may be due to the hydrogen dose difference between the conventionally and plasma implanted samples, and it is known that the roughness decreases as the dose increases [25].

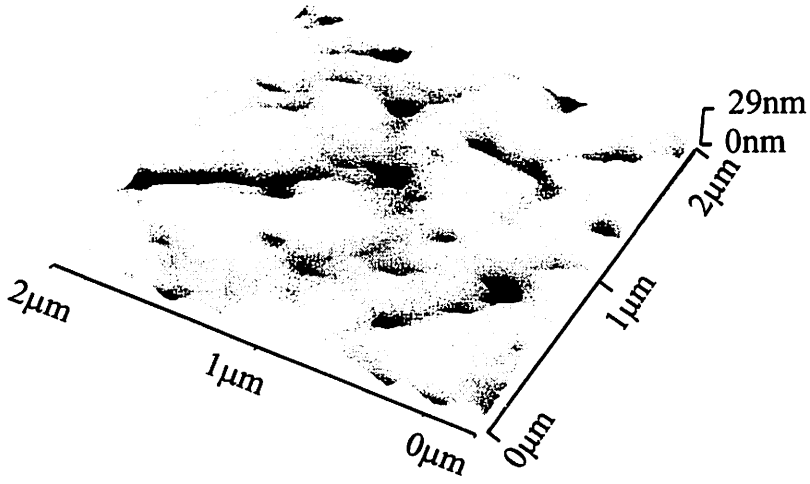


Figure 4.12 Transferred silicon layer by ion-cut with plasma implantation of hydrogen. The nominal hydrogen dose was ~1.0 ×10^{17} cm^{-2}. The RMS surface roughness was 4.1 nm.

4.5 Mechanical Cleavage of Hydrogen Implanted Silicon

For layer transfer of heterogeneous systems, it is desirable to keep the cleaving temperature as low as possible to minimize thermal expansion coefficients mismatch between thin films and substrates (e.g., silicon on glass).

In this experiment, the same wafers and bonding processes described in section 4.2 were used. After wafer bonding and curing at 200 °C, a crack-opening force was applied to the bonded pair either by inserting a solid wedge between the wafer pair [Figure 4.13 (a)] or by applying a torque from each side of the pair [Figure 4.13(b)]. Using these mechanical separation methods, a silicon layer was successfully transferred from a donor wafer to a handle wafer. Figure 4.14 shows an AFM of a transferred layer. Comparing this with Figure 4.4 for a thermally cleaved surface, the mechanically cleaved surface was a little smoother (~10 % or ~0.5 nm in RMS roughness). The transferred layer thickness was the same for both thermal and mechanical separation. Aside from solid wedge (see also [26]) or mechanical bending as shown in this section, there is also a method using a high-pressure gas jet to separate the bonded pair [27].

The reason mechanical splitting is possible can be explained in terms of surface energy. In a bonded pair with a hydrogen implanted donor wafer, two interfaces can be defined: the bonding interface and the damage peak (see Figure 4.14). In chapters 2 and 3, it was shown that the bonding interface could be stronger than the silicon lattice, and that the damage peak [(Si-H) – (Si-H) bond] was weaker than silicon lattice (Si–Si bond), respectively. Therefore, when there is an external force applied to the bonded wafer pair, the separation will occur along the weakest plane – the implanted damage peak, resulting in the layer transfer from one wafer to another.

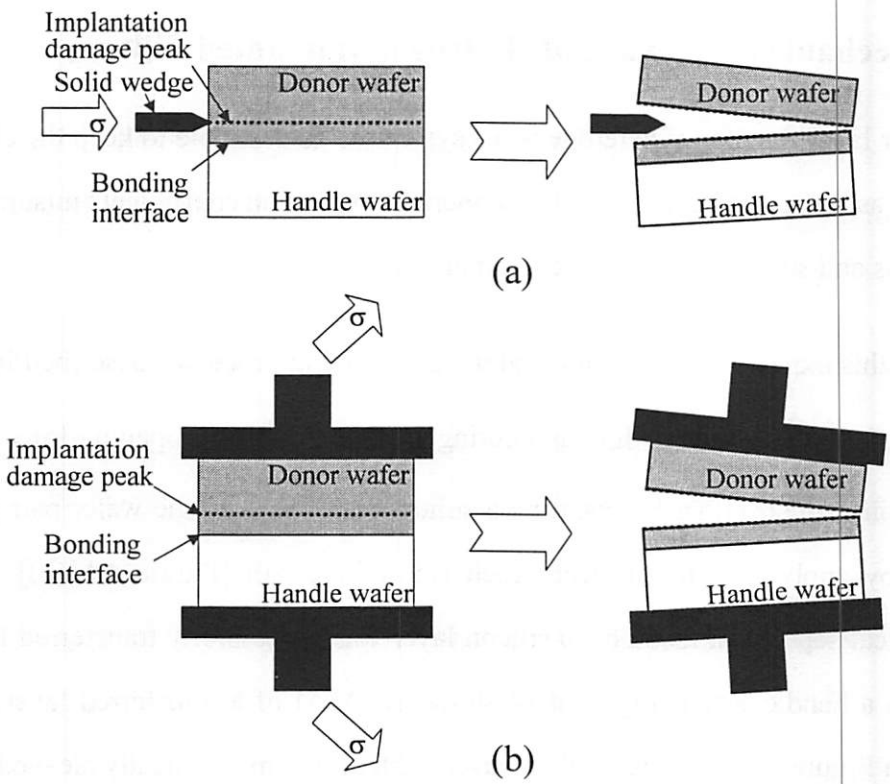


Figure 4.13 Mechanical cleavage methods. A crack-opening force can be applied to the bonded pair (a) by inserting a solid wedge between the wafer pair or (b) by applying a torque from each side of the pair.

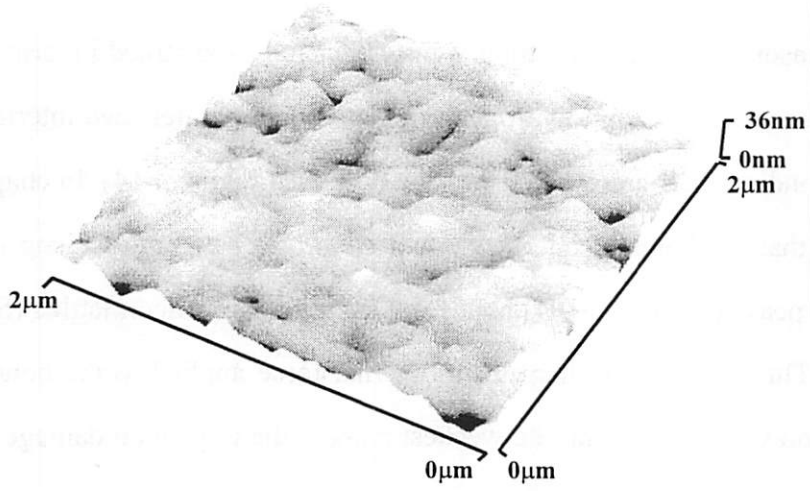


Figure 4.14 Mechanically cleaved silicon surface. The transferred layer thickness was ~670nm, and RMS surface roughness was 5.1nm.

4.6 Summary

Ion-cut was demonstrated for single and poly- crystalline silicon layer transfer. The thickness uniformity of the transferred layer was within 0.3 % over a 100 mm diameter wafer surface, and the RMS micro-surface roughness of the layer was better than 10 nm for all the implantation doses and energies attempted. The layer transfer time was found to be less sensitive to temperature as the hydrogen dose increased. For poly-silicon layer transfer, the layer transfer time was significantly reduced from that of single-crystal silicon, and was not very sensitive to temperature for temperatures greater than 350 °C. The layer transfer activation energy was almost 10 times smaller than that of its single-crystal counterpart.

Ion-cut was also successful with plasma immersion ion implantation of hydrogen, which has a higher implantation rate compared with conventional beam-line implanters. Even though there are three ion species (H^+, H_2^+, and H_3^+) in the hydrogen plasma, it was shown that the hydrogen-induced silicon cleavage followed the peak of the most dominant species.

Mechanical splitting was demonstrated for low-temperature process applications. Mechanical cleavage was only possible when the wafer bonding is stronger than the hydrogen-induced silicon damage peak, (Si-H) – (Si-H) bond.

References

[1] M. L. Alles, "Thin-film SOI emerges," *IEEE Spectrum*, vol. 34, no. 5, pp. 37-45, June 1997.

[2] J. P. Colinge, *Silicon-on-Insulator Technology: Material to VLSI*, 2nd ed., Kluwer Academic: Boston, 1997, pp. 1-5.

[3] M. Naydenkov and B. Jalali, "Advances in silicon-on-insulator photonic integrated circuit (SOIPIC) technology," in *1999 IEEE International SOI Conference Proceedings*, Rohnert Park, CA, 4-7 October 1999, pp. 56-62.

[4] G. T. A. Kovacs, N. I. Maluf, and K. E. Petersen, "Bulk micromachining of silicon," *Proceedings of IEEE*, vol. 86, pp. 1536-1551, 1998.

[5] K. Izumi, "History of SIMOX material," *MRS Bulletin*, vol. 23, no. 12, pp. 20-24, December 1998.

[6] S. Cristoloveanu, "Silicon films on sapphire," *Reports on Progress in Physics*, vol. 50, pp. 327-371, 1987.

[7] J. B. Lasky, S. R. Stiffler, F. R. White, and J. R. Abernathy, "Silicon-on-insulator (SOI) by bonding and etch-back," in *IEEE International Electron Device Meeting Technical Digest*, Washington, DC, 1-4 December 1985, pp. 684-687.

[8] B. Kloeck, S. D. Collins, N. F. DeRooij, and R. L. Smith, "Study of electrochemical etch-stop for high precision thickness control of silicon membranes," *IEEE Transactions on Electron Devices*, vol. 36, pp. 663-669, 1989.

[9] J. W. Neuner, A. M. Ledger, S. K. Schilb, and D. P. Mathur, "Improved uniformity in bonded SOI wafers with active layers from 1 to 30 μm at high throughputs," in *1998 IEEE International SOI Conference Proceedings*, Stuart, FL, 5-8 October 1998, pp. 169-170.

[10] M. Bruel, "Silicon on insulator material technology," *Electronics Letters*, vol. 31, pp. 1201-1202, 1995.

[11] J. F. Ziegler and J. P. Biersack, *SRIM (the Stopping and Range of Ions in Matter) – 2000 Program*, IBM Research, Yorktown, NY, 1999.

[12] Q. Y. Tong, K. Gutjahr, S. Hopfe, U. Gösele, and T. H. Lee, "Layer splitting process in hydrogen-implanted Si, Ge, SiC, and diamond substrate," *Applied Physics Letters*, vol. 70, pp. 1390-1392, 1997.

[13] B. Aspar, C. Lagahe, H. Moriceau, A. Soubie, and M. Bruel, "Kinetics of splitting in the Smart-Cut® process," in *1998 IEEE International SOI Conference Proceedings*, Stuart, FL, 5-8 October 1998, pp. 137-138.

[14] S. W. Bedell, *Blistering and layer transfer of hydrogen implanted crystals*, Ph.D. dissertation, State University of New York, Albany, NY, 2000, pp. 36-57.

[15] J. R. Conrad, J. L. Radtke, R. A. Dodd, F. J. Worzala, and N. C. Tran, "Plasma source ion-implantation technique for surface modification of materials," *Journal of Applied Physics*, vol. 62, pp. 4591-4596, 1987.

[16] N. W. Chueng, "Plasma immersion ion implantation for ULSI processing," *Nuclear Instruments & Methods in Physics Research B*, vol. 55, pp. 811-820, 1991.

[17] P. K. Chu, S. Qin, C. Chan, N. W. Cheung, and L. A. Larson, "Plasma immersion ion implantation – a fledging technique for semiconductor processing," *Materials Science and Engineering*, vol. R17, pp. 207-280, 1996.

[18] M. A. Lieberman and A. J. Lichtenberg, *Principles of Plasma Discharges and Materials Processing*, New York: Wiley, 1994, pp. 154-190.

[19] *Ibid.* pp. 413-434.

[20] F. F. Chen, *Introduction to Plasma Physics and Controlled Fusion*, 2nd ed., vol. 1, New York: Plenum, 1984, p. 45.

[21] X. Lu, *Material synthesis for silicon integrated-circuit applications using ion implantation*, Ph.D. dissertation, University of California, Berkeley, CA, 1997, pp. 108-119.

[22] S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era*, vol. 1, Sunset Beach, CA: Lattice, 1986, pp. 283-295.

[23] W. G. En, *Oxide charging damage in integrated circuit processing investigated with a coupled plasma/IC device model*, Ph.D. dissertation, University of California, Berkeley, CA, 1996, pp. 44-49.

[24] Z. Fan, *SOI synthesis by plasma immersion ion implantation*, Ph.D. dissertation, City University of Hong Kong, China, 1998, pp. 54-77.

[25] Y. J. Chabal, M. K. Weldon, Y. Caudano, B. B. Stefanov, and K. Raghavachari, "Spectroscopic studies of H-decorated interstitials and vacancies in thin-film silicon exfoliation," *Physica B*, vol. 273-274, pp. 152-163, 1999.

[26] K. Henttinen, I. Suni, and S. S. Lau, "Mechanically induced Si layer transfer in hydrogen-implanted Si wafers," *Applied Physics Letters*, vol. 76, pp. 2370-2372, 2000.

[27] W. G. En, I. J. Malik, M. A. Bryan, S. Farrens, F. J. Henley, N. W. Cheung, and C. Chan, "The Genesis Process™: a new SOI fabrication method," in *1998 IEEE In-*

ternational SOI conference Proceedings, Stuart, FL, 5-8 October 1998, pp. 163-164.

Chapter 5

GATE OXIDE DAMAGE DUE TO HIGH DOSE IMPLANTATION OF HYDROGEN

Abstract- The gate oxide damage from high dose implantation of hydrogen was evaluated using a stress induced leakage current (SILC) measurement. Metal-oxide-silicon (MOS) transistors with a gate area of 15 μm^2 and gate oxide thickness of 1.8, 3.5, and 5 nm were fabricated for this study. The MOS transistors were then implanted by hydrogen ions with doses of 4×10^{16} and 1.2×10^{17} cm^{-2} at 180 keV. After the implantation, SILC through the gate oxide was measured. Results show that SILC increases as hydrogen dose increases for the 3.5 and 5 nm gate oxides. The increase of SILC with increasing gate antenna ratio for these oxides was also observed. However, no SILC was detected for the 1.8 nm gate oxide, showing that damage from the implantation is not significant compared with direct tunneling leakage mechanism.

5.1 Introduction

Three-dimensional electronic device integration can enable high performance microelectronics and compact device structures. As a feasible technique to fabricate buried capacitors and dual-gate transistors, the hydrogen induced semiconductor layer transfer process has been reported [1], [2]. This hydrogen ion-cut layer transfer process has been employed previously for the fabrication of silicon-on-insulator (SOI) wafers [3]. In this process, a semiconductor donor wafer with pre-fabricated devices is chemical-mechanically polished followed by a high dose of hydrogen implantation. The implanted donor wafer is bonded to another substrate (handle wafer) by wafer bonding. This bonded wafer pair is then heated. As a consequence of the heating, the implanted hydrogen ions form

sub-surface micro-cracks beneath the wafer surface. The hydrogen induced silicon layer cleavage occurs along the implanted hydrogen peak concentration region, resulting in the silicon layer transfer from the donor wafer to the handle wafer [3]. Figure 5.1 illustrates the device layer transfer with the hydrogen ion-cut process.

The ion-cut technique typically requires a high dose (~10^{17} ions/cm^2) of hydrogen to be implanted through the device layer in order to cleave the silicon underneath [3]. This large amount of hydrogen could damage MOS devices exposed to the implantation. The "damage" means any degradation of gate oxide, and there are two main damage mechanisms in this case: (i) electrical stressing of the oxide and (ii) damage from physical bom-

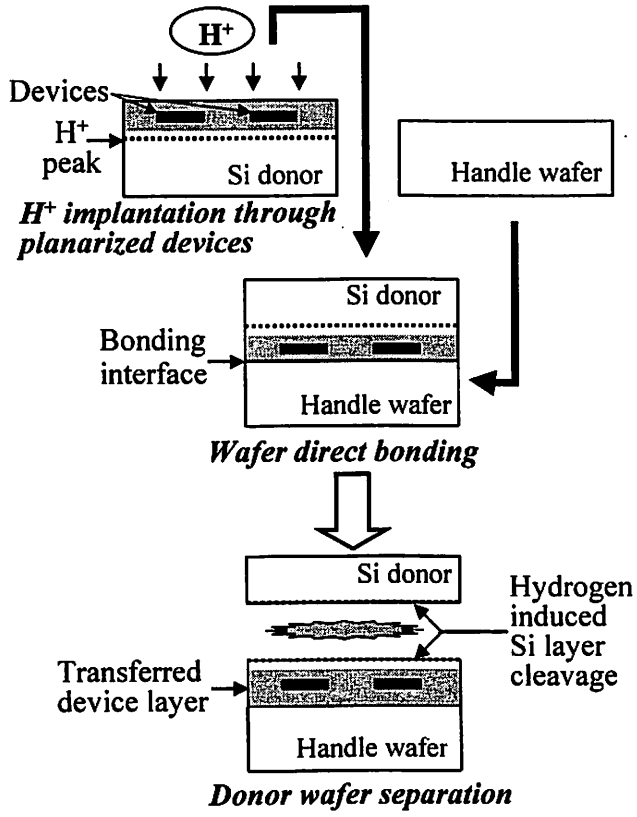


Figure 5.1 Process flow for device layer transfer by hydrogen ion-induced semiconductor layer cleavage (ion-cut process).

bardment of the oxide by the hydrogen ions. During the implantation, the positively charged ions (H^+) bombard the surface of the wafer [Figure 5.2(a)]. The interconnects conduct this charge from the wafer surface down to the MOS transistor gate, electrically stressing the gate oxide. With a large electrical field, significant tunneling currents flow. These electrical current may break chemical bonds in the gate oxide, degrading the bulk and interface properties of the oxide. Figure 5.2(b) illustrates the gate oxide damage caused by a passage of hydrogen ions through the oxide, and this is the primary concern in this experiment.

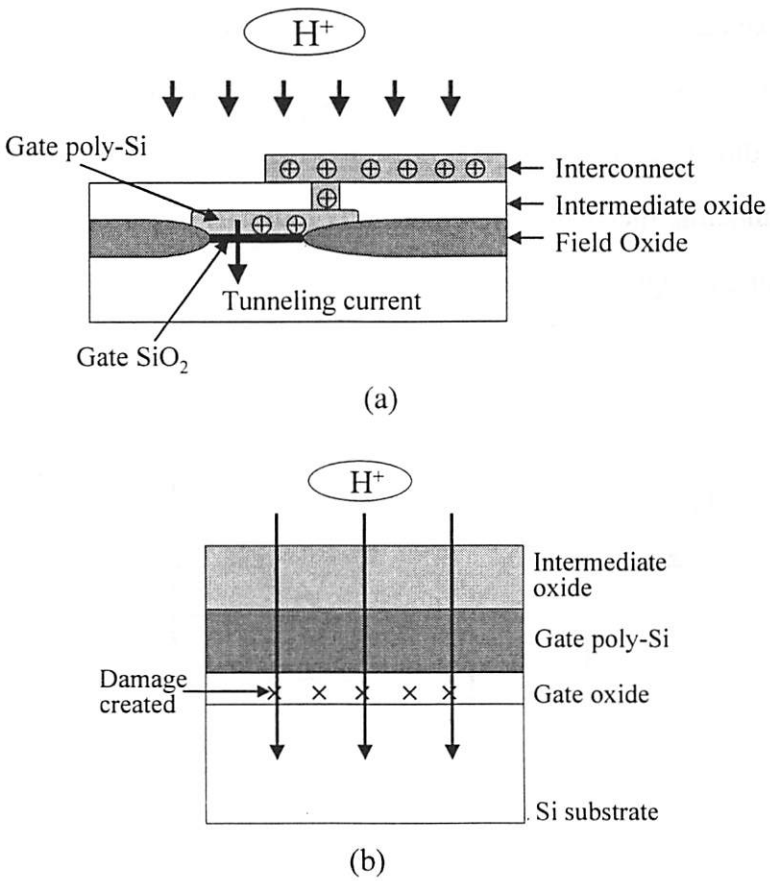


Figure 5.2 (a) Origin of gate oxide damage from electrical stressing. The surface conductor (interconnect) transfers charge from the hydrogen ions to gate poly-Si. If the electric field generated by this conducted charge is great enough, tunneling current flows through the gate oxide, resulting in electrical stress. (b) Gate oxide damage from physical bombardment of the oxide by the hydrogen ions due to the through-oxide implantation.

In this work, the gate oxide damage due to this high dose hydrogen implantation was evaluated using a SILC measurement.

5.2 Tunneling and SILC in Thin Oxide

Silicon dioxide is an amorphous insulator for a MOS gate material with a very high bandgap (~9 eV). The evolution of MOS technology has led to a continuous reduction of transistor size (from 0.35 to 0.18 μm) and corresponding gate oxide thickness (from 7 to 3 nm). For this thin SiO_2 or under very high electric field (~ several MV/cm), tunneling is a dominant mechanism for carrier (electron or hole) transport in the oxide. There are two major mechanisms governing electron tunneling through oxide: Fowler-Nordheim (F-N) tunneling and direct tunneling. Figure 5.3 shows these two tunneling mechanisms in thin oxides. The tunneling mechanisms are generally mutually exclusive, with only one dominating depending on applied biases.

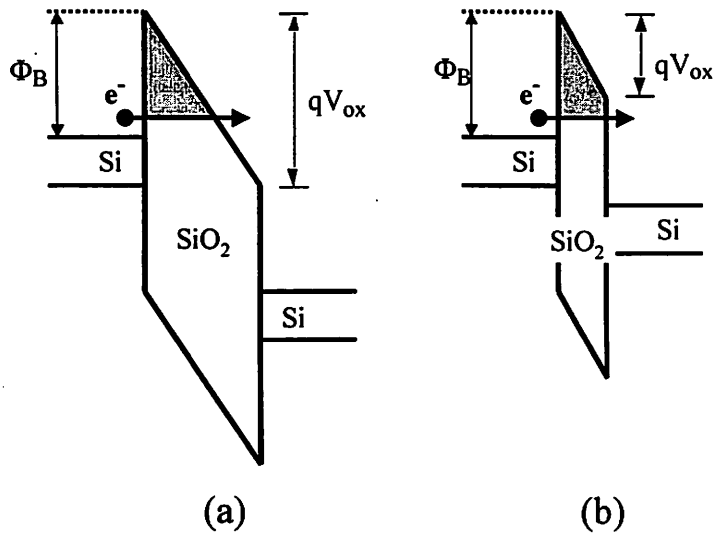


Figure 5.3 Tunneling mechanisms in thin oxides: (a) Fowler-Nordheim (F-N) tunneling and (b) direct tunneling.

When an applied oxide voltage, V_{ox}, is higher than the oxide potential barrier height, Φ_B (~3.2 eV for a poly-Si / SiO_2 system), F-N tunneling is dominant. In F-N tunneling, electrons tunnel through a triangular barrier into the conduction band of the gate oxide [see Figure 5.3(a)]. This tunneling mechanism has been studied for more than 70 years, originally by Fowler and Nordheim [4], and is well understood. The F-N tunneling current density, J_{FN}, can be expressed as [5]:

$$J_{FN} \approx E_{ox}^2 \exp\left[-\frac{4\sqrt{2m^*}(q\Phi_B)^{3/2}}{3q\hbar E_{ox}}\right] \tag{5.1}$$

where E_{OX} is the electric field across the oxide, and m^* is the carrier effective mass in the oxide conduction band. When the voltage is lower than 3.2 V for thin oxides, the tunneling barrier for electrons changes from triangular to trapezoidal [see Figure 5.3(b)]. In this case, the electrons no longer enter the oxide conduction band, but tunnel through the entire oxide directly from cathode to anode. Therefore, direct tunneling is the dominant conduction mechanism when the gate voltage is less than 3.2 V for oxides thinner than 3 nm [6]. The direct tunneling current density cannot be expressed easily in a closed form, although many approximations have been reported (see [7] for the most recent publication). Figure 5.4 shows the tunneling current through the different gate oxide thickness of 2.2, 3.7, 5.2, and 7.7 nm [8]. The dominant regions for F-N tunneling and direct tunneling are indicated. The F-N extrapolation into the direct tunneling regime shows that the direct tunneling current is much larger than the F-N mechanism, and this current remains high at even 1 V of gate bias. The direct tunneling current is very sensitive to oxide thickness, and this huge increase of current for the ultra-thin oxides poses a severe leakage problem, and potentially limits the future scaling of MOS transistors.

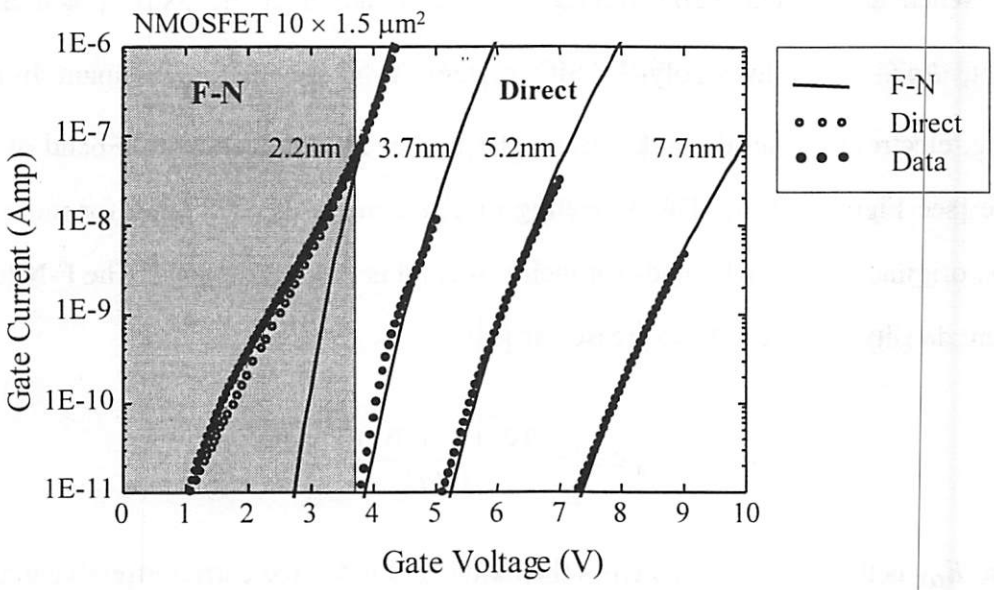


Figure 5.4 Tunneling current through the different gate oxide thickness of 2.2, 3.7, 5.2, and 7.7 nm. F-N tunneling and direct tunneling current was plotted according to theoretical calculations. Data were extracted from 10 μm × 1.5 μm NMOS gate by D. Park [8]. The F-N extrapolation into the direct tunneling regime shows that direct tunneling allows much more current that the F-N mechanism at lower electric fields.

If thin oxides are under electrical stress such as high field F-N tunneling and hot carrier injection, then the oxide degrades, and low field current leakage called SILC is created. SILC was first observed in 1982 on the 5 nm oxide with constant voltage stress of 6.3 V [9]. Recently, oxide degradation by trap generation is believed to be a key factor for SILC, and several trap generation mechanisms have been proposed (see [10] for review). SILC transforms from a steady-state current flowing through the oxide traps in thinner oxides to a transient current due to charging and discharging of the traps as the oxide thickness increases. Both transient and steady-state current components depend on oxide thickness. Thick oxides have a large transient component and low steady-state component, while thin oxides have a small transient component and a large steady state component. Figure 5.5 illustrates the two components of trap-assisted tunneling of thin

and thick oxides. Right after electrical stressing, the traps near the Si/SiO_2 interface are charged causing the transient component. In thick oxides, the probability that an electron has sufficient traps that can be used as hopping points for tunneling is very small, resulting in a small steady-state component. In thinner oxides, fewer traps are necessary for the electrons to move from cathode to anode and therefore the steady-state component will dominate. In terms of oxide surface area, SILC is proportional to the area, which means that the leakage paths are uniformly distributed over the oxide surface, unlike breakdown, which occurs in one or few localized defective regions of the oxide [11]. The SILC Ig-Vg curves are quite symmetric with respect to the gate bias polarity, indicating that the defects (leakage paths) are distributed in the volume of oxide rather than the oxide interface [11]. Nevertheless SILC generation is generally accompanied by a correlated creation of interface traps [12].

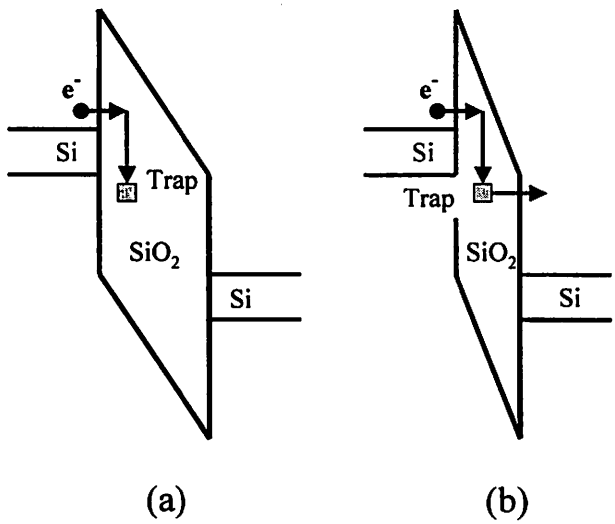


Figure 5.5 Trap assisted tunneling as a SILC mechanism. (a) transient current in thicker oxide. (b) steady-state current in thinner oxide. In thicker oxides, the electron trapping occurs, resulting in low steady-state current.

Measuring the low-field gate leakage current is the preferred method for damage detection in oxides thinner than 5 nm, since the excessive leakage current makes C-V measurement insensitive for these thin oxides. SILC is much more straight forward than C-V interface trap extraction, with no data transformation necessary [13]. Although comparing SILC data for different oxides is complicated by the varying intrinsic leakage current, SILC is always positively correlated to damage, with the leakage proportional to the trap density in the same oxide. Figure 5.6 shows the leakage current for a 3.7 nm oxide for increaseing levels of oxide stress.

5.3 Experimental

In this study, n-channel MOS transistors were fabricated using local oxidation of silicon (LOCOS) isolation and the in-situ n^+ poly-silicon gate process. Gate oxide with thicknesses of 1.8, 3.5, and 5 nm were grown in a 750-800 °C dry oxygen environment followed by nitrogen anneal at 900 °C for 20 minutes. After the gate poly-Si deposition,

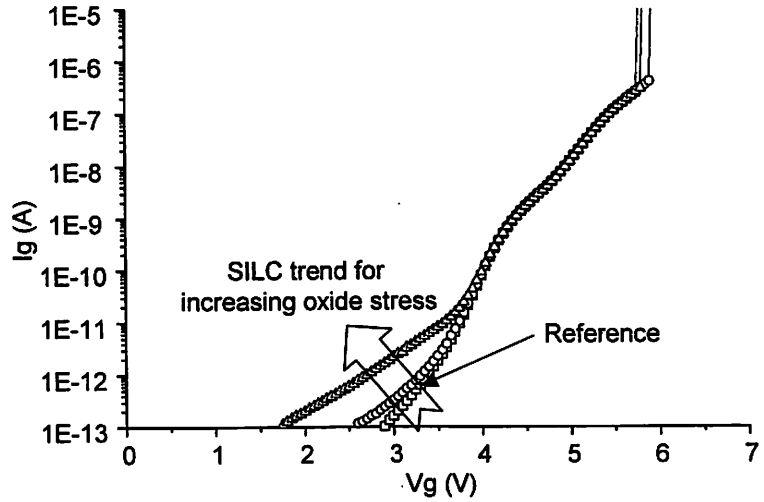


Figure 5.6 SILC trend for increasing oxide stress. SILC measurements with increasing oxide stress for a 3.7 nm oxide of area $1.5 \times 10\ \mu m^2$.

the gate area of L= 1.5 μm and W=10 μm was defined by reactive ion etching. Source / drain implantation was followed by low temperature oxide (LTO at 450 °C) deposition. After contact hole etching of LTO, another phosphorous doped poly-Si was deposited and patterned for contacts, pads, and antennas. The reason poly-Si was used rather than aluminum was to prevent potential Al melting from heat (~500 °C) application for the ion-cut layer transfer process. The poly-Si antenna areas were 640 μm × 640 μm, 160 μm × 160 μm, 80 μm × 80 μm, and 40 μm × 40 μm, which correspond to the antenna ratio (AR, antenna area divided by gate area) of 27300, 1710, 427, and 107, respectively. Figure 5.7 illustrates the device structure used in this experiment.

The MOSFETs were then implanted by hydrogen ions with doses of 4×10^{16} and 1.2×10^{17} H^+/cm^2 using 0.5 mA hydrogen beam current at 180 keV. With this energy, the hydrogen peak profile is estimated to be ~0.5 μm below the SiO_2/Si interface. After the high

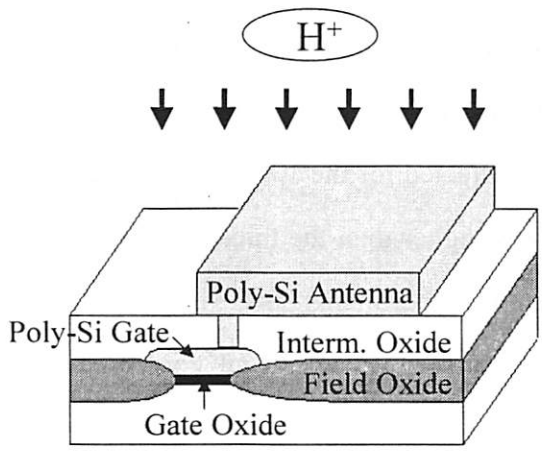


Figure 5.7 Device structure and hydrogen implantation in this study. Gate oxides are 1.8, 3.5, and 5 nm thick with the area of 1.5×10 μm^2. Poly-Si antenna area varies from 40×40 μm^2 to 640×640 μm^2.

dose implantation, the gate oxide leakage current was measured with a gate voltage sweep of 50 mV incremental steps and a 10 seconds delay at each step. This delayed measurement ensured that displacement currents for the pad and oxide were down to 10^{-15} A, the detection limit of an HP 4140B pico-ammeter.

5.4 SILC Measurement Results

Figure 5.8 shows the SILC measured before and after the hydrogen implantation for the gate oxide thickness of 5 nm. Figure 5.8(a) shows the hydrogen dose dependency of SILC between 4×10^{16} and 1.2×10^{17} H^+/cm^2. In this case, the AR was 27300 (640 μm × 640 μm antenna over 1.5 μm × 10 μm gate). The data show that SILC increases as hydrogen dose increases for the 5 nm gate oxide. The increase of SILC with increased AR for the 5 nm oxide is also observed [see Figure 5.8(b)]. This AR dependency implies that the gate oxide charging is a dominant damage mechanism in this experiment.

Figure 5.9 shows the SILC measurement for the 3.5 nm and 1.8 nm gate oxides. The hydrogen dose was 4×10^{16} ions/cm^2, and the data were plotted for the different AR's. SILC was observed for the 3.5 nm gate oxide, and it increases as the antenna size increases, Although the AR dependency is not as significant as that of the 5 nm oxide. However, no SILC was detected for the 1.8 nm gate oxide [see Figure 5.9(b)], even if the leakage current level was higher than the thicker oxides due to direct tunneling, which is in agreement with previous experiments [14]. This result indicates that ultra-thin oxide (~ 1.8 nm) degradation (if any) is insignificant compared with direct tunneling leakage current.

For the device layer transfer process, the ultra-thin oxide devices can be transferred by the method shown in Figure 5.1 without any degradation in the gate oxides. For

thicker oxides (> 3 nm), the gate oxide protection from hydrogen implantation is required. This can be done by the patterned ion-cut technique, in which MOS active region is masked by photoresists during the implantation.

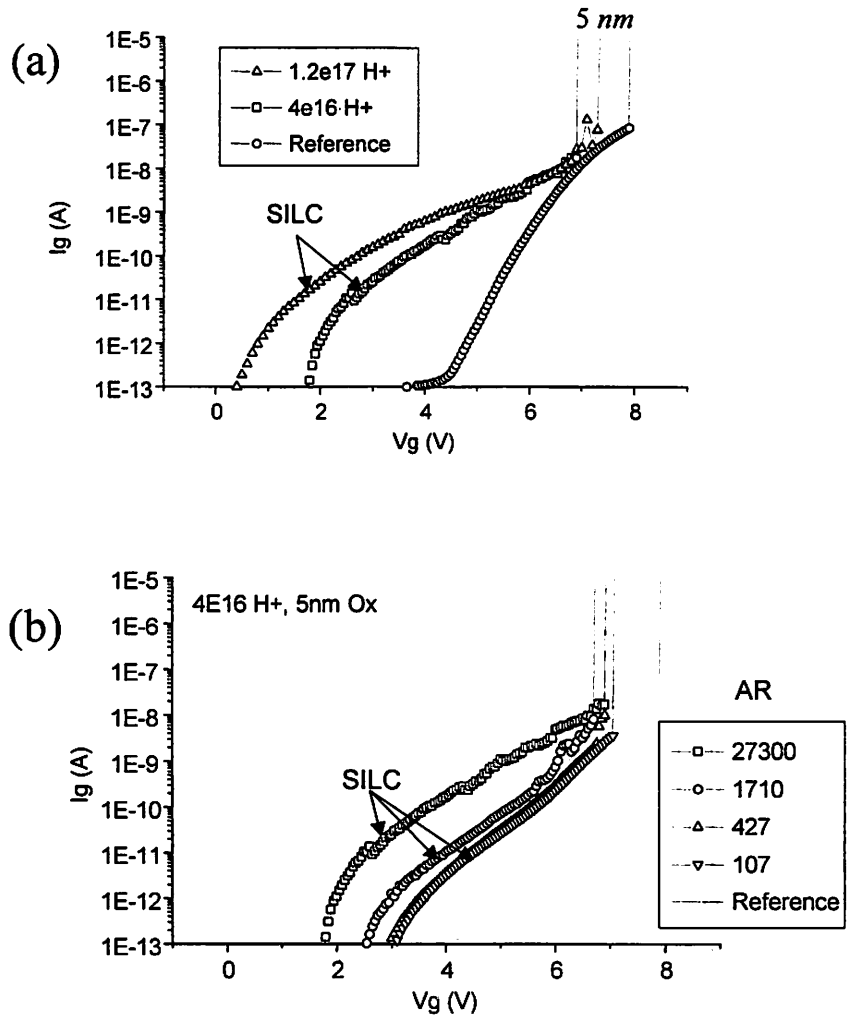


Figure 5.8 SILC measurement before and after the hydrogen implantation for the gate oxide thickness of 5 nm, showing (a) hydrogen dose dependency and (b) AR dependency. The gate area is $1.5 \times 10\ \mu m^2$.

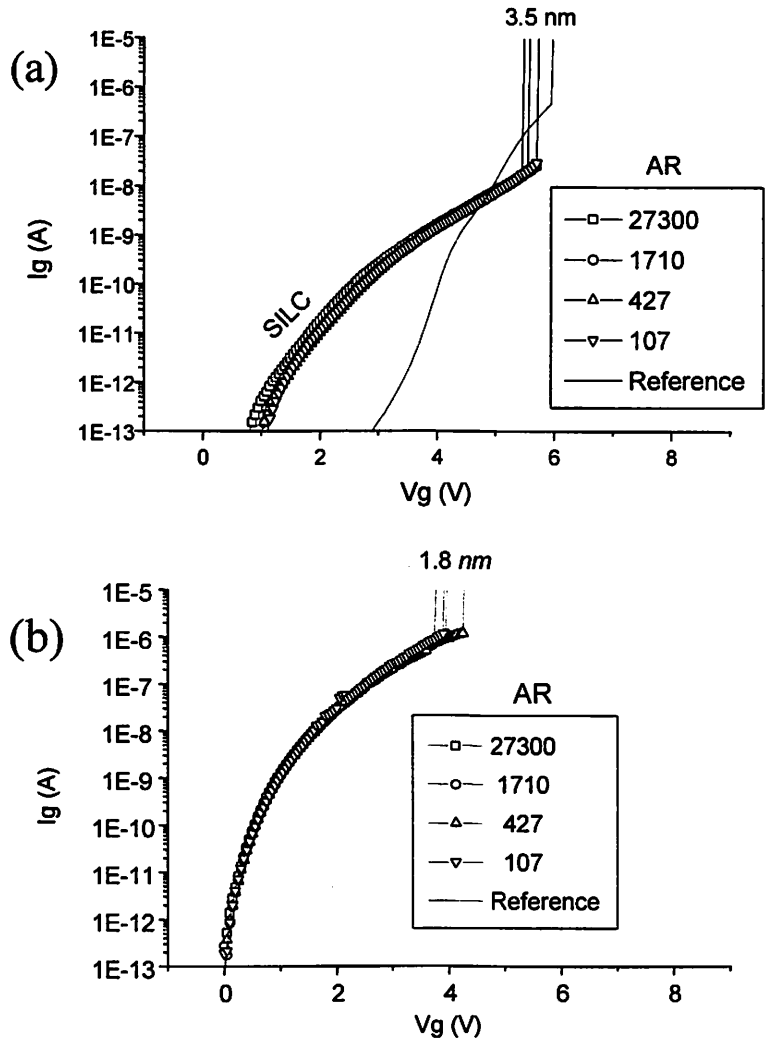


Figure 5.9 SILC measurement for the 3.5 nm and 1.8 nm gate oxides with the hydrogen dose of 4×10^{16} cm^{-2}. The data were plotted according to AR. The gate area is 1.5×10 μm^2.

5.5 Summary

Gate oxide damage due to high dose hydrogen implantation was observed by SILC measurement, which had strong dependence on antenna ratio for the 5 nm gate oxide. For ultra-thin oxide (1.8 nm), no additional SILC was observed from the hydrogen implanta-

tion, which suggests that thinner oxides are more forgiving for hydrogen ion-cut layer transfer for three-dimensional integration.

References

[1] B. H. Lee, G. J. Bae, K. W. Lee, G. Cha, W. D. Kim, S. I. Lee, T. Barge, A. J. Auberton-Herve, and J. M. Lamure, "A novel pattern transfer process for bonded SOI giga-bit DRAMs," in *1996 IEEE International SOI Conference Proceedings*, Sanibel Island, FL, 30 Sept. -3 Oct. 1996, pp. 114-115.

[2] B. E. Roberds, E. J. Whang, A. Rudolph, and B. S. Doyle, "Investigation of a novel self-aligned dual gate MOSFET structure," in *1998 IEEE International SOI Conference Proceedings*, Stuart, FL, 5-8 Oct. 1998, pp. 109-110.

[3] M. Bruel, "Application of hydrogen ion beams to silicon on insulator material technology," *Nuclear Instruments and Methods in Physics Research B*, vol. 108, pp. 313-319, 1996.

[4] R. H. Fowler and L. Nordheim, "Electron emission in intense electric fields," *Proceedings of the Royal Society of London Series A*, vol. 119, pp. 173-181, 1928.

[5] S. M. Sze, *Physics of Semiconductor Devices*, 2nd Ed., New York: Wiley, 1981, p. 403.

[6] K. F. Schuegraf, D. Park, and C. Hu, "Reliability of thin SiO_2 at direct-tunneling voltages," in *International Electron Device Meeting 1994 Technical Digest*, San Francisco, CA, 11-14 Dec. 1994, pp. 609-612.

[7] Khairurrijal, W. Mizubayashi, S. Miyazaki, and M. Hirose, "Analytic model of direct tunnel current through ultrathin gate oxides," *Journal of Applied Physics*, vol. 87, pp. 3000-3005, 2000.

[8] D. Park, "Plasma process-induced charging damage on thin gate oxides," Ph.D. dissertation, University of California, Berkeley, CA, 1998, p. 17.

[9] J. Maserjian and N. Zamani, "Behavior of the Si/SiO_2 interface observed by Fowler-Nordheim tunneling," *Journal of Applied Physics*, vol. 53, pp. 559-567, 1982.

[10] R. Degraeve, B. Kaczer, and G. Groeseneken, "Degradation and breakdown in thin oxide layers: mechanisms, models, and reliability prediction," *Microelectronics Reliability*, vol. 39, pp. 1445-1460, 1999.

[11] G. Ghibaudo, P. Riess, S. Bruyere, B. DeSalvo, C. Jahan, A. Scarpa, G. Pananakakis, and E. Vincent, "Emerging oxide degradation mechanisms: stress induced leakage current (SILC) and quasi-breakdown (QB)," *Microelectronic Engineering*, vol. 49, pp. 41-50, 1999.

[12] R. Rofan and C. Hu, "Stress-induce oxide leakage," *IEEE Electron Device Letters*, vol. 12, pp. 632-634, 1991.

[13] B. P. Linder, "Investigation of plasma implantation and gate oxide charging during plasma processing," Ph.D. dissertation, University of California, Berkeley, CA, 1999, pp. 143-146.

[14] D. Park, M. Kennard, Y. Melaku, N. Benjamin, T. J. King, and C. Hu, "Stress-induced leakage current due to charging damage: gate oxide thickness and gate poly-Si etching condition dependence," in *1998 3rd International Symposium on Plasma Process-Induced Damage*, Honolulu, HI, 4-5 June 1998, pp. 56-59.

Chapter 6

SILICON LAYER TRANSFER WITH PATTERNED IMPLANTATION OF HYDROGEN

Abstract- Silicon layers were successfully transferred from a patterned hydrogen-implanted silicon wafer to another wafer by either a thermal or mechanical cleavage process. The first wafer was masked with various patterns of 2~3 μm-thick photoresist or poly-silicon, and implanted with a hydrogen dose of 4~12 $\times 10^{16}$ ions/cm^2 at an energy of 150 ~ 180 keV. After stripping off the implantation mask, the wafer was bonded to a thermally grown oxide wafer face-to-face by low-temperature direct bonding. The bonded pair was then either heated or bent from both sides (mechanically) until the hydrogen-induced silicon cleavage occurred. This experiment showed that ion-cut silicon layer transfer is feasible even without a continuous hydrogen implantation of the entire wafer.

6.1 Introduction

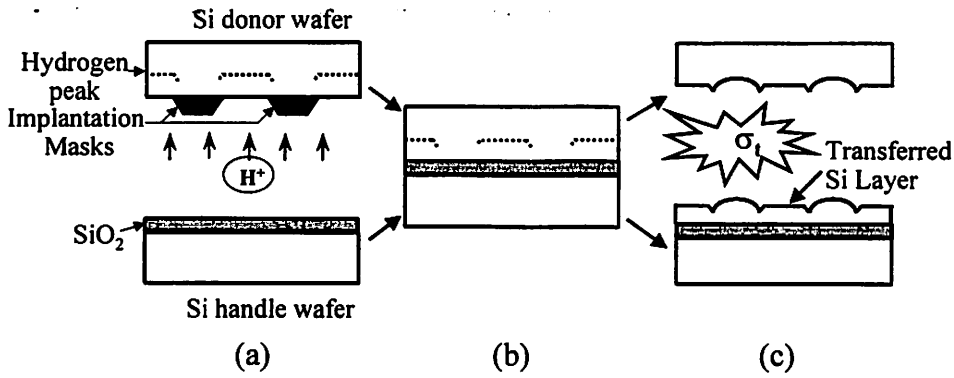
Three-dimensional integration of electronic, optical, and micro-electromechanical devices will provide applications in high performance compact microelectronics. As a promising technique for these applications, the ion-cut silicon layer transfer process using hydrogen implantation and wafer bonding has been introduced [1], [2]. The ion-cut technique typically requires a high dose (~10^{17} ions/cm^2) of hydrogen to be implanted through the device layer in order to cleave the silicon underneath [3]. In Chapter 5, the gate oxide degradation during the hydrogen implantation was evaluated (see also [4]). For the prefabricated electronic device layer transfer process, the ultra-thin oxide devices can be transferred by the method shown in Figure 5.1 without any degradation in the gate oxides. For thicker oxides (> 3 nm), the gate oxide protection from hydrogen implantation is

required. In this chapter, a novel process of patterned ion-cut is introduced, in which the active device area is protected from the hydrogen ions by an implantation mask [5]-[8]. In this process, it has been shown that a silicon layer can be transferred without a continuous implantation of hydrogen on the wafer surface. As for silicon cleavage processes in this patterned ion-cut, both thermal and mechanical cleavage methods were demonstrated, and process limitations were studied depending on the non-implanted area dimension, the fractional implantation area, and the hydrogen dose.

6.2 Experimental

Figure 6.1 illustrates the sequence of the patterned ion-cut process. In this study, both n and p type (5 to 50 Ω·cm) CZ-grown, prime grade silicon (100) and (111) wafers were used. At first, the silicon donor wafer was either spin-coated with 3 μm-thick photoresist or deposited with 2.3 μm-thick poly-silicon for hydrogen implantation masks. The masks are various shapes and sizes of polygons and lines with different dimensions of mask openings (e.g., see Figure 6.2). For the convenience of reference, each pattern was named after its "mask size - mask opening SHAPE", i.e., 10-5 SQUARE for 10 μm square mask with 5 μm implantation opening. Due to the limitations of our photolithography and etching, the actual implantation mask sidewall was slightly tapered. This pattern-masked silicon donor wafer was then implanted with a hydrogen dose between $4 \times 10^{16} \sim 1.2 \times 10^{17}$ ions/cm^2 using an energy of 150~180 keV. The patterned 2~3 μm-thick implantation mask consisting of photoresist or poly-silicon was applied to prevent the hydrogen ions from reaching the silicon wafer surface during the implantation, resulting in hydrogen ion implantation only in the mask openings. After the implantation, the implan-

(1) Thermal cleavage



(2) Mechanical cleavage

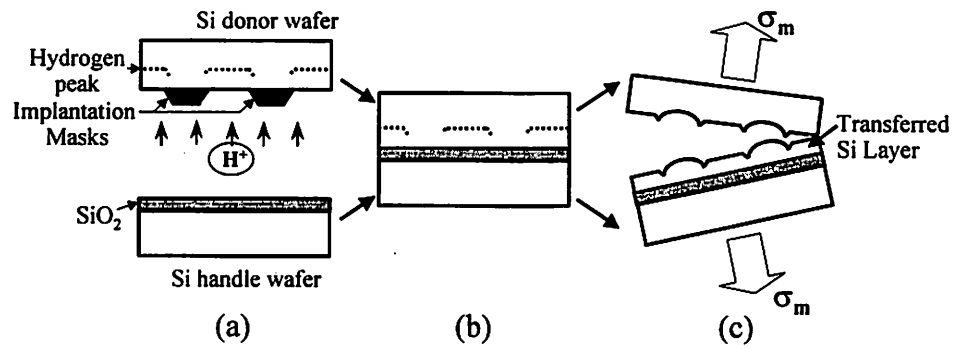


Figure 6.1 Patterned ion-cut process flow. (a) H^+ ion implantation through mask patterns. (b) Low temperature wafer direct bonding. (c) (1) Heat treatment or (2) mechanical bending for layer splitting along the hydrogen peak.

tation masks were stripped off by using oxygen plasma ashing for photoresists or by using XeF_2 etching for poly-silicon.

On the silicon handle wafer, a 100-200 nm-thick SiO_2 layer was grown in a thermal oxidation furnace. The implanted donor and oxidized handle wafers were bonded directly, face-to-face at room temperature after a standard RCA cleaning and an oxygen plasma surface activation for a better bonding interface [9]. The bonding interface was cured further at 200 °C for ~10 hours. The bonded wafer pair was then separated along the hydro-

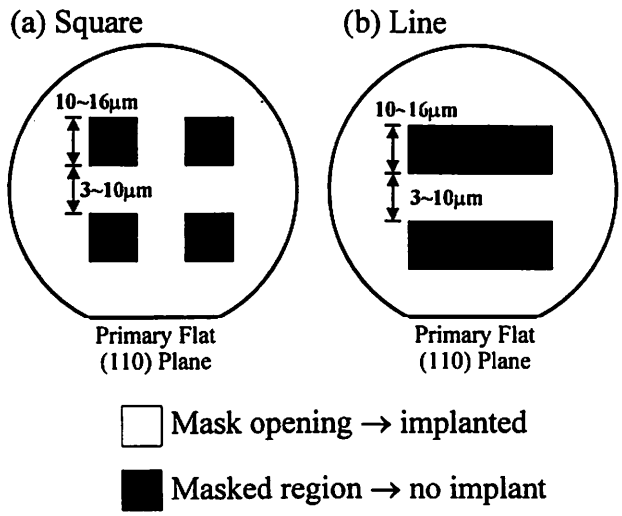


Figure 6.2 Implantation mask patterns. There were also triangles, parallelograms, and hexagons. The square and line patterns had 0° and 45° tilted versions with respect to the wafer primary flat.

gen peak either (1) by heating to ~600 °C in a rapid thermal annealer (RTA), or (2) by mechanical bending from both sides of the wafers. This (thermal or mechanical) ion-cut process enables the silicon layer transfer from the donor wafer to the handle wafer (see Figure 6.1).

6.3 Thermal Cleavage of Pattern-Implanted Silicon

6.3.1 Blistering of Pattern-Implanted Silicon

In order to determine the blistering temperature and see the effectiveness of the implantation mask, the 5×10^{16} H^+/cm^2 implanted silicon donor wafer was annealed to the temperatures between 400 ~ 600 °C for 5 minutes after removal of the implantation mask, without bonding to a handle wafer. It was found that hydrogen induced silicon surface blistering started at ~500 °C after 5 minutes of annealing. It was clear that all the nucleated hydrogen bubbles and silicon blisters were well confined to the implanted regions,

even though some of the coalesced bubbles extended into the non-implanted region. Figure 6.3 shows the optical micrograph of the 13-7 LINE pattern implanted donor wafer surface annealed at 600 °C for 60 sec. The coalesced hydrogen bubble islands were formed and were almost equally spaced along the vertical lines of the pattern.

Figure 6.4 compares blistering between mask shapes (square vs. parallelogram), fractional implantation areas (36% vs. 75%), and wafer orientations [(100) vs. (111)]. The fractional implantation area (FIA) is defined as the ratio of the implantation mask opening (implanted) area to the total (implanted + non-implanted) area. The wafers were hydrogen implanted with 8×10^{16} cm^{-2} at 180 keV, and annealed at 650 °C for 15 seconds. Figures 6.4 (a) and (b) compare two different FIA's in silicon (100) with square masks, and Figures 6.4 (c) and (d) compare those in silicon (111) with parallelogram masks. For small FIA, hydrogen induced bubbles were well-confined and continuous along the implantation mask opening. Silicon flaking was not observed. However, for large FIA, the silicon blisters and flakes were randomly distributed in the mask openings. Aside from the FIA dependence, we observed no effects of substrate orientations [(100) and (111)], and pattern shapes (square and parallelogram) for silicon blistering and flaking.

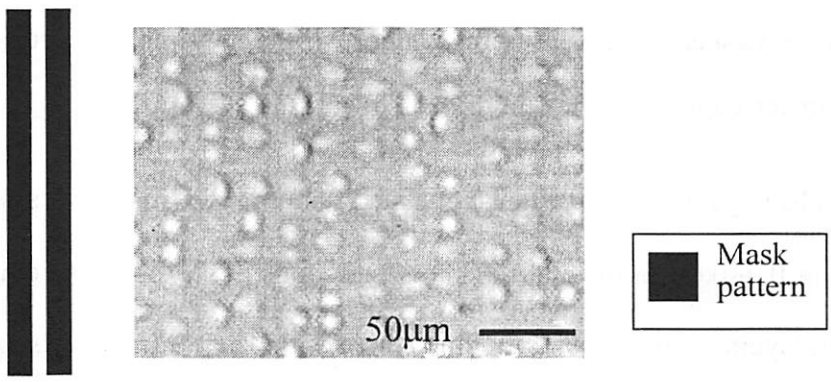
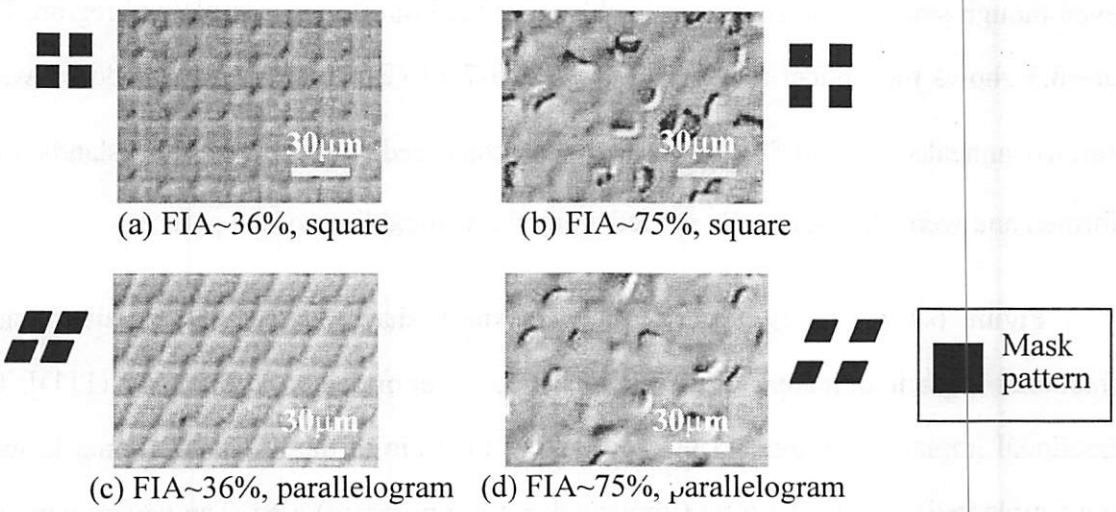


Figure 6.3 Optical micrograph of the 13-7 LINE implanted donor wafer after annealing at 600 °C for 60 sec. The coalesced hydrogen bubbles are almost equally spaced along the vertical lines of mask opening.



(a) FIA~36%, square (b) FIA~75%, square

(c) FIA~36%, parallelogram (d) FIA~75%, parallelogram

Figure 6.4 Optical micrographs of pattern implanted silicon donor wafer surfaces (i.e., no wafer bonding) after 650 °C for 15 sec of annealing. (a) and (b) for square masked implantation in Si (100). (c) and (d) for parallelogram masked implantation in Si (111). For small FIA, hydrogen induced bubbles are within the implanted region without flaking.

6.3.2 Surface Morphology of Transferred Silicon

Figure 6.5 shows optical micrographs of the transferred silicon layer on top of the handle wafer. The hydrogen implantation was done at 180 keV with a dose of 8×10^{16} ions /cm^2. Each of the polygons and lines is about 10 μm wide, and the inside of the polygons and lines were masked to prevent implantation. All the non-implanted regions were successfully transferred to a handle wafer.

After cleavage, most of the non-implanted regions were rough for silicon (100) wafers, showing 0.2~0.6 μm of total thickness variations (TTV) for an average of 1.5 μm-thick silicon layers. In the case of the line patterns, the cleaved surface showed so-called *river patterns*, in which the cleavage crack propagates along the faint lines [10], [11]. Figure 6.6 shows the river patterns of the cleavage fracture surfaces. As shown from the

pictures, the river patterns are aligned along <110> direction. This implies that the silicon fracture is favored along <110> direction, which is in good agreement with previous publications [11], [12].

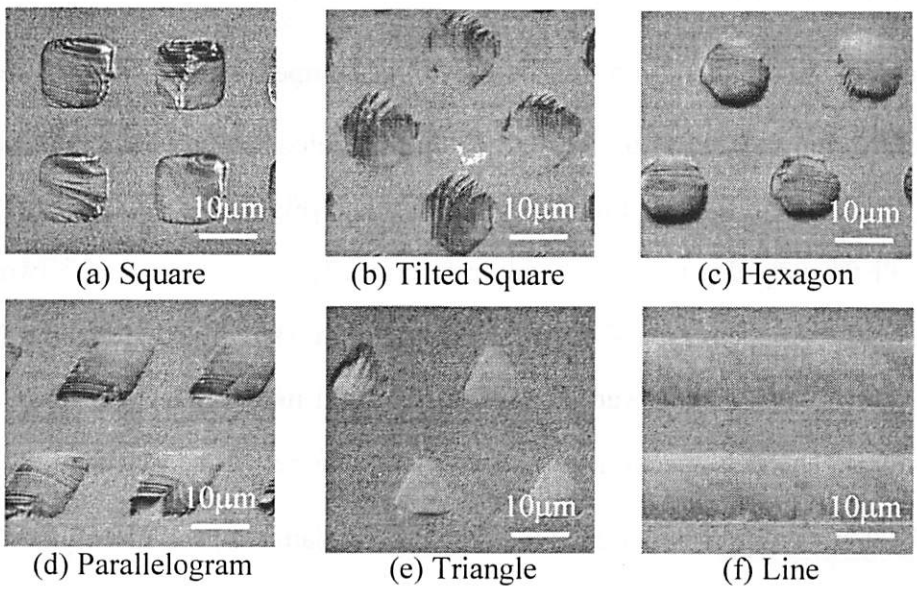


Figure 6.5 Optical micrographs of the transferred silicon layer surfaces

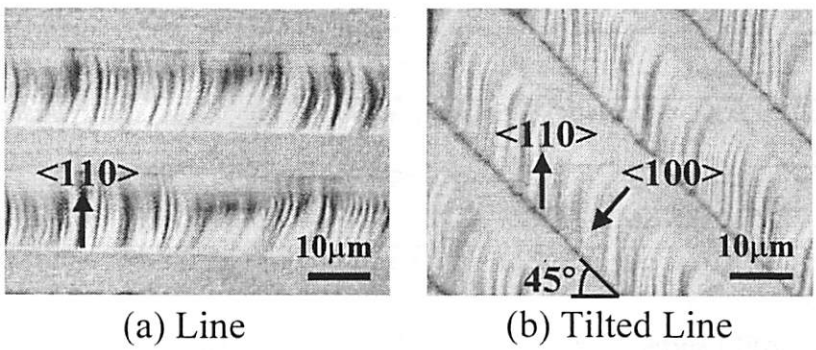


Figure 6.6 *River patterns* of the cleaved silicon fracture surfaces. The faint lines are aligned along <110> direction, implying the crack propagation is favored along <110> direction.

Figure 6.7 shows the atomic force microscopy (AFM) surface topographies across the rough regions of the transferred layer. The topography of most of these patterns shows a similar cleavage curve, except for 9-11 SQUARE and 16-4 LINE. In the non-implanted region, the silicon cleavage started from the mask boundary and propagated horizontally about 0.1~1.0 μm, and then went downward (towards the wafer bonding interface) to a depth of about 0.2 μm, followed by three competing tendencies: (i) the cleavage went upward and merged at the center of non-implanted region [Figures 6.7 (a)-(e) and 6.8 (a)], (ii) the cleavage went along the (100) plane [Figure 6.8 (b)], and (iii) the crack derailed all the way down to the bonding interface [Figure 6.7 (f)]. The two dominant cleavage characteristics for 13-7 SQUARE ion-cut are shown in Figures 6.8 (a) and 6.8 (b). Each one shows a tilted surface profile (top) and its cross-section across the rough area (bottom). The cross-section shows that the transferred silicon layer in the implanted regions is about 1.3 μm, in good agreement with the damage peak of 150 keV H^+ ions in silicon predicted by Monte-Carlo TRIM simulation [13].

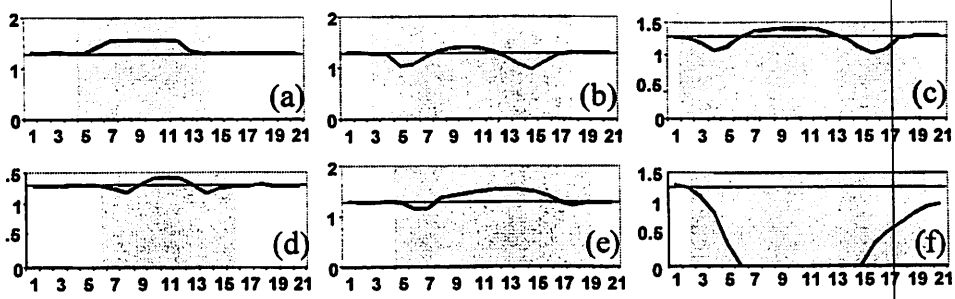


Figure 6.7 AFM surface topographies of the transferred silicon surfaces scanned across the non-implanted areas. The shaded regions are the implanted mask regions. The thin line shows the aver-age silicon over-layer thickness (~1.3 μm). All units are in micrometers. In (f), 16-4 LINE, only some part of silicon was transferred.

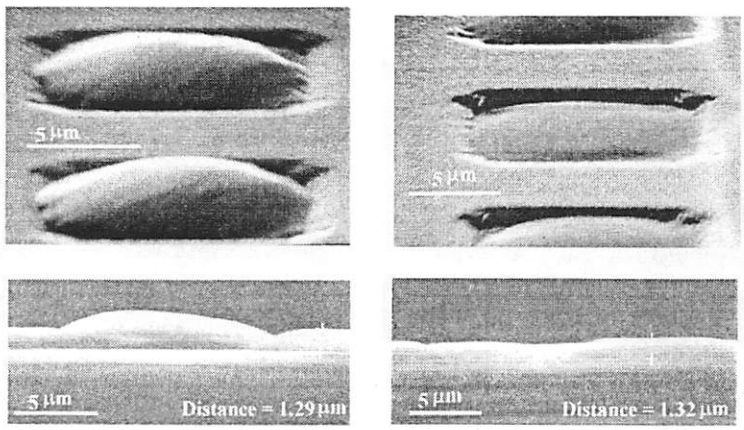
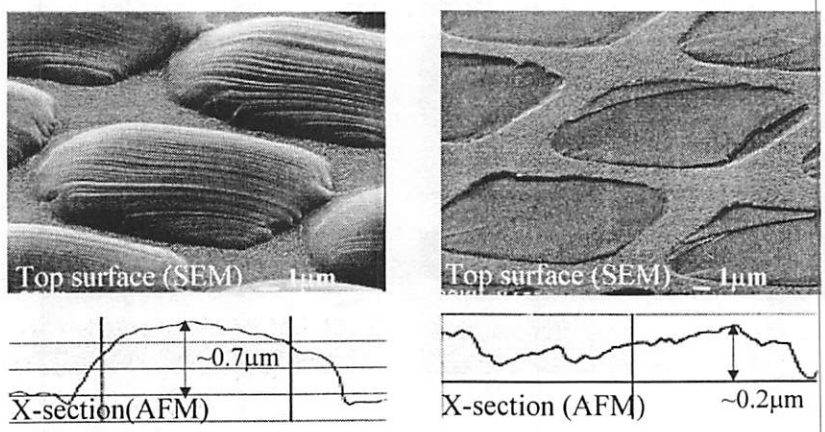


Figure 6.8 SEM of the transferred silicon over-layer surfaces (top) and cross-sections (bottom) from 13-7 SQUARE pattern. The surfaces were taken at a tilt angle of about 70°. These two kinds [(a) and (b)] of cleavage are the dominant features for pattern (b) splitting.

Figure 6.9 compares the typical fractured surfaces of Si (100) and Si (111) in this experiment. The pattern is 12-3 PARALLELOGRAM that is the 12μm × 12μm non-implanted parallelogram with the 3μm implantation opening. With a Si (111) wafer, the transferred surface is flatter with TTV ~0.2 μm. However with Si (100), the cleavage is consistently upward with TTV ~0.7 μm.

6.3.3 Cleavage Temperature and Limitations in Thermal-cut

As for the heat treatment for the cracking, Figure 6.10(a) compares the actual layer transfer time vs. temperature, between the blanket (FIA=100%), 10-10 SQUARE (FIA = 75%), and 16-4 SQUARE (FIA=36%) implantation. An FIA of 100% refers to the wafers without any masks, so the whole wafer surface area was implanted. Within the temperature range from 550 to 700 °C, there was no significant difference between the blanket

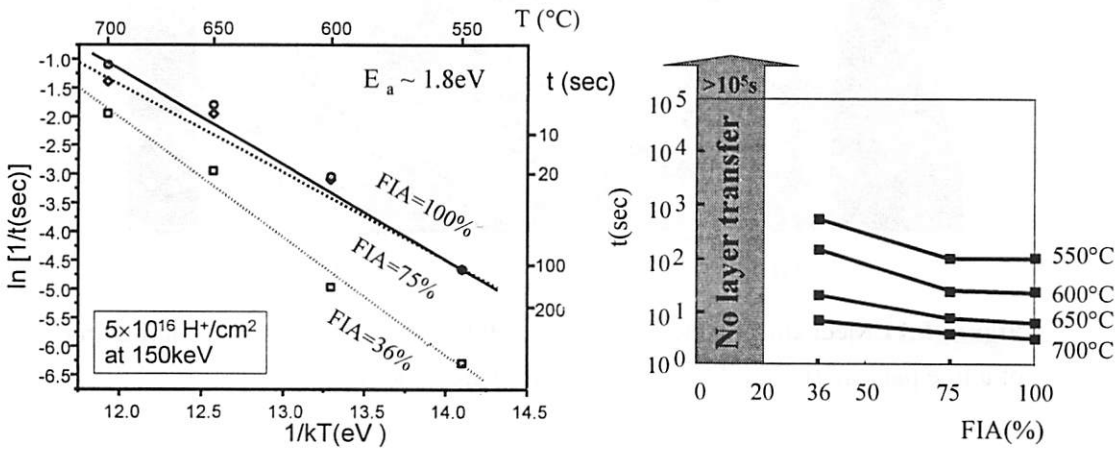


(a) Si (100) (b) Si (111)

Figure 6.9 Typical fractured surfaces of Si (100) and Si (111) in this experiment. The pattern is 12-3 PARALLELOGRAM. With a Si (111) wafer, the transferred surface is flatter with TTV~ 0.2μm. However, with Si (100), the cleavage occurs higher with a TTV~ 0.7μm.

and 10-10 SQUARE layer splitting. However, in 16-4 SQUARE, the time required for splitting at each temperature was longer than that of the blanket and 10-10 SQUARE implanted samples, especially in the low temperature regime. Figure 6.10(b) re-plots the graph in terms of layer transfer time vs. FIA. In addition, for an FIA of 20% and below, no layer transfer was observed for 10^5 seconds (~28 hours) for all temperatures. For example, with 5×10^{16} H^+/cm^2, 16-4 LINE patterns (FIA= 20%) were not cleaved, while 16-4 SQUARE patterns (FIA=36%) were.

From Figure 6.10(a), we calculated the silicon layer splitting activation energy to be about 1.6 eV and 1.9 eV for FIA= 75% and 36%, respectively, which are within the range (±10%) of the value (1.8 eV) obtained for FIA=100% (see section 4.2).

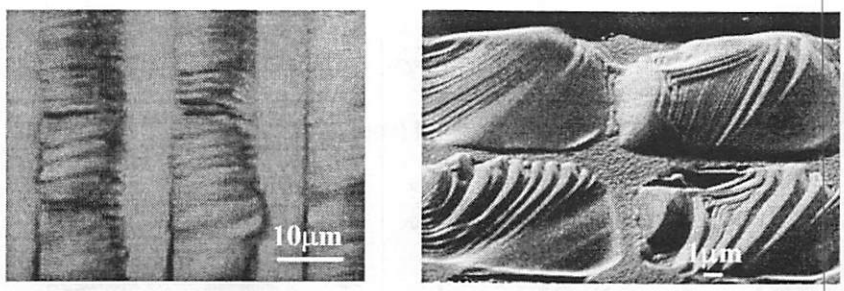


(a) (b)

Figure 6.10 Silicon layer transfer time vs. annealing temperature for different FIAs. Within the temperature range above, there was no significant difference between FIA=100% and FIA=75% layer splitting. However, in FIA=36%, it took longer time for splitting. For an FIA of 20% or below, no layer transfer was observed for ~28 hours for all temperatures.

6.4 Mechanical Cleavage of Pattern-Implanted Silicon

Silicon layers were successfully transferred through a mechanical separation method (mechanical bending of the bonded pair), but the cleaved surface of the non-implanted region was quite rough (similar to the thermal cleavage method, see Figure 6.11 for the surfaces). However, the maximum cleavage propagation distance across a non-implanted region is larger for mechanical cleavage (~100 μm) than thermal cleavage (~20 μm). Also, samples with an FIA of 20% were cleaved through the mechanical cut method.



(a) (b)

Figure 6.11 Mechanically cleaved silicon (100) surfaces. (a) Optical micrograph of a line pattern. (b) SEM tilted view of a square pattern.

6.5 Discussion

6.5.1 Crack Propagation in the Non-implanted Region

We have explained the internal crack propagation with the following scenario. First, the stress localization from the cleavage front from the surrounding implanted region propagates on the cleavage plane inward. The initial downward motion could be attributed to the fact that the implantation mask had a finite slope due to the resist exposure, development, and erosion during implantation (especially for the photoresist soft mask). Implantation through the tapered mask brings a bend on the implanted hydrogen profile toward the donor wafer surface, resulting in the initial downward cut (see Figure 6.1). The implanted hydrogen tends to form mechanically weakened platelets primarily on (100) and occasionally on (111) planes [14]. These two conflicting factors determine the crack direction in our case. We speculate that near the implantation boundary, the majority of (100) platelets tend to trigger the cleavage along the (100) plane, while the existence of the (111) platelets are the driving force for the upward or downward cut.

6.5.2 Fracture of Silicon

Figure 6.12 shows a unit cell of crystalline silicon. It has the diamond structure that is basically a face centered cubic (FCC) lattice with 2 basis atoms. Each silicon atom bonds 4 other silicon atoms. The bonds are covalent with a cohesive energy of 4.63 eV / atom [15]. In single crystalline solids, cleavage can occur on several planes. But the easier planes to cleave exist according to the surface energy. In the diamond silicon structure, {111} and {110} planes are known to be good cleavage planes. Figure 6.13 illustrates three important planes in silicon, and Table 6.1 gives surface energy values for those planes [16]. The numbers have wide variations from literature to literature. However, most of them agree that γ_{111} and γ_{110} is less than γ_{100}. This fact may explain why silicon (111) wafer cleavage was smoother than (100) in the section 6.3.2.

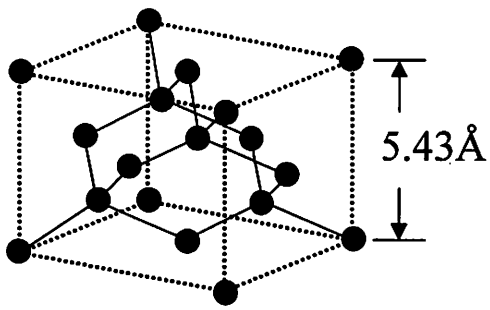


Figure 6.12 Silicon crystal structure. The lattice constant, a=5.43Å

Table 6.1 Surface energies in silicon [16].

Plane	**γ (J/m^2)**
{111}	2.07
{110}	2.62
{100}	2.93

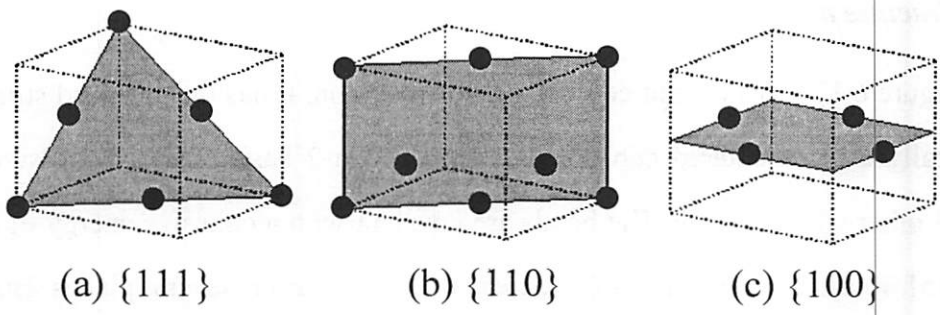


Figure 6.13 Three important planes in silicon.

The cleaved surface of a brittle crystalline solid would ideally be perfectly flat without any steps or roughness. However, the surface can show fractographic features as Figures 6.5, 6.6, 6.9, and 6.11. There might be several reasons: (i) The interaction of propagating crack with stress waves reflected from the surfaces of material. These can perturb the local crack field, resulting in alteration of the crack trajectory. (ii) Variations in applied load (mixed fracture modes). Accordingly, the crack front can be accelerated or decelerated, causing the uneven fracture surfaces. (iii) The interaction of the crack with preexisting or grown-in dislocations, etc [17]. The faint lines (river patterns) of Figure 6.6 are of particular interest. Again, the non-implanted silicon (the river patterned region) was broken by crack propagation from implanted region (the smooth region in the figure), and these lines initiated at the implant – non-implant boundary. Since the implanted wafer is Si (100), the crack tip stress field is believed to be along the {100} plane. Figure 6.14 illustrates a possible situation during crack propagation at the boundary. The plane of the paper represents a boundary of implanted – non-implanted regions, a $(1\bar{1}0)$ section of a silicon crystal. A straight crack on (001) plane (represented as the dotted line) has propagated away from the observer (implanted region) and has impinged on the crystal (non-implanted region) behind the paper. Since (001) is not a favored cleavage plane of silicon, the crack seeks new planes to follow, most likely {111} or sometimes {110} in silicon. When the crack follows the new orientation in the new plane, it reinstates along

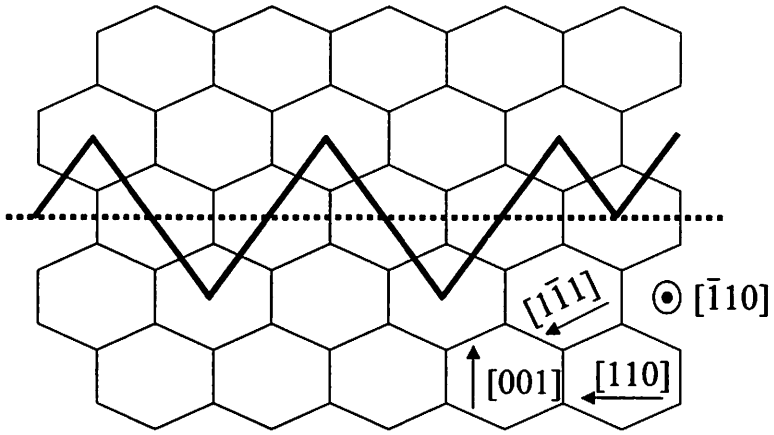


Figure 6.14 Possible crack propagation at the implant – non-implant boundary. The plane of the paper represents the boundary, a (1$\bar{1}$0) section of a silicon crystal. A straight crack on (001) plane (the dotted line) has propagated away from the observer (implanted region) and has impinged on the crystal (non-implanted region) behind the paper. Since (001) is not a favored cleavage plane of silicon, the crack seeks new planes to follow, most likely {111} or sometimes {110} in silicon.

the line formed by the crack tip, since the line represents the highest stress concentration at the edge of the non-implanted region. The many reinstated cracks then interact with their stress fields to join and form a new continuous crack front. This crack joining process makes the cleavage steps behind. Therefore the faint lines (river patterns) due to the cleavage steps show the direction of the crack propagation. From the river patterns in Figure 6.6, we can conclude the crack propagated along the <110> direction, and even if a crack started from <100> direction due to a tilted boundary, the crack changed its direction to <110> [Figure 6.6(b)]. This implies that the favored crack propagation direction is <110>. In a silicon (100) plane, the <110> has the highest atomic density direction with an inter-atomic distance of $a/\sqrt{2} = 3.84$ Å, while a= 5.43 Å for <100>, the second dense direction. It has been known that in covalent crystals, the crack tip stability is dependent upon the lattice trapping, and is related to the number of bonds to be broken [18]. That is,

crack propagation is easiest and most stable along the high atomic density directions, and those are <110> in {100}, <1$\bar{1}$0> in {100}, and <1$\bar{1}$0> in {111}, respectively.

6.5.3 Limitations in Thermal Cleavage

In the case of 16-4 SQUARE (FIA=36%) splitting, it took more time for cleavage occurring than the blanket and 10-10 SQUARE (FIA=75%) splitting, especially at lower temperatures (Figure 6.10). We speculate that this phenomenon is due to the areal ratio of the implanted to the non-implanted areas, and its effects in localized build-up of hydrogen pressure in the implanted regions only. In case of 10-10 SQUARE splitting, the cracking times are comparable with the blanket (FIA= 100%) splitting, since the implanted area is bigger than the non-implanted area with a ratio of 3:1, while in 16-4 SQUARE splitting, the implanted area is smaller than non-implanted area with a ratio of 0.56:1. Therefore more time is required for the hydrogen flux to supply bubble nucleation that creates enough stress for the silicon cleavage.

Figure 6.15 illustrates a possible scenario occurring inside the hydrogen-implanted region for the thermal-cut approach. Upon heating to the 550~700 °C range, hydrogen-induced micro-cracks become fully developed [19]-[21]. The crack tip (point C in Figure 6.15) then exerts a lateral stress to propagate through the non-implanted region. The maximum lateral stress at the crack tip, σ_C, can be expressed as [22]

$$\sigma_C = k_t \sigma_t = (1 + 2\sqrt{d/\rho})\sigma_t \qquad (6.1)$$

where k_t is a stress-concentration factor reflecting the crack tip geometry effect on the local crack tip stress, σ_t is normal stress exerted by hydrogen pressure, $2d$ is the crack dimension, and ρ is the radius of curvature of the crack tip. For the crack propagation through the non-implanted region, σ_C should exceed the fracture strength of crystalline

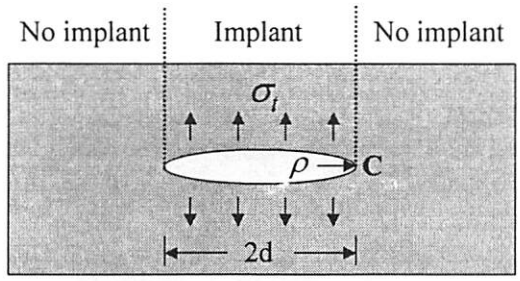


Figure 6.15 Fully-developed micro-crack inside the hydrogen implanted region in thermal-cut. Due to the elliptical geometry of a crack, the stress at the crack tip is enhanced by the factor in (6.1)

silicon. In the thermal cut method, σ_i is determined by the effective hydrogen gas pressure that is directly related to the hydrogen dose and FIA, and d is determined by the implantation mask opening related to the FIA. If the hydrogen dose is less than a certain value ($\sim 4\times10^{16}$ cm^{-2} for 100% FIA), or the FIA is under a certain value ($\sim$ 20% for 5×10^{16} H$^+$/cm^2), σ_C cannot exceed the fracture strength of non-implanted silicon, therefore layer transfer fails.

6.5.4 Mechanical Cleavage of Pattern-implanted Silicon

Figure 6.16 illustrates a probable situation occurring in silicon cleavage by mechanical bending. Due to the high dose hydrogen implantation that produces damage such as the breaking of Si-Si bonds to form hydrogen-decorated complexes in the crystal lattice (section 3.2), it becomes easier to crack along the highly damaged region [23], [24]. Upon applying a bending moment from both sides of the bonded wafer pair, a micro-crack will develop from the edge of the wafer. When the crack tip encounters the non-implanted region, the lateral stress can be expressed similarly as (6.1),

$$\sigma_C = k_m \sigma_m \tag{6.2}$$

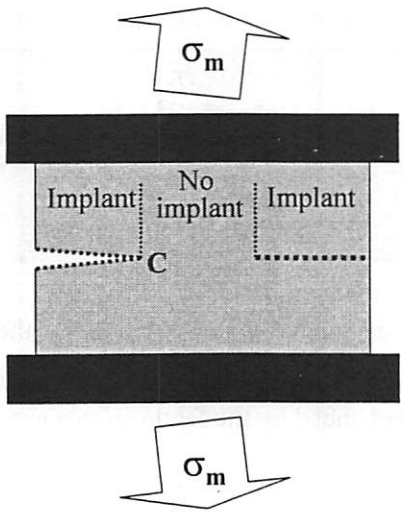


Figure 6.16 Edge-initiated cracking by mechanical bending

where k_m is a stress-concentration factor for the crack tip geometry in Figure 6.16, and σ_m is the applied mechanical stress [22]. In the mechanical cut method, the externally applied stress, σ_m, can be arbitrarily large. When σ_C exceeds the fracture strength of silicon, the successful layer transfer can happen for even small FIA samples. Furthermore, with edge initiated cracking, the stress enhancement at the tip is amplified further by a characteristic fraction of the crack opening.

6.6 Summary

The ion-cut silicon layer transfer with patterned implantation of hydrogen was demonstrated for various mask shapes and sizes. As shown in this work, 16 μm × 16 μm non-implanted area can be cleaved by implanting hydrogen ions in only 4 μm of the implanted opening around it (16-4 SQUARE pattern, FIA=36%). Crack propagation through a non-implanted region was found to favor the <110> direction, and the cleaved surface of sili-

con (111) surface was smoother than (100). The FIA effect on layer transfer time was shown for different temperatures, and it was observed that the layer transfer failed for an FIA of 20% or less in the thermal cleavage process. As an alternative to the thermal cut, a mechanical cleavage process was demonstrated, and shown that the cleavage propagation distance can be longer than the thermal cut with relatively similar roughness.

In the thermal cut method, hydrogen gas expansion is limited by the hydrogen dose and FIA, and no layer transfer can be achieved for non-implanted gaps larger than 20 μm or an FIA of 20% or lower. In the mechanical separation approach, one can utilize the applied stress to exceed the fracture strength of the non-implanted silicon, overcoming the limitation of the thermal cut method.

References

[1] B. H. Lee, G. J. Bae, K. W. Lee, G. Cha, W. D. Kim, S. I. Lee, T. Barge, A. J. Auberton-Herve, and J. M. Lamure, "A novel pattern transfer process for bonded SOI giga-bit DRAMs," in *1996 IEEE International SOI Conference Proceedings*, Sanibel Island, FL, 30 September – 3 October 1996, pp. 114-115.

[2] B. E. Roberds, E. J. Whang, A. Rudolph, and B. S. Doyle, "Investigation of a novel self-aligned dual gate MOSFET structure " in *1998 IEEE International SOI Conference Proceedings*, Stuart, FL, 5-8 October 1998, pp. 109-110.

[3] M. Bruel, "Application of hydrogen ion beams to silicon on insulator material technology," *Nuclear Instruments and Methods in Physics Research B*, vol. 108, pp. 313-319, 1996.

[4] C. H. Yun, D. Park, Y. K. Choi, and N. W. Cheung, "Gate oxide damage from high dose implantation of hydrogen," in *Proceedings of the Thirteenth International Conference on Ion Implantation Technology*, Alpbach, Austria, 17-22 September 2000, in press.

[5] C. H. Yun, A. B. Wengrow, N. W. Cheung, Y. Zheng, R. J. Welty, Z. F. Guan, K. V. Smith, P. M. Asbeck, E. T. Yu, and S. S. Lau, "Transfer of patterned ion-cut silicon layers," *Applied Physics Letters*, vol. 73, pp 2772-2774, 1998.

[6] C. H. Yun, A. B. Wengrow, N. W. Cheung, Y. Zheng, R. J. Welty, Z. F. Guan, K. V. Smith, P. M. Asbeck, E. T. Yu, and S. S. Lau, "Ion-cut silicon layer transfer with patterned implantation of hydrogen," in *Proceedings of the Ninth International Symposium on Silicon-on-Insulator Technology and Devices*, Seattle, WA, 2-7 May 1999, pp. 125-130.

[7] C. H. Yun and N. W. Cheung, "Fractional implantation area effects on patterned ion-cut silicon layer transfer," in *1999 IEEE International SOI Conference Proceedings*, Rohnert Park, CA, 4-7 October 1999, pp. 129-130.

[8] C. H. Yun and N. W. Cheung, "Mechanical transfer of silicon layer by selective surface area implantation of hydrogen," in *Thirteenth International Conference on Ion Implantation Technology. Abstracts*, Alpbach, Austria, 17-22 September 2000, p. P1-5.

[9] S. N. Farrens, J. R. Dekker, J. K. Smith, and B. E. Roberds, "Chemical free room temperature wafer direct bonding," *Journal of the Electrochemical Society*, vol. 142, pp. 3949-3955, 1995.

[10] C. D. Beachem, "Microscopic fracture processes," in *Fracture: an advanced treatise*, vol. I, H. Liebowitz, Eds. New York: Academic, 1968, pp. 243-349.

[11] G. Michot, "Fundamentals of silicon fracture," *Crystal Properties & Preparation*, vol. 17-18, pp. 55-98, 1988.

[12] J. A. Hauch, "Dynamic fracture in brittle materials," Ph.D. dissertation, University of Texas at Austin, TX, 1998, pp. 105-108.

[13] J. F. Ziegler, *TRIM (the Transport of Ions in Matter) – 1998 Program*, IBM Research, Yorktown, NY, 1998.

[14] Q. Y. Tong, R. Scholz, U. Gösele, T. H. Lee, L. J. Huang, Y. L. Chao, and T. Y. Tan, "A smarter-cut approach to low temperature silicon layer transfer," *Applied Physics Letters*, vol. 72, pp. 49-51, 1998.

[15] C. Kittel, *Introduction to Solid State Physics*, 6th ed. New York: Wiley, 1986, p. 55.

[16] C. P. Chen, M. H. Leipold, "Fracture toughness of silicon," *American Ceramic Society Bulletin*, vol. 59, pp. 469-472, 1980.

[17] D. R. Clarke, "Fracture of silicon and other semiconductors," in *Semiconductors and Semimetals*, vol. 37, R. K. Willardson, A. C. Beer, and E. R. Weber, Eds. San Diego: Academic, 1992, pp. 189-230.

[18] C. Hsieh and R. Thomson, "Lattice theory of fracture and crack creep," *Journal of Applied Physics*, vol. 44, pp. 2051-2063, 1973.

[19] Q. Y. Tong, T. H. Lee, K. Gutjahr, S. Hopfe, and U. Gösele, "Layer splitting process in hydrogen-implanted Si, Ge, SiC, and diamond substrates," *Applied Physics Letters*, vol. 70, pp. 1390-1392, 1997.

[20] M. K. Weldon, V. E. Marsico, Y. J. Chabal, A. Agarwal, D. J. Eaglesham, J. Sapjeta, W. L. Brown, D. C. Jacobson, Y. Caudano, S. B. Christman, and E. E. Chaban, "On the mechanism of the hydrogen-induced exfoliation of silicon," *Journal of Vacuum Science & Technology B*, vol. 15, pp. 1065-1073, 1997.

[21] M. Bruel, "Separation of silicon wafers by the smart-cut method," *Materials Research Innovations*, vol. 3, pp. 9-13, 1999.

[22] R. W. Hertzberg, *Deformation and Fracture Mechanics of Engineering Materials*, 4th ed., New York: Wiley, 1996, pp. 273-275.

[23] W. G. En, I. J. Malik, M. A. Bryan, S. Farrens, F. J. Henley, N. W. Cheung, and C. Chan, "The Genesis process: a new SOI wafer fabrication method," in *1998 IEEE International SOI Conference Proceedings*, Stuart, FL, 5-8 October 1998, pp. 163-164.

[24] K. Henttinen, I. Suni, and S. S. Lau, "Mechanically induced Si layer transfer in hydrogen-implanted Si wafers," *Applied Physics Letters*, vol. 76, pp. 2370-2372, 2000.

Chapter 7

SEMICONDUCTOR MEMBRANE AND SEALED CAVITY FABRICATION

Abstract- Silicon and oxide membranes were fabricated using ion-cut layer transfer process, which is suitable for sub-micron-thick membrane fabrication with good thickness uniformity and surface micro-roughness. After hydrogen ions were implanted into a silicon wafer, the implanted wafer was bonded to another wafer that has patterned cavities of various shapes and sizes. The bonded pair was then heated until hydrogen induced silicon layer cleavage occurred along the implanted hydrogen peak concentration, resulting in the transfer of the silicon layer from one wafer to the other. Using this technique, we have been able to form sealed cavities and channels of various shapes and sizes up to 50 μm-wide with a 1.6 μm-thick silicon membrane. As a process variation, we also have fabricated silicon dioxide membranes for optically transparent applications.

7.1 Introduction

Silicon membranes on top of buried cavities and channels have many applications in micro-mechanical and biochemical sensors [1], [2]. Until now, these structures have been fabricated using silicon wafer bonding at high temperature (~1000 °C), followed by etching-back the top wafer until the membranes are formed [3]. However, this bonding and etch-back process takes a considerable amount of time for the etch-back step, and is not cost effective in its use of wafers. In addition, the control of the membrane thickness

and uniformity require stringent etch-stop mechanisms. As an alternative, hydrogen induced silicon layer transfer (ion-cut) technology can be shown to be a more efficient method to fabricate these membranes over buried cavities [4].

The ion-cut method has been employed previously for the fabrication of silicon-on-insulator wafers [5]. The principle of this process consists of hydrogen ion implantation into a silicon donor wafer followed by low temperature direct wafer bonding to a silicon handle wafer. This bonded pair is then heated until hydrogen induced silicon layer cleavage occurs along the implanted hydrogen peak concentration region, resulting in the silicon layer transfer from the donor wafer to the handle wafer. The as-cleaved thickness uniformity of the ion-cut layer can be better than 10 nm across a 100 mm wafer with a surface roughness of less than 12 nm RMS [5].

7.2 Experimental

7.2.1 Silicon and Silicon-on-insulator Membrane Fabrication

Figure 7.1 shows the silicon membrane fabrication process using the ion-cut technique. The silicon donor wafers were implanted to a hydrogen dose range between 4~8 × 10^{16} ions/cm^2 with energies of 40, 80, or 180 keV. On the silicon handle wafer, 200 nm of thermal oxide was grown and patterned with a variety of 1~2 μm-deep cavities and channels by reactive ion etching with two steps for the oxide and silicon. The two wafers were then bonded directly face-to-face at ambient temperature and pressure after standard RCA cleaning and oxygen plasma surface activation for a better bonding interface [6] (see also section 2.3). The bonding interface was cured further at 200 °C for 10 hours.

The bonded wafer pair was then placed in a heater at 470~550 °C until hydrogen induced silicon layer cleavage took place. As a result, the cavities and channels were sealed with a silicon layer transferred from the hydrogen implanted donor wafer.

Silicon-on-insulator (SOI) membranes on top of buried cavities can be formed with slight changes of the process sequence for the silicon membrane fabrication. The difference is that hydrogen is implanted through a thermally oxidized wafer, so that the SiO_2/Si bi-layer is transferred.

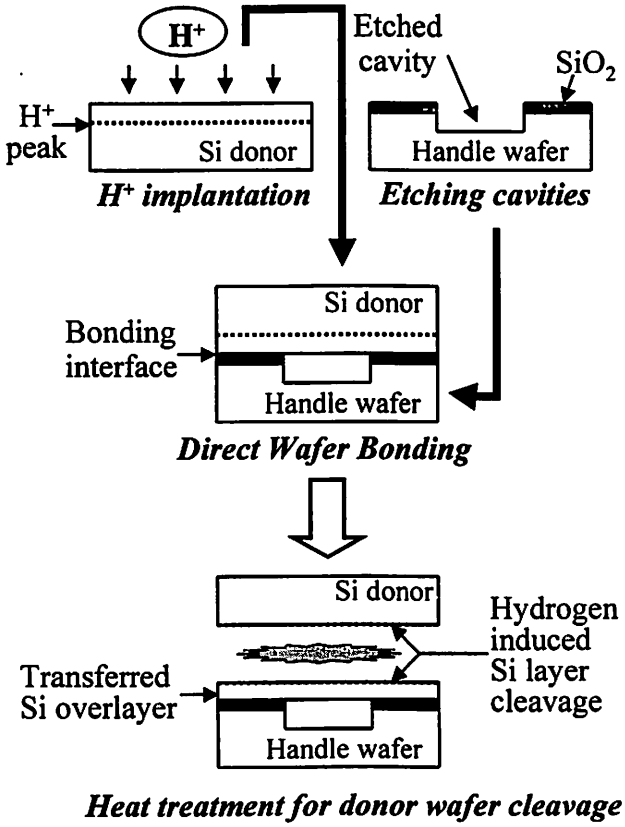


Figure 7.1 Process flow for Si membrane fabrication using ion-cut layer transfer. To fabricate an SOI membrane, an oxidized wafer can be used in place of Si donor wafer for SiO_2/Si bilayer transfer.

Since the silicon layer cleavage occurs at a depth corresponding to the peak concentration of the hydrogen implantation profile [5], and the hydrogen peak position is uniquely determined by the ion implantation energy, the Si or SOI membrane thickness can be tailored by controlling the hydrogen ion energy.

7.2.2 Oxide Membrane Fabrication

For optically transparent membrane fabrication, Figure 7.2 illustrates the oxide (SiO_2) membrane fabrication from the SOI membrane formed through the process described above. After forming SOI membranes, vapor-phase xenon difluoride (XeF_2) was used to etch away the top silicon layer to fabricate oxide membranes. Since XeF_2 has very high silicon etch selectivity over silicon dioxide [7], we could fabricate thin (~100 nm) and uniform oxide membranes over etched cavities.

7.3 Results

Figure 7.3 shows scanning electron micrographs (SEM) of cross-sections of Si [Figure 7.3(a)] and SOI [Figure 7.3(b)] membranes fabricated through the ion-cut layer trans-

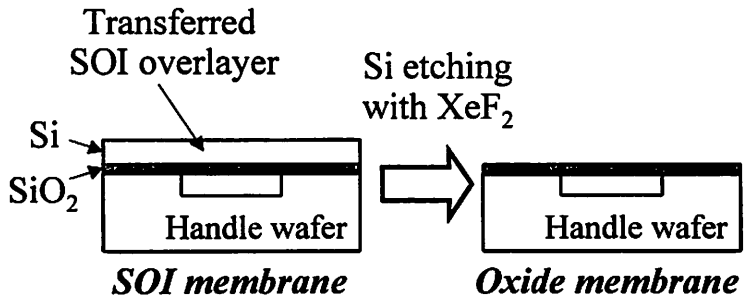


Figure 7.2 Oxide membrane fabrication process from an existing SOI membrane using XeF_2 vapor-phase isotropic dry etching. Since XeF_2 has very high silicon etch selectivity over silicon dioxide, a thin and uniform oxide membrane can be fabricated.

fer process described in part A of the previous section. The cavities were sealed as processed, and cleaved across for the cross-sectional SEM. In Figure 7.3(a), the cavity is 5 μm-wide and 2 μm-deep, and capped with a 0.5 μm-thick single-crystal silicon membrane. The silicon top layer was transferred from a silicon donor wafer implanted by 4×10^{16} H^+/cm^2 at 40 keV. In Figure 7.3(b), the 8 μm-wide and 1 μm-deep cavity is sealed with an approximately 0.5 μm-thick SOI (including the 60 nm-thick oxide underneath) overlayer. The donor wafer was a 60 nm-thick oxide grown silicon wafer, and it was implanted with hydrogen at 40 keV to the dose of 8×10^{16} ions/cm^2. After the ion-cut layer transfer, the oxide layer of the donor wafer became the buried oxide layer of the SOI membrane. In order to determine the uniformity of the transferred SOI film, the top silicon layer thickness was measured by an optical interferometric method [8]. As we can see from the values in Figure 7.4(a), the transferred silicon layer thickness uniformity is less than 0.3 % across a 100 mm wafer. The surface micro-roughness of the silicon membrane was measured to be 6 nm rms with an atomic force microscope (AFM) scan over 2 μm × 2 μm region [see Figure 7.4(b)].

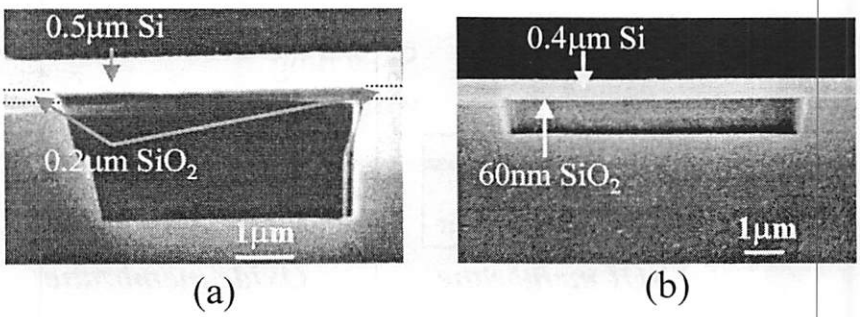


Figure 7.3 SEM cross-sections of 0.5 μm-thick Si (a) and SOI (b) membranes. The SOI membrane is a Si/SiO_2 bilayer composed of 0.4 μm-thick silicon and 60 nm-thick oxide.

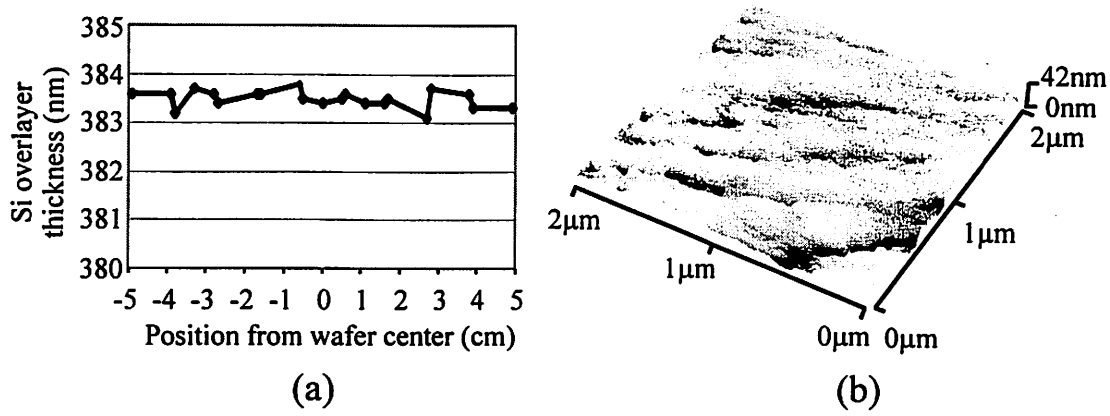


Figure 7.4 (a) Silicon top layer thickness values obtained from optical interferometric measurement. The thickness uniformity across a 100 mm wafer is better than 0.3%. (b) AFM scan over a membrane. The as-cleaved surface micro-roughness is 6 nm. All data was taken from 0.5 μm-thick SOI membranes.

Figure 7.5(a) shows optical microscopic top views of silicon handle wafers patterned with three elbow-shaped parallel channels (left picture) and the channels covered with transferred SOI layer (right picture). As we can see from the right picture of Figure 7.5(a) and its SEM cross-section [Figure 7.5(b)], those channels are covered with SOI layer after the ion-cut layer transfer process. The optical micrographs in Figure 7.6 show four different sealed cavities with more complicated layout shapes (i.e., the numbers "1", "2", "5", and "7"). The bright regions are 2 μm-deep buried cavities sealed with a 0.5 μm-thick silicon overlayer. This work demonstrates that various shapes of sealed channels and cavities can be fabricated, and applied to micro-storage or transport systems.

Figure 7.7 shows the oxide membrane formed by the fabrication process illustrated in Figure 7.2. Figure 7.7(a) shows the optical microscopic top view of various shapes of oxide membranes. The bright regions are buried cavity areas covered with a 100 nm-thick

oxide layer. Figure 7.7(b) shows an SEM cross-section of a cavity sealed with the oxide layer.

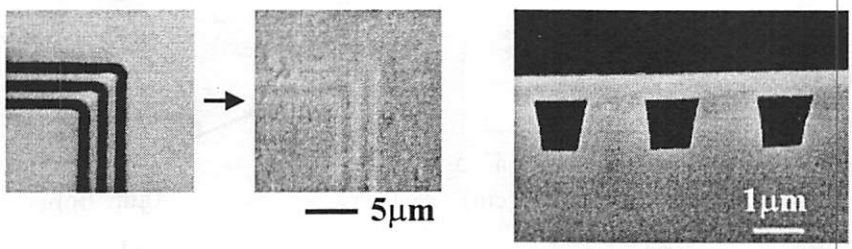


Figure 7.5 (a) Optical micrographs of elbow-shaped channels before (left) and after (right) the coverage of a 0.5μm-thick SOI membrane. The dark lines in the left picture show etched channels, while the bright lines in the right picture show those same channels now sealed with a SOI layer. (b) SEM cross-section of the SOI membrane over buried channels.

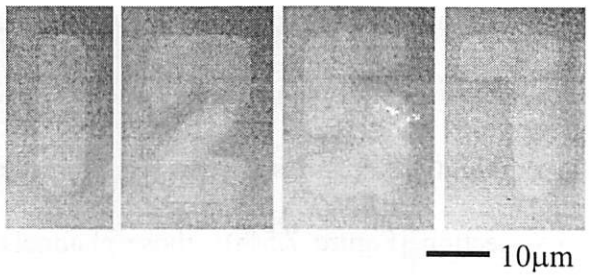


Figure 7.6 Optical micrographs of various cavity shapes (numbers "1", "2", "5", and "7") with depth of 2 μm sealed with a 0.5 μm-thick silicon layer.

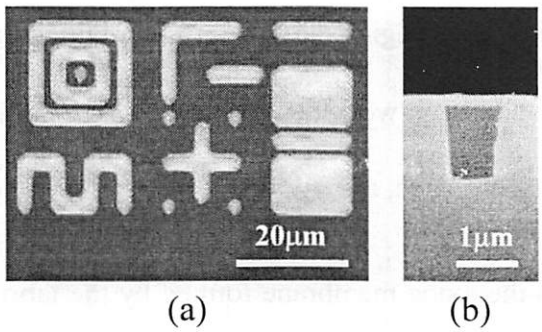


Figure 7.7 (a) Optical micrograph of various cavity shapes sealed with a 0.1 μm-thick SiO_2 layer, where bright regions indicate the membranes. (b) SEM cross-section of a cavity sealed with an oxide membrane.

In order to determine the silicon membrane formation dependence on cavity feature size, we patterned various widths and lengths (1~100 μm, respectively) of rectangular trenches on a handle wafer, and transferred various thicknesses of silicon layers from silicon donor wafers. As we have discussed earlier, thickness can be adjusted by the energy of H^+ implantation, and we transferred three different silicon layer thicknesses of 0.5 μm, 0.8 μm, and 1.6 μm. As a result of this experiment, Figure 7.8 shows the process window for membrane fabrication using the ion-cut method. The width (W), in this chart, refers to the short dimension of the trenches. For example, with the 1.6 μm-thick silicon layer transfer, we have been able to seal cavities up to about 50 μm-wide without any constraints in length. The success/failure border was determined by plotting the data of maxi-

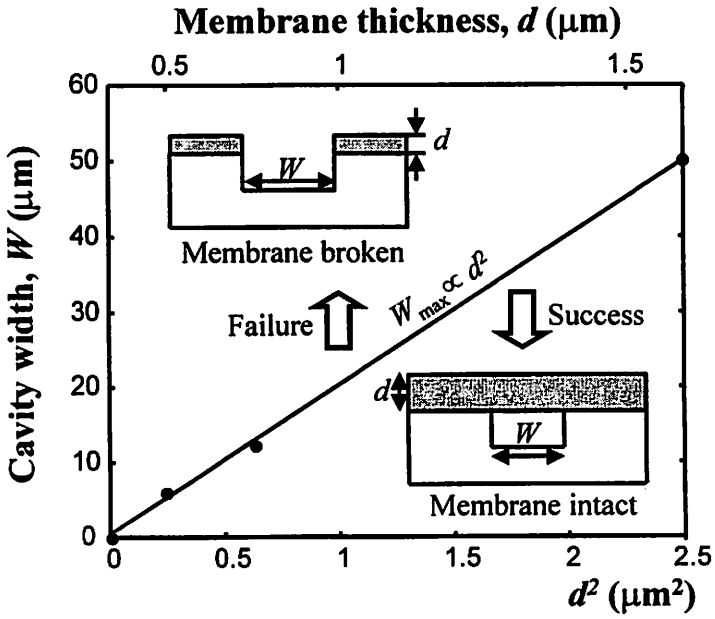


Figure 7.8 Process window for silicon membrane fabrication in terms of cavity width vs. membrane thickness. The success/failure border, fitted from experimental data, shows the maximum sealed cavity width achievable with a fixed membrane thickness.

mum achievable membrane width (W_{max}) with each membrane thickness (d). Figure 7.9 shows one example of a broken membrane (d= 0.5 μm, W= 10 μm). As we can see from this tilted SEM top view, the transferred silicon layer was broken and could not seal the elbow-shaped channels.

7.4 Discussion

From the process window chart (Figure 7.8), we observed that the maximum membrane width is increasing proportional to the square of the membrane thickness. To explain this $W_{max} \propto d^2$ relation, we propose the following model. During the thermal annealing step for layer transfer, H_2 molecules are formed and segregated around the implanted hydrogen peak in a silicon donor wafer [9], [10]. The high pressure inside the coalesced hydrogen bubbles is the driving force for the silicon layer cleavage. If there is no local stiffening force provided by the bonded wafer for lateral bubble expansion, the pres-

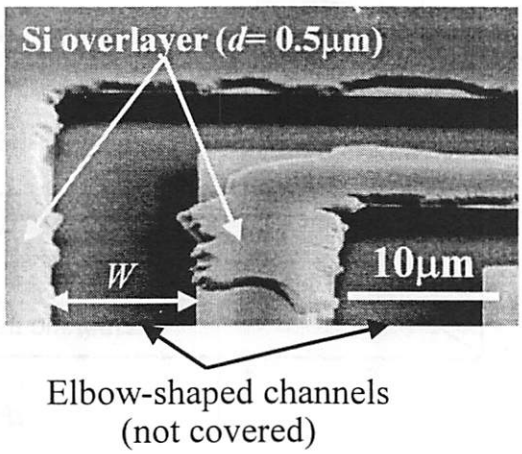


Figure 7.9 SEM tilted view showing broken transferred silicon layer and coverage failure across elbow-shaped channels. In this case, the channel width (W) is 10 μm and silicon overlayer thickness (d) is 0.5 μm.

surized bubbles will exert vertical force to the donor wafer surfaces. When this vertical lifting-off pressure becomes greater than silicon yield or fracture strength, silicon surface blistering or flaking is developed. Figure 7.10 illustrates the situation of blister formation in a cavity. To prevent the formation of blistering inside a cavity resulting in layer transfer failure, cavity width (W) must be smaller than the blister diameter ($2a$). In that way, cavity edges of the handle wafer can provide a restoring force that opposes the vertical lift-off of the blister. Blister diameter ($2a$) can be related to blister thickness (d) by modeling blister as uniformly loaded circular plate. With a uniform pressure loading (p) over the entire blister surface inside, the maximum stress at the edge of the blister is given by [11]

$$\sigma = \frac{3}{4} p \frac{a^2}{d^2} . \tag{7.1}$$

Shearing force balance at the edge of the shell is expressed as

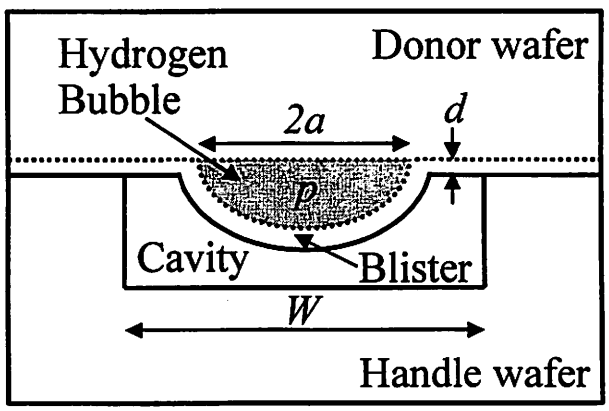


Figure 7.10 Model of hydrogen induced silicon surface blistering inside a cavity. To prevent the bursting of a blister, the cavity width (W) must be smaller than the blister size ($2a$), so that the cavity edge of the handle wafer can provide a stiffening force that opposes the vertical lift-off motion of the blister.

$$\pi a^2 p = 2\pi a Q \tag{7.2}$$

where Q is the shear force per unit length of the cylindrical section of radius a. Solving (7.2) for p, and putting it into (7.1) yields

$$\sigma = \frac{3}{4} Q \frac{2a}{d^2} \,. \tag{7.3}$$

The critical shear force per unit length for bursting blister is then

$$Q_{crit} = \frac{4}{3} \sigma_F \frac{d^2}{2a} \tag{7.4}$$

where σ_F is the fracture strength of silicon. With constant values of Q_{crit} and σ_F in silicon, $2a$ is proportional to d^2. Since cavity width (W) should be smaller than blister size ($2a$) for layer transfer over the cavity, therefore $W_{max} \propto d^2$.

7.5 Summary

We have demonstrated the ion-cut silicon layer transfer process to seal cavities and channels with well-defined thickness uniformity and surface micro-roughness of single-crystal silicon, SOI, and oxide membranes. Process window, in terms of membrane thickness vs. cavity width, has been determined. Using this technique, approximately 50 μm-wide cavities have been sealed with transferred 1.6 μm-thick silicon.

References

[1] L. Parameswaran, A. Mirza, W. K. Chan, and M. A. Schmidt, "Silicon pressure sensors using a wafer-bonded sealed cavity process," in *Proceedings of the 1995 Inter-*

national Solid-State Sensors and Actuators Conference – TRANSDUCERS '95, Stockholm, Sweden, 25-29 June 1995, pp. 582-585.

[2] P. C. Simpson, A. T. Woolley, and R. A. Mathies, "Microfabrication technology for the production of capillary array electrophoresis chips," *Biomedical Microdevices*, vol. 1, pp. 7-25, 1998.

[3] J. M. Noworolski, E. Klaassen, J. Logan, K. Petersen, and N. I. Maluf, "Fabrication of SOI wafers with buried cavities using silicon fusion bonding and electrochemical etchback," *Sensors and Actuators A*, vol. 54, pp. 709-713, 1996.

[4] C. H. Yun and N. W. Cheung, "SOI on buried cavity patterns using ion-cut layer transfer," in *1998 IEEE International SOI Conference Proceedings*, Stuart, FL, 5-8 October 1998, pp. 165-166.

[5] A. J. Auberton-Herve, M. Bruel, B. Aspar, C. Maleville, and H. Moriceau, "Smart-cut: The basic fabrication process for UNIBOND SOI wafers," *IEICE Transactions on Electronics*, vol. E80-C, pp. 358-363, 1997.

[6] S. N. Farrens, J. R. Dekker, J. K. Smith, and B. E. Roberds, "Chemical free room temperature wafer to wafer direct bonding," *Journal of the Electrochemical Society*, vol. 142, pp. 3949-3955, 1995.

[7] P. B. Chu, J. T. Chen, R. Yeh, G. Lin, J. C. P. Huang, B. A. Warneke, and K. S. J. Pister, "Controlled pulse-etching with xenon difluoride," in *Proceedings of the 1997 International Solid-State Sensors and Actuators Conference – TRANSDUCERS '97*, Chicago, IL, 16-19 June 1997, pp. 665-668.

[8] M. Ohring, *The Materials Science of Thin Films*, San Diego: Academic, 1992, pp. 253-261.

[9] X. Lu, N. W. Cheung, M. D. Strathman, P. K. Chu, and B. Doyle, "Hydrogen induced silicon surface layer cleavage," *Applied Physics Letters*, vol. 71, pp. 1804-1806, 1997.

[10] M. K. Weldon, V. E. Marsico, Y. J. Chabal, A. Agarwal, D. J. Eaglesham, J. Sapjeta, W. L. Brown, D. C. Jacobson, Y. Caudano, S. B. Christman, and E. E.

Chaban, "On the mechanism of the hydrogen-induced exfoliation of silicon," *Journal of Vacuum Science and Technology B*, vol. 15, pp. 1065-1073, 1997.

[11] S. Timoshenko and S. Woinowsky-Krieger, *Theory of Plates and Shells*, 2nd ed. New York: McGraw-Hill, 1959, pp. 54-56.

Chapter 8

CONCLUSION

In order to integrate multi-functional microsystems on a single chip using various disparate materials and devices, a *paste-and-cut* approach has been proposed. The paste-and-cut technology allows each material or device to be separately synthesized and processed prior to assembly on a final substrate. Among the methods for pasting and cutting, wafer direct bonding and ion-cut can transfer any crystalline material layers from one substrate to another. In the ion-cut layer transfer process, hydrogen is implanted into a wafer that has the layer to be transferred. The implanted hydrogen ions form a highly damaged region around the hydrogen stopping range. The implanted wafer is then bonded to another wafer by low-temperature direct bonding. By appropriate heat or mechanical treatment, the bonded wafer pair separates along the highly damaged region, resulting in the transfer of the layer from one wafer to the other.

Through the review of current understanding of wafer bonding, a bonding strength exceeding the silicon fracture strength was obtained after oxygen plasma treatment of the wafer surfaces and low-temperature (~200 °C) annealing of the bonded pair.

Using a gas-driven model for hydrogen-induced silicon surface blistering and by modeling a blister as a uniformly loaded circular plate, the relation between the blister shape and the hydrogen bubble pressure was obtained, and the condition for the rupture of a blister was derived.

With the ion-cut layer transfer process, we have been able to form silicon-on-insulator (SOI) structures by transferring single- and poly- crystalline silicon layers. Comparing the layer transfer time and temperature between single- and poly- crystalline silicon, the

activation energy of poly-crystal layer transfer was ~10 times smaller than that of single-crystal layer transfer. Further work is needed to elucidate the mechanism of poly-Si ion-cut. Plasma immersion ion implantation has been shown as an alternative to the hydrogen implantation method for ion-cut. We have also fabricated silicon, SOI, and oxide membranes on buried cavities and channels, which can be used for pressure transducers, micro-fluidic systems, and radio frequency filters and resonators. In these layer transfer demonstrations, we have observed good thickness uniformity (<1 %) across the wafer and surface micro-roughness (<10 nm) of the transferred layers.

For the transfer of pre-fabricated electronic device layers, gate oxide damage was first evaluated after high-dose and high-energy hydrogen implantation through metal-oxide-silicon (MOS) transistors. The results showed that stress-induced leakage current (SILC) through the gate oxide increased as the hydrogen dose increased for the 5 nm-thick oxide. For the 1.8 nm-thick gate oxide, no SILC was observed, showing that the implantation damage is not significant for ultra-thin (< 2 nm) oxides.

To protect the thicker (>3 nm) oxides from damage during the hydrogen implantation, we have proposed and demonstrated layer transfer with patterned implantation of hydrogen, in which active device regions were masked during the implantation. This experiment showed that the hydrogen induced silicon layer cleavage is feasible even without a continuous hydrogen implantation of the entire wafer, and that the silicon cleavage can propagate across at least 16 microns of non-implanted area from a 4 micron-wide implanted region each side. By a fractographical analysis of the silicon cleavage in the non-implanted region, the favored crack propagation direction was observed to be along <110> direction, and the favored crack plane was (111) rather than (100).

Mechanical cleavage has also been demonstrated for both SOI fabrication and patterned ion-cut. For the latter case, it has shown that the mechanical cleaving can overcome some non-implantation area limitations imposed by the thermal cleavage process.

The ion-cut layer transfer presented in this dissertation may be extended to both process development and mechanism study. Wafer bonding and ion-cut at even lower temperature (ideally room temperature) is necessary especially for glass or organic substrate applications. It may also be worthwhile to extend ion-cut to amorphous materials including polymers, and wafer bonding to plastic substrates. By investigating the interface (bonding and hydrogen-created) crack propagation, it may be possible to transfer thin films using wafer bonding and mechanical cleavage, with lower or even without hydrogen implantation.