THE DESIGN AND IMPLEMENTATION OF AN ULTRA LOW POWER RF OSCILLATOR USING MICROMACHINED RESONATORS

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Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II.**

Approval for the Report and Comprehensive Examination:

Committee:

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Research Advisor

8/2/02

Date

* * * * * * *

Professor Ali Niknejad
Second Reader

8/2/02

Date

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Brian P. Otis
Berkeley, California

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Chapter 1. Introduction

1.1 Motivation

Circuit design is not simply the means to an end. Circuit innovation is both the cause and effect of an ambitious system level application and difficult specifications. Thus, the motivation of this thesis is twofold. First, progress towards an ultra low power RF transceiver for the UC Berkeley PicoRadio project is documented. Second, an RF oscillator, designed using an RF MEMS/CMOS co-design philosophy, is proposed.

The goal of this research is to demonstrate that the co-design of RF MEMS and CMOS is a powerful tool in the design of low power RF transceiver components. This will set the framework for the implementation of additional transceiver blocks using similar design philosophies. This work is a stepping stone to the implementation of an entire ultra-low power RF transceiver.

1.2 Thesis Organization

This thesis focuses on the design of an ultra low power, 1.9GHz oscillator utilizing a micromachined FBAR resonator. Chapter 2 provides the reader with the background information necessary to understand the motivations behind this research. Chapter 3 consists of an evaluation of traditional methods of frequency generation. Quartz crystal stabilized synthesizers, surface acoustic wave (SAW) oscillators,

integrated LC oscillators, and direct digital frequency synthesis are discussed. In Chapter 4, the feasibility of an FBAR based oscillator is explored. The theoretical limitations on frequency stability, power consumption, and phase noise are derived and calculated. In Chapter 5, the design of the oscillator is performed. The concept of using a resonator/circuit co-design methodology is introduced. Implementation details are discussed, including layout, packaging, and design for test. Chapter 6 reveals the experimental results including the measured frequency spectrum, phase noise performance, output power levels, and oscillator start-up time. Finally, Chapter 7 concludes the report with a summary of the measured results and recommendations for future work.

Chapter 2. Background

2.1 Introduction

To better understand the motivations behind this research, this chapter provides some brief relevant background information. The UC Berkeley PicoRadio project is introduced. The specifications for the PicoRadio RF transceiver are identified. It will be shown that the PicoRadio project demands a highly integrated, ultra low power RF transceiver. To introduce some challenges associated with ultra low power RF design, case studies about two recent low power transceiver implementations are presented.

2.2 PicoRadio Project

The PicoRadio Project at UC Berkeley is an ambitious multi-disciplinary project that attempts to merge communications theory, networking theory, and implementation expertise to create a network of autonomous sensor nodes.[1] The PicoRadio team is vertically integrated to a high degree. The team is commissioned with a wide range of tasks including proof-of-concept prototype assembly, networking and protocol design, custom integrated circuit (IC) design, and custom packaging design and fabrication.

The ultimate goal of the PicoRadio group is to create a network of sensor nodes that collect data in building environments (eg. temperature, humidity, light levels, sound levels, airflow measurements, vibration measurements). In addition to sensing

capabilities, the nodes must have actuation capabilities that control environmental parameters. Thus, closed loop control of environmental microclimates can be accomplished, greatly increasing the efficiency and/or security of the location. To reduce the installation cost, the nodes must be completely wireless and autonomous. They must be able to asynchronously form smart ad-hoc networks that eliminate data redundancy, calculate and tabulate spatial node locations, and use optimal multi-hop paths for data transmission. The physical volume of each node should be less than $1cm^3$. The most stringent requirement is that all necessary node energy must be scavenged from the environment. This eliminates the need for wire-based power or battery replacement. Through a combination of solar and vibrational energy collection, enough energy can be collected to support a 100μW average node power consumption.[1]

The node-to-node data transmission is accomplished via a wireless RF link. The desired range is 10m, and the necessary data rate is 10kbps. This transceiver must exhibit a high level of integration to ensure a small form factor. Most importantly, the power consumption of the transceiver must be extremely low to allow total energy scavenging. The transceiver will be heavily duty-cycled, and will be on for approximately 1% of the time. To allow an average power dissipation of 10μW from the transceiver, the power dissipation while active must be 1mW. Many existing ultra-low power transceivers operate at low frequency ISM bands (434MHz). However, to enable small passive components (eg., inductors and antennae) for a high level of integration it is desirable to operate at a relatively high carrier frequency, such as 2-2.4GHz. Finally, to achieve a low cost solution, the circuitry must utilize standard submicron CMOS. These very

aggressive specifications provide motivation to investigate new technologies and RF design philosophies.

2.3 Ultra Low Power RF Systems

To provide motivation for low power oscillator research, it is instructive to briefly investigate existing ultra low power RF transceivers. This section will discuss, in case-study format, two recent successful implementations of ultra low power radios.

2.3.1 434MHz Direct Conversion Transceiver

One recent implementation has supplied not only interesting results to the low power RF design community, but also valuable insight into design philosophies that help enable low power CMOS RF circuit design.[2] A few of these will be summarized below:

- *For ultra-low power designs, g_m/I_d should be maximized by operating in moderate or weak inversion*
- *Bandwidth is severely limited in moderate and weak inversion, thus a relatively low carrier frequency (434MHz) was used*
- *A carrier frequency this low makes on-chip inductors very large; an off-chip SMD inductor was used in this design*
- *To avoid signal loss, DC control loops and DC coupling were used to eliminate the need for AC coupling capacitors*

Using the design philosophies stated above, this transceiver achieved a power dissipation of 1mW in receive mode with a 24kbps bitrate. Though this is a testament to the controversial use of CMOS in ultra low power RF systems and the skill of the designers, there are some issues that deserve mention. First, an inherent tradeoff between the level of integration and power consumption is observed. By operating at a low carrier frequency to reduce power consumption, the use of off-chip passives is necessitated. The next interesting observation is that, out of the 1mW receiver power budget, 63% is consumed by the frequency synthesizer. The frequency divider and voltage-controlled oscillator (VCO) are the main contributors. If this receiver were scaled up in carrier frequency to the GHz range, the synthesizer power consumption would increase dramatically.

2.3.2 1GHz Super-Regenerative Receiver

Super-regenerative receivers have faced extinction for decades until the concept was rediscovered by ultra low power transceiver designers. The concept of a super-regenerative receiver provides the promise of a high level of integration and very low power consumption. No frequency mixers are used. Instead, a high quality factor (Q) filter is synthesized from a low-Q LC tank by adding a negative resistance to cancel out the positive tank-loss resistance. This system is allowed to oscillate periodically, and the start-up time of the oscillation is measured. As the input signal level increases, the start-up time decreases. Impressive sensitivities are achieved with very little power consumption.

One recent implementation of a 1GHz super-regenerative receiver in 0.35μm CMOS achieves a 1.2kbps bitrate at a very low sensitivity of −113dbm while consuming1.2mW.[3] The oscillator, which is the most critical component of this design, used an off-chip inductor and variable capacitor. Since the tuning is set by the LC oscillator tank, and not a reference crystal, manual trimming is necessary to receive the desired frequency band. In addition, of the entire power budget of 1.2mW, the oscillator alone consumed 780μW (65%).

These case studies show that substantial research has been done in the area of ultra low power, low data rate CMOS transceivers. However, there are some inherent tradeoffs that are troublesome for system level implementations. As the frequency of operation increases, power dissipation invariably increases. As the frequency of operation is decreased to lower the power consumption, full integration of the passive components becomes difficult. Further, the main source of power dissipation in both of the aforementioned ultra low power receivers was the frequency generator. These findings set the stage for research into alternate methods of frequency generation in hopes of breaking the standoff between low power consumption and high levels of integration. The next chapter explores the traditional methods of frequency generation.

Chapter 3. Traditional Frequency Generation

3.1 Introduction

The heart of all narrowband RF systems is the frequency generator. Used to generate the transmitted carrier frequency and the local oscillator (LO) signal, a stable, low-noise RF sinusoid generator is crucial for the performance of an RF link. As discussed in the previous chapter, the frequency generator typically dominates the receiver power consumption in low power transceivers. The performance of a frequency generator is typically measured using some (or all) of the following criterion:

- *Fabrication Tolerance* – Measured in parts per million (ppm), this metric predicts the stability of the oscillation frequency over process variations of all oscillator components (eg. capacitors, resonators, transconductors, etc).

- *Phase Noise* – The phase noise performance of a sinusoid generator is measured in decibels below the carrier per Hertz (dBc/Hz). To see the effects of oscillator parameters on the short term stability of a free-running oscillator, it is instructive to note the simple Leeson model for phase noise as a function of offset frequency:[4]

$$L(\Delta\omega) = 10\log\left[\frac{2FkT}{P_{signal}} * \left(\frac{\omega_{osc}}{2Q\Delta\omega}\right)^2\right] \quad (3.1)$$

Where L is the phase noise in (dBc/Hz) as a function of the offset frequency $\Delta\omega$, F is the oscillator noise figure, Q is the loaded quality factor of the resonator, and P_{signal} is the signal power at the input to the oscillator.

- *Long Term Stability* – The long term stability of an oscillator is determined by the sensitivity of the oscillation frequency to temperature, supply voltage, and aging.

- *Power Consumption* – The power consumption of the frequency generator is of utmost importance in most applications. In the field of sensor node transceivers, as mentioned in Chapter 1, extremely low power dissipation is crucial for the success of the system.

- *Ability to Control Frequency* – Intentional frequency variation is often desirable. For example, frequency calibration, channel switching, and frequency modulation all require active control over the output frequency. In these systems, frequency control accuracy, switching time, and control range are important parameters for these systems.

- *Level Of Integration* – Increasing the level of integration decreases the form factor of the system, and, most importantly, decreases cost. It will be shown that there

are performance and efficiency compromises that are often made when increasing the level of integration.

This chapter explores different varieties of frequency generation mechanisms and evaluates them in terms of the criterion defined above.

3.2 Quartz Crystal Stabilized Synthesizer

For high performance RF systems, the frequency generation mechanism of choice is a crystal oscillator stabilized synthesizer. The synthesizer utilizes a phase locked loop (PLL) or delay locked loop (DLL) to "synthesize" a high-frequency sinusoid from a low frequency reference. A simplified classical PLL topology is shown in Figure 1.

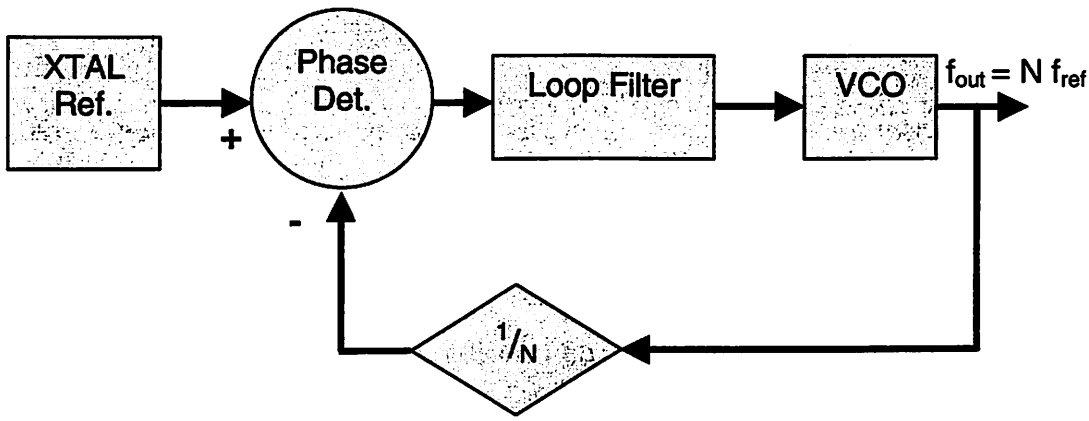

Figure 1. Classical Crystal Stabilized PLL

As shown in the Figure 1 above, a low frequency crystal reference oscillator (usually 1-100MHz) drives a negative feedback loop. The frequency divider in the feedback path

ensures an output frequency that is N times higher than the reference frequency. The voltage-controlled oscillator (VCO) is either a tunable resonant oscillator or a tunable ring oscillator. This architecture is frequently used because of the following attributes:

- The RF output frequency is fundamentally tied to the stable crystal reference
- Typical crystals achieve a fabrication tolerance of better than +/- 100ppm
- Aging stability of crystals is < 10ppm/year
- Crystal temperature stability is approximately 0.6ppm/°C (depending on cut)[5]
- A quantized control over output frequency is achievable by changing N
- Crystal oscillators can achieve very low phase noise

For these reasons, a crystal oscillator stabilized PLL or DLL is found in most RF systems. However, there are several issues with this topology that limit its usefulness. First, although the phase noise of the reference crystal oscillator is very low, the low Q of the VCO and finite loop bandwidth of the PLL severely degrade the phase noise of the entire system. Assuming that the reference oscillator is less noisy than the open loop VCO, Figure 2 depicts an approximation of the phase noise makeup of a frequency synthesizer.[6]

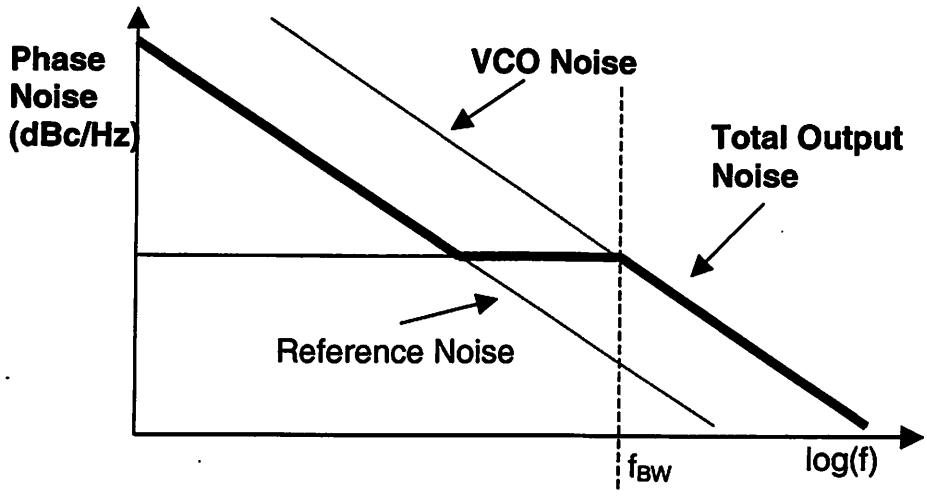

Figure 2. Frequency Synthesizer Phase Noise Contributions

Figure 2 plots phase noise vs. carrier offset frequency. As predicted by the Leeson model (equation (3.1) above), the phase noise of the open loop reference oscillator falls off at -20dB/decade and is lower at a given offset frequency than the open loop VCO. The phase noise of the crystal reference is much lower than the VCO because the Q of quartz crystal resonators is very high (>100,000). At offset frequencies above f_{BW} (the loop bandwidth of the synthesizer), the total noise is dominated by the VCO phase noise. For offset frequencies below f_{BW}, the loop gain of the synthesizer suppresses the natural VCO phase noise by locking the output signal to the (relatively) clean reference signal. This portion of the synthesizer phase noise output is called the "pedestal" because the phase noise is relatively independent of frequency offset within this regime. At extremely close-in frequency offsets, the total noise is dominated by the phase noise of the reference itself. **Thus, for most systems, the synthesizer phase noise is determined by the intrinsic VCO phase noise and the PLL loop bandwidth.** Typically, the PLL loop bandwidth can be increased at the expense of degrading the

frequency step resolution. As the aforementioned Leeson model predicts, the open loop VCO phase noise can be improved through additional power dissipation (higher signal swings) or a reduced level of integration (off-chip high Q passives). Therefore, for a quartz crystal stabilized synthesizer, there is an inherent tradeoff between power consumption and phase noise.

Figure 3 plots the phase noise measurements of a variety of crystal oscillators and synthesizers.

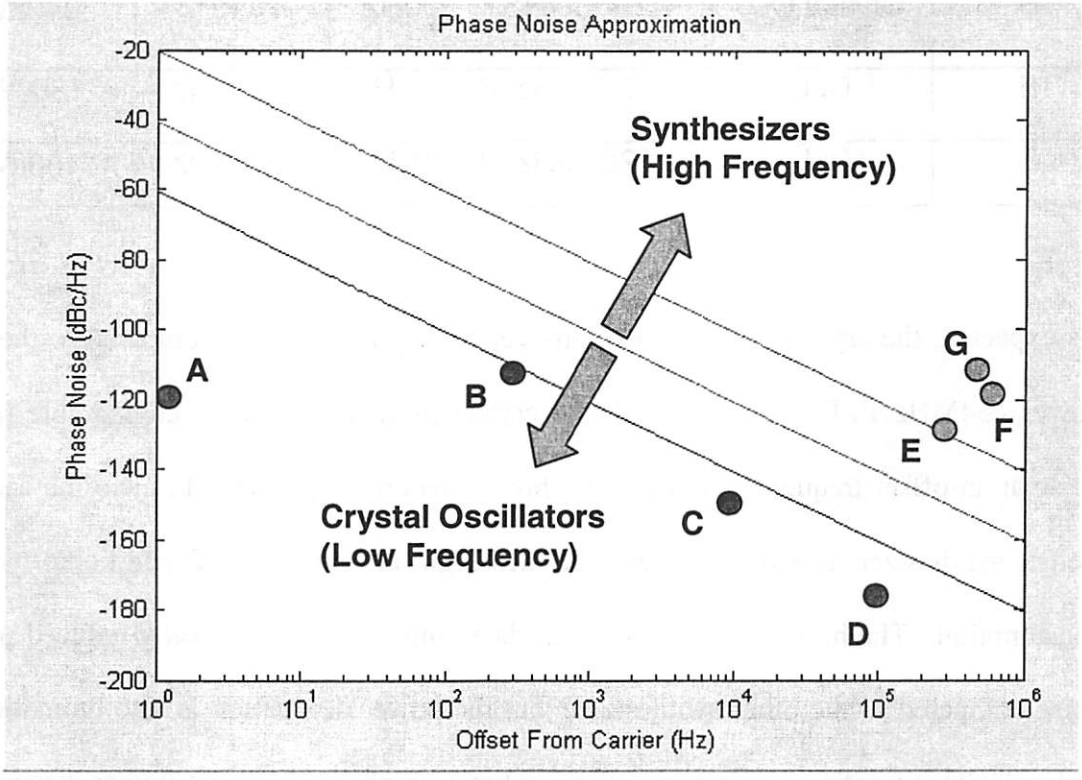

Figure 3. Phase Noise of Crystal Oscillators and Synthesizers

The parallel lines in Figure 3 indicate contours of constant phase noise, which are expected to fall off at –20dB/decade. The plot can be roughly divided into two regimes: the crystal oscillator regime and the frequency synthesizer regime. Data points A-D in

the above plot are examples of published crystal oscillators, and E-G are frequency synthesizers.[7,8,9,10,11,12,2] As expected, frequency synthesizers exhibit poor phase noise compared to the crystal references due to the limitations described above. It is worthwhile to examine, in addition to phase noise, the power dissipation and frequency of operation of some published frequency generators. Table 1 highlights some relevant specifications from three of the designs in Figure 3.

Table 1. Comparison of Various Sinusoid Generators

Data Point	Architecture	Phase Noise	Frequency	Power
B	Crystal Osc	-113dBc/Hz @ 300Hz	78MHz	340μW
E	DLL	-127dBc/Hz @ 330kHz	900MHz	130mW
G	PLL	-112dBc/Hz @ 500kHz	434MHz	400μW

As expected, the crystal oscillator exhibits very low phase noise. Compared to the low power 434MHz PLL (data point G), the crystal oscillator achieves comparable phase noise at an offset frequency greater than three orders of magnitude closer to the carrier. Better synthesizer phase noise can be achieved at the cost of additional power consumption. The high performance DLL (data point E) displays greatly reduced phase noise compared to the other synthesizers, but the power dissipation is also dramatically higher.[10] This verifies the dramatic tradeoff between phase noise and power dissipation in a quartz crystal stabilized frequency synthesizer.

3.3 SAW Oscillator

As described in the previous section, crystal stabilized frequency synthesizers exhibit very good long-term stability since the output frequency is tied to the crystal reference. There is a tradeoff, however, between short-term stability (phase noise) and power dissipation. To lift these constraints, different frequency generation techniques must be employed. One such technique is the use of surface acoustic wave (SAW) filters or resonators as a frequency reference for designing an oscillator. A SAW resonator is a passive structure that provides an electromechanical resonance at a well-defined frequency, similar to a quartz crystal. Although the achievable resonant frequencies are higher than quartz crystal resonators, the quality factor of SAW devices is over an order of magnitude smaller (around 10,000). Using a SAW resonator or filter, an RF sinusoid would be generated in open loop mode at the resonant frequency of the SAW device (eg. 433MHz). There are a number of advantages to this strategy:

- Spurious tones (common in frequency synthesizers) are absent
- The high Q resonator ensures excellent open loop phase noise
- Reduced power consumption and complexity over frequency synthesizer.

In a recent 1.2μm BiCMOS transmitter, a 433MHz SAW stabilized oscillator achieved a very low phase noise of −110dBc/Hz at a 10kHz offset.[13] Another implementation in GaAs realized a 300MHz SAW stabilized oscillator with a power consumption of 8.1mW.[14] The package dimensions of a single SAW resonator are

approximately (4.8 x 4.8)mm^2, limiting the form factor of the system-level design, especially if multiple resonators are needed.[15] There are additional concerns that limit the usefulness of a SAW stabilized oscillator:

- Poor resonator temperature tolerance (+/- 60ppm from –40°C to +80°C)[16]
- Poor fabrication tolerance (+/- 200ppm)[15]
- Difficult to modulate frequency due to high loaded Q
- Difficult system level integration
- Limited frequency choices

These limitations have relegated SAW resonator based oscillators mainly to transmitters for garage door openers and automobile security systems.

3.4 Integrated LC Oscillator

So far it has been shown that an open-loop oscillator can achieve low power consumption and a low complexity solution. However, SAW based oscillators suffer from large form factors and a narrow choice of oscillation frequency. Thus, one may wish to construct an open loop oscillator out of fully integrated passive components. This would allow the designer to control the resonant frequency and provide a fully integrated solution while realizing low power consumption. A hypothetical integrated 2GHz LC oscillator implementation is considered below.

The resonant frequency of such an oscillator is given by equation 3.2.

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}} \tag{3.2}$$

Where L is the tank* inductance value and C is the total implicit and explicit capacitance seen at the tank. Such an oscillator would require an on-chip (or bondwire) inductor on the order of 5nH to tune out a capacitance of 1.2pF. Assuming that our tank uncertainty is due to capacitive variations only (the inductance is well known and controlled), it can easily be shown that the frequency variation due to capacitor offsets is given by equation 3.3.

$$\frac{df_{osc}}{dC} = \frac{-C^{-3/2}}{4\pi\sqrt{L}} \tag{3.3}$$

For our sample oscillator, this corresponds to a frequency offset of 856 kHz/fF, or 428 ppm/fF. **Thus, if the capacitance varies by as little as 1fF, the oscillation frequency is off by 428 ppm.** It is not unusual for process variation on CMOS capacitors to be +/- 10%. This leads to a process variation of our LC oscillator of +/- 51,000 ppm (approximately 1.95GHz to 2.15GHz), which is unacceptable for most realistic applications. Hand trimming of a variable capacitor or switched capacitor auto-calibration would be necessary for tuning this oscillator.

In addition to very poor fabrication tolerances of the oscillation frequency, integrated LC oscillators suffer from poor phase noise. This is due to the low Q nature of integrated inductors, which usually have a Q of less than 10. Much work has proceeded on increasing the phase noise performance of low Q integrated LC oscillators for the design of VCOs in frequency synthesizers. As discussed in Section 3.2, the phase noise of a frequency synthesizer loop is limited in part by the open loop phase noise of its VCO. **Therefore, in order to achieve a low phase noise with a low Q tank, the signal swing must be maximized.** This is accomplished through differential structures and

* "Tank" refers to a parallel L-C resonant structure used to discriminate signals in the frequency domain.

high bias currents. A recent fully integrated low phase noise LC VCO, using similar component values to the ones specified above (L~5nH, C~1.2pF), achieves a phase noise of −112dBc/Hz at 100kHz offset with a high power dissipation of 20mW.[17]

Thus, an integrated LC oscillator can achieve a respectable phase noise by burning large amounts of power to achieve a high signal swing. The process variation, however, of the oscillation frequency of such an oscillator is prohibitively high to allow open loop operation.

3.5 Direct Digital Frequency Synthesis

One final method of sinusoid generation that will be considered is Direct Digital Frequency Synthesis (DDS). Figure 4 shows a simplified block diagram of a DDS system.

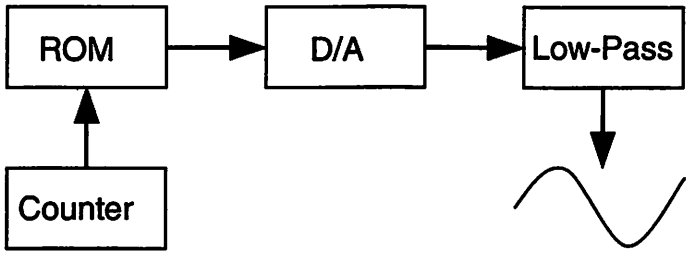

Figure 4. Direct Digital Frequency Synthesis

This method generates a sinusoid (or other arbitrary waveform) by stepping through a lookup table (LUT) in the digital domain and converting the waveform to the analog domain with a D/A with an appropriate level of quantization.[18] The low pass filter after the D/A removes high frequency components resulting from the D/A conversion. This method eliminates the PLL lock time and fine frequency stepping problems that plague

analog frequency synthesizers. Additionally, any desired modulation scheme can be read directly from the LUT and changed at any time at a software level. The main problem with this scheme is that, to satisfy the Nyquist sampling theorem, the LUT clock speed must be at least twice the desired output frequency of the synthesizer, leading to high digital complexity and power consumption.[18] Additionally, the implementation of the D/A converter would be extremely difficult for generating RF frequencies.

However, for generating low frequency signals, this approach is feasible. A recent DDS implementation used a 9-bit LUT, 8-bit D/A, and a 36 MHz input clock with a power dissipation of 20mW to perform a complex, synchronous frequency division.[19]

Chapter 4. MEMS Resonator Based Oscillator

4.1 Introduction

In the last chapter, traditional frequency generation methods were discussed. It was shown that, although quartz crystal stabilized frequency synthesizers are ubiquitous in RF systems, they suffer from an inherent tradeoff between phase noise and power. Additionally, even with a fully integrated VCO, they still require an off-chip quartz crystal. SAW based oscillators can achieve good phase noise performance, but the frequency choices are limited and they suffer from a bulky form factor and large parasitics. In this chapter, a frequency generator using an Agilent thin film bulk acoustic wave resonator (FBAR) is proposed. It will be shown that this topology can achieve very low power consumption, low phase noise, and has the potential to be a highly integrated solution.

4.2 FBAR Resonator Characteristics

The Agilent FBAR resonator consists of a film of aluminum nitride (AlN) sandwiched between two metal electrodes (see Figure 5).[20]

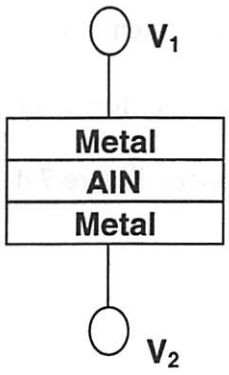

Figure 5. FBAR Resonator Cross Section

This metal/AlN/metal sandwitch forms a thin membrane. The AlN layer is a piezoelectric compound, thus allowing an electrical to mechanical conversion of energy. This energy is subjected to a high Q mechanical resonance, and is subsequently converted back to electrical energy. To form an acoustic cavity under the membrane, a directional wet etch of bulk silicon is performed with a KOH or EDP etchant.[21] Figure 6 shows a cross section SEM of an FBAR resonator.

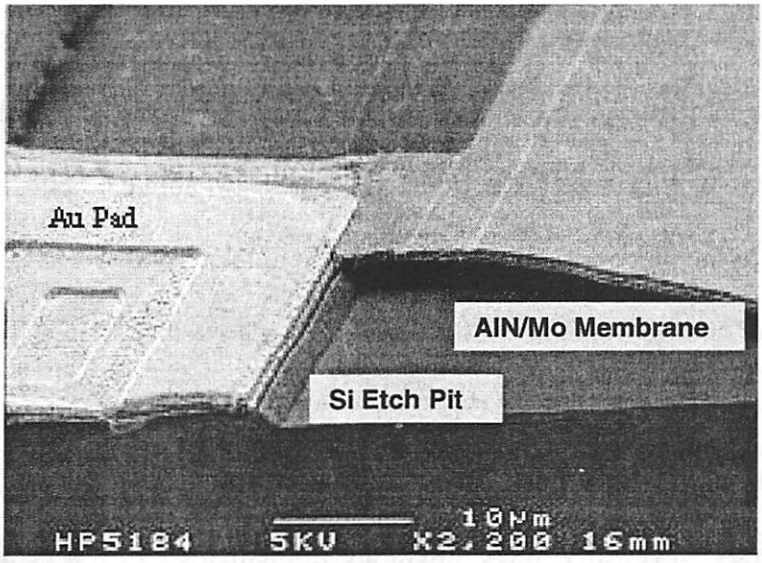

Figure 6. Cross Section Photograph of an FBAR Resonator
(Reprinted with permission from reference 20)

Figure 6 shows the thin piezoelectric membrane suspended above the silicon etch pit. This topology yields a structure that is electrically equivalent to a high-Q series LCR circuit with a high frequency resonance. Figure 7 depicts the circuit schematic equivalent model of an FBAR resonator.

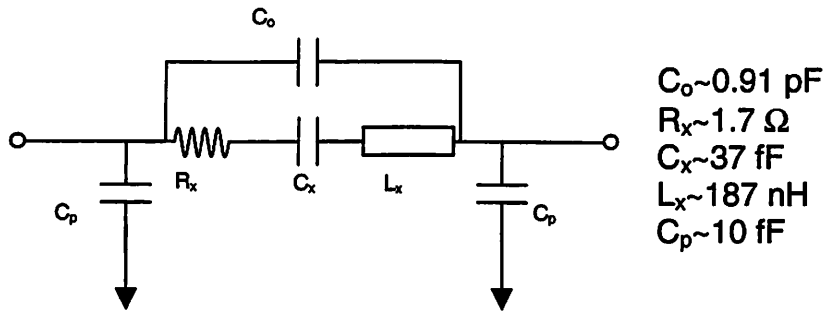

Figure 7. FBAR Resonator Circuit Equivalent Model

The series resonance is modeled by L_x, C_x, and R_x, and is shown to have a Q value of around 1300. The R_x component of a resonator model is known as the "motional resistance", and is a key factor in determining the Q of the device. As shown in Figure 7 above, there is a large feedthrough capacitance C_o. This is caused by the capacitance between the two parallel metal electrodes in Figure 5 above. The small parasitic capacitance due to the electrodes and bondpads are modeled by C_p. These resonators can be fabricated over a wide frequency range, and have been demonstrated from 1.5GHz up to 7.5GHz.[22]

FBAR resonators have been successfully used to create bandpass RF filters and antenna duplexers.[23] Typically, these filters are implemented with a ceramic filter or a surface acoustic wave (SAW) filter. However, ceramic filters suffer from large form factors, and SAW filters exhibit poor power handling capability and frequency instability.

By using FBAR resonators to create these filters, an extremely small form factor and high power handling capability has been achieved. To accomplish this, individual FBAR resonators are connected in ladder networks with mass loading used to slightly alter the resonant frequency of the shunting resonators by approximately 3%. This creates a well-defined bandpass structure with a very sharp roll off. Used in this manner, they have been shown to achieve a high power handling capability (>2 Watts) and a small form factor for cellular radio applications.

Besides creating RF bandpass filters and duplexers, these resonators hold much potential for creating new circuit topologies to achieve high performance and low power RF systems. To investigate this further, it is instructive to analyze the physical and electrical properties of a single FBAR resonator. See Figure 8 below.

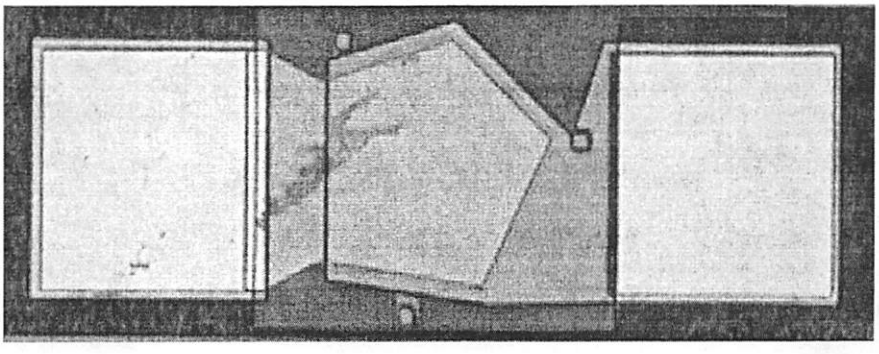

Figure 8. FBAR Resonator Top View

Figure 8 shows a top-down view of a single FBAR resonator. The gold bondpads on either side of the resonator are 100μm x 100μm, and the pentagonal* resonator also occupies approximately 100μm x 100μm. The resonant frequency of this device is approximately 1.9GHz. For effective use of the resonator, it is important to understand

* The pentagonal shape is used to attenuate harmonics of the fundamental resonance. See Ref. 20.

the various modes of excitation. See Figure 9 for the simulated frequency response of this resonator.

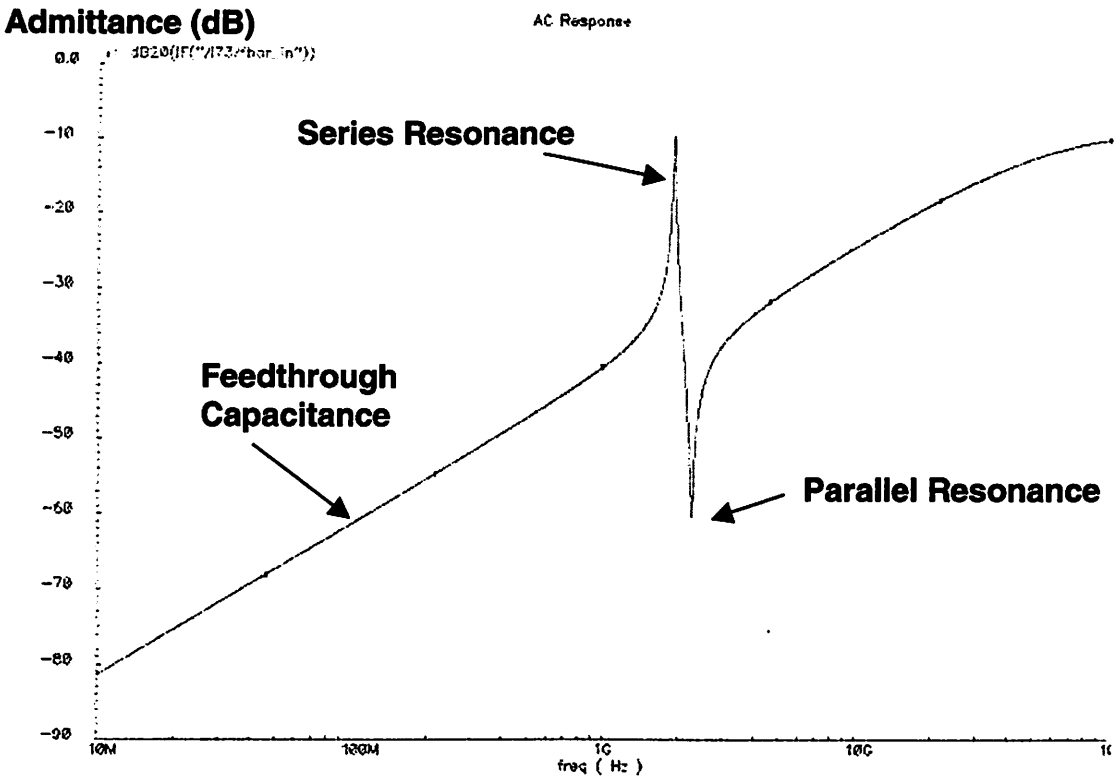

Figure 9. Simulated Resonator Admittance

Figure 9 shows the admittance vs. frequency of a single FBAR resonator with one terminal shorted to ground. Throughout most of the frequency range, the response is dominated by the response of the feedthrough capacitor, C_o. At the series resonance, the motional resistance (R_x) dominates the admittance. Soon after the series resonance, the parallel resonance occurs. During this regime, the resonator looks inductive and resonates with the feedthrough capacitance C_o, greatly reducing the admittance. At frequencies above the parallel resonance, the admittance follows the feedthrough capacitance response as it does for low frequencies. At extremely high frequencies, the

parasitic capacitances (C_p) begin to affect the frequency response by reducing the admittance through the structure. Let us derive expressions for the effective structure impedances and the frequencies at which they occur.[5]

Wideband response: *Impedance dominated by C_o.*

$$Z = \frac{1}{sC_o} \tag{4.1}$$

Series Resonance: *Impedance dominated by R_x (ideally zero).*

$$f_{series} = \frac{1}{2\pi\sqrt{L_x C_x}} \tag{4.2}$$

$$Q_{series} = \frac{\omega_o L_X}{R_X} = \frac{1}{\omega_o C_X R_X} \tag{4.3}$$

$$Z \approx \frac{1}{sC_o} // R_x \tag{4.4}$$

Parallel Resonance: *Impedance dominated by R_x and R_{cap} reflected across resonator (ideally infinite).*

$$f_{parallel} = \frac{1}{2\pi\sqrt{L_X \frac{C_X C_T}{C_X + C_T}}} = f_{series}\sqrt{1+\frac{C_X}{C_T}} \approx f_{series}\left(1+\frac{C_X}{2C_T}\right) \tag{4.5}$$

In equation (4.5), C_T is the total capacitance across the resonator = C_o + $C_{p1}//C_{p2}$. Assuming the feedthrough and parasitic capacitances have a finite quality factor (Q_{cap}), they suffer from an effective series resistance, as shown in equation (4.6):

$$R_{cap} = \frac{1}{Q_{cap} C_T \omega_{parallel}} \tag{4.6}$$

This parasitic resistance causes the parallel Q to be lower than the series Q of the resonator. This can be intuitively understood by realizing that, in the parallel resonance, there are circulating currents that flow through the capacitor C_T, in addition to the series Lx-Cx-Rx circuit. The effective parallel Q can be shown to be the following:

$$Q_{parallel} = \frac{1}{\omega_o C_X (R_X + R_{cap})} = Q_{series} \frac{R_x}{R_x + R_{cap}} \tag{4.7}$$

Thus, the quality factor of the capacitance seen by the resonator directly affects the parallel Q. The implication of this will be investigated in subsequent sections. Ideally, the impedance of the resonator at the parallel resonance would be infinite. In reality, this impedance is degraded by the motional resistance R_x and the resistance R_{cap} resulting from the finite capacitor Q. It can be shown that the effective impedance seen at the parallel resonance is given by equation (4.8):

$$R_{parallel} = \frac{1}{\omega_o^2 C_T^2 (R_X + R_{cap})} \tag{4.8}$$

Thus, the effective parallel impedance of the resonator is a strong function of the capacitance shunting the resonator. It is interesting to note that, although $R_{parallel}$ decreases as C_T increases, the parallel Q of the resonator is not directly affected. **Only adding a real resistance (not reactance) in the path of the circulating current dissipates power, thus causing a de-tuning of the resonator.**

Let us summarize this analysis in Table 2 by calculating the values for the resonator depicted above in Figure 7 using equations (4.1)-(4.8):

Table 2. FBAR resonator parameters

Impedance of C_T at f_{series}	92Ω
f_{series}	1.913GHz
Q_{series}	1330
R_{series}	~1.7Ω
Rejection ($Z_{series}/Z_{feedthrough}$)	1.7/92 = -34.6dB
$f_{parallel}$	1.939GHz
$Q_{parallel}$ (Q_{cap}=50, R_{cap}=1.7)	665
$R_{parallel}$	2.06kΩ

The above analysis shows that varying the feedthrough capacitance has a dramatic affect on the parallel resonance of the resonator. This phenomenon is occasionally useful and often detrimental, so it is important to have an intuitive understanding of these effects. Figure 10 shows the frequency response of the resonator depicted in Figure 7 for various feedthrough capacitances.

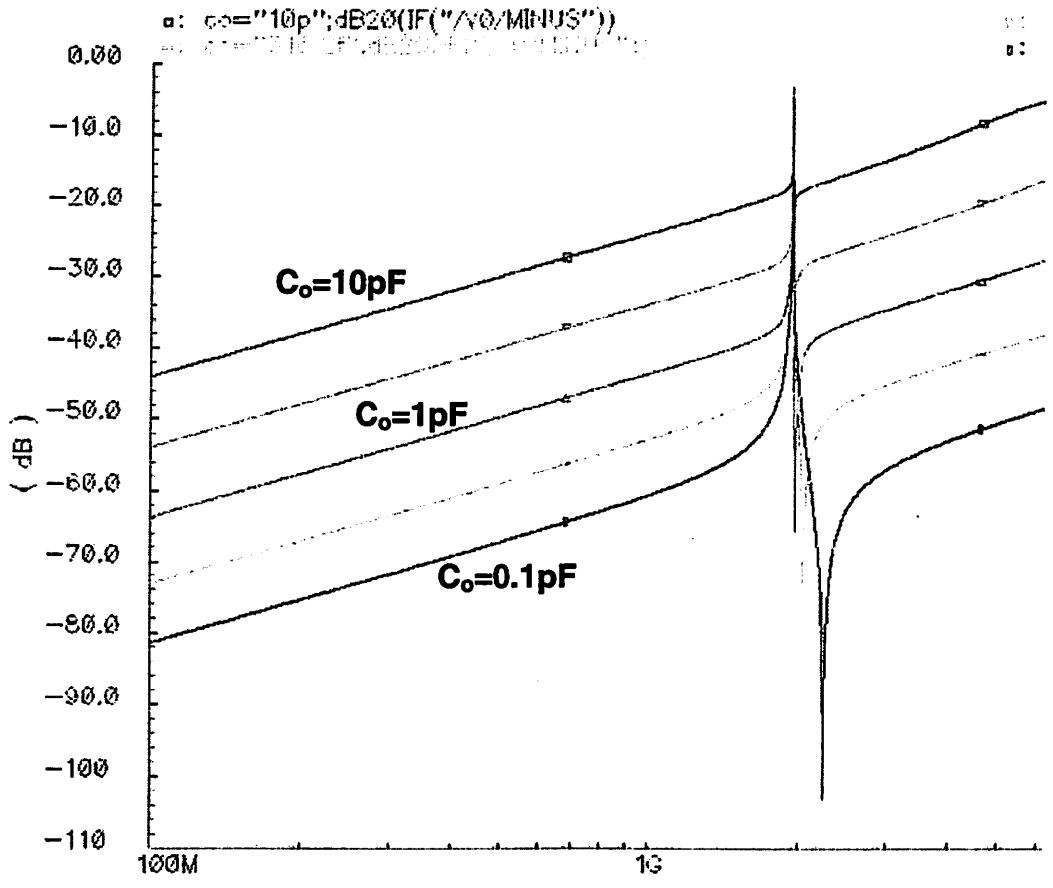

Figure 10. Effect of Feedthrough Capacitance on Resonator Response

Figure 10 shows the admittance vs. frequency of an FBAR resonator with one terminal grounded. The feedthrough capacitance, C_o, is varied logarithmically in five steps from 0.1pF to 10pF to demonstrate the effects of feedthrough capacitance on resonator frequency response. The first thing to notice is that, during the non-resonant bandwidth, increasing the feedthrough capacitance directly increases the wideband admittance of the resonator. Second, as predicted by the equations above, **neither the frequency nor the amplitude of the series resonance is affected by the value of the feedthrough**

capacitance. Thus, as C_o increases, the rejection* of the resonator degrades. Finally, the plot shows that as C_o increases, the parallel resonant frequency decreases and moves closer to the series resonance. Although the Q of the parallel resonance is unchanged, the reflected motional resistance ($R_{parallel}$) decreases as C_o increases. This is shown in the plot above by the parallel resonant peaks displaying higher admittances as the feedthrough capacitance increases. Understanding this plot is crucial to the successful development of oscillators and other circuits utilizing these resonators.

Besides the frequency and filter topology of the FBAR resonators, there is an additional degree of freedom that affords the designer greater power in achieving an optimal design. For a given resonant frequency, it is possible to vary the active area of the resonator membrane. As the area of the resonator increases, the motional resistance (R_x) decreases. Increasing the membrane area of the resonator increases the area of the parallel plate structure shown in Figure 5 above, thus increasing C_o. Conversely, as the area of the resonator membrane is decreased, R_x increases and C_o decreases. Thus, the area of the resonator should be appropriately and optimally sized for a given circuit.

The last point that will be mentioned about the FBAR resonator is one of integratability. Unlike ceramic, SAW, or quartz crystal resonators, the FBAR resonator is micromachined out of a silicon substrate and fabricated using traditional thin film IC and MEMS fabrication techniques. As such, FBAR resonators are ultimately integratable with active devices, including submicron CMOS processes. This would allow even higher performance by delivering smaller form factors, reduced interconnect parasitic

* The rejection will be defined as the ratio of the impedance at series resonance to the impedance just off series resonance.

capacitance and inductance, and higher frequency stability due to improved thermal matching.

4.3 Oscillator Performance Prediction

With the above analysis completed, the stage has been set to discuss the potential for the use of an FBAR resonator in an oscillator. This would be accomplished by utilizing the tightly controlled mechanical resonance to set an oscillation frequency in a solid-state oscillator. This section will explore the feasibility of this idea by investigating the frequency stability of the resulting oscillator, the predicted phase noise performance, and, most importantly, the theoretical limits on power consumption. To proceed with the analysis, some fundamental assumptions about the oscillator must be made. Two important questions will be posed, and the answers will provide intuition about the oscillator design philosophy and provide a starting place for the analysis.

1. ***Q.) Is it more desirable to use a bandpass FBAR resonator ladder network or a single resonator in the oscillator?***

   A.) To achieve minimal phase noise, minimize power consumption, and minimize oscillation frequency sensitivity to process variations, it is desirable to have a high resonator Q. The Q of a single resonator is inherently higher than the Q of a bandpass structure composed out of composite resonators. Thus, a single resonator architecture will be chosen. If, however, it is desirable to have a large oscillator tuning range (eg., for a VCO), it may be desirable to use composite resonators.

2. ***Q.) Should the series resonance or parallel resonance of the FBAR resonator be used?***

A.) In the analysis shown above, the impedance of the series resonance is approximately 1.7Ω. The impedance of the parallel resonance is approximately 2kΩ. It is important to remember that any circuit resistance in series with a series resonant oscillator or in parallel with a parallel resonant oscillator will directly de-Q the tank. It is much more natural for a CMOS or Bipolar circuit to compete with a 2kΩ impedance than a 1.7Ω impedance. For example, even a 2Ω series interconnect/contact resistance would reduce the loaded Q of the series resonance by a factor of two. Thus, to minimize the loading on the resonator, the parallel resonance should be used for oscillation, especially for a low-power design.

For this oscillator design, the parallel resonance of a single FBAR resonator will be used. Analysis of the predicted oscillator performance can now proceed.

4.3.1 Frequency Stability

Long-term frequency stability and fabrication tolerance is one of the most important characteristics of a reference oscillator. The fabrication tolerance analysis must take into account not only the tolerance of the resonator itself but also the CMOS

circuitry. The subsequent analysis predicts the frequency stability performance of an FBAR-based oscillator.

Since we are using the parallel resonance of the FBAR resonator, the oscillation frequency is the same as the parallel resonant frequency. Using the results from equation (4.5), the oscillation frequency is given in equation (4.9):

$$f_{osc} = f_{parallel} \approx f_{series}\left(1+\frac{C_X}{2C_T}\right) \tag{4.9}$$

This equation confirms our intuition that the oscillation frequency is fundamentally derived directly from the series resonance of the FBAR resonator. This parameter is controlled by various fabrication parameters, including the thickness of the films constituting the resonator membrane.[21] At the time of this writing, the fabrication tolerance of FBAR resonators is approximately +/- 500ppm (2GHz +/- 1MHz).[24] This fabrication tolerance is not a fundamental technical limitation; it is an engineering decision that has been made based on the tolerances necessary for bandpass RF filters and duplexer applications.[25] Thus, the fabrication tolerance of an FBAR resonator can ultimately be improved for stringent frequency reference applications.

In addition to the fabrication tolerance of the FBAR resonator, its sensitivity to temperature is also important. The FBAR resonator exhibits a temperature coefficient of approximately 25ppm/°C.[20] This is much higher than a quartz crystal (~0.6ppm/°C), and for highly sensitive applications the temperature coefficient of the FBAR based oscillator would have to be stabilized. One method that has been employed is the use of on-chip heaters to tune (or stabilize) the resonant frequency of the FBAR. A tuning range of 2%

(20,000ppm) can be achieved by locally heating the FBAR with 250mW of power.[21] This approach may be feasible for high performance applications, but is prohibitive for ultra-low power systems. Another option for calibration is the use of variable capacitors to "pull" the parallel resonant frequency, thus modifying the oscillation frequency. This technique has been used successfully in precision quartz crystal reference oscillators.[26]

Next, the sensitivity of the oscillation frequency to capacitive variation will be analyzed. The purpose of this is twofold. First, it is important to predict how the process variation of the CMOS device capacitances will affect the oscillation frequency. Second, it will allow us to discuss the feasibility of calibrating the oscillation frequency through the use of switchable or variable capacitors. For this analysis, C_T is the total capacitance shunting the resonator. C_T consists of the resonator membrane capacitance C_o and any other parasitic or explicit capacitance loading the resonator (pad, transistor, and interconnect capacitances). It can be shown that the sensitivity of the oscillation frequency to capacitive variation is given by equation (4.10):

$$\frac{\partial f_{osc}}{\partial C_T} \cong f_{series} \frac{-C_x}{2C_T^{\,2}} \tag{4.10}$$

Which can alternately be written as equation (4.11):

$$\frac{\partial f_{actual}}{\partial C_T} \cong \frac{-1}{4\pi R_X Q C_T^{\,2}} \tag{4.11}$$

Equations (4.10) and (4.11) predict that the oscillation frequency decreases as parasitic capacitance is added. This was shown in Figure 10 above. Also, as would be expected,

equation (4.11) shows that it is difficult to "pull" the frequency of a resonator with a high Q. This is why the extremely high Q of a quartz crystal is desirable for creating a frequency reference. For the FBAR resonator parameters given in Figure 7, the sensitivity of the oscillation frequency to capacitive variation is approximately -18 ppm/fF (-35.1 kHz/fF). Another interesting result of the above analysis is that as C_T increases, the sensitivity to capacitive variation decreases as C_T^2. If C_T were increased from 1pF to 10pF (easily achievable by shunting the resonator with 9pF of capacitance), the frequency sensitivity to capacitive variation decreased by two orders of magnitude to -0.18 ppm/fF (-350 Hz/fF). This will, however, greatly affect the power consumption of the oscillator (as will be shown in Section 4.3.2). Table 3 summarizes the findings of the above analysis.

Table 3. Prediction of Long Term Oscillation Frequency Stability

Resonator Process Variation	+/- 500ppm
Resonator Temperature Variation	25ppm/°C
Sensitivity to Capacitance Variation (C_T=1pF)	-18 ppm/fF
Sensitivity to Capacitance Variation (C_T=10pF)	-0.18 ppm/fF

The frequency stability analysis thus far has been general and can be applied to any LCR resonant structure with a feedthrough capacitance. This model must be expanded to include certain specificities that are unique to the FBAR resonator.

The sensitivity to capacitance variation has so far assumed that the entire value of C_T suffers from fabrication uncertainties. However, the membrane film thicknesses are necessarily tightly controlled to achieve a stable series resonance. **Thus, the membrane film feedthrough capacitance C_o is also very tightly controlled.** This must be taken

into account when analyzing the oscillation frequency sensitivity to capacitive variation. For this analysis, the total feedthrough capacitance C_T is the sum of the membrane capacitance (C_o) and any external capacitance (C_{ext}). It will be assumed that C_o is precisely known and fabricated and any capacitive variation is due to the non-ideal modeling and/or fabrication of C_{ext}. It is not unusual for the process variation of explicit CMOS capacitors to be greater than 10%. Thus, this analysis assumes that C_{ext} varies by +/- 10%. The results of this analysis are best understood by viewing Figure 11, which depicts the frequency variation (in ppm) due to a 10% variation in C_{ext} as a function of C_{ext}.

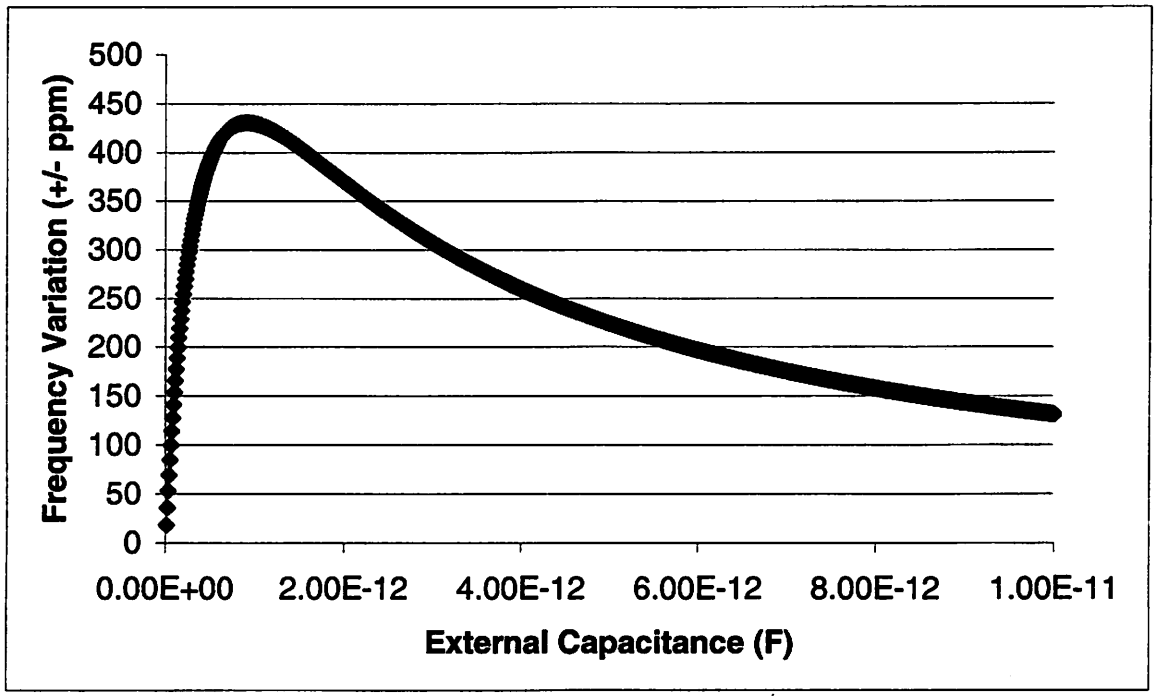

Figure 11. Oscillator Frequency Variation with 10% Tolerance on External Capacitors

To generate Figure 10, C_o = 1pF and is assumed to be precisely controlled. Therefore, when the external capacitance is negligible, the frequency variation due to the C_{ext} error is zero. It is interesting to note that this is a very different situation than is found in a

traditional quartz crystal oscillator. With a quartz crystal, C_o is *not* well known, and it is desirable to swamp C_o with a known C_{ext} of a suitable size to achieve the desired sensitivity. In this case, our variation is due solely to the process variation of C_{ext}. As the plot above shows, the frequency variation reaches a maximum for $C_o = C_{ext}$. In the regime where $C_{ext}>C_o$, increasing C_{ext} gives a lower frequency variation. However, as will be shown shortly, the oscillator power consumption increases dramatically as C_T increases.

In conclusion, the long-term frequency stability of an FBAR based oscillator is fundamentally limited by the fabrication tolerance of the FBAR resonator, the temperature coefficient of the resonator, and the frequency sensitivity due to external capacitor variations. If possible, the external capacitance should be much less than the membrane capacitance C_o for minimum frequency variation and power consumption. If this is not possible, there is a tradeoff between power consumption and frequency variation. The worst case frequency variation reaches a maximum for $C_o=C_{ext}$.

4.3.2 Theoretical Limits on Power Consumption

Since the goal of the project is to create an ultra-low power sinusoid generator, the theoretical limits on power consumption are crucial for the evaluation of the feasibility of the circuit. In this section, we will first perform a general analysis and then specify a theoretical limit using the resonator parameters provided in Figure 7.

For oscillation at the parallel resonance of a given LCR resonant device, the resonator acts as an inductor to resonate with the total device capacitance (C_T). In

essence, this entails using the FBAR resonator to simulate a very high Q inductor. Although this could conceivably be done in a variety of interesting ways, the fundamental problem is that the FBAR resonator does not pass any DC current. Typically, inductors are used to simultaneously tune out a capacitance and provide bias current to the active transconductor. This same issue is problematic in the design of crystal- and SAW-based oscillators. One solution is to use a three-point oscillator, which effectively uses a given resonator as an inductance while providing the necessary bias current to the transconductor through a current source. Figure 12 diagrams a model for the oscillator.

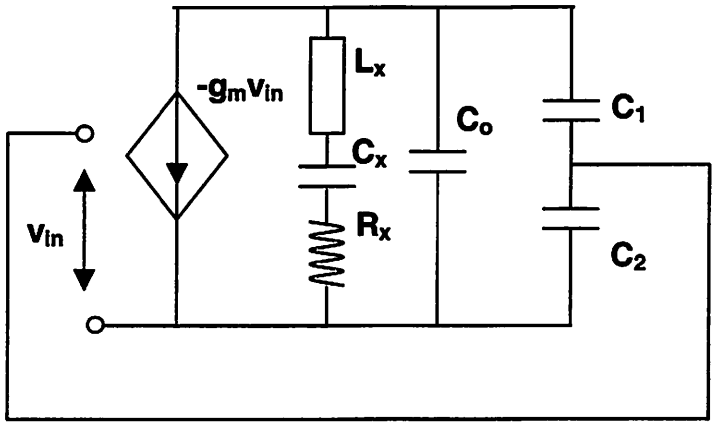

Figure 12. Conceptual Oscillator Diagram

As the schematic in Figure 12 shows, feedback to a transconductor is accomplished via a capacitive divider composed of C_1 and C_2. L_x, C_x, R_x, and C_o represent the intrinsic resonator circuit equivalent components. For an FBAR-based oscillator, the values of these capacitors are fundamentally limited by the parasitic capacitances (C_p) shown in Figure 7. The total capacitance (C_T) seen by the resonator in Figure 12 is given by equation (4.12):

$$C_T = C_o + C_1 // C_2 \tag{4.12}$$

Thus, at the oscillation frequency, the resonator can be modeled by an inductor (L_{eff}) which resonates with C_T at the parallel resonance. Now, the oscillation frequency is given by equation (4.13):

$$f_{osc} = f_{parallel} = \frac{1}{2\pi\sqrt{L_{eff} C_T}} \tag{4.13}$$

This is represented by the schematic shown in Figure 13:

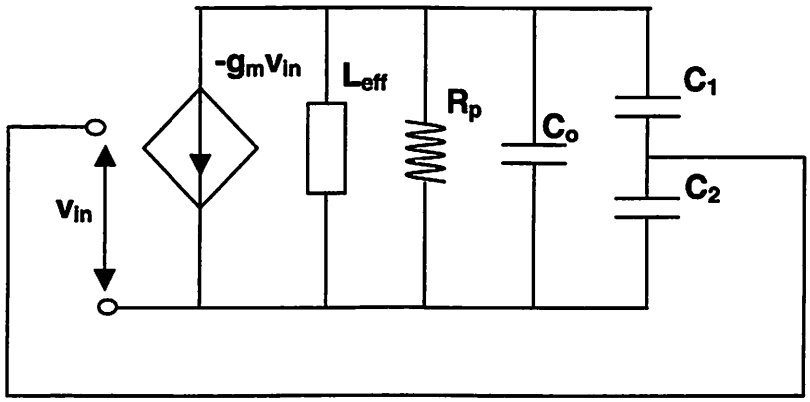

Figure 13. Oscillator Diagram with Effective Inductance

In Figure 13, R_p is the reflected motional resistance due to the motional resistance (R_x) and capacitor resistance (R_{cap}). It can be shown by inspection that positive feedback is achieved with a loop gain given by equation (4.14):

$$A_{CL} = g_m R_p \frac{C_1}{C_1 + C_2} \tag{4.14}$$

However, in actual implementations, the load resistance occurs in parallel with capacitor C_1. This is because the node connecting capacitors C_1 and C_2 is most conveniently connected to ground. Because of this, we must reflect R_p to appear in parallel with capacitor C_1 as shown in the Figure 14.

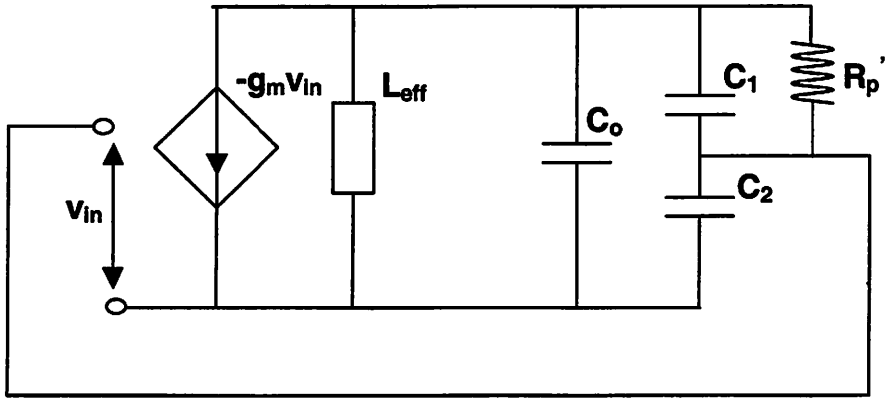

Figure 14. Oscillator Diagram with Reflected R_p

The resistance R_p is reflected through the capacitive transformer formed by C_1 and C_2 as shown in equation (4.15):

$$R_p' = R_p \frac{(C_1 // C_2)^2}{C_1^2} = R_p \frac{\left(\frac{C_1 C_2}{C_1 + C_2}\right)^2}{C_1^2} = R_p \frac{(C_1 + C_2)^2}{C_2^2} \tag{4.15}$$

It has been shown that the optimal frequency stability and start-up factor is achieved for $C_1=C_2$.[27] Thus, for optimal operation, equation (4.15) simplifies to equation (4.16):

$$R_p' = \frac{R_p}{4} \tag{4.16}$$

Now, the loop gain can be re-calculated to be equation (4.17):

$$A_{CL} = g_m R_p' \frac{C_1}{C_2} = g_m \frac{R_p}{4} \tag{4.17}$$

To achieve oscillation, we need $A_{CL}>1$. Equation (4.8) showed an expression for R_p in terms of the resonator device parameters. From equation (4.8) and equation (4.17), equation (4.18) predicts the critical transconductance necessary for oscillation.

$$g_m \geq \omega_o^2 \left(C_o + \frac{C_1 C_2}{C_1 + C_2} \right)^2 \left(\frac{(C_1 + C_2)^2}{C_2^2} \right) (R_x + R_{cap}) \tag{4.18}$$

The zero-peak output voltage swing can be calculated by equation (4.19):

$$V_o = I_1 R_p' \tag{4.19}$$

Where I_1 is the fundamental frequency component of the device current. A conservative assumption is that the ratio of the fundamental component to the device bias current (I_1/I_{bias}) is unity. We can now relate the desired output voltage swing directly to the required bias current in terms of the resonator parameters to give equation (4.20):

$$V_o \approx I_{bias} R_p' = \frac{I_{bias}}{\omega_o^2 \left(C_o + \frac{C_1 C_2}{C_1 + C_2} \right)^2 \left(\frac{(C_1 + C_2)^2}{C_2^2} \right) (R_x + R_{cap})} \tag{4.20}$$

The analysis thus far is general and can be used to calculate the theoretical minimum power consumption of an oscillator using the parallel resonance of any resonator. It is now possible to quantify the fundamental power consumption of the oscillator in terms of the actual resonator parameters provided at the beginning of this

chapter. Assuming that $C_1=C_2=C_p$, and $R_{cap}=1.4$, Table 4 predicts the fundamental limits on power consumption.

Table 4. Fundamental Limitations on Power Consumption

R_p'	607Ω
g_m required for oscillation	1.64mS
I_{bias} (V_o=100mV)	164μA
P_{diss} (V_{dd}=1V)	164μW

As shown in Table 4, the fundamental limit on power consumption would be 164μW to achieve a 100mV zero-peak output signal with a V_{dd} of 1V. Typically, an oscillator is either voltage-swing limited or start-up limited. **Since the g_m/I_{bias} ratio required by the numbers calculated in Table 4 is only 10, the power consumption is limited by the required bias current for the signal swing, not the necessary g_m.** The maximum achievable g_m/I_{bias} ratio for a MOSFET is approximately 30. Thus, if the predicted g_m/I_{bias} ratio were greater than 30, I_{bias} would be limited by the current necessary to achieve the critical g_m, not by the desired output swing. This analysis shows that is it possible to achieve extremely low power dissipation with an FBAR based oscillator.

4.3.3 Phase Noise Potential

The short-term stability (phase noise) of a frequency generator is crucial for many applications. A brief phase noise prediction will be performed using actual FBAR parameters and the analysis above. Calculating the fundamental phase noise limitation is important because it predicts, independent of the active devices used, the best possible

performance achievable. As discussed in Section 3.1, the Leeson model for phase noise in an oscillator is described by equation (4.21):

$$L(\Delta\omega) = 10\log\left[\frac{2FkT}{P_{signal}} * \left(\frac{\omega_{osc}}{2Q\Delta\omega}\right)^2\right] \tag{4.21}$$

The loaded Q of our oscillator is $Q_{parallel}$, which was shown in Table 2 to be 665. This is the theoretical limit, of course, because the finite output resistance of the transconductors and additional R_{cap} will decrease the loaded Q in an actual implementation. Additionally, to explore the theoretical limits, we will assume a device noise figure (F) of 0dB. The signal power (P_{signal}) is calculated using the numbers shown in Table 3 for a 100mV output swing across a reflected load of 607Ω. The result is given in equation (4.22):

$$P_{signal} = \frac{1}{2}\frac{\hat{V}^2}{R_L} = \frac{1}{2}\frac{(100mV)^2}{607\Omega} = 8.23\mu W = -20.8dBm \tag{4.22}$$

With a value of –20.8dBm calculated in (4.22), the Leeson model predicts a phase noise of –107dBc/Hz and –127dBc/Hz at a 10kHz and 100kHz frequency offset, respectively. This shows that the FBAR-based oscillator has extremely good phase noise potential due to the high resonator Q, even with very low signal power levels. As predicted by equation (4.22), increasing the output signal swing can further lower the phase noise.

This chapter described the FBAR resonator and derived important resonator characteristics. It was shown that a low power oscillator is feasible using the parallel

resonance of the FBAR resonator as a frequency reference. Fundamental limitations on frequency stability, power dissipation, and phase noise were derived and calculated. Chapter 5 focuses on the actual implementation of this oscillator.

Chapter 5. Oscillator Design

5.1 Introduction

In Chapter 4, it was shown that the parallel resonance of an FBAR resonator can be utilized to build a low power, low phase noise 2GHz oscillator. This section focuses on the design and implementation of an actual oscillator. Although the analysis thus far has been general with respect to the active devices used, the oscillator was implemented in an ST Microelectronics 0.18μm standard CMOS process. This 1-poly, 6-metal process uses a nominal V_{dd} of 1.8V. Standard CMOS was chosen for the implementation because, in addition to low power consumption, low cost is an important parameter for this project. It will be shown that the co-design of RF MEMS and standard CMOS circuitry enables a very efficient implementation of the oscillator.

5.2 Circuit Topology and Operation

The choice of oscillator topology is dictated by the need for low power consumption, low phase noise, and the need to oscillate on the parallel resonance of the FBAR resonator. To achieve low power consumption, the topology must exhibit low complexity and straightforward biasing. The Pierce oscillator topology was chosen because it provides excellent phase noise characteristics, uses the parallel FBAR resonance, and holds the potential for very low power consumption. For these reasons,

this topology is often chosen for low frequency quartz crystal oscillators.[27] A simplified circuit schematic is shown in Figure 15.

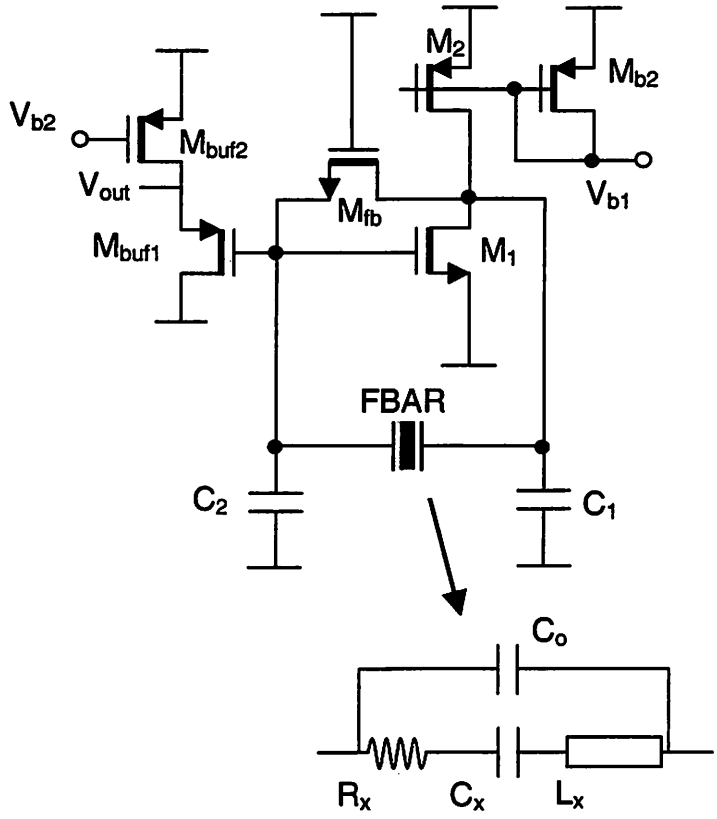

Figure 15. Simplified Oscillator Schematic

A brief description of the circuit operation follows. Transistor M_1 provides the critical transconductance for oscillation. The FBAR resonator is connected across the drain and gate of this device. Since the resonator does not pass DC, a large bias resistor formed by M_{fb} provides bias to the gate of M_1. Operation is class A, and the bias current is supplied and enforced by M_2. The signal is DC coupled to the first stage of the output buffer (M_{buf1}). For ultra low power RF design, DC coupling is preferable to avoid the

losses associated with AC coupling capacitors. This problem is particularly acute when poly-poly capacitors are not available, so a DC coupling philosophy was used throughout this design. Capacitors C_1 and C_2 represent the device, interconnect, and pad capacitances. C_1 includes the drain capacitors of M_1 and M_2, and C_2 includes the gate capacitors of M_1 and M_{buf1}. Accurate modeling and prediction of these values is crucial for high frequency implementation of this topology. At the parallel resonance of the resonator, C_1, C_2, and C_o are tuned out by the effective inductance L_{eff}, as discussed in Chapter 4. M_1 sees a high impedance at its drain node, allowing oscillation at this frequency.

5.3 Resonator/Circuit Co-Design

Once the topology has been chosen the design can proceed. In addition to designing the CMOS circuitry, optimal FBAR resonator parameters must be determined. To begin this optimization, fundamental Pierce oscillator design equations are derived.

5.3.1 Design Equations

The feedback factor, from the drain to the gate of M_1, at resonance, is given by equation (5.1):

$$f = \frac{C_1}{C_2} \tag{5.1}$$

The forward open-loop gain at resonance is:

$$A_{OL} = g_{m1} R_L \tag{5.2}$$

Where R_L is the real impedance at the drain of M_1. Therefore, the initial closed-loop gain at resonance exerts positive feedback with a value of $A_{initial}$, given by equation (5.3):

$$A_{initial} = g_{m1} R_L \frac{C_1}{C_2} \tag{5.3}$$

The initial loop gain must be larger than unity for oscillation. In Chapter 4, we calculated a theoretical maximum for R_L based only on FBAR parameters (607Ω). We will now expand this model to include the circuit non-idealities. First, we will review the transformation of the resonator motional resistance to R_L. As shown in Chapter 4, the load resistance due purely to R_X at the parallel resonance is given by equation (5.4):

$$R_L|_{R_x} = \frac{1}{R_x \omega_o^2 \left(C_o + \frac{C_1 C_2}{C_1 + C_2} \right)^2 \left(\frac{(C_1 + C_2)^2}{C_2^2} \right)} \tag{5.4}$$

Next we must take into account the finite Q of the resonator membrane capacitance and the lumped C_1 and C_2 capacitances. Given Q_{cap}, the equivalent resistance in series with the total capacitance is shown in equation (5.5):

$$R_{cap} = \frac{1}{\omega Q_{cap} C_T} \tag{5.5}$$

Where C_T is the capacitance seen by the resonator, given by equation (5.6):

$$C_T = \left(C_o + \frac{C_1 C_2}{C_1 + C_2} \right) \tag{5.6}$$

Thus, the load resistance due to finite capacitor Q is shown in equation (5.7):

$$R_L|_{Q_{cap}} = \frac{Q_{cap}}{\omega_o \left(C_o + \frac{C_1 C_2}{C_1 + C_2} \right) \left(\frac{(C_1 + C_2)^2}{C_2^2} \right)} \tag{5.7}$$

The next contribution to the loading of the oscillator is the bias resistor formed by M_{fb} in the schematic (Figure 15) above. Ideally infinite, the resistance R_{fb} formed by M_{fb} loads the output through the capacitive divider formed by C_1 and C_2. The loading to R_L can then be written as equation (5.8):

$$R_L|_{R_{fb}} = \frac{R_{fb}}{\left(\frac{(C_1 + C_2)^2}{C_2^{\,2}}\right)} \tag{5.8}$$

The final contributions to the oscillator loading are the finite output conductances of M_1 and M_2. We notice that, at resonance, the drain capacitance of M_1 and M_2 are tuned out by the inductive resonator. Thus, we see the DC value of the output conductance of these devices at resonance. As shown in equations (5.9) and (5.10), the output DC conductances of M_1 and M_2 directly load the oscillator.

$$R_L|_{M_1} = r_{01} \tag{5.9}$$

$$R_L|_{M_2} = r_{02} \tag{5.10}$$

We can now find the total loading of the oscillator due to all resonator and circuit non-idealities. This is most intuitively expressed as equation (5.11):

$$R_L = \frac{1}{G_1 + G_2 + G_3 + G_4 + G_5} \tag{5.11}$$

Where the conductances in equation (5.11) represent the individual components of the oscillator loading. These are shown in equations (5.12)-(5.16):

$$G_1 = \frac{1}{R_L|_{R_X}} \tag{5.12}$$

$$G_2 = \frac{1}{R_L|_{Q_{cap}}} \tag{5.13}$$

$$G_3 = \frac{1}{R_L|_{R_{fb}}} \tag{5.14}$$

$$G_4 = \frac{1}{R_L|_{M_1}} \tag{5.15}$$

$$G_5 = \frac{1}{R_L|_{M_2}} \tag{5.16}$$

Using the form of equation (5.11), the final expression for the loading of the oscillator can now be written as equation (5.17):

$$R_L = \frac{1}{\left(R_X\omega_0^2\left(C_0+\frac{C_1C_2}{C_1+C_2}\right)^2\left(\frac{(C_1+C_2)^2}{C_2^2}\right)\right)+\left(\left(\frac{(C_1+C_2)^2}{C_2^2}\right)\frac{\omega_0\left(C_0+\frac{C_1C_2}{C_1+C_2}\right)}{Q_{cap}}\right)+\left(\frac{\frac{(C_1+C_2)^2}{C_2^2}}{R_{FB}}\right)+\frac{1}{r_{01}}+\frac{1}{r_{02}}} \tag{5.17}$$

It is now possible to optimize various circuit and resonator parameters to achieve minimal power consumption and maximum performance. It is important to realize that the FBAR device parameters are innately coupled with the CMOS parameters in the oscillator design equations. As such, the design of the FBAR resonator must proceed

directly alongside the design of the CMOS circuitry. The sizing of the FBAR resonator will proceed in this following section with the CMOS design.

5.3.2 C_1/C_2 Ratio

First, the ratio of C_1 to C_2 will be optimized. As mentioned in Chapter 4, it has been shown in literature that optimal performance is obtained with $C_1=C_2$.[27] However, it is worthwhile to explore this design decision as it opens up an additional degree of freedom in the design of ultra-low power oscillators. Intuition can be gained by plotting the ratio of C_1/C_2 versus the startup factor. To achieve oscillation, the initial closed loop gain $A_{initial}$ must be larger than unity. For a given transconductance, $A_{initial}$ is determined only by the product of R_L and the feedback factor (C_1/C_2). We will therefore define the startup factor as [R_L*(C_1/C_2)]. The value of C_2 is assumed fixed (and relatively large) due to the gate capacitance of M_1. Thus, we will plot the startup factor vs. the ratio of (C_1/C_2) by varying only C_1. This is shown below in Figure 16. The estimated circuit values used in the computation of R_L are R_{o1}=1kΩ, R_{o2}=20kΩ, and C_2=1pF.

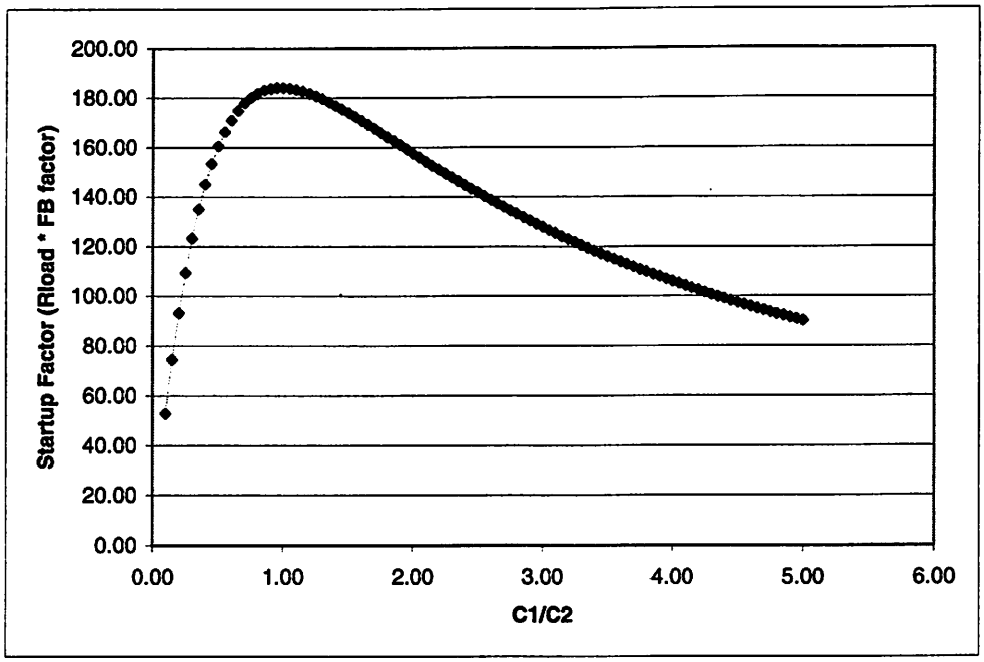

Figure 16. Optimization of the Capacitance Ratio C_1/C_2

Figure 16 shows that the start-up condition requiring the smallest g_m is given when $C_1=C_2$. Therefore, even though it would result in an increased total capacitance, it behooves the designer to add explicitly to the value of C_1 if it is smaller than C_2. The decision to add explicit capacitance also depends on whether the oscillator is operating in a g_m (startup factor) limited regime or a output signal swing (R_L) limited regime, as described in Chapter 4. If the bias current is not limited by the achievable transconductor g_m, it is best *not* to add explicit capacitance because it would increase the loading on the oscillator.

5.3.3 Feedback Transistor

Transistor M_{fb}, as shown in the schematic in Figure 15, merely provides a gate bias voltage for M_1. The only requirement is that the added capacitive and resistive

loading on the oscillator due to M_{fb} must be entirely negligible. In Chapter 4, the theoretical maximum R_L for a sample FBAR resonator based three-point oscillator was 607 Ω. As shown in equation (4.16), we know that any feedback resistance R_{fb} is reflected to the output as $R_{fb}/4$ (assuming $C_1=C_2$). We will design for the reflected value of R_{fb} being at least twenty times (20X) our theoretical output resistance (20*600*4 = 48kΩ). To calculate the device sizing necessary, we will use the ideal square-law MOSFET model.

$$R_{fb} = R_{ds,M_{fb}} \approx \frac{1}{\mu C_{ox} \frac{W}{L}\left(V_{gs} - V_T\right)} \tag{5.18}$$

Taking into account the body effect of M_{fb} on the threshold voltage, a sizing of W/L = (0.5μm/4μm) was deemed appropriate. The device capacitances are negligible in relation to C_1 and C_2. It is interesting to note that, although a submicron CMOS process was used, M_{fb} observed the ideal MOSFET square law model due to the extremely long channel length used.

5.3.4 FBAR Resonator Sizing

In Section 4.2, the discussion about the FBAR resonator indicated that, for a given resonant frequency, the area of the membrane can be varied. In summary, as the area increases, C_o increases and R_x decreases. The opposite occurs when the area is decreased. Further, one of the most important parameters in the oscillator design is the value of the real part of the output impedance at oscillation, R_L. Through intuition and the examination of equation (5.17), it is known that R_L decreases as C_o increases (loading

increases), but R_L increases as R_x decreases (loading decreases). This implies that an optimal FBAR membrane sizing for this oscillator exists. The most effective way to obtain the optimal value is by plotting R_L vs. FBAR membrane area. Figure 17 shows three different curves for three different values of C_1=C_2, (0.5pF, 1pF, and 2pF).

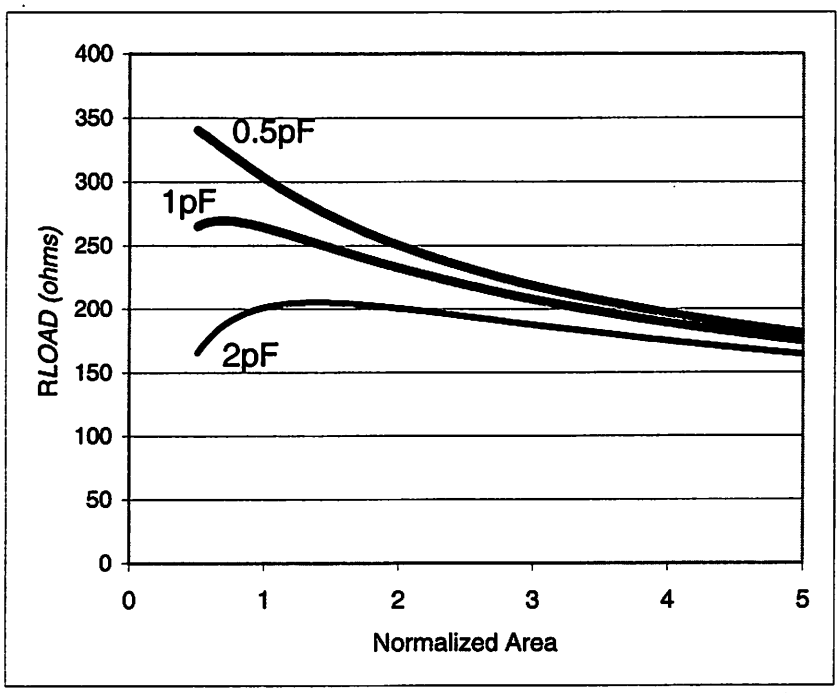

Figure 17. Optimization of FBAR Resonator Membrane Area

The x-axis of Figure 17 is the normalized area of the FBAR membrane. The y-axis is the total oscillator loading in ohms given by equation (5.17). This plot was completed using estimated circuit parameter values (R_{o1}=1.5kΩ, R_{o2}=20kΩ); iteration through the design methodology is necessary to converge on an optimal design. The first thing to notice is that R_L decreases as the capacitors C_1 and C_2 are increased. We know from equation (5.17) that the loading increases as C_T^2, so it is important to minimize the sizes of C_1 and C_2. From the plot above, there is a definite optimal FBAR membrane area. It was

predicted that the final values of C_1 and C_2 would be approximately 1pF, so an FBAR resonator with an normalized area parameter of 0.7 (approximately 100μm x 100μm) was fabricated.

5.3.6 Main Transconductor (M_1) Design

This section describes the sizing of transistor M_1 in the schematic of Figure 15. Since it provides the critical transconductance necessary for start-up, and because its capacitance dominates all parasitic capacitances in the oscillator, transistor M_1 is the most important device in the design. The device sizing depends on whether the oscillator is start-up limited or voltage-swing limited. To determine this, the g_m required for start-up is calculated and then the bias current to provide the desired output swing is determined. As discussed in Section 4.3.2, this design is voltage-swing limited.

To ascertain the necessary g_m required for start-up, an estimate of the total output load resistance must be calculated. Estimated circuit parameters of C_1=0.8pF, R_{o1} = 1.5kΩ, R_{o2} = 20kΩ, and R_{fb} = 50kΩ yields a value of R_L = 298Ω. With $C_1 = C_2$, we need a transconductance of $1/R_L$ to sustain oscillation. To ensure a reliable start-up, we will specify a g_m of at least $2/R_L$, or approximately 7mS.

To achieve the desired output voltage swing of 100mV zero-peak, we first need to determine the ratio of the fundamental harmonic component of the M_1 drain current to the bias current (I_1/I_{bias}). This depends on the operating region of M_1, which is typically weak inversion for most efficient operation.[27] For this design, the analytical value of (I_1/I_D)=1.3 agreed well with simulations. To calculate the bias current necessary for an output swing of 100mV, equation (5.19) is used:

$$\hat{V}_o = I_1 R_L = \frac{I_1}{I_{bias}} I_{bias} R_L \tag{5.19}$$

This corresponds to a bias current of approximately 260μA. To account for device and capacitive process variations, 300μA was chosen to achieve the desired output swing.

It can now be determined whether the oscillator is start-up limited or voltage-swing limited. With the values calculated thus far, the required (g_m/I_d) is (7mS/300μA)=23. This ratio is definitely achievable for a MOSFET in weak inversion, so we are slightly voltage-swing limited. M_1 should be sized to achieve a g_m of 7mS at a bias current of 300μA. This corresponds to a sizing of (500μm/0.18μm), yielding a drain junction capacitance of approximately 400fF and a total gate capacitance of approximately 500fF. The DC output resistance is 1.5kΩ. At this point, the critical parameters have been determined and iteration through the design flow can continue until the desired results are achieved.

5.3.7 Bias Design

For the oscillator, the bias design was relatively simple. It must supply bias current to M_1 and add negligibly to the capacitive and resistive loading to the output. In addition, the bias circuitry should not add appreciable noise to the oscillator core. Using an M_2 sizing of (25/0.5), an output resistance of 20kΩ was achieved with little capacitive loading. To suppress biasing noise, on-chip de-coupling capacitors totaling 29pF were placed on the gate of M_2.

5.3.8 Buffer Design

An on-chip buffer was designed to drive the off-chip test equipment. The design specifications of the buffer are listed below.

- Must drive a 50Ω, 1pF load at 2GHz
- Must minimize the capacitive loading to the oscillator (C_{in}<50fF)
- Must be DC coupled to the oscillator, $V_{dc}=V_{gs1}=0.4V$
- Power consumption of buffer not critical

These goals were achieved by using a PMOS source follower cascaded with an NMOS source follower. See the schematic below.

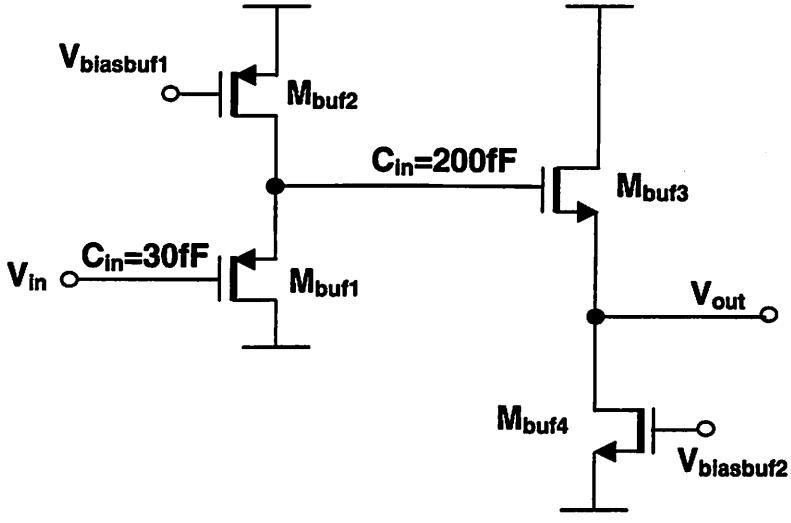

Figure 18. Simplified Oscillator Buffer Schematic

This topology allows a wide range of DC input voltages without using an AC coupling capacitor. As previously mentioned, a DC coupling-only philosophy was chosen for this

design. One of the main issues with this buffer design is the severe headroom constraint placed by the stacking of ($V_{gsM1} + V_{gsMbuf1} + V_{dsatMbuf2}$). Headroom issues dictate that the buffer core operate on no less than a V_{dd} of 1.8V. This buffer topology must be modified for supply voltages less than this. The total capacitive load presented to the oscillator is 30fF, and the output resistance of the buffer is less than 50Ω. The gain of each stage is less than unity, ensuring buffer stability. A total of 6mA are consumed in the buffer core. The total voltage gain from the oscillator to the output pad is approximately 0.5 (-6dB).

5.4 Implementation

As with all RF designs, great care must be taken in the actual implementation to ensure correct and robust operation, easy and repeatable testability, and tolerance to packaging and handling treachery. This section discusses the measures taken during the physical implementation to increase the probability of successful operation.

5.4.1 Layout

Substantial attention was paid in the layout of two very sensitive nodes: the oscillator input (gate of M_1) and the oscillator output (drain of M_1). As shown in the previous sections, minimizing the capacitance of these nodes is crucial. This was made especially difficult because both of these nodes have to be taken off-chip and bonded to the FBAR resonator. Because of this, the capacitance due to bondpads and any electro-static discharge (ESD) protection devices would directly load the oscillator. See Figure 19 for the CAD layout of the oscillator and buffer core.

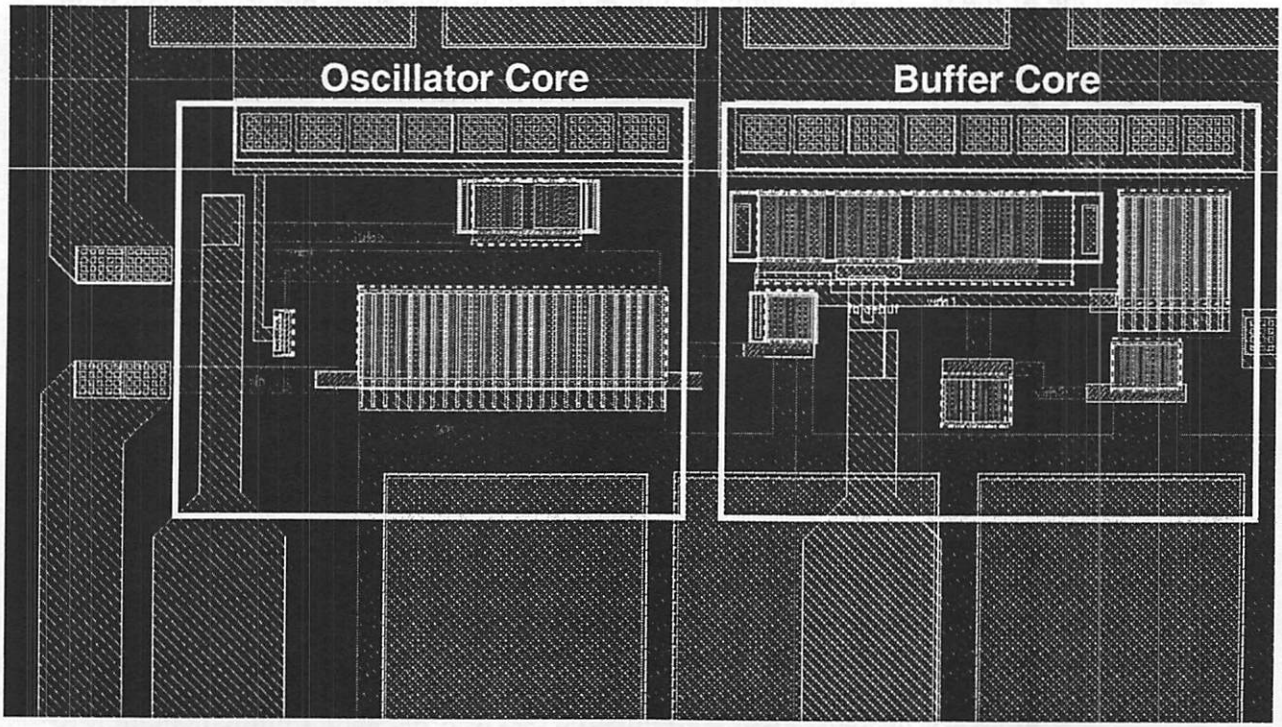

Figure 19. CAD Layout of Oscillator and Buffer Core

To minimize the capacitance of the bondpads, the signals were routed to a M6-M5 pad layer. M1 was used as a ground plane under the pad. This created a much lower parasitic capacitance than the standard M6-M1 pad stack. Using this method, the $(80x80)\mu m^2$ pads contributed less than 100fF of parasitic capacitance. The four DC bias pads (oscillator V_{dd}, buffer V_{dd}, oscillator bias, buffer bias) utilize a traditional M6-M1 pad stack.

For submicron CMOS processes with very thin gate oxides and copious use of plasma processing, the so called "antenna effect" is acute, especially when long metal lines are used. The antenna effect describes the process of building up enough charge on metal interconnects during processing to destroy the transistor gate oxide, rendering the circuit useless. In addition, ESD damage to the gate of M_1 could potentially reduce sample yield. Because of these concerns, a small diode was implemented between the

gate of M_1 and ground to reduce the probability of gate oxide damage. This diode added approximately 30fF of parasitic capacitance. No diode protection was used on the oscillator V_{out} node (drain of M_1) or the output of the buffer. This was appropriate because, in addition to being sensitive to parasitic capacitances, these nodes do not directly contact any gate oxide. All other pads used full ESD diode protection.

To reduce the effects of power supply noise, and eliminate the possibility of instability due to a power rail feedback loop, 100pF of on-chip de-coupling capacitance was added to the oscillator V_{dd} and the buffer V_{dd}. This was formed using poly to n-well capacitors, which offered a reasonable capacitance density. A large, fully contacted ground plane consisting of M_1 surrounded the active area to minimize ground inductance. Figure 20 shows a die photo of the oscillator implementation.

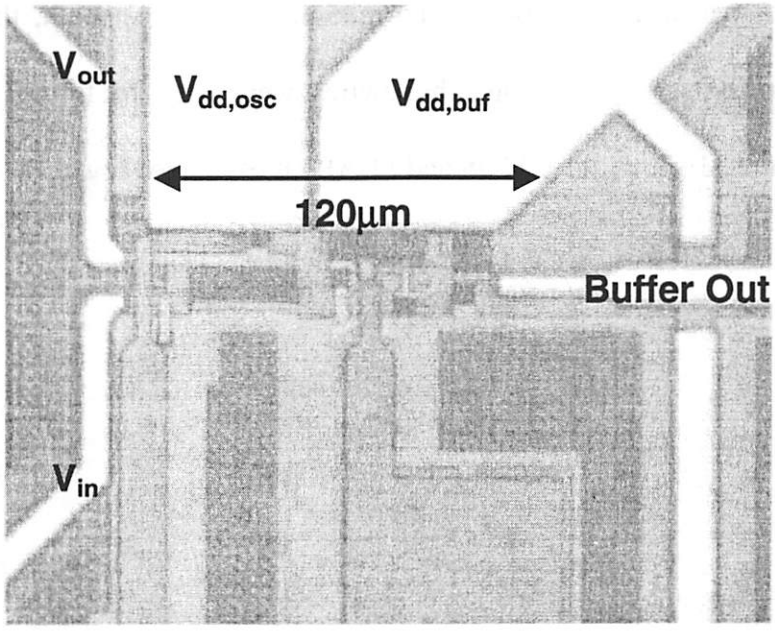

Figure 20. Oscillator Die Photo

Figure 20 shows the input and output signals of the oscillator routed in M6 to the bonding pads. These are the nodes that are wirebonded directly to the FBAR resonator. Also visible is the buffer output signal that drives the output pad.

5.4.2 Packaging

Since it was necessary to bond the CMOS chip to the FBAR resonator chip, packaging was an important part of the implementation. Both chips were designed with a pad-to-pad spacing of 290μm. This minimum spacing was dictated by the resonator sizing of (100x100)μm^2 as shown in the design section above.

Wirebonding was used to electrically bond the CMOS and FBAR chips together. The parasitic partial inductance of a typical wirebond is approximately 1nH/mm of wire length. For this design, it was necessary to minimize this parasitic inductance to avoid the possibility of parasitic oscillations. To minimize the wire length, the chips were placed less than 200μm apart. Dual bondwires were used to further decrease the inductance. Figure 21 shows the CMOS and FBAR chips bonded together.

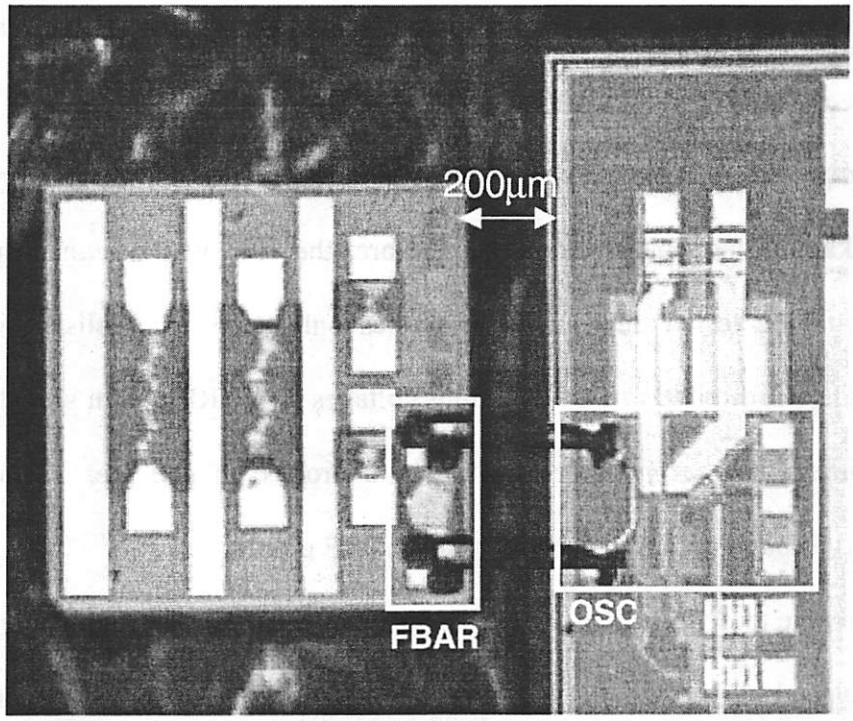

Figure 21. Oscillator Bonded To Resonator Chip

As shown in Figure 21, the FBAR chip shows multiple test structures. The only device in use is the resonator on the southeast corner of the chip. Both chips were bonded with conductive epoxy to a gold substrate.

5.4.3 Design for Test

Although generally considered a mundane task, thorough design-for-test is a crucial part of analog IC design. There are two main goals of design for test. First, it should be possible to fully characterize all important circuit aspects with minimal effort after fabrication. The most risky circuit elements should have easy-to-access knobs so troubleshooting can be performed. Secondly, the performance of the circuit in its actual system level habitat should be visible through the prototype performance. For example,

the device under test should not see additional loading from the test setup that it would not see in an actual system implementation.

For this design, it was desirable to be able to perform complete characterization without packaging and board design. Therefore, the chip was designed such that all functions could be tested through wafer probes only. To accomplish this, the total number of IOs was limited to 5 (4 DC input voltages and 1 RF output signal). It would not be feasible to place any more than 5 or 6 probes on one die. Grounding was accomplished through the Ground-Signal-Ground RF probes.

To be able to differentiate the performance of the oscillator and buffer, a separate buffer was placed on the die. The loading from the buffer is approximately what the oscillator would see from subsequent circuit blocks in a system level implementation. Thus, the measured performance is a good indicator of the achievable performance in a complete RF system. Chapter 6 will discus the measured performance results from the oscillator.

Chapter 6. Results

6.1 Introduction

This chapter discusses the measured experimental results of the FBAR based oscillator designed in Chapter 5. To facilitate testing, the phase noise measurements were taken with a packaged part. For the other measurements, data was taken directly from the die using a Cascade probe station and Cascade Air Coplanar Ground-Signal-Ground RF probes. Passive DC probes were used to apply the four bias voltages to the chip. An HP 6626A DC power supply was used to generate the requisite bias voltages.

6.2 Experimental Results

The basic circuit functionality, frequency spectrum, phase noise, signal power output, and start-up time of the oscillator are explored in this section.

6.2.1 Frequency Spectrum

The oscillator core was biased at 300μA with a power supply voltage of 1V. The measured oscillator frequency spectrum is shown below in Figure 22.

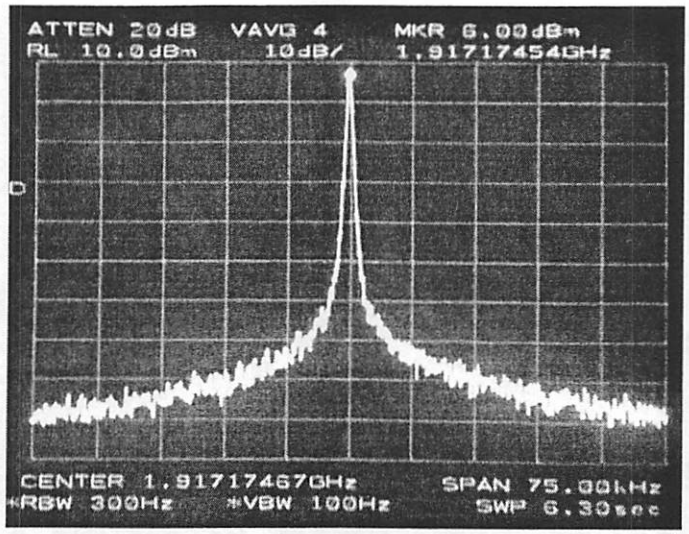

Figure 22. Measured Oscillator Frequency Spectrum

The measurement shown in Figure 22 was taken with an HP8563E spectrum analyzer. A wideband 50Ω amplifier with a power gain of 21dB (up to 5GHz) was inserted before the spectrum analyzer.* The spectrum amplitude marker in Figure 20 shows 6dBm, which indicates approximately –15dBm at the buffer output. This corresponds to a voltage of 56mV at the buffer output. Since the buffer gain was designed to be 0.5 (-6dB), the oscillator voltage swing is approximately 100mV zero-peak as designed (-17dBm across a 298Ω load). There are no spurious tones visible in the output spectrum. This indicates an absence of parasitic low-frequency mechanical resonances, which have plagued previous oscillators constructed using micromechanical passives.[28] Initial spurious tones were observed, but it was discovered that they arose due to insufficient substrate grounding. Grounding the chip through the Ground-Signal-Ground RF probe only will be avoided in the future. A subsequent ground wirebond eliminated the spurious tones.

* Amplifier designed and provided by Brian Kautz of Agilent Technologies.

The level of the harmonic components were all measured to be greater than 30dB below the carrier. For the 2nd, 3rd, 4th, and 5th harmonics, the amplitudes were measured to be 30dB, 36dB, 45dB, and 49dB below the carrier, respectively. These measurements were also taken with an HP8563E spectrum analyzer. A total of nine samples were bonded. All were functional, and Table 5 lists the measured output of all nine samples.

Table 5. Measured Results of all Oscillator Samples

Sample Number	f_{osc} (GHz)	Output Power (dBm)
1	1.91493	-15.67
2	1.91390	-14.67
3	1.89461	-15.33
4	1.89670	-14.50
5	1.89630	-13.50
6	1.90121	-14.67
7	1.91725	-15.67
8	1.89730	-13.67
9	1.91290	-15.5

This data corresponds to a standard deviation of oscillation frequency of 9.46 MHz (4,978ppm). As shown in Section 4.3.1, this large frequency variation is not possible through process variation in capacitor values alone. Thus, the variation is caused by actual variation in the series resonance of the FBAR samples. The FBAR samples used in this design did not undergo a final trimming step, which explains the

relatively large frequency variation observed. The output power measured at the buffer indicates a buffer output signal level range of 50mV to 66mV. This variation is due to process variations in the FBAR resonator, the oscillator component parameters, and variation in the buffer signal gain.

6.2.2 Phase Noise

The short-term stability, or phase noise, is one of the most important oscillator parameters. As mentioned in the introduction, the phase noise measurements were taken with a packaged part to ensure sufficient substrate grounding and make the measurement setup easier. Figure 23 shows a plot of the measured oscillator phase noise.

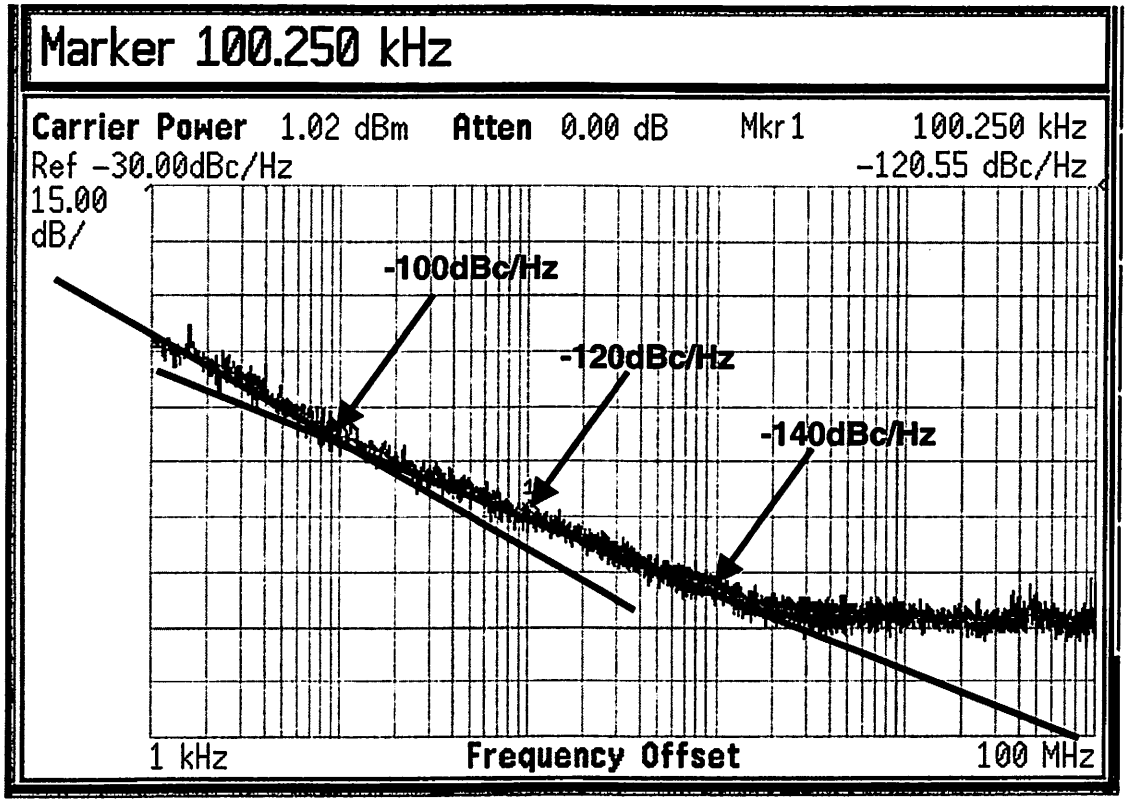

Figure 23. Measured Oscillator Phase Noise

The phase noise measurement in Figure 23 was acquired with an Agilent E4445A PSA. As shown in Figure 22 above, the measured phase-noise of the oscillator is –100dBc/Hz at 10kHz offset, -120dBc/Hz at 100kHz offset, and –140dBc/Hz at 1MHz offset. Our phase noise model introduced in an earlier chapter predicts a phase noise of -131dBc/Hz at 100kHz offset for the final oscillator design parameters. The additional phase noise is due to the active device noise figure and excess resistive loading on the oscillator, which reduces the loaded oscillator Q. As shown in Figure 22, the $1/(f)^3$ noise corner is approximately 10kHz and the $1/(f)^2$ noise corner is approximately 2MHz. All phase-noise data was re-measured and verified with an HP 3048A phase-noise measurement system.

6.2.3 Oscillator Start-Up

The oscillator start-up time determines the amount of overhead required to achieve oscillator steady-state. This metric is important for ultra low power systems using heavy duty-cycling, where the amount of overhead in enabling and disabling blocks must be minimized. Equation (6.1) predicts the time constant of the onset of oscillation for a tuned oscillator.

$$\tau = \frac{2Q_{LOADED}}{\omega_o(A_l - 1)} \sim 100nS \tag{6.1}$$

For the FBAR based oscillator, the approximate time constant is 100nS. Oscillator start-up occurs in less than 10 time constants. Thus, the start-up time of the oscillator is predicted to be <1μS. Figure 24 shows the measured transient start-up of this oscillator.

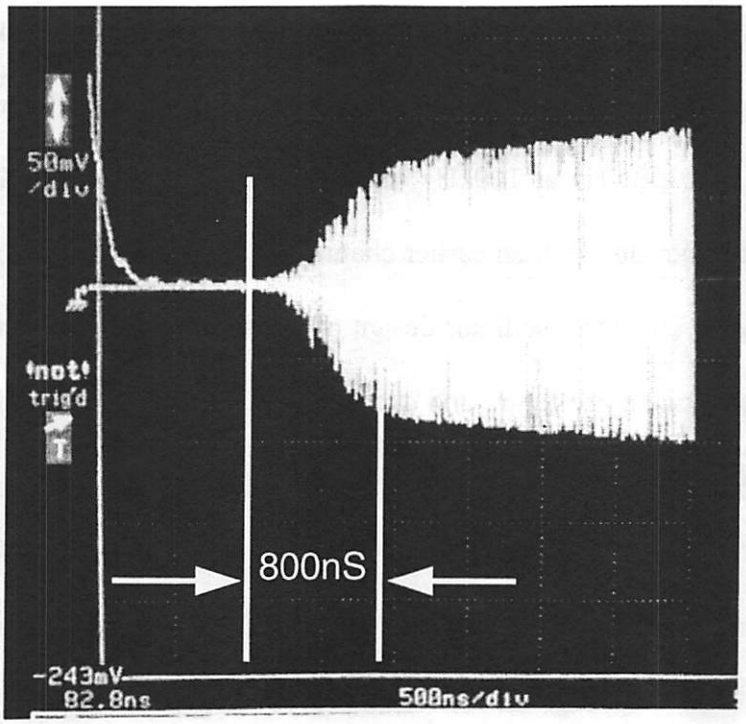

Figure 24. Measured Transient Start-Up of Oscillator

The start-up time of the oscillator is approximately 800nS. This is consistent with the anticipated $Q_{LOADED}/(A_I-1)$ ratio of approximately 600. The start-up time is significantly less than that of a frequency synthesizer, and it enables interesting modulation possibilities for ultra low power RF transceivers. For example, for low bitrate data signaling, it is possible to cycle the oscillator on and off between transmitted bits. In this manner, on-off keyed (OOK) signaling is performed while conserving system power through heavy duty cycling of the oscillator. Figure 25 shows the oscillator cycled on-off at 10kHz.

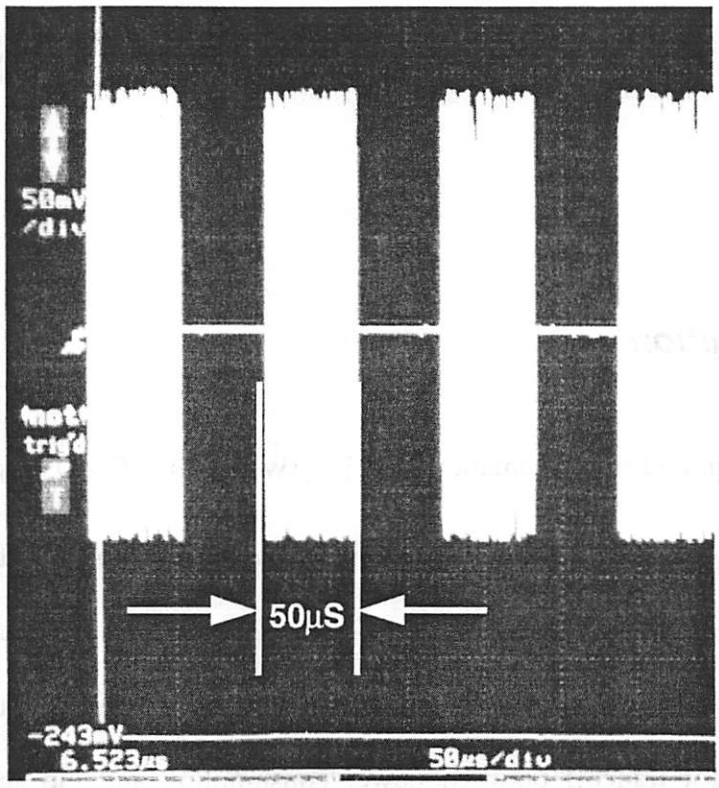

Figure 25. Oscillator Cycled On/Off at 10kHz

Thus, it is possible to cycle the oscillator on-off for OOK data transmission at rates at greater than 20kbps. It has also been shown that, by varying the rise and fall time of the oscillator bias current, analog pulse shaping of the transmitted pulse is possible with this oscillator.

This chapter reported the measured experimental results of the FBAR based oscillator. The frequency spectrum properties, frequency variation, output power, phase noise, and start-up time of the oscillator were measured. Variations between calculated and measured values were discussed.

Chapter 7. Conclusions

7.1 Introduction

The design and implementation of a 300μW, 1.9GHz CMOS oscillator utilizing FBAR resonators has been demonstrated. As discussed in Chapter 2, this research was motivated by the aggressive specifications for the RF transceiver required by the UC Berkeley PicoRadio project. It was shown that, in ultra low power RF transceiver design, there is an inherent tradeoff between power consumption and the achieved level of integration. It was also shown that a majority of the power consumption in low power receivers is consumed in the local oscillator. Another observation is the inherent tradeoff between power consumption and phase noise in traditional frequency synthesizers. These observations set the stage for research in alternate methods of sinusoid generation. An ultra low power, low phase noise oscillator was obtained by co-designing RF MEMS components with standard submicron CMOS. Since the Agilent FBAR resonator is micromachined out of a silicon substrate, this design could potentially constitute a fully integrated solution. This chapter summarizes the measured performance of the oscillator and recommends future work on the subject.

7.2 Summary of Research Results

Some important results from this research are summarized below:

- A 1.9GHz, 300μW frequency generator suitable for ultra low power RF transceivers was designed, implemented, and tested.
- A methodology for the design of ultra low power oscillators using RF MEMS resonators was introduced.
- Theoretical frequency stability, power dissipation, and phase noise performance limitations were derived in a general manner to facilitate the evaluation of new RF MEMS and CMOS technologies.
- The co-design of RF MEMS and CMOS as a powerful RF design technique was demonstrated.
- The oscillator achieved a phase noise of –120dBc/Hz @ 100kHz offset and a start-up time of 800nS.

7.3 Future Work

Though the initial goals of this project were met, there are areas of future research that would benefit the RF design community as a whole. These areas will be introduced in this section.

7.3.1 FBAR Based VCO

One of the most exciting areas for future research is utilizing the strengths of the FBAR resonator in other oscillator topologies. For example, this paper describes and

analyzes a constant frequency oscillator designed to run in an open-loop configuration. While frequency calibration via discrete capacitance switching was discussed, there are definite benefits to designing an FBAR based VCO. As previously mentioned, traditional quartz crystal stabilized frequency synthesizers suffer from phase noise degradation due to poor VCO phase noise characteristics. As shown in this work, FBAR based oscillators are capable of excellent phase noise with very little power consumption. Using an FBAR based VCO in a traditional frequency synthesizer loop would greatly reduce the power consumption and improve phase noise performance over what is currently achievable. The main issue that will need to be overcome in the implementation of an FBAR based VCO is the tuning range of the oscillator. Since the loaded Q of the proposed oscillator is very high, the tuning range will be limited. One potential solution is to selectively de-Q the oscillator or use a filter ladder network instead of a single resonator to increase the tuning range. This would, of course, jeopardize some of the phase noise performance. Continued research into this topic would solve these issues and yield exciting results.

7.3.2 Amplitude Control Loop

One modification that would benefit the proposed oscillator is an amplitude control loop. By detecting the amplitude of oscillation and closing a control loop back to the bias current of the main transconductor, an effective and efficient amplitude control loop can be implemented. This would have a number of substantial benefits to the oscillator performance. First, if the design is start-up limited (g_m limited), the power consumption will be lowered with an effective amplitude control loop. This is because, for start-up, we need our transconductance to be 2-3 times greater than $1/R_L$, the effective

oscillator loading. This is done to ensure unconditional start-up through process and environmental variations. An amplitude control loop will limit the current to deliver only the critical trasnconductance, increasing the efficiency of the oscillator. In addition, it has been shown that an amplitude control loop decreases oscillator non-linearities.[27] Finally, an amplitude control loop would decrease the oscillator start-up time by providing increased device current during start-up.

7.3.3 Differential Oscillator

Another area of further research is the investigation of a suitable differential oscillator topology. Whether the oscillator is designed as a VCO or as a frequency reference, a differential topology has a number of advantages. First, as with all differential analog circuits, this topology is less susceptible to power supply noise. The power supply rejection ratio (PSRR) becomes even more important when large-scale integration with digital components is considered. Another benefit that a differential structure would provide is increased signal swings. Increased signal swings can be utilized to improve the phase noise performance of oscillators. In addition, it may be desirable to connect the oscillator directly to the antenna of certain systems for data transmission. If so, large signal swings may be necessary to achieve the specified transmitted power. This is difficult to achieve with very low power supply voltages. A differential oscillator would help solve that problem by allowing larger signal swings.

7.3.4 Packaging

It is technologically possible to integrate RF MEMS (eg. Agilent FBAR) with silicon-based circuits (eg. CMOS). However, to maintain a high fabrication yield in both processes, it may be desirable to optimize each process separately and avoid full integration. In that case, the packaging of RF MEMS/CMOS components becomes critical to the form factor, cost, and performance of the design. Although this work demonstrates an efficient implementation constructed through wirebonding and close spatial placement of the chips, it is desirable to have an even more efficient packaging scheme. Flip chip techniques would allow a smaller form-factor and decreased inductance between the RF MEMS and CMOS components. Another option is to leverage a recently proposed wafer-level chip-scale encapsulation of the FBAR resonators.[29] Instead of encapsulating the resonator with a blank silicon die, the encapsulation layer would be the CMOS die. This would provide a small form-factor and short interconnects between the chips. A third option is using fluidic self-assembly (FSA) to assemble the chips on a common substrate.[30] This option would enable the use of very small bondpads, reducing the parasitic capacitances on sensitive nodes. Additionally, it would allow very short interconnects and the potential for all components (even antennae) on the same substrate. Future work in packaging is necessary to ensure economic and reliable mass production of RF MEMS/CMOS systems.

This chapter has summarized key findings and has proposed additional work to augment the research results described above. This will enable the migration of these technologies from ultra low power transceivers to other design regimes, including high performance RF communications systems.

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