SIX-INCH CMOS BASELINE PROCESS IN THE UC BERKELEY MICROFABRICATION LABORATORY

by

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Memorandum No. UCB/ERL M02/39

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

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Abstract

This year the Microlab reached a major milestone by completing the six-inch upgrade project. This report focuses on the six-inch upgrade, slight deviation from the traditional way of baseline reporting, to include: equipment upgrade, process development activities, parametric test results of the first six-inch baseline run, as well process and device simulation performed on our latest four-inch baseline process (a twin well 1.3 μm CMOS technology with double metal and double poly-Si option).

An entirely new DUV lithography module was implemented on our six-inch lithography equipment. A modified version of the latest four-inch CMOS baseline process flow was used to process our first six-inch run (CMOS150). Chemical-mechanical polishing (CMP) process was introduced at the interconnect module allowing for a triple metal layer process. The rest of the CMOS baseline processes was successfully transferred onto the newly upgraded six-inch equipment. This completed the six-inch upgrade project and the CMOS150 run (six-inch) was successfully processed through this fabrication line. This run was a crucial part of the six-inch upgrade project, and a determining factor in completion and release of the six-inch baseline process line. Advent of this run at a particular process step often energized the upgrade activities around that particular module, further defined the upgrade schedule and the planning phase of the project. Finally, electrical parametric tests were performed on PMOS and NMOS discrete transistors of the CMOS150 run, which are included in this report.

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1. Introduction

The Microfabrication Laboratory at the University of California, Berkeley has been supporting silicon MOS technology from the time the present VLSI facility was opened in 1983 [1,2]. In April 1992 a CMOS baseline was formally reestablished, which has been running on four-inch substrates up until recently, when the first six-inch CMOS baseline run was successfully completed. The first CMOS baseline report [3] described a 2 μm, n-well, double poly-Si, double metal CMOS process, which was subsequently developed into a twin-well, 1.3 μm, double poly-Si, double metal process. This process was further refined, and ultimately 1 μm transistors were fabricated on four-inch substrates in 2000 [4].

The CMOS baseline has always specified the standard process modules for VLSI operations, and provided test circuits and a starting point for various research groups such as: Berkeley Sensor and Actuator Center (BSAC), Berkeley Computer Aided Manufacturing group, and Berkeley Microfabrication Laboratory Affiliates [5,6,7]. The baseline run in conjunction with regular in-line monitoring of the process equipment has given the staff an effective means to discover, and address equipment and/or process problems in the Microlab. This is one reason why baseline process has continuously been modified (updated) to address current status of equipment.

The six-inch upgrade project demanded successful transfer of the latest CMOS baseline process over to the newly installed, and upgraded six-inch process equipment. The first six-inch run (CMOS150) played an important role in gauging the success of the six-inch upgrade project, further facilitated the final release of the six-inch equipment and CMOS baseline process. As always, the CMOS baseline run has proved its value, and will continue to do so, as we will install more advanced equipment, improve our existing equipment, which will need evaluation and monitoring. A more advanced baseline will be developed to push the envelope on the current and future equipment set, as part the of the ongoing CMOS baseline development activities in the Microlab.

2. Six–inch Equipment Upgrade and New Installations

For the past couple of years process staff has been busy developing processes for six-inch silicon wafers in the Microlab. This work was prompted by the installation of new six-inch lithography equipment, and the upgrade of others from four-inch capability to both four and six-inch capability. The installation of a new ASML 5500/90 stepper, CD-SEM, and SVG-8800 coater tracks provided us with the opportunity to implement a state of the art Deep-UV lithography process in the Microlab. This module is based on Shipley resist chemistry (UV210 DUV resist) at a resolution limit of 0.35 μm feature sizes, a great improvement over the I-line process used by the four-inch CMOS baseline processes. All of our diffusion and LPCVD furnaces and plasma etchers were gradually upgraded to enable the six-inch processes, while maintaining the four-inch operation. Oxide and metal etchers were upgraded to handle both four and six-inch substrates. This included RF electrode, diffuser ring replacement, and wafer handler hardware modification that could handle both four and six-inch substrates sizes in the lam2 and lam3 etchers. Lam4 was converted to a six-inch (only) machine to address both of our poly etch and nitride etch requirements.

Substantial effort was expended on characterizing the furnaces. This included temperature profiling, hardware integrity check, process development, and performing multiple runs aimed at optimizing various oxidation, annealing and deposition processes. The film quality is very much dependent on temperature control across the flat zone and without such control no reliable process could be realized.

A major issue with the new furnace elements was resolved. A defective heater element in Tystar10 (poly furnace) had to be replaced. This element produced about 40C temperature variation across the flat zone of the furnace. A different heater element supplier was then selected, which provided us with much better heater elements (design), hence, a much tighter temperature control was realized. Figure 1 shows the temperature profile for both defective and good element. Power connection, and element type (mass) issues were also internally addressed and corrected.

Process staff then was able to develop reliable six and four inch processes on our newly upgraded furnaces that often out perform the old four-inch process. A new wet sink (Sink9) was also installed to support the six-inch CMOS baseline process. This concluded the six-inch upgrade necessary for fabrication of the first six-inch baseline run in the Microlab.

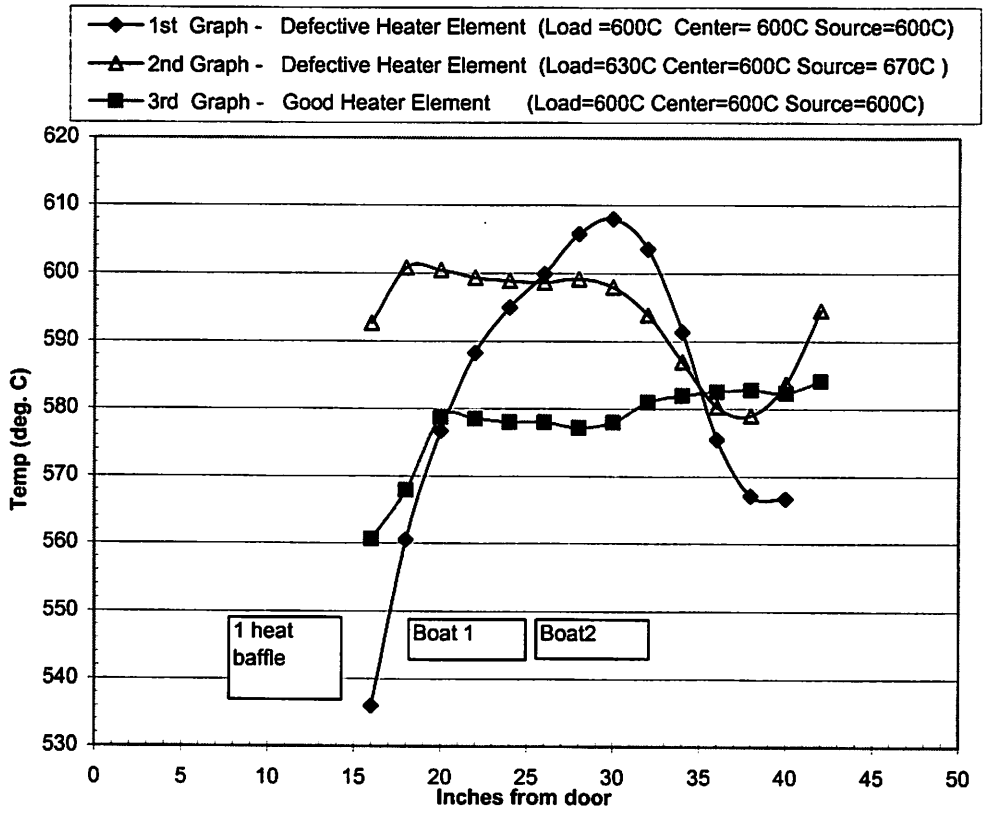


Figure 1 Temperature profile across center, source and pump zones of Tystar10, poly-Si LPCVD furnace

3. Six–inch Process Development and Characterization

The entire six-inch upgrade discussion could easily exceed the scope of this study; therefore, we only describe specific parts of the project that pertain to the six-inch CMOS process. The six-inch process was developed based on the latest four-inch, twin well, 1.3 μm, double poly-Si and double metal process. The six-inch process flow necessitated a completely new lithography module, modification of some other process modules, and the transfer of the rest onto the six-inch upgraded equipment set. Functional MOS devices and circuits, identical to those on four-inch substrates, were ultimately realized on six-inch substrates.

3 .1 Lithography Process Module

A new DUV lithography module was characterized and implemented based on Shipley's UV210 resist. All implant and etch steps were closely studied to determine the minimum resist thickness required at each masking layer (effective etch and implant blocks). A new 5X baseline mask set was generated for the ASML stepper, which included additional pre-alignment (PM) and reticle marks. The large exposure field (21mm X 21mm) offered by the new ASML stepper allowed for placement of four baseline (8.5 mm X 8.5 mm) mask layers onto one reticle. This considerably reduced the overall cost of the new mask set. The baseline chip and an example of four-layer combinational mask are shown in Appendix A. ASML jobs created by the staff accurately aligned all of our baseline mask layers with a proper shift and blade settings for the CMOS150 baseline run.

Shipley UV210 DUV resist was designed to address 0.35 um technology nodes and beyond, therefore, we had to relax the spin speed to maximize the thickness. Figures 2 and 3 exhibit spin speed and swing curve behavior of the UV210 resist.

Standard CMOS baseline process was set at 9050 Å (points A), more in compliance with the old baseline process for proper etch and implant blocking (clear energy shifted slightly for the repeat of the swing curve at higher thickness, current process, point A).

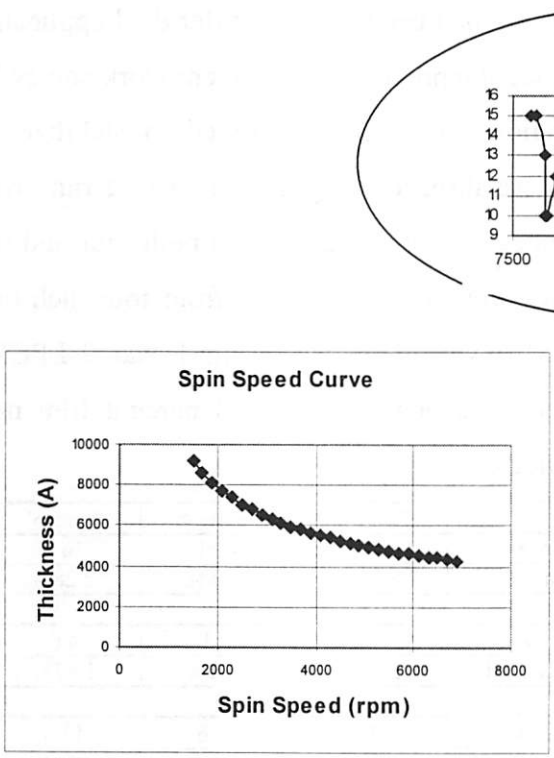


Figure 2 Spin speed curve (Shipley UV210)

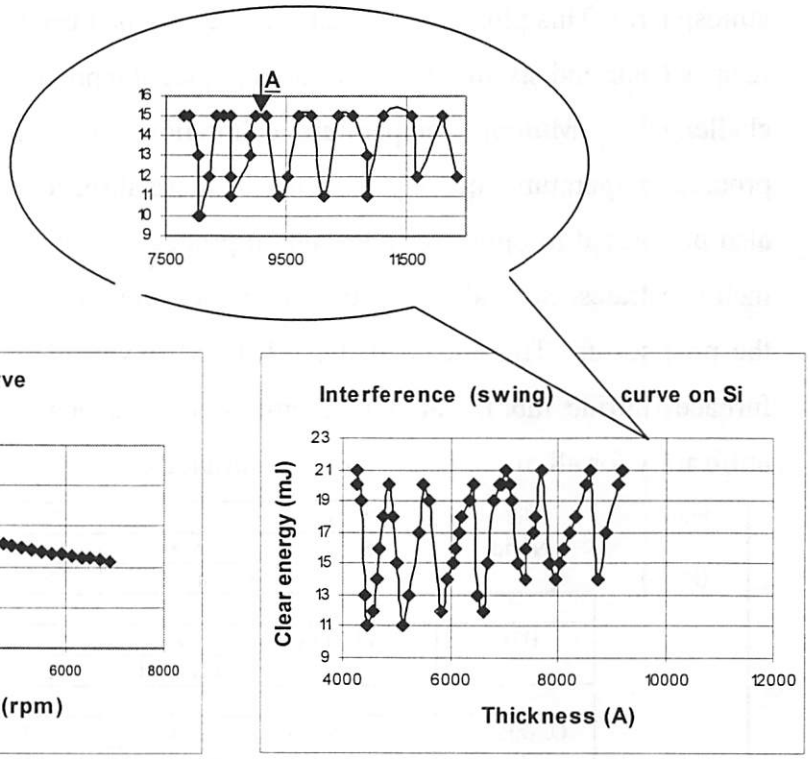


Figure 3 Swing curve (Shipley UV210)

Poly gates, as small as 0.4μm were printed and etched (proof of concept), however, the six-inch process was based on the 1.3 μm technology node, hence smaller transistors did not yield very well. SEM pictures of 0.5 μm resist and etched poly lines are shown in Figure 4, below (DUV lithography and Lam4 etch).

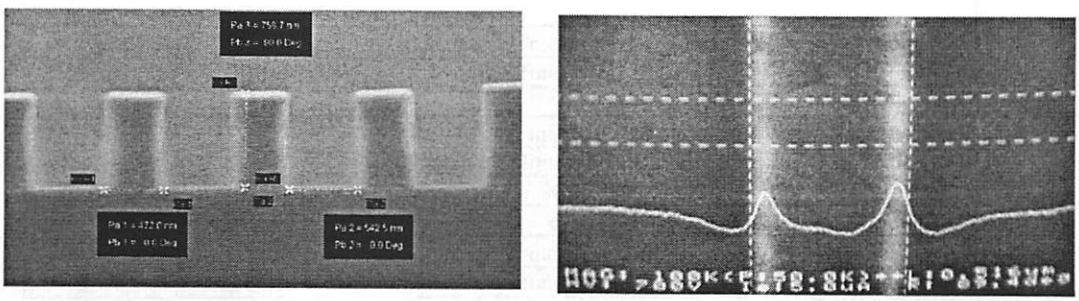


Figure 4 Cross section of a 0.5μm resist line (left); top view of 0.5μm poly gate (right)

3.2 Furnace Process Modules

The six-inch furnace tubes have 2.25 times the opening area than the four-inch tubes; hence, greater heat loss occurs at the wafer-loading step of the process (door open to atmosphere). This plus the fact that the decision had been made to offer dual application recipes (four and six-inch) at this station, made the process development work somewhat challenging. Multiple temperature calibration runs were performed to stabilize the process temperatures quickly for each of these furnaces. A great number of runs were also performed to optimize the standard processes that could cater to both four and six-inch substrates. Special application processes were also transferred from four-inch onto the new set up. This included the HTO and oxynitride processes in Tystar 9 LPCVD furnace (nitride tube). Table 1 summarizes the deposition rate and percent film non-uniformity for all of the bank3 LPCVD furnaces.

Furnace	Film	Recipe		Load 4"	Center 4"	Pump 6"
9 (MOS)	Nitride	9SNITA	A/min	45.4	42.1	36.6
			non-unif.	2.35%	0.95%	2.28%
	HTO	9VHTOA	A/min	4.3	4.4	4.6
			non-unif.	2.73%	1.91%	1.67%
	Oxynitride (2:1)	9OXYNITA	A/min	13.3	13.6	13.6
			non-unif.	1.26%	1.59%	2.21%
			RI (ave.)	1.722	1.742	1.735
10 (MOS)	Doped Poly	10SDPLYA	A/min	26.4	25.5	18.0
			non-unif.	2.22%	3.33%	5.03%
			ohm-cm	7.65E-04	8.79E-04	7.84E-04
	Undoped Poly	10SUPLYA	A/min	88.3	84.1	86.0
			non-unif.	1.02%	0.73%	3.78%
11 (MOS)	Doped LTO (PSG)	11SDLTOA	A/min	167.9	157.6	115.5
			non-unif.	3.28%	1.93%	1.28%
			P%	5.27	5.09	5.59
	Undoped LTO	11SULOTA	A/min	149.0	149.7	103.0
			non-unif.	4.41%	1.48%	1.25%
12 (MEMS)	Doped LTO (PSG)	12SDLTOA	A/min	143.5	137.3	
			non-unif.	6.72%	5.06%	
			P%	4.43	4.44	
	Undoped LTO	12SULOTA	A/min	154.7	141.5	
			non-unif.	9.39%	8.95%	

Table 1 - Test Monitor Data for Standard Nitride, Poly and LTO processes in Bank3

3.3 Etch Process Modules

The ASML stepper uses a special diffraction grating (8 and 8.8 μm wide trenches about 1200A deep) to align accurately all of the mask layers in a particular run. These marks are often referred to as "pre-alignment marks" (PM marks) or "Zero marks", and are printed and etched into the substrate at initial stages of the process. A special recipe "zero etch recipe" was developed that could accomplish this task on the lam4 etcher. Two PM marks and 4 back ups were etched into all wafers of the CMOS150 run. This run also required six-inch oxide, nitride/poly, and metal etch recipes on lam2, lam4 and lam3 respectively.

3.2.1 Zero layer (PM marks) recipe (lam4)

A new Lam4 recipe (6000) was developed based on Cl_2 chemistry to accurately etch pre-alignment marks into the CMOS150 initial substrates (ASML specification, trench depth =1200A $\pm$ 120). A 30 second etch resulted in 1200A deep trenches required by the ASML alignment system.
Zero etch recipe: 425mt/200W/0.8cm/200Cl2/400He

3.2.1 Oxide etch recipe

The initial trials with six-inch oxide test wafers in lam2 exhibited severe etch non-uniformity. Upon further inspection, we noticed considerable erosion in a four-inch area at the center of the upper graphite electrode. This was due to the fact that lam2 had been primarily used for four-inch wafers up until then. We decided to replace the top graphite electrode, before proceeding with more process characterization. Finally a simple design of experiment was set up to arrive at the best possible etch rate and etch non-uniformity. Process pressure, power and gap were varied to target a half micron per minute etch rate, and a reasonable percent of etch non-uniformity. Table 2 below shows the result of this experiment; the first run in this table provided a desirable etch rate and a reasonable percent non-uniformity for our selected oxide

etch process. This process recipe was used at contact etch for the six-inch CMOS150 run (4415A/min at less than 10% non-uniformity), which is noted in Table 3, below.

Run No.	RF Power (W)	Pressure (mTorr)	Gap (cm)	Etch Rate (A/min)	Non_uni (%)
1	**850**	**2.8**	**0.39**	**4415**	**9.6**
2	850	2.8	0.40	4043	12.2
3	850	2.8	0.50	1832	16.1
4	850	2.8	0.45	2947	26.6
5	950	2.8	0.5	1903	13.6
6	950	2.8	0.45	2955	26.0
7	850	3.2	0.5	1844	7.6
8	850	3.2	0.45	2106	16.1
9	950	3.2	0.5	1952	8.7
10	950	3.2	0.45	2198	14.5
11	900	3.2	0.4	3885	24.4
12	900	3.2	0.41	3400	28.1
13	800	3.2	0.4	3822	18.6
14	850	2.8	0.39	4928	18.8
15	850	2.8	0.40	4720	19.2
16	800	2.8	0.4	4576	21.2

Table 2 Experimental Matrix (oxide etch)

Recipe:	
2.8mt/850W/0.39cm/30CHF3/90CHF4/120He	Average Etch Rate: 4415 A/min Average Percent Non-Unif.: 9.60%

Table 3 Oxide Etch Recipe, Etch Rate and Uniformity Data for Oxide Layer on a Six-inch Substrate

3.2.2 Poly Gate Etch Recipe

A 3 factor, 2 level, half factorial experiment was designed to optimize the six-inch poly etch process on lam4. Three factors (power, pressure and total gas) were varied and two responses (etch rate and percent non-uniformity) were examined to arrive at

the optimum poly etch process recipe. Table 4 shows the details of the experimental matrix performed on lam4 etcher.

Run No.	RF Power (W)	Total Gas Flow (sccm)	Cl_2 Flow (sccm)	He Flow (sccm)	Pressure (mTorr)
1	275	580	180	400	425
2	275	640	200	440	375
3	325	580	180	400	375
4	**325**	**640**	**200**	**440**	**425**

Table 4. DOE Matrix (poly silicon)

Run Number 4 at high level of power, total gas, and pressure yielded the best results. Power was further increased to 330W, which then was selected as optimum process. This recipe was stored on lam4 disk (recipe 6440), as our standard six-inch poly etch recipe. Table 5 shows the oxide breakthrough and poly etch steps of this recipe, which etched 4913 Å/min poly film (average) with very good etch uniformity, below 2%. The nitride recipe was also developed on the same tool, based on a different chemistry (SF6), noted in table 6.

Recipe (6440):		
400mt/200W/1cm/100SF6 (oxide breakthrough)	Average Etch Rate:	4913 A/min
425mt/330W/0.8cm/200Cl2/440He (poly etch step)	Average Percent Non-Unif.:	1.28%

Table 5 Poly Etch Recipe (6440), Etch Rate and Uniformity for Polysilicon Layer on a Six-inch Substrate

Recipe (200):		
200mT/125W/0.9cm/150SF6/100He (nitride etch)	Average Etch Rate:	1200 A/min

Table 6 Nitride Etch Recipe (200), Etch Rate for Nitride Layer on a Six-inch Substrate

3.2.3 Metal etch process (lam3)

The metal etch process was not changed. Standard recipe yielded well for both four and six–inch substrates.

Recipe (standard): 250mT/250W/50BCl3/50N2/30Cl2/30CHCl3 (aluminum etch)	Average Etch Rate: 7000 A/min

Table 7 Metal Etch Recipe, Etch Rate for Aluminum Layer on a Six-inch Substrate

3.3 Process Monitoring

Process monitors are regularly performed on baseline equipment to track their performance and make sure they are running within specifications. Table 8 below, lists baseline equipment that currently are being monitored, as well as the frequency of the test and specification limits for each equipment. The latest test monitor data and the trend chart of each equipment can be seen at,

www.microlab.berkeley.edu/processmonitoring

Equipment		Monitoring		
Name	**Process**	**Parameters**	**Limits**	**Frequency**
tystar1	Gate Oxidation	Thickness Non-Uniformity	Within Wafer<10 %	1/month
			Wafer to Wafer<20%	
		IQF	<2.0	
tystar2	Dry/Wet Oxidation	Thickness Non-Uniformity	Within Wafer<10%	1/month
			Wafer to Wafer<20%	
		IQF	<2.0	
tystar5	Gate Oxidation	Thickness Non-Uniformity	Within Wafer<10%	1/month
			Wafer to Wafer<20%	
		IQF	<2.0	
tystar6	Gate Oxidation	Thickness Non-Uniformity	Within Wafer<10%	1/month
			Wafer to Wafer<20%	
		IQF	<2.0	
tystar9	LPCVD Nitride	Deposition Rate	50 A/min +/- 10%	1/month
		Thickness Non-Uniformity	Within Wafer <5%	
			Wafer to Wafer <20%	

tystar10	LPCVD Poly-Silicon	Deposition Rate	28 A/min +/- 15%	1/month
		Thickness Non-Uniformity	Within Wafer <10%	
			Wafer to Wafer <35%	
		Resistivity	12 Ohms/sq. +/- 25%	1/6 months
tystar11	LPCVD Phospho-Silicate Glass	Deposition Rate	180 A/min +/- 5%	1/month
		Thickness Non-Uniformity	Within Wafer <10%	
			Wafer to Wafer <30%	
		Dopant Concentration	6% - 7%	1/4 months
tystar12	LPCVD Phospho-Silicate Glass	Deposition Rate	130 A/min +/- 5%	1/month
		Thickness Non-Uniformity	Within Wafer <5%	
			Wafer to Wafer <10%	
		Dopant Concentration	5% - 6%	1/4 months
tylan16	LPCVD Poly-Silicon	Deposition Rate	80 A/min +/- 10%	1/month
		Thickness Non-Uniformity	Within Wafer <5%	
			Wafer to Wafer <20%	
tylan18	LPCVD Low-Stress Nitride	Deposition Rate	40 A/min +/- 10%	1/month
		Thickness Non-Uniformity	Within Wafer <15%	
			Wafer to Wafer <25%	
		Film Stress	300 +/- 50 MPa	
CPA	Sputtered Alumnium	Deposition Constant	80 nm*(cm/min)	1/2 months
		Reflectivity vs. bare Si	200%	
svgcoat1,2	I-Line Photoresist	Thickness Uniformity	Within Wafer <5%	1/2 weeks
			Wafer to Wafer <5%	
	G-Line Photoresist	Thickness Uniformity	Within Wafer <5%	1/2 weeks
			Wafer to Wafer <5%	
svgcoat6	DUV Photoresist	Thickness Uniformity	Within Wafer <5%	1/2 weeks
			Wafer to Wafer <5%	
ASML	DUV Resist Exposure	Clear Energy(E_o)	15 mJ/cm^2 +/- 15%	1/2 weeks
lam1	Nitride Plasma Etching	Etch Rate	1000 A/min +/- 10%	1/month
		Etch Rate Non-Uniformity	Within Wafer <10%	
			Wafer to Wafer <10%	
lam2	Oxide Plasma Etching	Etch Rate	5800 A/min +/- 10%	1/month
		Etch Rate Non-Uniformity	Within Wafer <20%	
			Wafer to Wafer <20%	
lam3	Aluminium Plasma Etching	Etch Rate	5000 A/min +/- 10%	1/3 months
lam5	Polysilicon Plasma Etching	Etch Rate	5000 A/min +/- 10%	1/month
		Etch Rate Non-Uniformity	Within Wafer <5%	
			Wafer to Wafer <5%	

Table 8 Process Monitoring Spec. Limits

4. CMOS Fabrication Process

The fabrication sequence for the first six-inch run (CMOS150) was based on our four-inch 1.3 μm twin-well CMOS technology. This means that our latest four-inch process was transferred over the 6-inch platform. P-type wafers at 20-40 Ω-cm resistivity, 675 μm thickness with <100> orientation were used for this run. N- and P- channel MOSFET devices and some simple circuitries were fabricated on these wafers. LOCOS isolation was used to define the active region of the transistors. A doped polysilicon (phosphorous doped) layer at thickness of about 2500 Å was deposited on 200 Å of gate oxide for both n and p type devices. Since single type polysilicon was used for both devices, P-type (boron) implant step was necessary to adjust the p-channel threshold voltages (Vt<-1 Volt). This made the PMOS device, a buried channel (compensated) type device. This run also used an additional metal layer as compared to previous process, which was facilitated by the CMP module. Triple metal process was needed to connect the additional test structures that were incorporated into the new six-inch mask layout.

This CMOS baseline process uses 8 implantation and 16 lithography steps. Table 9 and Table 10 list the implant and mask steps for this run. The baseline process and device parameter targets are shown in Table 13 at the end of this report. The schematic of the device cross section at various steps are shown in Figures 5(a)-(c). All process steps were completed in the Microlab facility, except for ion implantations. Implant process steps were performed by Ion Implant Services (Sunnyvale, CA), and later Core Systems (Sunnyvale, CA). Appendix B shows the six-inch process flow, which includes a detailed list of all the equipment used for the fabrication of CMOS150.

4.1 Test Chip

Appendix A shows the general layout of the test chip used for CMOS150. The scribe lane portion of the old layout (four-inch) was kept the same, but the drop-in area was modified to include: an 8-bit adder, a shift register, a 31 stage ring oscillator, a set of horizontally shrunk transistors down to 0.4 μm gate length, elbow patterns (down to 0.2 micron), alignment marks and verniers, and contact holes (for electrical test).

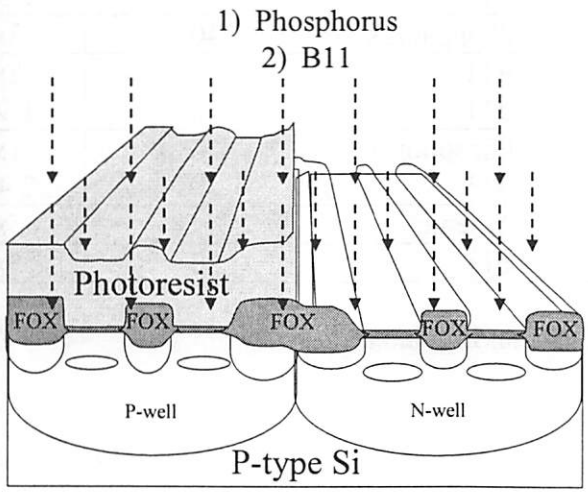
Process Step	Species	Energy (KeV)	Dose (cm^{-2})
N-Well Implant	Phosphorus	80	$4x10^{12}$
P-Well Implant	B11	80	$3x10^{12}$
P-Well Field Implant	B11	70	$1.5x10^{13}$
N-Well Field Implant	Phosphorus	40	$3x10^{12}$
N-Channel Punchthrough and Threshold Adjustment Implant	B11 B11	120 30	$8x10^{11}$ $1.9x10^{12}$
P-Channel Punchthrough and Threshold Adjustment Implant	Phosphorus B11	190 20	$1x10^{12}$ $2.4x10^{12}$
N+ S/D Implant	Arsenic	100	$5x10^{15}$
P+ S/D Implant	B11	20	$5x10^{15}$

Table 9. Ion Implantations

Lithography Step	Mask Name	Type	Field
Zero Layer Photo	PM Marks	Chrome	dark
N-well Formation	NWELL	Chrome	dark
Active Area Definition	ACTIVE	Chrome	clear
P-Well Field Implant Photo	PFIELD (inv. of NWELL)	Chrome	clear
N-Well Field Implant Photo	NWELL	Chrome	dark
N-Channel Punch-through and Threshold Adjustment Photo	PFIELD (inv. of NWELL)	Chrome	clear
P-Channel Punch-through and Threshold Adjustment Photo	PVT	Chrome	dark
Gate Definition	POLY	Chrome	clear
N+ S/D Photo	N+ S/D	Chrome	dark
P+ S/D Photo	P+ S/D	Chrome	clear
Contact Photo	CONT	Chrome	dark
Metal Photo	METAL1	Chrome	clear
VIA Photo	VIA	Chrome	dark
Metal2 Photo	METAL2	Chrome	clear
VIA2 Photo	VIA2	Chrome	dark
Metal3 Photo	Metal3	Chrome	clear

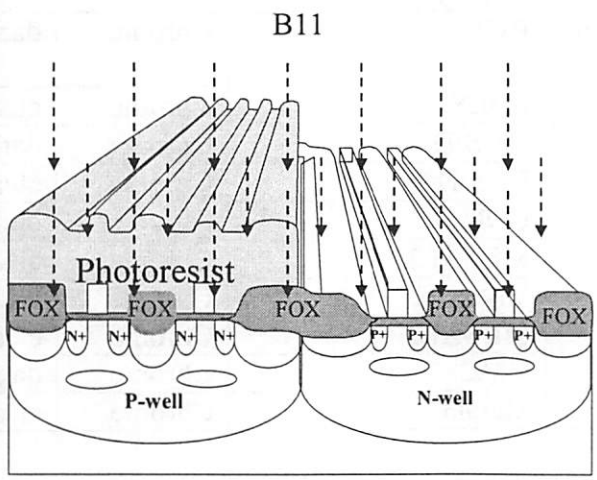
Table 10. Lithography Steps and Mask Identification

Fig. 5(a) LOCOS and Channel Implants



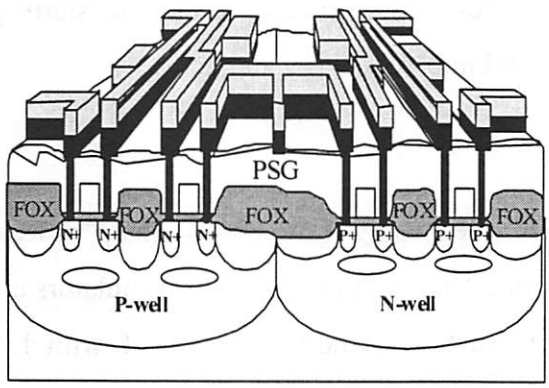
15. N-Well Field Implant Photo
16. N-Well Field Ion Implant: Phosphorus, 40 KeV, $3x10^{12}/cm^2$
17. Locos Oxidation: 650nm
18. Nitride Removal and (Thin Oxide Removal)
19. Sacrificial Oxide: 20nm
20. P-Field Photo
21. N-Channel Punch-through: B11, 120KeV, $8x10^{11}/cm^2$ and Threshold Adjustment Implant: B11, 30 KeV, $1.9x10^{12}/cm^2$
22. N-Field Photo
23. P-Channel Punch-through: Phosphorus, 190 KeV, $1x10^{12}/cm^2$ and Threshold Adjustment Implant: B11, 20 KeV, $2.4x10^{12}/cm^2$

Fig. 5(b) Gate Formation



24. Gate Oxidation and Poly-Si Deposition
25. Gate Poly Photo
26. Gate Poly Etch
27. Capacitor Oxidation
28. Capacitor Poly Deposition
29. Capacitor Photo/ Etch
30. N+ S/D Photo
31. N+ S/D Implant
32. N+ S/D Anneal
33. P+ S/D Photo
34. P+ S/D Implant

Fig. 5(c) Contact and Metallization



35. PSG Deposition & Post Densification
36. Contact Mask
37. Contact Etch
37. Metallization
38. Back Side Etch
39. Metallization (6000A)
40. Metal Mask
41. Al Etch
42. Sintering
43. Testing

4.2 Run Schedules

The first six-inch run, CMOS150 was started in July 2001, and completed in 2002. This run was parked on various occasions waiting for particular tool to be upgraded to six-inch or a new one to be installed. This also included problem solving steps and development activities needed to ensure a reliable process at that module. Some of the delays were caused by Sink7 (six-inch wet etch) installation, lam2 (oxide etcher) and lam3 (Aluminum etcher) upgrades. Implant steps also greatly delayed the schedule, as it took about a week to complete an implant step at an outside service company.

5. Process Simulation (TSUPREM4), Device Simulation (MEDICI)

We used Tsuprem4 [8] and Medici [9] simulation packages on the old four-inch process. The goal was to establish a baseline knowledge, and an additional gauge to compare the electrical/analytical test results of the newly fabricated six-inch run with the data obtained from the previous four-inch runs, if necessary. A simulation model can be used to evaluate the impact of certain factors on device performance to include: starting material, thermal budget, polysilicon thickness, and implant energy and dose.

Tsuprem4 process simulation

Two-dimensional simulation was performed using Tsuprem4 (silicon processing) and Medici (semiconductor device) programs. The input files for both simulators are attached in Appendix C. An N-channel device structure is shown in Figure 6 with 1.3 μm poly gate length.

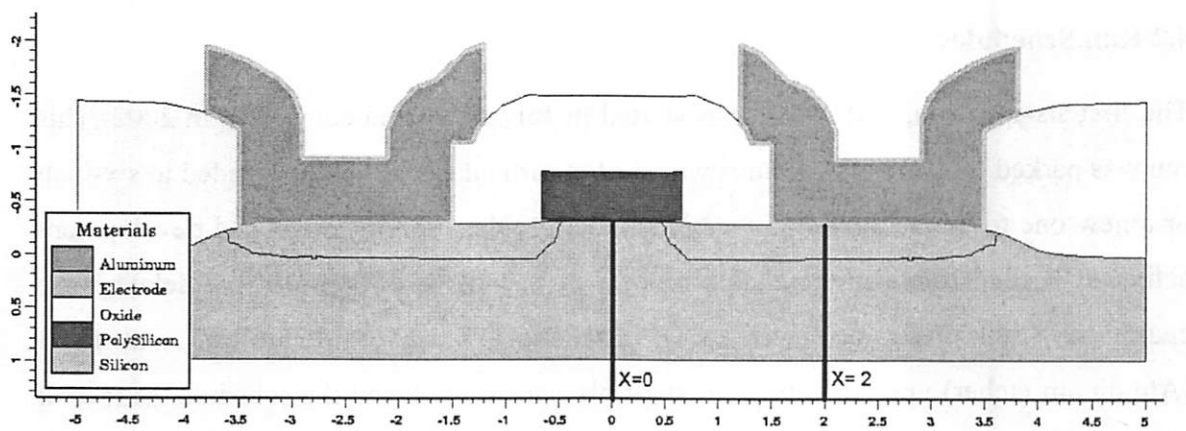


Figure 6 NMOS structure (Tsuprem4)

The four-inch layout design adopted by the new six-inch process used large contact holes (2X2 μm). The old design also used large contact to poly gate spacing. Minimum overlap of active/poly on contact followed the artifact of the old equipment limitation in the lab. The 6-inch equipment set could have addressed a more advanced technology node, however the goal was to the transfer the latest four-inch process over the new platform as an integral part of the six-inch upgrade project.

Two cuts were made on both NMOS and PMOS structures at position X=0 μm and X=2 μm. The doping profiles under the gate oxide for both NMOS and PMOS devices are shown in Figure 7(a) & Figure 8(a) at position X=0 μm, respectively. Similarly, doping profile under the source-drain region of an NMOS and PMOS devices are shown in Figure 7(b) and 8(b) at position X=2 μm. These results were compared to Spreading Resistance Analysis data obtained on the latest four-inch run [4] and the first six-inch baseline wafers (section 7.1).

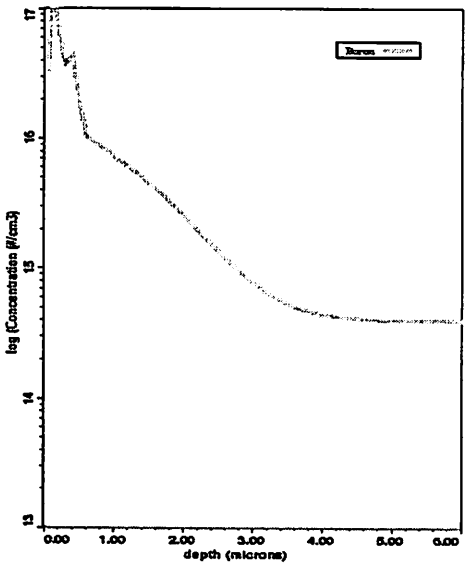


Fig. 7(a) N-channel doping profile under gate oxide

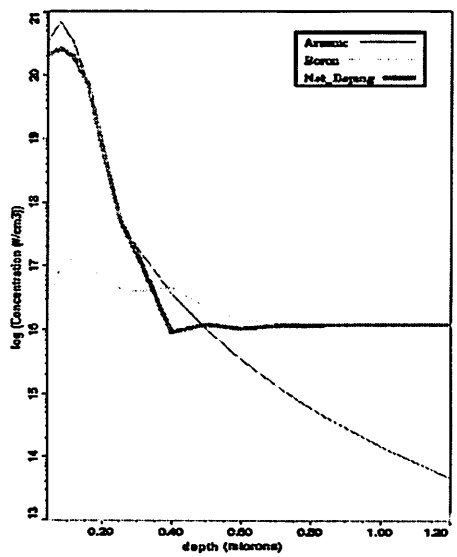


Fig. 7(b) N-channel doping profile under S/D area

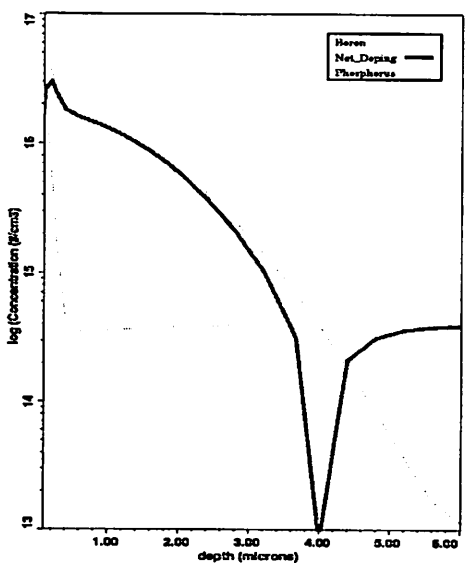


Fig. 8(a) P-channel doping profile under gate oxide

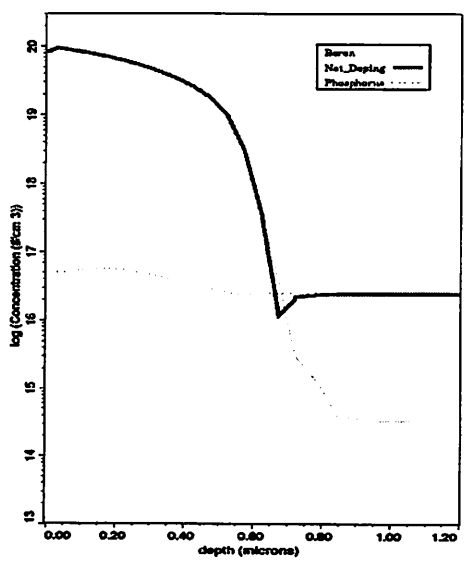


Fig. 8(b) P-channel doping profile under S/D area

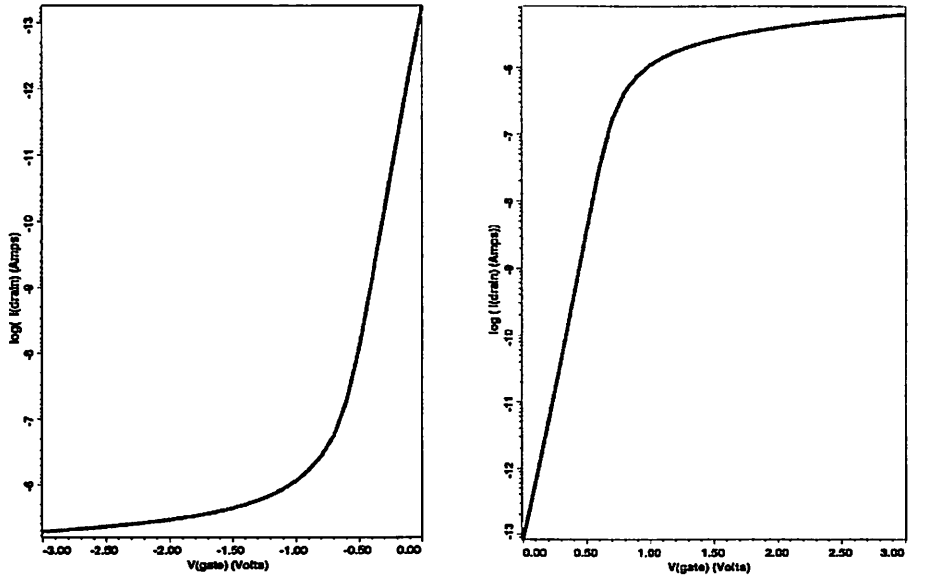
The well junction depth and source-drain junction depths in both cases looked deeper in the simulation than the SRA data. Simulation was closer to the SRA results when damage was ignored.

Medici device simulation

The output generated by Tsuprem4 was entered into Medici to predict the basic electrical characteristics of the N/P-channel devices (Fig.9). By using the *extract* statement the following device parameters were projected by the simulation (Table 11).

Parameters	N-Channel	P-Channel
Vt (V)	0.67	-0.69
Leff (μm)	1.01	0.6
Sub-threshold slope (mV/dec.)	102	94

Table 11 Extracted Parameters on Simulated 1.3 μm Devices



p-MOSFET n-MOSFET

Fig. 9 Simulated subthreshold I-V characteristics

6. SPICE model parameter extraction by using Windows version of BSIMPro

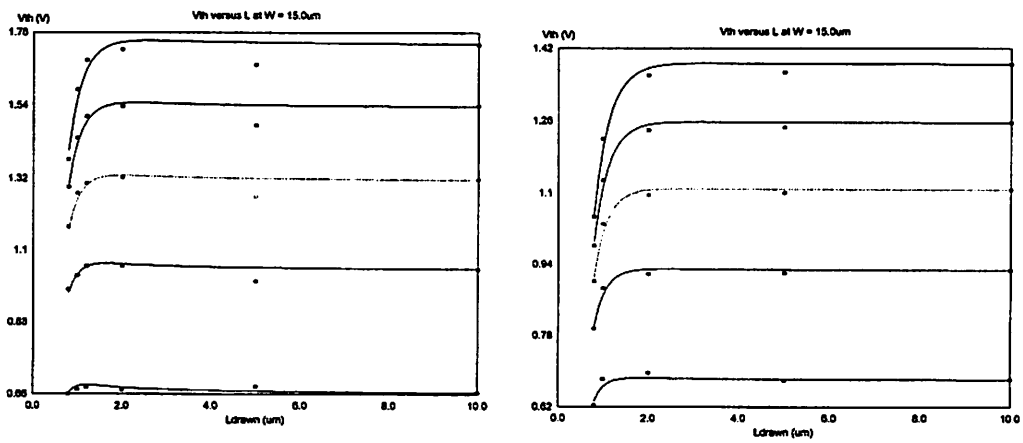
These results came from the latest four-inch process CMOS61. I-V data were measured on an Electroglass 2001 (autoprobe). See section 7.2 for more information about the measurement system.

Five devices were selected with different channel length (0.8, 1.0, 1.2, 5 and 10 μm) and width (10, 15 μm) to meet BSIMPro requirements [10]. Applied bias conditions for I-V measurements are displayed in Table 12, below.

I-V Data	Vgs	Vds	Vbs
Linear Ids-Vgs	$0 \leq Vgs \leq 5.0$, Vgs step = 0.1	Vds = 0.05	$Vbs \leq 0$, number of steps = 4
Saturation Ids-Vgs		Vds = 5.0	
Ids- Vds at Vbs=0.0	$2 \leq Vgs \leq 5.0$, Vgs step = 1	$0 \leq Vds \leq 5.0$, Vds step = 0.1	Vbs = 0.0

Table 12 I-V Data and Measurement Bias Conditions for NMOS
(for PMOS, the voltage polarity is reversed)

The measured I-V data from automatic probe station (EG 2001) were converted into BSIMPro data format. Extracted HSPICE parameter sets are presented in Appendix D. Dots represent the actual measurement, lines show the simulated characteristics in Figures 10-13.



(a) (b)

Fig. 10 Threshold voltage vs. channel length (drawn) with substrate bias
(a) 0 to –4 V for NMOS; (b) 0 to 4 V for PMOS

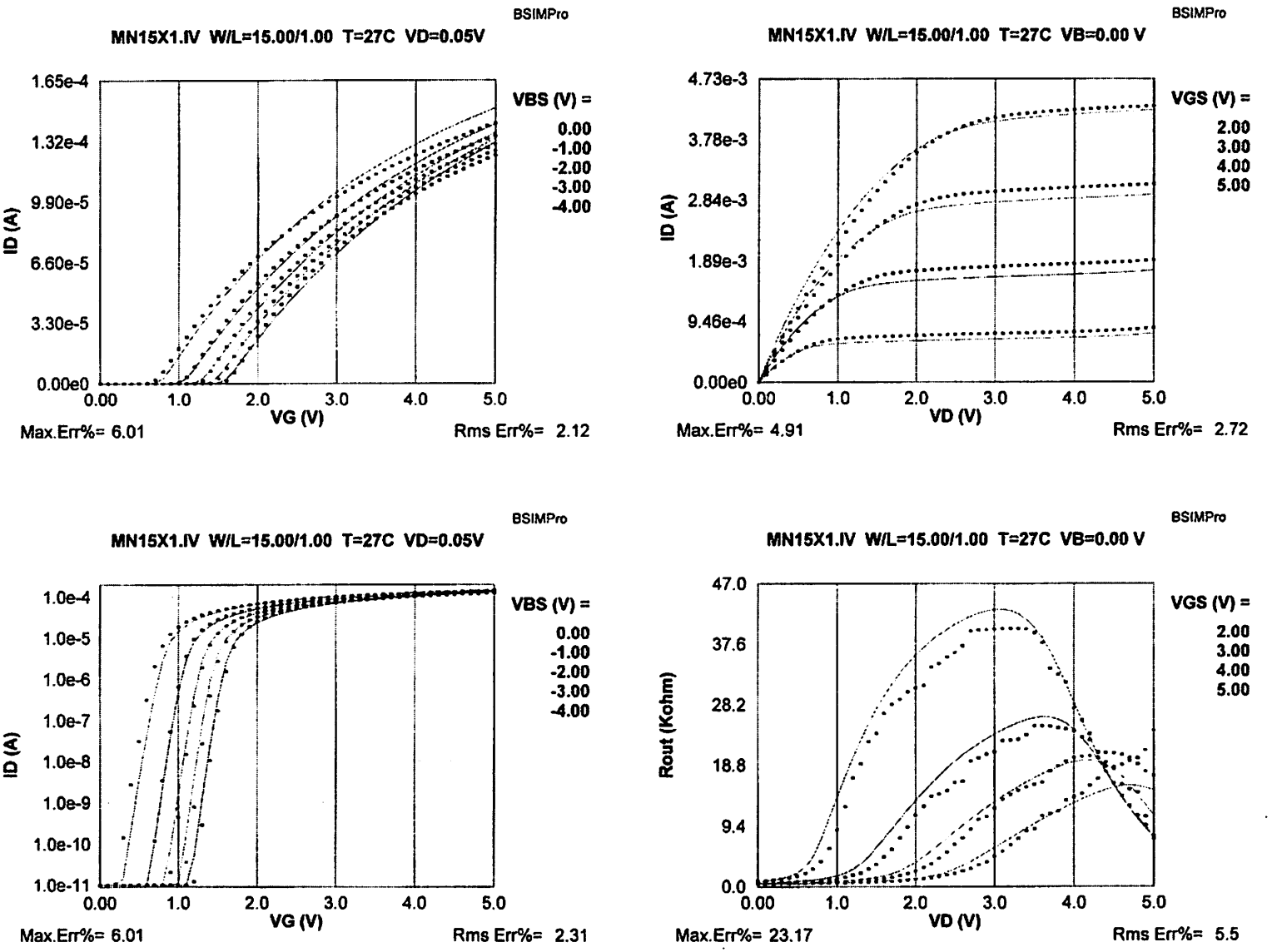


Fig. 11 I-V characteristics of an N- channel MOSFET (W/L=15/1), CMOS61, measured with autoprobe, simulated with BSIMPro

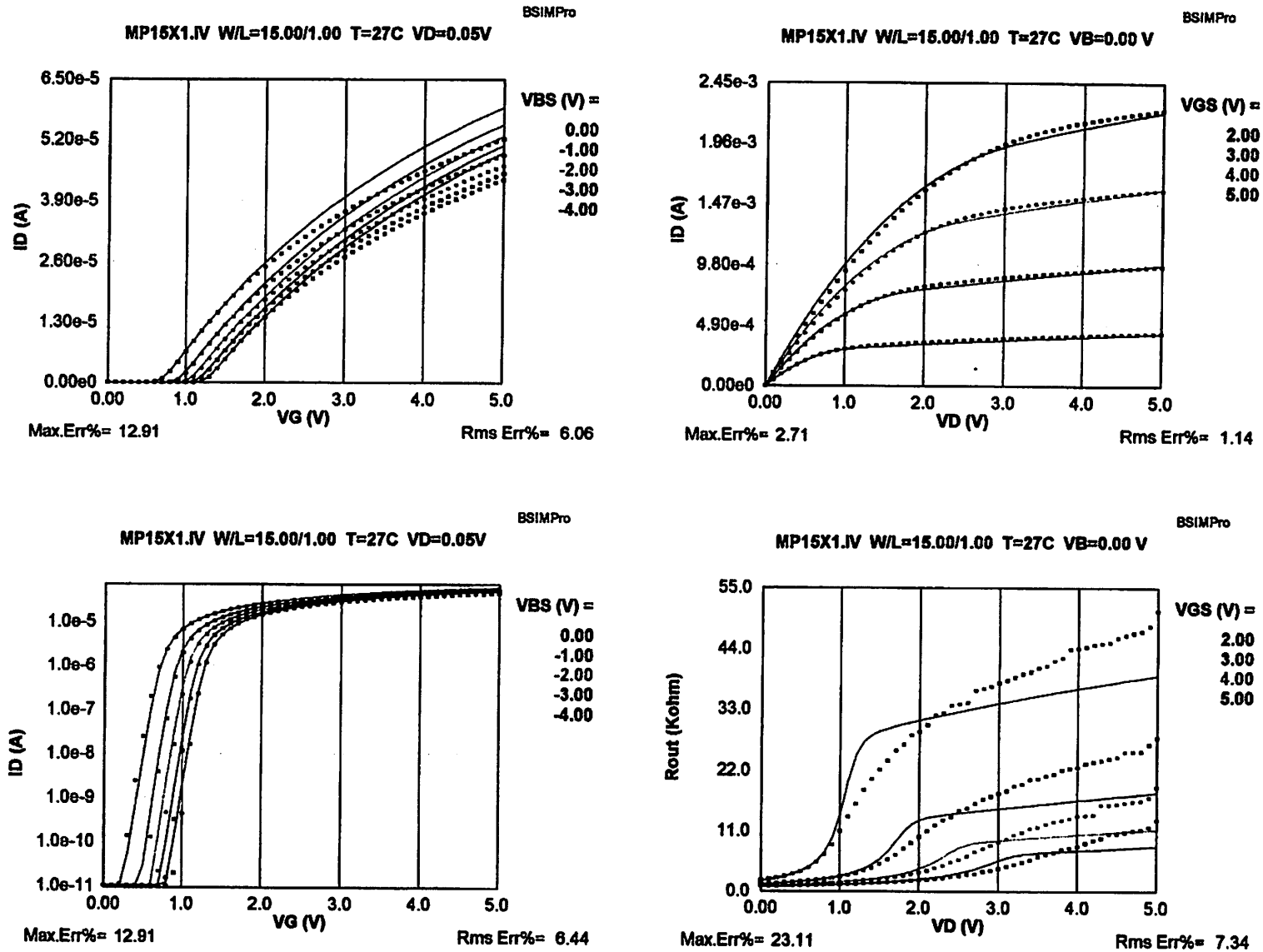
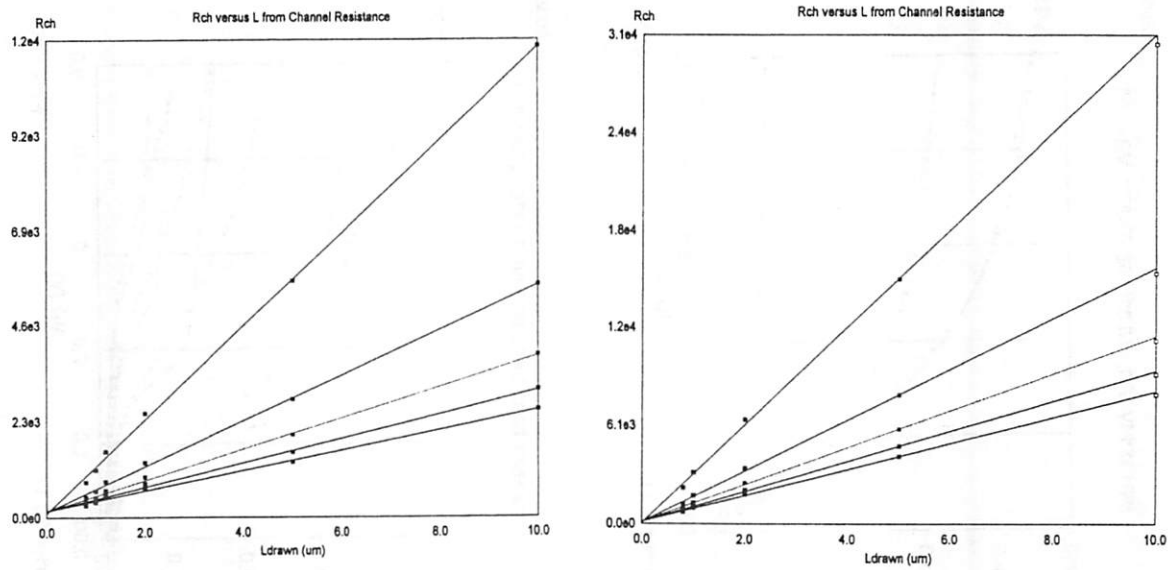
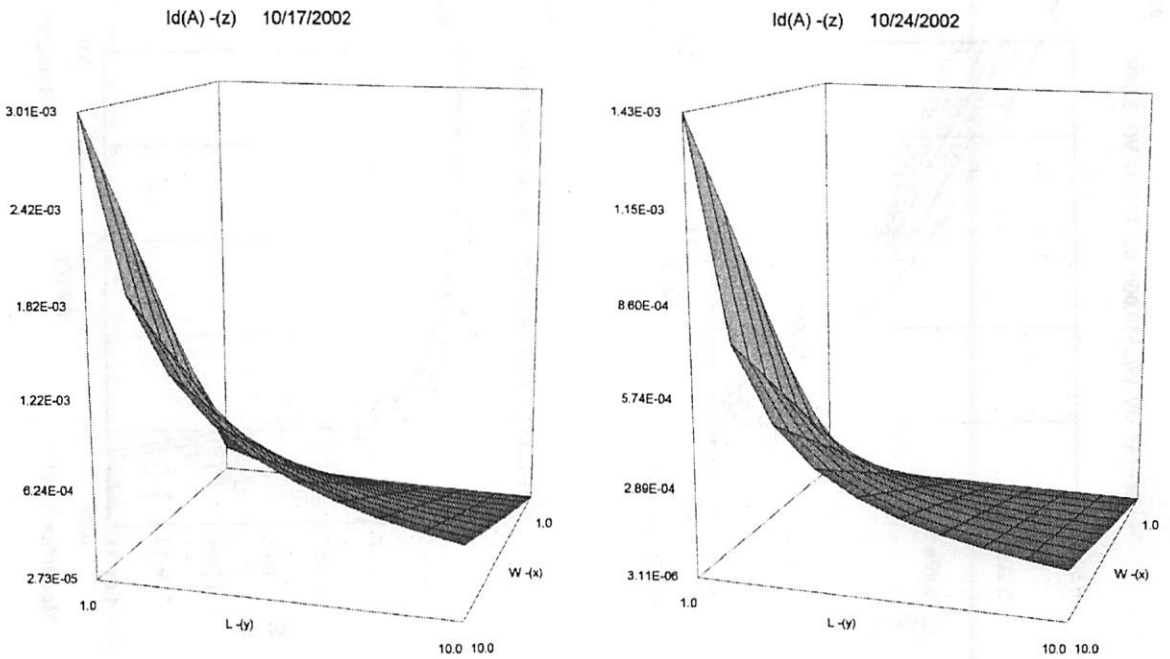


Fig. 12 I-V characteristics of a P- channel MOSFET (W/L=15/1), CMOS61, measured with autoprobe, simulated with BSIMPro



(a) NMOS (b) PMOS

Fig. 13 Effective channel length extraction



(a) NMOS (b) PMOS

Fig. 14 Drain current vs. gate length and width

7. Experimental Results of the Six-inch CMOS Baseline Process

7.1 Spreading Resistance Analysis (SRA)

The results of the Spreading Resistance Analysis (SRA) for CMOS150 run are shown in Fig. 15-16. The SRA was performed at Solecon Laboratories (Reno, NV).

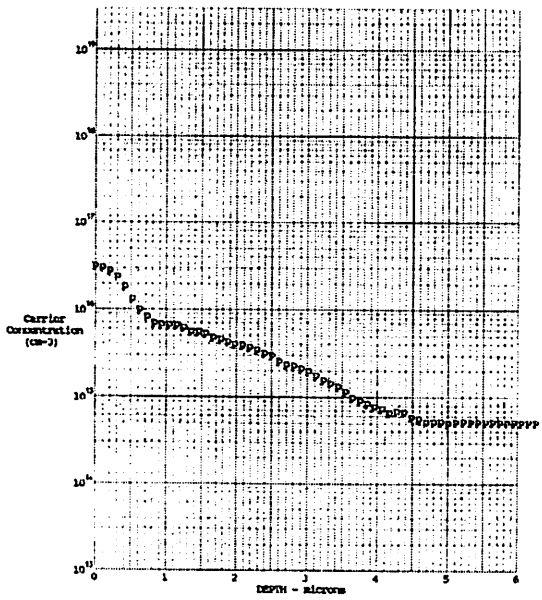


Fig. 15(a) N-channel doping profile under gate oxide

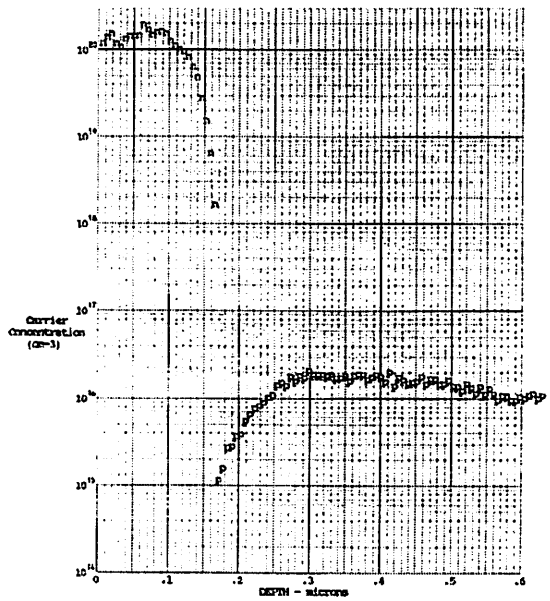


Fig. 15(b) N+ source-drain doping profile

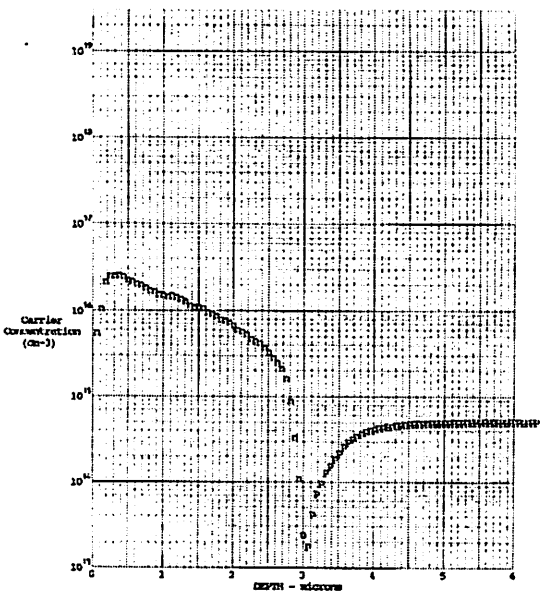


Fig. 16(a) P-channel doping profile under gate oxide

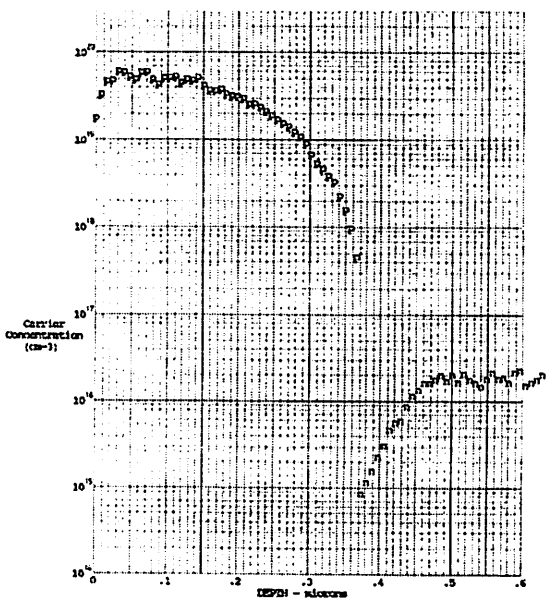


Fig. 16(b) P+ source-drain doping profile

7.2 Electrical Measurement Results from CMOS150 baseline process

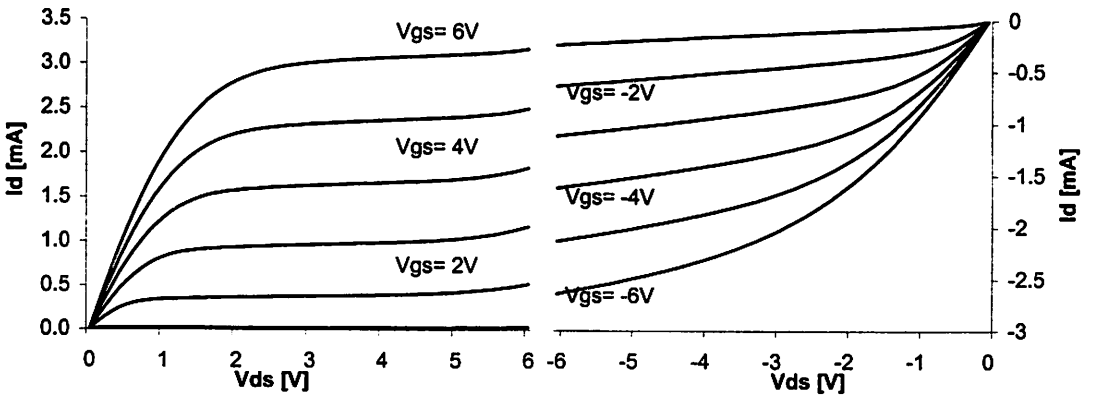
An automatic probe station (autoprober) was utilized to make electrical measurements on each wafer. The autoprober consists of an Electroglas probe station Model 2001X, an HP 4085A Switching Matrix, an HP4084 Switching Matrix Controller, an HP 4142 Source/Monitor and a UNIX workstation. The test structures are laid out such that the contact pads allow for 2x5 probe-card testing. New contact pads (2x15) were added to the six-inch test chip layout to make it possible to test an 8-bit adder on the test chip.

The autoprober enables the collection of large amounts of data for monitoring the process and for extracting device parameters. The source files for the in-house developed SUNBASE control software can be found at: ~eglas/src/sunbase/ on the Microlab's main file server (silicon). Sunbase3 is a modified version of the original SUNBASE program [7]. Sunbase3 has a new module (adder), which was developed to test an 8-bit adder by utilizing a 32-pin card.

The following subroutines (module names) have been used from the Sunbase program to display transistor characteristics and to extract transistor/process parameters (case sensitive):

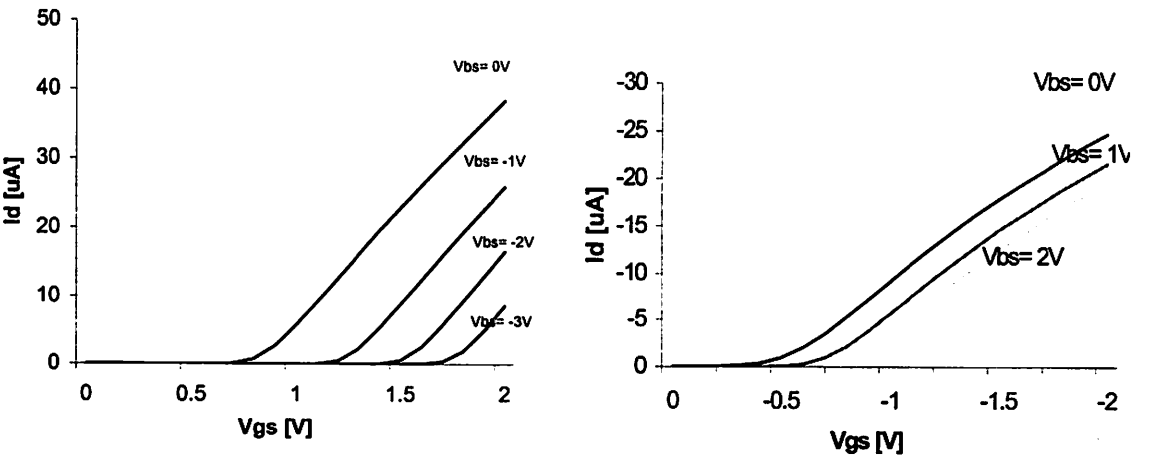
- IdVds – drain current vs. drain voltage measurement
- IdVg - drain current vs. gate voltage measurement
- VTWDLD – can be specified for extraction of the threshold voltage (Vt), delta width (ΔW), delta length (ΔL), body coefficient (gamma), and surface/substrate dopant concentration.
- SATTRANN, SATTRANP – K' (transconductance) in saturation
- SATCURN, SATCURP – saturation current
- DIBLN, DIBLP - subthreshold slope (S), S-D leakage
- EFFMOBN, EFFMOBP - effective mobility (μ_{eff}).
- SCBR - sheet resistance
- Conr - contact resistance

The following measurements were obtained using the autoprobe to display the I-V curves. NMOS and PMOS characteristics were obtained from CMOS150 process wafer#13. The features of the measured devices are W/L= 10/1.2 μm (drawn) in Figures 17-20.



(a) NMOS (b) PMOS

Fig. 17 NMOS and PMOS drain current vs. drain voltage characteristics



(a) NMOS (b) PMOS

Fig. 18 NMOS and PMOS drain current vs. gate voltage at varying substrate bias

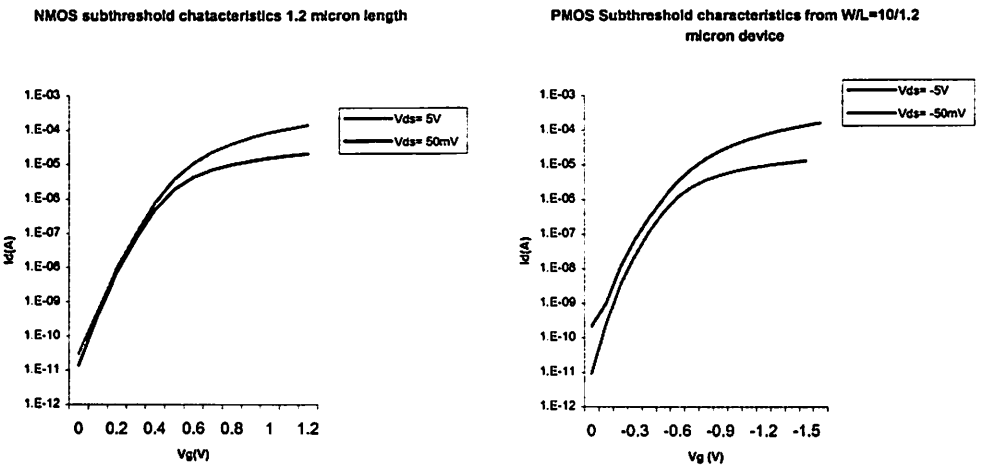
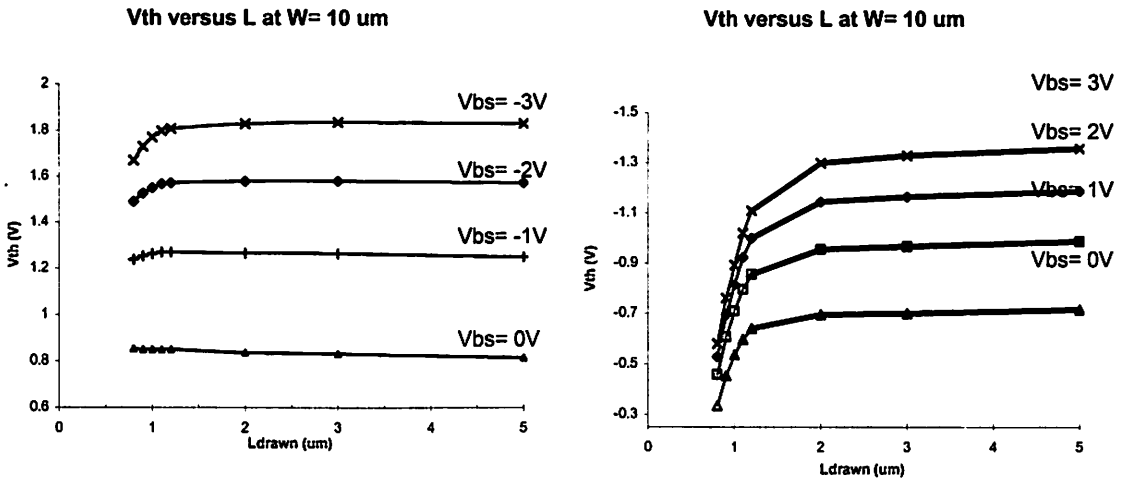


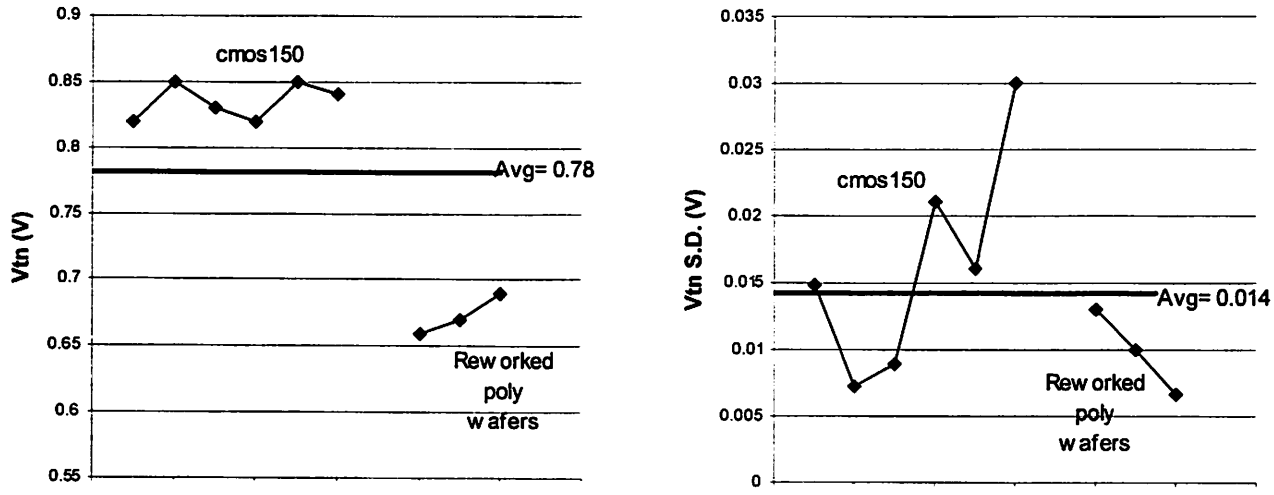
Fig. 19 NMOS and PMOS subthreshold characteristics

Measured threshold voltage versus gate length (drawn) on completed devices. P-channel transistors show a large decrease of the V_{th} for gate length less then 1.2 micron.



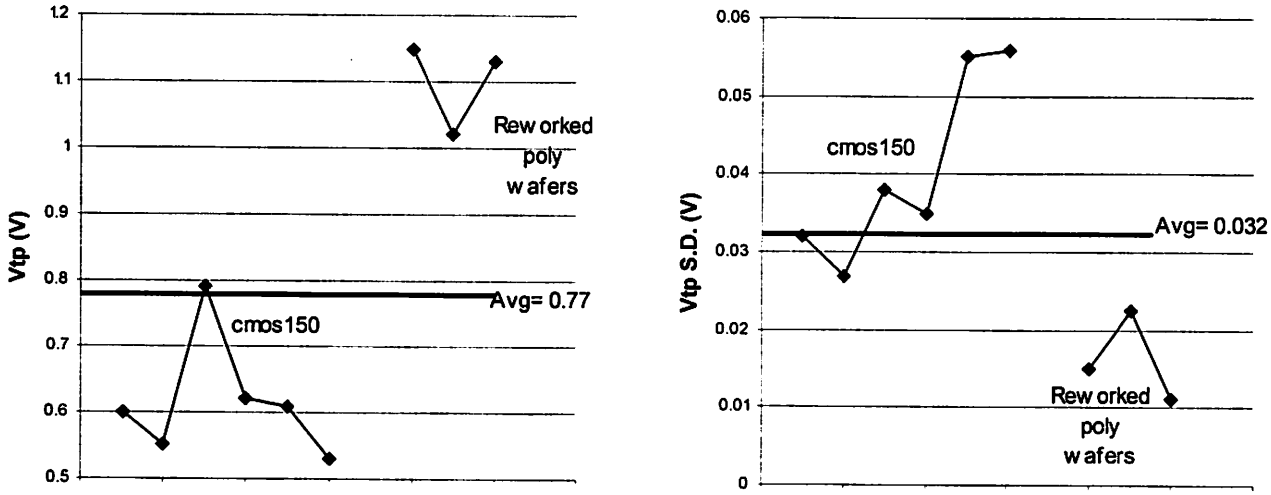
(a) n-channel transistor (b) p-channel transistor

Fig. 20 Threshold voltage roll-off vs. channel length (drawn)



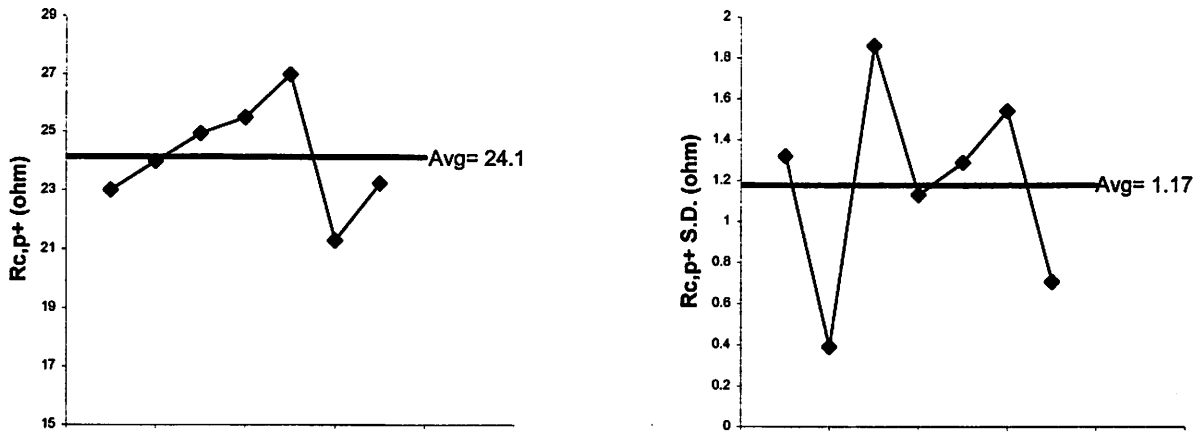
(a) (b)

Fig. 21 (a) NMOS threshold voltage distribution in CMOS150 process through the wafers. Each data point is the average of eighteen dies measured (device W/L of 10/1.2) across one wafer. (b) Standard deviation corresponding to data points in (a).



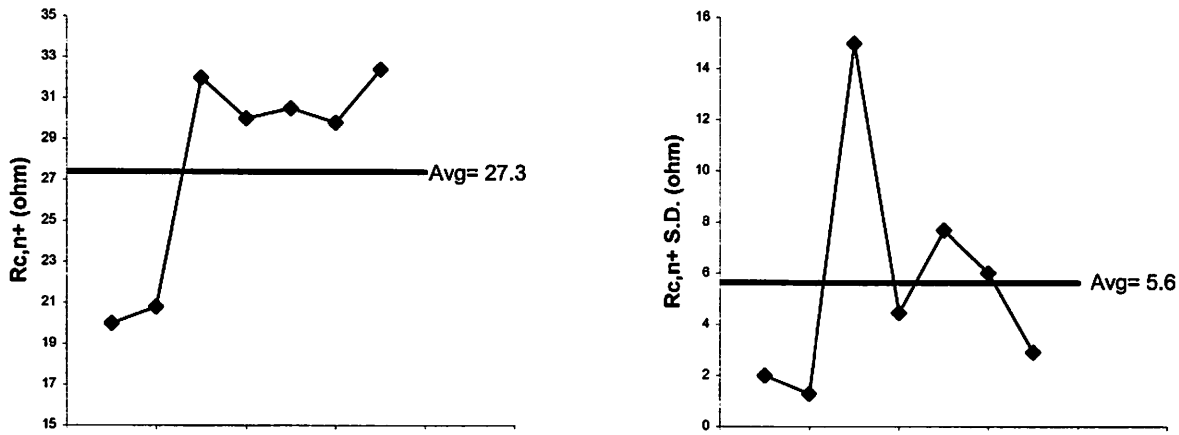
(a) (b)

Fig. 22 PMOS threshold voltage distribution in CMOS150 process through the wafers. Each data point is the average of eighteen dies measured (device W/L of 10/1.2) across one wafer. (b) Standard deviation corresponding to data points in (a).



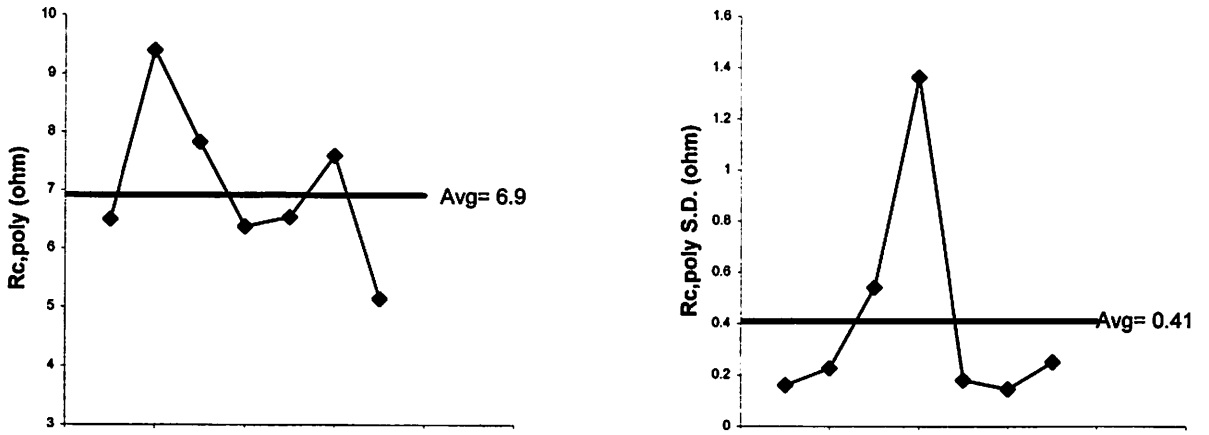
(a) (b)

Fig. 23 (a) Al-P+ contact resistance distribution in CMOS150 process through the wafers. Each data point is the average of fifteen dies measured across one wafer. (b) Standard deviation corresponding to data points in (a).



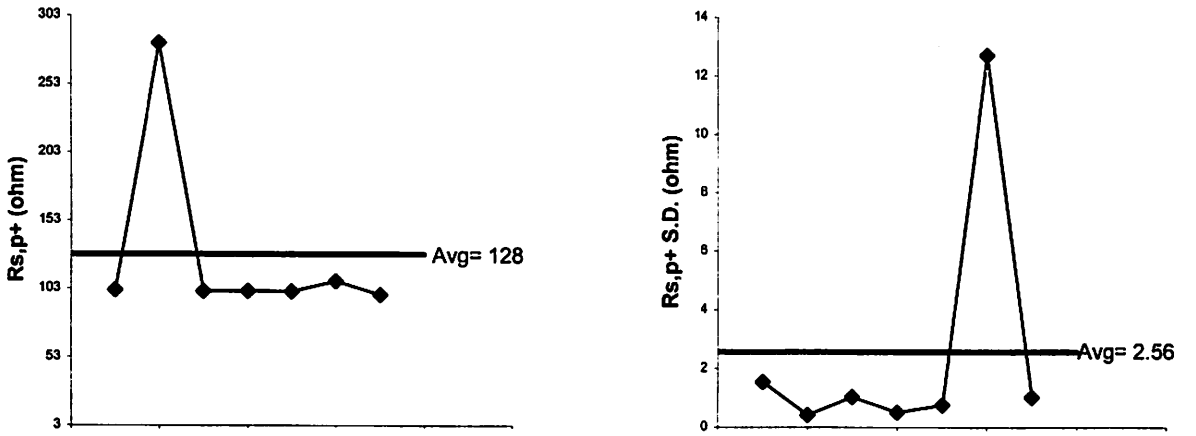
(a) (b)

Fig. 24 (a) Al-N+ contact resistance distribution in CMOS150 process through the wafers. Each data point is the average of fifteen dies measured across one wafer. (b) Standard deviation corresponding to data points in (a).



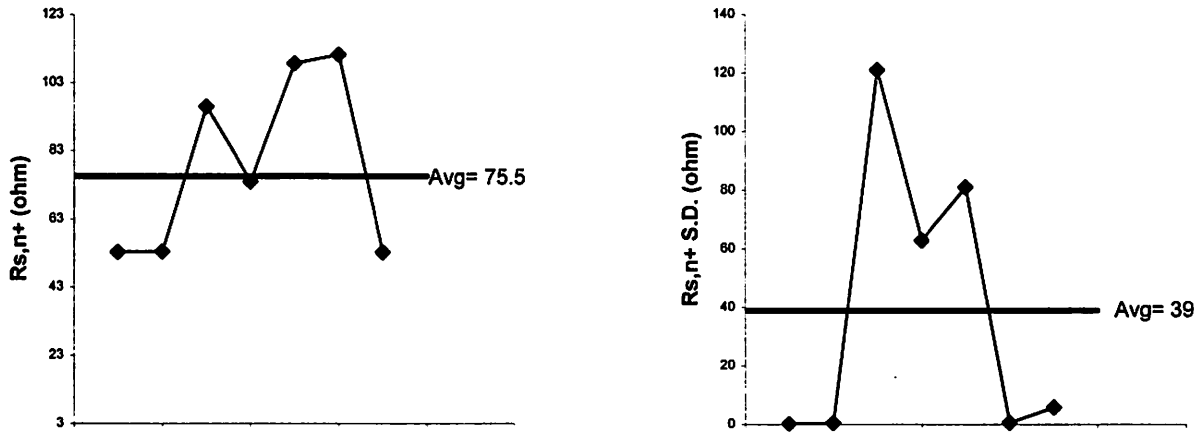
(a) (b)

Fig. 25 (a) Al-Poly contact resistance distribution in CMOS150 process through the wafers. Each data point is the average of fifteen dies measured across one wafer. (b) Standard deviation corresponding to data points in (a).



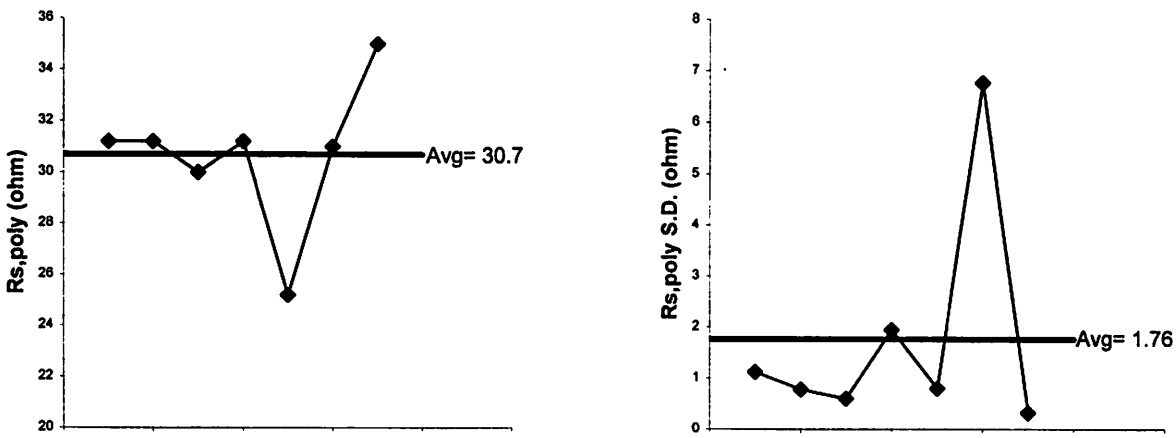
(a) (b)

Fig. 26 (a) P+ diffusion sheet resistance distribution in CMOS150 process through the wafers. Each data point is the average of fifteen dies measured across one wafer. (b) Standard deviation corresponding to data points in (a).



(a) (b)

Fig. 27 (a) N+ diffusion sheet resistance distribution in CMOS150 process through the wafers. Each data point is the average of fifteen dies measured across one wafer. (b) Standard deviation corresponding to data points in (a).



(a) (b)

Fig. 28 (a) Phosphorus doped poly sheet resistance distribution in CMOS150 process through the wafers. Each data point is the average of fifteen dies measured across one wafer. (b) Standard deviation corresponding to data points in (a).

7.3 Design Parameters

Table 13 shows the summary of the various measurements and testing results from the process designed to produce L=1.3 μm devices. Values shown in this table were extracted from measurements on L=1.2 μm devices.

Method and measurement conditions for parameters:

1. The threshold voltage was measured by the linear extrapolation method.

2. Subthreshold slope numbers came from Sunbase (DIBLE module).

3. K' were extracted from measurements, while the devices were in saturation.

4-5. Effective channel length and width were measured by autoprober, based on the resistance and conductance methods [11].

6-9. Surface dopant concentration numbers come from autoprober measurements, which matched the SRA results. Since the dopant concentration is not vertically uniform in the ion-implanted channel region, gamma1 and gamma2 were extracted at low and high substrate bias [12,13]. Based on these results, dopant concentrations at the surface and substrate were obtained.

10. Gate oxide thickness was measured by Nanospec during the process and also C-V measurement was applied on completed devices.

11-12. The well depth and the source-drain depth data came from the SRA graphs.

13-17. Parameters were measured on the automatic probe station using the electrical test structures described in Ref [7].

18-29. Measurements were taken by the Semiconductor Parameter Analyzer (HP 4145B).

20. Sunbase program (EFFMOB module).

No.	Parameters	Units	NMOS	PMOS
1.	$V_{threshold}$	V	0.78	-0.77
2.	Sub threshold Slope	mV/decade	97	103
3.	K'($\mu C_{ox}/2$)	$\mu A/V^2$	30	16
4.	delta L	μm	0.1	0.28
5.	delta W	μm	0.12	0.24
6.	γ_1 (low V_{SB})	$V^{1/2}$	0.87	-0.33
7.	γ_2 (high V_{SB})	$V^{1/2}$	0.67	-0.25
8.	Surface dopant concentration	$Atom/cm^3$	$3x10^{16}$	$3\text{-}4.3x10^{15}$
9.	Substrate dopant concentration	$Atom/cm^3$	$1.8x10^{16}$	$2\text{-}2.5x10^{15}$
10.	T_{ox}	Angstrom	200	200
11.	X_j (S-D)	μm	1.7	3.7
12.	X_w (Well depth)	μm	4.6	3
13.	R_{diff} (sheet resistance)	Ω/square	75.5	128
14.	R_{poly} (sheet resistance)	Ω/square	30.7	
15.	R_{well} (sheet resistance)	KΩ/square	0.45	1.45
16.	$R_{c\ M1\text{-}diff}$ (2μmx2μm)	Ω	27.3	24.1
17.	$R_{c\ M1\text{-}poly}$ (2μmx2μm)	Ω	6.9	
18.	S-D Breakdown	V	>7	>7
19.	S-D leakage (V_{ds}=5V, V_{gs}=0V)	pA/μm	0.33	20
20.	Eff. mobility (V_{bs}=0V, V_{gs}=1V)	cm^2/V-sec	242	156

Table 13 Process and Device Parameter Targets (from 10/1.2 device)

8. Future work

We are working on a new CMOS baseline process, which will better utilize our six-inch process capabilities. We hope to skip several technology generations by implementing a 0.35 μm CMOS baseline process in the Microlab. This will be a simplified version of such a process, as we are still lacking advanced oxide and metal etch capabilities. The new process will take advantage of DUV lithography, lightly doped drain (LDD) structure, salicidation, dual polygate and CMP planarization technique. In addition, we would like to incorporate shallow trench isolation (STI), if and when the etch capability arrives, and possibly address the 0.25 μm technology node in the upcoming years.

9. References

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Acknowledgments

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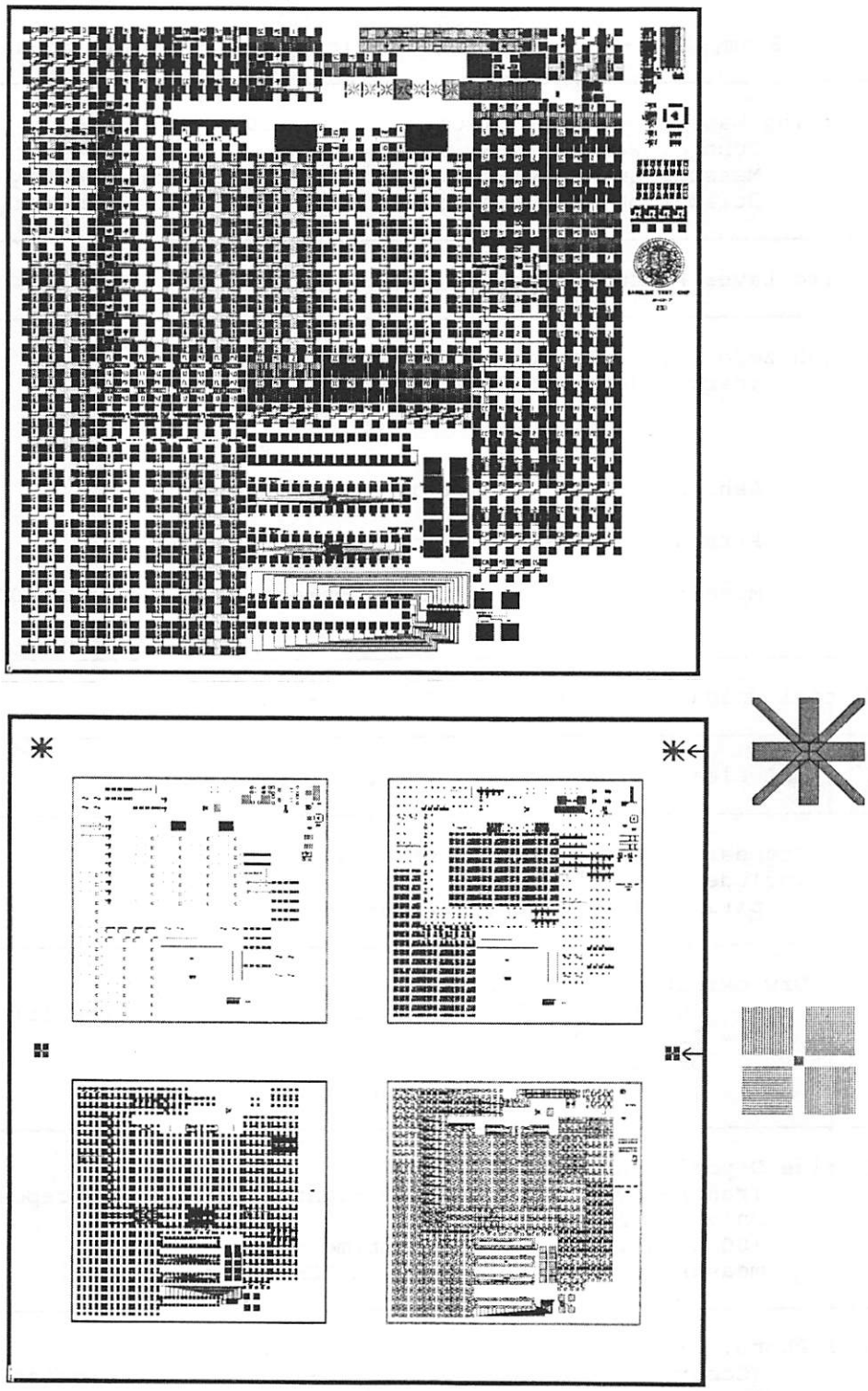
Biography

Siavash Parsa received the B.S. degree in electrical engineering and the M.S. degree in microelectronics, both from Arizona State University, Tempe, AZ. Shortly after finishing his graduate work in 1988, he began his career in Semiconductor industry. His last position held in industry was Senior Engineering Manager at Xicor, Inc. He has been with the University of California Berkeley Microlab for the past four years, managing the process engineering group.

Laszlo Voros received the M.S. degree in engineering physics in 1999 from the Technical University of Budapest, in Hungary. He spent 1999-2002 at UCB as an associate specialist in the Microfabrication Laboratory. His primary assignments were in baseline process support and development, device testing.

Appendix A



Modified baseline chip (top) and four mask layers on one ASML reticle, scaled by ¼ (bottom).

Appendix B

Microlab CMOS Process
Version 6.0 (2001)
1.3 um, twin-well, 150 mm, double poly-Si, double metal

0.0 Starting Wafers: 20-40 ohm-cm, p-type, <100>
Control wafers: PCH, NCH.
Measure bulk resistivity (ohms-cm) of each on sonogage.
Scribe lot and wafer number on each wafer, including controls.

1.0 Zero Layer Photo (PM marks: HMDS, coat, expose, PEB, hard bake)

2.0 Etch zero layer into the substrate in lam4.
(target depth=1200 A)

Ash photoresist in matrix.

Piranha clean and dip in sink9 (MEMS side).

Measure the depth of the alignment marks using as200.

1.0 Initial Oxidation: target = 30 (+/- 5%) nm

1.1 TCA clean furnace tube (tystar17), reserve tystar9.

1.2 Standard clean wafers in sink9 (MOS side):
Include PCH and NCH.
piranha 10 minutes, 10/1 HF dip, spin-dry.

1.3 Dry oxidation at 950 C (DRYOX.017):
60 min. dry O2 (Check the previous run result)
20 min. dry N2
Ox. time=
measure oxide thickness on PCH, Tox=

2.0 Nitride Deposition (9SNITA):
Transfer wafers to tystar9 right after 1.3 and deposit
Only include NCH.
100 nm nitride. Dep. time=
measure nitride thickness on NCH, Tnit=

3.0 Well Photo: Mask NWELL
(Control wafers are not included in any photoresist step)
Standard DUV lithography process
HMDS, spin (and soft bake) -> program 1,1 on svgcoat6
expose by ASML DUV stepper
post exposure bake, develop -> program 1,1 on svgdev6
inspect and UVbake (program: J)

4.0 Etch: Plasma etch nitride in lam4.
Recipe: 200 Power:125 W
Actual Etch Time:~ 50 sec. Overetch:
Check the oxide thickness on each work wafer:

5.0 N-Well Implant: phosphorus, 4E12/cm2, 80 KeV. Include PCH.

6.0 N-Well Cover Oxidation:

6.1 TCA clean furnace tube (tystar17).

6.2 Remove PR in O2 plasma and clean wafers in sink9 (MEMS side).

6.3 Standard clean wafers in sink9 (MOS), include PCH and NCH.

6.4 Well cover oxidation at 950 (WETOX.017):
30 min. dry O2
175 min. wet O2
30 min. dry O2
20 min. N2

7.0 Nitride Removal, include NCH

7.1 Dip in 10:1 BHF for 40 sec to remove thin oxide on top of Si3N4.

7.2 Etch nitride off in boiling phosphoric acid.
Measure Tox in n-well on work wafers.

8.0 P-Well Implant: B11, 3E12/cm2, 80 KeV. Include NCH

9.0 Well Drive-In:

9.1 TCA clean furnace tube (tystar17).

27.1 Standard clean wafers in sink9 (MEMS and MOS).
Include PCH and NCH.

9.3 Well drive at 1120 C (WELLDR.017):
60 min. temperature ramp from 750 C to 1120 C
240 min. dry O2
300 min. N2

Measure oxide thickness on two control wafers.
tox (PCH)= tox (NCH) =

9.4 Strip oxide in 5:1 BHF.
Measure Rs on PCH and NCH.
Rs (PCH) = Rs(NCH) =

10.0 Pad Oxidation/Nitride Deposition:
target = 30 (+6) nm SiO2 + 100 (+10) nm Si3N4

10.1 TCA clean furnace tube (tystar17). Reserve tystar9.

10.2 Standard clean wafers. Include PCH, NCH.

10.3 Dry oxidation at 950 C (DRYOX.017):
~1 hr. dry O2
30 minutes dry N2 anneal.
Measure the oxide thickness on NCH
Tox=

10.4 Deposit 100 (+10) nm of Si3N4 immediately (9SNITA):
Only include PCH.
approx.time = 30 min., temp.= 800 C.
Measure nitride thickness on PCH.
Tnit =

11.0 Active Area Photo: Mask ACTV
Standard DUV lithography process.
PR thickness should be more than 1.2 micron!

12.0 Nitride Etch:
Plasma etch nitride in lam4. Recipe: 200
Power:125 W Time:~50 sec. Overetch:
Measure Tox on each work wafer. (2 pnts measurement).
Do not remove PR. Inspect.
Measure PR thickness covering active area. tpr=
PR must be >800 nm.
UVBAKE program "J".

13.0 P-Well Field Implant Photo: Mask PFIELD
(Reversed NWELL mask)
Standard DUV lithography process. (Second photo)
PR thickness should be more than 1 micron.
Recommended PR: UV26-1.5
program No.2 on svgcoat6 and svgdev6.
N-Well area is covered with PR.

14.0 P-Well Field Ion Implant: B11, 70 KeV, 1.5E13/cm2.

15.0 N-Well Field Implant Photo: Mask NWELL

15.1 Remove PR in plasma O2. Clean wafers in sink9 (MEMS).

15.2 Standard DUV lithography process.
Recommended PR: UV26-1.5

16.0 N-Well Field Ion Implant: phosphorus, 40 KeV, 3E12.

17.0 Locos Oxidation: target = 650 nm

17.1 TCA clean furnace tube (tystar17).

17.2 Remove PR in O2 plasma and piranha clean wafers.
Standard clean wafers; dip in BHF 25:1 for 5-10 sec.
Include PCH, NCH.

17.3 Wet oxidation at 950 C (DRYOX.017):
5 min. dry O2
4 hrs. 40 min. wet O2
5 min. dry O2
20 min. N2 anneal
Measured tox on 3 work wafers. Tox=

18.0 Nitride Removal, include PCH.

18.1 Dip in 10:1 BHF for 60 sec to remove thin oxide on top of Si3N4.

18.2 Etch nitride off in phosphoric acid at 145 C.

19.0 Sacrificial Oxide: target = 20 (+/- 2) nm

19.1 TCA clean furnace tube (tystar17).

19.2 Standard clean wafers, include NCH and PCH.
Dip in 10:1 BHF until PCH and NCH dewet.

19.3 Dry oxidation at 950 C (DRYOX.017):
30 minutes dry O2
30 minutes N2 anneal
Measure Tox on PCH and NCH. Tox=

20.0 N-Channel Punchthrough and Threshold Adjustment Photo: Mask PFIELD
Standard DUV lithography process.
Recommended PR: UV26-1.5

21.0 N-Channel Punchthrough and Threshold Adjustment Implant. Include NCH.
1) B11, 120 KeV, 8E11/cm2.
2) B11, 30 KeV, 1.9E12/cm2.

22.0 P-Channel Punchthrough and Threshold Adjustment Photo: Mask PVT

Remove PR in plasma O2 and clean wafers in sink9 (MEMS side).
Standard DUV lithography process. Photoresist: UV26-1.5

23.0 P-Channel Punchthrough and Threshold Adjustment Implant. Include PCH.
1) Phosphorus, 190 KeV, 1E12,
2) B11, 20 KeV, 2.4E12.

24.0 Gate Oxidation/Poly-Si Deposition:
target = 20 (+/- 2.0) nm SiO2 + 450 (+/- 40) nm poly-Si

24.1 TCA clean furnace tube (tystar17).
Reserve poly-Si deposition tube (tystar10).

24.2 Standard clean wafers, include PCH, NCH,
Tox (prime P<100>), and one Tpoly1 monitoring wafers.

24.3 Dip off sacrificial oxide in 10:1 HF
until NCH and PCH dewet (approx. 1 min).

24.4 Dry oxidation at 950 C (DRYOX.017):
30 min dry O2 (Check previous run result)
30 min N2 anneal.

24.5 Immediately after oxidation deposit 450 nm of phos.doped
poly-Si (SDOPOLYI).
only include Tpoly1.
approx.time, temp.= 610 C
(Check previous run result)

24.6 Measurements
a) Measure oxide thickness on Tox, PCH and NCH.
b) Measure Dit and Qox on Tox.
c) Strip oxide from PCH and NCH, and measure the sheet resistivity.
d) Measure poly thickness on Tpoly1.
PCH and NCH proceed to step 27.2.
Tpoly1 proceeds to step 32.3.

25.0 Gate Definition: Mask POLY
Standard DUV lithography process.
Photoresist: UV210-0.6 (Shipley), BARC

26.0 Plasma etch poly-Si

26.1 Etch poly in Lam4 (Recipe: 400):
Pwr: Ave. etch time: Overetch:

26.2 Measure Tox in S/D area of each work wafer (2 pnts measurement).

26.3 Measure channel length using 1.0um gate.
CD =

27.0 Reoxidation and Capacitor Formation:
(If no capacitor is requested, skip step 27 through 29.2.)

27.1 TCA clean furnace tube (tystar17).
Reserve tystar11 and tystar10.

27.2 Standard clean wafers, including PCH, NCH, and two monitoring wafers, one for dry oxidation (Tpoly2) and one for LTO.
From here on: only 10 sec dip in 25/1 H2O/HF after piranha.

27.3 Dry oxidation at 900 C (SDRYOXB):
30 min dry O2
20 min N2 anneal.
Measure oxide thickness on Tpoly2:
Tpoly2 proceeds to Step 27.5.
PCH proceeds to Step 34 and NCH proceeds to Step 31.

27.4 1) Run a coating and monitoring LTO in tystar11 to get dep rate. Use recipe 11SULTOA and set 0 doping.
2) Deposit LTO for the desired oxide thickness.
3) Measure LTO thickness on monitoring wafer:

27.5 Second poly-Si deposition: immediately after oxidation
deposit 450 nm of phos.doped poly-Si:
only include Tpoly2.
approx.time = 2 hr. 18 min, temp.= 610 C.
Measure second poly thickness on Tpoly2:
Tpoly2 proceeds to step 32.3.

28.0 Capacitor Photo: Mask CAP-CE (CAP chrome-cf)
Standard DUV lithography process.

29.0 Plasma etch poly-Si:

29.1 Etch 2nd poly in Lam4 (Recipe: 400):
Power: Actual etch time: Overetch:

29.2 Measure Tox in S/D area on each work wafer.
Remove PR in O2 plasma.
Piranha clean wfrs in sink8.
Dehydrate wfrs in oven for > 30 min. at 120 C.

30.0 N+ S/D Photo: Mask N+S/D (NSD chrome-df)
Standard DUV lithography process.

31.0 N+ S/D Implant: Arsenic, 100 keV, 5E15/cm2, include NCH.

32.0 N+ S/D Anneal

32.1 TCA clean furnace tube (tystar17).

32.2 Remove PR in O2 plasma and piranha clean wafers
in sink9 MEMS side(no dip here).

32.3 Standard clean wafers in sink9 MOS side, incl. PCH, NCH, Tpoly1,
and Tpoly2.

32.4 Anneal in N2 at 900 C for 30 min (N2ANNEAL.017).

32.5 Strip oxide from NCH, Tpoly1, and Tpoly2.
Measure Rs of N+ S/D implant: Rs(NCH)=
Measure Rs of poly1 on Tpoly1: Rs(Tpoly1)=
Measure Rs of poly2 on Tpoly2: Rs(Tpoly2)=

33.0 P+ S/D Photo: Mask P+S/D (PSD chrome)
Standard DUV lithography process.
Photoresist: UV26-1.5 (Shipley)

34.0 P+ S/D Implant: B11, 20 keV, 5E15/cm2, include PCH.

35.0 PSG Deposition and Densification: target = 700 nm

35.1 Remove PR in O2 plasma and clean wafers in sink9 MEMS side (no dip).

35.2 Standard clean wafers in sink9 MOS side (10 sec dip).
Include one PSG monitoring wafer.

35.3 Deposit 700 nm PSG (11SDLTOA).
approx.time = 60 min. (check current dep. rate)
temp. = 450 C

35.4 Densify glass in tystar17 at 900 C, immediately after
PSG deposition (PSGDENS.017). Include PSG control.
5 min dry O2
20 min wet O2
5 min dry O2

Measure tPSG (using PSG control and working wafers):

N+ region Tox =
P+ region Tox =
Etch oxide on PCH.
Measure Rs of P+ S/D implant: Rs(PCH)=

35.5 Do wet oxidation dummy run afterwards to clean tube:
1 hr wet oxidation at 950 C (WETOX.017).

36.0 Contact Photo: Mask CONT (CONT chrome-df)
Standard DUV lithography process.

37.0 Contact Plasma Etch in lam2:
Recipe: Power: Etch time: Overetch:

38.0 Back side etch:

38.1 Remove PR in O2 plasma, piranha clean wafers in sink8 (no dip).
Dehydrate wafers in oven at 120 C for >30 min.

38.2 Etch backside:
(PCH and NCH can be included in b), c) and d).
a) Spin PR on front side, hard bake.
b) Dip off oxide (PSG) in 5:1 BHF.
c) Etch poly-Si (poly2 thickness) in lam4.
d) Etch oxide off in 5:1 BHF (cap. ox. thickness).
e) Etch poly-Si (poly1 thickness) in lam4.
f) Final dip in BHF until back dewets.
g) Remove PR in PRS2000, piranha clean wfrs in sink8 (no dip).

39.0 Metallization: target = 600 nm
Stnd clean wfrs and do a 30 sec. 25/1 H2O/HF dip just before metallization.
Sputter Al/2% Si on all wafers in CPA.

40.0 Metal Photo: Mask METAL1-CM (M1 chrome-cf)
Standard DUV lithography process. BARC

41.0 Plasma etch Al in Lam3.
Remove PR in PRS2000 or technics-c. tAl=
Probe test devices.

42.0 Sintering: 400 C for 20min in forming gas (tylan13).
No ramping, use VSINT400 program.

43.0 Testing:
1.0 um N- and P-channel devices, capacitors and inverter
Measure the sheet resistivities of PCH and NCH on prometrix.

44.0 Dielectric Film Deposition and Planerization:

44.1 Deposite 2 micron undoped LTO in tystar12 LPCVD (Non-MOS).
recipe:(12SULTOA)
approximate time: 230 min. temp:450 C

44.2 Planarization CMP. Standard recipe. time: 2min.

44.3 Clean wafers in CMPGREEN.

45.0 VIA Photo: Mask VIA (VIA chrome-df)
Standard DUV lithography process.

46.0 Etch VIA in lam2.
Recipe: Etch time: Overetch:
Need overetch.

47.0 Metal2 Metallization. target = 800-900 nm
Remove PR in matrix. Rinse the wafers in
sink7 and spin dry.
Sputter Al/2% Si CPA.

48.0 Metal Photo: Mask METAL2-CM (M2 chrome-cf)
Standard DUV lithography process. BARC
UVBAKE program "J".

49.0 Plasma etch Al in Lam3.
Remove PR in O2 plasma (matrix).

50.0 Sintering: 400 C for 20min in forming gas (tylan13).
No ramping, use VSINT400 program.

51.0 Testing:
Measure Metal1 and Metal2 contact chain.

End of Process

Appendix C

Input of TSUPREM4 (NMOS):

```
$ TITLE 1.3 um baseline process for NMOS
$ Define initial grid and substrate parameters

LINE X LOCATION=-5 SPACING=0.5 TAG=LEFT
LINE X LOCATION=-2 SPACING=0.2
LINE X LOCATION=-0.65 SPACING=0.1
LINE X LOCATION=0.0 SPACING=0.05 TAG=MIDDLE

LINE Y LOCATION=-.45 SPACING=0.25
LINE Y LOCATION=0 SPACING=0.1
LINE Y LOCATION=0.01 SPACING=0.05
LINE Y LOCATION=0.2 SPACING=0.1
LINE Y LOCATION=0.4 SPACING=0.25
LINE Y LOCATION=0.6 SPACING=0.3
LINE Y LOCATION=1.2 SPACING=0.4
LINE Y LOCATION=6 SPACING=0.4

eliminate col x.min=-0.6 y.min=0.4

INITIALIZE  boron=4e14 <100>

$ COMMENT Initial oxidation, 300 A
DIFFUSION temp=950 time=40 dryO2
DIFFUSION temp=950 time=30 INERT

$COMMENT P-WELL IMPLANT
IMPLANT boron dose=3e12 energy=80 damage

$ COMMENT Well DRIVE-in
DIFFUSION temp=1120 time=240 dryO2
DIFFUSION temp=1120 time=300 inert

ETCH oxide all

$ Pad oxide/nitride dep.
DIFFUSION time=60 temp=950 dryo2
DIFFUSION time=30 temp=950 inert
DEPOSIT NITRIDE thick=0.2 spac=5

$ etch nitride outside of the active region
ETCH nitride P1.X=-4 left

$ COMMENT P-Field implant (active area covered)
implant boron dose=1.5e13 energy=70

$ COMMENT LOCOS Oxidation
DIFFUSION temp=950 time=5 dryO2
DIFFUSION temp=950 time=280 wetO2
DIFFUSION temp=950 time=5 dryO2
DIFFUSION temp=950 time=20 inert

$ Etch all nitride
```

```
ETCH nitride all

$ Etch pad oxide
ETCH oxide trap thick=0.03

$ COMMENT sacrificial oxide, 200 A
DIFFUSION temp=950 time=30 dryO2
DIFFUSION temp=950 time=30 inert

$ COMMENT NVT Implant boron to shift the threshold, punch-throught
IMPLANT boron dose=8E11 energy=120 damage
IMPLANT boron dose=1.9e12 energy=30 damage

ETCH oxide trap thick=0.02

$ COMMENT Oxidize the gate targeting=200 A
DIFFUSION temp=950 time=30 dryo2
DIFFUSION temp=950 time=30 inert
print.1d  x.value=0.0        layers

$ COMMENT Deposit poly gate 4500 A
DEPOSIT polysilicon thickness=.45 phosph=1e20

$ Etch polysilicon
ETCH POLY LEFT P1.X=-0.65

$ N+ S/D IMPLANT
IMPLANT arsenic dose=5E15 energy=100 damage

$ Gate and S/D annealing
Diffuse time=30 temp=900 inert

$ PSG deposition
deposit oxide thick=0.7 spaces=3

$ PSG densification
DIFFUSION temp=900 time=5 dry
DIFFUSION temp=900 time=20 wet
DIFFUSION temp=900 time=5 dry

$ Etch contact holes

ETCH oxide start X=-3.5 Y=-1.2
ETCH oxide cont  X=-3.5 Y=-0.2
ETCH oxide cont  X=-1.5 Y=-0.2
ETCH oxide end   X=-1.5 Y=-1.2

ETCH oxide start X=-0.3 Y=-1.5
ETCH oxide cont  X=-0.3 Y=-0.75
ETCH oxide cont  X=0 Y=-0.75
ETCH oxide end   X=0 Y=-1.5

$ Deposit aluminum
DEPOSIT ALUMINUM thick=0.6 spac=3
```

```
$ Etch aluminum
ETCH aluminum P1.X=-3.8 left
ETCH aluminum P1.X=-1.2 right

$ Cut
$ STRUCTUR truncate bottom y=1.5

$ Create the whole structure
STRUCTUR REFLECT RIGHT

$ Save in MEDICI format
savefile out.file=nmos.med MEDICI
$ Save in TIF format
savefile  outf=nmos.tif      tif

STOP
else
```

Input of TSUPREM4 (PMOS):

```
$ TITLE 1.3 um baseline process for PMOS
$ Define initial grid and substrate parameters

LINE X LOCATION=-5 SPACING=0.5 TAG=LEFT
LINE X LOCATION=-2 SPACING=0.2
LINE X LOCATION=-0.65 SPACING=0.1
LINE X LOCATION=0.0 SPACING=0.05 TAG=MIDDLE

LINE Y LOCATION=-.45 SPACING=0.25
LINE Y LOCATION=0 SPACING=0.1
LINE Y LOCATION=0.01 SPACING=0.05
LINE Y LOCATION=0.2 SPACING=0.1
LINE Y LOCATION=0.4 SPACING=0.25
LINE Y LOCATION=0.6 SPACING=0.3
LINE Y LOCATION=1.2 SPACING=0.4
LINE Y LOCATION=6 SPACING=0.4

eliminate col x.min=-0.6 y.min=0.4

INITIALIZE  boron=4e14 <100>

$ COMMENT Initial oxidation, 300 A
DIFFUSION temp=950 time=40 dryO2
DIFFUSION temp=950 time=30 INERT

$COMMENT N-WEll IMPLANT
IMPLANT phosphorus dose=4e12 energy=80 damage

$ N-Well cover oxidation
Diffusion temp=950 time=30 dryo2
Diffusion temp=950 time=175 weto2
Diffusion temp=950 time=30 dryo2
Diffusion temp=950 time=20 inert
```

```
$ COMMENT Well DRIVE-in
DIFFUSION temp=1120 time=240 dryO2
DIFFUSION temp=1120 time=300 inert

ETCH oxide all

$ Pad oxide/nitride dep.
DIFFUSION time=60 temp=950 dryo2
DIFFUSION time=30 temp=950 inert
DEPOSIT NITRIDE thick=0.2 spac=5

$ Etch nitride outside of the active region
ETCH nitride P1.X=-4 left

$ COMMENT N-Field implant (active area covered)
implant phosphorus dose=3e12 energy=40

$ COMMENT LOCOS Oxidation
DIFFUSION temp=950 time=5 dryO2
DIFFUSION temp=950 time=280 wetO2
DIFFUSION temp=950 time=5 dryO2
DIFFUSION temp=950 time=20 inert

$ Etch all nitride
ETCH nitride all

$ Etch pad oxide
ETCH oxide trap thick=0.03

$ COMMENT sacrificial oxide, 200 A
DIFFUSION temp=950 time=30 dryO2
DIFFUSION temp=950 time=30 inert

$ COMMENT PVT Implant boron to shift the threshold, punch-throught
IMPLANT phosphorus dose=1E12 energy=190 damage
IMPLANT boron dose=2.4e12 energy=20 damage

$ Etch pad oxide
ETCH oxide trap thick=0.02

$ COMMENT Oxidize the gate targeting=200 A
DIFFUSION temp=950 time=30 dryo2
DIFFUSION temp=950 time=30 inert
print.1d  x.value=0.0         layers

$ COMMENT Deposit poly gate 4500 A
DEPOSIT polysilicon thickness=.45 phosph=1e20

$ Etch polysilicon
ETCH POLY LEFT P1.X=-0.65

$ P+ S/D IMPLANT
IMPLANT boron dose=5E15 energy=20 damage

$ PSG deposition
```

```
deposit oxide thick=0.7 spaces=3

$ PSG densification
DIFFUSION temp=900 time=5 dry
DIFFUSION temp=900 time=20 wet
DIFFUSION temp=900 time=5 dry

$ Contact holes

ETCH oxide start X=-3.2 Y=-1.2
ETCH oxide cont  X=-3.2 Y=-0.12
ETCH oxide cont  X=-1.5 Y=-0.12
ETCH oxide end   X=-1.5 Y=-1.2

ETCH oxide start X=-0.3 Y=-1.5
ETCH oxide cont  X=-0.3 Y=-0.6
ETCH oxide cont  X=0 Y=-0.6
ETCH oxide end   X=0 Y=-1.5

$ deposit aluminum
DEPOSIT ALUMINUM thick=0.6 spac=3

$ Etch aluminum
ETCH aluminum P1.X=-3.8 left
ETCH aluminum P1.X=-1.2 right

$ Cut
STRUCTUR truncate bottom y=1.5

$ Create the whole structure
STRUCTUR REFLECT RIGHT

$ Save in MEDICI format
savefile out.file=pmos.med MEDICI

$ Save in TIF format
savefile  outf=pmos.tif      TIF

STOP
```

Input of MEDICI (NMOS):

```
$ Medici 1.3 micron N-channel MOSFET

$ Mesh/impurity profiles imported from TSUPREM4
Mesh            inf=./nmos.med  tsuprem4        poly.elec=0     elec.bot

$ Electrode definition
Electrode       name=gate               x.min=-0.2      x.max=0.2       y.max=-0.6
Electrode       name=substrate  y.min=1         x.min=-1        x.max=1
Electrode       name=source             x.max=-1.6 x.min=-3.4   y.max=-0.25
Electrode       name=drain              x.min=1.6  x.max=3.4    y.max=-0.25

$ Specify fixed charge
INTERFAC QF=1E10

$ Regrid on doping
REGRID doping log ratio=2 smooth=1 ignore=2

$ Save in TIF format
savefile  out.file=afterregridnmos.tif          TIF

$ Specify physical models to use
Model           conmob          hpmob           consrh  auger   print

$ Symbolic factorization, solve initial
Symb            carrier=0
Solve           init

Symb            carrier=2       newton
Log             ivfile=nmos.log
Solve   v(gate)=0 v(drain)=0.05  vstep=0.1       nstep=30        electrode=gate
+v(source)=0 v(substrate)=0
Solve           out.file=nmos.sol

Extract         in.file=nmos.log  mos.para                gate=gate       drain=drain
Extract         in.file=nmos.log  n.resist  x.min=0.8     x.max=0.9       y.min=0.1

$ plot
Load            inf=./pmos.sol

Plot.2d             bound       fill        scale
Contour             potentia min=0 max=1.0 del=0.1
```

Input of MEDICI (PMOS):

```
$ Medici 1.3 micron P-channel MOSFET
$ Gate characteristics

$ Mesh/impurity profiles imported from TSUPREM4
Mesh            inf=./pmos.med  tsuprem4        poly.elec=0     elec.bot

$ Electrode definition
Electrode       name=gate               x.min=-0.2      x.max=0.2       y.max=-0.6
Electrode       name=substrate  y.min=1         x.min=-1        x.max=1
Electrode       name=source             x.max=-1.6      x.min=-3.4      y.max=-0.12
Electrode       name=drain              x.min=1.6       x.max=3.4       y.max=-0.12

$ Specify fixed charge
INTERFAC QF=1E10

$ Regrid on doping
REGRID doping log ratio=2 smooth=1 ignore=2

$ Save in TIF format
savefile  out.file=afterregridpmos.tif          TIF

$ Specify physical models to use
Model           conmob          hpmob           consrh  auger   print

$ Symbolic factorization, solve initial
Symb            carrier=0
Solve           init

Symb            carrier=2       newton
Log             ivfile=pmos.log
Solve           v(gate)=0 v(drain)=-0.05  vstep=-0.1      nstep=30        electrode=gate
+v(source)=0 v(substrate)=0
Solve           out.file=pmos.sol

Extract         in.file=pmos.log  mos.para                      gate=gate       drain=drain
Extract         in.file=pmos.log  n.resist  x.min=0.8      x.max=0.9       y.min=0.1

$ plot
Load            inf=./pmos.sol

Plot.2d             bound       fill        scale
Contour             potentia min=0 max=1.0 del=0.1
```

Appendix D

Output of BSIMPro: Model cards (text files)
HSPICE, (Cadence Compatibility Mode also available)

```
*model = bsim3
*NewModel =  3
*MetaSoftware Compatibility Mode
*These are BSIM3v3 Model Parameters.
*
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*
*LotName=CMOS61 UserName=VOROSL Date=11-14-2002
* Lmin=0.8 Lmax=10 Wmin=10 Wmax=15
.model NMOS NMOS
+Level= 49
*
* GENERAL PARAMETERS
*
+lmin=8.0e-7 lmax=1.0e-5 wmin=1.0e-5 wmax=1.5e-5
+Tref=27.0
+version =3.1
+Tox= 2.00E-08 Xj= 1.4000000E-07 Nch= 7.6703130E+16
+lln= 0.9554942 Mobmod=  1
+binunit= 2 xl= 0.00 xw= 0.00 Lmlt=  1 Wmlt=  1
+binflag=  0 Dwg= 0.00 Dwb= 0.00
*
* THRESHOLD VOLTAGE PARAMETERS
*
+Vth0= 0.6391217 K1= 0.9248490 K2= -5.0000000E-02 K3= 39.8961400
+Dvt0= 10.0000000 Dvt1= 0.5293429 Dvt2= 0.00
+Nlx= 3.8943220E-07 W0= 1.0000000E-06
+K3b= -10.0000000 Ngate= 1.0000000E+30
*
* MOBILITY PARAMETERS
*
+Vsat= 1.0000000E+05 Ua= 3.6807760E-09 Ub= 1.0000000E-18 Uc= 2.1654849E-10
+Rdsw= 7.8404940E+02 Prwb= -1.0000000E-03 Prwg= -1.0000000E-03
+Wr= 0.9291535 U0= 7.3223540E-02 A0= 1.0000000
+Keta= -2.5198845E-02 A1= 1.7735269E-02 A2= 0.9924715 Ags= 0.2662508
+B0= 1.2784894E-06 B1= 0.00
*
* SUBTHRESHOLD CURRENT PARAMETERS
*
+Voff= -8.0216180E-02 NFactor= 0.8527271 Cit= -1.0000000E-04
+Cdsc= 7.5308600E-04 Cdscb= 0.00 Cdscd= -1.5363394E-05
+Eta0= 5.5987510E-02 Etab= -0.1000000 Dsub= 0.5025811
*
* ROUT PARAMETERS
*
+Pclm= 1.5030025 Pdiblc1= 1.5839973E-02 Pdiblc2= 2.7644134E-03 Pdiblcb= 0.00
+Drout= 8.6171360E-02 Pscbe1= 3.3658770E+08 Pscbe2= 2.3683377E-05 Pvag= 0.00
+Delta= 1.0000000E-02 Alpha0= 0.00 Beta0= 30.0000000
```

```
*model = bsim3
*NewModel =  3
*MetaSoftware Compatibility Mode
*These are BSIM3v3 Model Parameters.
*
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*Using it in any form without explicit permission from BTA Technology, Inc. is strictly prohibited.
*
*LotName=CMOS61 UserName=VOROSL Date=11-14-2002
* Lmin=0.8 Lmax=10 Wmin=10 Wmax=15
.model PMOS PMOS
+Level= 49
*
* GENERAL PARAMETERS
*
+lmin=8.0e-7 lmax=1.0e-5 wmin=1.0e-5 wmax=1.5e-5
+Tref=27.0
+version =3.1
+Tox= 2.00E-08 Xj= 4.0000000E-07 Nch= 2.7047999E+16
+lln= 1.0000000 lwn= 1.0000000 wln= 1.0000000 wwn= 0.1000000 wint= 1.5000001E-07
+Mobmod=  1 binunit= 2
+Lmlt=  1 Wmlt=  1 binflag=  0
+Dwg= 5.0000000E-08 Dwb= 5.0000000E-08
*
* THRESHOLD VOLTAGE PARAMETERS
*
+Vth0= -0.7096410 K1= 0.5475855 K2= 0.00 K3= 1.0000000E-03
+Dvt0= 10.0000000 Dvt1= 0.9181482 Dvt2= -5.0000000E-02
+Nlx= 1.6097556E-07 W0= 1.0000000E-06
+K3b= -6.6307490 Ngate= 1.0000000E+30
*
* MOBILITY PARAMETERS
*
+Vsat= 1.0000000E+05 Ua= 5.1569220E-09 Ub= 9.9735260E-19 Uc= -1.0000000E-12
+Rdsw= 9.9974650E+02 Prwb= 0.00 Prwg= 0.00
+Wr= 0.9999283 U0= 2.9635694E-02 A0= 1.0000000
+Keta= -3.7500250E-02 A1= 0.00 A2= 0.9000000 Ags= 0.2507022 B0= 0.00 B1= 0.00
*
* SUBTHRESHOLD CURRENT PARAMETERS
*
+Voff= -8.5056040E-02 NFactor= 2.0000000 Cit= -1.0000000E-04
+Cdsc= 1.0000000E-03 Cdscb= 0.00 Cdscd= 5.2944400E-04
+Eta0= 0.7350919 Etab= 0.00
+Dsub= 0.6976542
*
* ROUT PARAMETERS
*
+Pclm= 5.6426010 Pdiblc1= 0.00 Pdiblc2= 1.0000000E-05 Pdiblcb= 0.00 Drout= 0.00
+Pscbe1= 1.0000000E+08 Pscbe2= 5.9430860E-08 Pvag= 10.0000000
+Delta= 1.0000000E-02 Alpha0= 0.00 Beta0= 30.0000000
```