AN INTERNATIONAL STANDARD MODEL FOR SOI CIRCUIT DESIGN

by

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
94720

An International Standard Model for SOI Circuit Design

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Pin Su

B.S. (National Chiao Tung University, Taiwan) 1992
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Committee in charge:

Professor Chenming Hu, Chair
Professor Tsu-Jae King
Professor Luke P. Lee

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Abstract

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Doctor of Philosophy in Engineering –
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Professor Chenming Hu, Chair

Scaling and high performance advantages make SOI an important CMOS technology. However, the main barrier to full exploitation of SOI performance and power is that the design of an SOI chip is a relatively risky process because the relative lacking of design experience makes it difficult to achieve fast turnaround and high probability of first-pass success. To surmount this barrier, a robust and physically accurate SPICE model is needed. SPICE modeling is the standard approach for precise design of standard cell libraries and critical-path sub-circuits in all large systems, as well as the basis for computing the look-up tables used in higher-level timing simulators. IP blocks are in turn designed using the speedier simulations. A compact SOI MOSFET model is crucial to the wide use of SOI technology.

The goal and the accomplishment of this work is to establish a standard SOI model for the semiconductor industry. This dissertation presents the approaches and

essential results of the research. First, we introduce BSIMPD (Berkeley Short-Channel IGFET Model - Partial Depletion), a derivative of the industry-standard bulk BSIM, for PD SOI design. We describe the three SOI-specific modules: floating-body model, self-heating model and body-contact model in BSIMPD. Besides, we propose a parameter extraction methodology for BSIMPD. We also demonstrate the ability of BSIMPD to capture the history effect. In addition, the simulation efficiency of BSIMPD is analyzed. BSIMPD has been selected by the EIA Compact Model Council as the standard model for SOI circuit design. Members of the council include Intel, IBM, TI, Motorola, TSMC, Philips, ST, Hitachi, AMD, and so on.

We have conducted research on the mechanism responsible for low voltage impact ionization in deep-submicrometer MOSFETs. This work is important to not only the prediction of the SOI floating-body effect, but also the understanding of hot carrier physics in both bulk and SOI MOSFETs at low voltage. We propose a *thermal activation energy* concept to explain the occurrence of impact ionization and thus the SOI kink effect at sub-bandgap drain voltage. The new concept suggests that self-heating induced impact ionization is the answer to the longstanding puzzle of anomalous gate bias dependence of the SOI substrate current. It also leads to a new and accurate compact impact ionization model in BSIMPD.

Finally, we present our approach to developing a Full Depletion (FD) SOI MOSFET model using BSIMPD as a foundation. We introduce the concept of *body-source built-in potential lowering* to unify the PD and FD models. With a single variable,

the same model can now represent both the PD and the FD devices. The unified BSIMSOI model is crucial to the SOI circuit design due to the coexistence of PD/FD devices in a single chip, and the coexistence of PD and FD behaviors in a single device depending on voltage bias.

To My Family

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Acknowledgments

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Chapter 1

Introduction

SOI (Silicon-On-Insulator) CMOS is emerging as a mainstream technology for high performance microprocessor [1]-[3] due to high speed and low power advantages. In addition, almost all major IC manufacturing companies have SOI on their roadmap. The remaining question is which technology generation to insert SOI for those companies. The importance of SOI rises as the scaling of bulk CMOS faces increasing difficulty [4].

SOI also offers better device scalability than its bulk counterpart. For a Partial Depletion (PD) SOI technology, thinning the SOI thickness in every generation allows the rise of channel doping concentration for better short channel control and device performance [5]. A superior subthreshold slope can be obtained for not only thin film Full Depletion (FD) devices, but also floating-body PD devices due to the beneficial gate-to-body capacitive coupling [6]. It is also worth noting that the forward body bias condition, typical of the operation of SOI devices, may reduce the built-in potential and therefore the short channel effect [7].

As the SOI technology gets mature, the main barrier to full exploitation of SOI performance and power is that the design of an SOI chip is a relatively risky process because a relative lacking of design experience makes it difficult to achieve fast turnaround and high probability of first-pass success. To surmount this barrier, a robust and physically accurate SPICE (compact) model is needed. SPICE modeling is the standard approach for precise design of standard cell libraries and critical-path sub-circuits in all large systems, as well as the basis for computing the look-up tables used in higher-level timing simulators. IP blocks are in turn designed using the speedier simulations. A compact SOI MOSFET model is crucial to SOI circuit design.

The goal of this work, therefore, is to establish a standard SOI model for semiconductor industry. This dissertation presents the essential research results and the approaches we have taken in developing this model. The organization is as follows.

Chapter 2 presents our BSIMPD (Berkeley Short-Channel IGFET Model - Partial Depletion) model, a sophisticated derivative of the industry-standard bulk BSIM [8][9]. BSIMPD [10][11] is already being used in production by major semiconductor companies such as IBM. It has contributed to the successful implementation of the 660-MHz 64-bit PowerPC [12] at its first design [13]. It was selected by the EIA Compact Model Council [14] as the standard SOI MOSFET model in December 2001. This chapter mainly describes the three SOI-specific modules: floating-body model, self-heating model and body-contact model in BSIMPD. Since we emphasize in this chapter

the physical mechanism behind the model, this chapter also serves as a complement of the BSIMPD users' manual [11]. It is worth noting that the simulation efficiency of BSIMPD, a crucial element for quality electronic design and a challenge for SOI modeling, is provided and analyzed.

Chapter 3 presents our research on the impact ionization phenomenon in state-of-the-art MOSFETs. This work is important in not only the prediction of the SOI floating-body effect, but also the fundamental hot carrier physics universal to both bulk and SOI deep-submicron MOSFETs. Our proposed *thermal activation energy* concept explains the occurrence of impact ionization and thus the SOI kink effect at sub-bandgap drain voltage. Notice that the supply voltage for the 65-nm (n+2) technology node is around 0.85 V. The thermal activation energy concept predicts the self-heating induced impact ionization and solves the longstanding difficulty in modeling the gate bias dependence of the SOI substrate current. The new concept also predicts a drain bias dependence of the low voltage ionization rate that is different from the classical model [15]. A generalization of both the thermally assisted model and the classical model results in the compact impact ionization model in BSIMPD.

Starting from the 0.13-μm technology node with around 20-Å equivalent oxide thickness, the oxide tunneling becomes significant. How might the gate tunneling current impact the dynamic behavior of SOI CMOS? Chapter 4 attempts to assess this question using BSIMPD. We first demonstrate the ability of BSIMPD to capture the history effect, a main concern for SOI circuit design and a challenge for SOI modeling. Then we can

investigate the impact of gate-body tunneling on dynamic behaviors of SOI CMOS with the aid of the proven BSIMPD model. This study is representative of technology generations with supply voltage above 1 V. For scaled SOI CMOS with sub-1V power supply, another case study via device simulation is used to predict the depletion trend of thin film SOI due to gate tunneling.

Since it is the model card (parameter set) that represents a specific SOI technology to circuit design, accurate parameter extraction for BSIMPD is crucial to creating designs that work the first time. Chapter 5 presents our strategy to attack the complication caused by the SOI-specific self-heating and floating-body effects in parameter extraction. The proposed methodology has been verified through the comparison between model and experimental data. The systematic parameter extraction approach as well as the satisfactory model accuracy is crucial to this industry standard model.

For the 65-nm (n+2) technology node and beyond, the SOI thickness is projected to be below 30 nm and the SOI device may get into full depletion easily. There is a need for an FD SOI MOSFET model. Chapter 6 presents our approach to developing the FD SOI model using BSIMPD as a foundation. We introduce the concept of *body-source built-in potential lowering* to consolidate both PD and FD models. This concept is important because it serves as a measure of the floating-body behavior of SOI devices. It is also the basis of the BSIMSOI framework. The unified BSIMSOI model is crucial to

the SOI circuit design due to the coexistence of PD/FD devices in a single chip, which has become one of the biggest challenges in the scaling SOI CMOS.

Chapter 7 summarizes essential research results and contributions of this dissertation work.

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Chapter 2

BSIMPD:

A Partial-Depletion SOI MOSFET Model for Deep-Submicron CMOS Designs

2.1 Introduction

Four technological trends set the stage for Partially-Depleted SOI (PDSOI) to become an important IC technology for the 21st century: (1) High performance. PDSOI provides a performance gain of 20 to 35 percent over bulk CMOS [1] due to the reduction of junction capacitance and the absence of the body-bias effect in series connected devices, e.g. in NAND and NOR gates. (2) Low power. With the same performance SOI can operate at a lower voltage and therefore lower power. (3) Mixed and Embedded Technologies. SOI provides a way to isolate analog circuits from substrate noise and provides high-Q inductors. It may be beneficial to embedded DRAM because of good

signal isolation from the logic circuit blocks. (4) Process simplicity. SOI may reduce some future bulk-technology's manufacturing difficulties such as isolation, shallow junction, and latchup sensitivity.

As PDSOI technology becomes more widely used, a robust and physically accurate SPICE model is sorely needed to reduce the risk of inadequate circuit designs. BSIMPD (Berkeley Short-Channel IGFET Model - Partial Depletion) attempts to serve as this critical communication vehicle between IC design and manufacturing.

BSIMPD [2] was jointly developed by University of California at Berkeley and IBM, and its source code may be downloaded from the web [14]. This model is a derivative of the industry-standard bulk-MOSFET model BSIM3v3 [3]. Three important additions are made to the SOI model: floating-body model, self-heating model and body-contact model.

In this chapter, we describe these SOI-specific modules as well as the BSIMPD simulation efficiency, a critical element to an industry-standard SOI MOSFET model [15]. The parameter extraction methodology for BSIMPD will be proposed in Chapter 5.

2.2 Floating-Body Model

To accurately model the potential of the floating body, which has strong impact on the device behavior, the circuit shown in Figure 2-1 is solved for the body voltage (V_{BS}). In DC, this voltage is determined by the various body current components. For AC/transient simulation, the displacement currents originating from capacitive couplings will also contribute. Once the body potential is found, the impact of the floating body on drain current (I_D) can be captured through an accurate threshold voltage model (Figure 2-2) and bulk charge model (Figure 2-3) in the high forward body-bias regime.

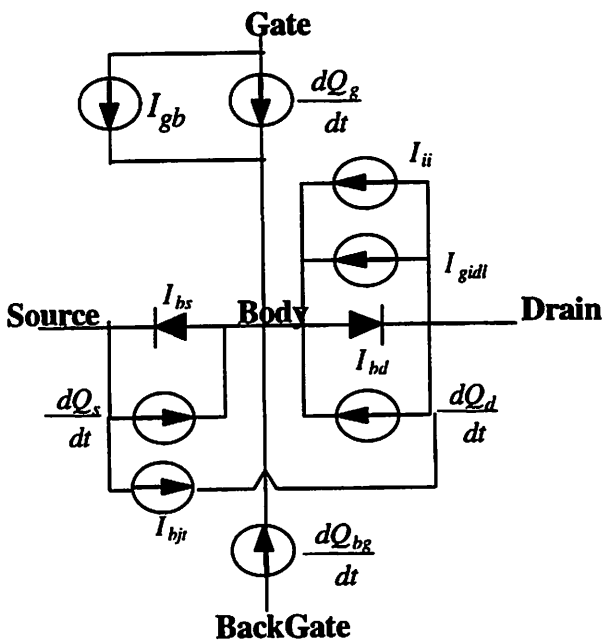


Figure 2-1. Circuit representation of the floating body. I_{gb}: oxide tunneling current. I_{ii}: impact ionization current. I_{gidl}: gate induced drain leakage. I_{bjt}: bipolar current. I_{bs}: recombination current. I_{bd}: junction leakage.

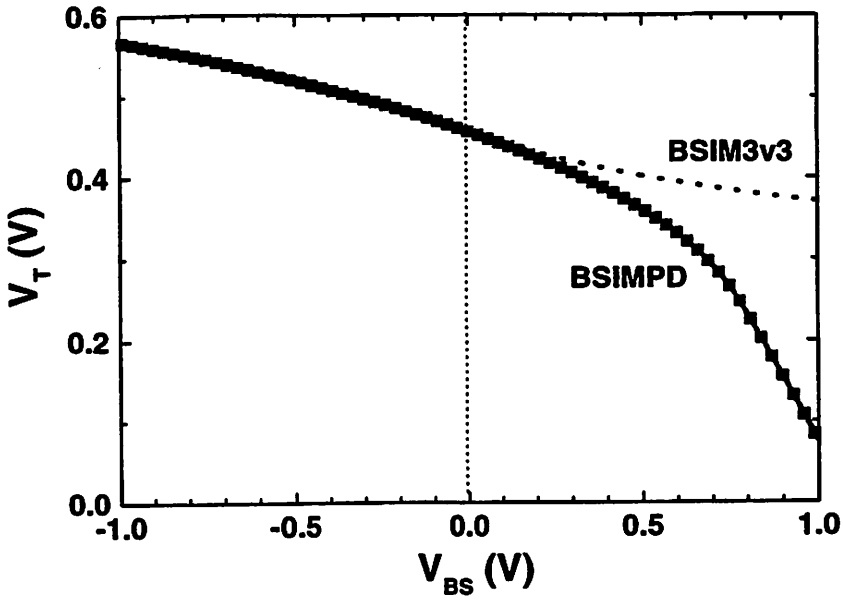


Figure 2-2. An accurate threshold voltage model in the high forward body-bias regime [7] is crucial to a PDSOI model.

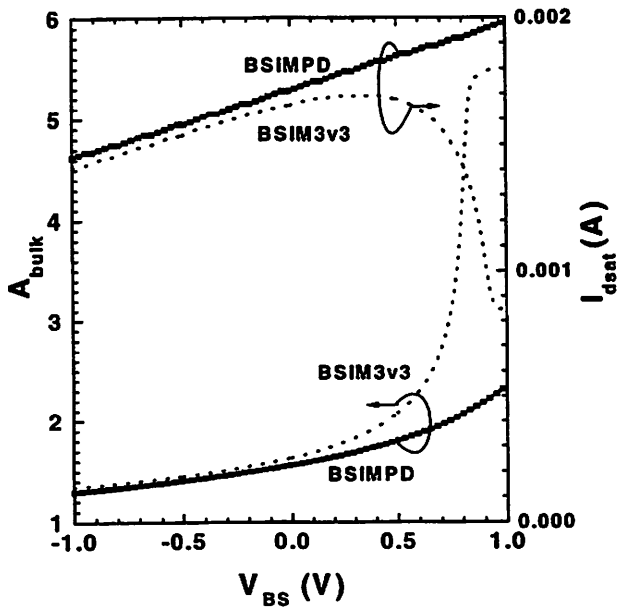


Figure 2-3. The model behavior of bulk charge effect (A_{bulk}) in the high forward body-bias regime [7] is critical to the model behavior of drain current (I_{dsat}) and thus simulation convergency.

2.2.1 DC Model

The IV characteristics in Figure 2-4 show kinks in the high drain-bias regime due to the rise in body voltage that is caused by the impact-ionization current (I_{II}). The excess I_D is a major source of performance gain of SOI over bulk and thus needs to be well modeled. Since the steady-state body potential is determined by the counter-balance of I_{II} and the body-source diode current, accurate I_{II} (detailed in Chapter 3) and diode current models [7], which takes into account the tunneling effect in the high-field halo (pocket implant) region of the junctions, are developed to achieve the accuracy of the BSIMPD model.

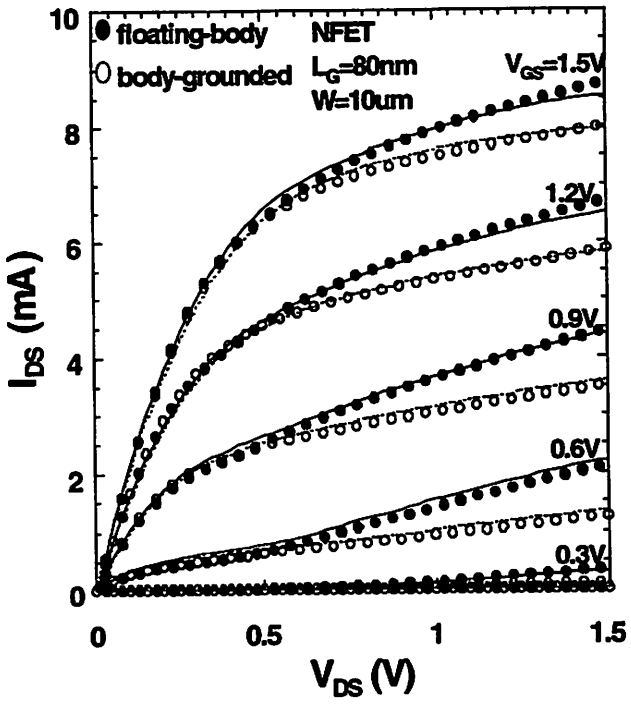


Figure 2-4. BSIMPD (line) accurately models the IV characteristics of a PDSOI transistor showing excess current drive due to floating-body kink effect [18].

2.2.2 AC/Transient Model

During switching, the body potential is determined by the initial state of the body charge as well as the body-to-gate/drain/source/backgate capacitive coupling. This results in the history dependence of gate delay shown in Figure 2-5. To catch this delay variation, an accurate modeling of the capacitances and the body time constant is required (detailed in Chapter 4). As shown in Figure 2-6, the model-prediction of the body potential for fast gate/drain voltage ramp shows good agreement with 2D device simulation. As the gate oxide thickness is scaled down, the impact of gate-to-body tunneling on the history effect (detailed in Chapter 4) as well as the impact of quantum effects on the gate capacitance becomes significant. A charge-thickness model (CTM) [4], which considers the quantization of inversion charges and poly-gate depletion in the capacitance model, is embedded in BSIMPD to support deep-submicron CMOS designs.

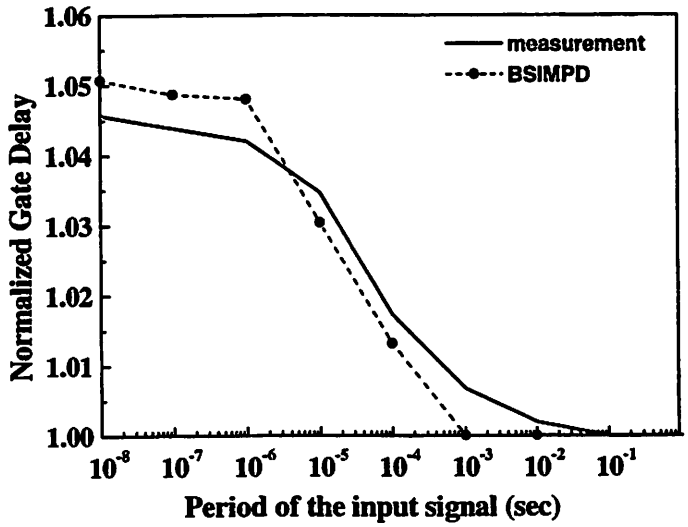


Figure 2-5. Delay per stage of a PDSOI unloaded inverter chain shows history dependence due to dynamic variations of the stored body charges and thus variation of V_T.

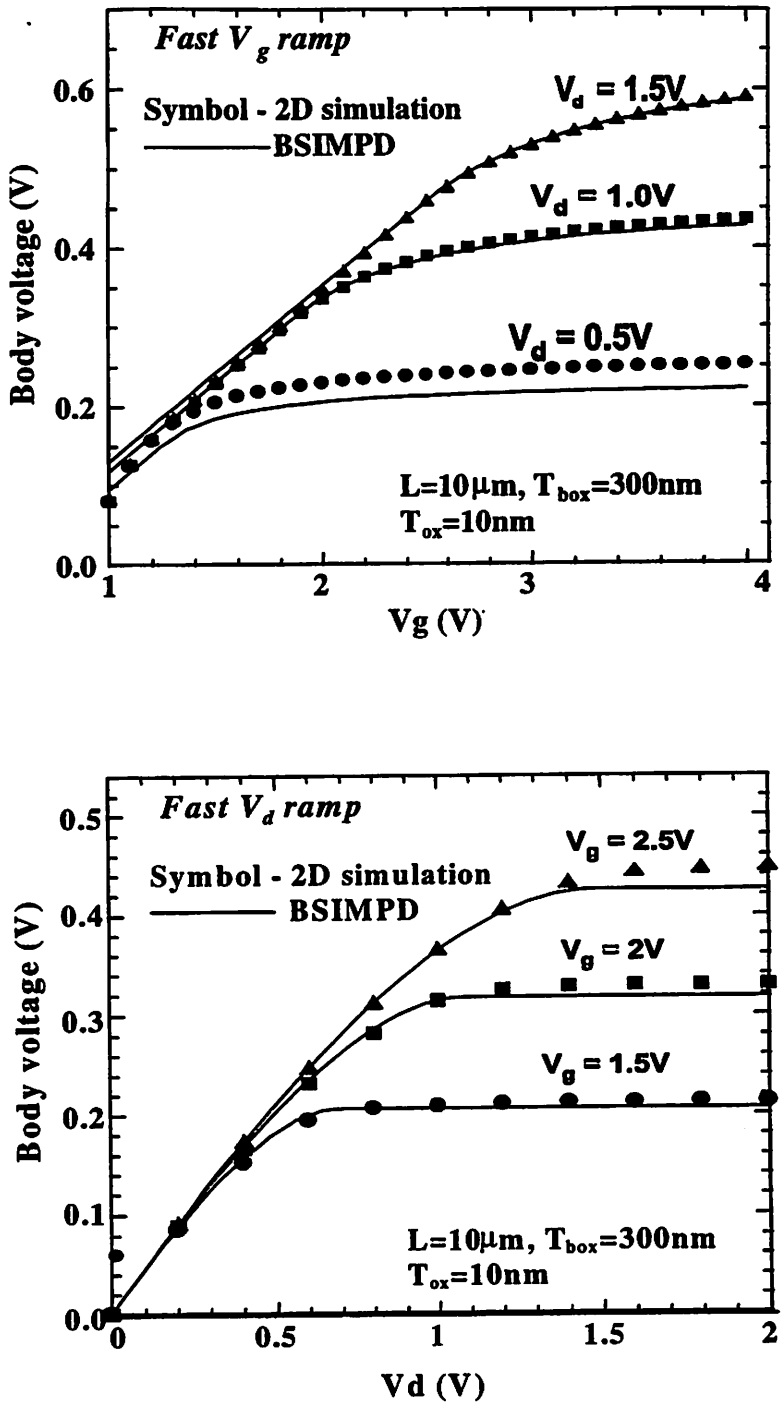


Figure 2-6. The body potential predicted by BSIMPD for fast gate/drain voltage ramp agrees well with 2D device simulation.

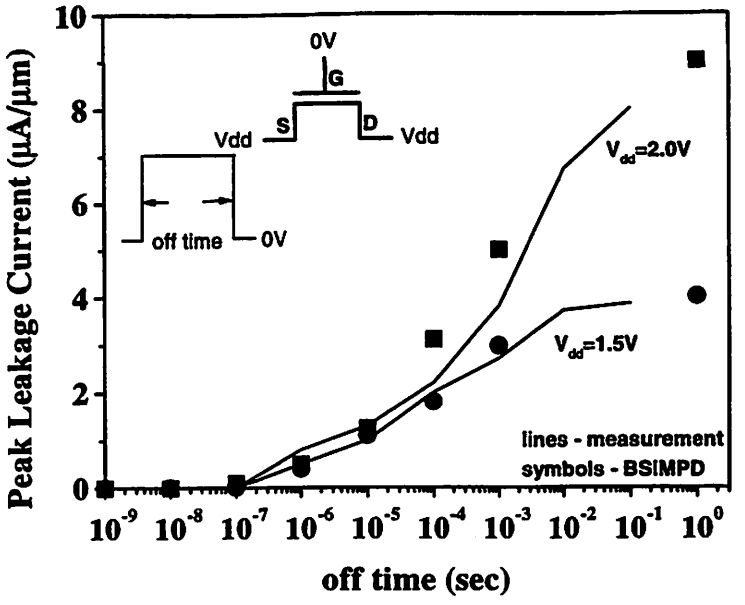


Figure 2-7. Peak leakage current of a pass-gate transistor following a fast pull down of the source voltage demonstrates another floating body effect, which is captured by BSIMPD.

The pass-gate leakage shown in Figure 2-7 is another consequence of the floating-body effect and can cause circuit failures. Since V_{BS} can be very high during a fast pull-down of the source voltage, a significant lateral bipolar current develops and gives rise to the leakage current. Therefore, an accurate bipolar current model [7] is important to pass-gate circuit simulation. Besides, the junction diffusion capacitance, which dominates the total junction capacitance in the high V_{BS} regime (Figure 2-8), plays an important role in the determination of V_{BS} during the fast pull-down of the source voltage. Therefore, a junction diffusion charge model [7] has been developed and implemented in BSIMPD.

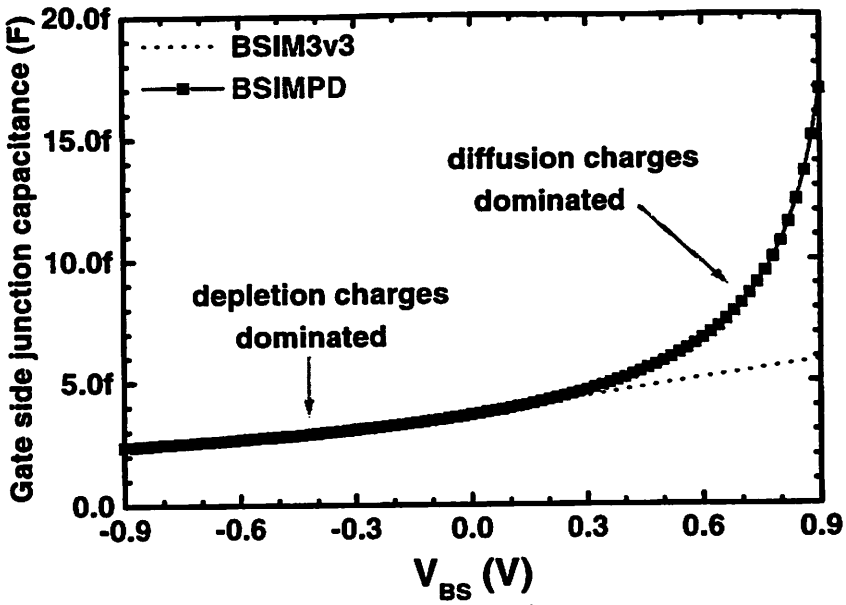


Figure 2-8. The junction diffusion charge/capacitance is crucial to a PDSOI model.

2.3 Self-Heating Model

Due to the low thermal conductivity of the buried oxide underneath the active device (about two orders of magnitude less than that of silicon), SOI MOSFETs are susceptible to the local thermal heating generated in the channel. This self-heating phenomenon varies the device temperature and thus the current drive. It has significant impact on analog parts of the design such as static I/O and PLL.

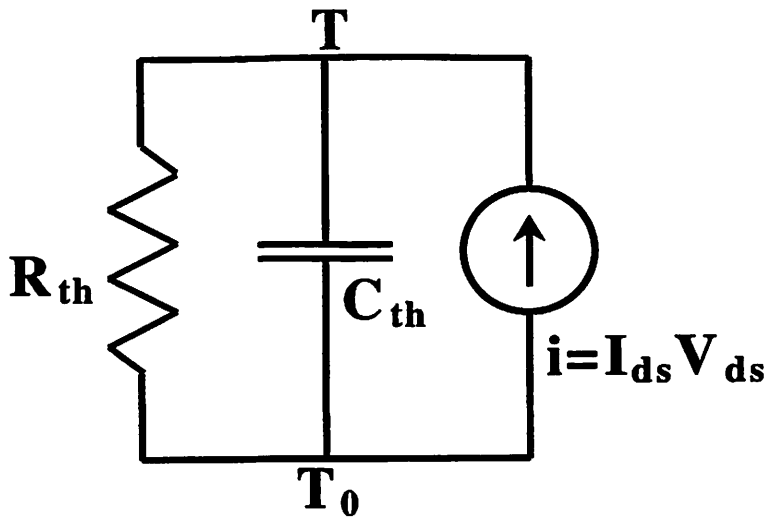


Figure 2-9. BSIMPD uses this self-heating equivalent circuit driven by the transistor power to model the device temperature (node-voltage of T).

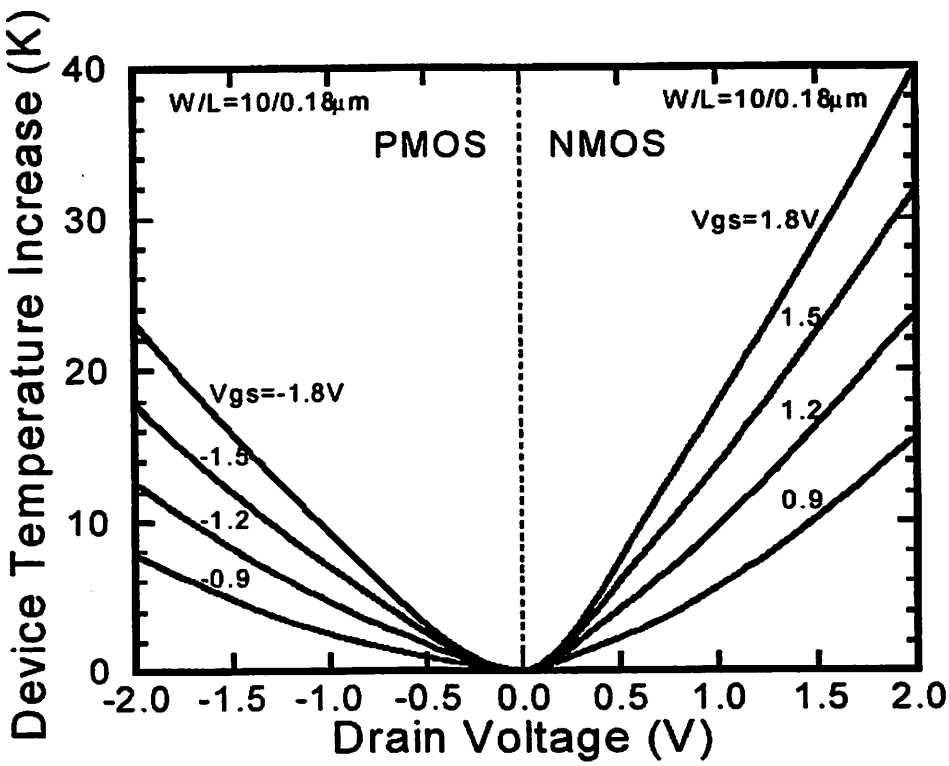


Figure 2-10. The device temperature rise due to self-heating is larger in NMOSFET than in PMOSFET for a given device geometry and bias condition [17].

2.3.1 Self-Heating Model in BSIMPD

To keep track of the device temperature rise (ΔT) with the bias, an auxiliary $R_{th}C_{th}$ circuit driven by a current source equal to the power dissipation (Figure 2-9) is employed in BSIMPD. Here R_{th} and C_{th} represent thermal resistance and thermal capacitance of the device, respectively. Figure 2-10 shows the calculated ΔT after the convergence between device temperature and the drain current is achieved. Notice that the impact of self-heating is larger in NMOS than in PMOS due to the difference in current drive capability.

As shown in Figure 2-11, the thermal conductance, G_{th} (= R_{th}^{-1}), is dependent on the gate width, W_g, of the device. The dependence has been modeled in BSIMPD as

$$G_{th} = W_g \cdot G_{th1} + G_{th0} \qquad (2\text{-}1).$$

Here the first term represents the heat dissipation via source/drain films and is proportional to W_g with a slope G_{th1}. The second term, a constant, is introduced to account for the heat dissipation via gate electrode and body contact region (additional for body-contacted devices) [17]. Notice that G_{th0} dominates the total thermal conductance for narrow width devices and explains the difference in G_{th} between body-contacted and floating-body devices.

However, the thermal time constant, τ_{th} (= $R_{th}C_{th}$), is nearly a constant for a given technology, as shown in Figure 2-12. In other words, the thermal capacitance C_{th} is

proportional to the thermal conductance G_{th} with a slope τ_{th}.

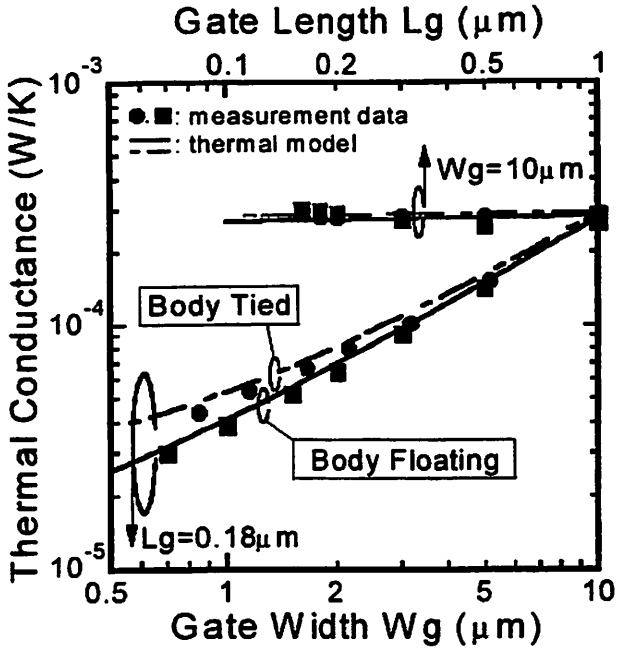


Figure 2-11. The geometry dependence of thermal conductance for NMOS devices with floating-body and body-contact structures, respectively [17].

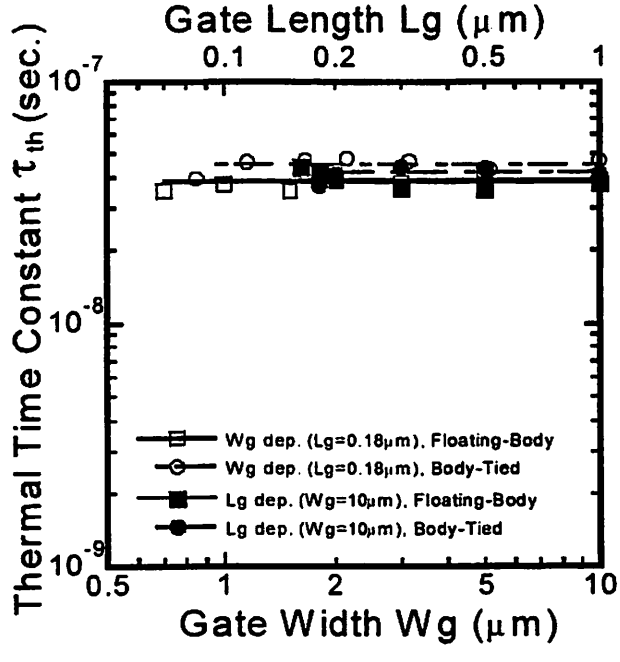


Figure 2-12. The geometry dependence of thermal time constant for NMOS devices with floating-body and body-contact structures, respectively [17].

2.3.2 Impact of Self-Heating on SOI Modeling

In DC, the device temperature rise due to self-heating reduces the body potential by inducing more diode leakage and thus degrades the current drive beyond the usual bulk-MOSFET temperature sensitivity, as shown in Figure 2-13. In other words, *self-heating complicates the prediction of the floating-body effect through temperature-sensitive body-current components, which determine the body potential.* The interplay of self-heating and floating-body effects imposes a much higher requirement in modeling the temperature dependence of the body currents for SOI than bulk. Therefore, an accurate temperature-dependence model for the junction leakage (Figure 2-14) has been developed [7] and implemented in BSIMPD to capture the floating-body effect coupled by self-heating.

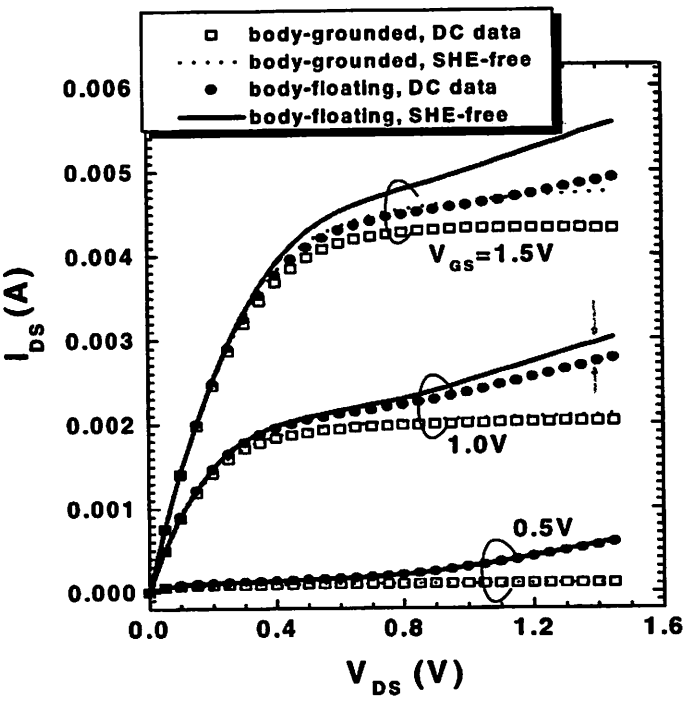


Figure 2-13. Self-heating effect (SHE) causes more drain current degradation for SOI devices through the floating-body effect. The SHE-free concept/method will be described in Chapter 5.

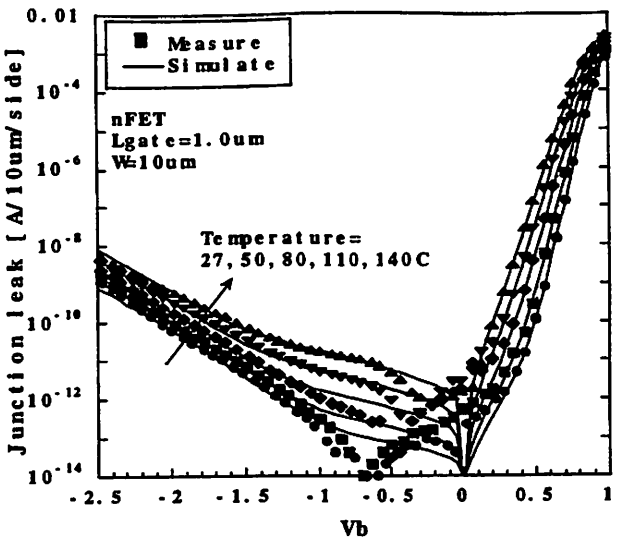


Figure 2-14. Self-heating interacts with the floating-body effect through the diode current, which is sensitive to device temperature [18].

Under dynamic operating conditions typical of digital circuit operation, however, the self-heating effect is generally insignificant. Since the average power consumption per device is low and its switching time (~10 ps) is much shorter than the thermal time constant (τ_{th} ~ 100 ns as shown in Figure 2-12) [17] for state-of-the-art high performance SOI CMOS, the time averaged temperature rise due to self-heating is quite small. For example, considering a chip with power consumption of 10 W, 10 million transistors, and R_{th} of 10^4 °C/W, the average device temperature increase can roughly be estimated as 0.01 °C and negligible. As a result, there is a gap between the self-heating-suffered modeling data measured in DC and the self-heating-free current drive present in most logic circuits.

In other words, self-heating is a modeling rather than performance issue for devices in low power logic circuits. The self-heating modeling solution along with the

BSIMPD parameter extraction methodology will be described in Chapter 5.

2.4 Body-Contact Model

Since the body-contact (BC) is widely used in critical circuits (e.g., PLL and other analog circuits), an accurate model that can represent the non-idealities of the contact is essential to precision-oriented simulations. Here we first present the impact of body-contact on the output conductance of SOI MOSFETs to demonstrate the need of a body-contact model. The complete body-contact model [5] implemented in BSIMPD is then described subsequently.

2.4.1 Case Study – Impact of Body Contact on Output Resistance

Floating Body Effect (FBE) in PDSOI MOSFETs has become a major concern, and body-contact is the most straightforward way to avoid FBE. However, the body resistance increases and has a distributed nature as the channel width is increased, the efficiency of the body tie is limited [8][9]. Here we report a degradation of AC output resistance (R_{out}) in PD devices due to the capacitive coupling between body-contact and drain. The effect should be taken into account in device design and circuit simulation.

All the four-terminal SOI devices used in this study adopt the side-contact scheme as shown in Figure 2-15. These PD nMOSFETs are fabricated on SIMOX wafer with 85 nm buried oxide and 160 nm film thickness. R_{out} is measured by the HP4194A gain phase analyzer with the HP4145B supplying the DC bias.

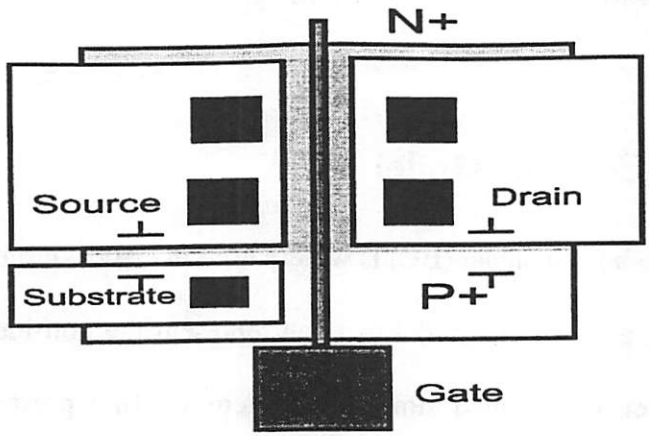


Figure 2-15. Layout of the four-terminal side-body contact scheme used in this measurement. Note the capacitor between drain and body-contact, which causes R_{out} degradation.

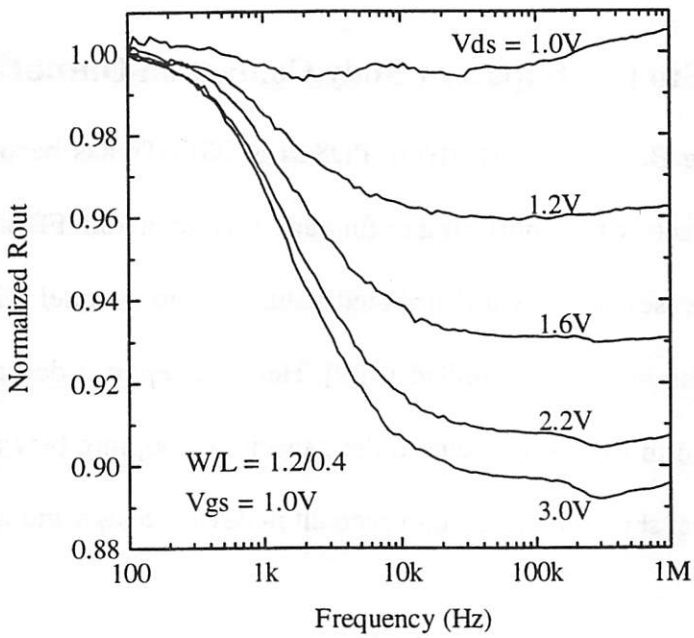


Figure 2-16. R_{out} versus frequency for various drain biases.

The R_{out} versus frequency characteristics with different drain bias V_{ds} are shown in Figure 2-16. R_{out} is normalized to its DC value. The R_{out} at saturation decreases with increasing frequency to a certain value, which depends on V_{ds}. Figure 2-17 shows R_{out} versus V_{ds} for various frequencies. It is noted that R_{out} stops dropping at a frequency around 10 kHz. The effect can be explained by the body potential fluctuation under the influence of drain coupling caused by body-contact. When a small signal v_d is applied, the floating body potential v_b can be estimated with the small-signal equivalent circuit shown in Figure 2-18 [10]. The capacitance C_d is composed of the intrinsic junction capacitance and the parasitic capacitance between the body-contact and the drain. The latter dominates when the device dimension becomes small. It causes an increase in the output conductance (i.e., a decrease in R_{out}) through the body effect. This drain coupling effect is insignificant at very low frequencies when the body resistor R_b provides an effective discharging path for the capacitive current from the drain. So, the value of R_b will affect the frequency f_c at which the R_{out} degradation appears. This can be verified by changing the substrate bias V_{bg} so that the thickness of neutral-body region and therefore R_b is modulated. Figure 2-19 shows that f_c increases as R_b decreases, as expected. C_b represents the equivalent capacitance from body to AC ground. It consists of the front gate, body-source diode and buried oxide capacitances. At high enough frequency (e.g., 10 kHz) v_b is determined by the voltage divider that is made of C_b and C_d, so R_{out} becomes a constant at high frequency. This constant value still depends on V_{bg} because C_b and C_d depends on V_{bg}.

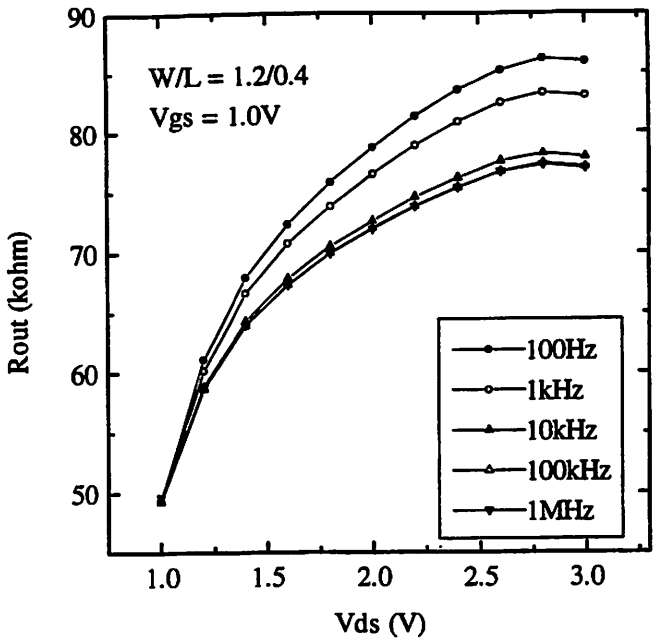


Figure 2-17. R_{out} versus drain bias for various frequencies.

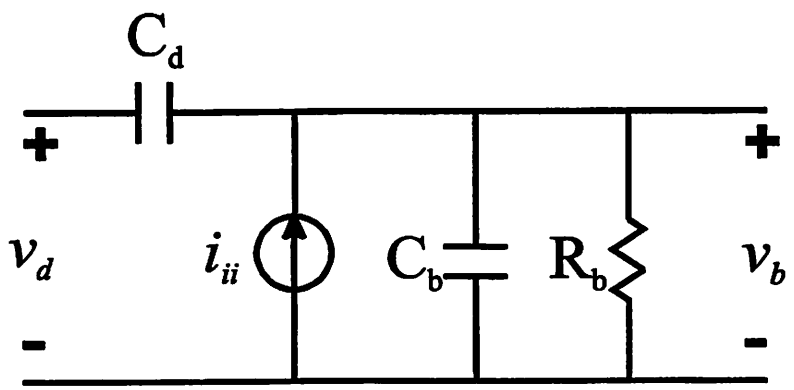


Figure 2-18. Small signal equivalent circuit for the floating body. C_d is dominated by the capacitance between drain and body-contact. C_b represents the equivalent capacitance from body to AC ground. R_b is the body resistance. i_{ii} is the impact ionization current.

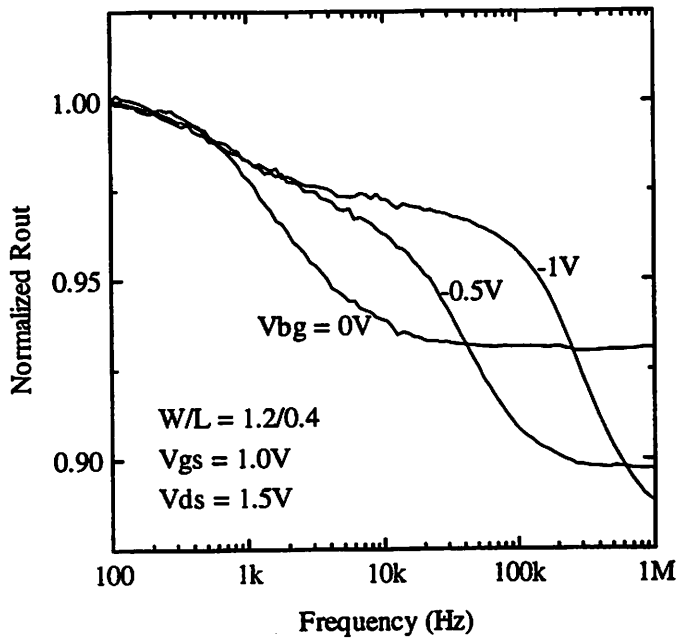


Figure 2-19. R_{out} versus frequency for various substrate biases showing the effect of R_b. R_b decreases as V_{bg} becomes negative.

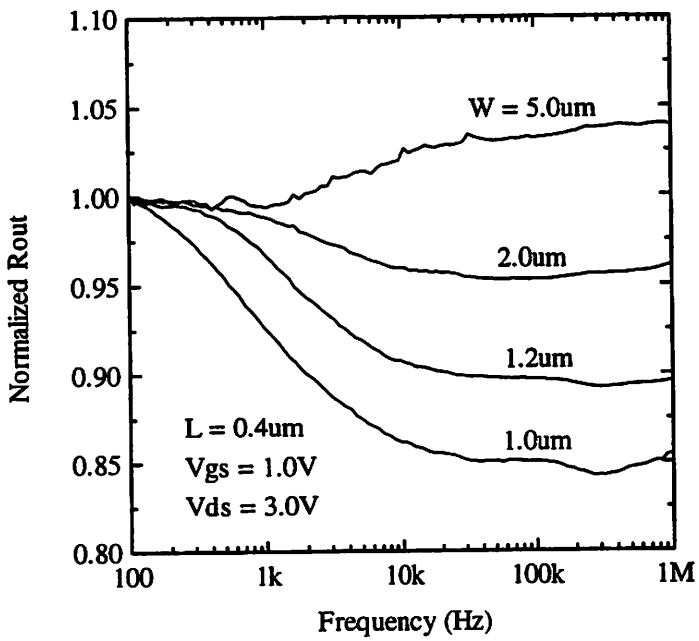


Figure 2-20. R_{out} versus frequency showing the width dependence of this drain coupling effect.

Figure 2-20 shows the width dependence of this effect. Instead of decreasing, R_{out} increases with frequency when W = 5 um. Since the drain coupling effect becomes negligible compared to the front gate coupling when the channel width is increased, v_b is mainly influenced by impact ionization current i_{ii} as has been reported previously [11]. The effect of i_{ii} decreases with frequency since fewer holes are generated during a half period as frequency increases. Hence R_{out} increases with frequency.

In conclusion, the drain coupling effect due to the body-contact structure will cause R_{out} degradation as channel width is narrowed down. This effect should be taken into account in device design and modeling. An accurate SOI circuit model accounting this width effect will be helpful to sensitive analog circuit design if a body-contact technology is used.

2.4.2 Body-Contact Model in BSIMPD

Making contact to the body of a PDSOI transistor offers another degree of design freedom. For example, DTMOS [12] has demonstrated that the body-contact can be used to enhance the power/delay performance. It has also been shown that the body-contact plays an important role in eliminating the floating-body instability [13] for sensitive circuits. As demonstrated in the previous section, however, the body-contact effect may be significant. Therefore, a complete SPICE model that explicitly addresses the non-idealities of the body-contact is surely needed for SOI circuit design. Here we present a compact body-contact SOI MOSFET model that has been implemented in BSIMPD [2][14] for circuit simulation.

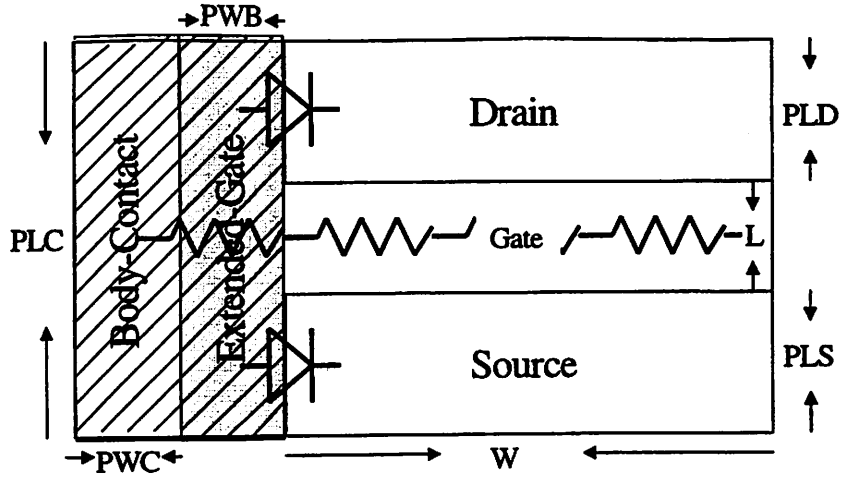


Figure 2-21. Layout representation illustrating the body-contact model of BSIMPD. Distributed body resistance as well as geometry-dependent parasitic source/drain diodes, gate-to-body (gray area) and body-to-backgate (hashed area) overlap capacitances are considered.

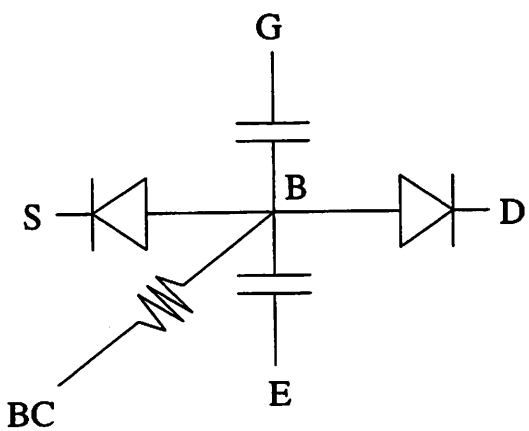


Figure 2-22. The equivalent circuit used in BSIMPD to model the non-ideal body contact. G: gate, E: substrate, S: source, D: drain, B: body, BC: body-contact. The diodes between B and S/D are the gated diodes at the sides of source/drain (in Figure 2-21 where "Extended-Gate" and "Source" / "Drain" intersect). The capacitance between G and B is the gate-to-body overlap capacitance in the "Extended-Gate" region. The capacitance between E and B is the substrate-to-body overlap capacitance in both the "Body-Contact" and the "Extended-Gate" region.

Model:

The model can be described using a transistor with the T-gate layout shown in Figure 2-21. The body-contact provides the transistor a resistive path for charging/discharging of the body. However the associated body-contact diffusion and the "Extended-Gate" region interact with other electrical terminals as well and may be represented by the equivalent circuit shown in Figure 2-22. The lumped resistance between B node and BC node consists of the intrinsic body resistance R_b and the extrinsic body resistance R_{bext}. R_b is modeled by $R_{body} \cdot W/L$, where R_{body} is the body sheet resistance along the channel width. R_{bext} is modeled by $R_{bsh} \cdot N_{rb}$, where R_{bsh} and N_{rb} are the body sheet resistance and the number of squares in the "Extended-Gate" region, respectively.

The parasitic diodes between B and S/D are characterized by the parameters P_{sbcp}/P_{dbcp}, the perimeter length of body-contact at the sides of source/drain. Similarly, the parasitic capacitances between B and G/E are characterized by the parameters A_{gbcp}/A_{ebcp}, which stand for the gate/substrate-to-body overlap. Since these parameters are layout-dependent, they are specified in a per-instance manner. According to the layout geometry of Figure 2-21, we have $P_{sbcp}=PLS$, $P_{dbcp}=PLD$, $A_{gbcp}=PWB \cdot PLC$ and $A_{ebcp}=(PWB+PWC) \cdot PLC$.

Due to the distributed nature of R_b, a lumped resistor is no longer satisfactory for sensitive circuits. Therefore, an accessible B node is provided in BSIMPD so that users can perform distributed simulation by partitioning a wide transistor and cascading the

body resistors of the sub-transistors (Figure 2-23). For each sub-transistor, the partition number, N_{seg}, should be specified so that the transistor current and charge can be scaled by N_{seg} without over-estimating the narrow-width effect. Note that the width can be non-uniformly partitioned as long as the sum rule $\Sigma N_{seg}^{-1}=1$ is fulfilled.

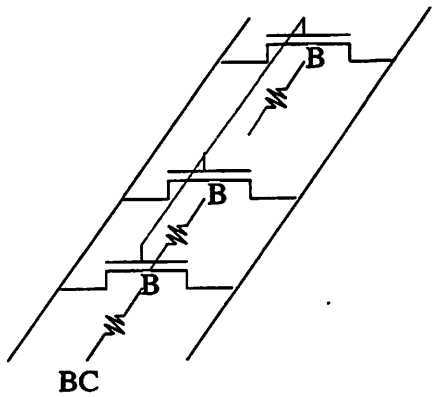


Figure 2-23. An accessible B node is provided in BSIMPD to facilitate the distributed simulation.

Impact on Device Parametrics:

The importance of body-contact model can be demonstrated from another perspective: Since most of the model parameters of floating-body transistors have to be extracted from body-contacted devices, the non-ideal body-contact effect needs to be taken into account in parameter extraction. Its impact on the key device parametrics in the high body-bias regime, which is essential to PDSOI operations, is investigated using a typical body-contact device with W = 5 μm, $L_{eff} \cong 0.1$ μm.

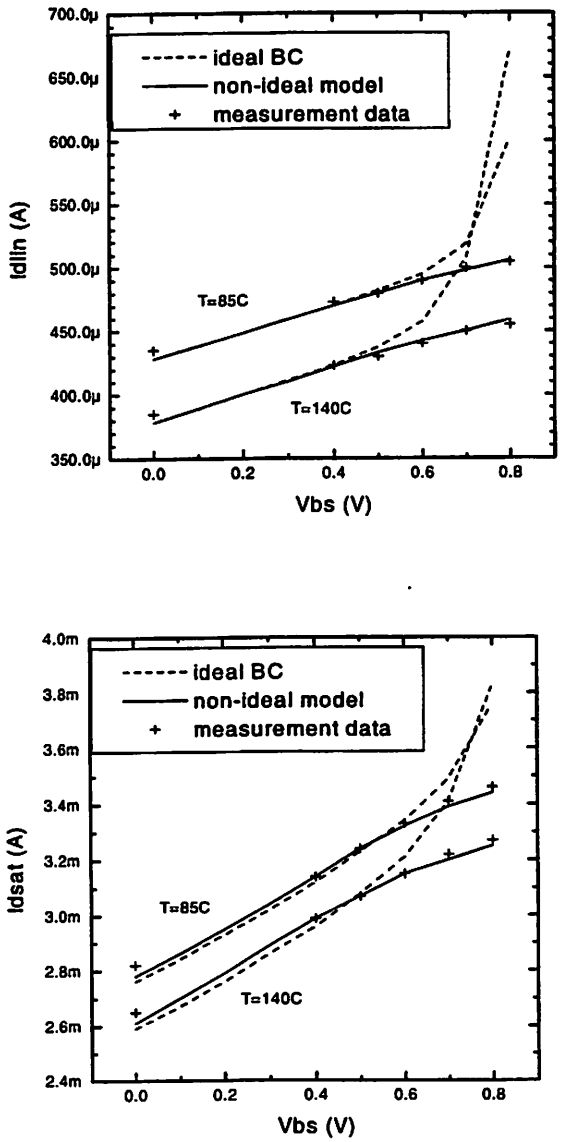
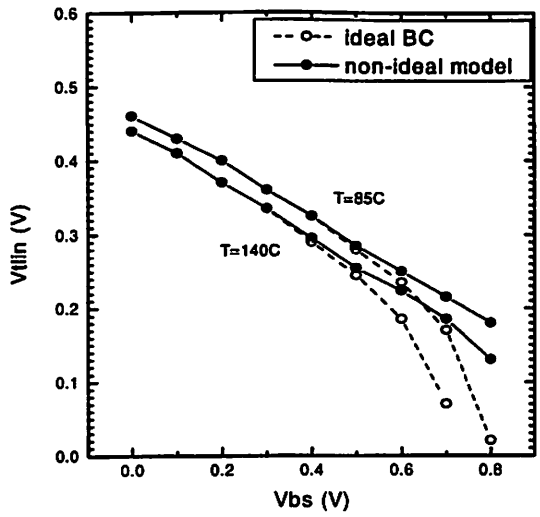


Figure 2-24. I_{dlin} (I_{ds} @ $V_{gs} = V_{dd}$, $V_{ds} = 0.05$ V) and I_{dsat} (I_{ds} @ $V_{gs} = V_{dd}$, $V_{ds} = V_{dd}$) versus V_{bs} showing the importance of body-contact model in the high body-bias regime.

Figure 2-24 shows that the drain current at high V_{bs} is much lower than what the ideal body-contact simulation predicts (steep increase). It is mainly due to the IR drop of body potential caused by the forward-biased diode current flowing through the distributed body resistance. Since the diode current increases with temperature, the discrepancy becomes larger at 140°C. It can be seen that the simulation result agrees very well with the measurement data after considering the non-ideal body-contact effect.

Figure 2-25 shows the correction of the threshold voltage in the high body-bias regime made by the non-ideal body-contact model. As expected, the threshold voltage drops much more slowly and smoothly in the non-ideal case. This implies that the ideal body-contact assumption in parameter extraction may lead to a wrong body-effect (V_T as a function of V_{bs}) prediction, which is crucial to the noise margin of the pass-gate and dynamic logic design.



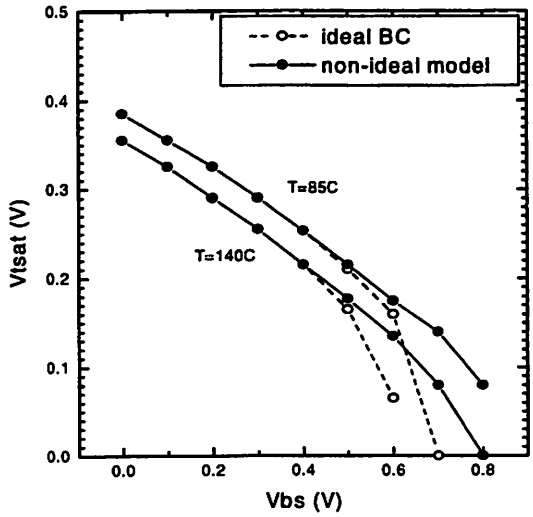


Figure 2-25. V_{tlin} (V_T @ $V_{gs} = V_{dd}$, $V_{ds} = 0.05$ V) and V_{tsat} (V_T @ $V_{gs} = V_{dd}$, $V_{ds} = V_{dd}$) versus V_{bs} showing the significant threshold-voltage roll-off in the high body-bias regime without considering the non-ideal body-contact effect.

Impact on Performance Prediction:

Figure 2-26 shows the impact of the non-ideal body-contact effect on the transistor switching speed. Due to the parasitic capacitances caused by A_{gbcp}/A_{ebcp}, and the extra junction charges induced by P_{sbcp}/P_{dbcp}, the speed performance of an inverter gate is approximately degraded by 30% in this case.

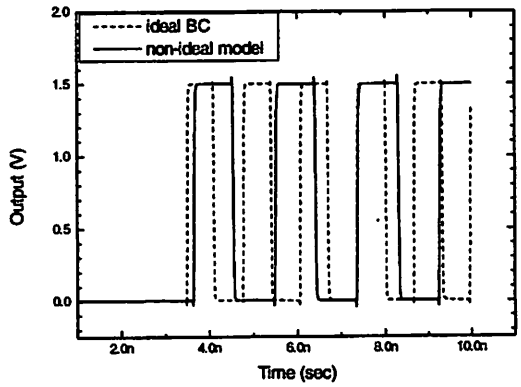


Figure 2-26. The output waveforms of an unloaded 51-stage ring oscillator showing the optimistic performance-prediction made by the ideal body-contact assumption. The error of switching speed is around 30% in this case.

In conclusion, since the body-contact is widely used in not only critical circuit design but also test structures for parameter extraction, a compact SOI body-contact model which can accurately capture the body potential is crucial to the accuracy of circuit simulation. A body-contact model, including layout-dependent parasitic diodes and capacitances, as well as an accessible body node for high-precision segmented-transistor simulation, has been developed and implemented in BSIMPD. The impact of the non-ideal body-contact effect on the device parametrics and performance are also investigated based on this model.

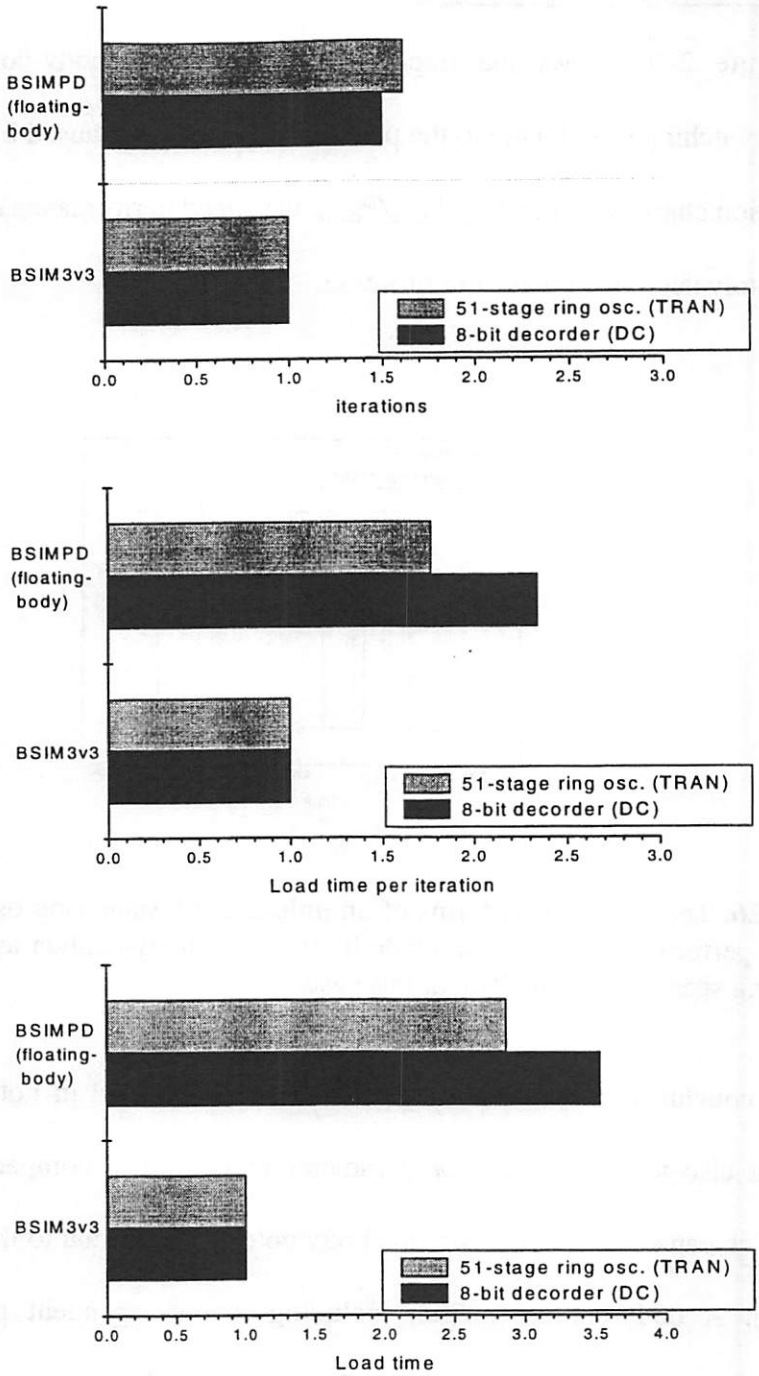


Figure 2-27. Comparison of simulation efficiency between BSIMPD and BSIM3v3 performed by Berkeley SPICE3f4.

2.5 Simulation Efficiency

Efficiency in circuit simulation impacts the productivity of circuit designers, and therefore is one important performance metric to a device model. To investigate the simulation efficiency of BSIMPD, two benchmark circuits: a 8-bit decorder and a 51-stage ring oscillator are employed to assess the model performance in DC and transient operation, respectively. As shown in Figure 2-27, the run-time statistics obtained from Berkeley SPICE3f4 are normalized based on the results of BSIM3v3 bulk model. The ~1.5X total iteration number (convergency) of BSIMPD originates from the stiff nature of the long floating-body time constant. While the ~2X load time per iteration (complexity) of BSIMPD is mainly due to the complex equations (e.g., exponential function) utilized in modeling the various body current components. The overall load time (efficiency) of the floating-body simulation is around 3X compared with the bulk BSIM3v3 model.

2.6 Summary

A physics-based partially-depleted SOI MOSFET model has been developed to support deep-submicron CMOS designs for SOI technologies of the 21st century. Based on the industry-standard BSIM3v3 bulk model, BSIMPD models the PDSOI-specific floating-body, self-heating and body-contact effects. This model is able to capture the various dynamic behaviors in the PDSOI circuitry by the floating-body simulation.

BSIMPD has been tested extensively within IBM on state-of-the-art high speed SOI technologies [6][16][19]. The accuracy of BSIMPD has also been verified by other semiconductor companies [17][18]. The average error of drain current at all bias conditions is comparable to what is normally achieved for bulk technologies [16]. This model has been implemented in Berkeley SPICE3f4 as well as many commercial circuit simulators such as HSPICE, SPECTRE, SmartSPICE and ELDO. Finally, BSIMPD was selected by the EIA Compact Model Council (CMC) [15] as the standard SOI MOSFET model in December 2001 after a year-long evaluation process.

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Chapter 3

Impact Ionization in Deep-Submicron MOSFETs

3.1 Introduction

Impact ionization current (I_{II}) plays an important role in the determination of the floating-body behavior of partially-depleted SOI MOSFETs. In addition, it has been suggested that the impact ionization current remains crucial even for double-gate SOI MOSFETs by enhancing the subthreshold leakage [1]. Therefore, a physical understanding and modeling of the impact ionization phenomenon in state-of-the-art SOI devices is critical to a standard SOI MOSFET model.

I_{II} has long been closely related to the maximum channel electric field, E_m, near the drain [2]. According to the classical model, the probability that a carrier will gain sufficient energy to cause impact ionization without suffering any scattering in the channel is $\exp(-\Phi_i/q\lambda E_m)$, where Φ_i is the energy required for impact ionization, and λ is

the mean free path. With the scaling of channel length and supply voltage, nevertheless, I_{II} may be determined by other non-scalable factors. Therefore, the classical carrier-phonon scattering mean-free path concept has difficulty in modeling the temperature, gate bias and drain bias dependence of the impact ionization rate.

In this chapter, we first demonstrate an observation of enhanced substrate currents in SOI MOSFETs [3]. The implications are presented subsequently. We then unveil the underlying mechanism using the *thermal activation energy* concept [4]. Finally, we present a compact impact ionization model for SOI circuit simulation based on the proposed thermal activation energy theory.

3.2 Self-Heating Enhanced Substrate Current

As SOI CMOS offers an alternative to bulk technology for device scaling, the hot-carrier effect that increases with device miniaturization is another important scaling issue that has to be considered for SOI MOSFETs. The hot-carrier effect is usually monitored by the substrate current (I_{SUB}) [2]. I_{SUB} results from impact ionization caused by energetic carrier in the channel. The impact ionization current may charge up the transistor body and vary the threshold voltage if the body charge is not readily dissipated. Therefore, measured I_{SUB} data from body-contacted devices also plays a crucial role in modeling the current drive of floating-body SOI MOSFETs [5][6].

I_{SUB} has long been closely related to the high channel electric field near the drain [2]. Accordingly, electric field has always been a main gauge of hot-carrier effects when

one-to-one comparisons between SOI and bulk devices are made [7]. With the scaling of channel length and supply voltage, however, a new source other than electric field for carrier heating may be present and may determine impact ionization. In this work, we demonstrate an enhanced I_{SUB} phenomenon in SOI MOSFETs. We describe the underlying physical mechanism and explain why this phenomenon affects the hot-carrier lifetime prediction as well as SOI modeling.

Co-processed bulk and body-contacted partial-depletion SOI MOSFETs using a 0.13 μm technology [8] are investigated in this study. For SOI, the thicknesses of the gate oxide, silicon film and buried oxide are 2.8 nm, 100 nm and 360 nm, respectively. Note that although all date shown in this paper are for PFETs, NMOS behave similarly, but with all voltages at opposite polarity.

Figure 3-1(a) shows that the substrate current in the SOI MOSFET is larger than the bulk counterpart at high gate bias. The impact-ionization rate defined as the ratio of the substrate current to the drain current, I_{SUB}/I_D, may be used to understand the underlying mechanism. As shown in Figure 3-1(b), the identical I_{SUB}/I_D at low gate bias demonstrates that the co-processed bulk and SOI samples are nearly identical. As gate bias increases, however, the impact-ionization rate of the SOI MOSFET becomes larger than the bulk one.

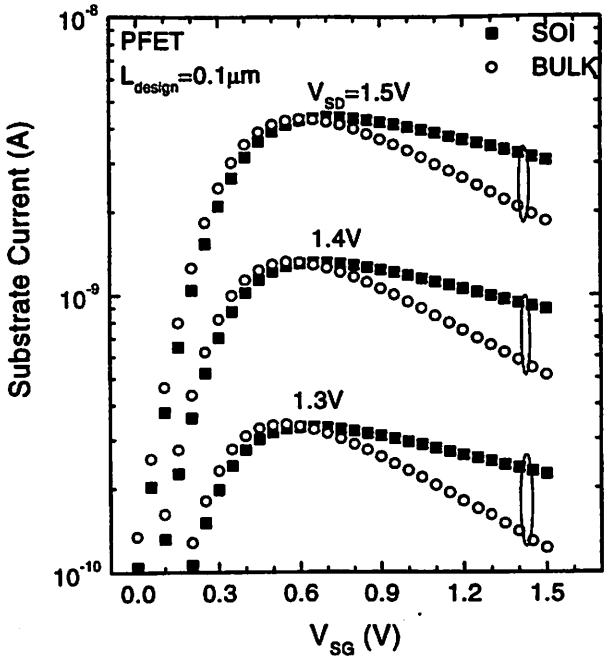

Figure 3-1(a). Larger substrate current is observed for the SOI transistor at high gate bias.

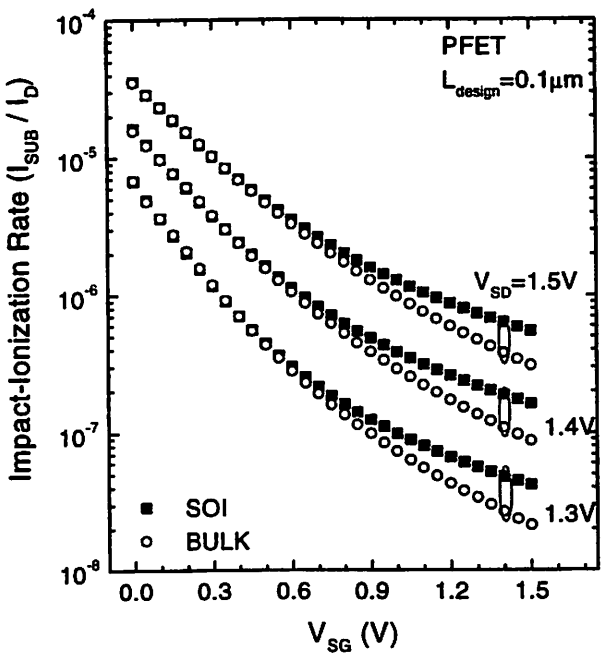

Figure 3-1(b). The impact-ionization rate of the SOI MOSFET is larger than the bulk counterpart at high gate bias, even though the two transistors are nearly identical.

As gate bias increases, the power and therefore the device temperature of the SOI MOSFET rises due to self-heating [9], a consequence of the low thermal conductivity of buried oxide (about two orders of magnitude less than that of silicon). In Figure 3-2 we show measured temperature dependence of the impact-ionization rate for both bulk and SOI devices by varying the substrate temperature using a variable temperature chuck. The increase of I_{SUB}/I_D with temperature explains the phenomenon observed in Figure 3-1. *The SOI-specific self-heating effect provides a source for carrier heating in the channel and enhances impact ionization.*

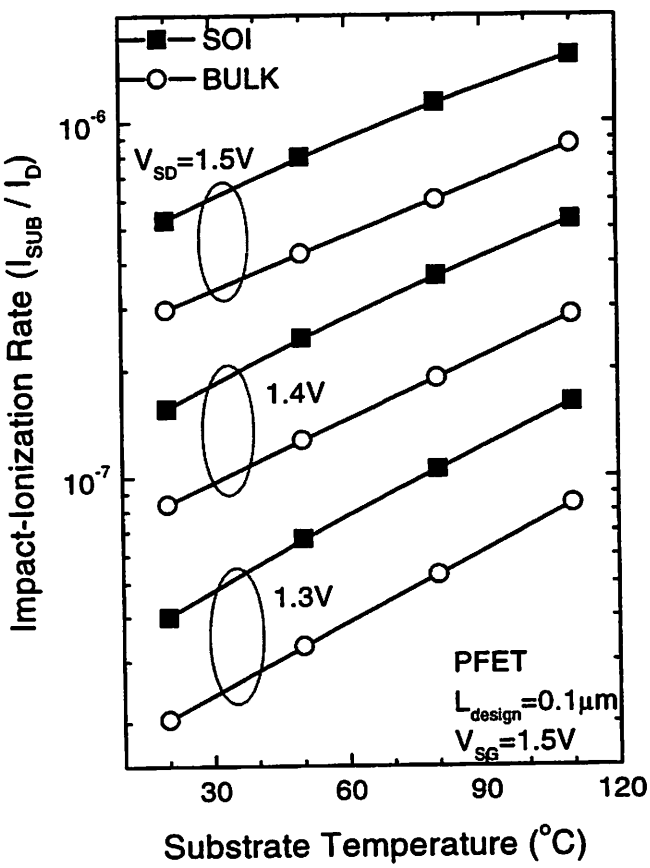

Figure 3-2. The impact-ionization rate increases as temperature rises. This explains the self-heating enhanced substrate current occurring at high gate bias in the SOI MOSFET.

The temperature rise (ΔT) due to self-heating in SOI devices is linear proportional to the static power dissipation with a slope, which can be interpreted as a thermal resistance from the channel to the chuck [9]. Since a larger current drive gives bigger power consumption, for a given technology the temperature rise and therefore the I_{SUB}/I_D enhancement is more significant for the SOI MOSFET with shorter channel length, as shown in Figure 3-3. For a given bias and substrate temperature (T_0), the SOI device temperature and thus ΔT can be projected by finding the corresponding temperature which gives the same amount of impact-ionization rate in the bulk device as illustrated in Figure 3-3. In this experiment, ΔT_1 and I_{D1} for the 0.12 μm device are 30 °C and 1.84 mA, respectively, while ΔT_2 and I_{D2} for the 0.1 μm device are 46 °C and 2.77 mA, respectively. The equivalence between the extracted $\Delta T_1/\Delta T_2$ and the measured I_{D1}/I_{D2} proves that the self-heating effect is indeed responsible for the excess substrate current in the SOI MOSFET.

The self-heating enhanced impact ionization present in DC bias conditions will be absent in most logic circuits. Since the average power consumption per device is low and its switching time (~10 ps) is much shorter than the thermal time constant (~100 ns) [7][8] for state-of-the-art high performance SOI CMOS, the time-averaged and transient device-temperature rises due to self-heating are quite small. For example, considering a chip with power consumption of 10 W, 10 million transistors, and thermal resistance of 10^4 °C/W, the average device temperature increase can roughly be estimated as 0.01 °C and negligible. Therefore, *extrapolating device dynamic lifetime by use of static lifetime,*

a common practice in hot-carrier reliability stress testing, will underestimate the actual lifetime of SOI MOSFETs in most logic circuits [9].

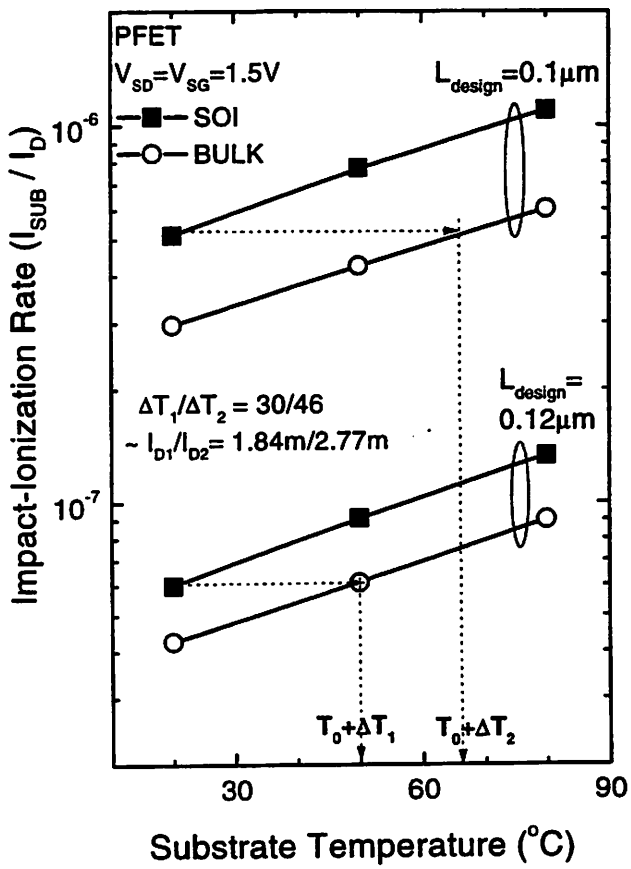

Figure 3-3. The I_{SUB} enhancement is more pronounced for the SOI MOSFET with shorter channel length. The SOI temperature rise (ΔT) due to self-heating can be projected by finding the corresponding temperature which gives the same amount of impact-ionization rate in the bulk counterpart. The equivalence of $\Delta T_1/\Delta T_2$ and I_{D1}/I_{D2} proves self-heating is responsible for the excess substrate current observed in the SOI MOSFET.

Similarly, the DC I_{SUB} data measured from body-contacted SOI MOSFETs may not represent the dynamic impact-ionization charging characteristics of rapidly switching floating-body devices in a digital circuit due to this effect. Self-heating-free I_{SUB} data, in

addition to heating-free I_D data [10]-[12], should be used and modeled for accurate logic circuit simulation. As shown in Equation (3-1),

$$I_{SUB,non-selfheated} = I_{SUB,DC} - \frac{\Delta I_{SUB,DC}}{\Delta T} R_{th} I_{DS} V_{DS} \qquad (3\text{-}1),$$

non-self-heated I_{SUB} characteristics can be reconstructed by establishing the device-temperature dependence of the substrate current for each bias point. Device temperature can be calculated by (T_0 + thermal resistance × power). Thermal resistance can be measured by several methods such as the poly gate resistance method [10], pulse measurement [11] and the AC output conductance method [12]-[14]. As shown in Figure 3-4, the constructed self-heating-free I_{SUB} characteristics using this approach agree well with bulk data. It can be clearly seen that the SOI device temperature and DC I_{SUB} data increase significantly at high gate bias.

The self-heating enhanced I_{SUB} phenomenon stems from the increase of the impact-ionization rate with temperature at low drain bias (Figure 3-2) [15][16], which contradicts the classical electron-phonon scattering mean-free path concept [17]. Further, for a given high gate bias this I_{SUB} enhancement does not decrease with the supply drain voltage ($\propto$ power $\propto \Delta T$), as demonstrated in Figure 3-1. It means that the temperature sensitivity of the impact-ionization rate actually increases as the drain bias decreases. Several explanations regarding the temperature dependence of the impact-ionization rate in the low drain bias regime were proposed in the past, including quasi-ballistic transport characteristics performed by deep-submicrometer devices [18]-[20], temperature-

dependent bandgap energy [18][19] and the memory effect [20]. This issue, nevertheless, deserves further experimental study and will be addressed in the next section.

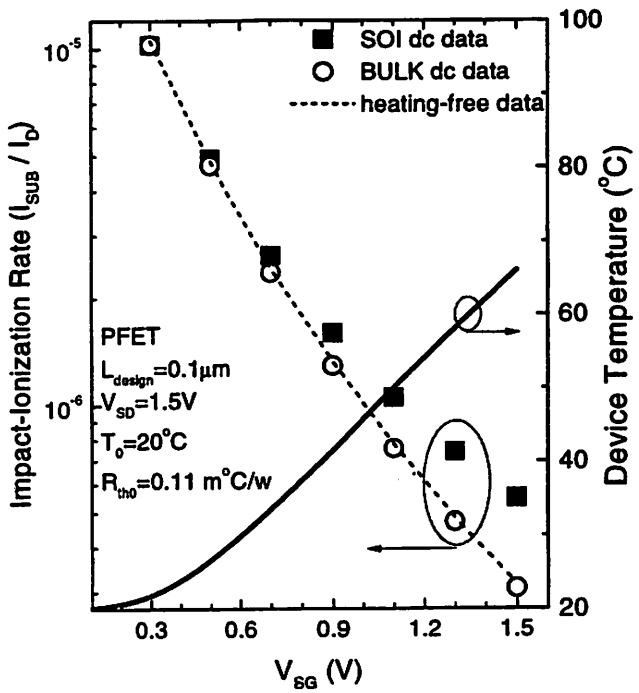

Figure 3-4. The SOI device temperature can be calculated by thermal resistance (R_{th0}) and used for the reconstruction of self-heating-free I_{SUB} characteristics, which should be modeled for most logic-circuit applications.

In conclusion, we report an enhanced substrate current phenomenon in state-of-the-art SOI MOSFETs. Due to self-heating, excess impact ionization is induced for the SOI transistor biased at high gate DC voltage. Since the temperature rise does not follow the instantaneous power dissipation under dynamic operating conditions typical of digital circuit operation, self-heating-free I_{SUB} characteristics should be reconstructed and used for the SOI dynamic lifetime prediction as well as circuit simulation of floating-body devices. This effect should also be taken into account when comparisons between SOI and bulk MOSFETs regarding hot-carrier effects are made.

3.3 A Thermal Activation View of Low Voltage Impact Ionization in MOSFETs

As the MOSFET dimensions and the power-supply voltage (V_D) are continuously scaled down, the hot-carrier effect that increases with device miniaturization is an important issue that demands further investigation at low supply voltages. The hot-carrier effect is usually monitored by the substrate current (I_{SUB}) [2] that results from impact ionization caused by energetic carrier in the channel. Previous report [3] on the self-lattice-heating enhanced substrate current, a manifestation of the increased impact-ionization rate (I_{SUB}/I_D) with lattice temperature at low drain bias [15][16], contradicts the classical carrier-phonon scattering mean-free path concept [17][21].

This paradoxical result casts some doubt on the understanding of the hot-carrier effect and the prediction of the long-term reliability of MOSFETs. Therefore, a great deal of Monte Carlo simulations concerning the temperature dependence of the impact-ionization rate in the low drain bias regime near the silicon bandgap were carried out in the past [7]-[9]. Several explanations have been proposed, including quasi-ballistic transport characteristics performed by deep-submicrometer devices [18]-[20], temperature-dependent bandgap energy [18][19], and the memory effect [20].

However, there has been little experimental assessment on the mechanisms responsible for low voltage impact ionization in state-of-the-art deep-submicrometer MOSFETs. In this work, we present a thermal activation perspective for impact ionization at low drain bias. By directly tackling the measured I_{SUB} data based on the

thermal activation viewpoint, we demonstrate the role lattice temperature plays in determining low voltage impact ionization experimentally.

The deep-submicrometer bulk MOSFETs used in this study were fabricated using a 0.13 μm technology [3][8][22][23]. The electrical oxide thickness is 2.8 nm. The test devices have a physical gate length of 0.08 μm and 0.1 μm for NMOS and PMOS, respectively. The substrate currents were measured at various substrate temperatures using a variable temperature chuck. The temperature range (20 °C < T < 170 °C) examined in this work is of special interest to high performance applications.

Figure 3-5 shows measured I_{SUB}/I_D versus reciprocal temperature for the PFET. It demonstrates that I_{SUB}/I_D increases with temperature. After we carefully subtract the junction leakage that may affect the measurement accuracy of impact ionization current at low drain bias (e.g. V_{SD} = 0.8 V) and high temperature, a linear relationship between $\log(I_{SUB}/I_D)$ and reciprocal temperature can be observed in Figure 3-5. This Arrhenius behavior reveals the thermally assisted nature of impact ionization at low drain bias. As depicted in Figure 3-5, the slope of the Arrhenius plot determines the activation energy, E_a, of the underlying mechanism and is plotted against the drain bias in Figure 3-6. Notice that E_a increases as the drain bias decreases.

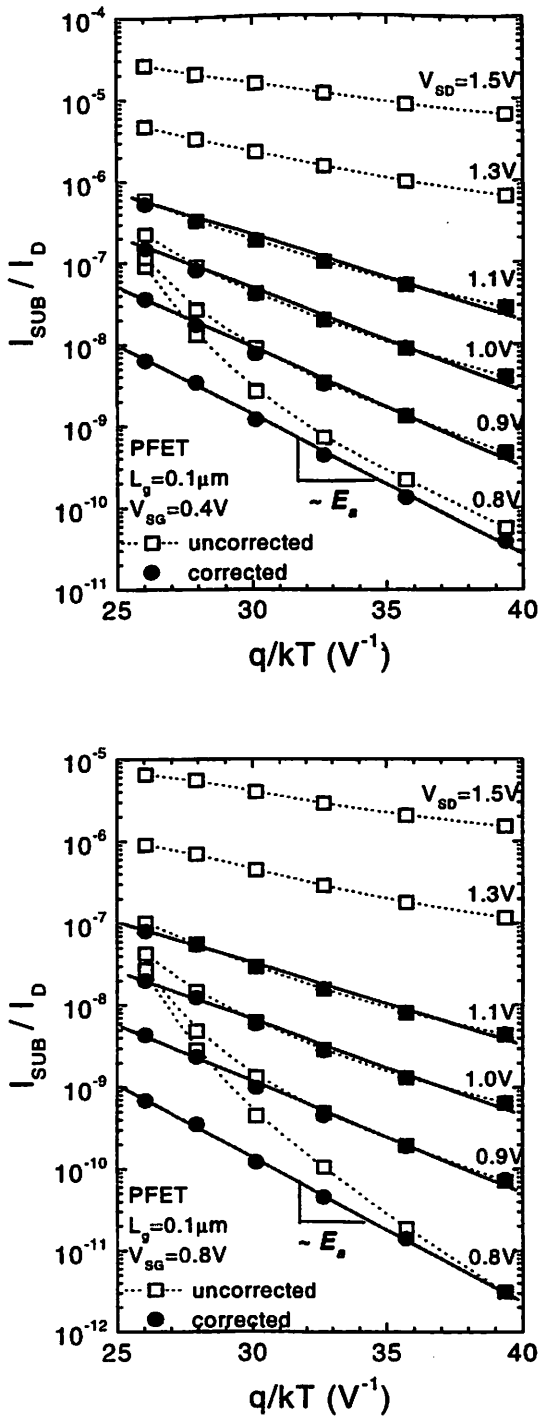

Figure 3-5. Measured I_{SUB}/I_D versus reciprocal temperature at $V_{SG} = 0.4$ V and $V_{SG} = 0.8$ V, respectively, for the PFET demonstrating the Arrhenius behavior of low voltage impact ionization. Junction leakage was carefully subtracted at each bias and temperature based on $\log(I_{SUB})$ versus V_{SD} characteristics.

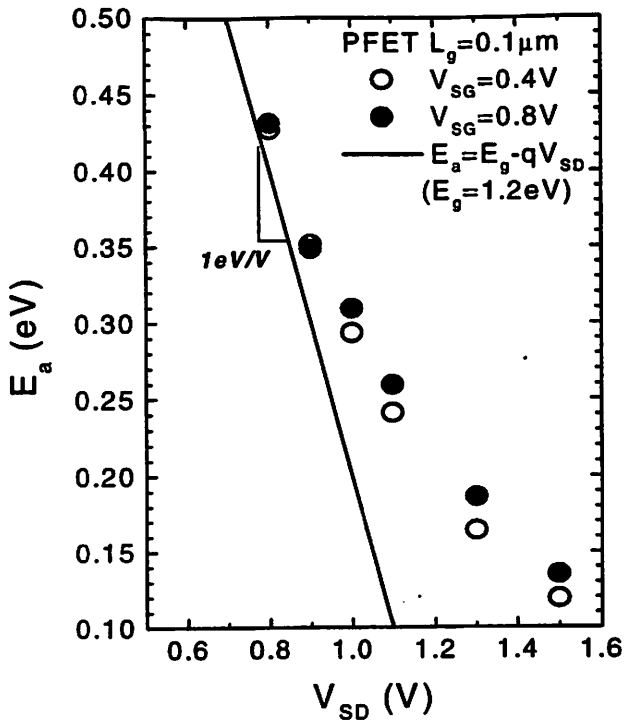

Figure 3-6. Activation energy versus V_D for the PFET demonstrating that the driving force of impact ionization is in a transition from the electric field to the lattice temperature with the power-supply scaling.

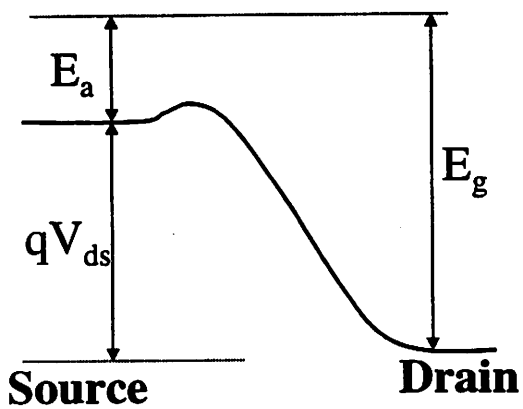

Figure 3-7. Band diagram showing for an electron traveling from the conduction band edge at the source to the drain, an additional energy is required to cause impact ionization.

As depicted in Figure 3-7, the activation energy can be interpreted as the energy in excess of that provided by the supply for the carrier traveling from the source to the drain. In the ballistic limit, $E_a = E_g - qV_D$ ($E_g \sim 1.2$ eV [24][25]) is the extra energy that must be acquired from the lattice for the carrier to cause impact ionization. As shown in Figure 3-6, the experimentally determined activation energy approaches this theoretical prediction as V_D is scaled down (notice the approach of the 1 eV/V theoretical limit of $\Delta E_a/\Delta V_D$). It indicates that *the driving force of impact ionization transitions from the electric field to the lattice temperature with power-supply scaling below 1.2 V.*

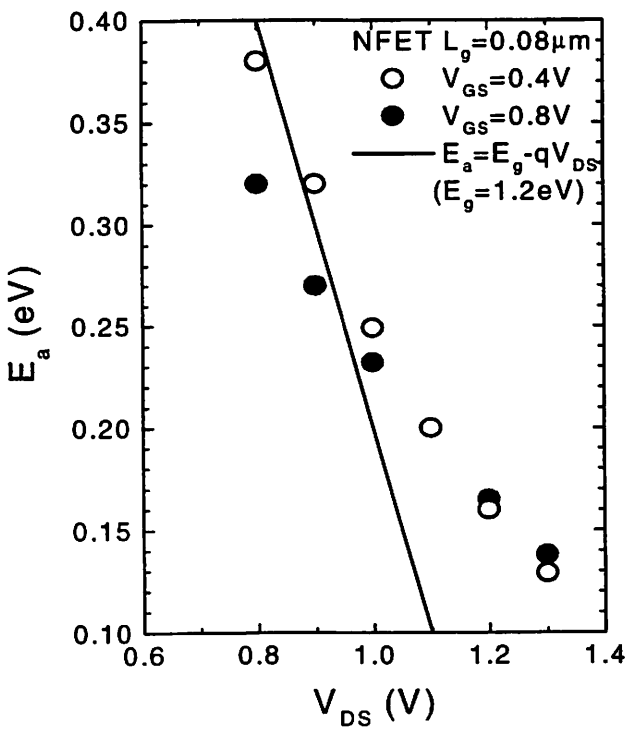

Figure 3-8. Activation energy versus V_D for the NFET demonstrating the signature of other energy gain mechanisms for low voltage impact ionization based on the activation energy lowering (e.g., $V_{GS} = 0.8$ V).

This thermal activation view also provides a way to experimentally monitor other energy gain mechanisms that may cause impact ionization at sub-bandgap drain bias. As shown in Figure 3-8, the measured activation energy for the NFET at V_{GS} = 0.4 V still follows the simple $E_a = E_g - qV_D$ model as V_D is scaled down. At V_{GS} = 0.8 V, nevertheless, the experimentally determined activation energy is smaller than the theoretical prediction at sub-bandgap drain bias, where other energy gain mechanisms play roles in the determination of impact ionization. It has been proposed [18][26][27] that electron-electron scattering may provide an additional source for carrier heating in the channel and enhance impact ionization at sub-bandgap drain bias. Notice that raising the gate bias (e.g. from 0.4 V to 0.8 V), and thus the channel electron concentration, causes a higher electron-electron scattering rate. In other words, the Arrhenius behavior of low voltage impact ionization may be shadowed by electron-electron scattering (especially at high gate bias) as shown in Figure 3-9.

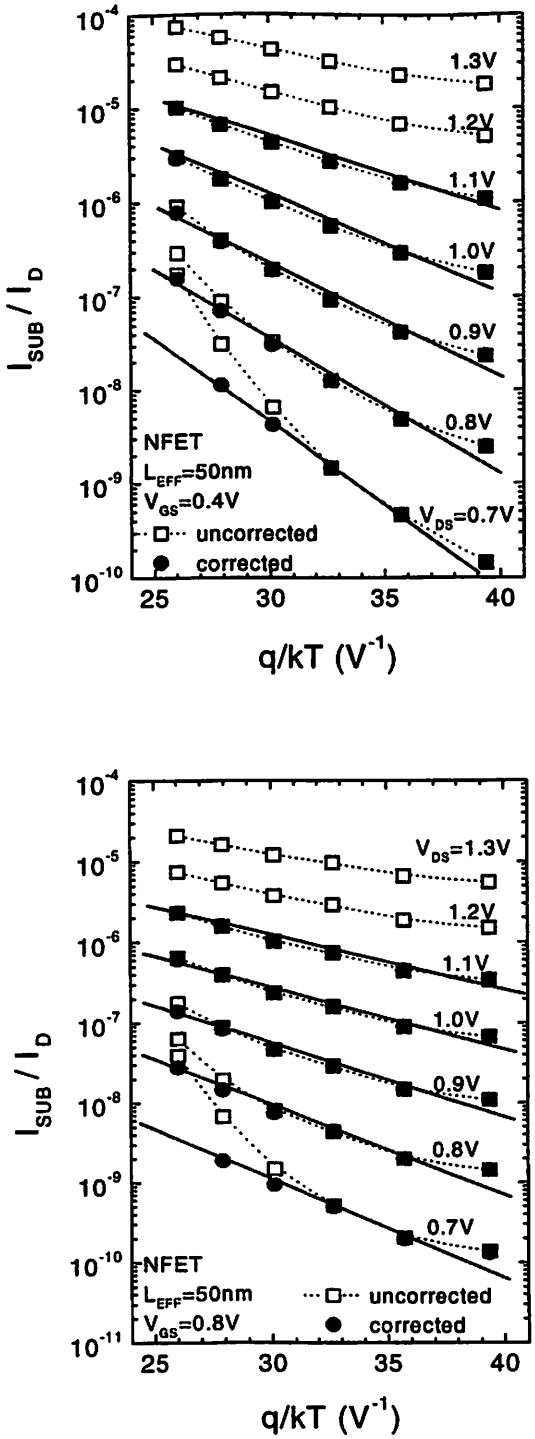

Figure 3-9. Measured I_{SUB}/I_D versus reciprocal temperature at $V_{GS} = 0.4$ V and $V_{GS} = 0.8$ V, respectively, for the NFET. The junction leakage has been subtracted.

The thermally-assisted impact ionization model ($I_{SUB}/I_D \sim \exp(-(E_g - qV_D) / kT)$) predicts a linear relationship between $\log(I_{SUB}/I_D)$ and V_D at sub-bandgap drain bias, as verified in Figure 3-10. Recall that the drain bias dependence of $\log(I_{SUB}/I_D)$ has been previously modeled as $-1/V_D$ [2] under the maximum electric field framework. The transition of driving force for impact ionization as V_D is scaled down, therefore, changes the drain bias dependence of the impact-ionization rate. This effect is crucial to accurate modeling of the MOSFET output characteristics, especially the SOI floating-body charging phenomenon [5], for low voltage applications. In addition, the gap of the drain bias dependence of the impact-ionization rate may potentially lower the accuracy of the long-term lifetime extrapolation based on the accelerated hot-carrier stressing. This issue deserves further experimental study in the future.

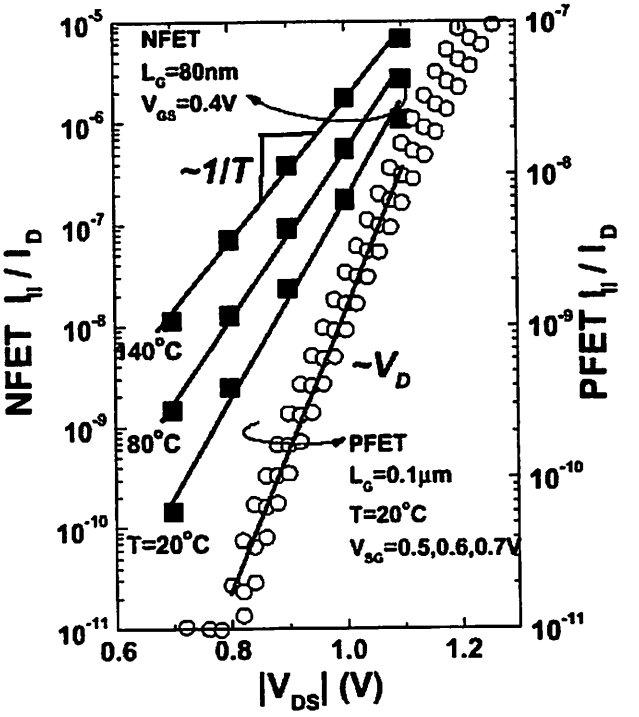

Figure 3-10. V_D dependence of the ionization rate at sub-bandgap drain bias.

In conclusion, we provide a thermal activation view of the low voltage impact ionization in deep-submicrometer MOSFETs. Based on this perspective, we experimentally assess the role lattice temperature plays in the determination of low voltage impact ionization. Our experimental result, the Arrhenius I_{SUB}/I_D behavior characterized by the lattice temperature at sub-bandgap drain bias, indicates that the main driving force of impact ionization is changing from the electric field to the lattice temperature with power-supply scaling below 1.2 V. This transition of driving force results in a linear relationship between $\log(I_{SUB}/I_D)$ and V_D at sub-bandgap drain bias, as predicted by the proposed thermally-assisted impact ionization model.

3.4 An Impact Ionization Model for SOI Circuit Simulation

Beside the hot-carrier reliability, impact ionization current (I_{II}) plays an important role in the determination of the SOI floating-body behavior. It was suggested that the I_{II} remains crucial even for double-gate MOSFETs by enhancing the subthreshold leakage [1]. An observation (Figure 3-11) shows that the onset of kink for state-of-the-art SOI devices is well below the silicon bandgap (E_g ~ 1.2 eV). The underlying low voltage ionization mechanism cannot be explained by the conventional wisdom of impact ionization driven by electric field. Based on the thermal activation energy theory [4] proposed in the previous section, we present a compact impact ionization model for SOI circuit simulation [28].

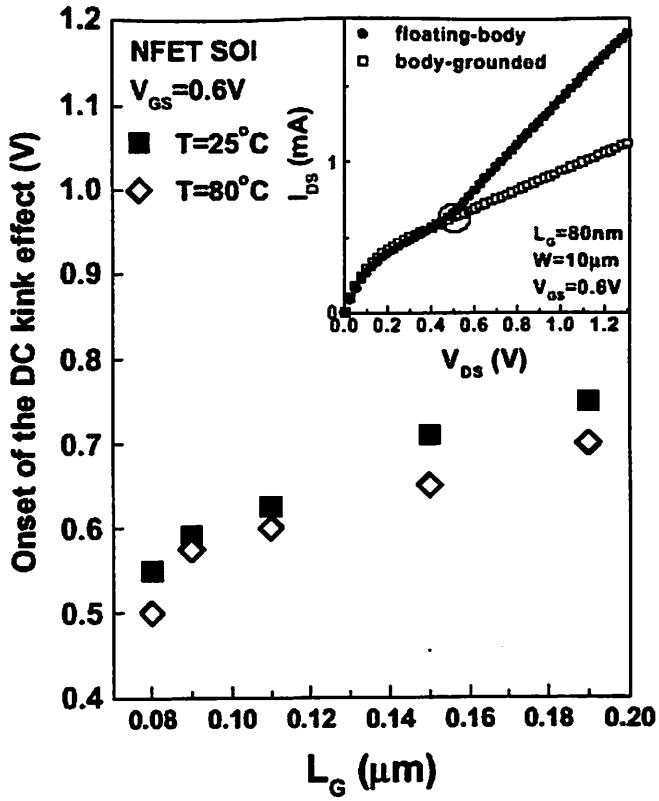

Figure 3-11. Onset voltage of the IV kink (inset) vs. gate length for a 0.13μm SOI technology.

According to our thermal activation energy theory [4], the cause of the sub-bandgap drain-voltage impact ionization and thus kink effect in SOI MOSFETs is attributed to the lattice temperature. In addition, thermally-assisted impact ionization in SOI MOSFETs cannot be considered alone, but together with self-heating. The impact ionization current versus gate voltage has been shown in Figure 3-1, indicating an increase of ionization rate at high gate bias due to self-heating [29]. The observation further confirms the thermal nature of the extra impact ionization current.

From the thermally-assisted impact ionization model [4], impact ionization current can expressed by

$$I_{II}/I_D \sim \exp(-(E_g - qV_D) / kT) \qquad (3\text{-}2).$$

Equation (3-2) predicts a linear relationship between $\log(I_{II}/I_D)$ and V_D in the sub-bandgap drain voltage, and has been verified in Figure 3-10. Recall that under the maximum electric field framework, $\log(I_{II}/I_D)$ has been previously modeled to vary with $-1/V_D$ [2], which is still applicable at high V_D. At some intermediate V_D, the dominant mechanism for impact ionization changes from electric-field driven to thermally driven. To capture both effects and their relative strength, the impact ionization current as a function of drain voltage can be modeled by the following unified expression:

$$I_{II}/I_D \sim \exp(V_D / (\beta_0 + \beta_1 V_D + \beta_2 V_D^2)) \qquad (3\text{-}3),$$

where β_0, β_1 and β_2 are model parameters [30]. The V_D dependence of this expression approaches the thermally-assisted model (Equation (3-2)) at low V_D, while returns to the classical model (i.e., $-1/V_D$) at high V_D.

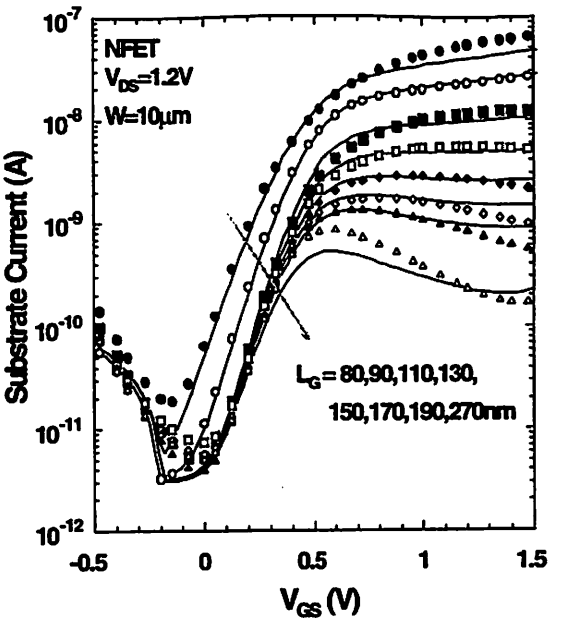

Figure 3-12. Substrate current fitting at $V_D=E_g/q$. Symbols are measurement and lines are simulation.

The accuracy of the model has been verified by experimental data. Figure 3-12 shows the fitting of the substrate current data of SOI MOSFET with different dimension and bias condition showing the accuracy of the proposed model at $V_D=E_g/q$. After including the thermally-assisted impact ionization current into the substrate current calculation, the body voltage can be correctly calculated using the floating-body model in BSIMPD [5][30], and the low voltage kink in the output characteristics of SOI transistors can be correctly captured as shown in Figure 3-13.

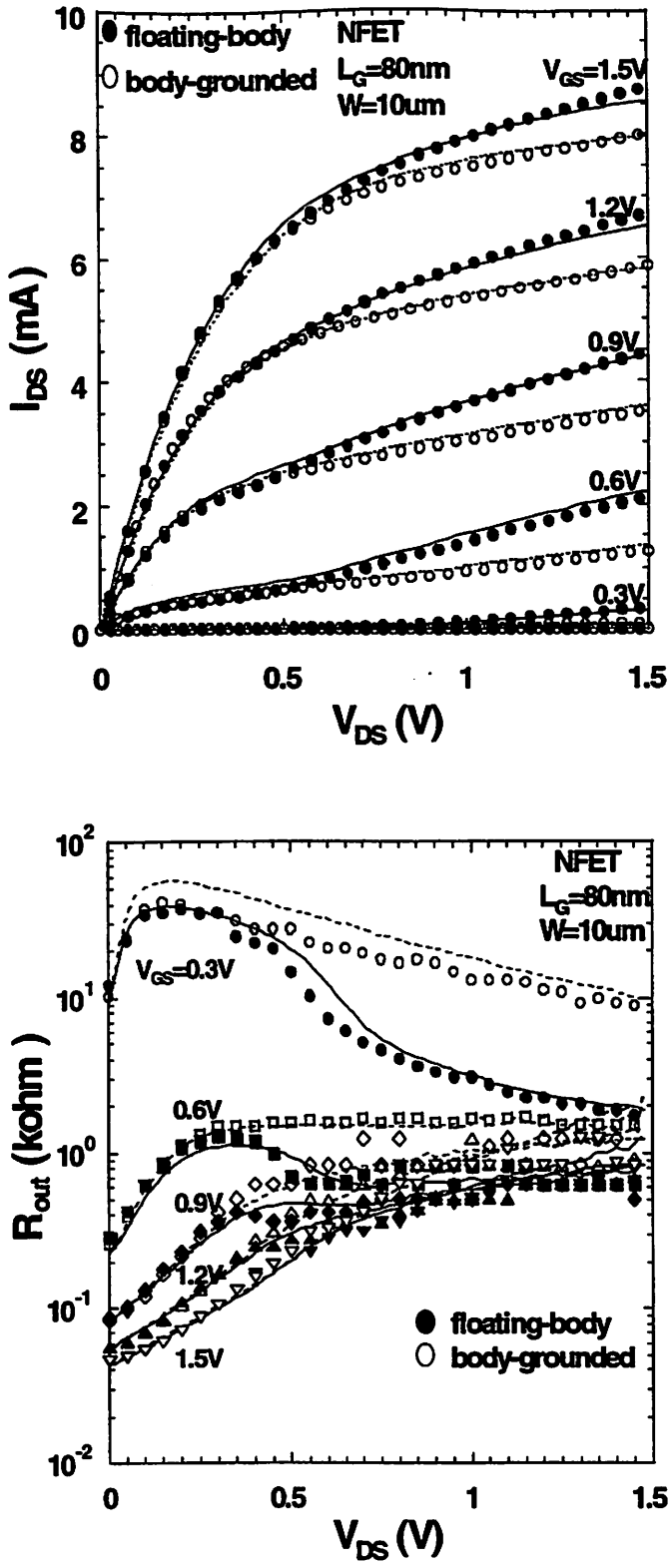

Figure 3-13. BSIMPD accuracy in modeling the SOI output characteristics. Symbols are measurement and lines are simulation.

3.5 Summary

In this chapter we discuss the mechanism responsible for low voltage impact ionization in deep-submicrometer MOSFETs. Our study indicates that the driving force of impact ionization transitions from the electric field to the lattice temperature with power-supply scaling below 1.2 V. Due to its thermally assisted nature, the ionization rate in self-heated SOI MOSFETs is enhanced at high gate DC bias. This effect needs to be considered in SOI modeling as well as hot-carrier reliability due to the gap between the fast logic switching and the long thermal time constant. The low voltage impact ionization behavior can be predicted by the proposed thermal activation energy theory, which also explains the sub-bandgap kink in SOI out characteristics. In addition, a compact model has been developed based on the thermal activation energy theory to capture the SOI device characteristics with both thermally assisted impact ionization and electric field induced impact ionization accounted for. This model has been implemented in BSIMPD [5][30].

3.6 References

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Chapter 4

Impact of Gate-Body Tunneling on SOI CMOS

4.1 Introduction

In this chapter, we study the SOI floating-body behavior with emphasis on the impact of gate tunneling, which is becoming increasingly important with oxide thickness scaling below 25 Å. We first demonstrate the key to capturing the SOI history effect in SPICE modeling. The accuracy of BSIMPD regarding history effect is also addressed. Then we investigate the impact of gate-body tunneling on dynamic behaviors of Partially-Depleted (PD) SOI CMOS with the aid of BSIMPD [1][2]. Finally, we discuss the tendency toward full depletion [3] due to gate-body tunneling, which has important implication for scaled SOI CMOS with supply voltage below 1 V.

4.2 History Effect Modeling in BSIMPD

As mentioned in Chapter 2, the main barrier to the acceptance of PD SOI by circuit designers is the requirement of careful analysis for the impact of floating body effects on individual blocks [4]-[7]. Due to the self-biasing of the floating body, PD SOI circuits present idiosyncratic dynamic behaviors (e.g. history and frequency dependence of switching speed) that may increase the risk of inadequate circuit designs.

The origin of SOI dynamic behaviors is the history dependence [8]-[10] of the floating body potential. Since the time constant of body charging is different for capacitive coupling, thermal generation and recombination, gate-induced-drain-leakage (GIDL), impact ionization [11], and oxide tunneling, the circuit representation of the floating body in Figure 2-1 is used in BSIMPD to capture the dynamic behavior of SOI.

Figure 2-1 shows various body leakages and displacement currents that determine the floating-body potential. As shown in the nodal equation at the body,

$$\left(\frac{dQ_G}{dt}+\frac{dQ_{bG}}{dt}+\frac{dQ_D}{dt}+\frac{dQ_S}{dt}\right) + (I_{II}+I_{GIDL}+I_{BS}+I_{BD})+I_{GB}=0 \qquad (4\text{-}1),$$

the SPICE solution of the differential equation at the body node depends not only on the present terminal voltages, but also on the initial condition of the body charge (past history). For example, if two input signals, one starting from DC GND and one from V_{dd},

are applied sequentially to a CMOS inverter, the SPICE-solved body potential of the pull-down device (NFET) and therefore falltime delay will depend on the initial condition of the input signal and vary with time, as shown in Figure 4-1. This demonstrates the need of a floating-body node for SPICE to simulate the history effect.

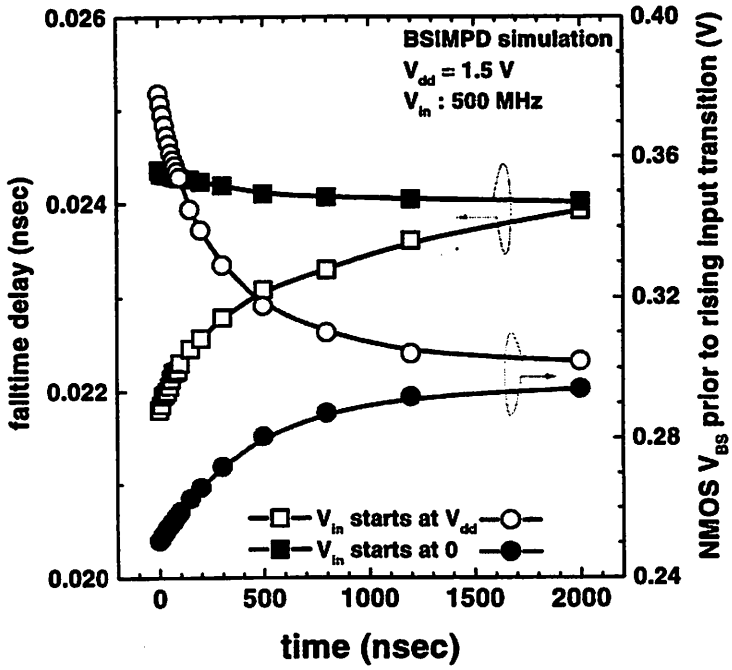


Figure 4-1. The switching speed of an SOI CMOS inverter depends on the initial condition of input signal and varies with time due to floating body.

It is clear from Equation (4-1) that the key to capturing the history effect is an accurate modeling of every body current and charge component. It has been shown (Figure 4-2) that BSIMPD can be used to accurately simulate the history effect [12]. Notice that in Figure 4-2 the history effect is defined as the delay range between the first and second switch, which will be further illustrated in the next section.

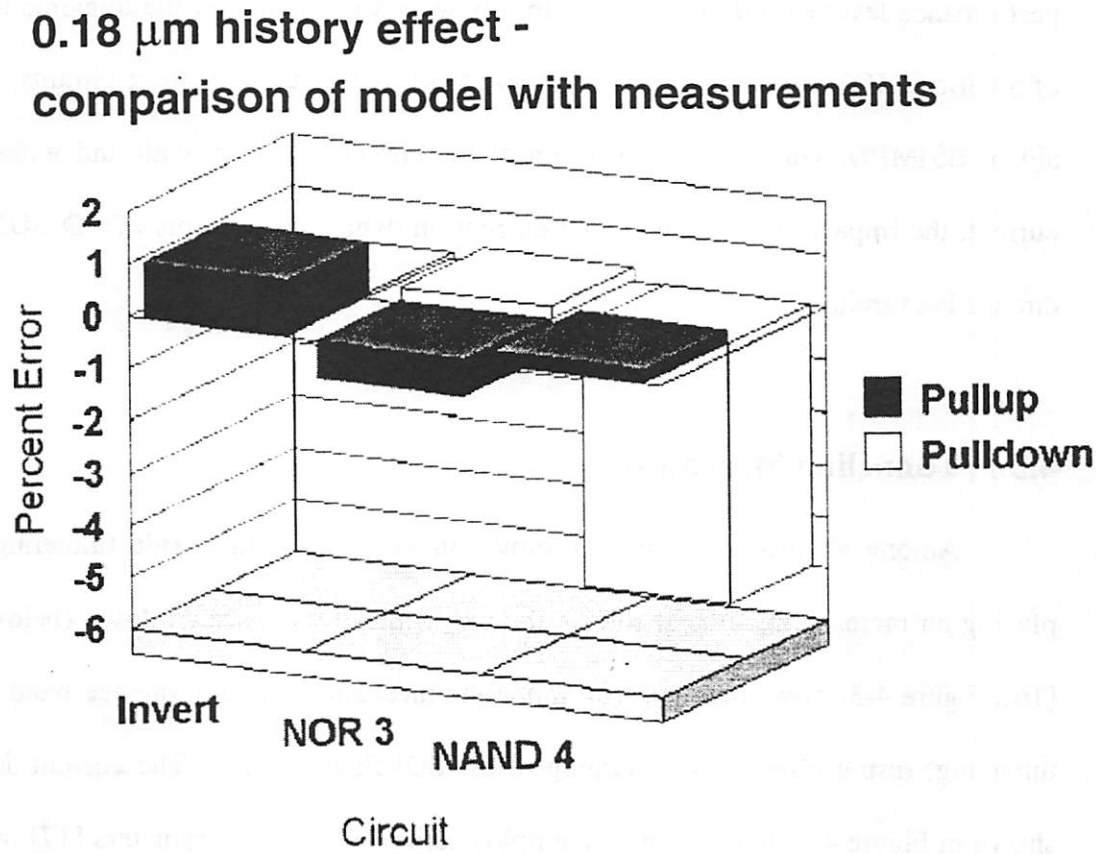


Figure 4-2. BSIMPD accuracy in history-effect prediction for CMOS inverter, 3-way NOR gate and 4-way NAND gate, respectively [12]. The percent error is between model and measurement data.

4.3 Studying the Impact of Gate Tunneling on Dynamic Behaviors of Partially-Depleted SOI CMOS using BSIMPD

With oxide scaling, the tunneling current [13]-[15] between the gate and the body introduces an element of complication to the history effect furthermore. It is worth noting from Equation (4-1) that the gate tunneling will alter the SPICE solution of the body potential. Since BSIMPD has been demonstrated to be able to accurately capture the history effect (Figure 4-2), we may further utilize it as a tool to study the impact of gate tunneling on SOI CMOS so that circuit designers may gain insight to fully exploit the

performance leverage offered by SOI. In this work we investigate the dynamic behavior of a static CMOS inverter, the basic building block of higher order logic circuits, with the aid of BSIMPD. Through a comparison of the circuit behavior, with and without gate current, the impact of oxide tunneling current on dynamic behaviors of PD SOI CMOS circuits is examined.

4.3.1 Tunneling Mechanism

Among all the body currents shown in Figure 2-1, the oxide tunneling, I_{gb}, is playing an increasingly crucial role as the oxide thickness is scaled down (below 25 Å) [16]. Figure 4-3 shows the dominant tunneling mechanism (direct valence-band electron tunneling) responsible for the charging of the SOI floating body. The current density is shown in Figure 4-4. In this work we employ calibrated model parameters [17] which are representative of state-of-the-art PD SOI technologies (L = 0.13 um, T_{Si} = 160 nm, T_{box} = 150 nm) to examine the impact of I_{gb}.

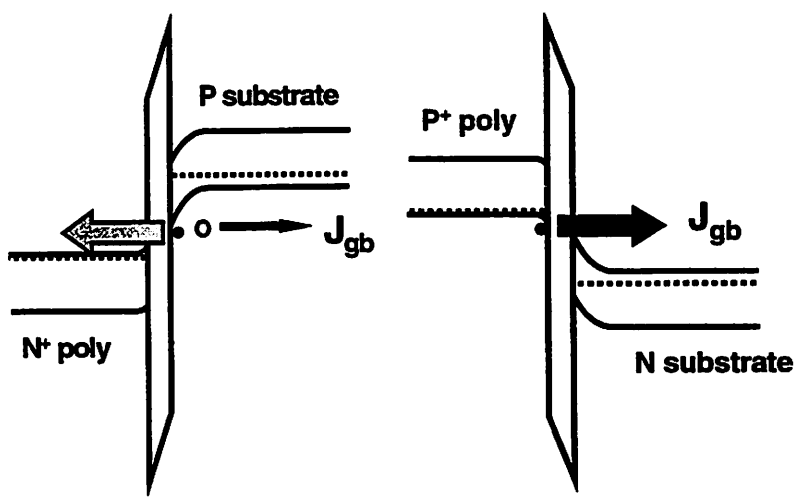


Figure 4-3. Band diagrams showing the dominant oxide tunneling mechanism responsible for charging the floating body – valence-band electron tunneling.

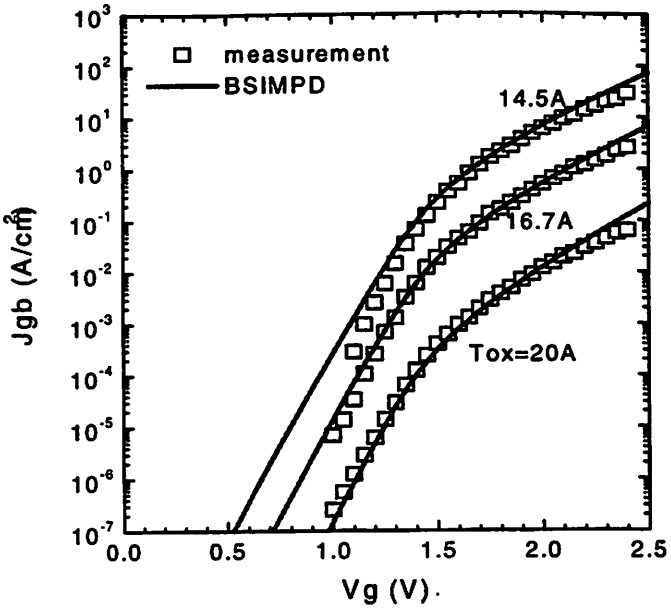


Figure 4-4. Oxide tunneling current model used in this study. J_{gb} depends on V_g (V_{dd}) and physical oxide thickness T_{ox} and agrees well with data [15].

4.3.2 Impact on Transient Responses of MOSFETS

Figure 4-5 shows the step turn-on response of a MOSFET. Without oxide tunneling, body charge falls off due to carrier recombination after the gate-to-body capacitive coupling is shielded by the surface inversion layer. With oxide tunneling current, I_{gb}, body charging continues until I_{gb} is counterbalanced by forward junction current after a finite amount of time. This time constant depends on the forward IV characteristics of body-source/drain diodes (for a given I_{gb}), and determines the degree of body potential, δV_{bn} and δV_{bp}, of the MOSFETs in steady state. In this study (Figure 4-5) since time constant (t_p) for the PMOSFET to reach steady state is longer than t_n due to smaller recombination current, net charge injection (the integration of net body current in

Figure 4-5(c)) for the PMOSFET and thus the induced forward bias δV_{bp} is larger than δV_{bn} for NMOSFET.

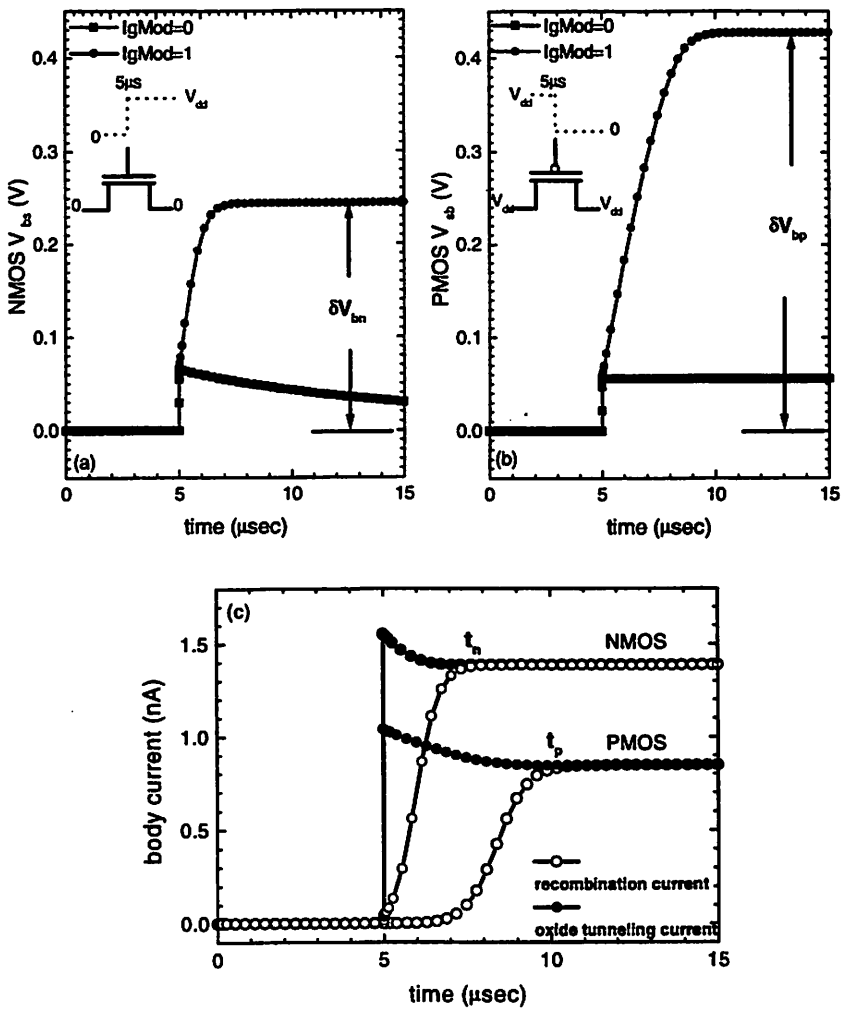
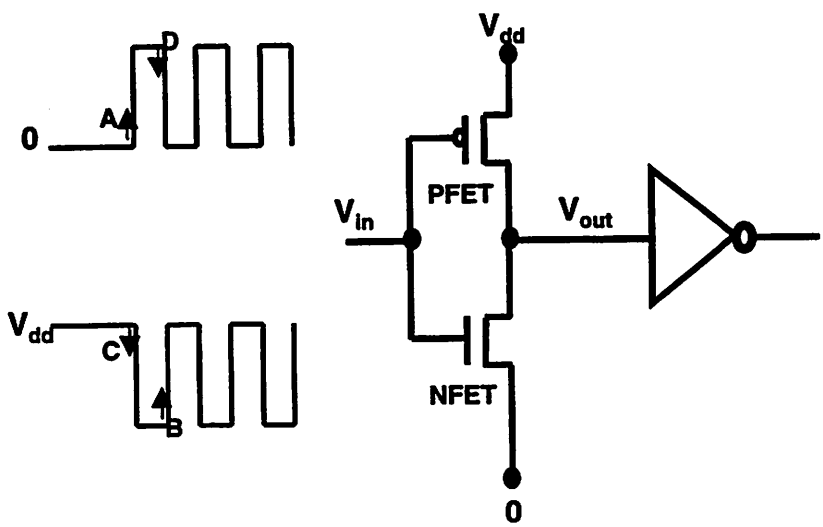


Figure 4-5. Impact of gate tunneling (IgMod=1) on the transient behavior of (a) NMOSFET, (b) PMOSFET and (c) body current. (V_{dd}=1.5V, T_{ox}=14.5Å, W=5μm)

4.3.3 Impact on Dynamic Behaviors of CMOS Circuits

Two 500-MHz input signals (with a 0.1 nanosecond slew and 0.9 nanosecond pulse width), one starting from DC GND and one from V_{dd}, are applied sequentially to a CMOS inverter (Figure 4-6). Figure 4-7 shows the body voltages of the MOSFETs in the inverter through the first cycle. Both V_{b0n} in Figure 4-7(a) and V_{b0p} in Figure 4-7(c) are determined by diode IV characteristics (a balance between the reverse leakage current from the diode across the body to drain junction and the forward bias current of the diode across the body to source junction). Contrary to the transistors starting at OFF state, the body voltages of the transistors starting at ON state are raised by the gate current as shown in Figure 4-7(b) and (d).



Case A: the first switch (low-to-high) when V_{in} starts at 0
Case B: the second switch (low-to-high) when V_{in} starts at V_{dd}
Case C: the first switch (high-to-low) when V_{in} starts at V_{dd}
Case D: the second switch (high-to-low) when V_{in} starts at 0

Figure 4-6. The inverter delay depends on the history of the applied signal. The first switch starts at 0.9nsec with a 0.1nsec slew. The pulse width is 0.9nsec.

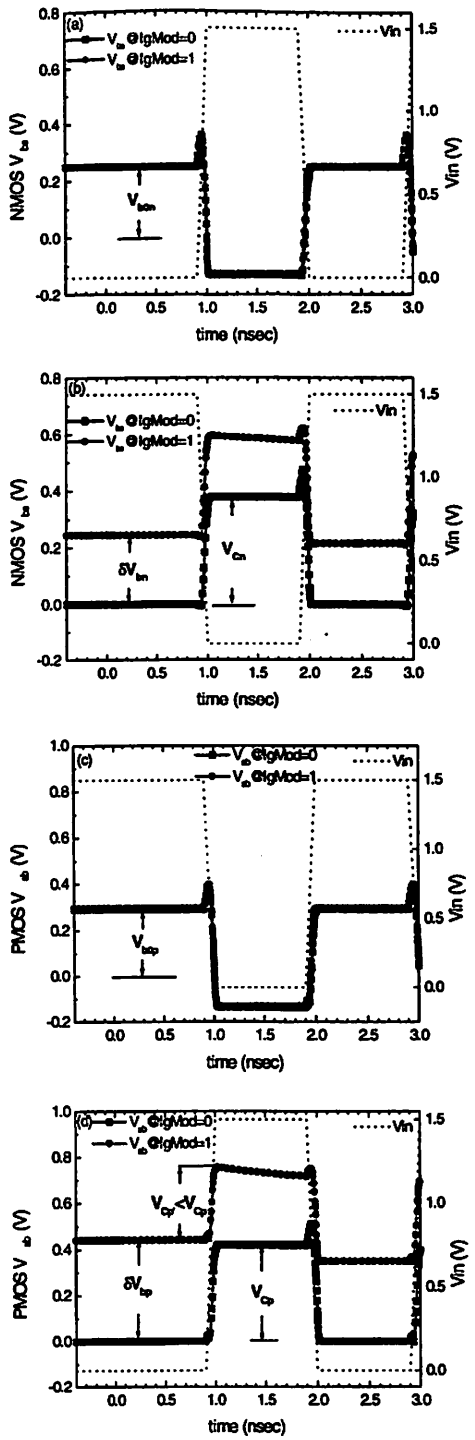


Figure 4-7. Body voltages of the MOSFETs in the CMOS inverter of Figure 4-6 (through the first cycle). The drain-to-body capacitive coupling swing V_{Cn} (V_{Cp}) is usually larger than V_{b0n} (V_{b0p}) due to thick silicon film thickness. Notice the drain-to-body capacitive-coupling swing in (d) becomes smaller due to δV_{bp}.

The impact on the inverter falltime-delay (TD_{fall}) is shown in Figure 4-8(a). When the input signal V_{in} starts at V_{dd}, the initial forward bias δV_{bn} lowers V_T and enhances the current drive of the NMOSFET and therefore shortens TD_{fall}. As the V_{bs} prior to rising-input transition (Figure 4-8(b)) drifts to the steady state value due to junction diode current, TD_{fall} becomes insensitive to the presence of oxide tunneling. On the other hand, when V_{in} starts at 0 the initial forward bias δV_{bp} raises the junction capacitance (depletion and diffusion capacitances (Figure 2-8)) of the PMOSFET and lengthens TD_{fall}. As the V_{sb} of PMOSFET (Figure 4-8(c)) drops towards its steady state, this loading effect gradually disappears and TD_{fall} settles to a slightly lower value due to higher steady-state NMOS-V_{bs} (Figure 4-8(b)) caused by gate-current charging.

Figure 4-8(a) demonstrates that the range of TD_{fall} difference between case A (defined in Figure 4-6) and case B increases by 3X in the presence of gate tunneling current. In other words the history effect, which may be quantified by the delay range, is more pronounced. Also, the frequency dependence of the delay range (Figure 4-9) is large and varies with V_{dd}.

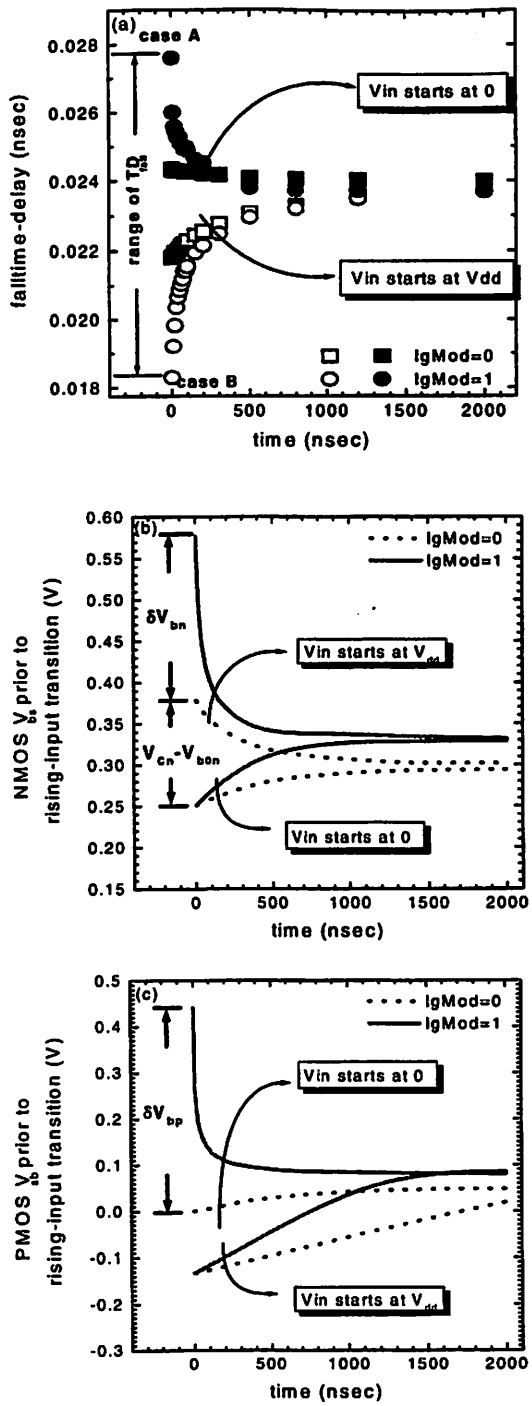


Figure 4-8. History dependence of (a) falltime-delay, (b) NFET-V_{bs} and (c) PFET-V_{sb}. Notice the crossover in (a) when V_{in} starts at 0.

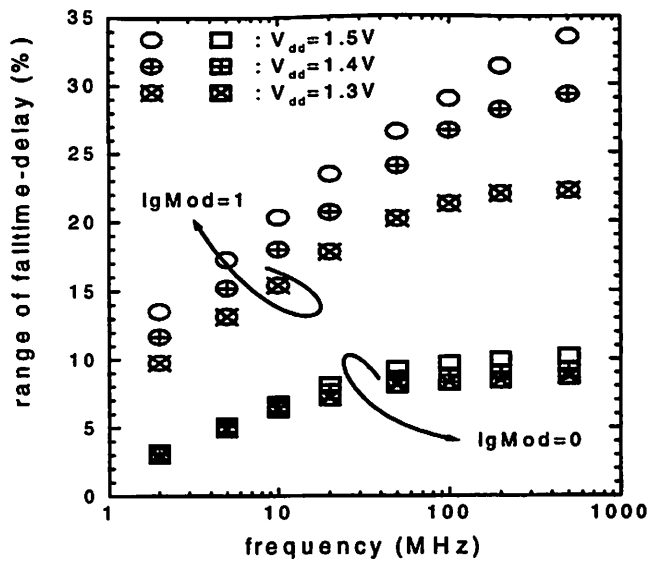


Figure 4-9. Frequency dependence of the falltime-delay range shows the deleterious impact of gate tunneling (T_{ox}=14.5Å).

Similarly, the initial forward bias δV_{bp} improves the current drive of the PMOSFET and thus shortens the risetime-delay (TD_{rise}) when V_{in} starts at 0 as shown in Figure 4-10(a). The effect is larger than the rising-input case since $\delta V_{bp} > \delta V_{bn}$ (due to leakier NMOSFET junctions). When V_{in} starts at V_{dd}, on the other hand, the forward-bias loading effect is smaller than the rising-input case because $\delta V_{bn} < \delta V_{bp}$. Contrary to the long time constant it takes for TD_{rise} to converge to its steady state due to small diode current of the PMOSFET, the gate current enlarges the history dependence of TD_{rise} substantially. This is also reflected in the frequency dependence of the TD_{rise} range (Figure 4-11), which occurs between case C (defined in Figure 4-6) and case D. Notice the 2X increase in delay range for (V_{dd} = 1.5 V, T_{ox} = 20 Å, frequency = 500 MHz) resulted from the presence of the tunneling current.

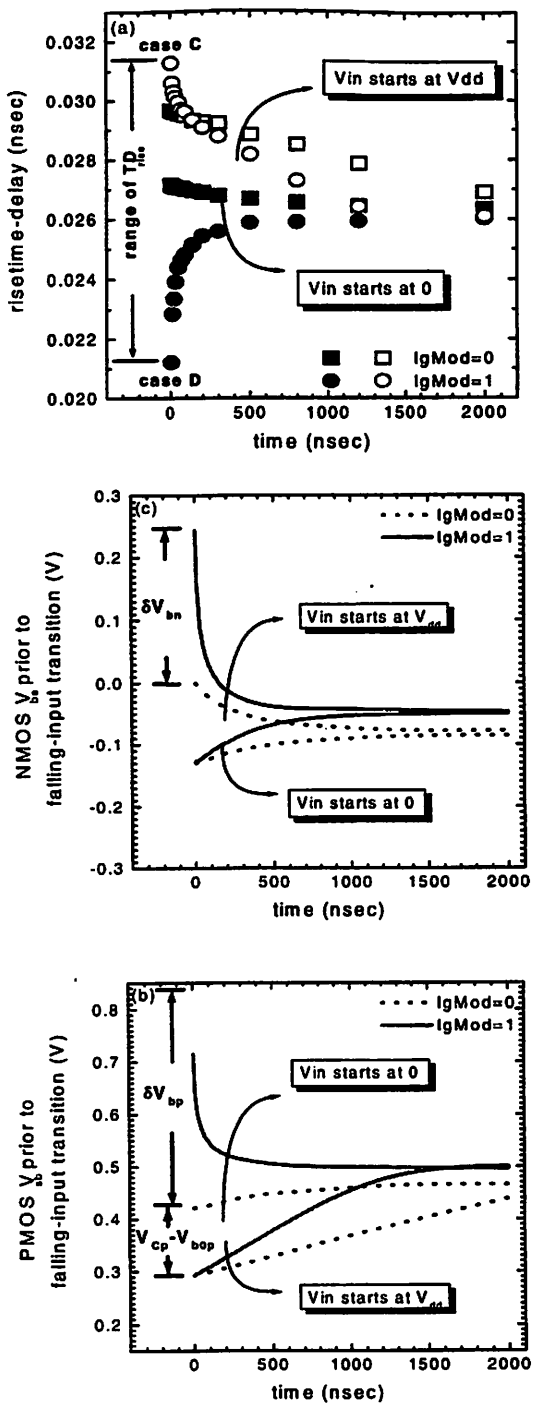


Figure 4-10. History dependence of (a) risetime-delay, (b) PFET-V_{sb} and (c) NFET-V_{bs}. Notice the crossover in (a) when V_{in} starts at V_{dd}.

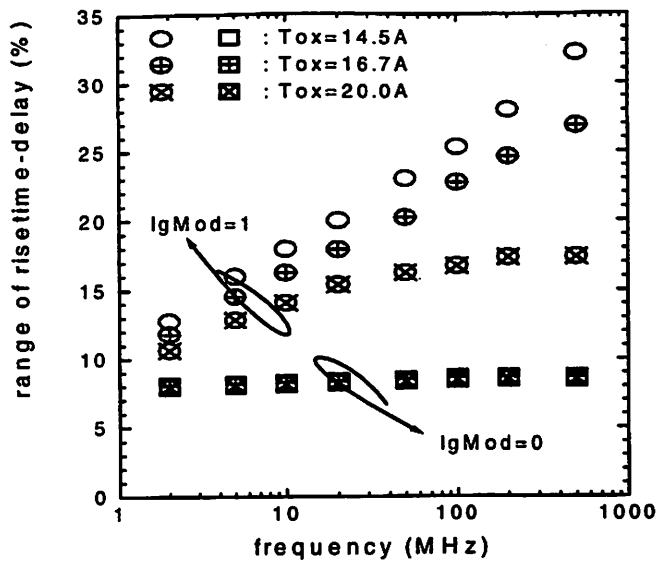


Figure 4-11. Frequency dependence of the risetime-delay range shows the deleterious impact of gate tunneling (V_{dd}=1.5V).

In conclusion, we have investigated and analyzed the impact of gate tunneling on dynamic behaviors of SOI CMOS with the aid of BSIMPD. The impact of gate tunneling on the floating-body effect, specially the history and frequency dependence of inverter delays, is examined. This study suggests that gate tunneling has a strong impact on the delay range of a PD SOI CMOS inverter. It is crucial for circuit designers to understand and contain this hysteretic delay variations caused by gate current. An accurate SPICE model including the oxide tunneling mechanism is needed to quantify the effect without undermining the performance benefit of a PD SOI technology.

4.4 Tendency toward Full Depletion due to Gate-Body Tunneling

In the previous section, we demonstrated that the valence-band electron tunneling raises the transistor body charge/potential at ON state. According to the band diagrams shown in Figure 4-3, however, this mechanism takes place only for the gate bias larger than around 1 V so that the valence-band energy level may rise above the conduction-band energy level [15]. Figure 4-12 further confirms that the onset of significant gate-body tunneling in the strong inversion regime is indeed around 1 V. Also shown in Figure 4-12, on the other hand, is the gate-body tunneling current in the accumulation regime, which may emerge as a more important tunneling component as the supply voltage is scaled to below 1 V.

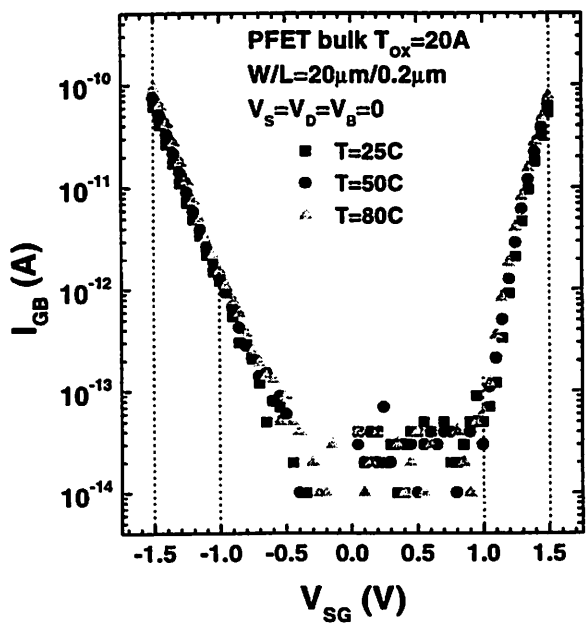


Figure 4-12. The gate-body tunneling current for a PMOSFET at V_{SG}=-1V is much larger than the one at V_{SG}=1V.

This tunneling mechanism in the accumulation regime originates from the conduction-band electron tunneling, which may lower the transistor body charge/potential. In other words, the body majority carrier concentration and thus the floating-body effect may be suppressed for scaled SOI CMOS with supply voltage lower than 1 V due to this mechanism. In this section, we demonstrate that ultra-thin film SOI substrate tends to become fully depleted under the influence of gate-body tunneling.

Our study [3] starts with calibrating the gate-body tunneling current and body-source/drain diode current using device simulation (MEDICI). The gate tunneling calibration uses a capacitor structure with N^+ poly-silicon gate and 10^{18} cm^{-3} p-type substrate. Parameters regarding the tunneling mechanism are adjusted to match the simulation to the published experimental data [16]. As for the diode current calibration, a lateral N^+-P diode is used. The p-type region is uniformly doped at 10^{18} cm^{-3} concentration, while the N^+ region has a doping of 10^{20} cm^{-3} with a Gaussian profile. The reverse junction leakage, which may counterbalance the gate-body tunneling current and determine the steady-state body potential, has also been carefully calibrated [17].

Pass-gate configuration for the calibrated NMOSFET structure with V_{dd} = 1 V is used to demonstrate the tunneling effect in this study. This is because the SOI body has the most majority carrier accumulation in a pass-gate configuration when $V_G = 0$ and $V_S = V_D = V_{dd}$. For a PD SOI NMOSFET under this configuration, the device is near flat-band operation without the influence of oxide tunneling (V_{GS} = -1 V ~ V_{FB}). With high gate-

body tunneling, nevertheless, the body may become more depleted due to the loss of majority carriers in the body.

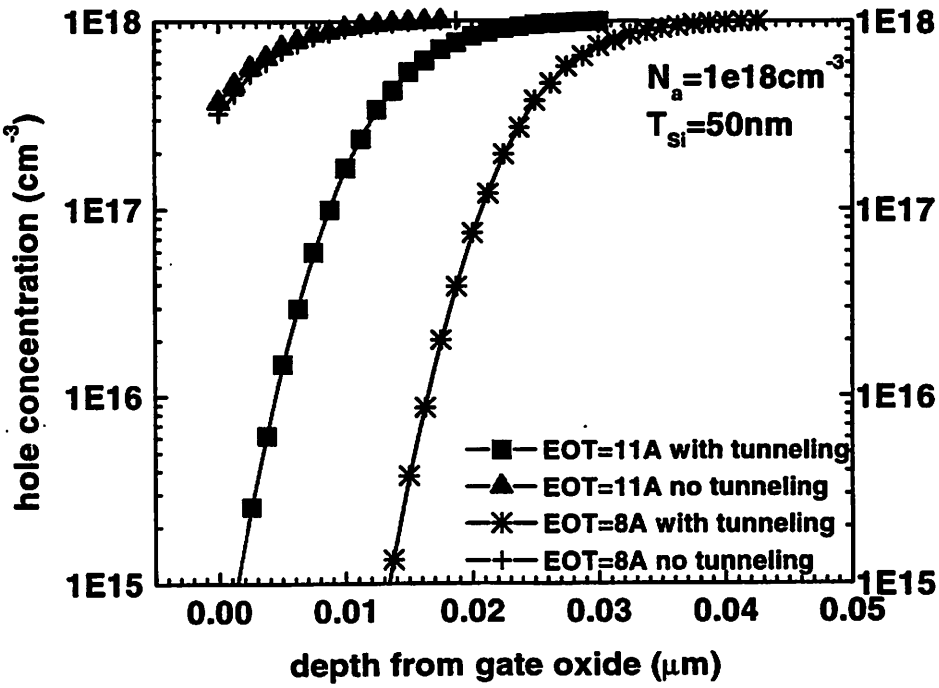


Figure 4-13. Impact of gate-body tunneling on the body majority carrier concentration [3].

Figure 4-13 shows the simulated hole-concentration profile in the body for 50-nm SOI thickness (T_{Si}), 10^{18}-cm^{-3} body doping (N_a), with equivalent oxide thickness (EOT) as a parameter, with and without gate tunneling. We can see that with the tunneling current, the hole concentration near the substrate surface is much lower than the case of without tunneling. The substrate near the surface is depleted. In Figure 4-14, furthermore, we show the hole-concentration profile in the body for T_{Si} = 20 nm, EOT = 11 Å, with N_a as a parameter. It can be seen that the substrate is fully depleted for $N_a = 10^{18}$ cm^{-3} due to the impact of gate-body tunneling.

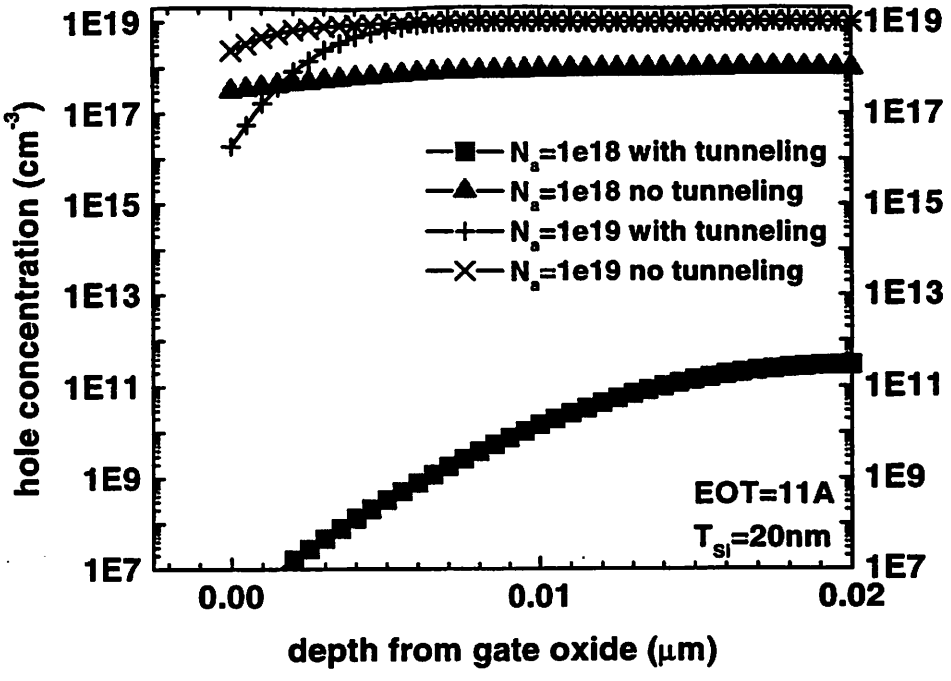


Figure 4-14. Tendency toward full depletion for ultra-thin film SOI due to gate-body tunneling [3].

The above results, which are based on monitoring the majority carrier concentration in the body, have verified and explained our earlier speculation that the floating-body effect in scaled SOI CMOS with V_{dd} below 1 V may be suppressed by gate-body tunneling. Indeed, the pass-gate leakage, as mentioned in Chapter 2 (Figure 2-7), has been observed [18] to diminish significantly due to this tunneling mechanism.

Therefore, we may conclude that the SOI device has a tendency toward full depletion for sub-1V supply voltage due to gate-body tunneling. This effect may ease the SOI circuit design due to the suppression of the floating-body effect. Further, the

equivalent oxide thickness, in addition to the silicon film thickness and the channel doping, has to be considered in the SOI device design regarding the body depletion [3]. Also, from the angle of compact modeling, a Full-Depletion (FD) SOI MOSFET model may become more important with CMOS scaling, partly due to this mechanism. The FD SOI modeling work will be addressed in Chapter 6.

4.5 Summary

In this chapter, we first investigate and analyze the impact of gate-body tunneling on dynamic behaviors of partially depleted SOI CMOS with the aid of the physically accurate BSIMPD model. We examine in particular the impact of gate tunneling on the history dependence of inverter delays. The examination reveals key requirements for capturing the history effect in SPICE modeling. This study suggests that the valence-band electron tunneling in the strong inversion regime has a significant impact on the delay range and should be considered in SOI circuit simulation. It is crucial for circuit designers to understand and contain the hysteretic delay variations caused by gate current. An accurate SPICE model that includes the oxide tunneling mechanism should be used to quantify the effect without undermining the performance benefit of a partially depleted SOI technology.

Then we investigate the impact of gate-body tunneling on the majority carrier concentration of the SOI body under 1V supply voltage. Our results indicate that the floating-body effect such as the pass-gate leakage may be suppressed and the thin SOI body may show a tendency toward full depletion due to the loss of majority carriers

through the conduction-band electron tunneling in the accumulation regime. This effect is becoming important for scaled SOI CMOS with supply voltage below 1 V.

4.6 References

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Chapter 5

BSIMPD Parameter Extraction Methodology

5.1 Introduction

In Chapter 2 we have proposed BSIMPD as a partial-depletion SOI MOSFET model for deep-submicron CMOS designs. This model can represent various SOI technologies using its model parameters. Since it is the model card (parameter set) that bridges a specific SOI technology and circuit design, accurate parameter extraction for BSIMPD is crucial to creating designs that work the first time.

Compared with the parameter extraction of BSIM bulk model [1], the challenge of BSIMPD parameter extraction lies in the SOI-specific self-heating and floating-body effects. In this chapter, we first present our modeling solution to the complication caused by self-heating. A strategy for BSIMPD parameter extraction with emphasis on capturing the floating-body effect is then proposed.

5.2 Modeling Solution to Self-Heating

In Section 2.3.2, we pointed out that the Self-Heating Effect (SHE) reduces the body potential of SOI devices by inducing more diode leakage and thus degrades the current drive beyond the usual bulk-MOSFET temperature sensitivity. Besides, self-heating is a modeling rather than performance issue for devices in low power logic circuits due to the relatively long thermal time constant as compared to circuit switching time. As a result, there is a gap between the DC modeling data (from which the model parameters for SPICE simulation are extracted) and the self-heating-free current drive present in most logic circuits.

In other words, extracting the model parameters from DC IV data without considering the self-heating effect will underestimate the circuit speed in SPICE simulation. Hence, *we propose to use self-heating-free data for parameter extraction and use constant device temperature in logic circuit simulation.* This strategy is based on the following thoughts:

(1) *Efficiency.* The thermal $R_{th}C_{th}$ sub-circuit can be turned OFF and thus the iteration for temperature node can be avoided in the SPICE simulation for logic circuits. This may reduce the size of the SPICE Jacobian matrix. Notice that the solve time for the SPICE sparse matrix is roughly $O(n^{1.4})$ [2], where n is the order of the matrix. In addition, during each SPICE iteration the calculation of all the temperature-derivatives is skipped and hence the matrix load time is reduced. Besides, the convergency may improve due to

the constant temperature simulation. Notice the cyclic dependence between device temperature and the drain current.

(2) *Accuracy*. It is more straightforward to tackle the device characteristics in real circuit operation rather than in DC. Specifically, targeting the heating-free (constant device temperature) data during parameter extraction ensures the validity of the temperature-sensitive parameters such as mobility. Moreover, the thermal resistance, R_{th}, is actually layout dependent. The R_{th} value for an isolated transistor is different from the one for a multi-finger device in real circuits [3]. It is therefore desirable to solve this modeling problem imposed by self-heating at the stage of model parameter extraction rather than in circuit simulation.

Hence, our modeling solution to self-heating lies in the construction of the heating-free modeling characteristics. Although the pulse IV measurement technique [4] was proposed to directly obtain the heating-free IV data, it is difficult and requires high-speed setup and careful consideration for capacitive coupling [5]. Therefore, we propose a new method to reconstruct the heating-free IV data. This method mainly deals with the following: adding back the drain current loss [6] and subtracting the enhancement of impact ionization [7] due to self-heating during ON state measurement (especially in the high power regime). As described in Equation (5-1),

$$\begin{aligned} I_{DS,non-selfheated} &= I_{DS} + \frac{\Delta I_{DS}}{\Delta T} R_{th} I_{DS} V_{DS} \\ I_{II,non-selfheated} &= I_{II} - \frac{\Delta I_{II}}{\Delta T} R_{th} I_{DS} V_{DS} \end{aligned} \qquad (5\text{-}1),$$

non-self-heated data can be reconstructed by establishing the device-temperature dependence and thus sensitivity of the drain current ($\Delta I_{DS}/\Delta T$) and impact ionization current ($\Delta I_{II}/\Delta T$) at each bias point. Device temperature can be calculated by (substrate temperature + thermal resistance (R_{th}) × power). The determination of R_{th} will be described in the next section.

The validity of this approach has been verified in Figure 3-4, based on the I_{SUB} (impact ionization current) data. As shown in Figure 5-1, the drain current loss due to self-heating at a given bias and device geometry is more significant in NMOS than in PMOS. The gate width dependence of the current loss of the body-tied NMOS is due to the additional heat path through the body contact region, which has been addressed in Section 2.3.1.

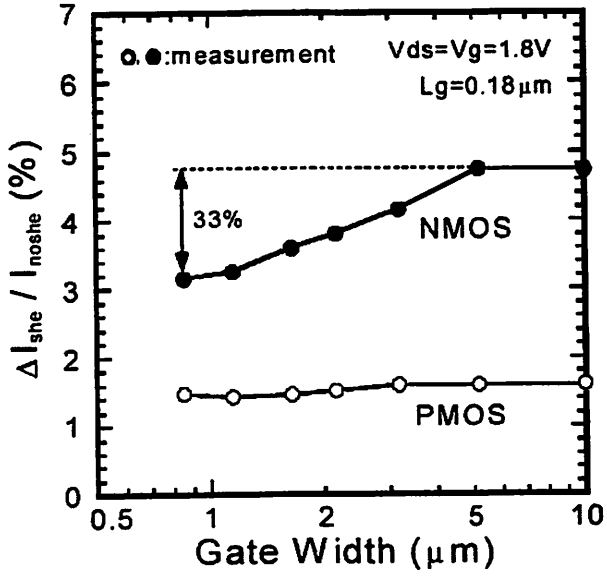

Figure 5-1. Gate width dependence of the drain current loss due to self-heating for NMOS and PMOS [6].

5.3 Determination of Thermal Resistance

From Equation (5-1) we know that the extraction of R_{th} plays a crucial role in the determination of self-heating-free data. Although the poly gate resistance method [8] was proposed to measure R_{th}, it requires special test structures. An alternative using conventional SOI test structures is the AC output conductance method [9]-[11].

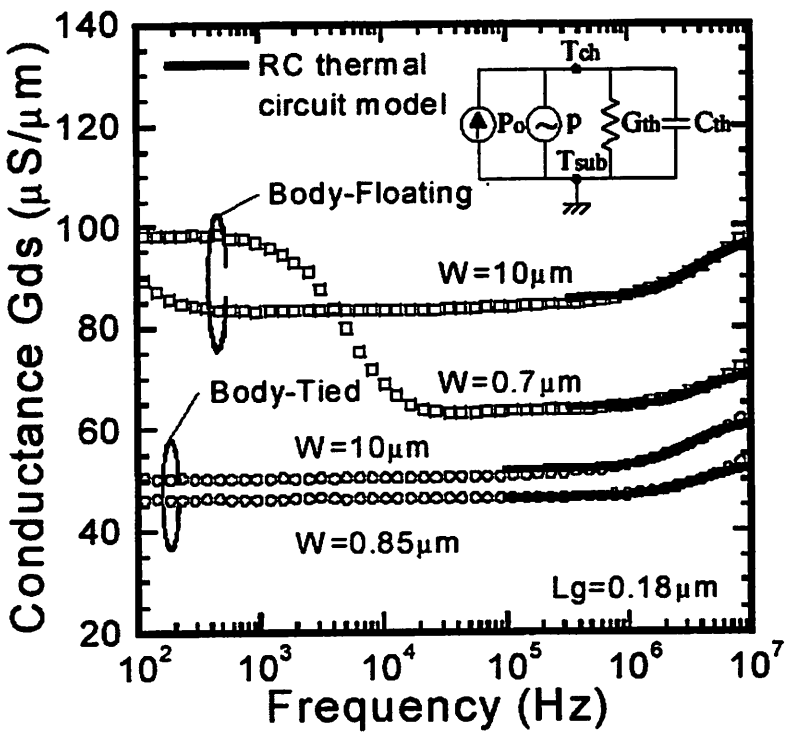

Figure 5-2. Frequency dependence of output conductance for NMOSFET. Drain bias, gate bias and small signal input voltages are 1V, 1.5V and 20mV, respectively [6].

In this AC method, the thermal conductance, G_{th} (= R_{th}^{-1}), and thermal capacitance, C_{th}, shown as an inset in Figure 5-2, can be extracted by fitting the AC drain conductance, G_{ds}, characteristics [6]. As shown in Figure 5-2, the thermal $R_{th}C_{th}$ cut-off

feature is observed as a roll-up of G_{ds} in the high frequency region (~ MHz) and can be expressed as [6]

$$G_{ds} = G_0 - \frac{I_0 + G_0 V_0}{V_0 - (G_{th} + j\omega C_{th})(\Delta I / \Delta T)^{-1}} \qquad (5\text{-}2),$$

where G_0 is the intrinsic drain conductance when the device temperature equals to the substrate temperature. The extracted G_{th} and thermal time constant, τ_{th} (= $R_{th}C_{th}$), using this method have been demonstrated in Figure 2-11 and Figure 2-12, respectively.

It is worth noting that the AC method provides us not only R_{th}, but also the thermal capacitance that does not impact the simulation result of fast logic circuits due to long thermal time constant. It is therefore desirable to find a simple DC way to extract R_{th} for efficiency.

An innovative way is using source-body diode as a temperature sensor for the measurement of R_{th}. Recall that the device temperature rise due to self-heating reduces the body potential by inducing more diode leakage. As shown in Figure 5-3, for a given amount of body injection, body potential decreases as device temperature increases. In other words, the device temperature and thus R_{th} may be determined based on the $I_{BS}(V_{BS}, T)$ diode characteristics (Figure 5-3) once the impact ionization current and body potential at a given bias are measured from body-contacted devices.

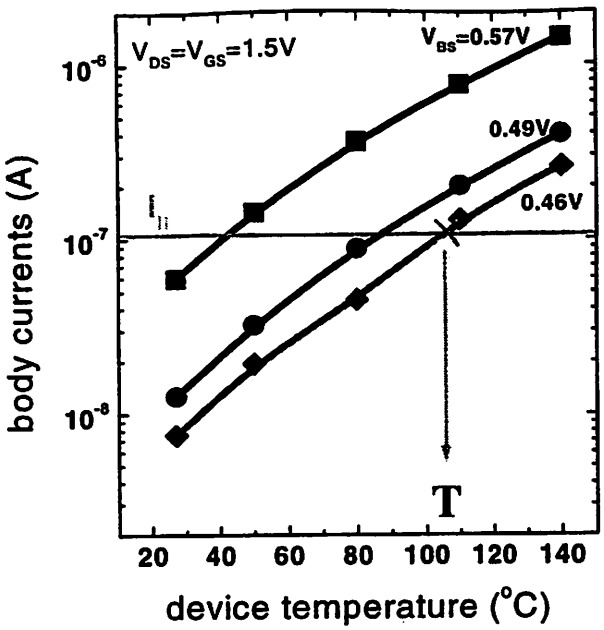

Figure 5-3. Body-source diode can be used as a temperature sensor to measure R_{th}.

5.4 Proposed BSIMPD Parameter Extraction Strategy

Figure 5-4 shows our proposed parameter extraction flow of BSIMPD. As described in Section 5.2, elimination of self-heating effect from measured IV data should first be performed. Specifically, we need to construct non-self-heated drain current characteristics from body-contacted test structures (H/T gate) for the extraction of basic MOSFET parameters. In addition, non-self-heated impact-ionization characteristics are needed to predict the kink effect, which will be verified by the non-self-heated drain current characteristics measured from floating-body test structures (I gate).

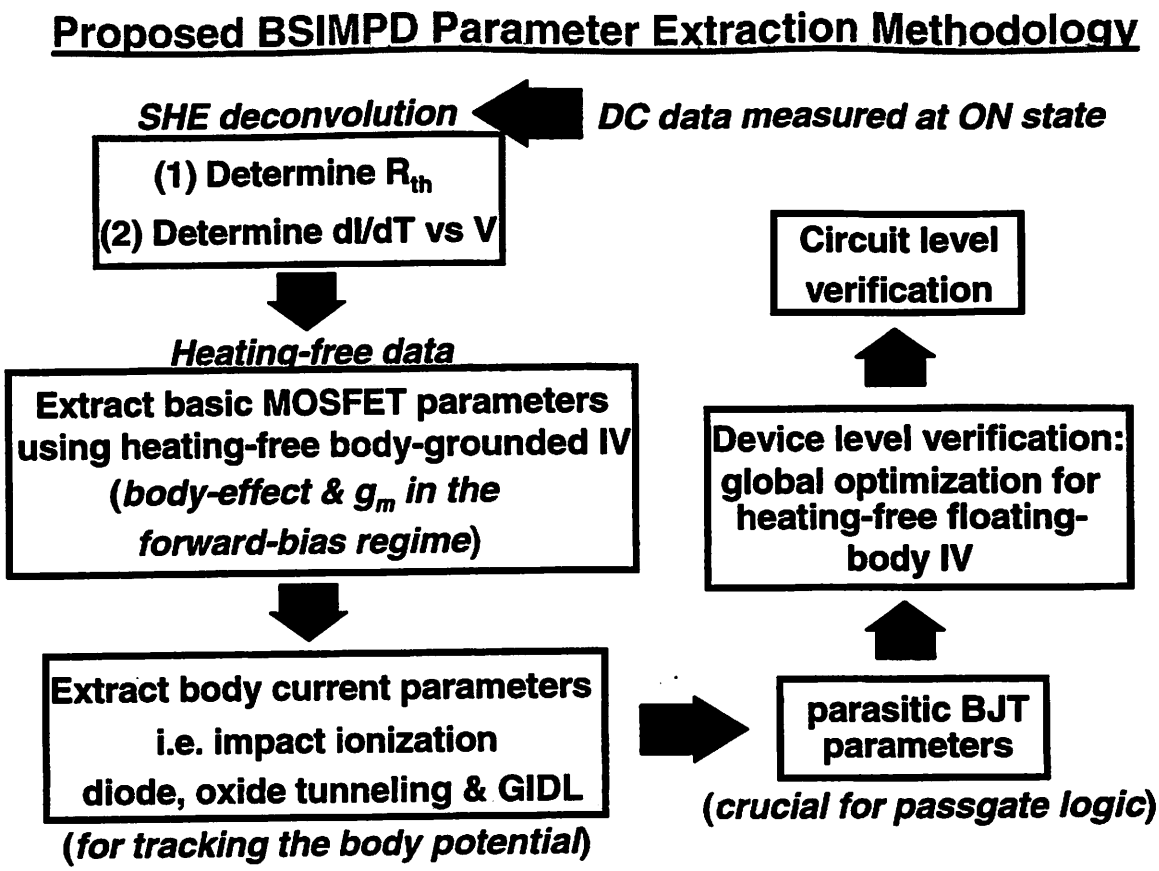

Figure 5-4. Proposed BSIMPD parameter extraction flow.

Once the self-heating effect is tackled, the remaining challenge is the floating-body effect. Based on the heating-free drain current characteristics from body-contacted devices, the basic MOSFET parameters can be extracted following procedures similar to bulk transistor modeling [1]. The forward body-bias regime, however, should be emphasized due to the floating-body operation. Notice that the drain and therefore the body voltage may be particularly high during the burn-in test.

The key to capturing the floating-body kink effect can be revealed by

$$\Delta I_{DS} = \frac{\Delta I_{DS}}{\Delta V_T} \cdot \frac{\Delta V_T}{\Delta V_{BS}} \cdot \Delta V_{BS} \qquad (5\text{-}3),$$

where the excess kink current, ΔI_{DS}, is determined by three factors. The first factor, $\Delta I_{DS}/\Delta V_T$, represents the transconductance of the device. Hence the parameters that determine the transconductance in the high V_{DS} (forward V_{BS}) regime need to be accurately extracted. The second factor, $\Delta V_T/\Delta V_{BS}$, represents the body effect in the device. The body-effect parameters can be accurately determined by targeting the transistor subthreshold characteristics for various V_{BS}. As shown in Figure 5-5, well-fitted I_{DS}-V_{GS} characteristics of an 80-nm-gate-length NFET for different positive body bias can be achieved.

Besides, it is worth noting from Section 2.4.2 that the body-contact effect [16] needs to be considered in parameter extraction. An observation from Figure 2-24 and Figure 2-25 suggests us that this effect is significant for the body bias higher than 0.6 V [5].

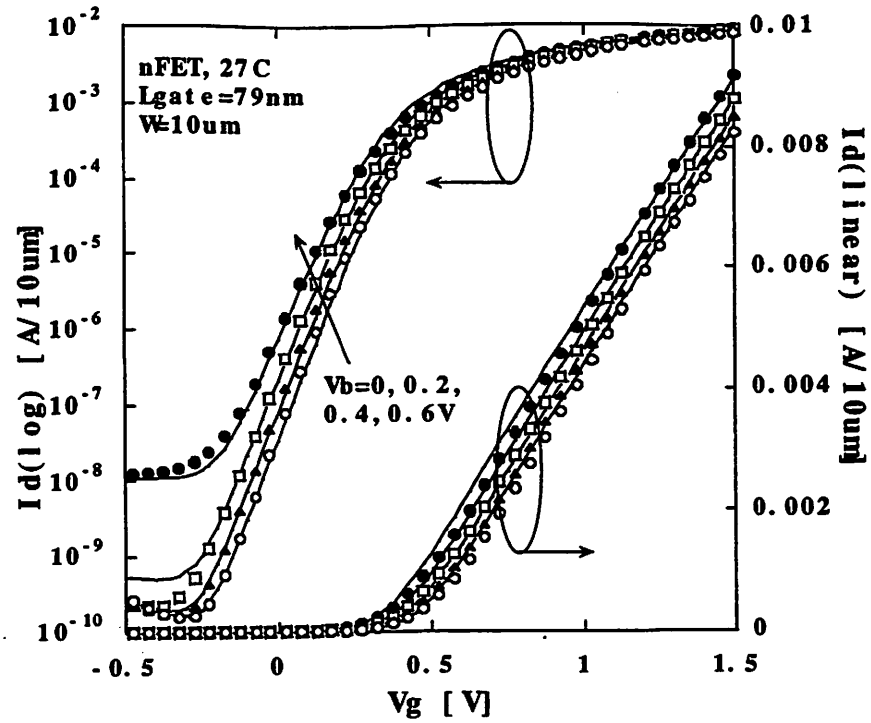

Figure 5-5. I_{DS}-V_{GS} characteristics can be used to extract the body effect parameters [12].

After obtaining the basic MOSFET parameters with special care on the transconductance and body effect in the forward body bias regime, we should focus on the prediction of the third factor of Equation (5-3), the floating-body potential. This requires extracting the model parameters of various body current components (i.e., heating-free impact ionization current, diode current, gate induced drain leakage (GIDL) and gate-to-body tunneling) from body-contacted devices. An accurate fitting result of diode characteristics for different temperatures has been demonstrated in Figure 2-14 [12]. The verification of impact ionization characteristics for various gate lengths has been shown in Figure 3-12. The verification for gate-to-body tunneling current has been shown in Figure 4-4.

The predicted heating-free floating-body IV needs to be verified with the measured data from the floating-body device. Fine-tuning the model parameters is usually required due to the discrepancy of device layout/structure between body-contacted and floating-body devices. It has been reported [13] that the side current of the body contact may induce a different effective width for the body-contacted device from the floating-body counterpart. Note that body-contacted devices with limited width are usually used to maintain the contact efficiency, as mentioned in Chapter 2. In addition, the carrier mobility may vary because the stress effect depends on the device structure [14].

It should also be aware that the impact of gate-to-body tunneling on the linear current in the high gate bias regime may become significant for thin oxide floating-body devices, as shown in Figure 5-6 [15].

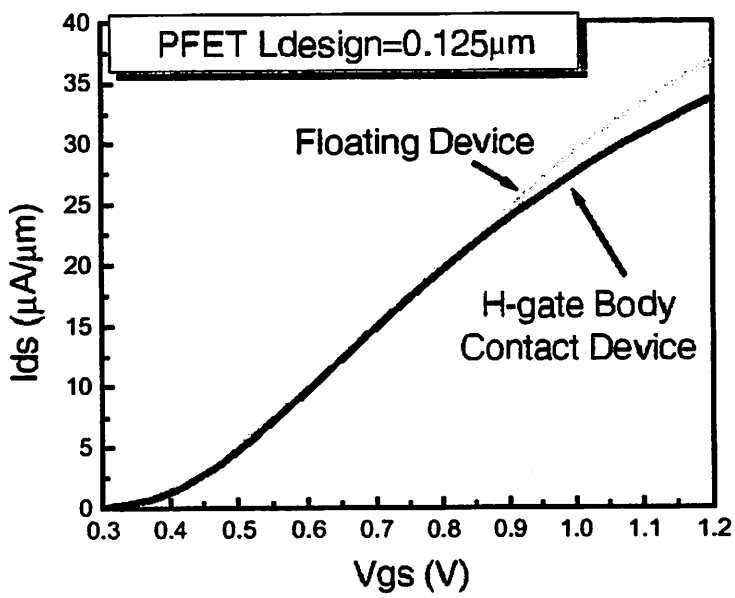

Figure 5-6. Impact of gate-to-body tunneling on the linear current of floating-body devices [15].

Figure 5-7 shows measured and simulated V_T roll-off characteristics of body-contacted and floating-body devices. Good simulated V_T roll-off characteristics in the linear and salutation region can be obtained for devices with gate length from 200 nm to 69 nm. I_{DS}-V_{DS} characteristics of the 80-nm NFET at both body-contacted and floating-body configurations have been shown in Figure 3-13. It can be seen that a good prediction for the floating-body effect is obtained. Also shown in Figure 3-13 is the output resistance (R_{out}) of the 80-nm NFET. Even the reduction of R_{out} due to the kink effect can be well modeled.

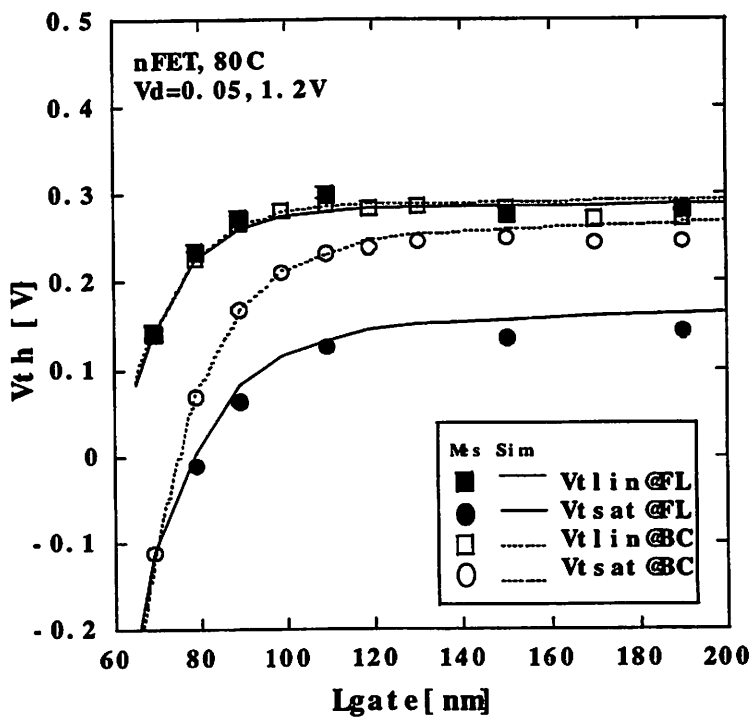

Figure 5-7. Liner and saturation V_T roll-off of body-contacted (BC) and floating-body (FL) devices [12].

Finally, a simulation example of inverter fall-time switching characteristics for a floating-body device using the model parameters extracted by the proposed methodology is shown in Figure 5-8 [6]. Input voltage (V_{in}), output voltage (V_{out}), NFET drain current (I_{dsn}) and device temperature rise (ΔT) are shown, comparing the simulation results between self-heating-ON and self-heating-OFF modes. Apparently, no significant difference is observed in V_{out} or I_{dsn} between both two modes. The only difference exists in ΔT. However, its difference of 30 mK is negligibly small. In other words, the impact of self-heating is insignificant in those devices. This is why we can execute the accurate logic circuit simulation in the self-heating-OFF mode, provided that heating-free model parameters are extracted and used.

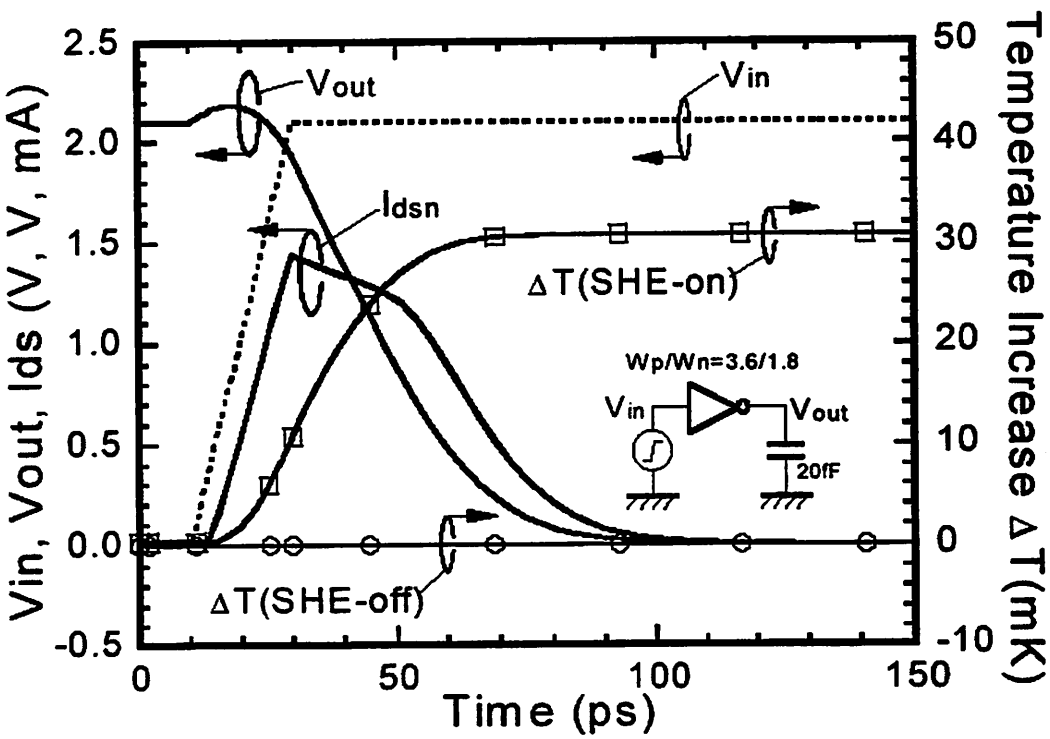

Figure 5-8. The impact of self-heating is negligible in fast switching logic circuits [6].

5.5 Summary

We have proposed a parameter extraction strategy for BSIMPD. We suggest that BSIMPD model parameters should be extracted based on self-heating-free device characteristics. The thermal $R_{th}C_{th}$ circuit can be turned OFF in fast logic circuit simulation once the heating-free parameters are used. Determination of thermal resistance, which is crucial to our self-heating modeling solution, has been addressed. A methodology for BSIMPD parameter extraction with emphasis on capturing the floating-body effect has also been proposed and verified.

5.6 References

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Chapter 6

BSIMSOI:

A Unified Model for Partial-Depletion and Full-Depletion SOI MOSFETs

6.1 Introduction

In Chapter 2, we introduced BSIMPD for Partial-Depletion (PD) SOI circuit design. As the SOI technology advances, however, the SOI thickness is scaled aggressively for reducing the junction capacitance and maximizing the device performance. The thinning of silicon film thickness also alleviates the floating-body effect and eases the SOI circuit design. For the 90-nm technology node, for example, the SOI thickness is around 50 nm [1] and is projected to go lower for future technology generations. Since the SOI device may get into Full Depletion (FD) easily for silicon film thickness below 40 nm [1], an FD SOI MOSFET model is needed for the 65-nm technology node (around 2005) and beyond.

Using BSIMPD as a foundation, we have developed a unified model for both PD and FD SOI circuit designs. In this chapter, we first introduce the concept of *body-source built-in potential lowering*, which is the enabler of the unified BSIMSOI model. Then we present the BSIMSOI framework and the model formulation of the built-in potential lowering. Finally, verification of the consolidated model with emphasis on the concept of FD index is demonstrated.

6.2 Body-Source Built-in Potential Lowering Concept

As the SOI technology gets mature [1]-[3] for low voltage and low power applications, the lack of efforts on characterizing and modeling the floating-body phenomenon is the main obstacle that hinders the SOI design [3]-[6]. One important floating-body phenomenon is the impact-ionization charging counter-balanced by self-biasing of the body-source junction. A recent report [7] on the interpretation of low voltage impact ionization indicates that the body charging mechanism remains significant with scaling. The degree of the resulting floating-body effect will consequently be determined by the built-in potential (V_{bi}) of the body-source junction.

As depicted in Figure 6-1, the body-source potential barrier causes the accumulation of majority carriers and then induces the floating-body effect [8]-[10]. This barrier exists in both PD and FD devices. The only difference between the two is that the FD device has a built-in potential lowering, ΔV_{bi}, and therefore a smaller potential barrier

height than the PD device. In other words, ΔV_{bi} is an index of the degree of full depletion.

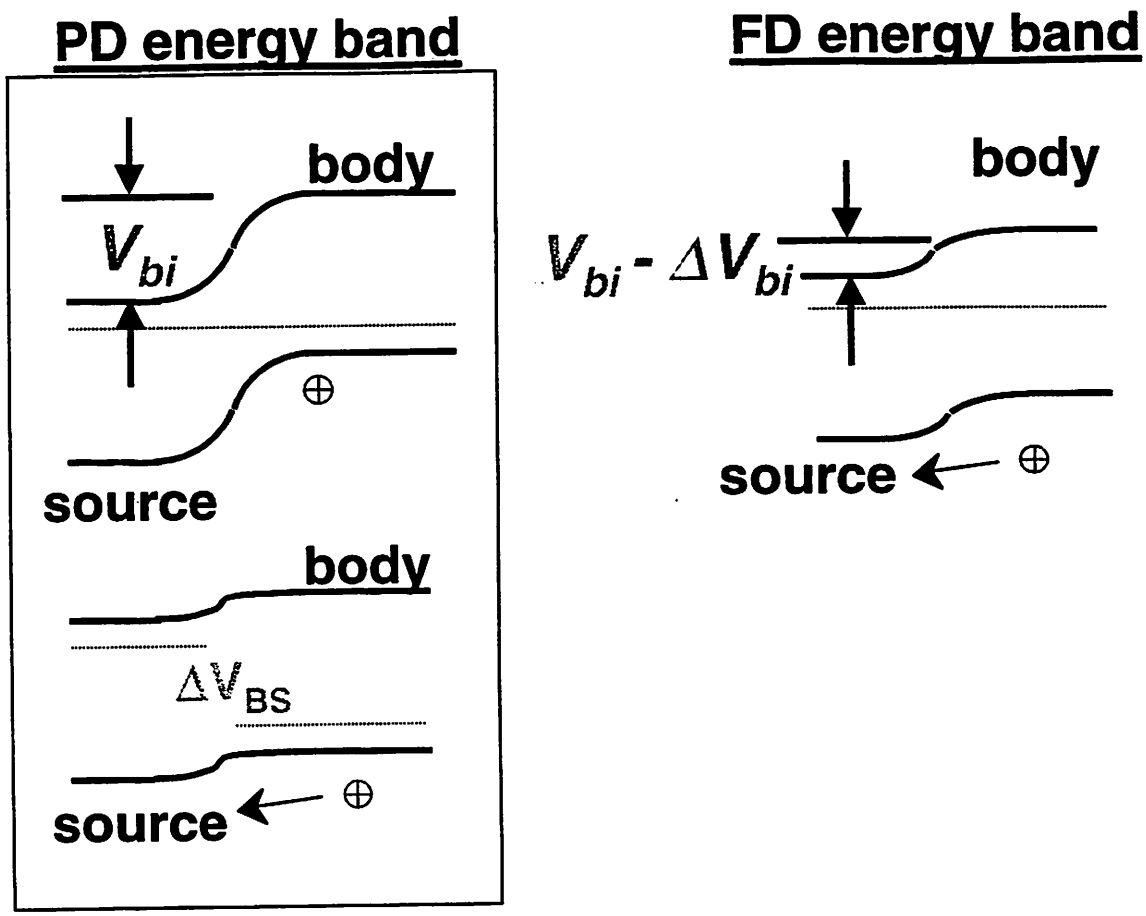

Figure 6-1. Energy band diagrams (NMOSFET) at the back surface of SOI between the body and source junction for PD and FD devices, respectively. The body-source built-in potential (V_{bi}) is responsible for the self-biasing (split of the Fermi level) of the floating body.

In this work, we investigate SOI MOSFETs from the angle of the body-source built-in potential lowering, which has rarely been experimentally tackled. This characterization also serves as a basis for the compact modeling of ΔV_{bi}. Moreover, we propose and address the need to link PD and FD SOI models using the concept of ΔV_{bi} for state-of-the-art SOI technologies.

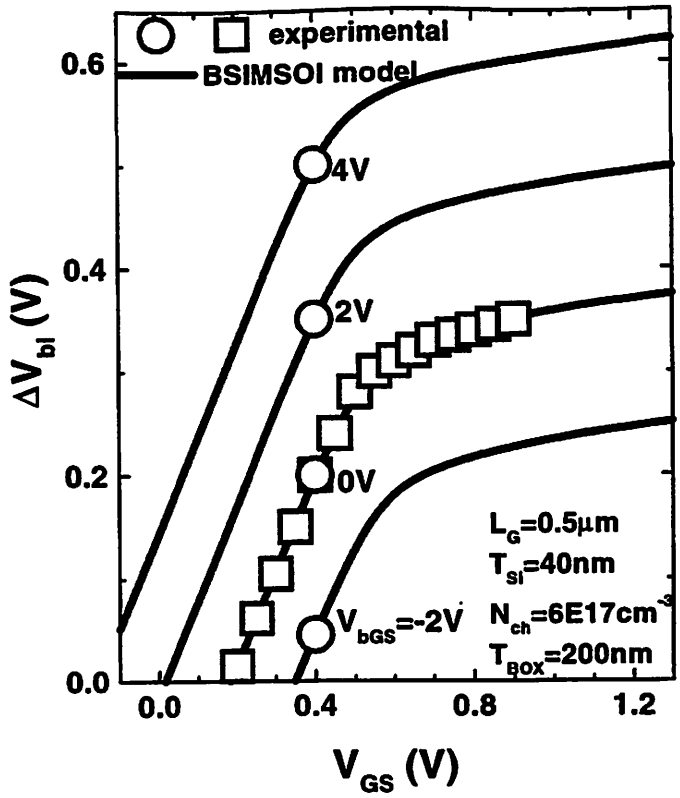

Figure 6-2. ΔV_{bi} is caused by the vertical coupling from frontgate to backgate. It can be experimentally determined using body-contacted devices.

A direct probe of ΔV_{bi} can be achieved by finding the onset of the external body bias (through a body contact) after which the threshold voltage (V_T) and hence the channel current of the FD SOI device is modulated. Notice that this onset voltage is negative for PD devices. As shown in Figure 6-2, ΔV_{bi} is induced by the vertical capacitive coupling from frontgate (V_{GS}) to backgate (V_{bGS}) and can be formulated by applying the Poisson equation in the vertical direction [11]. ΔV_{bi} increases as the channel doping (N_{ch}) or SOI thickness (T_{Si}) decreases, as shown in Figure 6-3. Notice that ΔV_{bi} is linearly dependent on N_{ch} with a slope proportional to T_{Si}^2, as predicted by the Poisson equation.

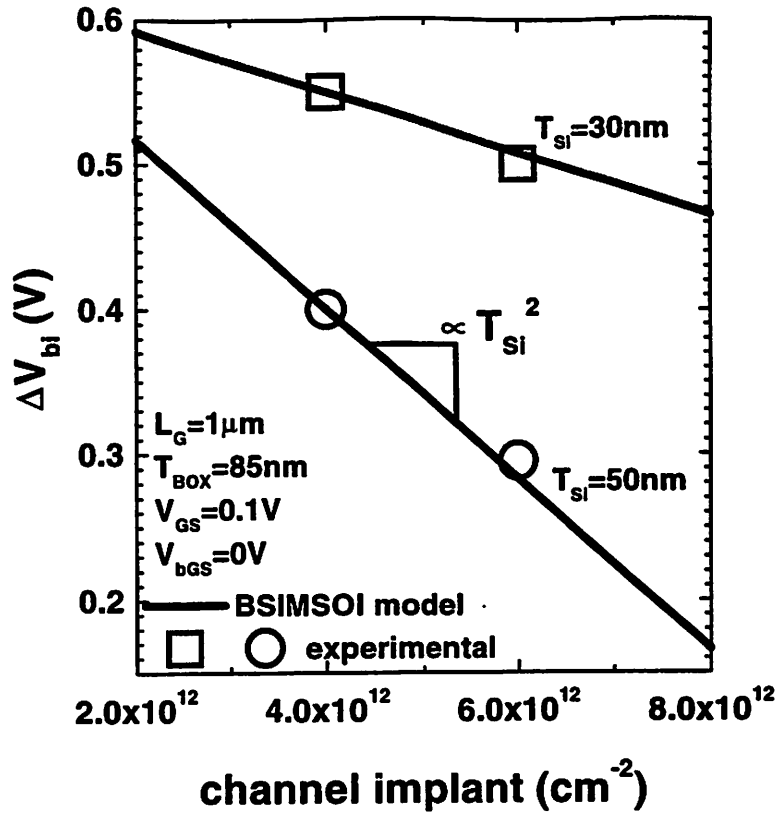

Figure 6-3. ΔV_{bi} linearly depends on the channel doping with a slope proportional to T_{Si}^2. It is an index of the degree of full depletion.

Besides the vertical coupling, ΔV_{bi} may be raised by an additional charge sharing [12] from source and drain electrode through the SOI buried oxide, an inherent feature of FD MOSFETs. As shown in Figure 6-4(a), ΔV_{bi} rolls up while V_T rolls off [13] as the gate length is scaled down due to drain field penetration. Also notice the reduction of the backgate effect on ΔV_{bi} due to the same mechanism, as shown in Figure 6-4(b). The enhanced ΔV_{bi} due to charge sharing suppresses further the floating-body effect in short-channel FD devices [14]-[16], which may determine the transistor off-state leakage.

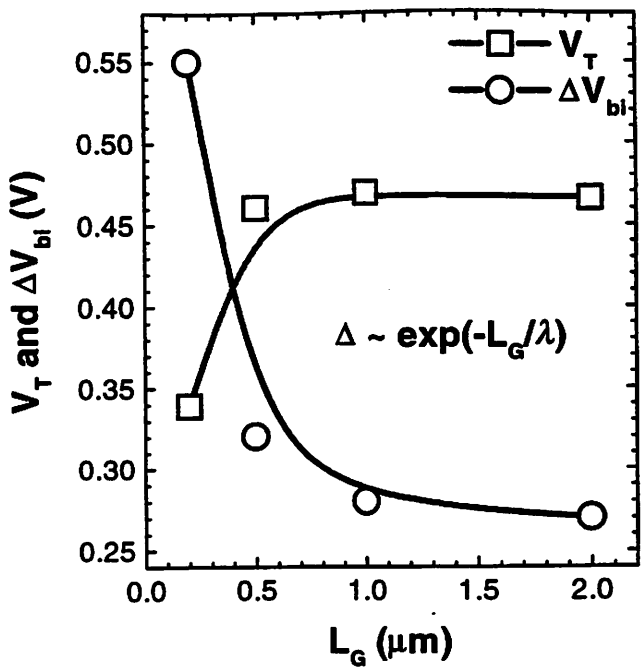

Figure 6-4(a). Drain field penetration causes V_T roll-off and raises ΔV_{bi} for the short-channel device.

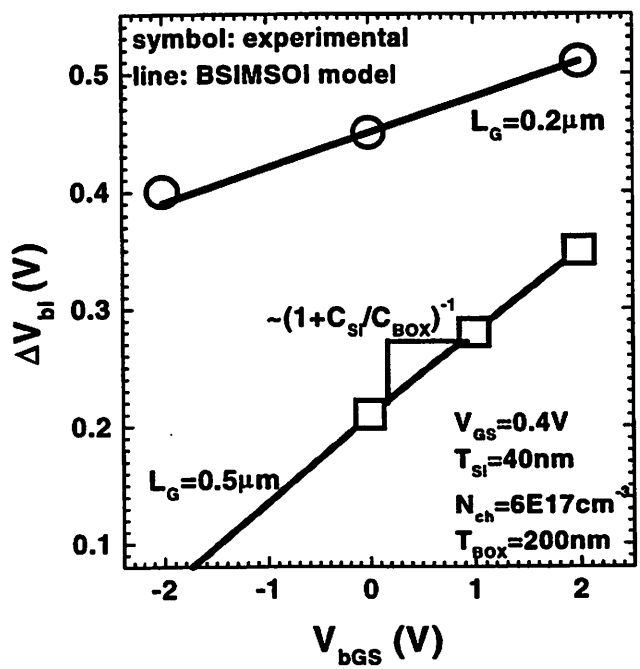

Figure 6-4(b). The backgate effect on ΔV_{bi} (slope) for the short-channel device is also reduced due to the charge sharing.

The importance of ΔV_{bi} to state-of-the-art high performance SOI technologies lies in the tendency toward full depletion due to the aggressive SOI thickness scaling [17]-[19]. Specifically, the need for multiple V_T/T_{OX} transistors for low active/standby power requirement in a single chip may result in the coexistence of both PD and FD devices in the same circuit by design. Furthermore, the laterally non-uniform channel doping (halo/pocket implant) may lead to PD nominal devices and FD long-channel devices with continuous variations in between. Since these medium to long channel FD devices are potential replacements of body-contacted devices, a compact SOI model continuously spanning PD and FD is needed for SOI circuit design. The concept of body-source built-in potential lowering enables us to capture all these scaling trends.

Therefore, we propose to link PD and FD using the ΔV_{bi} concept. Under the framework of the industry standard [20] PD SOI model, BSIMPD [21], ΔV_{bi} can be incorporated in the diode current model in an exponential manner and thus determine the body potential. As shown in Figure 6-5, for a given significant ΔV_{bi} (e.g., 0.52 V), the body-source diode can sink a huge amount of body charge injection (e.g., impact ionization) without varying the body potential. In other words, the transistor threshold voltage remains constant as long as the vertical coupling (ΔV_{bi}) is strong enough to hold the potential inside the body. Contrarily, for the PD device without built-in potential lowering (i.e., ΔV_{bi} = 0 V), the body potential is always changed as a function of the body-to-source current. Notice that even FD devices exhibit the floating-body effect to varying degrees, dependent on the level of majority carrier injection and ΔV_{bi}.

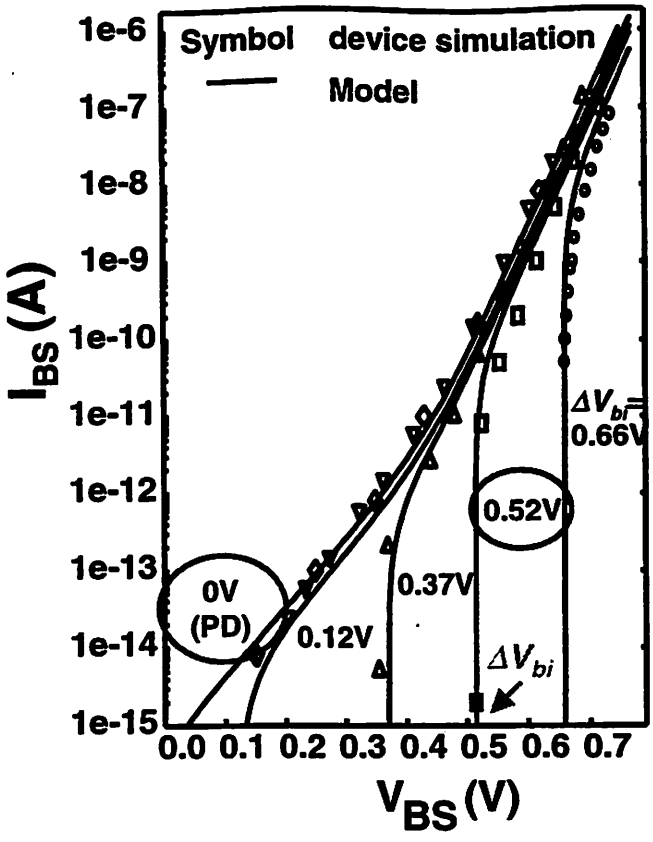

Figure 6-5. ΔV_{bi} determines the diode IV and therefore the body potential of SOI devices. It is the link between PD and FD models.

This unified SOI model [11] will approach the PD model when ΔV_{bi} is negligible at $V_{GS} = V_{dd}$ (ON state), while return to the ideal FD model (without the floating-body effect) when ΔV_{bi} is significant at $V_{GS} = 0$ V (OFF state). In other words, the ΔV_{bi} value can be used to determine the need of the floating-body simulation for efficiency [21]. In addition, ΔV_{bi} may also be used as a criterion for determining the degree of full depletion in the optimization of SOI devices. The SOI device may be designed to have a significant ΔV_{bi} and hence negligible history effect for the ease of circuit design and reduction of simulation computation time.

In conclusion, the body-source built-in potential lowering is the main difference between PD and FD SOI MOSFETs, as well as the connection of both types of devices. This physical measure not only serves as an index of the floating-body behavior of SOI devices, but also enables the unification of PD and FD models. This consolidation of compact models together with the trend of coexistence of PD/FD devices in a single chip has become one of the biggest challenges in the scaling SOI CMOS.

6.3 BSIMSOI Framework and Built-in Potential Lowering Model

As described in the previous section, we construct BSIMSOI based on the concept of body-source built-in potential lowering, ΔV_{bi}. There are three modes (soiMod = 0, 1, 2) in BSIMSOI: BSIMPD (soiMod = 0) can be used to model the PD SOI device, where the body potential is independent on ΔV_{bi} ($V_{BS} > \Delta V_{bi}$). Therefore the calculation of ΔV_{bi} is skipped in this mode. On the other hand, the ideal FD model (soiMod = 2) is for the FD device with body potential equal to ΔV_{bi}. Hence the calculation of body current/charge, which is essential to the PD model, is skipped. For the unified SOI model (soiMod = 1), however, both ΔV_{bi} and body current/charge are calculated to capture the floating-body behavior exhibited in FD devices. As shown in Figure 6-6, this unified model covers both BSIMPD and the ideal FD model.

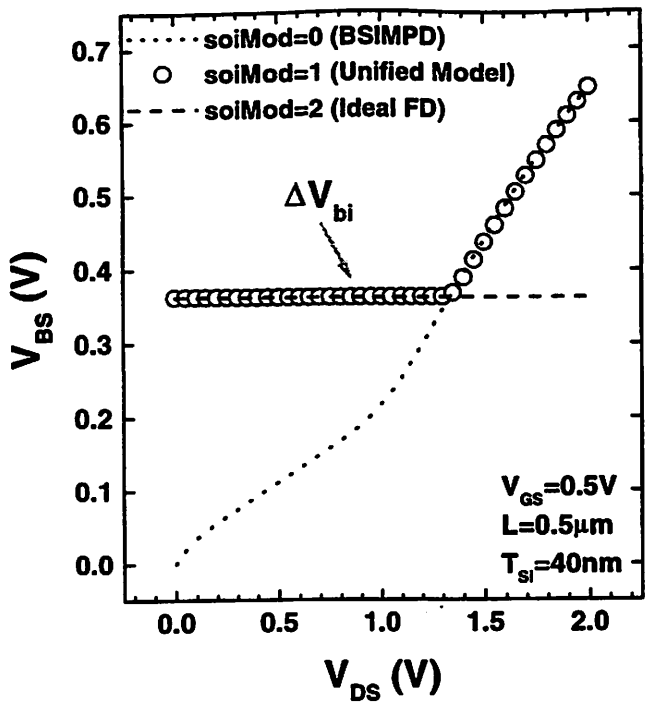

Figure 6-6. The body potential in the unified model approaches the V_{BS} solved in BSIMPD for PD devices, while returns to ΔV_{bi} for ideal FD devices.

This unified model shares the same floating-body module as BSIMPD (Figure 2-1), with a generalized diode current model considering the body-source built-in potential lowering effect ($I_{BS} \propto \exp(-q\Delta V_{bi}/kT)$). Therefore, an accurate and efficient ΔV_{bi} model is crucial. The following formulation for ΔV_{bi} is mainly based on the Poisson equation and the physical characterization for ΔV_{bi}, as presented in the previous section.

For a given surface band bending ϕ (source reference), ΔV_{bi} can be formulated by applying the Poisson equation in the vertical direction and continuity of normal displacement at the back interface:

$$\Delta V_{bi}(\phi) = \frac{C_{Si}}{C_{Si}+C_{BOX}} \cdot \left(\phi - \frac{qN_{ch}}{2\varepsilon_{Si}} \cdot T_{Si}^{\ 2} + \Delta V_{DIBL} \right) + \eta_e(L_{eff}) \frac{C_{BOX}}{C_{Si}+C_{BOX}} \cdot (V_{bGS} - V_{FBb}) \quad (6\text{-}1).$$

$$C_{Si} = \frac{\varepsilon_{Si}}{T_{Si}}, C_{BOX} = \frac{\varepsilon_{OX}}{T_{BOX}}, C_{OX} = \frac{\varepsilon_{OX}}{T_{OX}}$$

The first term of Equation (6-1) represents the frontgate coupling. T_{Si} is the SOI thickness. N_{ch} accounts for the effective channel doping, which may vary with channel length due to the non-uniform lateral doping effect. The second term of Equation (6-1) represents the backgate coupling (V_{bGS}). V_{FBb} is the backgate flatband voltage. Equation (6-1) shows that the impact of frontgate on ΔV_{bi} reaches maximum when the buried oxide thickness, T_{BOX}, approaches infinity.

In Equation (6-1), ΔV_{DIBL} represents the short channel effect on ΔV_{bi},

$$\Delta V_{DIBL} = D_{vbd0} \left(exp\left(-D_{vbd1} \frac{L_{eff}}{2l} \right) + 2exp\left(-D_{vbd1} \frac{L_{eff}}{l} \right) \right) \cdot (V_{bi} - 2\Phi_B) \quad (6\text{-}2),$$

as addressed in Section 6.2 (Figure 6-4(a)). This function form is derived from [13], where l is the characteristic length for the short-channel-effect calculation. D_{vbd0} and D_{vbd1} are model parameters. Similarly, the following equation

$$\eta_e(L_{eff}) = K_{1b} - K_{2b} \cdot \left(exp\left(-D_{k2b} \frac{L_{eff}}{2l} \right) + 2exp\left(-D_{k2b} \frac{L_{eff}}{l} \right) \right) \quad (6\text{-}3)$$

is used to account for the short channel effect on the backgate coupling, as described in Figure 6-4(b). D_{K1b}, D_{K2b}, K_{1b} (default 1) and K_{2b} (default 0) are model parameters.

The surface band bending, ϕ, is determined by the frontgate V_{GS} and may be approximated by

$$\phi = \begin{cases} \Phi_{ON} & \text{for } V_{GS} \geq V_T \\ \Phi_{ON} - \dfrac{C_{OX}}{C_{OX} + \left(C_{Si}^{-1} + C_{BOX}^{-1}\right)^{-1}} \cdot \left(V_T - V_{GS}\right) & \text{for } V_{GS} \leq V_T \end{cases} \qquad (6\text{-}4).$$

To improve the simulation convergency, the following single continuous function from subthreshold to strong inversion is used:

$$\phi = \Phi_{ON} - \frac{C_{OX}}{C_{OX} + \left(C_{Si}^{-1} + C_{BOX}^{-1}\right)^{-1}} \cdot N_{OFF,FD} V_t \cdot ln\left(1 + exp\left(\frac{V_{T,FD} - V_{gs\_eff} - V_{OFF,FD}}{N_{OFF,FD} V_t}\right)\right) \qquad (6\text{-}5).$$

Here V_{gs_eff} is the effective gate bias considering the poly-depletion effect. $V_{T,FD}$ is the threshold voltage at $V_{BS} = \Delta V_{bi}(\phi=2\Phi_B)$. $N_{OFF,FD}$ (default 1) and $V_{OFF,FD}$ (default 0) are model parameters introduced to improve the transition between subthreshold and strong inversion. V_t is the thermal voltage. Notice that the frontgate coupling ratio in the subthreshold regime approaches 1 as T_{BOX} approaches infinity.

To accurately model ΔV_{bi} and thus the device output characteristics, the surface band bending at strong inversion, Φ_{ON}, is not pinned at $2\Phi_B$. Instead, the following equation

$$\Phi_{ON} = 2\Phi_B + V_t \ln\left(1 + \frac{V_{gsteff,FD}\left(V_{gsteff,FD} + 2K1\sqrt{2\Phi_B}\right)}{moin \cdot K1 \cdot V_t^2}\right) \qquad (6\text{-}6)$$

is used to account for the surface potential increment with gate bias in the strong inversion regime [22]. Here *moin* is a model parameter. K1 is the body effect coefficient. Notice that a single continuous function,

$$V_{gsteff,FD} = N_{OFF,FD}V_t \cdot \ln\left(1 + \exp\left(\frac{V_{gs\_eff} - V_{T,FD} - V_{OFF,FD}}{N_{OFF,FD}V_t}\right)\right) \qquad (6\text{-}7),$$

has been used to represent the gate overdrive in Equation (6-6).

6.4 Verification - Index of Full Depletion

The BSIMPD parameter extraction methodology presented in Chapter 5 may still be used under the unified BSIMSOI framework, provided that the link between PD and FD, ΔV_{bi}, can be accurately extracted. As described in Section 6.2, a direct probe of ΔV_{bi} can be achieved by finding the onset of the external body bias (through a body contact) after which the threshold voltage and hence the channel current of the FD SOI device is modulated. When the body contact is not available, nevertheless, model parameters

related to ΔV_{bi} should be extracted based on the subthreshold characteristics of the floating-body device. As shown in Figure 6-7, the reduction of ΔV_{bi} with backgate bias is responsible for the transition from the ideal subthreshold swing (~ 60 mV/dec. at room temperature) to the non-ideal one.

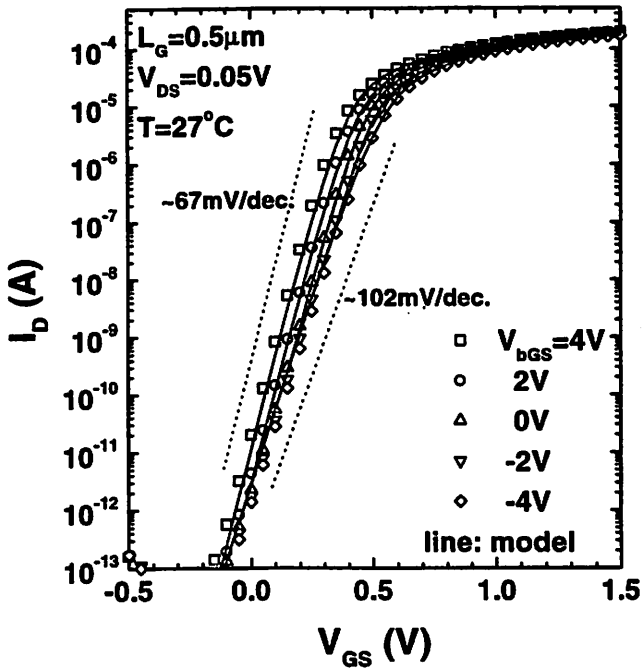

Figure 6-7. The PD/FD transition can be captured by modeling ΔV_{bi}.

Figure 6-7 clearly shows that the PD/FD transition can be captured by the ΔV_{bi} approach. In other words, ΔV_{bi} is indeed an index of the degree of full depletion, as pointed out in Section 6.2. As shown in Figure 6-8, larger floating-body effect can be observed for negative backgate bias due to smaller ΔV_{bi}. In case the ΔV_{bi} value is raised by charge sharing as described in Figure 6-4(a), it can be predicted that the short-channel device should exhibit less floating-body effect than the long-channel one due to larger ΔV_{bi}, as verified in Figure 6-9.

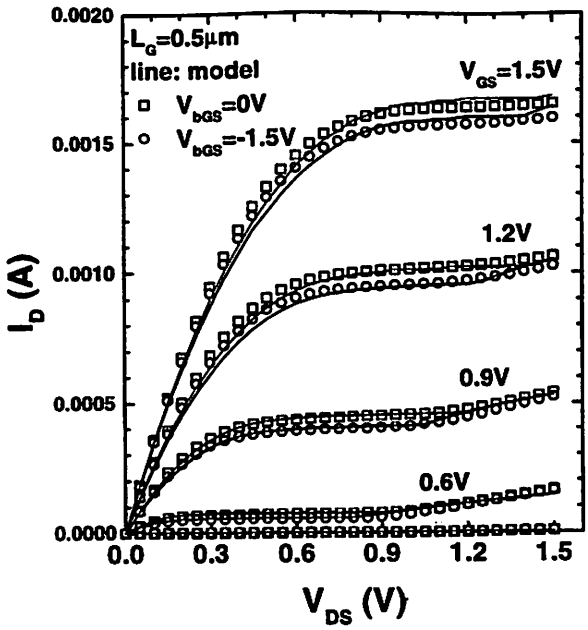

Figure 6-8. Larger floating-body effect can be seen for the negative backgate bias (source reference) due to smaller ΔV_{bi}.

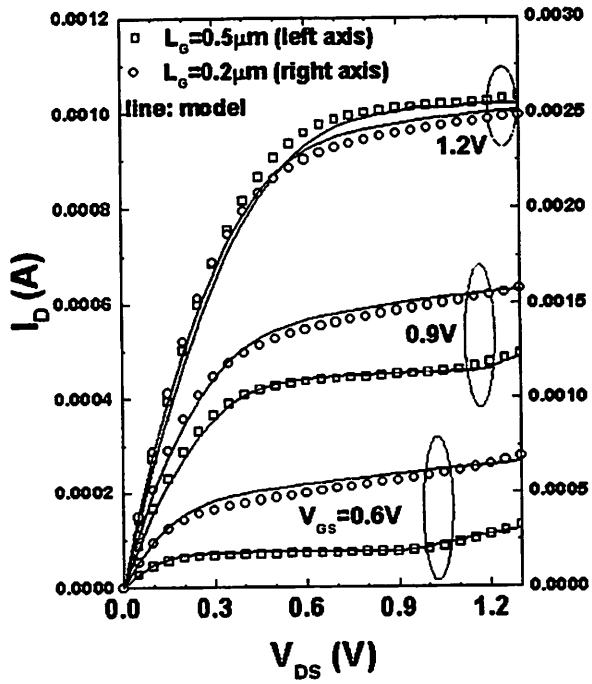

Figure 6-9. Less floating-body effect can be seen for the short-channel device due to larger ΔV_{bi}.

6.5 Summary

In this chapter, we have provided a viewpoint for the characterization of state-of-the-art thin film SOI MOSFETs. Based on *body-source built-in potential lowering*, the degree of full depletion can be quantified. In addition to serve as a measure of the floating-body behavior of SOI devices, the concept also enables the consolidation of PD and FD SOI compact models. This unified BSIMSOI model is crucial to the SOI circuit design due to the trend of coexistence of PD/FD devices in a single chip, which has become one of the biggest challenges in the scaling SOI CMOS.

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Chapter 7

Conclusion

Scaling and high performance advantages make SOI an important CMOS technology. However, the main barrier to full exploitation of SOI performance and power benefits is that the design of an SOI chip is a relatively risky process because the relative lacking of design experience makes it difficult to achieve fast turnaround and first-pass success. To facilitate the SOI circuit design process, we have developed BSIMSOI [1][2] – a SPICE model for accurate simulation of SOI circuits.

BSIMSOI has been implemented in Berkeley SPICE3f4 as well as many commercial circuit simulators such as HSPICE, SPECTRE, SmartSPICE and ELDO. This model has a direct impact on the semiconductor industry. For example, the Partial-Depletion (PD) mode of BSIMSOI, BSIMPD [1], contributed to the successful implementation of the 660-MHz 64-bit PowerPC [3] at its first design [4]. The EIA Compact Model Council [5] selected BSIMSOI as the standard SOI MOSFET model in December 2001.

Due to the SOI-specific floating-body effect, a physical understanding and modeling of the impact ionization phenomenon in state-of-the-art SOI devices is critical to a standard SOI MOSFET model. We have conducted research on the mechanism responsible for low voltage impact ionization in deep-submicrometer MOSFETs. Our study indicates that the driving force of impact ionization transitions from the electric field to the lattice temperature with power-supply scaling below 1.2 V. Due to its thermally assisted nature, the ionization rate in SOI MOSFETs is enhanced at high gate DC bias [6]. This effect needs to be considered in SOI modeling as well as hot-carrier reliability [7] due to the gap between the fast logic switching and the long thermal time constant [8]. The low voltage impact ionization behavior can be predicted by our thermal activation energy theory [9], which also explains the sub-bandgap kink in SOI out characteristics. In addition, a compact impact ionization model [10] has been developed based on the thermal activation energy theory to capture the SOI device characteristics with both thermally assisted impact ionization and electric field induced impact ionization accounted for. This model has been implemented in BSIMSOI.

We have also demonstrated the ability of BSIMPD to capture the history effect, a phenomenon that leads to excess design margin and therefore performance loss. With the aid of the physically accurate BSIMPD model, furthermore, we have investigated and analyzed the impact of gate-body tunneling on dynamic behaviors of PD SOI CMOS with emphasis on the history dependence of inverter delays [11]. This study suggests that the valence-band electron tunneling in the strong inversion regime has a significant

impact on the delay range and should be considered in SOI circuit simulation. For scaled SOI CMOS with supply voltage below 1 V, however, the floating-body effect such as the pass-gate leakage may be suppressed and the thin SOI body may show a tendency toward Full Depletion (FD) [12] due to the loss of majority carriers through the conduction-band electron tunneling in the accumulation regime.

This industry standard model represents various SOI technologies [4][8][13]-[15] and bridges manufacturing and design through extraction of the model parameters. Therefore, we have proposed a parameter extraction strategy for BSIMPD. We suggest that BSIMPD model parameters should be extracted from self-heating-free device characteristics. The thermal $R_{th}C_{th}$ circuit can be turned OFF in fast logic circuit simulation once the heating-free parameters are used [8]. A methodology for BSIMPD parameter extraction with emphasis on capturing the floating-body effect has also been proposed and verified [13][4].

Using BSIMPD as a foundation, we have developed a unified model for both PD and FD SOI circuit designs. Based on *body-source built-in potential lowering* [16], the degree of full depletion for thin film SOI MOSFETs can be quantified. In addition to servinge as a measure of the floating-body behavior of SOI devices, the concept also enables the consolidation of PD and FD SOI compact models. This unified BSIMSOI model is crucial to the SOI circuit design due to the trend of coexistence of PD/FD devices in a single chip, which has become one of the biggest challenges in the scaling SOI CMOS.

The unified BSIMSOI model is a generalization of BSIMPD. In other words, the unified model returns to BSIMPD when the body-source built-in potential lowering is negligible. On the other hand, it approaches the ideal FD mode (without floating body effect) when the built-in potential lowering is significant. Under this framework, BSIMSOI has provided n+2 node (i.e., 65 nm for 2005) readiness for SOI compact modeling. The current BSIMSOI model may also serve as a basis for future model development of thin-body and double-gate SOI MOSFETs.

Besides high performance microprocessor and low power logic, SOI CMOS technology with f_{max} up to 100 GHz has penetrated into the RF system-on-chip applications [17]. Notice that our modeling effort in BSIMSOI has mainly focused on the DC and transient behavior of SOI devices. It is therefore desirable to investigate and further extend BSIMSOI in the AC and high frequency regime around 10 GHz.

Finally, it is worth noting that BSIMPD is a generalization of BSIM bulk model in the forward body bias regime with two additional variables, body potential and device temperature. BSIMSOI may therefore be viewed as a unified bulk and SOI model. The advantage and importance of BSIMSOI may emerge with CMOS scaling. Notice that a significant impact on the output resistance due to self-heating has been observed in deep-submicron bulk MOSFETs [18]. Using active well with the emphasis of forward body bias to improve the speed/power of bulk CMOS has also been reported [19]. In addition, there is a growing requirement in the model accuracy of transistor body currents such as

impact ionization and junction leakages for bulk technologies. It remains to be seen whether this standard BSIMSOI model will also be used as a bulk model in the future.

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