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TOMOGRAPHY AS A METROLOGY TECHNIQUE FOR SEMICONDUCTOR MANUFACTURING

by

Michiel Victor Paul Krüger

Memorandum No. UCB/ERL M03/11

25 April 2003

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Tomography as a Metrology Technique for Semiconductor Manufacturing

by

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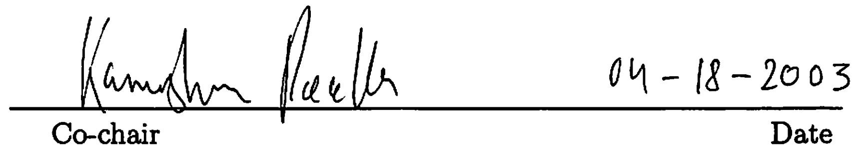

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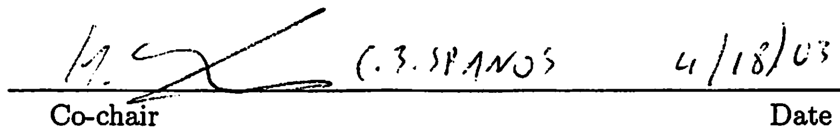

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Abstract

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This dissertation is concerned with exploring the feasibility of a class of sensors which provide temporally and spatially resolved wafer state information during semiconductor manufacturing. The common theme shared by this class of sensors is that they are based on Electrical Impedance Tomography (EIT). EIT is a non-destructive *in vivo* imaging technique principally used in medical applications.

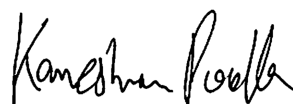
The basic idea of Electrical Impedance Tomography is to image the conductivity distribution in the interior of a conductive object by performing simple electrical measurements on the periphery of the object. In a semiconductor manufacturing context, physical and chemical effects during semiconductor manufacturing can induce a change in conductivity in the interior of a wafer. EIT techniques can be used to infer these conductivity changes. In turn, these changes can be related to the physical and chemical effects using appropriate models.

In this thesis, we first discuss the *status quo* of metrology methods in use in the semiconductor manufacturing industry. This discussion is followed by a thorough introduction to Electrical Impedance Tomography. We then argue that Electrical Impedance Tomography can be a compelling technique to obtain spatially and time-

resolved wafer state information during wafer processing. To illustrate these ideas, we design and analyze two EIT based sensors for use during semiconductor manufacturing.

Our first sensor is a device to measure etch rates or film thicknesses. We have designed, fabricated and tested this sensor. We use standard EIT techniques to estimate the conductivity distribution of a thin film of conductive polysilicon across a wafer. The estimated conductivity distribution can, in turn, be related to the thickness of the polysilicon film from first principles. Differential thickness measurements from our prototype etch rate sensor correlate very well with optical thickness measurements.

Next, we propose a novel EIT based sensor which can provide temporal and spatial wafer surface potential information during plasma processing. Our design relies on a resistive network containing discrete transduction elements whose conductivity is modulated by the variable of interest. To assess our idea, we performed simulation studies on a prototype sensor which uses depletion mode NMOSFETs as transduction elements. We have obtained promising simulation results with this novel EIT based metrology technique.



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To Michelle.

Contents

List of Figures v

List of Tables viii

List of Symbols ix

List of Acronyms xi

1 Introduction and Motivation 1
- 1.1 Introduction 1
- 1.2 The Holy Grail of metrology 2
- 1.3 Our metrology approach 3
- 1.4 Related work summary 4
- 1.5 Contributions of this dissertation 5
- 1.6 Thesis overview 6

2 Semiconductor Manufacturing Metrology: an overview 7
- 2.1 Semiconductor manufacturing 7
- 2.2 The role of metrology 11
- 2.3 Metrology: the status quo 13
- 2.4 Metrology: the future 19

3 Electrical Impedance Tomography: an overview 22
- 3.1 Operating principle 23
- 3.2 The governing equations 24
  - 3.2.1 The generic EIT experiment 24
  - 3.2.2 Notation 25
  - 3.2.3 The continuum model 25
  - 3.2.4 Modeling assumptions 27
- 3.3 The forward problem 28
  - 3.3.1 Analytical solution 28
  - 3.3.2 Finite element modeling 30

3.3.3 Finite element example 33
3.3.4 Simulation example 34
3.4 The inverse problem 35
3.4.1 Degrees of freedom 36
3.4.2 Parameterizing the conductivity profile 37
3.4.3 Kriging 37
3.4.4 Optimization 40
3.5 EIT example 42

4 EIT based Sensors for Semiconductor Manufacturing 48
4.1 The basic idea 49
4.2 An example 50
4.3 Three-stage approach 52
4.4 Design and implementation issues 54

5 Etch processes in Semiconductor Manufacturing: an overview 57
5.1 Etch processes 57
5.2 Wet etching 58
5.3 Plasma etching 59

6 EIT based Etch Rate Sensors 62
6.1 Motivation 63
6.2 Related work 65
6.2.1 Optical methods 65
6.2.2 Sensor wafers 67
6.3 Etch rate sensor: design and operation 68
6.3.1 Wafer design 68
6.3.2 Process flow 70
6.3.3 Experimental setup and hardware 71
6.4 Experimental results: XeF_2 etchant 72
6.4.1 Wafer design 73
6.4.2 XeF_2 etcher 73
6.4.3 Experimental details 74
6.4.4 Results 75
6.5 Experimental results: wet silicon etchant 76
6.5.1 Wafer design 76
6.5.2 Experimental details 77
6.5.3 Results: absolute measurements 77
6.5.4 Results: differential measurements 81
6.6 Discussion of results 84

7 EIT based Plasma Potential Sensors 89
7.1 Motivation 90
7.2 Related work 93
7.3 EIT: a resistive network approach 96
7.3.1 Downsides continuous EIT problem 96
7.3.2 Resistive networks 97
7.4 Sensor design and operation 98
7.4.1 Three stage approach 98
7.4.2 MOSFET operation 99
7.4.3 Depletion-mode NMOSFET 101
7.4.4 Wafer design and operation 104
7.5 Simulation results 105
7.5.1 Experimental details 106
7.5.2 Algorithm details 107
7.5.3 Simulation 1 107
7.5.4 Simulation 2 109
7.6 Conclusions 111

8 Conclusions 113
8.1 Dissertation summary 113
8.2 Future research 114

Bibliography 116

A Galerkin Method for a Single Triangular Element 129

B Extrapolation and Interpolation Using Kriging 133

C Code used in Hspice EIT Algorithm 136
C.1 `runtotal`: main program to perform EIT estimation (Perl) 136
C.2 `runspicetotal`: update and run spice simulation (Perl) 138
C.3 `matbg`: run Matlab in background (Shell script) 139
C.4 `runmatlab.m`: update gate potentials after each iteration (Matlab) . . 140
C.5 `main.sp`: main netlist (Hspice) 141
C.6 `vgate_org.sp`: original gate potentials (Hspice) 142
C.7 `common.sp`: network interconnection (Hspice) 142

List of Figures

2.1 Different locations for metrology tools (indicated by 'M') in the semiconductor manufacturing process. 15

3.1 The generic EIT setup 25
3.2 A disc of uniform conductivity (a) and a disc with a circular anomaly centered around the origin (b). 29
3.3 A conformal mapping can map an off-centered circular anomaly to a centered anomaly. 30
3.4 Characteristic function χ_i for an arbitrary triangular finite element discretization. 31
3.5 Simple hexagonal object containing 6 equilateral finite elements. . . . 33
3.6 A disc of uniform conductivity with two point current sources on the boundary. 34
3.7 Analytical and numerical solution to the Laplace equation on a circle for different Neumann boundary conditions. 35
3.8 Top: the left panel shows the real conductivity in Equation (3.13) across the unit disk; the right panel shows the spatial error between the true conductivity and the conductivity estimated with the Kriging algorithm. Bottom: the left panel shows the true (solid) and estimate (dashed) conductivity along various cross sections of the unit disk (see right panel). 39
3.9 Generic process flow in EIT to estimate the conductivity profile inside the object of interest. 43
3.10 The true conductivity distribution (left) and the estimated conductivity distribution (right). 44
3.11 The left panel shows the true (solid) and the estimated (dashed) conductivity distribution, as well as the least squares projection (dotted) along various cross sections of the unit disc (see right panel). 46

4.1 Schematic of four-point probe setup. 51
4.2 Schematic of three-stage approach. 53

5.1 Basic plasma etching system [80]. 60

6.1 Schematic of EIT based etch rate sensor 69
6.2 Picture of finished sensor wafer. 70
6.3 An edgeboard connector (left) connects the DAQ system to special pads at the perimeter of the wafer (right). 72
6.4 Mask used in XeF_2 experiment. Dark areas are etched in the experiment and should, hence, show a decrease in conductivity over time. . 73
6.5 Change in conductivity for different areas on wafer: estimated (solid) and four-point probe data (dashed). 76
6.6 Location of thickness measurement sites. 78
6.7 Noise distribution around mean potential pattern for different etching times. 79
6.8 Thickness at measurement sites according to optical metrology (solid) and EIT sensor (dashed). 80
6.9 Distribution around mean of the estimated parameters for different etching times. 81
6.10 Change in thickness at measurement sites according to optical metrology (solid) and EIT sensor (dashed). 82
6.11 To assess the spatial measurement capabilities of our sensor, we analyze the change in thickness along the cross sections of the polysilicon disk shown here. 83
6.12 Cross sectional view of change in thickness after 45 sec: optical (solid), EIT (dashed). 84
6.13 Cross sectional view of change in thickness after 75 sec: optical (solid), EIT (dashed). 85
6.14 Change in thickness in Å after 45 sec; optical (left), EIT sensor (right). 86
6.15 Change in thickness in Å after 75 sec; optical (left), EIT sensor (right). 87
6.16 Cross sectional view of change in thickness as measured with EIT sensor after 45, 75, 105, 135 and 165 seconds. 87
6.17 Change in thickness, estimated by the EIT sensor at the 36 measurement sites, vs time. 88

7.1 A uniform plasma is characterized by a balanced flow of ion and electron fluxes across the sheath (a). In a nonuniform plasma, these fluxes are, at least initially, not balanced (b). Accumulation of charge at the wafer surface can balance the ion and electron fluxes (c) or it can result in a Fowler-Nordheim current through the dielectric material (d) [35]. 90
7.2 Antenna effect (left) and its electrical circuit equivalence (right) [35, 33]. 91
7.3 Schematic of Langmuir probe used for plasma diagnostics. 93
7.4 Generic resistive network on wafer. 98
7.5 Schematic cross section of NMOSFET. 100

7.6 Schematic cross section of depletion NMOSFET (top left). Circuit diagram utilized in Hspice simulations (bottom left) to compute the resistance of the depletion mode NMOSFET for different values of V_{GB} and V_{BS}, $V_{DS} = 0.01$ `volts` (right). 102
7.7 Simulations revealing nonlinear behavior of depletion-mode NMOSFETs 103
7.8 Simulation results with the resistive network of 6 depletion mode NMOSFETs shown in the top left panel. The top right panel shows the estimated gate potential after each iteration in the nominal case, i.e. without noise. The bottom left panel shows the error between the mean gate potential and the "true" gate potential for different noise levels. The bottom right panel shows the standard deviation of the estimated gate potentials versus the noise level. 109
7.9 Simulation results with the resistive network of 10 depletion mode NMOSFETs shown in the top left panel. The top right panel shows the estimated gate potential after each iteration in the nominal case, i.e. without noise. The bottom left panel shows the error between the mean gate potential and the "true" gate potential for different noise levels. The bottom right panel shows the standard deviation of the estimated gate potentials versus the noise level. 110

A.1 Linear interpolation function used in single finite element. 130

B.1 Kriging is concerned with predicting the optimal value for y_0 at an unobserved location, given measurements $y_i, i = 1, \ldots, N$ at selected locations. 133

List of Tables

3.1 Hot spot parameters used in the EIT example. 44

3.2 Estimated parameter values α_{ij} for the various experiments discussed in the text. 47

7.1 Estimated gate potentials in `volts` for the various simulations performed on the resistive network containing 6 depletion mode NMOSFETs. 108

7.2 Estimated gate potentials in `volts` for the various simulations performed on the resistive network containing 10 depletion mode NMOSFETs. 111

List of Symbols

A	Ratio of A_f to A_g
A_f	Antenna area above field oxide
A_g	Antenna area above gate oxide
$\mathbf{B}(\mathbf{r})$	Magnetic field vector at $\mathbf{r}$
C_f	Capacitance of antenna structure over field oxide
C_g	Capacitance of antenna structure over gate oxide
C_{total}	Total capacitance of antenna structure over field and gate oxide
δ	Dirac pulse
e_l	Portion of $\partial\Omega$ covered by l-th electrode
$\mathbf{E}(\mathbf{r})$	Electrical field vector at $\mathbf{r}$
$\mathbf{E}(\boldsymbol{\sigma})$	Cost function in inverse EIT problem
ϵ	Electrical permittivity
ϵ_{ox}	Electrical permittivity of oxide
$I_{\text{F-N}}(V_{ox})$	Fowler-Nordheim current
I_k	Current entering or leaving through the k-th electrode
$\mathbf{J}$	Jacobian matrix
J_k	Current density at k-th electrode
$\mathbf{J}(\mathbf{r})$	Current density vector at $\mathbf{r}$
L	Number of electrodes placed at periphery of object
λ	Lagrange Multiplier

μ	Magnetic permeability
$\hat{\mathbf{n}}(\mathbf{r})$	Unit normal at points on $\partial\Omega$
N	Number of unknown parameters in inverse EIT problem
N_n	Number of nodes used in FEM approximation
Ω	Interior of the object
$\partial\Omega$	Boundary of the object
Q_{total}	Total accumulated charge per unit area
$\mathbf{r}$	Position vector of a point in Ω
R	Residual in FEM approximation
R_s	Sheet resistance
ρ	Resistivity of material or film
$\boldsymbol{\sigma}$	Parameterized conductivity distribution
$\sigma(\mathbf{r})$	Conductivity of the object at $\mathbf{r}$
t	Film thickness
t_f	Field oxide film thickness
t_g	Gate oxide film thickness
$u(\mathbf{r})$	Electrical potential at $\mathbf{r}$
$\mathbf{U}(\boldsymbol{\sigma})$	Vector of predicted electrode potentials
$\mathbf{V}$	Vector of observed electrode potentials
V_g	Potential across gate oxide
V_{ox}	Potential across oxide
w	Weighting function used in FEM approximation
χ_i	i-th characteristic function
Y	Conductance matrix

List of Acronyms

AC	Alternating Current
BEM	Boundary Element Method
CD	Critical Dimension
COO	Cost of Ownerhsip
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CCW	Counter Clock Wise
DAQ	Data Acquisition
DOF	Degrees of Freedom
DC	Direct Current
DUV	Deep Ultra Violet
EEPROM	Electrically Erasable Programmable Read-Only Memory
EIT	Electrical Impedance Tomography
FDM	Finite Difference Method
FEM	Finite Element Method
FET	Field Effect Transistor
F-N	Fowler-Nordheim
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
LS	Least Squares

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOSFET	N-type MOSFET
OEE	Overall Equipment Efficiency
PDE	Partial Differential Equation
PM	Preventive Maintenance
PMOSFET	P-type MOSFET
RF	Radio Frequency
RIE	Reactive Ion Etching
RtR	Run-to-Run
SEM	Scanning Electron Microscope
SPC	Statistical Process Control
TC	Thermocouple
UV	Ultra Violet

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Chapter 1

Introduction and Motivation

1.1 Introduction

Over the last three decades, we have witnessed increasing productivity in semiconductor manufacturing at a pace unprecedented in industrial history. The semiconductor industry has shown the remarkable and sustained capability to continuously increase the number of transistors per unit area without additional cost. This trend was first observed by Intel's co-founder George E. Moore and is often referred to as Moore's law [70].

The semiconductor industry uses highly specialized, advanced production tools and processes to print millions of transistors on each chip. With each new generation, the complexity and cost of these tools and processes increase rapidly. If the industry is to continue Moore's law, it must adopt advanced monitoring and control technologies to maintain equipment and processes within tight operating specifications. For this, there is widespread consensus that metrology will play an *enabling* role [91]. This is critical for 300 mm substrates where maintaining across-wafer process uniformity is particularly challenging.

Currently, off-line, in-line, and in-situ metrology techniques are used to monitor, diagnose, and control semiconductor manufacturing processes. Off-line metrology

inspects occasional wafers sampled from production runs. In-line metrology inspects every wafer upon completion of the process. In-situ metrology offers the ability to monitor conditions during actual processing.

These existing metrology choices have proven to be invaluable in reducing wafer-to-wafer and lot-to-lot product variability through improved process monitoring. These choices do not adequately address within wafer process variability. Within wafer uniformity becomes increasingly vital as the industry moves towards larger substrates and finer linewidths. This manufacturing requirement can only be met by a novel metrology paradigm: sensors that can provide spatially and time-resolved *wafer state* information.

1.2 The Holy Grail of metrology

The semiconductor industry is risk sensitive and reluctant to adopt novel metrology technologies unless they provably address concerns of process stability, tool contamination and ownership costs. To realize widespread adoption in high-volume semiconductor manufacturing facilities, novel metrology technologies must offer the following attributes:

- *Spatial and temporal wafer state information*

  Current in-line and in-situ metrology provide the necessary process state information to obtain wafer-to-wafer and lot-to-lot uniformity. However, as feature sizes shrink even further, within wafer uniformity becomes critical. As a result, spatially resolved wafer state information has now become necessary.

- *Cost effective reliable integration*

  The integration of metrology tools with process tools often requires significant software and hardware modifications. This can be time-consuming, expensive, and can compromise equipment reliability. It can also affect process stability

and can make production tools more vulnerable to false alarms due to metrology errors. Consequently, the large initial capital investment and the increased operating costs of metrology integration must be justified by the anticipated financial gains resulting from improved process capabilities and increased yields.

- *Ease of deployment*

  In many processes periodic wafer state measurements suffice to ensure process uniformity and repeatability. In these situations, the costs associated with permanent integration of the necessary metrology can not be justified. However, taking the tool off-line for inspection and calibration can also be prohibitively expensive. Hence, there is a need for simple and rapid metrology techniques which can be periodically deployed without making any modifications to the process tool.

- *No influence on process*

  The semiconductor industry expends considerable resources on maintaining an ultra-clean production environment to prevent catastrophic yield loss due to contamination. Any serious metrology choice should not contaminate the process being sensed. In addition, the metrology tool itself should not affect the process or distort the variables being sensed.

1.3 Our metrology approach

In this dissertation, we will investigate the feasibility of a class of sensors for semiconductor manufacturing applications. The common theme shared by this class of sensors is that they are based on Electrical Impedance Tomography (EIT), an *in vivo* imaging technology that has found widespread use in biomedical applications.

The basic idea of Electrical Impedance Tomography is to image the conductivity distribution in the interior of a conductive object by performing simple electrical

measurements on the periphery of the object. For example, in the human body different tissues and organs are characterized by different conductivity values. Hence, being able to image the conductivity distribution inside the human body allows us to pinpoint the locations and geometry of different organs and/or tissues.

In a semiconductor manufacturing context, physical and chemical effects during semiconductor manufacturing can induce a change in conductivity in the interior of a wafer. If we can measure these conductivity changes in the interior of the wafer with EIT techniques, we can infer the physical and chemical effects which cause these changes. The principle objective of this dissertation is to investigate the feasibility of metrology methods based on Electrical Impedance Tomography techniques to provide real-time, spatially resolved wafer state information.

1.4 Related work summary

The need for spatially resolved wafer state information has led to the development of a variety of sensor wafers. Simple wafer designs that employ an array of passive sensors to measure peak wafer state values during processing have been studied [62, 106, 76]. These wafers are easy to employ and are attractive for use in high volume manufacturing facilities. However, these wafer cannot provide time-resolved wafer state information. To address this drawback, a variety of tethered wafers have been developed to measure wafer states such as temperature, potential, etch rate and ion flux [92, 63, 6, 40, 53]. However, the tether prohibits facile loading of the sensor wafer with standard wafer handling robotics. Consequently, their use is limited to tool development and scheduled preventive maintenance. This serious shortcoming can be addressed by recently developed autonomous sensor wafers. The feasibility of this approach was demonstrated with several proof-of-concept wafer designs [41, 42, 40]. In addition, issues which have been addressed or which are currently under investigation by other groups are the power supply [18], encapsulation [112] and communication

schemes [78, 58]. Autonomous sensor wafers for temperature metrology are now commercially available [75].

1.5 Contributions of this dissertation

In this dissertation, we have developed a novel *class* of sensors for use during semiconductor manufacturing. These sensors exploit the spatial imaging capabilities of Electrical Impedance Tomography (EIT) to obtain spatially resolved wafer state information. EIT is a non-destructive *in vivo* imaging technique principally used in biomedical applications. To the best of our knowledge, the use of EIT techniques in semiconductor manufacturing applications as suggested in this dissertation is novel.

The essential idea in our approach is to place electrodes at the periphery of a wafer. We then perform simple electrical measurements. From these measurements, we infer the conductivity distribution inside the wafer, which, in turn, can be related to the variable of interest through simple physical or chemical models.

To illustrate our ideas, we discuss the design, fabrication and operation of a prototype etch rate sensor. Measurement data from this prototype etch rate sensor corresponds well with optical film thickness measurements. In contrast with traditional EIT applications, in our sensor wafer context we have the luxury of designing the interior of the object being imaged. In this dissertation we exploit this observation by applying EIT techniques to a resistive network containing discrete transduction elements. This approach allows us to circumvent some of the drawbacks associated with traditional EIT techniques. To illustrate our approach, we have designed a prototype sensor to measure the potential induced by a plasma at the wafer surface. We offer promising simulation results with this novel approach to EIT to validate our ideas.

1.6 Thesis overview

The remainder of this thesis is organized as follows. In Chapter 2 we provide an overview of the various metrology methods currently used in semiconductor manufacturing. We also summarize the challenges faced by the industry, and the role metrology will play to address these challenges. In Chapter 3 we offer a thorough introduction to Electrical Impedance Tomography. We discuss both theoretical and numerical aspects and illustrate our discussion with several simple examples. In Chapter 4 we describe how EIT techniques can be used in the context of semiconductor manufacturing. In particular, we discuss a class of autonomous sensor wafers which employ EIT techniques to obtain spatially and temporally resolved *wafer state* information. In Chapter 5 we provide a brief overview of etching processes in semiconductor manufacturing, and discuss the principal technological challenges that arise in this context. This discussion offers a compelling case for the development of spatially resolved sensor wafers for use during semiconductor manufacturing. In Chapter 6 we describe the design, fabrication and testing of such a prototype sensor wafer: an EIT based etch rate sensor. In Chapter 7 we discuss our results in developing a second prototype sensor employing EIT techniques: a sensor which measures the potential at the wafer surface during plasma etching. Finally, in Chapter 8 we offer a summary of this dissertation and draw some conclusions based on our research experience. We close by suggesting recommendations for future research.

Chapter 2

Semiconductor Manufacturing Metrology: an overview

This chapter offers an overview of semiconductor manufacturing metrology. After a brief discussion of the industry trends, the role of metrology in this industry is discussed. This is followed by a survey of currently available metrology choices. Finally, the future of metrology is discussed. In particular, the concept of autonomous sensor wafers is introduced.

2.1 Semiconductor manufacturing

Semiconductor manufacturing is a complex process involving the selective deposition and removal of thin films of different materials in order to create devices with millions of three-dimensional components (transistors, capacitors, resistors etc.). On completion of these individual components, similar fabrication techniques are used to interconnect them to create Integrated Circuits (ICs). The integration of enormous numbers of components onto a single chip results in higher circuit performance, greater functionality, and increased reliability, all at very low unit cost.

For more than three decades, the semiconductor manufacturing industry has been

able to reduce the smallest printable features on the wafer, allowing them to double the number of transistors per device at no additional cost every 18 months [70, 91]. This trend is called Moore's law, after Intel's co-founder George E. Moore. Moore's law has become a self-fulfilling prophesy and competitive forces compel the IC industry to maintain this trend. To this end, the IC industry is continuously improving the performance of the manufacturing processes and tools. These performance enhancements focus principally on the ability to consistently print smaller features, more reliably, and across larger substrates.

The following trends are discernible in modern semiconductor manufacturing:

1. *More advanced processing tools*

   Equipment manufacturers spend billions of dollars on the development of advanced production tools which are capable of printing smaller features. The development of plasma etching tools is a good illustration of this trend. A simple plasma etching tool applies an RF power between two parallel plates to create a plasma discharge. The chemical and ionic species in this plasma will then selectively etch a wafer which is placed on one of the electrodes (see Chapter 5 for more details). Reducing the pressure in the etch chamber improves the directionality of the ionic species which bombard the wafer surface, resulting in more vertical profiles. However, lower operating pressures result in lower plasma densities, which, in turn, reduce the etch rate. Increasing the RF power between the parallel plates to compensate for the decrease in etch rate can cause undesirable damage at the wafer surface. To counteract this coupling between plasma density and ion energy, the semiconductor industry has adopted high-density plasma etchers. These etchers employ an Inductively Coupled Plasma (ICP) source to generate a high density plasma. A second RF source controls the energy of the ions bombarding the substrate by adjusting the bias between the wafer and the plasma. These high density plasma etchers can operate at lower pressure, resulting in more vertical sidewalls, while maintaining high ion

fluxes and etch rates.

2. *New materials*

   In addition to smaller features, IC manufacturers also rely on new, exotic materials to boost the performance of their devices. For example, aluminum is replaced by copper to reduce resistive losses in long wires and low-k dielectric materials are used instead of SiO_2 to reduce the parasitic capacitance and cross talk between conductors. These new materials, however, often require completely new and innovative fabrication processes and tools, further increasing the costs of IC manufacturing.

3. *Larger wafers*

   Processing costs per wafer are relatively independent of wafer size. Hence, in order to compensate for the rising costs, the semiconductor industry has steadily moved to larger diameter wafers, allowing more chips to be fabricated simultaneously. Currently, 200 mm wafers are the standard in most production facilities, while 300 mm wafers are gradually being adopted in state-of-the-art facilities. These larger substrates offer 240% more die per wafer, 30% lower costs per die, all while reducing energy and chemical consumption by 40% [49]. This has the added and important benefit of reducing the environmental impact of semiconductor manufacturing.

Previous trends have helped the semiconductor manufacturing industry to keep pace with Moore's law. However, the emerging consensus is that Moore's law may break down in the near future if the industry does not adequately deal with the following two challenges:

- *Reliable pattern transfer*

  High volume production facilities are currently capable of printing 0.13 μm lines while research groups have recently shown that it is possible to print features

as small as 15 nm. Hence, further device scaling is technically feasible. However, efficient and cost-effective fabrication of these smaller devices will prove extremely challenging. The focus in the near future will, therefore, be on the reliable pattern transfer of smaller features on larger wafers.

- *Shorter time-to-market*

  The current IC market is characterized by intense competition and short product cycles. This results in rapid price erosion of new products, providing IC manufacturers with a small window of opportunity to recoup their large capital investments. Therefore, minimizing the time-to-market is particularly critical in this industry. To this end, IC manufacturers will have to ramp up production of new generations of devices quickly, while achieving high production yields.

In order to address these challenges, it is very important to obtain a thorough understanding of how equipment and processes affect the wafer surface. This information can then be used to adjust equipment and processes, improving product uniformity, throughput and yield. In addition, it is imperative to monitor processes vigilantly allowing early detection of undesirable process drifts. In current practice, IC manufacturers sample a few wafers per batch with high end metrology tools. However, as process specifications tighten, it will be necessary to sample each wafer in order to detect small process disturbances. Spatial wafer metrology can also reveal deterministic offsets and disturbances, enabling advanced feedforward and feedback control algorithms to compensate for these effects. Hence, there is widespread agreement that the IC industry will become more dependent on accurate, real-time metrology to improve their processes and to accelerate time-to-market and time-to-yield. In fact, in its latest technology roadmap, SEMATECH (an international consortium of IC manufacturers and tool suppliers) calls metrology an *enabler* for the introduction of future technology generations [91].

2.2 The role of metrology

Metrology is an indispensable ingredient of the semiconductor manufacturing process. It provides valuable wafer state information during and after each processing step. This information is used for:

- *Process design*

  Every process has to be thoroughly characterized before it is adopted by IC manufacturers in high-volume production. As a result, large numbers of test wafers are subjected to different processing conditions and the resulting state of each test wafer is recorded. A properly designed experiment can then provide the process engineer with a model which relates the variable of interest to the different processing parameters. For example, the etch rate in a plasma etcher depends on many variables such as gas flows, pressures, RF powers and wafer temperature. In order to characterize this process, process engineers perform factorial design experiments, changing process parameters one at a time. The observed etch rate information then yields a model which relates processing parameters to the etch rate. This model can, in turn, assist process engineers in optimizing the process and establishing the sweet spot where throughput is maximized while maintaining a stable and uniform process across the wafer.

- *Process validation*

  Processing tools are designed to be very repeatable. However, small disturbances invariably cause the process to drift over time. Therefore, a small number of production wafers in each batch is sampled to ensure that the process is still within specifications. For example, during plasma etch and deposition processes the walls of the reactor are in direct contact with the plasma. As a result, changes in wall conditions due to residue build-up can affect plasma properties such as ion density, reactive species concentrations and electron temperatures [44]. These changes in plasma properties can cause a shift in etch rate and/or

uniformity, selectivity and anisotropy.

- *Process control*

  In the early days of semiconductor manufacturing, IC manufacturers relied on the robustness of the process and the repeatability of production tools to keep their processes within specifications. Once dialed in, recipes remained fixed until a large excursion of a critical parameter was detected. However, shrinking critical dimensions (CDs) forced the IC industry to take a more proactive approach to improve yield and to reduce variability in the process. This has led to the adoption of Statistical Process Control (SPC) [69] and Run-to-Run (RtR) control algorithms [74, 83, 57]. Here, a small number of wafers in each batch is measured and the observed data is used to make small adjustments to critical processing parameters, closing the control loop around the process. RtR techniques allow IC manufacturers to make small adjustments to their processes more frequently, reducing process variance, improving disturbance rejection and enhancing overall process yield. Successful applications of RtR control include chemical mechanical polishing (CMP), etching and lithography [13, 47, 12]. Larger diameter wafers and tighter process specifications increase the economical risks of process drifts, failures and nonuniformities. Consequently, the IC industry is moving rapidly towards ubiquitous process control.

- *Equipment diagnosis and maintenance*

  During IC manufacturing equipment characteristics change as parts wear out or age, causing a slow drift in process performance. Early detection of these drifts is vital to minimize the number of lost product wafers. In addition, a rapid assessment of the root cause can reduce tool-downtime, increasing overall equipment efficiency. To this end, sensors built into the tool continuously record the tool state during processing. Tool failures often cause abrupt changes in tool states. Consequently, tool state sensors can often detect tool failures as

they happen, minimizing lost lots.

Preventive maintenance (PM) results in tool-downtime. However, a prolonged time without tool maintenance increases the risk of an abrupt tool failure. Thus, PM scheduling is a challenging task, trading lost production for tool reliability. Slow variations and drifts in tool states within certain bounds are in general acceptable. However, as certain tool states approach or exceed those bounds PM is necessary. Hence, tracking of tool states over many process runs provides a means of scheduling the PM events.

- *Equipment design*

  Minor changes in tool geometries can significantly affect the overall process performance and uniformity. Ideally, numerical simulations could be used to reveal these effects, allowing tool manufacturers to quickly optimize their design. However, process and tool complexity often preclude accurate and rapid numerical simulations [81]. Hence, in many cases tool manufacturers continue to rely on test wafers to assess their tool designs.

The variety of applications discussed above clearly shows the importance of metrology during semiconductor manufacturing. From initial tool design to high-yield volume production, metrology provides vital wafer state information. It assists process engineers in optimizing both equipment and processes and it reduces time-to-yield and the associated costs of lost products in high volume manufacturing facilities.

2.3 Metrology: the status quo

Both IC manufacturers and equipment suppliers rely on metrology to characterize and optimize equipment and processes, allowing larger wafers to be uniformly processed while increasing throughputs. In response, metrology vendors have developed a variety of tools to meet the different market needs. This section will discuss in more detail the various metrology choices currently available.

Traditionally, the semiconductor manufacturing industry has used off-line metrology to verify proper operation of the fabrication tools and to control the fabrication process. Here, from every batch production a select number of wafers is inspected with special, very accurate metrology tools, see Figure 2.1(a). However, these tools are expensive, occupy valuable real-estate within the fabrication facility and introduce a significant delay in the overall fabrication process. In addition, some metrology tools are destructive, resulting in yield-loss. A cross-sectional Scanning Electron Microscope (SEM) is a good example of an off-line metrology tool. This tool employs a focused beam of high energy electrons to obtain cross-sectional images of a processed wafer with a resolution below 5 nm [80]. These images provide valuable profile information to process engineers, allowing them to adjust and/or optimize the process appropriately.

Over the last five years, semiconductor manufacturing practice has evolved from using off-line metrology to using in-line metrology. Where possible, stand-alone metrology tools have been replaced with integrated metrology tools which are placed in proximity to or mounted on production tools, see Figure 2.1(b). These integrated metrology tools allow every wafer to be inspected after processing as opposed to just a fraction as is the case with off-line metrology. The benefits of this shift are numerous: the large amount of process data allows continual process monitoring, earlier fault detection and more frequent adjustments to the process, resulting in reduced process variance. In-line metrology also results in improved throughput: instead of removing selected wafers for off-line metrology, all wafers can, after inspection, continue to the next processing step.

Optical techniques such as scatterometry and ellipsometry are the technologies of choice for integration as they provide the desired precision and accuracy without impacting the tool throughput or affecting the process itself. Consequently, metrology vendors work closely with equipment manufacturers to incorporate optical metrology capabilities into production tools.

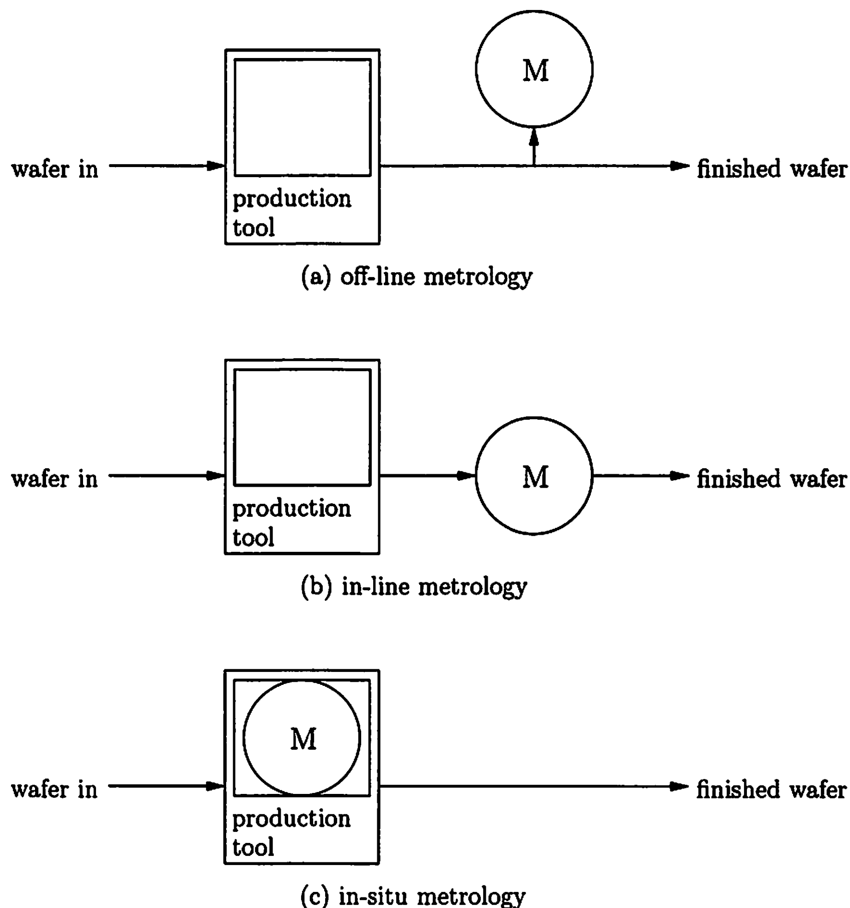

Figure 2.1: Different locations for metrology tools (indicated by 'M') in the semiconductor manufacturing process.

Although in-line metrology offers significant benefits, the associated ownership and operating costs can be significant. In addition, equipment engineers are often reluctant to deploy additional sensors and associated hardware to existing tools as these changes could affect process stability and possibly void equipment warranties. Processing tools also become more vulnerable to false alarms due to metrology errors and/or failure.

Both off-line and in-line metrology provide information about the *time-integrated* effect of the process of interest on the wafer, i.e. they can not detect within-process transients. For example, the pattern in DUV photoresists after post-exposure bake is very sensitive to the total thermal budget of the baking step: small variations in tran-

sient temperature characteristics can have a significant influence on the final profile [80]. In order to characterize the post-exposure bake step, test wafers covered with photoresist and the desired pattern are baked at different temperatures over different times. Post-exposure bake profile information is then used to deduce the effect of temperature and time on the photoresist profile. In this analysis it is assumed that the wafer temperature is constant during the bake. However, in reality the wafer will experience some heating and cooling transient effects when placed on and removed from the bake plate. This will translate into small variations in photoresist profiles across the wafer. This test-wafer approach cannot adequately address these transient effects. Real-time wafer temperature measurements offer a superior solution as they offer the time-resolved data necessary to account for and control these transient temperature effects.

Today, most processing tools are equipped with sensors to measure process variables such as pressures, gas flows, RF powers and wall/chuck temperatures in-situ, see Figure 2.1(c). Changes in these variables can seriously affect the resulting process near the wafer and these variables must therefore be controlled within tight specifications. However, the relation between tool state and wafer state is rather complex and requires extensive experimental modeling [8].

Active monitoring and control of *process states* is necessary to obtain uniform results between wafers and lots. However, this approach is insufficient for sub 0.15 μm linewidths on 300 mm wafers. For these dimensions, within wafer uniformity control becomes critical. For example, during plasma etching micro-loading effects become more pronounced as CDs shrink, i.e. dense line patterns exhibit reduced etch rates compared to isolated line patterns. Aggregate plasma state information is too coarse to reveal these effects. Consequently, there is a need to monitor the *wafer state*, i.e. process conditions at the wafer surface.

Recent research efforts have focused on the development of in-situ wafer state metrology, see Figure 2.1(c). Where possible, wafer state information is acquired in

real-time during wafer processing, for example by optical and acoustic techniques. Among the wafer variables measured with these techniques are wafer temperature and etch/deposition rate [85, 8, 79, 59].

Both optical and acoustic techniques provide accurate wafer state information. However, both technologies require hardware changes to the tool. Optical techniques require viewports for direct line-of-sight access to the wafer. Acoustic techniques rely on intimate mechanical contact between the backside of the wafer and a transducer/receiver pair mounted on rods. This requires the use of a modified wafer chuck. In addition, neither technique readily provides spatially resolved wafer state information. Optical techniques focus in general on a small area of the wafer surface while acoustic techniques obtain an average value of the wafer state due the large distance between the transducer/receiver pair.

With the widespread adoption of larger wafers, it becomes increasingly critical to maintain process uniformity across these larger substrates. Edge effects become critical with devices being produced within 2 mm of the wafer's edge. Consequently, IC manufacturers devote significant resources to optimize process recipes to guarantee across-wafer uniformity. For this, spatially resolved wafer state information is essential. This interest in spatially resolved wafer state information has led to the development of special *passive* sensors to measure peak wafer state values during processing. These passive sensors rely on a physical or chemical effect to induce a permanent change in sensor properties once the variable of interest exceeds a threshold value. An array of these sensors is then mounted or fabricated onto a test wafer and subjected to the process of interest. Upon completion, each sensor can be inspected and the maximum spatial wafer state can be assessed.

For example, CHARM II wafers have been developed to provide information about wafer charging damage due to non-uniform plasma processes. Non-uniform wafer charging can have a serious impact on process yields (see Chapter 7) and is, therefore, a major concern for high volume IC manufacturers. CHARM II wafers employ floating

gate EEPROM devices which are sensitive to electro-static charging and UV effects, causing a change in EEPROM threshold voltages [106]. Arrays of EEPROMS are fabricated across the surface of a special test wafer. After wafer processing, changes in threshold voltages can be electrically detected, providing spatial information of wafer charging effects.

Test wafers employing passive sensors are easy to use and can provide useful information about the peak wafer states achieved during processing. IC manufacturers can introduce these wafers into their processing tools with standard wafer handling robotics and without any equipment modifications, making them attractive for use in high volume manufacturing facilities. However, passive sensor wafers require additional post-processing time to obtain the wafer state information. In addition, many passive sensor wafers are single-use, requiring a new sensor wafer for each run. The principal shortcoming of passive sensor wafers is that, by their very nature, they can only record extremes over time and do not have the capability to monitor the time-resolved behavior of the variable of interest.

The demand for real-time spatially resolved wafer temperature information has led to the development of tethered TC-wafers These are standard silicon wafers with small thermocouples (TCs) embedded into their surface [92]. Real-time temperature information during wafer processing can then be obtained through a cable which connects the TCs on the wafer to a data acquisition system outside the processing tool.

Unfortunately, process tools do not readily accept these tethered TC wafers as the cable prohibits the TC wafer from being loaded with standard wafer handling robotics. As a result, the process tool has to be taken off-line and opened to provide loading access. In addition, a special feedthrough is required to thread the tether to the outside of the chamber. This results in significant tool-downtime and high cost-of-ownership. Hence, these wafers are mostly used for tool development or scheduled PM but not for routine process monitoring in production facilities.

2.4 Metrology: the future

Autonomous sensor wafers offer a promising alternative to in-line and/or in-situ metrology. These are sensors that externally resemble standard silicon wafers with embedded power, communications, and transduction elements. These autonomous sensor wafers can be introduced into equipment with existing wafer-handling robotics in cassette-to-cassette operations as regular product wafers. This eliminates the need to open the tool for sensor wafer loading and unloading. Sensor wafers can access wafer and process state information *during* processing as is available from equipment-based in-situ sensors. An added benefit is that sensor wafers can be significantly less complex and more cost-effective when compared with in-situ or in-line alternatives. In addition, autonomous sensor wafers can provide process engineers with temporal and spatial wafer state information, making it possible to fine tune the process rapidly while minimizing test wafers usage.

The feasibility of sensor wafers for semiconductor manufacturing applications has been shown in [41, 42, 40]. Several proof-of-concept designs to measure film-thickness, temperature and heat flux have been developed. These sensor wafers are capable of measuring the wafer state in real-time during selected IC processing steps. In order to obtain spatial wafer state information, several transduction elements are placed at the wafer surface. However, a large number of these elements have to be used to obtain satisfactory spatial resolution, particularly for 300 mm substrates.

An "ideal" sensor wafer must resemble a regular product wafer as closely as possible in order to avoid interference with the variable to be measured. Thus the thermal mass and topology of each transduction element should be minimized. In addition, the sensor wafer should strictly avoid exposing the process to any exotic materials which are incompatible with semiconductor manufacturing processes as this may result in unacceptable contamination of the tool. Hence, it is very desirable to fabricate sensor wafers with standard semiconductor processing techniques, if possible.

Processes in semiconductor manufacturing equipment often take place in harsh environments. For example, during plasma etching the wafer is exposed to high electro-magnetic fields and strong chemical etchants. In addition, many processes are performed at elevated temperatures, up to 1100 °C. Hence, an autonomous sensor wafer must be properly shielded to protect the on-board electronics and power supply. Temperature shielding is particularly challenging and may entail the design of a vacuum chamber around the electronics to eliminate thermal conduction and convection. However, this will severely complicate the overall design and it is therefore unlikely that any autonomous sensor wafer will be able to operate at temperatures above 150 °C. This limits their use to low temperature applications such as post-exposure bake plates and some plasma etchers.

We do not suggest that autonomous sensor wafers will replace all metrology currently in place. Compared to off-line and in-line metrology, the accuracy and precision of autonomous sensor wafers are limited. For example, state-of-the-art metrology tools that employ optical techniques to measure wafer properties such as film thicknesses, linewidths and sidewall profiles are irreplaceable, and they cannot be supplanted by autonomous sensor wafers. A further shortcoming is that on-board data storage will pose a limit on the maximum sampling rate and number of data points collected. Hence, the need for test wafers, while diminished, will remain.

Despite these challenges, we feel that IC manufacturers will adopt autonomous sensor wafers in the near future to obtain previously unaccessible wafer state information. Autonomous sensor wafers will be particularly vital during the ramp up phase of new production facilities or for rapid fault detection and isolation. In addition, they can also be used to quickly assess or validate the performance of individual processing tools, enhancing process uniformity and reducing the risks and associated costs of lost product.

We should remark that the IC industry is rather conservative in adopting new technologies to improve performance because of the concern that these may adversely

affect process stability. However, we remain optimistic that the successful use of autonomous sensor wafers in various applications such as etch and lithography will eventually drive their widespread acceptance in high volume manufacturing facilities.

Chapter 3

Electrical Impedance Tomography: an overview

Electrical Impedance Tomography is an *in vivo* imaging technique, principally used in medical applications. It has also found application in non-destructive product testing [52], fluid flow imaging [25, 109] and geophysics [26]. The technique consists of injecting electrical currents into an object and measuring the induced potentials at the surface of the object. These surface measurements are used to estimate the conductivity distribution in the interior of the object. The estimated conductivity distribution can then be directly related to different features within the object (organs in humans, processing faults in finished products) and can, therefore, be used as a diagnostic tool. The principal advantage of this technique is that it uses fairly inexpensive hardware and is non-destructive.

The remainder of this chapter offers a survey of Electrical Impedance Tomography (EIT). After a brief introduction, we derive the governing partial differential equations which model the electrical behavior of the object being imaged. This model forms the basis for any EIT algorithm. The following two sections treat computational aspects of simulating the EIT model, and inverting this model respectively. These computational problems form the core of all EIT algorithms. Finally, we offer a simple

numerical example to illustrate the ideal developed in this chapter.

3.1 Operating principle

Since the early 1900s, geophysicists have relied on electrical measurements at the earth's surface to obtain conductivity/impedance maps of the earth near the surface. These maps, in combination with the known electrical properties of rocks and minerals, can aid in prospecting for minerals and locating water and oil fields [86, 26]. In the biomedical context, the human body consists of a variety of tissues and organs with different characteristic conductivities/impedances. Consequently, electrical impedance techniques can be used for medical imaging, providing a tool to non-destructively detect and distinguish different tissues inside the human body. Since the early 1980s many different research groups have focused on developing and enhancing Electrical Impedance Tomography techniques for medical applications [7, 88, 16, 31, 101, 67, 15].

Electrical Impedance Tomography (EIT) techniques aim to infer the conductivity distribution inside an object based on simple electrical measurements performed at the boundary of the object. Therefore, a finite number of electrodes are mounted onto the surface of the object of interest. Early EIT systems applied known potentials between the different electrodes and recorded the resulting currents [54]. However, contact impedance between the electrodes and the object can seriously affect the measurements. Consequently, most EIT systems currently apply known currents between several electrodes and record the resulting potentials at all electrodes.

The observed potentials and prior information about the geometry of the object are then used in an algorithm to estimate the conductivity inside the object. The conductivity information can then be used to locate regions with a specified conductivity, for example the location of certain organs within the human body. The conductivity map can also help in assessing the conductivity of a specified region inside the body

such as lungs during the breathing cycle.

EIT is a noninvasive imaging technique, requiring relatively simple and inexpensive hardware. In addition, EIT does not damage any tissue and does not require the use of contrast chemicals. Hence, EIT is cost-effective compared to other medical imaging solutions such as X-ray imaging, gamma cameras and Magnetic Resonance Imaging [107, 95]. However, imaging using EIT is not without problems. The major drawback of EIT techniques is its limited resolution. Electrical measurements are performed at the periphery of the object, making it difficult to detect conductivity changes in the remote interior of the object. Consequently, EIT techniques do not supplant other imaging techniques.

3.2 The governing equations

Over the years, a variety of algorithms have been developed to solve the EIT problem. Despite their differences, each algorithm begins with the same partial differential equation describing the electrical behavior of the object of interest. In this section we will use Maxwell's equations to derive this governing partial differential equation.

3.2.1 The generic EIT experiment

Consider an object Ω as shown in Figure 3.1. A total number of L electrodes are mounted at the periphery $\partial\Omega$ of the object. Consider the experiment where a pattern of *constant* currents is applied to the electrodes. Let I_k be the current injected into the object through the k-th electrode. To ensure that charge does not accumulate in the object, we insist that $\sum_k I_k = 0$. The injected currents establish a potential distribution within the interior Ω and on the boundary $\partial\Omega$ of the object.

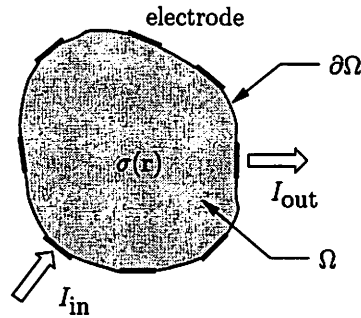

Figure 3.1: The generic EIT setup

3.2.2 Notation

In the remainder of this section we will derive the governing partial differential equation for the generic EIT experiment. To this end, we will introduce some notation

Ω	interior of the object	$\mathbf{E}(\mathbf{r})$	electrical field vector at $\mathbf{r}$
$\partial\Omega$	boundary of the object	$\mathbf{J}(\mathbf{r})$	current density vector at $\mathbf{r}$
$\mathbf{r}$	position vector of a point in Ω	$\mathbf{B}(\mathbf{r})$	magnetic field vector at $\mathbf{r}$
$\sigma(\mathbf{r})$	conductivity of the object at $\mathbf{r}$	$\hat{\mathbf{n}}(\mathbf{r})$	unit normal at points on $\partial\Omega$
$u(\mathbf{r})$	electrical potential at $\mathbf{r}$	e_l	portion of $\partial\Omega$ covered by l-th electrode

3.2.3 The continuum model

Consider an object with conductivity $\sigma(\mathbf{r})$ as function of the spatial position $\mathbf{r}$ in the object as depicted in Figure 3.1. Maxwell's equations then describe the relationship between an electric field $\mathbf{E}$ and a magnetic field $\mathbf{B}$ inside the interior Ω of object as follows:

$$\begin{aligned} \nabla \times \mathbf{E} &= -\frac{\partial \mathbf{B}}{\partial t} \\ \nabla \times \frac{\mathbf{B}}{\mu} &= \mathbf{J} + \frac{\partial}{\partial t}(\epsilon \mathbf{E}). \end{aligned}$$

Here ϵ is the electric permittivity, μ is the magnetic permeability and $\mathbf{J}$ is the current density which is related to the electric field $\mathbf{E}$ through Ohm's law

$$\mathbf{J} = \sigma \mathbf{E}. \tag{3.1}$$

Dimensional analysis of this equation shows that σ has units $1/(\Omega \mathrm{m})$ in the three-dimensional case and $1/\Omega$ in the two-dimensional case, i.e. in the latter case σ corresponds to the sheet conductivity (the reciprocal of the sheet resistance, see also Section 4.2) instead of the conductivity of the object of interest. For ease of notation, however, we will continue to refer to σ as the conductivity.

Almost universally, EIT applications use DC currents or AC currents of sufficiently low frequency that induced magnetic field effects are negligible. Our development will focus on the steady-state case of DC currents. Here, Maxwell's equations simplify to

$$\nabla \times \mathbf{E} = 0 \tag{3.2}$$

$$\nabla \times \frac{\mathbf{B}}{\mu} = \mathbf{J}. \tag{3.3}$$

It follows from Equation (3.2) that $\mathbf{E}$ is the gradient of an electric potential u inside Ω, i.e.

$$\mathbf{E} = -\nabla u. \tag{3.4}$$

Taking the divergence of Equation (3.3) leads to

$$\nabla \circ \mathbf{J} = 0.$$

Substituting Equations (3.1) and (3.4) into the above equation finally results in

$$\nabla \circ [\sigma(\mathbf{r}) \nabla u] = 0 \text{ for } \mathbf{r} \in \Omega. \tag{3.5}$$

This laplacian-like partial differential equation (PDE) describes the potential distribution in the interior Ω.

To solve this PDE we need appropriate boundary conditions. A variety of boundary conditions have been proposed, see for example [17, 16, 77, 94, 15]. The boundary

conditions suggested in the literature reflect different assumptions on how currents are injected into the object of interest. In the remainder we will assume that currents are injected through discrete electrodes at the periphery $\partial\Omega$ of the object. Consequently, the normal current density at points on the boundary is zero except at the electrodes. At the electrodes, we have current densities J_k:

$$\sigma\left(\nabla u \circ \hat{\mathbf{n}}\right)(\mathbf{r}) = \begin{cases} -J_k & \text{at } k\text{-th electrode} \\ 0 & \text{elsewhere} \end{cases} . \tag{3.6}$$

To avoid the accumulation of charge in the object during the experiment, we have to add the following constraint on this boundary condition:

$$\int_{\partial\Omega} \sigma\left(\nabla u \circ \hat{\mathbf{n}}\right)(\mathbf{r}) = 0.$$

The PDE in Equation (3.5) together with the boundary condition in Equation (3.6) yields a solution u that is unique upto an arbitrary additive constant. A unique solution can be obtained by assigning a ground potential to a point inside or on the boundary of the object. We will make this assignment so as to satisfy the constraint

$$\int_{\partial\Omega} u = 0.$$

3.2.4 Modeling assumptions

The continuum model [15] from the previous section assumes that a known current density is applied to the surface of the object. However, in reality, we rely on highly conductive, discrete electrodes to inject currents into the object. The continuum model does not take into account the discreteness of these electrodes and, as a result, does not always agree with experimental data [17]. The higher conductivity of discrete electrodes can cause a shunting effect at the boundary. In addition, there will also be a contact impedance between an electrode and the object. The so-called complete electrode takes all these electrode effects into account [17, 77, 94].

In the sequel we will assume that we known the current density at each electrode, allowing us to use the simpler continuum model.

3.3 The forward problem

For a given conductivity distribution $\sigma(\mathrm{r})$ inside the object and a known current density at the surface the continuum model, defined by Equations (3.5) and (3.6), can be used to predict the potential inside the object. The *forward problem* is concerned with solving these equations for u. For simple geometries and conductivity distributions, it is possible to find analytical solutions. However, for arbitrary conductivity distributions we must resort to numerical methods.

3.3.1 Analytical solution

In many EIT problems, and particularly in the context of our application, the object of interest is circular. For example, in industrial applications, objects of interest are pipes and vessels [25, 55] and in biomedical applications, EIT techniques are used to image the interior of approximately cylindrical body parts such as the human thorax and limbs [7, 88, 16, 31, 101, 67, 15]. Assume for the moment that the conductivity distribution σ in the interior of this circle of radius R is uniform, see Figure 3.2(a). The PDE in Equation (3.5) can then be written in cylindrical coordinates as:

$$u_{rr} + \frac{1}{r}u_r + \frac{1}{r^2}u_{\theta\theta} = 0$$

with boundary condition

$$\sigma \left.\frac{\partial u}{\partial r}\right|_{r=R} = f(\theta).$$

The solution to this problem can be found through separation of variables. The final solution which satisfies the Neumann boundary conditions is given by [28]:

$$\begin{aligned} u(r,\theta) &= \frac{1}{2}A_0 + \frac{r}{\sigma\pi}\int_{-\pi}^{\pi} f(\phi)\left\{\sum_{n=1}^{\infty}\frac{1}{n}\left(\frac{r}{R}\right)^n \cos(n(\theta-\phi))\right\} d\phi \\ &= \frac{1}{2}A_0 - \frac{r}{2\sigma\pi}\int_{-\pi}^{\pi} f(\phi)\log\left[R^2 - 2Rr\cos(\theta-\phi) + r^2\right] d\phi \end{aligned} \tag{3.7}$$

with A_0 an arbitrary additive constant, reflecting the non-uniqueness of the solution to this problem.

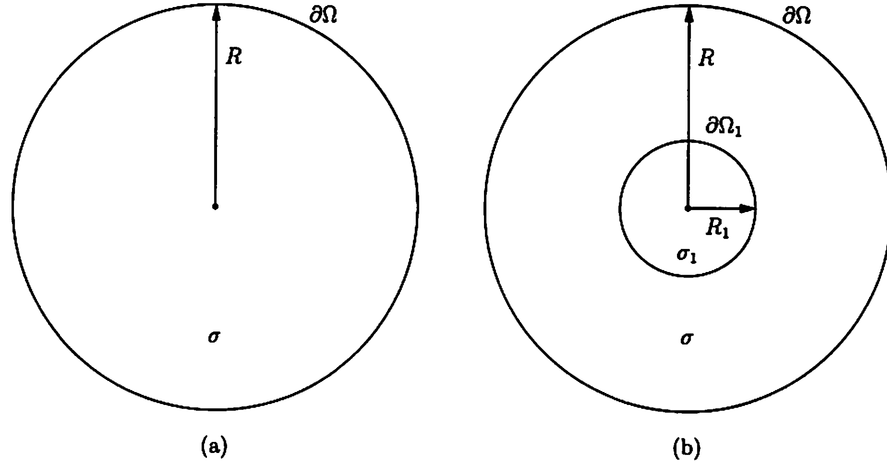

Figure 3.2: A disc of uniform conductivity (a) and a disc with a circular anomaly centered around the origin (b).

A similar approach can be used to find the solution to the Laplace equation with Neumann boundary conditions on a circle with a circular anomaly centered around the origin, see Figure 3.2(b). Here we have two concentric discs with conductivities σ and σ_1 as shown. The solution to this problem on the boundary is then given by [90, 89, 50]:

$$\begin{aligned} u(R,\theta) &= \frac{1}{2}A_0 + \frac{R}{\sigma\pi}\int_{-\pi}^{\pi} f(\phi)\left\{\sum_{n=1}^{\infty}\frac{1}{n}\frac{1+\nu\left(\frac{R_1}{R}\right)^{2n}}{1-\nu\left(\frac{R_1}{R}\right)^{2n}}\cos(n(\theta-\phi))\right\}d\phi, \quad (3.8)\\ \nu &= \frac{\sigma-\sigma_1}{\sigma+\sigma_1}. \end{aligned}$$

Now consider the case where the anomaly is not centered around the origin. The following conformal mapping (see Figure 3.3) can then be used to map the off-centered anomaly in the z-plane onto a centered circular anomaly in the w-plane [89, 56].

$$w = t\frac{z-s}{z-t} \quad (3.9)$$

with

$$\begin{aligned} t &= \frac{(R+d^2-r_1^2)+\sqrt{(R^2+d^2-r_1^2)^2-4d^2R^2}}{2d}\\ s &= \frac{R^2}{t} \end{aligned}$$

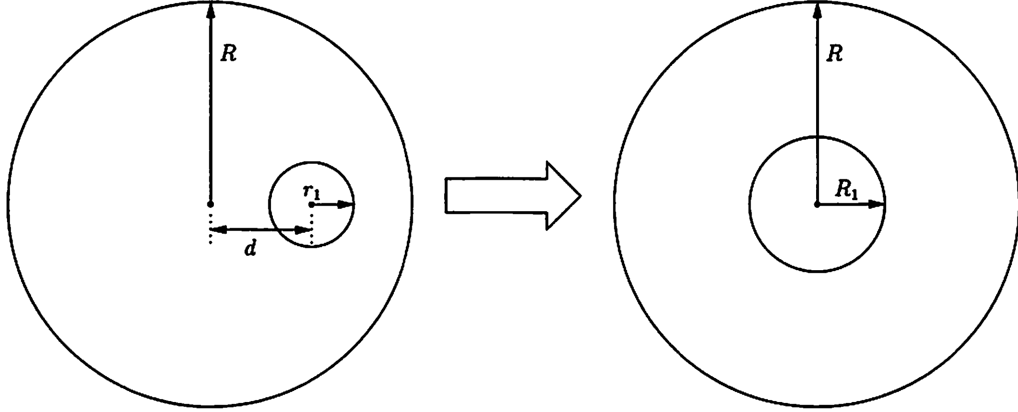

Figure 3.3: A conformal mapping can map an off-centered circular anomaly to a centered anomaly.

$$R_1 = r_1\left|\frac{t}{d-t}\right|.$$

Hence, after mapping, we can use Equation (3.8) to solve this problem with an off-centered anomaly.

We note that the conformal mapping in Equation (3.9) distorts the boundary. More specifically, the boundary point $z = Re^{j\theta}$ in the z-plane is mapped onto the following point in the w-plane:

$$\begin{aligned} w(\theta) &= Re^{jg(\theta)}, \\ g(\theta) &= \pi + 2\tan^{-1}\left(\frac{R\sin(\theta)}{R\cos(\theta)-s}\right) - \theta. \end{aligned}$$

Consequently, the boundary condition $\sigma \left.\frac{\partial u}{\partial r}\right|_{r=R} = f(\theta)$ in the z-plane must be suitably changed in the w-plane.

3.3.2 Finite element modeling

For certain conductivity distributions in the continuum model it is possible to solve for the surface potentials analytically. However, heterogeneous conductivity distributions inside the object, complex boundary conditions or irregular geometries will require numerical methods.

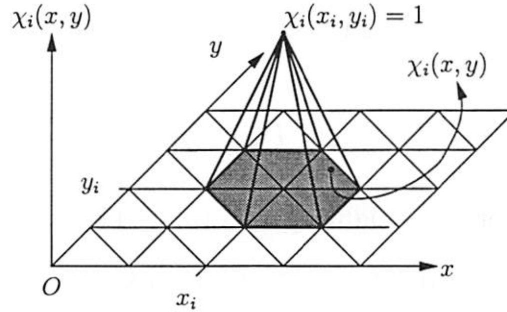

Figure 3.4: Characteristic function χ_i for an arbitrary triangular finite element discretization.

Numerical methods used to solve the forward problem in EIT include the Finite Element Method (FEM), the Finite Difference Method (FDM) and the Boundary Element Method (BEM). Of those, the Finite Element Method is generally preferred as it can deal with irregular geometries and arbitrary boundary conditions.

In the Finite Element Method [2, 14] the object is divided into small triangular elements with constant conductivity. Other geometries, such as quadrilaterals, can also be used. The vertices of the triangles are called nodes. The continuous potential distribution within the object is then assumed to be a linear combination of the potentials at each node, i.e.

$$u(x,y)=\sum_{i=1}^{N_n}\chi_i(x,y)u_i=\boldsymbol{\chi}^T\mathbf{u} \tag{3.10}$$

where N_n is the number of nodes used in the FEM approximation. The weights $\chi_i(x,y)$ (called characteristic functions) are pyramid-like continuous functions on each triangular element containing the i-th node. Inside these elements $\chi_i(x,y)$ decays from 1 at node i to 0 at all other nodes; outside these elements $\chi_i(x,y)=0$. The characteristic functions are illustrated in Figure 3.4. For more details, see Appendix A.

The interpolation function u in Equation (3.10) will in general not satisfy the PDE exactly, i.e.

$$R=\nabla\circ[\sigma\nabla u]\neq 0$$

where R is the residual. Hence, instead of solving $\nabla\circ[\sigma\nabla u]=0$ directly, an approx-

imate solution is computed such that the residual R will be evenly distributed over the object, i.e.

$$\int_{\Omega} wR = \int_{\Omega} w\nabla \circ [\sigma \nabla u] d\Omega = 0 \tag{3.11}$$

where w is an appropriate weighting function. This will result in an error which is zero in a spatially averaged sense. Using Green-Gauss' theorem, Equation (3.11) can be written as

$$\int_{\Omega} \nabla w \circ [\sigma \nabla u] d\Omega = \int_{\partial\Omega} w\sigma \left(\nabla u \circ \hat{\mathbf{n}}\right) ds.$$

Substituting Equation (3.10) and the boundary condition for the l-th electrode in Equation (3.6) into the previous expression yields

$$\left(\int_{\Omega} \nabla w \circ \left[\sigma \nabla \boldsymbol{\chi}^T\right] d\Omega\right) \mathbf{u} = \int_{e_l} w J_l ds.$$

In the Galerkin approach, w is chosen to be one of the characteristic functions $\chi_i, i = 1, \ldots, N_n$. The partial differential equation, including the boundary condition, can then be transformed into a system of N_n equations with N_n unknown node potentials. The equation for node i then becomes

$$\left(\int_{\Omega} \nabla \chi_i \circ \left[\sigma \nabla \boldsymbol{\chi}^T\right] d\Omega\right) \mathbf{u} = f_i \tag{3.12}$$

with

$$f_i = \begin{cases} \int_{e_l} \chi_i J_l ds & i\text{-th node on boundary under } l\text{-th electrode} \\ 0 & \text{elsewhere} \end{cases}.$$

This results in the following system of equations

$$Y\mathbf{u} = \mathbf{f}$$

with

$$Y(i,j) = \int_{\Omega} \nabla \chi_i \circ [\sigma \nabla \chi_j] d\Omega.$$

Note that the conductance matrix Y is singular. This is due to the fact that the underlying PDE does not have a unique solution. Assigning one node to ground, will yield a nonsingular conductance matrix.

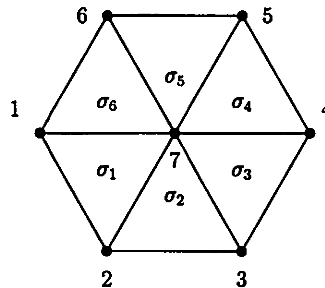

Figure 3.5: Simple hexagonal object containing 6 equilateral finite elements.

3.3.3 Finite element example

In Appendix A we describe at length how the Galerkin method can be applied to a single triangular element. The object of interest will contain many such triangular elements. In this section we provide a simple example to illustrate how the approximation of each of these triangular elements are combined to obtain the overall finite element model.

Consider an hexagonal object containing 7 vertices and 6 triangular finite elements, each with a constant conductivity $\sigma_i, i = 1, \ldots, 6$, see Figure 3.5. The side of each equilateral triangle has unit length. We will assume that currents enter/leave the object only through the vertices on the boundary, reflecting point current sources. For each triangular element, we can then use Equation (A.1) to express the relation between the node currents and the node potentials. For example, applying Equation (A.1) to element 1 yields

$$\frac{\sigma_1}{\sqrt{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ -1/2 & 1 & -1/2 \\ -1/2 & -1/2 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_7 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_7 \end{bmatrix}.$$

Similar equations can be written for the other elements. Combining all these equations

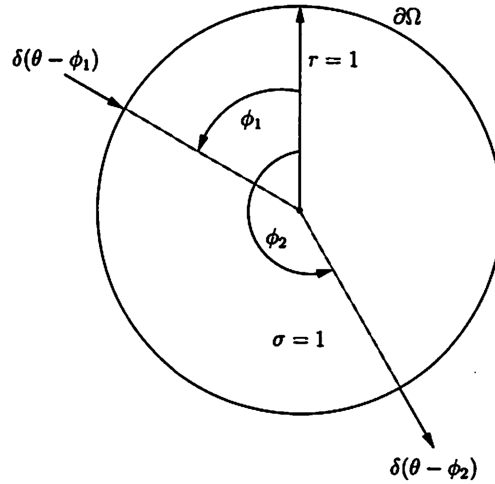

Figure 3.6: A disc of uniform conductivity with two point current sources on the boundary.

finally results in:

$$\frac{1}{\sqrt{3}}\begin{bmatrix} \sigma_1+\sigma_6 & -\sigma_1/2 & 0 & 0 & 0 & -\sigma_6/2 & -(\sigma_1+\sigma_6)/2 \\ * & \sigma_1+\sigma_2 & -\sigma_2/2 & 0 & 0 & 0 & -(\sigma_1+\sigma_2)/2 \\ * & * & \sigma_2+\sigma_3 & -\sigma_3/2 & 0 & 0 & -(\sigma_2+\sigma_3)/2 \\ * & * & * & \sigma_3+\sigma_4 & -\sigma_4/2 & 0 & -(\sigma_3+\sigma_4)/2 \\ * & * & * & * & \sigma_4+\sigma_5 & -\sigma_5/2 & -(\sigma_4+\sigma_5)/2 \\ * & * & * & * & * & \sigma_5+\sigma_6 & -(\sigma_5+\sigma_6)/2 \\ * & * & * & * & * & * & \sum_{i=1}^{N}\sigma_i \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \\ V_7 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \\ I_7 \end{bmatrix}.$$

3.3.4 Simulation example

Consider a disk of radius $r = 1$ with a uniform conductivity $\sigma = 1$, see Figure 3.6. The disk is subjected to two point current sources on the boundary, i.e.

$$\sigma \left.\frac{\partial u}{\partial r}\right|_{r=1} = f(\theta) = \delta(\theta-\phi_1) - \delta(\theta-\phi_2)$$

where δ is a Dirac pulse and ϕ_1 and ϕ_2 are the angles of the current sources through which currents respectively flow in and out of the object. The analytical solution (see

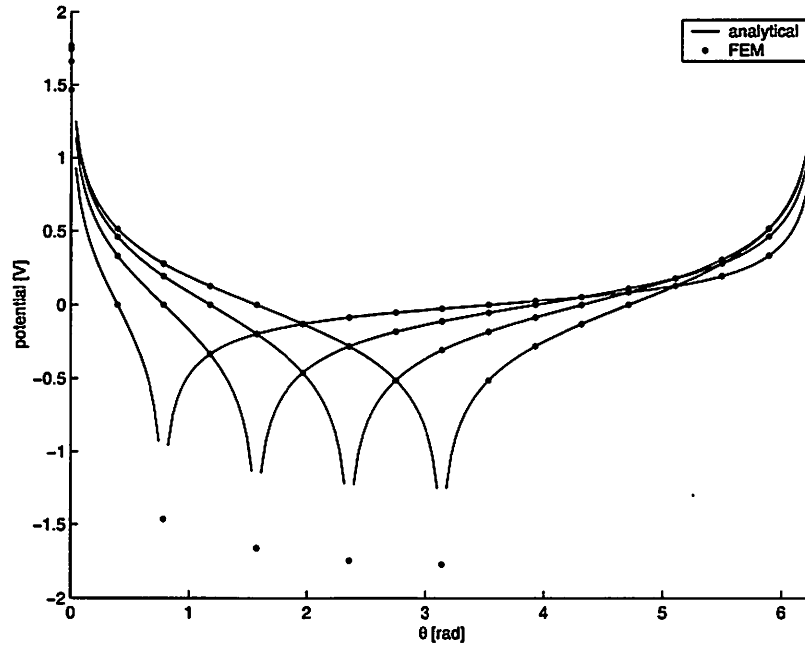

Figure 3.7: Analytical and numerical solution to the Laplace equation on a circle for different Neumann boundary conditions.

Equation (3.7)) is given by

$$u(1,\theta) = -\frac{1}{2\pi}\log\left(\frac{1-\cos(\theta-\phi_1)}{1-\cos(\theta-\phi_2)}\right).$$

This analytical solution is plotted in Figure 3.7 for different point current source locations ϕ_1 and ϕ_2. The underlying PDE in Equation (3.5) was also solved using the Finite Element Method. Here, the unit circle was divided into 3264 triangular elements. The FEM-solution, also shown in Figure 3.7, agrees very closely with the analytical solution. We conclude that this FEM discretization is sufficiently refined to accurately approximate the real solution.

3.4 The inverse problem

Consider the following experiment. Known currents are applied to electrodes on the surface of an object and the corresponding potentials on the electrodes are mea-

sured. The central question in EIT is then whether it will be possible to reconstruct $\sigma(\mathbf{r})$ based on these simple electrical measurements. This problem is called the *inverse problem* and is in general nonlinear and poorly conditioned. It is poorly conditioned because large changes in conductivity in the center of the object weakly influence the measured potential at the boundary. In addition, measurement noise can seriously influence the final estimate.

3.4.1 Degrees of freedom

Consider again the object as shown in Figure 3.1 with L electrodes mounted at the periphery. In the ideal case, these L electrodes allow at most $L-1$ independent current patterns to be applied to the object. Now assume that for each independent current pattern the resulting potentials at all electrodes are recorded. Consequently, we will obtain $L(L-1)$ potential measurements for the complete EIT experiment. However, not all of these measurements are independent. For example, forcing a known fixed current between nodes A and B will result in a potential difference V_{CD} between nodes C and D. Now assume that the same current is applied between nodes C and D. The reciprocity theorem tells us that the resulting potential V_{AB} between nodes A and B will equal V_{CD}, i.e. the the second measurement does not reveal any new information. Consequently, any EIT experiment performed with L electrodes will yield at most $L(L-1)/2$ independent measurements.

In certain EIT applications one of the electrodes at the periphery is used as reference electrode. In addition, potentials at current carrying electrodes are not recorded to eliminate the need to model contact resistance effects between current carrying electrodes and the object. In this case, the total number of independent measurements is further reduced to $L(L-3)/2$.

3.4.2 Parameterizing the conductivity profile

The conductivity distribution inside an object can be arbitrarily complex. Consequently, any EIT experiment which aims to infer the exact conductivity distribution inside the object of interest, requires an infinite number of independent electrical measurements. This is, of course, not feasible. In practice, obtaining a good approximation of the conductivity distribution suffices. Therefore, the conductivity distribution is parameterized, using only a modest number of unknown parameters. For example, some EIT algorithms assume that the object can be split up into N smaller elements, each with a constant (unknown) conductivity $\sigma_i, i = 1, 2, \cdots, N$.

In this approach, any correlation between the conductivity of neighboring elements is ignored. Consequently, large and abrupt changes in conductivity across the object can be estimated. This parameterization is very well suited to detect areas with significantly different conductivities inside the object of interest such as, for example, the lungs in the human thorax. However, in the context of our applications, the conductivity changes gradually across the object, i.e. the conductivity is a smooth function of the position inside the object. Taking this spatial smoothness into account can significantly reduce the number of unknown parameters, improving the stability of the EIT algorithm while reducing the computational effort. Hence, *a priori* knowledge of the conductivity inside the object is vital in selecting the appropriate parameterization. For example, in [102, 101] *a priori* anatomical information was used to create a set of basis functions. The conductivity distribution within the human thorax was then approximated as a linear combination of these preselected basis functions.

3.4.3 Kriging

In this subsection we offer a novel approach to parameterize the conductivity profile for EIT applications. Our approach is based on the statistical interpolation

technique of Kriging (see Appendix B) and does not suffer from the unnatural discontinuities common to other parameterizations.

An alternative approach to obtain continuous estimated conductivity profiles is to enforce the smoothness constraint in the inverse EIT solver itself. This can be done by introducing a non-smoothness penalty in the optimization criterion Equation (3.15) with an appropriate Lagrange multiplier λ. A proper choice for λ will then penalize large values of $\nabla\sigma$. Through trial and error we can then decide on the optimal value of the Lagrange multiplier. However, in this approach spatial correlation between conductivity values at neighboring points is indirectly taken into account. In addition, the number of unknown parameters is often still related to the number of triangles used in the forward FEM solver. To speed up the inverse solver, we would like to reduce the number of unknown parameters in the inverse problem. Hence, we have to *a priori* select a suitable low-dimensional basis which can accurately capture reasonably smooth conductivity variations.

Consider the following smooth conductivity distribution on a unit disk:

$$\sigma(x, y) = 1 + 0.1x - 0.2y - 0.1x^2 + 0.05y^2 - 0.05x^3 + 0.2y^3 + 0.05xy^2. \tag{3.13}$$

We will assume that we have exact knowledge of this function at 36 measurement sites as shown in Figure 6.6. The Kriging method then allows us to approximate the conductivity distribution at unobserved locations based on the known conductivity at those 36 fixed locations. To this end, we will use the Kriging Kernel

$$f(d) = \exp\left(-\frac{d}{D}\right) \tag{3.14}$$

with $D = 5$. The original conductivity distribution is shown in the top left panel of Figure 3.8. The top right panel in Figure 3.8 shows the error between the true conductivity distribution and the conductivity estimated with the Kriging algorithm. In this figure we have also included graphs of the estimated and the true conductivity along various cross sections of the unit disk. From Figure 3.8 it is evident that the

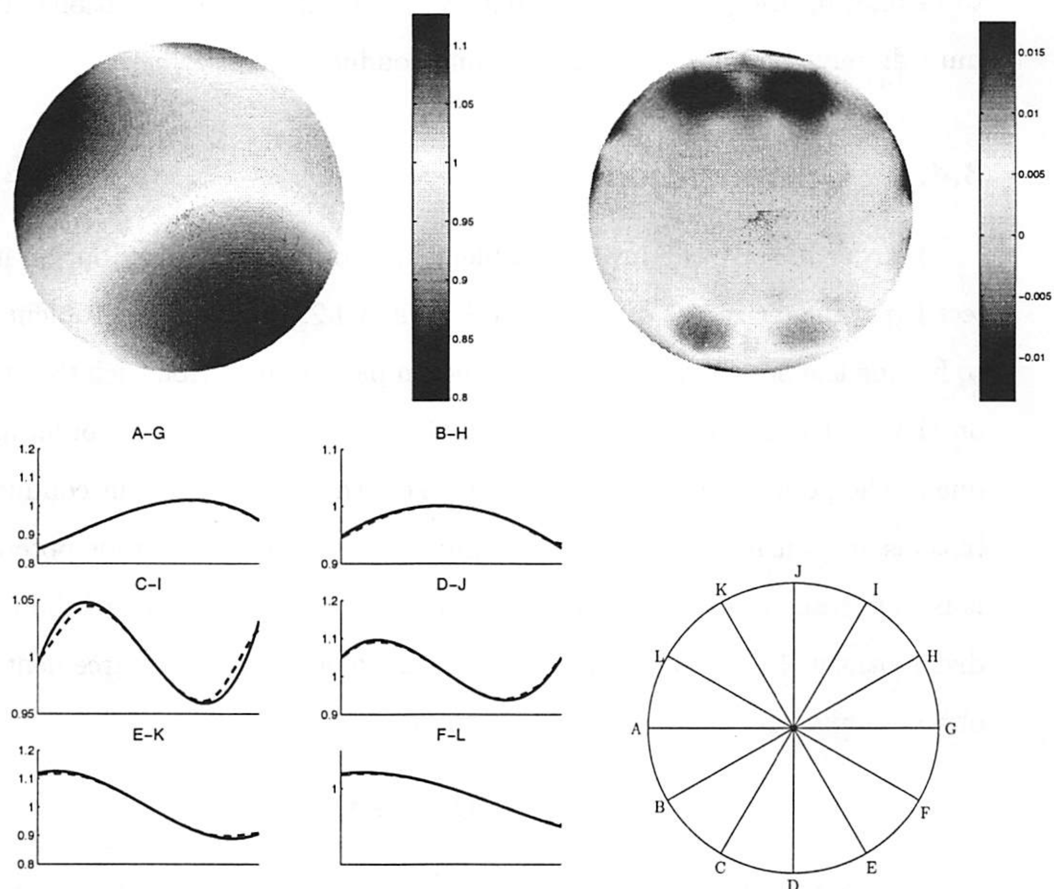

Figure 3.8: Top: the left panel shows the real conductivity in Equation (3.13) across the unit disk; the right panel shows the spatial error between the true conductivity and the conductivity estimated with the Kriging algorithm. Bottom: the left panel shows the true (solid) and estimate (dashed) conductivity along various cross sections of the unit disk (see right panel).

Kriging method approximates the true conductivity distribution accurately. (Note that the smoothness of the estimate can be easily varied by adjusting D in Equation (3.14).)

We believe that the Kriging method can provide a proper basis for use during EIT applications, with the conductivity at a few fixed locations as the unknown parameters in the inverse EIT algorithm. The inverse EIT algorithm then reduces

to estimating the proper conductivity values at these fixed locations, allowing us to immediately compute the corresponding conductivity elsewhere.

3.4.4 Optimization

In order to solve the inverse problem, the conductivity distribution inside the object is parameterized as discussed in Section 3.4.2. The inverse problem then reduces to finding the best parameters in the chosen parameterization such that the potentials on the electrodes in the model match the measured electrode potentials. However, due to the poor sensitivity of EIT, it is likely that many different conductivity distributions are consistent with the finite number of observed electrode potentials. Hence, it is important to choose an appropriate criterion to select one of the many possible distributions [11]. A rather naive criterion would seek exact agreement between the observed and predicted electrode potentials, i.e.

$$\mathbf{U}(\boldsymbol{\sigma}) = \mathbf{V}$$

with $\mathbf{U}(\boldsymbol{\sigma}), \mathbf{V} \in \mathbb{R}^n$ vectors of predicted and observed potentials, $\boldsymbol{\sigma} \in \mathbb{R}^N$ the vector of unknown conductivity parameters and n the total number of potential measurements for a variety of current patterns. However, this criterion does not guarantee a feasible solution. For example, the optimal conductivity may be negative in certain areas. In addition, noise in the observed dataset may introduce undesirable artifacts in the estimated conductivity distribution. Hence, a more appropriate criterion would be to minimize the error according to a statistical criterion

$$\min_{\boldsymbol{\sigma}} E(\boldsymbol{\sigma}) = \min_{\boldsymbol{\sigma}} \|\mathbf{U}(\boldsymbol{\sigma}) - \mathbf{V}\|^2. \tag{3.15}$$

This approach is adopted in most EIT algorithms [111, 16, 48, 30]. In [11, 68] a weighted least squares criterion is used, i.e. $\|W(\mathbf{U}(\boldsymbol{\sigma}) - \mathbf{V})\|^2$ is minimized.

The potential at the boundary of the object of interest is a nonlinear function of the conductivity distribution inside the object. Consequently, nonlinear programming

techniques are required to minimize the cost function in Equation (3.15) (see for example [60, 43, 24]). However, due to the nature of nonlinear programming, it is not possible to guarantee global convergence, i.e. the algorithm can converge to false local minima. Hence, an appropriate initial estimate for the conductivity distribution is critical to obtain meaningful results.

Let $\mathbf{U}(\boldsymbol{\sigma})$ denote the forward model, including appropriate boundary conditions. This model maps the parameterized conductivity distribution, $\boldsymbol{\sigma}$, into the vector of predicted electrode potentials $\mathbf{U}(\boldsymbol{\sigma})$. Differentiating the cost functional $E(\boldsymbol{\sigma})$ in Equation (3.15) yields

$$g(\boldsymbol{\sigma}) = \nabla E(\boldsymbol{\sigma}) = \mathbf{J}^T\left(\mathbf{U}(\boldsymbol{\sigma}) - \mathbf{V}\right) \tag{3.16}$$

where $\mathbf{J} = \nabla \mathbf{U}(\boldsymbol{\sigma})$ is the Jacobian matrix with

$$J_{ij} = \frac{\partial U_i(\boldsymbol{\sigma})}{\partial \sigma_j}, \quad i = 1, \ldots, n \text{ and } j = 1, \ldots, N.$$

The optimal conductivity distribution, $\boldsymbol{\sigma}_{opt}$, which minimizes the cost function in Equation (3.15), can be determined by solving the following equation

$$g(\boldsymbol{\sigma}_{opt}) = 0.$$

However, this optimal conductivity distribution cannot be found analytically as the function $g(\boldsymbol{\sigma})$ in Equation (3.16) is nonlinear. We therefore have to resort to nonlinear programming techniques to estimate $\boldsymbol{\sigma}_{opt}$.

Now assume that we have an initial estimate $\boldsymbol{\sigma}^{(n)}$ which is close to $\boldsymbol{\sigma}_{opt}$. In order to find an improved estimate $\boldsymbol{\sigma}^{(n+1)}$ of $\boldsymbol{\sigma}_{opt}$ we expand $g(\boldsymbol{\sigma})$ in Equation (3.16) as a Taylor series around $\boldsymbol{\sigma}^{(n)}$, i.e.

$$g(\boldsymbol{\sigma}^{(n+1)}) = g(\boldsymbol{\sigma}^{(n)}) + g'(\boldsymbol{\sigma}^{(n)})\Delta\boldsymbol{\sigma} + \text{higher order terms} \tag{3.17}$$

where $\Delta\boldsymbol{\sigma} = \boldsymbol{\sigma}^{(n+1)} - \boldsymbol{\sigma}^{(n)}$ and $g'(\boldsymbol{\sigma}^{(n)}) \approx \mathbf{J}^T\mathbf{J}$. Setting Equation (3.17) equal to zero and solving for $\Delta\boldsymbol{\sigma}$ finally results in the following iterative procedure [111]:

$$\Delta\boldsymbol{\sigma} \;=\; -\left(\mathbf{J}^T\mathbf{J}\right)^{-1}\mathbf{J}^T\mathbf{V}_{\text{diff}} \tag{3.18}$$

$$\mathbf{V}_{\text{diff}} = \mathbf{U}(\boldsymbol{\sigma}^{(n)}) - \mathbf{V}, \tag{3.19}$$

$$\boldsymbol{\sigma}^{(n+1)} = \boldsymbol{\sigma}^{(n)} + \Delta\boldsymbol{\sigma}. \tag{3.20}$$

In this iterative procedure the electrode potentials have to be computed for each updated conductivity distribution. Hence, an efficient implementation of the forward problem is essential.

The inverse of $\mathbf{J}^T\mathbf{J}$ is in general poorly conditioned, i.e. modest measurement noise can cause instability in the iterative scheme defined by Equations (3.18) - (3.20). Hence, regularization of the matrix is necessary. A popular regularization method is the Tikhunov method. This method trades off *a priori* knowledge about the solution against information about the solution from measurements by adding an extra term to the least squares cost function [23],[20], i.e.

$$E(\boldsymbol{\sigma}) = \min_{\boldsymbol{\sigma}} \|\mathbf{f}(\boldsymbol{\sigma}) - \mathbf{V}\| + P(\boldsymbol{\sigma}).$$

The simplest function choice here is

$$P(\boldsymbol{\sigma}) = \lambda\, \boldsymbol{\sigma}^T\boldsymbol{\sigma}.$$

This results in the following update for $\Delta\sigma$:

$$\Delta\boldsymbol{\sigma} = -\left(\mathbf{J}^T\mathbf{J} + \lambda\mathbf{I}\right)^{-1}\mathbf{J}^T\mathbf{V}_{\text{diff}}.$$

The parameter λ allows a tradeoff between fitting the observed data and boundedness of the solution $\boldsymbol{\sigma}$. Other penalty functions $P(\lambda)$, which can be used to regularize the solution, are discussed in [23].

Figure 3.9 show a schematic of the general process flow adopted in EIT to estimate the conductivity profile inside the object of interest.

3.5 EIT example

In this section we will discuss a simple EIT example. Consider a unit disc with 16 equidistant point electrodes at the periphery. Currents are injected between adjacent

1	perform experiment: apply known current patterns, collect corresponding potentials
2	start with initial estimate for conductivity distribution
3	use model to predict surface potential for given conductivity distribution
4	compute error between predicted and observed surface potentials
5	if error exceeds threshold use error to update estimate for conductivity distribution go back to 3 else accept conductivity profile
6	end

Figure 3.9: Generic process flow in EIT to estimate the conductivity profile inside the object of interest.

electrodes and the resulting potentials between the remaining adjacent electrodes are recorded. We started with the "true" conductivity distribution shown in Figure 3.10. This profile consists of two "hot spots" superimposed onto a uniform conductivity $\sigma = 0.15\ \Omega^{-1}$. Hot spots are commonly seen in semiconductor manufacturing and occur due to chucking problems or backside wafer contamination that interferes with wafer cooling. These hot spots can generate changes in the local conductivity of the wafer which we model as a spatial Gaussian kernel:

$$\Delta\sigma = K \exp\left(-\frac{(x - x_c)^2 + (y - y_c)^2}{\sigma_v^2}\right)$$

where K is the magnitude of the change, (x_c, y_c) defines the center of the hot spot and σ_v is the variance of the hot spot. The specific parameters used in this example can be found in Table 3.1.

The unit disc was divided into 3264 triangular elements. We then used a rudi-

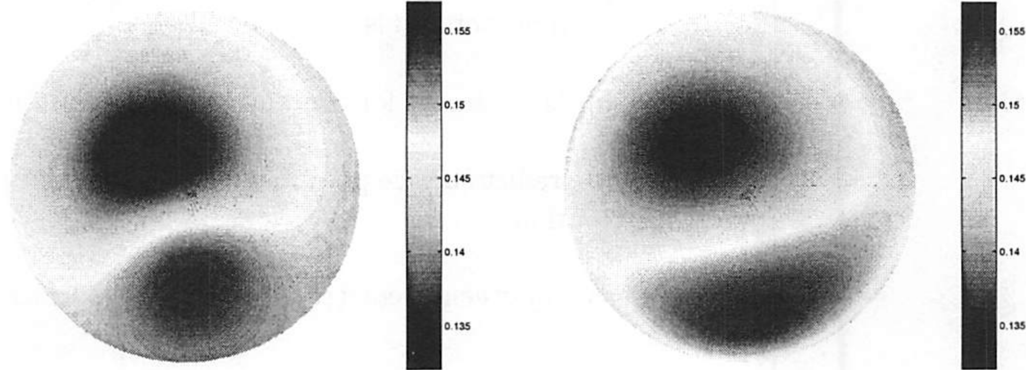

Figure 3.10: The true conductivity distribution (left) and the estimated conductivity distribution (right).

mentary FEM-based solver in MATLAB to solve the forward problem as defined in Equations (3.5) and (3.6). The resulting noise-free potential data at the electrodes was used in the inverse problem to estimate the original conductivity profile. In our inverse EIT solver, we model the conductivity distribution using multinomial basis functions as

$$\sigma(x,y) = \sum_{i=0}^{4}\sum_{j=0}^{i} \alpha_{ij} x^{i-j} y^{j}. \tag{3.21}$$

Note that this choice of parameterization decouples the degrees of freedom (DOF) in the EIT experiment, in this case 15 DOF, from the number of finite elements used in the discretization. Consequently, we can use a large number of finite elements both in the forward and inverse problem without causing numerical problems in the inverse estimation problem.

parameter	hot spot 1	hot spot 2
K	-0.02	0.015
(x_c, y_c)	(-0.14,0.09)	(0,-0.4)
σ_v	0.6	0.4

Table 3.1: Hot spot parameters used in the EIT example.

A least squares (LS) fit of our chosen multinomial bases to the true conductivity distribution provides the optimal values for the parameters α_{ij} in Equation (3.21). These optimal parameter values, in the least squares sense, provide a reference to assess the performance of our inverse estimation algorithm and are shown in the second column of Table 3.2.

The right panel in Figure 3.10 shows the estimated conductivity profile. This profile is the best fit to the true profile using the chosen bases in our inverse estimation problem. The corresponding parameters α_{ij} can be found in the third column of Table 3.2. From this table it is clear that the estimated values for α_{ij} are very close to the optimal LS values of α_{ij}. Any discrepancy can be attributed to the fact that the inverse EIT algorithm minimizes the error between the predicted and the observed potentials at each electrode. The optimal conductivity distribution in the least squares sense may not necessarily result in the smallest error between the predicted and the observed electrode potentials.

To illustrate the quality of the fit, we have plotted in Figure 3.11 the estimated and the true conductivity as well as the least squares projection along various cross sections of the unit disc. These cross sections show a fairly good match between the estimated conductivity profile and the true conductivity profile. Any discrepancies are due to the chosen bases which was not adequate to capture the rather rapid changes in conductivity near the center of the hot spots. This exemplifies the need to choose an appropriate bases which can capture the expected conductivity profile.

In order to assess the repeatability and variance in the estimated parameters, we tested the inverse EIT problem on artificial data corrupted with a small amount of random white noise. The variance of the additive noise was 0.5% and 1% of the maximum potential data in the forward problem. For each noise level, 50 EIT inverse problems were solved and the resulting values for the parameters α_{ij} recorded. In Table 3.2 the mean and the standard deviation for each of these parameters are shown. As expected, larger noise levels result in larger variances of the estimated

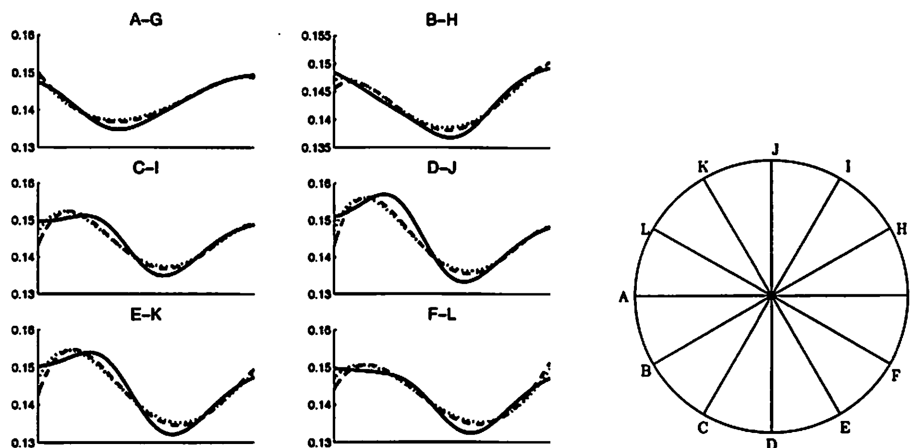

Figure 3.11: The left panel shows the true (solid) and the estimated (dashed) conductivity distribution, as well as the least squares projection (dotted) along various cross sections of the unit disc (see right panel).

parameters α_{ij}. In addition, Table 3.2 shows that the variances of some parameters exceed their mean values, i.e. there is no evidence in the data which can support the use of the corresponding basis functions to describe the true conductivity profile. Consequently, we can remove these particular basis functions without significantly deteriorating the estimated conductivity profile.

	LS	no noise	0.5% noise	1% noise
α_{00}	1.39e-01	1.38e-01	1.38e-01±1.50e-03	1.39e-01±3.44e-03
α_{10}	8.69e-03	9.43e-03	8.92e-03±2.06e-03	9.16e-03±3.81e-03
α_{01}	-1.89e-02	-2.11e-02	-2.09e-02±1.68e-03	-2.10e-02±3.65e-03
α_{20}	1.21e-02	1.45e-02	1.50e-02±8.95e-03	7.51e-03±1.92e-02
α_{11}	3.73e-03	3.79e-03	4.55e-03±7.17e-03	-1.31e-03±1.35e-02
α_{02}	3.41e-02	3.80e-02	3.85e-02±9.96e-03	3.34e-02±2.21e-02
α_{30}	-8.55e-03	-1.01e-02	-9.31e-03±3.03e-03	-9.65e-03±5.76e-03
α_{21}	2.25e-02	2.81e-02	2.76e-02±2.60e-03	2.72e-02±6.15e-03
α_{12}	-8.50e-03	-1.00e-02	-9.29e-03±3.41e-03	-9.40e-03±5.86e-03
α_{03}	1.95e-02	2.36e-02	2.34e-02±2.61e-03	2.37e-02±5.46e-03
α_{40}	-1.36e-03	-3.30e-03	-3.84e-03±1.00e-02	4.86e-03±2.12e-02
α_{31}	-3.48e-03	-3.61e-03	-4.55e-03±1.03e-02	4.51e-03±1.96e-02
α_{13}	-3.53e-03	-3.78e-03	-4.93e-03±1.09e-02	2.74e-03±2.05e-02
α_{22}	-2.89e-02	-3.70e-02	-3.79e-02±1.89e-02	-2.70e-02±3.99e-02
α_{04}	-2.48e-02	-3.03e-02	-3.11e-02±1.14e-02	-2.60e-02±2.48e-02

Table 3.2: Estimated parameter values α_{ij} for the various experiments discussed in the text.

Chapter 4

EIT based Sensors for Semiconductor Manufacturing

We submit that Electrical Impedance Tomography can be a compelling technique for use in semiconductor manufacturing applications. It provides a means to obtain spatially and time-resolved wafer state information during wafer processing.

In this chapter we introduce a novel *class* of sensors based on EIT. In particular, we focus on EIT based autonomous sensor wafers. First, we present a brief explanation of how EIT techniques can be used to obtain spatially resolved wafer state information. This section is followed by a discussion of the four-point probe measurement, a measurement technique used in semiconductor manufacturing to obtain the resistivity of thin films. This technique can be regarded as a special case of the more general EIT technique. Next, we introduce a three-stage approach for the design and operation of our EIT based sensors. We conclude with a discussion of various design and implementation issues that must be addressed to practically realize these sensors.

4.1 The basic idea

The need to measure real-time spatial wafer state information during IC processing has led to the development of so-called autonomous sensor wafers (see Section 2.4). Here, small sensors are mounted on the surface of a standard silicon wafer. During wafer processing, these sensors record valuable wafer state information which can be used for process evaluation/optimization and equipment design. Spatial wafer state information is obtained by distributing sensors across the wafer surface. A large number of sensors has to be used to obtain reasonable resolution, especially for 300 mm wafers. However, each sensor has to be addressed and powered independently, making the design, fabrication, and operation of these wafers increasingly complex.

This chapter will introduce a new *class* of sensors, for measuring wafer state information based on Electrical Impedance Tomography. These sensors are fundamentally different from the discrete sensors currently used: instead of using an array of point sensors to obtain spatial information, a single sensor, which exploits the inherent spatial imaging capability of EIT, is used.

During semiconductor manufacturing, chemical and physical effects at the wafer surface can induce conductivity changes in the interior of a wafer. By placing electrodes at the periphery of a wafer, simple EIT experiments can be performed during semiconductor manufacturing. These measurements can then be used to infer the conductivity changes in the interior. In turn, these changes in conductivity can be related to chemical and/or physical effects using appropriate models. Hence, it is possible to design a *class* of simple sensors for semiconductor manufacturing based on EIT techniques. The small size of the electrodes, the placement of the electrodes at the periphery of the wafer, and the large number of independent degrees of freedom (32 electrodes offer 496 degrees of freedom to fit the conductivity profile to the observed data) make this class of sensors attractive for use during semiconductor manufacturing.

An EIT based sensor has the following key characteristics. First, the sensor provides spatially resolved *wafer state* information. Second, the sensor requires modest interconnections that can be conveniently located near the periphery of the wafer, allowing for simple and *inexpensive* fabrication. Third, the absolute resolution of the sensor is ultimately determined by the number of electrodes and the measurement accuracy during EIT experiments.

The geometry of an EIT based sensor (thickness of conductive layer $\ll$ diameter) justifies the use of two dimensional EIT techniques, simplifying the EIT analysis significantly.

4.2 An example

During the semiconductor manufacturing process, it is important to maintain individual processing steps consistently within tight specifications to ensure optimal operation of the final devices. In particular, parameters which affect the electrical behavior (film thickness, critical dimensions, resistivity and doping concentration) need to be closely monitored and regulated. Therefore, special test structures are processed onto the wafer in parallel with the regular features. Some of these structures may be placed in the scribe lanes that separate dies. Simple electrical measurements, performed on these test structures, can reveal whether or not the process complies with the desired engineering specifications [22].

In order to extract process parameters from these electrical test structures, accurate knowledge of the sheet resistance of the film in question is required. The four-point probe is a simple and commonly used metrology tool in semiconductor manufacturing which can provide this information [99]. It consist of four equally spaced probes, see Figure 4.1. Current is forced through the two outer probes and the resulting potential difference between the two inner probes is recorded. The four-point probe can be regarded as a simple example of the more general EIT based

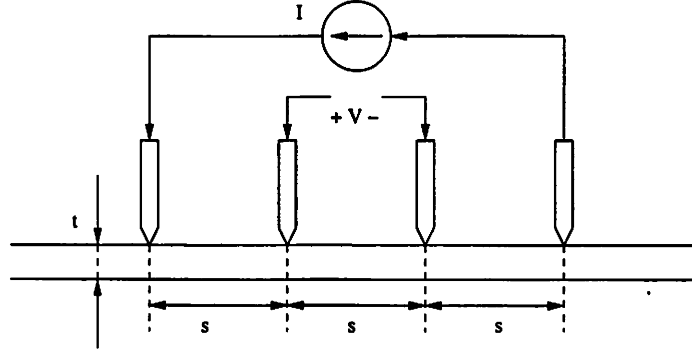

Figure 4.1: Schematic of four-point probe setup.

sensor. The thickness t of the film of interest is usually small compared to the spacing s of the probes. For an infinite slab, the sheet resistance R_s is then given by [80]:

$$R_s = \frac{\pi}{\ln 2} \frac{V}{I}.$$

If the thickness t of the material is known (for example using interferometry or ellipsometry), the resistivity ρ of the material can be easily inferred as

$$\rho = R_s t.$$

Here, it is assumed that the resistivity is constant across the film.

Resistivity maps of the wafer can be obtained by sampling the wafer at many sites and interpolating the results. However, these measurements are time-consuming and they may contaminate the wafer surface.

In order to address the drawbacks of the four-point probe measurements a new EIT based measurement strategy was proposed in [27]. This work is, to the best of our knowledge, the first application of EIT techniques to semiconductor manufacturing. Here, special probe-cards with 16 and 32 equally spaced probes were fabricated. The probes are placed within a narrow exclusion zone near the periphery of the wafer. Currents are injected between different electrode pairs and the resulting potentials at all electrodes are recorded.

Experimental results with this setup show that this EIT based method is applicable to a wide range of sheet resistance values with resolution, accuracy and repeatability comparable to four point probe measurements [27]. This method offers some additional advantages. First, the method is faster as the wafer/probes do not have to be moved to sample the whole wafer. Second, contamination of the center is reduced as probes are placed only near the edge of the wafer. Finally, the method is also less sensitive than the four-point probe to variations in contact resistances between probe and wafer. However, the major drawback of this method is that it cannot be used on product wafers.

In Chapters 6 and 7 of this dissertation we will describe our work in developing novel EIT based sensors to measure etch rate and plasma potentials at the wafer surface.

4.3 Three-stage approach

The general design and operation of the EIT based class of sensors consists of three stages as shown in the block diagram in Figure 4.2.

- **Stage A: Wafer Design**

  The first stage involves the design of a special wafer that is sensitive to the wafer state of interest, $X(r,\theta)$. Recall that EIT allows us to infer the conductivity profile $\sigma(r,\theta)$ in the interior of the wafer. We, therefore, need to design a special wafer which exploits simple physical and chemical effects so that

$$\sigma(r,\theta) = f(X(r,\theta)) \tag{4.1}$$

  where f is invertible. In this case, changes in $X(r,\theta)$ manifest as changes in $\sigma(r,\theta)$ which can be inferred using standard EIT techniques.

- **Stage B: EIT**

  This stage deals with the estimation of the conductivity distribution inside the

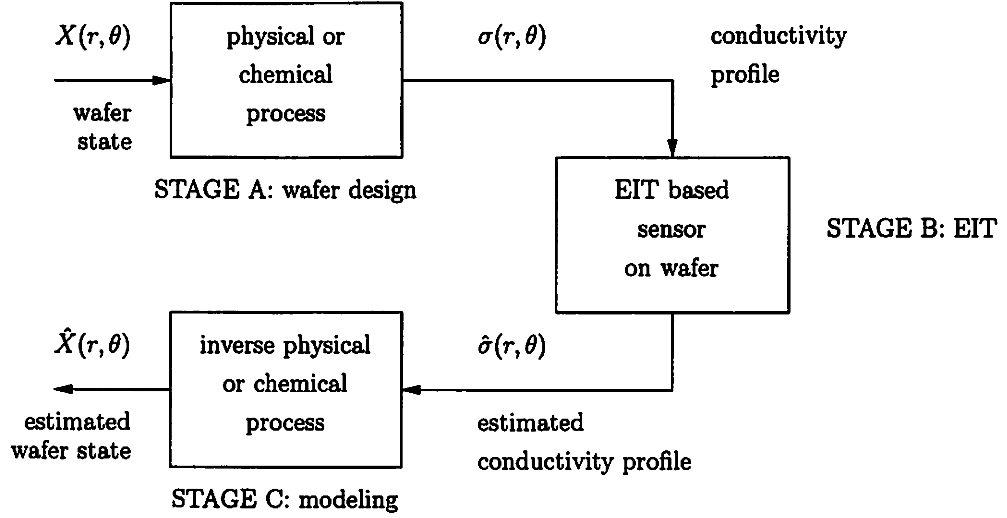

Figure 4.2: Schematic of three-stage approach.

film. For this, special electrodes have to be fabricated at the periphery of the conductive film on the wafer. During operation, these electrodes are used to inject different current patterns into the film and to record the resulting potentials. The recorded data is then fed into a standard EIT algorithm to obtain an estimate of the conductivity distribution, $\hat{\sigma}(r,\theta)$.

- **Stage C: Modeling**

  The goal in this stage is to estimate the state of interest from the estimated conductivity distribution $\hat{\sigma}(r,\theta)$ in the interior of the wafer by inverting the model in Equation (4.1), i.e.

$$\hat{X}(r,\theta) = f^{-1}\left(\hat{\sigma}(r,\theta)\right).$$

  Hence, an accurate model of the physical or chemical effect, exploited in stage A, has to be available.

In this approach stages A and C are sensor specific while stage B is generic.

4.4 Design and implementation issues

In the previous section, we presented a general approach to the design of EIT bases sensors. In Chapters 6 and 7 we will illustrate in detail this approach in the context of two simple applications. These illustrations serve as a proof-of-concept. To fully realize the potential of our EIT based sensors in a production environment many significant issues need to be addressed. These include:

- *Accuracy & sensitivity*

  The three stages, proposed in Section 4.3, will contribute differently to the overall accuracy and sensitivity of this EIT based spatial sensor. The sensitivity of the sensor will intimately depend on the physical/chemical effect which is exploited in stage A, while modeling errors in stage C will affect the accuracy of the EIT sensor. In addition, measurement errors in stage B will both affect the sensitivity and the accuracy of the sensor. Hence, each stage will require careful design.

- *Contamination*

  During semiconductor manufacturing, particle contamination at the wafer surface can cause short circuits, causing catastrophic yield loss. In addition, some materials and chemicals which are incompatible with standard semiconductor manufacturing practices can cause significant drifts in the electrical properties of the final device. Consequently, semiconductor manufacturers spend significant resources on maintaining a clean production environment. In particular, they are very reluctant to deploy non-product wafers, as these may contaminate product wafers in production tools. A sensor wafer should, therefore, strictly avoid exposing the production tool to any exotic materials which are incompatible with semiconductor manufacturing practices.

- *Lifetime*

  Long term exposure to harsh processes and elevated temperatures, conditions often encountered in etch chambers and bake plate applications, can affect the mechanical and physical integrity of any sensor wafer and degrade its performance. Consequently, the lifetime of a sensor wafer is limited. For example, the EIT based etch rate sensor, which is proposed in Chapter 6, is consumed during an etch experiment and lasts only a few etch cycles. Factors which will affect its lifetime are the nominal etch rate during the experiments and the initial film thickness.

- *Repeatability*

  Sensor repeatability is very important in our context. Semiconductor manufacturers periodically perform test wafer runs to ensure that their processes and/or tools are within the desired specifications. Based on these test runs, tool operators decide whether the process and/or tool perform satisfactorily. Small variations in test results can force the operator to take the tool off-line for further inspection, reducing Overall Equipment Efficiency. Consequently, false alarms due to small drifts and unrepeatable behavior of the metrology equipment are unacceptable.

- *Temperature compensation*

  In many semiconductor processes the wafer is exposed to external heat sources, causing the temperature of the sensor wafer to vary over time. These variations in temperature, in turn, can cause drifts in the sensor output. Consequently, temperature compensation may be required to obtain an unbiased sensor output.

- *Calibration*

  Over time, any sensor will inevitably show small drifts in its output. Consequently, the sensor will need to be periodically calibrated. Calibration proce-

dures that are simple and rapid need to be developed. This allows the end-used to periodically perform a calibration, ensuring reliable and repeatable measurement results.

- *Cost of ownership*

  The cost of ownership (COO) of a tool or sensor refers to all costs incurred by the user to acquire, utilize and maintain the tool or sensor. A low cost of ownership is paramount in order to penetrate the semiconductor metrology market and realize actual deployment in production facilities. In a semiconductor manufacturing context, the money saved by a sensor through improved product quality and reduced product variance must exceed the COO of the sensor over its life time.

Chapter 5

Etch processes in Semiconductor Manufacturing: an overview

Semiconductor manufacturers employ a variety of etching techniques to selectively remove exposed areas at the wafer surface to create the desired three dimensional devices such as transistors, capacitors and interconnects. In this chapter, we offer an overview of these etching techniques. After a brief introduction, we discuss the role of wet etch technologies, including its limitations. This section is followed by a discussion of plasma (dry) etch processes which are currently the method of choice for high performance etching.

5.1 Etch processes

Etch processes are critical to semiconductor manufacturing. They are used to transfer the complicated two dimensional patterns, designed by circuit engineers onto the wafer surface. To this end, the wafer is coated with photoresist which is subsequently patterned with sophisticated lithography equipment. The wafer is then selectively etched, removing exposed areas on the wafer surface.

Current CMOS process flows contain a large number of etching steps in which

different materials are selectively removed. One of the most critical etching steps in the CMOS process flow is the transistor gate etch. In this etch step, the transistor gates (thin lines of doped polysilicon) are etched out of a uniform layer of polysilicon on an extremely thin layer of SiO_2 (< 5 nm). Smaller gate lengths allow devices to be packed more densely. In addition, reduced gate capacitance allows transistors to switch faster, increasing the overall speed of the chip.

As the number of devices per chip increases, the interconnection of individual devices into functional units becomes more complex. To address this difficulty, semiconductor manufacturers have steadily increased the number of interconnect layers. Consequently, the importance of metal and interlayer dielectric etch steps, which define the metal lines as well as the vias between the different metal layers, has increased significantly.

5.2 Wet etching

Early on, the semiconductor manufacturing industry relied on wet etching techniques to define the desired patterns in the thin films deposited onto the wafer. Here, wafers are simply immersed in a bath containing chemicals which selectively etch the exposed layers. Due to the chemical nature of the etching process (etchants chemically react with the material of interest to create water-soluble or gaseous byproducts) wet etching can be very selective. However, despite its simplicity and high selectivity, wet etchants were soon supplanted by plasma (dry) etching techniques for the following reasons. First, wet etchants exhibit isotropic etching behavior, i.e. the etch front progresses in all directions at the same speed. Consequently, the wet etchant undercuts the protective mask layer, reducing the lateral dimension of the resulting feature and creating non-vertical sidewalls. Second, etch rate and uniformity are difficult to control. For example, small deviations in temperature can cause significant changes in etch rates across the wafer. Finally, suitably selective etchants are not available for

some novel and exotic materials such as silicon nitride and high-k dielectric materials for use in the gate stack. Despite these drawbacks, wet etching remains in wide use for non-critical process steps such as wafer cleaning and the removal of pad oxide and masking layers.

5.3 Plasma etching

Plasma (dry) etching is currently the method of choice for the selective removal of deposited materials to create three dimensional structures in critical process steps. It relies on the generation of highly reactive chemical species which can etch more vigorously than wet etchants. In addition, ionic species which are directed normal to the wafer surface make the etch process much more directional. Consequently, problems due to undercutting of the photoresist mask which plague wet etching are avoided, allowing more densely packed structures to be fabricated.

A plasma is a mixture of electrons and ionized particles which is, on average, electrically neutral. A basic plasma etching system utilized in semiconductor manufacturing applications is shown in Figure 5.1. It consists of a small vacuum chamber with two parallel electrodes. The wafer to be etched is placed on one of the electrodes. At low pressures (1 mTorr - 1 Torr) an electro-magnetic field between the two electrodes produces ionized particles and free electrons, creating a weakly ionized plasma. This plasma is often called a low pressure glow discharge due to the distinct optical emission of the excited gas species.

During etching a mixture of halogens containing reactive gases, such as CF_4, HBr and Cl_2 and diluting gases such as O_2 and Ar are fed into the process chamber. Free electrons in the plasma react with these gas species to create free radicals, electrically neutral species with incomplete bonding sites. For example, one free electron can dissociate CF_4 into the radicals CF_3 and F [80]. These radicals are highly reactive and bond quickly to the material to be etched to create volatile byproducts. For

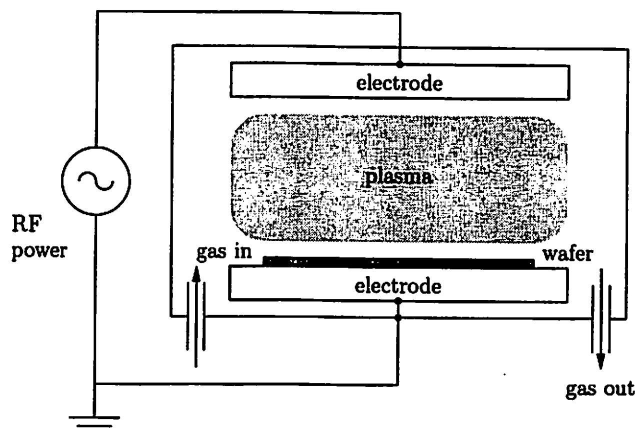

Figure 5.1: Basic plasma etching system [80].

example, four free F radicals can bond to a Si atom, creating SiF_4 gas. As is the case in wet etching, this chemical component in plasma etching is selective and isotropic.

The free electrons in a plasma have much smaller mass than the ions, making the electrons significantly more mobile. Due to their higher mobility, more electrons than ions are initially lost to the electrodes and the reactor walls, leaving the bulk plasma with a net positive charge with respect to the electrodes/walls. The resulting potential drop between the plasma and the electrodes/walls occurs in a small region near the electrodes, called the sheath. Free ions, entering the sheath region, are accelerated towards the electrodes/walls and strike the wafer perpendicularly, sputtering atoms from the exposed wafer surface. This physical component in the plasma etching process is in general less selective.

Etch rates during plasma etching are often significantly higher than the sum of the individual physical and chemical etching components. This enhancement in etch rate is attributed to ion-enhanced etching effects: the high energy ions which strike the wafer surface, facilitate one or more steps of the chemical etch process [80].

Despite its widespread use in the semiconductor manufacturing process, plasma etching remains poorly understood and extremely complicated. At any time, many dozens of reactions and processes take place in a plasma etcher, making it very difficult

to accurately model and/or simulate the complete etching process. In addition, many variables such as pressures, gas compositions and flows, RF powers and temperatures can be adjusted to influence the overall etching process. Consequently, equipment suppliers as well as semiconductor manufacturers spend significant resources to empirically tune their plasma etch processes [29]. This effort is particularly focused on optimizing etch rate/uniformity, etch profile, and selectivity while reducing and/or preventing substrate damage due to the bombardment by high energy ions and electrons [91].

Chapter 6

EIT based Etch Rate Sensors

In this chapter we discuss the design, fabrication and operation of a prototype etch rate sensor for use during semiconductor manufacturing. Our sensor uses standard EIT techniques to estimate the conductivity distribution of a thin film of conductive polysilicon across a wafer. The estimated conductivity distribution can, in turn, be related to the thickness of the polysilicon film from first principles. Differential thickness measurements from our prototype etch rate sensor correlate very well with optical thickness measurements.

The remainder of this chapter is organized as follows. First we motivate our decision to design a prototype etch rate sensor. This discussion is followed by an overview of current film thickness/etch rate metrology choices available to the semiconductor industry. We then discuss the design of our prototype etch rate sensor. In particular, we illustrate how the three stage approach, discussed in Section 4.3, can be effectively used to obtain spatially resolved etch rate information. In the subsequent two sections we elaborate on the experimental results obtained with this prototype sensor. We conclude this chapter with a discussion of the experimental results.

6.1 Motivation

Etching processes are extremely complex and depend on many factors that have to be carefully controlled. For example, plasma etching is sensitive to pressure, RF powers, and gas compositions/flows. Small variations in any of these parameters can significantly affect the overall process, resulting in undesirable etch results. Even the wet etch process, despite its relative simplicity, can be rather complex. To maintain consistent etch results, etch solutions often need to buffered. This prevents depletion of the active ingredients over time. In addition, the temperature of the etch solution needs to be actively controlled as the etch rates can be a sensitive function of temperature. As a result, tool and process characterization and recipe development is a vital but expensive and time-consuming process for both tool suppliers and IC manufacturers.

Etch processes are often tuned to reduce their sensitivity to variations in process parameters while maintaining acceptable performance. Nevertheless, etch processes drift away from the desired region of operation over time. For example, in some etch processes a thin protective film builds up over time on the chamber walls, adversely affecting the overall etch performance. In addition, extended exposure to the harsh plasma environment can degrade the integrity of certain mechanical parts inside the plasma chamber. If unchecked, these process drifts can easily result in yield loss on product wafer lots in high volume semiconductor manufacturing facilities. Hence, semiconductor manufacturers spend significant resources on regularly verifying proper operation of each production process and tool.

The most important performance metrics for a plasma etcher are: etch rate, etch uniformity and selectivity. The etch rate determines the achievable tool throughput and is obviously important for factory profitability. The etch process should exhibit a very uniform behavior both spatially, i.e. across the wafer, and over time (within run and run-to-run). This will result in die-to-die processing uniformity. Also, a uniform

process will reduce the overetch time needed to clear the whole wafer, increasing throughput and minimizing the adverse effects of overetching. Some areas on the wafer will clear faster than others, exposing the layer underneath to the etchant. In general, etching of the mask and the layer underneath is undesirable and should be avoided. Hence the etch process has to be very selective, i.e. the etch rate of the film to be etched should be substantially higher than etch rates for underlying layers or protective masks.

In order to characterize and/or verify the operation of a plasma etcher, process engineers process test wafers, covered with the layer of interest, through the plasma etcher. After processing, the thickness of the layer is measured and the spatial etch rate is computed. The computed etch rate, however, is an *average over time*, i.e. etch rate and uniformity variations during etching can not be detected by this method. The use of test wafers has several additional drawbacks. First, each test wafer corresponds to a lost time slot for a production wafer, reducing the overall equipment efficiency (OEE). Currently, non-product wafers account for more than 15% of all wafer starts in a production facility [91]. Consequently, semiconductor manufacturers will have to reduce the number of test wafers used for process characterization and/or verification to improve OEE, particularly for bottleneck tools. Second, test wafer require special preparation and can, often, only be used once, and provide a single sample of the process results. Consequently, many test wafers need to processed in order to obtain a good understanding of the influence of the different variables such as gas flow, pressure and RF power on the final etch process. Finally, test wafers often need to be analyzed off-line, affecting the turn around time between experiments.

Most of the aforementioned drawbacks can be attributed to the lack of temporal wafer state information during the etch process. For example, an autonomous sensor wafer (see Section 2.4) could provide valuable real-time wafer state information at different operating setpoints, including transient effects, in a single run, reducing the number of test runs and wafers. In addition, the recorded wafer state information

can be analyzed during or upon completion of the experiment, reducing turnaround times.

The technological and economic importance of having temporal etch rate/uniformity information is unquestionable. We will further investigate the feasibility of EIT based spatial etch rate sensors in this chapter.

6.2 Related work

There are a variety of in-situ metrology techniques for film thickness and/or etch rate measurement that are in common use. In this section we will briefly review some of these methods.

6.2.1 Optical methods

Many commercial metrology tools rely on optical techniques to measure film thickness. These tools project light on the sample of interest and record the reflected light. The properties of the reflected light, such as polarization and intensity, can then be used to infer the film thickness of interest.

Reflectometers analyze the intensity of reflected light from one or several lasers [5, 103] or a wide-bandwidth light source [73] to determine the film thickness. Consider a monochromatic light source focused onto the sample of interest. Some incident light will directly be reflected from the surface. However, if the film layer of interest is transparent, some light will also reflect from the substrate underneath. Depending on the wavelength used, constructive or destructive interference between the wavefronts will occur. Consequently, sweeping the incident wavelength, typically between 400 and 800 nm, will cause maxima and minima in the intensity of the reflected light. Given the refractive index of the material of interest, an optical model of the film stack is fitted to the observed intensity profile, yielding the thickness of the film of interest [80]. This method works well for films thicknesses between 20 nm and 20 μm

[73]. Alternatively, during an etch process the intensity of reflected monochromatic light will vary over time in a sinusoidal manner as the film thickness decreases. The time between a maximum and minimum corresponds to the time it takes to etch a distance equal to half the incident wavelength, hence, allowing the etch rate to be approximated. However this method cannot be used for films thinner than half an interference fringe [85]. An additional drawback of this method is the limited time resolution of the method, i.e. it only provides an average etch rate between successive maxima and minima [104]. To address this drawback, Vincent *et al.* [104] use Extended Kalman Filtering in combination with a dynamic model of the etch process and an optical reflection model of the film stack of interest. Their algorithm allows fast estimation of the etch rate from single and multiple wavelength reflectometry. This information can then be used to actively control the etch rate and the etch depth [103].

Ellipsometry is closely related to reflectometry. However, unlike reflectometry, polarized light is used. The reflected light will, in general, exhibit a different polarization, allowing both the index of refraction and the thickness of the film to be inferred [65, 80]. This technique relies on relative intensities in orthogonal polarization modes of the reflected light. Consequently, ellipsometry is relatively insensitive to slow drifts over time, making it suitable for in-situ applications. Ellipsometers can accurately measure both the index of refraction and the thickness of the film of interest (down to 1 nm compared to 20 nm with reflectometry [73, 80]).

In-line use of optical metrology comes at a significant price. The metrology equipment has to be integrated with the processing tool. This often requires adding additional viewports to the processing tool in order to obtain direct line-of-sight optical access to the wafer surface. In addition, problems with the integrated metrology can force the processing tool to be taken out of production for repair and/or maintenance, adversely affecting its productivity.

The accuracy of optical metrology is partially offset by the limited spatial reso-

lution. Optical metrology often focuses on a small spot of the wafer. The etch rate information obtained is often not representative for the rest of the wafer. Several groups have utilized advanced optics to focus the incident laser light on several spots on the wafer [5, 103]. However, the limited space around production tools in addition to the reluctance of equipment vendors to make major modifications to their tools, limits the potential of these solutions.

6.2.2 Sensor wafers

The use of special wafers consisting of an array of sensors mounted on their surface can address many of the shortcomings of optical methods for etch rate/film thickness metrology. First, sensor wafers resemble standard product wafers, eliminating the need for modifications to the processing chamber. Second, an array of sensors placed across the wafer surface can provide unprecedented real-time spatial wafer state information.

A novel in-situ etch rate monitoring technique was proposed in Baker *et al.* [6]. Their prototype sensor consisted of a polyimide platform which was micromachined onto a silicon substrate. The micromachined platform was electrostatically driven into resonance. The resonant frequency of the platform was measured capacitively while the drive frequency was swept with a network analyzer. To test their sensor, the micromachined platform was etched in a reactive ion etching (RIE) system, causing a near linear shift in resonance frequency over time. This shift in resonance frequency correlated well with the change in thickness of the polyimide platform. However, despite its proven performance, it is unlikely that this sensor will be utilized in an autonomous sensor wafer due to its complicated drive and measurement electronics.

An electrical etch rate sensor for use on autonomous sensor wafers was developed by Freed [40]. The sensor utilized the van der Pauw method to infer the thickness of a thin film of conductive polysilicon. The van der Pauw method is in general used to measure the sheet resistivity of an arbitrary shaped conductive film [100]. To that

end, four electrodes are placed at the periphery of the film of interest and currents are injected between two different sets of electrodes while the resulting potentials between the remaining two electrodes are recorded. From these two measurements, it is possible to infer the resistivity of the material, assuming that the thickness of the film is known. Alternatively, one can infer the thickness assuming that the resistivity of the material is known.

Three of these sensors in series have been successfully used in a gaseous XeF_2 etcher, providing spatial etch rate information. A significant number of these sensors will be required, though, to obtain reasonable spatial resolution, in particular if this approach is used for 300 mm wafers. However, each sensor has to be probed individually. Consequently, wiring a large array of these sensors can be cumbersome and expensive.

6.3 Etch rate sensor: design and operation

In the remainder of this chapter we will perform a feasibility study of a novel etch rate sensor which can provide spatially and time-resolved wafer state information. In contrast to previous approaches which employ an array of individual point sensors, we will develop a *single* sensor based on EIT to obtain spatial wafer state information.

6.3.1 Wafer design

The operation of any sensor based on EIT is characterized by three stages, as discussed in Section 4.3. The first stage involves the design of a special wafer which exploits a physical or chemical effect to map the variable of interest across the wafer into a conductivity distribution. The variable of interest in an etch rate sensor is the time-resolved thickness of the material to be etched; the etch rate can then be deduced by numerically differentiating the observed temporal thickness trajectory. Hence, an EIT based etch rate sensor has to map spatial film thickness into a conductivity

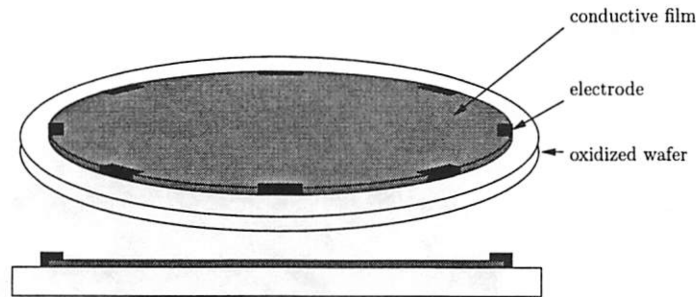

Figure 6.1: Schematic of EIT based etch rate sensor

distribution.

The sheet conductivity of a thin film of material depends on the thickness and the resistivity of the material used. Now consider a thin film of conductive material deposited onto an insulated wafer, see Figure 6.1. If this wafer is exposed to an etchant, the resistivity of the conductive material will, in general, remain constant. Hence, any change in sheet conductivity of the material can then be attributed to a change in thickness.

The geometry of the thin conductive film (thickness $\ll$ diameter) justifies the assumption that we are dealing with a two dimensional object. Recall from Section 3.2 that if the object of interest is, in fact, two dimensional, EIT techniques will actually infer the sheet conductivity instead of the conductivity. Hence, electrodes, equally spaced at the periphery of the conductive film on the wafer, can be used to perform simple EIT experiments to infer the sheet conductivity of the film. The thickness of the film t can then be calculated according to

$$t = \rho\sigma \tag{6.1}$$

where ρ is the known resistivity of the material.

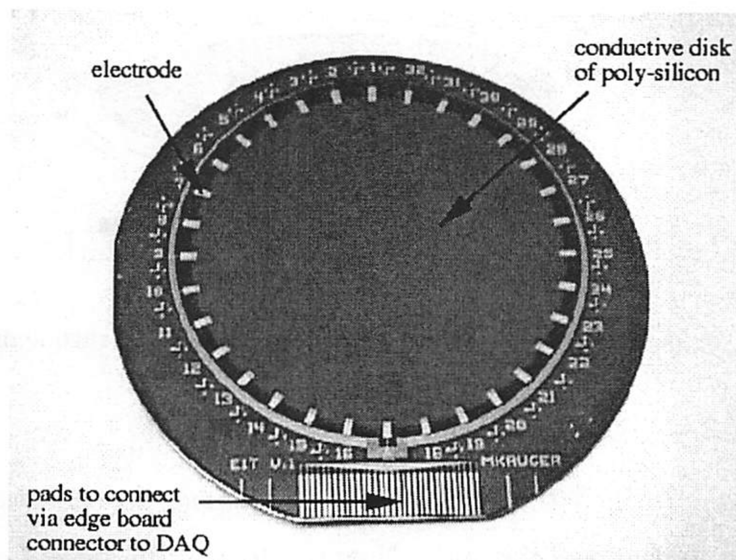

Figure 6.2: Picture of finished sensor wafer.

6.3.2 Process flow

As proof-of-concept, we have fabricated a prototype etch rate sensor for in-line and in-situ measurements using simple semiconductor processing techniques. The fabrication process included 2 patterning steps. First, we oxidized a standard 4 inch wafer to create an electrically isolated substrate. We then deposited a conductive layer of doped polysilicon onto the substrate. In the first patterning step we defined a circular disk with a radius of 3.5 cm in the conductive polysilicon layer. After aluminum deposition, we performed a second patterning step to define evenly spaced electrodes at the periphery of the polysilicon disk. In this patterning step we also defined aluminum leads which connect the electrodes at the periphery of the conductive disk to an array of contact pads at the perimeter of the wafer to facilitate quick testing with off-board data acquisition (DAQ) electronics. A photograph of a finished wafer is shown in Figure 6.2.

Several design iterations were performed to enhance the performance of the sensor wafer. Design changes were mainly focused on reducing the nominal conductivity of the sensor in order to enhance the signal to noise level. For this, the doping of the polysilicon layer as well as the thickness were reduced.

6.3.3 Experimental setup and hardware

We fabricated and tested our prototype etch rate sensor in the Berkeley Microfabrication Lab. In our experiments, we exposed the sensor wafers to liquid or gaseous etchants which selectively etch the polysilicon layer.

Before each experiment, we performed an EIT experiment to obtain a reference conductivity distribution of the initial sensor wafer. We then subjected the wafer to several etching cycles. After each cycle, we removed the wafer from the etchant and measured the new conductivity profile (in-line measurements). In addition, we performed thickness and/or the conductivity measurements of the wafer surface with a reflectometer and/or a four-point probe for validation purposes.

We used an edge board connector (SAMTEC MB1 series [84]), which fits on one side of the wafer, to connect the electrodes, via the contact pads, to a data acquisition (DAQ) system, see Figure 6.3. The DAQ system consisted of a 12 bit National Instruments data acquisition card (AT-MIO-64E-3), a shielded I/O connector block and several analog multiplexers (MAXIM DG406). The multiplexers, controlled by the DAQ card, selected two electrodes at a time to inject a DC current into the conductive layer. The resulting potentials on all electrodes were then recorded with the DAQ card and stored for further analysis. In order to reduce the noise on the data, we averaged the electrode potentials over multiple samples. Each EIT experiment consisted of several independent current patterns.

We performed our initial experiments in a XeF_2-etcher. XeF_2 is a very selective gaseous (isotropic) silicon etchant. Due to its high selectivity, it was not necessary to protect the aluminum interconnects or the substrate from the XeF_2. However,

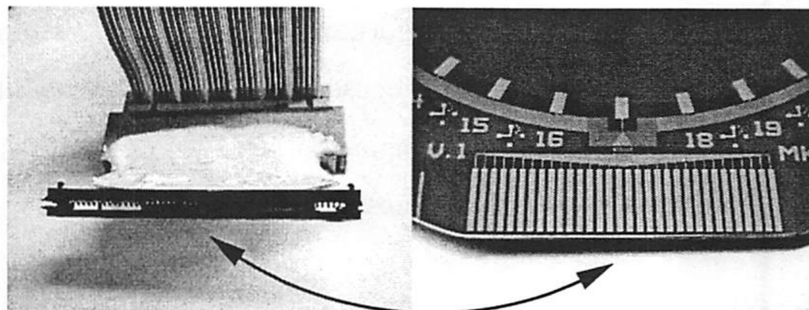

Figure 6.3: An edgeboard connector (left) connects the DAQ system to special pads at the perimeter of the wafer (right).

a thin layer of native oxide can inhibit etching. Consequently, XeF_2 can cause a very rough surface, making it difficult to validate the results with optical thickness measurement techniques. We therefore used a four-point probe to validate the XeF_2 etch experiment.

To circumvent the problem caused by etchant induced surface roughness, we also performed some experiments in a liquid silicon etchant. The surface of the polysilicon layer remained relatively smooth in the early stages of the etch process, allowing us to use optical techniques to validate the EIT results. However, the etch front tends to propagate faster along the polysilicon grain boundaries, once again causing surface roughness towards the end of the etch process.

In the next two sections we will discuss both experiments (gaseous and liquid etchant) in more detail.

6.4 Experimental results: XeF_2 etchant

In this section we discuss experimental results from our prototype etch rate sensor. To this end, the prototype sensor was selectively coated with photoresist and subjected to a gaseous silicon etchant. To validate our experimental results, the

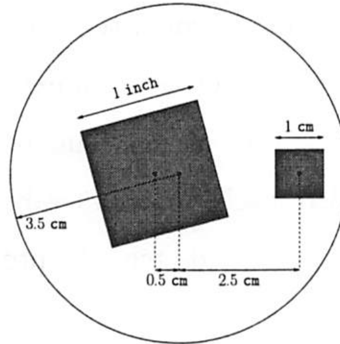

Figure 6.4: Mask used in XeF_2 experiment. Dark areas are etched in the experiment and should, hence, show a decrease in conductivity over time.

conductivities in the exposed areas were also measured with a four-point probe.

6.4.1 Wafer design

The sensor wafer consisted of approximately 1 μm of highly doped polysilicon on top of an insulating oxide layer. We performed all EIT measurements through 32 electrodes at the periphery of the disk. We used a special mask, see Figure 6.4, to define two square regions on the conductive disk to be etched. A 1 inch square, rotated 15° CCW, is located 0.5 cm left of the center of the polysilicon disk and a 1 cm square is located 2.5 cm right of the center. The remainder of the disk and wafer were protected during etching by photoresist. Hence, we expect changes in conductivity to occur only in the exposed square regions. At the end of the etching experiment both square areas were completely etched.

6.4.2 XeF_2 etcher

We performed the experiments in a Xetch® xenon difluoride etching system [110]. This tool is similar to the controlled pulse-etching system described in [19]. It consists of an aluminum process chamber with a clear Plexiglas lid. A separate source bottle

contains solid XeF_2 salt which, at room temperature, has a sublimation pressure of 2.7 Torr. A valve connects this bottle to an expansion chamber in which XeF_2 and N_2 are mixed before entering the process chamber. Once the partial pressure of XeF_2 and N_2 reach their specified levels, a second valve opens and the mixture flows into the process chamber. After a timed-etch, the process chamber is purged and a new etch cycle is initiated.

XeF_2 is a very selective gaseous (isotropic) silicon etchant. It exhibits high etch rates and reaction probabilities at room temperature without the use of any external excitation source or ion bombardment. Due to this high selectivity, a thin layer of native SiO_2 can significantly arrest the onset of etching [108, 19]. In addition, XeF_2 causes increased surface roughness over time [108, 19, 1].

6.4.3 Experimental details

Before the first etch experiment, we performed an optical thickness measurement of the conductive polysilicon layer at the surface of the sensor wafer, yielding a uniform thickness $t \approx 1$ μm of the conductive polysilicon layer; given that $\rho = 6.4 \cdot 10^{-4}\ \Omega \cdot \mathrm{cm}$, this results in $\sigma = 0.154\ \Omega^{-1}$ uniformly across the wafer. However, our EIT measurements with the unetched sensor wafer resulted in a non-uniform conductivity profile across the wafer. This non-uniformity is likely the result of the finite size of the electrodes on the sensor wafer (the electrodes are modeled as point contacts) and unaccounted resistances and nonlinearities in the DAQ system. In order to suppress the effect of these nonlinearities in the results obtained with the sensor wafer, we will look only at the *difference* between the estimated conductivity profile after etching and the conductivity profile before etching.

The experiment consisted of several etching cycles in a XeF_2 etching tool. In order to control the etch rate, we diluted the XeF_2 with N_2. After each cycle, we took the wafer out of the tool and connected it to the DAQ system with the edge board connector. Through this connector we injected DC currents and measured

the resulting DC potentials on each electrode. The measured data (averaged over 100 samples) was stored for further analysis. In order to enhance the sensitivity to conductivity changes in the center of the wafer, we injected currents through almost diametrically opposed electrode pairs, i.e. electrode pairs $(i, i+15),\ i = 1, \ldots, 17$ and $(i, i+17),\ i = 1, \ldots, 15$.

The potentials at all electrodes were recorded. However, line resistance and contact resistances (aluminum-silicon and wafer-edge board connector) affect the measured potentials at the current injecting electrodes. Hence, we decided not to use the distorted potentials at the current injecting electrodes in the inverse problem algorithm.

6.4.4 Results

At the start of the experiment σ was equal to 0.154 Ω^{-1} across the wafer. As the etch progresses, the conductivity in the exposed square regions slowly drops. Hence, we do not expect any change in conductivity in the unexposed regions, i.e. $\Delta\sigma = 0\ \Omega^{-1}$. For the exposed regions, we expect a net change in conductivity of $-0.154\ \Omega^{-1}$ when these areas are completely etched.

Prior knowledge of the object of interest can be fruitfully used to enhance the performance of any EIT algorithm. For example, in this etch experiment we can distinguish three different regions on the wafer: the two squares and the unexposed area. If we assume that the conductivity in each region changes uniformly during the experiment, we will only need three parameters to describe the conductivity profile. Figure 6.5 shows the estimated change in conductivity in each region over time. Conductivity measurements, conducted with a four-point probe, are also shown. The estimated and measured conductivity change show very good agreement, particularly at the beginning of the experiment.

During etching, differences in exposed surface areas across the wafer can result in different etch rates across the wafer. This so-called loading effect [80] is very well

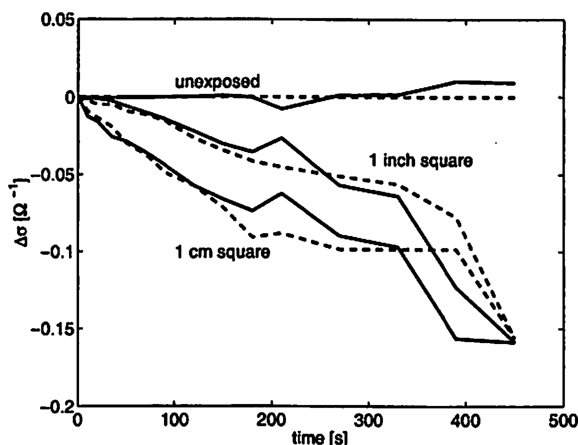

Figure 6.5: Change in conductivity for different areas on wafer: estimated (solid) and four-point probe data (dashed).

noticeable in Figure 6.5.

6.5 Experimental results: wet silicon etchant

It was not possible to corroborate the performance of our EIT based etch rate sensor in the XeF_2 etcher using independent film thickness metrology. This is principally because the surface roughness of the etching technique precluded the possibility of accurate or meaningful film thickness measurements via optical methods. These factors motivated us to examine the performance of our EIT etch rate sensor in a wet silicon etch process. Here, the etched surface remains moderately smooth, at least in the initial stages of the process. We now detail our experimental setup and results in this component of our work.

6.5.1 Wafer design

The sensor wafer in this experiment contained 16 equally spaced electrodes around a polysilicon disk with radius r = 3.5 cm. The polysilicon layer was lightly doped

with an average thickness $t = 2144$ Å and an average sheet resistance $R_s = 86.2\ \Omega/\Box$. The sensing area was completely exposed to the etchant, allowing real spatial etch rate measurements to be performed. All aluminum lines were protected from the wet etchant by a thin layer of photoresist.

6.5.2 Experimental details

The sensor wafer was subjected to five timed etching cycles (totaling 165 seconds) by gently dipping it into a silicon etch solution (50 HNO_3 : 20 H_2O : 1 NH_4F), with a nominal etch rate of approximately 3000 Å/min [108]. In order to slow down the etch rate, this solution was diluted. Between each etch experiment, the thickness of the polysilicon layer was optically recorded at 36 fixed sites, 20 sites in the interior of the wafer and 16 sites immediately adjacent to the electrodes (see Figure 6.6). In addition, after each etch cycle, the wafer was connected to a DAQ system through an edge-board connector and subjected to 50 EIT experiments, each consisting of 16 current patterns. The resulting potentials at all electrodes were then recorded and stored for subsequent analysis.

The granular structure of the polysilicon layer, caused the etchant to advance faster along the grain boundaries. Consequently, the surface roughness of the polysilicon layer increased slowly over time. After being exposed to the etchant for 105 seconds surface roughness caused the variability in the optical thickness measurements to be unacceptable. Consequently, we do not have any reliable data to validate the EIT experiments from the third etch cycle onwards.

6.5.3 Results: absolute measurements

After each etch cycle, 50 EIT experiments were performed. This redundancy in EIT data after each etch cycle allows us to analyze the effects of noise on the final estimate and to assess the repeatability of the experiments. We first computed the

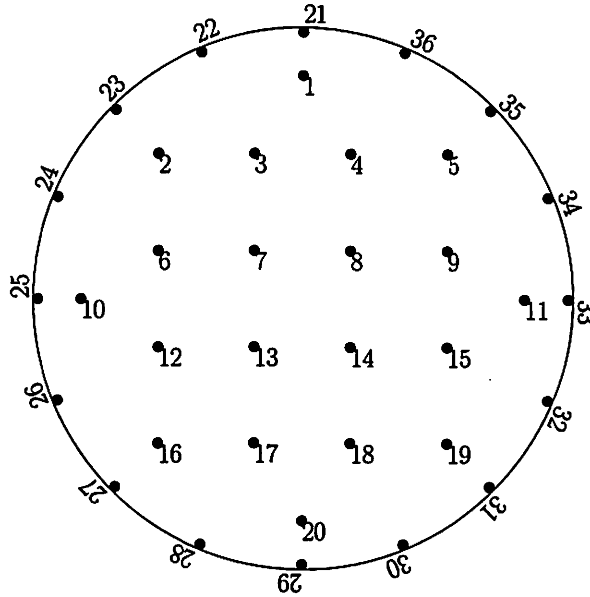

Figure 6.6: Location of thickness measurement sites.

average potential pattern at the boundary for each etch cycle and current pattern. Next, for each etch cycle, we computed the difference between these average potential patterns and the 50 observed potential patterns. The histograms of these differences for each etch cycle are shown in Figure 6.7. From this figure it is evident that the variance of the potential measurements is well within 1 mV. However, we do see a slightly larger variance, possibly due to a deterioration of the contact between the electrodes and the disk, after the last etch cycle.

The average potential patterns where used to estimate the absolute conductivity distribution across the wafer after each etch cycle. Our EIT algorithm, which utilized the Kriging basis function approach as discussed in Section 3.4.3, estimated the conductivity at 36 sites at the wafer surface. These correspond with the sites where optical thickness measurements were performed to validate the EIT sensor data. The estimated conductivity can be converted to thickness measurements according to Equation (6.1) if we know the resistivity ρ of the lightly doped polysilicon. There are two ways to obtain an estimate of ρ. First, one can infer the resistivity from

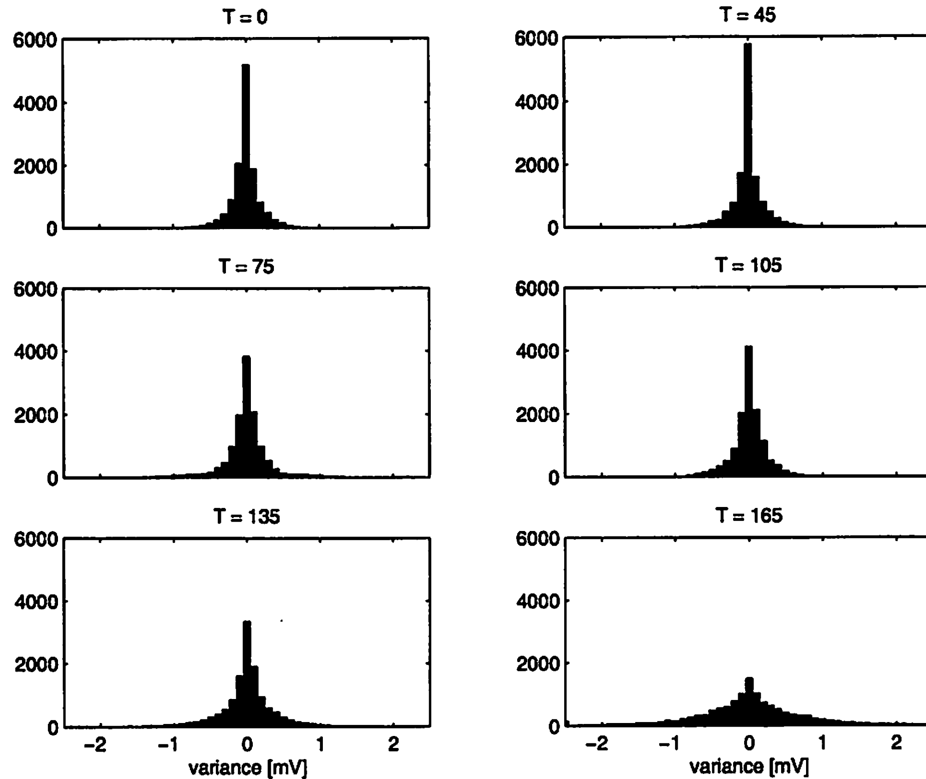

Figure 6.7: Noise distribution around mean potential pattern for different etching times.

four-point probe measurements and optical measurements before the etching cycle. Second, one can infer the optimal ρ such that the error between the EIT thickness measurements and the optical thickness measurements is minimized. The first approach resulted in $\rho = 1.85 \cdot 10^{-3}\ \Omega \cdot \mathtt{cm}$. However, this estimate is not very accurate due to the modest repeatability and accuracy of the four-point probe measurements. The second approach resulted in $\rho = 1.79 \cdot 10^{-3}\ \Omega \cdot \mathtt{cm}$. Figure 6.8 shows the absolute thickness, measured with the optical metrology tool and the EIT sensor, at the 36 measurements sites before the start of the experiment and after the first 2 etching cycles.

It is clear from this graph that the absolute thickness measurements from the EIT

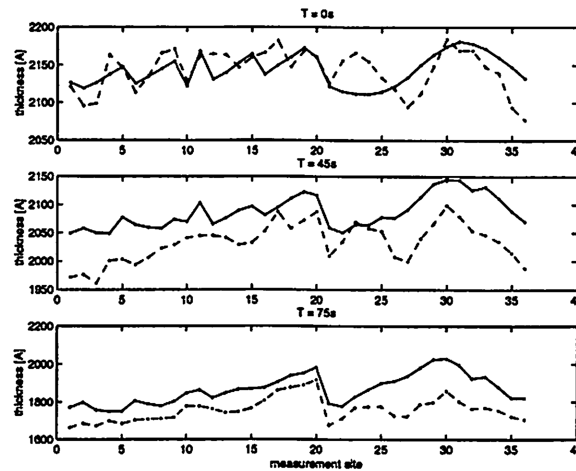

Figure 6.8: Thickness at measurement sites according to optical metrology (solid) and EIT sensor (dashed).

sensor do not compare well with the optical thickness measurements. This is probably due to nonlinearities in the DAQ system as well as undermodeling of the electrodes.

In order to assess the influence of measurement noise on the 36 thickness estimates, we applied the EIT algorithm to all 50 individual EIT data sets after each etch cycle. Figure 6.9 shows a histogram of the variance around the 36 thickness measurements based on the averaged potential patterns. From this figure it is evident that the influence of the measurement noise is relatively small. The variance in the estimated parameters is well within 1 nm. This confirms that the estimation procedure is robust and repeatable, i.e. small amounts of measurement noise result only in small thickness variations. This correlates well with the histogram of the measurement noise in Figure 6.7. It is clear that increased variance in the potential measurements after the last etch cycle results in a significantly larger variance in the thickness measurements.

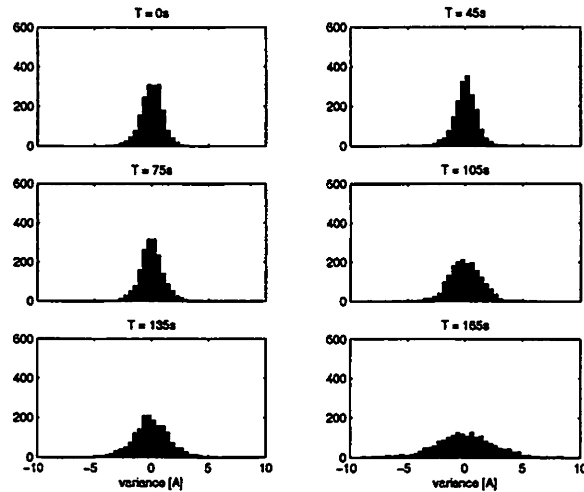

Figure 6.9: Distribution around mean of the estimated parameters for different etching times.

6.5.4 Results: differential measurements

From the previous section it is clear that the EIT sensor is not capable of measuring absolute thicknesses. The most likely culprits which cause this are nonlinearities in the DAQ system, undermodeling of the electrodes and biases in the potential measurements. It is not unreasonable to assume that these factors remain stationary. We can therefore subtract the initial profile to obtain unbiased differential measurements. This approach is perfectly suitable in our applications as we are not aiming to obtain very accurate absolute thickness measurements. There are many existing tools that can do this reliably. We are principally interested to see how the etch progresses over time. In the remainder of this section we will therefore focus on the change in thickness over time with respect to our initial thickness profile as measured with our EIT based etch rate sensor.

Figure 6.10 shows the change in thickness at the 36 measurements sides after one and two etch cycles according to the optical metrology and the EIT based sensor. Apart from an increasing offset, the differential thickness measurements at each site

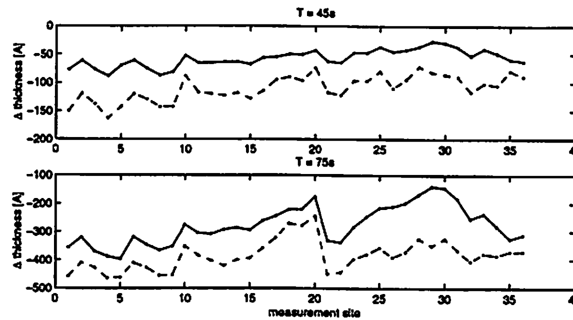

Figure 6.10: Change in thickness at measurement sites according to optical metrology (solid) and EIT sensor (dashed).

as observed with our EIT based sensor seem to correlate very well with the optical measurements.

In order to assess the spatial measurement capabilities of the sensor, we will analyze the change in thickness along various cross sections of the disk (see Figure 6.11). The changes in thickness along the different paths, measured with the optical metrology tool and the EIT based sensor, are shown in Figure 6.12 and Figure 6.13, corresponding respectively to 45 sec and 75 sec of etching. Apart from the offset, the variations in thickness along the different cross sections as measured with the EIT based sensor correspond well with the interpolated thickness variations as measured with the optical metrology.

The color coded pictures in Figure 6.14 and Figure 6.15 show the spatial change in thickness after the first and second etching cycle. Both the optical metrology tool and the EIT based sensor show the same remarkable etching pattern, corresponding to a significantly nonuniform etch.

The results clearly show that the differential thickness measurements are significantly better than the absolute measurements. They correspond well with optical thickness measurements. However, there is a substantial bias, which increases over time. The bias between the optical measurements and the EIT based measurement

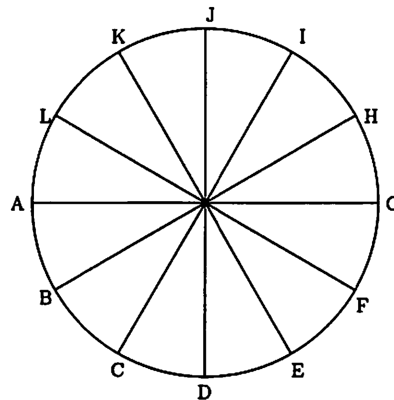

Figure 6.11: To assess the spatial measurement capabilities of our sensor, we analyze the change in thickness along the cross sections of the polysilicon disk shown here.

can be attributed to the fact that these techniques are actually measuring *different* variables. The EIT based sensor measures the conductivity, which is converted to an *electrical* thickness. During etching the etch front at a microscopic scale does not progress uniformly, i.e. the etch progresses faster along the grain boundaries of the polysilicon, causing surface roughness. Consequently, the electrical film thickness will be smaller than the optical film thickness. Over time, surface roughness increases, causing the bias between the two to increase as well.

Due to surface roughness, the optical metrology could not properly assess the thickness of the film after the second etch cycle. Consequently, we cannot verify the etch rate results, obtained with the EIT sensor, after the second etch cycle. However, measurement noise (Figure 6.7) and variance in the estimated thicknesses at the 36 measurement sites (Figure 6.9) do not increase dramatically over time. Hence, we believe that the differential EIT measurements after the second etch cycle, can still provide valuable information regarding the etch process. Figure 6.16 illustrates the evolution of the electrical thickness over time along the cross sections shown in Figure 6.11. The change in thickness over time as estimated with the EIT sensor for each measurement site is shown in Figure 6.17. From this graphs it is evident that the etch rate during the first etch cycle is much slower than the other etch cycles. This

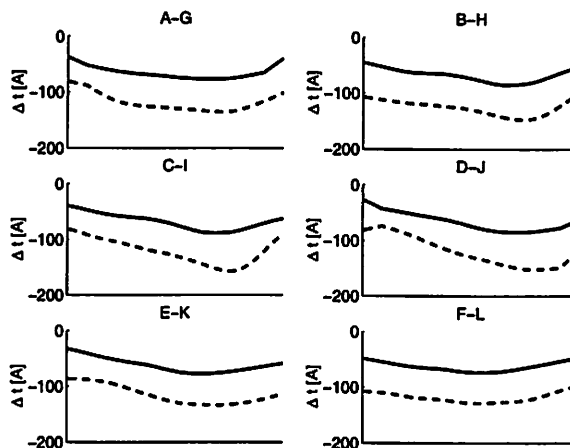

Figure 6.12: Cross sectional view of change in thickness after 45 sec: optical (solid), EIT (dashed).

reduction in etch rate is due to the thin layer of native oxide, present on the wafer surface at the beginning of the experiment [108]. As expected, consecutive etching cycles exhibit a linear decrease in thickness over time, corresponding to an average etch rate of approximately 600 Å/minute.

6.6 Discussion of results

In this chapter we have discussed a novel EIT based etch rate sensor for use during semiconductor manufacturing. A prototype etch rate sensor has been designed, fabricated and tested both in a gaseous XeF_2 etchant and a wet silicon etchant. Results obtained with the etch rate sensor are very repeatable and correlate well with four-point probe and/or optical thickness measurements. However, absolute thickness measurements are not possible due to nonlinearities in the DAQ system, and undermodeling of the system. In addition, surface roughness introduces a significant offset between the thickness measured with the EIT sensor and optical thickness measurements.

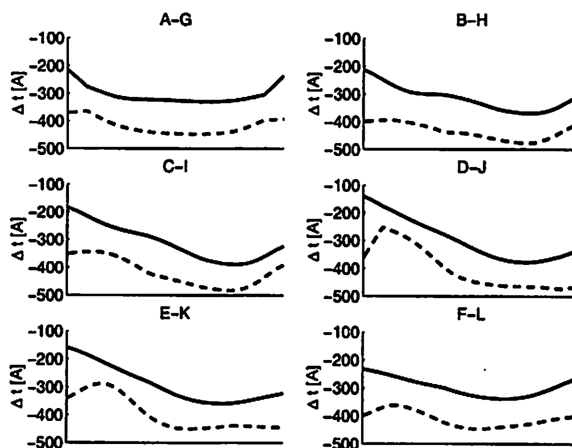

Figure 6.13: Cross sectional view of change in thickness after 75 sec: optical (solid), EIT (dashed).

Plasma etch processes are currently the method of choice to selectively remove materials from the wafer surface. Therefore, any practical etch sensor has to be able to withstand the harsh plasma environment. However, in its current evolution the EIT sensor discussed in this chapter will not operate reliably and safely within a plasma chamber. In particular, charge could accumulate onto the conductive polysilicon disk, which is directly exposed to the plasma. Consequently, parasitic currents could flow into the conductive disk. The magnitude and location of these currents are unknown. This causes problems in our current EIT inverse algorithm. In order to deal with this problem, we suggest replacing the DC currents in our EIT experiments with AC currents. If we choose the frequency of the injected AC currents outside the bandwidth of plasma induced currents, we can use standard techniques to filter these parasitic effects. *A priori* information of the etch process can also be effectively used to filter out undesirable and/or unrealistic artefacts in the estimated conductivity distribution. For example, we know that the thickness of the film of interest will monotonically decrease as the etch process progresses. Hence, we can use a simple Kalman Filter to enforce monotonicity in the estimated film thickness across the

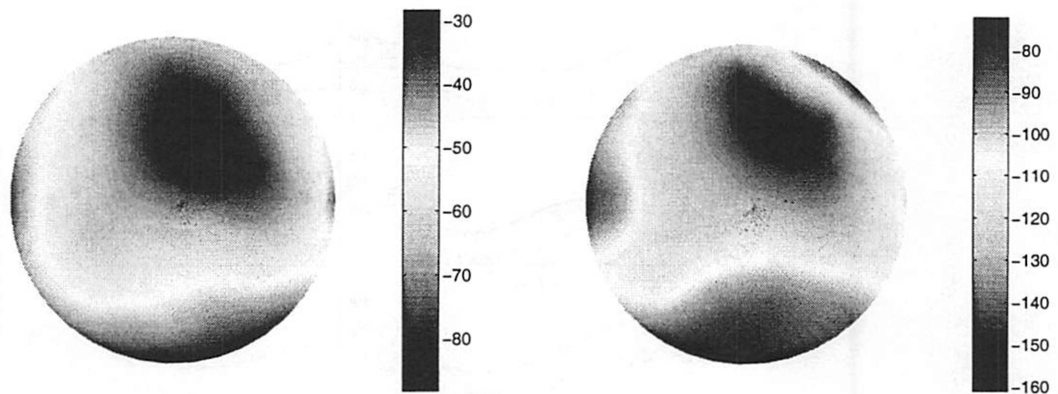

Figure 6.14: Change in thickness in Å after 45 sec; optical (left), EIT sensor (right).

sensor wafer.

The EIT based etch rate sensor developed in this chapter estimates the thickness of the film of interest based on its conductivity (the conductivity is linearly related to its thickness) and can be used to measure the thickness of any conductive material. Consequently, unlike optical in-situ etch rate sensors, this sensor is not restricted to transparent films only and could, for example, provide valuable etch rate information of opaque films, such as aluminum, in-situ. Conversely, our sensor requires an electrically conductive film. This excludes a class of materials of great interest in the semiconductor manufacturing industry such as dielectric materials.

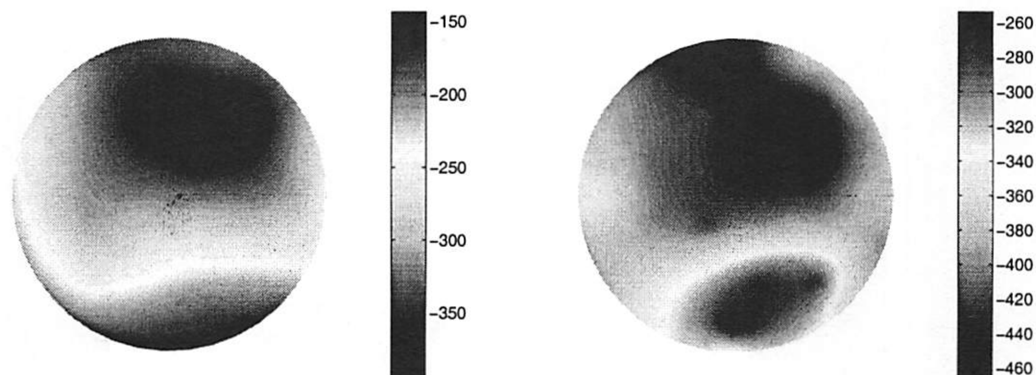

Figure 6.15: Change in thickness in Å after 75 sec; optical (left), EIT sensor (right).

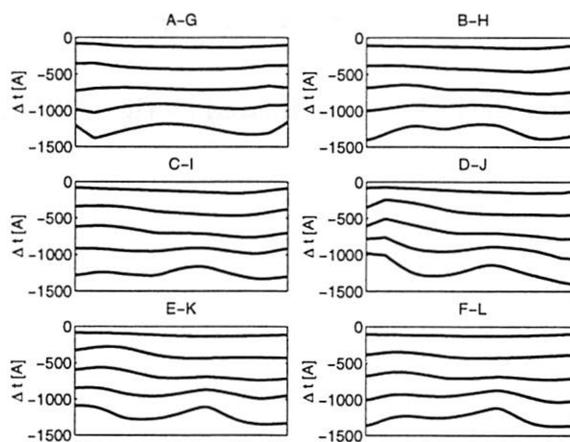

Figure 6.16: Cross sectional view of change in thickness as measured with EIT sensor after 45, 75, 105, 135 and 165 seconds.

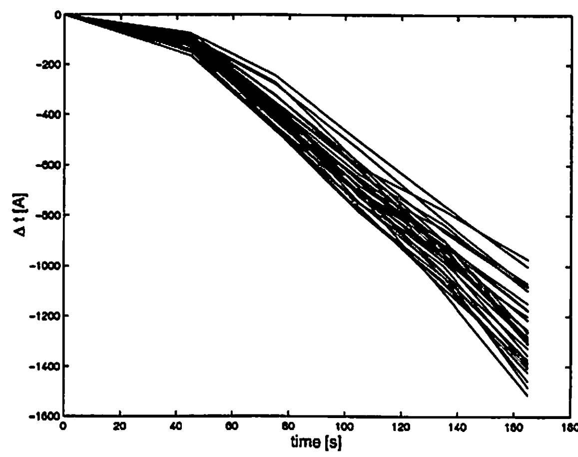

Figure 6.17: Change in thickness, estimated by the EIT sensor at the 36 measurement sites, vs time.

Chapter 7

EIT based Plasma Potential Sensors

During plasma processing charges can locally accumulate at the wafer surface. This wafer charging phenomenon can seriously damage circuitry and results in unacceptable yield losses. The effect is exacerbated by spatial nonuniformities in the plasma. Metrology solutions that can monitor wafer charging are invaluable to the industry. They can be used as simple diagnostic and monitoring tools, or for optimizing plasma recipes to minimize wafer charging effects. In this chapter we propose a novel EIT based sensor which can provide temporal and spatial wafer surface potential information during plasma processing.

The remainder of this chapter is organized as follows. First we explain the mechanisms that cause charge accumulation at the wafer surface during plasma etching. This discussion is followed by an overview of the various metrology choices currently available to assess the uniformity of plasma processes and to detect charging effects at the wafer surface. We then propose a novel EIT based sensor to measure wafer potentials. This sensor applies traditional EIT techniques to a resistive network containing discrete transduction elements. We conclude this chapter with several simulation studies which illustrate the feasibility of our approach.

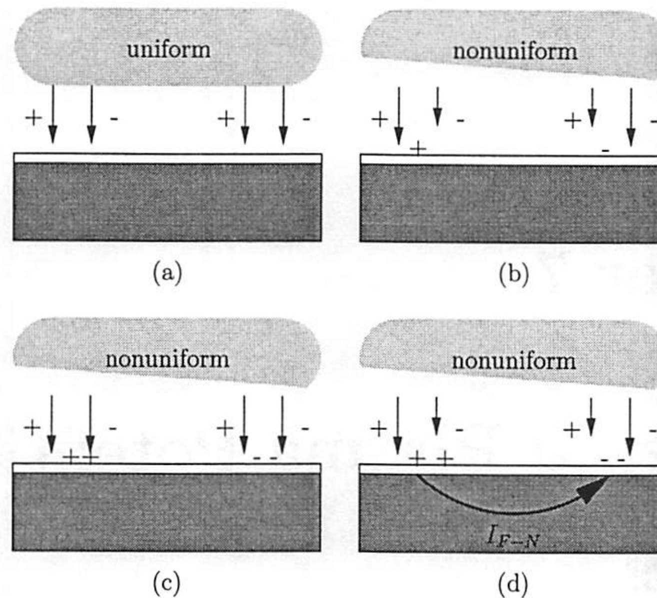

Figure 7.1: A uniform plasma is characterized by a balanced flow of ion and electron fluxes across the sheath (a). In a nonuniform plasma, these fluxes are, at least initially, not balanced (b). Accumulation of charge at the wafer surface can balance the ion and electron fluxes (c) or it can result in a Fowler-Nordheim current through the dielectric material (d) [35].

7.1 Motivation

A critical problem encountered in plasma processes (and also ion implantation) is the undesired accumulation of charge on dielectric materials at the wafer surface. This accumulation of charge can be particularly detrimental to the thin metal oxide semiconductor (MOS) gate oxide, causing a decrease in oxide breakdown voltage and reducing device yield and reliability [46, 37, 39, 97].

In a uniform plasma, the local electron and ion fluxes across the sheath between the bulk plasma and the wafer surface are in balance over each RF cycle (average current to the wafer is zero) [35]. Conversely, a nonuniform plasma can cause nonuniform electron and ion fluxes to the wafer surface. A nonconductive surface, such as a wafer covered with an oxide layer, will prevent surface currents from flowing to balance these nonuniform ion and electron fluxes from the plasma, causing the local accumulation

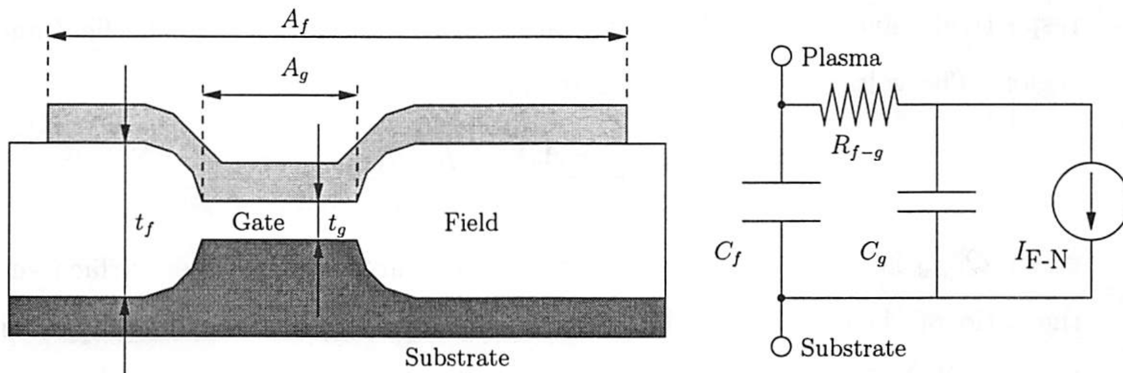

Figure 7.2: Antenna effect (left) and its electrical circuit equivalence (right) [35, 33].

of positive and negative charges at the wafer surface [35, 36, 38]. Further charge accumulation will stop when local ion and electron fluxes across the sheath become balanced. This will happen when appropriate local wafer surface potentials affect the incoming fluxes, or when a tunneling current closes the current loops. In this second situation, the tunneling current is known as the Fowler-Nordheim (F-N) current (see Figure 7.1). The relation between the F-N current and V_{ox}, the potential difference across the gate oxide, is given by [93, 34]:

$$I_{\text{F-N}}(V_{ox}) = K\frac{V_{ox}^2}{t_g}\exp\left(-\frac{Bt_g}{V_{ox}}\right)$$

with t_g the thickness of the gate oxide and K and B constants related to the geometry and quality of the gate oxide. This F-N current can seriously degrade the electrical performance of the oxide.

Charging damage to the gate oxide is often enhanced by the so-called antenna effect [37, 34, 33]. Consider a typical MOSFET device with the conductive gate extending over a much thicker field oxide as illustrated in Figure 7.2. The total capacitance C_{total} of the device is then given by [33]:

$$C_{\text{total}} = C_g + C_f = \frac{\epsilon_{ox}A_g}{t_g} + \frac{\epsilon_{ox}A_f}{t_f} = \epsilon_{ox}\frac{(A_f t_g + A_g t_f)}{t_f t_g}.$$

Here, ϵ_{ox} is the permittivity of oxide, C_f and C_g are the capacitances above the field and gate oxides respectively, t_f and t_g are the thicknesses of the field and gate oxides

respectively, and A_f and A_g are the areas of the antenna above the field and gate region. The voltage V_g across the gate oxide is:

$$V_g = \frac{Q_{\text{total}}(A_f + A_g)}{C_{\text{total}}} = \frac{Q_{\text{total}} t_f t_g}{\epsilon_{ox}} \frac{(A+1)}{(At_g + t_f)}$$

where Q_{total} is the accumulated charge per unit area at the wafer surface and A is the ratio of A_f to A_g. As A increases from 0 to ∞, the effective capacitance of the overall device changes from C_g to C_f. Note that C_f is in general 10-100 times smaller than C_g. Consequently, the potential across the gate for a fixed accumulated charge increases significantly with larger A. This results in higher F-N currents which adversely affect the likelihood of early oxide breakdown [66].

Future device generations will exhibit even smaller gate areas. According to the International Technology Roadmap for Semiconductors, the physical gate length will decrease from 70 nm to 35 nm within the next couple of years [91]. If we assume that the gate width will decrease accordingly, the gate area will reduce by a factor of 4. However, the interconnect area which extends over the field oxide will not scale proportionally. As a result, the parameter A can increase significantly, making the antenna effect much more pronounced as we move to smaller feature sizes.

The accumulation of charge at the wafer surface can also affect the overall etch profile. Consider an ion which is accelerated towards the wafer surface across the sheath. In the ideal case, the ion will impact the wafer surface with normal incidence, resulting in a very anisotropic etching process. However, if significant areas of accumulated charge are present on the wafer surface, the incoming path of these ions will become more glancing. This will result in undercut and/or slanted profiles [72]. This mechanism becomes particularly critical for deep contact hole etching and dielectric etching.

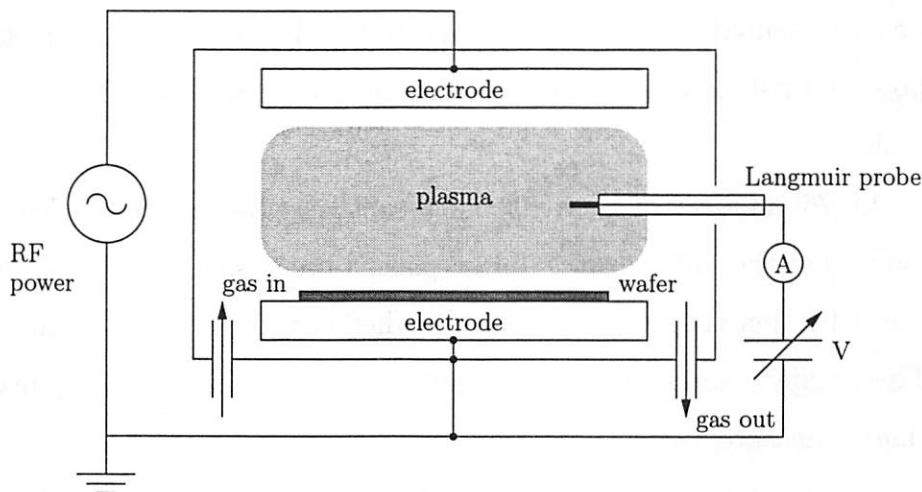

Figure 7.3: Schematic of Langmuir probe used for plasma diagnostics.

7.2 Related work

There is a compelling need to assess the extent of wafer charging during plasma etch processes. This information can then be used to adjust or tune the process to alleviate the adverse effects of wafer charging. In this section we will briefly discuss the principal measurement techniques currently used to assess wafer charging.

For more than 50 years, Langmuir probes have been used to analyze glow discharges. Here, a small conductive probe tip is placed in the plasma. The probe tip is then DC biased with respect to the chamber wall. The current to the probe tip is recorded for various values of the applied bias potential [87]. The scheme is illustrated in Figure 7.3. The resulting current-voltage characteristic can reveal important plasma parameters such as the plasma potential, the floating potential, and ion and electron energies and densities. Moving the probe inside the process chamber yields spatial plasma state information, allowing the assessment of the plasma uniformity. Plasma nonuniformities observed with Langmuir probes correlate well with measured oxide failures across the wafer due to wafer surface charging [35, 38]. However, the Langmuir probe is an invasive technique that will distort the plasma process

being measured. As a result, this indirect and time consuming method to assess the potential risk of wafer charging is unsuitable for use in high volume manufacturing tools.

In [76] an array of micromachined cantilever beams was used to assess the charge induced at the wafer surface during plasma processing. The beams exhibit a mechanical deflection towards the substrate when charges accumulate at the wafer surface. These deflections can then be optically measured in-situ, yielding reasonably accurate charge measurement ($< 5\%$ error).

During plasma processing, some beams can deflect sufficiently to touch the substrate and remain permanently adhered to the substrate even after discharge. By creating an array of beams with different stiffnesses, this phenomenon can be exploited to measure the maximum charge during wafer processing across the wafer. Visual inspection of the beams upon completion of the process can then quickly reveal the uniformity of the plasma. However, this approach has several drawbacks. First, this method does not allow to distinguish between positive and negative charges during wafer processing. Second, in-situ operation requires access to an optical viewport and the number of locations which can be simultaneously sampled is limited. Finally, visual inspection upon completion can only reveal the maximum absolute charges achieved during wafer processing, i.e. temporal wafer charging information is completely lost.

CHARM-2 monitor wafers provide a sophisticated alternative to measure the effects of plasma nonuniformities at the wafer surface during wafer processing [62, 106]. These wafers employ an array of pre-programmed floating gate EEPROM devices, which are sensitive to electro-static charging effects. During plasma processing accumulation of charge on the floating gate, which is exposed to the plasma, will alter the EEPROM threshold voltage. After processing, this shift in threshold voltage can be measured with a special probing system. These monitor wafers can provide a wealth of spatial wafer state information, including surface potentials (positive and

negative) and charge fluxes. Consequently, these wafers have been successfully used in many different applications [62, 61, 106]. However, these wafers only record peak wafer states. Temporal wafer state information is again lost. In addition, special testing equipment is required to program and interrogate the EEPROM devices. If this equipment is not locally available in the fab, turnaround times are severely impacted.

A single plasma etch process usually consists of several steps, each with different settings for gas compositions and flow rates, RF powers and pressures. Consequently, a wafer will experience changing plasma conditions during a single plasma etch process. In order to assess the risk of wafer charging across the process, temporal wafer charging information is necessary. To this end, a special tethered wafer has been developed, capable of measuring real-time wafer charging during processing [63, 82, 64]. This wafer consists of an array of aluminum pads on a layer of oxide. During plasma processing the DC voltage between these pads and the wafer substrate are recorded, providing wafer charging information during transient conditions. The operating simplicity of this metrology technique makes it an attractive candidate for use in an autonomous sensor wafer. However, in order to obtain reasonable spatial resolution, a significant number of these sensors is required, in particular if this approach is used for 300 mm wafers. Each sensor has to be probed individually, and the necessary interconnections can prove expensive.

A similar sensor wafer approach has been used to develop an array of planar Langmuir probes at the wafer surface [53]. Here, ten circular metal pads were patterned onto an oxidized wafer. During plasma processing, the Langmuir probe array is DC biased at -70 volts with respect to ground to maintain the probe array in the ion saturation regime of the current-voltage characteristics. The resulting currents through the probes are then recorded, yielding time-resolved and spatial ion flux information. However, the large DC bias potentials needed during operation necessitate an external power supply. Consequently, use of this this probe array is limited to experimental tools for use by equipment manufacturers.

7.3 EIT: a resistive network approach

In the remainder of this chapter we will conduct a feasibility study of a novel EIT based sensor which can provide temporal and spatial wafer surface potential information during semiconductor manufacturing.

In stark contrast with traditional biomedical EIT applications, in the semiconductor metrology context we have the luxury of designing the object being imaged. In this section we will discuss how we can exploit this to circumvent some of the problems associated with standard EIT approaches. We begin by briefly discussing some of the disadvantages inherent in traditional EIT approaches. We will then detail our approach which is based on a resistive network with discrete components. We note that our approach was inspired by work of Baroudi *et al.* [10, 9]. Their research focused on estimating gas temperature distributions based on EIT measurements of the resistance of thin metal filaments positioned across the gas flow.

7.3.1 Downsides continuous EIT problem

Traditional EIT techniques have been used successfully in a variety of applications, including our etch rate sensor (see Chapter 6). However, these traditional EIT approaches have several shortcomings.

First, it can be very difficult to accurately model the object of interest. An inaccurate model in the forward problem results in unreliable predictions for the edge potentials. These can, in turn, yield erroneous estimates for the conductivity distributions in the inverse problem. Modeling of boundary conditions at the electrodes can be particularly difficult. A variety of electrode models have been proposed to describe the current flow near the periphery.

Second, the iterative approaches utilized in many EIT algorithms are slow and computationally expensive. Many EIT algorithms rely on FEM techniques to solve the forward problem numerically. However, the accuracy and speed of these FEM

techniques depend on the discretization used. A coarse discretization (i.e. relatively few nodes and elements) will accelerate the computation. However this benefit comes at the expense of accuracy in the forward problem, which, in turn will affect the accuracy of the inverse problem in the remote interior of the wafer.

Finally, the sensitivity to changes in conductivity is not uniform across the object [113]. For example, conductivity changes near the periphery are easier to detect than changes in the center. Consequently, small amounts of noise on the potential measurements can significantly affect the estimated conductivity profile in the remote interior of the wafer.

7.3.2 Resistive networks

The FEM techniques, utilized in many EIT algorithms to solve the forward problem, approximate the conductive continuum inside the object with a large resistive network. A natural specialization is to replace the conductive continuum on the wafer with an array of discrete components to create a resistive network as shown in Figure 7.4. This approach is in particular useful in our application where we have access to the interior of the object being imaged. Using a resistive network, instead of a conductive continuum, allows us to circumvent some of the problems associated with traditional EIT approaches.

First, modeling a resistive network is much simpler than modeling a conductive continuum. For example, modeling the complex boundary conditions in the vicinity of the electrodes as required in the continuum case is no longer a problem.

Second, the computational cost of the forward (and inverse) EIT solver for resistive networks is significantly smaller than for continuum problems. In continuum problems, we use FEM techniques to approximately solve the governing equations. The accuracy of the solution depends on the number of nodes n used in the FEM approximation. For example, for a typical problem with 16 electrodes, corresponding to 120 degrees of freedom, we use 1700 nodes to obtain reasonable accuracy. In contrast,

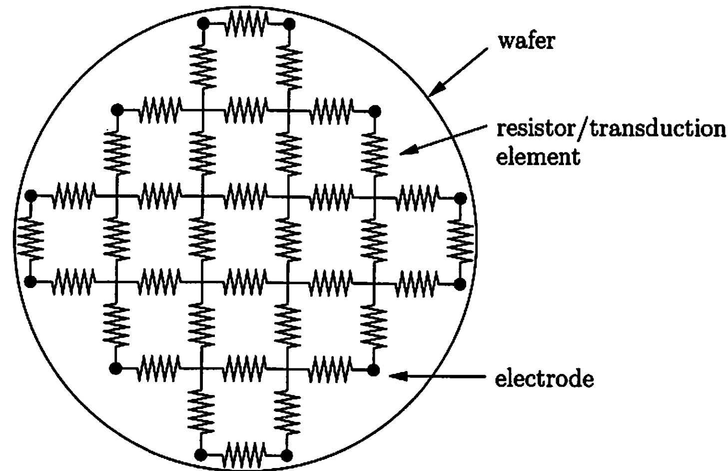

Figure 7.4: Generic resistive network on wafer.

a resistive network with 120 discrete elements can be interconnected using 16 external electrodes. The corresponding EIT solvers use only 16 "nodes" and yield comparable resolution. We note that the forward problem on n nodes has $O(n^3)$ complexity.

Finally, the topology of the resistive network and the individual conductance of each discrete component can be designed to enhance the overall sensitivity, even in the remote interior of the object.

7.4 Sensor design and operation

In this section we investigate the design and operation of our EIT sensor for measuring plasma induced potential at the wafer surface. Unlike the EIT based etch rate sensor of Chapter 6, this sensor relies on a network of discrete transduction elements.

7.4.1 Three stage approach

In Chapter 4 we described at length our three-stage approach for the design and operation of EIT based sensors. The first step in this approach is concerned with

exploiting a physical and/or chemical effect which can map the variable of interest to a change in conductivity in the interior of the wafer. While our earlier discussion dealt with applications of a conductive *continuum*, this approach can equally well be used in a discrete network. In this context, we will use a network of discrete transduction elements which map the variable of interest at the wafer surface into a change in conductivity within the resistive network.

In our case, we are interested in measuring the plasma induced potential at the wafer surface. This can be related to and is caused by the unwanted accumulated charge density on dielectric materials at the wafer surface during plasma processing. Hence, in our EIT sensor we need to employ a transduction element whose conductivity can be modulated by the application of an external electric field at the wafer surface. A suitable device for this purpose is the Field Effect Transistor (FET).

7.4.2 MOSFET operation

The Field Effect Transistors (FETs) was first developed in 1935. However, it took thirty more years for reliable and stable manufacturing processes to be developed to fabricate large numbers of MOSFETs in integrated circuits (ICs). Since then, MOSFETs have enabled the electronics revolution, vastly improving the reliability, functionality and speed of electronic devices. In this section we will briefly discuss the basic operation of a MOSFET, introducing only those characteristics which are relevant to our purpose. A much more comprehensive treatment of MOSFET devices can be found in [71, 96].

A MOSFET is a 4 terminal semiconductor device which can modulate the current flow between a pair of terminals by applying an electric field across the other pair. Built on a semiconductor substrate, MOSFETs exploit the characteristics of semiconductor materials to control the current flow in the device. Semiconductor materials exhibit the unique capability that their electrical conductivity can be varied over a wide range by introducing small amount of dopants. Certain dopants contribute ad-

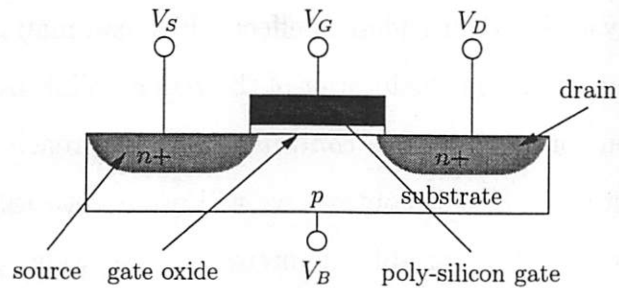

Figure 7.5: Schematic cross section of NMOSFET.

ditional electrons to the semiconductor material, creating a so-called n-type material, while other dopants contribute additional holes (lack of electron) to the semiconductor material, creating a so-called p-type material [71].

The schematic cross section of an N-type MOSFET is shown in Figure 7.5. This device consist of a p-type Si substrate (B), a polysilicon gate electrode (G) on top of a thin SiO_2 film and highly doped n-type source (S) and drain (D) regions. Under unbiased or reverse-biased conditions, the interface between any p-type and n-type silicon prevents any current from flowing across these junctions. Consequently, when the gate potential, V_G, is zero or negative, no current can flow between the source and drain regions, effectively creating an open circuit between S and D. Now consider the case where a positive potential is applied between the gate and substrate. The resulting electric field will drive the excess holes away from the surface between the p-type silicon and the gate oxide, creating a depletion region. Further increasing the gate potential will attract free electrons from the bulk substrate to the surface. At a sufficiently high potential the electron density will exceed the hole density near the surface (surface inversion), creating a highly conductive channel underneath the gate oxide between the source and drain regions. Now assume that a small potential is applied between the drain and source region ($V_{DS} > 0$). The resulting electric field between the source and drain region will allow current to flow through the conductive channel between the source and drain regions. The amount of current flowing between

the source and drain can modulated by the gate voltage.

The gate voltage for which inversion just occurs is often called the threshold voltage. For a standard NMOSFET device, the threshold voltage is around 0.5 volts. Thus a positive gate potential is required to create a conductive channel between the source and drain regions. Consequently, if we would employ NMOSFETs as transduction element in our potential sensor, we would only be able to measure potentials above the threshold voltage. Any voltage below the threshold voltage of the NMOSFET would turn the device off, preventing any current from flowing between the source and drain.

This problem could potentially be solved by using P-type MOSFETs in parallel with NMOSFETs. A P-type MOSFET is also a switch and its operation is similar to that of an NMOSFET. However PMOSFETs are fabricated onto an n-type substrate with p-type source and drain regions. In addition, currents between the source and drain regions in PMOSFETs are carried by holes instead of electrons. Finally, PMOSFETs are characterized by negative threshold voltages. Hence, in our potential sensor, PMOSFETs could be utilized as transduction elements to measure negative potentials. However, this means that we need two transduction elements at every site in order to measure potentials of both polarities, decreasing the spatial resolution of our resistive network approach. In addition, for small gate potentials (-0.5 volts $< V_G <$ 0.5 volts) both the NMOSFET and the PMOSFET are off, creating a dead-zone in which the potential sensor is unable to measure the gate potential.

A more elegant solution would be to use so-called depletion mode NMOSFETS.

7.4.3 Depletion-mode NMOSFET

Advancements in ion implantation techniques in the late 1960's resulted in tools which could perform shallow and low-dose ion implantations. This allowed semiconductor manufacturers to adjust the doping characteristics under the gate oxide by

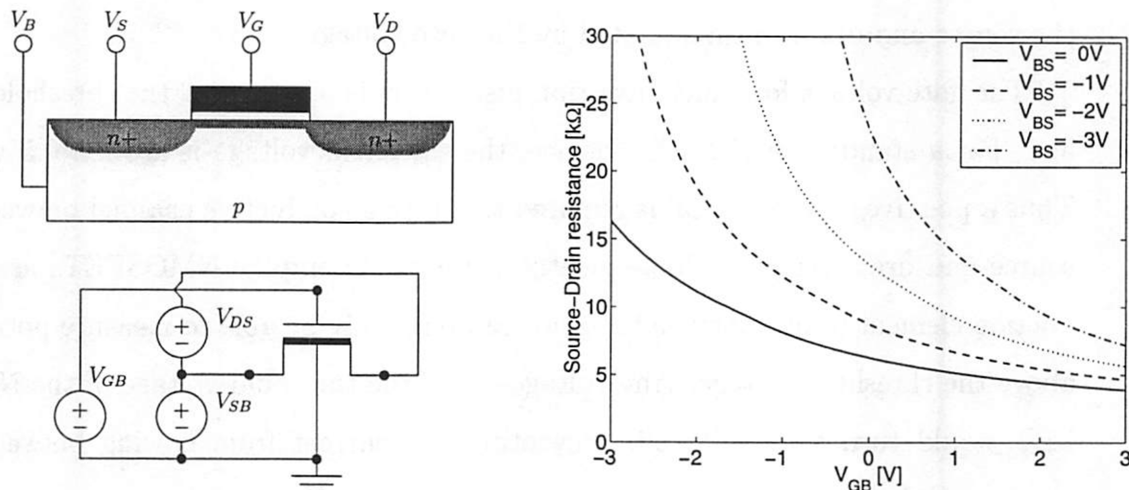

Figure 7.6: Schematic cross section of depletion NMOSFET (top left). Circuit diagram utilized in Hspice simulations (bottom left) to compute the resistance of the depletion mode NMOSFET for different values of V_{GB} and V_{BS}, $V_{DS} = 0.01$ volts (right).

implanting small amounts of dopants near the gate-oxide/substrate interface. In particular, a shallow implantation of n-type dopants in the p-type substrate can create a small conductive channel between the source and drain regions, causing a negative shift in the threshold voltage. The resulting depletion mode NMOSFET can conduct currents between the source and drain even for small negative gate potentials, making them attractive for use in a potential sensor. An extensive analysis of depletion mode NMOSFETs is beyond the scope of this thesis, and the interested reader is referred to [32, 98, 96] for more details.

In the remainder of this section we will briefly discuss two simulation examples to highlight the typical behavior of a depletion mode NMOSFET. The simulations were performed in Hspice, an analog circuit simulator from Avant! [3] which supports a variety of transistor models. In our study we utilized the level 5 MOS model as discussed in [4].

A schematic cross section of the depletion mode NMOSFET is shown in Figure 7.6. This picture clearly shows the conductive path under the gate oxide, created by a

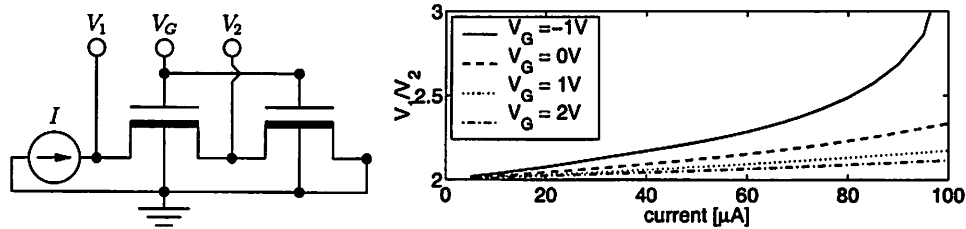

Figure 7.7: Simulations revealing nonlinear behavior of depletion-mode NMOSFETs

shallow implant of n-type donors into the p-type substrate. The circuit diagram, as simulated in Hspice, is also shown in this Figure. During the simulations, both V_{GB} and V_{BS} were varied and the corresponding source-drain currents for fixed V_{DS} were recorded. Figure 7.6 also shows a graph of the resulting resistance values for a typical depletion mode NMOSFET as a function of V_{GB} and V_{BS} (V_{DS} = 0.01 volts). As expected, this graph shows that the depletion mode NMOSFET remains on for small negative gate potentials. In addition, as the gate potentials become more negative, the resistance between the source and drain regions increases significantly. More interesting is the significant effect of V_{BS} on the source-drain resistance for fixed V_{GB}. A large reverse bias between the source region and the substrate increases the resistance of the depletion mode NMOSFET dramatically.

Another simulation example was performed with the circuit shown in Figure 7.7. This circuit contained two identical depletion NMOSFET devices, with identical gate bias V_{GB}, in series. The current forced through the series interconnection varied from 5 to 100 μA. If ideal identical resistors were used, instead of depletion mode NMOSFETs, the ratio V_1/V_2 would be constant at 2 and independent of the current forced through the series interconnection. However, the simulation results with the depletion mode devices, shown in Figure 7.7, clearly show that the ratio V_1/V_2 slowly increases from the nominal value of 2 with increasing currents through the circuit. In addition, the ratio is a strong, nonlinear function of V_{GB}.

From the previous simulation examples we can conclude that the resistance char-

acteristics of a depletion mode NMOSFET are highly nonlinear. In particular, the channel resistance is a strong function of the experimental conditions. Hence, the resistance of each depletion mode NMOSFET in a resistive network will severely depend on which electrodes/nodes are used to inject currents into the network. Consequently, we are faced with the odd situation that the resistance value of each depletion mode NMOSFET in our sensor is a nonlinear function of both the gate potential (the variable of interest) as well as the EIT experiment itself. This observation is critical and deserves emphasis: the class of EIT problems that arise in the context of our plasma potential sensor are unique and unusual in that EIT experiments themselves nonlinearly alter the internal conductivity of distributions. Our approach to this class of EIT problems is detailed in Section 7.5.2.

7.4.4 Wafer design and operation

During plasma processing charge accumulation at the wafer surface manifests itself as an electric field across dielectric materials, for example across the transistor gate oxide. Now consider the situation where the gate electrode of a depletion mode NMOSFET is exposed to the plasma. Charge accumulation at this gate electrode will result in an electric field across the gate oxide between the gate and base electrode. This, in turn, modulates the channel conductivity between the source and drain terminals of the depletion mode NMOSFET. Consequently, by fabricating a depletion mode NMOSFET onto a wafer and monitoring its conductivity in-situ we can infer the induced potential at the wafer surface during plasma processing.

In order to obtain spatially resolved wafer potential information, we need to employ an array of depletion mode NMOSFETs. However, unlike traditional sensor wafer approaches in which each transduction element is individually powered and measured, we propose to connect all the individual depletion mode NMOSFETs into a single resistive network. This allows us to perform simple EIT experiments to measure the conductivity of the individual depletion mode NMOSFETs. From this

information we can then infer the gate potential at each individual transduction element.

The proposed wafer potential sensor has the following key properties. First, standard IC manufacturing techniques can be used to fabricate the array of individual depletion mode NMOSFETs at the wafer surface, reducing the risk of tool contamination by the proposed sensor wafer. Second, the topology and interconnections can be chosen to enhance the sensitivity of the wafer in particular areas. For example, we can place more transduction elements near the periphery of the wafer in order to assess edge effects during plasma processing. In addition, unlike traditional EIT applications, we can design the interconnection between the individual transduction elements and the nominal conductivity of each transduction element such that the sensitivity of the sensor in the remote interior of the wafer is enhanced.

We did not, in the context of this dissertation, fabricate our proposed EIT based plasma potential sensors. This effort would take us too far afield into expensive and time-consuming fabrication, modeling and testing complexities and divert our focus from the operation principle of EIT for these sensors. Indeed, the tomography aspect of our sensors is the principal subject of this dissertation. We therefore have chosen to focus on simulation studies to evaluate the feasibility of our ideas.

7.5 Simulation results

In this section we will demonstrate the feasibility of a plasma potential sensor based on a network of depletion mode NMOSFETs. Our feasibility study is limited to performing several simulation studies with simple networks for the reasons detailed above in Section 7.4.4.

7.5.1 Experimental details

All simulations were performed in Hspice [4]. This simulation environment contains an extensive library of device models to describe the behavior of complex devices, such as transistors, over a wide range of operating conditions. Each model contains many variables which can be chosen by the circuit designer to tune the behavior of the model to fit real experimental results. A properly tuned model will yield reliable predictions of the overall circuit when implemented. Consequently, Hspice can provide a cost-effective, reliable and fast tool to simulate and test a variety of electrical circuits for virtual prototyping

To test the feasibility of a plasma potential sensor based on a network of depletion mode NMOSFETs, we have implemented two different networks in Hspice with 6 and 10 depletion mode NMOSFETs. The network contained four or five "electrodes", i.e. nodes through which currents can be injected into the network. This network was then used to create *simulated* measurement data, which will be used to estimate the gate potential of each depletion mode NMOSFET in the network.

In order to create the simulated measurement data, each gate was assigned a potential between -2.5 and 2.5 `volts`. The network was then excited by different current patterns between pairs of electrodes. Note that the network of transistors does not exhibit the symmetric and linear behavior associated with networks containing linear resistive elements. For example, $V_{AB|CD}$ (the potential between points A and B due to a current between points C and D) is not necessarily the same as $V_{CD|AB}$. In addition, doubling the current injected into the network does not necessarily double the associated potentials and reversing the direction of the current does not simply reverse the polarity of the observed potentials, i.e. $V_{AB|CD} \neq -V_{AB|DC}$.

A traditional EIT experiment with L electrodes would yield at most $L(L-1)/2$ degrees of freedom. However, due to the nonlinear behavior of a network of transistors each new current pattern in an EIT experiment provides an additional degree of freedom. In our simulation example, the network was excited by fixed amplitude

($I_{AB} = 100\mu$A) current patterns between adjacent electrode pairs.

7.5.2 Algorithm details

An iterative algorithm was developed to solve the inverse EIT problem for the network of transistors using techniques similar to those used in the traditional problem (see Chapter 3). The algorithm consisted of several software modules written in various software languages (see Appendix C for the code of each module for a network of 6 depletion mode NMOSFETs).

The `runtotal` module (written in Perl) is the core of the EIT algorithm. It starts with an initialization routine and is followed by a forward simulation of the the transistor network of interest to create the simulated electrode data. To this end, we implement the transistor network in Hspice, excite it by small current patterns between pairs of electrodes and store the resulting electrode potentials. Finally we use an iterative routine to update the estimate of the gate potential for each transistor.

In each iteration, we first solve the forward problem in Hspice for the most recent estimate of the gate potentials. We perturb each gate potential by a small amount, allowing us to compute the Jacobian matrix. This is used to assess the sensitivity of the electrode potentials with respect to small variations in the gate potentials. The electrode potentials for the most recent gate potentials are then compared with the "true" electrode potentials. The error between the electrode potentials and the Jacobian matrix are then used to update the estimate of the gate potentials.

To test the robustness of our sensor, we also performed several simulations studies with small amounts of white noise added to the original simulation data.

7.5.3 Simulation 1

In this simulation we consider a simple network of 6 depletion mode NMOSFETs, shown in Figure 7.8. We injected four different current patterns into the network

	original	no noise	0.5% noise	1% noise	2% noise
$V_{g,1}$	-1.500	-1.499	-1.511±0.045	-1.503±0.091	-1.465±0.222
$V_{g,2}$	1.500	1.499	1.451±0.088	1.431±0.159	1.460±0.344
$V_{g,3}$	-2.500	-2.499	-2.468±0.062	-2.462±0.122	-2.481±0.299
$V_{g,4}$	-0.500	-0.500	-0.477±0.051	-0.502±0.122	-0.488±0.258
$V_{g,5}$	0.500	0.498	0.500±0.048	0.501±0.145	0.430±0.284
$V_{g,6}$	2.500	2.501	2.478±0.059	2.479±0.181	2.516±0.389

Table 7.1: Estimated gate potentials in `volts` for the various simulations performed on the resistive network containing 6 depletion mode NMOSFETs.

through pairs of electrodes. The resulting simulated electrode potentials were then used in the inverse problem to estimate the gate potentials for each depletion mode NMOSFET. The backward iterative EIT solver was initialized with the initial guess of 0 `volt` for each gate potential. We performed 15 iterations and recorded the estimated gate potentials for each iteration. The gate potentials versus iteration number, as estimated by the algorithm, are also shown in Figure 7.8. This graph clearly shows that the estimated gate potentials converge within 10 iterations to the "true" gate potentials.

In order to assess the robustness of this example, we corrupted the simulation data with a small amount of random white noise. The variance of the noise was 0.5%, 1%, and 2% of the maximum potential data in the forward problem. For each noise level we performed 25 inverse EIT problems (each with 15 iterations) and the resulting estimates for the gate potentials were recorded. In Table 7.1 the mean and the standard deviation for each of these gate potentials are shown. In this table we also included the true gate potentials and the estimated gate potential for the nominal case without noise. This table clearly demonstrates the feasibility of our EIT approach to estimate the gate potentials of depletion mode NMOSFETs in a resistive network. As expected, the variance of the estimated gate potentials increases with increasing additive noise levels on the simulation data. However, this has only limited influence on the estimated gate potentials (see also Figure 7.8).

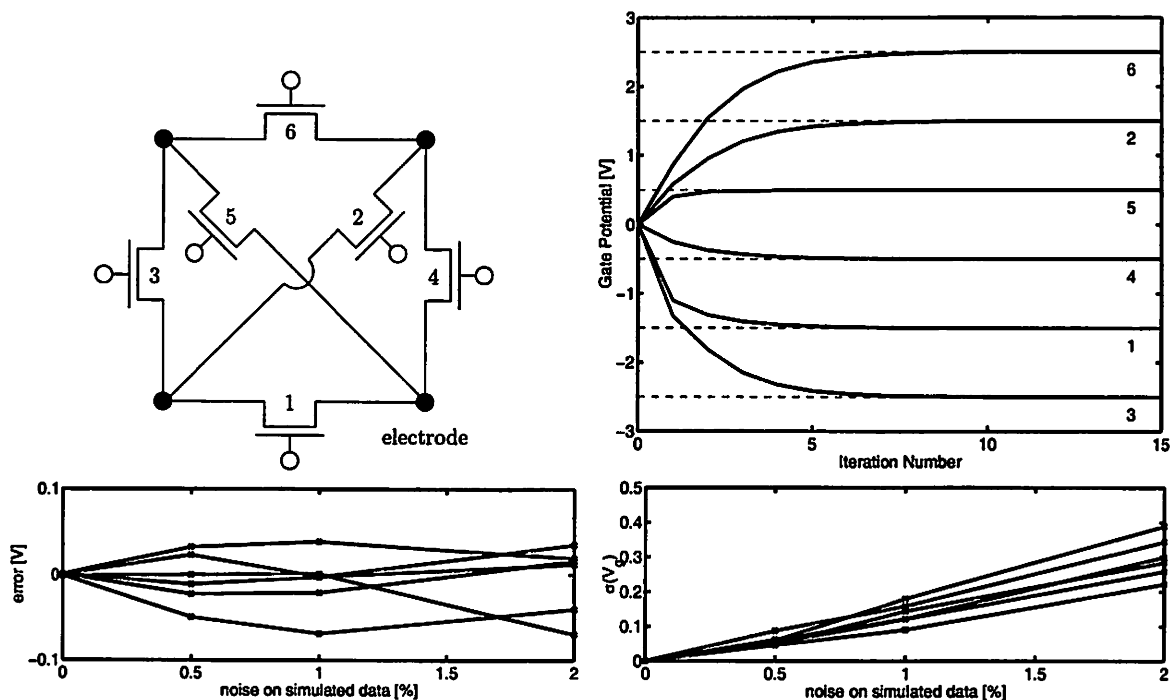

Figure 7.8: Simulation results with the resistive network of 6 depletion mode NMOSFETs shown in the top left panel. The top right panel shows the estimated gate potential after each iteration in the nominal case, i.e. without noise. The bottom left panel shows the error between the mean gate potential and the "true" gate potential for different noise levels. The bottom right panel shows the standard deviation of the estimated gate potentials versus the noise level.

7.5.4 Simulation 2

In this section we examine a second example of a resistive network containing 10 depletion mode NMOSFETs (see Figure 7.9). In this simulation, we used five electrodes to inject five different current patterns between pairs of electrodes. The true gate potentials of each depletion mode NMOSFET were chosen between -2.5 and 2.5 `volts`. Similar to the previous simulation (see Section 7.5.3), we first performed the inverse EIT problem on nominal simulated electrode data. The estimated gate potentials versus iteration number are also shown in Figure 7.9. This graph shows that the inverse EIT algorithm is once again capable of estimating the "true" gate potentials.

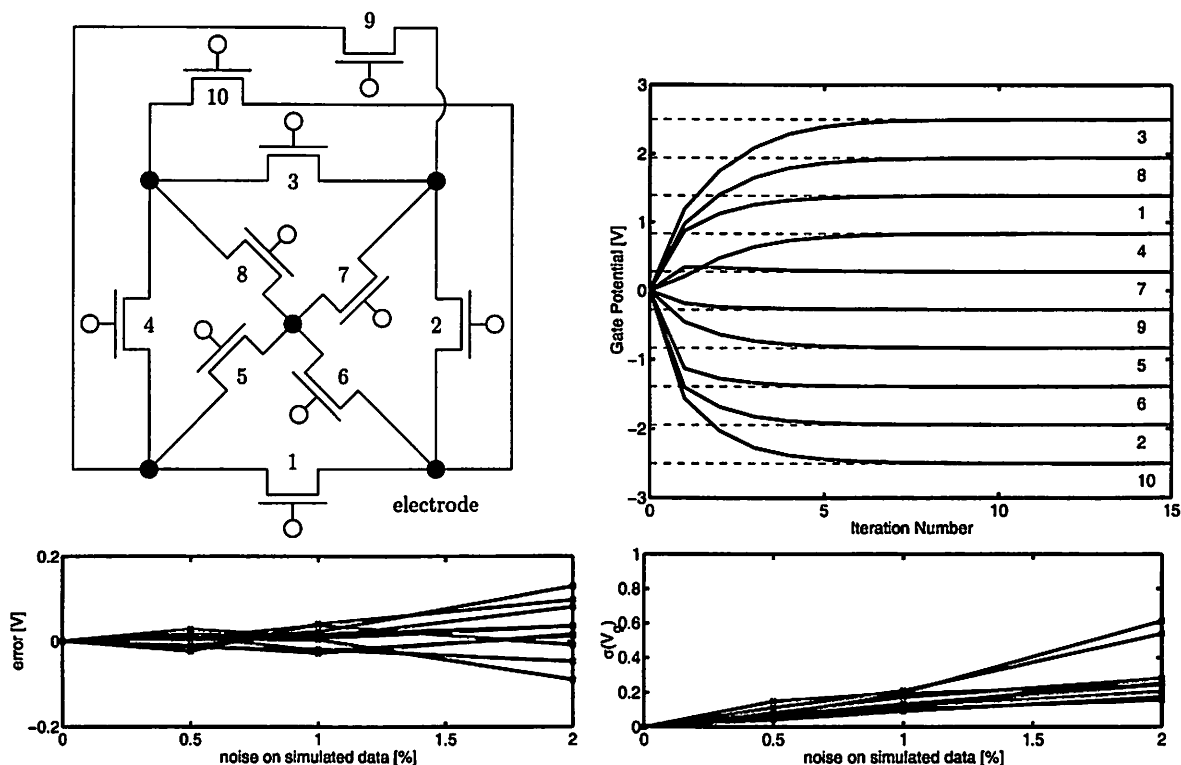

Figure 7.9: Simulation results with the resistive network of 10 depletion mode NMOSFETs shown in the top left panel. The top right panel shows the estimated gate potential after each iteration in the nominal case, i.e. without noise. The bottom left panel shows the error between the mean gate potential and the "true" gate potential for different noise levels. The bottom right panel shows the standard deviation of the estimated gate potentials versus the noise level.

In this simulation example we also added small amounts of white noise to the simulated electrode data to test the robustness of our example to small perturbations. The resulting mean gate potentials, including their standard deviations, are shown in Table 7.2 and Figure 7.9. These results confirm the robustness of this simulation example to small perturbations. However, it is evident from this table and figure that the error and the variance of the estimated gate potentials are increasing functions of the complexity of the resistive network.

	original	no noise	0.5% noise	1% noise	2% noise
$V_{g,1}$	1.389	1.388	1.379±0.076	1.361±0.120	1.405±0.284
$V_{g,2}$	-1.944	-1.943	-1.959±0.070	-1.963±0.132	-1.991±0.255
$V_{g,3}$	2.500	2.499	2.507±0.149	2.538±0.199	2.492±0.613
$V_{g,4}$	0.833	0.835	0.810±0.113	0.874±0.210	0.931±0.539
$V_{g,5}$	-0.833	-0.833	-0.829±0.048	-0.829±0.105	-0.923±0.156
$V_{g,6}$	-1.389	-1.389	-1.399±0.043	-1.372±0.092	-1.353±0.175
$V_{g,7}$	0.278	0.278	0.290±0.061	0.255±0.121	0.291±0.206
$V_{g,8}$	1.944	1.945	1.963±0.072	1.952±0.126	1.981±0.248
$V_{g,9}$	-0.278	-0.277	-0.273±0.071	-0.255±0.193	-0.148±0.243
$V_{g,10}$	-2.500	-2.500	-2.472±0.082	-2.490±0.172	-2.419±0.281

Table 7.2: Estimated gate potentials in `volts` for the various simulations performed on the resistive network containing 10 depletion mode NMOSFETs.

7.6 Conclusions

The simulation studies in the previous sections show the feasibility of our approach in which we apply standard EIT techniques to a resistive network of discrete transduction elements. The simulation results are very encouraging and we are confident that EIT based sensor wafers which use a resistive network of transduction elements, can provide the desired spatial resolution across the wafer without the challenges associated with EIT based sensors which rely on a conductive continuum.

Unlike traditional EIT applications, our network of depletion mode transistors is very nonlinear, i.e. the EIT experiments themselves alter the conductivity of each transistor, making the EIT problem significantly more complex and challenging. Nevertheless, our algorithm is very well capable of estimating the correct gate potentials, even in the case where a small amount of random white noise is added to the simulated electrode potentials.

Our algorithm relies on Hspice simulations to solve the forward problem and to obtain the Jacobian for use in the inverse EIT problem. These simulations are rather slow due to the nonlinear behavior of the resistive network. Consequently, solving the inverse EIT problem can be very time consuming, making the proposed plasma

potential sensor not suitable for real-time sensor applications. Instead, experimental EIT data from the proposed plasma potential sensor will need to be stored for off-line analysis.

We believe that a properly designed resistive network can reduce the unfavorable sensitivity in the remote interior of the wafer often seen in the continuum approach. Our conjecture is that optimal sensitivity can be achieved by minimizing the number of nodes in the resistive network. In particular, we think that each discrete element should be placed such that it directly interconnects a pair of electrodes. In the previous simulation studies we illustrated this approach for resistive networks with four and five electrodes respectively. In both studies we placed each depletion mode NMOSFET in the resistive network such that it creates a direct interconnection between a pair of electrodes. We note that this approach only constrains the manner in which each depletion mode NMOSFET is interconnected. The physical placement of each depletion mode NMOSFET is unaffected and can be arbitrarily chosen across the wafer to suit the needs of the enduser.

Chapter 8

Conclusions

8.1 Dissertation summary

There is widespread consensus that metrology will be an enabling technology if the semiconductor manufacturing industry is to continue the pace at which it has increased productivity over the last three decades. Where possible, off-line metrology will be replaced with in-line and in-situ metrology, allowing semiconductor manufacturers to improve process uniformity and to reduce the risk and associated cost of lost product. We believe that semiconductor manufacturers will augment their metrology toolset in the near future with novel metrology technologies such as autonomous sensor wafers which can provide unprecedented real-time spatially resolved wafer state information. Advanced and ubiquitous metrology offers an insurance policy against yield loss and enables very tight process control.

In this dissertation, we have explored a *class* of sensors to measure wafer state information during wafer processing. These sensors exploit the spatial imaging capabilities of Electrical Impedance Tomography (EIT), a non-destructive *in vivo* imaging technique principally used in biomedical applications. In our application, we place electrodes at the periphery of a wafer. Various current patterns are then injected into the wafer and the resulting potentials at all electrodes are recorded. From these

electrical measurements we can infer the conductivity distribution inside the wafer, which, in turn, can be related to the variable of interest through simple physical or chemical models. To illustrate this idea, we discussed the design, fabrication and operation of one such sensor to measure the thickness of a conductive polysilicon film across a wafer. The measurement data from this prototype etch rate sensor corresponds well with optical film thickness measurements.

Traditional EIT techniques have several drawbacks: they require an accurate electrical model of the object being imaged, making the EIT technique computationally expensive, and they exhibit nonuniform sensitivity across the object to conductivity changes, i.e. conductivity changes in the remote interior are hard to detect. However, unlike traditional EIT applications, in our sensor wafer context we have the luxury of designing the interior of the object being imaged, allowing us to alleviate some of these problems. In this dissertation we have explored the feasibility of applying EIT techniques to a resistive network containing discrete transduction elements whose conductivity is modulated by the variable of interest. To illustrate this approach we performed simulation studies on a prototype sensor which can measure the potential induced by a plasma at the wafer surface. Depletion mode NMOSFETs were used as transduction elements. We obtained promising simulation results with this novel EIT based metrology technique.

8.2 Future research

In this dissertation we investigated the feasibility of EIT based sensor wafers. We discussed at-length two prototype sensor wafers which can provide spatially resolved wafer state information during semiconductor manufacturing. However, much work still needs to be done before these EIT based sensors can be deployed in high volume semiconductor manufacturing facilities. In particular, the following topics need extended study:

- *Integration of power and communication*

  The goal in this thesis was to assess the feasibility of an EIT based sensor component for use on autonomous sensor wafers. However, an autonomous sensor wafer contains many other components which are equally important. For example, on-board power is necessary to allow untethered operation. In addition, the sensor data has to be either stored on the wafer or wirelessly transmitted to a receiver. All these components must operate reliably and repeatably over extended periods of time while being exposed to harsh process environments. Form factors are another major challenge. The autonomous sensor wafer has to resemble a regular product wafer as closely as possible (both in dimensions as well as weight) to avoid interference with the wafer handling equipment and production tools.

- *Closing the control loop*

  Autonomous sensor wafers can provide a wealth of wafer-state information during semiconductor manufacturing. However, there is currently no appropriate infrastructure in place to use all this data to improve the production process. For example, most semiconductor manufacturers rely on Statistical Process Control (SPC) and Run-to-Run (RtR) control techniques to maintain a certain parameter, such as the average film thickness across the wafer, within the desired specifications. Real-time process control and active across-wafer CD uniformity control are still in their relative infancy. These advanced control problems demand the availability of suitable sensor technologies and appropriate process models which can accurately predict the wafer state based on the tool and process states.

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Appendix A

Galerkin Method for a Single Triangular Element

In this Appendix we show how the Galerkin method [2, 14] can be used on a single triangular element to solve

$$\nabla \circ [\sigma(\mathbf{r})\nabla u] = 0 \text{ for } \mathbf{r} \in \Omega$$

in the interior of the element given appropriate boundary conditions. Consider a single triangular element with uniform conductivity σ as shown in Figure A.1. The continuous potential distribution inside this element is approximated by a simple linear interpolation function $V(x, y) = \alpha_1 + \alpha_2 x + \alpha_3 y$. This interpolation $V(x, y)$ must, of course, satisfy the potentials at the vertices, i.e

$$\begin{bmatrix} V(x_1, y_1) \\ V(x_2, y_2) \\ V(x_3, y_3) \end{bmatrix} = \begin{bmatrix} 1 & x_1 & y_1 \\ 1 & x_2 & y_2 \\ 1 & x_3 & y_3 \end{bmatrix} \begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \alpha_3 \end{bmatrix} = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}.$$

The solution to this set of equations is

$$\begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \alpha_3 \end{bmatrix} = \frac{1}{2A} \begin{bmatrix} x_2y_3 - x_3y_2 & x_3y_1 - x_1y_3 & x_1y_2 - x_2y_1 \\ y_2 - y_3 & y_3 - y_1 & y_1 - y_2 \\ x_3 - x_2 & x_1 - x_3 & x_2 - x_1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

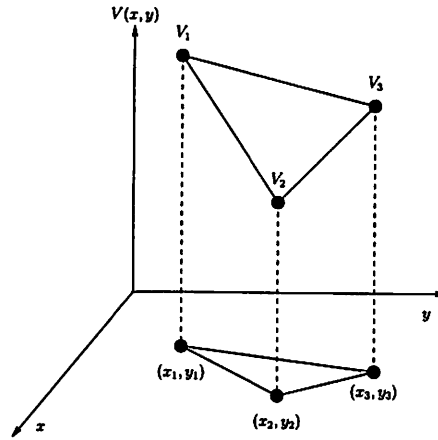

Figure A.1: Linear interpolation function used in single finite element.

$$= \frac{1}{2A}\begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ c_1 & c_2 & c_3 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

where the area A of the triangle is given by

$$A = \frac{1}{2}\det\begin{bmatrix} 1 & x_1 & y_1 \\ 1 & x_2 & y_2 \\ 1 & x_3 & y_3 \end{bmatrix}.$$

The linear interpolation function $V(x, y)$ for the triangular element can then be written as

$$V(x,y) = [\ \chi_1 \quad \chi_2 \quad \chi_3\ ]\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

with $\chi_i, i = 1, 2, 3$ the characteristic functions which only depend on the geometry of the triangular element:

$$\begin{aligned} \chi_1 &= \frac{1}{2A}(a_1 + b_1 x + c_1 y) \\ \chi_2 &= \frac{1}{2A}(a_2 + b_2 x + c_2 y) \\ \chi_3 &= \frac{1}{2A}(a_3 + b_3 x + c_3 y). \end{aligned}$$

The partial derivatives of $V(x,y)$ with respect to x and y are

$$\begin{bmatrix} \frac{\partial V}{\partial x} \\ \frac{\partial V}{\partial y} \end{bmatrix} = \begin{bmatrix} \frac{\partial \chi_1}{\partial x} & \frac{\partial \chi_2}{\partial x} & \frac{\partial \chi_3}{\partial x} \\ \frac{\partial \chi_1}{\partial y} & \frac{\partial \chi_2}{\partial y} & \frac{\partial \chi_3}{\partial y} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

$$= \frac{1}{2A} \begin{bmatrix} b_1 & b_2 & b_3 \\ c_1 & c_2 & c_3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}.$$

As discussed in Section 3.3.2, the partial differential equation on this single triangular element, including the boundary conditions, can be transformed using

$$\left(\int_\Omega \nabla \chi_i \circ \left[\sigma \nabla \boldsymbol{\chi}^T\right] d\Omega\right) \mathbf{u} = f_i$$

into the following system of three equations with three unknown node potentials

$$\int_\Omega \sigma \left(\begin{bmatrix} \frac{\partial \chi_1}{\partial x} \\ \frac{\partial \chi_2}{\partial x} \\ \frac{\partial \chi_3}{\partial x} \end{bmatrix} \begin{bmatrix} \frac{\partial \chi_1}{\partial x} & \frac{\partial \chi_2}{\partial x} & \frac{\partial \chi_3}{\partial x} \end{bmatrix} + \begin{bmatrix} \frac{\partial \chi_1}{\partial y} \\ \frac{\partial \chi_2}{\partial y} \\ \frac{\partial \chi_3}{\partial y} \end{bmatrix} \begin{bmatrix} \frac{\partial \chi_1}{\partial y} & \frac{\partial \chi_2}{\partial y} & \frac{\partial \chi_3}{\partial y} \end{bmatrix} \right) \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} d\Omega =$$

$$\int_\Omega \frac{\sigma}{4A^2} \begin{bmatrix} b_1^2 + c_1^2 & b_1 b_2 + c_1 c_2 & b_1 b_3 + c_1 c_3 \\ * & b_2^2 + c_2^2 & b_2 b_3 + c_2 c_3 \\ * & * & b_3^2 + c_3^2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} d\Omega = \int_{\partial\Omega} \sigma \begin{bmatrix} \left(\frac{\partial V}{\partial n}\right) \chi_1 \\ \left(\frac{\partial V}{\partial n}\right) \chi_2 \\ \left(\frac{\partial V}{\partial n}\right) \chi_3 \end{bmatrix} ds.$$

For a triangular element the integral $\int_\Omega d\Omega = A$. Hence, simplifying the previous equation yields

$$\frac{\sigma}{4A} \begin{bmatrix} b_1^2 + c_1^2 & b_1 b_2 + c_1 c_2 & b_1 b_3 + c_1 c_3 \\ * & b_2^2 + c_2^2 & b_2 b_3 + c_2 c_3 \\ * & * & b_3^2 + c_3^2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \int_{\partial\Omega} \sigma \begin{bmatrix} \left(\frac{\partial V}{\partial n}\right) \chi_1 \\ \left(\frac{\partial V}{\partial n}\right) \chi_2 \\ \left(\frac{\partial V}{\partial n}\right) \chi_3 \end{bmatrix} ds.$$

We will assume that currents enter/leave the triangular element only through the nodes, i.e.

$$\sigma(\nabla V \circ \hat{\mathbf{n}}) = I_1 \delta(\mathbf{r} - \mathbf{r}_1) + I_2 \delta(\mathbf{r} - \mathbf{r}_2) + I_3 \delta(\mathbf{r} - \mathbf{r}_3)$$

with $\mathbf{r}_i, i = 1,2,3$ the location of the vertices and $I_i, i = 1,2,3$ the total current entering/leaving the element through vertex i. Note that $\int_{\partial\Omega} \sigma \left(\frac{\partial V}{\partial n}\right) \chi_i ds = I_i$. Hence, we finally obtain the following set of equations

$$\frac{\sigma}{4A}\begin{bmatrix} b_1^2+c_1^2 & b_1b_2+c_1c_2 & b_1b_3+c_1c_3 \\ * & b_2^2+c_2^2 & b_2b_3+c_2c_3 \\ * & * & b_3^2+c_3^2 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix}. \qquad \text{(A.1)}$$

Appendix B

Extrapolation and Interpolation Using Kriging

Ordinary or punctual kriging is a linear estimation procedure concerned with optimally predicting the value y_0 at an unobserved location within a domain given spatial measurement data at selected locations within that domain [51, 21, 105, 45], see Figure B.1. We seek to obtain an unbiased minimum variance estimate of y_0. For simiplicity we will restrict ourselves to linear estimatiors of the form

$$\hat{y}_0 = \sum_{i=1}^{N} w_i y_i = \mathbf{w}^* \mathbf{y}$$

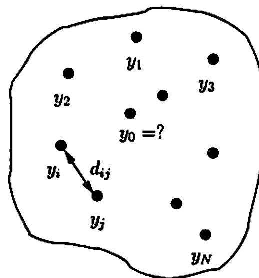

Figure B.1: Kriging is concerned with predicting the optimal value for y_0 at an unobserved location, given measurements $y_i, i = 1, \ldots, N$ at selected locations.

where $\hat{y}_0$ is the optimal predictor, y_i is the observed value at location i, w_i is an appropriate weight and N is the number of spatial measurements. In the remainder we will assume that $\mathbf{E}[y_i] = m$, $i = 1, \ldots, N$, where m is not known *a-priori*. In addition, let

$$\mathbf{E}\left[\begin{pmatrix} y_0 - m \\ \vdots \\ y_N - m \end{pmatrix}\begin{pmatrix} y_0 - m \\ \vdots \\ y_N - m \end{pmatrix}^*\right] = \left[\begin{array}{c|c} p & \mathbf{r}^* \\ \hline \mathbf{r} & \mathbf{Q} \end{array}\right] \tag{B.1}$$

with $p \in \mathbb{R}$, $\mathbf{r} \in \mathbb{R}^{N\times 1}$ and $\mathbf{Q} \in \mathbb{R}^{N\times N}$.

We require the predictor $\hat{y}_0$ be unbiased, i.e. $\mathbf{E}[\hat{y}_0] = \mathbf{E}[y_0] = m$. This condition translates into the following requirement on the weights w_i, $i = 1, \ldots, N$ [51, 21, 105, 45]:

$$\sum_{i=1}^{N} w_i = \mathbf{e}^*\mathbf{w} = 1 \tag{B.2}$$

with $\mathbf{e} = \begin{bmatrix} 1 & \ldots & 1 \end{bmatrix}^T \in \mathbb{R}^{N\times 1}$. The weight vector $\mathbf{w} \in \mathbb{R}^{N\times 1}$ is chosen to minimize the variance of the predictor, i.e.

$$\begin{aligned} \min_{\mathbf{w}} \sigma_E^2 &= \min_{\mathbf{w}} \mathbf{E}\left[(y_0 - \hat{y}_0)^2\right] \\ &= \min_{\mathbf{w}} \mathbf{E}\left[\left(y_0 - m - \sum_{i=1}^{N} w_i(y_i - m)\right)\left(y_0 - m - \sum_{i=1}^{N} w_i(y_i - m)\right)^*\right] \\ &= \min_{\mathbf{w}} p + \mathbf{w}^*\mathbf{Q}\mathbf{w} - 2\mathbf{w}^*\mathbf{r} \end{aligned}$$

subject to the constraint in Equation (B.2). To find the optimal weight $\mathbf{w}$, we use Lagrange multipliers to solve this constrained optimization problem. Define the cost function

$$J(\mathbf{w}) = p + \mathbf{w}^*\mathbf{Q}\mathbf{w} - 2\mathbf{w}^*\mathbf{r} + 2\lambda(\mathbf{e}^*\mathbf{w} - 1).$$

Taking the derivative of this cost function with respect to $\mathbf{w}$ and λ yields

$$\begin{bmatrix} \mathbf{Q} & \mathbf{e} \\ \mathbf{e}^* & 0 \end{bmatrix}\begin{bmatrix} \mathbf{w} \\ \lambda \end{bmatrix} = \begin{bmatrix} \mathbf{r} \\ 1 \end{bmatrix}. \tag{B.3}$$

The optimal weight vector $\mathbf{w}_{opt}$ is then given by

$$\mathbf{w}_{opt} = \mathbf{Q}^{-1}(\mathbf{r} - \lambda \mathbf{e}). \tag{B.4}$$

The multiplier λ can be obtained from Equation (B.3) as

$$\mathbf{e}^*\mathbf{w}_{opt} = 1 \quad \Rightarrow \quad \lambda = \frac{\mathbf{e}^*\mathbf{Q}^{-1}\mathbf{r} - 1}{\mathbf{e}^*\mathbf{Q}^{-1}\mathbf{e}}.$$

Substituting this expression into Equation (B.4) finally results in the following expression for the optimal weight vector [51, 21, 105, 45]:

$$\mathbf{w}_{opt} = \mathbf{Q}^{-1}\mathbf{r} - \mathbf{Q}^{-1}\mathbf{e}\frac{\mathbf{e}^*\mathbf{Q}^{-1}\mathbf{r} - 1}{\mathbf{e}^*\mathbf{Q}^{-1}\mathbf{e}}.$$

Let d_{ij} denote the distance between the points $i, j = 0, \ldots, N$. The covariance elements $\mathbf{E}\left[(y_i - m)(y_j - m)^*\right]$ in Equation (B.1) are often not exactly known. However, in many applications it is reasonable to assume that they are a function *only* of the distance between the two points i and j,

$$\mathbf{E}\left[(y_i - m)(y_j - m)^*\right] \approx f(d_{ij}).$$

The function f is known as the kriging kernel. Common choices for the kriging kernel are

$$f(d) = \exp\left(-\frac{d}{D}\right) \text{ or } f(d) = \exp\left(-\frac{d^2}{D^2}\right)$$

where the *mixing length* D defines the domain over which the measurements are significantly correlated.

Appendix C

Code used in Hspice EIT Algorithm

C.1 runtotal: main program to perform EIT estimation (Perl)

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
runtotal
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
#! /usr/sww/bin/perl
######################
# (1) Initialization #
######################
# create constants used in simulation
$Niter = 15;                  # iterations
$Nnode = 4;                  # nodes
$Nnmos = 6;                 # transistors
$Ncurrent = $Nnode*($Nnode-1); # current patterns
$guess = 0;                  # intial guess for V_G

# save constants to file
print `rm info.txt`;
open(FILE,">info.txt")
  || die "cannot open file";
print FILE "$Niter\n";
print FILE "$Nnode\n";
print FILE "$Nnmos\n";
close(FILE);
```

```
# remove previous results and vgate files
print `rm results*.out`;
print `rm vgate[0-9]*.sp`;

# copy vgate_org.sp to vgate.sp
print `cp vgate_org.sp vgate.sp`;

# create dcpert.sp
$text = ".print ";
for ($index = 1; $index <= $Nnode; $index++){
$text = $text . "v(n$index,gnd) ";
}
open(FILE,">dcpert.sp")
  || die "cannot open file";
print FILE "$text\n";
close(FILE);

###########################################
# (2) Compute artificial measurement data #
###########################################
print `./runspicetotal $Nnode main.sp 0`;

###########################
# (3) Update Hspice files #
###########################
# create intial estimate for vgate.sp
open(FILE,">vgate.sp")
  || die "cannot open file";
for ($index = 1; $index <= $Nnmos; $index++){
print FILE ".param gate$index=$guess\n";
}
close(FILE);
print `cp vgate.sp vgate0.sp`;

# update create dcpert.sp file
open(FILE,">dcpert.sp")
  || die "cannot open file";
print FILE "$text\n";
for ($index = 1; $index <= $Nnmos; $index++){
print FILE ".dc vg$index start = 'gate$index-0.1'
stop = 'gate$index+0.1' step = 0.2\n";
print FILE "$text\n";
```

```
}
close(FILE);

#########################
# (4) Start iterations #
#########################
print("Start iterations \n");
for ($index=1; $index <= $Niter; $index++){ # loop 1

  # step 1: do a spice run first to obtain partial derivatives
  print `./runspicetotal $Nnode main.sp $index`;

  # step 2: make copy of results.out for matlab calculation
  print `cp results$index.out resultstemp.out `;

  # step 3: run matlab and compute update for gate potentials
  print `./matbg runmatlab.m matlab.out`;

  # step 4: wait till matlab has written data to files before
  # continuing
  while (!(-e "flag.mat")){
  }
  while(-s "flag.mat"<150){
  }
  print `rm matlab.out`;
  print `rm flag.mat`;
  print `cp vgate.sp vgate$index.sp `;

}                                          # end loop 1

##################################
# (5) Remove intermediate files #
##################################
print `rm vgate.sp`;
print `rm dcpert.sp`;
print `rm source.sp`;
```

C.2 runspicetotal: update and run spice simulation (Perl)

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
runspicetotal
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
#! /usr/sww/bin/perl

# argument 0: number of nodes
# argument 1: spice file to run
# argument 2: index number given to results file

# number of nodes at periphery
$Nnode = $ARGV[0];

for ($index1 = 1; $index1 <= $Nnode; $index1++){    # loop 1

  for ($index2 = 1; $index2 <= $Nnode; $index2++){  # loop 2

    if ($index1 != $index2){                        # start if-loop

  # first create new source.sp file
      open(FILE,">source.sp")                       # open source.sp
        || die "cannot open input file";
      print FILE "I1 n$index2 n$index1 dc 1e-4\n";  # define current source
      print FILE "v1 n$index2 gnd      dc 0 \n";    # define gnd
      close(FILE);                                  # close file

      # second, run hspice simulation and extract data
      print `hspice $ARGV[1] |
          grep "[[:digit:]][[:digit:]]e-[[:digit:]]" >> results$ARGV[2].out`;


    }                                               # end if-loop

  }                                                 # end loop 2

} # end loop 1

# remove intermediate spice files
print `rm *.st0`;
```

C.3 matbg: run Matlab in background (Shell script)

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
matbg
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
#!/bin/tcsh -f
# For running matlab in the background
unsetenv DISPLAY
nohup matlab -nojvm  < $1 > $2 &
```

C.4 runmatlab.m: update gate potentials after each iteration (Matlab)

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
runmatlab.m
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% initialize
load info.txt
Nnode = info(2);
Nmos = info(3);
Ncurrent = Nnode*(Nnode-1);

% load measurements
load results0.out
meas = results0(:,2:Nnode+1);
for i = 1:Ncurrent
  Vmeas((i-1)*Nnode+1:i*Nnode,1) = meas(i,:)';
end

% load simulation results
data = load('resultstemp.out');
N = size(data,1);

% create Vest vector
temp = data(1:2*Nmos+1:N,2:Nnode+1);
for i = 1:Ncurrent
  Vest((i-1)*Nnode+1:i*Nnode,1) = temp(i,:)';
end
clear temp

% create gradient matrix
for i = 1:Ncurrent
  temp((i-1)*2*Nmos+1:i*2*Nmos,:) = data((i-1)*(2*Nmos+1)+2:i*(2*Nmos+1),:);
end
```

```
N = Ncurrent*Nmos*2;
num = temp(2:2:N,2:Nnode+1)-temp(1:2:N,2:Nnode+1);
den = kron(ones(1,Nnode),(temp(2:2:N,1)-temp(1:2:N,1)));
gradmatrix = num./den;

% rearrange Vdiff to obtain gradient matrix
for i = 1:Ncurrent
  J((i-1)*Nnode+1:i*Nnode,:) = gradmatrix((i-1)*Nmos+1:i*Nmos,:)';
end

% load estimated Vgate parameters
fid = fopen('vgate.sp');
for i = 1:Nmos
  tline = fgetl(fid);
  N = size(tline,2);
  Nequal = find(tline == '=');
  Vgate(i,1) = str2num(tline(Nequal+1:N));
end
fclose(fid);

% compute update
Vdiff = Vmeas-Vest;
Vgate_new = Vgate+0.5*inv(J'*J)*J'*Vdiff;

% write new Vgate potential to vspice.sp
fid = fopen('vgate.sp','w');
for i = 1:Nmos
  fprintf(fid,'%s\n',['.param gate',num2str(i),'=',num2str(Vgate_new(i))]);
end

% create a signal file
flag = 1;
save flag flag

% exit matlab
exit
```

C.5 main.sp: main netlist (Hspice)

```
%%%%%%%%%%%%%%%%%
main.sp
```

```
%%%%%%%%%%%%%%%%%
.options list node post
.options ingold = 2

* load param list
* this file is updated after each iteration
.include vgate.sp

* load netlist of transistors
.include common.sp

* load current pattern and gnd node
* this file is updated for each different current pattern
.include source.sp

* do DC analysis for small perturbations of Vgate
* first do DC analysis
.dc
.include dcpert.sp

.end
```

C.6 vgate_org.sp: original gate potentials (Hspice)

```
%%%%%%%%%%%%%%%%%
vgate_org.sp
%%%%%%%%%%%%%%%%%
.param gate1=-1.5
.param gate2=1.5
.param gate3=-2.5
.param gate4=-0.5
.param gate5=0.5
.param gate6=2.5
```

C.7 common.sp: network interconnection (Hspice)

```
%%%%%%%%%%%%%%%%%
common.sp
%%%%%%%%%%%%%%%%%
* 6 depletion mode N-Mosfets
m1  n1 g1  n2  gnd nch l=20u w=20u
```

```
m2  n1 g2  n3  gnd nch l=20u w=20u
m3  n1 g3  n4  gnd nch l=20u w=20u
m4  n2 g4  n3  gnd nch l=20u w=20u
m5  n2 g5  n4  gnd nch l=20u w=20u
m6  n3 g6  n4  gnd nch l=20u w=20u

* depletion mode parameters
.model nch nmos level=5 zenh=0.0
+ vt=-4.0 frc=.03 tox=800 dnb=6e14 xj=0.8 latd=0.7
+ del=0.4 cj=0.1e-3 phi=0.6 exa=0.5 exp=0.5 fsb=3e-5
+ ecv=5 vst=4e7 ub=850 scm=0.5 ni=5.5e11 dp=0.7 uh=1200

* define voltage sources between the different gates and gnd
vg1 g1 gnd dc gate1
vg2 g2 gnd dc gate2
vg3 g3 gnd dc gate3
vg4 g4 gnd dc gate4
vg5 g5 gnd dc gate5
vg6 g6 gnd dc gate6
```