TECHNOLOGY TREND - IMPACT OF PROCESS VARIATIONS ON CIRCUIT PERFORMANCE

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Technology Trend - Impact of Process Variations on Circuit Performance

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Abstract: In this paper, the impact of process variations on circuit performance (delay and energy consumption) is investigated. A CMOS eight-bit mirror adder, a standard interconnect structure and finally a circuit composed of the combination of the eight-bit adder and the interconnect structure are chosen as the representative circuit elements to study the performance variations. Correlation coefficients among the parameters of interest are estimated, MATLAB is then used to generate the correlated normally distributed samples. Lastly, HSPICE serves as the circuit simulation tool to study the performance fluctuations by simulating the samples obtained from MATLAB. Focus is placed upon studying the performance variation trend in four technology nodes: 70, 100, 130 and 180nm.

Introduction: Predictability of circuit performance relies heavily upon the ability to control process variations. Having this goal in mind, this paper aims to investigate the impact of parameter fluctuations on performances. In particular the four technology nodes that would be studied are 70, 100, 130 and 180 nm. The paper is organized in four major sections. The first section discusses in details the experimental set-up involving the use of MATLAB and HSPICE to generate data and simulate fluctuations. The second section addresses the impact of the device parameter fluctuations on a simple combinational logic circuit, namely the eight-bit CMOS mirror adder. The third section discusses the delay and the energy variations resulting from the interconnect parameter fluctuations. In the last section the adder and the interconnect structure are combined to form a simple, yet realistic circuit element in which the overall performance variability is investigated.

1. Experimental Steps: Using the σ values reported by Cao [1] and obtaining the recommended device and the interconnect structure dimensions from the BPTM website [2], a table listing the nominal values of the parameters and their 3 σ variations is found in the appendix.

In order to generate correlated data in MATLAB, correlation coefficients must first be estimated. To estimate the correlation coefficient between: (1) long-channel threshold voltage (vth0) and oxide thickness (tox) and (2) long-channel threshold voltage and channel doping (nch), the following steps are taken:

a. The equation of vth0 written in terms of tox and nch is shown below:

$$V_{TH0} = V_{FB} + 2\psi_B + \frac{\sqrt{2 q N_{CH} \epsilon_S 2\psi_B}}{C_{OX}} \quad \textit{(Equation 1)}$$

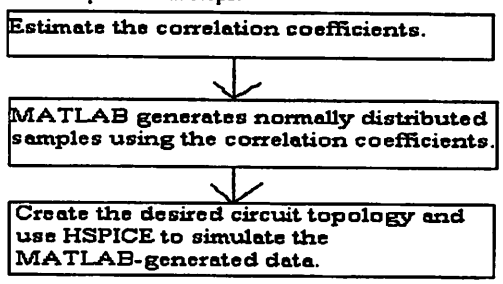
b. MATLAB is then used to generate normally distributed samples of tox and nch values whose sigma and mean are specified by the program.
c. Calculate vth0 using the equation above for each value of tox and nch.
d. Calculate correlation coefficient between vth0 and tox, and vth0 and nch.

Since virtually all devices with channel length less than 1um experience more or less channel-length dependent threshold voltage, it is thus desirable to estimate the correlation coefficient between channel length and vth0 as well. A simple, first-order equation known as Yau's model is used to perform such estimation. Yao's equation is included below for completeness sake (the derivation can found in most of the elementary device physics textbook):

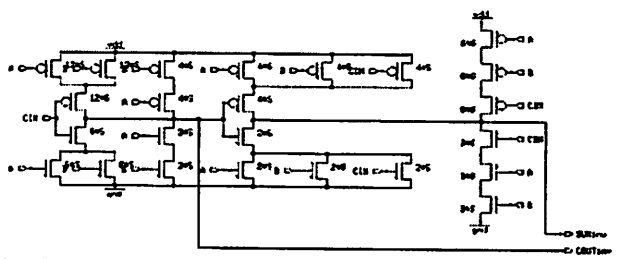
$$\Delta V_T(\text{short channel}) = -\frac{q N_{ch} W_T}{C_{OX}} \frac{r_j}{L}\left(\sqrt{1+\frac{2W_T}{r_j}} - 1\right) \quad \textit{(Equation 2)}$$

Next, correlation coefficients among interconnect parameters must be estimated as well. Assuming constant pitch throughout the interconnect structure, width of the wire and the space between the wires are negatively correlated with correlation coefficient of -1. Furthermore thickness of the wire and the distance of the wire above the ground plane are negatively correlated with correlation coefficient of -0.5 [1].

As soon as the all the required correlation coefficients are found, the statistics package in MATLAB provides a built-in function known as mvnrnd() which can be used to generate correlated samples. The final step is to perform simulation in HSPICE using the MATLAB-generated data. In particular 1,000 samples are generated and simulated for each trial. The following process summarizes the overall experimental steps:



2. Trend of the impact of device parameter fluctuations on 8-bit mirror adder performance variations: In this section, an 8-bit mirror adder is created using the schematic editor SUE. The transistor level schematic of a 1-bit mirror full adder is shown below:



The impact of device parameter fluctuations on performance variations (delay and energy consumption) is investigated for four technology nodes – 70, 100, 130 and 180 nm. To define quantitatively the meaning of performance variation, the following terminology is used throughout this paper:

$$\%\,\text{Performance Variation} = \frac{\sigma \text{ of delay or energy}}{\text{Mean of delay or energy}} \times 100\% \quad \textit{(Eq 3)}$$

Using the 3 σ and the nominal values reported in *Table 1A* in appendix, and applying equation 3 above to calculate % performance variations, *Figure 1* (below) shows the result obtained from HSPICE simulation.

Furthermore performance variations caused by variations of vth0 and lint (print gate length - 2×source drain extension) at each technology node are investigated as well. The following steps are taken to measure the performance variations contributed by vth0 and lint.

a. Measure the sigma of the delay and energy consumption with all the device parameters vth0, lint, tox, nch, and rdsw varying simultaneously.
b. Measure the sigma of the delay and energy consumption with ONLY vth0 (or lint) varying.
c. The ratio of the value in step (b) and the value in step (a) gives the % variation caused by vth0 (or lint).

Figure 2 and *Figure 3* show the results obtained from HSPICE simulation. Performance variations contributed by other parameter variations (tox, nch and rdsw) were studied as well, however it was found that these parameters do not contribute significant performance variations. Therefore plots for these parameters are omitted.

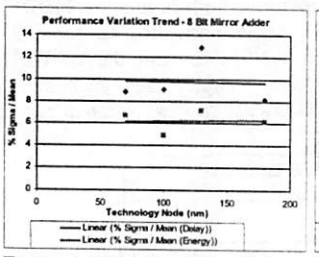


Figure 1 (Above)

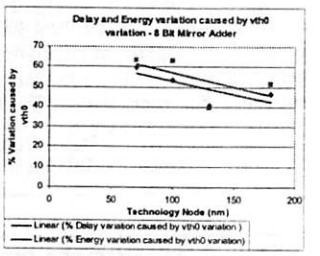


Figure 2 (Above)

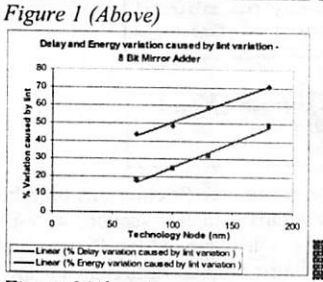


Figure 3(Above)

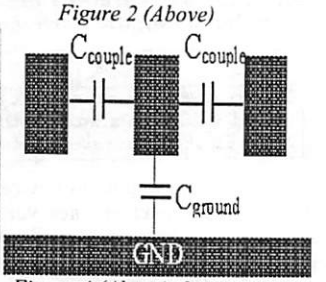
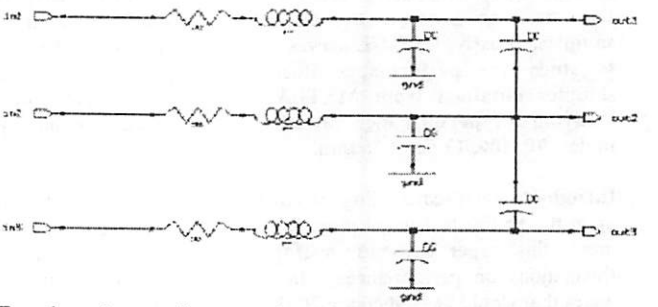


Figure 4 (Above) -Interconnect

As it can be seen in *Figure 1*, one can conclude that if the fluctuations of the device parameters can be controlled to within the σ value reported in *Table 1A*, performance variation does not show significant change as technology scales down to 70 nm node. However as transistor dimension continues to scale, lithography and other processing steps are becoming more challenging. Consequentially, maintaining the 3 σ values reported in *Table 1A* is thus more difficult.

Figure 2 shows that as critical dimension scales, performance variations caused by vth0 increase from ~43% (at 180nm) to ~60% (at 70nm). *Figure 3* shows the opposite behavior for lint. As transistor size shrinks, velocity saturation causes the delay of the transistor rather insensitive to channel length. As a result of this, delay variation caused by lint fluctuation falls from ~50% (at 180nm) to ~20% (at 70nm). Energy variation contributed by lint fluctuation falls off almost the same amount as well, from ~70% (at 180nm) to ~40% (at 70nm).

3. Trend of the impact of wire parameter fluctuations on interconnect performance variations: In this section a common interconnect structure whose cross section shown in *Figure 4* is studied. Dimensions of the interconnect parameters and their 3 σ variations (width, spacing, length ...etc) are listed in *Table 1B*. Furthermore in order to perform the HSPICE simulation, the interconnect structure is divided into segments with each of length 100 um. Therefore for instance, a 70-nm node interconnect structure with total length of 2000 um would contain 20 joined-identical segments. The schematic for the segment is shown below (note that mutual inductance between the adjacent lines is taken into account during simulation):



Equations for coupling capacitors between adjacent lines, line-to-ground capacitor, self-inductance of the line, mutual inductance between the lines and line resistances are shown below. These equations are obtained from the BPTM website [2].

$$C_{COUPLE} = \epsilon \left[1.44 \frac{t}{s} \left(\frac{h}{h + 2.059\,s} \right)^{0.0944} + 0.7428 \left(\frac{w}{w + 1.592\,s} \right)^{1.144} + 1.158 \left(\frac{w}{w + 1.874\,s} \right)^{0.1612} \left(\frac{h}{h + 0.9801\,s} \right)^{1.179} \right]$$

$$C_{GROUND} = \epsilon \left[\frac{w}{h} + 2.21 / \left(\frac{s}{s + 0.702\,h} \right)^{2.193} + 1.171 \left(\frac{s}{s + 1.510\,h} \right)^{0.7642} \left(\frac{t}{t + 4.532\,h} \right)^{0.1204} \right]$$

$$L = \frac{\mu l}{2\pi} \ln \left(\frac{2l}{w + t} \right) + 0.5 + 0.2235 \frac{w + t}{l}$$

$$M = \frac{\mu l}{2\pi} \left[\ln \left(\frac{2l}{s} \right) - 1 + \frac{s}{l} \right]$$

$$R = \frac{R_{OU}\, l}{w\, t},$$

$$R_{OU} = 2.2\,\Omega - cm$$

Using the equations above and the values in *Table 1B*, correlated normally distributed samples are generated in MATLAB. Applying the performance variation terminology defined in *equation 3* and following the steps described in section 2 for find the variation caused by each individual parameter, HSPICE simulation results are shown below (*Figure 5 ~ 10*) using those MATLAB-generated samples. Note that the term 'energy' appearing in the following figures refers to the amount of energy needed to charge up the line instead of the energy dissipated by the resistive elements.

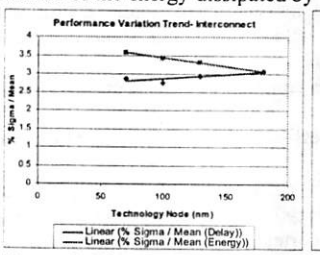


Figure 5 (Above)

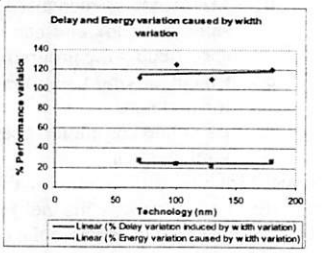


Figure 6 (Above)

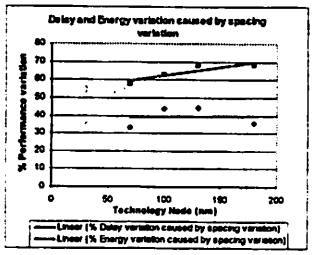


Figure 7 (Above)

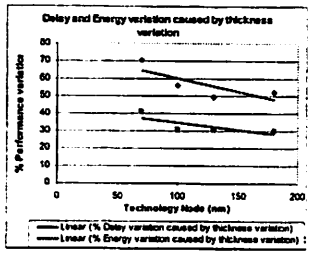


Figure 8 (Above)

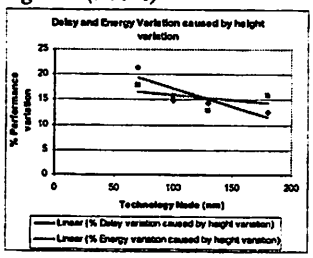


Figure 9 (Above)

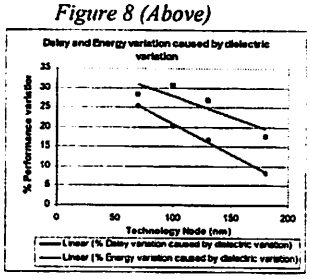
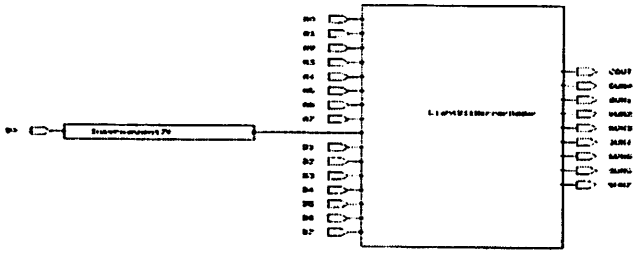


Figure 10 (Above)

An important detail worth mentioning is that from *Figure 5*, again it is seen that if the interconnect parameters vary according to the 3 σ values reported in *Table 1B*, the observed performance variation remains small. This is the same conclusion drawn previously in section 2. See *Figure 1* for comparison.

4. Trend of the impact of wire && device parameter fluctuations on overall performance variations: A circuit composed of an interconnect structure and an 8-bit mirror adder is shown below. Bit B0 is driven by a voltage pulse. Then the delay is measured from the time the pulse is applied to the time in which the bit SUM7 rises to half of voltage supply value. Another quantity that is measured is the energy consumption, which is the amount of energy needed to cause bit SUM7 to rise (or fall).



The goal of this section attempts to find out how much of the delay (or energy) variation is caused by the interconnect (or device) parameter fluctuations. To obtain the data shown in *Figure 11* (below), device parameters (vth0, lint, tox...etc) are fixed temporarily and only interconnect parameters are allowed to vary. As it can be seen from the plot, interconnect parameter fluctuations almost contribute nothing to delay variations (blue line). *Figure 12* on the other hand shows a plot in which interconnect parameters are fixed, while the device parameters are allowed to vary. In this plot it clearly shows that delay variation is ultimately due to device variations only. Figure 11 and Figure 12 together also show that interconnect variations contribute most to the energy variation.

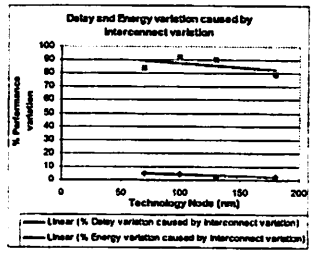


Figure 11 (Above)

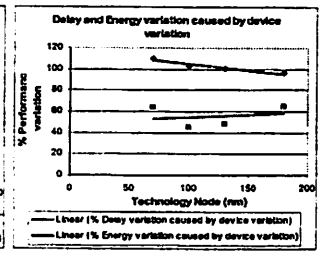


Figure 12 (Above)

Conclusion: In this paper, an 8-bit mirror adder, interconnect structure (*Figure 4*) and a circuit containing both the adder and the interconnect structure are chosen as representative circuit elements to study performance variations due to parameter fluctuations. It is found that if the parameters vary according to the 3 σ variations reported in *Table 1AB*, overall performance variation stays constant even when critical dimension scales down to 70nm node. Furthermore the delay and the energy variation trend for the 8-bit mirror adder show that vth0 contributes increasing amount of variation as transistor size scales while the opposite is true for lint variation due to the velocity saturation phenomenon. Lastly it is observed that when interconnect structure and logic (transistors) element are both present in a circuitry, logic element contributes mostly to the delay variation while interconnect structure contributes mostly to the energy variation.

Acknowledgement: The author would like to thank his advisor Costas Spanos for providing insightful discussions about the project.

Bibliography:

[1] Y.Cao, P.Gupta, A.B.Kahng, D.Sylvester and J.Yang, "Design Sensitivities to Variability: Extrapolations and Assessments in Nanometer VLSI", ASIC, 2002.

[2] "Berkeley Predictive Technology Model", http://www-device.eecs.berkeley.edu/~ptm

APPENDIX

TABLE 1A - Technology Trend – Device parameter values and their 3 σ variations

	180 nm		130 nm		100 nm		70 nm	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
Vdd (V)	1.8		1.2		1.0		0.9	
Vth0 (V)	0.3999 ± 30%	-0.4014 ± 30%	0.3353 ± 30%	-0.3499 ± 30%	0.2607 ± 30%	-0.3030 ± 30%	0.1902 ± 30%	-0.1987 ± 30%
Lint (m)	4e-8 ± 20.88%	3e-8 ± 33.40%	2.5e-8 ± 26.72%	2e-8 ± 37.58%	2e-8 ± 25.05%	2e-8 ± 25.05%	1.6e-8 ± 19.83%	1.5e-8 ± 22.27%
Tox (m)	4e-9 ± 4%	4e-9 ± 4%	3.3e-9 ± 4%	3.3e-9 ± 4%	2.5e-9 ± 4%	2.5e-9 ± 4%	1.6e-9 ± 4%	1.6e-9 ± 4%
Nch (cm^-3)	5.95e17 ± 10%	5.92e17 ± 10%	5.6e17 ± 10%	6.85e18 ± 10%	9.7e17 ± 10%	1.04e18 ± 10%	1.2e18 ± 10%	1.2e18 ± 10%
Rdsw (ohm/sq)	250 ± 10%	450 ± 10%	200 ± 10%	400 ± 10%	180 ± 10%	300 ± 10%	150 ± 10%	280 ± 10%

TABLE 1B - Technology Trend – Global Interconnect parameter values and their 3 σ variations

	180 nm	130 nm	100 nm	70 nm
Fixed Length (m)	5000e-6	3300e-6	2500e-6	2000e-6
Width (m)	0.80e-6 ± 20%	0.60e-6 ± 20%	0.50e-6 ± 20%	0.45e-6 ± 20%
Spacing (m)	0.80e-6 ± 20%	0.60e-6 ± 20%	0.50e-6 ± 20%	0.45e-6 ± 20%
Thickness (m)	1.25e-6 ± 10%	1.20e-6 ± 10%	1.20e-6 ± 10%	1.20e-6 ± 15%
Height (m)	0.65e-6 ± 15%	0.45e-6 ± 15%	0.30e-6 ± 15%	0.20e-6 ± 15%
Dielectric	3.5 ± 3%	3.2 ± 5%	2.8 ± 5%	2.2 ± 5%