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ADVANCED MATERIALS AND STRUCTURES FOR NANOSCALE CMOS DEVICES

by

Dae-Won Ha

Memorandum No. UCB/ERL M04/46

6 December 2004

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ELECTRONICS RESEARCH LABORATORY

College of Engineering
University of California, Berkeley
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Advanced Materials and Structures for Nanoscale CMOS Devices

by

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B.S. (Yonsei University, Korea) 1993
M.S. (Yonsei University, Korea) 1995

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Nov. 16, 2004

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Nov. 24, 2004

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Fall 2004

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Abstract

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Doctor of Philosophy in Engineering –

Electrical Engineering and Computer Sciences

University of California, Berkeley

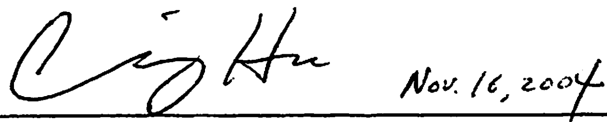
Professor Chenming Calvin Hu, Chair

Technological innovations have accomplished the continued scaling of CMOS devices well into nanometer regime. Short channel effects have been suppressed by the use of thinner gate oxide, shallower junction depth, and sophisticated channel doping profile without changing its basic structure. However, further CMOS scaling will be much more intricate due to fundamental materials and process limitations. The advanced thin-body transistor structures can effectively suppress the short channel effects, separating the need of heavy channel doping and the state-of-the-art thin gate oxide. This dissertation investigates the integration of advanced materials in front-end processes with advanced thin-body transistor structures.

Two essential processes in molybdenum (Mo) metal gate technology are developed: damage-free sputtering and high-selectivity dry etching. The physical origin of Mo gate work function engineering is simultaneous modification of the microstructure and chemistry at the gate dielectric interface, as discussed in chapter 2.

The impact of gate process technology on hafnium oxide (HfO_2) gate dielectric is explored. The increase in equivalent oxide thickness and leakage current is resulted from the generation of oxygen vacancy, which causes silicon interfacial layer formation and gate electrode Fermi-level pinning in MOS devices, as discussed in chapter 3.

Tunable work function Mo gate is demonstrated for adjusting threshold voltages of ultra-thin body MOSFETs for the first time. Integration of metal gate and high-*k* gate dielectric employing FinFETs is demonstrated for the first time; Mo-gated HfO_2 CMOS FinFETs reduce gate leakage current over 3 orders-of-magnitude for inversion equivalent oxide thickness (1.72 nm) with comparable carrier mobility, as discussed in chapter 4.



Professor Chenming Calvin Hu

Dissertation Committee Chair

To my parents,
for their unforgettable love and sacrifices

To my wife,
for her everlasting love, support and encouragements

To my son,
for his brilliant and ambitious future

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Dae-Won Ha

November 2004,

Berkeley, California

Chapter 1

Introduction

1.1 Future of CMOSFETs

Remarkable progress in semiconductor industry has led to the proliferation of microelectronic devices and information technology. The predominant technology is based on silicon CMOSFETs, the basic building blocks of integrated circuits. Over the past three decades, rapid and steady improvements in circuit performance and packing density have been achieved through the scaling of CMOS devices. The CMOS scaling has been accomplished with technological innovations, and leads the device dimensions well into the nanometer regime, as illustrated in **Figure 1.1** [1.1, 1.2].

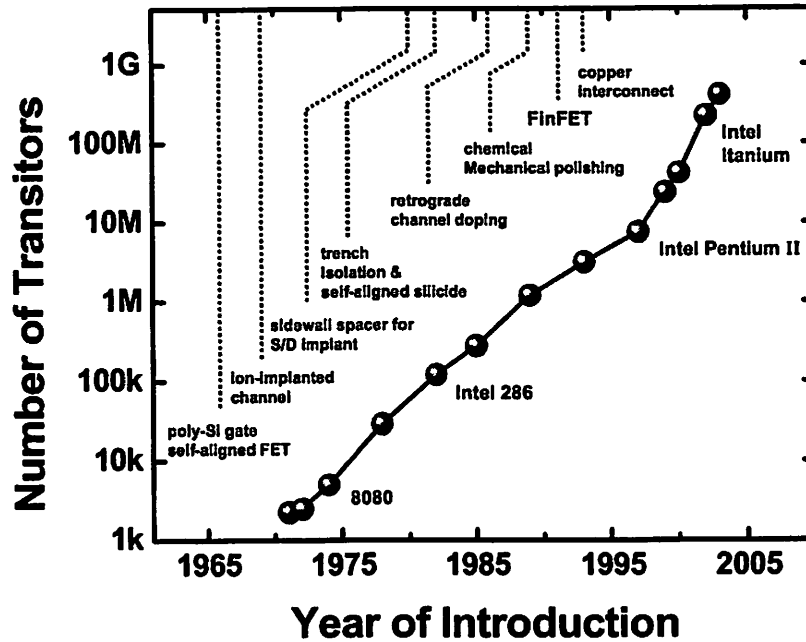


Figure 1.1 Remarkable progress in integration of transistors into a central processing unit (CPU). Technological innovations have accomplished the continued scaling of silicon-based CMOS devices, and shrunk them into the nanometer regime [1.1, 1.2].

However, new technological barriers should be overcome for future nanoscale CMOS scaling, because some fundamental materials and process limits are rapidly approached [1.3]; emphasis will be on the reduction of standby power consumption without aggravating the device performance.

To achieve low off-state leakage current of a bulk-Si MOSFET, the channel potential should be controlled by the gate electrode rather than the drain electrode; thus, the gate-to-channel capacitance should be larger than the drain-to-channel capacitance.

Historically, this has been achieved through the use of thinner gate oxide, shallower source/drain junction depth, and complex channel doping engineering [1.4, 1.5].

Thinner gate oxide, *silicon dioxide*, increases gate capacitance. However, for a silicon dioxide thickness of 2.0 nm or below, direct quantum mechanical tunneling through the dielectric leads to an exponential increase in leakage current with decreasing oxide thickness [1.6]. Therefore, thicker and higher permittivity dielectrics need to be investigated as an alternative gate dielectric to replace the traditional silicon dioxide.

Shallow junction depth decreases the capacitive coupling of the drain to the channel. However, the formation of ultra-shallow junction depth is limited due to the finite energy of ion implantation and transient enhanced dopant diffusion during the thermal budget for dopant activation [1.7]. Parasitic series resistance in the junction regions could degrade the transistor on-state current, demanding technological innovations such as raised source/drain structures or activation of dopants at concentrations higher than the solid solubility.

Higher channel doping concentration with a localized halo in a bulk-Si transistor shields the channel from the influence of the drain potential [1.8]. However, too heavy channel doping decreases carrier mobility, increases parasitic junction capacitance and

leakage current, and worsens the subthreshold slope. These factors combined can significantly deteriorate either performance or standby power consumption. Variations in device properties due to random dopant fluctuation effects may limit chip yield due to the intolerable clock skews or malfunction of the circuits [1.2].

Recently, advanced thin-body transistor structures such as ultra-thin body (UTB) single gate and double gate MOSFETs have been proposed to suppress the off-state leakage current without degrading the on-state current [1.9, 1.10]. The use of ultra-thin undoped channel can effectively suppress the off-state leakage current, overcoming the aforementioned challenges in nanoscale bulk-Si MOSFETs. Reduced vertical electric field improves the gate dielectric reliability and reduces gate tunneling current. Circuit performance can be further increased due to the higher channel carrier mobility and reduced parasitic junction capacitance. However, implementation of such device structures has difficulties in process integration, except for the FinFET which provides self-alignment of top and bottom gates, highest packing density and easy access to all four transistor electrodes [1.11]. Remaining challenges for FinFETs to maximize the performance and minimize the standby power consumption are illustrated in **Figure 1.2**, and addressed in the subsequent chapters.

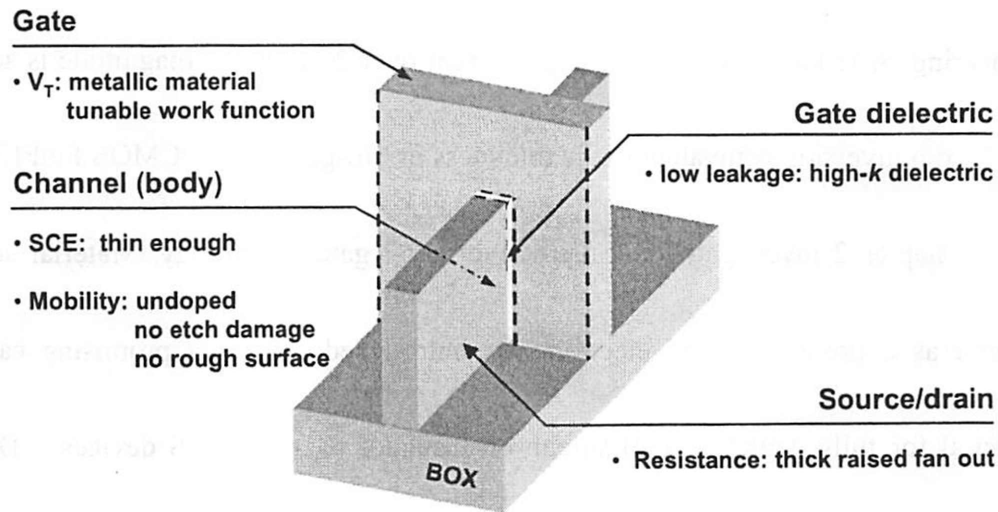


Figure 1.2 The FinFET provides relatively simple process integration, thus is one of the most promising double gate structures manufacturable below sub-25 nm gate length. However, technological innovations illustrated are required to maximize the performance benefits.

1.2 Objectives

In this dissertation, the key technological innovations illustrated in Figure 1.2 are addressed for the future nanoscale CMOS technologies. The process integration challenges and device performance of the advanced gate stack materials employing the advanced thin-body transistor structures are experimentally explored for the first time. A method of adjusting threshold voltages of ultra-thin body MOSFET and FinFET is

demonstrated for the first time with tunable molybdenum (Mo) gate work function engineering. A reduction of gate leakage current over 3 orders-of-magnitude is achieved for 1.72 nm inversion equivalent oxide thickness in Mo-gated HfO_2 CMOS FinFETs.

Chapter 2 investigates the alternative metal gate technology. Material selection criteria as a promising gate electrode are introduced; Mo is a promising candidate material for fully depleted (FD) silicon-on-insulator (SOI) CMOS devices. Damage-free sputtering with *plasma charge trap* and highly-selective dry etching processes are discussed and the analysis results of the work function shift for nitrogen implanted Mo gate are presented.

Chapter 3 explores the alternative high-*k* gate dielectric technology. The key basic material properties as a promising gate dielectric are summarized; HfO_2 is one of the most promising materials to replace SiO_2. The impact of gate process technology is experimentally investigated. Successful integration of HfO_2 depends on minimizing the oxygen vacancy formation during CMOS fabrication through a reduction of post gate deposition thermal budget, and careful selection of the gate electrode material.

Chapter 4 investigates design methodology and process integration challenges for the advanced thin-body transistor structures. Adjustment of the desired threshold

voltages without degrading the performance benefits becomes a serious challenge. Mo gate work function engineering is experimentally demonstrated to be an attractive approach for adjusting the threshold voltages of advanced thin-body transistor structures. Integration of Mo gate and HfO_2 gate dielectric employing FinFET is experimentally demonstrated to reduce the gate leakage current over 3 orders-of-magnitude for 1.72 nm inversion equivalent oxide thickness.

Chapter 5 provides an overall summary of this dissertation. Key research contributions and suggestions for future research directions and possibilities are highlighted.

1.3 References

[1.1] G. E. Moore, "No Exponential Is Forever: But "Forever" Can Be Delayed!," in *Int. Solid State Circuits Conf. Dig.*, pp. 20-23, 2003.

[1.2] H.-S. P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann, and J. J .Welser, "Nanoscale CMOS," *Proc. IEEE*, vol. 87, no. 4, pp. 537-570, 1999.

[1.3] *International Technology Roadmap for Semiconductors*, Semiconductor Industry Association, 2003 (available at http://public.itrs.net).

[1.4] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," IEEE J. Solid-State Circuits, vol. 9, pp. 256-268, 1974.

[1.5] J. R. Brews, W. Fichtner, E. H. Nicollian, and S. M. Sze, "Generalized Guide for MOSFET Miniaturization," *IEEE Electron Device Lett.*, vol. 1, pp. 2-4 , 1980.

[1.6] S.-H. Lo, D. A. Buchanan, and Y. Taur, "Modeling and Characterization of Quantization, Polysilicon Depletion, and Direct Tunneling Effects in MOSFETs with Ultrathin Oxides," *IBM J. Res. Develop.*, vol. 43, no. 3, pp. 327-337, 1999.

[1.7] A. Hokazono, K. Ohuchi, M. Takayanagi, Y. Watanabe, S. Magoshi, Y. Kato, T. Shimizu, S. Mori, H. Oguma, T. Sasaki, H. Yoshimura, K. Miyano, N. Yasutake, H. Suto, K. Adachi, H. Fukui, T. Watanabe, N. Tamaoki, Y. Toyoshima, and H. Ishiuchi, "14 nm Gate Length CMOSFETs utilizing Low Thermal Budget Process with Poly-SiGe and Ni Salicide," in *IEEE Int. Elec. Dev. Meet. Tech. Dig.*, pp. 639-642, 2002.

[1.8] Y. Taur, C. H. Wann, and D. J. Frank, "25nm CMOS design considerations," in *IEEE Elec. Dev. Meet. Tech. Dig.*, pp. 789-792, 1998.

[1.9] R.-H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: From Bulk to SOI to Bulk," *IEEE Trans. Elec. Dev.*, vol. 39, no.7, pp. 1704-1710, 2000.

[1.10] D. J. Frank, S. E. Laux, and M. V. Fischetti, "Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?," in *IEEE Elec. Dev. Meet. Tech. Dig.*, pp. 553-556, 1992.

[1.11] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," in *IEEE Elec. Dev. Meet. Tech. Dig.*, pp. 67-70, 1999.

Chapter 2

Metal Gate Technology

2.1 Introduction

Polycrystalline silicon (poly-Si) gate technology has been used in CMOS devices for several decades. One of the primary reasons is its excellent thermal stability on SiO_2 during the high temperature source/drain annealing steps. This allows the source/drain regions to be self-aligned to the gate, thus eliminating parasitic capacitance from overlay misalignment during the lithography process [2.1]. Another reason is the easy controllability of its work function at the SiO_2 interface. Its work function can be modified from a low value (~4.17 eV) to a high value (~5.1 eV) by the ion implantation of appropriate dopants; dual-doped poly-Si gates allow the threshold voltages of NMOS

and PMOS to be adequate for CMOS applications, thus dramatically reducing the circuit power consumption [2.2].

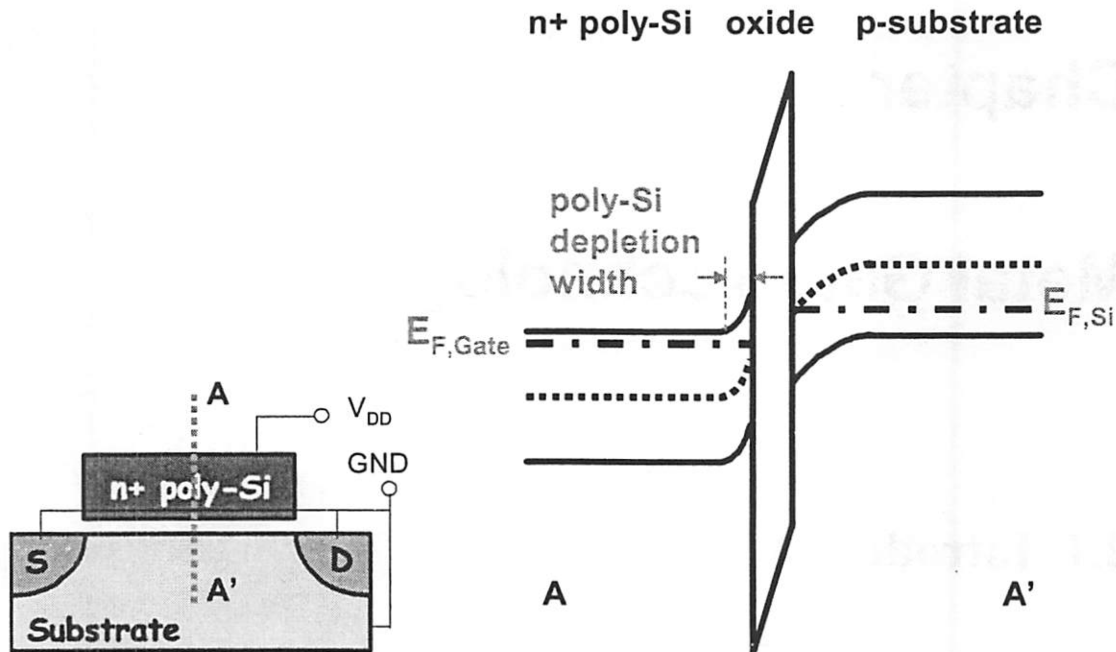
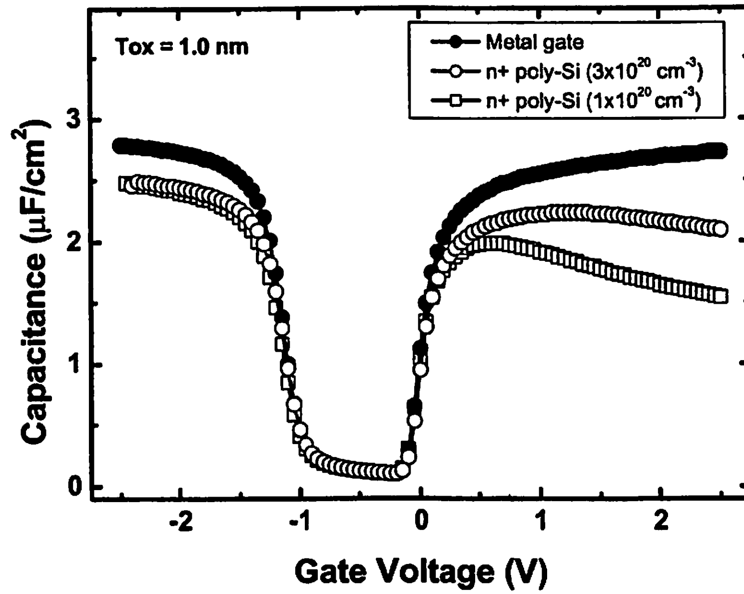


Figure 2.1 Energy band diagram of a n-channel MOS capacitor showing the depletion layer in the poly-Si gate, which typically adds several angstroms to the capacitance equivalent gate dielectric thickness (CET) when the channel is in strong inversion.

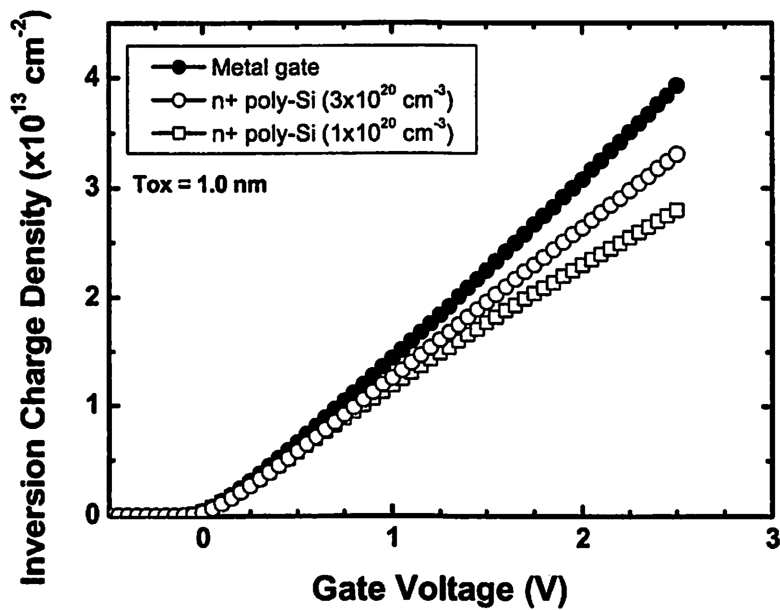
However, dual-doped poly-Si gates may not be promising any longer for nanoscale CMOS transistors due to poly-Si gate depletion effect (PDE), high sheet resistance, and boron dopant penetration through the gate oxide, etc. Among these concerns, the poly-Si gate depletion effect (PDE) is the most compelling reason; that is, a heavily doped poly-Si gate becomes slightly depleted at the gate oxide interface when the

channel is in strong inversion [2.3]. **Figure 2.1** illustrates a schematic band diagram across a MOS transistor in strong inversion. When the MOS transistor is biased into the strong inversion, an electric field is developed across the gate oxide. Since the oxide field points in the direction of accelerating a negative charge toward the gate, the bands in the poly-Si gate bend slightly upward toward the oxide interface, which depletes the surface of electrons and forms a thin depletion region ($W_{d,poly}$) in the poly-Si gate. This effectively increases the capacitance-equivalent thickness (CET) of the gate dielectric and decreases the inversion charge density in the channel, thus lowering the total gate capacitance and driving current of transistors. **Figure 2.2** shows the quantum-mechanical simulation results of (a) C-V characteristics, and (b) inversion charge densities of poly-Si and metal gate NMOS transistors [2.4]. Since the oxide field becomes stronger with a thinner oxide (< 1.5 nm), the poly-Si gate depletion effect has more detrimental effects on nanoscale CMOS transistor performance.

Another concern with the poly-Si gate electrode is the high sheet resistance. Since the sheet resistance (R_S) is a function of thickness (t) and resistivity (ρ) of the gate electrode material, a thicker poly-Si gate and/or a lower resistivity is helpful to decrease the sheet resistance. However, a thicker gate stack proves to a poor choice due to the



(a)



(b)

Figure 2.2 Quantum-mechanical (QM) simulation results of (a) C-V characteristics, and (b) inversion charge density of poly-Si (open symbols) and metal gate (solid circle) n-channel MOS transistors.

increased parasitic gate-to-source/drain capacitance, thus compromising the circuit performance [2.5]. Also, in the poly-Si gate, the resistivity is determined by the active dopant concentration, which is limited by the solid solubility and thermal annealing of dopants in silicon. While the solid solubility of dopants is a material property, the use of high temperature annealing is limited due to the need for an abrupt retrograded channel doping and shallow source/drain junction doping profiles in nanoscale CMOS transistors.

Other concerns with dual-doped poly-Si gates include dopant (boron) penetration through thin gate oxide due to the large variation in threshold voltage and degradation in gate oxide reliability [2.6], thermodynamic incompatibility with future high-k gate dielectrics such as ZrO_2 [2.7], HfO_2 [2.8], and so on.

Metal gate electrodes can eliminate all of the aforementioned concerns, thus are indispensable for sub-65 nm CMOS technology node [2.9]. However, there are challenges in process integration that should be overcome to apply the metal gate technology to nanoscale CMOS devices.

2.2 Material Selection for Gate Electrode

In selecting alternative CMOS gate electrode materials, several factors must be considered [2.10]; these include the thermal stability on gate dielectric during high-temperature annealing step(s), the compatibility of the material growth and patterning with the conventional CMOS processes, the work function on a gate dielectric, the impact of gate processes on device performance and reliability, and the extendibility to future high-*k* gate dielectrics.

The highest-temperature annealing step(s) used in today's CMOS fabrication occurs during the source/drain dopant activation. Typically, the dopant activation is accomplished through rapid thermal annealing (RTA) at temperatures around or slightly above 1000°C for a few seconds in an inert ambient. Therefore, prospective gate materials should be thermodynamically stable on the gate dielectric, and have a higher melting point than 1000°C. It is worthwhile to note that choosing a material with a thermal expansion coefficient close to that of silicon is very desirable because the thermally induced stress may result in cracking or peeling of the gate stack materials.

The processes for material deposition and patterning should be compatible with the conventional CMOS processes. The deposition process plays an important role on

the interface quality between gate electrode and dielectric. Most thin metal films are deposited using either chemical vapor deposition (CVD) or physical vapor deposition (PVD) method. While CVD method leads to minimal damage and a smooth interface with the underneath gate dielectric, the precursors for only a limited number of metal films like tungsten (W), aluminum (Al), titanium nitride (TiN) have been well identified. On the other hand, PVD method can be used for most of the metal films with minimal incorporation of impurities, although new techniques need to be developed to prevent physical damage to the gate dielectric from the energetic particles (metal ions and/or electrons). Also, the dry etching process with high selectivity and vertical sidewall profile is indispensable for nanoscale CMOS device fabrication. While wet chemical etching results in high selectivity to the gate dielectric, the inherent isotropic etching characteristic prevents it from patterning the gate electrode in nanoscale CMOS device fabrication. Therefore, the dry etching process condition should be optimized (or developed) for the gate material.

The effect of the work function of gate electrode on the device operation is through its control of the threshold voltage (V_T), which determines how much a gate voltage should be applied to invert the channel. For conventional bulk transistors, the

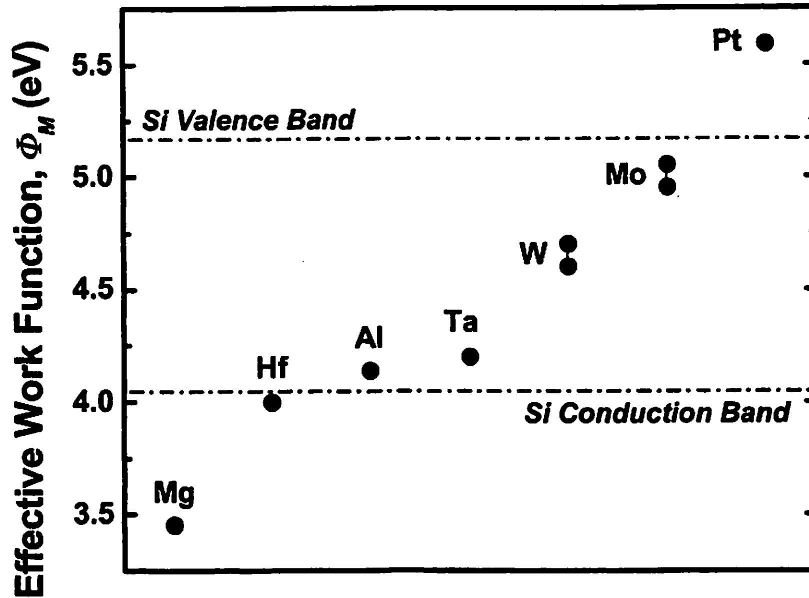


Figure 2.3 Experimental work function data for metals on silicon oxide (SiO_2) [2.12].

silicon channel has a heavily (10^{16} – 10^{18} cm^{-3}) retrograded-doping profile to suppress the short channel effects. Thus, the work function difference between gate electrode and silicon channel affects the threshold voltage. A comprehensive quantum-mechanical (QM) simulation study shows that the device performance and short channel effects can be optimized simultaneously with metal gate electrode whose work function is near the conduction band (E_C) for NMOS device and the valence band (E_V) for PMOS device [2.11]. **Figure 2.3** shows the experimental work function data for metals on silicon dioxide (SiO_2) [2.12]. On the other hand, for advanced thin-body transistors, the silicon

channel has an undoped or lightly (< 10^{16} cm^{-3}) uniform doping profile to minimize the dopant fluctuation effect and maximize the carrier mobility. Thus, threshold voltage adjustment should be achieved by the work function of gate electrode due to the negligible depletion charge [2.12]. It is worth to note that a lightly doped thin-body can effectively suppress the short channel effects through the proper design of the device parameters such as the ratio of gate length to body thickness, $\zeta = L_G/T_{Si}$. The optimized gate electrode work function is 0.35 eV below (above) the conduction (valence) band for NMOS (PMOS) devices [2.10]. **Figure 2.4** shows the theoretical data for threshold voltage of the thin-body MOSFET as a function of the gate work function [2.13].

Several material systems and process integration approaches which satisfy the aforementioned criteria have been investigated to date for CMOS applications: dual metal (Ti/Mo) [2.14], metal interdiffusion (Ti/Ni) [2.15], metal alloying (Ru/Ta) [2.16], fully silicided ($NiSi_x$) doped polysilicon [2.17], and tunable-work-function metal (Mo) gate [2.18, 2.19, 2.20].

The tunable-work-function Mo gate technology offers the simplest CMOS process integration and better compatibility with high-*k* gate dielectric materials [2.19].

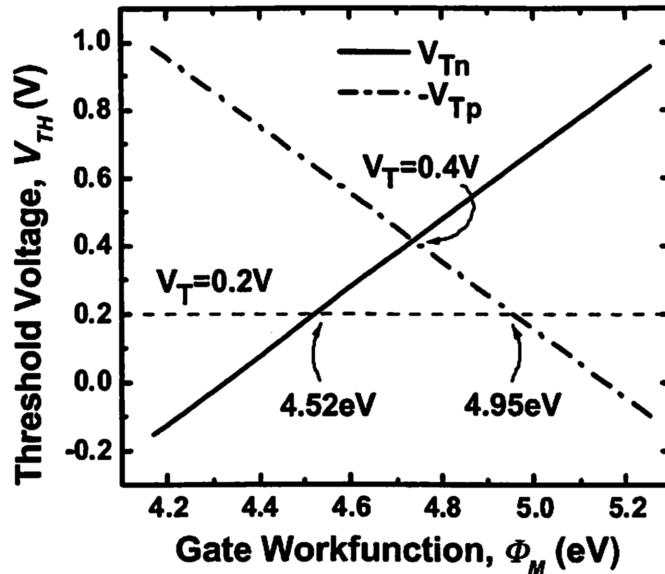


Figure 2.3 Theoretical data for threshold voltage of the thin-body MOSFET as a function of the gate work function [2.13].

Gate work function engineering via selective nitrogen implantation into the Mo gate electrode will provide multiple values of threshold voltage (V_T) for NMOS and PMOS transistors on a single substrate. A higher melting point (2617°C) [2.21] and thermodynamic stability on SiO_2 and high-*k* dielectrics such as ZrO_2, HfO_2, etc [2.22, 2.23] allow for the self-aligned (gate-first) CMOS transistor fabrication. It should be noted that the adjustable-work-function fully silicided ($NiSi_x$) method may not be applied on the future high-k dielectrics due to the thermodynamic instability [2.24]. The following sections will discuss the process details of the tunable-work-function Mo gate technology.

2.3 Damage-free Molybdenum Sputtering

Physical vapor deposition (PVD), also known as sputter deposition, and chemical vapor deposition (CVD) are the most widely used techniques for the fabrication of thin-film structures on semiconductor wafers. The physical vapor deposition as compared with chemical vapor deposition provides an important advantage of minimal incorporation of impurities. However, the physical vapor deposition is a relatively violent, atomic-scale process in which an energetic particle strikes a solid, resulting in the emission of one or more atoms from the solid sputtering target; thus, sputtering process may introduce damage to the gate dielectric.

2.3.1 Sputtering System for Molybdenum

A DC-magnetron sputtering system (*Novellus m2i with Quantum source*) was used to deposit the Mo gate films. **Figure 2.5** illustrates the schematics of the sputtering system; it has two load-lock stations, a wafer degassing station, sputtering chambers, and a cooling station. The base pressure of the sputtering chamber is maintained below $5x10^{-8}$ Torr, and argon (Ar) gas was used for Mo target sputtering.

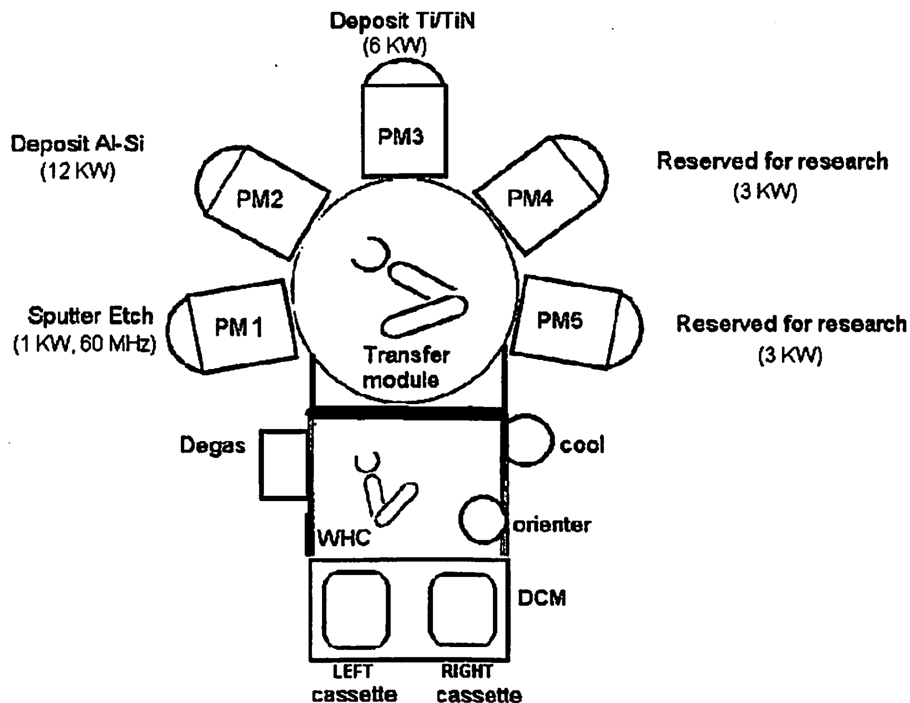


Figure 2.5 Schematic of the Mo sputtering system; loaded wafers in load-lock station are transported to process module 5 for Mo sputtering.

The critical requirements for a gate deposition process are: zero damage to the gate dielectric and good step coverage for non-planar transistor structures. Sputtering damage can result in degraded gate-oxide integrity (GOI) and transistor drive current due to degraded field-effect carrier mobility. The sputtering damage can be minimized by eliminating the high-energy particle bombardment by interposing an electrically grounded *Plasma Charge Trap* (PCT) between the Mo target and substrate, separating the plasma excitation and Mo film deposition [2.25]. **Figure 2.6** illustrates a schematic

of the sputtering chamber with the PCT, which is made of 1.66 mm thick stainless steel and has arrays of closely packed 3.32 mm diameter holes (40.3% aperture area). Since the PCT is electrically grounded, it collects high energy ions as well as a fraction of the neutral Mo atoms which are traveling toward the cathode/sample plane. These particles are deposited onto the PCT, and hence are not deposited onto the wafer surface. Therefore, the sputtering damage can be minimized. It is worth noting that the Mo deposition rate with the PCT is reduced by about 70% and is proportional to the PCT aperture area.

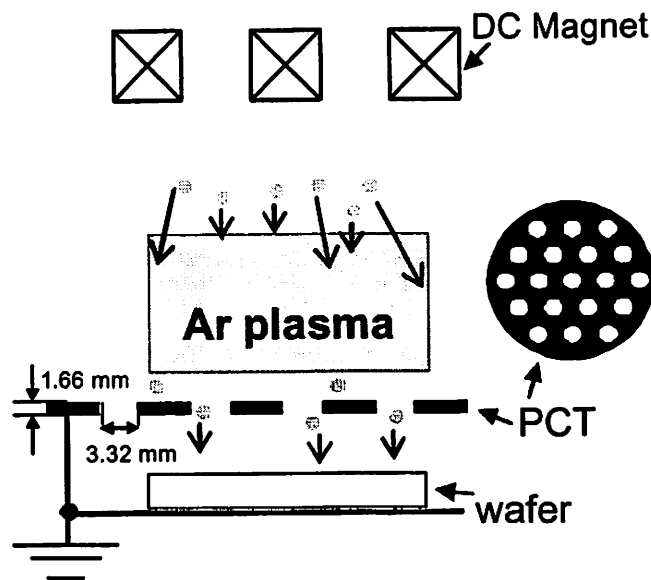


Figure 2.6 Schematic of the sputtering chamber with the plasma charge trap (PCT), which is inserted between the sputtering target (Mo) and wafer.

2.3.2 Experimental Results and Discussion

To investigate the efficacy of the plasma charge trap (PCT) for minimizing the sputtering damage, conventional bulk silicon p-channel MOSFETs were fabricated with Mo gates sputtered either with or without the PCT. Mo-gate films with 50 – 150 nm thicknesses were deposited at 200°C with 10 mTorr process pressure and 300 W sputtering power.

Damage to the gate dielectric can be assessed by measuring the gate leakage current density and gate-dielectric lifetime. Gate leakage current densities for Mo-gated PMOS capacitors are compared against those of p+ poly-Si gated PMOS capacitors (control samples) as shown in **Figure 2.7**. The p+ poly-Si gated devices show a large variation in gate leakage current due to boron dopant penetration through the gate oxide. The Mo-gated devices have lower gate leakage with much tighter distributions; the PCT provides ~30% lower gate leakage due to the lower (more negative) threshold voltage of the Mo-gated devices, even though the electrical stressing condition is more severe compared to the control samples,.

Figure 2.8 shows the Charge-to-Breakdown (Q_{BD}) and measured Time Dependent Dielectric Breakdown (TDDB) of gate oxide. The measured transistor gate

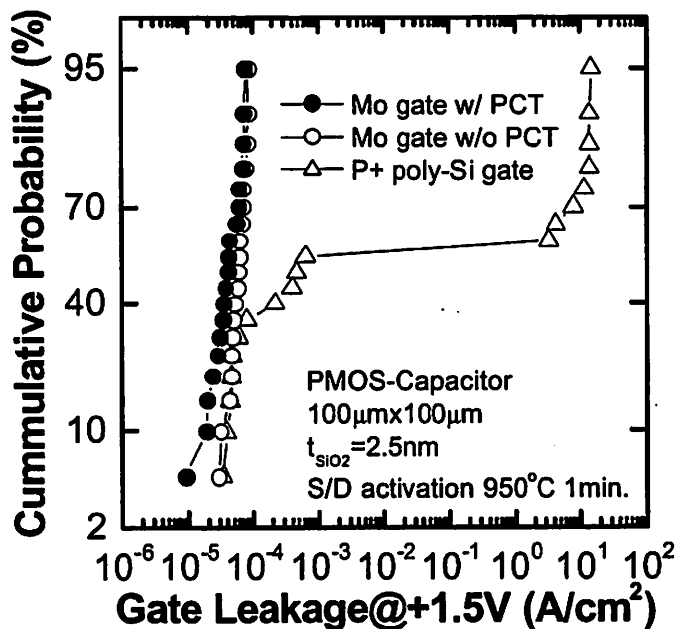


Figure 2.7 Gate leakage current densities of Mo-gated PMOS capacitors are compared against those of p+ poly-Si gated PMOS capacitors.

area is 150 μm^2. For the Q_{BD} measurements, the devices were biased at a constant gate voltage +4.4 V. Since the devices have the same threshold voltage, the effective stressing condition is the same for both groups of samples. It is worth to note that the breakdown of a thinner gate oxide occurs by bulk trap generation, not by interface trap generation, and is therefore driven by gate voltage [2.26]. With PCT Mo sputtering, the gate oxide integrity is significantly improved; indicating that low sputtering damage to gate dielectric is achieved.

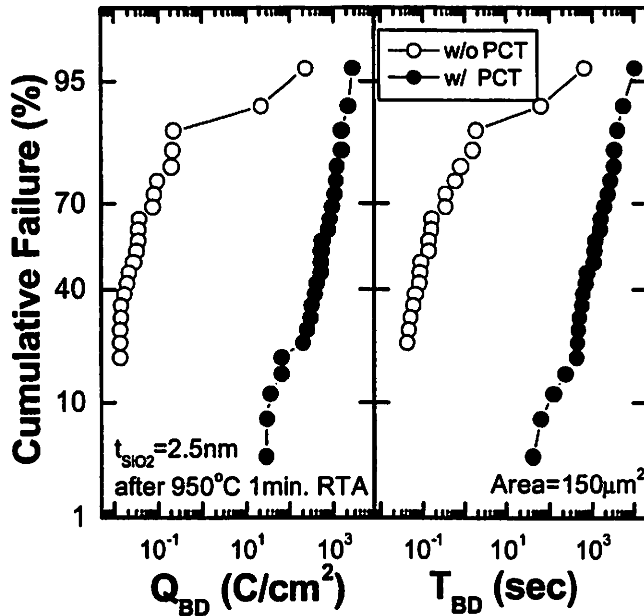
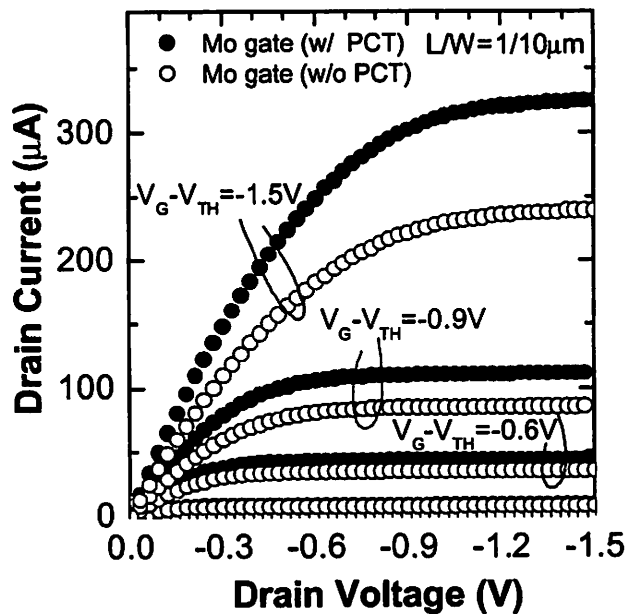
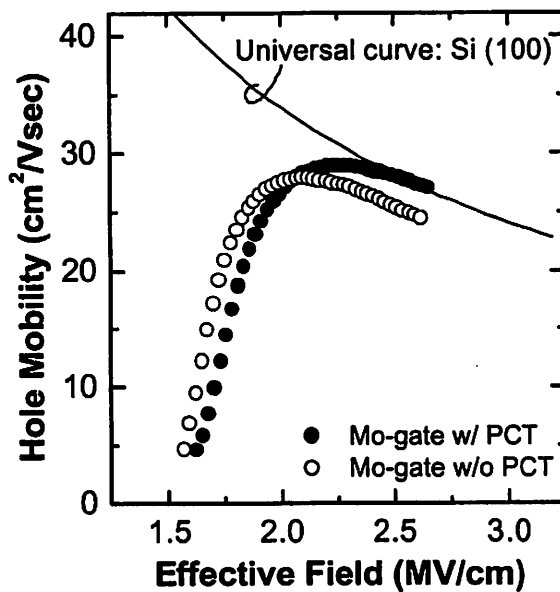


Figure 2.8 Measured Charge-to-Breakdown (Q_{BD}) and Time Dependent Dielectric Breakdown (TDDB) of Mo-gated p-channel MOSFETs. With PCT Mo sputtering, the gate oxide integrity is significantly improved, indicating that low sputtering damage to gate dielectric is achieved.

Figure 2.9 (a) shows the measured $I_D - V_D$ characteristics of Mo-gated bulk-Si p-channel MOSFETs. The drive current achieved with a PCT sputtered Mo gate is higher due to improved hole mobility as shown in **Figure 2.9** (b), which matches the universal mobility curve. The improved hole mobility is attributed to reduced interface traps (Q_{it}) and/or fixed charge (Q_f) due to the damageless Mo gate sputtering process [2.27].



(a)



(b)

Figure 2.9 (a) Measured $I_D - V_D$ characteristics, and (b) measured effective hole mobility of Mo-gated p-channel bulk-Si MOSFETs.

2.4 Highly Selective Molybdenum Dry Etching

It is known that fluorine (F) and chlorine (Cl) radicals can etch Mo films at an appreciable rate [2.28]. Therefore, Mo-gate films can be etched using either F-based or Cl-based etching gases such as CF_4, CF_3Cl, Cl_2, etc. However, fluorinated carbon compounds like CF_4 and/or CF_3Cl, which may attack the underneath gate dielectric (SiO_2) [2.29], are precluded due to the selectivity requirement. Thus, focusing on a Cl_2/O_2 gas mixture, the dependences of etch rate and selectivity to SiO_2 on Cl_2/O_2 gas flow rates, source and bias RF powers were investigated.

2.4.1 Dry Etching System for Molybdenum

A Transformer Coupled Plasma etcher (*LAM Research TCP 9400*) was used to etch the Mo gate films. **Figure 2.10** illustrates the schematic of the dry etching system; it has load (unload)-lock stations and a process chamber. The process chamber has two RF power (source, bias) supplies running at the same time during the dry etching process, which results in a high-density plasma with adjustable substrate bias.

The critical requirements for a gate etching process are high selectivity to the gate dielectric (SiO_2) and vertically etched profile. **Figure 2.11** shows the minimum

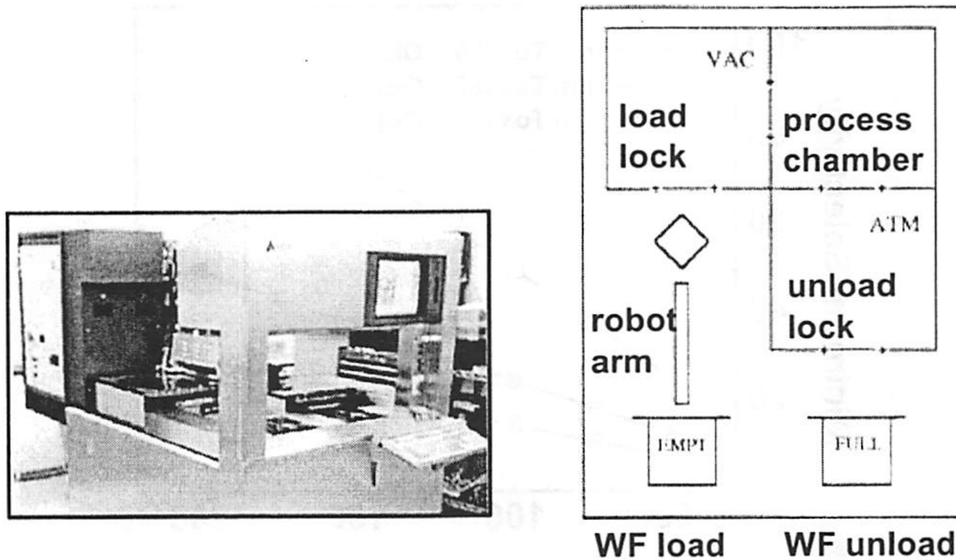


Figure 2.10 Schematics of the Mo dry etching system (LAM Research TCP9400).

etch selectivity required, as a function of gate stack thickness. For example, the etching selectivity must be higher than 25:1, assuming that the thicknesses of the Mo gate and SiO_2 gate oxide are 100 nm and 2 nm, respectively, with a 50% over-etch.

2.4.2 *Experiment Results and Discussion*

Conventional bulk-Si sample wafers with 100 nm thick thermally grown SiO_2 and 300 nm thick Mo film (or 1 μm thick photo resist) on the SiO_2 were prepared to investigate the etching characteristics of Cl_2/O_2 gas mixture. To calculate the etch rate of the thin films, physical step-height and optical thickness measurements were adopted

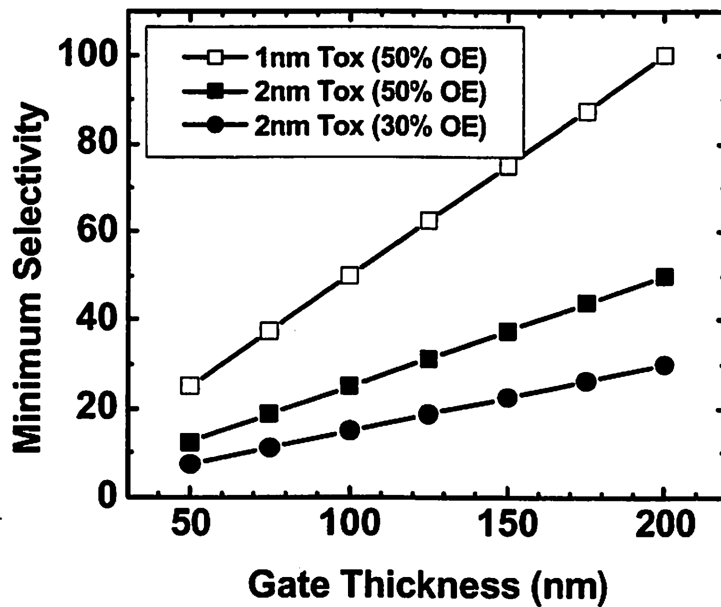


Figure 2.11 Minimum etch selectivity required as a function of gate stack thickness.

before and after the dry etching process of each sample wafer. The Mo film was sputtered in the Novellus system, SiO_2 was thermally grown in a wet oxidation furnace at 900°C, and *i*-line (OCG OiR-10i) photo resist was hard baked in 10 minutes at 120°C.

Figure 2.12 shows the dependence of the etch rates of Mo, SiO_2 and photo resist (PR) on the oxygen partial pressure in a Cl_2/O_2 gas mixture. The total gas flow rate was held constant at 130 sccm, and the process pressure was 13 mTorr with 150W/100W source/bias RF powers. With sufficient chlorine and oxygen radicals, the addition of oxygen gas increases the Mo-gate etching rate and decreases the SiO_2 etch rate, and hence improves the selectivity. This implies that the surface of the Mo film can be

easily oxidized and reacted with chlorinated gas to sublimate at ~100°C in the form of molybdenum oxychlorine (MoO_xCl_y) [2.30]. It should be noted that more than 75% oxygen results in significant etching of the photo resist (PR), which may prevent it from being used as a useful masking material.

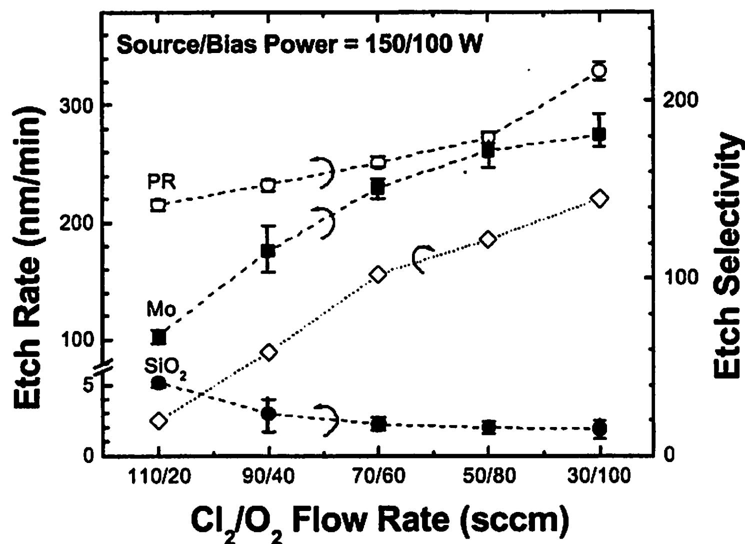


Figure 2.12 Etch-rate dependences of Mo, SiO_2, and photoresist (PR) on the oxygen partial pressure in the Cl_2/O_2 gas mixture. The total gas flow rate was held constant at 130 sccm, and the process pressure was 13 mTorr with 150 W source RF power and 100 W bias RF power.

Figure 2.13 shows the dependence of Mo and SiO_2 etch-rate on source power with a constant gas flow rate (Cl_2/O_2 = 70/60 sccm), process pressure (13 mTorr), and bias power (100 W). The etch rates of Mo and SiO_2 increase linearly with source power

because more chlorine and oxygen radicals are available, but the selectivity decreases due to the faster increase in SiO_2 etch rate. For source powers below 150 W, the etch rate of SiO_2 is constant due to the DC self-bias voltage, so that the etch selectivity is degraded.

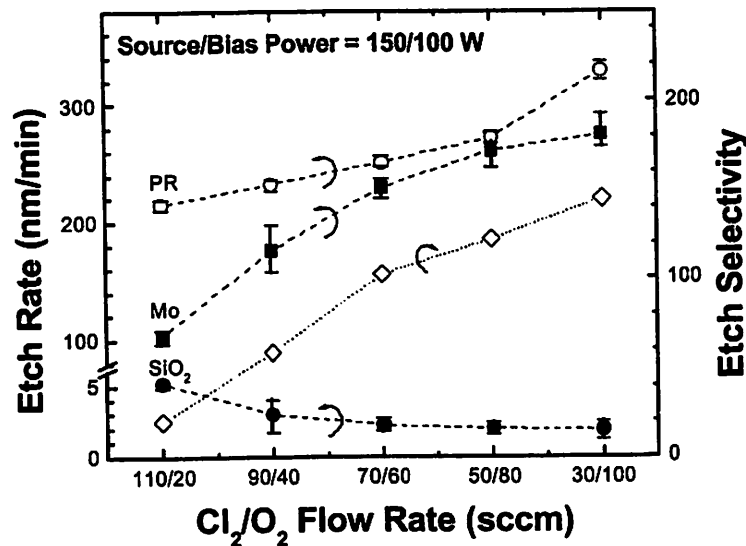


Figure 2.13 Etch-rate dependences of Mo and SiO_2 on source power with constant gas flow rate (Cl_2/O_2 = 70/60 sccm), process pressure (13 mTorr), and bias power (100 W).

Figure 2.14 shows the dependence of Mo and SiO_2 etch-rate on bias power with constant gas flow rate (Cl_2/O_2 = 70/60 sccm), process pressure (13 mTorr), and source power (150 W). The Mo etch rate saturates above 100 W bias power, whereas SiO_2 etching rate increases monotonically. Therefore, the etch selectivity decreases with increasing bias power. This indicates that energetic ion bombard-ment does not always

increase the Mo etch rate, and that chemical etching plays an important role. It is worth to note that the bond dissociation energy of SiO_2 is larger than that of Mo [2.31].

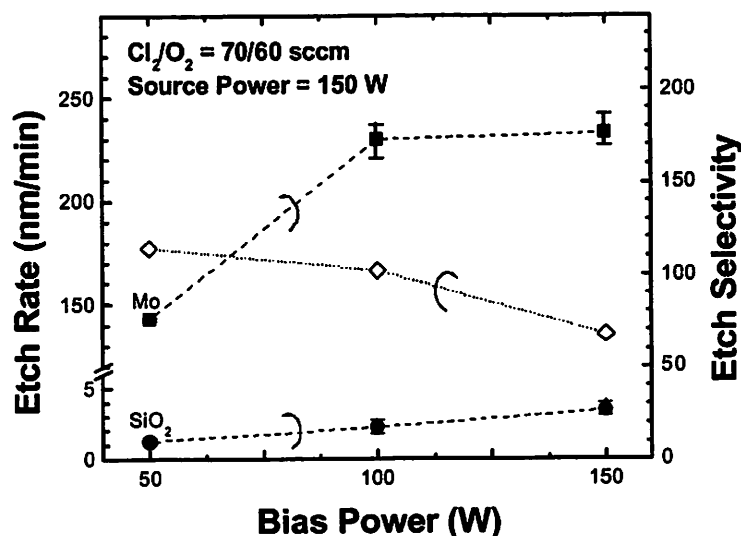


Figure 2.14 Etch-rate dependences of Mo and SiO_2 on bias power with constant gas flow rate (Cl_2/O_2 = 70/60 sccm), process pressure (13 mTorr), and source power (150 W).

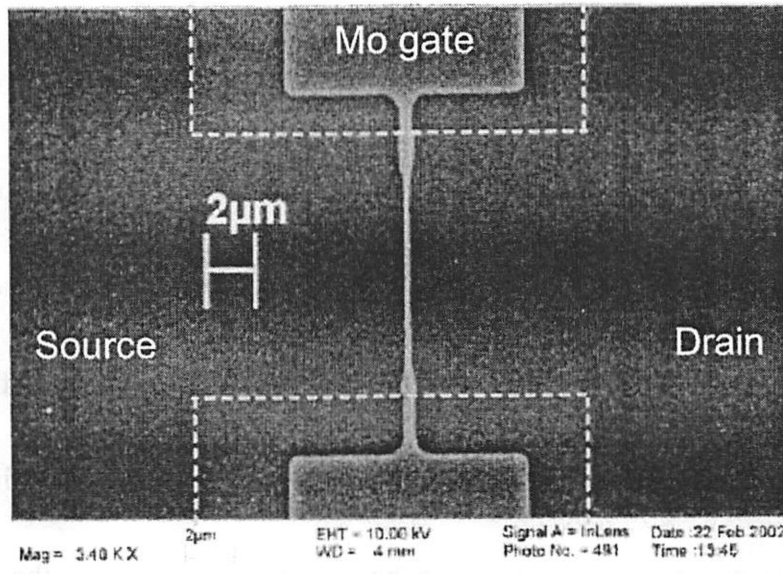
Table 2.1 summarizes the optimized Mo gate etch process condition which yields 230 nm/min etch rate and ~100:1 (Mo:SiO_2) etch selectivity: Cl_2/O_2 = 70/60 sccm, process pressure = 13 mTorr, source/bias RF power = 150/100 W.

Figure 2.15 shows the plane- and tilted-view scanning electron microscopy (SEM) picture of the etched Mo gate profiles using the optimized etch recipe. Neither micro-trenching nor Mo gate residue was observed due to the high etching selectivity;

thus, this process condition can be directly applicable to the thin-body transistor structures including FinFETs.

Table 2.1 Optimized Mo gate dry-etching process condition.

	Step 1	**Step 2**	**Step 3**	**Step 4**	**Step 5**
	Stabilize	Stabilize	Time	Stabilize	EPD
Gap (cm)	5.8	5.8	5.8	5.8	5.8
Pressure (mTorr)	-	30	30	13	13
Source Power (W)	0	0	300	0	150
Bias Power (W)	0	0	120	0	100
CF_4 (sccm)	0	100	100	0	0
Cl_2 (sccm)	0	0	0	70	70
O_2 (sccm)	0	0	0	60	60
Time (sec)	30	30	7	30	30
End-Point-Detect	-	-	-	-	Ch A



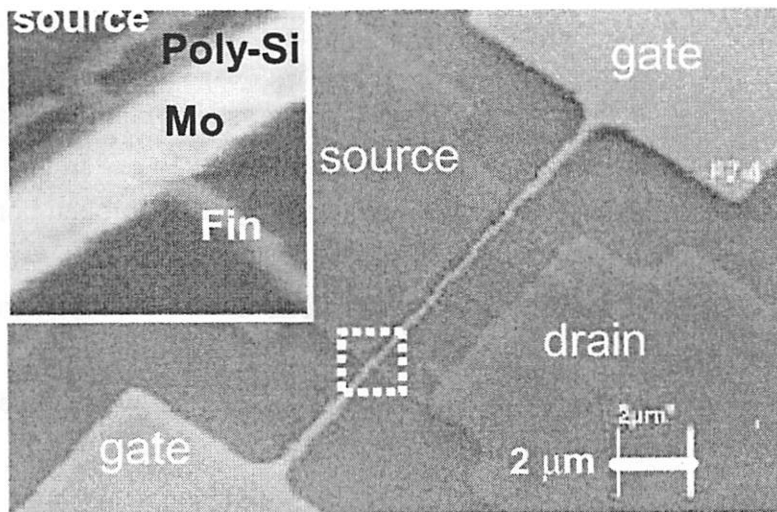


Figure 2.15 Plane- and tilted view scanning electron microscopy (SEM) picture of the etched Mo gate profiles using the optimized process condition.

2.5 Tunable-Work-Function Molybdenum Process

A *work function*, defined as a minimum energy necessary to extract an electron from a metal surface, is a fundamental property of metals that depends on both the electronic and ionic structure at that metal surface. Thus, the work function can be engineered by modifying the microstructure and/or chemistry of a metal film.

Microstructural modification can be achieved by changing the film texture or preferred orientation, crystalline phase, and crystal lattice, etc. For example, the work function of a metal film is, in general, dependent on the surface orientation (also known as the *work function anisotropy*); closely packed crystallographic surfaces show high work functions due to the smooth surface and relatively fewer broken bonds, while open crystallographic surfaces show low work functions due to a great number of broken bonds [2.32]. Experimentally it has been observed the work function in metals decreases (110) (100) (111) trend [2.33]. In addition, this was experimentally demonstrated for molybdenum (Mo) and tungsten (W) with modification of the film microstructures (surface orientation, crystalline phase) by implanting inert Ar^+ ions and/or controlling the deposition parameters [2.17, 2.34].

Chemical modification can be achieved by nitridizing, oxidizing, and alloying the metal film. It should be noted that the metal film after chemical modification should maintain high metallic conductivity to be used as a gate electrode. Modifying the film chemistry through nitridizing Mo film [2.35, 2.36], and alloying Ru-Ta [2.15] was experimentally demonstrated.

Both microstructural and chemical modifications can be simultaneously achieved by introducing foreign elements such as oxygen and nitrogen into a metal. Ion implantation is the most widely used technique to introduce dopant ions into films due to its precise control of implant dose ($\#/cm^2$), energy (eV) and tilt angle. For example, the implantation of nitrogen ions (N^+) into Mo film with subsequent annealing can modify the microstructure and chemical properties with precise control through inducing a nitridation reaction of Mo films [2.17].

2.5.1 Experimental Results and Discussion

Mo-gated capacitors were fabricated on lightly doped ($\sim 10^{15}$ cm^{-3}) p-type Si substrates with thermally grown SiO_2 as a gate dielectric. In order to account for the influence of oxide fixed charge (Q_F), multiple SiO_2 thicknesses were obtained on a single

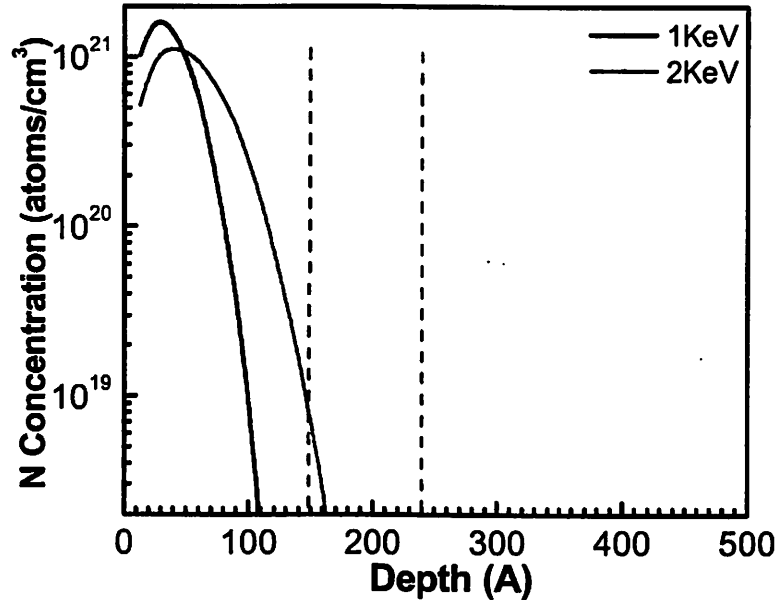


Figure 2.16 Simulated nitrogen concentration-depth profiles in the Mo/SiO_2/Si stack (Dose = 5×10^{15}/cm^2).

substrate by selective etchback using dilute HF solution. 15 nm thick Mo films were sputtered at 200°C in Novellus sputtering system, as described in Chapter 2.3, with a base pressure of 1×10^{-8} Torr and a process pressure of 10 mTorr. For some wafers, the Mo gate was implanted with nitrogen ions. The implant energies were 1 keV and 2 keV with implant dose of 5×10^{15} and 1×10^{16} cm^{-2}. Ultra-shallow nitrogen ion implantation to very thin Mo gate films was adopted to minimize the ion penetration into the gate dielectric due to the shallower projected range (R_P) and smaller straggle (ΔR_P) while allowing for high atomic nitrogen content inside the Mo films. **Figure 2.16** shows

SRIM simulation results of the nitrogen concentration-depth profiles in the $Mo/SiO_2/Si$ stacks with nitrogen implant dose of $5x10^{15}$ cm^{-2}, which is estimated to introduce about 5 % nitrogen inside the 15 nm thick Mo gate [2.37]. After gate patterning, wafers were annealed from 500°C to 900°C in N_2 ambient, followed by forming gas anneal (400°C, 15 min).

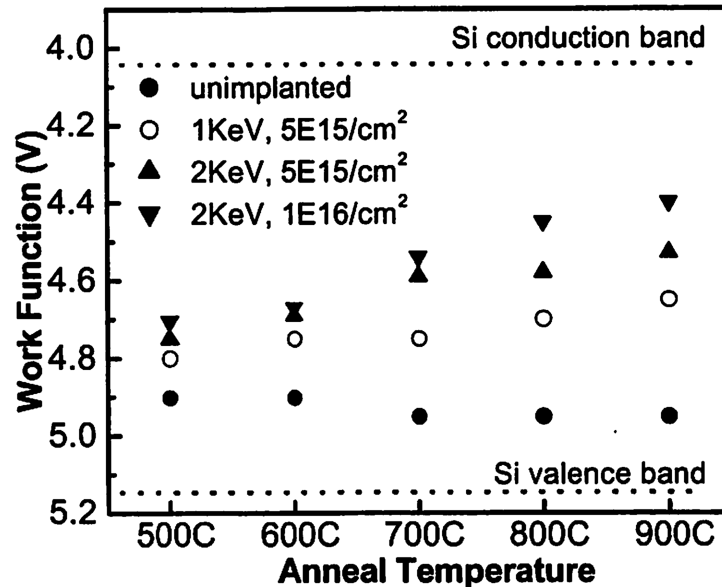


Figure 2.17 The extracted Mo work function with subsequent thermal annealing temperature. All anneals were 15 min long except for 900°C anneal (15s).

Figure 2.17 shows the extracted work function of Mo gate as a function of subsequent annealing temperature. The flatband voltages (V_{FB}) of the Mo-gated

capacitors was determined from capacitance–voltage (*C–V*) measurements, and used to extract the work function (Φ_M) [2.38]. The work function of un-implanted Mo gates increased slightly upon annealing, but is fairly stable at 4.95 eV. This increase can be ascribed to an improvement in the crystalline quality of the Mo film (increase in the columnar grain size). It is worth to note that this work function value is in good agreement with the published values for the (110) Mo work function. X-Ray Diffraction (XRD) analysis, as shown in Chapter 2.5.1, indicates that the deposited Mo film has a (110) preferred orientation.

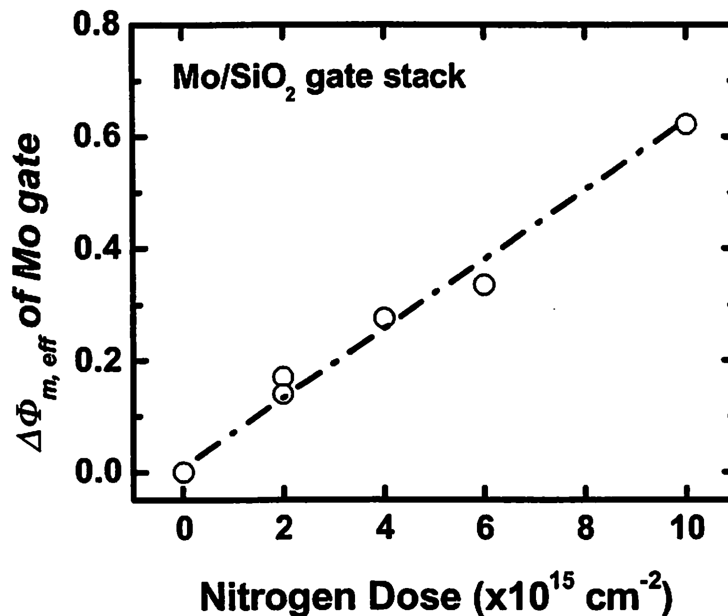


Figure 2.18 The effective work function shift of Mo gate as a function of nitrogen implant dose.

Figure 2.18 shows the effective work function shift ($\Delta\Phi_{m,eff}$) of Mo gate as a function of nitrogen implant dose. All samples were annealed at 900°C in N_2 ambient. It can be seen that the Mo gate work function decreases with a decrease in nitrogen implant doses. The amount of reduction in gate work function is proportional to the nitrogen implant dose.

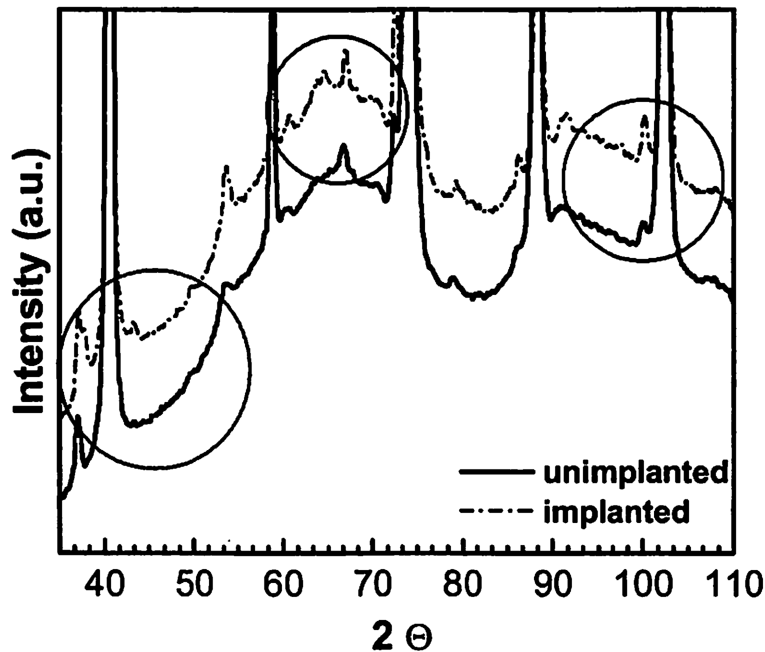


Figure 2.19 XRD analysis of nitrogen implanted and un-implanted Mo films.

In order to investigate the origin of the work function shift, x-ray diffraction (XRD) analysis of nitrogen implanted (dose = 1×10^{16} cm^{-2}) and un-implanted wafers were performed (**Figure 2.19**). Several diffraction peaks corresponding to Mo_2N can be

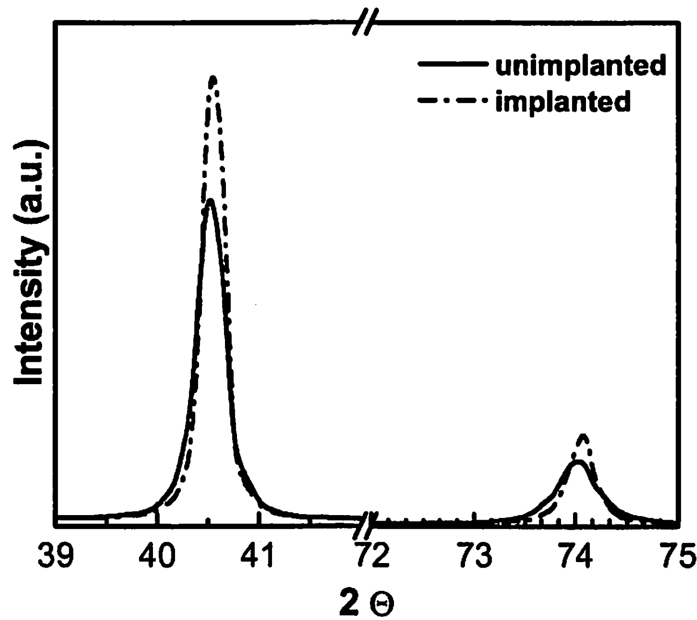


Figure 2.20 Comparison of the XRD intensities for the 110 and 112 peaks.

observed in nitrogen implanted wafers. **Figure 2.20** compares the intensities for the (110) and (112) peaks, indicating that both Mo gates have predominantly a (110) texture. **Figures 2.21** (a–d) shows the details of diffraction peaks, indicating that peaks for Mo_2N are observed in the nitrogen implanted sample while no such peaks are observed in the un-implanted sample. **Figure 2.22** (a–b) compares the dependence of Mo_2N (112) peak intensity on nitrogen implant dose (5×10^{15}, 1×10^{16} cm^{-2}) and subsequent annealing temperature (700, 900°C). It can be seen that increasing the dose or annealing temperature leads to an increase in the Mo_2N peak intensity. It is believed that an increase

in annealing temperature enhances segregation of nitrogen at the Mo/SiO_2 interface, resulting in a lowering of the interfacial work function.

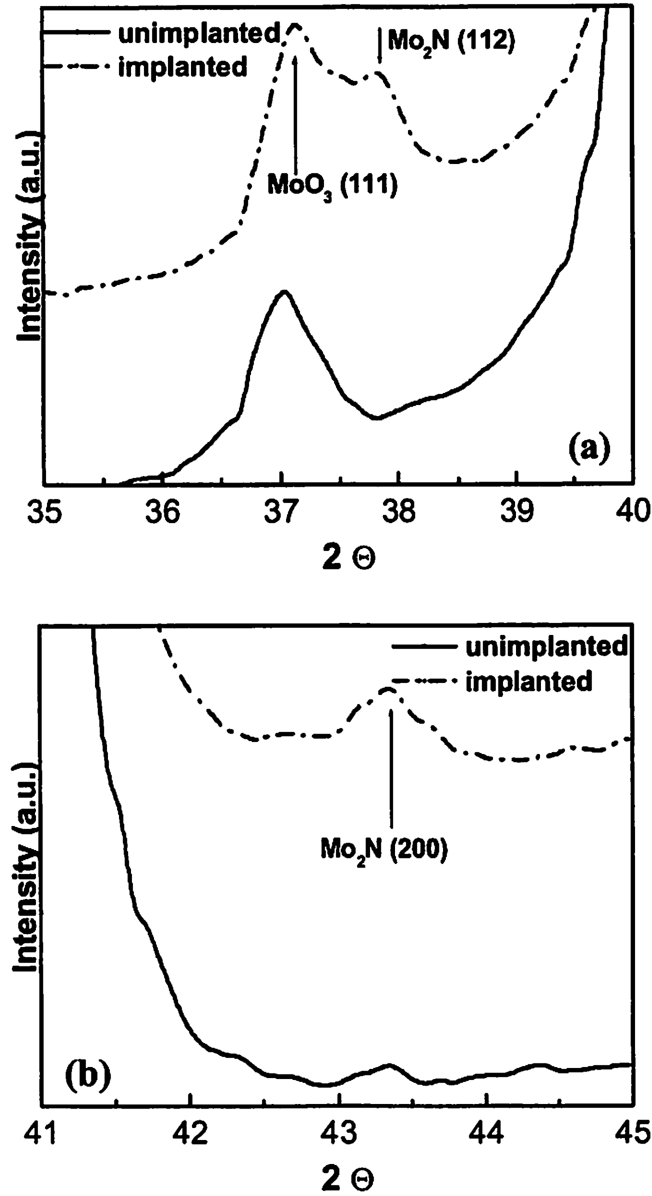
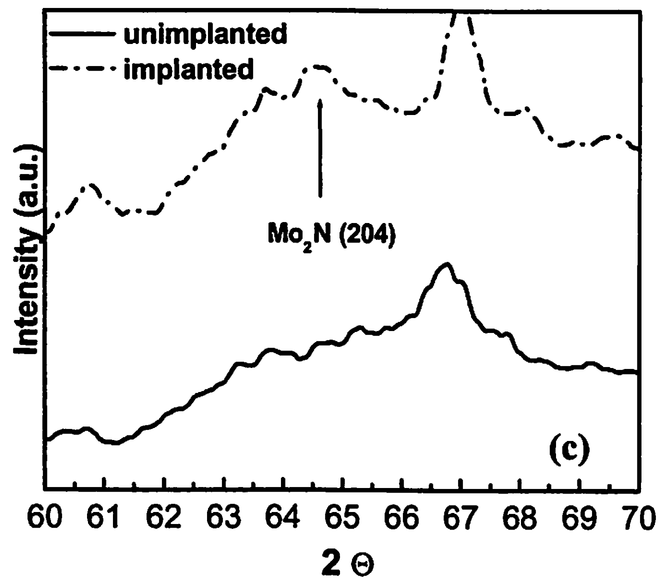


Figure 2.21 (a-d) Details of XRD peaks highlighted in Figure 2.19. Peaks indicative of Mo_2N formation are observed in the nitrogen implanted sample while no such peaks are observed in the control (un-implanted) sample.



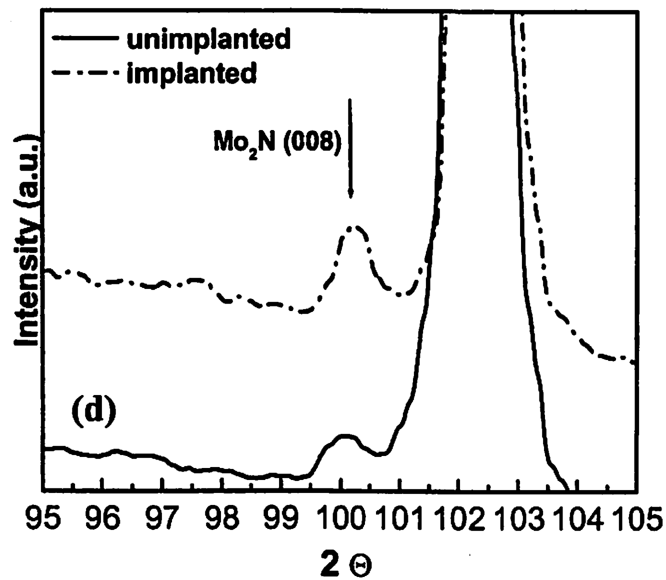
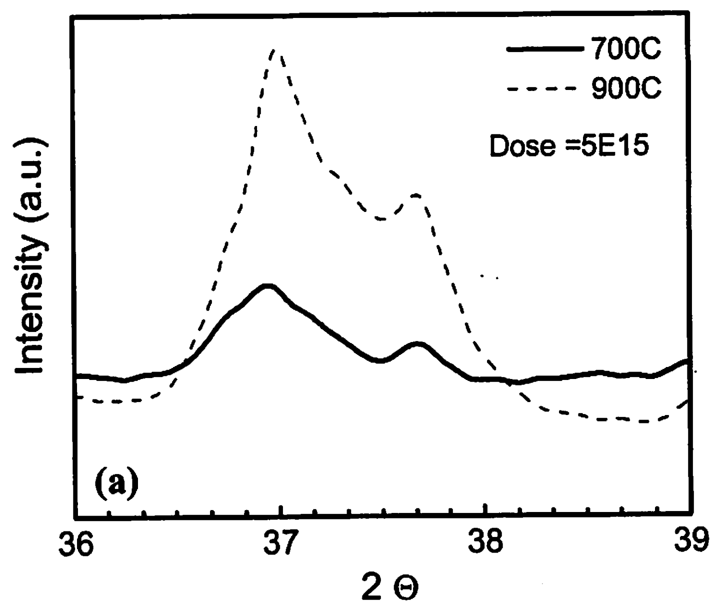


Figure 2.21 (a-d) Details of XRD peaks highlighted in Figure 2.19. Peaks indicative of Mo_2N formation are observed in the nitrogen implanted sample while no such peaks are observed in the control (un-implanted) sample.



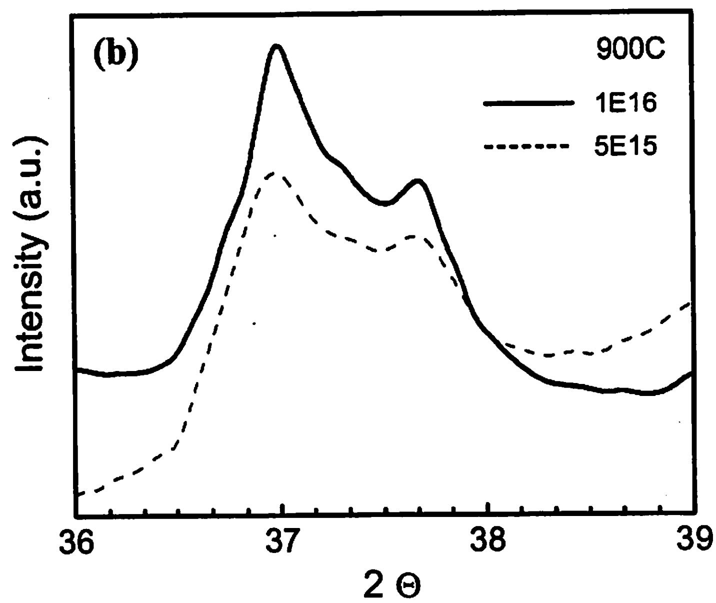


Figure 2.22 (a-b) Details of XRD peaks highlighted in Figure 2.19. Peaks indicative of Mo_2N formation are observed in the nitrogen implanted sample while no such peaks are observed in the control (un-implanted) sample.

To further analyze the chemical changes in the nitrogen implanted Mo films, x-ray photoelectron spectroscopy (XPS) analysis was performed. **Figure 2.23** shows the results of XPS analysis illustrating electron counts *vs.* binding energy for Mo and N signals at several points through the depth of Mo film. There is a significant overlap between the Mo 3p peak and the N 1s peak since they are separated by ~4 eV. Hence, the overall peak was deconvolved to isolate the Mo and N contributions. A stronger N signal accompanies the Mo signal when approaching the Mo/SiO_2 interface (point D). It is worth to note that the XPS analysis does not show the formation of MoO_2, MoO_3 or Mo-silicide at the SiO_2

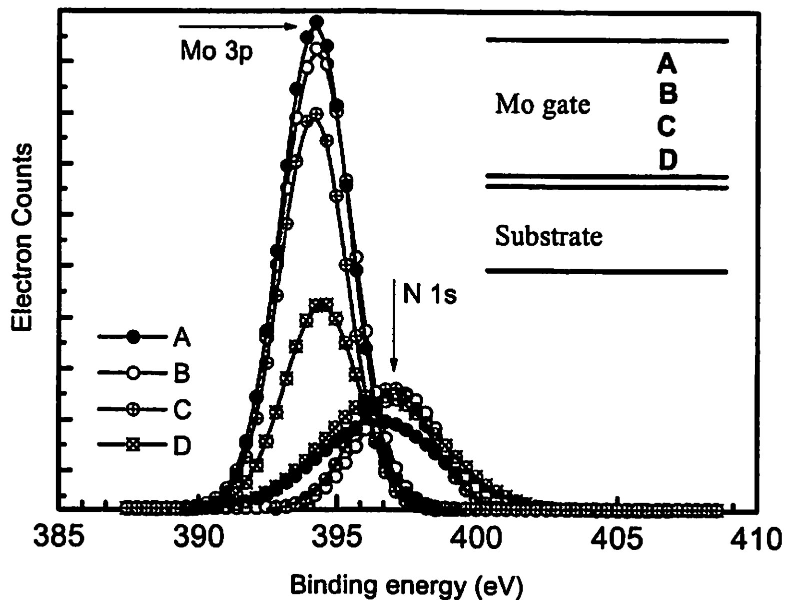


Figure 2.23 Mo 3p and N 1s binding energy at different positions across the Mo film thickness. A significant N signal is observed throughout the Mo film, indicating a diffusion of the implanted N across the film thickness.

interface, indicating the thermodynamic stability of Mo on SiO_2 at 900°C.

The diffusivity and solubility of N inside Mo at high temperatures (> 1000°C) have been evaluated [2.39,2.40]. While the relevant data for lower temperatures is not available, the extrapolated N diffusion coefficient at 900°C is very high (~2×10^{-8} cm^2/s). Low temperature diffusivities in poly-crystalline thin films are expected to be much higher, since the grain boundary diffusion would tend to dominate over bulk diffusion in the low temperature regime [2.41]. The low solid solubility of N in Mo (<1% at 1000°C) supports the observed formation of Mo_2N after N implantation. The implanted N atomic content for a dose of 1×10^{16} cm^{-2} into a 15 nm Mo film is ~10%. Thus, a combination of enhanced diffusivity and low solubility leads to the segregation of N and formation of Mo_2N in N implanted Mo films. Therefore, the work function shift of nitrogen implanted Mo gate results from a simultaneous evolution of the Mo film morphology and chemistry at the gate dielectric interface.

Figure 2.24 shows the sheet resistance (R_S) of 100-nm-thick Mo films for various nitrogen ion implantation doses after 900°C, 1-minute rapid thermal annealing (RTA) in nitrogen ambient. The sheet resistance increases slightly with implantation dose because of the increased impurity (nitrogen in Mo) scattering. The average grain

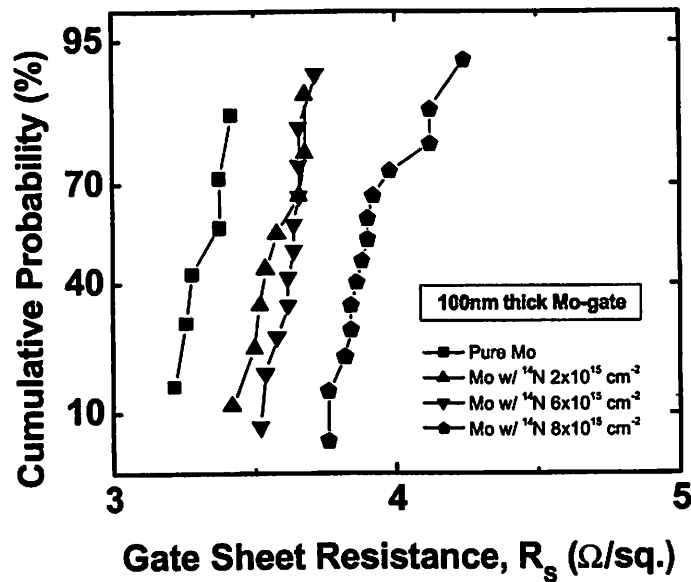


Figure 2.24 Sheet resistance (R_S) of 100 nm-thick Mo films for various $^{14}N^+$ implantation doses.

size was estimated from the full-width at half maximum (FWHM) of X-ray diffraction peaks using the Scherer formula, as shown in Figure 2.20 [2.42]. The estimated grain sizes for pure and nitrogen implanted (dose of 1×10^{16} cm^{-2}) Mo films are 46.3 nm and 63.8 nm, respectively. It is worth noting that the grain size increases as more nitrogen is incorporated [2.43].

2.6 Summary

This chapter summarized the requirements of metal gate technology for the future nanoscale CMOS technology generations. Molybdenum (Mo) is a promising

candidate gate material for fully depleted (FD) silicon-on-insulator (SOI) CMOS devices. Damage-free sputtering and high-selectivity dry etching processes for Mo gate films have been developed. With a plasma charge trap (PCT), sputtering damage to the gate dielectric can be minimized for improved drive current and gate oxide integrity (GOI). Mo gate electrodes can be patterned without leaving any residue or stringers due to the highly selective etch process. The work function of a Mo gate can be tuned by nitrogen implantation followed by a thermal anneal, to provide a means for adjusting the threshold voltage of thin-body MOSFETs. The work function shift of nitrogen implanted Mo gate is resulted from the simultaneous modification of the microstructure and chemistry of Mo film at the gate dielectric interface. The nitrogen implantation induces a slight increase in sheet resistance due to impurity scattering, although it results in a slightly larger average grain size.

2.7 References

[2.1] J. C. Sarace, R. E. Kerwin, D. L. Klein, and R. Edwards, "Metal-Nitride-Oxide-Silicon Field-Effect Transistors with Self-Aligned Gates," *J. Solid-State Electro.*, vol. 11, pp. 653-660, 1968.

[2.2] F. M. Wanlass, and C.T. Sah, "Nanowatt Logic using Field-Effect Metal-Oxide-Semiconductor Triodes," in *IEEE Int. Solid-State Circuits Conf. Digest*, pp. 32-33, 1963.

[2.3] C. Y. Wong, J. Y.-C. Y. Taur, C. S. Oh, R. Angelucci, and B. Davari, "Doping of N+ and P+ Polysilicon in a Dual-Gate CMOS Process," in *IEEE Int. Electron Device Meet. Digest*, pp. 238-241, 1988.

[2.4] Shred simulation (available at http://www.nanohub.org/)

[2.5] S. Balasubramanian, L. Chang, B. Nikolic, and T.-J. King, "Circuit-Performance Implications for Double-Gate MOSFET Scaling below 25nm," *IEEE Silicon Nano-electronics Workshop*, pp. 16 –17, 2003.

[2.6] J. Y.-C. Sun, C. Y. Wong, Y. Taur, and C. Hsu, "Study of Boron Penetration Through Thin Oxide with P+ Polysilicon Gate," in *IEEE VLSI Tech. Symp. Digest*, pp. 17-18, 1989.

[2.7] C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "MOS Characteristics of Ultra Thin Rapid Thermal CVD ZrO_2 and Zr Silicate Gate Dielectrics," in *IEEE Int. Electron Device Meet. Digest*, pp. 27-30, 2000.

[2.8] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi Level Pinning at the PolySi/Metal Oxide Interface," in *IEEE VLSI Tech, Symp. Digest*, pp. 9-10, 2003.

K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Kohno, T. Chikyo, H. Kitajima, and T. Arikado, "Physics in Fermi Level Pinning at the PolySi/Hf-based High-k Oxide Interface, in *IEEE VLSI Tech. Symp. Digest*, pp. 108-109, 2004.

[2.9] *International Technology Roadmap for Semiconductors*, Semiconductor Industry Association, 2003 (available at http://public.itrs.net).

[2.10] D. Ha, H. Takeuchi, Y.-K. Choi, and T.-J. King, "Molybdenum Gate Technology for Ultra-Thin-Body MOSFETs and FinFETs," *IEEE Trans. on Elec. Dev.*, vol. 51, pp. 1989-1996, 2004.

[2.11] I. De, D. Johri, A. Srivastava, and C. M. Osburn, "Impact of Gate Work-Function on Device Performance at the 50 nm Technology Node," *J. Solid-State Electro.*, pp. 1077-1080, 2000.

[2.12] Y.-C. Yeo, "Gate-Stack and Channel Engineering for Advanced CMOS Technology, " *Ph.D Thesis*, University of California, Berkeley, 2002.

[2.13] L. Chang, S. Tang, T.-J. King, J. Bokor, and C. Hu, "Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFETs," in *IEEE Int. Electron Device Meet. Digest*, pp. 719-722, 2000.

[2.14] Y.-C. Yeo, Q. Lu, P. Ranade, H. Takeuchi, K. J. Yang, I. Polishchuk, T.-J. King, C. Hu, S.C. Song, H. F. Luan, D. -L. Kwong, "Dual-Metal Gate CMOS Technology with Ultra-Thin Silicon Nitride Gate Dielectric", *IEEE Elec. Dev. Lett.*, vol. 22, no. 5, pp. 227-229, May 2001.

[2.15] I. Polishchuk, P. Ranade, T.-J. King and C. Hu, "Dual Work Function Metal Gate CMOS Transistors by Ni-Ti Interdiffusion", *IEEE Elec. Dev. Lett.*, vol. 23, no. 4, pp. 200-201, April 2002.

[2.16] J. H. Lee, H. Zhong, Y.-S. Suh, G. Heuss, J. Gurganus, B. Chen, and V. Misra, "Tunable Work Function Dual Metal Gate Technology for Bulk and Non-Bulk CMOS," in *IEEE Int. Electron Device Meet. Digest*, pp. 359-362, 2002.

[2.17] J. Kedzierski, E. Nowak, T. Kanarsky, Y. Zhang, D. Boyd, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong, D. Canaperi, M. Krishnan, K.-L. Lee, B. A. Rainey, D. Fried, P. Cottrell, H.-S.P Wong, M. Ieong, W. Haensch, "Metal-Gate FinFET and Fully-Depleted SOI Devices using Total Gate Silicidation," in *IEEE Int. Electron Device Meet. Digest*, pp. 247-250, 2002.

[2.18] P. Ranade, Y. K. Choi, D. Ha, A. Agarwal, M. Ameen, T.-J. King, "Tunable Work Function Molybdenum Gate Technology for FDSOI-CMOS," in *IEEE Int. Electron Device Meet. Digest*, pp. 363-366, 2002.

[2.19] R. J. P. Lander, J. C. Hooker, J. P. van Zijl, F. Roozeboom, M. P. M. Maas, Y. Tamminga, R.A.M. Wolters, "A Tunable Metal Gate Work Function using Solid State Diffusion of Nitrogen", in *Proc. European Solid-State Dev. Res. Conf.*, pp. 103-106, 2002.

[2.20] D. Ha, H. Takeuchi, Y.-K. Choi, T.-J. King, W. P. Bai, D.-L. Kwong, A. Agarwal, and M. Ameen, "Molybdenum-Gate HfO_2 CMOS FinFET Technology," in *IEEE Int. Electron Device Meet. Digest*, 2004.

[2.21] A. G. Dirks, R. A. M. Wolters, A. E. M. De Veirman, "Columnar Microstructures in Magnetron-Sputtered Refractory Metal Thin Films of Tungsten, Molybdenum and W-Ti-(N)," *Thin Solid Films*, vol. 208, pp. 181-188, 1992.

[2.22] R. Beyers, "Thermodynamic Considerations in Refractory Metal-Silicon-Oxygen Systems," *J. Appl. Phys.*, vol. 56, no. 1, pp. 147-152, 1984.

[2.23] Q. Lu, R. Lin, P. Ranade, Y. C. Yeo, X. Meng, H. Takeuchi, T.-J. King, C. Hu, H. Luan, S. Lee, W. Bai, C.-H. Lee, D.-L. Kwong, X. Guo, X. Wang, and T.-P. Ma, "Molybdenum Metal Gate MOS Technology for Post-Sio_2 Gate Dielectrics," in *Int. Elec. Dev. Meet. Digest*, pp. 641-644, 2000.

[2.24] J. Schaefeer, S. Samavedam, L. Fonseca, C. Capasso, O. Adetutu, D. Gilmer, C. Hobbs, E. Luckowski, R. Gregory, Z.-X. Jiang, Y. Liang, K. Moore, D. Roan, B.-Y. Nguyen, P. Tobin, B. White, "Investigation of Metal Gate Electrodes on HfO_2 Gate Dielectrics," in *Proc. Mat. Res. Symp.*, vol. 811, pp. 137-148, 2004.

[2.25] T. Fuyuki, T. Furukawa, T. Oka, and H. Matsunami, "Deposition of High-Quality Silicon Dioxide by Remote Plasma CVD Technique," *IEICE Trans. Electron.*, vol. E75-C, no. 9, pp. 1013-1018, 1992.

[2.26] P. E. Nicollian, W. R. Hunter, and J. C. Hu, "Experimental Evidence for Voltage Driven Breakdown Models in Ultrathin Gate Oxides," in *Int. Reliab. Phys. Symp.*, pp. 7-15, 2000.

[2.27] H. Takeuchi, M. She, K. Watanabe, and T.-J. King, "Damageless Sputter Deposition for Metal Gate CMOS Technology," in *61th Dev. Res. Conf.*, pp. 35-36, 2003.

[2.28] Y. Kuo, "Factors Affecting the Molybdenum Line Slope by Reactive Ion Etching," *J. Electrochem. Soc.*, vol. 137, no. 6, pp. 1907-1911, 1990.

[2.29] M. Schaepkens, and G. S. Oehrlein, "A Review of SiO_2 Etching Studies in Inductively Coupled Fluorocarbon Plasmas," *J. Electrochem. Soc.*, vol. 148, no. 3, pp. C211-C221, 2001.

[2.30] Y. Kurogi, and K. Kamimura, "Molybdenum Etching using CCl_4/O_2 Mixture Gas," *Jpn. J. Appl. Phys.*, vol. 21, no. 1, pp. 168-172, 1982.

[2.31] *CRC handbook of Chemistry and Physics (1985-1986)*, p. F-178, CRC Press, Inc., Boca Raton, FL, 1985.

[2.32] R. Smoluchowski, "Anisotropy of the Electronic Work Function of Metals," *Physical Rev.*, vol. 60, pp. 661-674, 1941.

[2.33] S. Berge, P. O. Gartland, and B. J. Slagsvold, "Photoelectric Work Function of a Molybdenum Single Crystal for the (100), (110), (111), (112), (114), and (332) Faces," *Surf. Sci.*, vol. 43, pp. 275 – 292, 1974.

[2.34] P. Ranade, "Advanced Gate Materials and Processes for Sub-70 nm CMOS Technology," *Ph.D Thesis*, University of California, Berkeley, 2002.

[2.35] R. J. P. Lander, J. C. Hooker, J. P. van Zijl, F. Roozeboom, M. P. M. Maas, Y. Tamminga, R.A.M. Wolters, "A Tunable Metal Gate Work Function using Solid State Diffusion of Nitrogen", in *Proc. European Solid-State Dev. Res. Conf.*, pp. 103-106, 2002.

[2.36] T. Amada, N. Maeda, and K. Shibahara, "Degradation in a Molybdenum Gate MOS Structure Caused by N+ Ion Implantation for the Work Function Control," in *Proc. Mater. Res. Soc. Symp.*, p.60, 2002.

[2.37] SRIM simulation (available at http://www.srim.org)

[2.38] Q. Lu, R. Lin, P. Ranade, T.-J. King, and C. Hu, "Metal Gate Work Function Adjustment for Future CMOS Technology," in *IEEE VLSI Tech. Symp. Digest*, pp. 45-46, 2001.

[2.39] G. Qi, W. M. Small, and T. Debroy, "Thermochemistry and Diffusion of Nitrogen in Solid Molybdenum", *Met. Trans. B*, v.22, p. 219, April 1991.

[2.40] J. H. Evans, and B.L. Eyre, "The Heat of Solution and Diffusivity of Nitrogen in Molybdenum," *Acta Metallurgica*, vol. 17, no. 8, pp. 1109-1115, 1969.

[2.41] K. T. Ho, M.-A. Nicolet, and D. M. Scott, "Effects of Ion-Implanted Nitrogen Impurities on Molybdenum Silicide Formation," *Thin Solid Films*, vol. 127, pp. 171-179, 1985.

[2.42] B.D. Cullity, and S.R. Stock, *Elements of X-Ray Diffraction*, 3rd Edit., Prentice Hall, Inc., 2001.

[2.43] P. Hones, N. Martin, M. Regula, and F. Levy, "Structural and Mechanical Properties of Chromium Nitride, Molybdenum Nitride, and Tungsten Nitride Thin Films," *J. Phys. D: Appl. Phys.*, vol. 36, pp. 1023-1029, 2003.

Chapter 3

High-*k* Gate Dielectric Technology

3.1 Introduction

Over the past several decades, the successful improvement in CMOS transistor performance and integration of ultra-large scale (ULSI) semiconductor devices has relied on scaling down the silicon dioxide (SiO_2) or its derivatives (SiO_xN_y) gate dielectric. The advantage of primary reasons are that thermally grown amorphous SiO_2 dielectric are low fixed charge densities (Q_f) on the order of $q10^{10}$ cm^{-2}, mid-gap interface state densities (Q_{it}) of ~$q10^{10}$ cm^{-2} and a large breakdown electric field over 10 MV/cm [3.1]. Thinner gate oxide increases the drive current of transistors by increasing the areal gate

capacitance and suppresses short channel effects by providing strong gate control of the channel potential.

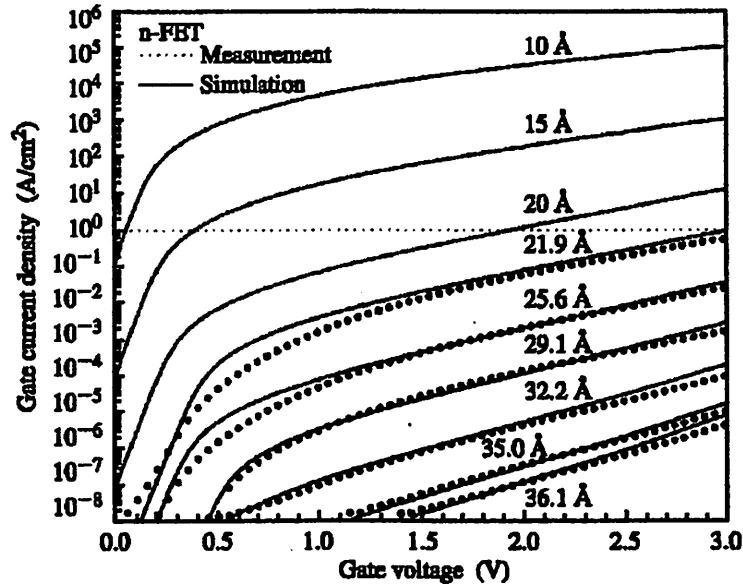


Figure 3.1 Measured and simulated I_G-V_G characteristics under inversion conditions of n-channel MOSFETs. The dotted line is indicates the 1 A/cm^2 limit for gate leakage current [3.2]

However, silicon dioxide is not attractive as a gate dielectric when its thickness approaches 1 nm; one of the fundamental issues for scaling of the gate dielectric thickness is the exponential increase in direct tunneling current with decreasing SiO_2 thickness. For example, gate leakage current density can rise to 0.1 – 10 A/cm^2 at 1.0 V gate voltage for 1.5 – 2 nm thick SiO_2, as shown in **Figure 3.1** [3.2] This high current can affect the circuit operations and dissipate power. Even though high power

dissipation may be tolerable for high-performance micro-processor applications, this will lead to serious problems for low-power portable applications. Theoretical modeling studies of the SiO_2/Si interface predicted that the physical thickness of SiO_2 will be fundamentally limited to 0.7 nm due to the overlap of Si-rich interface regions from the silicon channel and the poly-silicon gate, causing an effective electrical short through the dielectric [3.3]. However, the practical scaling limit of SiO_2 as the gate dielectric will be 1.2 nm mainly due to interface roughness, degraded transistor performance, dielectric reliability, etc. [3.4, 3.5, 3.6].

The reduction of the gate leakage current density is, therefore, the most compelling reason for replacing SiO_2-based dielectrics. For a given CMOS technology generation, devices are designed with a specific areal gate capacitance, which is a function of the dielectric constant (k) and physical thickness (T_{ox}). In order to decrease the leakage current while maintaining the same gate capacitance (or equivalent oxide thickness, *EOT*), a thicker film with a higher dielectric constant should be adopted. Many materials appear favorable as an alternative gate dielectric, but very few materials

are promising with respect to the key basic material properties, compatibility with CMOS processes and integration, as will be discussed in the following section.

3.2 Material Selection for Gate Dielectric

Several materials have been investigated for replacing silicon dioxide or silicon nitride as the gate dielectric for sub-65nm CMOS technology generations [3.7]; these include the simple metal oxides such as tantalum oxide (Ta_2O_5) [3.8], titanium oxide (TiO_2) [3.9], lanthanum oxide (La_2O_3) [3.10], yttrium oxide (Y_2O_3) [3.11], cerium oxide (CeO_2) [3.12], aluminum oxide (Al_2O_3) [3.13], zirconium oxide (ZrO_2) [3.14], and hafnium oxide (HfO_2) [3.15, 3.16], and the ferroelectric materials such as barium strontium titanate (BST) [3.17]. As a promising candidate gate dielectric, however, the new materials should demonstrate the key basic material properties including high permittivity (or dielectric constant), large potential barrier heights to prevent tunneling current, thermodynamic stability in contact with silicon, good interface quality and film morphology [3.18]. In addition, the high-k dielectric should be compatible with the gate electrode material(s) and CMOS process integration without compromising device reliability and circuit performance [3.19].

To minimize the gate tunneling current, it seems reasonable to adopt a material whose dielectric constant (*k*) is as high as possible, allowing an increase in the high-*k* film thickness for the same SiO_2 equivalent oxide thickness. However, if the high-*k* dielectric thickness approaches the gate length, fringing fields from source/drain regions to the channel becomes significant, resulting in weak control over the channel potential, hence compromising short channel behavior; this is the so called fringing-induced-barrier-lowering (FIBL) effect [3.20]. Intensive simulation study [3.21] predicted that

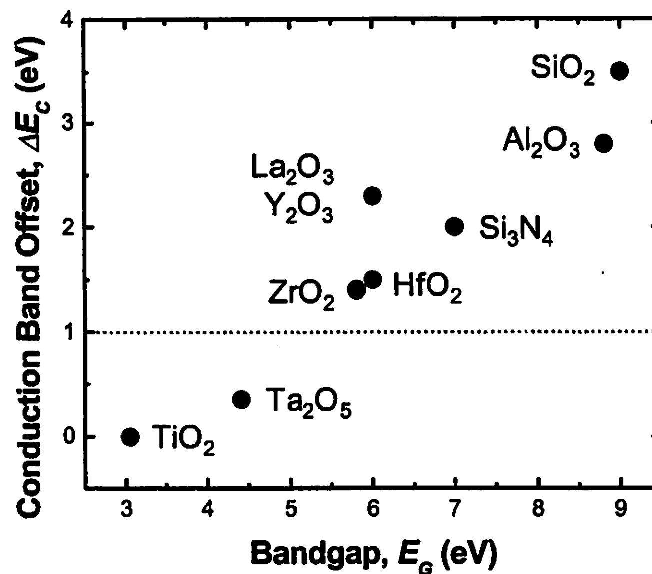


Figure 3.2 Theoretically calculated conduction band barrier height (ΔE_C) *vs.* energy bandgap (E_G). In general, a larger bandgap leads to a larger conduction band barrier height [3.3].

when the ratio of dielectric thickness to gate length (T_{ox}/L_G) is great than 1/5, more than 10% degradation in subthreshold swing occurs, ruling out the use of very high-*k* (> 40) materials such as TiO_2 and BST.

Together with the high dielectric constant, the conduction barrier height (ΔE_C) should be high enough to prevent a significant tunneling current because both the thickness and height of the barrier have an exponential influence upon the tunneling leakage current. Barrier heights have been theoretically calculated for several potential high-k materials [3.22]. In general, a larger bandgap (E_G) leads to a larger conduction band offset (ΔE_C), as shown in **Figure 3.2**. However, for most high-*k* dielectrics, the bandgap is inversely proportional to the dielectric constant [3.23]. Hence, even if there is a significant reduction of tunneling leakage current due to the increased thickness, this may be compensated by the reduction of the bandgap, or barrier height. Therefore, a high-*k* dielectric, whose conduction band offset (ΔE_C) is smaller than 1.0 eV, may not replace the silicon dioxide [3.22]. Identifying a dielectric that provides even a moderate increase in dielectric constant, but that also produces a sufficiently large tunneling barrier height is indispensable. La_2O_3, Y_2O_3, ZrO_2, and HfO_2 offer relatively high dielectric constant and conduction band-offset.

For very thin gate dielectrics, the interface with silicon determines the overall electrical properties. Thermodynamic stability in direct contact with silicon during CMOS fabrication processes is therefore indispensable [3.24]. Most high-*k* metal oxides including Ta_2O_5 and TiO_2 are not thermally stable on silicon; reacting with silicon to form an undesirable SiO_2 or medium-*k* interfacial layer, or metal silicide [3.25, 3.26], as shown in **Figure 3.3**. The underlying SiO_2 or interfacial layer limits the scaling of the equivalent oxide thickness (EOT). For example, if 1.5 nm EOT is required and 1.0 nm SiO_2 is formed at the interface, only 0.5 nm remains for the high-k material, making the use of high-*k* material ineffective due to the significant increase in tunneling leakage

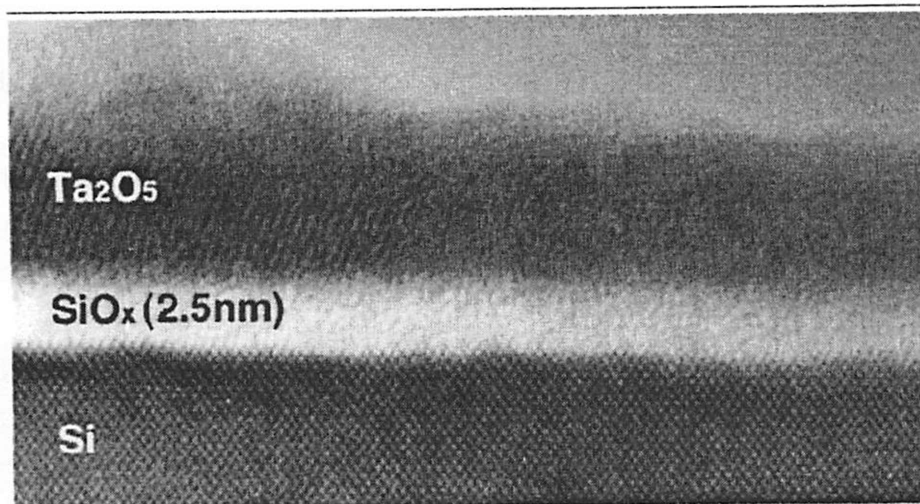


Figure 3.3 An example of thermodynamic instability of Ta_2O_5 in direct contact with silicon. A reaction at the interface results in the formation of an undesirable thin SiO_2 layer [3.26]

current, as illustrated in **Figure 3.4**.

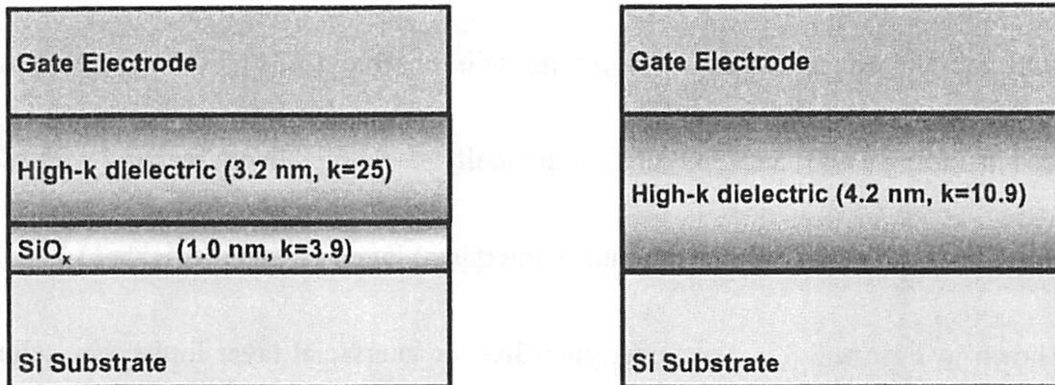


Figure 3.4 Comparison of stacked gate dielectric and single layer gate dielectrics in transistor. Both gate dielectrics result in the same equivalent oxide thickness, *EOT* = 1.5 nm. Ultimate scaling of *EOT* can be limited due to the interface layer formation.

Glassy phase (amorphous) gate dielectrics during CMOS fabrication are very desirable, because they will have isotropic electrical properties and not have grain boundaries, which typically serve as leakage current paths [3.18]. In addition, grain size and orientation changes lead to significant variations in dielectric constant. However, nearly all metal oxides under investigation form polycrystalline films upon source/drain annealing, which may necessitate an intentionally grown amorphous interfacial layer to reduce the leakage current. It is worthwhile to note that despite relatively low dielectric

constant (9~15), Al_2O_3 [3.27], $ZrSi_xO_y$ [3.28] and $HfSi_xO_y$ [3.29] appears promising because their morphology remains amorphous during high temperature annealing.

Low midgap interface state density (Q_{it}) and fixed charge density (Q_f) are crucial to meet the performance requirements of nanoscale CMOS transistors; channel carrier mobilities, threshold voltage shift, and subthreshold swing can be greatly affected. This will lead to the need for a sufficiently high quality interface with the silicon channel, challenging for high-*k* dielectrics as compared to SiO_2 [3.19].

Thus, it may be appropriate to replace SiO_2 gate dielectric with a material which provides only moderate increase (15 – 30) in dielectric constant, but also provides a large tunneling barrier height (> 1.0 eV) and high-quality (Q_{it}, $Q_f < 10^{11}$ cm^{-2}) interface to the silicon channel.

3.3 HfO_2 Gate Dielectric

Hafnium dioxide (HfO_2) has shown much promise as a candidate to replace SiO_2, as discussed in Chapter 3.2; it has a high dielectric constant (k ~ 25) with the bandgap of 5.7 eV, large energy-band offsets (ΔE_C ~ 1.5 eV), thermodynamic stability in direct contact with silicon substrate, and negligible frequency dispersion [3.22, 3.30, 3.31,

3.32]. For the gate electrode, polycrystalline silicon (poly-Si) has been the preferred material because it offers simplicity of process integration. However, when poly-Si is used as the gate material together with HfO_2 as the gate dielectric, increases in equivalent oxide thickness (EOT) and gate leakage current can result upon high-temperature annealing (*e.g.* during source/drain dopant activation) due to interfacial layer formation at the HfO_2/Si interface [3.33]. Recently, polycrystalline silicon-germanium (poly-SiGe) has received much attention as an alternative gate-electrode material, because it alleviates gate depletion and boron penetration issues, and yields thinner EOT for HfO_2 gate dielectric [3.34, 3.35, 3.36].

3.3.1 Fabrication of HfO_2 MOS Capacitors

MOS capacitors were fabricated on epitaxially grown silicon (p-type dopant concentration (N_A) below 10^{15} cm^{-3}) on heavily doped p+ silicon wafers. **Figure 3.5** summarizes the fabrication sequences for HfO_2 MOS capacitors. 100 nm thick SiO_2 was thermally grown in wet oxidation furnace at 950°C and patterned to define the device active regions. Pure Hf was then deposited by DC magnetron sputtering at 300°C and 210 W power (base pressure of 5×10^{-8} Torr), and rapid thermal annealing at 700°C, 30s in

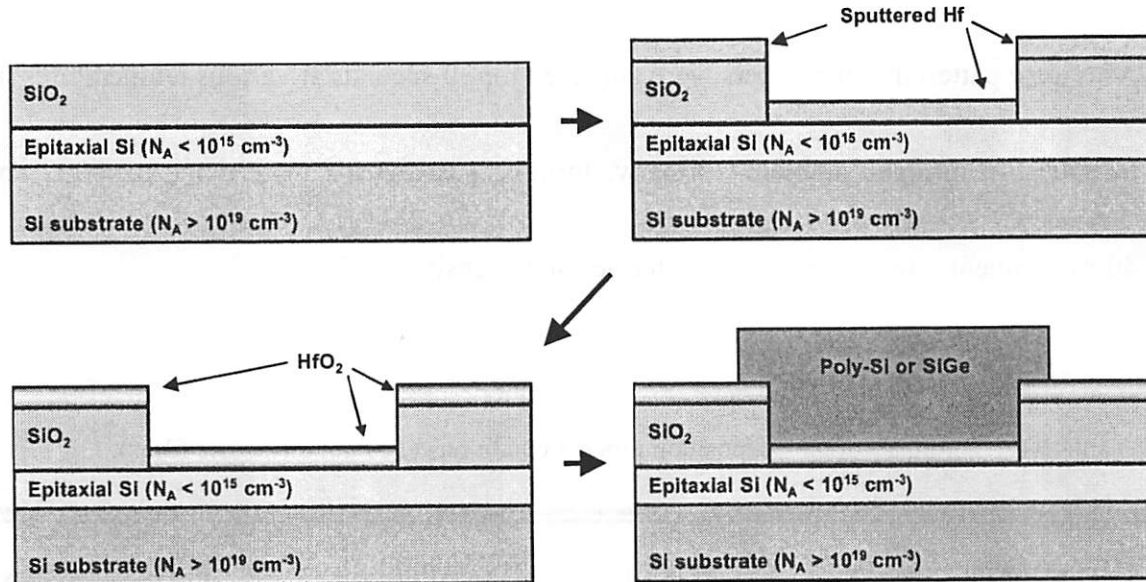


Figure 3.5 Fabrication sequences for HfO_2 gate dielectric MOS capacitors.

oxygen ambient was used to form HfO_2. It is worth noting that the wafers were precleaned in a diluted HF solution to remove the chemical oxide and no intentional interfacial layer was grown before HfO_2 formation. Afterwards, the gate electrode materials (either poly-Si or $Si_{0.75}Ge_{0.25}$) were deposited in a conventional low-pressure chemical vapor deposition (LPCVD) furnace at 550°C, using either SiH_4 or Si_2H_6 as the gaseous Si source, and GeH_4 as the gaseous Ge source. In order to minimize gate depletion, all the gate films were *in-situ* n+ doped using phosphine (PH_3). The gate deposition conditions are summarized in **Table 3.1**. Shorter deposition times were used

for poly-$Si_{0.75}Ge_{0.25}$ and Si_2H_6–based poly-Si in order to achieve the same film thickness. After gate patterning, the wafers were annealed for 30 seconds at various temperatures up to 950°C in nitrogen ambient. Finally, forming gas anneals were done at 600°C and 400°C sequentially to improve the interface state density [3.37].

Table 3.1 Summary of gate deposition process conditions (100 nm thick gate films).

Gate material	Poly-Si	Poly-Si	Poly-$Si_{0.75}Ge_{0.25}$
Precursor gas	SiH_4	Si_2H_6	$SiH_4 + GeH_4$
Deposition temperature	550°C	550°C	550°C
Deposition time	270 min	7.5 min	54 min

3.3.2 *Experimental Results and Discussion*

Figure 3.6 shows the measured high-frequency *C-V* characteristics of the HfO_2 capacitors. For the poly-Si gated capacitors, the capacitance decreases with increasing the subsequent annealing temperature. This is more pronounced for SiH_4-based poly-Si

gated capacitors (ΔEOT = 1.3nm) compared to Si_2H_6-based poly-Si gated capacitors (ΔEOT = 0.65nm).

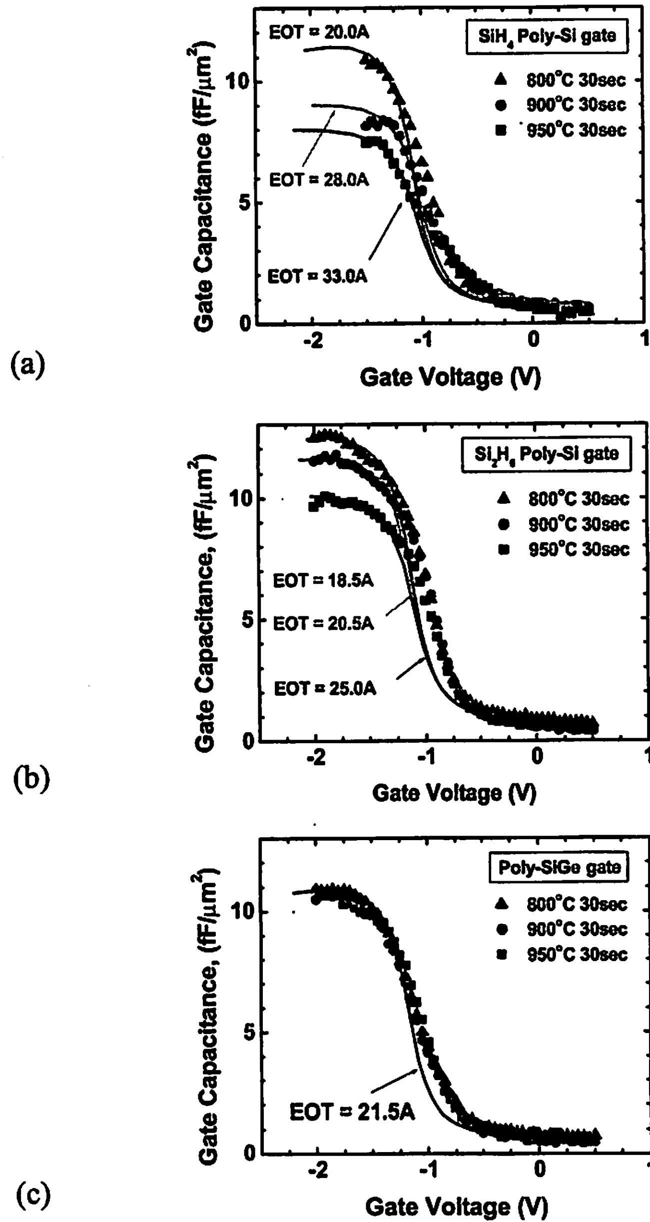


Figure 3.6 High-frequency (100 KHz) C-V curves for HfO_2 MOS capacitors with (a) poly-Si gate deposited using SiH_4, (b) poly-Si gate deposited using Si_2H_6, and (c) poly-$Si_{0.75}Ge_{0.25}$ gate. The solid lines shown were obtained from quantum-mechanical simulation and used to extract the EOT values as indicated.

These results indicate that a reduction in the gate deposition time is helpful to prevent increases in EOT with high-temperature annealing. However, for poly-SiGe gated capacitors, negligible change in capacitance ($\Delta EOT \cong 0$) was observed for annealing temperatures up to 950°C. This result can only be partially attributed to the reduced gate deposition time (refer to Table 3.1).

Figure 3.7 shows the measured leakage current characteristics of the HfO_2 capacitors. The leakage current for SiH_4-based poly-Si capacitors is much larger than that of Si_2H_6-based poly-Si capacitors. This indicates that reduction of thermal budget in gate deposition is very effective for reducing leakage current through the HfO_2 gate dielectric. It is worthwhile to note that the leakage current increases with annealing temperature, *i.e.*, thicker EOT. Both *C-V* and *I-V* measurements show that poly-Si as a gate material yields a thicker EOT with higher leakage current for HfO_2 gate dielectric, as compared with poly-$Si_{0.75}Ge_{0.25}$. These results cannot be explained simply by the formation of an interfacial layer.

In order to elucidate the leakage mechanism, the dependence of gate leakage current on temperature was investigated for HfO_2 capacitors with either SiH_4-based poly-Si or poly-SiGe gate material, as shown in **Figure 3.8**. The leakage current shows an

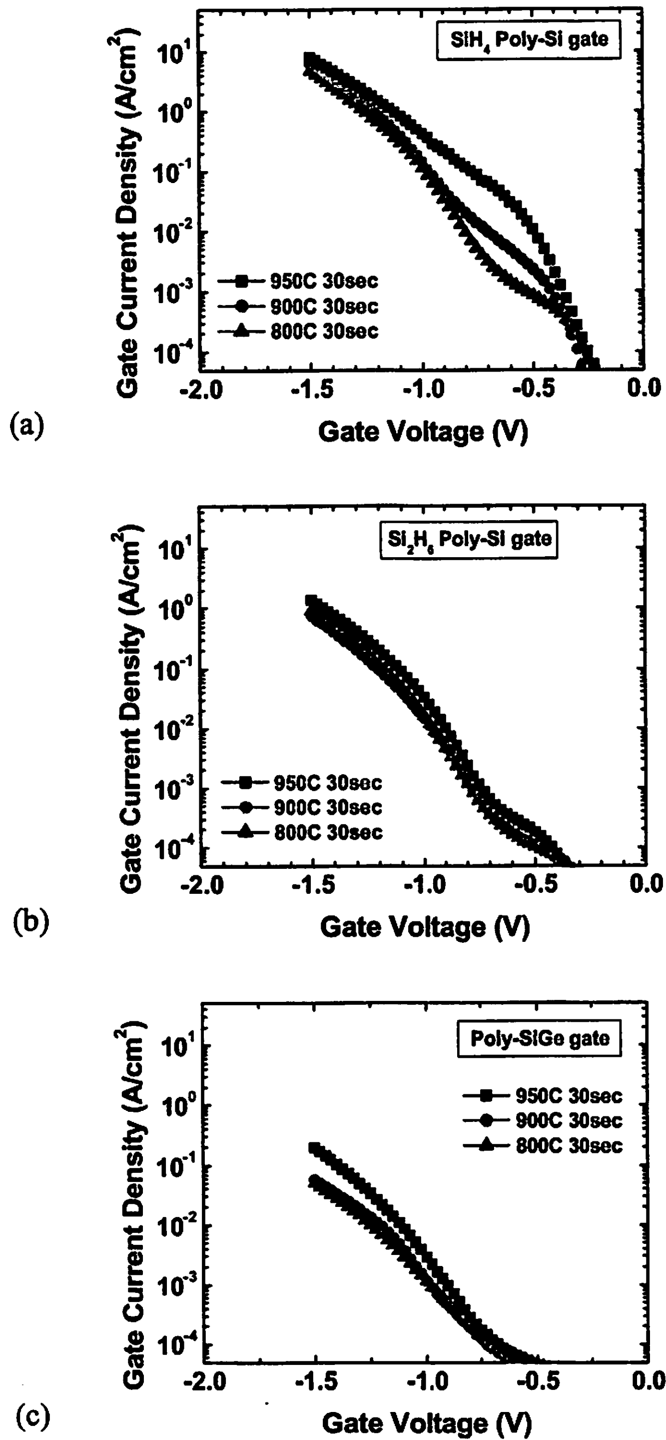


Figure 3.7 Gate leakage current characteristics of HfO_2 MOS capacitors with (a) poly-Si gate deposited using SiH_4, (b) poly-Si gate deposited using Si_2H_6, and (c) poly-SiGe gate.

exponential dependence on voltage and temperature, which corresponds to Frenkel-Poole emission [3.38]. From the characteristic slope for different gate voltages from −1.0V to −1.5V, the trap energy level in HfO_2 can be extracted. Since the same trap energy level can be seen for each gate material, and the poly-SiGe gated capacitors exhibit ~100 times lower leakage current, it is concluded that the HfO_2 defect density is lower for poly-SiGe gate material.

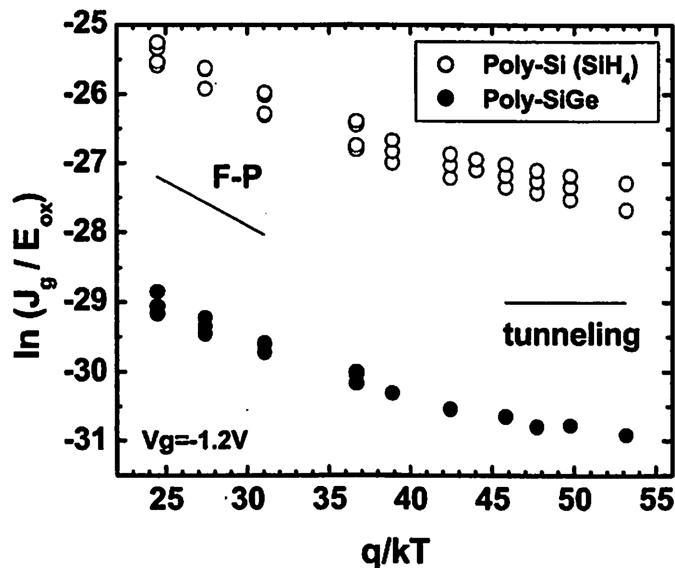


Figure 3.8 Leakage current *vs*. temperature for HfO_2 MOS capacitors with either poly-Si gate deposited using SiH_4, or poly-SiGe. The devices were annealed at 900°C.

Figure 3.9 shows the cross-sectional transmission electron microscopy (XTEM), which reveals that a bottom interfacial layer exists at the HfO_2/Si interface before and

after high-temperature annealing for both poly-Si and poly-SiGe gate materials. This interfacial layer was likely formed during the Hf oxidation process due to excessive oxidation. Thus, the increase in leakage current upon high-temperature annealing cannot be attributed to the bottom interfacial layer.

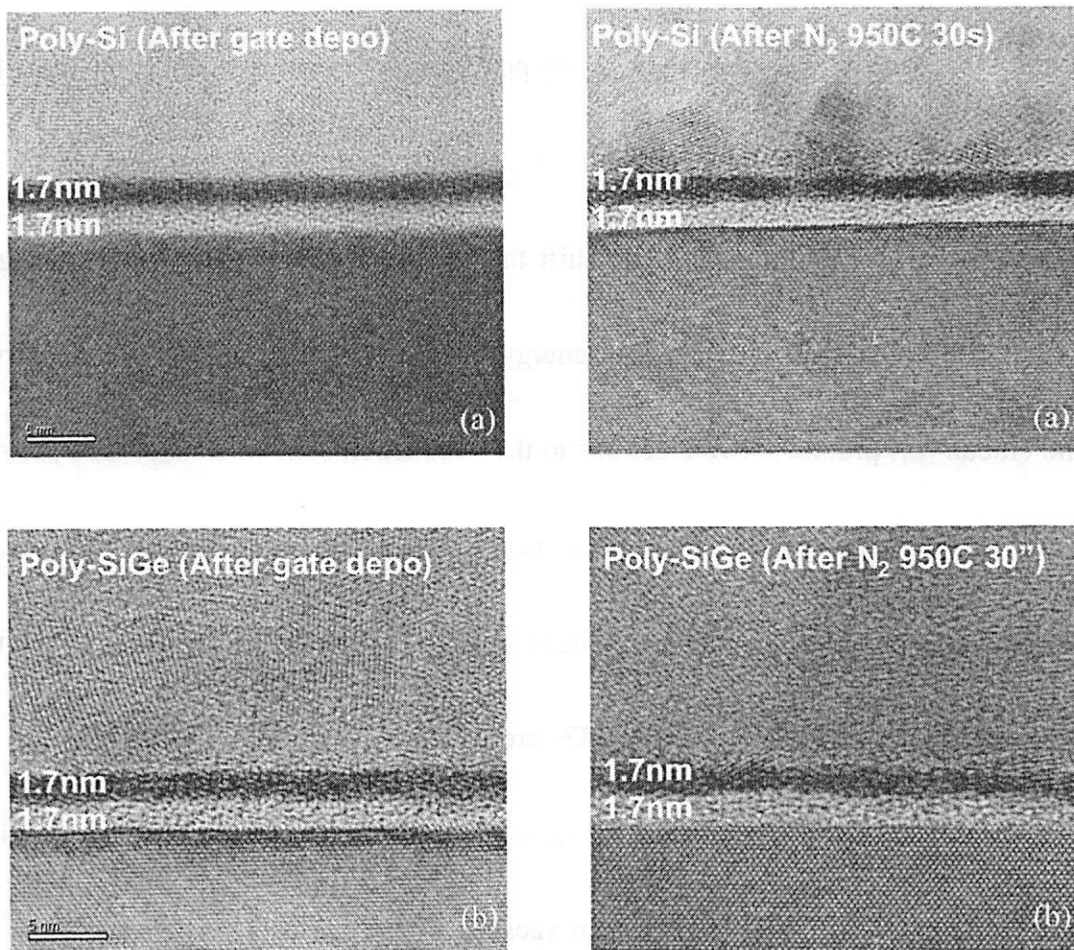


Figure 3.9 Cross-sectional transmission electron microscopy (X-TEM) for HfO_2 gate stacks annealed at 950°C with (a) poly-Si and (b) poly-SiGe gates. Bottom interface layer exists at the HfO_2/Si interface before and after high-temperature annealing.

On the other hand, at the top interface between the HfO_2 and the gate electrode, the formation of an interfacial film upon annealing was observed. Although it has been predicted to be thermodynamically stable in direct contact with silicon [3.39], HfO_2 readily forms an interfacial silicate layer; the reaction $HfO_2 + Si \rightarrow Hf + SiO_2$ does not seem likely to occur, since the Gibbs free energy change is positive ($\Delta G = +1.14$ eV at 1000K). However, a recent study [3.40] pointed out that oxygen transport from HfO_2 into Si generates conduction electrons in the HfO_2, and the energy supplied by their transition to lower energy states can shift the overall ΔG to negative values. **Figures 3.10** illustrate the sequence using an energy band diagram. Transport of oxygen (O) into silicon (Si) promotes two electrons to the conduction band in HfO_2. The promoted electrons then fall into available lower-energy states: the unoccupied oxygen vacancy (V_O) level in HfO_2 and the conduction band in Si. The energy difference between these states and the conduction band of HfO_2 are –1.2 eV and –1.5 eV, respectively. The electron transfer results in a charge dipole at the oxide/Si interface as depicted in **Figure 3.10 (b)**. Transport of O (i.e., oxygen vacancy formation inside HfO_2) continues until the electrostatic dipole energy balances the effective reaction energy. Hence, interfacial silicate layer formation is thermodynamically driven and imposes thermal process

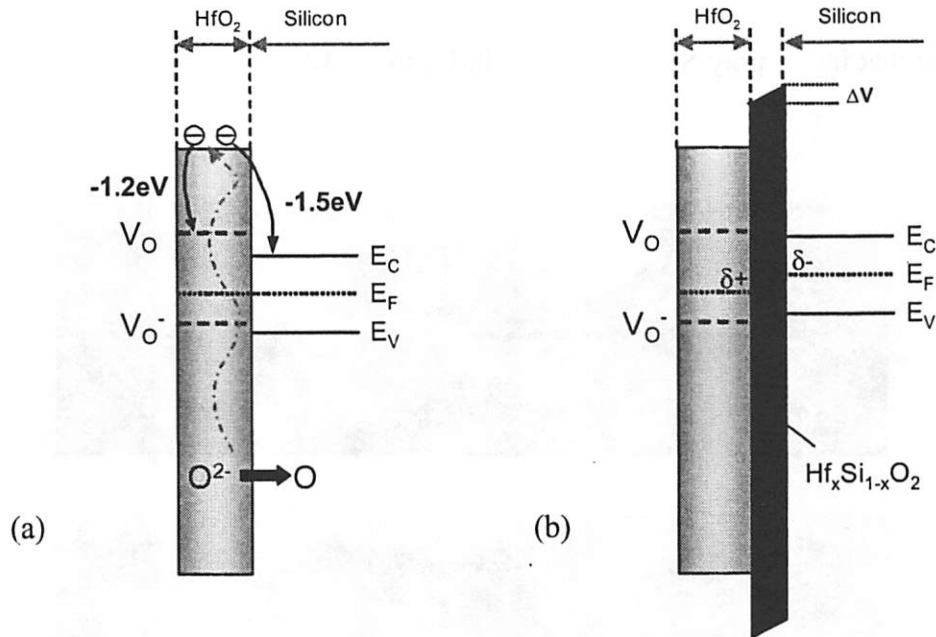


Figure 3.10 (a) Electron transfer resulting from oxygen transport across the interface. Two electrons promoted to E_C in HfO_2 fall to unoccupied states, Vo in HfO_2 and E_C in the silicon substrate. (b) an interfacial silicate layer and potential drop is formed.

constraints for HfO_2 on Si. It is interesting to note that 0.2 V potential drop has been observed by x-ray photoelectron spectroscopy (XPS) [3.41]. In contrast, high-k dielectrics in contact with Ge do not form interfacial layers because of the larger *ΔG* for GeO_2 formation [3.42].

Figure 3.11 shows that the density of this interfacial layer is much higher for poly-Si gate capacitors after 950°C 30s RTA in nitrogen ambient. From compositional analyses using energy dispersive x-ray spectrometry (EDX), it was found that both

oxygen (O) and hafnium (Hf) concentration inside poly-Si near the top interface is much higher that that inside poly-SiGe, as shown in **Figure 3.12**.

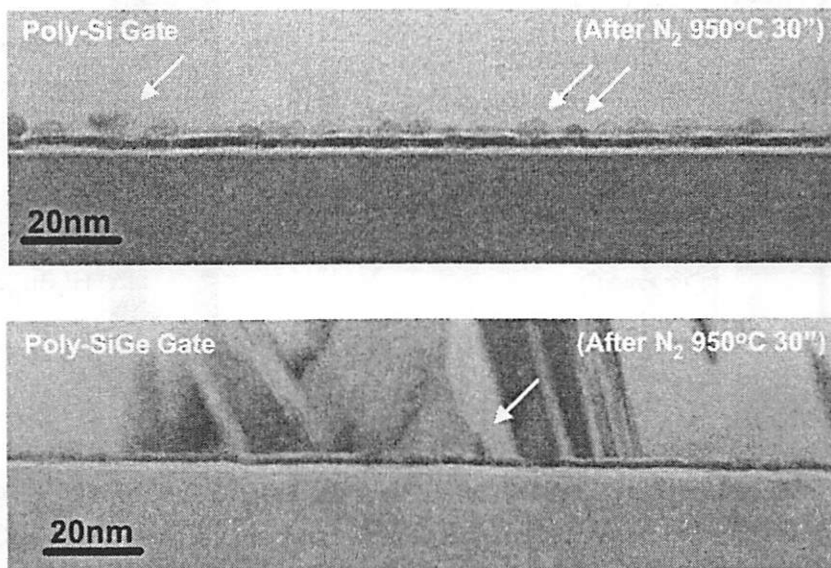


Figure 3.11 Cross-sectional transmission electron microscopy (X-TEM) for HfO_2 gate stacks annealed at 950°C with (a) poly-Si and (b) poly-SiGe gates. Defect density at top interface layer for poly-Si gate is much higher than that for poly-SiGe gate.

Figure 3.13 shows the x-ray photoelectron spectroscopy (XPS) spectra of Hf 4f before and after amorphous Si deposition and after 950°C 30s RTA. The Hf 4f spectra did not exhibit an Hf-Si peak, indicating that no Hf silicide forms after 950°C 30s RTA. However, a +0.4 eV shift of the Hf-O peak was observed after silicon deposition; an additional +0.3 eV shift can be seen after 950°C 30s RTA. The positive shift of the Hf-

O peak is known to be caused by the second-neighbor effect due to Hf-O-Si formation [3.43]. These results indicate that the intermixing of Hf, Si, and O occurs during gate deposition and proceeds during subsequent thermal processing steps.

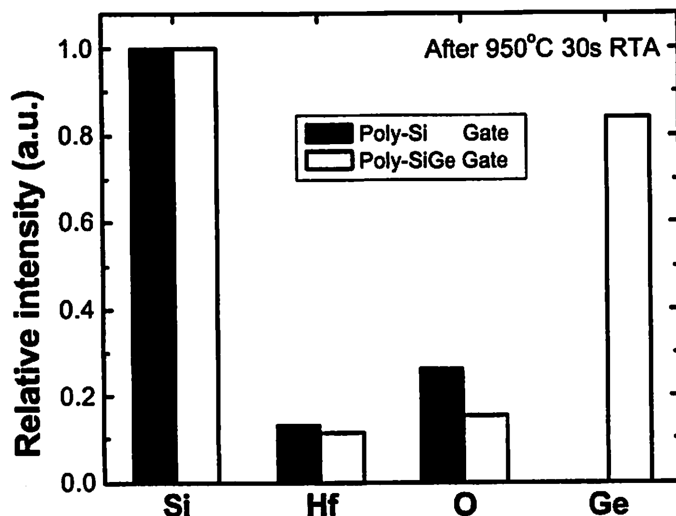


Figure 3.12 Comparison of relative intensity of energy dispersive X-ray spectrometry (EDX) analysis for gate/HfO_2 interface. The samples were annealed at 950°C 30s in N_2.

Detail experimental investigation on the impact of the oxidation process on an HfO_2 film [3.44] found that insufficiently oxidized Hf films are non-stoichiometric, and the origin for the extra absorption peak (defects) detected in spectroscopic ellisometry (SE) was attributed to the oxygen vacancies inside the HfO_2 films. It is worth noting that oxygen vacancies in metal oxides including ZrO_2 [3.45], TiO_2 [3.46], SnO_2 [3.47], and Ta_2O_5 [3.48] are known to induce electronic states in the band gap.

Therefore, the increases in EOT and gate leakage current with an increase in thermal process budget likely result from the formation of an Hf silicate layer at the top (gate electrode) interface and oxygen-vacancy-trap assisted tunneling through the HfO_2. Also, the smaller increases in EOT and gate leakage current with poly-SiGe gate compared to those with poly-Si gate can be attributed to reduced transport of oxygen into the poly-SiGe gate electrode, hence leading to less interfacial layer formation.

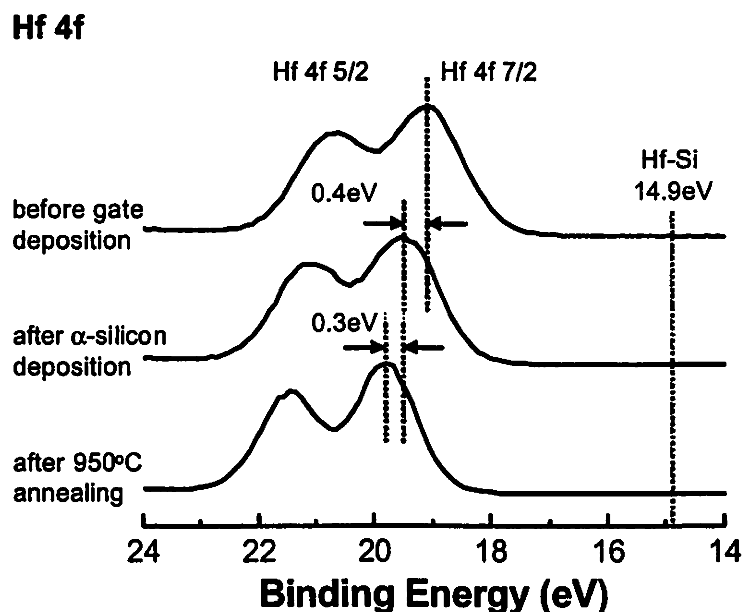


Figure 3.13 X-ray photoelectron spectroscopy (XPS) spectra of Hf 4f before and after amorphous Si deposition and after 950°C 30s RTA.

3.3.3 *Considerations for alternative gate electrode materials*

Successful integration of HfO_2 gate dielectric depends on the minimization of oxygen vacancy formation; a reduction in post gate deposition thermal process budget, and careful selection of the gate stack materials is therefore necessary. **Table 3.2** summarizes the heat of formation of oxide (E_{MOx}), vacuum work function ($\Phi_{M,vac}$), and effective reaction enthalpy (E_{eff}) for candidate gate electrode materials on HfO_2 [3.49]. Most of these elements are found to exhibit negative E_{eff}, and thus would suffer from the Fermi-level pinning effect on HfO_2 [3.50]. Cobalt (Co), palladium (Pd), and ruthenium (Ru) appear to be promising candidates for a PMOS gate electrode material. However, n+ doped germanium (Ge) is the only candidate with positive E_{eff} and low $\Phi_{M,vac}$ suitable for a NMOS gate electrode material. The relatively small shift in effective work function for Mo-gate as compared to p+ poly-Si gate can be expected by the difference in E_{eff} (-0.24 eV vs. -1.39eV). The addition of Al_2O_3 into HfO_2 seems to be effective not only for increasing thermal stability [3.43], but also for reducing the Fermi-level pinning effect at the poly-Si gate interface [3.40] due to the lower E_{MOx} of Al_2O_3 than HfO_2.

Table 3.2 Summary of estimated effective reaction enthalpy for oxygen transfer from HfO_2 to gate electrode [3.49].

Gate electrode material	Vacuum work function, $\Phi_{M,Vac}$ (eV)	Formation enthalpy of E_{MOX} (eV)*1	Effective enthalpy, E_{eff} (eV)*2
Al	4.06	-5.80 (Al_2O_3)	-2.57
Co	5.00	-1.65 (CoO)	0.65
Cr	4.50	-3.10 (CrO_2)	-0.31
Cu	4.48	-2.47 (CuO)	0.34
Ge	4.00*3	-3.01 (GeO_2)	0.28
Hf	3.90	-5.94 (HfO_2)	-2.55
Mo	4.95	-2.58 (MoO_3)	-0.24
Ni	5.04	-3.39 (Ni_2O_3)	-1.14
Pd	5.22	-0.89 (PdO)	1.19
Pt	5.64	-4.07 (PtO*4)	-2.41
Ru	4.71	-1.58 (RuO_2)	1.00
Si	4.05*3	-4.73 (SiO_2)	-1.49
Ta	4.15	-4.25 (Ta_2O_5)	-1.11
Ti	4.33	-4.90 (TiO_2)	-1.94
V	4.30	-6.44 (V_2O_5)	-3.45
W	4.55	-3.06 (WO_2)	-0.32
Zr	4.05	-7.62 (ZrO_2)	-4.38

*1 normalized by number of oxygen atom.

*2 calculated using the following formula: $E_{eff} = E_{MOx} - E_{HfO2} - 1.2eV - (1.5eV + \Phi_{M,Vac} - E_{C,Si})$.

*3 E_C is used for semiconductor materials.

*4 gaseous diatom bond enthalpy used.

3.4 Summary

This chapter reviewed the requirements for a high-k gate dielectric for future nanoscale CMOS technology generations. For hafnium oxide (HfO_2), the impact of gate process technology on equivalent-oxide-thickness and leakage current was investigated. Even though hafnium oxide (HfO_2) is one of the most promising candidates, successful integration of HfO_2 into CMOS fabrication depends on the minimization of oxygen vacancy formation through careful selection of the gate electrode materials, and reduction of post-gate-deposition thermal budget.

3.5 References

[3.1] M. L. Green, T. W. Sorsch, G. L. Timp, D. A. Muller, B. E. Weir, P. J. Silverman, S. V. Moccio, and Y. O. Kim, "Understanding the Limits of Ultrathin SiO_2 and Si-O-N Gate Dielectrics for sub-50 nm CMOS," *Microelectron. Eng.*, vol. 48, pp. 25-30, 1999.

[3.2] S.-H. Lo, D. A. Buchanan, and Y. Taur, "Modeling and Characterization of Quantization, Polysilicon Depletion, and Direct Tunneling Effects in MOSFETs with Ultrathin Oxides," *IBM J. Res. Develop.*, vol. 43, no. 3, pp. 327-337, 1999.

[3.3] S. Tang, R. M. Wallace, A. Seabaugh, and D. King-Smith, "Evaluating the Minimum Thickness of Gate Oxide on Silicon using First-Principles Method," *Appl. Surf. Sci.*, vol. 135, pp. 137-142, 1998.

[3.4] D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, "The Electronic Structure at the Atomic Scale of Ultrathin Gate Oxides," *Nature*, pp. 758-761, 1999.

[3.5] G. Timp, K. K. Bourdelle, J.F. Bower, F. H. Baumann, T. Boone, R. Cirelli, K. Evans-Lutterodt, J. Garno, A. Ghetti, H. Gossmann, M. Green, D. Jacobson, Y. Kim, R. Kleiman, F. Klemens, A. Kornblit, C. Lochstampfor, W. Mansfield, S Moccio, D.A. Muller, L. E. Ocola, M. I. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, D. M. Tennant, W. Timp, B.E. Weir, "Progress toward 10 nm CMOS Devices," in *Int. Elec. Dev. Meet. Digest*, pp. 615-618, 1998.

[3.6] D. A. Buchanan, "Scaling the Gate Dielectric: Materials, Integration, and Reliability," *IBM J. Res. Develop.*, vol. 43, no. 3, pp. 245-264, 1999.

[3.7] *International Technology Roadmap for Semiconductors*, Semiconductor Industry Association, 2003 (available at http://public.itrs.net).

[3.8] G. Q. Lo, D. L. Kwong, and S. Lee, "Metal-Oxide-Semiconductor Characteristics of Chemical Vapor Deposited Ta_2O_5 Films," *Appl. Phys. Lett.*, vol. 60, pp. 3286-3288, 1992.

[3.9] S. A. Campbell, D. C. Gilmer, X. C. Wang, M. T. Hsieh, H. S. Kim, W. Gladfelter, and J. Yan, "MOSFET Transistors Fabricated with High Permittivity TiO_2 Dielectrics," *IEEE Trans. Elec. Dev.*, vol. 44. pp. 104-109, 1997.

[3.10] A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, "High Quality La_2O_3 and Al_2O_3 Gate Dielectrics with EOT 5-10 Angstroms", in *IEEE VLSI Tech. Symp. Digest*, pp. 16-17, 2004.

[3.11] R. N. Sharma and A. C. Rastogi, "Structure and Composition of Interfacial Silicon Oxide Layer in Chemical Vapor Deposited Y_2O_3-SiO_2 Bilayer Dielectrics for Metal-Insulator-Semiconductor Devices," *J. Appl. Phys.*, vol. 76, pp. 4215-4224, 1994.

[3.12] T. Chikyow, S. M. Bedair, and *N.* A. El-Masry, "Reaction and Regrowth Control of CeO_2 on Si (111) Surface for the Silicon-on-Insulator Structure," *Appl. Phys. Lett.*, vol. 65, pp. 1030-1032, 1994.

[3.13] J. M. Hergenrother, G. D. Wilk, T. Nigam, F. P. Klemens, D. Monroe, P. J. Silverman, T. W. Sorsch, B. Busch, M. L. Green, M. R. Baker, T. Boone, M. K. Bude, N. A. Ciampa,E. J. Ferry, A. T. Fiory, S. J. Hillenius, D. C. Jacobson, R. W. Johnson, P. Kalavade, R. Keller, C. A. King, A. Kornblit, H. W. Krautter, J. T.-C. Lee, W. M. Mansfield, J. F. Miner, M. D. Morris, S.-H. Oh, J. M. Rosamilia, B. J. Sapjeta, K. Short, K. Steiner, D. A. Muller, P. M. Voyles, J. L. Grazul, E. Shero, M. E. Givens, C. Pomarede, M. Mazanec, C. Werkhoven, "50 nm Vertical Replacement-Gate nMOSFETs with ALD HfO_2 and Al_2O_3 Gate Dielectrics," in *Int. Elec. Dev. Meet. Digest*, pp. 51-54, 2001.

[3.14] T. S. Kalkur and Y. C. Lu, "Electrical Characteristics of ZrO_2-Based Metal-Insulator-Semiconductor Structures on p-Si," *Thin Solid Films*, vol. 207, pp. 193-196, 1992.

[3.15] C. T. Hsu, Y. K. Su, and M. Yokoyama, "High Dielectric Constant of RF-Sputtered HfO_2 Thin Films," *Jpn. J. Appl. Phys.* **31,** 2501 (1992).

[3.16] C. T. Kuo, R. Kwor, and K. M. Jones, "Study of Sputtered HfO_2 Thin Films on Silicon," *Thin Solid Films*, vol. 213, pp. 257-264, 1992.

[3.17] H. D. Chen, K. R. Udayakumar, and L. C. Niles, "Dielectric, Ferroelectric, and Piezoelectric Properties of Lead Zirconate Titanate Thick Films on Silicon Substrates," *J. Appl. Phys.*, vol. 77, pp. 3349-3353, 1995.

[3.18] G. D. Wilk, R. M. Wallace, and J. M. Anthony, "High-k gate dielectrics: Current status and materials properties considerations", *J. Applied Physic*s, vol. 89, no. 10, pp. 5243-5275, 2001.

[3.19] T. Schram, S. Bechx, S. De Gendt, J. Vertommen, and S. Lee, "Integrating High-k Dielectrics: Etched Polysilicon or Metal Gates?," *Solid-State Technol.*, pp. 61-63, June 2003.

[3.20] G. C. F. Yeap, and S. Krishnan, "Fringing-Induced Barrier Lowering (FIBL) in sub-100 nm MOSFETs with high-*k* Gate Dielectrics," *Electron. Lett.*, vol. 34, no. 11, pp. 1150-1152, 1998.

[3.21] B. Cheng, M. Cao, R. Rao, A. Inani, P. Vande Voorde, W. M. Greene, J. M. C. Stork, Z. Yu; P. M. Zeitzoff, J. C. S. Woo, "The impact of high-*k* gate dielectrics and metal gate electrodes on sub-100 nm MOSFETs," *IEEE Trans. Elec. Dev.*, vol. 46, no. 7, pp. 1537-1544, 1999.

[3.22] J. Robertson, "Band Offsets of Wide-Band-Gap Oxides and Implications for Future Electronic Devices," *J. Vac. Sci. Technol. B*, vol. 18, pp. 1785-1791, 2000.

[3.23] R. M. Wallace, and G. D. Wilk, "Identifying the Most Promising High-k Gate Dielectrics," Semicon. Internat., pp. 227-236, July 2001.

[3.24] P.S. Lysaght, P. J. Chen, R. Bergmann, T. Messina, R. W. Murto, H. R. Huff, "Experimental Observations of the Thermal Stability of High-*k* Gate Dielectric Materials on Silicon," *J. Non-Crystal. Sol.*, vol. 303, pp. 54-63, 2002.

[3.25] K. J. Hubbard, and D. G. Schlom, "Thermal Stability of Binary Oxides in Contact with Silicon," *J. Mater. Res.*, vol. 11, pp. 2757-2776, 1996.

[3.26] G. B. Alers, D. J. Werder, Y. Chabal, H. C. Lu, E. P. Gusev, E. Garfunkel, T. Gustafsson, and R. S. Urdahl, "Intermixing at the Tantalum Oxide/Silicon Interface in Gate Dielectric Structure," Appl. Phys. Lett., vol. 73, pp. 1517-1519, 1998.

[3.27] A. Chin, "Device and Reliability of High-*k* Al_2O_3 Gate Dielectric with Good Mobility and Low D_{it}," in *IEEE VLSI Tech. Symp. Digest*, pp. 135-136, 1999.

[3.28] J. Kim, and K. Yong, "Characterization of Zirconium Silicate Gate Dielectrics Deposited on Si(100) using $Zr(NEt_2)_4$ and $Si(O^nBu)_4$" *Electrchem. Solid-State Lett.*, vol. 7, pp. F35-F37, 2004.

[3.29] H. Watanabe, M. Saitoh, N. Ikarashi, "High-Quality $Hfsi_xo_y$ Gate Dielectrics Fabricated By Solid Phase Interface Reaction Between Physical-Vapor-Deposited Metal–Hf And SiO_2 Underlayer," *Appl. Phys. Lett.*, vol. 85, no. 3, pp. 449-451, 2004.

[3.30] M. Balog, M. Schieber, M. Michman, and S. Patai, "Chemical Vapor Deposition and Characterization of HfO_2 Films from Organo-Hafnium Compounds," *Thin Solid Films*, vol. 41, pp. 247-259, 1977.

[3.31] B. H. Lee, L. Kang, W.-J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, "Ultrathin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application," in *Int. Elec. Dev. Meet. Digest*, pp. 133-136, 1999.

[3.32] S. J. Lee, H. F. Luan, W. P. Bai, C. H. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "High Quality Ultra Thin CVD HfO_2 Gate Stack with Poly-Si Gate Electrode," in *Int. Elec. Dev. Meet. Digest*, pp. 31-34, 2000.

[3.33] L. Kang, K. Onishi, Y. Jeon, B.H. Lee, C. Kang, W.-J. Qi, R. Nieh, S. Gopalan, R. Choi, and J.C. Lee, "MOSFET Devices with Polysilicon on Sigle-Layer HfO_2 High-k Dielectrics," in *Int. Elec. Dev. Meet. Digest*, pp. 35-38, 2000.

[3.34] W. C. Lee, T.-J. King, and C. Hu, "Optimized Poly-$Si_{1-x}Ge_x$-Gate Technology for Dual Gate CMOS Application," in *IEEE VLSI Tech. Symp. Digest*, pp. 190-191, 1998.

[3.35] B. Tavel, F. Monsieur, P. Ribot, and T. Skotnicki, "Investigations on Poly-SiGe Gate in Full 0.1μm CMOS Integration," in *Proc. European Solid-State Dev. Res. Conf.*, pp. 127-130, 2002.

[3.36] Q. Lu, H. Takeuchi, X. Meng, T.-J. King, C. Hu, K. Onishi, H.-J. Cho, and J. Lee, "Improved Performance of Ultra-Thin HfO_2 CMOSFETs using Poly-SiGe Gate," in *IEEE VLSI Tech. Symp. Digest*, pp. 86-87, 2002.

[3.37] K. Onishi, C.S. Kang, R. Choi, H.-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J.C. Lee, "Effects of High-Temperature Forming Gas Anneal on HfO_2 MOSFET Performance," in *IEEE VLSI Tech. Symp. Digest*, pp. 22-23, 2002.

[3.38] S.M. Sze, *Physics of Semiconductor Devices*, 2nd ed. (John Wiley & Sons, 1981), p.402.

[3.39] K. J. Hubbard, and D.G. Schlom "Thermal Stability of Binary Oxides in Contact with Silicon," *J. Mater. Res.*, vol. 11, pp. 2757-2776, 1996.

[3.40] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Kohno, T. Chikyo, H. Kitajima, and T. Arikado, "Physics in Fermi Level Pinning at the PolySi/Hf-based High-k Oxide Interface," in *IEEE VLSI Tech. Symp. Digest*, pp. 108-109, 2004.

[3.41] S. Miyazaki, "Characterization of high-k gate dielectric/silicon interfaces," *Appl. Surf. Sci.*, vol. 190, pp. 66-74, 2002.

[3.42] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, K. C. Saraswat, "Germanium MOS Capacitors Incorporating Ultrathin High-*k* Gate Dielectric, " *IEEE Elec. Dev. Lett.*, vol. 23, pp. 473-475, 2002.

[3.43] G. D. Wilk, M. L. Green, M.-Y. Ho, B. W. Busch, T. W. Sorsch, F. P. Klemens, B. Brijs, R. B. van Dover, A. Kornblit, T. Gustafsson, E. Garfunkel, S. Hillenius, D. Monroe, P. Kalavade, and J. M. Hergenrother, "Improved Film Growth and Flatband Voltage Control of ALD HfO_2 and Hf-Al-O with N^+ Poly-Si Gates using Chemical Oxides and Optimized Post-annealing," in *IEEE VLSI Tech. Symp. Digest*, pp. 88-89, 2002.

[3.44] H. Takeuchi, D. Ha, and T.-J. King, "Observation of Bulk HfO_2 Defects by Spectroscopic Ellipsometry," *J. Vac. Sci. Technol. A*, vol. 22, no. 4, pp. 1337-1341, 2004.

[3.45] C. Morant, A. Fernandez, A. R. Gonzalez-Elipe, L. Soriano, A. Stampfl, A. M. Bradshaw, and A. M. Sanz, "Electronic Structure of Stoichiometric and Ar^+-Bombarded ZrO_2 Determined by Resonant Photoemission," *Phys. Rev. B*, vol. 52, pp. 11711-11720, 1995.

[3.46] S. Munnix, and M. Schmeits, "Origin of Defect States on the Surface of TiO_2," *Phys. Rev. B*, vol. 31, pp. 3369-3371, 1985.

[3.47] J. M. Themlin, R. Sporken, J. Darville, R. Caudano, J. M. Gilles, and R. L. Johnson, "Resonant-Photoemission Study of SnO_2: Cationic Origin of the Defect Band-gap States," *Phys. Rev. B*, vol. 42, pp. 11914-11925, 1990.

[3.48] H. Sawada and K. Kawakami, "Electronic Structure of Oxygen Vacancy in Ta_2O_5," *J. Appl. Phys.*, vol. 86, pp. 956, 1999.

[3.49] H. Takeuchi, H. Y. Wong, D. Ha, and T.-J. King, "Impact of Oxygen Vacancies on High-*k* Gate Stack Engineering," to be appeared in *Int. Elec. Dev. Meet. Digest*, 2004.

[3.50] Y.-C. Yeo, P. Ranade, T.-J. King, and C. Hu, "Effects of High-*k* Gate Dielectric Materials on Metal and Silicon Gate Workfunctions," *IEEE Elec. Dev. Lett.*, vol. 23, no. 6, pp. 342-344, 2002.

Chapter 4

Advanced Transistor Structures

4.1 Introduction

The scaling of CMOS devices has been continued over many technology generations, leading to improvement in both circuit performance and packing density; according to the Moore's law, integrated circuit complexity would increase at a rate of roughly a factor of two per year [4.1]. The semiconductor industry has kept this trend over thirty years, mainly fueled with technological innovations. The design of MOSFET at smaller dimensions has been predominantly guided by the constant electric field scaling theory [4.2] and its variants [4.3]; without changing the basic transistor

structure, lateral dimension can be scaled down together with reduction in vertical dimension and operation voltage (V_{DD}), as illustrated in **Figure 4.1**.

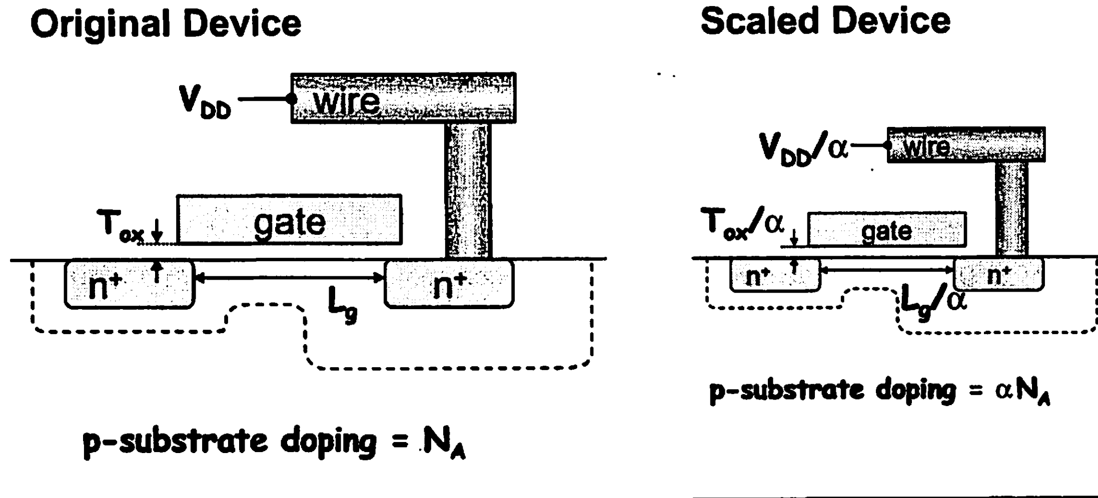


Figure 4.1 Schematic illustration of the constant electric field scaling theory of MOSFET devices [4.2].

To suppress the short channel effects, the channel potential in a MOSFET should be controlled by the gate electrode rather than the drain electrode; thus, the gate capacitance (C_g) should be larger than the drain capacitance (C_d). Otherwise, the characteristics of the MOSFET approach that of a resistor [4.3]. Traditionally, these issues have been successfully resolved by the reduction in gate oxide thickness (T_{ox}), channel depletion width (W_D) and source/drain junction depth (X_J). However, as the device dimensions

shrink down to nanometer scale regime, the integration of ever increasing number of devices without degrading yield, and reliability faces fundamental physics barriers.

The increase in gate capacitance can be achieved through thinning down the gate oxide thickness. However, there are fundamental limitation in SiO_2 vertical scaling due to the direct tunneling current as discussed in Chapter 3 [4.4, 4.5], and still remaining issues in the alternative high-*k* dielectrics such as threshold voltage instability and mobility degradation [4.6, 4.7, 4.56, 4.57].

The influence of drain field on the channel potential can be shielded through increasing the channel and/or localized halo doping concentration (*i.e.*, minimizing the depletion depth) [4.8]. However, the very thin depletion depths needed for the future nanoscale CMOS require very high body doping concentration, probably above $5\text{x}10^{18}$ cm^{-3} for sub-50 nm MOSFET. At these doping levels direct tunneling leakage current from body to drain is expected to become a serious problem [4.9]. The increased parasitic junction capacitance (C_J) and degraded channel carrier mobility can deteriorate the circuit performance. Furthermore, the fluctuations of device properties can be induced due to the random fluctuation of the placement and number of the dopant atoms [4.10]; this may limit the number of devices which can be integrated on a single chip,

because of the intolerable clock skews or malfunction of the circuits that depends on the matched or absolute values of device properties [4.9].

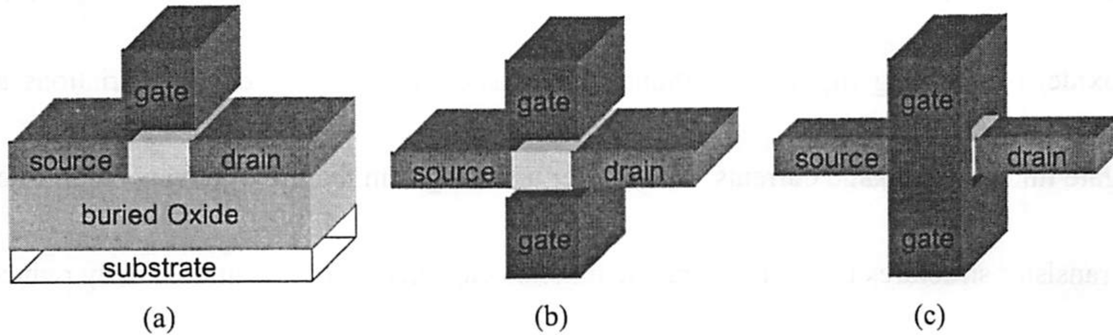


Figure 4.2 Advanced thin-body transistor structures; (a) ultra-thin body single gate (UTB) MOSFET, (b) double gate (DG) MOSFET, and (c) multiple gate (MG) MOSFET.

Alternative way to suppress the short channel effects without degrading the circuit performance is adopting the advanced thin-body transistor structures such as ultra-thin body single gate (UTB) MOSFET, double gate (DG) MOSFET, and multiple gate (MG) MOSFET, as shown in **Figure 4.2**; the use of an ultra-thin undoped silicon channel can effectively eliminate the off-state leakage current (I_{Off}) between source and drain. **Figure 4.3** illustrates the elimination of the silicon channel region whose potential is not well controlled by the gate electrode effectively suppresses the off-state leakage current; the buried oxide (BOX) prevents the channel potential from the drain field. The device parameters used for the 2-D device simulations [4.11] are 35 nm gate length (L_G), 2.0 nm

gate oxide thickness (T_{OX}), 1x10^{15} cm^{-3} channel doping concentration (N_A), 5 nm thick silicon body (T_{Si}) with 1.2 V operation voltage (V_{DD}). It should be noted that I_{Off} was quite well suppressed without using a heavy body doing and state-of-the-art thinner gate oxide, overcoming the aforementioned issues such as statistical dopant variations and gate tunneling leakage currents. The other advantages in the use of advanced thin-body transistor structures is that the parasitic junction capacitance (C_J) is dramatically reduced, and the source/drain junction depth (X_J) is naturally determined by the silicon body thickness (T_{Si}).

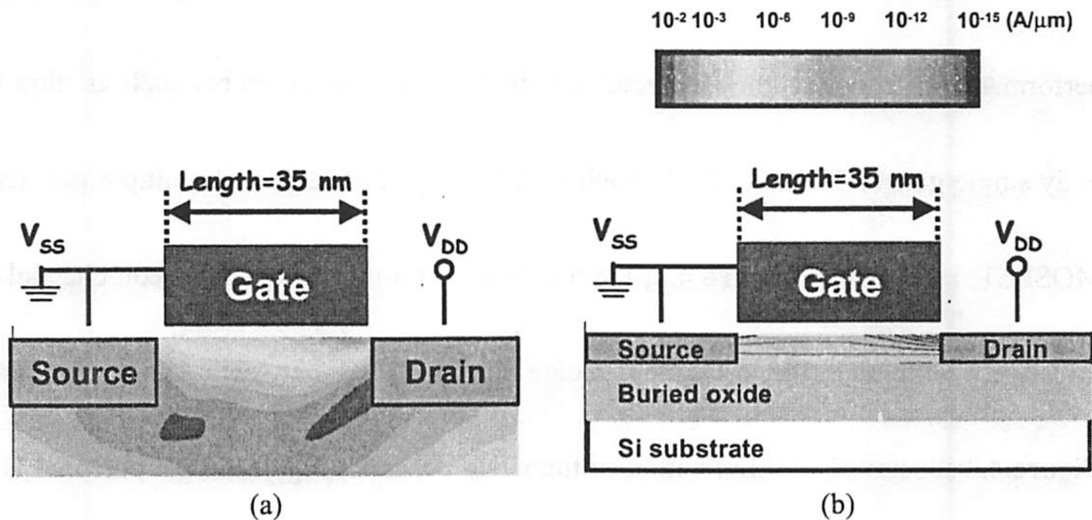


Figure 4.3 Comparison of leakage current density for (a) conventional MOSFEET, and (b) UTB MOSFET (V_{GS}=0V, V_{DS}=1.2V, L_G =35 nm, T_{ox}=2.0 nm, and N_A = 10^{15} cm^{-3}).

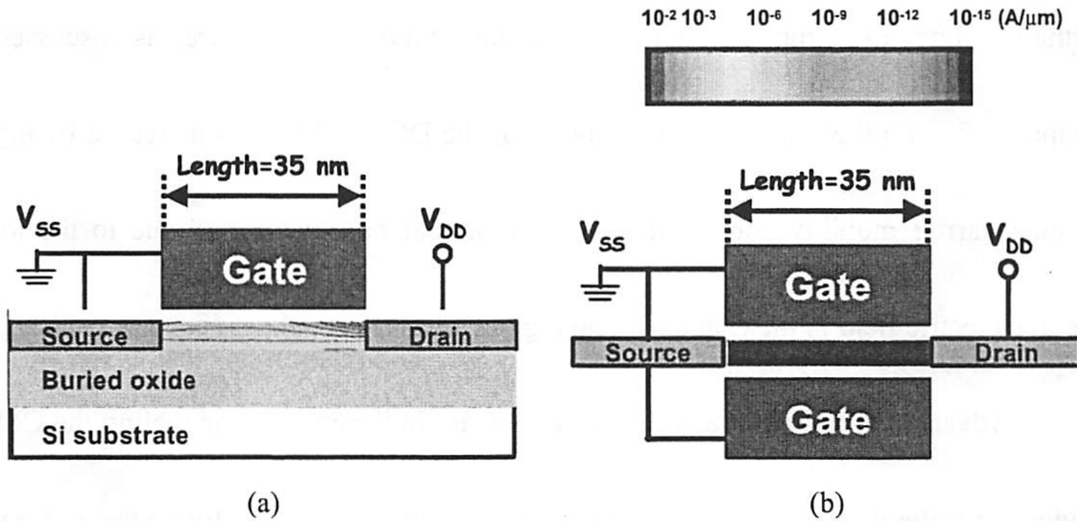


Figure 4.4 Comparison of leakage current density for (a) UTB MOSFET, and (b) double gate (DG) MOSFET (V_{GS}=0V, V_{DS}=1.2V, L_G =35 nm, T_{Si} = 5 nm, T_{ox}=2.0 nm, and N_A = 10^{15} cm^{-3}).

The double gate (DG) and multiple gate (MG) MOSFET has electrostatically much more robust control over the channel potential than the single-gated MOSFET, since two (or multiple) gates shields the channel potential from the drain field, suppressing the short channel effects, as shown in **Figure 4.4**. It is worth noting that the substrate with heavy channel doping for conventional MOSFET plays the identical role of the bottom shield, which results in a tradeoff between the degree of shielding and the reduction of the subthreshold swing [4.9]. However, such tradeoff does not exist for DG (or MG) MOSFETs, allowing the scalability of gate length down below sub-35 nm CMOS technology node [4.12]; DG MOSFET structures enable approximately 2 times

further scaling, as compared to the single gate MOSFET structure, as discussed in Chapter 4.2. Furthermore, the performance of the DG MOSFET is increased by higher channel carrier mobility compared to a conventional bulk MOSFET due to the lower average electric field in the channel, reducing the interface roughness scattering [4.13]

Advanced thin-body transistor structures are indispensable for scaling the CMOS devices into the deep nanometer regime without degrading the performance and power consumption. However, in order to apply for nanoscale CMOS devices, the unique device parameters needs to be designed adequately, and the process integration challenges should be overcome.

4.2 Design Methodology and Challenges for Advanced Transistor Structures.

The most straightforward implementation of the advanced thin-body transistor structures is the UTB MOSFET, in which the device is fabricated in the silicon film of a silicon-on-insulator (SOI) wafer. The body thickness (T_{Si}) is determined by the thickness of the SOI layer. **Figure 4.5** shows the impact of body thickness on the subthreshold characteristics of UTB MOSFET. It can be seen that the off-state leakage

current decreased by 3 orders-of-magnitude and the subthreshold swing is improved by 25 mV/dec through the reduction in body thickness from 7 nm to 3 nm for 18 nm gate length. The subthreshold swing of the UTB MOSFET with 3 nm thick body shows an almost ideal value (*i.e.*, 60 mV/dec at room temperature), despite of any heavy body doping concentration. It is worth noting that the behavior of fully depleted (FD) SOI device (T_{Si} = 20 nm) is similar to that of a resistor due to the short channel effects.

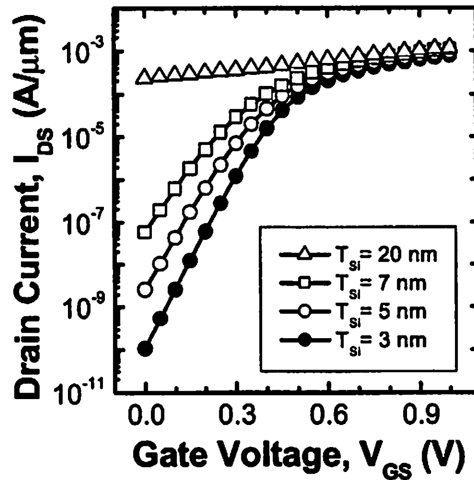


Figure 4.5 Impact of body thickness on the subthreshold characteristics of UTB MOSFET (L_G=18 nm, T_{ox}=1.5 nm, and $N_A = 10^{15}$ cm^{-3}).

Figure 4.6 shows the simulation results of drain induced barrier lowering (DIBL) as a function of the ratio of gate length to body thickness ($\zeta = L_G/T_{Si}$). It can be seen that the ratio of gate length to body thickness (ζ) should be properly designed for a given

technology node and device structure; while $\zeta = 4$ is necessary for UTB MOSFETs to suppress the short channel effects, the required ζ is reduced to 2 for DG MOSFETs due to the stronger control over the channel potential. For example, for 40 nm gate length, $T_{Si} < 10$ nm is needed for UTB MOSFETs, while $T_{Si} < 20$ nm for DG MOSFETs.

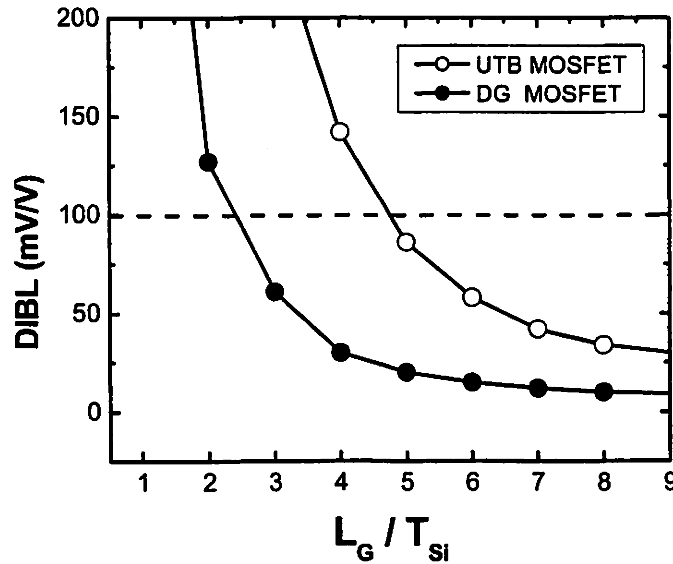


Figure 4.6 Simulation results of drain induced barrier lowering (DIBL) as a function of the ratio of gate length to body thickness ($\zeta = L_g/T_{Si}$) for UTB and DG MOSFETs.

Another big benefit from DG MOSFETs is alleviating the stringent body thickness requirement, allowing approximately 2 times further scaling of the MOSFET with a given silicon body thickness. It should be noted that when the silicon body becomes thinner than 10 nm, threshold voltage (V_T) varies because quantum mechanical (QM)

shift of the ground state energy is inversely proportional to the square of the body thickness. The uncertainty of the threshold voltage (σV_T), to the first order, can be expressed by $\Delta V_T = (h^2\pi^2/qm^*)(1/T_{Si}^2)(\Delta T_{Si}/T_{Si})$ [4.14], as shown in **Figure 4.7**. Numerical simulation and experimental studies show that V_T shifts rapidly as the silicon body thickness scales thinner than 5 nm [4.15, 4.16, 4.17].

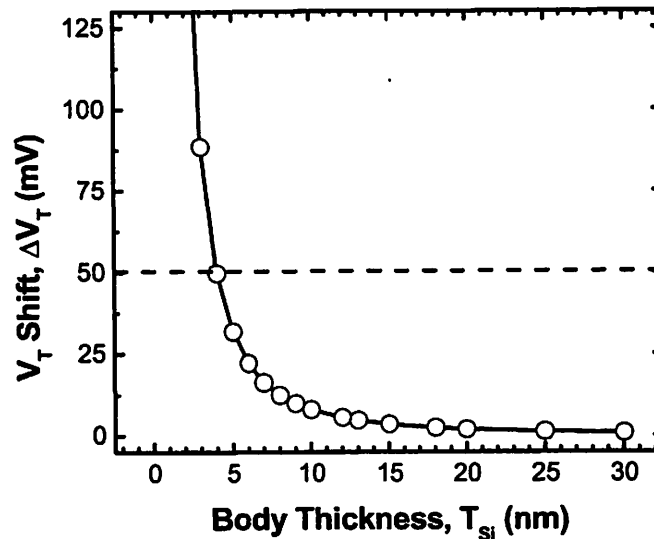


Figure 4.7 Impact of the body thickness on threshold voltage shift for advanced thin-body transistor structures [4.14].

There are three basic configurations to implement DG MOSFET, as illustrated in **Figure 4.8** [4.18]. In a type I configuration, the silicon body thickness can be easily controlled uniformly compared to the other two configurations, which is the most critical

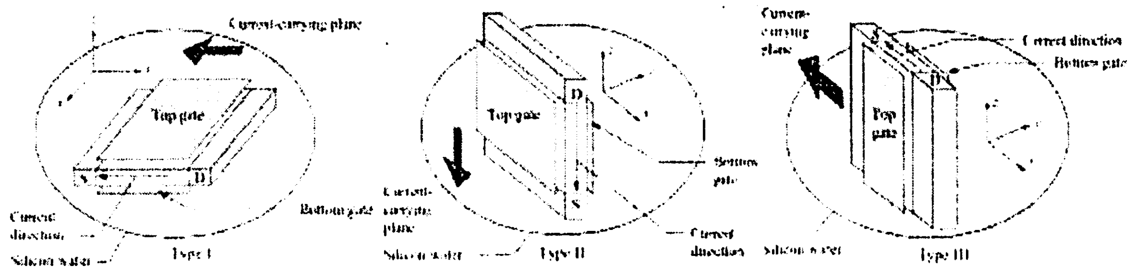


Figure 4.8 Three basic configurations of the double gate (DG) MOSFET [4.18].

dimension in DG MOSFET. However, complexity in process integration and difficulty in self-aligning the top and bottom gate without introducing substantial parasitic resistance and capacitance should be overcome; **Figure 4.9** shows the scanning electron microscopy (SEM) image of a misaligned DG MOSFET [4.19]. Simulation study predicted that 25 % misalignment between top and bottom gate induced 33 % increase in delay [4.20]. Type II configuration has the better control of the gate length uniformly, and provides the most compact layout for DRAM applications. However, there are challenges in avoiding a large parasitic gate-to-source/drain overlap capacitance, obtaining more than one gate length, and connecting individual devices without sacrificing the layout area for CMOS logic applications [4.21, 4.22]. Type III configuration, the *FinFET*, has the highest packing density and allows easy access to all four electrodes with the self-alignment of top and bottom gate. However, there are

challenges in obtaining the critical dimension of body thickness and minimizing the plasma etching damage of the channel. It is worthwhile to note that *spacer lithography* process has been demonstrated to pattern the body thickness down to 30 nm with a good uniformity, which is by far below the today's lithographical limit [4.23], and *hydrogen annealing* process has shown to provide high surface quality on etched silicon surface [4.24].

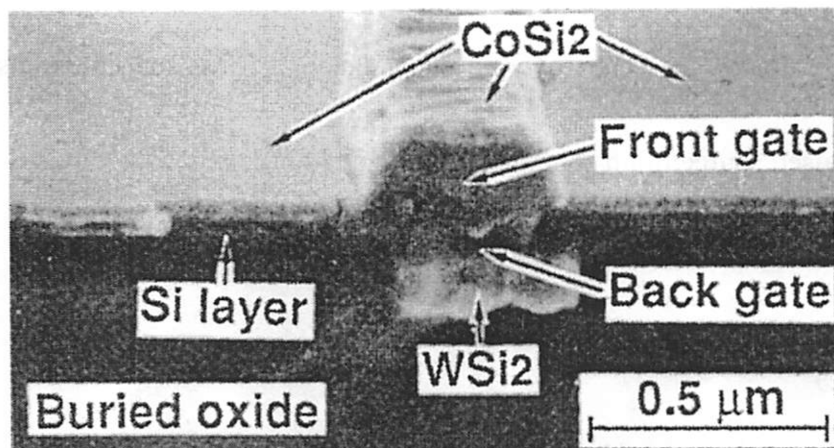


Figure 4.9 Cross-sectional scanning electron microscopy (SEM) image of a misaligned double gate (DG) MOSFET (Type I configuration) [4.19].

For advanced transistor structures regardless of the configurations, there are two challenges resulted from the nature of ultra-thin body thickness; parasitic resistance and threshold voltage adjustment. The parasitic resistance due to the ultra-thin body

thickness should be reduced using thick source/drain fanout structures self-aligned to gate electrode in order to fully achieve the aforementioned performance improvements [4.25, 4.26, 4.27], but this results in layout area penalty. By using selective deposition, a raised source/drain structure can be created to reduce the parasitic resistance as shown in **Figure 4.10**. Several methods have been demonstrated, including selective silicon (Si) epitaxial growth [4.26], selective silicon-germanium (SiGe) epitaxial growth [4.28], and selective germanium (Ge) deposition [4.29]. One drawback is, however, that it inevitably results in increased overlap capacitance. Thus, spacer widths between the gates and raised source/drain should be optimized [4.30].

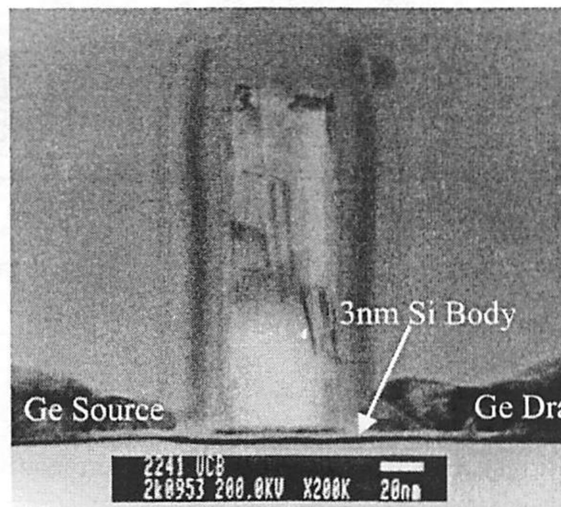


Figure 4.10 Cross-sectional transmission electron microscopy (X-TEM) image of selectively deposited raised germanium (Ge) source/drain ultra-thin body (UTB) MOSFET [4.30].

Threshold voltage adjustment should be achieved by gate work function engineering due to the lack of channel body dopants in advanced thin-body transistor structures. Even though the use of heavy channel doping (> 5×10^{18} cm^{-3}) is an alternative way to control the threshold voltage, this reintroduces problems with reduced carrier mobility and random dopant fluctuations [4.31]. An asymmetric DG MOSFET structure can also achieve an appropriate threshold voltage by using conventional n^+ and

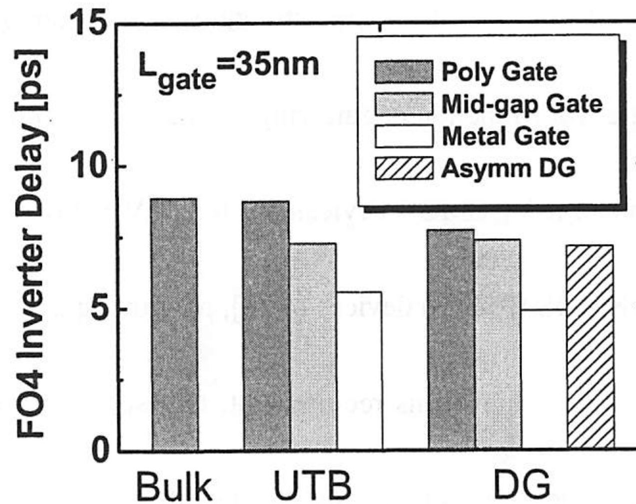


Figure 4.11 The impact of methods for controlling threshold voltage on the fanout of four (FO4) inverter delay. Note that all the devices have the identical V_T values [4.32].

p^+ poly-Si gates at the cost of increased transverse electric field [4.19]. As a result, both channel doping and an asymmetric DG MOSFET structure result in degraded device performance as shown in **Figure 4.11** [4.32]. Therefore, the need for gate work

function engineering is emphasized as a unique solution for the performance benefits and reliable-operations of the advanced thin-body transistor structures. The theoretical data for threshold voltage as a function of gate work function is shown in Figure 2.3

4.3 Tunable Work Function Mo-Gated SiO_2 UTB MOSFET

For advanced thin-body transistor structures, it is desirable to adjust threshold voltage through gate work function engineering. The gate work function values needed for low and symmetrical V_T CMOS devices are 0.35 eV below (above) the conduction (valence) band for NMOS (PMOS) devices [4.33], precluding the use of doped poly-Si as the gate electrode. To achieve this requirement, two separate metals with appropriate work functions are necessary on a single substrate. However, this approach has difficulties in avoiding the process complexity and in providing the multiple V_T values for low voltage and high performance applications; that is, low V_T devices are adopted to reduce the delay in the critical paths, while high V_T devices in minimizing the standby leakage power [4.34]. Thus, it is preferable to deposit a single gate material and subsequently adjust its work function selectively. Molybdenum (Mo) is a candidate

gate material for future fully depleted (FD) SOI CMOS technology, because it is compatible with a standard CMOS process flow and its work function can be adjusted within the desired range (4.5-5.0 eV) via nitrogen implantation as discussed in Chapter 2.5 [4.24, 4.35, 4.36]. In this section, the tunability of the Mo gate work function on SiO_2 is demonstrated for the first time using p-channel UTB MOSFETs [4.37].

4.3.1 Fabrication of Mo-gated SiO_2 p-channel UTB MOSFETs

The process sequence used to fabricate p-channel UTB MOSFETs is depicted in **Figure 4.12**. The starting substrates were Unibond® SOI wafers, with 100 nm thick lightly doped (ρ = 10 – 15 Ω-cm) p-type (100) silicon on 400 nm thick buried oxide. The silicon film was thinned down to ~15 nm by thermal oxidation. The body thickness was chosen not to be too thin, to avoid threshold voltage (V_T) shifts due to quantum confinement [4.15, 4.16, 4.17, 4.38]. Isolation is simply achieved by patterning the silicon into active-area islands without the need for further dielectric deposition and planarization processes because of the small step height (< 15 nm). After active-area patterning, a 3.0 nm thick SiO_2 gate dielectric was thermally grown, and a 40 nm thick Mo film was deposited at 200°C using a DC magnetron sputtering system (10^{-7} Torr base

pressure). It should be noted that *plasma charge trap* (PCT), as discussed in Chapter 2.3, was not applied, thus sputtering damage may be introduced to the gate dielectric during the sputtering process. Then, nitrogen implantation was performed at various doses for V_T adjustment (see **Table 4.1**). Afterwards, *in-situ* phosphorus doped poly-Si and a hard mask low temperature oxide (LTO) were sequentially deposited. The purpose of the hard mask was to prevent shorting of the source/drain (S/D) with gate during the subsequent selective germanium (Ge) deposition to form raised S/D regions.

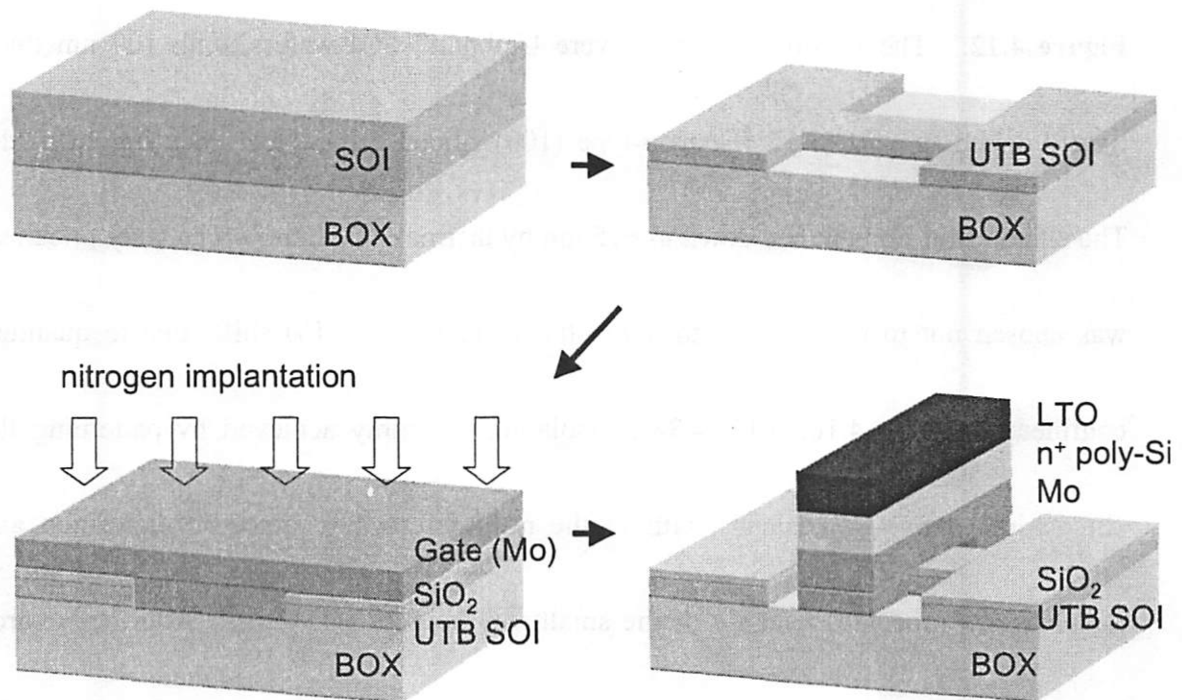


Figure 4.12 The fabrication sequences used for p-channel ultra-thin body (UTB) MOSFET.

A highly selective dry etch process, as discussed in Chapter 2.4, was adopted to etch the Mo gate on thin gate oxide. After gate-sidewall spacer formation, Ge was selectively deposited by low-pressure chemical vapor deposition (LPCVD), and S/D dopants were implanted. Device fabrication was completed with rapid thermal annealing (RTA) at 700°C, 60s in N_2 ambient to activate the implanted S/D dopants. This rather conservative anneal was used because Ge and Si intermixing is known to be enhanced in the presence of dopants [4.39], for the formation of abrupt p-n junctions with low thermal budget. **Figure 4.13** shows a cross-sectional transmission electron microscopy (X-TEM) of the completed p-channel UTB MOSFET.

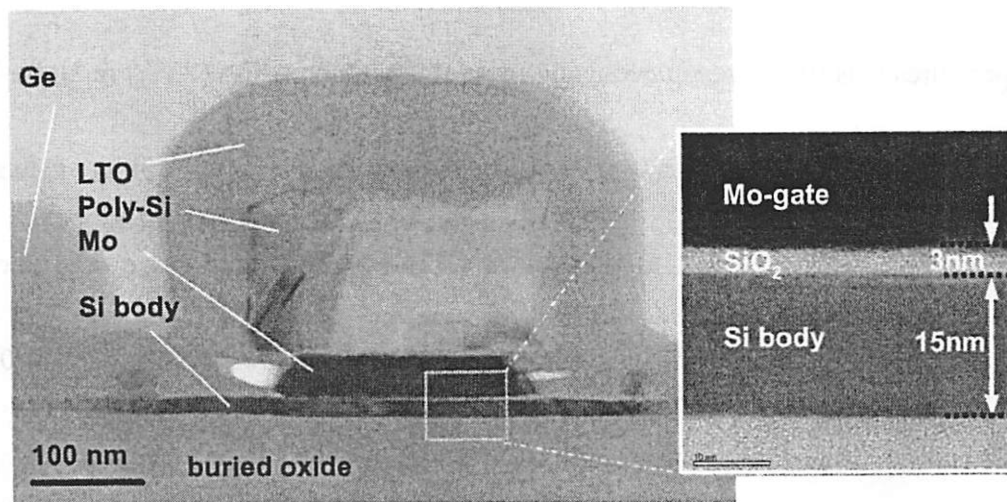


Figure 4.13 A cross-sectional transmission electron microscopy (X-TEM) of an ultra-thin (15 nm) silicon body Mo-gated MOSFET (T_{OX} = 3 nm, L_G=290 nm). The notched gate profile resulted from the unintended wet cleaning process.

Table 4.1 Summary of the process split conditions.

	Substrate	Channel doping (N_A)	Gate Stack	$^{14}N^+$ implant condition
WF #1	Bulk Si	$< 10^{15}$ cm^{-3}	Mo/SiO_2	–
WF #2	Bulk Si	$< 10^{15}$ cm^{-3}	Mo/SiO_2	20 KeV, 2x10^{15} cm^{-2}
WF #3	Bulk Si	$< 10^{15}$ cm^{-3}	Mo/SiO_2	20 KeV, 4x10^{15} cm^{-2}
WF #4	SOI	$\sim 10^{15}$ cm^{-3}	Mo/SiO_2	–
WF #5	SOI	$\sim 10^{15}$ cm^{-3}	Mo/SiO_2	20 KeV, 2x10^{15} cm^{-2}
WF #6	SOI	$\sim 10^{15}$ cm^{-3}	Mo/SiO_2	20 KeV, 4x10^{15} cm^{-2}

4.3.2 Results and Discussion of Mo-gated SiO_2 p-channel UTB MOSFETs

The thermal stability of Mo in contact with SiO_2 gate dielectric at various temperatures was first investigated using rapid thermal annealing (RTA) in N_2 for bulk-Si MOS capacitors. It is worth noting that all the fabrication steps to form the gate stack of these wafers were processed together with UTB MOSFETs. **Figure 4.14** shows the measured high-frequency C-V curves. For annealing temperatures up to 900°C, the accumulation capacitance does not change at all. The capacitance decreases after a 1000°C anneal, however, due to the reaction of Mo with SiO_2. These results indicate

that Mo gate is thermodynamically stable on SiO_2 at temperatures up to 900? , which is sufficient for S/D dopant activation in selective Ge raised S/D UTB MOSFET structures.

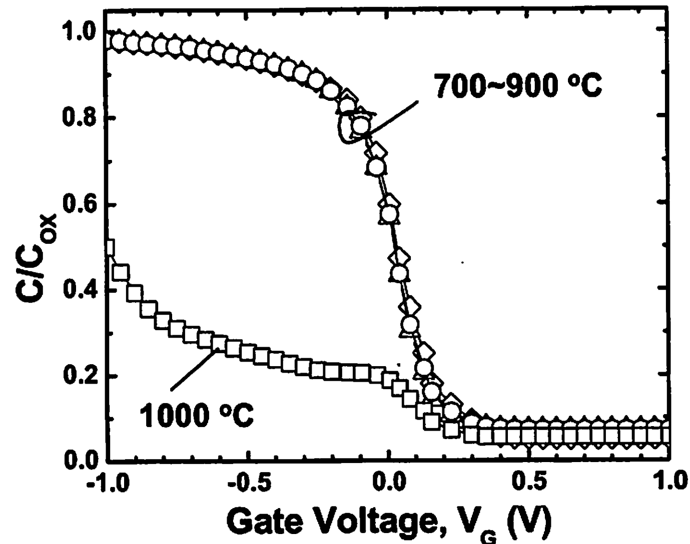


Figure 4.14 Measured high frequency (100 KHz) C-V curves of Mo-gated SiO_2 bulk-Si MOS capacitors annealed in N_2 ambient for 1 min. at various temperatures (T_{OX} = 3.0 nm, Area = 50x50 μm^2).

Figure 4.15 shows the measured high-frequency C-V curves for p-channel UTB MOSFETs implanted with various doses of nitrogen. It can be seen that the threshold voltage shift to more negative values with increasing nitrogen implant dose. The measurement set-up can be shown in the inset of Figure 4.15 [4.40]; when the channel is inverted, the measured capacitance corresponds to the gate dielectric capacitance. It is

worthwhile to note that the inversion capacitance does not decrease with increasingly negative gate voltage, *i.e.* there is no poly-Si depletion effect (PDE) due to the Mo gate.

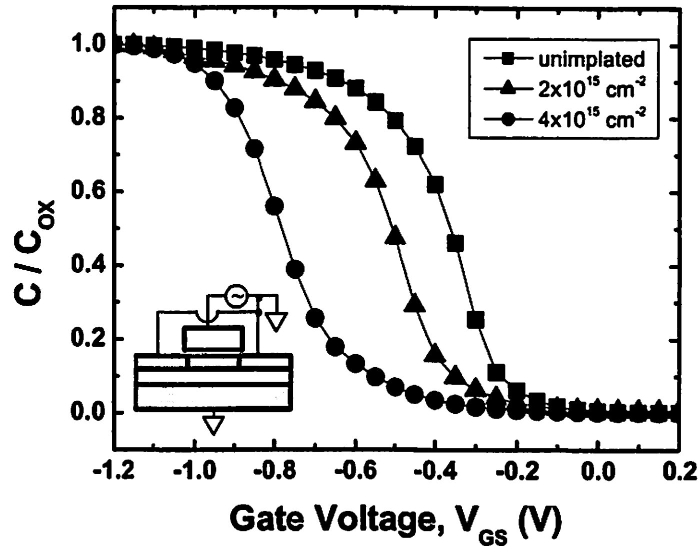


Figure 4.15 Measured high frequency (100 KHz) C-V curves of Mo-gated SiO_2 p-channel UTB MOSFETs implanted with various doses of nitrogen.

V_T values for the Mo-gated p-channel UTB MOSFETs were extracted using the maximum transconductance ($g_{m,max}$) method, as shown in **Figure 4.16.** The V_T for unimplanted Mo-gate device is –0.2 V, and shifts by approximately –65mV for every 1 x 10^{15} cm^{-2} increment in nitrogen implant dose. Thus, the threshold voltage for the UTB MOSFETs can be adjusted via Mo-gate work function engineering. In order to achieve

the desired V_T (0.2 ~ 0.3 V) in n-channel UTB MOSFETs, an estimated dose of 6 – 8×10^{15} cm^{-2} would be needed.

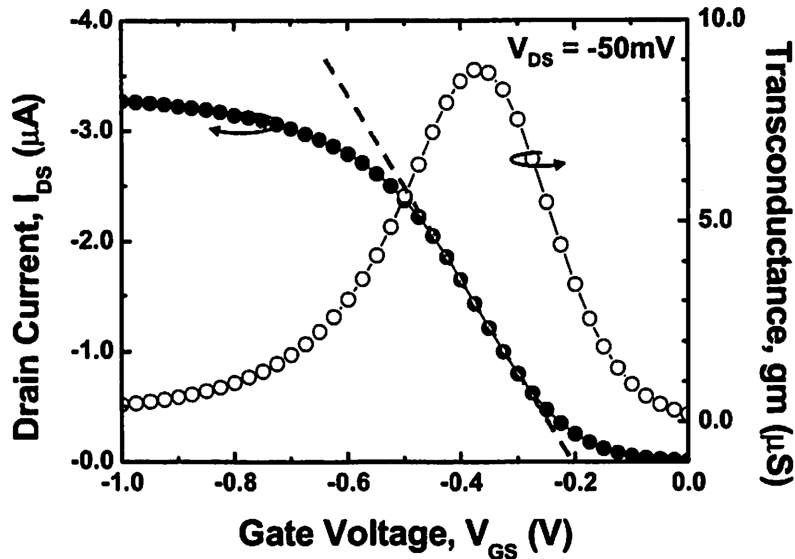


Figure 4.16 Maximum transconductance method is used to extract the V_T of Mo-gated SiO_2 p-channel UTB MOSFET. Data is shown for L_G = 300nm, T_{Si} = 15nm, and un-implanted Mo-gate.

Figure 4.17 shows the I_{DS}-V_{GS} characteristics for p-channel UTB MOSFETs. The subthreshold slope is somewhat high (106.9 mV/dec), considering that the body thickness (T_{Si}) is more than 4 times smaller than the gate length (L_G), i.e. ζ = 20, so that the subthreshold slope should be nearly ideal (~60 mV/dec) as discussed in Chapter 4.2. This may be due to the damage incurred during Mo film sputtering, which can be avoided

by either using a chemical vapor deposition (CVD) method or sputtering with *plasma charge trap* (PCT) as discussed in Chapter 2.3. It should be noted that since the Mo film has the columnar crystal structure, low-energy and large tilted-angle implantation can prevent $^{14}N^{+}$ implant damage with reduced channeling effect [4.41].

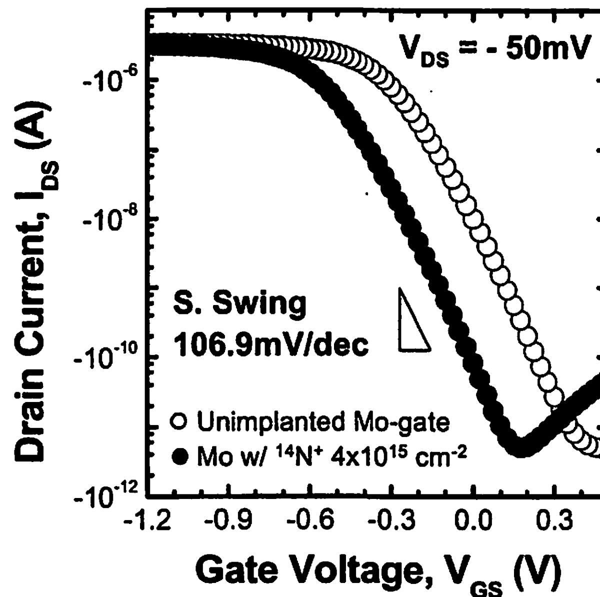


Figure 4.17 Measured I_{DS}-V_{GS} characteristics for Mo-gated SiO_2 p-channel UTB MOSFETs.

Figure 4.18 shows the measured drain induced barrier lowering (DIBL) for p-channel UTB MOSFETs. Despite of the lightly doped body (10^{15} cm^{-3}), DIBL is greatly suppressed less than 40 mV/V for less than 300 nm gate length due to the ultra-thin body thickness (15 nm), hence $\zeta > 4$. It should be noted that there is no tradeoff

between the degree of drain field shielding, *i.e.*, short channel effects and the threshold voltages, *i.e.*, channel doping concentration in UTB MOSFETs.

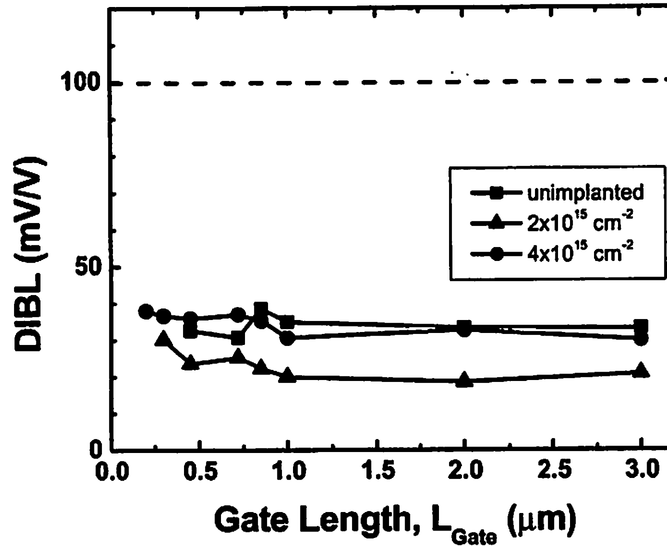


Figure 4.18 Measured drain induced barrier lowering (DIBL) as a function of the gate length of Mo-gated SiO_2 p-channel UTB MOSFETs (T_{Si} = 15 nm, and T_{OX} = 3.0 nm).

Figure 4.19 shows the measured I_{DS}–V_{DS} characteristics for the p-channel UTB MOSFETs. The channel length modulation is greatly reduced because UTB MOSFETs can effectively shield the drain field from affecting the channel potential. The low drain current is mainly due to the insufficient overlap of source/drain with gate, which is caused by the unintended lateral etching of Mo film during the cleaning process (see **Figure 4.13**).

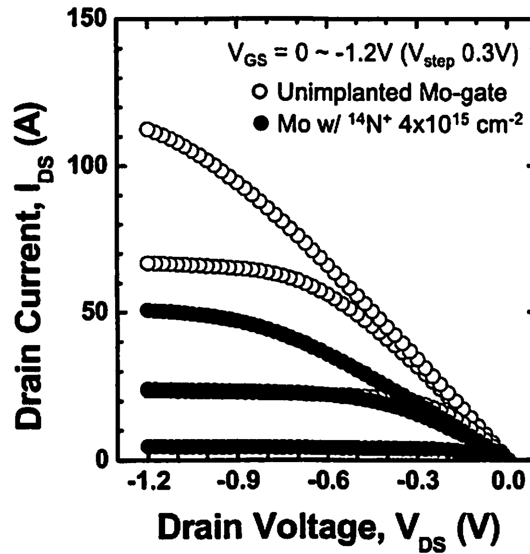


Figure 4.19 Measured I_{DS}–V_{DS} characteristics of Mo-gated SiO_2 p-channel UTB MOSFETs (L_G = 300 nm, W = 10 μm, T_{Si} = 15 nm, and T_{OX} = 3.0 nm).

4.4 Tunable Work Function Mo-Gated HfO_2 CMOS FinFETs

The double-gate (DG) FinFET is one of the most promising transistor structures for scaling CMOS technology to sub-25 nm gate lengths. Integration of metal gate and high-*k* gate dielectric is desirable to reduce the equivalent gate-oxide thickness (EOT) while maintaining low gate leakage current, to improve transistor drive current and to relax the fin-width requirement for controlling short-channel effects [4.42, 4.43, 4.44].

In order to maximize carrier mobilities and avoid statistical dopant fluctuation effects on threshold voltage (V_T), the body of a FinFET should be undoped; V_T adjustment must be achieved by tuning the gate work function, in this case. Molybdenum (Mo) is a candidate gate material for future FD-SOI CMOS technology, because it is compatible with a standard CMOS process flow and its work function can be adjusted within the desired range (4.5-5.0 eV) via nitrogen implantation [4.24, 4.35, 4.36]. In this section, the tunability of the Mo gate work function on HfO_2 is demonstrated for the first time using FinFETs [4.45].

4.4.1 *Fabrication of Mo-gated HfO_2 CMOS FinFETs*

Figure 4.20 outlines the FinFET process flow. UNIBOND® wafers were used as the starting substrates, and oxidized to reduce the SOI thickness to 50 nm. 80-nm wide Si fins were then defined by *spacer lithography*, while the source/drain (S/D) contact regions were defined by *i*-line photolithography [4.23]. After patterning of the SOI and NH_3 pretreatment of the Si fin (110) sidewall surfaces, HfO_2 was deposited by CVD using Hf t-butoxide ($Hf(OC(CH_3)_3)_4$) as a precursor at 500°C. A 60 nm thick

molybdenum (Mo) film was then deposited by DC magnetron sputtering with a *plasma charge trap* (PCT) to minimize sputtering damage, as described in Chapter 2.3.

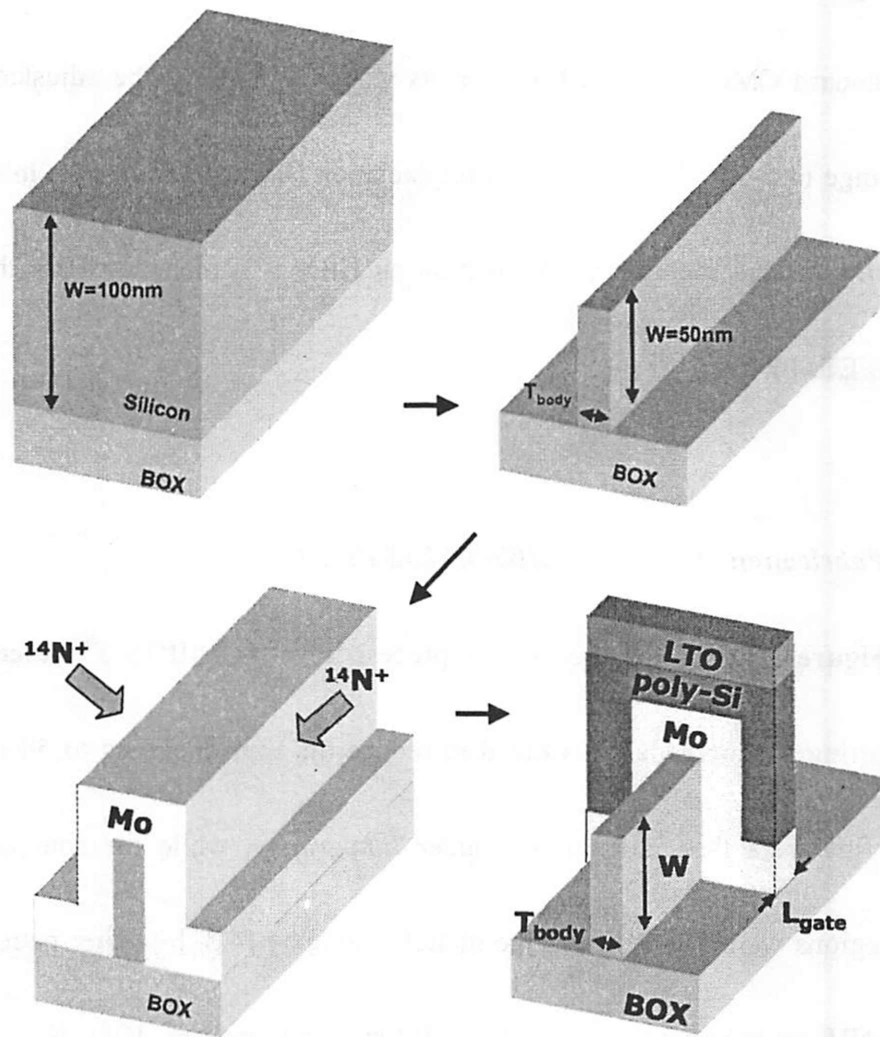


Figure 4.20 The fabrication sequences used for the Mo-gated HfO_2 CMOS FinFETs

For some n-channel FinFETs, nitrogen ($1x10^{16}$ cm^{-2}, 5 keV) was implanted into the Mo gate film at 30° tilt on each side of the Si fins (*i.e.*, 60° tilt on the normal to the Mo gate surface) in order to reduce the effective Mo work function and achieve low V_T. The use of a low-energy tilted implant prevents nitrogen penetration into the underlying gate dielectric as shown in **Figure 4.21**. The Mo was capped with *in-situ* n^+ doped poly-Si and planarized by chemical mechanical polishing (CMP). After gate patterning and source/drain ion implantation, a 900°C 60s RTA in N_2 was used to activate the dopants. Finally, the devices were annealed at 400°C in forming gas.

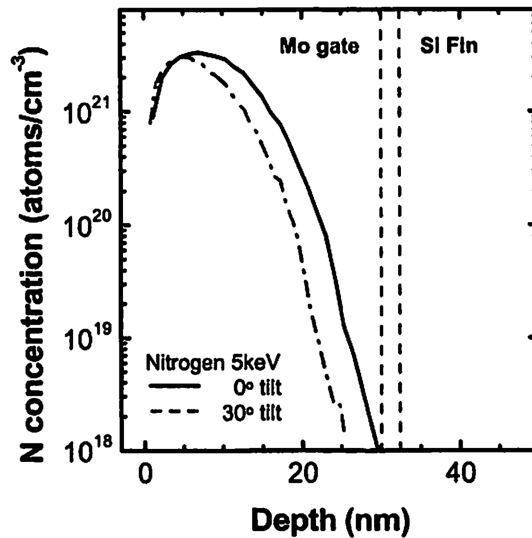


Figure 4.21 *SRIM®* simulation results for the nitrogen implantation profiles in the Mo/HfO_2 gate stack (dose=$5x10^{15}$ cm^{-2}).

Figures 4.22 are tilted-view scanning electron microscopy (SEM) images of the completed Mo/HfO_2 FinFETs. Neither micro-trenching nor Mo gate residue was observed due to the high etching selectivity, as discussed in Chapter 2.4. It should be noted that no metallization or silicided S/D structure was used in this study. **Figures 4.23** show cross-sectional transmission electron microscopy (TEM) image, and close-up view of the gate stack at the silicon fin sidewall. The undercut of buried oxide beneath the fin occurred during the sacrificial oxide removal using diluted HF. It should be noted that this undercut may introduce the yield issues, but shield the channel potential from drain field [4.46]. It is worth noting that the Mo gate layer is continuous at the bottom of the Si fin due to the improved step-coverage with PCT sputtering [4.47].

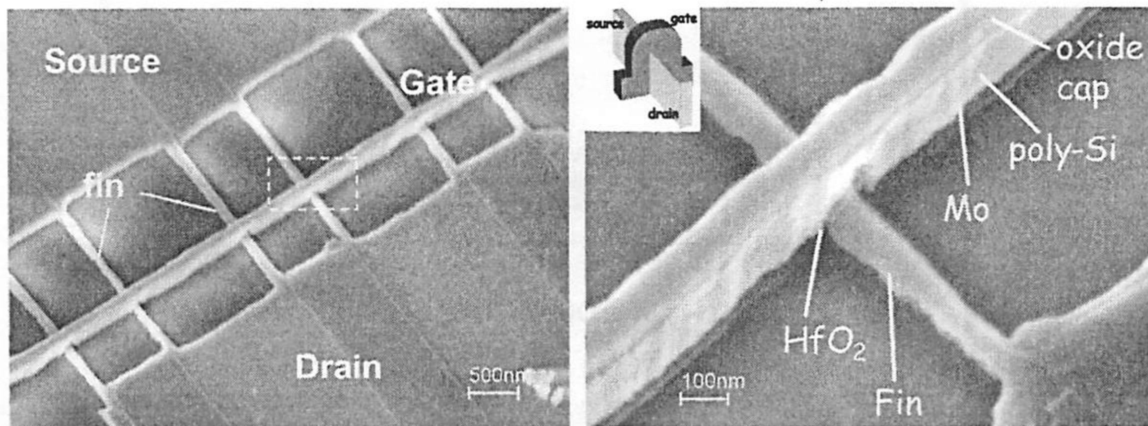


Figure 4.22 Tilted-view scanning electron microscopy (SEM) images of the Mo/HfO_2 FinFETs.

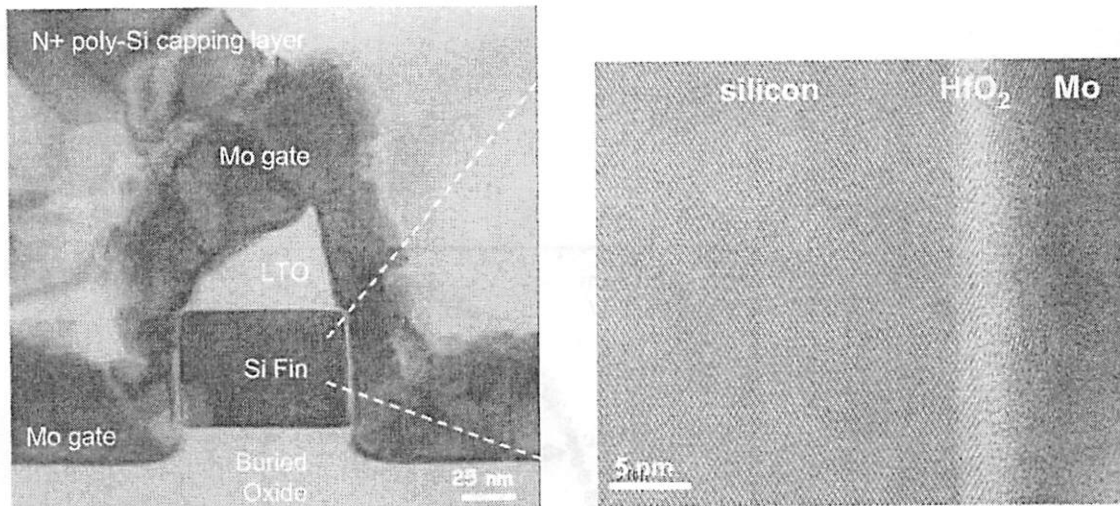


Figure 4.23 Cross-sectional transmission electron microscopy (X-TEM) images of the Mo/HfO_2 FinFETs.

4.4.2 Results and Discussion of Mo-gated HfO_2 CMOS FinFETs

Figure 4.24 compares the measured I_{DS}-V_{GS} characteristics for Mo-gate HfO_2 n-channel FinFETs with and without nitrogen gate implantation. It can be seen that V_T (defined as the gate voltage when I_{DS} = 100 nA/μm for V_{DS} = 50 mV) is shifted from 0.73 V down to 0.28 V by the nitrogen implant. This indicates that the Mo-gate work function was effectively reduced by the nitrogen implant. Compared to the previous studies [4.24, 4.35, 4.36], the subthreshold swing is greatly improved due to the

minimization of Mo gate sputtering damage and the low-energy tilted nitrogen implantation [4.47].

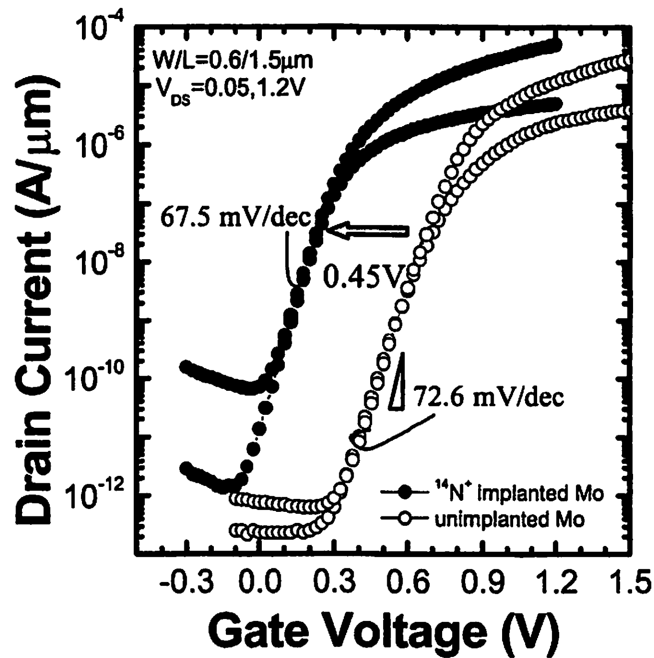


Figure 4.24 Measured I_{DS}-V_{GS} characteristics of pure and nitrogen implanted Mo-gated HfO_2 FinFETs. Nitrogen implantation into Mo-gate is effective for VT control without degrading the subthreshold swing.

The amount of reduction in gate work function is proportional to the nitrogen implant dose as shown in **Figure 4.25**, but it is less for Mo on HfO_2 than for Mo on SiO_2 due to the *Fermi-level pinning effect* [4.6, 4.7, 4.48, 4.49] and nitrogen diffusion into the HfO_2. [4.45].

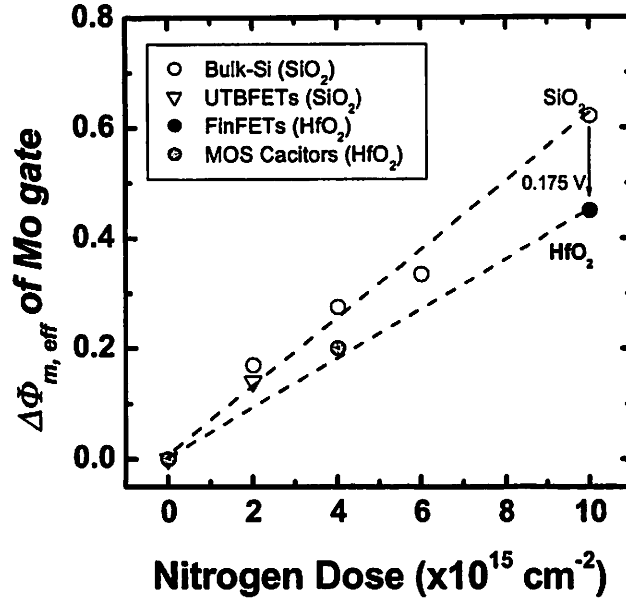
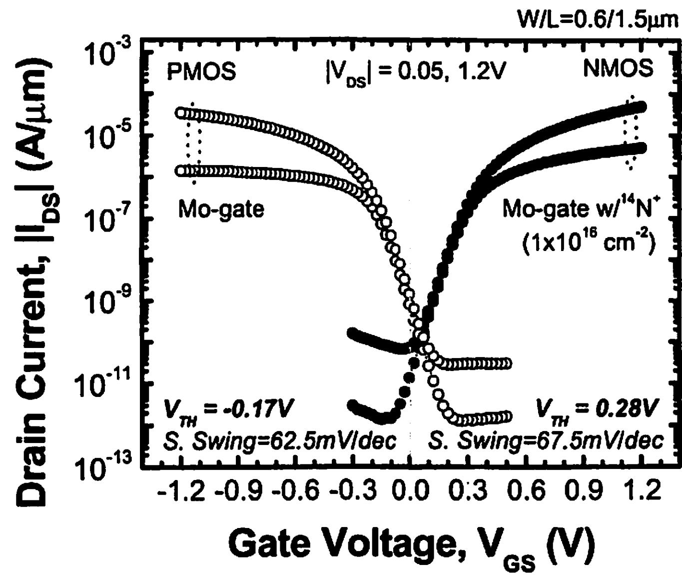
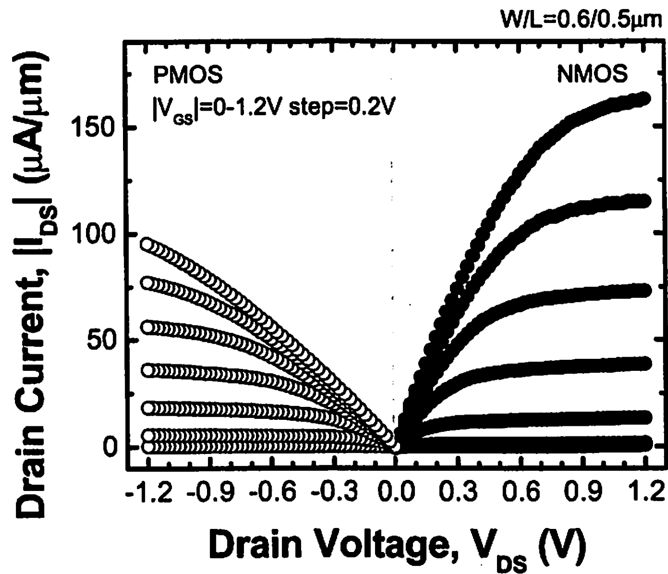


Figure 4.25 Change in effective Mo gate work function ($\Delta\Phi_{m,eff}$) *vs*. nitrogen implantation dose.

Figure 4.26 shows measured I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics for n-channel (with nitrogen-implanted Mo gate) and p-channel (with pure Mo gate) FinFETs. The V_T and subthreshold swing values for the n-channel (p-channel) device are 0.28 (-0.17) V, and 67.5 (62.5) mV/dec, respectively. The p-channel device exhibits higher parasitic resistance than the n-channel device due to differences in p-type *vs*. n-type dopant redistribution in thin SOI during rapid thermal annealing [4.50].



(a)



(b)

Figure 4.26 Measured (a) I_{DS}-V_{GS} and (b) I_{DS}-V_{DS} characteristics of Mo-gated HfO_2 CMOS FinFETs. Low energy (5 KeV) and 30-degree tilted nitrogen implantation has been applied to Mo-gate for n-channel FinFET.

Figure 4.27 compares measured C_G-V_G curves (circles) with quantum-mechanical simulations (lines) [4.51]. The measured multi-fin device structure is shown in the inset. Extracted equivalent oxide thickness (EOT) in inversion is 1.95 or 1.92 nm for n-channel or p-channel devices, respectively. Stretch-out in the measured C-V characteristic can be seen for the n-channel device, but not for the p-channel device.

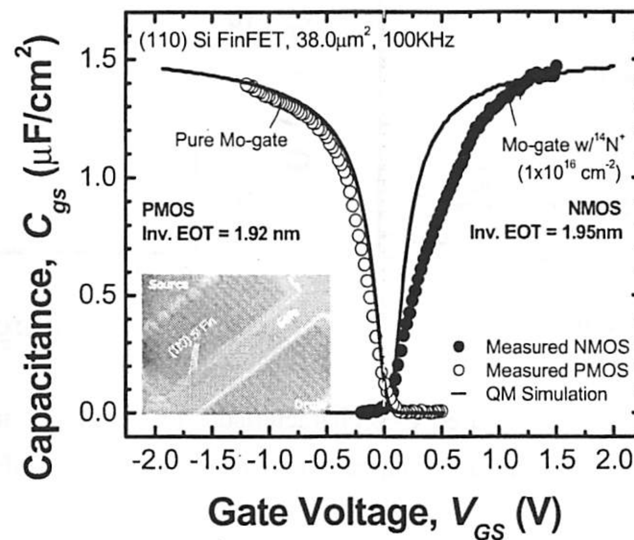


Figure 4.27 Comparison of measured C-V characteristics (circles) and quantum mechanical simulations (lines) for n-channel and p-channel Mo/HfO_2 FinFETs.

This result indicates an asymmetrical distribution of interface traps (D_{it}) within the energy bandgap (*i.e.*, higher D_{it} above E_i) [4.52], which explains the larger subthreshold swing of the n-channel FinFET as shown in Figure 4.26. As can be seen in **Figure 4.28**,

the deviation from the ideal C-V characteristic is larger for a nitrogen-implanted Mo gate, indicating a higher interfacial trap density. This is likely due to the formation of an interfacial HfO_xN_y layer at the Si surface [4.53].

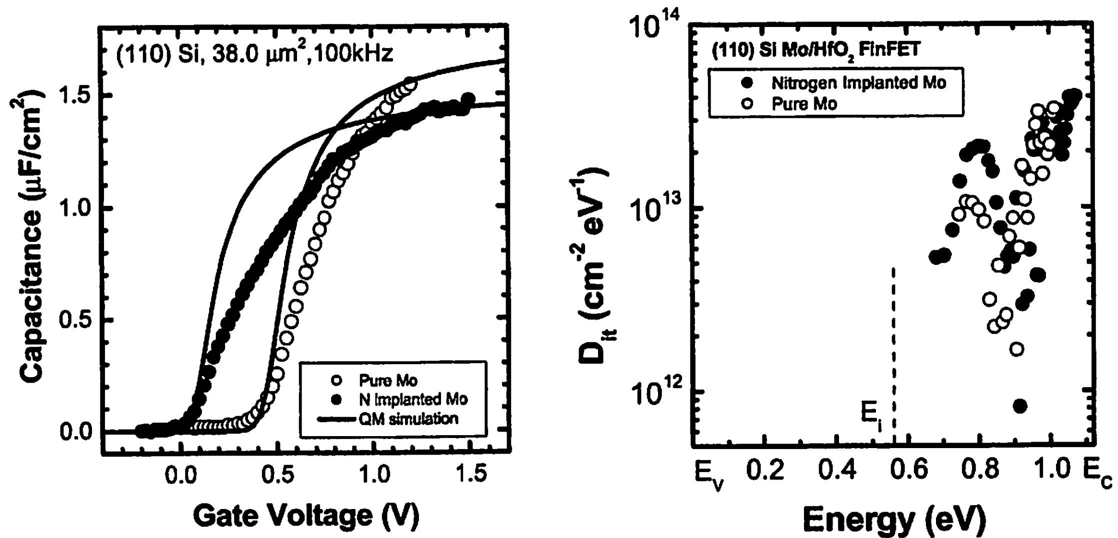


Figure 4.28 Comparison of measured C-V characteristics and extracted interface trap densities (D_{it}) for pure and nitrogen implanted n-channel Mo/HfO_2 FinFETs.

Figure 4.29 shows the field-effect electron mobility for (110) Si sidewall Mo-gated HfO_2 FinFETs with (lines) and without (symbols) correcting interface trap density [4.54]. The apparent electron mobility is lower for the nitrogen-implanted device as compared to the unimplanted device, due to the higher interface trap density. **Figure 4.30** shows the field-effect hole mobility for a (110) Si sidewall Mo-gated HfO_2 FinFET.

Both the electron mobility and the hole mobility are significantly degraded compared to the universal mobility curves for a (110) Si surface with SiO_2 gate dielectric [4.55].

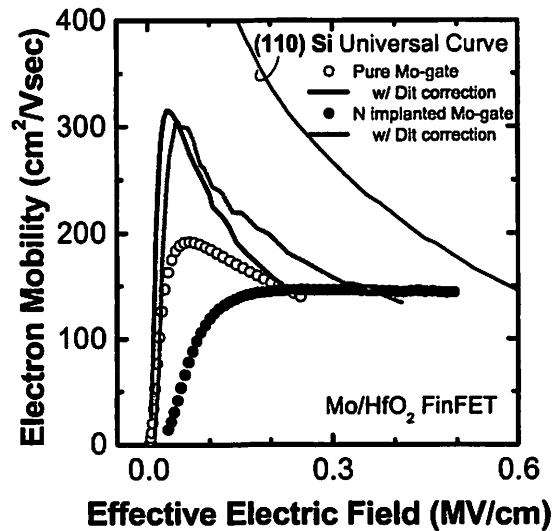


Figure 4.29 Effective electron mobility with and without interface trap density (D_{it}) correction for pure and nitrogen implanted (110) n-channel Mo/HfO_2 FinFET.

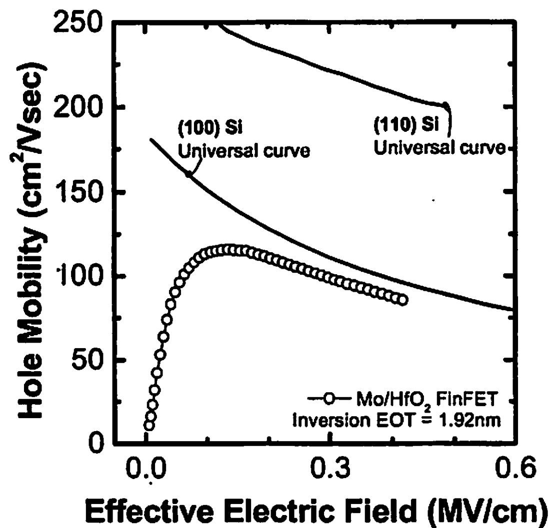


Figure 4.30 Effective hole mobility for (110) p-channel Mo/HfO_2 FinFET.

In order to elucidate the reason for this, the carrier mobility dependence on temperature (in the range from –50°C to 200°C) was investigated. Both electron and hole mobilities increase with decreasing temperature due to reduced phonon scattering as shown in **Figure 4.31**. However, at low field strength (0.1 MV/cm for electrons and 0.2 MV/cm for holes) they exhibit a weaker temperature dependence ($\mu_{eff} \sim T^{-0.95}$) compared to mobilities for SiO_2 gate dielectric ($\mu_{eff} \sim T^{-1.5}$), as shown in **Figure 4.32**. This result indicates that the mobilities are limited by HfO_2 soft phonon scattering [4.56, 4.57].

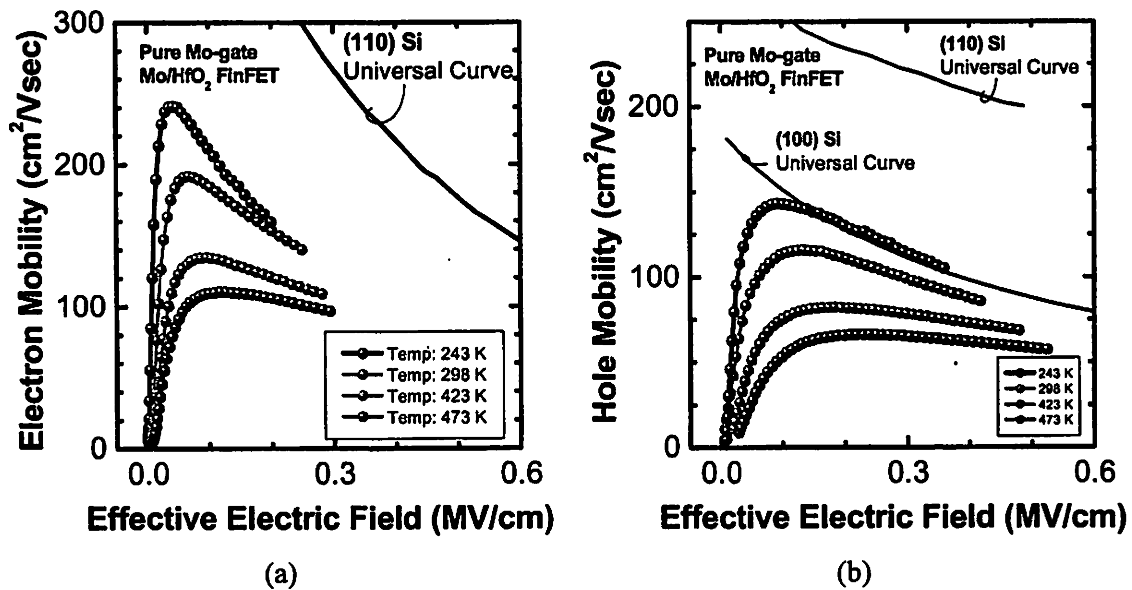


Figure 4.31 Effective (a) electron and (b) hole mobility at various measurement temperatures.

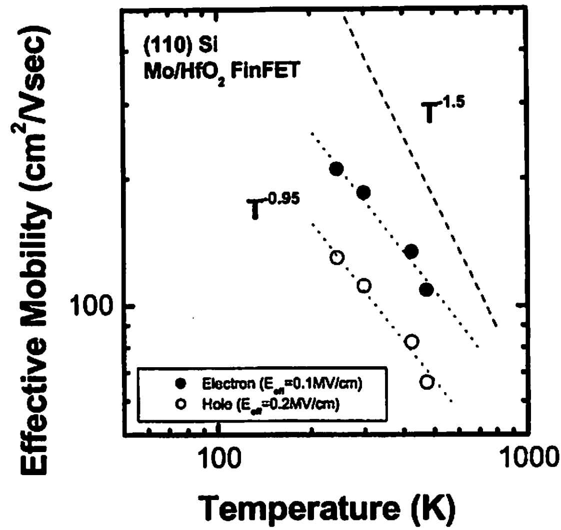


Figure 4.32 Electron and hole mobility for Mo/HfO_2 FinFET less depends on temperature, compared to SiO_2.

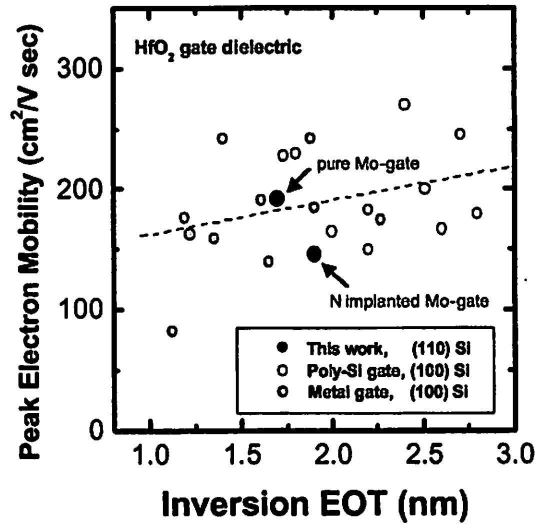


Figure 4.33 Peak electron mobility *vs.* inversion equivalent oxide thickness (EOT).

Figure 4.33 shows that the peak electron mobility achieved in this work is comparable to previously published data for (100) Si with HfO_2 gate dielectric. This is

notable because the electron mobility is lower for a (110) Si surface than for a (100) Si surface, with SiO_2 gate dielectric.

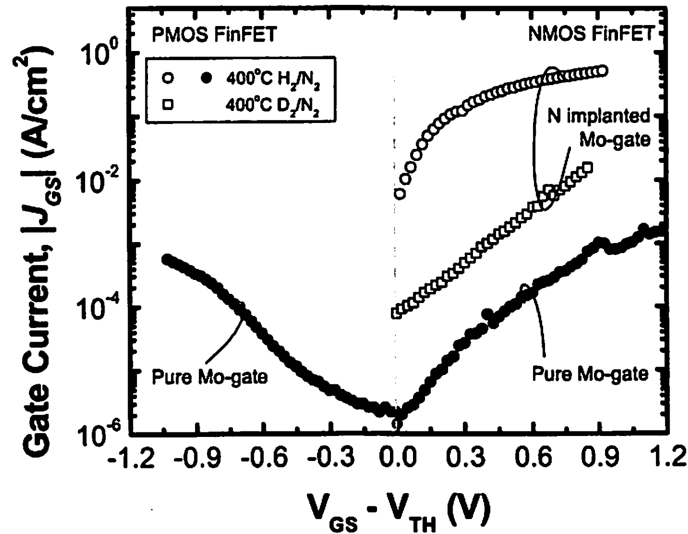


Figure 4.34 Gate leakage current characteristics for n-channel and p-channel Mo/HfO_2 FinFETs. Deuterium (D_2) annealing is effective to reduce the gate current.

Figure 4.34 shows the measured gate leakage current density characteristics. Lower gate leakage can be seen for the p-channel FinFET as compared to the n-channel FinFET (unimplanted Mo gate), due to the larger hole barrier height for HfO_2 [4.58]. Compared to a poly-Si gated SiO_2 stack, the gate leakage current is reduced by 3-4 orders of magnitude for the same EOT as shown in **Figure 4.35**. The nitrogen-implanted Mo-

gate n-channel FinFET shows increased gate current, likely due to nitrogen diffusion into the HfO_2 which degrades the interfacial and bulk properties of HfO_2 [4.53].

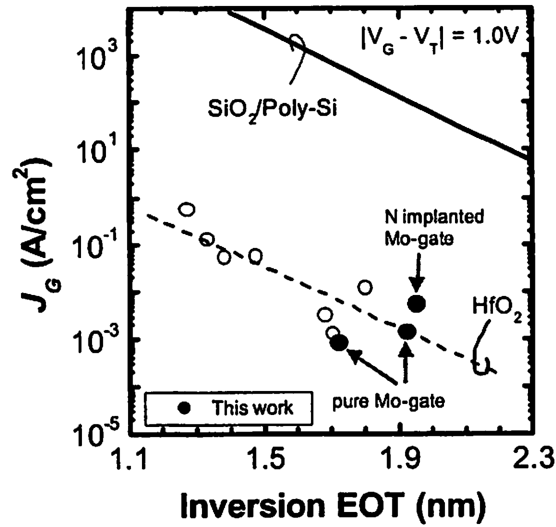


Figure 4.35 Inversion equivalent oxide thickness (EOT) *vs.* gate leakage current density (J_G).

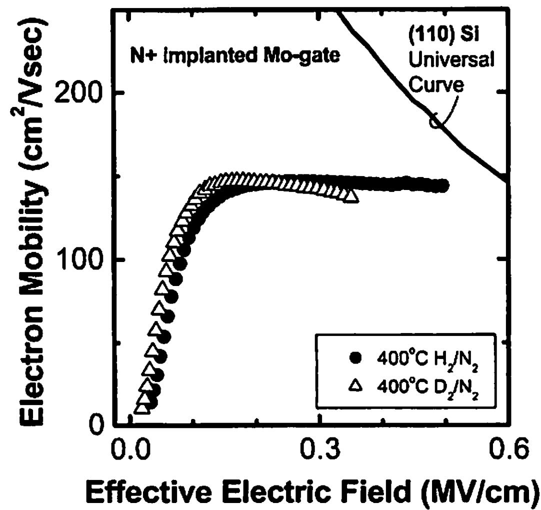


Figure 4.36 Effective electron mobility for different forming gas annealing conditions.

Deuterium annealing is effective to reduce the gate current by 1-2 orders of magnitude as shown in Figure 4.35, and to improve the effective electron mobility slightly as shown in **Figure 4.36**. This implies that deuterium can effectively passivate traps within HfO_xN_y.

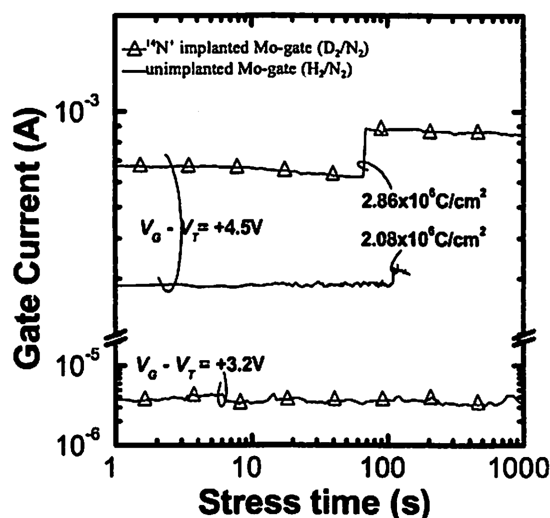


Figure 4.37 Gate dielectric breakdown characteristics for pure and nitrogen implanted Mo-gated HfO_2 FinFETs.

Figure 4.37 shows the gate dielectric charge-to-breakdown (Q_{BD}) characteristics under constant voltage stressing. These initial results indicate that the reliability of a nitrogen-implanted Mo-gate device is comparable to that of a pure Mo-gate device. Key results are summarized in **Table 4.2**.

Table 4.2 Summary of key device results of Mo-gated HfO_2 FinFETs.

	NMOS		PMOS
	Low VT	High VT	Low VT
nitrogen implant dose (cm^{-2})	$1x10^{16}$	—	—
measured V_T (V) (@100nA/μm)	0.28	0.73	– 0.17
subthreshold swing (mV/dec)	67.5	72.6	62.5
Inversion EOT (nm)	1.95	1.75	1.92
gate current density (mA/cm^2)	5.55	0.86	0.52
peak mobility ($cm^2/Vsec$)	146.7	191.9	115.9

4.5 Summary

Design methodology and challenges for the advanced thin-body transistor structures have been investigated. Scalability of the gate length strongly depends on the silicon body thickness, necessitating the technological innovations in achieving critical dimensions below the limit of today's lithography process. Adjustment of the desired threshold voltages without degrading the performance benefits is a serious challenge; the ideal solution is the metal gate work function engineering.

Metal gate work function engineering is demonstrated to be a feasible approach for adjusting the threshold voltages of p-channel UTB MOSFETs for the first time. The range of work function values achieved with molybdenum (Mo) gate technology makes it an attractive candidate for the future nanoscale CMOS technologies, particularly for low power and high performance applications.

Integration of metal gate and high-*k* dielectric employing the advanced thin-body transistor structure is demonstrated for the first time; CMOS FinFETs with Mo gate on HfO_2. Low gate leakage current density was achieved for a thin inversion equivalent oxide thickness (EOT) down to 1.72 nm with carrier mobilities comparable to previously reported works, which is limited by soft phonon scattering. Threshold voltage control is shown to be feasible by tuning the effective Mo work function via nitrogen implantation. Further process optimization is needed to prevent nitrogen diffusion into the HfO_2 gate dielectric to make Mo-gated HfO_2 FinFET technology suitable for future nanoscale CMOS technology.

4.6 References

[4.1] G. E. Moore, "Cramming More Components Onto Integrated Circuits," *Electronics*, vol. 38, no. 8, April 19, 1965.

[4.2] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions," IEEE J. Solid-State Circuits, vol. 9, pp. 256-268, 1974.

[4.3] J. R. Brews, W. Fichtner, E. H. Nicollian, and S. M. Sze, "Generalized Guide for MOSFET Miniaturization," *IEEE Electron Device Lett.*, vol. 1, pp. 2-4 , 1980.

[4.4] S. Tang, R. M. Wallace, A. Seabaugh, and D. King-Smith, "Evaluating the Minimum Thickness of Gate Oxide on Silicon using First-Principles Method," *Appl. Surf. Sci.*, vol. 135, pp. 137-142, 1998.

[4.5] D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, "The Electronic Structure at the Atomic Scale of Ultrathin Gate Oxides," *Nature*, pp. 758-761, 1999.

[4.6] C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, and P. Tobin, "Fermi Level Pinning At The Polysi/Metal Oxide Interface," in *IEEE VLSI Tech. Symp. Digest,* pp. 9-10, 2003.

[4.7] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Kohno, T. Chikyo, H. Kitajima, and T. Arikado, "Physics in Fermi Level Pinning at the PolySi/Hf-based High-*k* Oxide Interface," in *IEEE VLSI Tech. Symp. Digest*, pp. 108-109, 2004.

[4.8] Y. Taur, and E. J. Nowak, "CMOS Devices below 0.1 μm: How High Will Performance Go?," in *IEEE Int. Electron Device Meet. Digest*, pp. 215-218, 1997.

[4.9] H.-S. P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann, and J. J .Welser, "Nanoscale CMOS," *Proc. IEEE*, vol. 87, no. 4, pp. 537-570, 1999.

[4.10] H.-S. Wong, and Y. Taur, "Three-Dimensional 'Atomistic' Simulation of Discrete Mircoscopic Random Dopant Distributions Effects in Sub-0.1 μm MOSFET's," in *IEEE Int. Electron Device Meet. Digest*, pp. 705-708, 1993.

[4.11] MEDICI version 4.1 manual, Avant! Corporation, 1998.

[4.12] M. Ieong, H.-S. P. Wong, Y. Taur, P. Oldiges, and D. Frank, "DC and AC Performance Analysis of 25 nm Symmetric/Asymmteric Double-Gate, Back-Gate and Bulk CMOS," in *Int. Conf. Simulation Semiconductor Processes and Devices*, pp. 147-150, 2000.

[4.13] S. Takagi, I. Iwase, and A. Toriumi, "On The Universality Of Inversion-Layer Mobility In N- And P-Channel MOSFET's," in *IEEE Int. Electron Device Meet. Digest*, pp. 398-401, 1988.

[4.14] H.-S. Wong, D. Frank, and P. Solomon, "Device Design Considerations for Double-Gate, Ground-Plane, and Single-gated Ultra-Thin SOI MOSFET's at the 25 nm Channel Length Generation," in *IEEE Int. Electron Device Meet. Digest*, pp. 407-410, 1998.

[4.15] H. Majima, H. Ishikuro, and T. Hiramoto, "Threshold Voltage Increase by Quantum Mechanical Narrow Channel Effect in Ultra-Narrow MOSFETs," in *IEEE Int. Electron Device Meet. Digest*, pp. 379-382, 1999.

[4.16] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, "Quantum-Mechanical Effects On The Threshold Voltage Of Ultrathin-SOI Nmosfets," *IEEE Elec. Dev. Lett.*, vol. 14, pp. 569-571, 1993.

[4.17] Y.-K. Choi, D. Ha, T.-J. King, and C. Hu, "Threshold Voltage Shift by Quantum Confinement in Ultra-Thin Body Devices," in *Dev. Res. Conf.*, pp. 85-86, 2001.

[4.18] H.-S. Wong, K. Chan, and Y. Taur, "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel," in *IEEE Int. Electron Device Meet. Digest*, pp. 427-430, 1997.

[4.19] T. Tanaka, K. Suzuki, H. Horie, and T. Sugii, "Ultrafast Low-Power Operation of p^+–n^+ Double-Gate SOI MOSFET's," in *IEEE VLSI Tech. Symp. Digest*, pp. 11-12, 1994.

[4.20] H.-S. Wong, D. Frank, Y. Taur, and J. Stork, "Design and Performance Considerations for sub-0.1 μm Double-Gate SOI MOSFET's," in *IEEE Int. Electron Device Meet. Digest*, pp. 747-750, 1994.

[4.21] S. Nakajima, K. Miura, T. Somatani, and E. Arai, "A Trench MOSFET with Surface Source/Drain Contacts," in *IEEE Int. Electron Device Meet. Digest*, pp. 200-2003, 1985.

[4.22] S.-H. Oh, J. M. Hergenrother, T. Nigam, D. Monroe, F. P. Klemens, A. Kornblit, W. M. Mansfield, M. R. Baker, D. L. Barr, F. H. Baumann, K. J. Bolan, T. Boone, N. A. Ciampa, R. A. Cirelli, D. J. Eaglesham, E. J. Ferry, A. T. Fiory, J. Frackoviak, J. P. Garno, H. J. Gossmann, J. L. Grazul, M. L. Green, S. J. Hillenius, R. W. Johnson, R. C. Keller, C. A. King, R. N. Kleiman, J. T.-C. Lee, J. F. Miner, M. D. Morris, C. S. Rafferty, J. M. Rosamilia, K. Short, T. W. Sorsch, A. G. Timko, G. R. Weber, G. D. Wilk, and J. D. Plummer, "50 nm Vertical Replacement-Gate (VRG) pMOSFETs," in *IEEE Int. Electron Device Meet. Digest*, pp. 65-68, 2000.

[4.23] Y.-K. Choi, T.-J. King, and C. Hu, "Nanoscale CMOS Spacer FinFET for the Terabit Era," *IEEE Elec. Dev. Lett.*, vol. 23, pp. 25-27, 2002.

[4.24] Y.-K. Choi, L. Change, P. Ranade, J.-S. Lee, D. Ha, S. Balasubramanian, A. Agarwal, M. Ameen, T.-J. King, and J. Bokor, "FinFET Process Refinements For Improved Mobility And Gate Work Function Engineering," in *IEEE Int. Electron Device Meet. Digest*, pp. 269-262, 2002.

[4.25] S.-D. Kim, C.-M. Park, and J. C. S. Woo, "Advanced Model and Analysis of Series Resistance for CMOS Scaling into Nanometer Regime – Part II Quantitative Analysis," *IEEE Trans. Electron Devices,* vol. 49, pp. 467–472, 2002.

[4.26] B. Doyle, R. Arghavani, D. Barlage, S. Datta, M. Doczy, J. Kavalieros, A. Murthy, and R. Chau, "Transistor Elements for 30 nm Physical Gate Lengths and Beyond," *Intel Tech. J.*, vol. 6, pp. 42–54, 2002.

[4.27] B. Doris, M. Ieong, T. Kanarsky, Y. Zhang, R. A. Roy, O. Dokumaci, Z. Ren, F.-F. Jamin, L. Shi, W. Natzle, H.-J. Huang, J. Mezzapelle, A. Mocuta, S. Womack, M. Gribelyuk, E. C. Jones, R. J. Miller, H.-S. P. Wong, and W. Haensch, "Extreme Scaling with Ultra-Thin Si Channel MOSFETs," in *IEEE Int. Electron Devices Meeting Tech. Dig.*, pp. 267–270, 2002.

[4.28] W. B. De Boer, D. Terpstra, and J. G. M. Van Berkum, "Selective versus Nonselective Growth of Si and SiGe," *Mater. Sci. Eng.*, vol. B67, pp. 46–52, 1999.

[4.29] Y.-K. Choi, D. Ha, T.-J. King, and C. Hu, "Nanoscale Ultrathin Body PMOSFET's with Raised Selective Germanium Source/Drain," *IEEE Electron Device Lett.*, vol. 22, pp. 447–448, 2001.

[4.30] S. Zimin, L. Litian, and L. Zhijian, "Optimization of MOSFET's with Polysilicon-Elevated Source/Drain," in *Proc. Int. Conf. Solid-State and Integrated Circuit Tech.*, pp. 188–189, 1998.

[4.31] D. A. Antoniadis, "MOSFET Scalability Limits and New Frontier Devices," in *IEEE VLSI Tech. Symp. Digest*, pp. 2-5, 2002.

[4.32] L. Chang, Y.-K. Choi, D. Ha, P. Ranade, S. Xiong, J. Bokor, C. Hu, and T.-J. King, "Extremely Scaled Silicon Nano-CMOS Devices," *Proc. IEEE*, vol. 91, pp. 1860-1873, 2003.

[4.33] I. De, D. Johri, A. Srivastava, and C. M. Osburn, "Impact of Gate Work-Function on Device Performance at the 50 nm Technology Node," *J. Solid-State Electro.*, vol. 44, pp. 1077-1080, 2000.

[4.34] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, "1-V Power Supply High-Speed Digital Circuit Technology With Multithreshold-Voltage CMOS," *IEEE J. Solid-State Circuits*, vol. 30, no. 8, pp. 847-854, 1995.

L. Wei, Z. Chen, M. Johnson, K. Roy, and V. De, "Design and optimization of low voltage high performance dual threshold CMOS circuits," *in IEEE Proc. 35th Design Automation Conf.*, pp. 489-494, 1998.

[4.35] P. Ranade, Y.-K. Choi, D. Ha, and T.-J. King, "Tunable Work Function Molybdenum Gate Technology For FDSOI-CMOS," in *IEEE Int. Electron Device Meet. Digest*, pp. 363-366, 2002.

[4.36] D. Ha, P. Ranade, Y.-K. Choi, J.-S. Lee, T.-J. King, and C. Hu, "Molybdenum Gate Work Function Engineering for Ultra-Thin-Body Silicon-on-Insulator (UTB SOI) MOSFETs," *Jpn. J. Appl. Phys.*, vol. 42, pp. 1979-1982, 2003.

[4.37] D. Ha, P. Ranade, Y.-K. Choi, J.-S. Lee, T.-J. King, and C. Hu, "Ultra-Thin Body Silicon-On-Insulator (UTB SOI) MOSFET with Metal Gate Work-function Engineering for sub-70 nm Technology Node," in *Int. Conf. Solid-State Dev. Mater.*, pp. 782-783, 2002.

[4.38] Y.-K. Choi, D. Ha, T.-J. King, and C. Hu, "Ultra-Thin Body PMOSFETs with Selectively Deposited Ge Source/Drain," in *IEEE VLSI Tech. Symp. Digest*, pp. 19-20, 2001.

[4.39] P. Ranade, H. Takeuchi, V. Subramanian, and T.-J. King, "Observation Boron and Arsenic Mediated Interdiffusion Across Germanium/Silicon Interfaces," *Electrochem. and Solid-state Lett.*, vol. 5, pp. G5-G7, 2002.

[4.40] J. Chen, R. Solomon, T.-Y. Chan, P.-K. Ko, and C. Hu, "A CV Technique For Measuring Thin SOI Film Thickness," *IEEE Electron Device Lett.*, vol. 12, pp. 453-455, 1991.

[4.41] T. Amada, N. Maeda, and K. Shibahara, "Degradation in a Molybdenum Gate MOS Structure Caused by N+ Ion Implantation for the Work Function Control," in *Proc. Mat. Res. Soc. Symp.*, p. 60, 2002.

[4.42] D. Frank, Y. Taur, and H.-S. P. Wong, "Generalized Scale Length for Two-Dimensional Effects in MOSFET's," *IEEE Elec. Dev. Lett.*, vol. 19, pp. 385-387, 1998.

[4.43] B. Guillaumot, X. Garros, F. Lime, K. Oshima, B. Tavel, J. A. Chroboczek, P. Masson, R. Truche, A. M. Papon, F. Martin, J. F. Damlencourt, S. Maitrejean, M. Rivoire, C. Leroux, S. Cristoloveanu, G. Ghibaudo, J. L. Autran, T. Skotnicki, and S. Deleonibus, "75 nm Damascene Metal Gate and High-*k* Integration for Advanced CMOS Devices," in *IEEE Int. Electron Device Meet. Digest*, pp. 355-358, 2002.

[4.44] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-*k*/Metal-Gate Stack and Its MOSFET Characteristics," *IEEE Elec. Dev. Lett.*, vol. 25, pp. 408-410, 2004.

[4.45] D. Ha, H. Takeuchi, Y.-K. Choi, T.-J. King, W. P. Bai, D.-L. Kwong, A. Agarwal, and M. Ameen, "Molybdenum-Gate HfO_2 CMOS FinFET Technology," to be presented in *IEEE Int. Electron Device Meet. Digest, 2004.*

[4.46] J.-T. Park, J.-P. Colinge, and C. H. Diaz, "Pi-Gate SOI MOSFET," *IEEE Elec. Dev. Lett.*, vol. 22, pp. 405-406, 2001.

[4.47] D. Ha, H. Takeuchi, Y.-K. Choi, and T.-J. King, "Molybdenum Gate Technology for Ultra-Thin-Body MOSFETs and FinFETs," *IEEE Trans. Elec. Dev.*, vol. 51, pp. 1989-1996, 2004.

[4.48] Y.-C. Yeo, P. Ranade, T.-J. King, and C. Hu, "Effects of High-*k* Gate Dielectric Materials on Metal and Silicon Gate Workfunctions," *IEEE Elec. Dev. Lett.*, vol. 23, no. 6, pp. 342-344, 2002.

[4.49] H. Takeuchi, H. Y. Wong, D. Ha, and T.-J. King, "Impact of Oxygen Vacancies on High-*k* Gate Stack Engineering," to be presented in *IEEE Int. Elec. Dev. Meet. Digest*, 2004.

[4.50] H. Park, E.C. Jones, P. Ronsheim, C. Cabral, Jr., C. D'Emic, G. M. Cohen, R. Young, and W. H. Rausch, "Dopant Redistribution in SOI during RTA: a Study on Doping in Scaled-Down Si Layers," in *IEEE Int. Electron Device Meet. Digest*, pp. 337-340, 1999.

[4.51] Shred simulation (available at http://www.nanohub.org).

[4.52] J.-P. Han, E. M. Vogel, E. P. Gusev, C. D'Emic, C. A. Richter, D. W. Heh, and J. S. Suehle, "Asymmetric Energy Distribution of Interface Traps in n- and p-MOSFETs with HfO_2 Gate Dielectricon Ultrathin SiON Buffer Layer," *IEEE Elec. Dev. Lett.*, vol. 25, pp. 126-128, 2004.

[4.53] K. Sekine, S. Inumiya, M. Sato, A. Kaneko, K. Eguchi, and Y. Tsunashima, "Nitrogen Profile Control By Plasma Nitridation Technique For Poly-Si Gate Hfsion CMOSFET With Excellent Interface Property And Ultra-Low Leakage Current," in *IEEE Int. Electron Device Meet. Digest*, pp. 103-106, 2003.

[4.54] W. Zhu, J.-P. Han, and T. P. Ma, "Mobility Measurement And Degradation Mechanisms Of Mosfets Made With Ultrathin High-K Dielectrics," *IEEE Trans. Elec. Dev.*, vol. 51, pp. 98-105, 2004.

[4.55] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On The Universality Of Inversion Layer Mobility In Si MOSFET's: Part II-Effects Of Surface Orientation," *IEEE Trans. Elec. Dev.*, vol. 41, pp. 2363-2368, 1994.

[4.56] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective Electron Mobility in Si Inversion Layers in Metal-Oxide-Semiconductor Systems with a High-*k* Insulator: The Role of Remote Phonon Scattering," *J. Appl. Phys.*, vol. 90, pp. 4587-4608, 2001.

[4.57] Z. Ren, M. V. Fischetti, E. P. Gusev, E. A. Cartier, and M. Chudzik, "Inversion Channel Mobility In High-*k* High Performance MOSFETs," in *IEEE Int. Electron Device Meet. Digest*, pp. 793-796, 2003.

[4.58] J. Robertson, "Band Offsets of Wide-Band-Gap Oxides and Implications for Future Electronic Devices," *J. Vac. Sci. Technol. B*, vol. 18, pp. 1785-1791, 2000.

Chapter 5

Conclusion

5.1 Summary of Contributions

Technological innovation has accomplished remarkable progress in the semiconductor industry and CMOS scaling well into the nanometer regime [5.1, 5.2]. Technological challenges in the near future, however, should be overcome for the reduction of standby power consumption without aggravating the device performance. This dissertation addressed the important issues and technological barriers for the integration of advanced gate stack materials and transistor structures into nanoscale CMOS technologies.

To continue CMOS scaling, key technological innovations for advanced thin-body transistor structures are presented. The use of ultra-thin silicon body can suppress the short channel effects effectively, thus eliminating the need of heavy channel doping and state-of-the-art thin gate oxide. Undoped or lightly doped channel can improve the channel carrier mobility due to the reduced impurity scattering and vertical electric field, and eliminating the troublesome issues such as statistical random dopant fluctuation. Self-limited junction depth to ultra-thin body thickness significantly reduces parasitic junction capacitance and leakage current. These benefits combined will significantly improve the overall circuit performance without degrading the standby power consumption.

The most pressing challenge to realize these benefits is the adjustment of threshold voltage. The ideal solution is the gate work function engineering technology; other potential solutions such as heavy channel doping and asymmetrical double gate structures will lose many of the above benefits [5.3]. For the first time, tunable molybdenum (Mo) gate work function technology is demonstrated to adjust the threshold voltage of ultra-thin body (UTB) MOSFETs. Integration of Mo technology and high-*k* dielectric (HfO_2) employing FinFETs is demonstrated, for the first time. For these

implementations, two process technologies were developed; damage-free sputtering and high-selectivity dry etching of Mo films.

Major conclusions on the topics listed above are summarized as follows.

5.1.1 Metal Gate Technology

Metal gate electrodes in a CMOS transistor eliminate problems such as the poly-Si gate depletion (PDE), boron dopant penetration, and high sheet resistance. Material selection criteria for integration of alternative gate electrode materials were summarized.

Molybdenum (Mo) is a promising candidate gate material. Two critical process technologies were developed for Mo gate films; *damage-free sputtering and high-selectivity dry etching*. With a plasma charge trap (PCT), sputtering damage to the gate dielectric can be minimized for improved drive current and gate oxide integrity (GOI). Mo gate can be patterned without leaving any residue or stringers due to the highly selective etch process and directly applicable to advanced thin-body transistor structures.

The work function of Mo gate can be tuned by nitrogen implantation followed by a thermal anneal, to provide a means for adjusting the threshold voltage of advanced thin-body transistor structures. The work function shift of nitrogen implanted Mo gate is

resulted from the simultaneous modification of the microstructure and chemistry of Mo film at the gate dielectric interface.

5.1.2 High-k Gate Dielectric Technology

High-*k* gate dielectrics decrease the leakage current through the dielectric while maintaining the same gate capacitance, thus are indispensable for the low-power potable application of nanoscale CMOS technologies. The key basic material properties for integration of alternative gate dielectric materials were summarized.

Hafnium oxide (HfO_2) is one of the most promising candidates to replace the silicon dioxide (SiO_2). Through experimental device fabrication, the impact of gate process (poly-Si *vs.* poly-SiGe) technology on equivalent-oxide-thickness (EOT) and leakage current was investigated; thermal budget reduction and careful selection of gate electrode material leads to thinner EOT and smaller gate leakage current. The impact of oxygen vacancies in HfO_2 gate dielectric was discussed. Generation of oxygen vacancies in HfO_2 is thermodynamically driven and causes Si interfacial layer formation and gate Fermi-level pinned in MOS devices.

Successful integration of HfO_2 into CMOS fabrication depends on the minimization of oxygen vacancy formation through careful selection of the gate electrode materials and reduction of post-gate-deposition thermal budget.

5.1.3 Advanced Transistor Structures

Advanced thin-body transistor structures suppress the short channel effects without the use of heavy channel doping and ultra thin gate oxide thickness. Design methodology and challenges were investigated. Adjustment of the desired threshold voltages to maximize the performance benefits is a serious challenge; the ideal solution is the metal gate work function engineering.

Tunable work function Mo gate is demonstrated to be a feasible approach for adjusting the threshold voltages of UTB MOSFETs for the first time. The range of work function values achieved with Mo gate technology makes it an attractive candidate for advanced thin-body transistor structures. Integration of metal gate and high-*k* dielectric employing FinFETs is demonstrated for the first time; Mo-gated HfO_2 CMOS FinFETs achieved the reduction of gate leakage current over 3 orders-of-magnitude for inversion

equivalent oxide thickness down to 1.72 nm. Measured carrier mobilities are comparable to previously reported works, which is limited by the soft phonon scattering.

Further process optimization is needed to prevent nitrogen diffusion into the HfO_2 gate dielectric to make Mo-gated HfO_2 FinFET technology suitable for future nanoscale CMOS technologies.

5.2 Suggestions for Future Work

5.2.1 Mobility Enhancement for Advanced Transistor Structures

Process-induced strain in the channel of a MOSFET can enhance mobility and hence circuit performance, and is already employed in CMOS production today [5.4]. For a p-channel bulk-Si MOSFET, uniaxial compressive strain induced by epitaxially grown $Si_{1-x}Ge_x$ source/drain regions is very effective for enhancing hole mobility [5.4]. This approach may not be directly applicable to advanced thin-body transistor structures, however, because of the lack of a crystalline Si lattice directly beneath the source/drain regions to serve as a template for epitaxial growth of $Si_{1-x}Ge_x$. Biaxially tensile strained (in the plane parallel to the wafer surface) silicon-on-insulator (SOI) films can be

achieved with a wafer-bonding process [5.5]; however, this approach is relatively expensive and would not provide biaxial strain in the plane of current conduction for the FinFET structure. Therefore, alternative approaches to inducing strain in the channel of advanced thin-body FET structures are necessary through a stressed capping layer, stressed gate electrode(s), or strained-$Si_{1-x}Ge_x$ S/D regions.

5.2.2 Reliability of Advanced Materials and Transistor Structures

Investigation of reliabilities for advanced thin-body transistor structures such as hot carrier injection, gate dielectric integrity, and low-frequency noise should be carried out before putting such device structures into mass-production. Nonetheless, only a few works for the advanced transistor structures has been done to date [5.6, 5.7, 5.8].

Thinner silicon body is helpful to reduce the hot carrier injection, thus improving the hot carrier reliability due to the reduced electron temperature and generated electron-hole pair generation rate [5.6]. On the other hand, the use of silicon surface orientation other than (100) and rough surface with plasma etching damage together with nitrogen implantation into Mo-gate may cause degradation in gate oxide integrity, necessitating proper treatments such as hydrogen annealing and so on [5.9, 5.10]. While these

advanced transistor structures with advanced gate stack materials may appear immune to hot carrier reliability [5.6, 5.11], more detail and comprehensive reliability studies are in pressing need for the adaptation into IC production.

5.3 References

[5.1] G. E. Moore, "No Exponential Is Forever: But "Forever" Can Be Delayed!," in *Int. Solid State Circuits Conf. Dig.*, pp. 20-23, 2003.

[5.2] H.-S. P. Wong, D. J. Frank, P. M. Solomon, C. H. J. Wann, and J. J .Welser, "Nanoscale CMOS," *Proc. IEEE*, vol. 87, no. 4, pp. 537-570, 1999.

[5.3] L. Chang, "Nanoscale Thin-Body CMOS Devices," *Ph.D Thesis*, University of California, Berkeley, 2003.

[5.4] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," in *IEEE Int. Elec. Dev. Meet. Tech. Dig.*, pp.978-980, 2003.

[5.5] K. Rim, K. Chan, L. Shi, D. Boyd, J. Ott, N. Klymko, F. Cardone, L. Tai, S. Koester, M. Cobb, D. Canaperi, B. To, E. Duch, I. Babich, R. Carruthers, P. Saunders, G. Walker, Y. Zhang, M. Steen, and M. Ieong, "Fabrication and Mobility Characteristics of Ultra-Thin

Strained Si Directly on Insulator (SSDOI) MOSFETs," in *IEEE Elec. Dev. Meet. Tech. Dig.*, pp. 49-52, 2003.

[5.6] Y.-K. Choi, D. Ha, E. Snow, J. Bokor, and T.-J. King, "Reliability Study of CMOS FinFETs," in *IEEE Elec. Dev. Meet. Tech. Dig.*, pp. 177-180, 2003.

[5.7] S. Maeda, J.-A. Choi, J.-H. Yang, Y.-S. Jin, S.-K. Bae, Y.-W. Kim, and K.-P. Suh, "Negative Bias Temperature Instability in Triple Gate Transistors," in *IEEE Proc. Int. Reliabilty Phy. Symp. Tech. Dig.*, pp. 177-180, 2003.

[5.8] J.-S. Lee, Y.-K. Choi, D. Ha, S. Balasubramanian, T.-J. King, and J. Bokor, "Hydrogen Annealing Effect on DC and Low-Frequency Noise Characteristics in CMOS FinFETs," in *IEEE Electron Device Letters*, vol. 24, no. 3, pp. 186-188, 2003.

[5.9] K. Sekine, S. Inumiya, M. Sato, A. Kaneko, K. Eguchi, and Y. Tsunashima, "Nitrogen Profile Control By Plasma Nitridation Technique For Poly-Si Gate Hfsion CMOSFET With Excellent Interface Property And Ultra-Low Leakage Current," in *IEEE Int. Elec. Dev. Meet. Digest*, pp. 103-106, 2003.

[5.10] A. I. Chou, C. Lin, K. Kumar, P. Chowdhury, M. Gardner, M. Gilmer, J. Fulford, and J. C. Lee, "The effects of nitrogen implant into gate electrode on the characteristics of dual-gate MOSFETs with ultra-thin oxide and oxynitrides," in *IEEE Proc. Int. Reliability Phys. Symp.*, pp. 174-177, 1997.

[5.11] Q. Lu, H. Takeuchi, R. Lin, T.-J. King, C. Hu, K. Onishi, R. Choi, C.-S. Kang, and J. C. Lee, "Hot Carrier Reliability of n-MOSFET with Ultra-Thin HfO_2 Gate Dielectric and Poly-Si Gate," in *IEEE Proc. Int. Reliability Phys. Symp.*, pp. 429-431, 2002.

Appendix A

Fabrication Processes for Mo-gated UTB MOSFETs

STEP	PROCESS	CONDITIONS	EQUIPMENT	COMMENT
	Initial wafers	4" (100) p-type 100nm thick SOI with 400 nm BOX		Unibond® SOI
0.0	**LABELING**			
0.1	Label		Diamond pencil	
0.2	DI Rinse	3 Cycle DI Water Rinse	Sink6	
0.3	Thickness Measure	Silicon	NanoDuv	R:4
0.4	HF Cleaning	10:1 HF 5min	Sink6	
1.0	**BODY THINNING**			
1.1	Piranha Cleaning	120°C 10min	Sink6	
1.2	Wet Oxidation	Wet O_2 850°C 90min	Tystar2	R:SWETOXB
1.3	Wet Etching	10:1 HF 10min	Sink6	
1.4	Thickness Measure	Silicon	NanoDuv	R:4
1.5	Piranha Cleaning	120°C 10min	Sink6	
1.6	Wet Oxidation	Wet O_2 850°C 60min	Tystar2	R:SWETOXB
1.7	Wet Etching	10:1 HF 5min	Sink6	
1.8	Thickness Measure	Silicon	NanoDuv	R:4
1.9	Piranha Cleaning	120°C 10min	Sink6	
1.10	Dry Oxidation	Dry O_2 850°C 15min	Tylan6	R:SGATEOX
1.11	Wet Etching	10:1 HF 2min	Sink6	
1.12	Thickness Measure	Silicon	NanoDuv	R:4
2.0	**ACTIVE**			
2.1	HMDS	120°C 1min	Primeoven	R:0
2.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
2.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: Active
2.4	Post Exp. Bake	120°C 1min	Svgdev	
2.5	Develop	60sec	Svgdev	OPD4262
2.6	Hard Bake	120°C 10min	Vwroven	

STEP	PROCESS	CONDITIONS	EQUIPMENT	COMMENT
2.7	Active Dry Etching	Lam5 BT: TP/BP=200/40W 30mT CF_4=100sccm 7sec ME: TP/BP=300/150W 15mT Cl_2/HBr =50/150scm EPD OE: TP/BP=70/30W 15mT HBr/He/O_2=50/50/1 sccm 15sec		
2.8	Thickness Measure	Buried Oxide	NanoDuv	R:1
2.9	PR Ashing	O_2 300W 5min	Technics-C	
2.10	Piranha Cleaning	120°C 10min	Sink8	
2.11	CD Measure	SEM	LEO	
3.0	**GATE STACK**			
3.1	Piranha Cleaning	120°C 10min	Sink6	
3.2	HF Cleaning	25:1 HF 30sec	Sink6	
3.3	Gate Oxidation	Dry O_2 750°C 13min 30sec N_2 900 °C 20min	Tylan5	R:Thin_Ann
3.4	Thickness Measure	Oxide (monitor wafer)	Sopra	
3.5	Mo Deposition	200°C 300W 10mT	UHV Sputtering	Without PCT
3.6	Rs Measure	Monitor wafer	4PointProbe	
4.0	**NITROGEN IMPLANTATION**			
4.1	HMDS	120°C 1min	Primeoven	R:0
4.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
4.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: Blank
4.5	Develop	60sec	Svgdev	OPD4262
4.6	Nitrogen Implant	$^{14}N^+$ 20KeV (dose split)	Implant Service	Foundry Company
4.7	PR Ashing	O_2 200W 7min	Technics-C	
4.8	PR Strip	Acetone	Manual Bath	
4.9	HF Cleaning	25:1 HF 20"	Sink7	
4.10	N^+ Poly-Si Deposition	Nucleation: 550°C 300mT SiH_4=200sccm 1min Deposition: 550°C 300mT SiH_4/PH_3=200/5sccm		Tystar19 (dedicated boat)
4.11	Thickness Measure	Silicon (monitor wafer)	NanoDuv	R:4
4.12	LTO Deposition	450°C 6min undoped	Tystar11	R:11SULTOA
4.13	Thickness Measure	Oxide (monitor wafer)	NanoDuv	
5.0	**GATE**			
5.1	HMDS	120°C 1min	Primeoven	R:0
5.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i

STEP	PROCESS	CONDITIONS	EQUIPMENT	COMMENT
5.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: Gate
5.4	Post Exp. Bake	120°C 1min	Svgdev	
5.5	Develop	60sec	Svgdev	OPD4262
5.6	Hard Bake	120°C 1min	Vwroven	
5.7	CD Measure	SEM	LEO	
5.8	Ashing	O_2 30W 1min	Technics-C	Repeat
5.9	CD Measure	SEM	LEO	
5.10	Gate Stack Dry Etching	Equipment: Lam5 BT: TP/BP=200/40W 30mT CF_4=100sccm 60sec Poly-Si ME: TP/BP=300/150W 15mT Cl_2/HBr=50/150 sccm EDP + 10sec Mo ME: TP/BP=150/100W 13mT Cl_2/O_2=70/60 sccm EDP + 20sec		
5.11	HF Cleaning	200:1 HF 30sec	Sink7	
5.12	PR Ashing	O_2 200W 7min	Technics-C	Repeat
5.13	HF Cleaning	200:1 HF 15sec	Sink7	
5.14	Polymer Removal	Acetone	Manual Bath	
5.15	LTO Deposition	450°C 1min Undoped	Tystar11	R:11SULTOA
5.16	Thickness Measure	Buried Oxide & monitor wafer	NanoDuv	
5.17	Spacer Dry Etching	Equipment: Lam5 TP/BP=200/40W 30mT CF_4=100sccm 30sec		
5.18	HF Cleaning	25:1 HF 10sec	Sink7	
6.0	**SELECTIVELY RAISED GE SOURCE/DRAIN**			
6.1	HF Cleaning	200:1 HF 30sec	Sink7	
6.2	Ge Deposition	340°C 300mT GeH_4=200sccm 10min	Tystar19	
6.3	LTO Deposition	450°C 90sec Undoped	Tystar11	R:11SULTOA
7.0	**N+ SOURCE/DRAIN IMPLANTATION**			
7.1	HMDS	120°C 1min	Primeoven	R:0
7.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
7.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: N+ Active
7.4	Post Exp. Bake	120°C 1min	Svgdev	
7.5	Develop	60sec	Svgdev	OPD4262
7.6	Hard Bake	120°C 10min	Vwroven	
7.7	N+ Implant	As 40KeV 5E15cm^{-2} Tilt 0°	Implant Service	Foundry Company
7.8	PR Ashing	O_2 300W 5min	Technics-C	

STEP	PROCESS	CONDITIONS	EQUIPMENT	COMMENT
7.9	Piranha Cleaning	120°C 5min	Sink8	
8.0	**P+ SOURCE/DRAIN IMPLANTATION**			
8.1	HMDS	120°C 1min	Primeoven	R:0
8.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
8.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: P+ Active
8.4	Develop	60sec	Svgdev	OPD4262
8.5	P+ Implant	B 20KeV 3E15cm^{-2} Tilt 0°	Implant Service	Foundry Company
8.6	PR Ashing	O_2 300W 5min	Technics-C	
8.7	Piranha Cleaning	120°C 5min	Sink8	
8.8	Piranha Cleaning	120°C 5min	Sink6	
8.9	RTA	N_2 700°C 60sec	Heatpulse3	
9.0	**METAL CONTACT**			
9.1	LTO Deposition	450°C 20min Undoped	Tystar11	ILD1
9.2	HMDS	120°C 1min	Primeoven	R:0
9.3	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
9.4	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: MC
9.5	Post Exp. Bake	120°C 1min	Svgdev	
9.6	Develop	60sec	Svgdev	OPD4262
9.7	Hard Bake	120°C 20min	Vwroven	
9.8	Contact Etching	Equipment: Lam5 TP/BP=200/40W 30mT CF_4=100sccm 3min		
9.9	Thickness Measure	Buried Oxide	NanoDuv	
9.10	HF Cleaning	25:1 HF 1min	Sink7	Repeat
9.11	Thickness Measure	Buried Oxide	NanoDuv	
9.12	PR Ashing	O_2 300W 5min	Technics-C	
9.13	Piranha Cleaning	120°C 5min	Sink8	
9.14	HF Wet Etching	25:1 HF 30sec	Sink7	
9.15	Al Deposition	6mT 15cm/min 1pass	Cpa	
10.0	**METALLIZATION**			
10.1	HMDS	120°C 1min	Primeoven	R:0
10.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
10.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: Metal

STEP	PROCESS	CONDITIONS	EQUIPMENT	COMMENT
10.4	Post Exp. Bake	120°C 1min	Svgdev	
10.5	Develop	60sec	Svgdev	OPD4262
10.6	Hard Bake	120°C 20min	Vwroven	
10.7	Al Wet Etching	Al Etchant	Sink8	
10.8	Thickness Measure	Buried Oxide	NanoDuv	
10.9	PR Ashing	O_2 300W 5min	Technics-C	
10.10	DI Rinse	3 Cycle DI Water Rinse	Sink8	
10.11	Sintering	400°C 10% H_2 30min	Tylan13	R:VSINT400

Appendix B

Fabrication Processes for Mo-gated HfO_2 FinFETs

STEP	PROCESS	CONDITIONS	EQUIPMENT	COMMENT
	Initial wafers	4" (100) p-type 100nm thick SOI with 400 nm BOX		Unibond® SOI
0.0	**LABELING**			
0.1	Label		Diamond pencil	
0.2	DI Rinse	3 Cycle DI Water Rinse	Sink6	
0.3	Thickness Measure	Silicon	NanoDuv	R:4
0.4	HF Cleaning	10:1 HF 5min	Sink6	
1.0	**BODY THINNING**			
1.1	Piranha Cleaning	120°C 10min	Sink6	
1.2	Wet Oxidation	Wet O_2 850°C 100min	Tystar2	R:SWETOXB
1.3	Wet Etching	10:1 HF 10min	Sink6	
1.4	Thickness Measure	Silicon	NanoDuv	R:4
1.5	Piranha Cleaning	120°C 10min	Sink6	
1.6	Dry Oxidation	Dry O_2 900°C 4min	Tylan6	R:SGATEOX
1.7	Piranha Cleaning	120°C 10min	Sink6	
1.8	Sac. SiGe Deposition	Tystar19 Nucleation: 550°C 300mT SiH_4=200sccm 30sec Deposition: 450°C 300mT SiH_4/GeH_4=124/80sccm 30sec 18min		
1.9	Measurement	SiGe	α-step	
2.0	**ACTIVE FIN**			
2.1	HMDS	120°C 1min	Primeoven	R:0
2.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
2.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: Fin
2.4	Post Exp. Bake	120°C 1min	Svgdev	
2.5	Develop	60sec	Svgdev	OPD4262
2.6	Hard Bake	120°C 10min	Vwroven	
2.7	Sac SiGe Etching	Lam5 BT: TP/BP=200/40W 30mT CF_4=100sccm 7sec ME: TP/BP=300/150W 15mT Cl_2/HBr=50/150sccm EDP+5sec		

STEP	PROCESS	CONDITIONS	EQUIPMENT	COMMENT
2.8	HF Cleaning	200:1 HF 10sec	Sink7	
2.9	PR Ashing	O_2 300W 5min	Technics-C	
2.10	HF Cleaning	200:1 HF 10sec	Sink7	
2.11	Piranha Cleaning	120°C 10min	Sink8	
2.12	LTO Deposition	450°C 3min Undoped	Tystar11	Spacer Lithography
2.13	Thickness Measure	Oxide	NanoDuv	
3.0	ALIGNMENT KEY PROTECTION			
3.1	HMDS	120°C 1min	Primeoven	R:0
3.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
3.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: Alignment
3.4	Post Exp. Bake	120°C 1min	Svgdev	
3.5	Develop	60sec	Svgdev	OPD4262
3.6	Hard Bake	120°C 10min	Vwroven	
3.7	LTO Spacer Etching	Lam5 TP/BP=200/40W 30mT CF_4=100sccm 30sec (EPD detection)		
3.8	SiGe Removal	Lam5 BT: TP/BP=200/40W 30mT CF_4=100sccm 7sec ME:TP/BP=250/120W 35mT HBr/O2=200/5 60sec		
3.9	HF Cleaning	200:1 HF 10sec	Sink7	
3.10	PR Ashing	O_2 300W 5min	Technics-C	
3.11	HF Cleaning	200:1 HF 10sec	Sink7	
3.12	Piranha Cleaning	120°C 10min	Sink8	
4.0	ACTIVE PAD			
4.1	HMDS	120°C 1min	Primeoven	R:0
4.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
4.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: Active
4.4	Post Exp. Bake	120°C 1min	Svgdev	
4.5	Develop	60sec	Svgdev	OPD4262
4.6	Hard Bake	120°C 1min	Vwroven	
4.7	Ashing	O_2 30W 1min	Technics-C	Repeat
4.8	CD Measure	SEM	LEO	
4.9	Active Etching	Lam5 BT: TP/BP=200/40W 30mT CF_4=100sccm 40sec ME: TP/BP=300/150W 15mT Cl_2/HBr=50/150 sccm EDP + 5sec		
4.10	HF Cleaning	200:1 HF 10sec	Sink7	

STEP	PROCESS	CONDITIONS	EQUIPMENT	COMMENT
4.11	PR Ashing	O_2 300W 5min	Technics-C	
4.12	HF Cleaning	200:1 HF 10sec	Sink7	
4.13	Piranha Cleaning	120°C 10min	Sink8	
4.14	CD Measure	SEM	LEO	
4.15	Piranha Cleaning	120°C 10min	Sink6	
4.16	Sac. Oxidation	Dry O_2 900°C 3min	Tylan6	R:SGATEOX
4.17	Thickness Measure	Oxide	NanoDuv	
5.0	**GATE STACK**			
5.1	HF Cleaning	25:1 HF 60sec		Univ of Texas, Austin
5.2	Surface Treatment	NH_3 700°C 500T 10sec		
5.3	HfO_2 Deposition	500°C 4T 3min $Hf(OC(CH_3)_3)_4$		
5.4	Post Depo. Treatment	N_2 700°C 500T 30sec		
5.5	Mo Deposition	200°C 300W 10mT	Novellus	With PCT
5.6	Rs Measure	Monitor wafer		
6.0	**NITROGEN IMPLANTATION**			
6.1	HMDS	120°C 1min	Primeoven	R:0
6.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
6.3	Expose	Focus: 248 ET: 5.0sec	Gcaws1,2	Mask: Blank
6.5	Develop	60sec	Svgdev	OPD4262
6.6	Nitrogen Implant	$^{14}N^+$ 5KeV 1E16cm^{-2} 30° tilt		Axcelis Inc.
6.7	PR Ashing	O_2 200W 7min	Technics-C	
6.8	PR Strip	Acetone	Manual Bath	
6.9	HF Cleaning	25:1 HF 20sec	Sink7	
6.10	N^+ Poly-Si Deposition	Nucleation: 550°C 300mT SiH_4=200sccm 1min Deposition: 550°C 300mT SiH_4/PH_3=200/5sccm		Tystar19 (dedicated boat)
6.11	Thickness Measure	Silicon (monitor wafer)	NanoDuv	
6.12	CMP	CMP DF=8psi Table/Chuck=24/6rpm BP=1psi Slurry=100ml/min		
6.13	Post Cleaning	Sink8 DI Rinse NH_4OH 1min Piranha 120°C 1min 5:1 BHF 10sec		
6.14	Post Cleaning2	Manual Bath $H_2O/NH_4OH/H_2O_2$=5/1/1 65°C 5min		
6.15	Thickness Measure	Silicon (monitor wafer)	NanoDuv	R:4
6.16	LTO Deposition	450°C 8min30sec undoped	Tystar11	R:11SULTOA

STEP	PROCESS	CONDITIONS	EQUIPMENT	COMMENT
6.17	Thickness Measure	Oxide (monitor wafer)	NanoDuv	
7.0	**GATE**			
7.1	HMDS	120°C 1min	Primeoven	R:0
7.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
7.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: Gate
7.4	Post Exp. Bake	120°C 1min	Svgdev	
7.5	Develop	60sec	Svgdev	OPD4262
7.6	CD Measure	SEM	LEO	
7.7	Ashing	O_2 30W 1min	Technics-C	Repeat
7.8	CD Measure	SEM	LEO	
7.9	LTO Dry Etching	Lam5 BT: TP/BP=200/40W 30mT CF_4=100sccm 60sec		
7.10	PR Ashing	O_2 200W 7min	Technics-C	
7.11	CD Measure	SEM	LEO	
7.12	LTO Trimming	200:1 HF 30sec	Sink7	Repeat
7.13	CD Measure	SEM	LEO	
7.14	Gate Stack Dry Etching	Lam5 BT: TP/BP=200/40W 30mT CF_4=100sccm 60sec Poly-Si ME: TP/BP=300/150W 15mT Cl_2/HBr=50/150 sccm EDP + 10sec Mo ME: TP/BP=150/100W 13mT Cl_2/O_2=70/60 sccm EDP + 20sec		
7.15	HF Cleaning	200:1 HF 30sec	Sink7	
7.16	Polymer Removal	Acetone	Manual Bath	
7.17	DI Rinse	3 Cycle DI Water Rinse	Sink8	
8.0	**N+ SOURCE/DRAIN IMPLANTATION**			
8.1	HMDS	120°C 1min	Primeoven	R:0
8.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
8.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: N+ Active
8.4	Develop	60sec	Svgdev	OPD4262
8.5	N+ Implant	P 40&30KeV 2E15cm^{-2} Tilt 0°		Axcelis Inc.
8.6	PR Ashing	O_2 200W 7min	Technics-C	
8.7	PR Strip	Acetone	Manual Bath	
8.8	DI Rinse	3 Cycle DI Water Rinse	Sink8	
9.0	**P+ SOURCE/DRAIN IMPLANTATION**			
9.1	HMDS	120°C 1min	Primeoven	R:0

STEP	PROCESS	CONDITIONS	EQUIPMENT	COMMENT
9.2	PR Coating	1.1μm 90°C Soft Bake	Svgcoat1,2	OCG OiR 897-10i
9.3	Expose	Focus: 248 ET: 3.1sec	Gcaws1,2	Mask: P+ Active
9.4	Develop	60sec	Svgdev	OPD4262
9.5	P+ Implant	BF_2 25KeV 3E15cm^{-2} Tilt 0°	Implant Service	Foundry Company
9.6	PR Ashing	O_2 300W 5min	Technics-C	
9.7	PR Strip	Acetone	Manual Bath	
9.8	DI Rinse	3 Cycle DI Water Rinse	Sink8	
9.9	RTA	N_2 900°C 60sec		
9.10	DI Rinse	3 Cycle DI Water Rinse	Sink8	
9.11	Sintering	600°C 10% H_2 30min	Tylan18	R:H2SINT6A
9.12	Sintering	400°C 10% H_2 (D_2) 30min	Tylan18	R:H2SINT4A