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MICRO POWER RADIO FREQUENCY OSCILLATOR DESIGN

by

Nathan M. Pletcher

Memorandum No. UCB/ERL M05/4

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ELECTRONICS RESEARCH LABORATORY

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Micro Power Radio Frequency Oscillator Design

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December 21, 2004

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by Nathan M. Pletcher

Research Project

Submitted to the Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, in partial satisfaction of the requirements for the degree of **Master of Science, Plan II**.

Approval for the Report and Comprehensive Examination:

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Dec 14, 2004
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* * * * * *

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Table of Contents

List of Figures iii

List of Tables v

Acknowledgments vii

1 Introduction 1

1.1 Motivation 1

1.2 Thesis Organization 2

2 Background 3

2.1 The PicoRadio Project 3

2.2 Reactive Radio Architecture 5

3 Low Power Analog Techniques 9

3.1 Introduction 9

3.2 Design for Low Supply Voltage 10

3.2.1 Trends in CMOS Supply 10

3.2.2 Opportunities for Reduced Supply 12

3.3 Subthreshold Operation 14

3.3.1 Basics of Subthreshold Operation 17

3.3.2 Benefits of Subthreshold Operation 22

3.3.3 Challenges for Subthreshold RF Circuits 23

3.3.4 Inversion Coefficient Methodology for Design 29

4 Integrated Inductors 37

4.1 Introduction 37

4.2 Structure and Layout 38

4.2.1 Inductance 39
4.2.2 Quality Factor 40
4.2.3 Self-Resonant Frequency 41
4.2.4 Loss Mechanisms 41
4.3 Inductor Modeling 42
4.4 Measurements and Parameter Extraction 44
4.4.1 Inductor Measurement Process 46
4.4.2 De-embedding Procedure 48
4.4.3 Extraction of Final Model Parameters 49
4.5 RF-MEMS 53

5 Oscillator Design **55**
5.1 Introduction 55
5.2 Design Objectives 55
5.3 CMOS Oscillator Background 56
5.4 Topology Choice 59
5.5 Circuit Design 61
5.5.1 Oscillator Core 61
5.5.2 Output Buffer 69
5.6 Implementation and Layout 72

6 Results **77**
6.1 Measurement Setup and Instrumentation 77
6.2 Nominal Performance 78
6.3 Performance Across Bias Conditions 79
6.3.1 Varying Supply Voltage 79
6.3.2 Varying Bias Current 82
6.4 Phase Noise Performance 84
6.5 Comparison to Traditional Oscillators 87

7 Conclusions **89**
7.1 Summary of results 89
7.2 Future Work 90

List of Figures

2.1 Reactive radio system block diagram 6

3.1 ITRS projections for CMOS supply voltage scaling 11
3.2 Schematic of low voltage LC oscillator 13
3.3 g_m/I_D and f_T for a modern CMOS 0.13μm process 16
3.4 I_D vs. V_{GS} ($V_{DS} = 50$mV), comparing strong and weak inversion models 20
3.5 Comparison of f_T with technology scaling 25
3.6 Comparison of g_m/I_D with technology scaling 26
3.7 Comparison of g_m/I_D for BSIM3v3 and MM11 models 28
3.8 Comparison of g_m/I_D for dual-threshold NMOS and PMOS devices . 32
3.9 Comparison of g_m/I_D for different device lengths 33
3.10 Comparison of g_m/I_D across process corners 34
3.11 Comparison of g_m/I_D for different substrate bias 35

4.1 Sample layout of integrated inductor illustrating design parameters . 39
4.2 Equivalent circuit for simple π-model 43
4.3 Equivalent circuit for a more complex π-model 44
4.4 Photograph of inductor test structure 45
4.5 Measured raw s-parameter magnitude for inductor test structure . . . 47
4.6 Block diagram of de-embedding flow 48
4.7 Admittance network representation of inductor model 49
4.8 Model parameters as a function of frequency from measured data . . 51
4.9 Overall Q factor for measured inductor 52

5.1 Simple model of oscillator as resonant tank 56
5.2 Root locus of basic oscillator model in (a) startup and (b) steady-state 57
5.3 (a) Colpitts topology (b) Cross-coupled differential topology 59
5.4 Complete schematic of final oscillator design 62

5.5 Operating point of M_1 and M_2 on inversion coefficient curve 68
5.6 Complete schematic of output buffer 70
5.7 Layout capture of basic inductor $L2$ 74
5.8 Layout capture of advanced inductor $L3$ with shield 74
5.9 Photo of oscillator with $L2$ 75
5.10 Photo of oscillator with $L3$ 75

6.1 Measured output spectrum and startup transient 78
6.2 Variation of frequency for range of V_{DD} 80
6.3 Variation of output swing for range of V_{DD} 81
6.4 Variation of frequency for range of I_{bias} 83
6.5 Variation of output swing for range of I_{bias} 83
6.6 Photo of bonded oscillator on printed circuit board 84
6.7 Measured phase noise spectrum 85
6.8 Measured spot phase noise at 1 MHz offset for range of V_{DD} 86

List of Tables

3.1 Extracted I_0 values for selected devices 31

4.1 Extracted inductor model parameters for design 51

5.1 Device type, sizing, and IC for oscillator and buffer transistors 72

6.1 Comparison to other published work 87

Acknowledgments

The work presented in this thesis would not have been possible without the direct influence and aid of quite a few individuals. The last two and a half years at Berkeley have been an exciting time and that is due, in no small part, to the people I have met here.

First, I would like to thank Professor Jan Rabaey, who has provided a constant source of support and encouragement. Jan always sees the big picture, providing guidance and setting ambitious goals. Thanks also to Professor Roger Howe for reading this thesis with great interest and providing several insightful comments and directions for further study.

The Berkeley Wireless Research Center is truly a great place to be for a circuit designer. I am continually amazed by the willingness of students here to answer questions and discuss problems. Brian Otis has been a great friend and colleague from the beginning, entertaining my endless questions and conversations on everything from device physics to the surf report at Linda Mar. Ruth Wang has been a friend of mine since my first semester here, and I thank her for meticulously reading this thesis and providing many valuable suggestions. I've enjoyed working with Richard

Lu, Yuen Hui Chee, and Simone Gambini in the PicoRadioRF group, and especially hitting the links with Richard! Several other students, both in BWRC and Cory Hall, have also been a great source of advice and distraction for me, particularly Chinh Doan, Johan Vanderhaegen, Ian O'Donnell, Patrick McElwee, Brian Limketkai, Sayf Alalusi, Axel Berny, Mark Chew, Mike Chen, David Sobel, and Henry Jen.

I would also like to thank Dr. Carl Helrich and Dr. John Ross Buschert, both professors of physics at Goshen College, for giving me my first taste of research. Electronics class with John Ross was the deciding factor in my choice to pursue electrical engineering as a career.

From the beginning, my family has been a strong source of support and encouragement. My Mom, Dad, and brother Todd have all contributed greatly to my life over the years, and I am very grateful for that.

Last but certainly not least, my wife Andrea deserves recognition for putting up with many late nights and weekends in the lab, with only occasional (yet severe) protest. She has been a constant companion and I look forward to many more adventures. Thank you.

Nathan M. Pletcher

Berkeley, California

Chapter 1

Introduction

1.1 Motivation

During the past 50 years, all aspects of electronic circuit design have advanced at an amazing and rapid pace of innovation. This progress, along with unprecedented levels of integration, has continuously enabled new and exciting applications for electronic devices. For future designs, it appears that the metrics of cost, integration, and power consumption will be the primary drivers in electronics research. Within the application space of low power integrated designs, wireless sensor nodes have emerged as a system that must be small, cheap, and ideally self-powered. One of the most critical components making up an efficient sensor node is the wireless transceiver, which transmits and receives data packets in order to provide the communication link between distributed nodes.

The goal of this research is to explore the limitations of low power radio fre-

quency (RF) design for wireless sensor network applications. With ultra low power consumption as the fundamental design constraint, methodologies for designing wireless communications circuits require a departure from traditional approaches to RF design. In this work, novel tradeoffs and strategies for extreme low current and low voltage circuit design are investigated, with the design and test of a low power RF oscillator as a test vehicle for these strategies.

1.2 Thesis Organization

This thesis concentrates on the design and implementation of a micro power RF oscillator for low power transceiver applications. Chapter 2 provides background and context that serves to motivate research on ultra low power RF circuits. In Chapter 3, techniques for the design of analog circuits for low supply voltages and low current levels are investigated. In light of rapid technology scaling, subthreshold transistor operation is evaluated as a means of reducing power consumption in RF circuits. Chapter 4 focuses on the design and test of integrated inductors and the issues associated with implementation. A basic modeling framework is developed to enable accurate circuit design using on-chip inductors. The oscillator design and implementation is described in detail in Chapter 5, including background on topology choice for low power applications. In Chapter 6, measurement results from silicon are presented for the low power oscillator, including the variation of output swing, oscillation frequency, and phase noise across a range of bias points. Chapter 7 concludes the thesis with a brief summary of results and discussion of future research directions.

Chapter 2

Background

2.1 The PicoRadio Project

As mentioned in Chapter 1, the emerging field of wireless sensor networks is an area of research rich with opportunities for multi-disciplinary innovation. The PicoRadio project at U.C. Berkeley aims to develop design solutions for all aspects of peer-to-peer sensor networks [1]. The integrated research group comprises studies that focus on all levels of complete system design, from physical layer circuits research to high-level protocol definitions and routing algorithms. This integrated and system-wide approach is necessary to ensure that development at each level is mindful of the global implications resulting from all design decisions.

The primary design goal for wireless sensor networks is to realize a solution that is low cost, low power, and achieves a high level of integration. In order to create truly ubiquitous networks, sensor nodes will be deployed in large numbers; driving

down cost to a minimum for each node is thus a key requirement. In addition to low cost, high levels of integration are essential for ensuring not only small physical dimensions, but also for allowing mass production of nodes. Finally, the node must consume extraordinarily little power in order to extend battery life, because battery replacement for sensor network applications is prohibitively expensive. One of the distinguishing features of sensor networks is that the nodes may be widely scattered over areas that are not conveniently accessible by humans, such as industrial or hazardous environments. In these applications, battery replacement is not an option and nodes must be self-sufficient for the entire lifetime of the network. Recent technological advancements may even allow the node to scavenge energy from its environment, such as solar or vibrational energy sources [2, 3]. Even with these scavenging methods, energy constraints are stringent and power consumption is at the forefront of circuit design challenges for the sensor network environment.

The context of this research is the physical layer of a wireless sensor node, namely the radio frequency (RF) transceiver. The application imposes unique constraints on the transceiver; in contrast to traditional transceivers (e.g. cellular), wireless sensor networks require short range, low data-rate links. To meet these specifications, the use of recently developed technology in radio-frequency micro-electromechanical systems (RF-MEMS) is being investigated. Thus far, research has yielded a prototype transceiver consuming 3mW of active power [4]. Related research is ongoing to increase the level of integration and further reduce the power consumption.

2.2 Reactive Radio Architecture

In a sensor network environment where communication is relatively rare and packet lengths are short, the power consumed while monitoring channel activity may dominate the overall budget. Therefore, from an energy efficiency perspective, it is desirable to keep each node powered down whenever possible. In order for two nodes to communicate, however, a rendezvous scheme must be implemented to ensure that both will be simultaneously active to initiate the communication. Such schemes may be broadly categorized as purely synchronous, pseudo-asynchronous, and purely asynchronous.

Purely synchronous schemes require synchronization across the entire network, which is difficult for sensor networks because of the ad-hoc nature of the network. To overcome the prohibitive costs of fully synchronous communications, pseudo-asynchronous methods may be used, which employ a beaconing protocol to wake nodes up periodically and monitor data transmission in the channel. The node initiating communication repeatedly broadcasts a beacon signal until a neighboring node senses the signal during its periodic phase of monitoring the channel. Upon receiving the beacon signal, the second node sends an acknowledgment, allowing the communication to commence. In contrast to this pseudo-asynchronous model, fully asynchronous rendezvous schemes consist of nodes that constantly monitor the channel using a carrier sense receiver, or wake-up radio. The sole purpose of the wake-up radio is to monitor the channel for beacon signals from other nodes and appropriately enable the main data radio of the node for communication. Because the wake-up radio

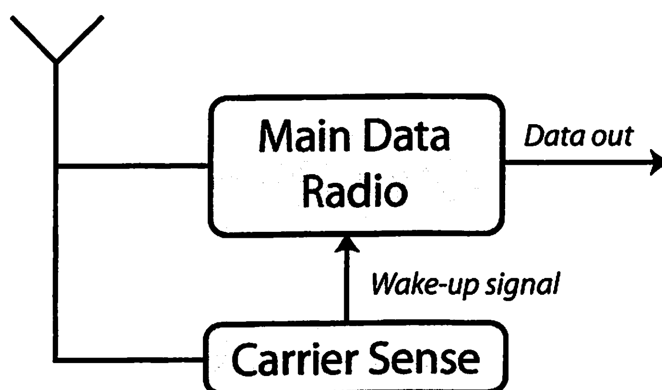

Figure 2.1: Reactive radio system block diagram

is *always* monitoring the channel, its power consumption must be minimal. Previous work establishes an upper bound of 50μW for the power consumption of the wake-up radio in order to surpass existing pseudo-asynchronous rendezvous schemes [5].

Figure 2.1 shows the integration of a wake-up radio with the main data radio, forming a fully reactive radio architecture. The main data radio is a high sensitivity transceiver with low bit-error rate (BER). With the current pseudo-asynchronous rendezvous scheme, the main data radio turns on at pre-defined intervals and monitors the channel for a short time. If a transmission is not detected during that time, it resumes sleep mode. In the proposed asynchronous approach, however, the main data radio remains in sleep mode indefinitely until it is activated by the carrier sense receiver.

As mentioned earlier, the carrier sense receiver must consume less than 50μW in order to out-perform pseudo-asynchronous schemes. When compared with the state of the art, this is an extremely aggressive target for any type of RF receiver.

The implementation of the wake-up radio requires a re-thinking of traditional RF design techniques, for which power consumption emerges as the clear limiting design constraint. In the following chapters, techniques for ultra low power RF design are developed to enable the design of this carrier sense receiver.

Chapter 3

Low Power Analog Techniques

3.1 Introduction

Standard CMOS technology has become prevalent in analog and RF circuit design mainly due to the low production cost and potential for integration with accompanying digital circuits. As outlined in Chapter 2, cost and integration are two essential considerations in the design of circuits for wireless sensor networks. Thus, scaled sub-micron CMOS technology is a natural choice for implementation of these circuits. In addition, deep sub-micron CMOS opens up new frontiers in low voltage and current circuit design. In this chapter, design techniques are outlined to fully explore the advantages of modern CMOS devices and achieve minimal power consumption for RF circuits.

3.2 Design for Low Supply Voltage

Although CMOS scaling has been extremely beneficial for digital circuits, analog circuits have often been hindered by these advances. One of the most difficult problems is the constantly diminishing supply voltage for modern CMOS processes, causing reduced voltage headroom and dynamic range for analog and RF applications.

3.2.1 Trends in CMOS Supply

Figure 3.1 shows projected trends in CMOS supply voltage scaling over the next 15 years, as predicted by the International Technology Roadmap for Semiconductors (ITRS) [6]. Scaling trends are shown for three different *digital* technology targets. The low power operation digital roadmap is the most aggressive, since supply voltage scaling is one of the main strategies for reducing power consumption in digital circuits [7]. Trends for high performance and low standby power designs lag by several generations, but are also expected to experience supply voltage scaling below 1V in the next ten years.

These digital roadmaps are an important indicator for the state of future analog designs because digital performance drives technology scaling. In order to reap the cost benefits of integration, analog and RF designs must conform to the specifications of digital technologies. One common strategy for dealing with reduced voltage in analog designs is to use special analog process options or high voltage I/O devices for the analog portions of the design. Though effective, this solution raises cost and increases power usage of the analog block.

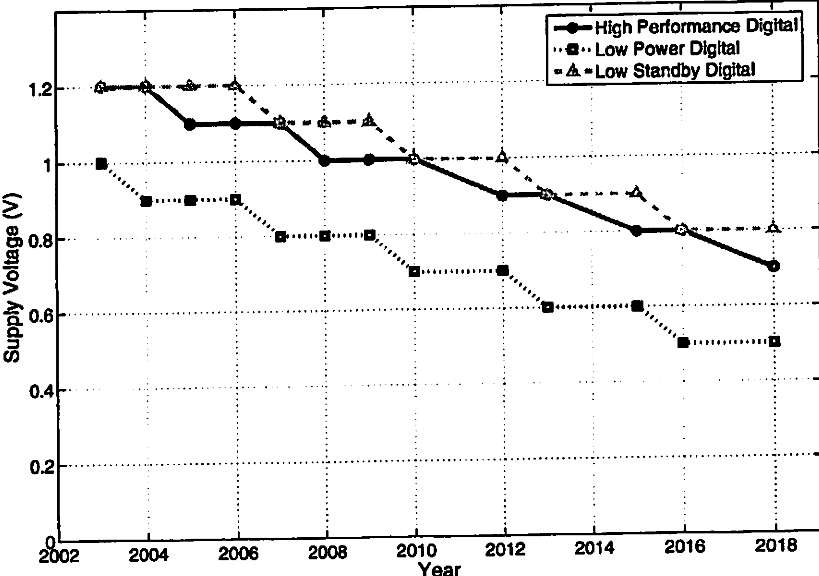

Figure 3.1: ITRS projections for CMOS supply voltage scaling

It is clear that future analog and RF designs will be subjected to ever more stringent supply voltage constraints. In many cases, however, it may be feasible to embrace this trend and reduce the supply voltage as low as possible as a means of achieving minimum power consumption. For low power designs, the minimum bias current is usually determined by the required circuit performance and cannot be arbitrarily reduced. On the other hand, the supply voltage is usually set at a standard value that may not be optimal for the design. If the current levels are optimized, the technique of reducing the supply voltage may result in additional power savings. In the following section, possible opportunities for low voltage RF design are discussed.

3.2.2 Opportunities for Reduced Supply

The standard differential *LC* oscillator shown in Figure 3.2 is an example of a circuit that is able to operate with a very low supply voltage. It contains only two stacked transistors, and the inductors comprising the resonant load do not consume any additional voltage headroom, enabling the output to swing above the supply voltage V_{DD}. Theoretically, the oscillator may operate on a supply voltage as low as $V_{Dsat1} + V_{Dsat3}$, where V_{Dsat} is the MOSFET saturation voltage. Furthermore, if the cross-coupled devices M_1 and M_2 are designed to operate in the subthreshold regime, V_{GS} and V_{Dsat} may be quite small. Subthreshold device operation is discussed at length in Section 3.3.2.

The main drawback to operating under such a low V_{DD} is the reduction in output voltage swing. Most oscillators for transceiver applications are designed for maximum

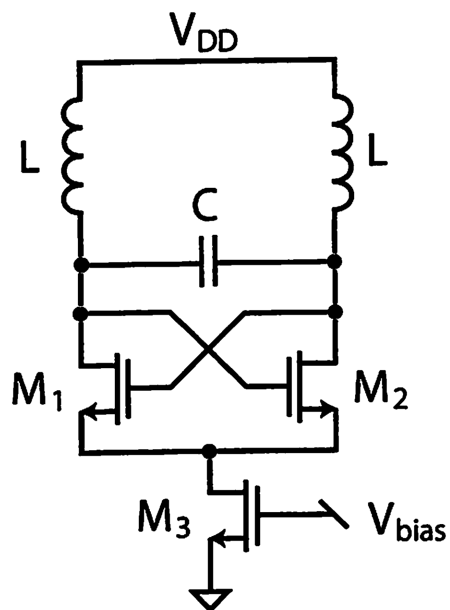

Figure 3.2: Schematic of low voltage LC oscillator

swing in order to minimize phase noise. Obviously, a high supply voltage is preferred for those applications. For an ultra-low power oscillator, on the other hand, phase noise performance will most likely be sacrificed for power savings. This results in a startup-limited design where swing is not limited by supply voltage. A reduced supply voltage is thus beneficial for applications like sensor network transceivers.

Finally, when designing low voltage circuits and choosing the optimal power supply voltage, system level considerations are critical. Supply voltage is not typically considered a variable parameter available to the designer, because a system in which each component requires its own unique supply is impractical from an integration perspective. However, it is entirely possible that at least two supply voltages will be available in a sensor network environment: high voltage for active mode and low voltage for sleep mode. Recent research in low voltage digital design has shown that significant savings in memory leakage power may be achieved by reducing the supply to a few hundred millivolts during standby periods [8]. If a lower voltage supply is made available for use in digital standby mode, it may also be used as the operating supply for analog circuits.

3.3 Subthreshold Operation

Traditionally, transistors for high frequency applications are operated in strong inversion to take advantage of the high device transit frequency (f_T) in this regime. Transit frequency is defined as the frequency where the current gain of the device

falls to unity and is normally given by:

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{3.1}$$

where g_m is the small-signal transconductance and C_{gs} and C_{gd} represent the gate-source and gate-drain capacitances, respectively. The transit frequency is a common figure-of-merit for comparing device speed in different technologies.

It has long been understood that subthreshold device operation (also known as weak inversion) provides more transconductance g_m for a given bias current, and that this property may be exploited to design extremely low power CMOS circuits [9]. Unfortunately, the increased transconductance efficiency comes at the expense of lower device f_T, so subthreshold design has historically been associated with low frequency applications. Figure 3.3 shows the conflicting trends of transconductance efficiency and f_T over the entire range of device operation. The independent variable *inversion coefficient*, or IC, will be discussed in Section 3.3.1. Briefly, the inversion coefficient is a measure of the degree of inversion for a given device bias condition. $IC = 1$ represents the center of moderate inversion, while $IC \ll 1$ indicates weak inversion and $IC \gg 1$ signifies strong inversion. In Figure 3.3, the inversion coefficient is varied by changing the DC bias current density (A/m) of the device over several orders of magnitude. The vertical line in the figure indicates the center of moderate inversion. The method of plotting device small-signal parameters against IC provides a graphical correlation of bias current with the device operating point.

Obviously, there is a significant speed penalty associated with operation below

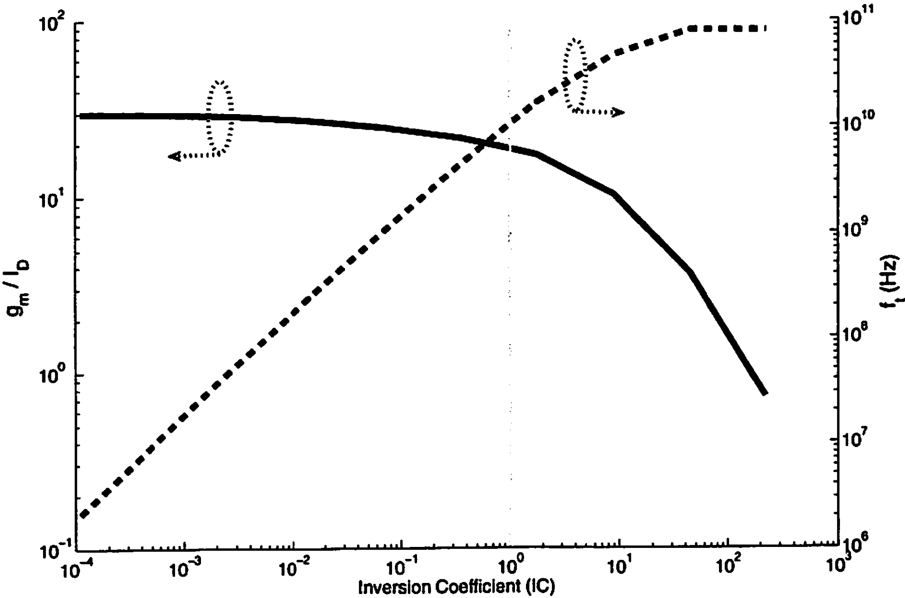

Figure 3.3: g_m/I_D and f_T for a modern CMOS 0.13μm process

strong inversion. With recent CMOS technologies boasting maximum f_T above 100GHz, however, it is no longer necessary to bias devices for the highest possible f_T. By carefully choosing the region of operation for critical transistors, the designer may trade off device bandwidth for transconductance efficiency to achieve a lower power design.

3.3.1 Basics of Subthreshold Operation

The MOSFET device exhibits distinct operating characteristics depending on bias conditions. The simplified square law model is the most conducive to manual calculations. The square law model for a MOSFET assumes that there are no free carriers in the channel when $V_{GB} < V_{th}$, where V_{GB} is the gate-bulk voltage and V_{th} is the threshold voltage. This implies that there is no inversion charge and therefore no current conduction from drain to source when the gate is biased below the threshold voltage V_{th}. Using this simple model, Equations 3.2 and 3.3 may be derived for the device drain current in triode and saturation regions, respectively:

$$I_{D,triode} = \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS} \tag{3.2}$$

$$I_{D,sat} = \frac{\mu C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_{th} \right)^2 \tag{3.3}$$

These equations assume that all drain-source current is due to drift current in the inverted channel and that there is zero inversion charge when $V_{GB} < V_{th}$. These assumptions hold only in the strong inversion regime, so Equations 3.2 and 3.3 are

valid only in strong inversion.

A more accurate analysis using the charge sheet model [10] assumes that mobile charge *does* exist in the channel before the onset of strong inversion. The inversion charge in the channel Q_I is given by:

$$Q_I = -C_{ox}\left(V_{GB} - V_{FB} - \psi_s + \frac{Q_B}{C_{ox}}\right) \tag{3.4}$$

where V_{FB} is the flatband voltage, ψ_s is the surface potential in the silicon, and Q_B is the charge in the depletion region. Using the charge sheet model, drain current equations may be derived that are valid in all regions of operation. Unfortunately, the resulting model is computationally intensive and unsuitable for compact model simulation. However, the model may be used to derive simple equations for the drain current in regions of operation other than strong inversion. In weak inversion, the drain current is given by [11]:

$$I_D = \frac{W}{L} I_0 \exp\left(\frac{V_{GS} - V_{th}}{nU_t}\right)\left(1 - \exp\left(\frac{-V_{DS}}{U_t}\right)\right) \tag{3.5}$$

where

$$\begin{aligned} I_D &= \text{device drain current} \\ \frac{W}{L} &= \text{device aspect ratio} \\ n &= \text{subthreshold slope factor} \\ U_t &= kT/q \end{aligned}$$

$$V_{th} = \text{gate to source threshold voltage}$$

$$I_0 = 2n\mu_0 C_{ox} U_t^2$$

The quantity I_0, known as the *specific current*, is discussed later in this section. For now, I_0 may be understood as a technology dependent parameter representing the normalized current in the region directly between weak and strong inversion.

Equation 3.5 reveals that the drain current becomes exponentially dependent on the gate voltage in subthreshold operation, similar to a bipolar device. In this region, the drain current is composed of *diffusion* current and the device operates like a bipolar transistor with the body acting as the base. The gate terminal modulates the bulk through the capacitive divider formed by the oxide and depletion capacitances. In Equation 3.5, it is this divider that gives rise to the factor of n in the denominator of the first exponential. The subthreshold slope factor n is typically between 1.3 and 1.5 for deep submicron CMOS technologies. It follows that for a given bias current, the achievable g_m for a subthreshold MOSFET will always be less than a bipolar device.

Figure 3.4 shows the logarithm of drain current with increasing gate voltage for a fixed drain bias of 50mV. In the figure, the simple models for weak and strong inversion regimes are fit to an actual MOS Model 9 curve for a 0.18μm CMOS technology. The threshold voltage in this technology is approximately 450mV. Due to the simplistic nature of the modeling equations, the device length for the simulation is chosen to be 5μm to avoid short channel effects. When $V_G < V_{th}$, Equation 3.5

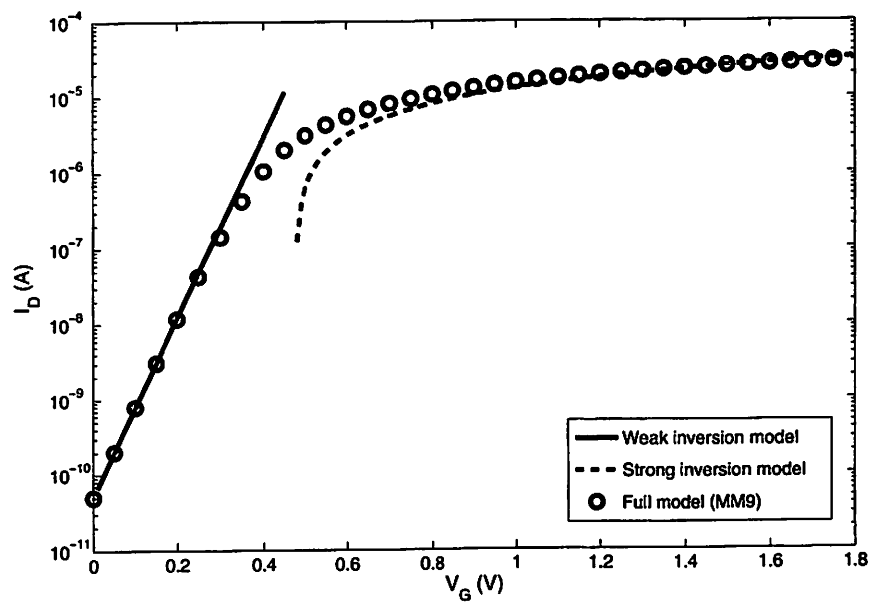

Figure 3.4: I_D vs. V_{GS} ($V_{DS} = 50\text{mV}$), comparing strong and weak inversion models

predicts the drain current quite well and the exponential dependence is valid. In strong inversion, on the other hand, the square law relationship must be used. The device is primarily operating in the triode region for this small V_{DS}, so Equation 3.2 is used here. Clearly, the square law model is only valid when $V_G > V_{th}$, since the drain current rapidly and incorrectly approaches zero close to the threshold voltage.

Figure 3.4 also clearly shows the region of discontinuity between the weak and strong inversion models, which is purely a simulation artifact. In reality, this transition occurs smoothly in physical devices as gate bias and inversion charge increase. This discontinuous region in between is known as moderate inversion, for which the drain current is a combination of drift and diffusion components. Traditionally this transition is the most difficult to model accurately; most simplified models rely on interpolation in this region, as evidenced by the MOS Model 9 curve in Figure 3.4.

One approach to gain intuition, developed in the EKV model [11], is to define a *specific current* I_0 that represents the intersection of the weak inversion and strong inversion asymptotes. I_0 depends on the device aspect ratio, mobility μ_0, and subthreshold slope factor, and is given by:

$$I_0 = 2n\mu_0 C_{ox} U_T^2 \tag{3.6}$$

Physically, I_0 represents the characteristic current for the device in the center of moderate inversion, providing a convenient normalization factor. The drain current

of a given device may be normalized to I_0, producing the *inversion coefficient* IC:

$$IC = \frac{I_D}{I_0 \frac{W}{L}} \tag{3.7}$$

Because all technology-dependent aspects of the device are contained in I_0, the inversion coefficient provides an intuitive feel for the region of operation:

$$\begin{aligned} IC &\ll 1 : \text{weak inversion} \\ IC &\approx 1 : \text{moderate inversion} \\ IC &\gg 1 : \text{strong inversion} \end{aligned}$$

The MOSFET is truly a versatile device, with distinctive characteristics in each operating regime. In the following sections, the relative merits and drawbacks of circuits operating in subthreshold are outlined.

3.3.2 Benefits of Subthreshold Operation

Subthreshold biasing enables the most DC gain for the least amount of current, as evidenced by the high g_m/I_D ratio in this region. For a given bias current, the available transconductance may be several times higher than in strong inversion. This is a major benefit for wireless sensor network applications, in which power consumption is the major concern.

Another advantage of subthreshold operation is the relatively low drain saturation

voltage, which is typically around $3U_T$ (~75mV). Furthermore, in contrast to strong inversion, the value of V_{Dsat} in subthreshold does not depend on the gate bias. The low saturation voltage implies that transistors operating in weak inversion require less voltage headroom than do devices in strong inversion. With constantly diminishing supply voltages, the reduced headroom requirement is critical for the implementation of circuits with several stacked transistors. Subthreshold operation is therefore a natural choice for circuits operating with a reduced supply voltage.

In certain applications, the exponential drain current dependency may also be useful. Since the device operates similarly to a bipolar junction transistor, it is possible to build translinear and log-domain circuits in pure CMOS technology. For example, in [12] a filter is implemented to operate on a low 1V supply, despite the use of 0.5μm CMOS technology with threshold voltages of about 0.6V. For such a low supply voltage, weak inversion operation is the only means of achieving sufficient dynamic range.

3.3.3 Challenges for Subthreshold RF Circuits

Although the benefit in DC gain makes subthreshold operation attractive, there are also drawbacks to operating in this region. The first and most obvious problem is reduced bandwidth. Figure 3.3 reveals that in weak inversion, the device f_T is several orders of magnitude below the peak value intrinsic to the process. In the past, this speed limitation has been a prohibitive barrier for most applications, especially RF designs.

Fortunately, technology scaling is starting to provide the solution; with the present generation of CMOS technology, subthreshold RF design is already becoming feasible. This point is illustrated in Figure 3.3; the peak f_T is approximately 100GHz, dropping off sharply at lower inversion coefficient. However, at the center of moderate inversion, indicated by the vertical line at $IC = 1$, f_T remains near 5GHz. Clearly, this bandwidth is adequate to realize circuits operating in the 100s of MHz or above. Because CMOS scaling shows no signs of slowing, it is reasonable to expect that imminent technologies will provide sufficient bandwidth for subthreshold circuits up to the low GHz range. In Figure 3.5, device f_T is simulated across inversion level for three generations of submicron CMOS. The technology nodes are 180nm, 130nm, and the current state of the art, 90nm.

It is evident that f_T increases in all regions of operation with each generation of scaling. At the center of moderate inversion, f_T is approximately 6GHz for 180nm, 12GHz for 130nm, and 21GHz for the 90nm node. This represents an increase of 75 to 100% for each technology node.

For comparison, Figure 3.6 plots transconductance efficiency in all regions of operation for the same three CMOS processes. Note that the main difference between the technologies is scaling of the inversion coefficient. For example, the 90nm curve is shifted to the left with respect to the other curves. This shift is due to higher values of $\mu_0 C_{ox}$ and a higher subthreshold slope factor n, which leads to a higher specific current I_0. The important point is that the achievable transconductance efficiency does not deteriorate significantly with technology scaling. From the trends demonstrated in Figures 3.5 and 3.6, it appears that the increased bandwidth from technology scaling

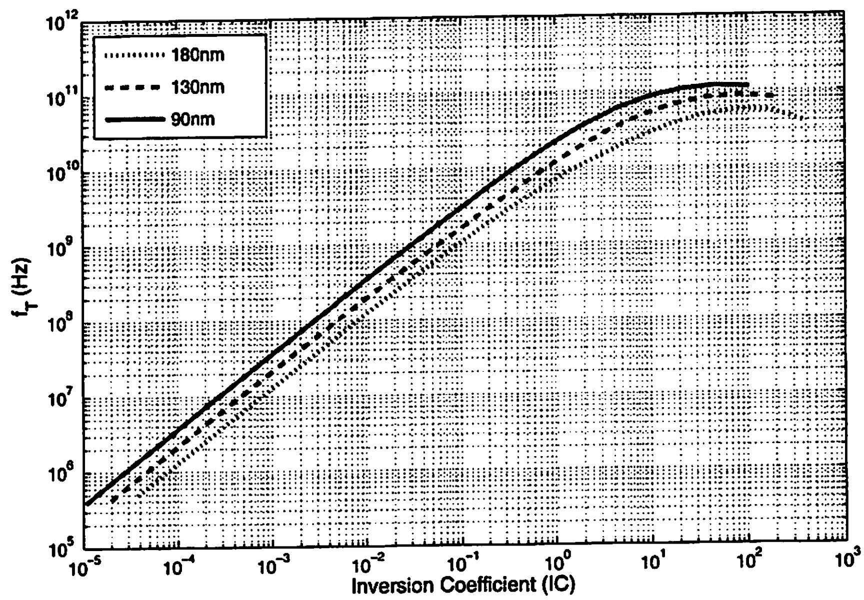

Figure 3.5: Comparison of f_T with technology scaling

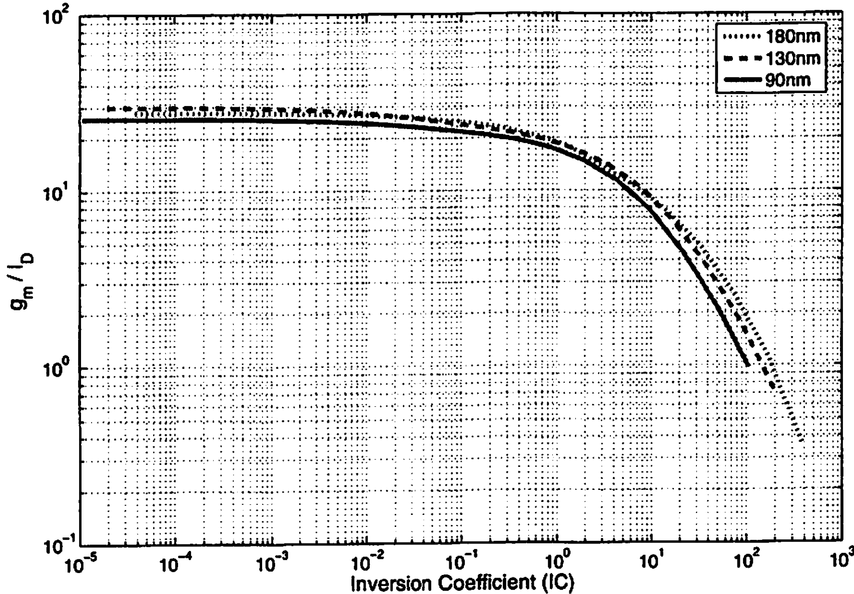

Figure 3.6: Comparison of g_m/I_D with technology scaling

will alleviate the problem of low f_T in weak and moderate inversion.

In addition to reduced f_T, there is a subtle problem with subthreshold design that does not stem from technological limitations of the MOSFET device itself. Historically, MOS compact device models have not accurately modeled the moderate and weak inversion regimes. As a result, many designers have come to regard subthreshold operation as a pitfall to be avoided. In industry, where design mistakes and revisions are extremely costly, designers cannot afford to risk such modeling uncertainty. To illustrate the discrepancies, Figure 3.7 compares small-signal g_m/I_D across the entire range of inversion for two compact MOS models, BSIM3v3 [13] and MOS Model 11 [14].

Both models are developed to fit the same $0.13\mu m$ CMOS process from STMicroelectronics. As seen in the figure, however, the shape of the two curves is fundamentally different. The greatest discrepancy occurs around weak to moderate inversion. Older models like BSIM3v3 have difficulty accurately modeling the transition between weak and strong inversion. Obviously, this is a problem for the reliable design of circuits operating in this region. Since subthreshold regions have not been important design targets in the past, the modeling deficiency has only recently begun to be addressed. For example, in digital circuits, subthreshold conduction manifests itself as leakage current. With leakage power in digital circuits becoming a serious concern in recent technology generations, the accurate modeling of the subthreshold region is a priority for digital design as well. MOS Model 11 is a surface potential-based model that was developed to provide a suitable model for digital, analog, and RF design. Recognizing the need for accurate MOS models at RF frequencies, recent research

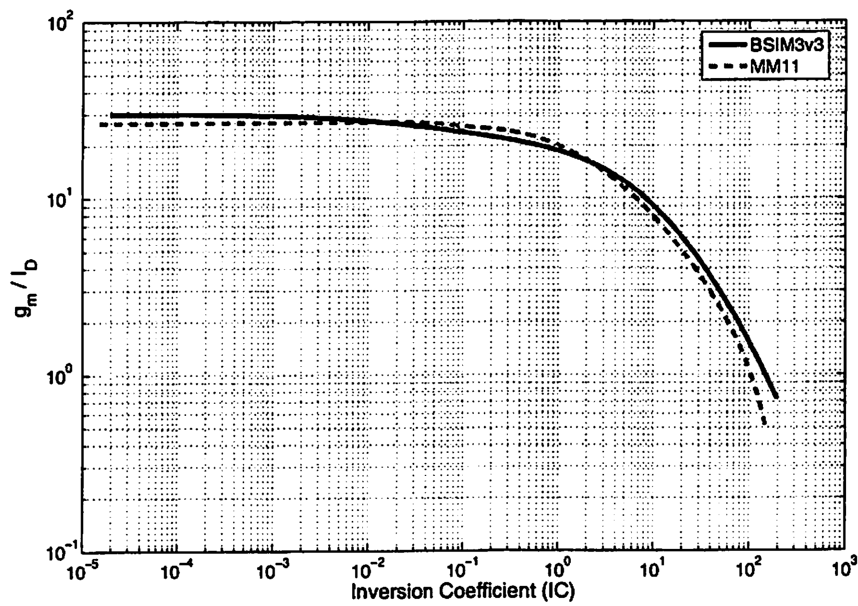

Figure 3.7: Comparison of g_m/I_D for BSIM3v3 and MM11 models

has been dedicated to the evaluation of the model for typical RF applications with regard to gain, noise, and linearity [15].

Accurate high frequency models for RF are also critical, because devices operated in subthreshold will be operated at frequencies closer to f_T than in strong inversion designs. When the operating frequency approaches f_T, it is important to evaluate the appropriateness of the quasi-static channel approximation. Historically, researchers address this modeling issue by formulating extensions for standard compact models that account for the non-quasi-static nature of the channel at high frequencies [16]. More recent models are already beginning to incorporate the effect directly into the model. In [17], the transistor channel is divided into several segments in order to more accurately model the distributed nature of the channel. With this approach, the non-quasi-static gate resistance and gate current noise are accurately modeled in all regimes.

3.3.4 Inversion Coefficient Methodology for Design

As shown in the previous section, future technologies will likely provide solutions for the existing barriers to subthreshold RF design. To fully exploit design opportunities in all regions of operation, the designer should consider the operating region of each device as an additional degree of freedom. Instead of setting the bias current and tweaking transistor sizes through exhaustive simulations, the designer may use simulated characterization plots to design for a particular operating region. The appropriate transistor sizing is then dictated by the inversion coefficient and desired

bias current. In this section, a design methodology based on the inversion coefficient of individual devices is presented, which helps the designer to gain an intuitive understanding of the tradeoffs involved.

In Section 3.3.1, the concept of inversion coefficient was introduced. The inversion coefficient IC is a useful design metric because it is directly proportional to the current density flowing in a device, which is one way of defining the operating region. Although the concept of inversion coefficient has been known for some time, it is especially pertinent now because it provides a link to bridge the gap between design intuition and simulation. The designer cannot produce an optimal circuit without some intuition. Even with accurate computer models, the circuit designer must also understand how to evaluate the available tradeoffs. Because simple equations no longer suffice for calculating transistor characteristics, a method must be found for presenting simulation data clearly to the designer. The inversion coefficient provides this link, because for any device or bias condition, the specific current I_0 may be extracted from accurate simulations. I_0 is dependent on technology and bias condition, but once this parameter is extracted it may be used for quick hand calculations for design. Once a library of curves is developed for a given technology it is simpler to see the design tradeoffs and trends [18].

For reference and comparison, Table 3.1 lists extracted I_0 values for several devices. Once I_0 is known, the inversion coefficient IC is easily extracted from the bias current and aspect ratio W/L, as shown in Equation 3.7. As expected, NMOS devices exhibit higher values of I_0 than PMOS, due to their higher mobility. The data also show that I_0 increases with each generation of technology scaling, due to higher mobility and

Gate Length (μm)	Device type	V_{th}	Remark	I_0 (nA)
0.13	NMOS	low high		662 600
0.13	PMOS	low high		164 141
0.13	NMOS	low low	fast corner slow corner	786 573
0.18 0.25 0.35	NMOS	low low low		632 627 622
0.18	NMOS	low	0.18μm tech	469
0.10	NMOS	low	90nm tech	941

Table 3.1: Extracted I_0 values for selected devices

generally higher subthreshold slope factor n.

In the remainder of this section, sample plots are provided that show the dependence of small-signal transconductance efficiency on various device types and bias conditions. The simulations are performed for a 0.13μm standard CMOS process, and all plots are normalized to inversion coefficient as the independent variable. The mobility and subthreshold slope parameters are extracted using simple graphical methods with transistors in typical bias conditions. Note that the technology dependent parameters should be extracted from simulation of devices that are biased to match the intended usage. Alternatively, it is also possible to extract parameters from a more complex model using curve fitting, as developed in [19].

Figures 3.8 and 3.9 are examples of two basic curves that may be used for design. Figure 3.8 compares the transconductance efficiency for both high and low threshold NMOS and PMOS devices with minimum channel length; Figure 3.9 extends this to

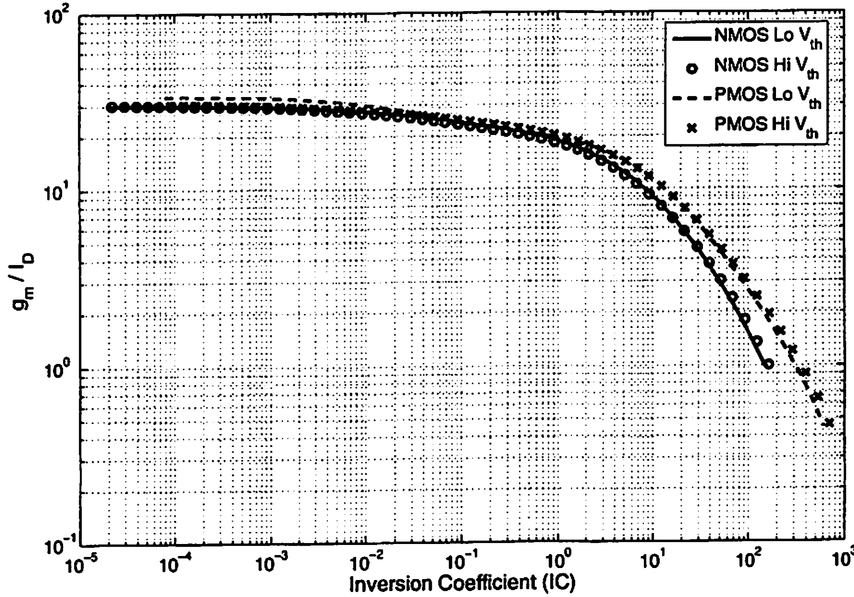

Figure 3.8: Comparison of g_m/I_D for dual-threshold NMOS and PMOS devices

a range of larger channel lengths. These curves show that longer channel lengths provide slightly more transconductance in deep subthreshold, since the longer devices have more ideal subthreshold slope factor (closer to 60mV/decade). Biasing with $IC < 0.01$, however, results in impractically large devices (large W/L); therefore, the principal region of interest is $0.01 < IC < 10$ for low power designs. In this region, corresponding to moderate inversion, minimum channel length devices provide better performance.

Figures 3.10 and 3.11 illustrate the convenience of the normalized inversion coefficient when used as an independent parameter, rather than arbitrary quantities such as current or voltage. In Figure 3.10, small-signal parameters are compared over

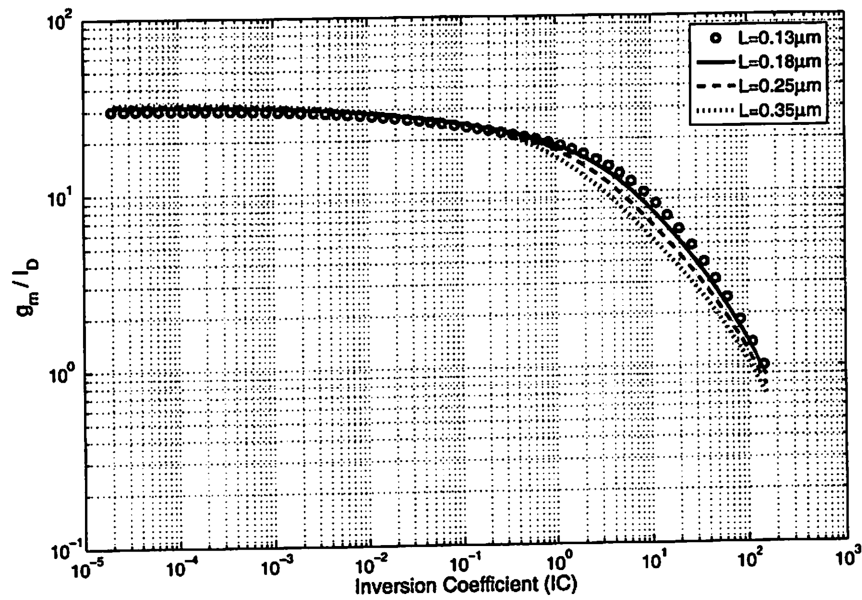

Figure 3.9: Comparison of g_m/I_D for different device lengths

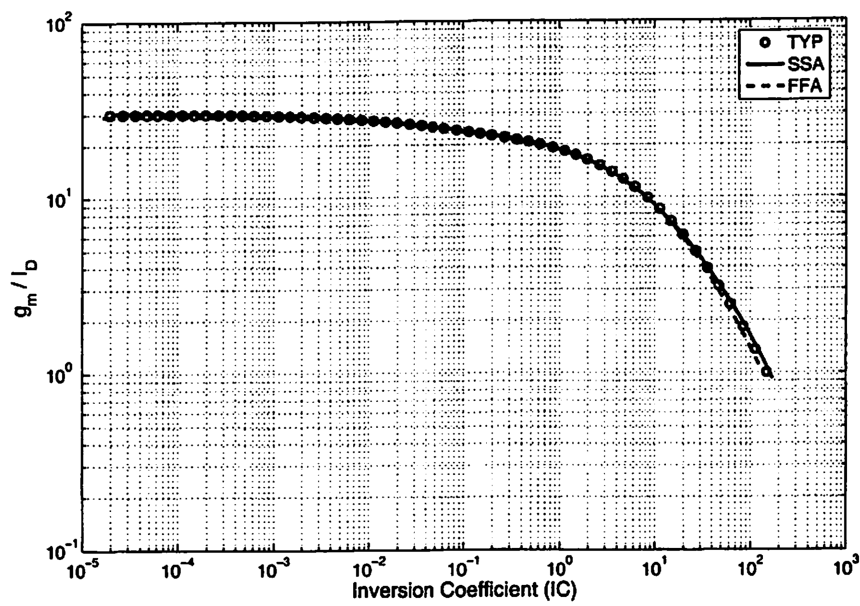

Figure 3.10: Comparison of g_m/I_D across process corners

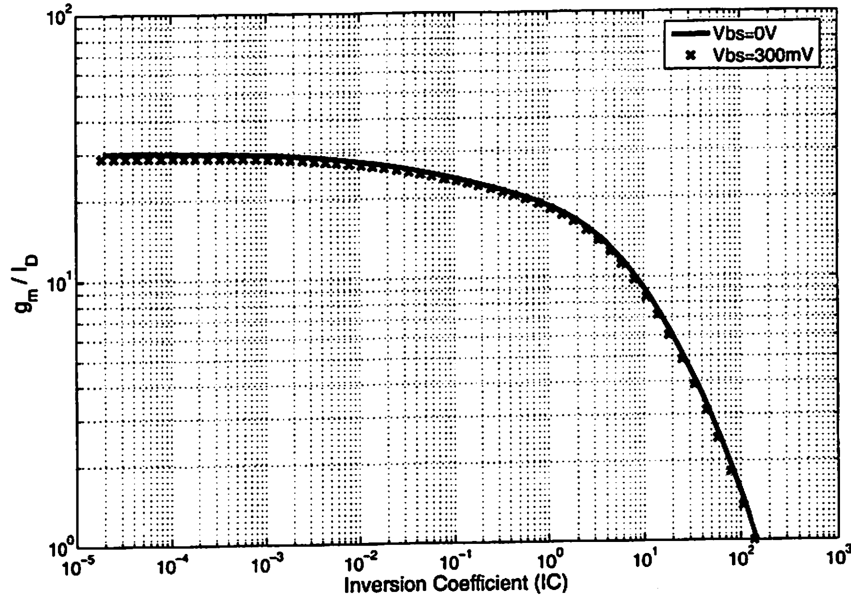

Figure 3.11: Comparison of g_m/I_D for different substrate bias

fast, typical, and slow corners. Because a different inversion coefficient is calculated for each corner, the plots are normalized with respect to inversion level. The curves are virtually identical across process, confirming that the small-signal parameters are unchanged as long as inversion level is maintained.

Similarly, the inversion coefficient also accounts for substrate bias and body effect. Figure 3.11 shows that g_m/I_D remains unchanged with a large substrate bias of 300 mV; the threshold shift is contained within the inversion coefficient parameter.

After investigating the advantages and disadvantages of subthreshold operation in this section, it appears that moderate inversion is an attractive compromise between the speed of strong inversion and the improved gain of weak inversion. In current

technologies, moderate inversion is a realistic target for the realization of RF circuits. Moderate inversion also benefits from lower electric fields in the device, avoiding high field effects that degrade performance and reliability [16].

In this chapter, design approaches utilizing subthreshold biasing and low supply voltage were presented and motivated. Equipped with these low power design methods, an oscillator is designed in Chapter 5 to test and verify the techniques.

Chapter 4

Integrated Inductors

4.1 Introduction

In Chapter 3, several techniques to reduce the power consumption of RF circuits were discussed. Those approaches were focused on the active devices. For highly integrated RF circuits, the quality of available passives is equally important. In fact, low power RF circuits are often limited by the quality of integrated inductors and capacitors. These passives are necessary in most RF circuits to provide frequency tuning and to construct matching networks. Unfortunately, performance of passive devices does not scale like active devices with new technology generations. On the contrary, passive quality may actually decrease with smaller dimension technologies.

One potential solution to this difficulty is to use off-chip passives. Unfortunately, the use of off-chip passives is problematic for several reasons. Most importantly, additional off-chip components decrease the level of integration and increase cost, which

is unacceptable for sensor network applications. Almost as critical, the prohibitively large parasitics associated with signals leaving the chip may outweigh the benefits of the higher quality elements.

For these reasons, it is desirable to utilize on-chip passives whenever possible. The focus of this chapter is on the design of integrated inductors because they are typically the lowest quality passive on the chip. On-chip capacitors, by comparison, often achieve a quality factor that is an order of magnitude higher than the inductors. First, the conventional structure and layout of integrated inductors is introduced, followed by modeling issues associated with these structures. Finally, measurement results and parameter extraction are presented for a typical inductor in a modern deep-submicron CMOS technology.

4.2 Structure and Layout

A simple square inductor structure is shown in Figure 4.1. The coil is formed by a metal trace, with several possible variations in the basic shape. In most modern technologies, non-Manhattan geometry is allowed, and thus octagonal shapes are often used. To realize this shape, a lower metal layer forms an underpass and allows access to the inside end of the coil (shown as the lighter segment in the figure). The most important design parameters associated with this structure are labeled in Figure 4.1:

D → diameter of coil

W → width of coil trace

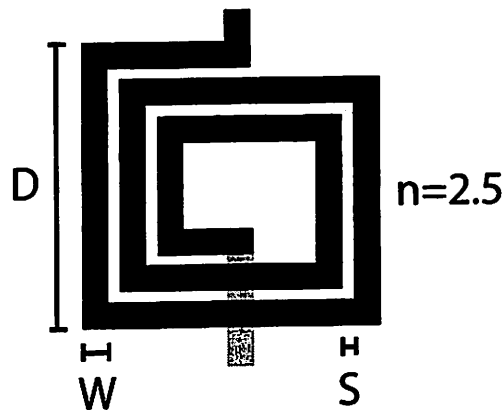

Figure 4.1: Sample layout of integrated inductor illustrating design parameters

S → inter-turn spacing

n → number of turns (2.5 here)

In the following sections, the important properties and metrics of integrated inductors are defined.

4.2.1 Inductance

The inductance is defined by the magnetic flux through the coil, and is primarily determined by the diameter of the coil and the number of turns. High inductance values will result in large silicon area, which is expensive. Accordingly, for RF frequencies (> 1GHz) the largest value of inductance that is feasible to implement on-chip is approximately 10nH. Inductors of larger values are possible for lower frequency

operation, where the larger parasitics and losses of the structure are not as critical.

4.2.2 Quality Factor

The general definition for the quality factor Q of any passive component is given by [20]:

$$Q = \omega \frac{E_{stored}}{P_{dissipated}} \tag{4.1}$$

where E_{stored} is the energy stored in the component and $P_{dissipated}$ is the average power dissipated. A high quality factor is desirable for most RF circuits because losses will be reduced, enabling lower power consumption. For an oscillator, high Q is particularly critical because the losses in the resonant tank must be overcome by active circuitry. Therefore, the minimum achievable power consumption is directly proportional to the quality factor of the tank. High Q also results in sharper filtering in the tank and lower phase noise.

For an inductor, the definition for quality factor becomes:

$$Q = \frac{\omega L}{R_s} \tag{4.2}$$

where R_s is a series resistor to model the losses and L is the inductance. Equation 4.2 shows that for an ideal inductor, with no loss, Q is infinite. Of course, all practical inductors have losses, and one of the primary sources is the physical series resistance of the metal trace, which reduces the Q. For this reason, several metal layers may be shunted in parallel to reduce the series resistance. The thick top copper layers that

are available in some technologies also help minimize the losses.

4.2.3 Self-Resonant Frequency

Another important property of an integrated inductor is the usable frequency range. The traces that make up the coil will always have a parasitic capacitance to the substrate or ground plane. At some frequency, the inductor will actually resonate with its own parasitic capacitance. Above this frequency, called the *self-resonant frequency*, the structure behaves as a capacitor rather than an inductor. The self-resonant frequency is the maximum usable frequency of the inductor. For large values of inductance, the structure is physically large and the parasitic capacitances may be excessive. The self-resonant frequency often limits the size of inductors that may be integrated on-chip.

4.2.4 Loss Mechanisms

At high frequencies, there are several other physical effects and loss mechanisms that degrade inductor performance. For example, at high frequencies, the self inductance of the metal trace causes the current in the coil to flow near the outer edge of the conductor, leading to an increase in the resistance. Since the current becomes restricted to a thin layer at the conductor surface, this phenomenon is known as the skin effect [21]. Additional losses arise from coupling to the substrate in the form of eddy currents that are induced in the substrate. This is particularly problematic in modern digital processes where the substrate has low resistivity to prevent latchup. All

aspects of integrated inductor design, including detailed descriptions of the physical loss mechanisms, are available in [21].

It is evident that many complex tradeoffs are present in the design of on-chip inductors. For this reason, inductors are usually designed and optimized using a full electromagnetic solver software package The simulation time may be significant, however, and the model accuracy from simulation may not be adequate. For high accuracy, the best method is to measure an existing inductor and extract a circuit model. An array of components with various inductance values and geometries is fabricated in a given technology. Design may then proceed using this well-characterized library of measured components.

It should be mentioned that a large body of research is dedicated to understanding integrated inductors and improving their performance. One approach is to add special process options with thick metal layers. Another more novel approach is to completely etch away the substrate beneath the inductor [22]. This reduces coupling and loss to the substrate, increasing the quality factor and self-resonant frequency. These approaches have not been widely accepted, however, due to extra processing steps that increase both cost and complexity.

4.3 Inductor Modeling

In order to design circuits using integrated passives, an accurate circuit model of each component is essential. For inductors, there are several common representations that offer a tradeoff between model accuracy and complexity. The simplest, known as the

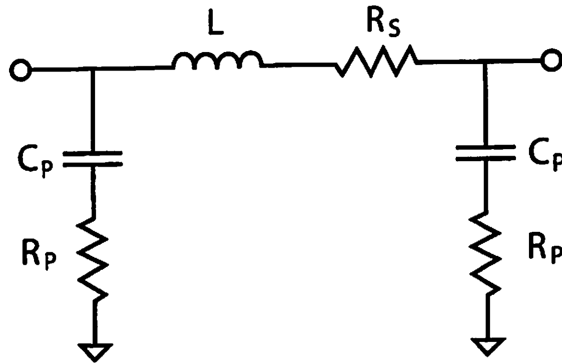

Figure 4.2: Equivalent circuit for simple π-model

π-model, is shown in Figure 4.2. In the figure, L represents the inductance of the coil and series loss is modeled by R_s, which is mostly due to the skin effect at high frequencies. In addition, each port of the inductor includes a capacitor and resistor to ground, in which C_p models the parasitic capacitance of the coil to the substrate and R_p represents the losses associated with coupling to the substrate, primarily due to eddy currents. The simple π-model provides a relatively accurate representation of the inductor, but it is important to note the model is narrowband because the modeling parameters are frequency dependent. For a particular set of parameters, the model is only valid over a narrow frequency range. Therefore, the model parameters must be extracted from measured S-parameters or electromagnetic simulation for a given frequency of interest.

More complex models are also used. These models augment the simple model with additional elements to include higher order effects. An example of a more complex model is depicted in Figure 4.3. In this model, a feedthrough capacitor C_f with

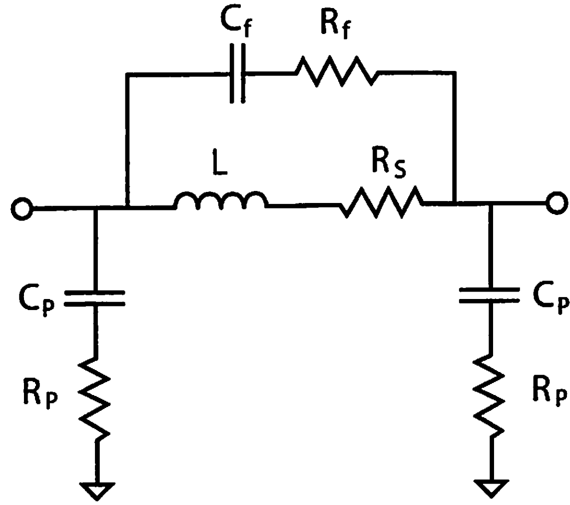

Figure 4.3: Equivalent circuit for a more complex π-model

finite Q is added across the inductor terminals to model the capacitance between the windings. The addition of extra components usually makes the model wider band and physically intuitive. However, a narrowband approximation is usually adequate for oscillator applications, where the operating frequency is well-defined by a reference. Thus, the simple π-model of Figure 4.2 is used for this design.

4.4 Measurements and Parameter Extraction

For the oscillator design in this work, an existing inductor test structure was characterized in order to provide a well-defined model. A photograph of the inductor is shown in Figure 4.4. The inductor layout was designed for a nominal inductance of 10nH. This is close to the upper limit of inductance values that are practical to

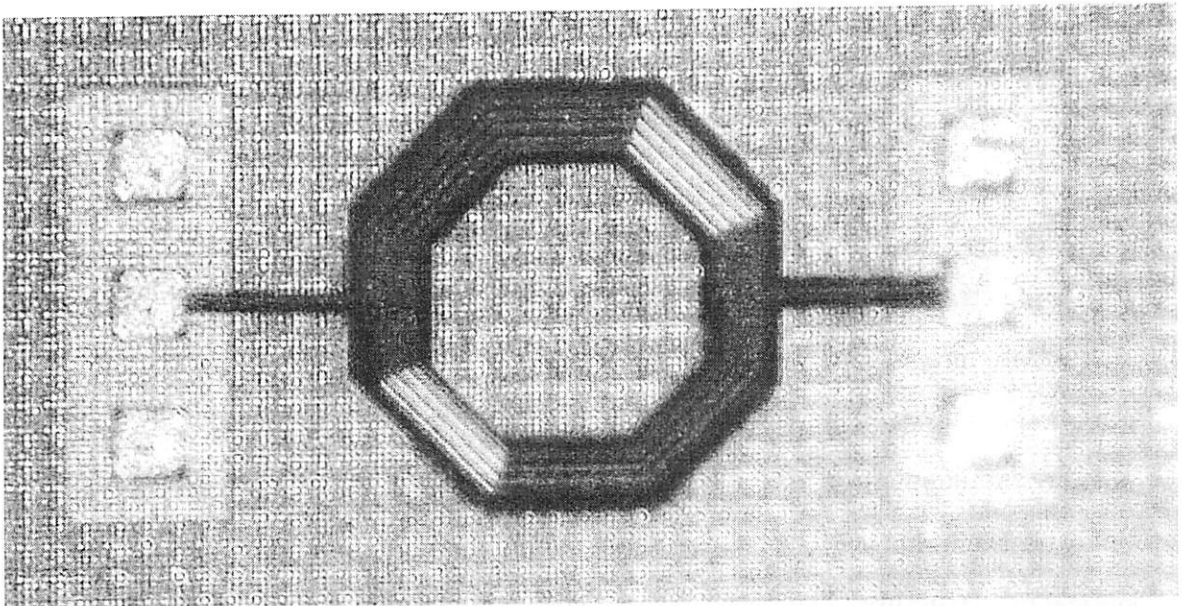

Figure 4.4: Photograph of inductor test structure

fabricate on a chip. Accordingly, the structure is approximately 450μm on a side. The coil consists of the topmost copper layer, Metal 6, shunted with a layer of Metal 5 to reduce the series resistance, with Metal 4 forming the underpass. Upper metal layers are used to maximize the distance to the substrate and minimize substrate losses. The trace width W is 12μm, the inter-turn spacing is 3.5μm, and the number of turns $n = 3.5$.

4.4.1 Inductor Measurement Process

In order to extract the model parameters, the raw S-parameters of the 2-port inductor structure are measured and the effects of parasitics removed through de-embedding. Because the pads used for probing will add parasitic capacitance, inductance, and resistance, standard short and open calibration structures are included on the chip along with the inductor. The calibration structures and the inductor under test have identical pad structure. The open structure consists of the pads alone, while the short incorporates an electrical short to the ground plane.

A Cascade Microtech probestation with Cascade 40GHz Infinity ground–signal–ground (GSG) RF probes is used for all on-chip measurements. First, the HP 8719C network analyzer is calibrated using the standard short-open-load-through (SOLT) technique with a calibration substrate. Next, raw s-parameters are measured for the inductor, along with the short and open calibration structures. Measured s-parameter magnitude for the inductor is shown in Figure 4.5.

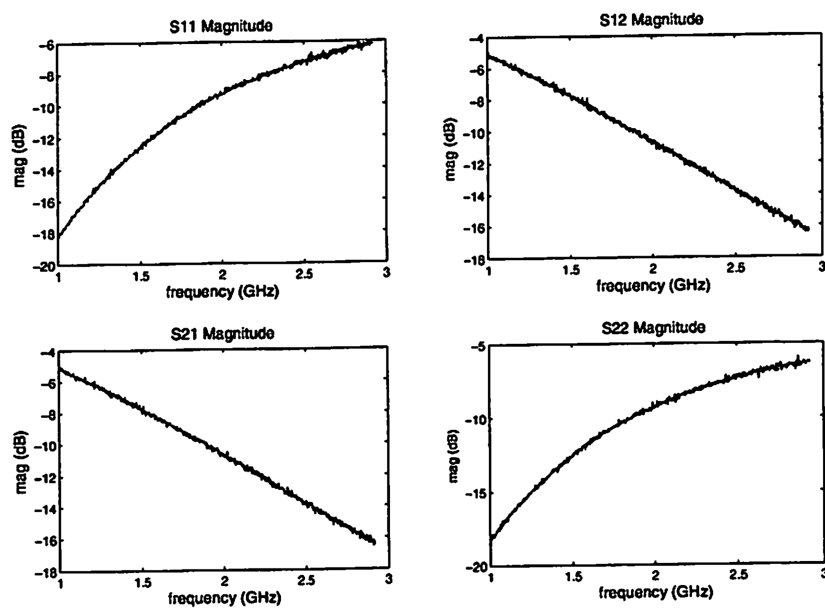

Figure 4.5: Measured raw s-parameter magnitude for inductor test structure

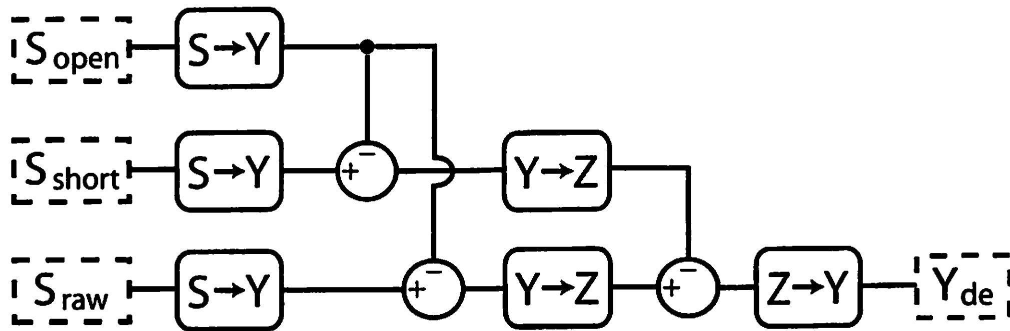

Figure 4.6: Block diagram of de-embedding flow

4.4.2 De-embedding Procedure

Once all the required s-parameters have been measured, the effects of measurement parasitics are removed through a standard de-embedding process. A block diagram of the flow is shown in Figure 4.6 [23]. All two-port parameter conversions are done in Matlab using the conversion procedures given in [24]. First, all s-parameters from the 50Ω test environment are converted to y-parameters. The parasitic pad capacitance is in parallel with the inductor under test, so the open y-parameters may simply be subtracted to remove these parasitics. The parasitic resistance and inductance of the pads, on the other hand, are in series with the test inductor. Therefore, the y-parameters must be converted to z-parameters before subtracting the effects of the short. The result is the calibrated z-parameters of the test inductor alone. For convenience in solving for the final model parameters, the final step is to convert the z-parameters back to y-parameters, leaving the de-embedded y-parameters Y_{de} in Figure 4.6.

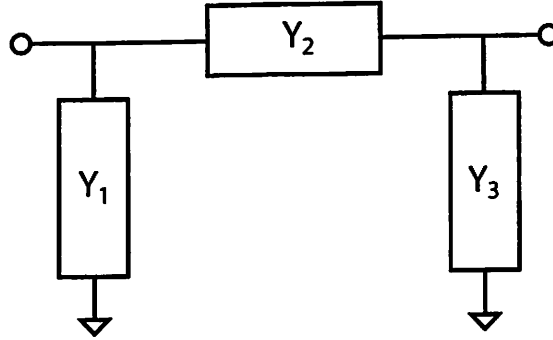

Figure 4.7: Admittance network representation of inductor model

4.4.3 Extraction of Final Model Parameters

One of the reasons for the popularity of the simple π-model is that the model parameters may be directly calculated from measurement data for a given frequency, obviating the need for curve fitting. The model in Figure 4.2 may be viewed as an admittance network as shown in Figure 4.7. Solving for the y-matrix of the network in Figure 4.7 and comparing to the π-model results in the following relation:

$$\begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix} = \begin{pmatrix} Y_1 + Y_2 & -Y_2 \\ -Y_2 & Y_2 + Y_3 \end{pmatrix} \tag{4.3}$$

where

$$Y_1 = \frac{j\omega C_{p1}}{1 + j\omega R_{p1} C_{p1}} \tag{4.4}$$

$$Y_2 = \frac{1}{R_s + j\omega L} \tag{4.5}$$

$$Y_3 = \frac{j\omega C_{p2}}{1 + j\omega R_{p2} C_{p2}} \tag{4.6}$$

Also, the quality factors associated with the reactive elements in the model are given by the ratio of reactive to resistive portions of the y-parameters:

$$Q_L = \frac{Im(y_{12})}{Re(y_{12})} \tag{4.7}$$

$$Q_{C_{p1}} = \frac{Im(y_{11} + y_{12})}{Re(y_{11} + y_{12})} \tag{4.8}$$

$$Q_{C_{p2}} = \frac{Im(y_{22} + y_{21})}{Re(y_{22} + y_{21})} \tag{4.9}$$

Using Equations 4.3–4.9 above, the model parameters may be solved for in terms of frequency and measured y-parameters:

$$L = \frac{1}{\omega}\left(\frac{Q_L^2}{Q_L^2 + 1}\right)\left(\frac{1}{Im(y_{12})}\right) \tag{4.10}$$

$$R_s = \frac{-1}{Re(y_{12})(Q_L^2 + 1)} \tag{4.11}$$

$$C_{p1} = \frac{1}{\omega}\left(\frac{Q_{C_{p1}}^2 + 1}{Q_{C_{p1}}^2}\right)\left(Im(y_{11} + y_{12})\right) \tag{4.12}$$

$$R_{p1} = \frac{1}{Re(y_{11} + y_{12})(Q_{C_{p1}}^2 + 1)} \tag{4.13}$$

Since the π-model is fully symmetric, $C_{p2} = C_{p1}$ and $R_{p2} = R_{p1}$. Figure 4.8 shows the evaluation of Equations 4.10–4.13 as a function of frequency for the measured inductor data. From Figure 4.8, a model may be extracted for the frequency of interest. This inductor will be used in a 1.5GHz oscillator, so an appropriate model for design at this frequency is summarized in Table 4.1. The overall Q of the inductor

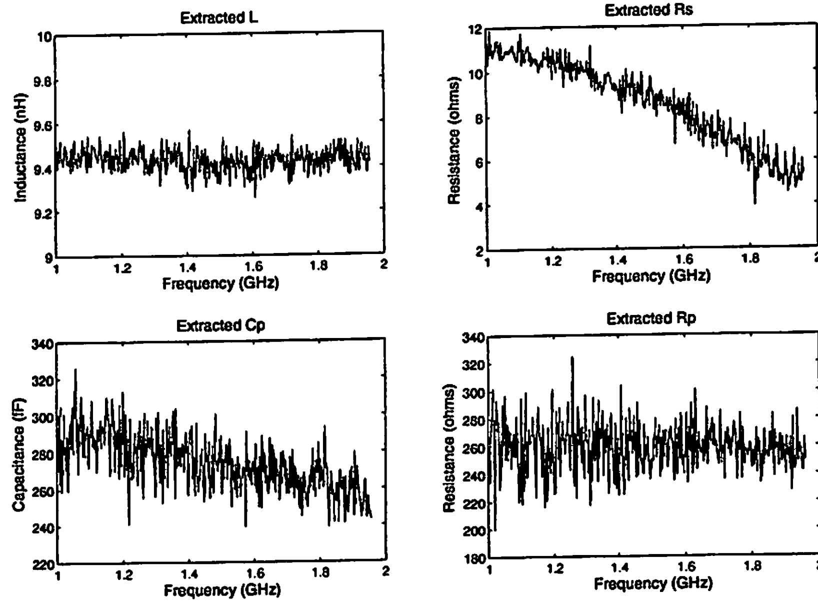

Figure 4.8: Model parameters as a function of frequency from measured data

Model Element	*Parameter Value*
L	9.4 nH
R_s	9 Ω
C_p	280 fF
R_p	260 Ω

Table 4.1: Extracted inductor model parameters for design

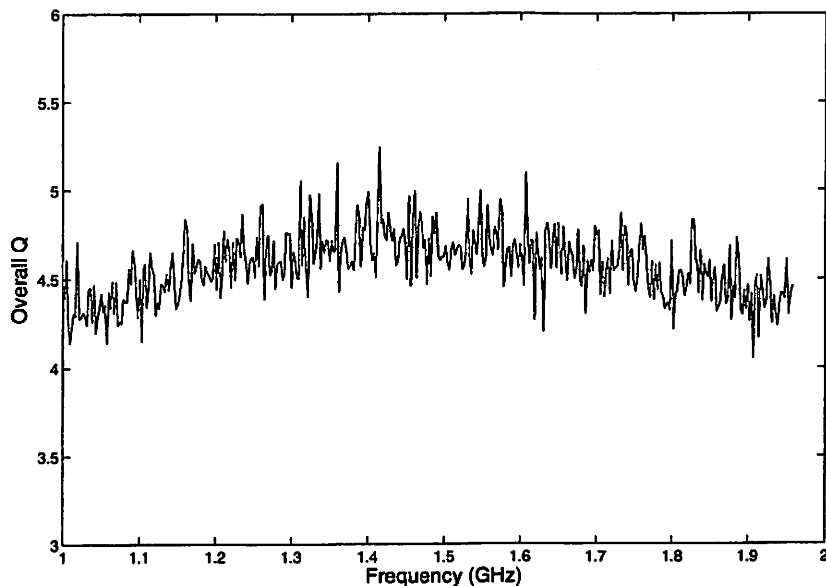

Figure 4.9: Overall Q factor for measured inductor

may be also be calculated from the extracted parameters of Figure 4.8. The plot of Q across frequency is shown in Figure 4.9. The peak Q is approximately 4.5 around 1.5GHz, a disappointingly low result that illustrates the significant losses associated with on-chip inductors. For comparison, bondwires or off-chip components typically have quality factors at least an order of magnitude higher. The noise of the data in Figures 4.8 and 4.9 is due to the multiple conversion steps involved in de-embedding and extracting the parameters. As seen in Figure 4.5, the measured S-parameter data is quite clean. The noise and loss of numerical precision is the result of subtracting very small numbers from each other in the conversion routines. The improvement of the conversion process to refine the final calibrated data is a topic for future work.

4.5 RF-MEMS

It should also be mentioned that RF-MEMS, mentioned in Chapter 2, are emerging as a possible alternative to traditional integrated passives. The current solutions for inductor design and characterization are clearly not optimal, so these alternative solutions are an area of active research.

The field of RF-MEMS encompasses a wide range of research. The most promising advances are in micromechanical resonators, which may potentially replace crystal oscillators and phase-locked loops in transceiver applications. RF-MEMS are potentially advantageous for wireless sensor network applications; MEMS resonators are extremely small and have high quality factor, enabling unprecedented levels of integration. A recently reported 1.9GHz oscillator employing bulk acoustic wave (BAW) resonators consumes just 300μW of power but still achieves low phase noise of -120dBc/Hz at 100kHz offset [25].

Fabrication processes are also under development to permit MEMS resonators to be integrated on the same silicon substrate with CMOS circuitry. In [26], a poly-SiGe process is proposed to allow resonators to be fabricated on top of CMOS circuitry. The process must be low temperature in order to avoid damaging the metal interconnect stack of the CMOS portion. Such high levels of integration will make high quality MEMS components an attractive replacement for traditional integrated passives.

Chapter 5

Oscillator Design

5.1 Introduction

In the previous chapters, some of the necessary tools to implement low power RF oscillators were developed, addressing the subjects of both active and passive devices. In this chapter, the design and implementation of a test oscillator in STMicroelectronics 0.13μm CMOS is presented. First, oscillator background information is introduced, followed by the choice of topology. Lastly, the final design and implementation is presented.

5.2 Design Objectives

The goals for this oscillator design are twofold. First, the design should consume minimal power and push the power limits of fully integrated RF oscillators. Secondly,

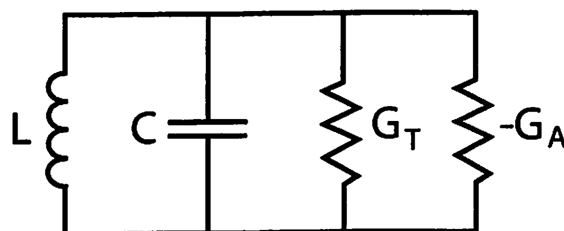

Figure 5.1: Simple model of oscillator as resonant tank

the oscillator should be a test vehicle for the concepts of low voltage and low current design presented earlier. With this goal in mind, the design should be sufficiently flexible to accommodate testing across a wide range of bias conditions. The ultimate objective is to illustrate the feasibility of RF oscillators operating in subthreshold for power levels under 200μW.

5.3 CMOS Oscillator Background

As shown in Figure 5.1, an LC oscillator may be modeled as a lossy LC resonant tank in parallel with a negative conductance. G_T represents the losses in the tank due to the finite Q of the inductor and capacitor. G_A is a negative conductance that models the active devices. This is a second order linear system with two poles in the complex plane. Figure 5.2 shows the complex plane representation and root locus for the second order system. During startup, the poles are in position (a). The active devices provide a negative conductance to overcome the losses in the tank. This linear analysis predicts a growing sinusoidal waveform, since the poles are in the right-half plane. Eventually, nonlinearities in the system become significant and the poles move

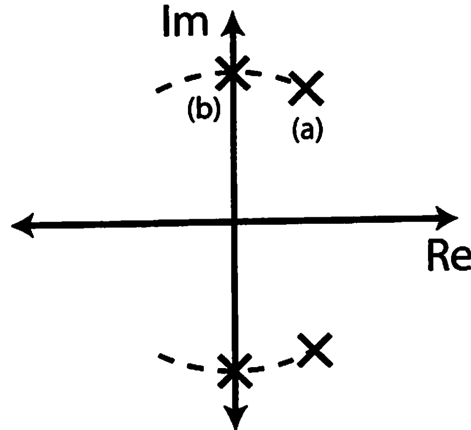

Figure 5.2: Root locus of basic oscillator model in (a) startup and (b) steady-state

back to the imaginary axis, stabilizing the amplitude. Position (b) in Figure 5.2 represents the steady-state condition. The amplitude limiting mechanism depends on both bias current and supply voltage [27]. Initially, the shape of the drain current waveform is a sinusoid, but as the amplitude grows the transistor eventually operates almost like a switch. A plot of the drain current looks like pulses whose magnitude is determined by the available bias current. Therefore, the peak output swing will be proportional to the bias current:

$$\hat{V}_o \propto I_{bias} R_{tank} \tag{5.1}$$

If the bias current is increased, amplitude will also increase. Thus, this region is known as the *current-limited* regime.

As the bias current is increased or (equivalently) the supply voltage reduced,

the output swing becomes limited by the available voltage headroom. Once the swing becomes large enough so that the active devices leave the saturation region, nonlinearities become significant and the amplitude saturates. Beyond this point, increasing the bias current no longer increases the output swing. Consequently, the oscillator is described as *voltage-limited.*

It is important to understand the operating regimes described above in order to maximize oscillator output swing and power efficiency. Maximizing output swing helps to reduce phase noise, which is an important performance metric for oscillators used in communication systems. The simple Leeson model for oscillator phase noise is given by [28, 29]:

$$L(\Delta\omega) = 10\log\left(\frac{2FkT}{P_{sig}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right) \tag{5.2}$$

where L is the phase noise in dBc/Hz at a given offset frequency $\Delta\omega$ from the carrier ω_0. The loaded quality factor of the tank is given by Q, while P_{sig} is the signal power at the input of the oscillator. The noise contributed by the oscillator itself is represented by its noise factor F. More rigorous phase noise models have since been developed [30], but the original Leeson formula of Equation 5.2 provides intuition about the major factors that determine oscillator phase noise. Most importantly, note that increasing signal swing (P_{sig}) and tank quality factor helps to lower phase noise.

With oscillator basics established, the next step is to choose an oscillator topology that meets the requirements for the design as outlined in Section 5.2.

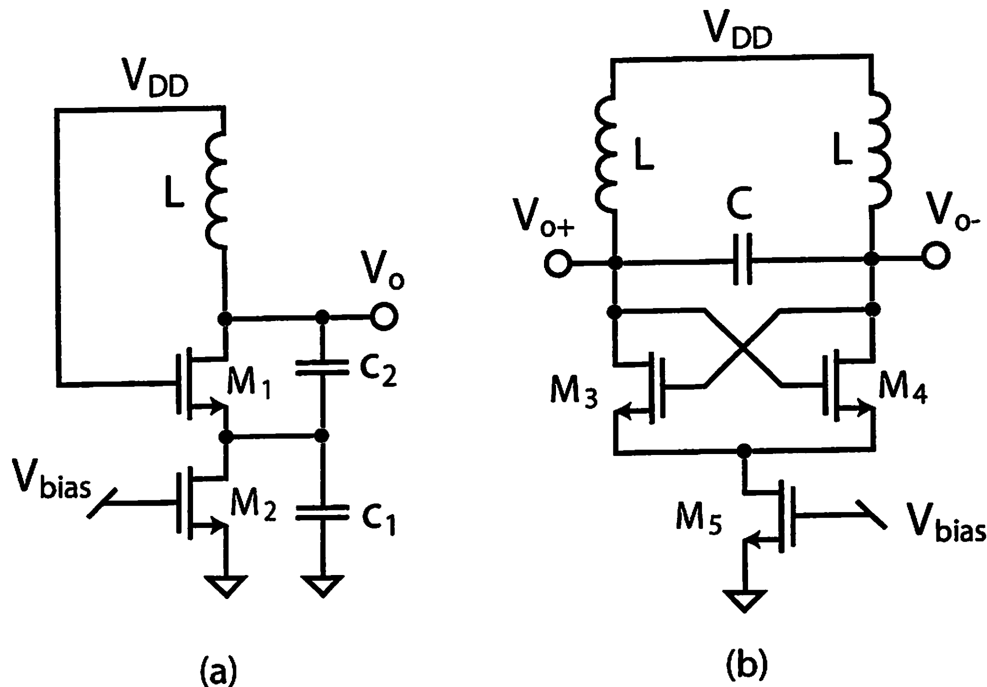

Figure 5.3: (a) Colpitts topology (b) Cross-coupled differential topology

5.4 Topology Choice

There are a wide range of oscillator topologies available in modern integrated circuits. Possibilities include ring oscillators, relaxation oscillators, and resonant tank tuned oscillators. For this design, where the intended application is wireless communications systems, a resonant tank oscillator is preferred because it will provide lower phase noise, due to the higher energy storage capability (Q) of LC tanks. One of the primary design goals is low voltage operation, so the chosen topology should be able to operate on a low supply voltage.

Within the category of tuned oscillators, the circuit may take either single-ended or differential form. A classic example of a single-ended design is the Colpitts topology, shown in Figure 5.3(a). A capacitive transformer formed by C_1 and C_2 feeds back the output signal at the drain of M_1 to the source node, establishing the positive feedback required for oscillation.

A fully differential tuned oscillator is shown in Figure 5.3(b). Here, the cross-coupled pair M_3 and M_4 provide the necessary negative transconductance to cancel the losses in the tank. This topology may also be viewed as the series cascade of two tuned amplifiers in a positive feedback configuration.

The differential topology provides two key advantages. First, the differential output is inherently less sensitive to common-mode noise, such as supply voltage variation and substrate noise. Secondly, a fully differential oscillator may provide a larger output swing when the supply voltage limits the swing. To see this, recall from Section 5.3 that an oscillator may operate in either current-limited or voltage-limited regimes. If the oscillator is current-limited, the swing is proportional to bias current and both topologies will have equivalent output swing for a given bias current. However, if the oscillator is voltage-limited, the differential topology has an advantage because the two individual devices only need to provide half the total swing. Therefore, the cross-coupled differential topology is chosen for this design. There are several variations on the differential topology depending on the biasing method. The complementary topology [27], using both NMOS and PMOS cross-coupled pairs, is popular but impractical for this design because it contains three stacked transistors. In order to enable operation on a low voltage supply, a standard topology is chosen

with NMOS cross-coupled pair and NMOS tail device for biasing.

5.5 Circuit Design

The complete circuit design consists of both the oscillator core and buffers to drive the signal off-chip. In the next section, the core design is described, followed by the buffer design.

5.5.1 Oscillator Core

With the basic topology selected, the next step is to define the design space, starting with the tank parameters. The oscillation frequency is given by the familiar equation for the resonant frequency of an LC tank:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{5.3}$$

The target oscillation frequency is chosen to be 1.5GHz as a convenient frequency point to demonstrate subthreshold transistor operation. In Chapter 4, a model was developed for the 10nH integrated inductor. Using this inductor and solving Equation 5.3 for the required tank capacitance at 1.5GHz yields about 1.1pF. This establishes the total capacitance budget for the entire oscillator, including device capacitance, inductor parasitics, and output buffers.

The final oscillator schematic is shown in Figure 5.4. The core supply voltage, $V_{DD,osc}$, is chosen to be 0.5V for nominal operation. Designing for this mid-range

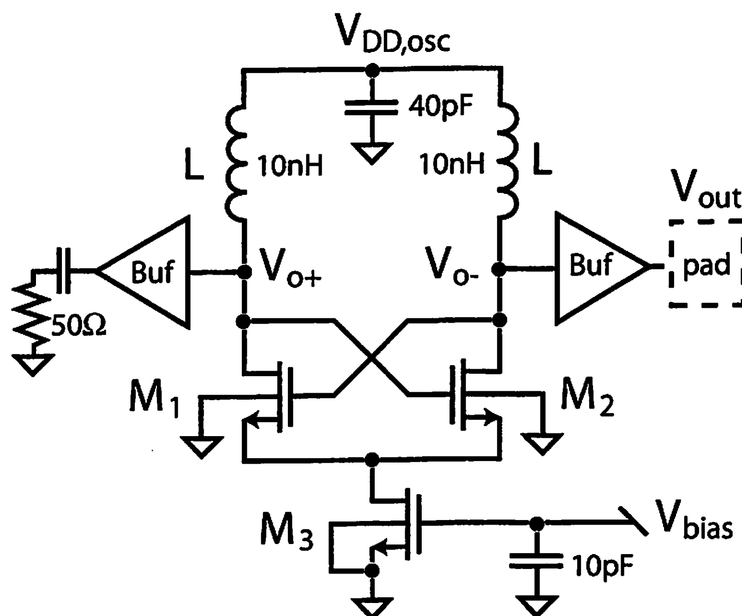

Figure 5.4: Complete schematic of final oscillator design

supply will allow the circuit to be easily tested with both ultra low supply (below 0.5V) and a more typical 1.2V. The core bias current through tail transistor M_3 is controlled by externally applied voltage V_{bias} on the gate of M_3. The required bias current is determined by both startup and output swing specifications; startup requirements are considered next.

In the fully-differential topology, the cross-coupled pair presents a small-signal negative resistance equal to $-1/g_{m1,2}$. As outlined in Section 5.3, the cross-coupled pair must provide enough negative resistance to cancel the tank losses and allow oscillations to build up. Therefore, the critical parameter for oscillator startup is the transconductance of the cross-coupled devices. The required g_m for startup establishes a lower limit on the current consumption of the oscillator.

To determine the necessary g_m for startup, the tank losses must first be calculated from the inductor model. In Chapter 4, the calculated Q_{tank} was about 4.5 at 1.5GHz. At the resonant frequency, the LC tank may be modeled as depicted in Figure 5.1, where the tank losses are contained in the conductance G_T. The equivalent parallel resistance at resonance may be calculated by treating the capacitor as lossless and calculating the parallel conductance G_T for an inductor with finite Q given by the overall tank quality factor:

$$R_{p,tank} = \frac{1}{G_T} = Q_{tank}\omega L \tag{5.4}$$

At 1.5GHz, the calculated $R_{p,tank} \approx 400\Omega$. Therefore, the minimum g_m required for

startup is:

$$g_{m,crit} = \frac{1}{R_{p,tank}} \approx 2.5\text{mS} \tag{5.5}$$

In practice, the differential pair is designed to have a transconductance that is twice the minimum value in order to ensure reliable startup. The specified transconductance is therefore set at 5mS.

Equation 5.4 shows explicitly why large inductance values are beneficial from a power consumption perspective; for a given Q, the parallel tank resistance is directly proportional to the inductance L. For a given operating frequency, therefore, it is desirable to use the largest possible inductor in the LC tank, reducing the tank capacitance appropriately. In practice, the size of the inductor is usually limited by the difficulty of implementing large coils on-chip; as outlined in Chapter 4, inductors larger than 10nH are not normally integrated on the die. The importance of high Q inductors is also plain from Equations 5.4 and 5.5. The critical transconductance for startup is inversely proportional to tank quality factor, so an improvement in inductor Q leads directly to reduced startup current requirements and lower power consumption.

To optimize the transconductance for minimal bias current, devices M_1 and M_2 are designed to operate with inversion coefficient between 0.1 and 1. Referring to Figure 3.8, g_m/I_D of around 20 to 25 is achievable in this range. Sizing of M_1 and M_2 then proceeds by choosing a nominal bias current and calculating the required aspect ration W/L:

$$\frac{W}{L} = \frac{I_{tail}}{2I_0(IC)} \tag{5.6}$$

where IC is the desired inversion coefficient and specific current I_0 is the value extracted in Chapter 3 for low threshold NMOS devices with minimum channel length (given in Table 3.1 as 662nA). The total bias current sourced by M_3 is designated I_{tail}, and the current flowing in either M_1 or M_2 is therefore $I_{tail}/2$. As discussed above, at the target inversion level the device g_m will be 25 times the bias current. The required transconductance for startup is 5mS, leading to a first estimate of 400μA for the nominal bias current.

Above, the bias current is chosen based on startup requirements. However, recall that the output swing is also dependent on the tail current according to Equation 5.1. In steady state oscillation, the differential pair devices behave as switches and the tail current is fully commutated back and forth between M_1 and M_2, generating the maximum output swing at the fundamental frequency for that bias current; higher harmonics are attenuated by the LC tank. Assuming a square wave shape for the current in M_1 or M_2, the proportionality constant in Equation 5.1 is $4/\pi$ [27], and the predicted differential output swing for $I_{tail} = 400\mu$A is 200mV. If this output swing is not sufficient for the application, the oscillator is swing-limited and the bias current or tank Q must be increased. Although small compared to traditional low phase noise oscillators, this output swing is acceptable for the ultra low power oscillator designed here. Of course, the output swing will vary depending on the bias current being tested. In reality, the output swing prediction above is optimistic for small swing because the differential pair will not switch hard enough to generate a square current waveform.

With an estimate of the bias current, sizing of the main transconductor devices

M_1 and M_2 may now proceed by calculating W and L via Equation 5.6. For operation in weak inversion, it is desirable to size the devices as large as possible for a given bias current; the limiting factor then becomes transistor parasitic capacitance. The total capacitance budget was calculated earlier in this section as 1.1pF, in order to resonate with the 10nH inductor at the desired frequency. This value represents the total capacitance allowed on each of the individual output nodes (V_{o+} and V_{o-} in Figure 5.4). The capacitance on these nodes arises from several different sources and is summarized in the following relation:

$$C_{total} = C_{device} + C_{inductor} + C_{buffer} + C_{parasitic} \tag{5.7}$$

where

$$\begin{aligned} C_{device} &= \text{all parasitics associated with } M_1 \text{ and } M_2 \\ C_{inductor} &= \text{parasitic capacitance from inductor model} \\ C_{buffer} &= \text{input capacitance of buffer} \\ C_{parasitic} &= \text{any additional layout parasitics} \end{aligned}$$

In Equation 5.7, the last three terms are relatively fixed. The inductor contributes 280fF of capacitance, while an additional 100fF are budgeted for layout parasitics. The buffer input capacitance is dependent on the buffer design itself, but it is reasonable to allocate 100fF for a typical source follower topology, leaving 620fF for the

devices. The equivalent device capacitance on each output is given by:

$$C_{device} \approx C_{gg} + 4C_{dd} \tag{5.8}$$

where C_{gg} and C_{dd} are the total gate and drain capacitances from the BSIM3V3 model, respectively. The factor of 4 for C_{dd} is due to the Miller multiplication of the two gate-drain capacitances connected across the output. The model capacitances also include the drain to substrate diodes, which are not Miller multiplied, so Equation 5.8 is approximate. Devices M_1 and M_2 should now be sized with W/L as large as possible within the capacitance budget. Differential pair devices in oscillators are often designed with non-minimum channel length to reduce flicker noise [31], but in this design minimum 0.13μm lengths are chosen since large devices will be necessary for weak inversion operation. For longer channel lengths, the required width will also be greater, leading to prohibitively large parasitic capacitance.

Subject to the constraints outlined above, the final device W/L for M_1 and M_2 was chosen to be 240μm/0.13μm. Low threshold devices are used for M_1 and M_2 to minimize the required voltage headroom. The resulting inversion coefficient at the nominal 400μA bias current is 0.16, which is near the desired bias point between weak and moderate inversion. Figure 5.5 indicates the nominal operating point on the transconductance efficiency curve, along with the expected range of test bias points. Figure 5.5 also demonstrates the range of feasible operating points for practical designs. For a fairly large W/L ratio of 240μm/0.13μm, the device operates between weak and moderate inversion. For the same bias current, a device operating with

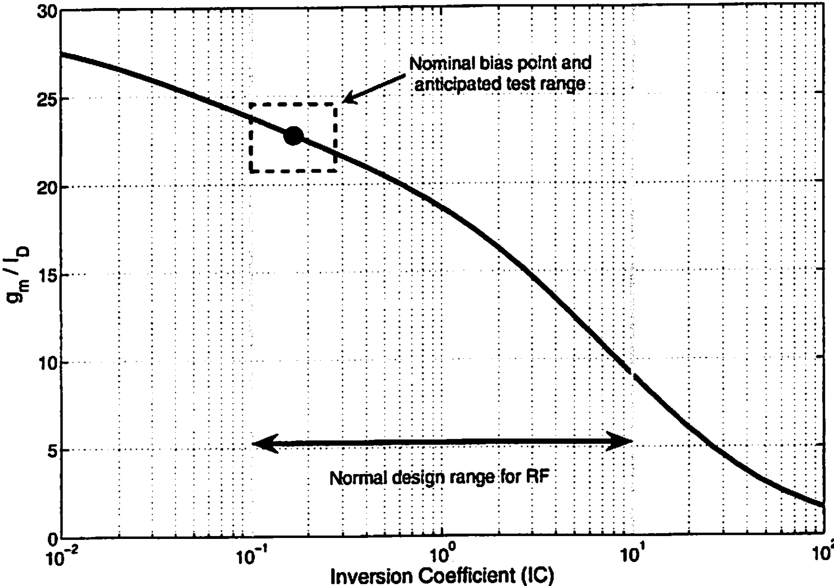

Figure 5.5: Operating point of M_1 and M_2 on inversion coefficient curve

$IC = 0.01$ would require an aspect ratio 16 times larger, having unacceptably large parasitics. The device bandwidth would also be insufficient for most RF designs. To see the overall trends, it is instructive to generate the design plots in Chapter 3 over a large range of inversion coefficient; in practice, however, most designs will utilize transistors biased with $0.1 < IC < 10$.

Finally, the tail current source device M_3 is sized primarily for high output resistance r_o. Accordingly, a long 1μm channel length is adopted, and the device operates in strong inversion. In retrospect, it would be better to size M_3 to operate in weak inversion, taking advantage of the low saturation voltage in that regime. As the supply voltage is reduced, M_3 eventually enters the triode region, which limits the minimum V_{DD}. The low V_{Dsat} achievable in subthreshold would enable testing at the lowest possible supply voltage.

5.5.2 Output Buffer

Output buffers are necessary for measurement in order to drive instrumentation with 50Ω inputs. The only requirement for the buffer is that it should not load the oscillator excessively. An NMOS source follower topology was chosen due to its low input capacitance and flat gain response over a wide range of frequencies. A schematic of the output buffer design is depicted in Figure 5.6. The output impedance of the follower is $1/g_{m5}$, requiring

$$50\Omega = \frac{1}{g_{m5}} \Rightarrow g_{m5} = 20\text{mS}$$

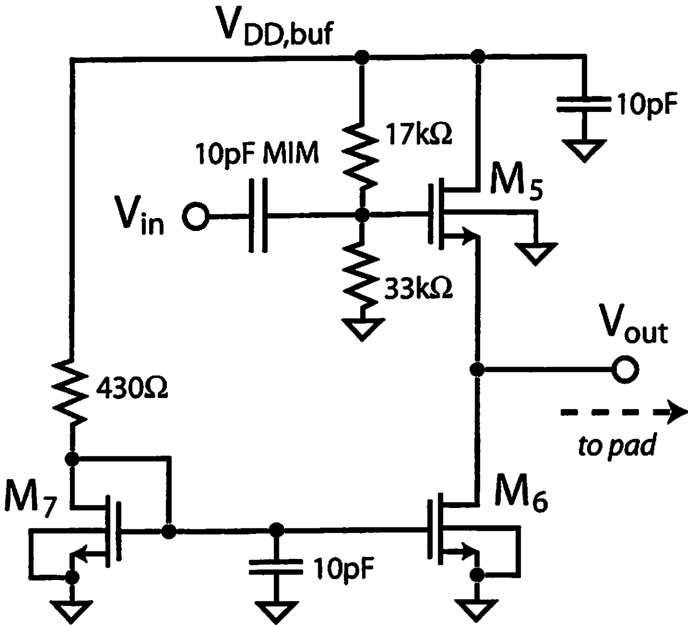

Figure 5.6: Complete schematic of output buffer

For high bandwidth and low input capacitance, signal transistor M_5 is sized to operate in strong inversion with $IC \approx 5$. Referring back to Figure 3.8, g_m/I_D is around 10 in this region, dictating a bias current of approximately 2mA and device aspect ratio $W/L = (100/0.13)\mu$m. When driving a 50Ω load, the simulated gain of the buffer is roughly -6dB up to 10GHz, which is plenty of bandwidth for this application.

The buffer operates from a separate 1.2V supply to facilitate oscillator core testing with a wide range of supply voltages. Since the oscillator DC output level varies with the supply voltage, the buffer is AC-coupled to the oscillator output through a 10pF metal–insulator–metal (MIM) capacitor, forming a 1.4MHz high-pass response. A MIM capacitor was chosen because of its high quality and small backplate parasitics.

For measurement simplicity, only one of the differential outputs is brought out to a pad. To ensure matched loading on the oscillator core, however, a separate buffer is included for both outputs and one output is simply terminated with a 50Ω resistor on-chip. This is shown schematically in Figure 5.4. The simulated input capacitance of the buffer is approximately 100 fF, including layout parasitics, which is acceptable loading for the oscillator core. The total current consumption of each buffer, including biasing, is about 4.5mA from a 1.2V supply. The final device types and aspect ratios are summarized in Table 5.1; the inversion coefficient for each device is also tabulated.

Device	*Threshold*	*Sizing* (μm/μm)	*IC*
M_1,M_2	low	240/0.13	0.16
M_3	high	30/1	22
M_5-M_7	low	100/0.13	4

Table 5.1: Device type, sizing, and IC for oscillator and buffer transistors

5.6 Implementation and Layout

The final design is realized in a 0.13μm standard CMOS process with 6 metal layers from STMicroelectronics. For high frequency circuits, layout must be done carefully to avoid introducing unnecessary loss and parasitics. In this design, the most sensitive nodes are the cross-coupled gates of the differential pair. In particular, the traces that connect to the inductors must be as short as possible to avoid introducing any additional loss in the tank.

The oscillator was designed and laid out so that it was possible to test entirely using wafer probes, without requiring a printed circuit board. This was accomplished by limiting the design to four DC bias lines and one RF output. Probe testing enabled the flexible testing of several dice without the cost of multiple printed circuit boards. All resistors are implemented with unsilicided $p+$ polysilicon. To avoid the need for an additional probe, the buffer is self-biasing using a resistor and current mirror device M_7. Ample poly to n-well decoupling capacitors are connected to the supply rail and bias nodes in order to suppress supply noise.

To investigate the effect of different integrated inductor structures, a second version of the oscillator was also fabricated using a different inductor. This coil was

entirely generated using commercial parameterized cells, which are qualified for the process. The nominal inductance is 10nH, and the same trace width and spacing are used for both coils. However, the new inductor is different from the inductor presented in Chapter 4 in several key ways. First, it adds a third shunt layer, in addition to Metal 6 and Metal 5, employing the top aluminum MIM layer, which should reduce the series resistance slightly. In addition, it includes a patterned groundshield on the substrate made from poly and active, which helps to isolate the inductor from the substrate, thus reducing loss and enhancing the Q [32]. Unfortunately, the presence of a groundshield also increases the parasitic capacitance to the substrate, degrading the self-resonant frequency. Note also that second inductor has 6.5 turns as opposed to only 3.5 for the original one, resulting in a somewhat smaller diameter of about 350μm.

For convenience, the original inductor and new inductor will be referred to as $L2$ and $L3$, respectively, referring to the number of shunt layers used in each structure. Figures 5.7 and 5.8 show the layout of both inductors. The patterned groundshield is visible in Figure 5.8, with alternating lines of polysilicon and active running perpendicular to the inductor coil on all sides.

All the circuits were identical for both oscillator designs; the inductor type was the only variable. Care was taken in layout to maintain similar connection lengths and overall geometries for both versions, allowing a direct comparison of measurements between the two different inductor structures. Unfortunately, no die area was available for a standalone test structure for this inductor, so it was not possible to extract a circuit model. Figures 5.9 and 5.10 present die photos of both oscillators.

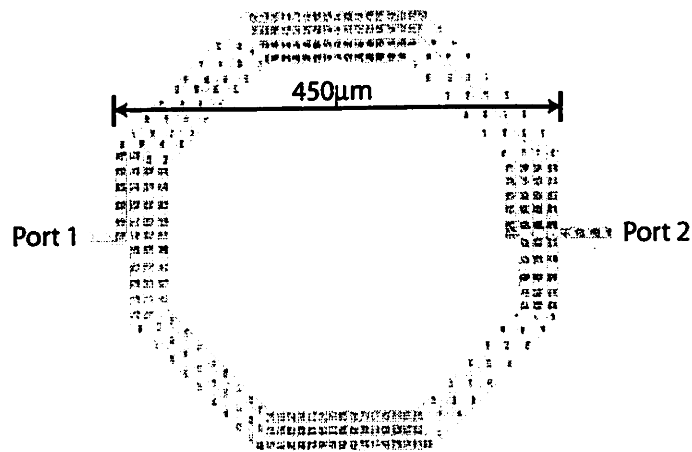

Figure 5.7: Layout capture of basic inductor $L2$

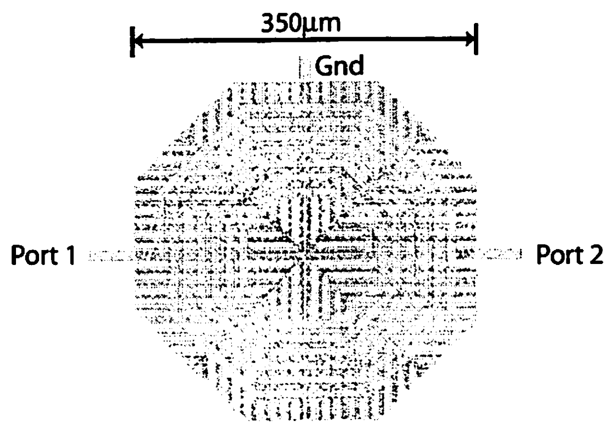

Figure 5.8: Layout capture of advanced inductor $L3$ with shield

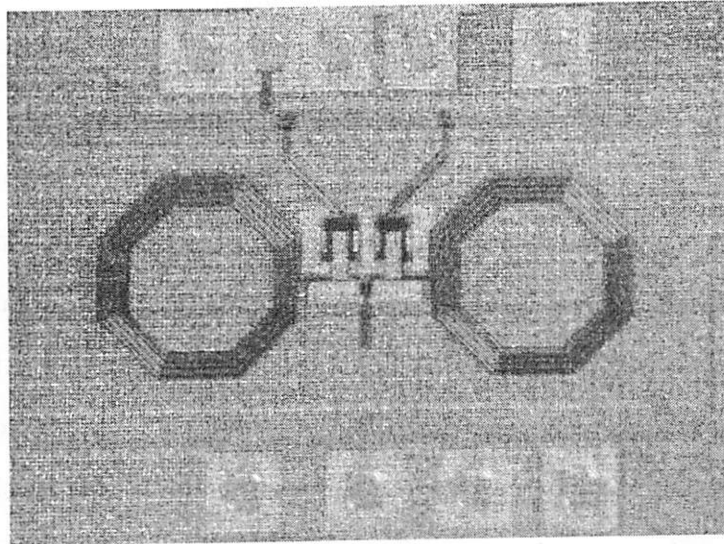

Figure 5.9: Photo of oscillator with $L2$

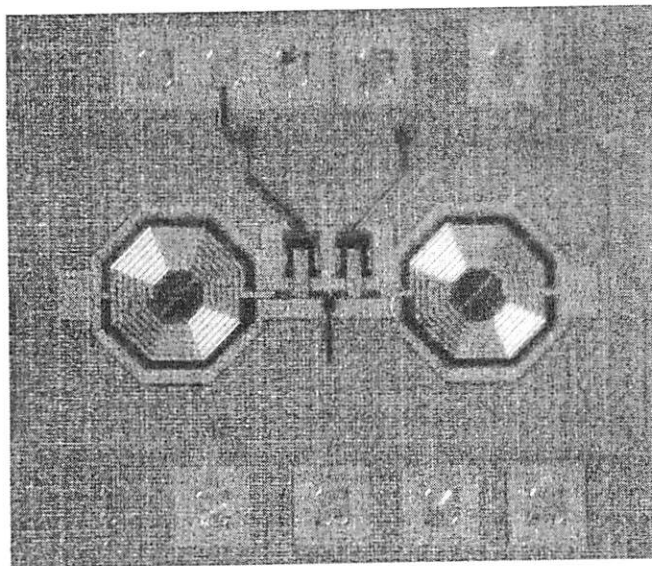

Figure 5.10: Photo of oscillator with $L3$

Protection from electrostatic discharge (ESD) is accomplished by the use of protection diodes on all DC pads. No ESD diodes are present on the buffer RF output since this node is sensitive to parasitic capacitance. In addition to ESD protection, immunity to plasma-induced charging effects is also critical. Modern CMOS processes make heavy use plasma-enhanced steps for etching and deposition, and during processing it is possible for local variations to cause charge build-up on metal lines [33]. If these lines are connected to transistor gates, which is often the case, oxide degradation or even complete breakdown may occur. In this design, the supply voltage lines for the oscillator core and buffer run all the way around the chip, resulting in very long traces. To remedy the problem, small diodes are strategically placed near the decoupling capacitors, connecting the first metal layer to the substrate and providing a discharge path for all subsequent metal layers during fabrication.

Chapter 6

Results

6.1 Measurement Setup and Instrumentation

In this section, measurement results from the fabricated oscillator are presented. Excluding phase noise, all measurements were performed on a Cascade Microtech probestation with a Cascade 40GHz Infinity ground–signal–ground (GSG) RF probe. As described in Section 5.5.2, the oscillator output is single-ended, meaning that only one RF probe is necessary and precluding the need for an output balun. Oscillation frequency and output voltage swing were measured with an HP 8563E spectrum analyzer. The time domain startup transient was obtained with an Agilent Infiniium 54844A sampling oscilloscope. Supply and bias voltages were generated with an HP 6626A DC power supply.

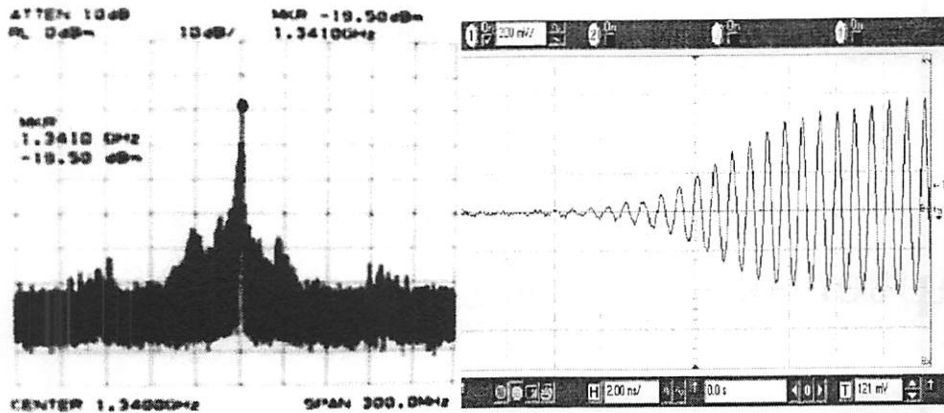

Figure 6.1: Measured output spectrum and startup transient

6.2 Nominal Performance

As defined in Section 5.5.1, the nominal oscillator bias conditions are $I_{tail} = 400\mu A$ and $V_{DD} = 0.5V$. Figure 6.1 shows a capture of the output spectrum and startup transient for the oscillator with three layer inductor and groundshield ($L3$). The nominal oscillation frequency is 1.35GHz with 20mV zero-peak swing at the buffer output. The spurs on either side of the fundamental are most likely due to noise from the switching power supply, since the spurs were not observed in the phase noise measurement, where a battery was used for the supply. Since the buffer output is single-ended and driving the 50Ω instrument input, the in-situ differential voltage swing is approximately 4 times higher than the measured swing (assuming that the actual gain of the buffer is exactly -6dB). The transient capture shows that the startup time for this bias point is approximately 10ns.

6.3 Performance Across Bias Conditions

As outlined in Section 5.2, the oscillator is designed to be tested over a wide range of bias points in order to verify performance at low supply voltages along with various levels of inversion. Oscillation frequency and output swing are the two performance metrics of interest; accordingly, two different parameter sweeps were performed. First, the tail bias current is held constant while supply voltage is varied. This verifies the functionality at low supply voltages. Secondly, the bias current is swept while supply voltage is held constant at a nominal value. This measurement demonstrates the performance for different transistor regions of operation.

6.3.1 Varying Supply Voltage

Figure 6.2 shows the measured oscillation frequency as V_{DD} is swept from 0.3V to 1.2V. Bias current through the tail device is held constant at 400μA for all measurements. This results in an inversion coefficient of about 0.16, so the cross-coupled pair operates in weak to moderate inversion. Measured data is displayed for oscillators using both $L2$ and $L3$ alongside circuit simulations incorporating the inductor model of Chapter 4. The nonlinear device capacitance changes with applied voltage, so the oscillation frequency varies across the supply range. For low supply voltages, the drain-source voltage of the tail current source transistor is compressed and the device enters the triode region. Beyond this point, it becomes difficult to bias the oscillator at the constant 400μA. As shown in the figure, the oscillator with inductor $L3$ operates all the way down to 250mV, while the $L2$ oscillator stops at 300mV.

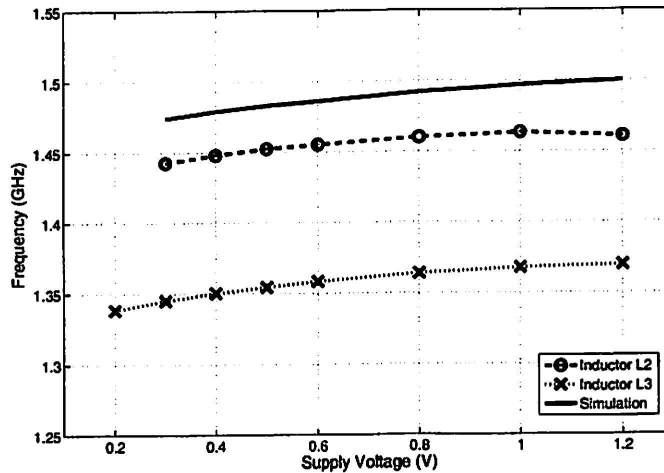

Figure 6.2: Variation of frequency for range of V_{DD}

The frequency of Oscillator $L3$ is about 100MHz lower across the entire range, confirming that the addition of a groundshield to the structure increases the parasitic capacitance associated with the inductor. The measured data for Oscillator $L2$ is closer to simulations, since the simulations use the inductor model extracted from measurements. The small discrepancy is probably due to layout parasitics that are not modeled in the simulations.

Figure 6.3 plots the output swing for the same supply voltage sweep. Note that the output swing stays nearly constant across the entire range. The oscillator maintains equal performance even at extremely low supply voltages of less than 300mV. In fact, Oscillator $L3$ is able to operate at 200mV with no output swing degradation. Since the output swing is constant across supply, both oscillators are operating in the current-limited regime where the output swing is proportional to bias current. Note

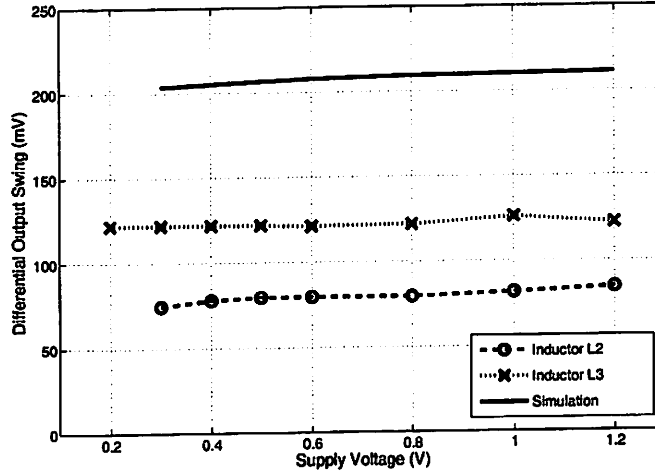

Figure 6.3: Variation of output swing for range of V_{DD}

also that the output swing of Oscillator $L3$ is about 50% higher than Oscillator $L2$. This indicates that the quality factor of inductor $L3$ is higher than that of $L2$, since the equivalent parallel resistance of the tank at resonance is proportional to Q. The higher quality factor of $L3$ makes sense since it has more metal layers in parallel and the groundshield should reduce losses in the substrate.

The measured output swing for both oscillators is substantially lower than the simulated values. There a several possible causes for this. One possible explanation is that the actual gain of the output buffer is not exactly 1/2. Any gain error or impedance mismatch in the buffer will directly alter the measured swing. It is also possible that parasitic resistance in the layout is causing increased losses in the tank. However, parasitic extraction on the actual layout resulted in no substantial decrease in output swing. A final possibility is the non-quasi-static effect [10]. Since the

transistors are biased in subthreshold, the operation frequency is getting closer to f_T. At frequencies close to f_T, the quasi-static approximation no longer holds, and the real gate resistance will degrade the tank Q. This effect is not modeled in simulation, so it could be the cause of the disagreement. This point highlights the need for more accurate CMOS models for RF design. Designing circuits to operate in weak or moderate inversion may need to take this effect into account.

6.3.2 Varying Bias Current

Figures 6.4 and 6.5 again present the variation of frequency and output swing, but this time the supply is held constant at 0.5V and bias current is swept up to 600μA. On the low end, the bias current is reduced until the oscillator no longer starts up reliably.

These measurements confirm that inductor $L3$ has higher Q, since its minimum current for startup is 250μA. The necessary transconductance (and therefore bias current) for startup is determined by Equations 5.4 and 5.5. Oscillator $L2$, with a lower Q inductor, requires 350μA of startup current. At a bias current of 600μA, the inversion coefficient is approximately 0.25 and close to the center of moderate inversion. For low bias currents of 250μA to 350μA the inversion coefficient is closer to weak inversion with $IC \approx 0.1$.

Note that Figure 6.5 illustrates a linear dependence of output swing on bias current, confirming that the oscillator is operating in the current-limited regime. This is because the output swing is small enough that it is not being limited by the available voltage headroom.

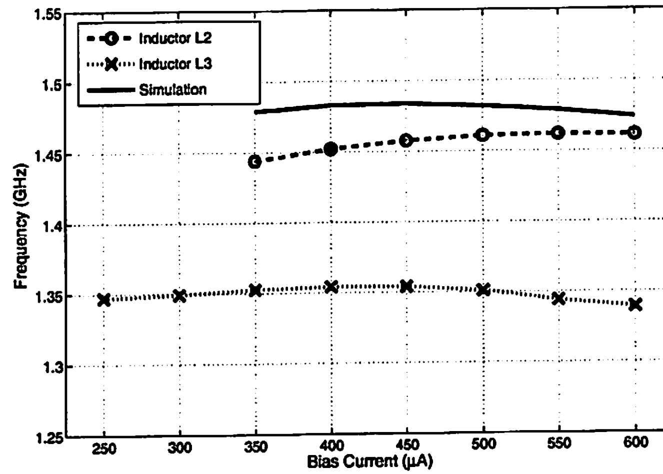

Figure 6.4: Variation of frequency for range of I_{bias}

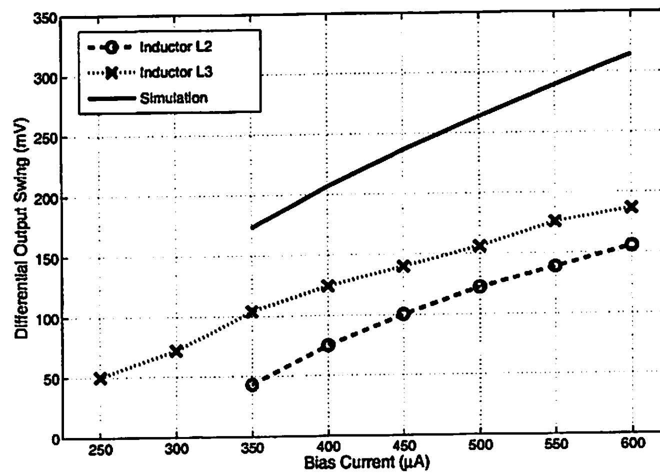

Figure 6.5: Variation of output swing for range of I_{bias}

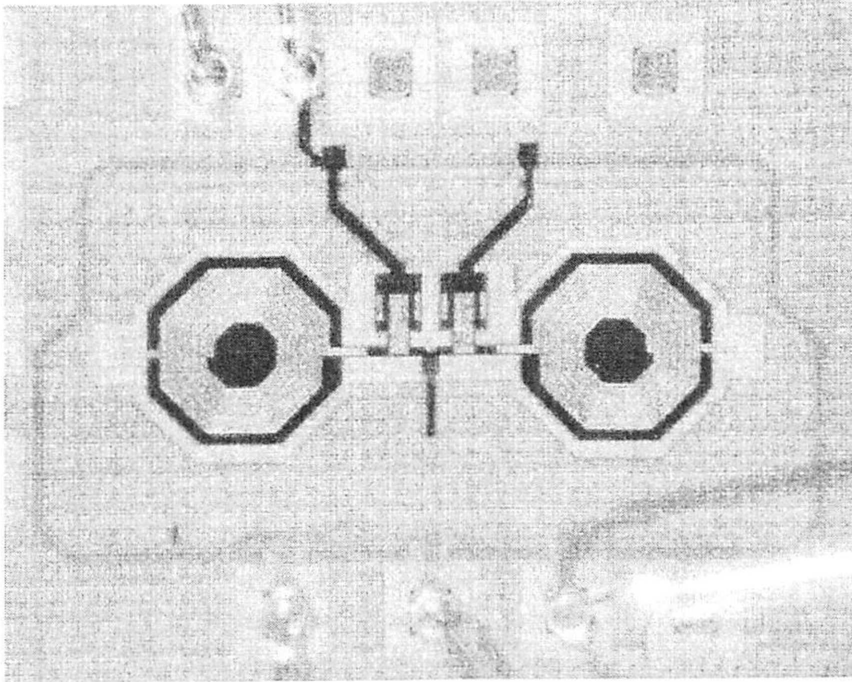

Figure 6.6: Photo of bonded oscillator on printed circuit board

6.4 Phase Noise Performance

In order to measure phase noise, the die was mounted on a printed circuit board using standard chip-on-board (COB) technology and wirebond connections to the die. Oscillator $L3$ was measured since the higher inductor Q will result in the lowest phase noise. All phase noise measurements were done with an Agilent E4440A spectrum analyzer. Figure 6.6 shows the oscillator that was bonded out to the test board.

Figure 6.7 shows the phase noise spectrum for one representative bias point. For this measurement, $V_{DD,osc}$ and $V_{DD,buf}$ are both set at 1.3V and supplied directly from a battery for low supply noise. V_{bias}, which controls the current in the oscillator

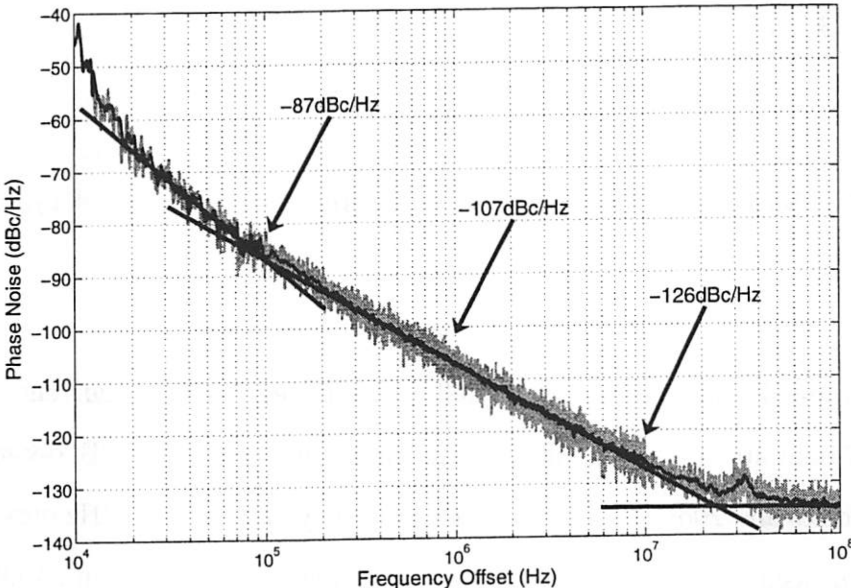

Figure 6.7: Measured phase noise spectrum

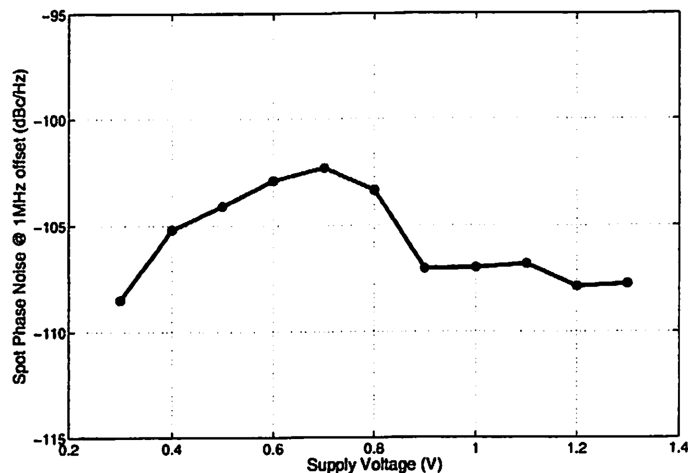

Figure 6.8: Measured spot phase noise at 1 MHz offset for range of V_{DD}

core, is bootstrapped from the battery as well and adjusted for a bias current of 400 μA. Figure 6.7 exhibits the classic phase noise shape, dropping off 30dB/decade for close-in frequencies and 20dB/decade at higher frequency offsets. At 1MHz offset, the phase noise is measured to be -107dBc/Hz. The 1/f noise corner is around 100kHz.

Figure 6.8 illustrates the effect of supply voltage on phase noise at a fixed 1 MHz offset. Spot noise is plotted for V_{DD} ranging from 0.3V to 1.3V, with bias current held constant at 400 μA. The phase noise exhibits minor variation that may be attributed to the limited resolution in the adjustment of bias current. Since the output swing remains constant even for low supply voltages, the phase noise varies by only a few dB down to $V_{DD} = 300mV$. Most importantly, the phase noise is not significantly degraded for reduced supply voltages.

	[34]	*This work*
Technology	0.18μm CMOS	0.13μm CMOS
Supply voltage	1.5V	0.5V
Bias current	3.2mA	400μA
Core power	4.8mW	200μW
Phase noise	-123.5dBc/Hz at 600kHz	-103dBc/Hz at 600kHz

Table 6.1: Comparison to other published work

6.5 Comparison to Traditional Oscillators

Traditionally, most RF oscillator research has been focused on voltage- controlled oscillators (VCOs) for wireless communication systems. In these systems, the VCO is used in a synthesizer to provide a well-known frequency reference. In the receiver, the synthesizer supplies the local oscillator to drive down-conversion mixers. Likewise, the transmitter needs the synthesizer to generate a carrier frequency. In both of these applications, the phase noise and output swing are the most critical oscillator performance metrics since wireless standards often specify very low phase noise. Power consumption is a concern, but phase noise requirements take priority.

The oscillator demonstrated in this research is a significant departure from these traditional VCOs. To put things in perspective, it is useful to compare the oscillator performance with other published VCO work. Table 6.1 presents a few of the relevant performance numbers for a recent voltage-controlled oscillator [34].

Since the VCO in [34] is designed to meet difficult phase noise specifications, it requires much more power. The phase noise of the oscillator presented here is clearly not adequate for typical cellphone standards like GSM. However, the cause of the

poor phase noise performance is the low output swing, as dictated by the low bias current. It is possible to increase the output swing by using higher Q inductors or burning more power. Bondwire inductors regularly provide a factor of ten in Q-factor improvement. In certain applications, it may be possible to operate with relaxed phase noise specifications and this work shows that there is room to reduce the power consumption significantly for these applications.

Chapter 7

Conclusions

7.1 Summary of results

In this research, design approaches and methodologies were presented to enable the realization of very low power RF circuits for wireless sensor networks. Subthreshold device operation was explored as a possible method of reducing power consumption in transceiver circuits, along with the use of unusually low supply voltages. To demonstrate the techniques, an oscillator core was designed and tested, with two versions fabricated to compare the performance of different integrated inductor layouts.

Ultimately, the ability to design a 1.5GHz oscillator with nominal power consumption below 200μW was demonstrated. The minimum power consumption achieved was less than 100μW. The circuit was biased to run in weak inversion, and operation with a supply voltage of less than 300mV was also demonstrated.

7.2 Future Work

In Chapter 2, the concept of asynchronous communication using ultra low power wakeup radios was introduced. The eventual objective of this research is to develop a carrier sense receiver consuming less than 50μW when active, enabling an entirely reactive radio architecture. To accomplish this goal, the most important component is the development and application of low power circuit techniques for the RF transceiver. The techniques described and applied in this research are a first step towards the realization of the carrier sense receiver.

Building on the low power oscillator work presented here, the addition of frequency tuning is an area for future research. Traditional analog varactor frequency tuning may prove to be problematic for very low supply voltages, since the required varactor tuning voltage may be quite large. Digital frequency tuning using switched capacitors is one possible solution to this problem [35, 36].

In addition, future development in RF-MEMS may provide exciting alternatives to existing on-chip passive components. For the oscillator designed here, the low quality of the integrated inductors sets the lower bound on power consumption of the oscillator core. The use of MEMS resonator structures in transceiver circuits is an area for future exploration, as these components may help to reduce power consumption by eliminating the dependence on low Q passives.

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