A 3-10GHz Ultra-Wideband Pulser

Jan M. Rabaey
Simone Gambini
Davide Guermandi

Electrical Engineering and Computer Sciences
University of California at Berkeley

Technical Report No. UCB/EECS-2006-136
http://www.eecs.berkeley.edu/Pubs/TechRpts/2006/EECS-2006-136.html

October 19, 2006

Acknowledgement

The authors Acknowledge ST microelectronics for Chip fabrication and GSRC for funding

An UltraWideBand 3-10 GHz Pulser

We approach the design of a UWB pulser for carrier-based 3-10GHz systems. This first transmitter prototype uses the carrier VCO itself to generate the duty cycling signal, and does not require any external component. (See Fig.1)

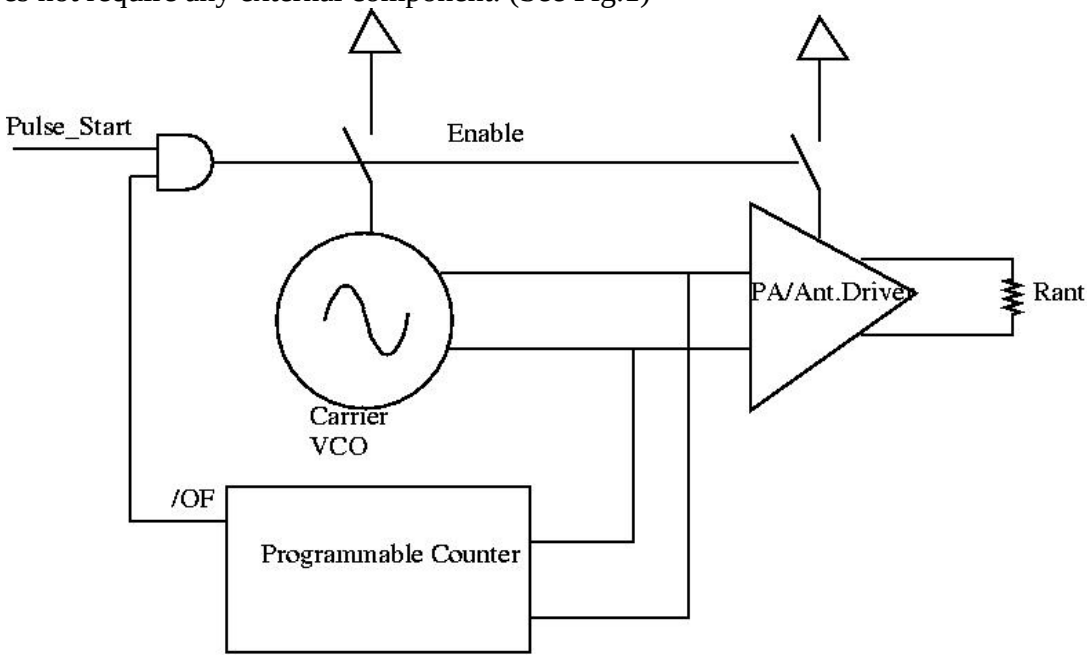

Figure 1:Pulser Architecture

Relying on the accuracy of the VCO obviates the need for bandwidth calibration, and hence of an off the chip frequency reference.

In the following discussion the bandwidth of the signal is intended as the wideness of the main lobe in the power spectrum. Remember that an UWB signal requires at least a 500 MHz bandwidth. The transmitter exploits the fact that for carrier-based high-frequency UWB, the VCO defining the carrier always has a period shorter than the pulse duration and can be therefore be used as a time base. A divider is therefore used to define the pulse duration from the carrier by counting a fixed number of cycles. Neglecting oscillation startup and decay times, the approach gives a pulse shape that is a modulated rectangular wave.

For N periods of a sine wave at frequency f_0 the bandwidth (according to the previous definition) is given by $BW = 2\ f_0/N$.
A single period gives a main lobe from 0 to 2 f_0 ($BW = 2f_0$), 2 periods gives a main lobe between $f_0/2$ and $3/2\ f_0$ ($BW = f_0$) and so on.

For a 500 MHz bandwidth (with a step of 250 MHz in the VCO frequency) the generated UWB spectrums are shown in figure 2. A maximum division ratio of 32 is assumed, resulting in a bandwidth slightly higher than 500 MHz for the highest frequencies.
The minimum VCO frequency is 3.25 GHz, the maximum 9.75 GHz.

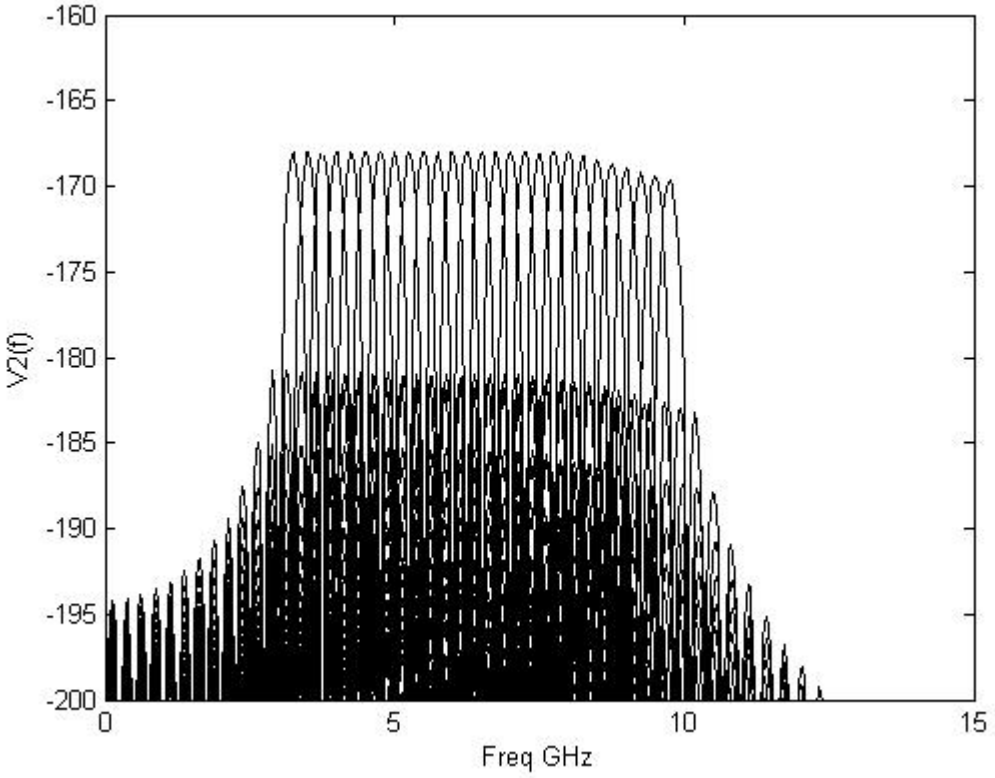

Figure 2: Overlaid output spectra for BW=500MHz

For 1 GHz bandwidth (with a step of 250 MHz) the generated UWB spectrums are shown in figure 3. In this case a maximum division ratio of 16 is assumed. The minimum VCO frequency is 3.5 GHz, the maximum 9.5 GHz.

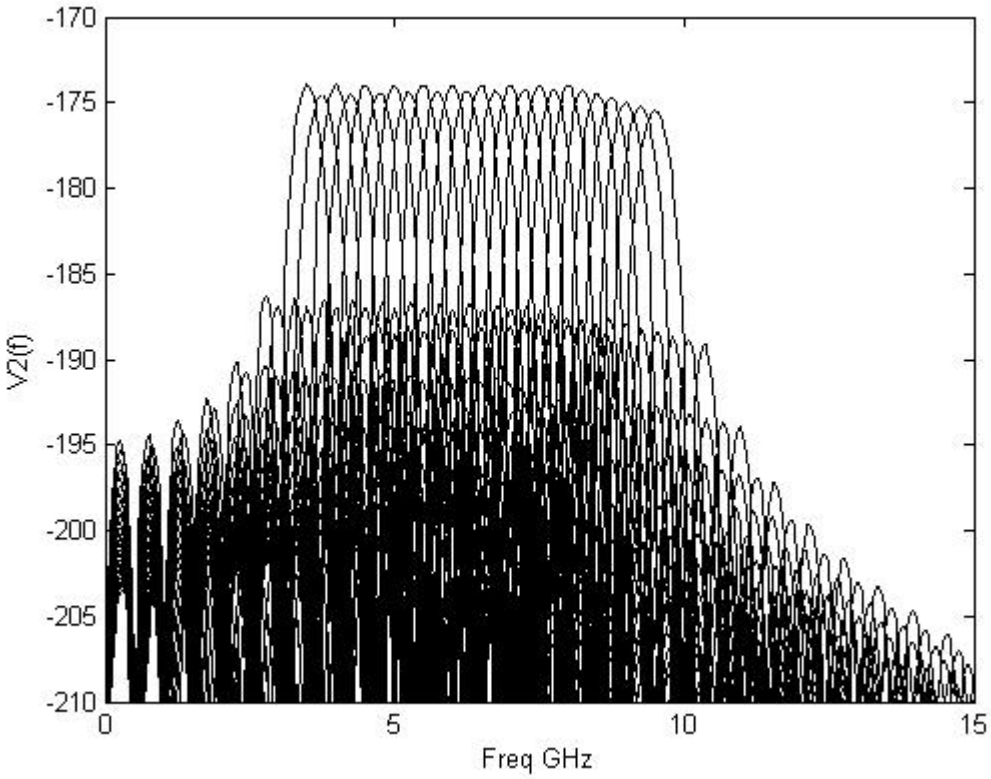

Figure 3: Overlaid output spectra for BW=1GHz

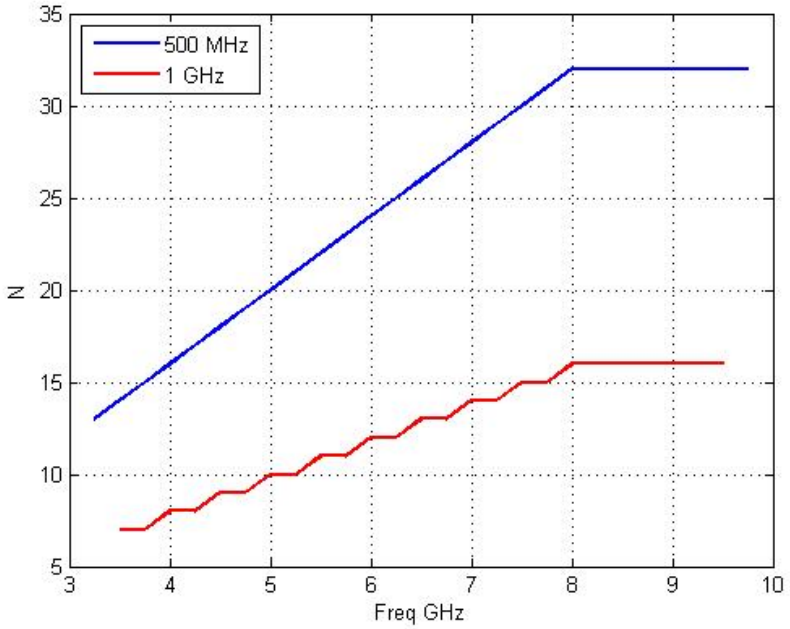

Figure 4: Required division ratio

Figure 4 shows the division ratio required in the two cases as a function of the VCO frequency. The division ratio is limited at 16 for 1GHz UWB and 32 for 500 MHz UWB.

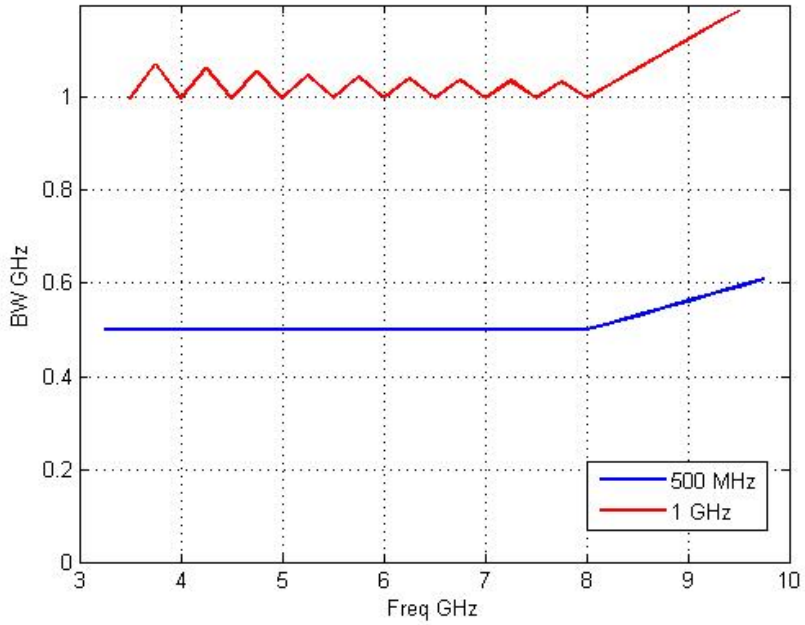

Figure 5: Bandwidth as a function of carrier frequency for a fixed divider architecture

Figure 5 shows signal bandwidth as a function of the oscillator frequency and for the optimal division ratio up to 16 and 32.

Voltage Controlled Oscillator

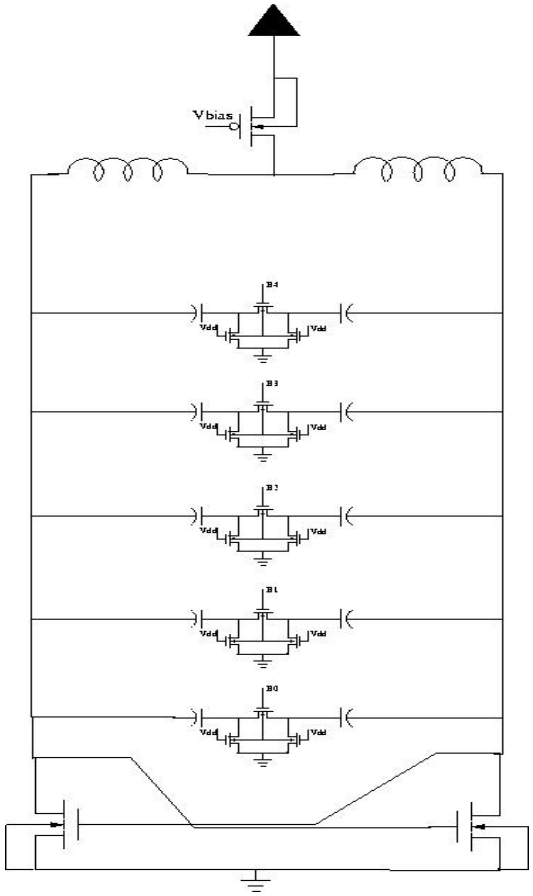

Figure 6: LC Oscillator Schematic

The voltage controlled oscillator uses an NMOS only LC topology to minimize parasitics (Fig.5). The main challenge is to guarantee wide tuning range (1:3) without degrading the inductor quality factor. Notice that this last limitation is actually a conservative assumption, stemming from the fact that we did not evaluate the effect of finite resonator Q on UWB link performance. Evaluating this effect is the subject of future work.

Oscillator tuning is achieved through a 5-bit binary weighted switched MIM capacitor array. Following the design methodology described in [3], we come to the conclusion that in order to meet the range and quality factor specifications in the presence of 100fF parasitics capacitance and 500pH inductance, a Con/Coff ratio of 12:1 is needed. This value can be achieved by using differential switching [3] and a 1.1V operating supply.

The inductance value determines the power dissipation of the VCO at each center frequency. Since the frequency range is 3:1, the power dissipation also varies by an approximate factor of 3. An optimal bias can be chosen in a feedforward fashion controlling a binary weighted 2-bits bias DAC. The bias current varies between 1 and 3 mA.

In order to match our spectrum model closely, the startup time of the oscillator should be minimized and made as repeatable as possible. Notice that this time is composed of 2-

phases: a bias startup phase in which the biasing circuits are powered up and the oscillator achieves its correct operating point, so that the loop gain is grater than 1, and an oscillation startup phase. We separate the two phases by introducing a shunting switch across the tank, which is released only after phase 1 is complete. In this way, no oscillation is generated during bias startup and any variability in the duration of phase 1 is removed. Ensuring a stable and short oscillation startup remains a major problem. We kick the oscillator symmetrically using a pair of small devices, reducing both the startup time and the uncertainty on the initial oscillator phase.

Power Amplifier/Antenna Driver

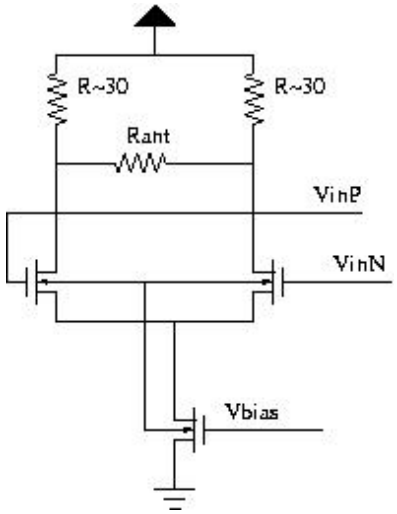

Figure 7: Power Amplifier /Antenna Driver

In order to power match into the antenna 50 resistance, we use a simple power amplifier based on a differential pair (Fig.7). The PA is loaded with polysilicon resistors to minimize parasitics. In order to ensure a 250mV voltage swing on the antenna, a bias current of 10 mA is required.

The PA is turned on and off using the same mechanism used for the VCO. The global chip temporization is shown in figure 8.

Bias-turn on is simulated to be 3ns, and constitutes 75% of the total chip active time. Further optimization is required to reduce this value. Also, this metric improves with technology scaling. At 10MP/s, considering a 4/100=4% duty cycling the 15mA peak chip power translates into a 600μW average power dissipation, or an energy of 60pJ/Pulse.

Divider Architecture

The proposed frequency divider is realized with a TSPC divider by two prescaler [1] followed by a CMOS programmable counter [2].
Two programmable counters have been designed in the range 2-8 (3 bits) or 3-16 (4 bits), depending on the desired UWB bandwidth.
If not differently specified, the simulations have been performed on post layout RCMax extracted.

TSPC divider

The schematic of the TSPC divider by two is shown in figure 8. The width (in um) of the transistor is indicated while the length is minimum for all.

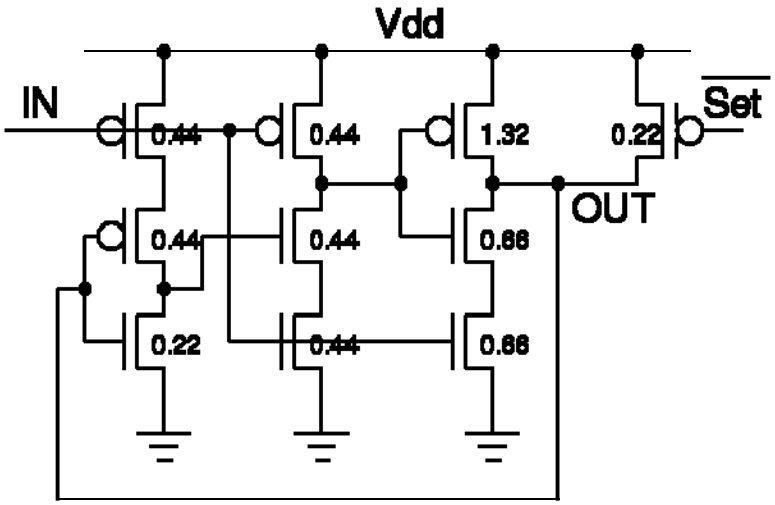

Figure 8: TSPC prescaler

The TSPC divider by two achieves a maximum operating frequency (PLS) of 11 GHz in TT at 27C and 8 GHz in SS at 80C. The power consumption is 140 and 105 uA respectively, including a BFSVTX2 output buffer and a 5fF load capacitance.
In the FF corner at 27C, 15 GHz maximum frequency is reached.
Operation in cross corners (SF and FS at 80C) has been proved up to 8 GHz

Simulations have been performed driving the input with an IVSVTX4 (driven by a rail-to-rail sine wave).

A PMOS has been added to preset the output at high level during the “non operating” interval. Since the following stage is sensible to the rising edge, the behavior of the system depends on the logic value of the TSPC output at the beginning of the counting phase.

Programmable divider

The programmable divider is realized in an asynchronous fashion (ripple carry counter), so to achieve the minimum logic depth in the feedback loop (that is zero gate in case of an inverting FF). Each FF is connected as a divider by two, and a proper network provide the needed programmability by means of the asynchronous input Set and Reset in the chained FF. The programmable divider is shown in figure 9, while the control network in Figure 10.

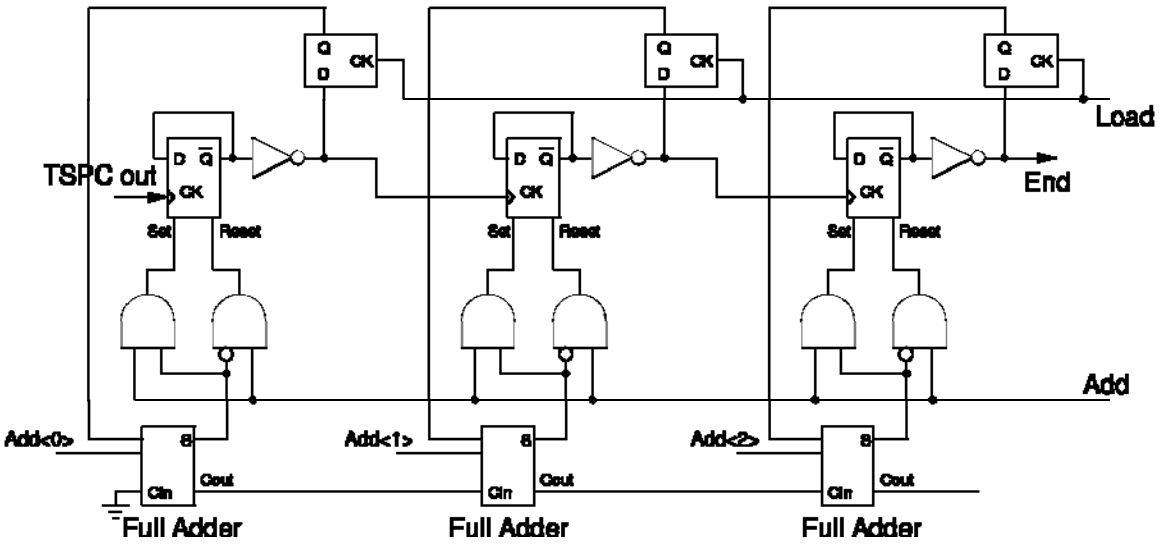

Figure 9: Programmable Divider

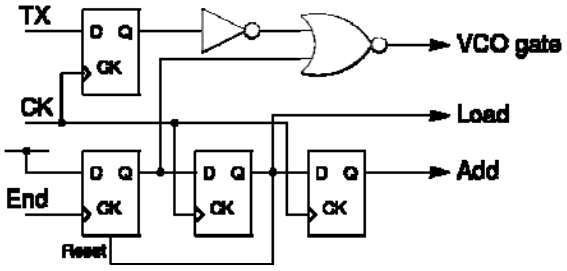

Figure 10: Control Logic

An external low frequency clock is required. This can be inaccurate and at almost any frequency that is at least 3 times the pulse rate. The TX signal is synchronized with this clock.

Because of the topology of the counter, that need to be “reloaded” at the end of the counting phase, an estimation of the energy for division cycle will be provided instead of the current consumption (integrating the current over a 20 ns window). Note that for a given modulus the number of transition is the same, and therefore even the required energy. The “current” is calculated by dividing the energy by the output period.

Also the minimum counting base if a function of the number of FF (3 or 4) and of the input frequency (and it tends to increases as the frequency increases because of the higher FF delay relatively to the clock period).

3 bit counter.
Frequency = 5 GHz, TT at 27C, mod = 16 Energy = 850 fJ (I = 265 uA)
Frequency = 5 GHz, TT at 27C, mod = 3 Energy = 600 fJ (I = 1 mA)
Frequency = 1.5 GHz, TT at 27C, mod = 16 Energy = 738 fJ (I = 69 uA)
Frequency = 1.5 GHz, TT at 27C, mod = 2 Energy = 550 fJ (I = 41 u)

In SS corner at 80C the maximum operating frequency is about 3.7 GHz.
Similar results are obtained for the 4 bit counter.
After many layout modifications I was not able to make it runs over 3.7 GHz in the SS corner at 80C.

Divider Overall Simulations

Post Layout simulations of the whole divider (by 2x8) have been performed. The critical part is the interface between the TSPC prescaler and the CMOP divider, even if a BFSVTX2 has been used. Probably a bigger design effort is required in the sizing of the TSPC and the CMOS interface (TSPC version 2). With SS corners and parasitic capacitances, problems arise because the first cycle of the TSPC is lost by the programmable divider. Another critical part is, as expected, the first FF of the programmable divider that gets an input frequency up to 5 GHz.

In TT corner at 27C (PLS) the frequency divider can operated with an input frequency up to 10 GHz (dividing by 2x8).

In SS corner at 80C (PLS) the maximum frequency (dividing by 2x8) is 7.4 GHz. The schematic works but after many manipulation of the layout is seems to be impossible make it working over 7.4 GHz in the SS corner at 80C.

Operation up to 10GHz has been verified in SF and FS corners at 27C.

Operation at 3 GHz (dividing by 1x2) for the FF corner at 0C results in an erroneous division ratio (+1). This holds because the programmable counter delay is lower than 1 TSCP output period. Alternatively, the scheme can be changed ant this results in a -1 in the pulse count.

Figure 8 shows the divider waveforms at 10 GHz input frequency and a division ratio of 16, while figure 9 the waveforms at 3 GHz input frequency divided by 2 (note that actually the output is given by 3 pulses). This problem does not appear for frequency higher than 5 GHz.

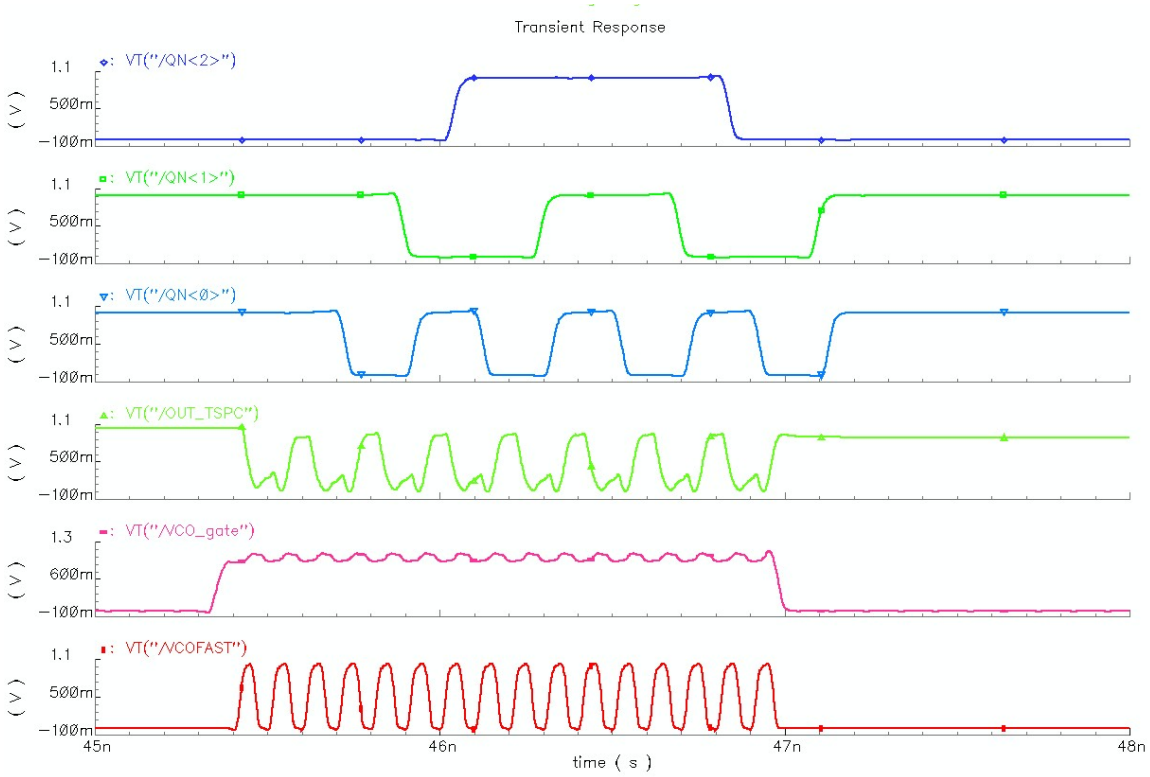

Figure 11: Divider Waveforms for div 16 at 10 GHz

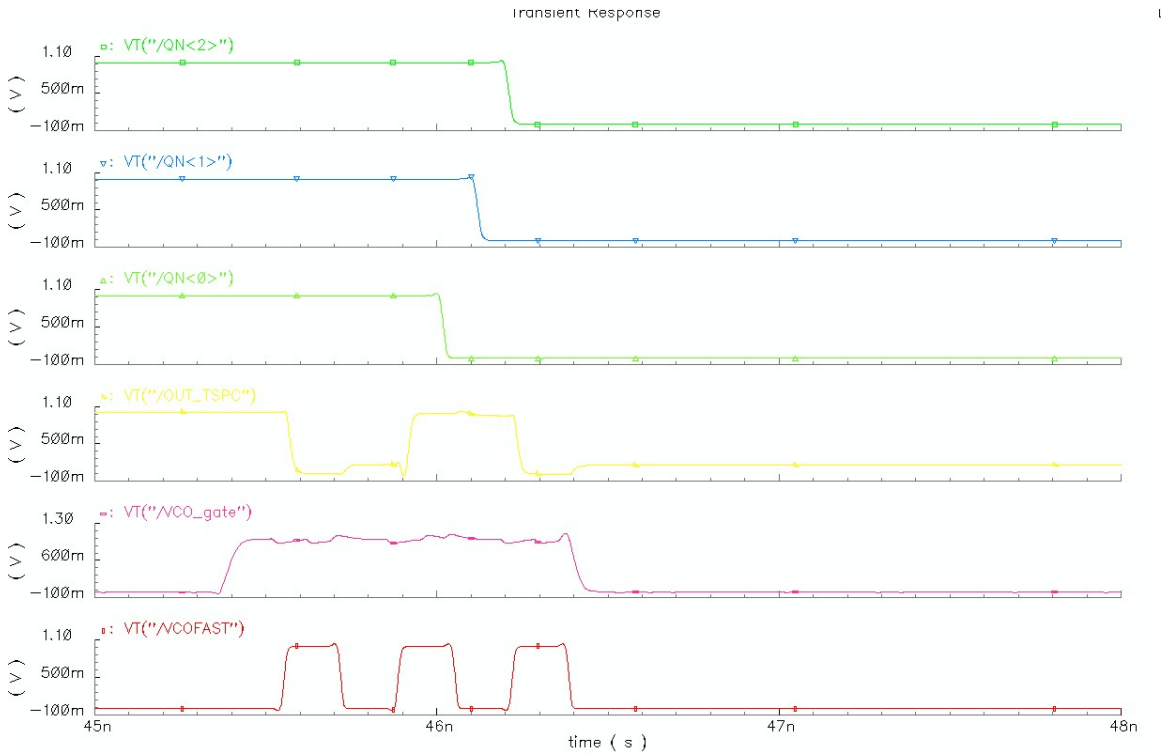

Figure 12: Divider waveforms for div 2 at 3 GHz (error occur)

Figure 13 shows the full custom layout of the TSPC divider including the buffer, while Figure 14 the layout of the programmable divider. The Set reset FF layout is full custom while the rest is based on standard cells, since it operates at lower frequency.

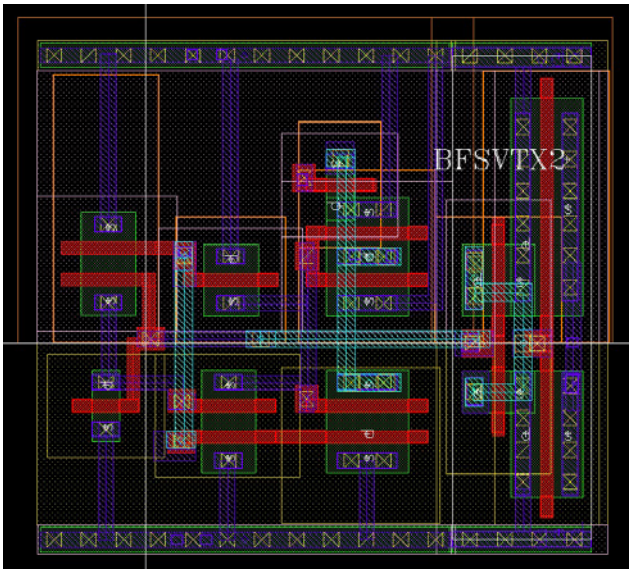

Figure 13: TSPC Layout

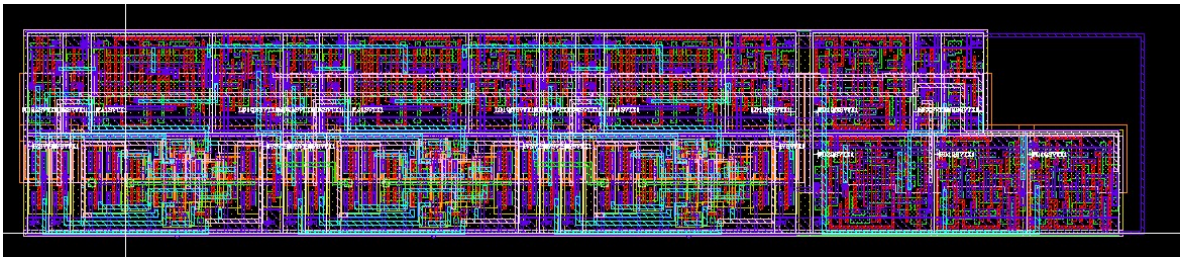

Figure 14: Programmable Divider Layout

References

[1] S. Pellerano, S. Levantino, C. Samori, and A. L. Lacaita, “A 13.5-mW 5-GHz Frequency Synthesizer With Dynamic-Logic Frequency Divider”, IEEE JSSC, Vol. 39, No. 2, Feb 2004, pp 378-383

[2] D. Guermandi, E. Franchi, A. Gnudi and G. Baccarani, “A CMOS programmable divider for RF multistandard frequency synthesizers”, Proc. of the 28th ESSCIRC, Firenze, Italy, Sep. 2002, pp. 843-846

[3] A. Berny, R.G. Meyer, A. Niknejad, “A 1.8Ghz VCO with 1.3GHz tuning range and digital amplitude calibration”, IEEE JSSC, Vol.40,No.4, April 2005