Advanced Pulse Width Modulation Controller ICs for Buck DC-DC Converters

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by

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Chair Date

Date

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University of California, Berkeley

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Abstract

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This dissertation develops power management ICs to tackle the challenges of both accurate and efficient power delivery for today's high performance processors. A double-edge multi-phase low-latency pulse width modulator IC is implemented in a 0.18 μm CMOS process with 0.04 mm^2 active area, and demonstrates a fast double-edge pulse width modulation scheme which is important for achieving fast controller response for high bandwidth applications. A multi-mode 4-phase digital IC controller for voltage regulator application is implemented in a 0.18 μm CMOS process with 4 mm^2 active area. The controller combines load current feedforward with voltage mode feedback to achieve fast transient response. A multi-mode control strategy improves the converter efficiency by at least a factor of ten in light load condition. A

load-scheduled integrator array is developed in the controller IC which improves the load transient response when the voltage regulator transitions between continuous conduction mode and discontinuous conduction mode.

Professor Seth R. Sanders
Dissertation Committee Chair

To my parents,

to my wife and my son

Acknowledgments

The past five years I spent in Berkeley are no doubt going to be the most memorable years of my life. I have been very fortunate to be surrounded by inspiring professors and encouraging friends and colleagues who have continuously offered me support and encouragement. I thank, from my bottom of my heart, for their contributions to my professional and personal growth.

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Chapter 1

Introduction

1.1 Motivation

Design of power management circuitry for today's complex ICs is getting significantly more difficult for each new CMOS technology node. As CMOS technology keeps scaling down, supply voltages have dropped while chip power consumption either remains constant or even increases, causing chip currents to increase. More severely, as aggressive clocking schemes are applied to enable different power saving modes, the slew rate of the supply current grows dramatically. The decreasing processor voltages also requires tighter voltage tolerances. The combination of tighter voltage regulation and higher current forces a very low power supply impedance. Achieving this low impedance in conjunction with the fast changing supply current can be extremely challenging.

High efficiency power delivery over a wide load range also presents challenges to voltage regulator (VR) design. For application such as server designs, the power supply density has reached limits due to the cooling bottleneck [1]. Here, high efficiency power delivery enables higher power supply density. For applications in portable devices, the load current in active mode or standby mode varies over a wide range. Thus, high efficiency over a wide load range is of high priority for power management in portable devices, as total energy is limited by the capacity of the battery.

An important trend for today's power management circuity is for more system power management functionality required besides the power regulation function [2]. There is a growing need to monitor the output power and currents, to provide dynamic

voltage adjustment [1], to enable intelligent fault management, power sequencing and tracking, communication with a host system, and more.

This dissertation develops power management ICs to tackle a number of the challenges outlined above. A double-edge multi-phase low-latency pulse width modulator IC is implemented in 0.18 μm CMOS process with 0.04 mm^2 active area and demonstrates a fast double-edge pulse width modulation scheme which is important for achieving fast controller response for high bandwidth applications. A multi-mode 4-phase digital IC controller for VR application is implemented in a 0.18 μm CMOS process with 0.5 mm^2 active area. The controller combines load current feedforward with voltage mode feedback to achieve fast transient response, and a multi-mode control strategy improves the converter efficiency by at least a factor of ten in light load condition. A microcontroller is embedded into the IC controller, enabling advanced power management functions such as communication with a host system, programmability without a change in hardware, system monitoring and sophisticated calibration functions.

1.2 Research Contributions

The main contributions of this research work is summarized below:

1. A new double-edge multi-phase low-latency pulse width modulator IC is developed. A fast double-edge pulse width modulation scheme is demonstrated in a prototype IC in 0.18 μm CMOS process. The fast transient response, good re-

configurability, good linearity and noise immunity, low power and low cost make it an attractive pulse width modulator candidate for integrated power management ICs of high bandwidth applications such as those arising in applications like microprocessor voltage regulator modules (VRM) or dynamic power supplies for RF power amplifiers.

2. A multi-mode 4-phase digital IC controller for VR application is developed. The proposed controller architecture partitions the system into the power regulation domain and the power management domain. The power regulation subsystem combines load current feedforward control with a load-scheduled digital PID feedback compensator to enable fast and glitch-free large-signal transient response. A load-scheduled digital integrator scheme is implemented in the controller IC, aiming to improve the transient response when the VR transitions to and from discontinuous conduction mode. The multi-mode operation improves the converter efficiency by at least a factor of ten in light load condition. The power management subsystem performs advanced power control and management tasks, such as communicating with the host system, updating control parameters, monitoring system variables such as load current and output voltage, dynamic adjusting reference voltage, etc.

3. Dedicated analog and digital interface modules, particularly suited for VR applications, are developed. A 13-bit subnanosecond resolution digital pulse width modulation (DPWM) module is developed. Critical timing synchronization issues is discussed in Chapter 4. A 4 mV resolution ring oscillator based ADC enables tight

DC regulation.

1.3 Thesis Overview

An overview of the contents is given here. In Chapter 2, we review the conventional single edge and double edge pulse width modulators and discuss the associated latency of the modulation process. A ring oscillator based double-edge pulse width modulation (PWM) scheme is introduced. The small signal model is derived and latency of the modulator is analyzed. The circuit implementation of the ring oscillator based pulse width modulator is presented. Experimental results obtained with the prototype IC demonstrate the developed ring oscillator based double-edge PWM modulator has fast transient response, good re-configurability, good linearity and noise immunity, low power and low cost.

In Chapter 3, the architecture of the multi-mode multi-phase IC controller for VR application is presented. The digital controller, based on the functionality, can be partitioned into power regulation and power management domains. The power regulation subsystem implements the voltage regulation function, providing tight DC regulation and fast load transient response. The power management subsystem performs advanced power control and management tasks, such as optimizing converter efficiency, communicating with the host system, updating control parameters, monitoring system variables such as load current and output voltage and providing fault protection and recovery, etc. The IC controller combines load current feedforward

with a digital PID feedback control to achieve a fast load transient response. A multi-mode control strategy is applied in the designed controller IC, allowing high efficiency operation of voltage regulator over a wide load range. A load-scheduled feedback control scheme is proposed to achieve fast transient response when VR runs in discontinuous conduction mode. A new soft start scheme is proposed to achieve a smooth regulator start-up process.

The circuit implementations of a ring oscillator based ADC and a high resolution DPWM are discussed in Chapter 4. Timing synchronization issues are discussed in order to achieve subnanosecond DPWM resolution.

A prototype IC is built with 0.18 μm standard CMOS process. A fast and glitch-free large-signal transient response is achieved by combining load current feedforward control and load-scheduled digital PID feedback control. The multi-mode operation improves the converter efficiency by at least a factor of ten in light load condition. More details on the experimental set-up and test results are presented in Chapter 5.

Chapter 2

Double-Edge Multi-Phase Low-Latency Pulse Width Modulator

2.1 Introduction

A multi-phase double-edge pulse-width modulation (PWM) scheme with low latency is important for achieving fast controller response for high bandwidth applications, such as those arising in applications like microprocessor voltage regulator modules (VRM) [3] or dynamic power supplies for RF power amplifiers [4].

Although, the required functionality might be realized with a conventional ramp-comparator modulator, such a modulator imposes a maximum duty cycle of 1/N, where N is the number of phases. Another embodiment of the conventional ramp-comparator modulator to realize multi-phase operation without the duty cycle constraint requires N comparators and N uniformly skewed ramp signals.

The modulator described in this chapter realizes all the desired features in a single simple circuit cell. The PWM signal is generated by comparing the phase difference between two matched ring oscillators, each of which functions as a current-controlled oscillator. These two matched oscillators are fed by the currents developed in a differential input stage. This balanced input stage is driven by the command voltage waveform, and a feedback voltage developed in a minor loop that forces the average frequency of each of the current-controlled ring oscillators to be equal. The minor loop constrains the duty ratio of the PWM signal to be proportional to the input modulation voltage over the full bandwidth of the minor loop. Both rising and falling edges of the PWM signal are controlled by the instantaneous input voltage, resulting in a low latency relative to that achieved with conventional latched PWM circuitry.

The developed pulse width modulator has high precision, good linearity, good noise immunity and wide duty ratio range. Further, it can be flexibly reconfigured for multi-phase PWM operation with no restriction on duty cycle range.

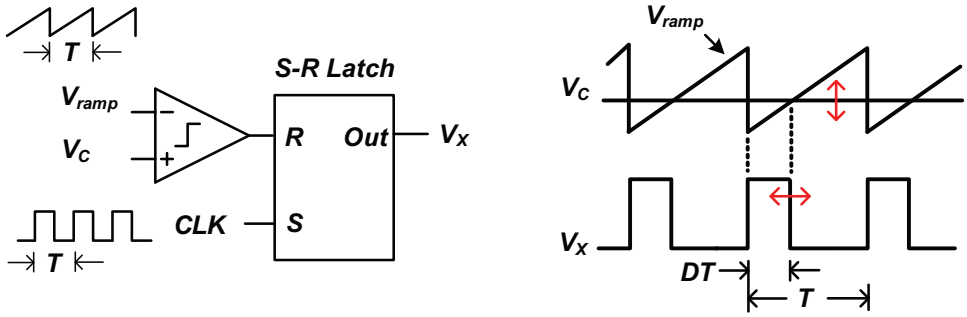
In Section 2.2 we review the conventional single-edge and double-edge pulse-width modulators and discuss the associated latency of the modulation process. Section 2.3 introduces the ring-oscillator-based pulse-width modulator, derives the small signal model, analyzes the latency of the modulator. Section 2.4 gives the circuit implementation of the proposed ring-oscillator-based pulse-width modulator. Section 2.5 shows the experimental results of the prototype IC of the developed ring-oscillator-based pulse-width modulator.

2.2 Overview of Conventional Pulse Width Modulator

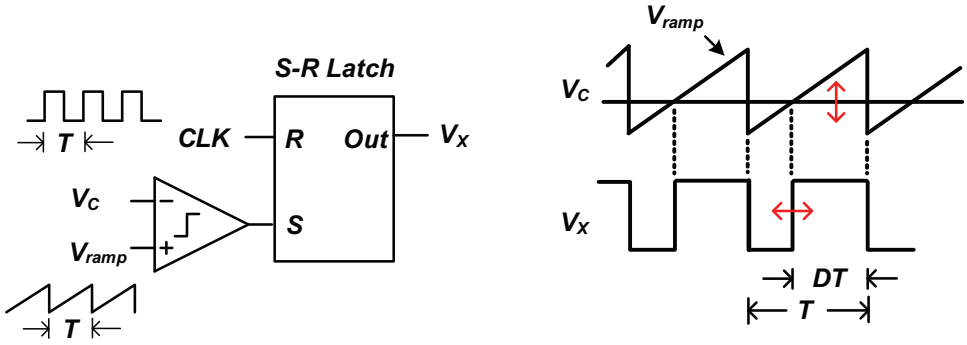
2.2.1 Single-Edge Pulse-Width Modulator

A conventional pulse-width modulator modulates the pulse width of the switch function by comparing an analog modulation signal to a sawtooth signal. A set-reset latch is typically applied to prevent multiple transitions per switching period. Pulse width modulation can be performed on the leading-edge and trailing-edge of the output pulse, termed leading-edge and trailing-edge modulation respectively.

In a trailing-edge pulse width modulator, as illustrated in Fig. 2.1(a), a clock



(a)



(b)

Figure 2.1: Conventional pulse width modulators and switching waveforms (a)Trailing edge PWM modulator (b)Leading edge PWM modulator

signal is used to set the latch and a comparator to reset the latch. The output pulse is set to one at the beginning of the switching period and reset to zero once the ramp voltage V_{ramp} is greater than the modulation voltage V_C . The output pulse stays at zero until the start of the next switching cycle. Therefore, only one control action can be taken every switching cycle, at the trailing edge of the output pulse. The set and reset operations for a leading-edge pulse-width modulator, and the resulting switching waveforms are illustrated in Fig. 2.1(b).

This set-reset latch scheme creates fundamental large signal delay in the pulse width modulator. As illustrated in Fig. 2.2(a), the turn-on delay as illustrated in for trailing-edge modulator is defined between the time of the input transient and the response of the modulator. The modulator is opaque to any control voltage transient happening after the falling edge of the output pulse until the start of the next switching cycle. The turn-off delay for a leading-edge modulator as illustrated in Fig. 2.2(a) is defined in the similar way.

The maximum large signal delay associated with the single-edge pulse-width modulation process can be expressed as

$$t_{turn-on} = (1 - D)T_s \tag{2.1}$$

for the trailing-edge modulator, and

$$t_{turn-off} = DT_s \tag{2.2}$$

for the leading-edge modulator, where T_s is the switching period, D is the steady

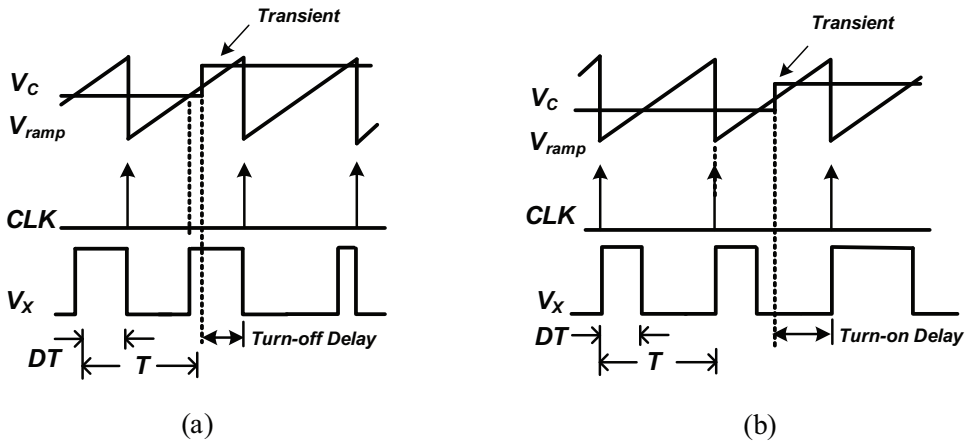


Figure 2.2: Large signal delay of single edge PWM modulator (a)Turn-off delay for leading-edge modulator (b)Turn-on delay for trailing-edge modulator

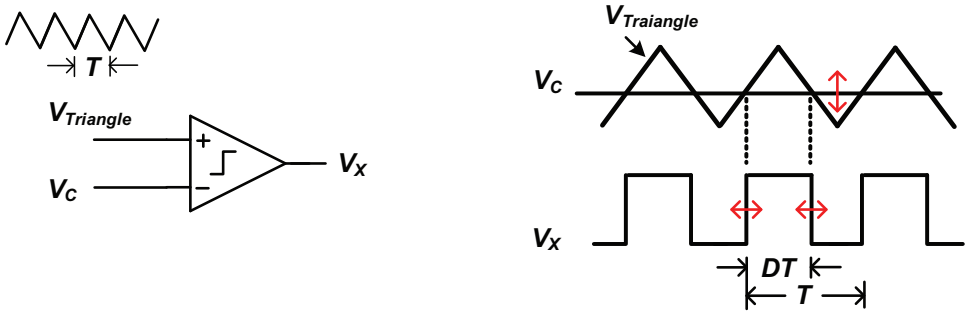


Figure 2.3: Double edge pulse width modulator and switching waveforms

state duty cycle.

2.2.2 Double-Edge Pulse-Width Modulator

Double-edge pulse-width modulator has the pulse-width modulation process performed on both edges of the output pulse. Both rising and falling edges of the PWM signal are generated by comparing the modulation voltage to a triangle signal as shown in Fig. 2.3.

Comparing to the single-edge pulse-width modulator, control actions are taken on both edges of the output pulse every switching cycle. Therefore, the large signal delay issue related with the set-reset latch scheme is resolved.

2.3 Ring-Oscillator-Based Pulse-Width Modulator

2.3.1 Theory of Operation

A simplified schematic of the proposed ring-oscillator-based pulse-width modulator is shown in Fig. 2.4(a). A matched pair Mp1 - Mp2 drives two identical ring oscillators as a matched load. As illustrated in Fig. 2.4(b), the phase difference of the two oscillators is detected by a phase detector, the output of which is used as the PWM signal. This phase-sensitive signal is then passed through a low pass filter (LPF), aimed at removing ripple, with the resulting signal V_{FB} applied to the differential pair in an internal feedback loop. In steady state, the voltage V_{FB} which is proportional to the duty cycle, is forced to be equal to the command voltage V_C by the minor feedback loop. When the command modulation voltage V_C increases, the error voltage between V_C and V_{FB} develops differential current in the two ring oscillators that results in instantaneous differential frequency and phase shift as shown in Fig. 2.4(c). The resulting phase difference of the two ring oscillators will be increased until the signals V_C and V_{FB} are equal. When the command modulation voltage V_C decreases, as shown in Fig. 2.4(d), the phase difference of the two ring oscillators

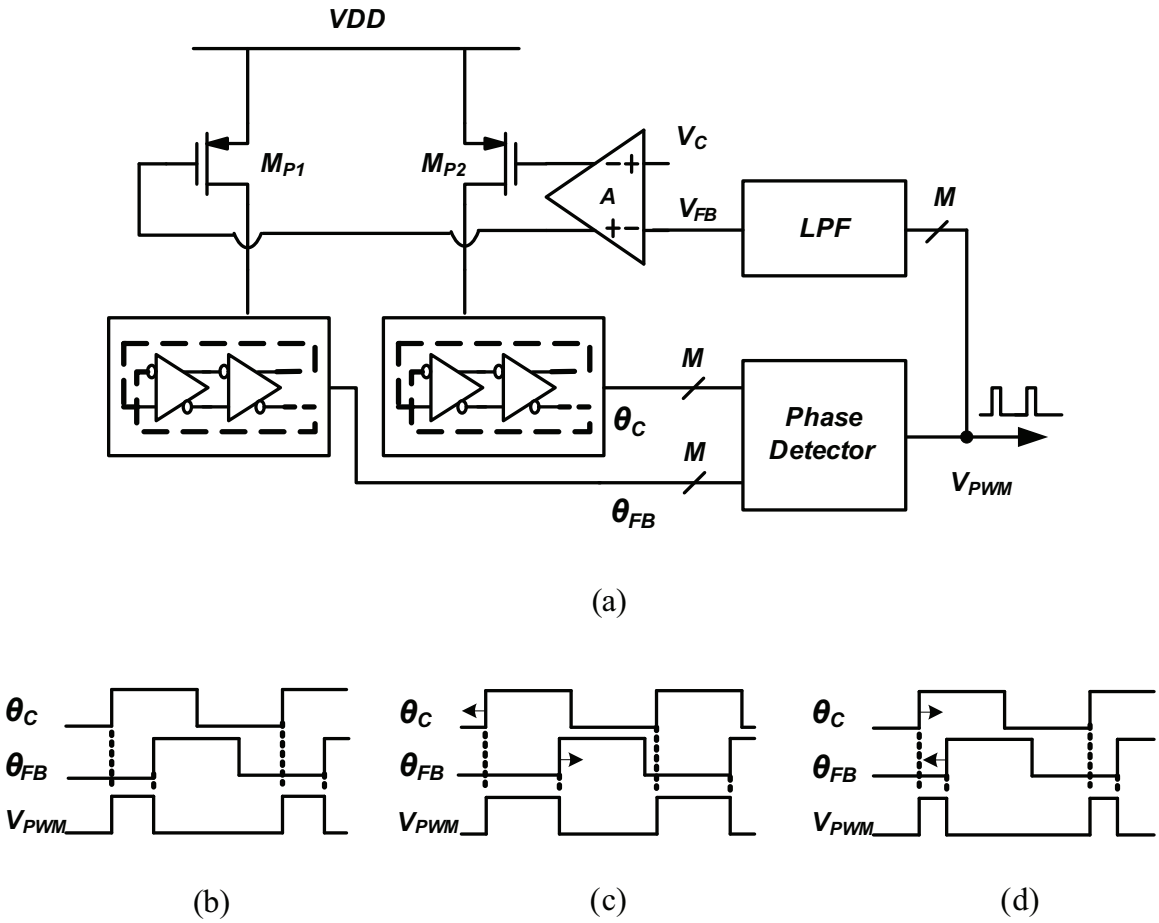


Figure 2.4: (a)Simplified schematic of ring oscillator based pulse width modulator (b)Steady state switching waveform (c)Switching waveforms as input control voltage increases (d)Switching waveforms as input control voltage decreases

will be decreased until the voltages V_C and V_{FB} are equal. As both edges of the output PWM signal are modulated by the input command voltage V_C, the behavior of this ring-oscillator-based pulse-width modulator is similar to a double-edge PWM modulator.

The phase difference of the two ring oscillators is actually equal to the time integral of the differences of the two ring oscillator frequencies, which is proportional to the

error voltage. Therefore, integration inherently takes place in the loop and any high frequency noise or glitch at the input is filtered, suppressing false transitions. Instead of comparing the phase difference once per switching period, M uniformly spaced taps on each respective ring oscillator are compared in a multi-phase phase detector, reducing latency and increasing ripple frequency. Further, uniformly spaced multi-phase PWM signals are available from the multi-phase phase detector. A multi-input low pass filter is applied to suppress ripple in the minor loop. The detailed circuit implementation will be described in Section 2.4.

2.3.2 Linear Model and Loop Analysis

Ignoring the nonlinearity of the input differential pair and phase comparator, a linear model representing the ring oscillator based pulse width modulator is shown in Fig. 2.5, which consists of the input differential pair with transconductance G_m, the phase comparator, the low pass filter (LPF), the buffer with voltage swing of V_{DD} to drive the low pass filter, and the current-starved ring oscillator. The phase comparator can be modeled as a gain term K_{PD} as the high frequency components are suppressed by the low pass filter [5]. Under the steady state, two ring oscillators have the same bias current I_{bias} and oscillation frequency ω_{osc}. When the ring oscillator runs in current-starved mode with transistors operating in subthreshold region, the oscillation frequency ω_{osc} has a highly linear dependency on the bias current I_{bias} [See

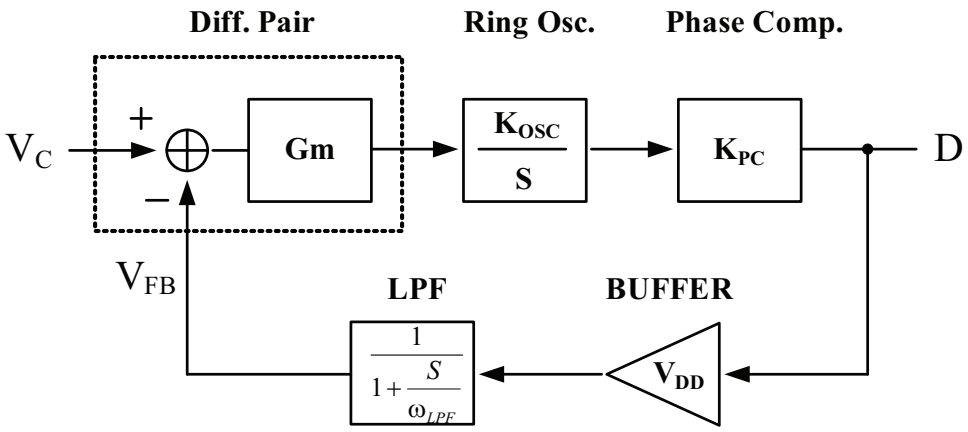


Figure 2.5: Block diagram of the ring oscillator based pulse width modulator

Chapter 4], which satisfies

$$\omega_{OSC} = K_{OSC} I_{bias} + \omega_0 \tag{2.3}$$

where K_{OSC} is the current-frequency gain of the ring oscillator and ω_0 is a constant offset.

The phase of the ring oscillator output ϕ_{osc} is equal to the time integral of the oscillator frequency

$$\phi_{osc}(t) = \phi_{osc}\,|_{t=0} + \int_0^t \omega(t)\,\mathrm{d}t \tag{2.4}$$

Thus the current starved ring oscillator can be modeled as an integrator $1/s$ with gain K_{OSC}. And, the closed-loop transfer function of the pulse width modulator is given by

$$\frac{D}{V_{PWM}} = \frac{K_{OSC} K_{PD} G_m (s + \omega_{LPF})}{s^2 + \omega_{LPF} s + K_{OSC} K_{PD} G_m V_{DD} \omega_{LPF}} \tag{2.5}$$

where D is the duty cycle of the pulse width modulator output, and ω_{LPF} is the $-3dB$ frequency of the low pass filter. Since there is one open-loop pole at the origin,

the loop gain goes to infinity as $s \rightarrow 0$. This ensures that the error voltage goes to zero in steady state and that the duty cycle of the modulator output is proportional to the input control voltage. In Equation 2.5, by making $s \rightarrow 0$, the duty cycle of the pulse width modulator output is given by

$$D = \frac{V_C}{V_{DD}} \tag{2.6}$$

Equation 2.5 can also be expressed as

$$\frac{D}{V_C} = \frac{\omega_n^2 + \frac{\omega_n}{2\zeta}s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2.7}$$

where

$$\omega_n = \sqrt{K_{OSC}K_{PD}G_m V_{DD}\omega_{LPF}} \tag{2.8}$$

and

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{OSC}G_m}} \tag{2.9}$$

It is a second-order feedback loop with two open-loop poles given by $p_1 = 0$ and $p_2 = \omega_{LP}$. The stability analysis is straight forward from the root locus plot in Fig. 2.6. As the loop gain further increases, the two poles become complex with real part equal to $-\omega_{LP}/2$ and move in parallel with the $j\omega$ axis. The loop gain, which is equal to $K_{OSC}K_{PD}G_m V_{DD}$, is designed such that the loop has large bandwidth for fast dynamic response and enough phase margin not to cause significant overshoot in step response.

The dynamic response of the modulator is analyzed by applying a voltage step

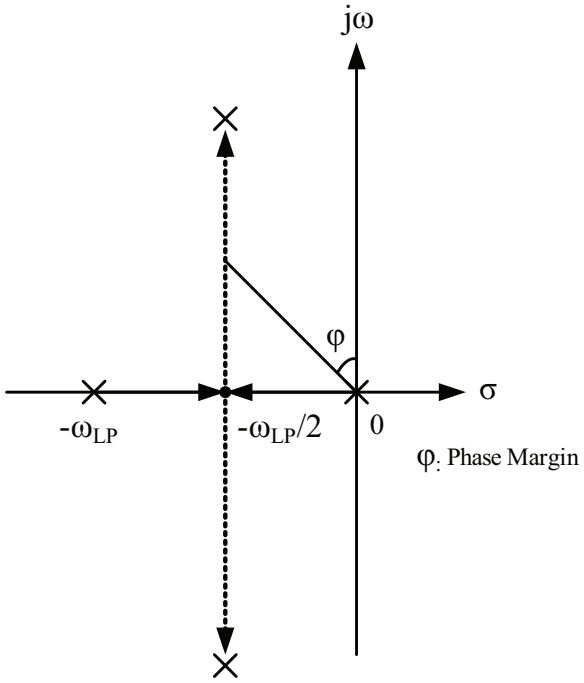


Figure 2.6: Root locus of the modulator inner feedback loop

$\Delta V_c u(t)$ at the input, the resulting modulator output duty-cycle is equal to

$$D = [1-\exp(-\zeta\omega_n t)[\frac{1}{\sqrt{1-\zeta^2}}\sin(\omega_n\sqrt{1-\zeta^2}t+\theta)+\frac{1}{2\zeta\sqrt{1-\zeta^2}}\sin(\omega_n\sqrt{1-\zeta^2}t)]\Delta V_c u(t) \tag{2.10}$$

where $\theta = \arcsin(\sqrt{1-\zeta^2})$. The step response of the duty cycle contains sinusoidal components which decay with a time constant of $\frac{1}{\zeta\omega_n}$. Combining Equation 2.8 and Equation 2.9 gives the time constant

$$\frac{1}{\zeta\omega_n} = \frac{1}{2}\omega_{LPF} \tag{2.11}$$

This time constant determines how fast the duty cycle output approaches its final

value. As an example, for duty cycle settling of 0.5% to its final value requires

$$e^{-\zeta\omega_n T_s} = e^{-\frac{1}{2}\omega_{LPF} T_s} < 0.005 \Rightarrow T_s \geq \frac{5.29\omega_{LPF}}{2} \tag{2.12}$$

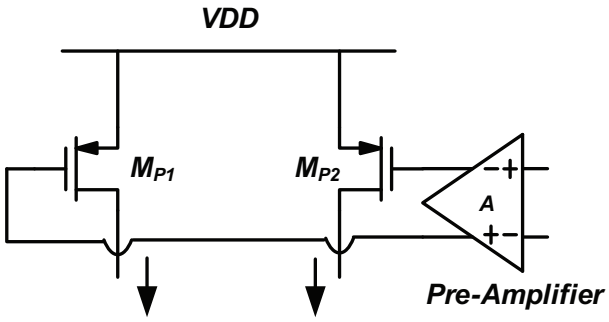
2.4 Circuit Implementation

2.4.1 Input Stage

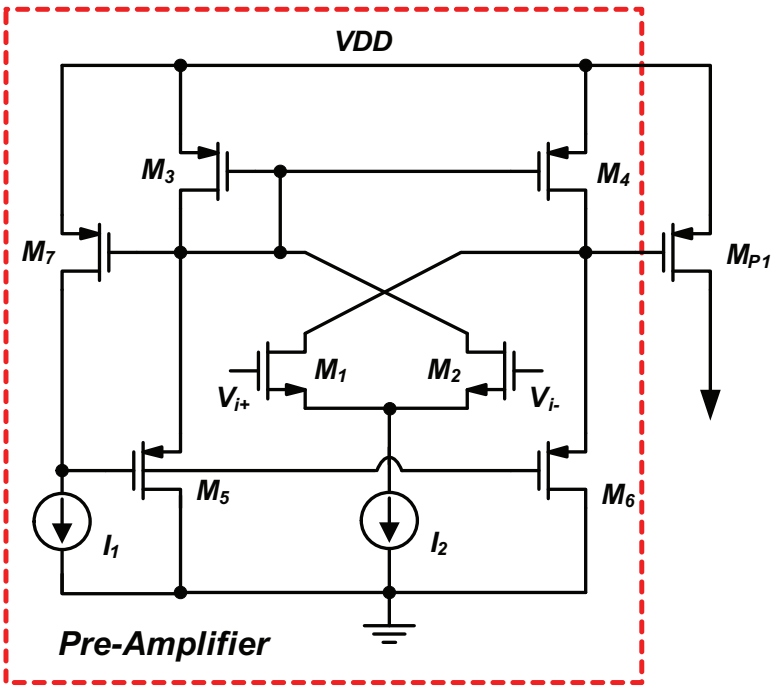
The input stage compares the voltage difference between V_C and V_{FB} and converts voltages into currents to bias the ring oscillators. There are several design considerations regarding the input stage of this ring oscillator based pulse width modulator. First, the input stage should not saturate with large differential voltage as saturation would significantly limit the large signal transient response of the modulator. Second, as shown in Equation 2.10, transconductance of the input stage should be large enough to achieve the desired loop bandwidth, and be well controlled to keep good phase margin. Finally, the quiescent current supplied to the ring oscillator must be well controlled as it determines the nominal ring oscillator frequency, which is the same as the PWM switching frequency.

Based on the above considerations, common-source transistor MP1 and MP2 together with a pre-amplifier [6] are used as the input stage and is shown in Fig. 2.7(a). The whole input stage is symmetric and Fig. 2.7(b) shows half of the circuit.

The error voltage at the input is sensed by differential pair M_1 and M_2, which is biased by the tail current source I_2. Common drain transistors M_5 and M_6 are in



(a)



(b)

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Figure 2.7: (a)Simplified schematic of the input stage. (b) Half circuit of pre-amplifier

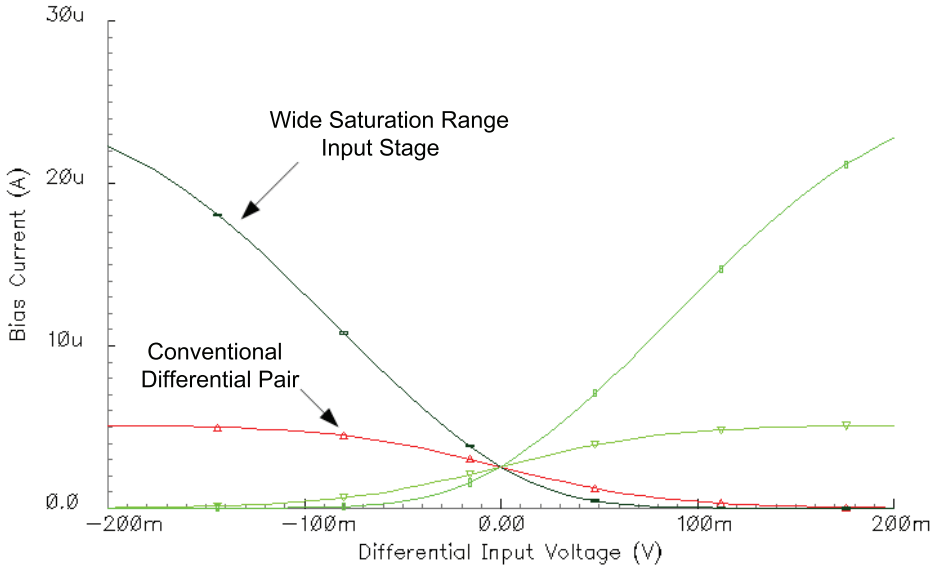


Figure 2.8: Simulated ring oscillator bias current versus differential input voltage: proposed input stage versus conventional differential pair

parallel with the current mirror load M_3 and M_4 to reduce the output resistance so that the gain of the error amplifier can be set to a well-defined value. The negative feedback loop, including transistors M_5, M_3, M_7 and current source I_1, adjusts the gate voltage of M_5 such that M_7 operates in the active region and conducts I_1. In steady state, the gate voltage of M_3 is equal to the drain voltage of M_4. Therefore, the quiescent bias current of M_{P1} can be expressed as

$$I_{D,MP1} = I_{D3}\frac{(W/L)_{MP1}}{(W/L)_3} = I_1\frac{(W/L)_7}{(W/L)_1} \tag{2.13}$$

The quiescent bias current supply to the ring oscillator is well controlled by bias current source I_1. This negative feedback loop also forces the small-signal resistance at the input of the current mirror M_3 and M_4 to approximately zero [7]. Therefore,

the transconductance of the error amplifier is

$$G_m = g_{m1} = g_{m2} \tag{2.14}$$

As the output resistance of the amplifier is set by the common-drain transistor M_6, ignoring the body effect, the gain of the pre-amplifier is

$$A = G_m R_{out} = \frac{g_{m1}}{g_{m6}} \tag{2.15}$$

And the overall transconductance of the input stage is

$$G_m = A g_{m,MP1} = \frac{g_{m1}}{g_{m6}} g_{m,MP1} \tag{2.16}$$

The simulated ring oscillator bias current versus differential input voltage is shown in Fig. 2.8, with the comparison of the proposed input stage proposed to a conventional differential pair. Compared to the conventional differential pair, this input stage provides a large relative constant transconductance over a wide range of differential input voltage, and quiescent bias current of M_{P1} can be precisely controlled by current source I_1.

2.4.2 Ring Oscillator and Level Shifter

A current starved differential ring oscillator similar to the design in [8] is used here for its small area and low power consumption. As shown in Fig. 2.9, the supply current to the ring oscillator is generated by the common source transistor M_{P1} from the input stage. The differential delay buffer in the ring oscillator is a pair of inverters

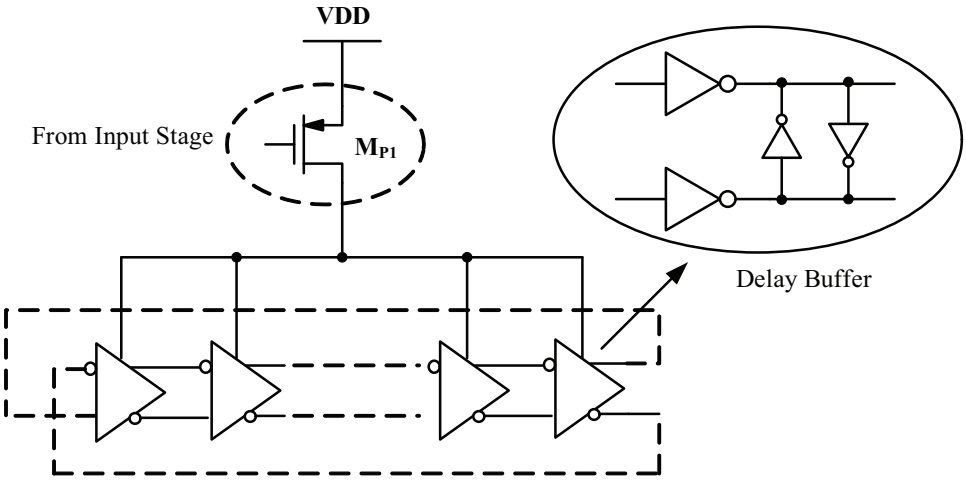
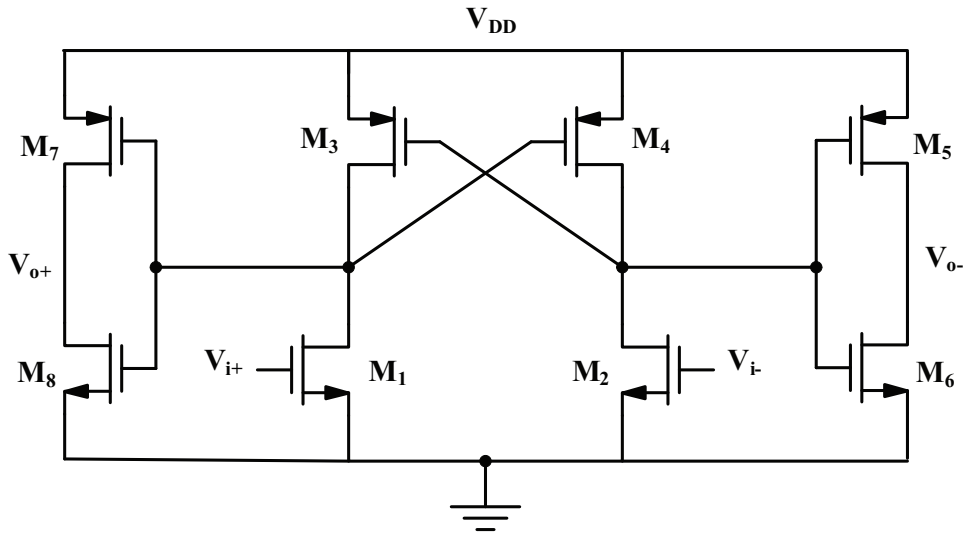


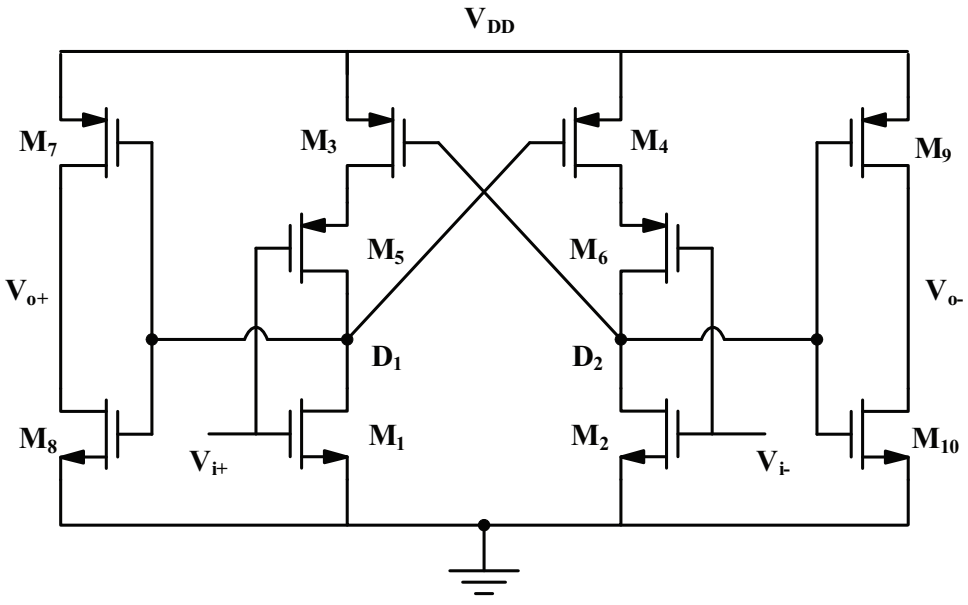
Figure 2.9: (a)Differential ring oscillator biased by the input stage (b)Delay buffer used in the ring oscillator

with outputs coupled by weak cross-coupled inverters, aiming at minimizing the delay skew between two paths. The voltage swing on the ring oscillator are below the thresholds of the MOSFETs, which gives the ring oscillator a good linear dependency of the oscillation frequency on the supply current [Chapter 4]. Level shifters are used to restore the low swing differential signals to full swing digital signals.

The conventional level shifter, as shown in Fig. 2.10(a), has been used in some ultra low power circuit [9] [10] that operates in subthreshold region. The two PMOS transistors M_3 and M_4 act as swing-restoring devices to pull the outputs to full voltage swing. There is a contention between the PMOS cross-coupled transistors and the NMOS pull-down devices M_1 and M_2. The NMOS devices have to be designed much larger than the PMOS transistos to pull down the output towards ground voltage level as the input voltage is below the threshold voltage. Still the contention between the PMOS and NMOS transistors still causes a large output transition time, delay



(a)



(b)

Figure 2.10: (a)Conventional level shifter (b)Fully differential contention mitigated level shifter

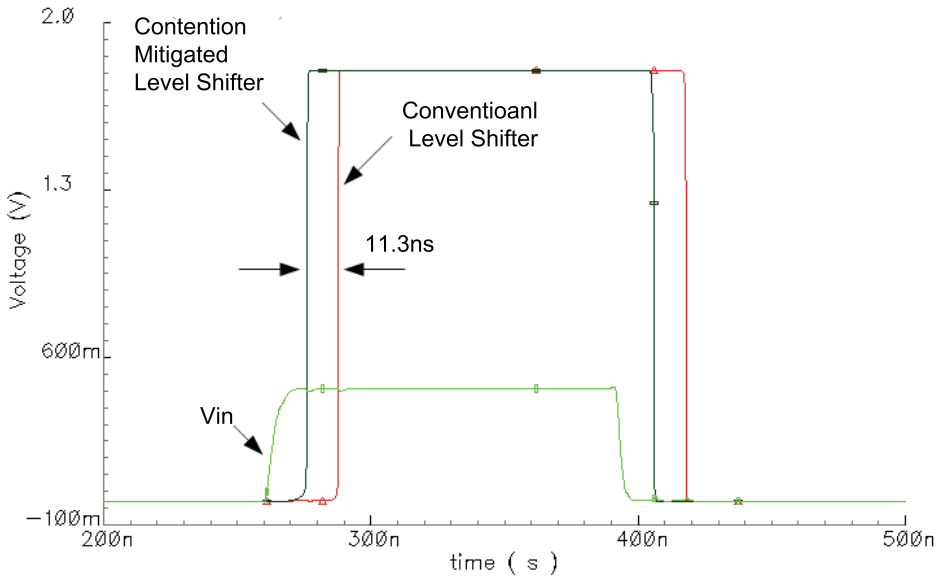


Figure 2.11: Simulated switching waveforms of two level shifters

and extra short-circuit power consumption. A single-ended contention mitigated level shifter has been proposed in [11], here we developed a fully differential level shifter to reduce the contention problem. As shown in Fig. 2.10(b), the PMOS transistors M_5 and M_6 helps the input NMOS pair to establish the voltage on node D_1 and D_2 faster than the conventional level shifter, which reduces the output delay and transition time of the level shifter. The size of transistors M_7 and M_8, M_9 and M_{10} are skewed in favor of output low to high transitions in order to match the rise and fall transition time of the level shifter output.

The delay and power reduction of the new level shifter are verified by the simulation. The ring oscillator runs at 4MHz with 470mV voltage swing, two level shifters

are used to restore the low swing signal back to full voltage swing. As shown in Fig. 2.11, a delay reduction of 11.3ns of the new level shifter over the conventional design is observed. The power consumption of this level shifter is also reduced compared to the conventional design since the time that both NMOS and PMOS devices are on is reduced. The simulation shows a power consumption of 0.21 $\mu A/MHz$ compared to $1.08\mu A/MHz$ for the conventional level shifter.

2.4.3 Phase Comparator

The phase comparator compares the phase difference of the two ring oscillators, and the PWM signal is taken from its output. The phase comparator is designed to have comparison range from 0 to 2π, linearly corresponding to 0 to 100% duty ratio. When the instantaneous phase difference exceeds the zero to 2π range, the duty cycle should ideally saturate to 0 or 100%, and the frequency of the two oscillators should keep lock to avoid wind-up. Therefore, the phase comparator should incorporate frequency detection in addition to phase detection. A phase frequency detector (PFD) used in [5] is shown in Fig. 2.12(a). As shown in Fig. 2.12(b), the phase difference has a linear relationship with the the low pass filter output which is proportional to the PWM duty cycle output. When the phase difference is equal to or exceeds zero to 2π range, the duty cycle is saturated to 0 or 100%.

The problem with this conventional phase frequency detector design is the frequency of the two oscillators will lose lock if the phase difference exceeds zero to 2π

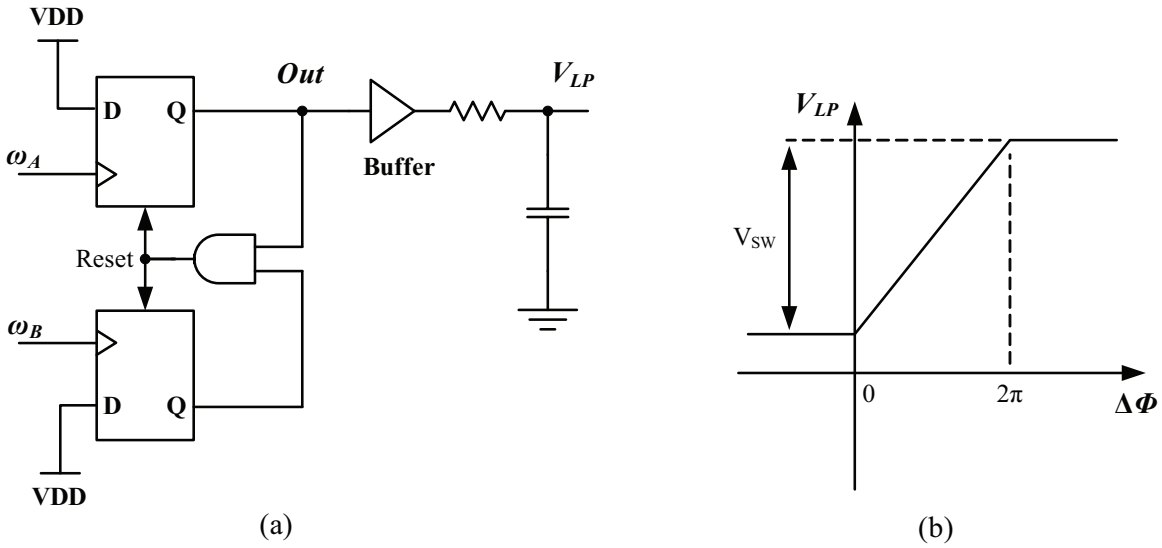
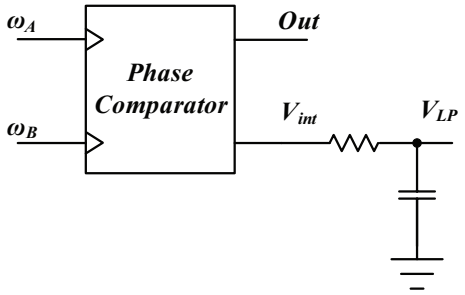


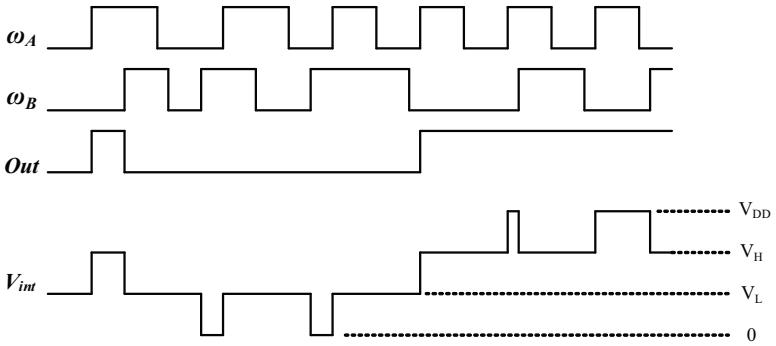
Figure 2.12: (a) Conventional phase frequency detector followed by low-pass filter (b) Output characteristic of the phase frequency detector

range, as more feedback voltage will have to be applied to the input differential pair in order for the oscillator phase to shift accordingly. However, the phase detector can produce no more dc output voltage to shift the oscillator frequency further as the duty ratio reaches 0 or 100%, so the loop will lose lock and become unstable.

To resolve this frequency tracking problem, a new phase and frequency detection scheme is developed as shown in Fig. 2.13(a). A phase-frequency comparator compares the phase and frequency difference of two ring oscillators, and the PWM signal is taken from the output. Instead of feeding back the DC component of the PWM signal, a four-level signal V_{int} as shown in Fig. 2.13(b) is developed from the phase comparator to close the internal feedback loop. When the phase difference Φ is within 0 to 2π range, V_{LP} swings between V_L and V_H, linearly corresponding to 0 to 100% duty ratio. When the phase difference becomes negative, i.e. $-2\pi < \Phi < 0$, V_{LP}



(a)



(b)

Figure 2.13: (a)Proposed phase frequency detector followed by low-pass filter (b)Switching waveforms of the proposed phase frequency detector

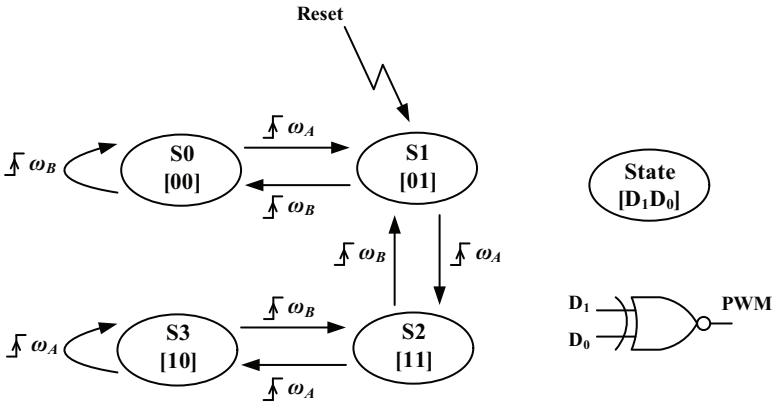


Figure 2.14: State transition diagram of the phase comparator and generation of PWM signal

swings between 0 and V_L, providing extra voltage to pull the phase difference of the two ring oscillators back to zero and keep the loop locked. An analogous case applies when phase difference exceeds 2π, i.e. $2\pi < \Phi < 4\pi$, V_{LP} swings between V_H and V_{DD}, providing extra voltage room on the feedback node to keep the loop in lock.

The proposed phase and frequency detection scheme is implemented by using a state machine with the state transition diagram shown in Fig. 2.14. State transitions happen only when the rising edge of either one of the frequency inputs is detected by the phase comparator. When the phase difference is within 0 to 2π range, transitions only happen between states S_1 and S_2. When the state machine receives two consecutive rising edges from either one of the frequency inputs, meaning the phase difference exceeds 0 to 2π range, the state machine will transition to saturation state, with S_0 and S_3 corresponding to the cases where phase difference is below 0 or exceeds 2π, respectively. The PWM signal is taken by combining the two bits of the state in a XNOR gate. A four-level buffer as shown in Fig. 2.15 is designed to generate four

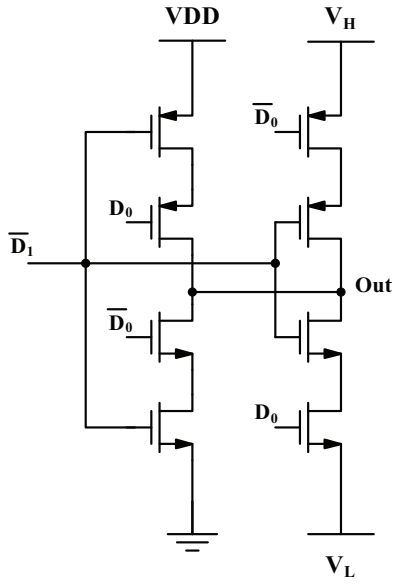


Figure 2.15: Schematic of four-level buffer

different voltage levels corresponding to four different states in the state machine.

Multiple phase frequency comparators and associated four-level buffers are used to compare all M taps from two ring oscillators to reduce the latency. And, a multi-input low pass filter is used to reduce the ripple voltage and increase the loop bandwidth, which will be discussed in Section 2.4.4.

2.4.4 Multi-input Low Pass Filter

The simplified schematic of the multi-input low pass filter is shown in Fig. 2.16. It combines all outputs of the multi-phase phase comparator. The transfer function of this multi-input low pass filter is given by

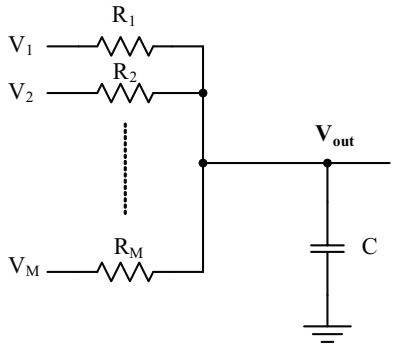


Figure 2.16: Simplified schematic of a multi-input low pass filter

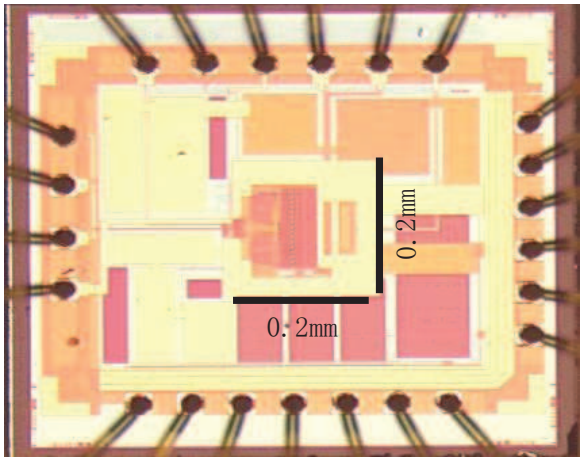


Figure 2.17: Chip micrograph.

$$H(s) = \frac{1}{1 + sRC/M} \tag{2.17}$$

From Equation 2.11, the settling time of the duty cycle is determined by the $-3dB$ frequency of the low pass filter, which is $\frac{M}{RC}$ for this multi-input low pass filter. Compared with a single-input RC low pass filter with a similar output voltage ripple, the $-3dB$ frequency and loop bandwidth are boosted up by M times.

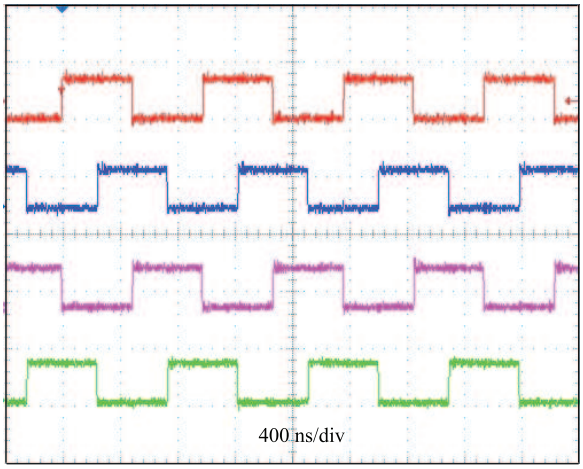


Figure 2.18: Four symmetric PWM output signals.

2.5 Experimental Results

The complete double-edge pulse width modulator IC is implemented in a 0.18 μm CMOS process. The die photo of the chip is shown in Fig. 2.17. The active chip area is 0.04 mm^2. It can generate as many as sixteen PWM outputs. Fig. 2.18 shows four of sixteen symmetric PWM output signals. The quiescent bias current of the chip is 80 μA at 1.2 MHz PWM frequency, and much higher PWM frequency is possible by increasing the bias current of the ring oscillator.

Fig. 2.19 shows the time domain response of the modulator to a triangle input voltage command V_{in} without duty ratio saturation. The functionality of the proposed phase comparator is verified by applying a large triangle voltage command V_{in} at the input and forcing the duty ratio of the PWM signal to saturate to zero and 100%. Fig. 2.20 shows the corresponding time domain response of the modulator output. The

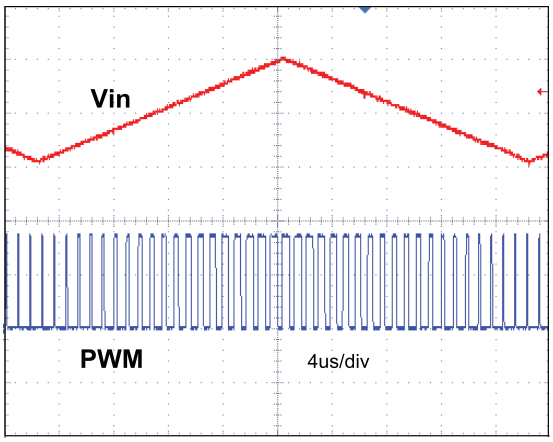


Figure 2.19: Experimental time domain response of the modulator to a triangle input voltage without duty ratio saturation.

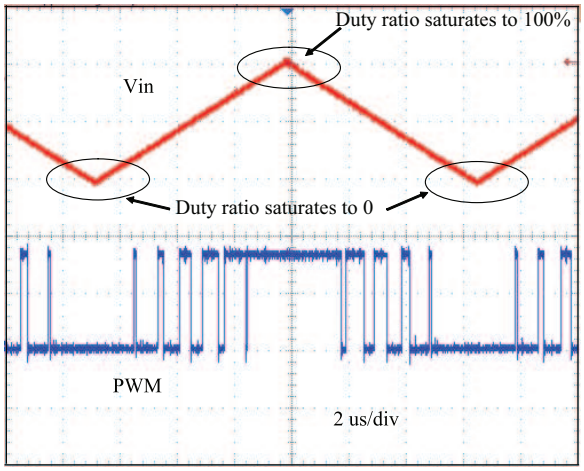


Figure 2.20: Experimental time domain response of the modulator to a triangle input voltage with duty ratio saturates to both 0 and 100%.

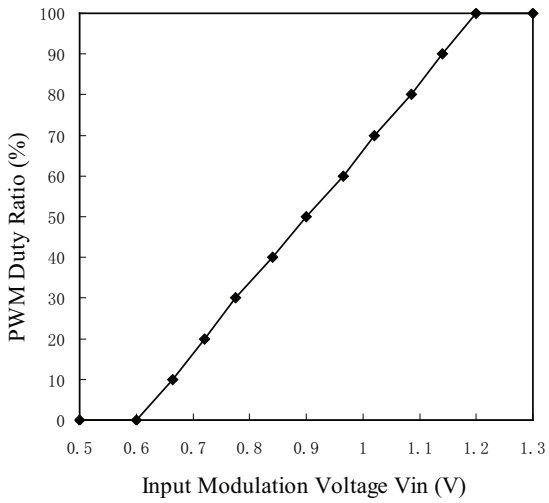
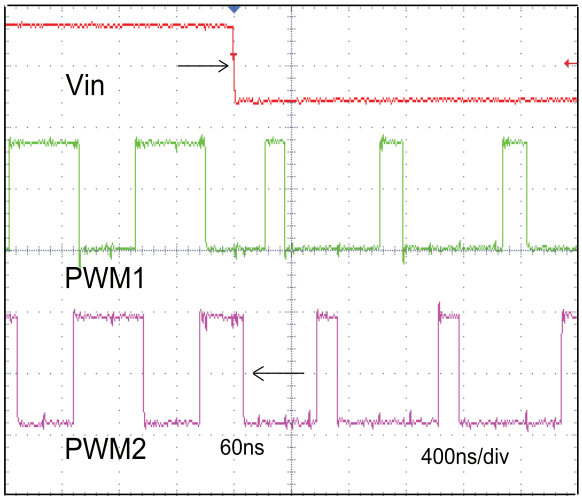
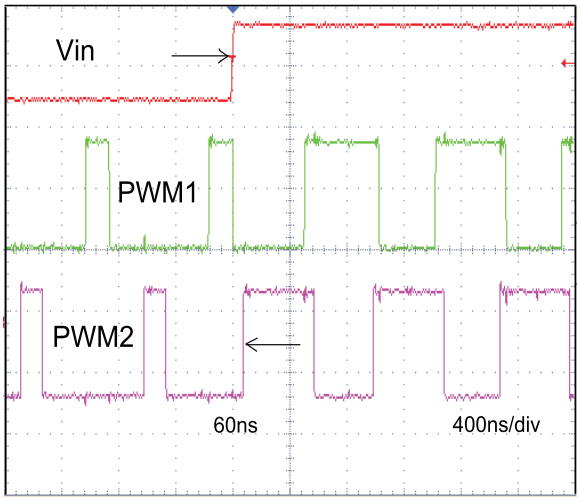


Figure 2.21: Measured transfer characteristic of PWM duty ratio versus input voltage.

modulator is able to generate PWM signal with zero and 100% duty ratio and recover from saturation state to normal operation. Fig. 2.21 gives the measured output PWM duty ratio versus input voltage command V_{in}, showing the good linearity of the pulse width modulator. The double-edge modulation characteristic is verified by applying a large step voltage at the input. A positive step input voltage and two of the sixteen PWM output signals (with 180 degree phase shift) are shown in Fig. 2.22(a). The period of the PWM signal is approximate 880ns. The rising edge of PWM2 is generated right after applying the voltage step at the input with 60ns delay. The response to a negative step input voltage is shown in Fig. 2.22(b), the falling edge of PWM_2 is generated right after applying the voltage step at the input with 60ns delay. As seen, both edges of the PWM signal are modulated by the input voltage and the designed pulse-width modulator provides fast transient response.



(a)



(b)

Figure 2.22: Experimental transient response of pulse width modulate (a) Applying step up voltage at input (b) Applying step down voltage at input

Chapter 3

Architecture of Multi-Mode Multi-Phase Digital Controller for VR Application

3.1 Overview of System Architecture

The system architecture of the digitally controlled four-phase voltage regulator is shown in Fig. 3.1, in which a 4-phase interleaved buck topology is used to share the large load current and reduce the output voltage ripple. The digital controller, based on functionality, can be partitioned into power regulation domain and power management domain. The power regulation subsystem implements the voltage regulation function, providing tight DC regulation and fast load transient response. The power management subsystem performs advanced power control and management tasks, such as optimizing converter efficiency, communicating with the host system, updating control parameters, monitoring system variables such as load current and output voltage and providing fault protection and recovery, etc.

In the power regulation domain, analog power supply variables, such as output voltages, load currents and reference voltage, are sampled and quantized by fast windowed-type analog-to-digital converters. These digitized quantities are processed by the digital loop compensator, which generates the command to the digital pulse width modulator (DPWM). The DPWM module converts the digital command to pulses to control the on/off of the power MOSFETs in the power stage.

The power management domain consists of an embedded microcontroller and corresponding data and program memory, which enables advanced control and management functions; analog-to-digital converters to sense and monitor system variables; digital-to-analog converter to set the reference; I^2C/PMBus interface to communicate

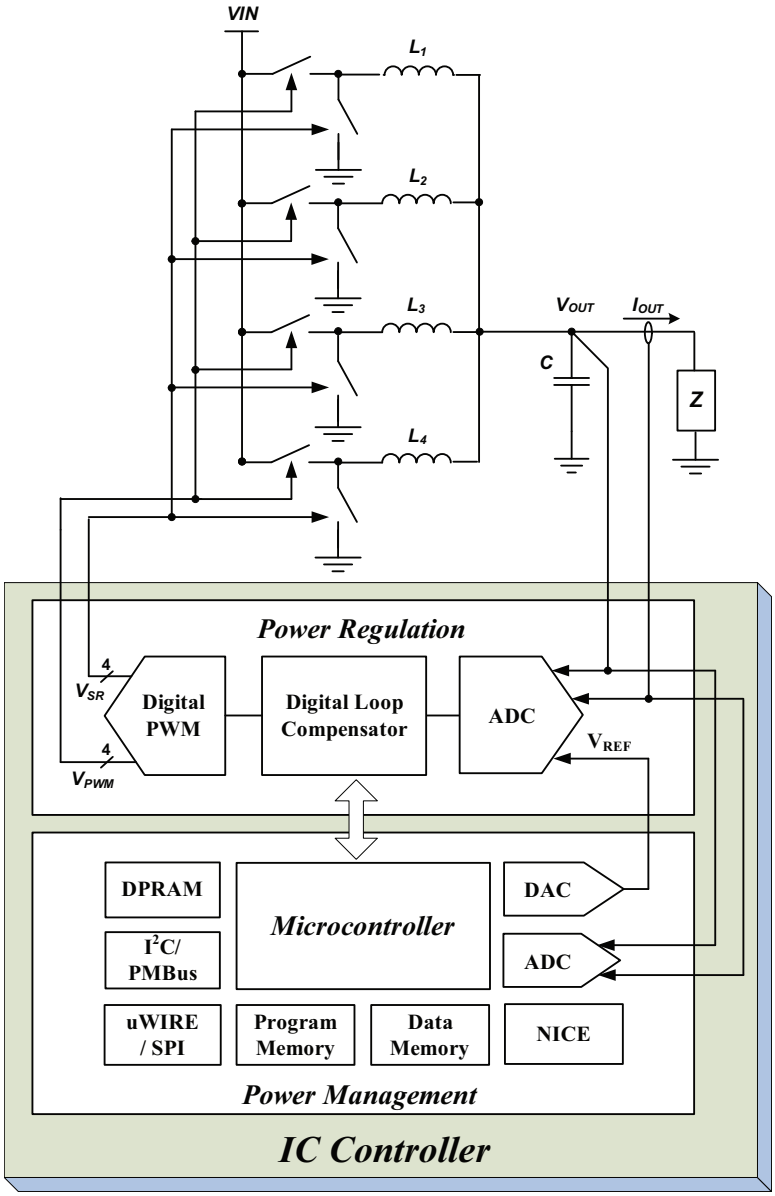


Figure 3.1: System architecture of a digital controlled four-phase voltage regulator

with the host system and the debug ports.

The block diagram of the controller is shown in Fig. 3.2. The controller IC combines a voltage feedback loop and a load current feedforward control. The use of load current feedforward control extends the useful bandwidth beyond the limits imposed by feedback stability constraints, which improves the load transient response of the voltage regulator [3]. The output V_{out} and load line voltage $V_{ref} - I_{out}R_{ref}$ are directly combined in the analog domain at the ADC input of the feedback loop. To reduce the latency of feedforward control and relax the sampling speed requirement of the load current, a high pass filter is applied to the load current before it is quantized by the ADC in the feedforward control. Since the dc level of the feedforward signal is blocked by the high pass filter, a simple low-resolution windowed ADC structure [8] can be used to quantize it. The required gain of the feedforward control is adjusted appropriately in the digital domain. The total duty ratio command is obtained by combining the output of the digital PID compensation network and feedforward control.

A multi-mode control strategy is applied in the designed controller. When the load current is high, the converter runs in fixed frequency continuous conduction mode (CCM). At light loads, the converter enters discontinuous conduction mode (DCM), where the inductor current is zero during part of the switching period. At very light loads, the converter operates in variable-frequency pulse skipping mode. The optimal synchronous rectifier (SR) timing is scheduled as a function of the load current and

stored in a look up table. Depending on the load current, transitions among different operation modes occur automatically by timing the SR switch appropriately and by suppressing gate pulses to effect pulse skipping. The optimal SR timing obtained from off-line power loss measurement is programmed into the dead-time look up table and scheduled as a function of the load current. The DPWM module takes the duty ratio command and the SR timing as inputs and converts this data into four-phase PWM and SR signals that control the high side and low side switches.

During the voltage regulator start up, a programmable soft start counter is enabled to slew the digital integrator to the value close to the external reference voltage, so that the power train will not be overstressed.

In order to achieve tight voltage regulation, a high resolution 13-bit DPWM is designed with effective 1.5mV step size. The ADC quantization step size is designed to be 4mV to avoid the sub-harmonic limit cycling [12]. The circuit implementation of the ADC and DPWM module will be discussed in detail in Chapter 4.

An 8-bit microcontroller and associated program and data memory are embedded in the designed IC controller. It has a built-in MICROWIRE/SPI interface to set the reference voltage, and to program control registers in the power regulation domain. A dual-port ram is used here as the deadtime look up table, which is programmed by the microcontroller and read by the DPWM module. A I^2C/PMBus interface is used to communicate with the external host system.

Section 3.2 discusses application of the load current feedforward control to digital

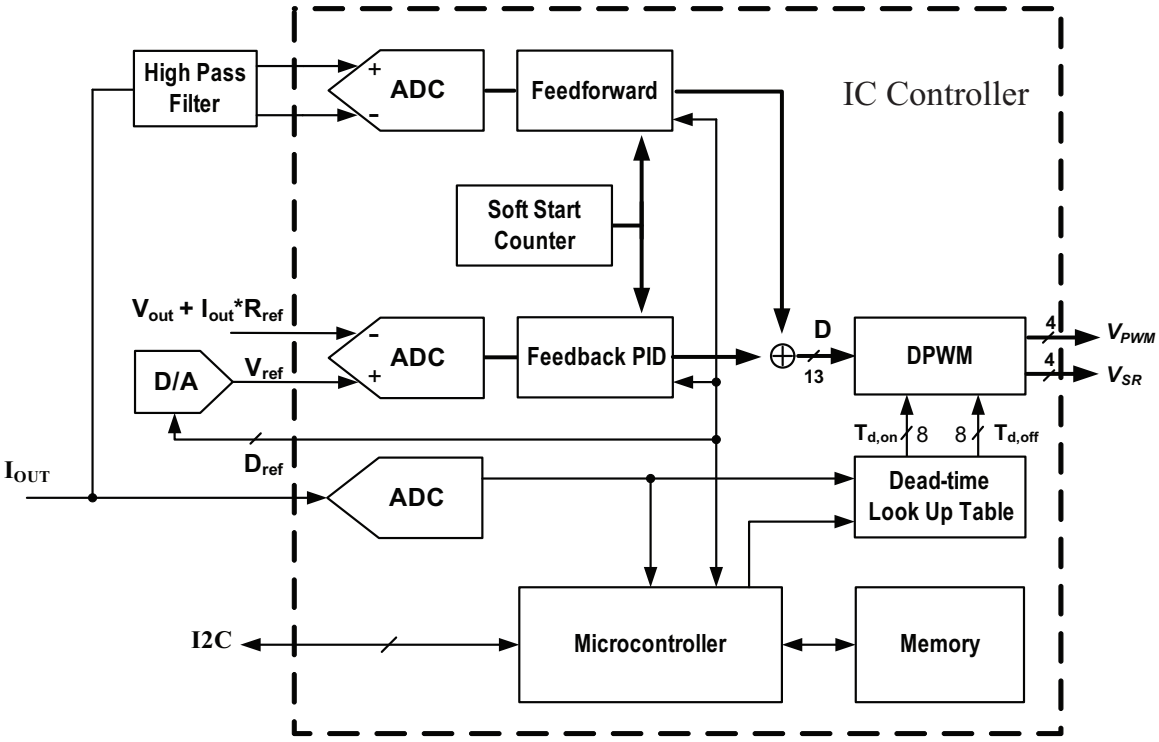


Figure 3.2: Block diagram of the IC controller for four-phase voltage regulator

control loop, aiming to improve the load transient response. In Section 3.3, the multi-mode buck converter operation is discussed. The load-scheduled dead time control to improve the converter efficiency is presented. The feedback compensator with load-scheduled integrator array aiming to improve the transient response in discontinues conduction mode is proposed in Section 3.4. Section 3.5 discusses the embedded microcontroller subsystem and memory interface.

3.2 Load Current Feedfoward Control

The specifications for modern microprocessor voltage regulators (VR's) require that the microprocessor supply voltage follows a prescribed load line with a slope of about one milliohm [13]. This requires tight regulation of the voltage regulator output impedance. The method of using load-current feedforward to extend the useful bandwidth beyond the limits imposed by feedback stability constraints has been proposed in [3]. With this approach, feedforward is used to handle the bulk of the regulation action, while feedback is used only to compensate for imperfections of the feedforward and to ensure tight DC regulation. In this case, the size of the output capacitor is determined by large signal transient and switching-ripple considerations, and not by a feedback stability constraint.

In [3], load current feedforward control is developed in a continuous-time analog framework as shown in Fig. 3.3 and the control law can be approximated as

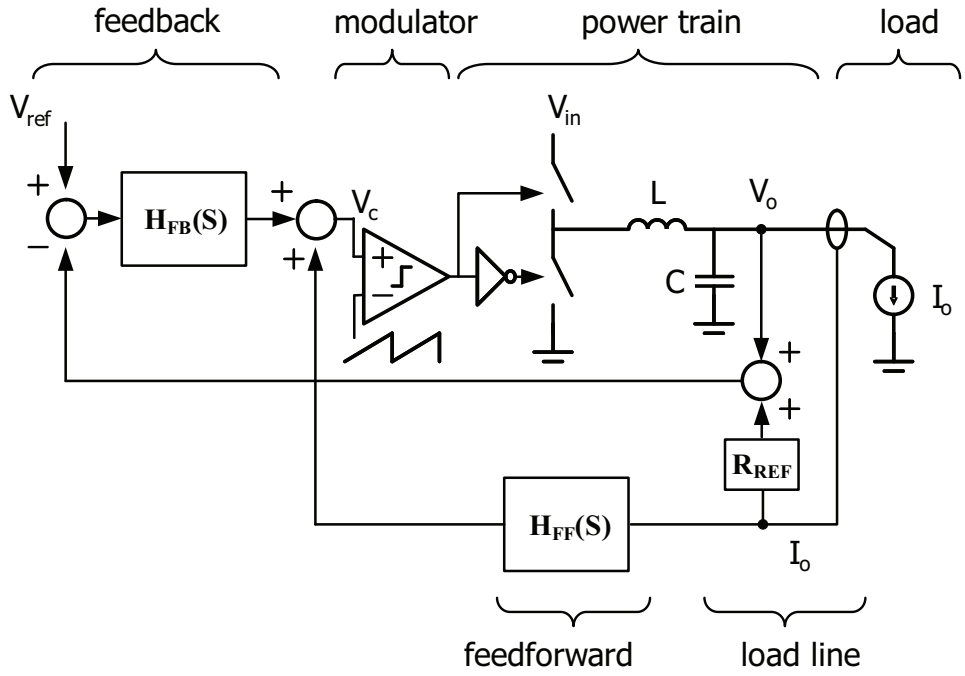


Figure 3.3: Block diagram of a buck converter with load current feedforward control

$$H_{FF}(s) \approx \frac{sL}{sR_{ref}C + 1} \tag{3.1}$$

Where R_{ref} is the load line reference impedance. Low latency associated with the load current feedforward control is essential for achieving a fast controller response.

There are several technical issues when applying the load current feedforward to a discrete-time, digital control implementation by directly sampling and processing the load current in the digital domain. Most significantly, the aggressive load current transient (with the slew rate of $1A/ns$ according to [13]) requires fast sampling and processing of the load current. Another issue is the large dynamic range requirement by directly quantizing the load current over a wide load range.

Fig. 3.4 shows the discrete time, digital implementation of feedforward control.

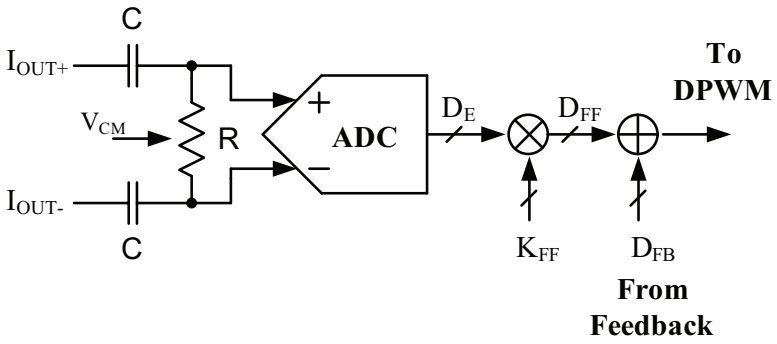


Figure 3.4: Bloack diagram of feedforward control in digital controller

To relax the sampling speed requirement and reduce the latency associated with the processing of load current in the digital domain, most of the feedforward control law is implemented in the analog domain by using a simple RC type high pass filter with transfer function

$$H(s) = \frac{sRC/2}{sRC/2 + 1} \tag{3.2}$$

Ignoring the sampling and processing delay, the feedforward control law will be equivalent in the analog and digital implementations by matching the RC time constants in Equation 3.2 and Equation 3.1, and adjusting the feedforward gain K_{FF} in the digital domain, which can be done by a simple digital multiplier. The total duty ratio commands is obtained by combining the output of the feedback compensator D_{FB} and feedforward control D_{FF}. The sampling speed of the feedforward ADC is determined by the duty cycle command update rate in the DPWM module, since feedforward control output sampling rate faster than the duty cycle command update

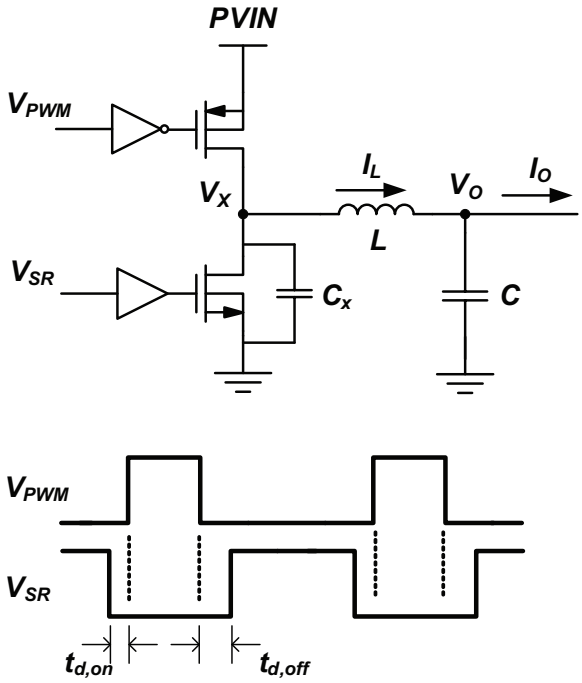


Figure 3.5: Synchronous buck converter and corresponding switch control signals

rate will not be reflected in the PWM output. In the prototype IC, the sampling rate of the feedforward control is set to 4MHz, which is equal to the update rate of the DPWM module. Since the dc level of the feedforward signal is blocked by the high pass filter, a simple moderate-resolution windowed ADC structure [8] can be used to quantize it, and the imperfection of the feedforward control due to the sampling delay and moderate quantization resolution will be compensated by the feedback loop.

3.3 Multi-Mode Control

3.3.1 Multi-Mode Operation

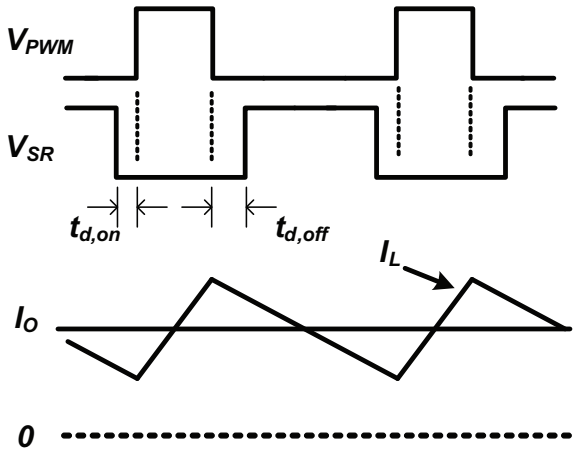
A synchronous buck converter with corresponding high side and low side switch control signals is shown in Fig. 3.5. Under different load conditions, there are different optimal gating patterns for the switches. To ensure high efficiency operation over a wide load range, the buck converter can be operated in different modes depending on the load current.

3.3.1.1 Continuous Conduction Mode

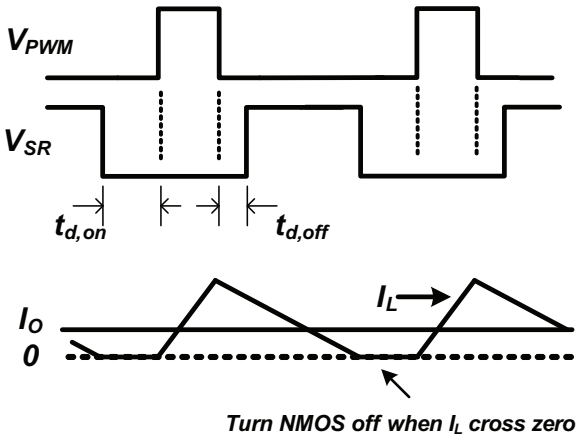
At heavy load, the converter operates in CCM with a fixed switching period T_s. The buck converter switching waveforms are shown in Fig. 3.6(a). The control switch on-time is $T_{on} = DT = MT$, where D is the duty ratio, $M = V_o/V_{in}$ is the conversion ratio, and V_{in} and V_o are the input and output voltages, respectively. The inductor current ripple ΔI_L is given by

$$\Delta I_L = \frac{V_o(1-D)}{L} T_s \tag{3.3}$$

The load current I_o equals the DC component of the of the inductor I_L. When I_o is greater than $\Delta I_L/2$, the inductor current remains positive over the entire switching cycle. The converter is considered to be in continuous conduction mode. The optimal turn-off dead time $t^*_{d,off}$ depends on the intrinsic turn-off delay $t_{d,off0}$ of the control



(a)



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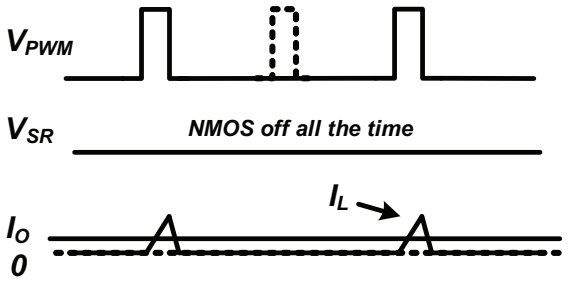


(c)

Figure 3.6: Buck converter switching waveforms (a)Continuous conduction mode (b)Discontinuous conduction mode (c)Pulse skipping mode

switch M_1, and the time it takes to discharge the switching node capacitance C_x [14],

$$t^*_{d,off} = \frac{V_{in}C_x}{I_o} + t_{d,off0}, \tag{3.4}$$

Further, the optimal turn-on deadtime $t^*_{d,on}$ is a small constant to prevent conduction overlap between the control switch and the SR.

The power losses in CCM are typically dominated by conduction losses caused by the load current and the inductor current ripple ΔI_L flowing through the switches and the inductor [15],

$$P_{loss,CCM} = r'_L \left(I_o^2 + \frac{1}{12}\Delta I_L^2 \right), \tag{3.5}$$

where r'_L is the average switch resistance in series with the inductor resistance.

3.3.1.2 Discontinuous Conduction Mode

At lighter loads, when load current I_o is less than $\Delta I_L/2$, the inductor current takes on negative values during some intervals of the switching period with the deadtime discussed in the previous subsection. To minimize the power loss, the SR is gated so that it does not allow negative inductor current. The converter is considered to run in discontinuous conduction mode as the inductor current is zero for a finite interval of each switching period. The corresponding DCM switching waveforms are shown in Fig. 3.6(b). The duty ratio now depends on the load current,

$$D = \sqrt{\frac{2LI_oM}{V_{in}T(1-M)}} \tag{3.6}$$

The optimal turn-off dead time still follows (3.4). The optimal $t_{d,on}$ is equal to the time the inductor current is zero,

$$t^*_{d,on} = T\left(1 - \frac{D}{M}\right) + t_{d,on0}. \tag{3.7}$$

And, the corresponding conduction power loss in DCM is [14]

$$P_{loss,cond,DCM} = \frac{r'_L}{3}(2I_o)^{3/2}\Delta I^{1/2}_{L,CCM}. \tag{3.8}$$

Clearly, allowing the converter to enter DCM by appropriately timing the SR at light load results in significant power savings.

3.3.1.3 Variable-Frequency Pulse Skipping Mode

At very light load in constant frequency operation, the converter loss would be dominated by switching losses [15],

$$P_{loss,sw} = \left[\frac{1}{2}C_x V^2_{in} + C_g V^2_G\right] f_{sw}, \tag{3.9}$$

where C_g is the total high-side and low-side gate capacitances, and V_G is the gate drive voltage swing. The switching loss consists of hard switching loss, $\frac{1}{2}C_x V^2_{in}$ in Equation 3.9, and gate drive loss, $C_g V^2_G$ in Equation 3.9. They are both proportional to the switching frequency. Thus, it is advantageous to allow variable frequency operation at very light loads. This can be done by setting a minimum duty ratio D_{min} in the digital controller. When the duty ratio command is less than D_{min}, the PWM pulse will be skipped and switching frequency varies. The corresponding switching waveforms are shown in Fig. 3.6(c).

3.3.2 Load-Scheduled Dead Time Control

As discussed above, transitions among different operation modes can occur automatically by timing the SR switch appropriately based on the load current. The optimal SR switch timing can be derived from the theoretical equations, such as Equation 3.4 and Equation 3.7, or obtained from off-line efficiency measurements. Experimental results [Chapter 5] show that there is a broad minimum in the power loss versus SR timing curve, and only moderate precision timing data is required. Therefore, it is straightforward to program the optimal SR timing obtained from off-line power loss measurement into the dead-time look up table and scheduled as a function of the load current.

3.4 Load-Scheduled Feedback Controller

3.4.1 Feedback Compensator

Fig. 3.7 shows the digital feedback compensation network with soft start control. A digital PID control law is used to calculate the duty ratio command D_c for the next switching period. For the PID controller implementation shown in Fig. 3.7, D_c is given by

$$D_c[n+1] = K_P D_e[n] + K_D(D_e[n] - D_e[n-1]) + K_I D_i[n] \tag{3.10}$$

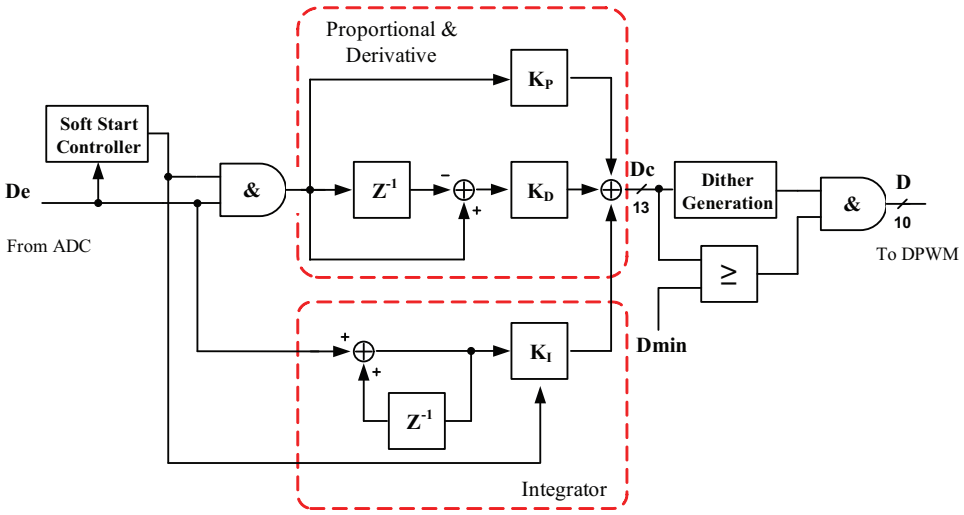


Figure 3.7: Block diagram of feedback compensator with soft start control

where $D_e[n]$ is the digitized error voltage generated from the ADC, $D_c[n]$ and $D_i[n]$ are the duty cycle command and digital integrator value of the sampling period

$$D_i[n] = D_i[n-1] + D_e[n-1] \tag{3.11}$$

From Equation 3.10 and Equation 3.11, the Z-domain transfer function of the compensator is

$$H(Z) = K_P + K_D(1 - Z^{-1}) + K_I \frac{Z^{-1}}{1 - Z^{-1}} \tag{3.12}$$

K_P is the proportional gain, K_D is the derivative gain, and K_I is the integral gain. The design of the digital PID compensator can be based on the average continuous-time model, and by transforming the PID compensator transfer function from the s-domain to the Z-domain. Or, the direct digital design method can be used. Both methods will be discussed in detail in Appendix A. The parameters K_P , K_I and K_D are all programmable by the embedded microcontroller to be able to accommodate

different external power trains.

To avoid power train over stress during the voltage regulator start up, a soft start function is integrated into the controller by disabling the proportional and derivative term and slewing the digital integrator to the value close to the external reference voltage. In [8], a startup counter that is clocked by the internal clock from the DPWM module gives a start-up sequence and slews the integrator to reach the appropriate steady-state value. Since the startup time is fixed by the internal clock frequency no matter what the reference voltage level is, overshoot or sub-harmonic oscillation might occur when the programmed start up time is too small or too large.

In this work, during the voltage regulator start up, the proportional and derivative term are disabled and the integrator gain is set to a value which is determined by the slope of the ramp that the output voltage is commanded to follow during the start-up. The start-up process ends when error voltage V_e is within the zero error bin of the reference voltage. At this time step, the proportional and derivative term is enabled and the integrator gain is set back to the designed nominal value.

3.4.2 Load-Scheduled Integrator Array

When a buck voltage regulator runs in discontinuous conduction mode (DCM), from Equation 3.6, the steady-state duty-ratio command varies substantially as a function of the load current, unlike in CCM where it is ideally constant. The load transient response is slow since the integrator has to slew over a wide range (see

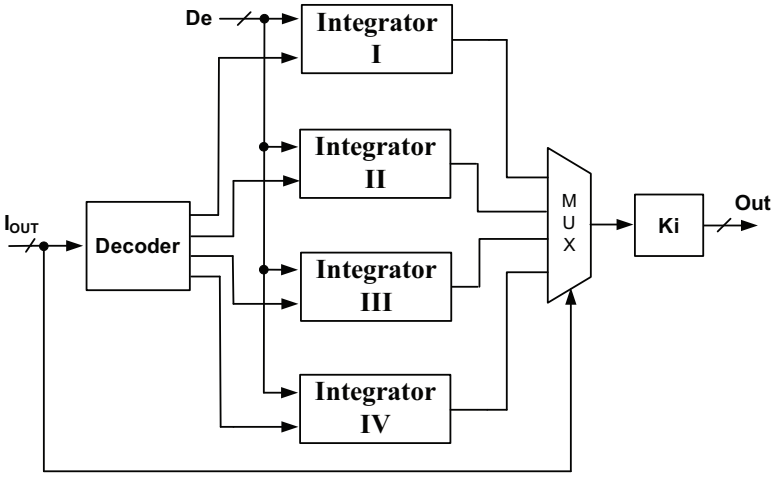


Figure 3.8: Block diagram of load-scheduled integrator array

chapter 5 for experimental results). An adaptive scheme in the digital feedback compensation network is applied to resolve this problem. As shown in Fig. 3.8, the integral component of the duty cycle command is parameterized as a function of the load current. Instead of a single integrator in the PID controller, multiple integrators are used, to span the converter operating load range. A decoder, addressed by the load current, is used to choose which integrator is enabled, and its corresponding value goes to the output. The deselected integrators are simply locked with their current states. In this way, no integrator needs to slew over a wide range when the buck voltage regulator transitions between DCM and CCM operation. Glitch free fast transient response is achieved. Experimental results are reported in Chapter 5.

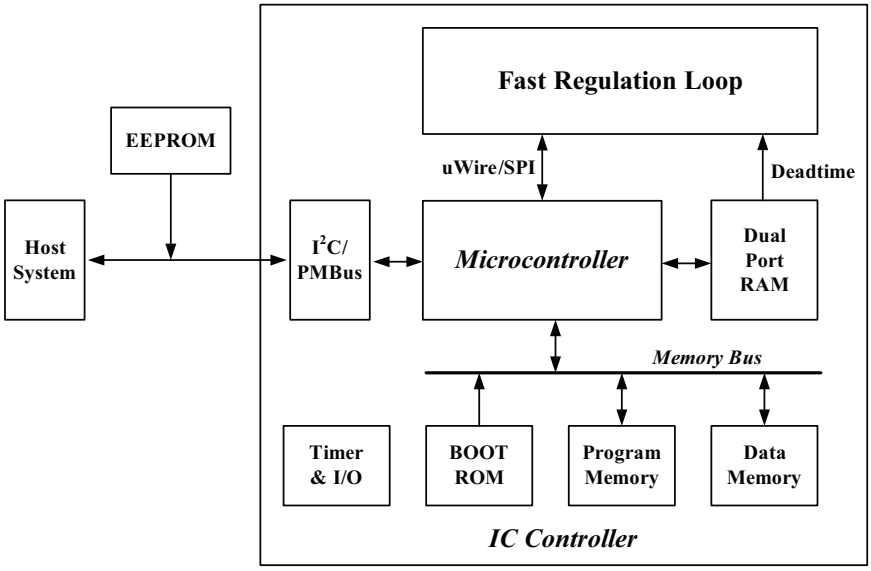


Figure 3.9: Block diagram of embedded microcontroller subsystem

3.5 Microcontroller and Memory

A 8-bit microcontroller is embedded in the designed IC controller enabling advanced control schemes and power management functions. The block diagram of the microcontroller subsystem is shown in Fig. 3.9. The microcontroller subsystem consists of a COP8 microcontroller, associated program memory and data memory, dual port RAM used as the deadtime look up table. This subsystem also has a built-in MICROWIRE interface which programs the control registers in the regulation loop, and an I^2C interface which communicates with the external host system.

When the system is initialized, the COP8 microcontroller is booted from an external Electrically-Erasable Programmable Read-Only Memory (EEPROM). The external EEPROM is also used to store some parameters like PID coefficients and dead-

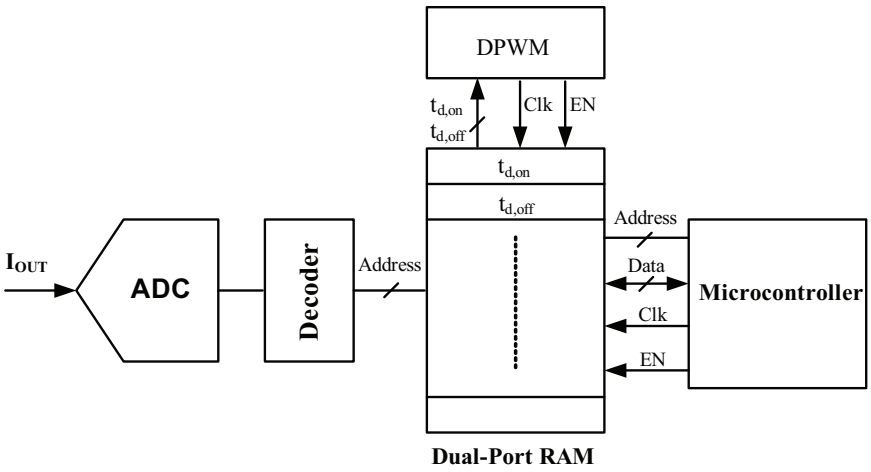


Figure 3.10: Dual-port RAM to implement the deadtime look up table

time that are used to initialize the power controller. After system reset, the processor accesses the EEPROM though the I2C interface port, reads the length of the program, and copies it into the internal program RAM. When the program is copied, the processor begins executing the software. The software can then disable the external EEPROM, as it is not required for normal system operation, and wait for a command from the external host system. Certain default parameters are programmed into the developed controller IC when the system starts without the external EEPROM, so that the controller can operate alone without the external host system.

As shown in Fig. 3.10, A 128-byte dual port RAM is used as the deadtime look up table. It is programmed by the microcontroller and the quantized output current I_{out} is decoded and used as the address for reading from the look up table. The deadtime output to the DPWM module is synchronized with the clock of the duty cycle command and combined to generate the SR control signal. The detail of timing

generation will be discussed in Chapter 4.

Chapter 4

Circuit Implementation for Multi-Mode Multi-Phase Digital Controller

4.1 ADC Design

4.1.1 ADC architecture

The block diagram of the ring-oscillator-based ADC is shown in Fig. 4.1, similar to the design reported in [9]. The analog section of the ADC consists of an input stage, converting the input voltage to current and driving two identical ring oscillators, and level shifters used to restore the low-swing outputs of the ring oscillator to large-swing digital signals. The error voltage V_e between converter output voltage V_o and reference voltage V_{ref} is amplified by the input stage and converted to a differential current that results in instantaneous differential frequency in the two ring oscillators. The digital section of the ADC generates the digital error command D_e, based on the frequency difference of two ring oscillators. Instead of counting the frequency from one tap per ring oscillator, all M uniformly spaced taps on each respective ring oscillator are observed for frequency information, increasing the ADC resolution by M. Offset cancellation and programmable quantization resolution adjustment are also done in the digital domain.

Ignoring the nonlinearity of the input differential pair, a linear model representing the ring-oscillator-based ADC is shown in Fig. 4.2. The error command D_e is given by

$$D_e = \int_0^{T_s} G_m V_e K_{OSC} = G_m K_{OSC} \int_0^{T_s} V_e \tag{4.1}$$

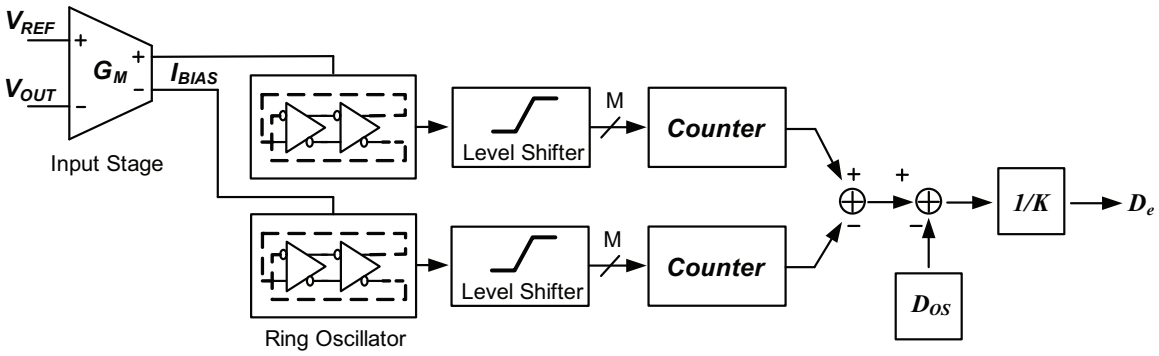


Figure 4.1: Block diagram of the ring oscillator based ADC

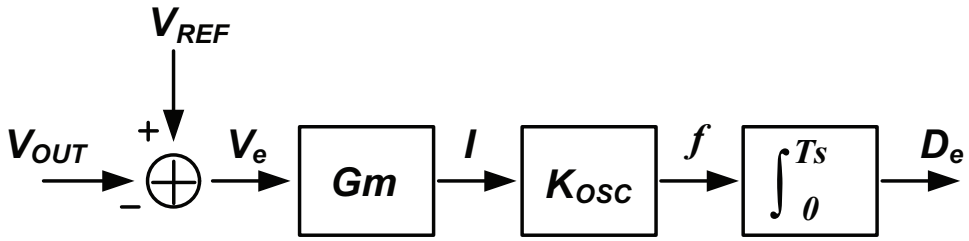


Figure 4.2: Linear model of ring-ADC

where K_{OSC} is the supply current to frequency gain of the ring oscillator and T_s is the switching period. Since an integration inherently takes place in the loop when counting the frequency of the ring oscillator, this ADC is robust against high frequency switching noise or glitch at the input.

Assuming the average error voltage per switching period is $\overline{v_e}$, the error command in Equation 4.1 can be simplified as

$$D_e = MG_mK_{OSC}\overline{v_e}T_s \tag{4.2}$$

For a given oscillator structure, as will be shown in Section 4.1.2, K_{OSC} is inversely

proportional to the number of ring oscillator stages M. Therefore, MK_{OSC} is relatively constant for a given technology, and resolution of the ring-oscillator-based ADC with sampling period T_S is determined by the transconductance of the input stage. The same conclusion is also drawn in [16].

There are several design considerations regarding the input stage of this ring oscillator based ADC. First, to achieve fine ADC resolution, the input stage should have a large transconductance since the ADC resolution is inversely proportional to the transconductance of the input stage as shown in Equation 4.2. Second, to achieve good linearity of the analog to digital conversion, the input stage should have a wide saturation range. Finally, the input stage should have constant transconductance and provide constant bias current to the ring oscillator over a wide common mode input range, such that the overall loop gain remains constant, regardless of the output voltage.

There is a good linear dependency of the ring oscillator frequency on bias current with transistors operating in subthreshold region [Chapter 3]. Therefore, the ring oscillator is designed to be biased in this mode. The tradeoff between the small bias current, wide saturation range and large transconductance pose design difficulties if applying a conventional differential pair as the input stage. A class-AB type input stage can provide large transconductance and a wide saturation range. However, it requires a large differential input voltage to achieve the desired transconductance, resulting in poor output voltage regulation.

Based on the above considerations, the input stage used in Chapter 3 is also used here. It has large transconductance over wide saturation range and good common mode range.

4.1.2 Linearity and Temperature Dependency of ADC

The linearity of the ring-oscillator-based ADC relies on the linear dependency of the frequency on bias current in the ring oscillator. The frequency-current dependency of the ring oscillator can be modeled by using the alpha-power law model, as proposed in [17]. The drain current of a MOSFET is modeled as

$$I_{DS} = K\frac{W}{L}\mu(V_{GS} - V_{th})^{\alpha} \tag{4.3}$$

where μ is the device channel mobility, and K and α are empirical parameters which can be extracted from the device model. References [18] and [19] show that the alpha-power law model is also valid for transistors operating in subthreshold region. It has been shown in [17] that a CMOS inverter delay can be expressed as

$$t_{pHL}, t_{pLH} = (\frac{1}{2} - \frac{1 - v_T}{1 + \alpha})t_T + \frac{C_L V_{DD}}{2I_{D0}}, \quad v_T = \frac{V_{th}}{V_{DD}} \tag{4.4}$$

where t_{pHL} and t_{pLH} is the time from a half-V_{DD} point of the input to a half-V_{DD} point of the output, with rising and falling edges at the inverter input and output, respectively. Parameter I_{D0} is the nominal saturation drain current at $V_{GS} = V_{DS} = V_{DD}$; t_T is the transition time of the inverter input, which can be approximated as

$$t_T = \frac{C_L V_{DD}}{I_{D0}}\left(\frac{0.9}{0.8} + \frac{V_{D0}}{0.8V_{DD}} \ln \frac{10V_{D0}}{eV_{DD}}\right) \tag{4.5}$$

where V_{D0} is drain saturation voltage at $V_{GS} = V_{DD}$, and can be expressed as

$$V_{D0} = \left(\frac{V_{DD} - V_{th}}{V_{DD,REF} - V_{th}}\right)^{\frac{\alpha}{2}} V_{D0,REF} \tag{4.6}$$

and $V_{D0,REF}$ is the value measured at the reference supply voltage of $V_{DD,REF}$.

Assuming the delay stage in the ring oscillator is designed such that the inverter delay t_{inv} is equal to t_{pHL} and t_{pLH}, the frequency of an M-stage ring oscillator can be expressed as

$$f_{OSC} = \frac{1}{Mt_{inv}} \tag{4.7}$$

Combining Equations 4.4 and 4.5, and assuming bias current of the ring oscillator I_{bias} is approximate equal to the inverter average on-current I_{D0}, the ring oscillator frequency-current dependency is given by

$$f_{OSC} = \frac{I_{bias}}{\left[\left(\frac{1}{2} - \frac{1-v_T}{1+\alpha}\right)\left(\frac{0.9}{0.8} + \frac{V_{D0}}{0.8V_{DD}} \ln \frac{10V_{D0}}{eV_{DD}}\right) + \frac{1}{2}\right] MC_L V_{DD}} \tag{4.8}$$

where V_{D0} is defined in Equation 4.6, and V_{DD} is the voltage swing on the current-starved ring oscillator. Equation 4.8 is a general equation which gives the frequency and supply current dependence of the ring oscillator in all operating conditions. In particular, when the ring oscillator runs in subthreshold region, in which $V_{DD} \approx V_{th}$,

Equation 4.4 and Equation 4.6 give

$$v_T = 1 \; and \; V_{D0} = 0 \tag{4.9}$$

Therefore, Equation 4.8 can be further simplified as

$$f_{OSC} = I_{bias} K_{OSC} \tag{4.10}$$

and

$$K_{OSC} = \frac{1}{\frac{16}{17} M C_L V_{DD}} \tag{4.11}$$

which is close to the frequency-current dependence equation derived in [16].

Although the ring oscillator frequency has a positive temperature dependence [19] [20], the temperature dependence of K_{OSC} is relative constant, which can be seen from the simulation plot in Fig. 4.3. The variation of K_{OSC} as the temperature changes from -40C to 125C is less than 5%. Therefore, the ADC LSB resolution sensitivity to temperature of the ring oscillator is small.

4.1.3 Offset Cancellation

The mismatch in the input stage and in the matched ring oscillators causes DC offset in the ADC. An auto-zero type offset cancelation scheme is used to cancel the DC offset as shown in Fig. 4.4. The DC offset caused by device mismatch in the input stage and ring oscillators is modeled as an input-referred offset voltage V_{OS}. During the offset cancelation period, S_1 and S_2 turn on and the ADC inputs are shorted to

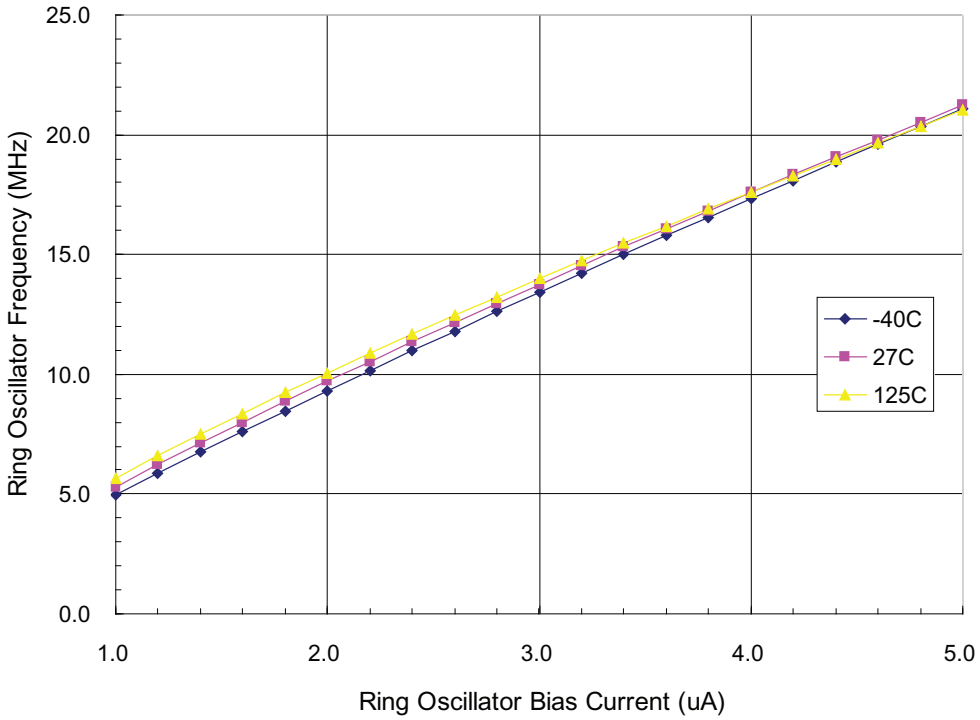


Figure 4.3: Simulated frequency-current dependency of ring oscillator for different temperature

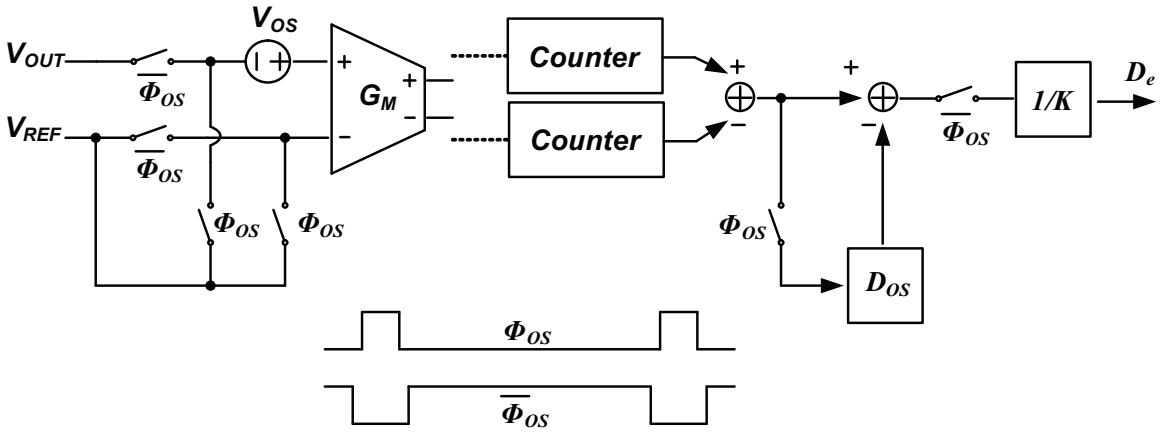


Figure 4.4: Simplified block diagram of ADC offset cancelation

the reference voltage V_{ref}, the offset voltage V_{OS} is quantized by the ADC and the corresponding digital representation D_{OS} is stored into the offset register. During the normal conversion period, the quantized offset voltage D_{OS} is subtracted from the digital error command and the resulting ADC output is offset-free.

During the offset cancelation period, the ADC stops sampling the output voltage and the previous digital error signal D_e may be used. Since the offset cancellation is only done once per one thousand switching cycles to follow the temperature changes, the impact to the system transient response is small.

In this work, the offset cancellation is performed during the soft-start period of the voltage regulator. The digital offset command is stored into a digital register and to be subtracted from the digital error voltage command. In this way, the system transient response is not affected by the ADC offset cancellation.

4.1.4 Implementation of ADC

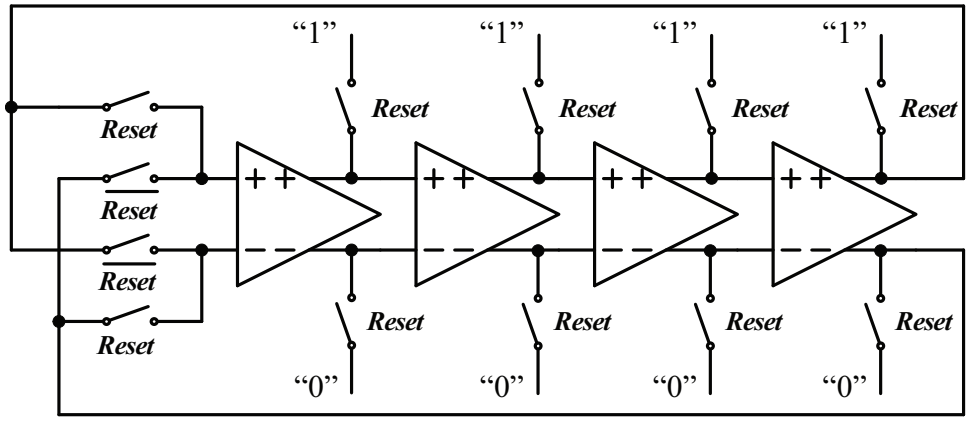
It has been shown in previous work [16] that the minimum quantization step size of the ring-ADC is bounded below by

$$\Delta V = \frac{2}{G_m K_{OSC} T_s} \tag{4.12}$$

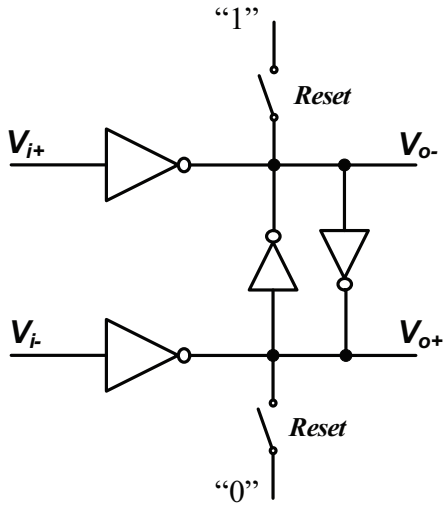
due to the initial phase uncertainty in the two ring oscillators at the beginning of the sampling period. This poses a big overhead to achieve fine ADC resolution, as the large G_m requirement results in more power dissipation.

Since the start and stop pulses for the counters are asynchronous with respect to the ring oscillator signals, the risk of metastability is present when synchronizing the ring oscillator outputs with the reference clock.

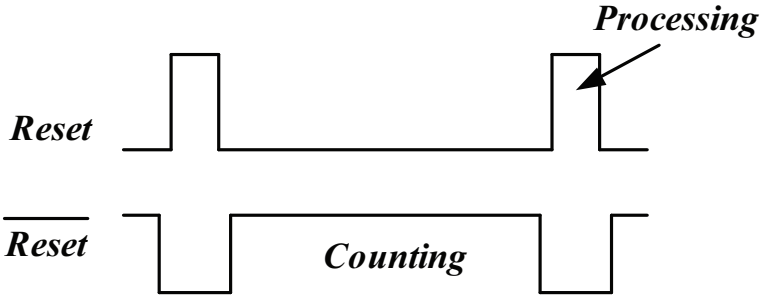
The synchronization problem and uncertainty in the initial phase can be solved by having a state-reset ring oscillator. The ring oscillator is designed such that it is restarted from a known state at the beginning of the sampling period. The block diagram of the ring oscillator, delay stage of the ring oscillator and corresponding switch timing is shown in Fig. 4.5. When reset signal is low, as shown in Fig. 4.5(c), the reset switch is off and the $\overline{reset}$ switch is on, the ring oscillator is configured to have the normal oscillation pattern. The counter starts to count the ring oscillator frequency. When reset signal is high, the oscillator loop breaks and the state of the ring oscillator is simply set as shown in Fig. 4.5(a). The counter stops counting and the post processing digital circuit generates the digital error command.



(a)



(b)



(c)

Figure 4.5: 4-stage differential ring oscillator (a)Simplified schematic with reset switch (b)Delay stage in the differential ring oscillator (c)Corresponding switch timing

4.2 High Resolution DPWM Design

4.2.1 Overview of digital pulse width modulator architecture

The digital pulse width modulation can be done by applying the conventional analog ramp-comparator pulse width modulation scheme in the digital domain. In the method reported in [21], a digital pulse width modulator is constructed by using a fast-clocked counter, which served as the function of a digital ramp, and a digital comparator. The resolution of the pulse width in time domain is determined by the clock period. A clock with frequency $2^n f_s$ is needed to achieve n-bit resolution for a given switching frequency of f_s. For example, a 1 GHz clock is needed to generate a 1 MHz switching frequency PWM signal with 10-bit resolution, which results in excessive power consumption and design complexity to meet the timing constraint.

A tapped delay-line DPWM as proposed in [22] and a similar ring oscillator MUX DPWM scheme as developed in [9] and [8] circumvent the high-frequency clock requirement. In either case, the delay line or the ring oscillator only runs at the converter switching frequency and fine resolution is achieved by multiplexing a particular tap to the output, according to the duty cycle command. Power consumption is significantly reduced compared to the counter-comparator method. However, this approach requires a large-size multiplexer and a large-size delay line or ring oscillator in order to achieve high resolution. For example, a 1024-tap multiplexer and 1024-stage delay line or ring oscillator are needed to generate a 10-bit resolution DPWM signal. This

requires relatively large silicon area. Another issue with this approach is that it is not suitable for high resolution multi-phase application, which requires precise duty cycle matching among all the phases, due to the process variation and mismatch of the ring oscillator. Typically, N large size multiplexors are needed to generate N-phase DPWM signals. It is difficult to achieve good matching among all the delay paths for large size multiplexers and ring oscillators. The stringent symmetry timing requirement of the multi-phase PWM module is difficult to meet due to this delay mismatch

An alternative approach to the ring oscillator MUX scheme has been reported in [23] and [24], in which the delay stages is binary-weighed and the number of delay cells is reduced. The silicon area and power consumption is further reduced compared to the ring oscillator MUX scheme. However, this segmented DPWM architecture has poor linearity and even the monotonicity is not inherently guaranteed by the architecture itself [23]. It also has the similar delay matching problem with the ring oscillator approach when applied to multi-phase application.

A hybrid scheme based on combining the counter-comparator and ring-oscillator-MUX has been reported in [25], [26] and [27]. In this approach, the MSBs of the DPWM resolution are achieved by a counter-comparator scheme, and the LSBs of the DPWM resolution are obtained through a ring-oscillator-MUX scheme. This hybrid approach relaxes the fast clock requirement and reduces the power consumption significantly compared to the counter-comparator approach. Compared to the ring-

oscillator-MUX scheme, the hybrid approach reduces the area and routing complexity. For the multi-phase application, the matching requirement among the phases can be met by sharing the same ring oscillator and MUX. In the hybrid scheme reported by [25] and [26], the resolution of the DPWM is limited by the pulse width of the non-overlapping pulses generated by the delay cell. Therefore, it is difficult to achieve sub-nanosecond resolution.

In this work, a 1 MHz switching frequency four-phase DPWM module with 10-bit resolution and programmable deadtime is implemented based on a hybrid ring-oscillator-MUX and counter-comparator approach. Five MSB resolution is achieved through the counter-comparator and five LSB resolution is obtained from the ring-oscillator-MUX. A race-free synchronization scheme is used to synchronize the pulse signals generated from the comparator and the MUX. The synchronous rectifier signal with programmable deadtime is also generated by this DPWM module. The circuit implementation is presented in Section 4.2.2.

4.2.2 Hybrid DPWM with Programmable Deadtime

4.2.2.1 Single Phase Application

A 10-bit hybrid DPWM is illustrated in Fig. 4.6. The rising edge of the PWM signal is generated by a fixed clock signal and the falling edge is generated by combining a 5-bit counter-comparator and a 5-bit ring oscillator MUX DPWM. The ring oscillator runs at the frequency of $2^5 f_s$, and the 5-bit counter divides the switching

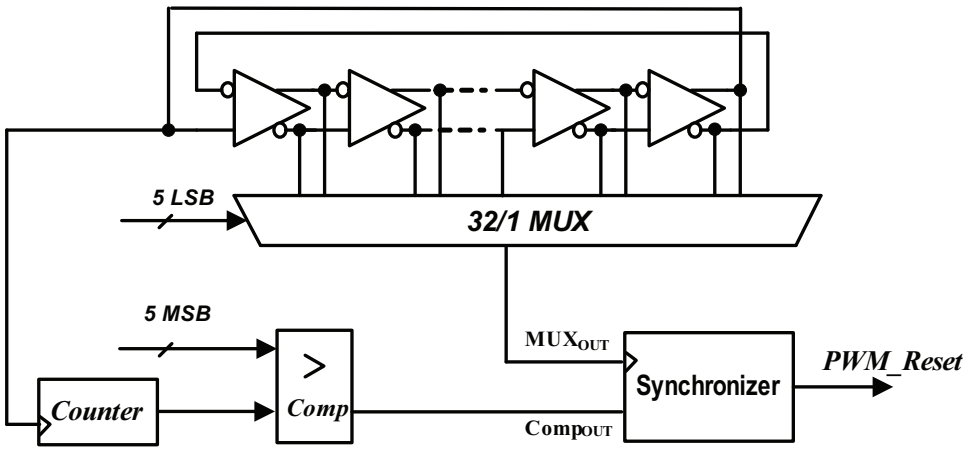


Figure 4.6: Block diagram of the 10-bit DPWM

period into 2^5 segments. In each segment, the ring oscillator generates 2^5 equally spaced square waves from the symmetrically oriented taps. A synchronizer is used to combine the multiplexer and comparator output. The rising edge of the PWM signal is generated at the beginning of the switching cycle. The falling edge of the PWM signal is generated from the tap which is specified by the MUX according to the 5 LSB of the duty cycle command, after the counter reaches the count corresponding to the five MSB's of the duty cycle command.

In [27], a single flip-flop is used to combine the comparator and multiplexer outputs. As shown in Fig. 4.7, a potential race condition occurs when the delay difference between the counter-comparator and the multiplexer is large enough such that the set up time requirement of the flip-flop is violated. The metastability of the flip-flop causes the uncertainty of the pulsewidth of the PWM signal.

A new synchronization scheme is proposed here to combine the comparator and

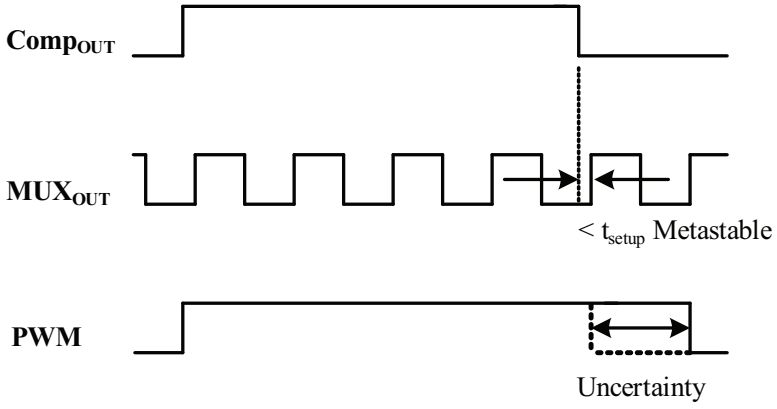


Figure 4.7: Switching waveform of DPWM module

multiplexer outputs and avoid any potential race condition. The synchronization circuit is shown in Fig. 4.8(a) and the switching waveforms assuming the five LSB input of '00001' are shown in Fig. 4.8(b). The comparator output, which represents the coarse DPWM resolution, is sampled by a delayed ring oscillator tap X_0 through a flip-flop D_A, with the delay matching that of the multiplexer. The resulting rising and falling edges of the sampled comparator output Q_A are synchronized with the tap X_0 of the ring oscillator. A second flip-flop D_B is used to combine the multiplexer output and sampled comparator output. The set-up and hold time requirement will be violated if the rising edge of the multiplexer output MUX_{OUT} and the edges of the sampled comparator output Q_A are aligned or close to each other caused by the D-Q delay of flip-flop D_A, routing delay between the output of flip-flop D_A and input of D_B, and the clock skew between D_A and D_B. Such race condition can be avoided by providing sufficient set-up and hold time margin to the flip-flop D_B. This is done by merge the taps X_{31}, X_0 and X_1 to the adjacent taps X_{30} and X_2 as illustrated

in Fig. 4.9(a). The missing timing information of tap X_{31}, X_0 and X_1 is recovered by sampling through $MUX_{OUTShift}$, which is generated by a second MUX with the signal connection shown in Fig. 4.9(b). The inputs of this second MUX shift several taps compared with the first MUX that used to generate signal MUX_{OUT}. In this way, the set-up and hold time requirement of flip-flop D_c can be easily met. With this synchronization scheme, a subnanosecond resolution DPWM is achievable and the DPWM can be fully synthesized.

The ring oscillator consists of 2^{N-1} stage fully differential cells. The full differential cell has the same architecture as the one used in the ring-oscillator-based pulse-width modulator that described in Chapter 2, which allows the ring oscillator to have an even number of stages. The design of the multiplexer is shown in Fig. 4.10. It applies a bit slice architecture and there is only one pass transistor in the signal path, the bit decoding logic determines which transistor is turned on. Since the logic path is separated from the signal path, the delay from the signal input to the multiplexer output is minimized, in comparison to other multiplexer architectures. When laying out the multiplexer, the pass transistors are separated from the decoding logic to achieve good device matching. Since decoding logics are not on the critical timing path, they can be synthesized with other digital logic and the layout accomplishing by automatic place and route tools.

Fig. 4.11 shows the block diagram for generating the synchronous rectifier (SR) control signal with programmable deadtime and its corresponding switching wave-

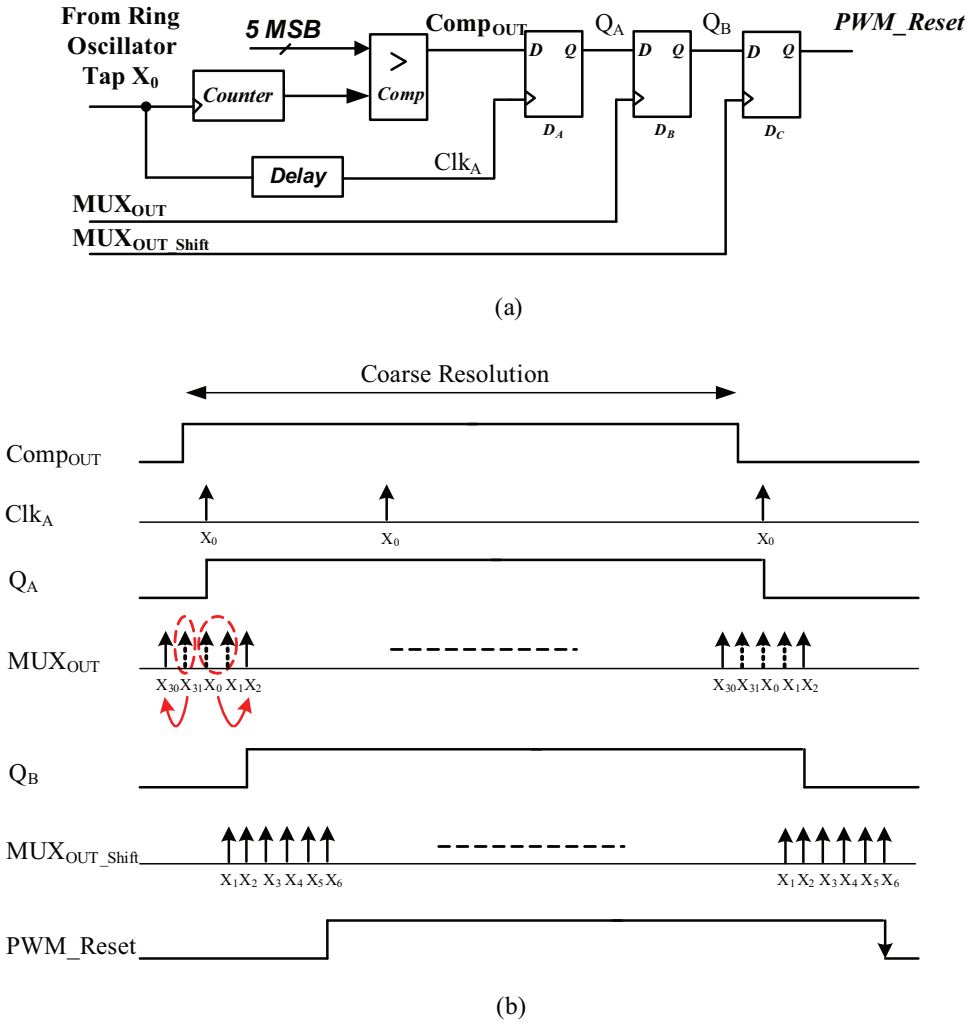
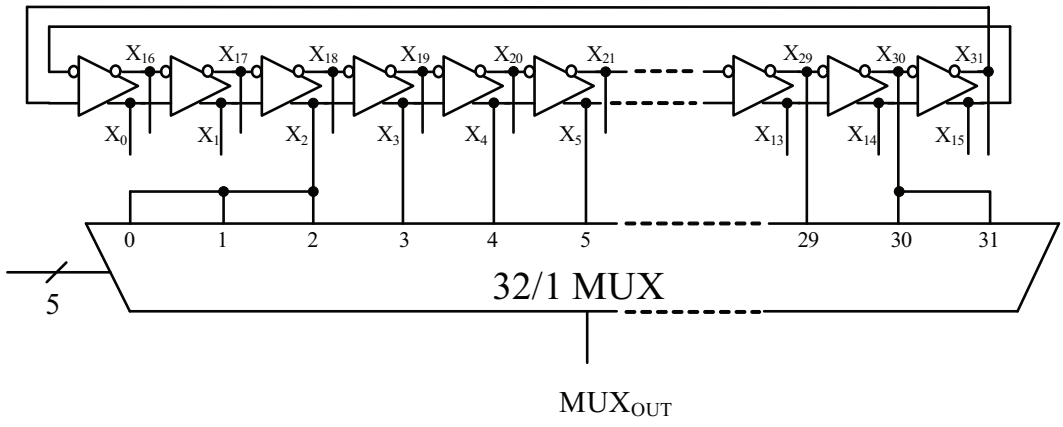
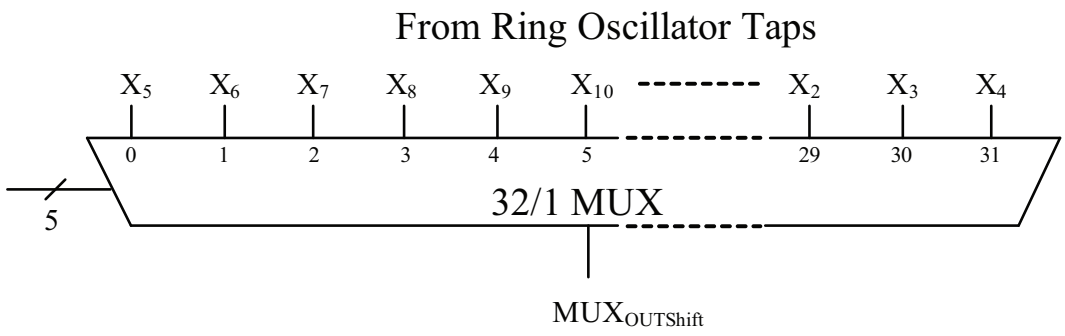


Figure 4.8: Double flip-flop synchronization scheme (a)simplified schematic and (b)switching waveforms



(a)



(b)

Figure 4.9: Connection between ring oscillator and multiplexer (a)generation of MUX_{OUT} signal (b) generation of $MUX_{OUTShift}$ signal.

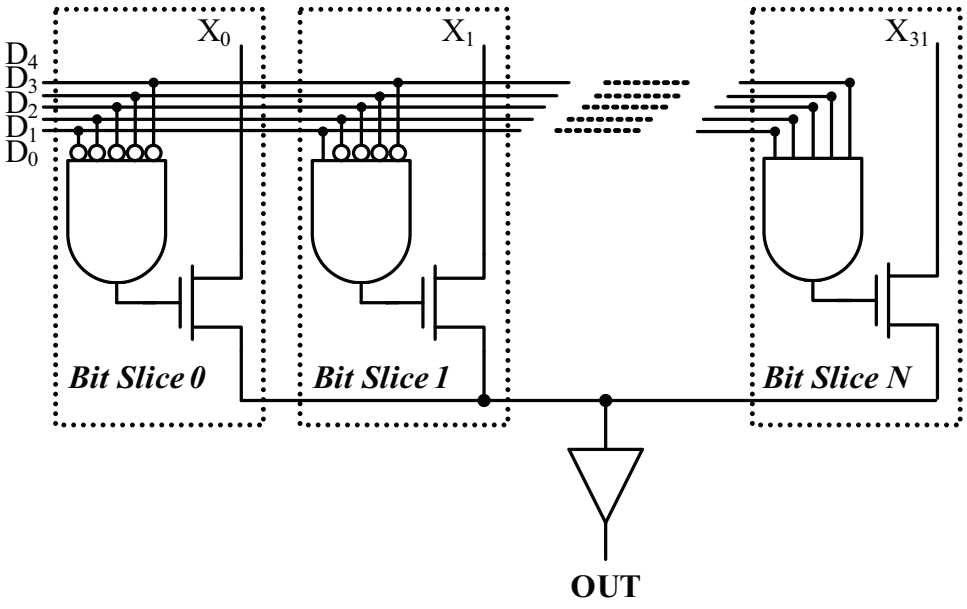


Figure 4.10: Simplified schematic of multiplexer

form. The synchronous rectifier has a complementary switching pattern with deadtime $t_{d,on}$ and $t_{d,off}$ relative to the rising and falling edges of the PWM signal. The same circuit used to generate PWM signal is used here to generate the rising edge and falling edge of the SR control signal respectively with duty cycle input $D + t_{d,off}$ and $1 - t_{d,on}$ respectively. A falling edge triggered set-reset flip-flop is used to combine the two signals to generate the SR control signal. The deadtime $t_{d,on}$ and $t_{d,off}$ are stored in registers and can be programmed externally through a serial parallel interface.

4.2.2.2 Multi-Phase Application

The single-phase DPWM module presented in Section 4.2.2.1 can be easily expanded to a multi-phase application. As shown in Fig. 4.12, the fine resolution

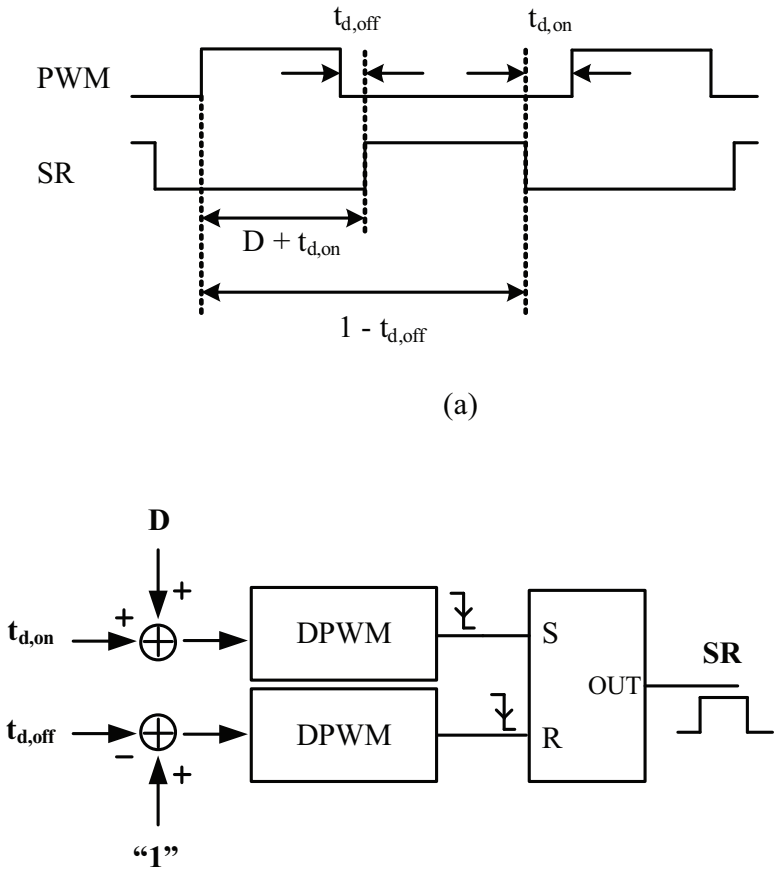


Figure 4.11: Synchronous rectifier control signal generation (a)Switching waveforms (b)Block diagram

generated by the ring-oscillator and multiplexer is shared among all the phases. The five MSB's are generated by the counter-comparator in each phase, and phase shift is implemented through a constant offset added to the counter. Good duty cycle matching among the phases is inherently guaranteed by this architecture, and is only limited by the clock skew which can be well managed by using the automated place and routing tools. The duty cycle command updates at a rate of N times the switching frequency, in which N is the number of the phases in the power train. The update of the duty cycle command is synchronized with the ADC sampling frequency and the sampling frequency of the digital PID feedback loop filter. The multi-phase operation can be reconfigured online by programming the digital offset value that is added to the counter of each individual phase, and by enabling certain phase outputs. For example, the DWPM module can be configured to operate with single phase, two phases or four phases.

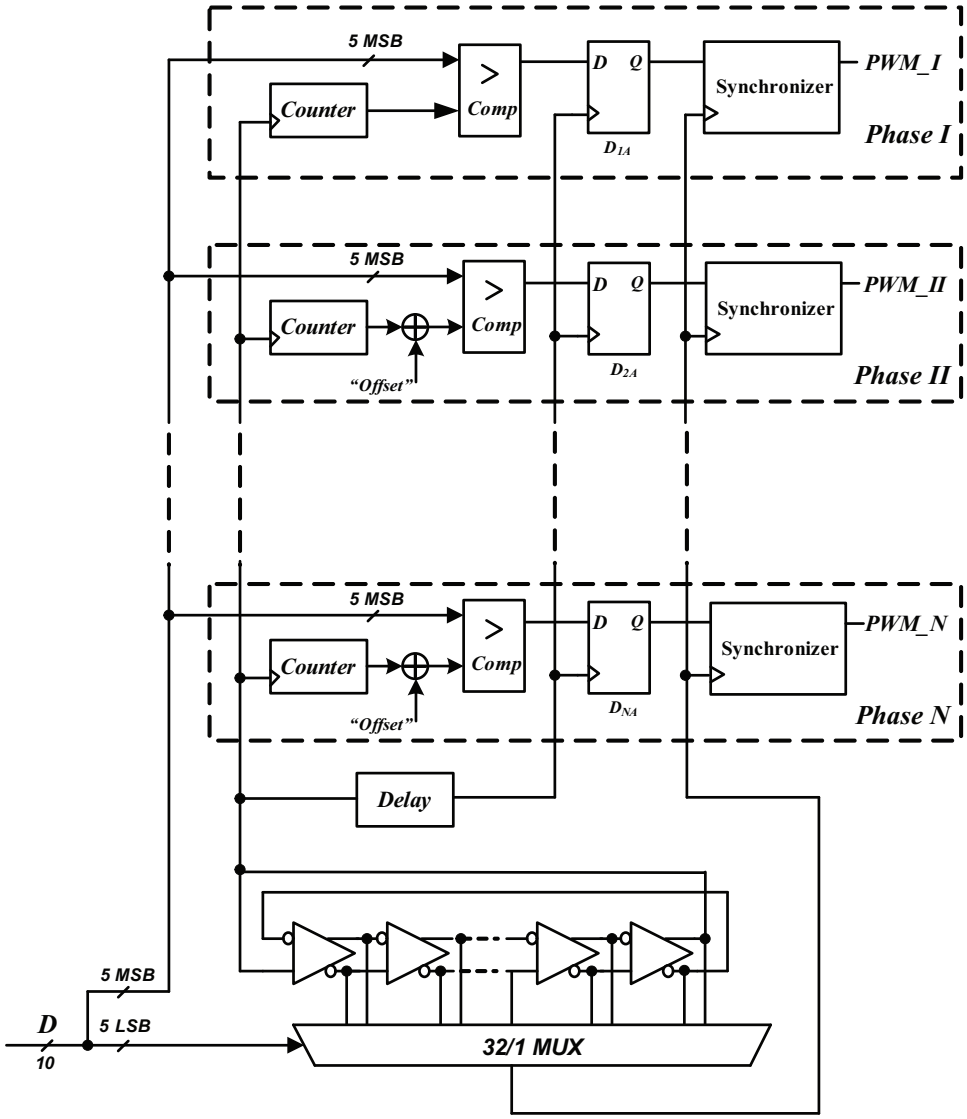


Figure 4.12: Simplified block diagram of a multi-phase DPWM module

Chapter 5

Experimental Results and Conclusions

5.1 Test Platform

To demonstrate the functionality of the prototype multi-mode 4-phase digital controller IC, a test platform was built and set up as shown in Fig. 5.1. A corresponding system block diagram is shown in Fig. 5.2. The test platform consists of three boards. An FPGA board with USB controller is used to connect to a host PC, which runs a software interface that can program on-line the controller IC and monitor certain variables such as duty cycle command, load current, etc. A voltage regulator board containing the designed IC controller and a 4-phase 80 A synchronous buck regulator power train to convert the 12 V input voltage to near 1 V output voltage. These two boards communicate through I^2C/PMBus and MICROWIRE/SPI interfaces. The regulator board could operate stand-lone with the controller IC parameters and programme storing at an external EEPROM. The controller IC parameters and programme are loaded when the system starts up. A third board that serves as a dynamic load that can toggle load current at the output in an ultra-fast manner is used to test the transient response of the VR. The detailed functionalities of these three boards will be discussed in the following sections.

5.1.1 FPGA Board

Fig. 5.3(a) shows the FPGA board used in the test platform. The FPGA board programs the parameters of the IC controller such as PID coefficients, deadtime, voltage reference and so on; and reads back the monitoring variables such as output

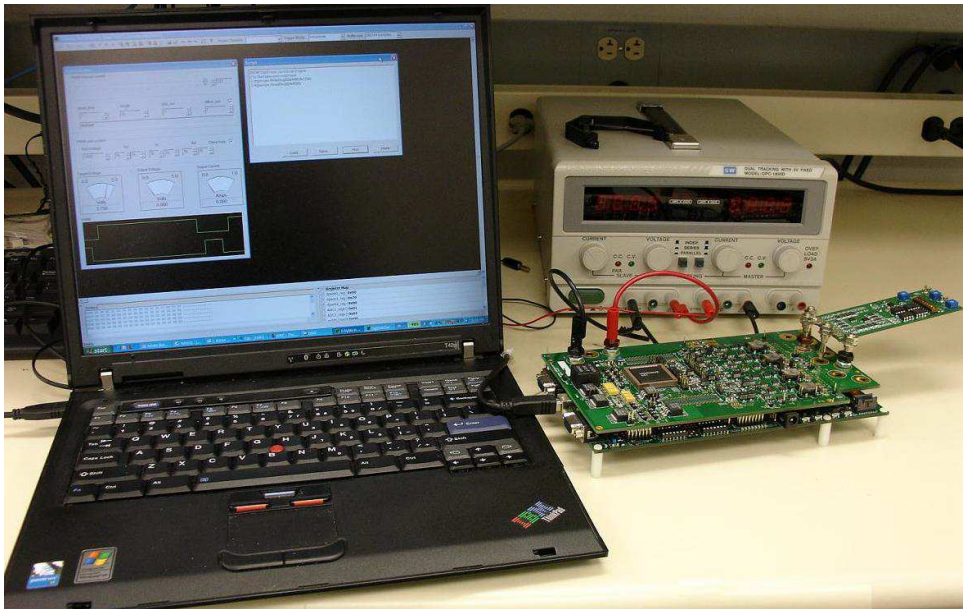


Figure 5.1: Experiment set-up

voltage, load current, duty cycle command, etc. The FPGA board communicates with a host PC through an on-board USB controller. The read and write operation to the IC controller is done through both the I^2C/PMBus and MICROWIRE/SPI interfaces which are integrated into the controller IC. The programming and monitoring data is stored in FPGA board memory. A software GUI with a built-in Java script engine is used to access the program and data memory, which provides PMBus host interface and facilitates the controller IC test process.

5.1.2 Regulator Board

The regulator board is shown in Fig. 5.3(b). The regulator board implements the hardware of the digitally-controlled four-phase voltage regulator with 1 MHz PWM

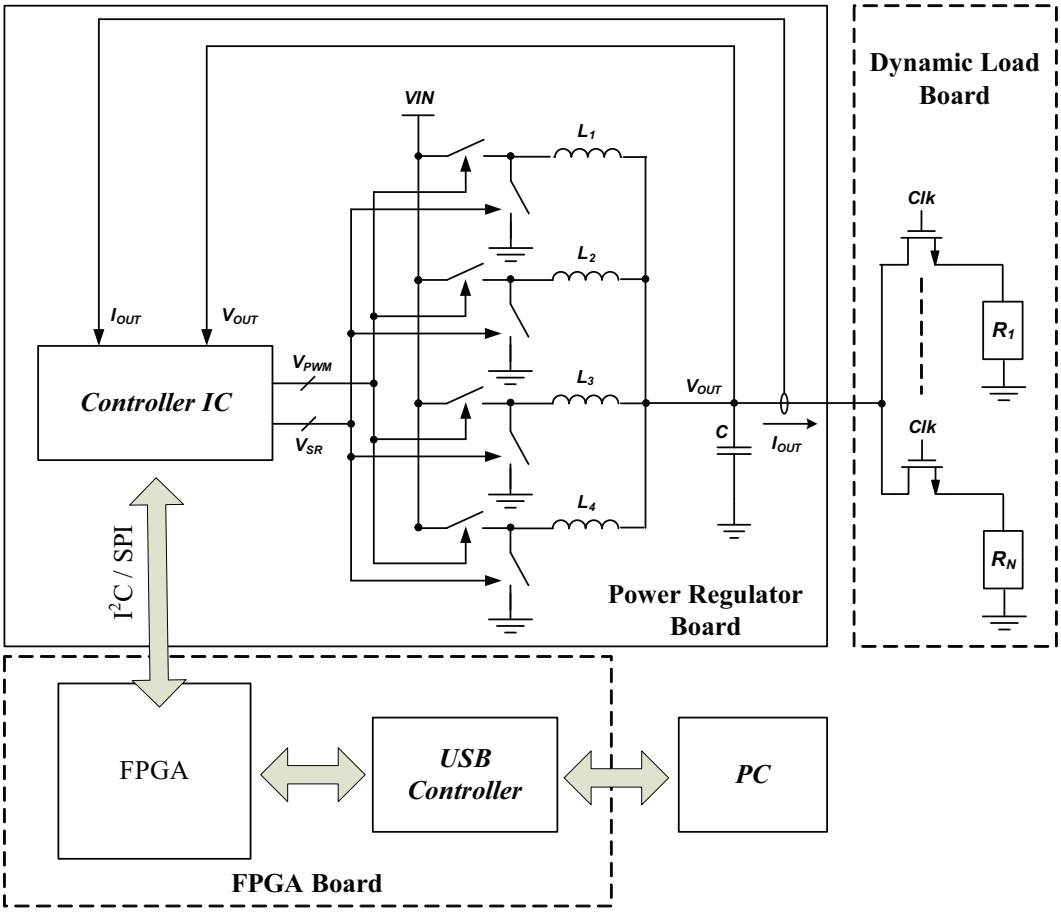
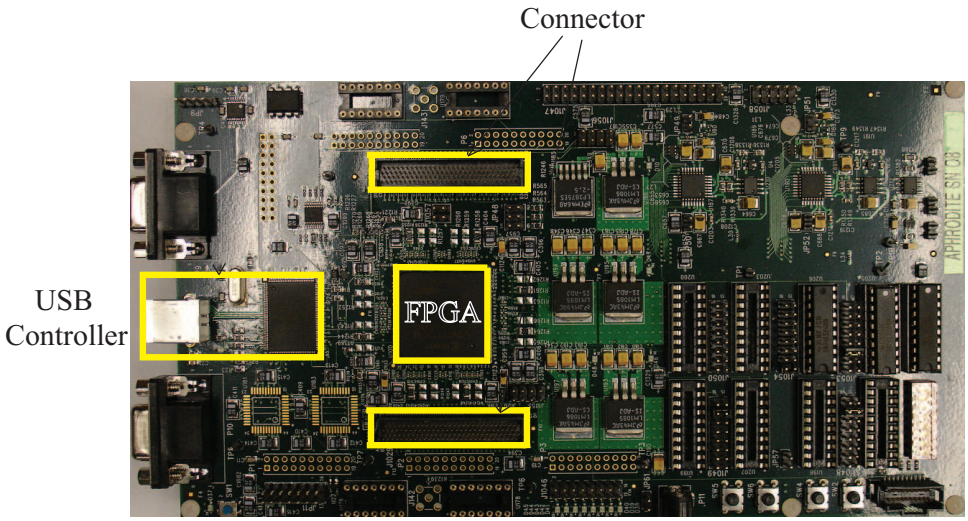
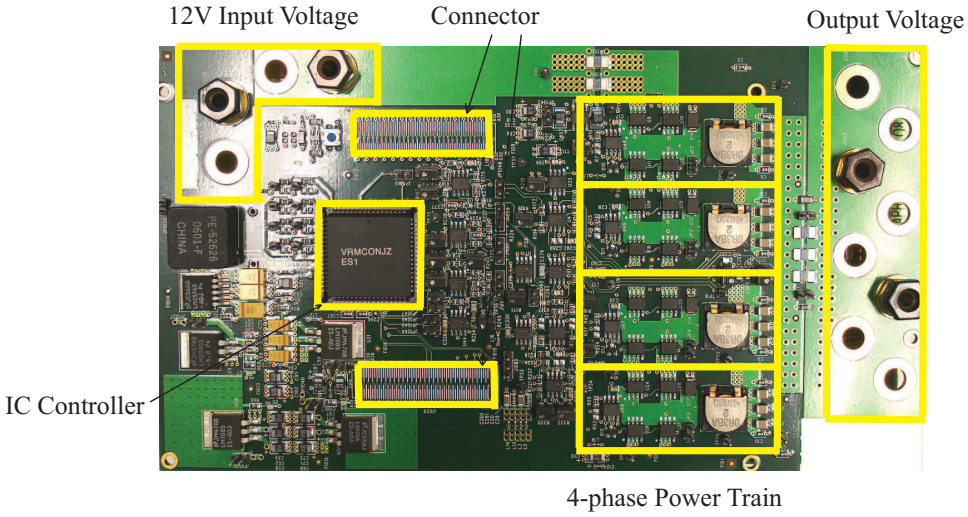


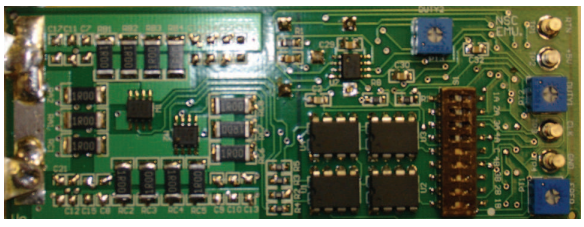
Figure 5.2: Block diagram of the experiment set-up



(a)



(b)



(c)

Figure 5.3: Test platform (a) FPGA board (b) Power regulator board (c) Dynamic load board.

switching frequency. The regulator board contains the power train and the digital controller IC. The voltage regulator board and the FPGA board stack up as shown in Fig. 5.1. For load current sensing, a lossless estimation scheme has been proposed in [14] and a more sophisticated on-line trace resistance calibration method has been proposed in [28]. For the scope of testing in this research, a simple sense resistor in series with the output load is used on the prototype board to measure the load current. Table 5.1 summarizes the parameters of the voltage regulator.

5.1.3 Dynamic load Board

Fig. 5.3(c) shows the dynamic load board used to test the transient response of the controller IC. This load board can toggle the load current at the output of regulator in an ultra-fast manner. A fast switched resistive load is used to generate load current with high slew-rate. The load current level depends on the setting on the board and also depends on the output voltage. An on-board sense resistor is used to measure the load current. This dynamic load board is placed very close to the output capacitors of the regulator board, aiming to minimize the series inductance.

5.2 Experimental Results

The complete multi-mode 4-phase digital-controlled VRM IC controller is implemented in a 0.18 μm CMOS process. The die photo is shown in Fig. 5.4. The

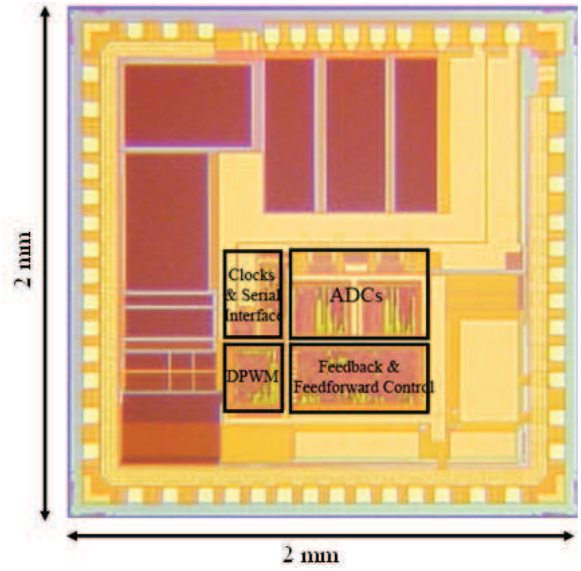


Figure 5.4: Chip micrograph.

active area of the chip is about 0.5 mm^2. Table 5.2 summarizes the application and measured performance of the IC.

Fig. 5.5(a) shows the switching waveform of the converter while running in continuous conduction mode with 20A output current. Signals V_{PWM} and V_{SR} are high side and low side n-channel MOSFET command voltages generated by the IC controller, and V_X is the corresponding switching node waveform. Fig. 5.5(b) and Fig. 5.5(c) show the switching waveform corresponding to discontinuous conduction and pulse skipping modes, respectively, with output current at 4A and 0.5A, respectively. The delay between the rising edges of V_{PWM} and V_X, and the delay between the rising edge of V_{SR} and the falling edge of V_X are caused by the MOSFET driver. These delays are approximate 50ns and 30ns respectively, according to the datasheet of the

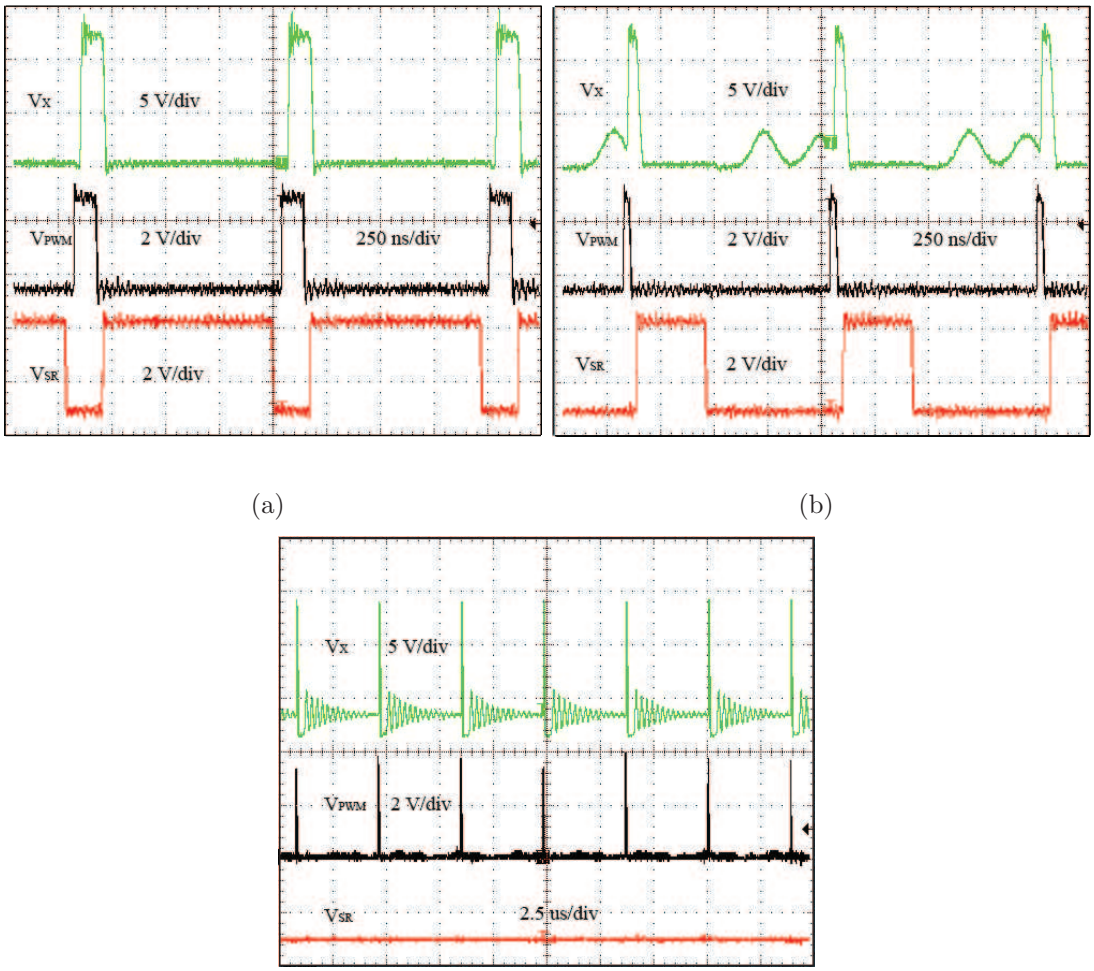


Figure 5.5: Measured switching waveforms when VRM runs in different operation mode (a) Continuous conduction mode (b) Discontinuous conduction mode (c) Pulse skipping mode.

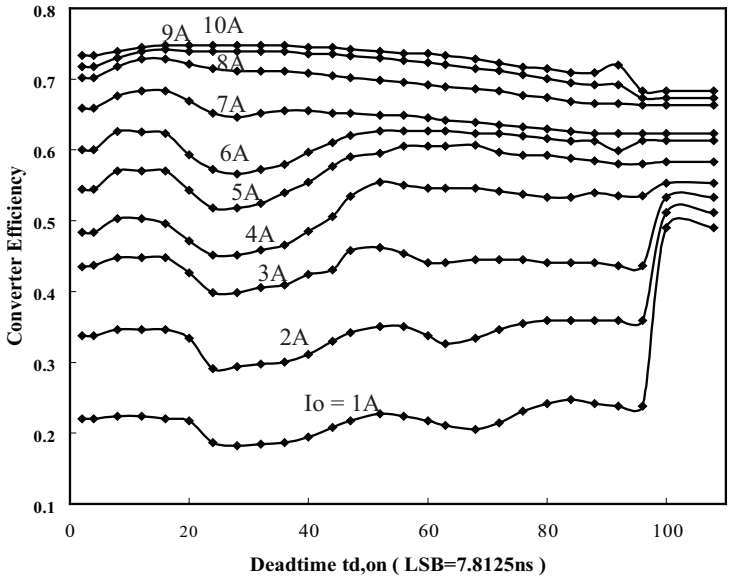


Figure 5.6: Measured converter efficiency as a function of deadtime $t_{d,on}$ parameterized by load current

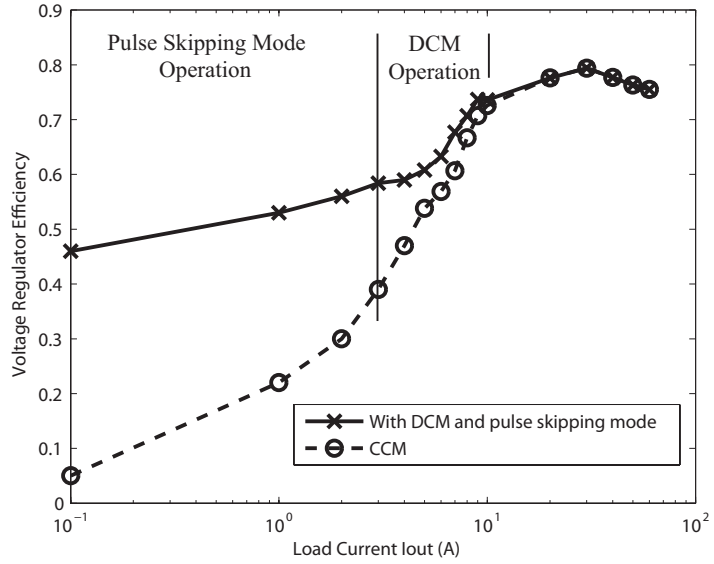


Figure 5.7: Measured converter efficiency as a function of output current with V_{in} = 12V and V_{out} = 1.3V.

MOSFET driver [29].

The measured converter efficiency as a function of deadtime $t_{d,on}$ and parameterized by the load current is shown in Fig. 5.6. This data shows that there is a broad minimum in the curve of power loss versus SR timing parameter $t_{d,on}$, and thus, only moderate precision timing data is required and can be programmed into a look-up table and scheduled as a function of the load current. The efficiency of the converter as a function of load current is plotted in Fig. 5.7. The peak efficiency is moderate (about 80%) due to the particular power train used. However, with DCM and pulse skipping mode operation, the VR efficiency improves substantially in the light load condition compared to the efficiency with only CCM operation.

When the load current is less than 3A, the converter runs in pulse skipping mode with *average* switching period following approximately [14]

$$T_{sw} \approx \frac{V_{in} T_{on}^2 (1 - V_{in}/V_{out})}{2 L I_o V_{in}/V_{out}}. \tag{5.1}$$

For constant frequency operation, the converter loss is dominated by switching loss as discussed in Chapter 3,

$$P_{loss,sw} = \left[\frac{1}{2} C_x V_{in}^2 + C_g V_G^2 \right] f_{sw}, \tag{5.2}$$

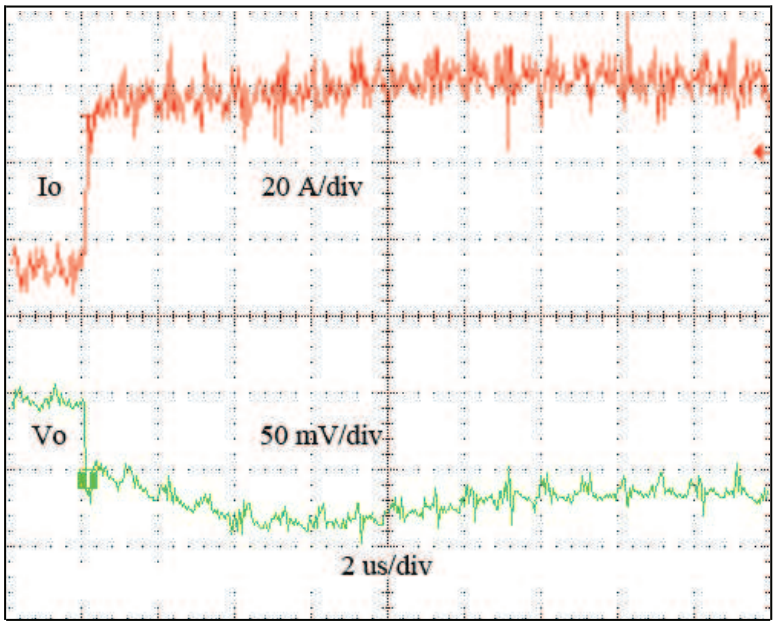
where C_g is the high-side gate capacitance, C_x is the switching node capacitance, and V_G is the gate drive voltage swing. From Equation 5.1 and Equation 5.2, the converter loss is scaled down as the load current reduces with pulse skipping mode operation. Unlike the fixed frequency CCM operation, the converter efficiency is

relatively constant in light load condition. As seen from Fig. 5.7, with pulse skipping mode operation, the VR efficiency is relatively flat as the load current ranging from 0.1A to 3A compared to the case with only CCM operation.

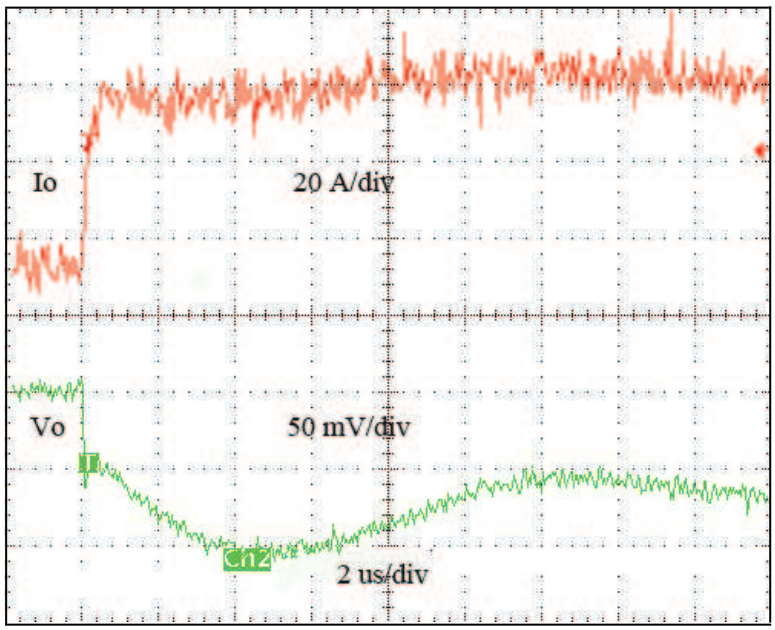
From Equation 5.1, the *average* switching frequency is about 400 kHz when the VR load current equals to 1A. The total VR switching loss is about 0.5W (both gate capacitance and switching node capacitance are estimated from the datasheets of MOSFET [30] and [31]). The total VR conduction loss is about 0.6W (assuming voltage drop of the body diode is about 0.6V). Ignoring the stray inductive switching loss and quiescent power, the efficiency of the VR at 1A load current is estimated at 54%. This is close to the measured result of 52%.

Fig. 5.8(a) and Fig. 5.8(b) show the VR transient responses, with and without load current feedforward, for a 40A loading step between 10A and 50A with load slew rate of 400A/us. It can be seen from Fig. 5.8(a) that with both feedback and feedforward control, the output voltage follows the desired load line well, with less than 20mV overshoot voltage. With only the feedback control, however as shown in Fig. 5.8(b), the overshoot voltage reaches about 50mV which reflects the bandwidth limitation of the feedback controller. The faster transient response has been achieved with feedforward control.

In the unloading transient in Fig. 5.9, an extra overshoot of 40mV can be observed, due to the duty ratio being saturated to zero during the unloading transient, and this is expected given the prototype power train parameters [14]. However, with both

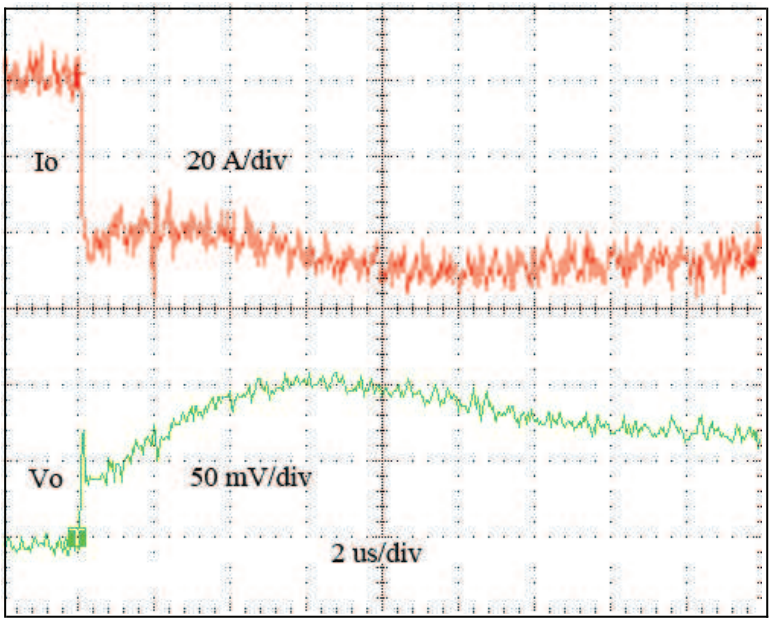


(a)

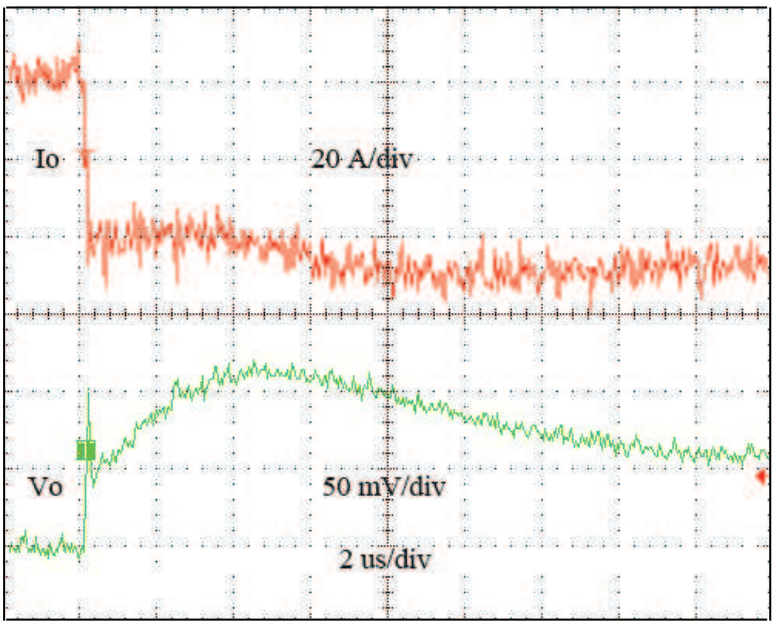


(b)

Figure 5.8: Experimental 40A loading transient with 400A/μs slew rate (a) With load current feedforward and feedback control (b) With feedback control only.



(a)



(b)

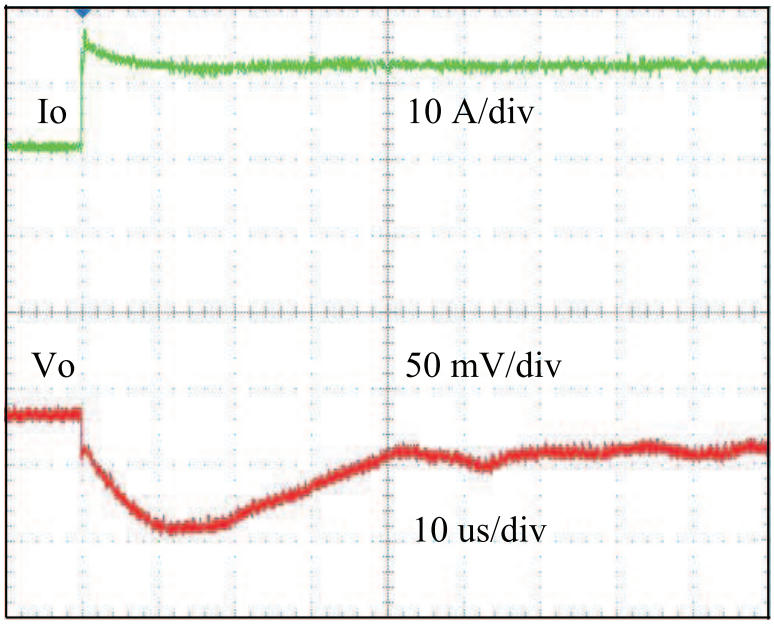
Figure 5.9: Experimental 40A unloading transient with 400A/μs slew rate (a) With load current feedforward and feedback control (b) With feedback control only.

the feedback and feedforward control, slightly less overshoot is achieved than with feedback control alone.

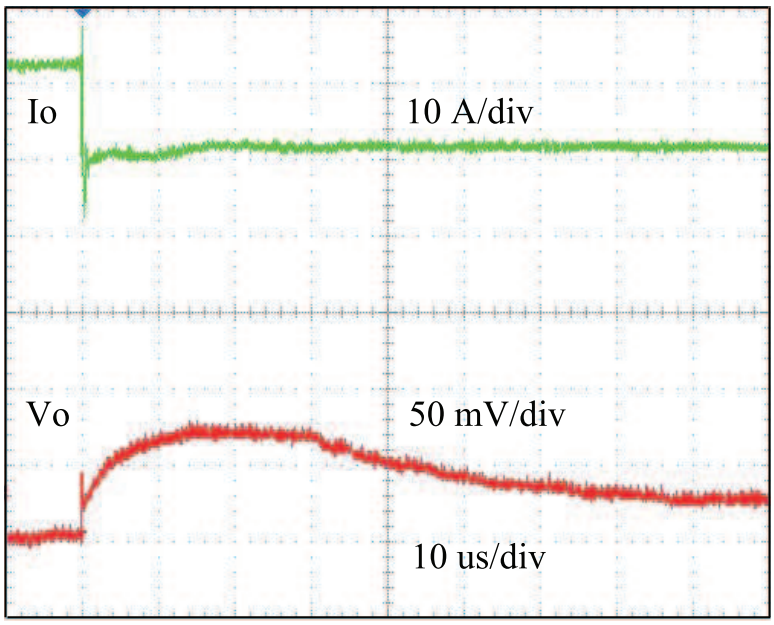
Fig. 5.10 shows the VR transient response, with the VR operating between DCM and CCM with a single integrator, for 12A loading and unloading between 4A and 16A. A relative large output overshoot and long settling time is observed in the loading and unloading transient as the integrator has to slew over a wide range between DCM and CCM. As a comparison, Fig. 5.11 shows the VR transient response with the load-scheduled integrator array enabled. Both the output overshoot voltage and settling time are substantially reduced.

5.3 Conclusions

A CMOS double-edge pulse-width modulator has been demonstrated in this dissertation. The PWM signal is generated by comparing the phase difference between two ring oscillators, which are driven by the input command voltage and a feedback voltage developed in a minor feedback loop that forces the average frequency of the two oscillators to be equal. A multi-state phase frequency detection scheme is developed to keep the frequency of two oscillators always in lock. Both rising and falling edge of the PWM signal are controlled by the instantaneous input voltage, resulting in a low latency relative to that achieved with conventional PWM circuitry. The fast transient response, good re-configurability, good linearity and noise immunity, low power and low cost make it an attractive pulse width modulator candidate for

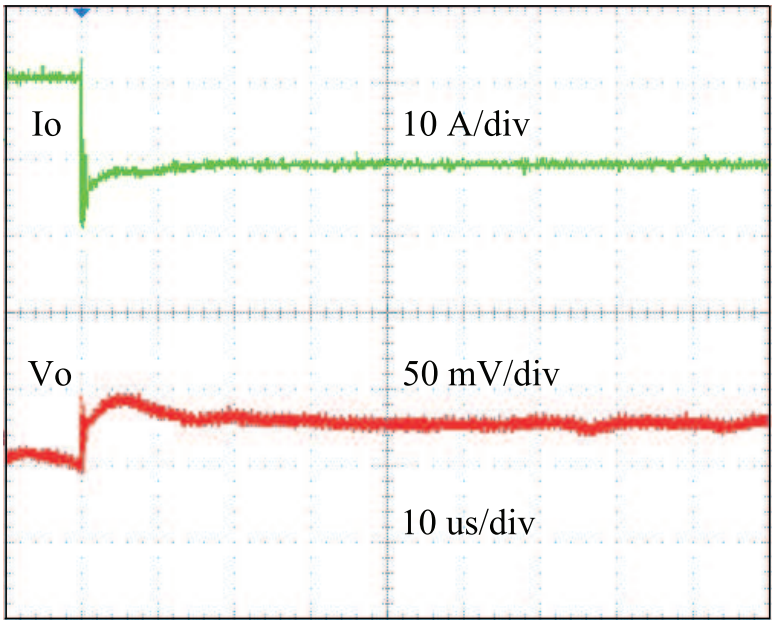


(a)

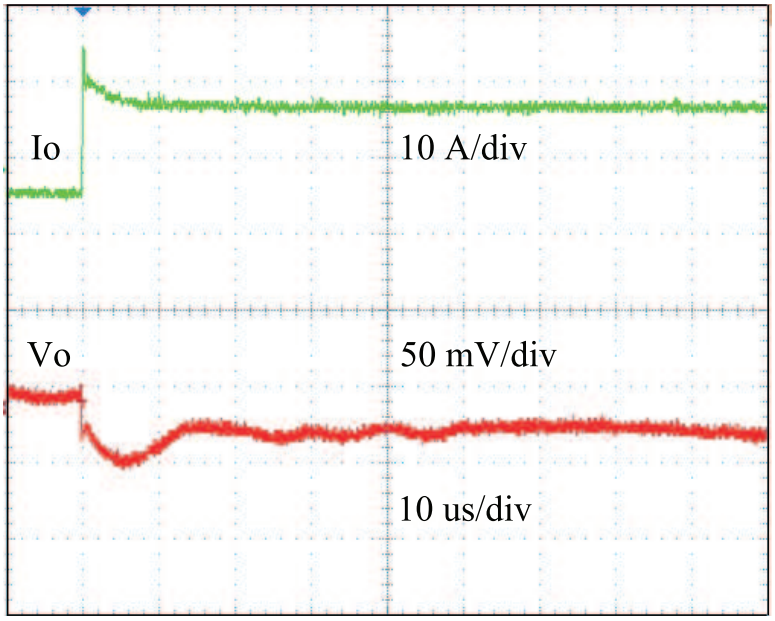


(b)

Figure 5.10: Experimental 12A load transient response with single integrator (a) Unloading transient with VR operating from CCM to DCM (b) Loading transient with VR operating from DCM to CCM.



(a)



(b)

Figure 5.11: Experimental 12A load transient response with load-scheduled integrator array (a) Unloading transient with VR operating from CCM to DCM (b) Loading transient with VR operating from DCM to CCM.

integrated power management ICs.

A digital multi-mode 4-phase IC controller for the voltage regulator application is developed in this dissertation. The multi-mode operation improves the converter efficiency by at least a factor of ten in light load condition. Combined load current feedforward and load-scheduled digital PID control enable fast and glitch-free large-signal transient response. A high resolution digital pulse width modulator and 4mV quantization bin analog to digital converter is implemented in the IC controller to ensure tight DC regulation.

Table 5.1: Prototype 1 MHz buck voltage regulator parameters

	Power Train	
N	number of phases	4
V_{in}	input voltage	12 V
$I_{o,max}$	max. load current	80 A
$r_{h\phi}$	high-side switch on-resistance	20 mΩ
$r_{l\phi}$	low-side switch on-resistance	1/2X 5.5 mΩ
L_ϕ	phase inductors	300 nH @ 15 A
$r_{L\phi}$	inductor ESR & trace resistance	1 mΩ
C_{bulk}	output bulk capacitance	10×100 μF (ceramic)
τ_{Cbulk}	output bulk capacitor ESR time constant	0.6 μs
	Power Train Devices	
$High-side\ MOSFET$	Vishay	Si4892DY
$Low-side\ MOSFET$	Vishay	2X Si4362DY
Inductor	Panasonic	ETQP2H0R3BFA
Bulk capacitor	TDK	C5750X5R0J107K
$MOSFET\ driver$	National Semiconductor	LM27222
	Feedback PID Controller	
V_{ref}	reference voltage	1.3 V
R_{ref}	closed-loop output impedance	1.5 mΩ
f_{sw}	switching frequency	1 MHz
K_P	proportional gain of digital PID controller	32
K_I	integrator gain of digital PID controller	0.25
K_D	derivative gain of digital PID controller	192
t_d	estimated controller delay	$<$ 100 ns
	Feedforward Controller	
R_{FF}	resistor of feedforward high pass filter	5 kΩ
C_{FF}	capacitor of feedforward high pass filter	20 nF

Table 5.2: Chip performance summary.

Technology	0.18-μm CMOS
Number of Phases	4
External LC filter	L_{Phase}=300 nH, C_{total}=1000 μF
Input voltage	12 V
Output voltage range	0.8-1.8 V
Switching frequency	1 MHz
DPWM resolution	120 ps (13 bit resolution)
ADC sampling frequency	4 MHz
PWM command update rate	4 MHz
DC output voltage precision	$\pm$0.2%
Power consumption	3.78 mW
Active chip area	0.5 mm^2

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Appendix A

Design Flow and Simulation

A practical design flow of the digital IC controller for the voltage regulator (VR) application is summarized and illustrated in Fig. A.1. The design specifications define the input and output voltage, steady state and transient voltage regulation band, load current step, slew rate and so on. Based on the design specifications, the power train parameters such as number of phases, inductor and capacitor values, switching frequency, etc, can be derived based on design procedures as described in [32] and [33]. The resolution of the DPWM module can be specified based on the requirement of the output voltage regulation accuracy. The resolution of the ADC has to be less than that of the DPWM to avoid sub-harmonic limit cycling [12]. The sampling speed of ADC and update rate of DPWM module should be identical and be no less than the switching frequency. Faster sampling speed of the ADC and faster update rate of the duty cycle command through the DPWM give faster transient response, but require more hardware and power consumption.

The digital compensator design follows a standard PID template. The traditional techniques described in [33] are used to design an analog compensator with transfer function $H_C(s)$. The digital PID coefficients K_P, K_I and K_D can be derived from bilinear transformation of the analog compensator transfer function $H_C(s)$ with pre-warp. The loop gain and phase margin is analyzed through Bode plot and the PID coefficients can be fine tuned to achieve desired gain and phase margin. A MATLAB Simulink plus Powersim (PSIM) co-simulation is used to perform the system level simulation as shown in Fig. A.2. The controller which includes ADC, digital PID

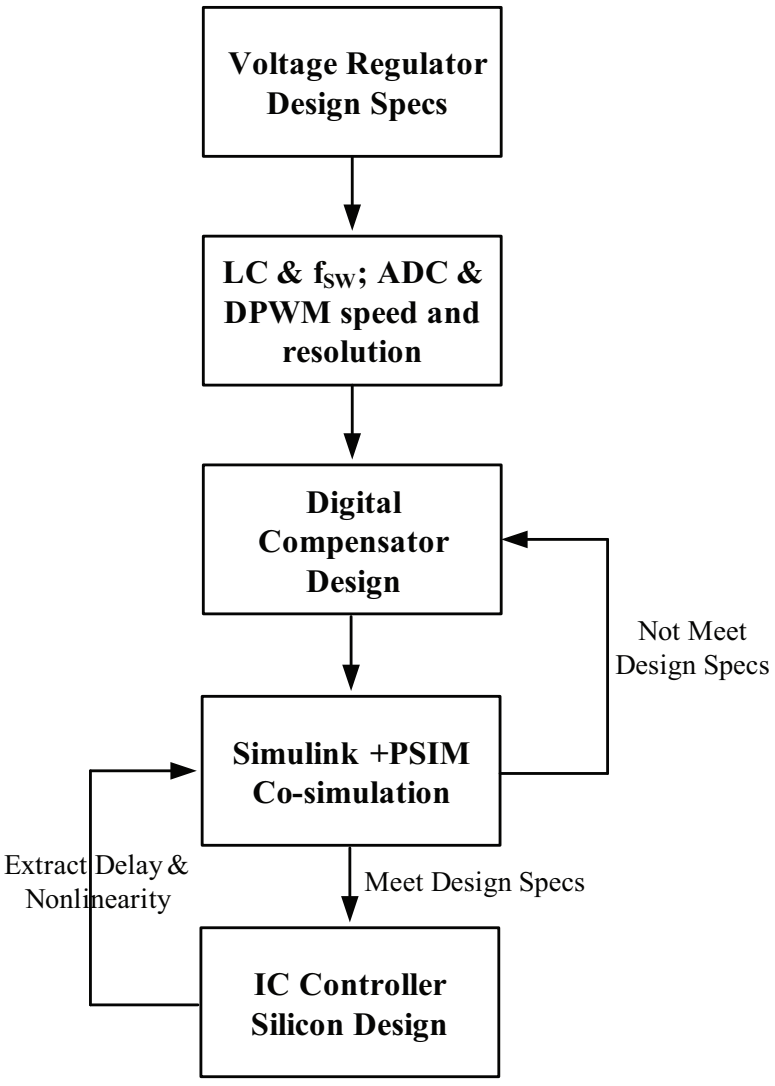


Figure A.1: Design flow of digital IC controller for VR application

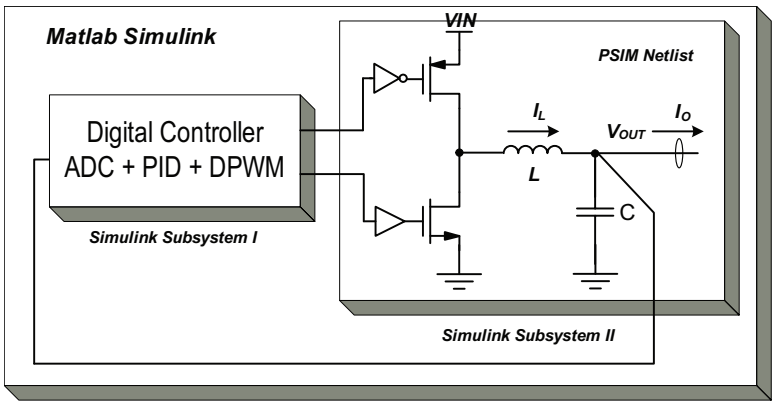


Figure A.2: MATLAB Simulink and PSIM co-simulation platform

compensator, DPWM and load current feedforward control is modeled in MATLAB Simulink. The power train and sensing circuit are modeled in PSIM. Based on the simulation results, PID coefficients can be further fine tuned. The associated delay and nonlinearity of each individual block can be extracted from the Cadence circuit simulation and modeled in Simulink, aiming to match the MATLAB simulation with the Cadence circuit simulation. The whole process can be reiterated if needed to achieve desired steady state and transient response.

Fig. A.3 shows a voltage regulator system modeled in MATLAB Simulink. The ring oscillator based ADC, digital PID compensator, load current feedforward control, dither modulation and DPWM module are modeled in Simulink. The four-phase power train is modeled in PSIM as shown in Fig. A.4, and embedded in Simulink as a separate module called SimCoupler. In PSIM, the output voltage and load current are connected to output link nodes, and these values are passed to Simulink. In return, eight modulation signals, four-phase high side and low side switch control signals, are

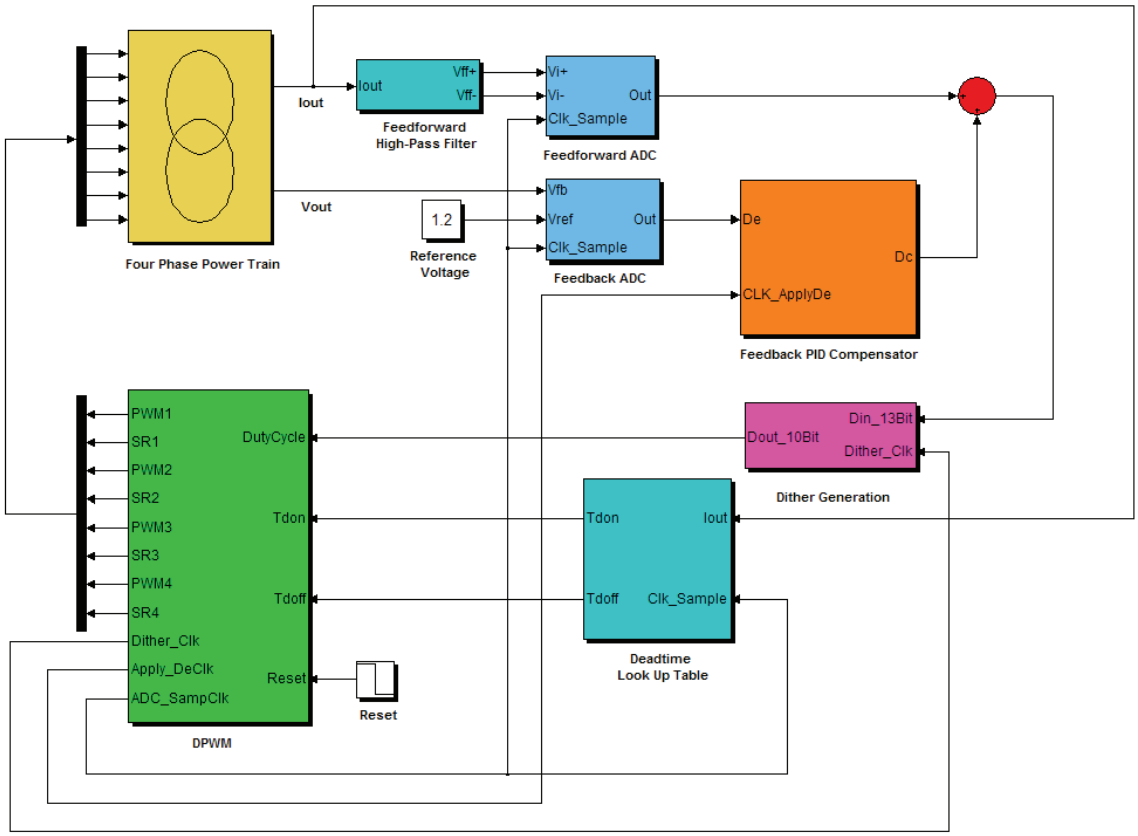


Figure A.3: Voltage regulator modeled in MATLAB Simulink

connected to input link nodes to receive values back from Simulink. In Simulink, the SimCoupler block (four phase power train) represents the PSIM simulation.

Fig. A.5(a) illustrates the model of the ring oscillator based ADC in Simulink and the model of the ring oscillator with single phase output is shown in Fig. A.5(b). The multi-phase outputs are implemented by multi-phase voltage controlled oscillator with different initial phase offset.

The model of digital PID compensation network is shown in Fig. A.6. The delay block in the PID compensator is modeled by a sample and hold stage with the sample

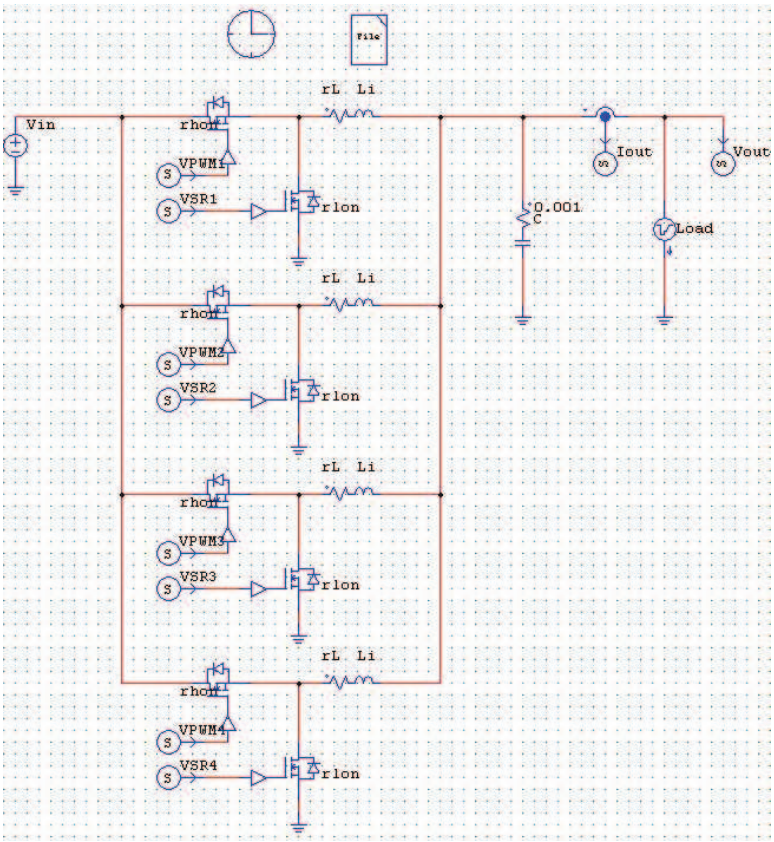
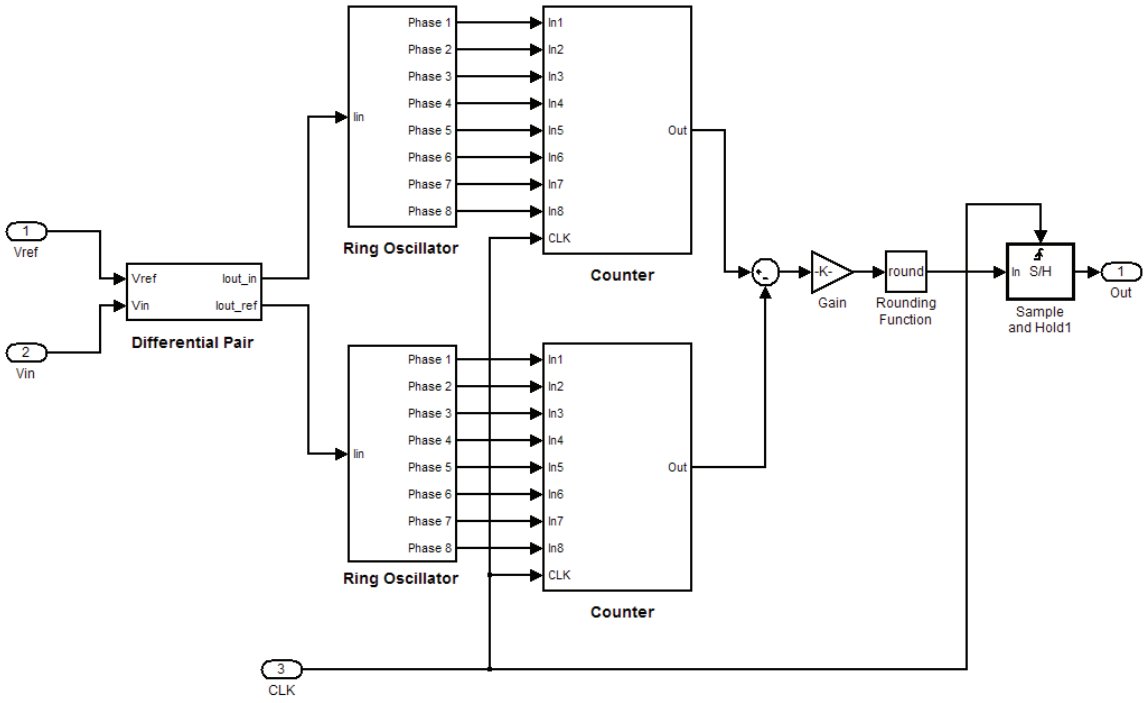
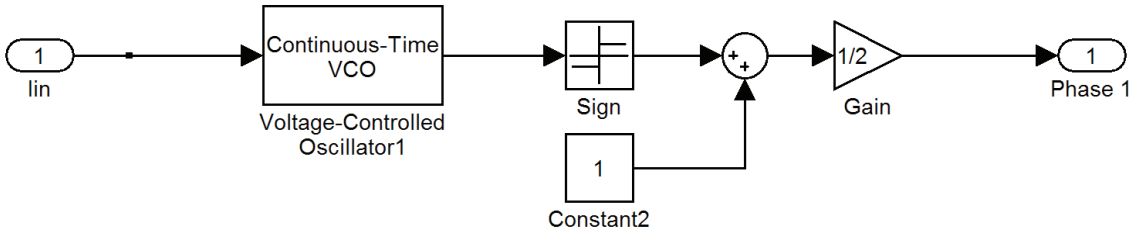


Figure A.4: Schematic of a four-phase power train in PSIM



(a)



(b)

Figure A.5: Ring oscillator based ADC modeled in Simulink (a) Complete ADC model (b) One phase of ring oscillator

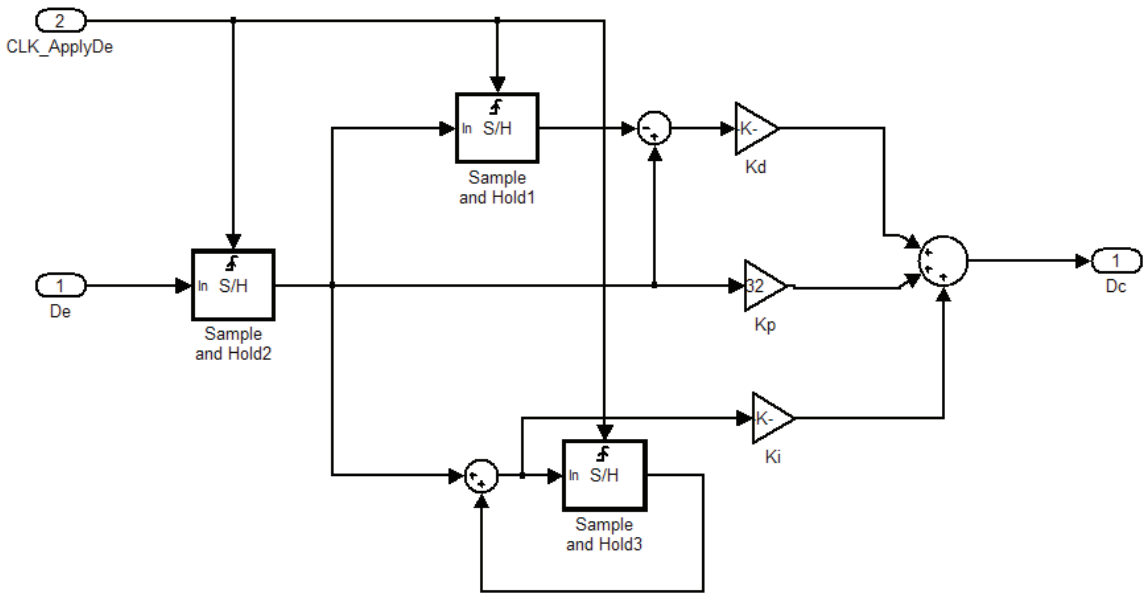


Figure A.6: Model of digital PID compensator in Simulink

clock synchronized with the DPWM update clock.

The 10-bit DPWM model is shown in Fig. A.7. The model includes a 32-phase clock with the frequency of $32f_s$ (f_s is switching frequency)and 32-tap multiplexer which is used to generate 5-LSB fine resolution of the PWM pulse. The 5-MSB coarse resolution is obtained through counter-comparator which is clocked by the $32f_s$ frequency clock. The comparator output and multiplexer output is combined as described in a synchronization scheme that described in Chapter 4 and illustrated in Fig. A.7.

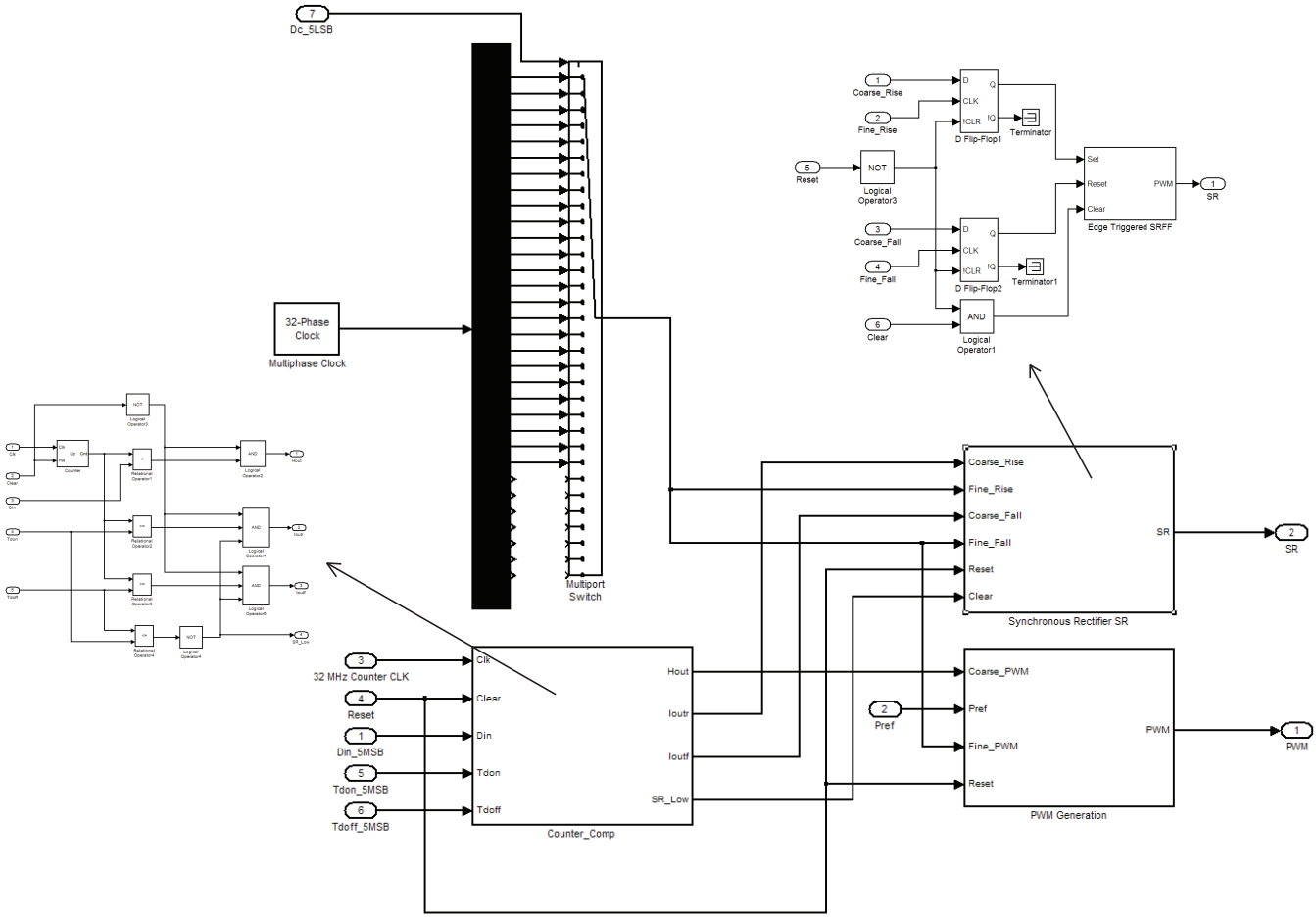


Figure A.7: Model of digital PWM in Simulink